RC 70 COMPUTER

INTERFACE DESIGN MANUAL

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INTERFACE DESIGN MANUAL

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SECTION I
GENERAL INFORMATION

1.1 INTRODUCTION

This interface design manual has been prepared to assist engineers in connecting external equipment to the RC 70 Computer.

Information in this manual is divided into four sections and an appendix. Section I contains general information on the types of interface and a general discussion of each type with the cabling requirements for each type. Section I also describes the electrical characteristics of the interface, cable characteristics, and design aids. Section II describes the processor-controlled interface with the appropriate instructions and timing diagrams for each instruction operation. Section III describes the direct memory access (DMA) interface with a logic description of the operations and timing diagrams. Section IV describes the priority interrupt interface and the clock signals used within the DMA and interrupt options. The appendix provides information and diagrams of the connectors used for the three types of interface, a table defining the terms used in the interface, and logic diagrams of the interface lines.

Throughout this manual, hexadecimal notation is represented by a string of hexadecimal digits enclosed in single quotation marks and preceded by the letter X. For example, the hexadecimal notation for the decimal number 234 is written as X'EA'.

Note

Timing information, signal nomenclature, and systems cabling descriptions included in this manual are not intended for use as maintenance data.

1.2 INTERFACE SYSTEMS

The RC 70 I/O interface provides an efficient, reliable means of communication between the central processor unit (CPU) and multiple peripheral devices. The basic I/O system interface is provided as a standard item. Direct memory access (DMA) and priority interrupt interfaces are available as options. Figure 1-1 illustrates the computer system interface configuration.

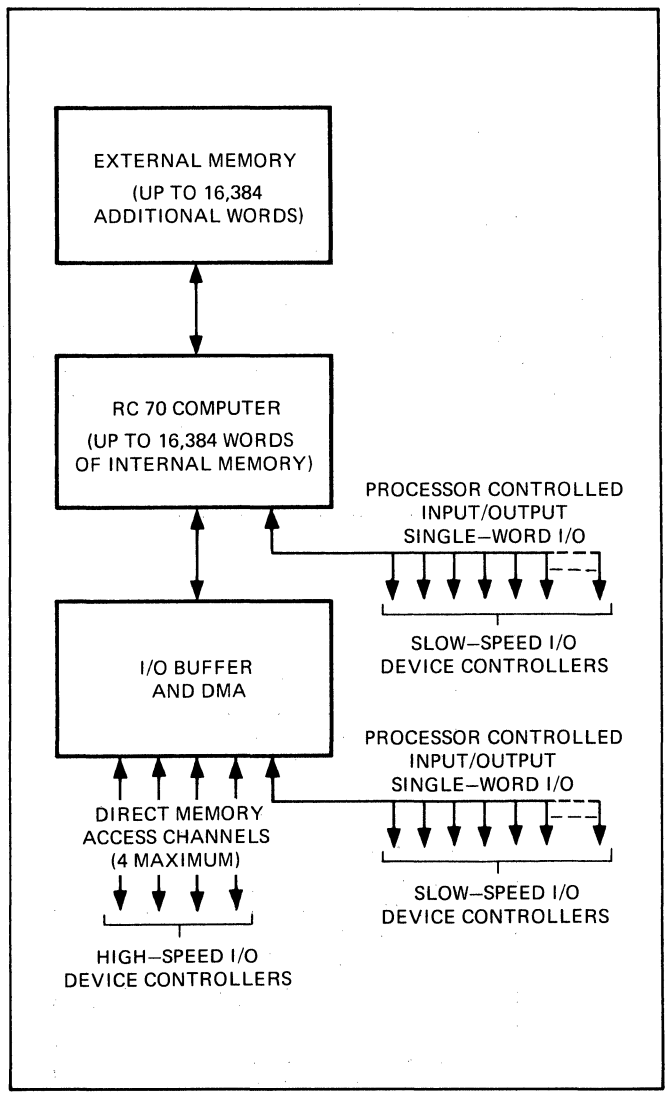


Figure 1-1. RC 70 Computer System, Interface Configuration

1.3 PROCESSOR-CONTROLLED INPUT/OUTPUT

The basic I/O system interface (processor-controlled input/output) allows information interchange to occur between the CPU and peripheral devices under program control. Single-word parallel data transfers are used. Each peripheral device is normally controlled by its own device controller. In special conditions, more than one device may be connected to a single controller. The basic system interface uses eight address lines to provide the capability of addressing a maximum total of 256 device controllers. However, certain addresses are preassigned for various input/output functions such as sense switch testing, interrupt arming and disarming, and DMA control and are not available for device addressing if the particular system contains these functions.

Figure 1-2 is a functional diagram of the basic input/output system. Communication and data transfers between the CPU and external I/O devices may be carried out through an I/O bus to which the external I/O devices are connected in party-line fashion or through a controller chassis.

1.4 DIRECT MEMORY ACCESS (DMA) INTERFACE

The basic input/output system of the computer can be expanded by the addition of optional block-transfer channels that operate through the DMA interface. From one to four channels can be added as options.

The DMA option allows control of high-speed I/O devices without direct program intervention. Two methods of transferring data can be used with the DMA option. One method consists of transferring a single block of words. The second method consists of transferring multiple blocks of words and is referred to as chaining. Parallel data transfers of one word per memory cycle can be accomplished at rates of up to 1.1 million words per second.

Operation of the DMA option is through the controller chassis.

1.5 INTERRUPT INTERFACE

The priority interrupt option provides the computer with the capability to respond quickly to a variety of external stimuli. The interrupt option is especially useful for efficient program control of input/output operations in a real-time environment. The priority logic determines the order of precedence of the external devices.

The priority interrupt option consists of from one to four interrupt cards inserted into the controller chassis. Each interrupt card contains eight levels of priority interrupt.

Operations within the DMA and interrupt options are controlled by the basic computer clock.

1.6 CONTROLLER CHASSIS

As illustrated in figure 1-3, the controller chassis contains 26 slots labeled J1 through J26. Three of

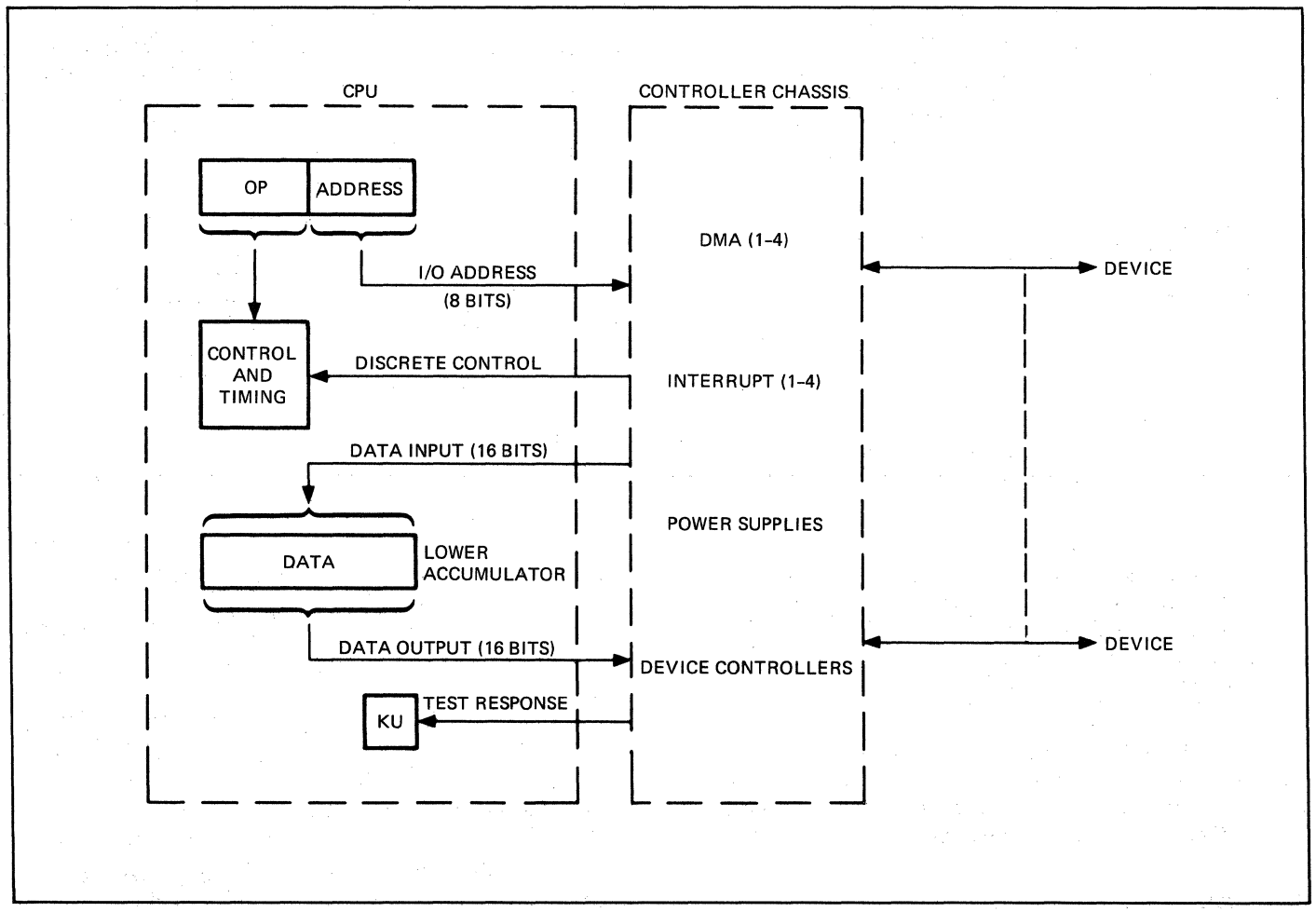


Figure 1-2. Basic Processor-Controlled Input/Output, Functional Diagram

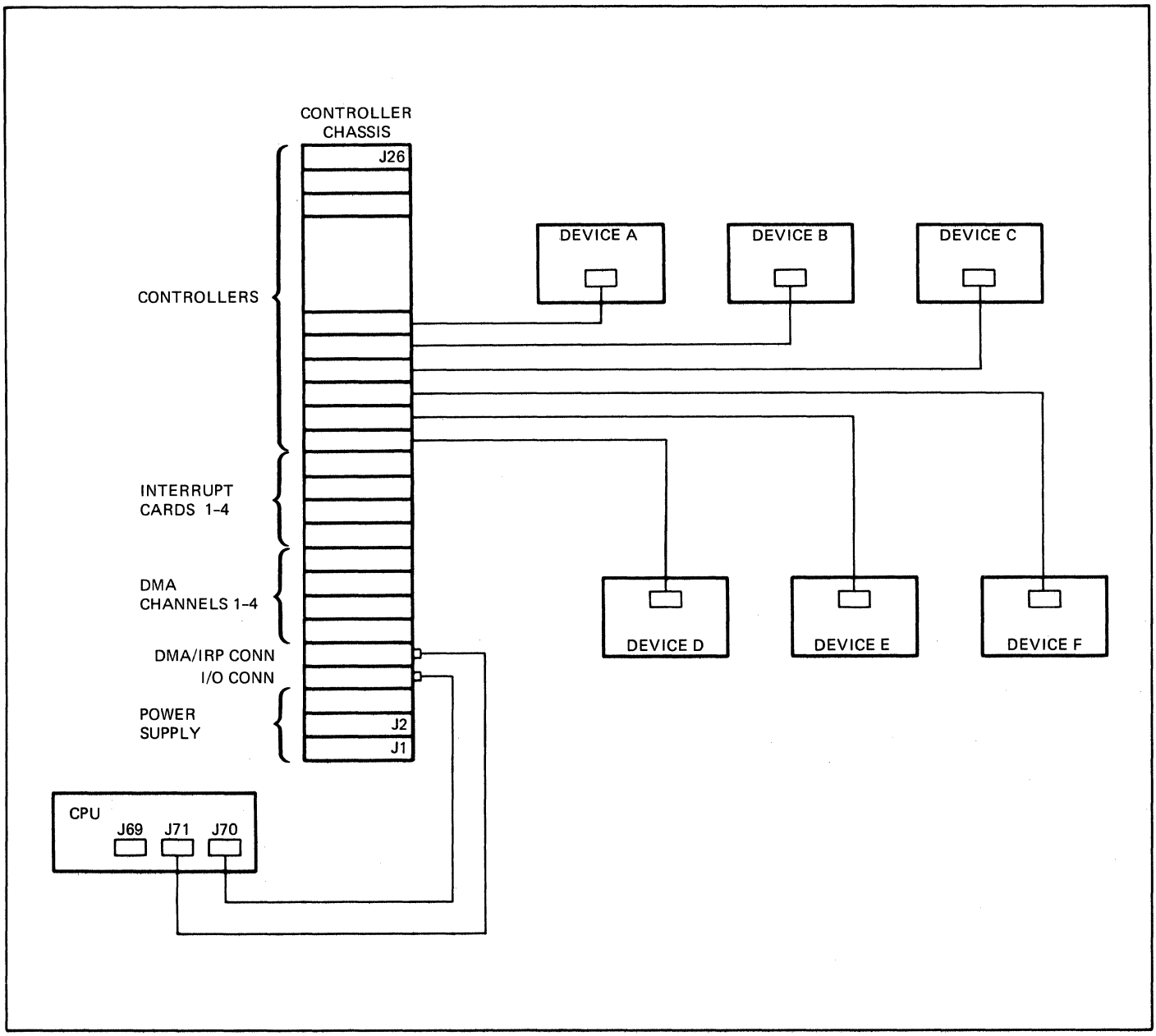


Figure 1-3. Typical Interface Configuration

these slots are normally reserved for a power supply although more than one power supply may be included in a chassis. The remaining slots may be used for DMA cards, interrupt cards, an I/O connector card, a DMA/IRP connector card and controller cards.

The controller chassis may contain up to four DMA cards and up to four interrupt cards. If the particular system does not contain a full complement of DMA and interrupt cards, these slots may be used for controller cards.

Since DMA operations are inhibited during the I/O instructions (Parallel Input, Parallel Output, Set and Sense), a controller card which is normally intended to run under processor-controlled input/output will operate in a controller card slot that is wired for DMA control. However, the opposite will not work.

Either DMA or interrupt cards may be used without the other but if either is used, the DMA/IRP connector card and cable must be used.

1.7 CABLING

Three interface connectors are located on the rear of the CPU. Two are identical 90-pin I/O connectors. The third is a 56-pin DMA/IRP connector.

1.8 I/O CONNECTORS

The I/O connectors provide the signals required for transferring information to and from the CPU under program control. The input/output lines on this connector are as follows:

a. Four control lines: $\overline{\text{OPIP}}$, $\overline{\text{OPOP}}$, $\overline{\text{OSET}}$, $\overline{\text{OSNS}}$

b. Two timing lines: $\overline{\text{ODOIO}}$, $\overline{\text{PRST}}$

c. Eight address lines: $\overline{\text{OAD0}}$ through $\overline{\text{OAD7}}$

d. Sixteen data output lines: $\overline{\text{OUT1}}$ through $\overline{\text{OUT16}}$

e. Sixteen data input lines: $\overline{\text{UIN1}}$ through $\overline{\text{UIN16}}$

f. One discrete status line: $\overline{\text{DSCRU}}$

Pin numbers and signals on this connector are given in table A-2 in the appendix. When the controller chassis is not used, interconnection of the CPU and controllers is accomplished using a single cable connected to an I/O connector on the CPU and to the input connector on the controller. Additional controllers are connected by a cable from the output connector on the first controller to the input connector on the succeeding controller or by a two-cable connector connecting all controllers in the party-line configuration.

When the controller chassis is used, a cable is connected to an I/O connector on the CPU and the other end containing the I/O connector card is inserted into one of the slots in the controller chassis.

1.9 DMA/IRP CONNECTORS

The DMA/IRP connector provides the signals required for transferring information and control to the DMA or priority interrupt option. The input/output lines on this connector are as follows:

a. One interrupt request line: $\overline{\text{XIRP}}$

b. Two DMA control lines: $\overline{\text{CYSTL}}$, $\overline{\text{CYSTW}}$

c. Fifteen DMA address lines: $\overline{\text{U2}}$ through $\overline{\text{U16}}$

d. One line for acknowledging an interrupt request: $\overline{\text{YIDL}}$

e. One line for acknowledging a DMA request: $\overline{\text{UADS}}$

f. Four timing lines for DMA/interrupt operation: OIOIO, XODD, CLK, ORSTB

Pin numbers and signals on this connector are given in table A-1 in the appendix.

Interconnection of the CPU and the controller chassis is accomplished using two cables and two connector cards, one for the I/O connector and one for the DMA/interrupt connector on the CPU. The I/O cable connects to an I/O card and the DMA/interrupt cable connects to a DMA/interrupt connector card.

Signals from the DMA and I/O connector cards are applied to all the connectors in the controller chassis through backplane wiring. Therefore, the DMA, interrupt, and controller cards can be inserted in any connector. The power supply is normally inserted in the first three slots.

If additional controllers are required, an additional chassis may be added to accommodate the extra controllers.

All DMA and interrupt control signals normally used at the controller chassis for these cards are also available for edge connection on the device edge connector pins of the cards.

1.10 ELECTRICAL CHARACTERISTICS

Electrical interface is accomplished using source-terminated, twisted-pair transmission lines. The individual transmission lines are formed into a flat cable to control the amount of cross coupling.

Three separate types of transmission lines are used. The first type consists of those lines in the system connector that are driven from the CPU using a TTL power gate through a 100-ohm series termination resistor. Each device connected to these lines requires a high-impedance (greater than 10,000 ohms) receiver to eliminate excessive reflections. Figure 1-4 illustrates this type of transmission line.

The second type consists of those lines in the system connector that are driven by any one of the external devices. These lines must be driven in the negative direction at the selected device through a 100-ohm series termination resistor by bare collector gates (Signetics N8881, or equivalent). The lines are driven in the positive direction at the CPU by a discrete active pullup circuit through a 100-ohm series termination resistor. The active pullup circuit is disabled by the appropriate CPU command, thereby allowing the lines to be selectively pulled negative by an external device. Figure 1-5 illustrates this type of transmission line.

The third type consists of lines that have a single source and a single destination. These lines are driven at the signal source by a normal TTL gate through a 100-ohm series termination resistor. Figure 1-6 illustrates this type of transmission line.

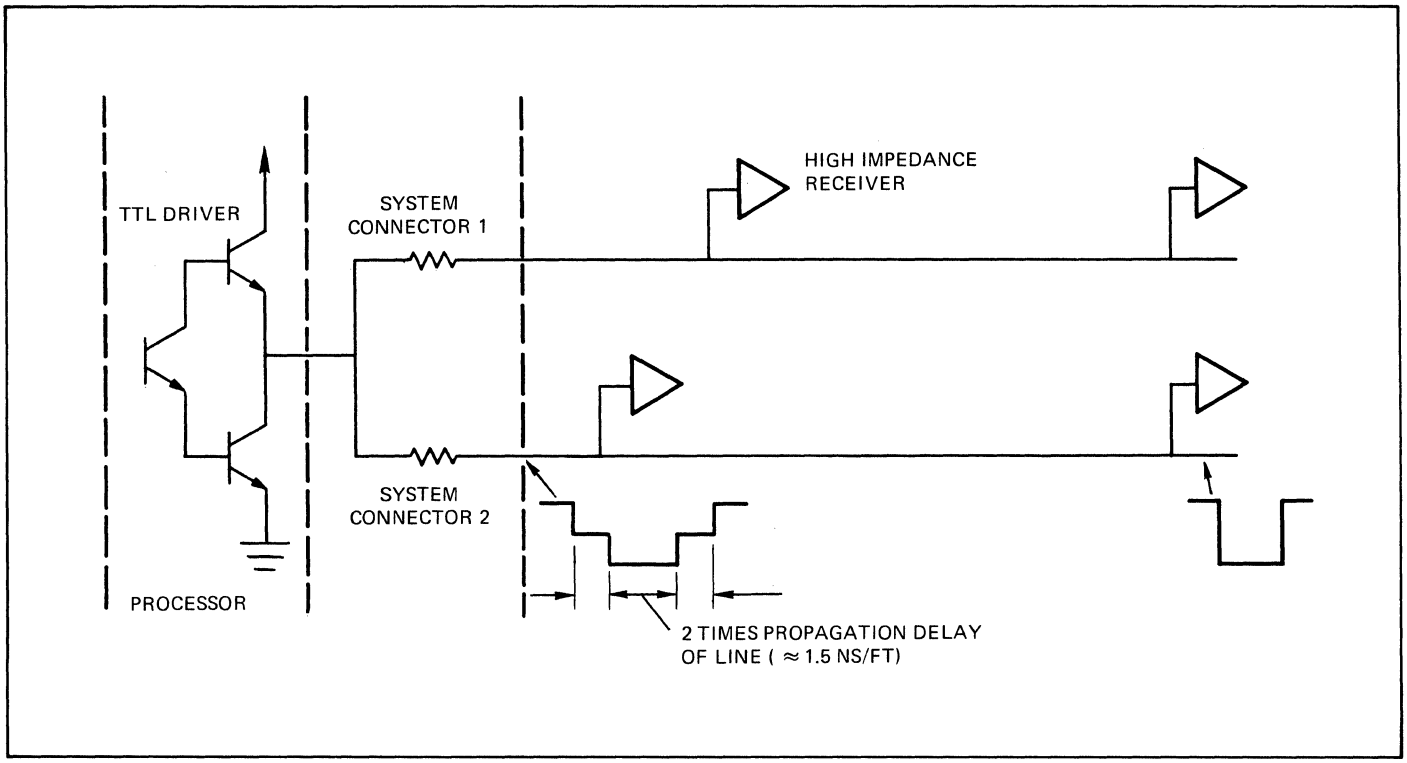


Figure 1-4. Processor-Driven I/O Connector Transmission Lines

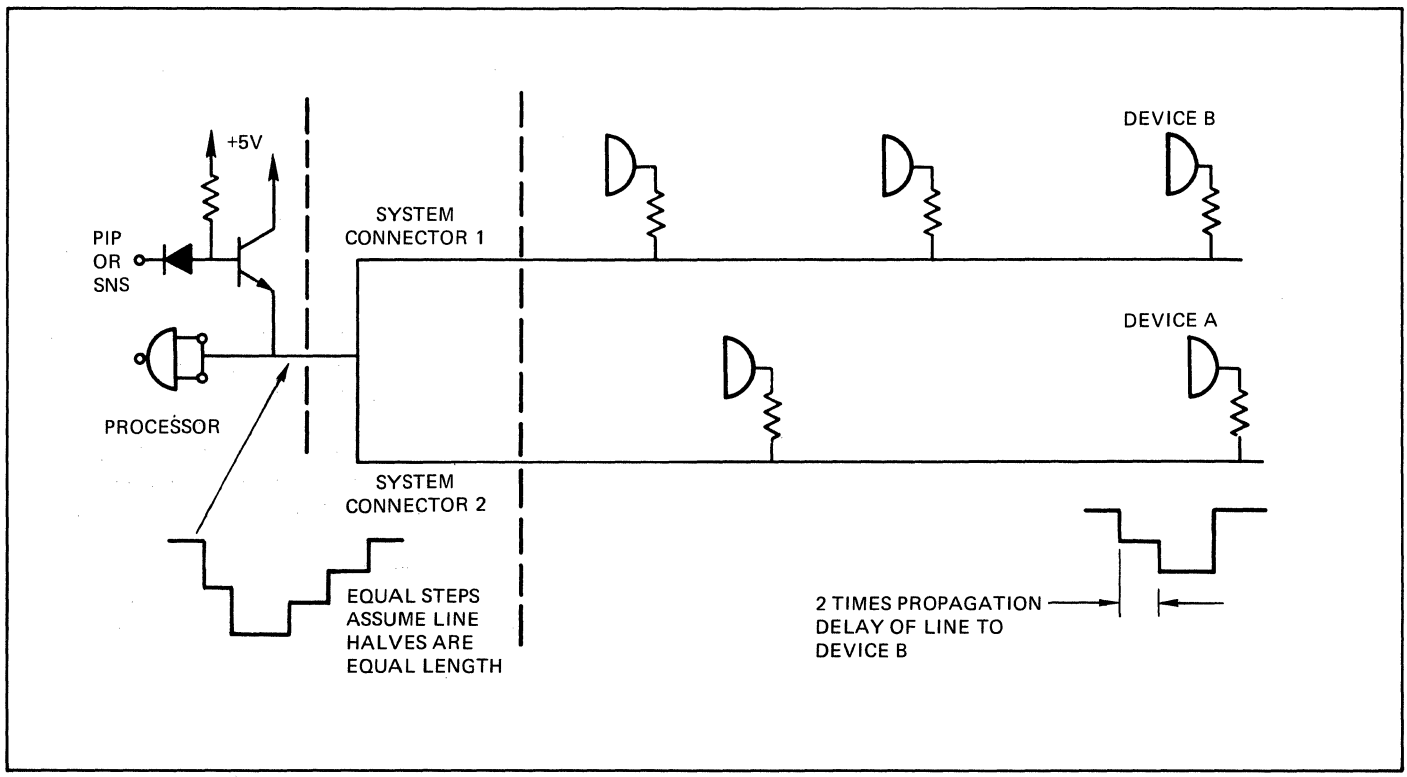


Figure 1-5. External Device Driven I/O Connector Lines

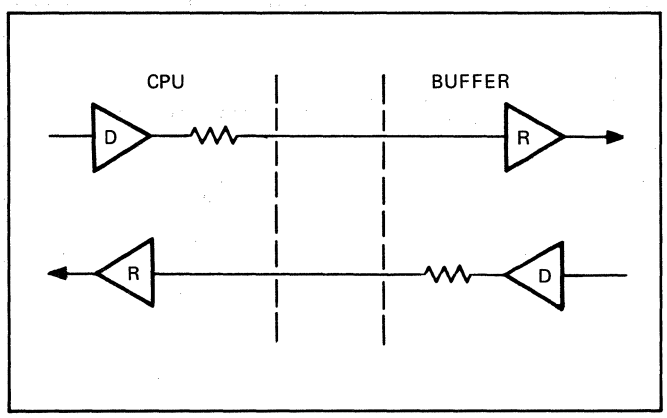


Figure 1-6. DMA/IRP Connector Lines

In the controller chassis, the I/O receivers and drivers are contained on the I/O connector card. The output of these receivers are double inverted with the output to be used on the chassis coming from a power driver in its true form (+5V true). The inputs from the controllers in the chassis must be the same type of bare collector gates but without the 100-ohm series resistor. These signals are inverted.

1.11 CABLE CHARACTERISTICS

All interfaces described in this manual use the same means of interunit cabling. Each cable consists of 64 twisted-pair wires formed into a flat cable. The cable and connectors must be furnished by the user and fabricated into the desired length. Table A-18 in the appendix lists the connector and cable requirements. Tables A-1 through A-17 of the appendix list the connectors and required signals on each pin and the backboard wiring for the applicable connectors.

Cable length restrictions are as follows:

Processor-controlled interface	100 feet maximum
DMA/interrupt interface	50 feet maximum

Signals are inverted through the power driver or receiver and are, therefore, presented on the interface cable in their inverted form. The following conventions are used:

Logical one: +5V

Logical zero: 0V

1.12 DRIVER-RECEIVER CIRCUITS

Signal inversion occurs in both drivers and receivers. If the input to a driver is a logical one (+5V), the line driven goes to logical zero (0V). If a line is at logical zero (0V), the receiver output is at logical one (+5V).

In the controller chassis the output of the receivers are double inverted with the output to be used coming from a power driver in the true form (+5V true).

The allowable load on any controller card in the controller chassis for any signal from the I/O connector power drivers is two loads per card.

Figure 1-7 illustrates the driver/receiver configuration on the I/O connector card in the controller chassis, and figure 1-8 illustrates a power receiver used for party-line controllers and on the I/O connector card in the controller chassis.

1.13 DESIGN AIDS

The following considerations should be observed by the interface design engineer:

a. Power drivers used to drive the I/O bus from the computer require high-impedance loads of over 10,000 ohms. Each power driver is capable of driving up to 16 receivers of the IC TTL type.

b. Power drivers used to drive the DMA/interrupt options are single source and single destination. Each power driver is capable of driving one IC TTL load.

c. Lines driven by the external device require an input impedance of over 10,000 ohms. These lines must be driven in the negative direction at the device through a 100-ohm series termination resistor.

d. Data lines should not be driven by an external device unless a PIP command is on the line, and the appropriate address is on the address lines.

e. The status line should not be driven by an external device unless a SNS command is on the line, and the appropriate address is on the address lines.

f. Data output lines from the computer should not be strobed by a device controller unless a control pulse is on the line, and the appropriate address is on the address lines.

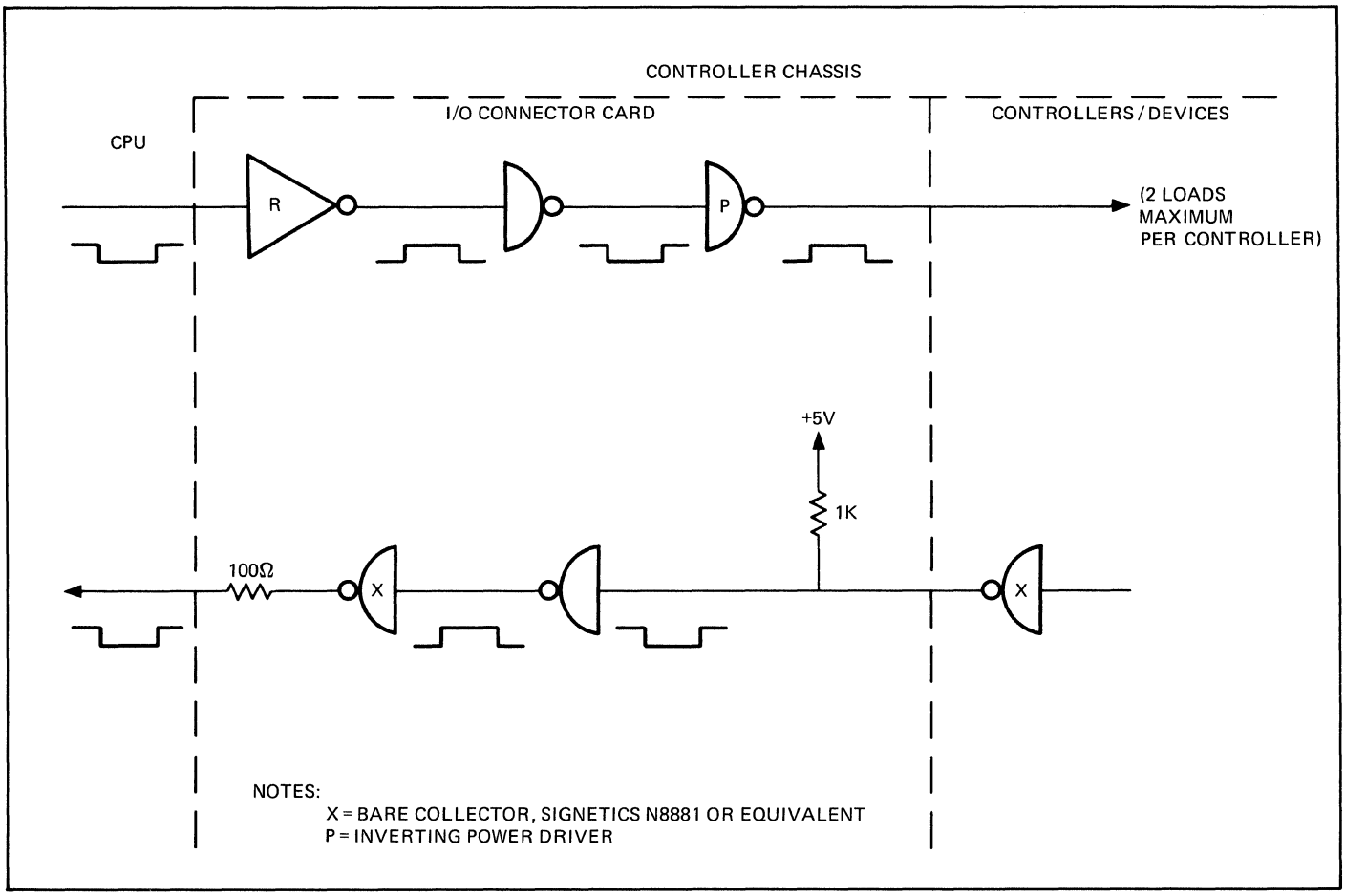


Figure 1-7. Driver/Receiver Configuration in Controller Chassis

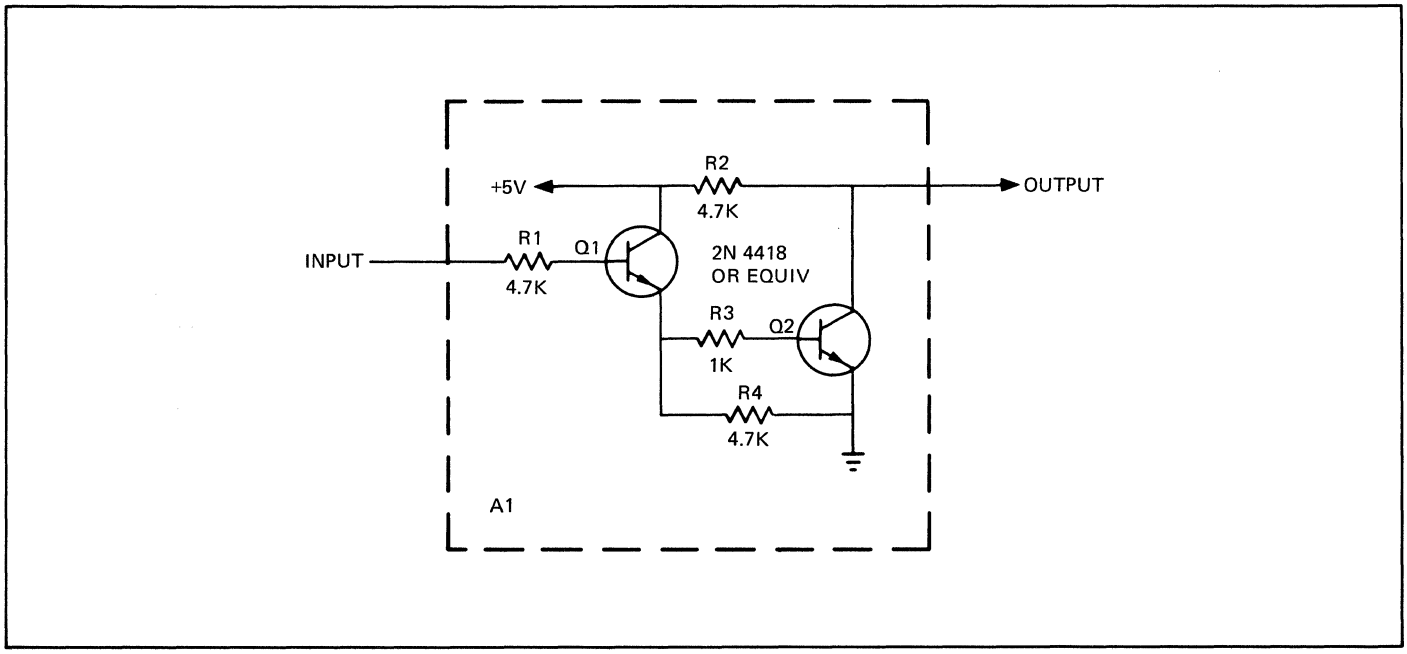


Figure 1-8. Power Receiver, Schematic Diagram

SECTION II
PROCESSOR-CONTROLLED INPUT/OUTPUT INTERFACE

2.1 INTRODUCTION

The basic input/output system permits discrete control and sensing of I/O devices by means of Set and Sense instructions and permits the transfer of single words to and from I/O devices through Parallel Output (POP) and Parallel Input (PIP) instructions.

Communications and data transfers between the computer and external I/O devices are carried out through the I/O bus to which the I/O devices are connected. Each I/O device connected to the bus has a unique address to differentiate it from all other devices on the bus. This address is used by each of the input/output instructions to alert a specific device for operation. Since all devices are connected to the same address lines, only the device whose address matches that specified by the instruction responds. Each command includes the address field in the eight least significant bits of the instruction. The eight least significant bits of the instruction register (I-register) in the CPU are used directly to control the output address line drivers. Therefore, the address lines change with every instruction executed by the CPU.

2.2 INPUT/OUTPUT SIGNALS

Two identical system connectors, J69 and J70, on the rear of the CPU are used to connect the CPU to external equipment. The signal names, pin assignments, and types of signals are listed in table A-2 in the appendix. A signal dictionary is contained in table A-19 of the appendix.

As all signals are inverted through the drivers and receivers, a signal name with a bar over it indicates that the line is at ground level when the signal is true in the CPU. If the signal name has no bar, the line is at +5V when the bar term is true in the CPU.

2.3 INPUT/OUTPUT CONTROL

Peripheral devices connected to the I/O bus are controlled by four input/output instructions: Parallel Input (PIP), Parallel Output (POP), Sense (SNS), and Set (SET).

Each of the four control instructions causes a control pulse to appear on one of the four control lines. These control lines are labeled $\overline{\text{OPIP}}$, $\overline{\text{OPOP}}$, $\overline{\text{OSNS}}$, and $\overline{\text{OSET}}$.

The four instructions are discussed in the following paragraphs. A timing diagram is provided for each instruction. The basic computer clock (CLK) is 430 nanoseconds. A delay clock, used during YOAS time, adds another 200 nanoseconds. Signal YOAS defines the time during which the operand address is selected and the instruction is read.

2.4 SET INSTRUCTION (SET)

The SET instruction is used to transmit a discrete control signal to an I/O device to perform such operations as resetting operating conditions, starting a mechanical operation, rewinding tape, or stopping an operation. Figure 2-1 illustrates the timing for a SET operation. The $\overline{\text{OSET}}$ control pulse is at ground for 860 nanoseconds during execution of the SET instruction.

As indicated on figure 2-1, during X1 time the address of the selected controller appears on address lines $\overline{\text{OAD0}}$ through $\overline{\text{OAD7}}$ from the instruction register. After the end of YOAS time, signal SET goes true, causing signal $\overline{\text{OSET}}$ to go to ground level at the end of the next clock. Signal $\overline{\text{OIOIO}}$ is driven to ground level during the last 1.7 microseconds of all I/O instructions.

2.5 SENSE INSTRUCTION (SNS)

The SNS instruction is used to test the operational status of an I/O device. When the instruction is executed, Unequal indicator KU is set or reset to indicate the status of the condition specified by the instruction.

As indicated on figure 2-2, during X1 time the address of the selected controller appears on address lines $\overline{\text{OAD0}}$ through $\overline{\text{OAD7}}$ from the instruction register. At the end of YOAS time, signal SNS goes true, causing signal $\overline{\text{OSNS}}$ to go to ground level at the end of the next clock for approximately 1.3 microseconds. At the middle of X3 time, discrete status line $\overline{\text{DSCRU}}$ is sampled. If the line is negative, the external device is ready.

2.6 PARALLEL INPUT INSTRUCTION (PIP)

The PIP instruction is used to transfer information from an external device data register into the CPU accumulator. Figure 2-3 illustrates the timing of a PIP operation. During X1 time, the address of the selected controller appears on address lines $\overline{\text{OAD0}}$ through $\overline{\text{OAD7}}$ from the instruction register. At the end of YOAS time, signal

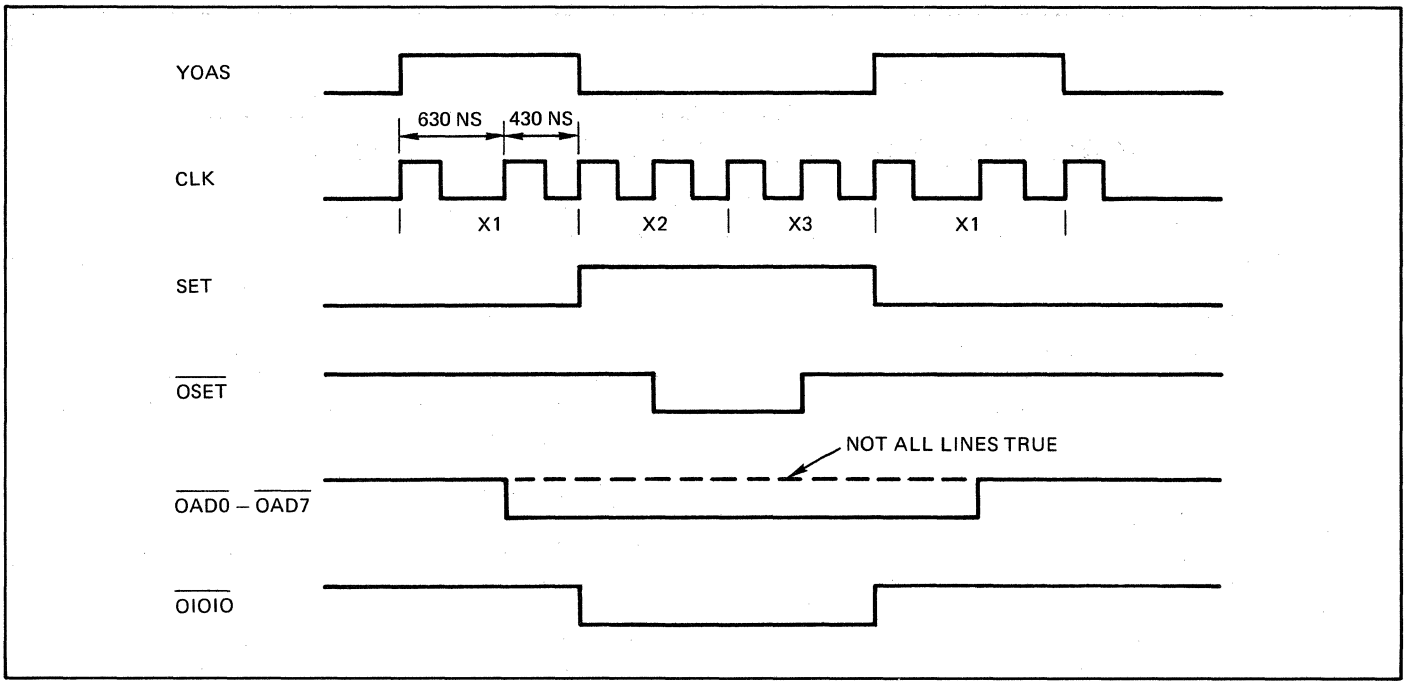


Figure 2-1. SET Operation, Timing Diagram

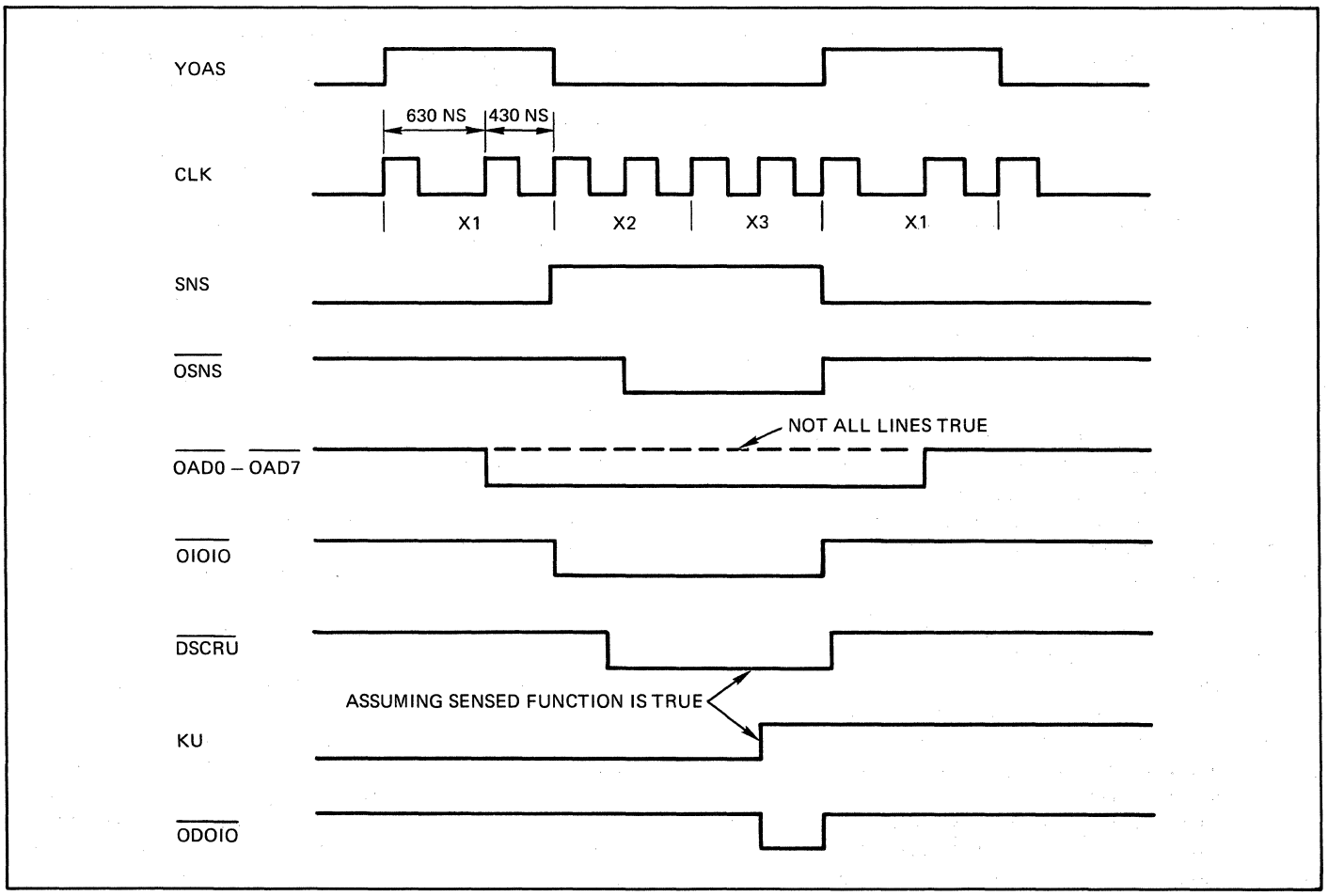


Figure 2-2. Sense Operation, Timing Diagram

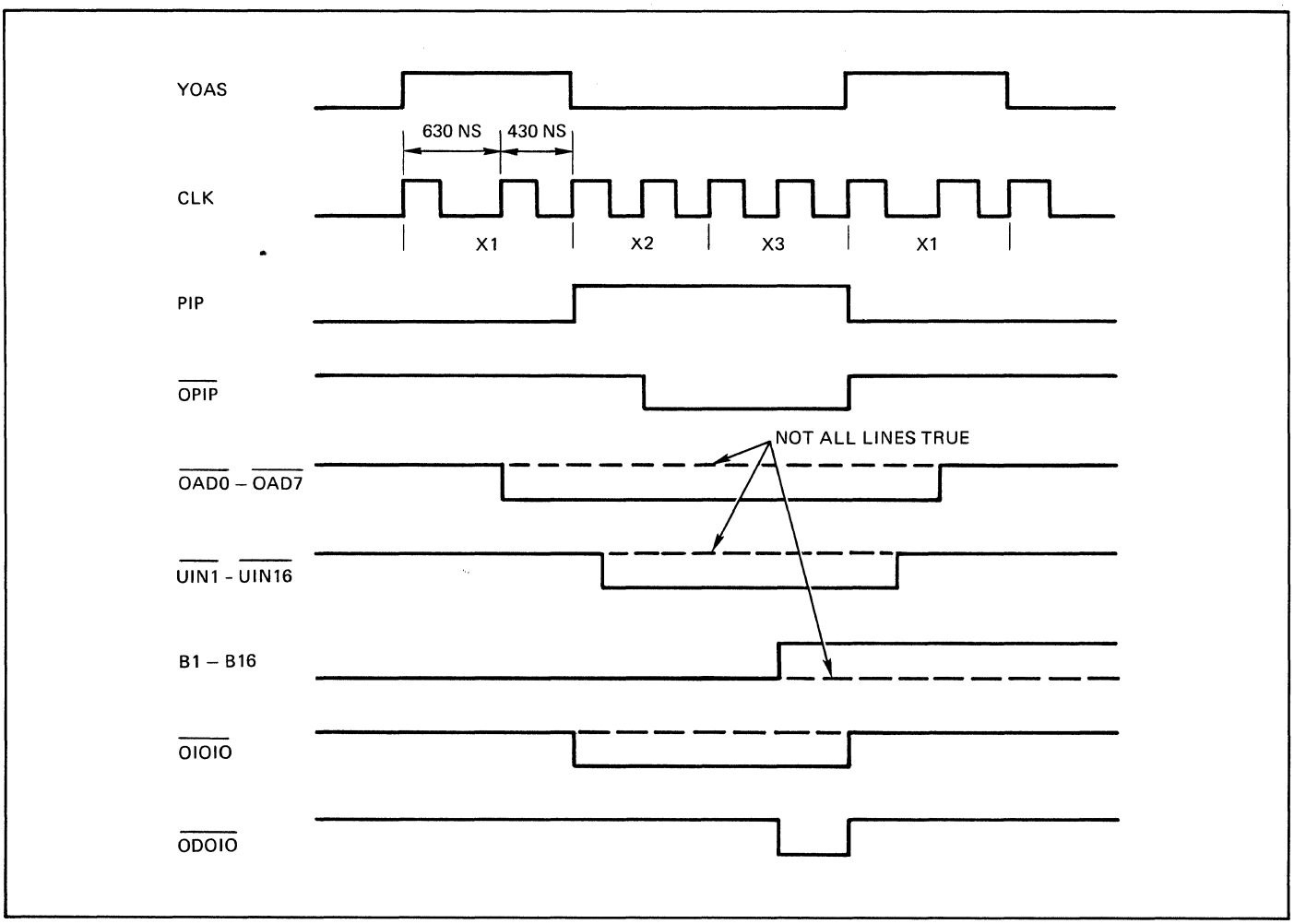


Figure 2-3. Parallel Input Operation, Timing Diagram

PIP goes true, causing signal $\overline{\text{OPIP}}$ to be driven to ground level at the end of the next clock for approximately 1.3 microseconds. At the end of X1 time, the data from the controller should be available on the $\overline{\text{UIN1}}$ through $\overline{\text{UIN16}}$ data lines. At the middle of X3 time, the data on lines $\overline{\text{UIN1}}$ through $\overline{\text{UIN16}}$ are strobed into the accumulator (B1 through B16). During the last 1.7 microseconds of the PIP instruction, signal $\overline{\text{OIOIO}}$ is driven to ground level. When this signal rises, data may be removed from the data lines.

2.7 PARALLEL OUTPUT INSTRUCTION (POP)

The POP instruction is used to transfer information from the accumulator to an external device data register. The information to be transferred must be loaded into the accumulator prior to the POP instruction. Figure 2-4 illustrates the timing for a POP instruction. During X1 time, the address of the selected controller appears on address lines $\overline{\text{OAD0}}$ through $\overline{\text{OAD7}}$ from the instruction register. At the end of YOAS time, signal POP goes true, causing signal $\overline{\text{OPOP}}$ to be driven to ground level at the end of the next clock for approximately 860 nanoseconds. At the end of X1 time, the data from the accumulator is placed on output data lines $\overline{\text{OUT1}}$ through $\overline{\text{OUT16}}$ for transmittal to the address controller. Signal $\overline{\text{OIOIO}}$ is driven to ground level during the last 1.7 microseconds of the POP instruction. This signal indicates the data is on the output data lines to the external device. The data should be strobed into the external device input register by the end of X3 time.

2.8 DATA LINES

Output data is transmitted from the accumulator to the I/O power drivers on a 16-bit data bus. The output drivers invert the applied data and gate the data onto output data lines $\overline{\text{OUT1}}$ through $\overline{\text{OUT16}}$.

When the POP signal goes true at the end of X1 time (see figure 2-4), the data from the accumulator is gated onto the output data lines and remains there until the end of X3 time.

When signal $\overline{\text{OIOIO}}$ is received by the device controller, the data on the output data lines should immediately be

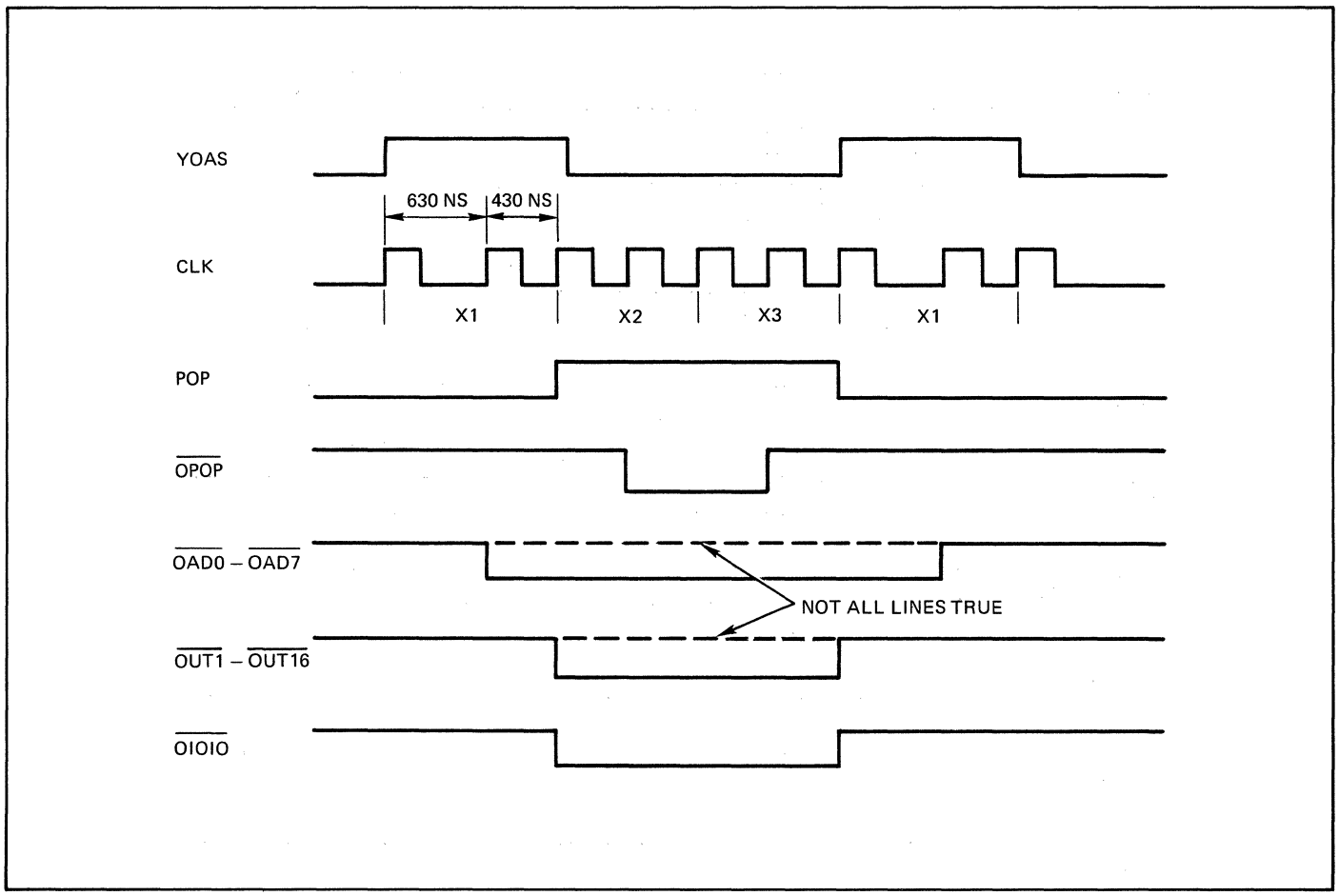


Figure 2-4. Parallel Output Operation, Timing Diagram

strobed into the peripheral input buffer register. At the end of X3 time, signal OIOIO returns to +5V and the data is removed from the output lines.

Any time an instruction being executed causes a store into memory, the data being stored also appears on the output data lines. Therefore, the data lines should not be strobed unless an I/O control signal is present.

Input data from an external device must be placed on input data lines UIN1 through UIN16 in inverted form. At the end of X1 time, signal PIP goes true, indicating the data should be placed on the input data lines.

At the end of X2 time, data on the input data lines is strobed into the accumulator (B1 through B16 on figure 2-3). During the last 1.7 microseconds of the PIP operation, signal OIOIO is driven to ground level, indicating the data may be removed from the input data lines.

2.9 ADDRESS LINES

Eight address lines (OAD0 through OAD7) are used to indicate the address of the I/O device that is to perform the desired operation.

The last eight bits (9 through 16) of the I-register are gated onto the address lines at all times regardless of the instruction being executed. Therefore, the address lines should not be strobed unless one of the I/O control signals is present.

Certain addresses are preassigned and may not be used for addressing I/O devices. Table 3-2 lists the I/O addresses used for DMA addressing. Table 2-1 lists the I/O addresses preassigned for other I/O purposes.

2.10 CONTROL LINES

Each of the four instructions causes a control pulse to be transmitted on one of four control lines. The control lines are labeled OPIP, OPOP, OSNS, and OSET.

The OPIP and OSNS signals are driven to ground for 1.3 microseconds during execution of PIP and SNS instructions, respectively.

The OPOP and OSET signals are driven to ground for 860 nanoseconds during execution of POP and SET instructions, respectively.

Table 2-1. Preassigned I/O Addresses

INSTRUCTION	ADDRESS		FUNCTION
	Hexadecimal	Decimal	
Set	EA	234	Enable priority interrupts
	EE	240	Reset active priority interrupt
Sense	00	0	Test sense switch 8
	01	1	Test sense switch 1
	02	2	Test sense switch 2
	03	3	Test sense switch 3
	04	4	Test sense switch 4
	05	5	Test sense switch 5
	06	6	Test sense switch 6
	07	7	Test sense switch 7
	0A	10	Test memory parity
Parallel Input	01	1	Read console data switches into lower accumulator
Parallel Output	00	0	Display most significant byte of lower accumulator on programmable display indicators
	EA	234	Arm/disarm priority interrupt levels 1 through 16
	EE	240	Arm/disarm priority interrupt levels 17 through 32

These control signals are in inverted form on the interface lines and may be used by the controller for operation control during the applicable operation.

2.11 TIMING AND STATUS LINES

Two timing lines are used to indicate particular time relationships to the controller. Signal $\overline{\text{OIOIO}}$ is driven to ground level during the last 1.7 microseconds of all I/O instructions. Signal $\overline{\text{XPRST}}$ is at ground level during power-off and power turn-on sequences.

Discrete signal line $\overline{\text{DSCRU}}$ provides a ready signal from the controller to the CPU. The signal source is selected by address lines $\overline{\text{OAD0}}$ through $\overline{\text{OAD7}}$ and is sampled at the middle of X3 time of a SNS instruction.

SECTION III
DIRECT MEMORY ACCESS INTERFACE

3.1 INTRODUCTION

The basic input/output system of the computer can be expanded by the addition of optional block-transfer channels that operate through the direct memory access (DMA) feature. From one to four channels can be added as options. Each channel can be set up by the program to transfer single blocks or multiple blocks of 16-bit words directly between memory and an I/O device. After setting up the channel, the program initiates the transfer, and from then on the channel controls the transfer operation without further program intervention. Each time the I/O device is ready to transmit or receive data, the channel interrupts the computer after the current memory cycle and uses the next memory cycle to transfer one word of data. The channel keeps stealing memory cycles until the entire block of words has been transferred or until the program stops the transfer. More than one channel can be set up to operate at the same time, and, if this is done, the channels operate on a priority basis with channel 1 having the highest priority, and channel 4, the lowest.

3.2 CONTROLLER CHASSIS

A controller chassis is added to the central processor when the DMA feature is used. All input/output signals between the processor and the controllers pass through the backplane wiring of the chassis. Figure 3-1 is a simplified logic diagram of the DMA interface. Four DMA cards can be inserted into the controller chassis. All connections to the cards are made through backplane wiring. Output and input to the DMA channels to and from the device controllers is made through the backplane wiring.

Connection to the DMA channels may also be made to the card edge connectors if the device controller is located external to the controller chassis. Signals on the device board edge appear in their inverted forms as $\overline{\text{CAD0}}$ through $\overline{\text{CAD7}}$, $\overline{\text{BUFIN}}$, $\overline{\text{BUFOT}}$, $\overline{\text{BUFSN}}$, $\overline{\text{CWRT}}$, and $\overline{\text{DSCRC}}$.

The pin assignments and signals on the pins for the DMA backplane wiring are listed in appendix A, tables A-4 through A-7.

3.3 BLOCK-TRANSFER CONTROL WORDS

Each DMA channel requires two control words for a block-transfer operation: one word specifying the starting address of the block to be transferred and one word specifying the number of words in the block. These words must be loaded by the program into memory locations reserved for communication between the channels and the processor before a block transfer is initiated. The memory locations reserved for use by each DMA channel are listed in table 3-1.

3.4 SINGLE-BLOCK TRANSFER

The sequence of operations for a single-block transfer through a DMA channel is as follows:

a. The program loads the block starting address and word count into the memory locations assigned to the channel being used.

b. The program loads the I/O device controller address into the lower accumulator, and then executes a Parallel Output instruction with an effective address of X'E2' (channel 1), X'E4' (channel 2), X'E6' (channel 3), or X'E8' (channel 4) to transfer the address to the appropriate channel.

c. The program executes a Set instruction with an effective address of X'E2' (channel 1), X'E4' (channel 2), X'E6' (channel 3), or X'E8' (channel 4) to initiate the transfer.

d. The DMA channel makes two memory accesses to fetch the control words and stores them in two control registers in the channel.

e. As soon as the I/O device is ready to transmit or receive data, the channel stops normal computer operation for one cycle and makes the transfer. After the transfer, the contents of the starting address register in the channel are increased by one, and the word count register is decreased by one in readiness for the next word transfer. When the device is ready again, another cycle of operation takes place. This sequence continues until the contents of the word count register equal zero, or until the program executes a reset DMA Set instruction with the appropriate channel address (X'E2', X'E4', X'E6', or X'E8'). The program can also determine at any time the number of words that have been transferred by executing a Parallel Input instruction to transfer the contents of the channel word count register into the accumulator.

f. Transfer completion can be sensed. This same signal is available to initiate an interrupt.

Table 3-2 contains a list of standard preassigned DMA I/O instruction addresses.

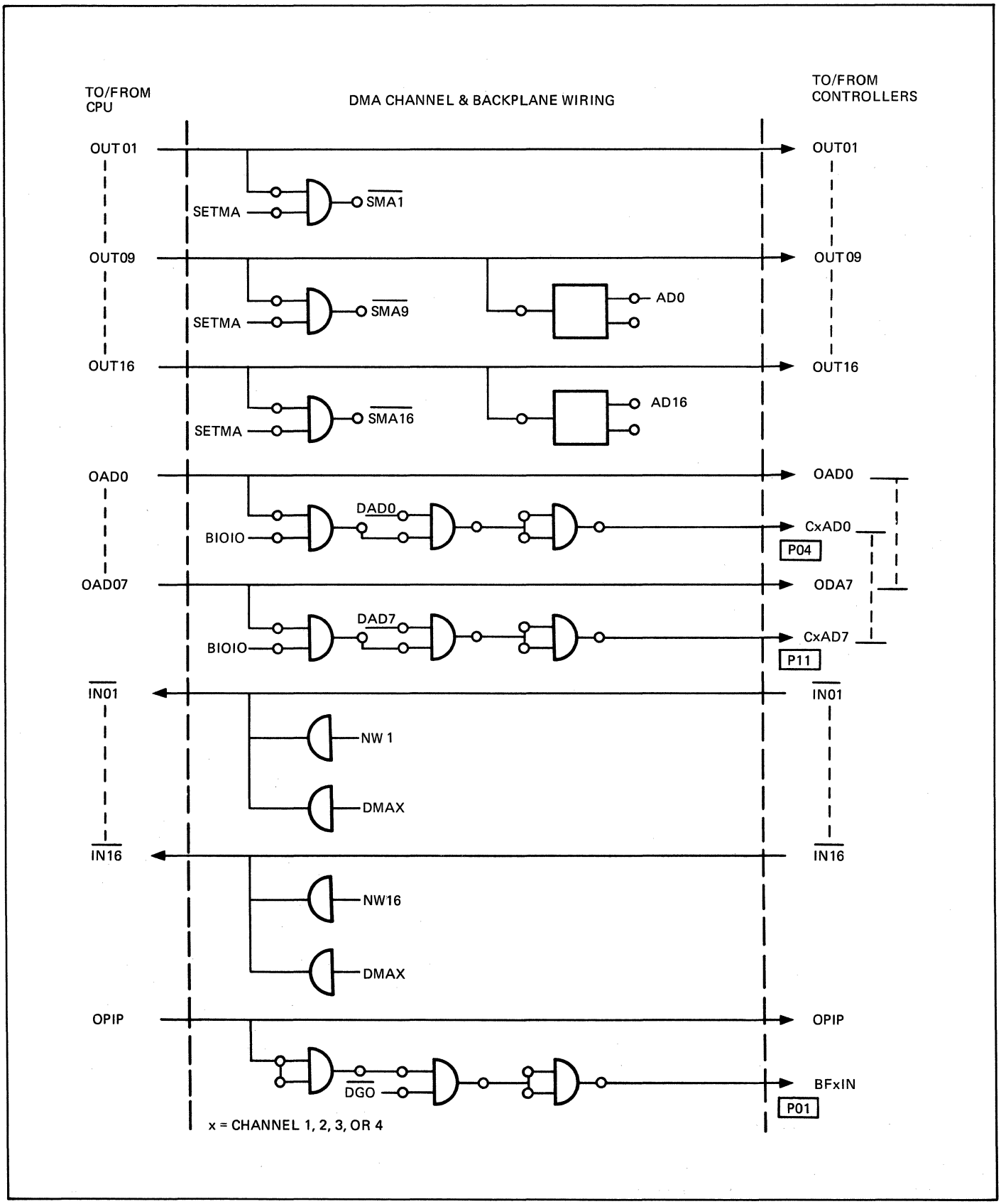


Figure 3-1. DMA Interface, Simplified Logic Diagram (Sheet 1 of 2)

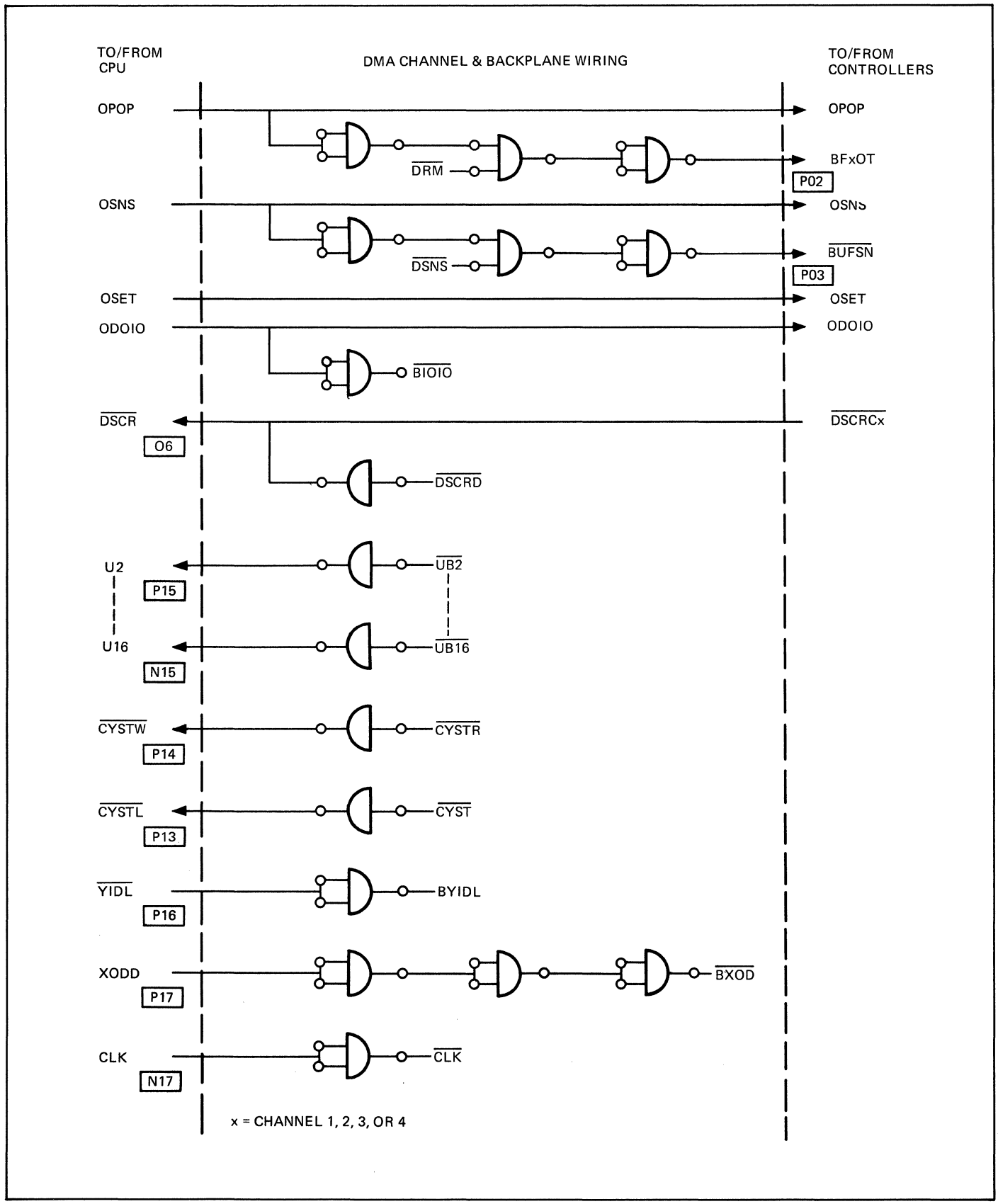


Figure 3-1. DMA Interface, Simplified Logic Diagram (Sheet 2 of 2)

Table 3-1. Block-Transfer Control Word Locations

ADDRESS		CHANNEL NO.	CONTROL WORD
Hexadecimal	Decimal		
20	32	1	Block starting address
21	33		Block word count
22	34	2	Block starting address
23	35		Block word count
24	36	3	Block starting address
25	37		Block word count
26	38	4	Block starting address
27	39		Block word count

Table 3-2. Standard DMA I/O Addresses

INSTRUCTION	ADDRESS		FUNCTION
	Hexadecimal	Decimal	
Set	E2	226	Start block transfer, DMA channel 1
	E3	227	Reset DMA channel 1
	E4	228	Start block transfer, DMA channel 2
	E5	229	Reset DMA channel 2
	E6	230	Start block transfer, DMA channel 3
	E7	231	Reset DMA channel 3
	E8	232	Start block transfer, DMA channel 4
	E9	233	Reset DMA channel 4
Sense	E2	226	Test chain ready or transfer complete, DMA channel 1
	E4	228	Test chain ready or transfer complete, DMA channel 2
	E6	230	Test chain ready or transfer complete, DMA channel 3
	E8	232	Test chain ready or transfer complete, DMA channel 4
Parallel Input	E2	226	Read word count register, DMA channel 1
	E4	228	Read word count register, DMA channel 2
	E6	230	Read word count register, DMA channel 3
	E8	232	Read word count register, DMA channel 4
Parallel Output	E2	226	Transfer device controller address, DMA channel 1
	E4	228	Transfer device controller address, DMA channel 2
	E6	230	Transfer device controller address, DMA channel 3
	E8	232	Transfer device controller address, DMA channel 4

3.5 MULTIPLE-BLOCK TRANSFER

The sequence of operations for a multiple-block transfer is similar to that for a single-block transfer with the following exceptions:

a. When the program sets up the control words, it sets the chaining flag (bit 1 of the word count control word) to 1 before initiating the operation.

b. After initiating the transfer, the program executes a Sense instruction with the appropriate channel address to determine when the first block control words have been fetched by the channel. When the control words for the first block have been transferred to the channel, the program sets up two new control words, again setting the chaining flag if more blocks are to follow. When the program sets up the control words for the last block, it signals the channel that the next block is the last by setting the chaining flag to 0. From this point on the channel handles the transfer as though it were a single-block transfer.

3.6 FUNCTIONAL DESCRIPTION

In the following description, all references to DMA operation use DMA channel 1 as an example. Certain logic signal names change depending on the channel used. Those signals in this description contain a 1 in the signal name to indicate channel 1. This number is replaced by a 2, 3, or 4 to agree with the channel used. Figure 3-2 is a functional block diagram of the DMA channel.

3.7 CPU-TO-DMA LOGIC

The CPU-to-DMA logic accepts data, timing, and control inputs from the processor and, where necessary, modifies them for use within the DMA logic.

Logic inputs from the processor include I/O instruction signals OSET for a Set instruction, OSNS for a Sense instruction, OPIP for a PIP instruction, OPOP for a POP instruction, and OIOIO which goes true when any of the I/O instructions occur.

These signals are brought into the controller chassis through the I/O connector card. The signals are used to generate signals $\overline{\text{BF1IN}}$, $\overline{\text{BF1OT}}$, $\overline{\text{BUFSN}}$, and $\overline{\text{BIOIO}}$.

The data input signals from the CPU are received on the OUT01 through OUT16 data lines. These signals are used as follows:

a. Signals OUT09 through OUT16 are used to load DMA address flip-flops AD0 through AD7. This transfer occurs by a programmed POP instruction.

b. Signals OUT01 through OUT16 are gated with signal SETMA to load flip-flops SMA1 through SMA16 to provide the starting address of the block of words to be transferred. This transfer occurs by DMA.

c. Signals OUT01 through OUT16 are gated with signal RSTNW to load flip-flops NW1 through NW16 to provide the number of words in the block to be transferred. This transfer occurs by DMA.

Eight address signals, OAD0 through OAD7, are derived from the eight least significant bits of the instruction register. The signals are brought into the controller chassis through high-impedance receivers.

Control signal $\overline{\text{PRST}}$ is received from the processor. Signal $\overline{\text{PRST}}$ is the processor power-on reset signal which goes to ground level momentarily when power is turned on. As illustrated on figures A-6 and A-4 in the appendix, when $\overline{\text{PRST}}$ goes to ground, signal ORSTB is generated. This signal is used to generate RSTB in the DMA logic.

3.8 Controller Address Register

The controller address register is loaded with the selected controller address by a POP instruction. The address is brought into the controller chassis on data lines OUT09 through OUT16 through the I/O connector card.

The DMA channel 1 controller address register consists of flip-flops AD0 through AD7. The inputs to the flip-flops are OUT09 through OUT16.

The controller address is loaded into the register by the positive-going edge of clock CLKAD. Signal CLKAD goes false and then true when DMA channel 1 is addressed by a POP instruction with a 0 in bit position OAD7. Clock CLKAD is generated by the DMA logic.

3.9 Controller Address Power Drivers

The controller address output drivers provide the selected controller address to the output lines. The drivers are gated either by an I/O command from the processor or by the controller address register outputs when operating under DMA control.

Eight power drivers are used to place the controller address onto the output lines to the controllers. Two sets of gates control the drivers. One set of gates has signal DMAIO as the enabling input. Signal DMAIO is generated by the DMA logic from signals $\overline{\text{BIOIO}}$ and GATED. When this signal is true, the drivers are controlled by the outputs of the controller address register. The other set of gates has signal BIOIO as the enabling input. When this signal is true, the drivers are under processor control and the output is determined by address bits AD0 through AD7. The outputs of the drivers are placed on the C1AD0 through C1AD7 lines to the controllers.

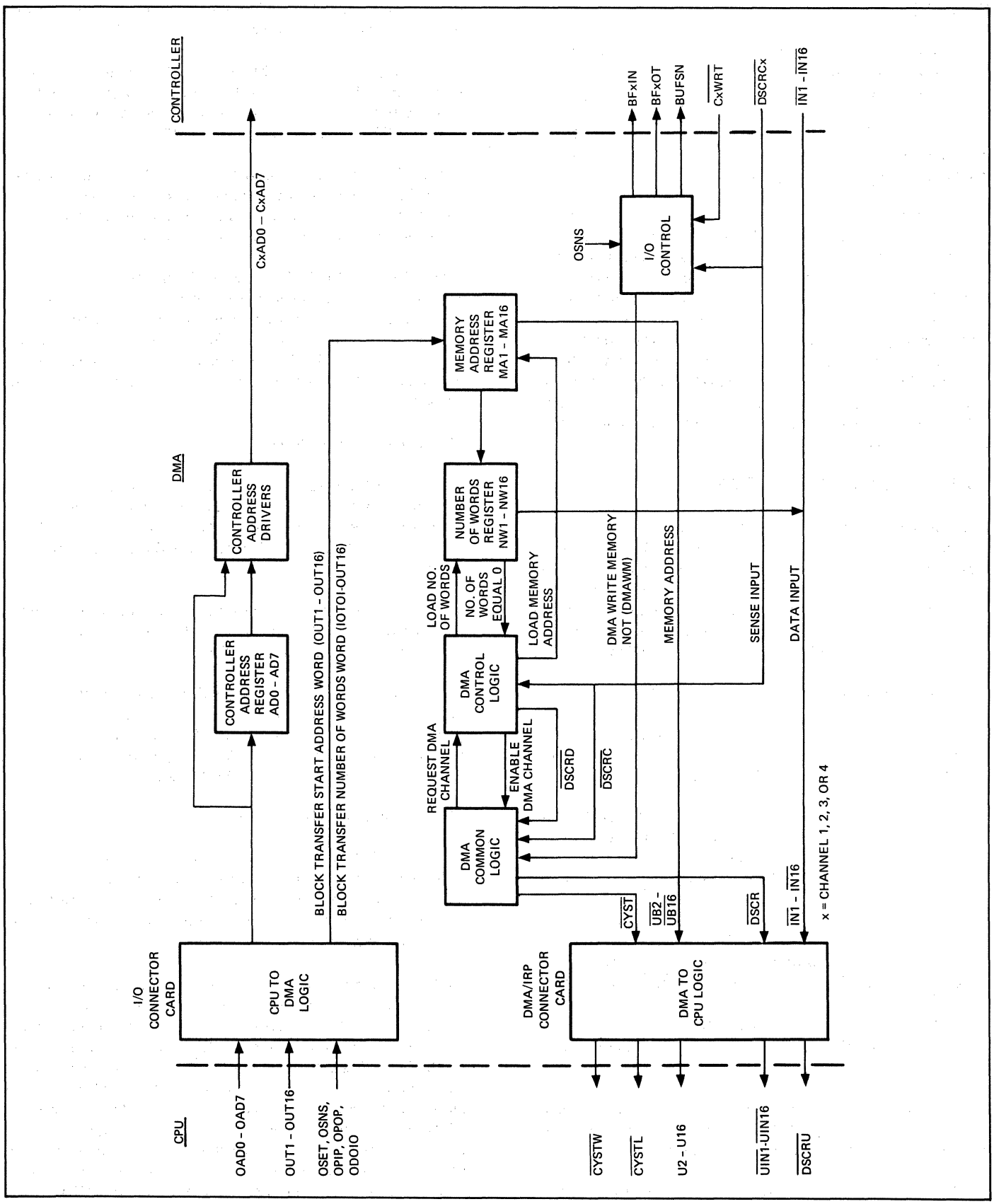


Figure 3-2. DMA Channel 1, Functional Block Diagram

3.10 DMA OPERATION

The DMA portion of the I/O consists of the DMA selection logic, DMA control logic, number-of-words register, memory address register, and I/O control logic.

3.11 DMA Selection Logic

The DMA selection logic determines which of the DMA channels is being addressed and transmits a signal that enables the control logic for the selected channel. The selection logic is also used for enabling interrupts.

The DMA channel address is transmitted from the processor on the OAD0 through OAD7 address lines. The DMA group address is established by the four most significant bits (OAD0 through OAD3) of the address portion of the control instruction. The group address for DMA channels 1 and 2 is OAD0 OAD1 OAD2 $\overline{\text{OAD3}}$. When these signals are true, signal BGRP is generated. Signal BGRP is then combined with the three least significant address bits (OAD4 through OAD6) to select the DMA channel within the addressed group. The address for DMA channel 1 is BGRP OADA OADB OADC. When these signals are true, signal DGRP is generated. Signals OADA, OADB, and OADC are generated by selecting OAD4, OAD5, and OAD6 or their complements.

3.12 DMA Control Logic

The DMA control logic controls the loading of the number-of-words register and the memory address register. It also determines, through inputs from the controller, whether the DMA transfer is to be a read or a write cycle. In addition, the control logic provides a DMA ready signal to the DMA-to-CPU logic for transmittal to the processor.

3.13 Memory Address Register

The memory address register consists of 16 flip-flops that are loaded with the starting address of the block of words to be transferred under DMA control. As each word is transferred, the register is increased by one count. The outputs of the flip-flops are placed on the DMA address lines to the processor.

The memory address register consists of flip-flops MA1 through MA16. The inputs to the flip-flops are the contents of memory location X'0020', which is the memory location containing the starting memory address for DMA channel 1.

3.14 Number-of-Words Register

The number-of-words register consists of 16 flip-flops that are loaded with the number of words in the selected block from memory location X'0021' for channel 1. As each word is transferred, the register is decreased one count. When the count reaches zero, a signal is generated to terminate the transfer.

The number-of-words register consists of flip-flops NW1 through NW16. Flip-flop NW1 determines whether the operation is to be a single block transfer or a chained transfer. A 1 in this bit indicates a chained transfer. A 0 indicates either a single block transfer or the terminating block in a chained transfer.

3.15 I/O Control

The I/O control logic generates sense command BUFSN, parallel input command BF1IN, and parallel output command BF1OT to the controller.

Figure 3-3 illustrates the timing for a BUFSN operation. As indicated on the figure, signal BUFSN follows signal $\overline{\text{BXOD}}$ when a processor-controlled I/O is not taking place. When the processor sends an SNS instruction, signal BUFSN goes true coincident with signal OSNS and remains true for one clock time after signal OSNS goes false. The addressed controller responds to this instruction by forcing $\overline{\text{DSCR}}$ false when it is ready to transfer data. At the end of the instruction, signal BIOIO goes false, enabling flip-flop RQSTD to set on the next clock pulse. When signal UADS goes true, the controller response is being transferred to the processor.

Signal BF1IN goes true when either a PIP command or a DMA channel 1 GO signal is generated.

Signal BF1OT goes true when either a POP instruction or a read memory command occurs.

Timing of signals BF1OT and BF1IN is illustrated on figure 3-4. The timing diagrams indicate the signals as applicable to DMA channel 1.

3.16 DMA-to-CPU Logic

The DMA-to-CPU logic gates either the DMA channel address or, in the event of an interrupt, address X'000F' onto the U2 through U16 lines to the processor. It also puts the contents of the number-of-words register onto the IN lines in response to a PIP X'E2' instruction. When an interrupt is active, the DMA-to-CPU logic puts the interrupts level address onto the IN lines. The cycle steal (CYSTL) and the cycle steal write (CYSTW) signals are generated in this logic.

3.17 DMA TRANSFER OPERATIONS

Initial conditions for a transfer operation are established by signal $\overline{\text{DRST}}$, which goes to ground level when power-on reset signal CPRST goes true, or when DMA channel 1 is addressed by a DMA reset Set instruction with OAD7 true (OSET DGRP OAD7). All of the control flip-flops are forced to their false state.

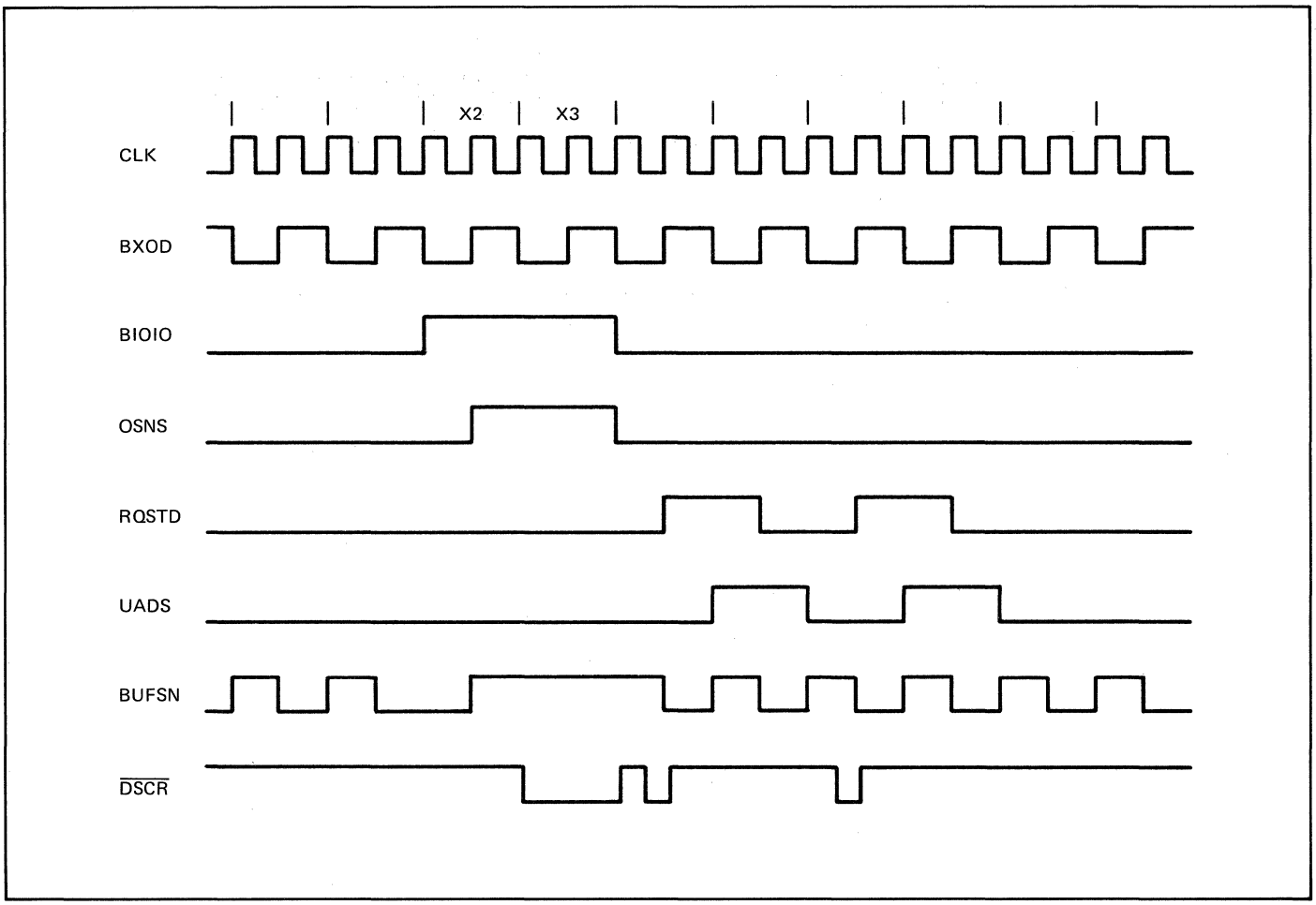


Figure 3-3. BUFSN, Timing Diagram

The DMA transfer is initiated by a start transfer Set instruction with a 0 in the OAD7 bit position. The DMA channel 1 address (DGRP OADA OADB OADC) causes signal DGRP to go true. Signals DGRP OSET OAD7 GATED set flip-flop RQSTD to its true state on the next CLKEV pulse. Signals RQSTD $\overline{\text{DTA}}$ cause signal DMA to be generated. Signal $\overline{\text{DTA}}$ indicates that no DMA channel of a higher priority is requesting service.

Figure 3-4 illustrates the timing for a DMA transfer of write two words and read two words. Logic diagrams for the DMA transfer operation are contained in the appendix.

When signal DMA goes true, signal $\overline{\text{CYST}}$ is made to go false. Signal $\overline{\text{CYST}}$ causes signal $\overline{\text{CYSTL}}$ to go false. The cycle steal signal inhibits normal processor operation at the end of the current memory cycle and enables the processor to generate signal UADS. The UADS signal is used in the CPU to gate DMA memory address lines U2 through U16 to the memory.

Signals DMA $\overline{\text{GATED}}$ and $\overline{\text{LODMA}}$ set flip-flop LODNW at the next CLKOD clock. Flip-flop LODNW controls the loading of the number of words in the block. The LODNW signal is used in forcing the processor to DMA number-of-words memory location X'0021' and in loading the contents of that address onto the OUT01 through OUT16 data lines and into the memory address register. The contents of the memory address register are then clocked into the number-of-words register.

Flip-flop LODMA controls the loading of the starting address into the memory address register. The flip-flop is enabled by signal LODNW and is clocked by signal CLKOD. Signal LODMA is used to force the processor to DMA memory start address location X'0020' and in loading the contents of that location onto the OUT01 through OUT16 data lines and into the memory address register.

Flip-flop RQSTD is reset on the CLKEV clock that occurs after flip-flop LODMA is set. Signals LODMA $\overline{\text{RQSTD}}$ enable flip-flop GATED to set on the next CLKOD clock. At the same time, flip-flops LODMA and LODNW are reset.

With signal GATED true and no I/O instruction in progress, signal DMAIO is generated by GATED BIOIO. When

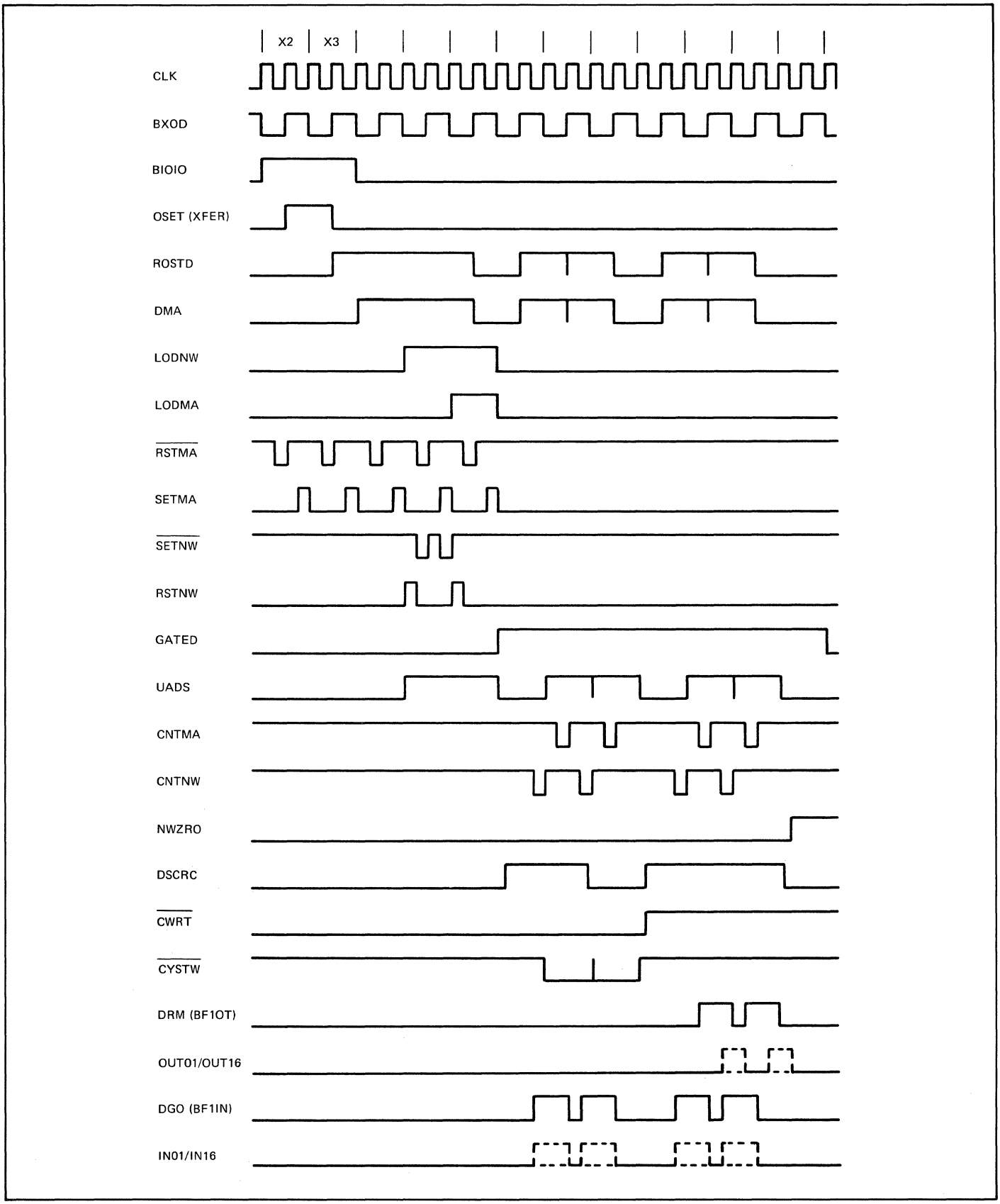


Figure 3-4. Write Two Words-Read Two Words, Timing Diagram

the controller is ready to write into memory, it forces DSCRC and CWRT false and DSCRC true. Signals NWZRO DMAIO DSCRC enable flip-flop RQSTD to go true on the next CLKEV clock. At that time, signal DMA goes true. Signals DMA GATED DGO CLK direct set flip-flop DGO. Signals DGO and CWRT force the DMA write memory signal DMAWM to ground level. Cycle steal read flip-flop CYSTR is then reset at the next CLKOD clock. With signal CYSTR true, signal CYSTW goes false. When signal UADS is generated by the processor, the first word contained on the IN lines is written into memory.

Flip-flop DGO is reset by clock CLKEV and is then set again by signals DMA GATED DGO CLK for the next word.

When bits NW2 through NW16 of the number-of-words register are zero, signal NWZRO goes true. Signals NWZRO GATED NW1 enable the DMA ready flip-flop D1RDY to set on the next CLKOD clock. Signal D1RDY is used with signal DGRP to generate signal DSCRD in response to a transfer complete Sense instruction. Signals DSCRD and SNRDY force signal DSCR to ground level, indicating to the processor that the DMA channel is ready.

The read cycle is essentially the same as the write cycle except that cycle steal read flip-flop CYSTR remains set (CYSTW true), the channel 1 read memory flip-flop is set (DRM true), and the BF1OT I/O signal to the controller goes false.

3.18 MEMORY ADDRESS REGISTER

The memory address register is reset by signal RSTMA going to ground level when signals GATED RSTNW BXOD CLK are true.

When signal DMA is true and flip-flop LODNW sets, signal FRCU goes true. Signal FRCU causes signal U11 to go high. Signals FRCU LODMA cause signal U16 to go high. Address X'0021' is forced onto the U2 through U16 lines. This address is the memory location containing the number of words for DMA channel 1. The processor then puts the contents of memory location X'0021' onto the OUT01 through OUT16 lines. When signal SETMA goes true (signals GATED BXOD CLK true), the word count is loaded into the memory address register.

The outputs of memory address flip-flops MA1 through MA16 are applied to the gates controlling the direct reset inputs to the number-of-words register flip-flops. When signal RSTNW goes true (signals LODNW EVPULS BXOD true), the number-of-words register is loaded with the contents of the memory address register.

When flip-flop LODMA sets, signal FRCU is again generated. Since signal LODMA is false, only U11 goes high and address X'0020' is forced onto the U2 through U16 lines. This is the starting address of the block to be transferred. The processor puts the contents of memory location X'0020' onto the OUT01 through OUT16 lines. When signal SETMA goes true, the address is loaded into the memory address register. The same clock that resets flip-flop LODMA sets flip-flop GATED. The GATED and DMA signals cause signal MATU to go true and the contents of the memory address register are gated onto the U2 through U16 lines. As each word is transferred, the memory address register is increased one count by signal CNTMA going false and then true.

3.19 NUMBER-OF-WORDS REGISTER

Initial conditions for the number-of-words register are established by signal SETNW which goes to ground level when signals LODNW LODMA CLK are true. The register is loaded with the contents of the memory address register when signal RSTNW goes true.

As each word is transferred, the number-of-words register is decreased one count by signal CNTNW going false and then true. When the register has counted down to zero, signal NWZRO goes true. Signals NWZRO GATED NW1 enable flip-flop DRDY to set. Signal DRDY indicates the channel is ready for the next operation.

When DMA channel 1 is addressed by a PIP instruction (with address X'E2' for channel 1), the contents of the number-of-words register are gated onto the IN1 through IN16 lines. Signals OPIP DGRP OAD7 generate signal PIPNW, which is the gating signal common to all 16 IN lines. The other inputs to the IN lines are the outputs of the number-of-words register flip-flops.

3.20 DATA CHAINING

In the data chaining mode, a 1 is set into the most significant bit position of the number-of-words memory location. The 1 in this bit position sets number-of-words register flip-flop NW1 when the register is loaded. As soon as the memory address is loaded and flip-flop RQSTD is reset, flip-flop D1RDY is enabled to set, indicating to the processor that DMA channel 1 memory locations can be loaded with a new address and number of words. Flip-flop D1RDY is reset with a Sense instruction.

When the content of the number-of-words register is zero, signal NWZRO goes true. NWZRO causes GATED to reset at the next CLKOD clock. Signals NWZRO NW1 GATED enable flip-flop RQSTD to set and a new DMA sequence begins.

The last block to be transferred is identified by a 0 in the most significant bit position of the number of words to be transferred.

3.21 ACTIVE PULLUPS

The DSCR and UIN1 through UIN16 lines to the processor have active pullup circuits. These circuits ensure that the lines return to +5V after being driven to ground level.

SECTION IV
PRIORITY INTERRUPT INTERFACE

4.1 INTRODUCTION

The priority interrupt option provides the computer with the capability to respond quickly to external requirements. The interrupts are combined into four groups with eight levels of interrupts in each group for a maximum of 32 levels. Each interrupt card contains eight levels of interrupts.

All clock signals used throughout the DMA and priority interrupt options are generated from the CPU clock signals. The clock signals are used internally and are not transmitted to the controllers. A 2-MHz clock ($\overline{\text{BCLK}}$) is available for controller use.

4.2 PRIORITY INTERRUPTS

Priority interrupt levels are designated 1 through 32, with level 1 having the highest priority. This level is preassigned as the power-on interrupt; all other levels are unassigned and can be used for any purpose.

Each interrupt level is assigned two locations in memory for storage of a double word Branch Unconditional instruction. When an interrupt level becomes active, program control is automatically transferred to the location assigned to that interrupt, and the Branch Unconditional instruction stored there then branches the program to the interrupt servicing routine. The memory location assignments for the priority interrupt levels (assuming a 16K memory system) are listed in table 4-1.

4.3 INTERRUPT LEVEL STATES

All priority interrupt levels have four operational states: disarmed, armed, waiting, and active (except the power-on interrupt which is always armed and enabled). The significance of each state is as follows:

a. Disarmed. When an interrupt level is disarmed, the level cannot accept an interrupt signal from its assigned source. This is the inactive state.

b. Armed. When an interrupt level is armed, the level can accept and remember an interrupt signal from its assigned source. Upon receiving the interrupt signal, the level advances to the waiting state.

c. Waiting. All interrupt levels that have been armed and have received an interrupt signal remain in the waiting state until the interrupts are enabled. When enabled, the highest priority waiting interrupt level becomes active and all other waiting levels remain in the waiting state.

d. Active. When the interrupt levels are enabled, the highest priority waiting interrupt level becomes active upon completion of the instruction being executed.

When an interrupt level becomes active, the following sequence occurs:

a. The interrupt address of the interrupt level is written into basic interrupt memory location X'000F'. This transfer occurs by direct memory access.

b. The computer executes an indirect Branch and Put instruction with a reference address of X'000F'. The Branch and Put instruction stores current program status and the link address in the roll table, fetches the interrupt level address from location X'000F', and then transfers program control to that address.

c. The computer executes the double word Branch Unconditional instruction stored at the interrupt level address to enter the interrupt level servicing routine.

When an interrupt level becomes active, the NABLX flip-flop is reset, thereby disabling all interrupt levels. No interrupt level can advance to the active state until the program again enables the interrupts. If the interrupt levels are again enabled at the beginning of the servicing routine and a higher priority level advances to the waiting state, the higher priority interrupt is allowed to interrupt the servicing routine of the lower priority interrupt. In no case can a lower priority interrupt level interrupt the servicing routine of a higher priority interrupt.

Once an interrupt level becomes active, it remains active until the level is reset by the program (normally at the end of the servicing routine). Resetting the level causes NABLX to set, thereby enabling the interrupts. If a lower priority interrupt level is waiting when the current level is reset, the lower priority level advances to the active state.

4.4 INTERRUPT CONTROL

Priority interrupt levels are controlled by the Parallel Output and Set instructions. Arming and disarming of the levels are controlled by the Parallel Output instruction; enabling and resetting are controlled by the Set instruction.

Table 4-1. Priority Interrupt Level Assignments

ADDRESS		GROUP	LEVEL	PRIORITY	ASSIGNMENT
Decimal	Hexadecimal				
16,320 16,321	3FC0 3FC1	4	32	32	Unassigned
16,322 16,323	3FC2 3FC3		31	31	Unassigned
16,324 16,325	3FC4 3FC5		30	30	Unassigned
16,326 16,327	3FC6 3FC7		29	29	Unassigned
16,328 16,329	3FC8 3FC9		28	28	Unassigned
16,330 16,331	3FCA 3FCB		27	27	Unassigned
16,332 16,333	3FCC 3FCD		26	26	Unassigned
16,334 16,335	3FCE 3FCF		25	25	Unassigned
16,336 16,337	3FD0 3FD1	3	24	24	Unassigned
16,338 16,339	3FD2 3FD3		23	23	Unassigned
16,340 16,341	3FD4 3FD5		22	22	Unassigned
16,342 16,343	3FD6 3FD7		21	21	Unassigned
16,344 16,345	3FD8 3FD9		20	20	Unassigned
16,346 16,347	3FDA 3FDB		19	19	Unassigned
16,348 16,349	3FDC 3FDD		18	18	Unassigned
16,350 16,351	3FDE 3FDF		17	17	Unassigned

Table 4-1. Priority Interrupt Level Assignments (Cont.)

ADDRESS		GROUP	LEVEL	PRIORITY	ASSIGNMENT
Decimal	Hexadecimal				
16,352 16,353	3FE0 3FE1	2	16	16	Unassigned
16,354 16,355	3FE2 3FE3		15	15	Unassigned
16,356 16,357	3FE4 3FE5		14	14	Unassigned
16,358 16,359	3FE6 3FE7		13	13	Unassigned
16,360 16,361	3FE8 3FE9		12	12	Unassigned
16,362 16,363	3FEA 3FEB		11	11	Unassigned
16,364 16,365	3FEC 3FED		10	10	Unassigned
16,366 16,367	3FEE 3FEF		9	9	Unassigned
16,368 16,369	3FF0 3FF1	1	8	8	Unassigned
16,370 16,371	3FF2 3FF3		7	7	Unassigned
16,372 16,373	3FF4 3FF5		6	6	Unassigned
16,374 16,375	3FF6 3FF7		5	5	Unassigned
16,376 16,377	3FF8 3FF9		4	4	Unassigned
16,378 16,379	3FFA 3FFB		3	3	Unassigned
16,380 16,381	3FFC 3FFD		2	2	Unassigned
16,382 16,383	3FFE 3FFF		1	1	Power on

The levels are individually armed or disarmed 16 levels at a time by executing a Parallel Output instruction with an effective address of X'EA' (levels 1 through 16) or X'EE' (levels 17 through 32). The contents of the accumulator at the time the instruction is executed specify the state to which each level is set. Each bit position of the control word corresponds to one interrupt level.

The levels are enabled by executing a set enable Set instruction with an effective address of X'EA' or by executing a reset highest MRK Set instruction with an effective operand address of X'EB'. These instructions enable the interrupt levels as a whole but only the highest priority waiting interrupt can advance to the active state if no higher priority interrupt is active.

An active level is reset by executing a reset highest MRK Set instruction with an effective address of X'EB'. This instruction resets the currently active level and permits the next highest priority waiting and enabled level to advance to the active state.

4.5 FUNCTIONAL DESCRIPTION

Figure 4-1 is a logic block diagram of the priority interrupt feature. As indicated on the diagram, the interrupt feature consists of arm register flip-flops, an interrupt register, a mark register, interrupt level selection logic, and address selection logic.

The arm register consists of eight flip-flops for each group of interrupts. The arm register is set up by a Parallel Output instruction with an effective address of X'EA' for levels 1 through 16 and an effective address of X'EE' for levels 17 through 32.

The interrupt register consists of eight flip-flops for each group of interrupts. When an interrupt signal is received, the selected interrupt flip-flop sets if the corresponding arm flip-flop has been set.

The mark register consists of eight flip-flops for each group of interrupts. The mark register keeps track of the interrupt being processed. Once a mark flip-flop has been set, no lower priority interrupt is recognized. If a higher priority interrupt occurs, the program branches to the new subroutine, processes the interrupt, and then returns to the previous interrupt level.

The interrupt level selection logic controls the inhibiting or enabling of the mark register flip-flops.

The address selection logic provides the address of the selected interrupt address to the drivers that activate the $\overline{IN}$ lines to the processor.

No new interrupt can occur unless the NABLX flip-flop is set. The NABLX flip-flop enables the MRK flip-flops, which are required to initiate the correct level interrupt.

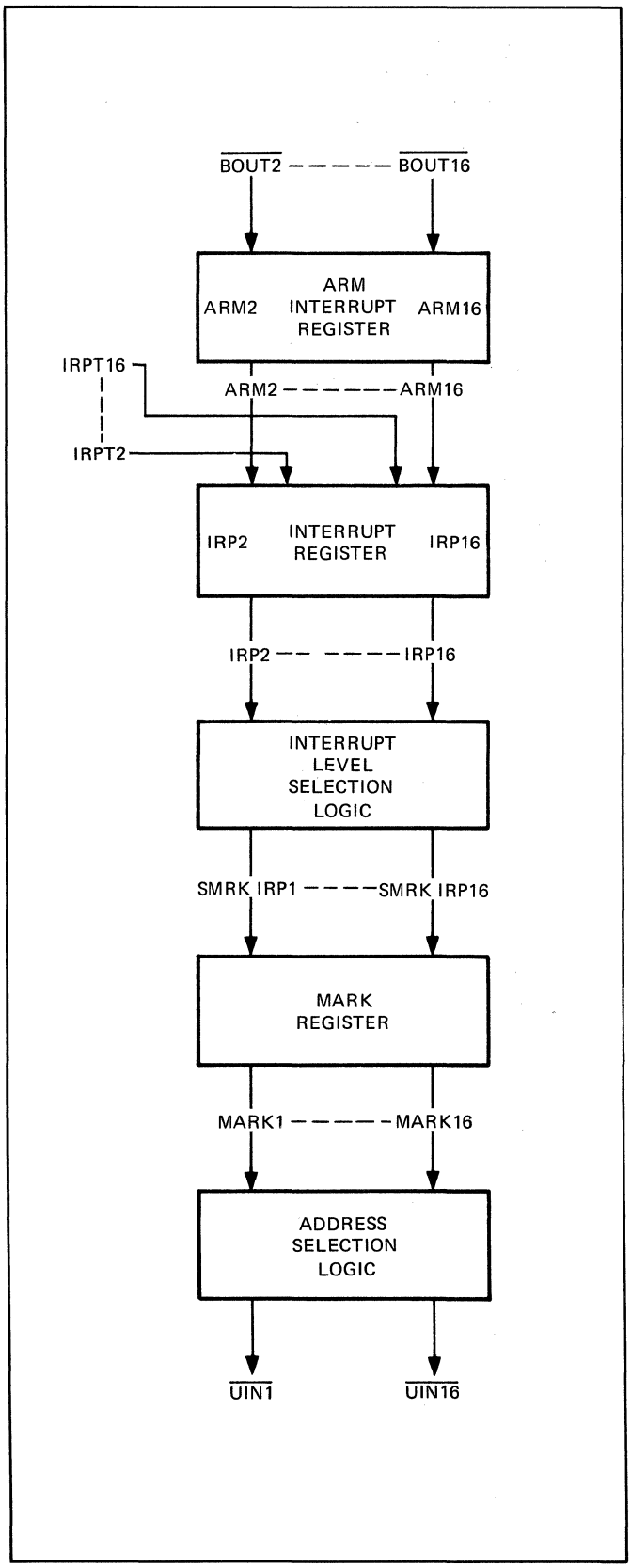


Figure 4-1. Priority Interrupt, Logic Block Diagram

4.6 Interrupt Sequence

Initial conditions for the interrupt logic are established by signal $\overline{\text{PRSTB}}$. Signal $\overline{\text{PRSTB}}$ goes to ground momentarily when power is turned on at the computer. While at ground level, signal $\overline{\text{PRSTB}}$ sets interrupt enable flip-flop NABLX and resets external interrupt flip-flop IRPX, mark register flip-flops MRK1 through MRK7, and register flip-flops ARM01 through ARM08. The 0-volt outputs of the ARM flip-flops direct reset interrupt flip-flops IRP1 through IRP8.

If the power shutdown option is installed, level 1 is used as the power shutdown interrupt and should not be armed. This interrupt forces the computer to memory location X'3FFE', the power-on interrupt location. The power-on interrupt servicing routine is performed restoring the next instruction address, the states of the computer indicator flip-flops and the contents of the page, word, and index registers that were in effect at the time power was turned off. The computer is then restored to correct initial conditions.

During a Parallel Output or Set instruction with an effective address of X'EA', X'EB', or X'EE', interrupt group address signal PGRP is generated from the address bits on the OAD0 through OAD7 I/O buffer lines.

The I/O instructions used with the interrupt function are the following:

Instruction	Function
POP X'EA'	Arm interrupt group 1
POP X'EE'	Arm interrupt group 2
SET X'EA'	Set interrupt enable
SET X'EB'	Reset mark flip-flop

SET X'EA' and X'EB' set the NABLX flip-flop. SET X'EB' also resets the highest MRK flip-flop.

In the following discussion, interrupt level 2 is used as an example. The other interrupt levels would function similarly. Figure 4-2 illustrates the timing associated with the interrupt sequence.

Figure 4-3 illustrates the logic for the following interrupt sequence. With the initial conditions set as

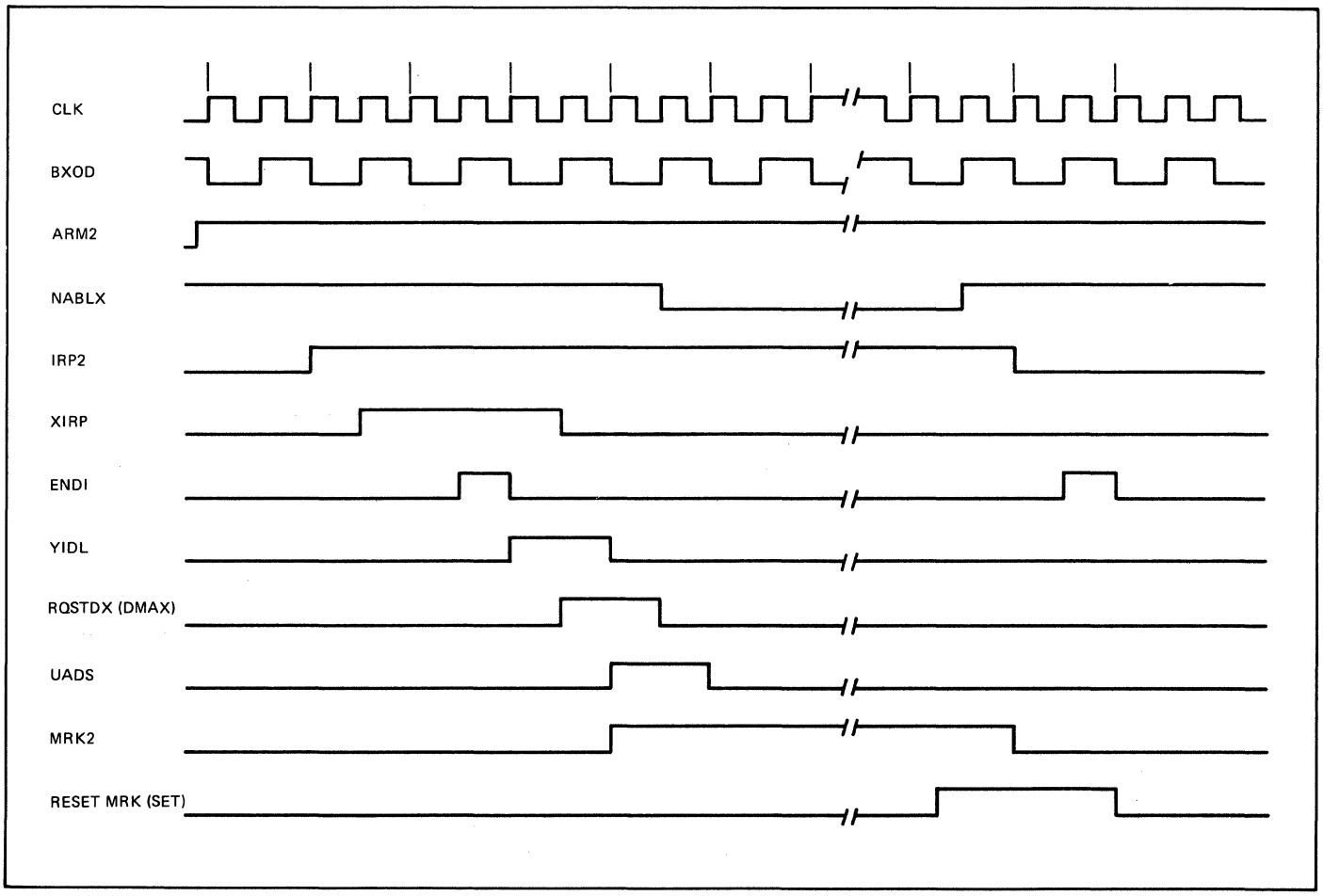


Figure 4-2. Interrupt Operation, Timing Diagram

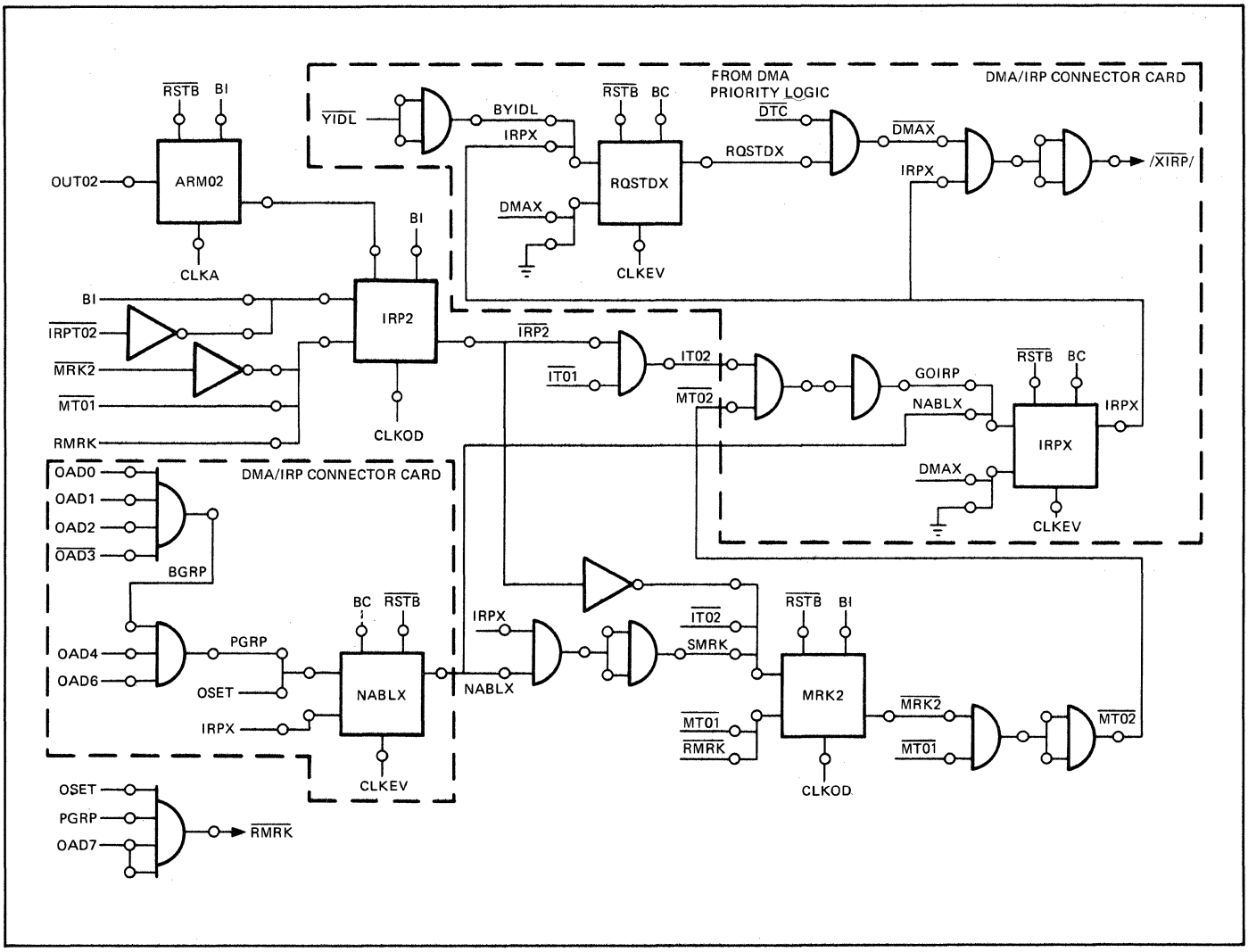


Figure 4-3. Interrupt Sequence Level 2, Logic Diagram

discussed above, a Parallel Output instruction with an effective address of X'EA' is executed (signal OUT02 true). When computer clock CLK occurs, parallel output signal OPOP causes clock CLKA to be generated. Signals OUT02 and CLKA set flip-flop ARM02. With flip-flop ARM02 set, flip-flop IRP2 is enabled.

A SET instruction with an effective address of X'EA' is executed to enable all interrupt levels. The SET instruction signal OSET enables flip-flop NABLX to set on the next CLKEV clock pulse.

The ARM02 signal enables flip-flop IRP2. When the interrupt 2 request signal IRPT02 goes to ground flip-flop IRP2 sets on the next CLKOD clock pulse.

When flip-flop IRP2 sets, the interrupt level select logic generates signal IT02. The MRK flip-flops being reset generate signal MT2. The IT02 and MT2 signals are applied to a gate to generate interrupt signal GOIRP.

Signals GOIRP and NABLX enable flip-flop IRPX to set on the next CLKEV clock pulse.

Signal IRPX is applied to a gate to generate external interrupt signal XIRP to the computer.

The XIRP signal causes the computer to go to the idle state at the end of the current instruction. Signal BYIDL then goes true. Expression BYIDL IRPX enables flip-flop RQSTDX to set on the next CLKEV clock pulse.

Signals IRPX and NABLX are applied to a gate to generate signal SMRK. This signal enables flip-flop MRK2 to set at the next CLKOD clock pulse. Signal MRK2 going true causes signal MT2 to go to zero.

When flip-flop RQSTDX is set, the true output signal enables gate DMAX to go true as soon as no higher priority DMA channel is being requested. DMAX is always the lowest priority. Signals MRK2 and MRK1 being true

generate signal PAD15. The DMAX and PAD15 signals force address X'3FFC' onto lines $\overline{IN1}$ through $\overline{IN16}$. This address is loaded into memory location X'000F' in the computer. The DMAX signal also forces address X'000F' onto DMA memory address lines U3 through U16.

The computer executes an indirect Branch and Put instruction to memory location X'000F', fetches the stored address, branches to location X'3FFC' and executes an unconditional branch to the interrupt subroutine.

The DMAX signal enables flip-flops RQSTDX and IRPX to reset on the next CLKEV clock. Flip-flop MRK2 is reset with a SET instruction with an effective address X'EB'.

4.7 Interrupt Servicing Routine

When an interrupt level advances to the active state, the computer automatically stores the status of the program at the time of the interruption by means of a Branch and Put instruction. It also stores the next instruction address for return linkage from the servicing routine. This permits a Branch Back instruction at the end of the servicing routine to return the program to the point at which the interrupt occurred.

Since the interrupt levels are automatically disabled as soon as an interrupt becomes active, the servicing routine must contain an interrupt enabling instruction (SET X'EA') at the beginning of the routine if it is desired to allow higher priority interrupts to interrupt the routine.

The normal exit instruction sequence is an interrupt reset instruction (SET X'EB') followed by a Branch Back instruction. The Set instruction resets the active interrupt level and sets the NABLX flip-flop if it was not set earlier in the routine; the Branch Back instruction transfers control back to the point at which the interrupt occurred.

4.8 INTERRUPT INTERFACE

Interrupt request signals are brought into the interrupt logic through the backplane wiring on the controller chassis or by connecting to the interrupt card edge connector. Tables A-8 through A-11 in the appendix list the pin and signal requirements for the backplane wiring. Each interrupt card contains eight levels of interrupts.

The interrupt request signals consist of signals $\overline{IRPT01}$ through $\overline{IRPT32}$ from the controllers or external devices. The interrupt signals are used by the IRP1 through IRP32 flip-flops to initiate the waiting state of the interrupt. Signals $\overline{IRPT01}$ through $\overline{IRPT32}$ are normally high. They must go low for a minimum of 1.1 microseconds to ensure acceptance by the IRP flip-flops. The signals may stay low longer if convenient, but they must be brought high before the NABLX flip-flop is set.

4.9 CLOCK INTERFACE

The basic computer clock (CLK) is 430 nanoseconds in duration. During the time that the operand address is selected and the instruction is read, a delay clock (YOAS) is used to add an additional 200 nanoseconds.

An additional timing signal (XODD) is received from the computer. Signal XODD is an 860-nanosecond signal coincident with the phase of basic clock CLK.

Clock CLK is received by the controller chassis from the computer and is buffered to form clock signal $\overline{CLK}$. Signal XODD is received by the controller chassis and is applied to three NAND gates to form signals BXOD and $\overline{BXOD}$.

The $\overline{CLK}$ and $\overline{BXOD}$ signals are applied to a power driver to provide a clock signal CLKEV. The $\overline{CLK}$ and BXOD signals are applied to two power drivers. The outputs of the drivers are tied together to provide clock signal CLKOD.

These clock signals are used within the DMA and interrupt logic for timing and control. The clocks are not transmitted to the controllers.

Figure 4-4 illustrates the clock generation logic within the I/O buffer.

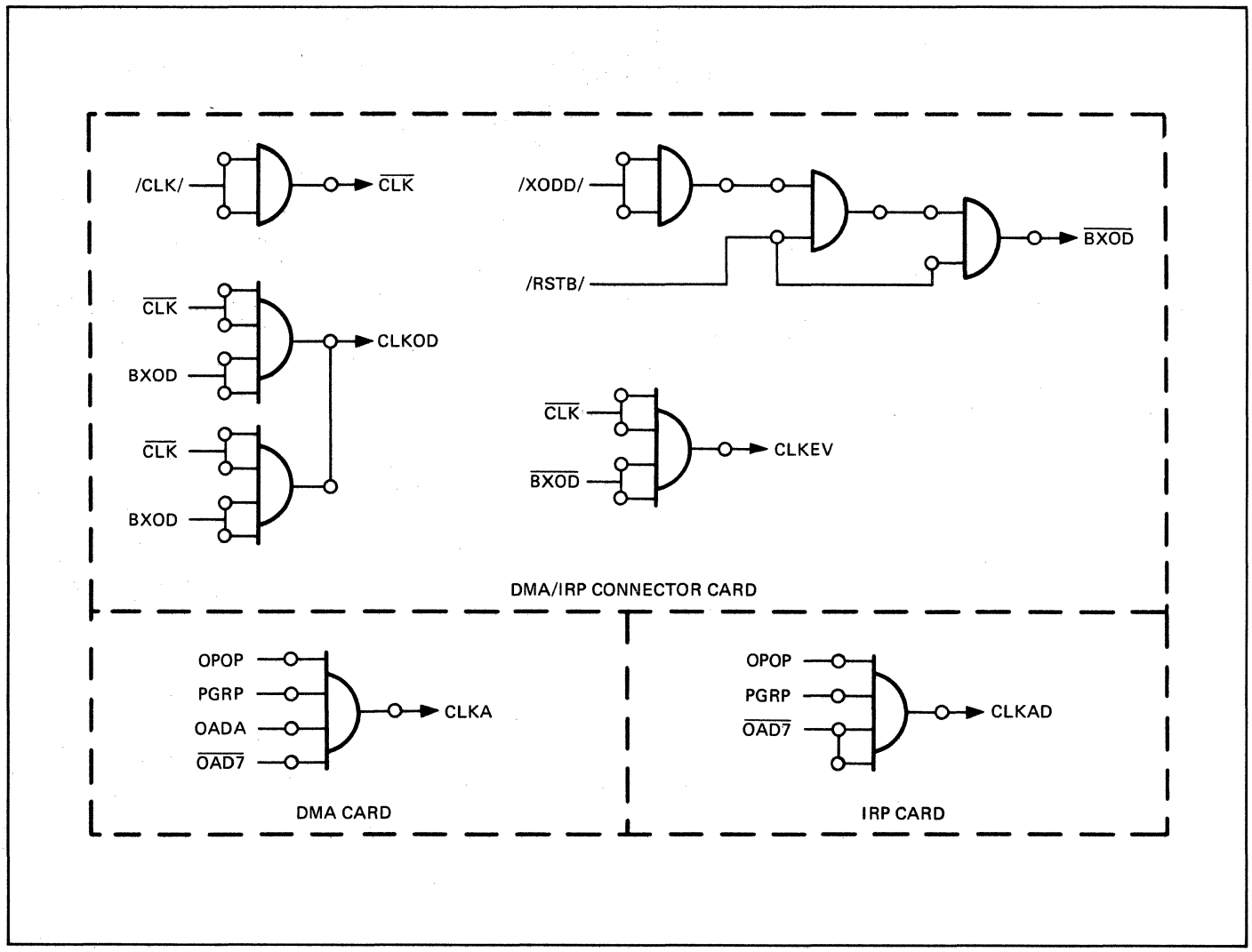


Figure 4-4. Clock Generation, Logic Diagram

APPENDIX A
REFERENCE DATA

A.1 INTRODUCTION

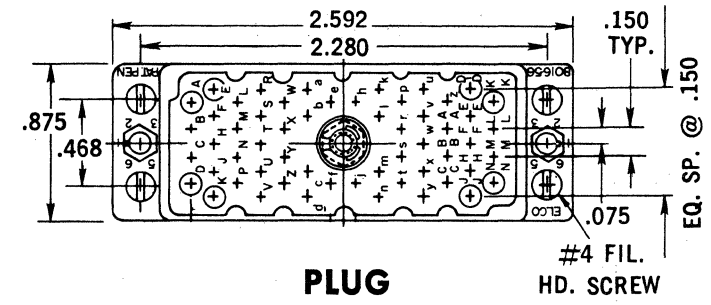
The appendix contains listings of signals and the pin numbers where they are available for the CPU connectors, the connector cards on the controller chassis, and the backpanel wiring for the DMA channels, interrupt groups, and controller cards. Also contained are a signal dictionary and diagrams illustrating generation of the various logic signals.

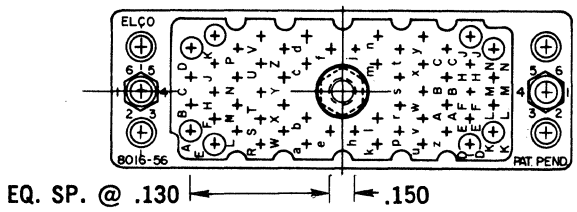
A.2 CONTENTS

Tables A-1 and A-2 list the signals available at CPU DMA/IRP and I/O connectors. Tables A-3 through A-17 list the backplane wiring for the DMA/IRP and I/O connector cards, DMA channels 1 through 4 backplane wiring, interrupt groups 1 through 4 backplane wiring and the DMA controlled Controller card backplane wiring. Table A-18 contains the connector and cable requirements and the manufacturers' names. Table A-19 contains the interface logic signal dictionary.

Figures A-1 through A-6 contain logic drawings of the interface and the DMA. Figure A-7 illustrates the layout of the controller chassis.

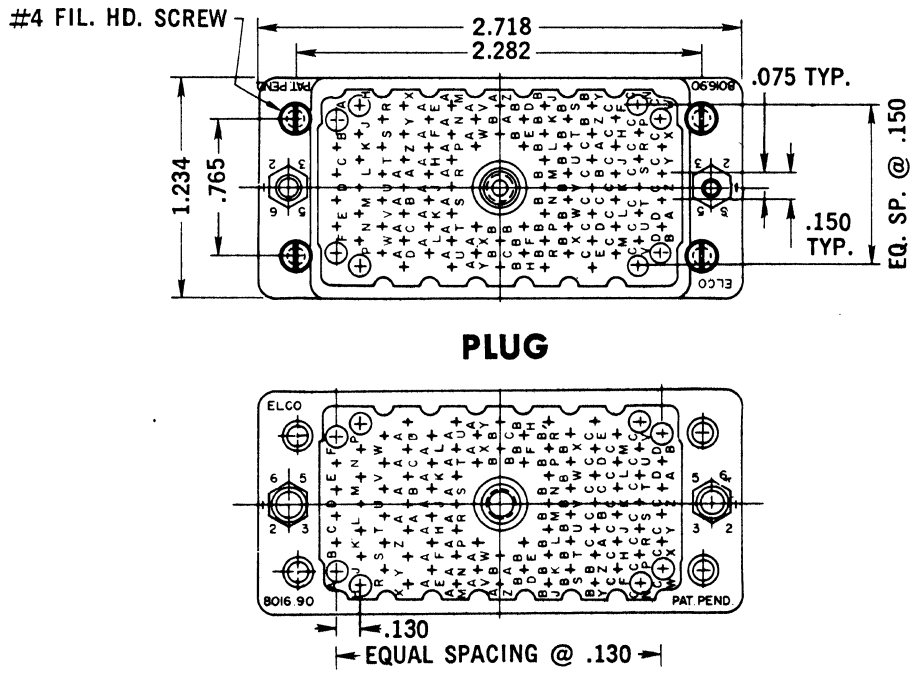
Table A-1. Interface Cable Signals at CPU Connector J71 (DMA/IRP)





Signal Pin No.	Return Pin No.	Signal	Signal Pin No.	Return Pin No.	Signal
JJ	d	XIRP	U	x	U16
y	d	U3	C	x	$\overline{\text{CYSTL}}$
V	d	U4	N	J	$\overline{\text{CYSTW}}$
n	d	U5	E	J	U2
D	P	U6	Y	J	$\overline{\text{YIDL}}$
K	P	U7	BB	J	XODD
f	P	U8	MM	s	$\overline{\text{UADS}}$
Z	P	U9	FF	s	$\overline{\text{OIOIO}}$
CC	t	U10	T	s	CLK
j	t	U11	H	s	$\overline{\text{LIDL}}$
m	t	U12	a	L	PLUPIN
NN	t	U13	R	L	$\overline{\text{OMPTY}}$
HH	x	U14	u	L	$\overline{\text{CK2MS}}$
c	x	U15	p	L	ORSTB

Table A-2. Interface Cable Signals at CPU Connectors J69 and J70 (I/O)



Signal Pin No.	Return Pin No.	Signal	Signal Pin No.	Return Pin No.	Signal
CV	BC	$\overline{\text{OPIP}}$	BB	AT	$\overline{\text{OUT3}}$
CE	BC	$\overline{\text{OPOP}}$	AC	V	$\overline{\text{OUT4}}$
BR	BC	$\overline{\text{OSET}}$	N	V	$\overline{\text{OUT5}}$
AU	F	$\overline{\text{OSNS}}$	E	V	$\overline{\text{OUT6}}$
AD	F	$\overline{\text{OIOIO}}$	AK	BW	$\overline{\text{OUT7}}$
P	F	$\overline{\text{PRST}}$	AX	BW	$\overline{\text{OUT8}}$
AL	BH	-6V	BF	BW	$\overline{\text{OUT9}}$
AY	BH	+5V	CL	CC	$\overline{\text{OUT10}}$
BX	CU	+12V	DA	CC	$\overline{\text{OUT11}}$
CD	AT	$\overline{\text{OUT1}}$	CT	CC	$\overline{\text{OUT12}}$
BP	AT	$\overline{\text{OUT2}}$	BN	M	$\overline{\text{OUT13}}$

Table A-2. Interface Cable Signals at CPU Connectors J69 and J70 (I/O) (Cont.)

Signal Pin No.	Return Pin No.	Signal	Signal Pin No.	Return Pin No.	Signal
AS	M	$\overline{\text{OUT14}}$	AP	K	$\overline{\text{UIN3}}$
AB	M	$\overline{\text{OUT15}}$	Z	K	$\overline{\text{UIN4}}$
D	BV	$\overline{\text{OUT16}}$	B	AW	$\overline{\text{UIN5}}$
U	BV	+5V	S	AW	$\overline{\text{UIN6}}$
AJ	BV	$\overline{\text{OAD0}}$	AF	AW	$\overline{\text{UIN7}}$
CK	CB	$\overline{\text{OAD1}}$	BE	CX	$\overline{\text{UIN8}}$
CZ	CB	$\overline{\text{OAD2}}$	CT	CX	$\overline{\text{UIN9}}$
CS	CB	$\overline{\text{OAD3}}$	CH	CX	$\overline{\text{UIN10}}$
BM	L	$\overline{\text{OAD4}}$	CP	BA	$\overline{\text{UIN11}}$
AR	L	$\overline{\text{OAD5}}$	BZ	BA	$\overline{\text{UIN12}}$
AA	L	$\overline{\text{OAD6}}$	BK	BA	$\overline{\text{UIN13}}$
C	BU	$\overline{\text{OAD7}}$	AN	A	$\overline{\text{UIN14}}$
AH	BU	KEY	Y	A	$\overline{\text{UIN15}}$
CR	CA	$\overline{\text{UIN1}}$	J	A	$\overline{\text{UIN16}}$
BL	K	$\overline{\text{UIN2}}$	R	AV	$\overline{\text{DSCR}}$

Table A-3. DMA/IRP Connector Card Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{IN05}$	15	$\overline{OMPTY}$	29	$\overline{UB13}$	43	$\overline{UB02}$	57	PAD15A	71	OAD1	85
GNDB	2	$\overline{IN06}$	16	$\overline{GOIRP1}$	30	$\overline{UB14}$	44	$\overline{CPRST}$	58	PAD15B	72	OAD0	86
$\overline{DSCRD}$	3	$\overline{IN03}$	17	$\overline{GOIRP2}$	31	$\overline{UB11}$	45	PLS5C	59	PAD14	73	$\overline{CLK}$	87
$\overline{DMAWM}$	4	$\overline{IN04}$	18	$\overline{GOIRP3}$	32	$\overline{UB12}$	46	PLS5D	60	PAD13	74	ODOIO	88
$\overline{IN15}$	5	$\overline{UADS}$	19	$\overline{GOIRP4}$	33	$\overline{UB09}$	47	$\overline{DTC}$	61	$\overline{PAD12}$	75	OSNS	89
$\overline{DSCR}$	6	$\overline{DSCRC1}$	20	MRKP	34	$\overline{UB10}$	48		62	PAD11	76	OSET	90
$\overline{IN13}$	7	$\overline{DSCRC2}$	21	IRPTP	35	GNDC	49	$\overline{RMRK}$	63	RMDLY	77	BUFSN	91
$\overline{IN14}$	8	$\overline{DSCRC3}$	22	$\overline{CK2MS}$	36	GNDD	50	$\overline{SMRK}$	64	NABLX	78	RQSTDX	92
$\overline{IN11}$	9	$\overline{DSCRC4}$	23	RSTB	37	$\overline{UB07}$	51	$\overline{BIOIO}$	65	OAD7	79	CLKEV	93
$\overline{IN12}$	10	$\overline{LIDL}$	24	$\overline{CYST}$	38	$\overline{UB08}$	52	$\overline{BXOD}$	66	OAD6	80	CLKOD	94
$\overline{IN09}$	11	$\overline{C1WRT}$	25	PLS5A	39	$\overline{UB05}$	53	BXOD	67	IRPX	81		95
$\overline{IN10}$	12	$\overline{C2WRT}$	26	PLS5B	40	$\overline{UB06}$	54	EVPULS	68	OAD4	82		96
$\overline{IN07}$	13	$\overline{C3WRT}$	27	$\overline{UB15}$	41	$\overline{UB03}$	55	DMAX	69	OAD3	83	GNDE	97
$\overline{IN08}$	14	$\overline{C4WRT}$	28	$\overline{UB16}$	42	$\overline{UB04}$	56	PGRP	70	OAD2	84	GNDF	98

NOTE: Pin 35 signal becomes MRKP if power interrupt is used.
Pin 61 signal becomes $\overline{DT1}$ if DMA1 is used.
Pin 61 signal becomes $\overline{DT2}$ if DMA1 and DMA2 are used.
Pin 61 signal becomes $\overline{DT3}$ if DMA1, DMA2, and DMA3 are used.
Pin 61 signal becomes $\overline{DT4}$ if DMA1, DMA2, DMA3, and DMA4 are used.

Table A-4. DMA Channel 1 Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{IN05}$	15	OUT07	29	$\overline{UB13}$	43	$\overline{UB02}$	57	C1AD7	71	OAD1	85
GNDB	2	$\overline{IN06}$	16	OUT08	30	$\overline{UB14}$	44	RMDLY	58	C1AD6	72	OAD0	86
$\overline{DSCRD}$	3	$\overline{IN03}$	17	OUT05	31	$\overline{UB11}$	45	PLS5C	59	C1AD5	73	$\overline{CLK}$	87
$\overline{DMAWM}$	4	$\overline{IN04}$	18	OUT06	32	$\overline{UB12}$	46	PLS5D	60	C1AD4	74	ODOIO	88
$\overline{IN15}$	5	$\overline{IN01}$	19	OUT03	33	$\overline{UB09}$	47	$\overline{BIOIO}$	61	C1AD3	75	BUFSN	89
$\overline{IN16}$	6	$\overline{IN02}$	20	OUT04	34	$\overline{UB10}$	48	$\overline{DT1}$	62	C1AD2	76	OSET	90
$\overline{IN13}$	7	OUT15	21	OUT01	35	GND	49	$\overline{C1WRT}$	63	C1AD1	77	OPOP	91
$\overline{IN14}$	8	OUT16	22	OUT02	36	GND	50	$\overline{DSCRC1}$	64	C1AD0	78	OPIP	92
$\overline{IN11}$	9	OUT13	23	RSTB	37	$\overline{UB07}$	51	$\overline{BIOIO}$	65	OAD7	79	CLKEV	93
$\overline{IN12}$	10	OUT14	24	$\overline{CYST}$	38	$\overline{UB08}$	52	BXOD	66	OAD6	80	CLKOD	94
$\overline{IN09}$	11	OUT11	25	PLS5A	39	$\overline{UB05}$	53	$\overline{BXOD}$	67	OAD5	81	$\overline{D1RDY}$	95
$\overline{IN10}$	12	OUT12	26	PLS5B	40	$\overline{UB06}$	54	EVPULS	68	OAD4	82		96
$\overline{IN07}$	13	OUT09	27	$\overline{UB15}$	41	$\overline{UB03}$	55	BF1IN	69	OAD3	83	GNDE	97
$\overline{IN08}$	14	OUT10	28	$\overline{UB16}$	42	$\overline{UB04}$	56	BF1OT	70	OAD2	84	GNDF	98

Table A-5. DMA Channel 2 Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29	$\overline{\text{UB13}}$	43	$\overline{\text{UB02}}$	57	C2AD7	71	OAD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30	$\overline{\text{UB14}}$	44	RMDLY	58	C2AD6	72	OAD0	86
$\overline{\text{DSCRD}}$	3	$\overline{\text{IN03}}$	17	OUT05	31	$\overline{\text{UB11}}$	45	PLS5C	59	C2AD5	73	$\overline{\text{CLK}}$	87
$\overline{\text{DMAWM}}$	4	$\overline{\text{IN04}}$	18	OUT06	32	$\overline{\text{UB12}}$	46	PLS5D	60	C2AD4	74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33	$\overline{\text{UB09}}$	47	$\overline{\text{DT1}}$	61	C2AD3	75	BUFSN	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34	$\overline{\text{UB10}}$	48	$\overline{\text{DT2}}$	62	C2AD2	76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GND	49	$\overline{\text{C2WRT}}$	63	C2AD1	77	OPOP	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GND	50	$\overline{\text{DSCRC2}}$	64	C2AD0	78	OPIP	92
$\overline{\text{IN11}}$	9	OUT13	23	RSTB	37	$\overline{\text{UB07}}$	51	$\overline{\text{BIOIO}}$	65	OAD7	79	CLKEV	93
$\overline{\text{IN12}}$	10	OUT14	24	$\overline{\text{CYST}}$	38	$\overline{\text{UB08}}$	52	BXOD	66	OAD6	80	CLKOD	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39	$\overline{\text{UB05}}$	53	$\overline{\text{BXOD}}$	67	OAD5	81	$\overline{\text{D2RDY}}$	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40	$\overline{\text{UB06}}$	54	EVPULS	68	OAD4	82		96
$\overline{\text{IN07}}$	13	OUT09	27	$\overline{\text{UB15}}$	41	$\overline{\text{UB03}}$	55	BF2IN	69	OAD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28	$\overline{\text{UB16}}$	42	$\overline{\text{UB04}}$	56	BF2OT	70	OAD2	84	GNDF	98

Table A-6. DMA Channel 3 Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29	$\overline{\text{UB13}}$	43	$\overline{\text{UB02}}$	57	C3AD7	71	OAD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30	$\overline{\text{UB14}}$	44	RMDLY	58	C3AD6	72	OAD0	86
$\overline{\text{DSCRD}}$	3	$\overline{\text{IN03}}$	17	OUT05	31	$\overline{\text{UB11}}$	45	PLS5C	59	C3AD5	73	$\overline{\text{CLK}}$	87
$\overline{\text{DMAWM}}$	4	$\overline{\text{IN04}}$	18	OUT06	32	$\overline{\text{UB12}}$	46	PLS5D	60	C3AD4	74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33	$\overline{\text{UB09}}$	47	$\overline{\text{DT2}}$	61	C3AD3	75	BUFSN	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34	$\overline{\text{UB10}}$	48	$\overline{\text{DT3}}$	62	C3AD2	76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49	$\overline{\text{C3WRT}}$	63	C3AD1	77	OPOP	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50	$\overline{\text{DSCRC3}}$	64	C3AD0	78	OPIP	92
$\overline{\text{IN11}}$	9	OUT13	23	RSTB	37	$\overline{\text{UB07}}$	51	$\overline{\text{BIOIO}}$	65	OAD7	79	CLKEV	93
$\overline{\text{IN12}}$	10	OUT14	24	$\overline{\text{CYST}}$	38	$\overline{\text{UB08}}$	52	BXOD	66	$\overline{\text{OAD6}}$	80	CLKOD	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39	$\overline{\text{UB05}}$	53	$\overline{\text{BXOD}}$	67	OAD5	81	$\overline{\text{D3RDY}}$	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40	$\overline{\text{UB06}}$	54	EVPULS	68	OAD4	82		96
$\overline{\text{IN07}}$	13	OUT09	27	$\overline{\text{UB15}}$	41	$\overline{\text{UB03}}$	55	BF3IN	69	OAD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28	$\overline{\text{UB16}}$	42	$\overline{\text{UB04}}$	56	BF3OT	70	OAD2	84	GNDF	98

Table A-7. DMA Channel 4 Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29	$\overline{\text{UB13}}$	43	$\overline{\text{UB02}}$	57	C4AD7	71	OAD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30	$\overline{\text{UB14}}$	44	RMDLY	58	C4AD6	72	OAD0	86
$\overline{\text{DSCRD}}$	3	$\overline{\text{IN03}}$	17	OUT05	31	$\overline{\text{UB11}}$	45	PLS5C	59	C4AD5	73	$\overline{\text{CLK}}$	87
$\overline{\text{DMAWM}}$	4	$\overline{\text{IN04}}$	18	OUT06	32	$\overline{\text{UB12}}$	46	PLS5D	60	C4AD4	74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33	$\overline{\text{UB09}}$	47	$\overline{\text{DT3}}$	61	C4AD3	75	BUFSN	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34	$\overline{\text{UB10}}$	48	$\overline{\text{DT4}}$	62	C4AD2	76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49	$\overline{\text{C4WRT}}$	63	C4AD1	77	OPOP	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50	$\overline{\text{DSCRC4}}$	64	C4AD0	78	OPIP	92
$\overline{\text{IN11}}$	9	OUT13	23	RSTB	37	$\overline{\text{UB07}}$	51	$\overline{\text{BIOIO}}$	65	OAD7	79	CLKEV	93
$\overline{\text{IN12}}$	10	OUT14	24	$\overline{\text{CYST}}$	38	$\overline{\text{UB08}}$	52	BXOD	66	OAD6	80	CLKOD	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39	$\overline{\text{UB05}}$	53	$\overline{\text{BXOD}}$	67	OAD5	81	$\overline{\text{D4RDY}}$	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40	$\overline{\text{UB06}}$	54	EVPULS	68	OAD4	82		96
$\overline{\text{IN07}}$	13	OUT09	27	$\overline{\text{UB15}}$	41	$\overline{\text{UB03}}$	55	BF4IN	69	OAD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28	$\overline{\text{UB16}}$	42	$\overline{\text{UB04}}$	56	BF4OT	70	OAD2	84	GNDF	98

Table A-8. Interrupt Group 1 (Levels 1-8) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IRPT05}}$	15	OUT07	29	$\overline{\text{MT08}}$	43	$\overline{\text{MT02}}$	57	ARM01	71		85
GNDB	2	$\overline{\text{IRPT04}}$	16	OUT08	30	BI1	44	$\overline{\text{MT03}}$	58	ARM02	72		86
	3	$\overline{\text{IRPT03}}$	17	OUT05	31	$\overline{\text{IT08}}$	45	PLS5C	59	ARM03	73	$\overline{\text{CLK}}$	87
	4	$\overline{\text{IRPT02}}$	18	OUT06	32		46	PLS5D	60	ARM04	74		88
	5	$\overline{\text{IRPT01}}$	19	OUT03	33		47	$\overline{\text{MT04}}$	61	ARM05	75		89
PAD15A	6		20	OUT04	34		48	$\overline{\text{MT05}}$	62	ARM06	76		90
PAD13	7	$\overline{\text{IT01}}$	21	OUT01	35	GNDC	49	$\overline{\text{MT06}}$	63	ARM07	77	OPOP	91
PAD14	8	$\overline{\text{IT02}}$	22	OUT02	36	GNDD	50	$\overline{\text{MT07}}$	64	ARM08	78		92
	9	$\overline{\text{IT03}}$	23	RSTB	37		51		65	OAD7	79		93
	10	$\overline{\text{IT04}}$	24		38	$\overline{\text{SMRK}}$	52	BXOD	66		80	CLKOD	94
	11	$\overline{\text{IT05}}$	25	PLS5A	39	$\overline{\text{RMRK}}$	53	BI1	67	OAD5	81		95
$\overline{\text{IRPT08}}$	12	$\overline{\text{IT06}}$	26	PLS5B	40	$\overline{\text{GOIRP1}}$	54	PGRP	68		82		96
$\overline{\text{IRPT07}}$	13	$\overline{\text{IT07}}$	27		41		55		69		83	GNDE	97
$\overline{\text{IRPT06}}$	14		28	BI1	42	$\overline{\text{MT01}}$	56		70		84	GNDF	98

Table A-9. Interrupt Group 2 (Levels 9-16) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IRPT13}}$	15	OUT15	29	$\overline{\text{MT16}}$	43	$\overline{\text{MT10}}$	57	ARM09	71		85
GNDB	2	$\overline{\text{IRPT12}}$	16	OUT16	30	$\overline{\text{IT08}}$	44	$\overline{\text{MT11}}$	58	ARM10	72		86
	3	$\overline{\text{IRPT11}}$	17	OUT13	31	$\overline{\text{IT16}}$	45	PLS5C	59	ARM11	73	$\overline{\text{CLK}}$	87
	4	$\overline{\text{IRPT10}}$	18	OUT14	32		46	PLS5D	60	ARM12	74		88
	5	$\overline{\text{IRPT09}}$	19	OUT11	33		47	$\overline{\text{MT12}}$	61	ARM13	75		89
PAD15B	6		20	OUT12	34		48	$\overline{\text{MT13}}$	62	ARM14	76		90
PAD13	7	$\overline{\text{IT09}}$	21	OUT09	35	GNDC	49	$\overline{\text{MT14}}$	63	ARM15	77	OPOP	91
PAD14	8	$\overline{\text{IT10}}$	22	OUT10	36	GNDD	50	$\overline{\text{MT15}}$	64	ARM16	78		92
	9	$\overline{\text{IT11}}$	23	RSTB	37		51		65	OAD7	79		93
PAD12	10	$\overline{\text{IT12}}$	24		38	$\overline{\text{SMRK}}$	52	BXOD	66		80	CLKOD	94
	11	$\overline{\text{IT13}}$	25	PLS5A	39	$\overline{\text{RMRK}}$	53	BI2	67	OAD5	81		95
$\overline{\text{IRPT16}}$	12	$\overline{\text{IT14}}$	26	PLS5B	40	$\overline{\text{GOIRP2}}$	54	PGRP	68		82		96
$\overline{\text{IRPT15}}$	13	$\overline{\text{IT15}}$	27		41		55		69		83	GNDE	97
$\overline{\text{IRPT14}}$	14		28	$\overline{\text{MT08}}$	42	$\overline{\text{MT09}}$	56		70		84	GNDF	98

Table A-10. Interrupt Group 3 (Levels 17-24) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IRPT21}}$	15	OUT07	29	$\overline{\text{MT24}}$	43	$\overline{\text{MT18}}$	57	ARM17	71		85
GNDB	2	$\overline{\text{IRPT20}}$	16	OUT08	30	$\overline{\text{IT16}}$	44	$\overline{\text{MT19}}$	58	ARM18	72		86
	3	$\overline{\text{IRPT19}}$	17	OUT05	31	$\overline{\text{IT24}}$	45	PLS5C	59	ARM19	73	$\overline{\text{CLK}}$	87
	4	$\overline{\text{IRPT18}}$	18	OUT06	32		46	PLS5D	60	ARM20	74		88
	5	$\overline{\text{IRPT17}}$	19	OUT03	33		47	$\overline{\text{MT20}}$	61	ARM21	75		89
PAD15A	6		20	OUT04	34		48	$\overline{\text{MT21}}$	62	ARM22	76		90
PAD13	7	$\overline{\text{IT17}}$	21	OUT01	35	GNDC	49	$\overline{\text{MT22}}$	63	ARM23	77	OPOP	91
PAD14	8	$\overline{\text{IT18}}$	22	OUT02	36	GNDD	50	$\overline{\text{MT23}}$	64	ARM24	78		92
PAD11	9	$\overline{\text{IT19}}$	23	RSTB	37		51		65	OAD7	79		93
	10	$\overline{\text{IT20}}$	24		38	$\overline{\text{SMRK}}$	52	BXOD	66		80	CLKOD	94
	11	$\overline{\text{IT21}}$	25	PLS5A	39	$\overline{\text{RMRK}}$	53	BI3	67	OAD5	81		95
$\overline{\text{IRPT24}}$	12	$\overline{\text{IT22}}$	26	PLS5B	40	$\overline{\text{GOIRP3}}$	54	PGRP	68		82		96
$\overline{\text{IRPT23}}$	13	$\overline{\text{IT23}}$	27		41		55		69		83	GNDE	97
$\overline{\text{IRPT22}}$	14		28	$\overline{\text{MT16}}$	42	$\overline{\text{MT17}}$	56		70		84	GNDF	98

Table A-11. Interrupt Group 4 (Levels 25-32) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IRPT29}}$	15	OUT07	29	$\overline{\text{MT32}}$	43	$\overline{\text{MT26}}$	57	ARM25	71		85
GNDB	2	$\overline{\text{IRPT28}}$	16	OUT08	30	$\overline{\text{IT24}}$	44	$\overline{\text{MT27}}$	58	ARM26	72		86
	3	$\overline{\text{IRPT27}}$	17	OUT05	31	$\overline{\text{IT32}}$	45	PLS5C	59	ARM27	73	$\overline{\text{CLK}}$	87
	4	$\overline{\text{IRPT26}}$	18	OUT06	32		46	PLS5D	60	ARM28	74		88
	5	$\overline{\text{IRPT25}}$	19	OUT03	33		47	$\overline{\text{MT28}}$	61	ARM29	75		89
PAD15B	6		20	OUT04	34		48	$\overline{\text{MT29}}$	62	ARM30	76		90
PAD13	7	$\overline{\text{IT25}}$	21	OUT01	35	GNDC	49	$\overline{\text{MT30}}$	63	ARM31	77	OPOP	91
PAD14	8	$\overline{\text{IT26}}$	22	OUT02	36	GNDD	50	$\overline{\text{MT31}}$	64	ARM32	78		92
	9	$\overline{\text{IT27}}$	23	RSTB	37		51		65	OAD7	79		93
PAD12	10	$\overline{\text{IT28}}$	24		38	$\overline{\text{SMRK}}$	52	BXOD	66		80	CLKOD	94
	11	$\overline{\text{IT29}}$	25	PLS5A	39	$\overline{\text{RMRK}}$	53	BI4	67	OAD5	81		95
$\overline{\text{IRPT32}}$	12	$\overline{\text{IT30}}$	26	PLS5B	40	$\overline{\text{GOIRP4}}$	54	PGRP	68		82		96
$\overline{\text{IRPT31}}$	13	$\overline{\text{IT31}}$	27		41		55		69		83	GNDE	97
$\overline{\text{IRPT30}}$	14		28	$\overline{\text{MT24}}$	42	$\overline{\text{MT25}}$	56		70		84	GNDF	98

Table A-12. I/O Connector Card Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29		43		57		71	OAD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30		44		58		72	OAD0	86
	3	$\overline{\text{IN03}}$	17	OUT05	31		45	PLS5C	59		73		87
$\overline{\text{DSCR}}$	4	$\overline{\text{IN04}}$	18	OUT06	32		46	PLS5D	60		74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33		47		61		75	OSNS	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34		48		62		76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49		63		77	OPOP	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50		64	$\overline{\text{BCLK}}$	78	OPIP	92
$\overline{\text{IN11}}$	9	OUT13	23		37		51		65	OAD7	79	$\overline{\text{PRST}}$	93
$\overline{\text{IN12}}$	10	OUT14	24		38		52		66	OAD6	80	$\overline{\text{CPRST}}$	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39		53		67	OAD5	81		95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40		54		68	OAD4	82		96
$\overline{\text{IN07}}$	13	OUT09	27		41		55		69	OAD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28		42		56		70	OAD2	84	GNDF	98

Table A-13. Controller Card (DMA Channel 1 Controlled) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29		43		57		71	C1AD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30		44		58		72	C1AD0	86
	3	$\overline{\text{IN03}}$	17	OUT05	31		45	PLS5C	59		73		87
$\overline{\text{DSCRC1}}$	4	$\overline{\text{IN04}}$	18	OUT06	32		46	PLS5D	60		74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33		47		61		75	BUFSN	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34		48		62		76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49	$\overline{\text{C1WRT}}$	63		77	BF1OT	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50		64	$\overline{\text{BCLK}}$	78	BF1IN	92
$\overline{\text{IN11}}$	9	OUT13	23		37		51		65	C1AD7	79	$\overline{\text{PRST}}$	93
$\overline{\text{IN12}}$	10	OUT14	24		38		52		66	C1AD6	80	$\overline{\text{CPRST}}$	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39		53		67	C1AD5	81	PLS24VA	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40		54		68	C1AD4	82	PLS24VB	96
$\overline{\text{IN07}}$	13	OUT09	27		41		55		69	C1AD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28		42		56		70	C1AD2	84	GNDF	98

Table A-14. Controller Card (DMA Channel 2 Controlled) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29		43		57		71	C2AD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30		44		58		72	C2AD0	86
	3	$\overline{\text{IN03}}$	17	OUT05	31		45	PLS5C	59		73		87
$\overline{\text{DSCRC2}}$	4	$\overline{\text{IN04}}$	18	OUT06	32		46	PLS5D	60		74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33		47		61		75	BUFSN	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34		48		62		76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49	$\overline{\text{C2WRT}}$	63		77	BF2OT	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50		64	$\overline{\text{BCLK}}$	78	BF2IN	92
$\overline{\text{IN11}}$	9	OUT13	23		37		51		65	C2AD7	79	$\overline{\text{PRST}}$	93
$\overline{\text{IN12}}$	10	OUT14	24		38		52		66	C2AD6	80	$\overline{\text{CPRST}}$	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39		53		67	C2AD5	81	PLS24VA	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40		54		68	C2AD4	82	PLS24VB	96
$\overline{\text{IN07}}$	13	OUT09	27		41		55		69	C2AD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28		42		56		70	C2AD2	84	GNDF	98

Table A-15. Controller Card (DMA Channel 3 Controlled) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29		43		57		71	C3AD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30		44		58		72	C3AD0	86
	3	$\overline{\text{IN03}}$	17	OUT05	31		45	PLS5C	59		73		87
$\overline{\text{DSCRC3}}$	4	$\overline{\text{IN04}}$	18	OUT06	32		46	PLS5D	60		74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33		47		61		75	BUFSN	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34		48		62		76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49	$\overline{\text{C3WRT}}$	63		77	BF3OT	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50		64	$\overline{\text{BCLK}}$	78	BF3IN	92
$\overline{\text{IN11}}$	9	OUT13	23		37		51		65	C3AD7	79	$\overline{\text{PRST}}$	93
$\overline{\text{IN12}}$	10	OUT14	24		38		52		66	C3AD6	80	$\overline{\text{CPRST}}$	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39		53		67	C3AD5	81	PLS24VA	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40		54		68	C3AD4	82	PLS24VB	96
$\overline{\text{IN07}}$	13	OUT09	27		41		55		69	C3AD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28		42		56		70	C3AD2	84	GNDF	98

Table A-16. Controller Card (DMA Channel 4 Controlled) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29		43		57		71	C4AD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30		44		58		72	C4AD0	86
	3	$\overline{\text{IN03}}$	17	OUT05	31		45	PLS5C	59		73		87
$\overline{\text{DSCRC4}}$	4	$\overline{\text{IN04}}$	18	OUT06	32		46	PLS5D	60		74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33		47		61		75	BUFSN	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34		48		62		76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49	$\overline{\text{C4WRT}}$	63		77	BF4OT	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50		64	$\overline{\text{BCLK}}$	78	BF4IN	92
$\overline{\text{IN11}}$	9	OUT13	23		37		51		65	C4AD7	79	$\overline{\text{PRST}}$	93
$\overline{\text{IN12}}$	10	OUT14	24		38		52		66	C4AD6	80	$\overline{\text{CPRST}}$	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39		53		67	C4AD5	81	PLS24VA	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40		54		68	C4AD4	82	PLS24VB	96
$\overline{\text{IN07}}$	13	OUT09	27		41		55		69	C4AD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28		42		56		70	C4AD2	84	GNDF	98

Table A-17. Controller Card (Not DMA Controlled) Backplane Signal List

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
GNDA	1	$\overline{\text{IN05}}$	15	OUT07	29		43		57		71	OAD1	85
GNDB	2	$\overline{\text{IN06}}$	16	OUT08	30		44		58		72	OAD0	86
	3	$\overline{\text{IN03}}$	17	OUT05	31		45	PLS5C	59		73		87
$\overline{\text{DSCR}}$	4	$\overline{\text{IN04}}$	18	OUT06	32		46	PLS5D	60		74	ODOIO	88
$\overline{\text{IN15}}$	5	$\overline{\text{IN01}}$	19	OUT03	33		47		61		75	OSNS	89
$\overline{\text{IN16}}$	6	$\overline{\text{IN02}}$	20	OUT04	34		48		62		76	OSET	90
$\overline{\text{IN13}}$	7	OUT15	21	OUT01	35	GNDC	49		63		77	OPOP	91
$\overline{\text{IN14}}$	8	OUT16	22	OUT02	36	GNDD	50		64	$\overline{\text{BCLK}}$	78	OPIP	92
$\overline{\text{IN11}}$	9	OUT13	23		37		51		65	OAD7	79	$\overline{\text{PRST}}$	93
$\overline{\text{IN12}}$	10	OUT14	24		38		52		66	OAD6	80	$\overline{\text{CPRST}}$	94
$\overline{\text{IN09}}$	11	OUT11	25	PLS5A	39		53		67	OAD5	81	PLS24VA	95
$\overline{\text{IN10}}$	12	OUT12	26	PLS5B	40		54		68	OAD4	82	PLS24VB	96
$\overline{\text{IN07}}$	13	OUT09	27		41		55		69	OAD3	83	GNDE	97
$\overline{\text{IN08}}$	14	OUT10	28		42		56		70	OAD2	84	GNDF	98

Table A-18. Connector and Cable Requirements

Connector	Plug Part No.	Manufacturer
J69 (I/O)	00-8016-090-000-703	ELCO Corporation
J70 (I/O)	00-8016-090-000-703	ELCO Corporation
J71 (DMA/IRP)	00-8016-056-000-703	ELCO Corporation
Controller board edge	2VH44/1JN5	Viking Corporation
Cable	**Part No.**	**Manufacturer**
All interface cable	ST-12830-7B-64TW-PR	Spectra-Strip Corporation, P.O. Box 415, Garden Grove, California 92642

Table A-19. Interface Logic Signal Dictionary

Signal	Definition
BF1IN	Signal from DMA channel 1 to controller contained on DMA channel 1 backplane wiring. Signal is true for 1.3 microseconds during execution of Parallel Input instruction.
BF1OT	Signal from DMA channel 1 to controller contained on DMA channel 1 backplane wiring. Signal is true for 860 nanoseconds during execution of Parallel Output instruction.
BUFSN	Signal from DMA channels to controllers contained on DMA backplane wiring and DMA/IRP connector card. Signal goes true coincident with $\overline{\text{BXOD}}$ internal buffer signal when an I/O command is not present. When a Sense instruction is executed, signal goes true coincident with $\overline{\text{OSNS}}$ signal and remains true one clock time after $\overline{\text{OSNS}}$ goes true.
C1AD0 - C1AD7	Address lines from DMA channel 1 to controller contained on DMA channel 1 backplane wiring.
$\overline{\text{C1WRT}}$	Write signal from controller to DMA channel 1. Contained on DMA channel 1 backplane wiring.
$\overline{\text{CK2MS}}$	2-millisecond clock from computer.
$\overline{\text{OMPTY}}$	Memory parity not. Contained on CPU DMA/IRP connector.
CLK	430-nanosecond clock from computer. Contained on CPU DMA/IRP connector.
$\overline{\text{CYSTL}}$	When at ground level, forces a direct memory access to occur. Contained on CPU DMA/IRP connector.
$\overline{\text{CYSTW}}$	Determines whether a direct memory access will be a read or a write function. If line is at ground level, a write operation occurs. Contained on CPU DMA/IRP connector.
$\overline{\text{D1RDY}}$	DMA channel 1 ready signal. New number of words and starting address required during chaining block. Transfer complete after terminating block. Contained on DMA channel 1 backplane wiring.
$\overline{\text{DSCRC1}}$	Discrete controller ready signal from DMA channel 1. Contained on DMA channel 1 backplane wiring.
$\overline{\text{DSCR}}$	Discrete signal from external source to computer. Signal source is selected by address lines $\overline{\text{OAD0}}$ through $\overline{\text{OAD7}}$ and sampled during the Sense instruction. Contained on CPU I/O connector.
$\overline{\text{IRPT02}}$ - $\overline{\text{IRPT32}}$	Interrupt request signals from external devices. Contained on interrupt groups 1-4, backplane wiring.
$\overline{\text{LIDL}}$	Signal goes to ground momentarily when computer leaves idle state. Contained on CPU DMA/IRP connector and DMA/IRP connector card.
OAD0 - OAD7	Eight address lines used to define input/output device when executing an I/O instruction. From CPU I/O connector to DMA/IRP connector card.

Table A-19. Interface Logic Signal Dictionary (Cont.)

Signal	Definition
ODOIO	Signal from computer. Signal is true during last 430 nanoseconds of an I/O instruction. Contained on DMA/IRP connector card.
OIOIO	Signal from computer. Signal is true during last 1.7 microseconds of an I/O instruction. Contained on CPU connectors DMA/IRP and I/O.
OPIP	Signal from computer. Signal is true for 1.3 microseconds during execution of a Parallel Input instruction. From CPU I/O connector to I/O connector card.
OPOP	Signal from computer. Signal is true for 860 nanoseconds during execution of a Parallel Output instruction. From CPU I/O connector to I/O connector card.
ORSTB	Reset signal used to reset DMA channels. From CPU DMA/IRP connector. Becomes signal RSTB on DMA/IRP connector card.
OSET	Signal from computer. Signal is true for 860 nanoseconds during execution of a Set instruction. From CPU I/O connector to I/O connector card.
OSNS	Signal from computer. Signal is true for 1.3 microseconds during execution of the Sense instruction. From CPU I/O connector to I/O connector card.
OUT1 - OUT16	Sixteen data lines from the processor to external equipment. From CPU I/O connector to I/O connector card.
PLUPIN	Pullup signal for the $\overline{\text{UIN}}$ lines. Signal goes false when DMA write memory signal goes false. Contained on CPU DMA/IRP connector.
$\overline{\text{UADS}}$	Signal from DMA/IRP connector. Signal goes to ground level during the memory cycle when a direct memory access is selected. Signal is used to gate DMA address lines in the CPU.
U2 - U16	Direct memory access address lines to the computer. Contained on CPU DMA/IRP connector. Signals originate as $\overline{\text{UB02}}$-$\overline{\text{UB16}}$ at DMA/IRP connector card.
$\overline{\text{UIN1}}$ - $\overline{\text{UIN16}}$	Sixteen data lines from external source into computer. Contained on CPU I/O connector. Signals originate as $\overline{\text{IN01}}$-$\overline{\text{IN16}}$ on DMA cards.
$\overline{\text{XIRP}}$	Interrupt signal from external device. When line goes to ground, processor enters interrupt sequence. Contained on CPU DMA/IRP connector. Signal originates as IRPX at DMA/IRP connector card.
XODD	Defines phase of computer regular clock with respect to memory timing. Contained on CPU DMA/IRP connector. Becomes BXOD on DMA/IRP connector card.
$\overline{\text{PRST}}$	Signal at ground level during power-off and power turn-on sequences. From CPU I/O connector to I/O connector card.
$\overline{\text{YIDL}}$	Shows state of computer when an interrupt is selected. When signal is at ground level, computer is in idle state. Contained on CPU DMA/IRP connector card.

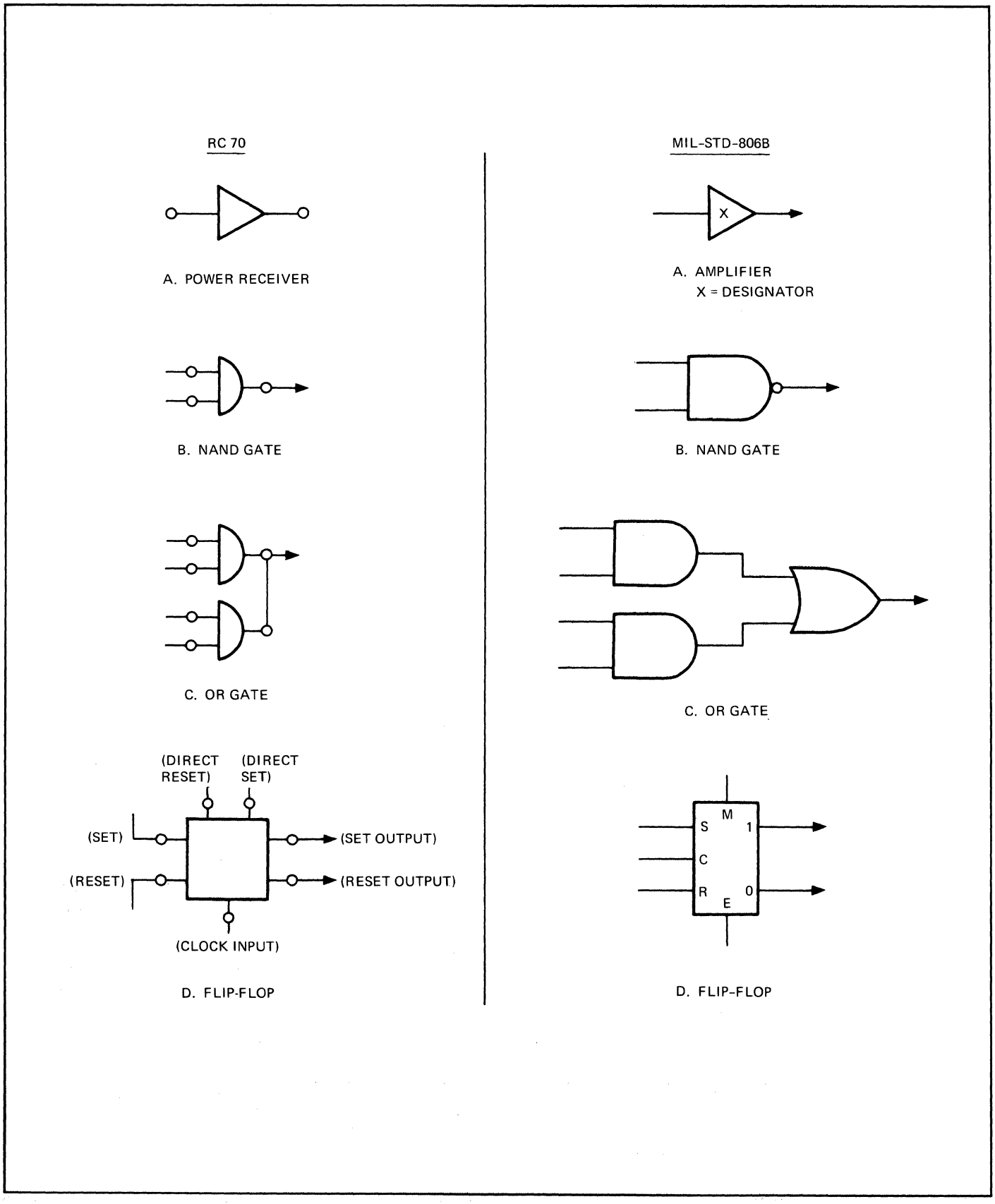


Figure A-1. Logic Symbol Diagram

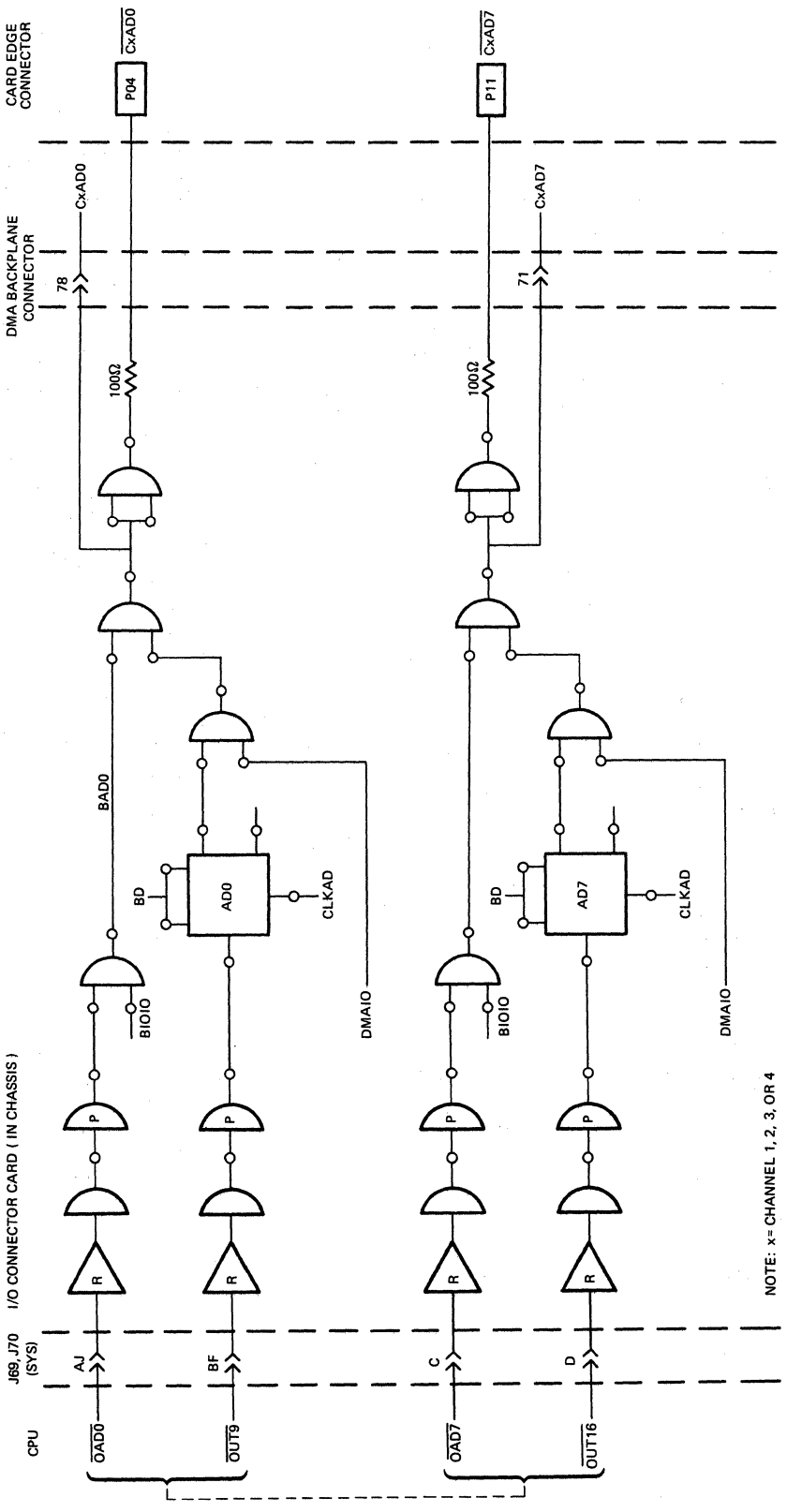


Figure A-2. Address Lines, Interface Logic Diagram

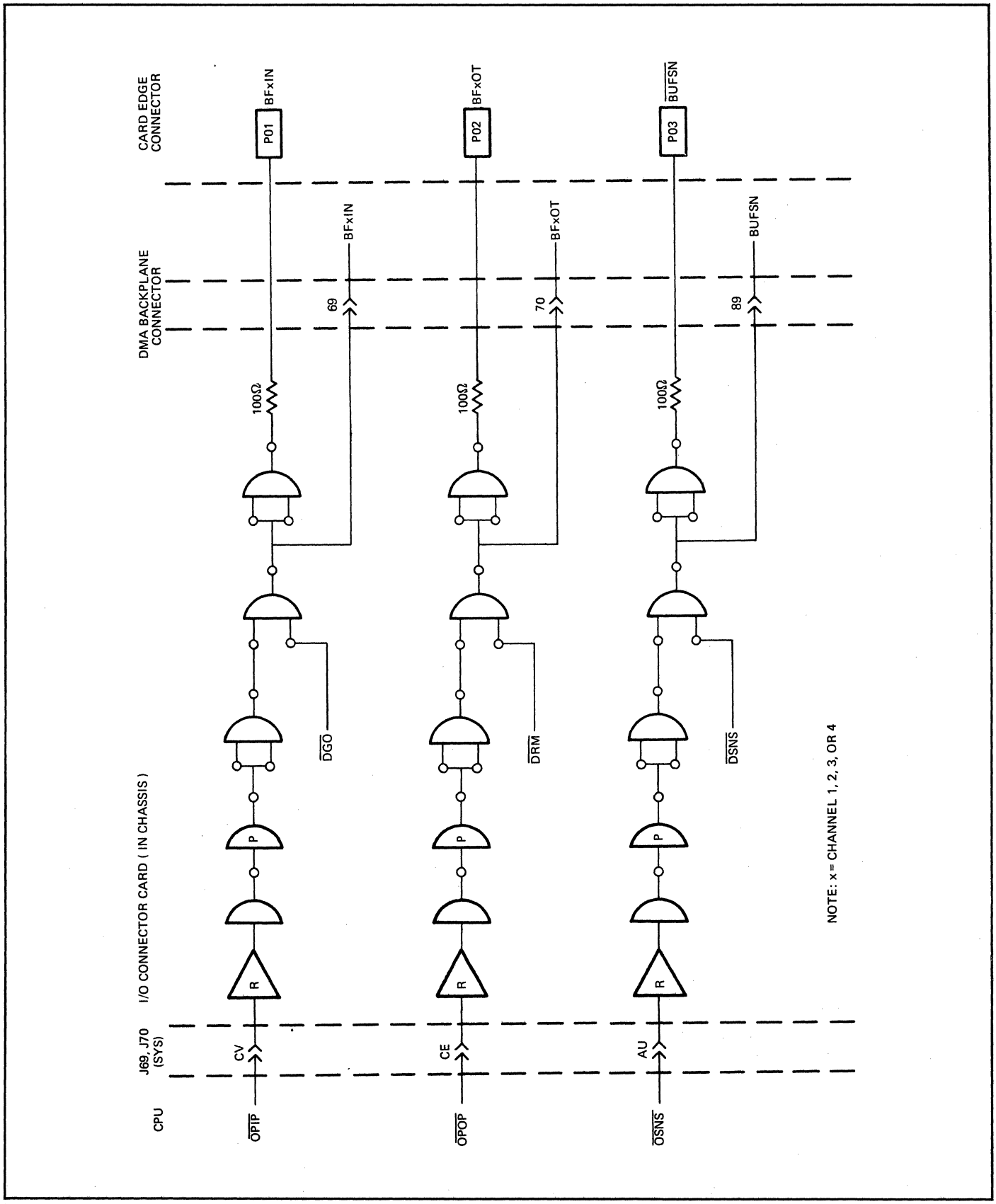


Figure A-3. Operation Signals, Interface Logic Diagram

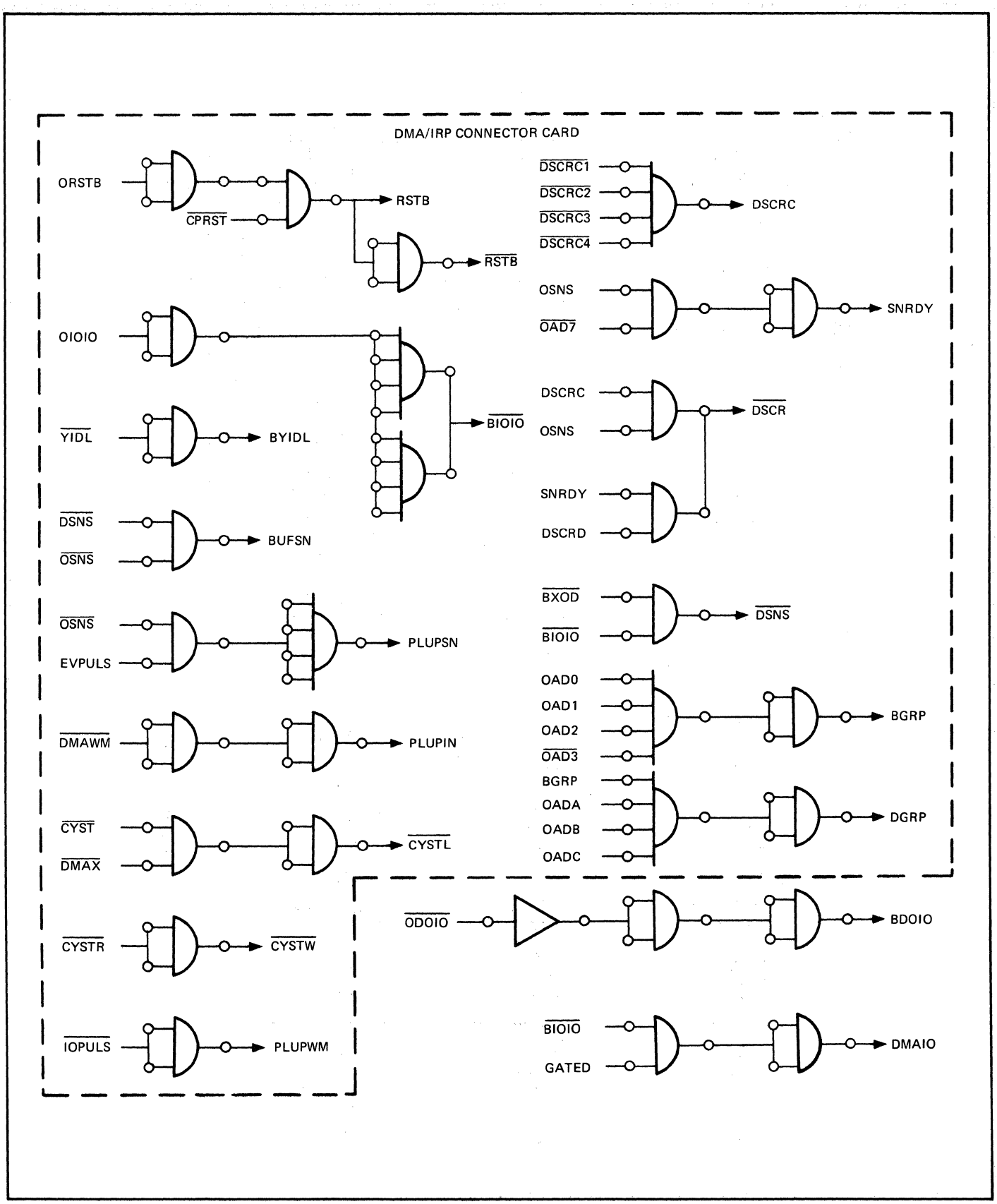


Figure A-4. DMA Channel, Simplified Logic Diagram (Sheet 1 of 5)

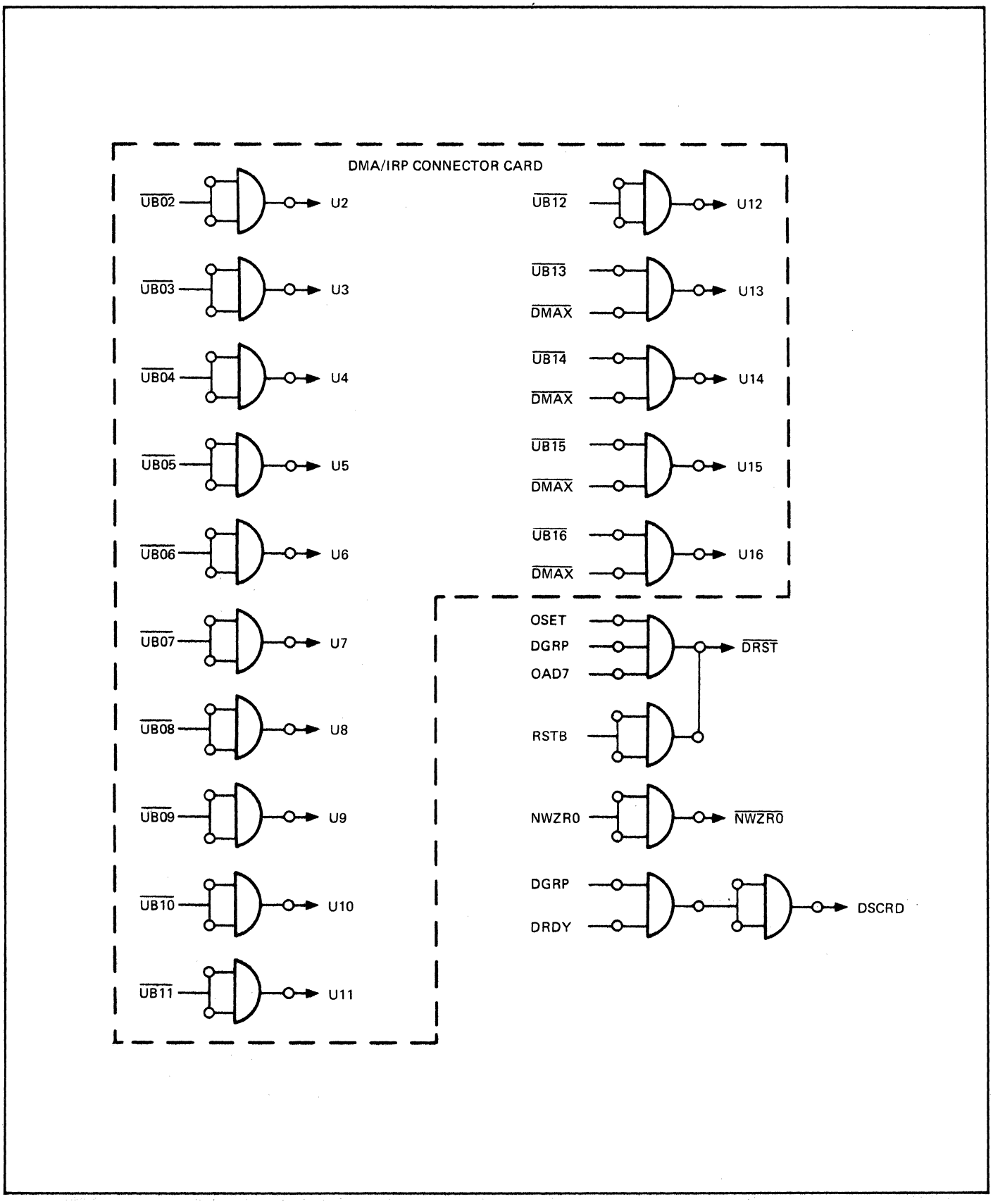


Figure A-4. DMA Channel, Simplified Logic Diagram (Sheet 2 of 5)

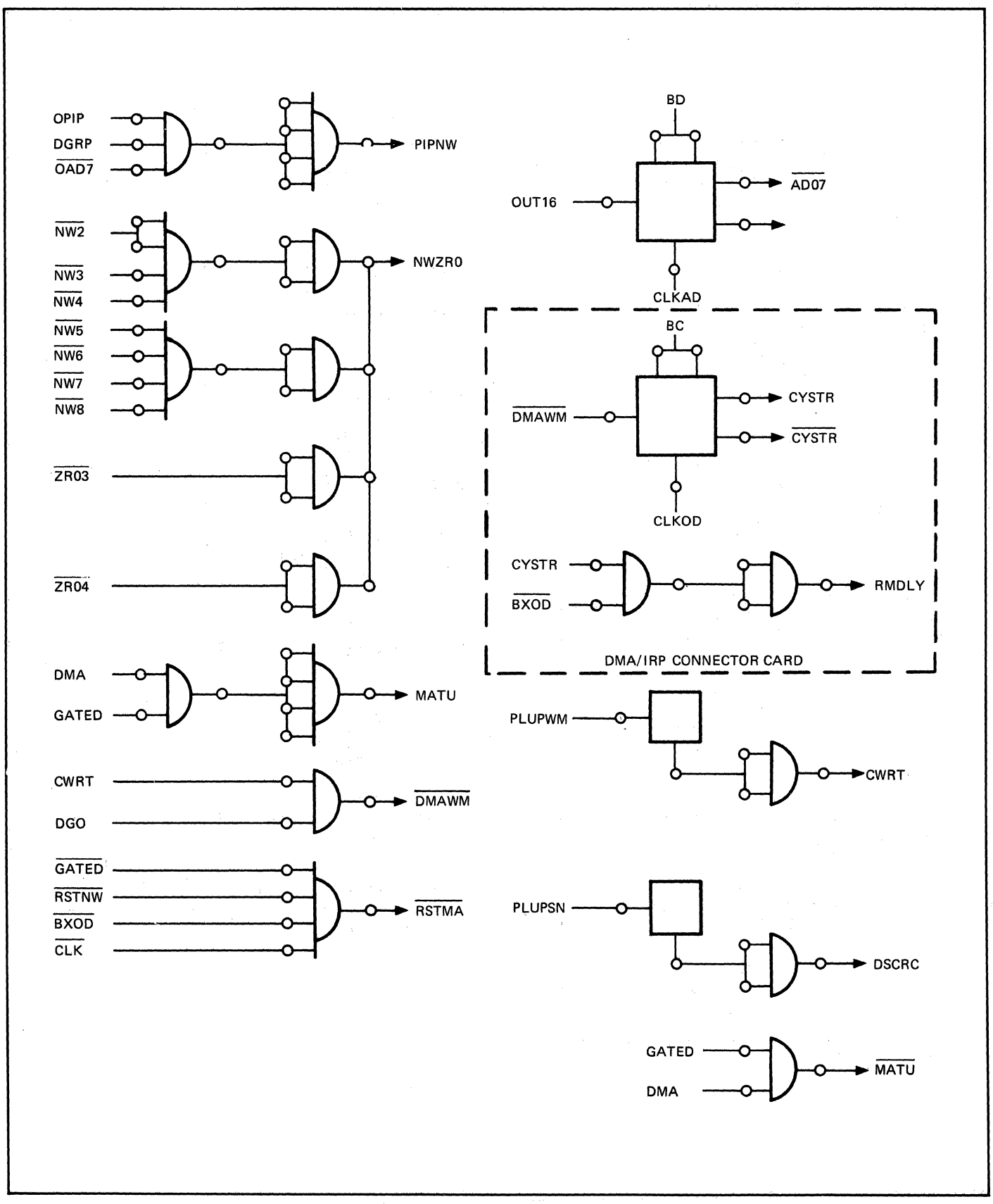


Figure A-4. DMA Channel, Simplified Logic Diagram (Sheet 3 of 5)

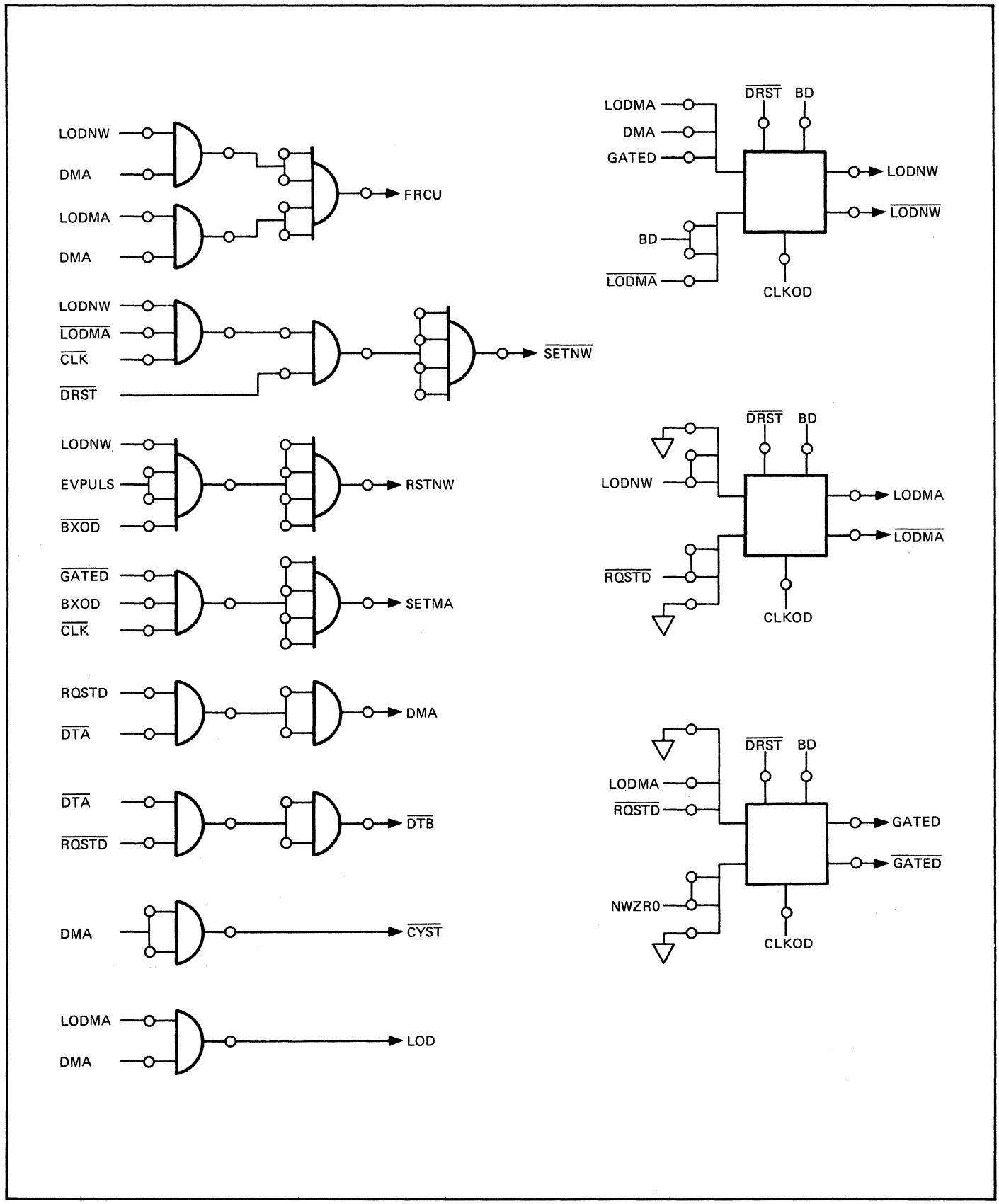


Figure A-4. DMA Channel, Simplified Logic Diagram (Sheet 4 of 5)

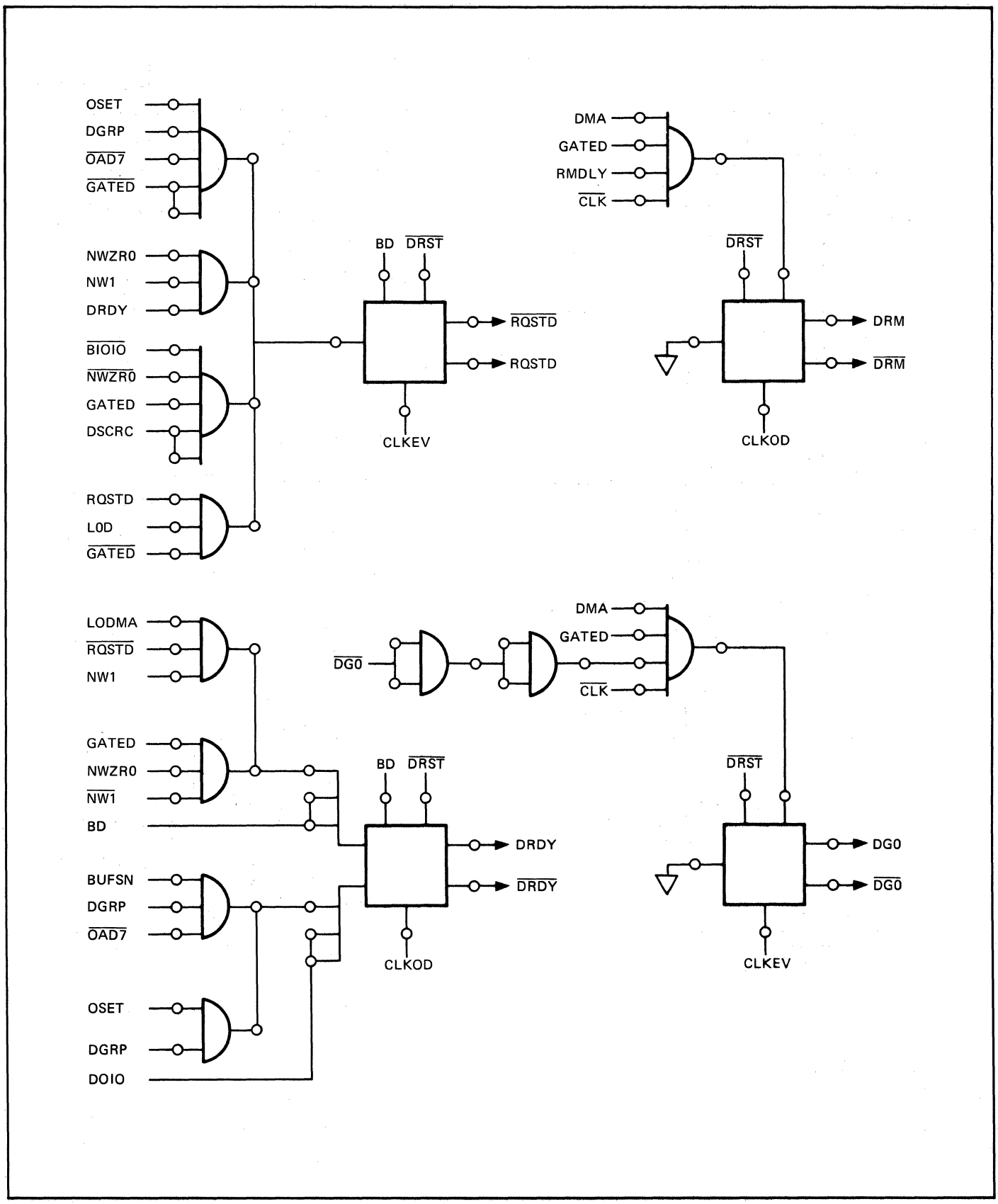
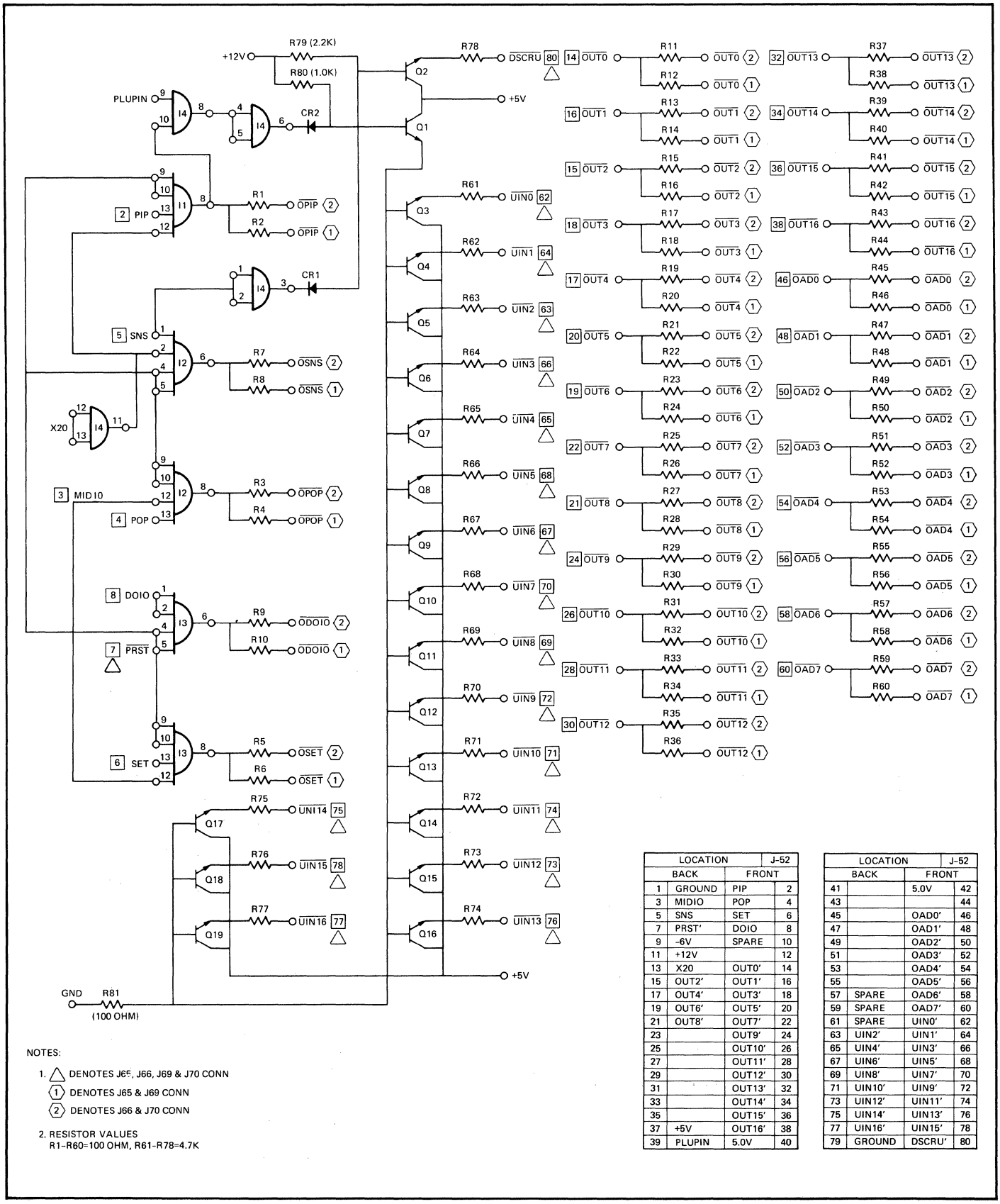


Figure A-4. DMA Channel, Simplified Logic Diagram (Sheet 5 of 5)



LOCATION		J-52	
BACK		FRONT	
1	GROUND	PIP	2
3	MIDIO	POP	4
5	SNS	SET	6
7	PRST'	DOIO	8
9	-6V	SPARE	10
11	+12V		12
13	X20	OUT0'	14
15	OUT2'	OUT1'	16
17	OUT4'	OUT3'	18
19	OUT6'	OUT5'	20
21	OUT8'	OUT7'	22
23		OUT9'	24
25		OUT10'	26
27		OUT11'	28
29		OUT12'	30
31		OUT13'	32
33		OUT14'	34
35		OUT15'	36
37	+5V	OUT16'	38
39	PLUPIN	5.0V	40

LOCATION		J-52	
BACK		FRONT	
41		5.0V	42
43			44
45		OAD0'	46
47		OAD1'	48
49		OAD2'	50
51		OAD3'	52
53		OAD4'	54
55		OAD5'	56
57	SPARE	OAD6'	58
59	SPARE	OAD7'	60
61	SPARE	UIN0'	62
63	UIN2'	UIN1'	64
65	UIN4'	UIN3'	66
67	UIN6'	UIN5'	68
69	UIN8'	UIN7'	70
71	UIN10'	UIN9'	72
73	UIN12'	UIN11'	74
75	UIN14'	UIN13'	76
77	UIN16'	UIN15'	78
79	GROUND	DSCRU'	80

NOTES:

1. △ DENOTES J65, J66, J69 & J70 CONN
   (1) DENOTES J65 & J69 CONN
   (2) DENOTES J66 & J70 CONN
2. RESISTOR VALUES
   R1-R60=100 OHM, R61-R78=4.7K

Figure A-5. CPU I/O Connector Interface (Sheet 1 of 2)

400801-1				400801-2				400801-1				400801-2			
PIN B	CONNS J65X & J66X SIGNAL		PIN A	BRD ROW B&D	CONNS J69 & J70 PIN		BRD ROW A&C	PIN B	CONNS J65Y & J66Y SIGNAL		PIN A	BRD ROW B&D	CONNS J69 & J70 PIN		BRD ROW A&C
1	OPIP'	RETURN	1	1	CY		1	1	OAD0'	RETURN	1	31	AJ	RV	31
2	OPOP'		2	2	CE	BC	2	2	OAD1'		2	32	CK		32
3	OSET'		3	3	BR		3	3	OAD2'		3	33	CX	CB	33
4	OSNS'		4	4	AU		4	4	OAD3'		4	34	CS		34
5	ODOIO'		5	5	AD	F	5	5	OAD4'		5	35	BM		35
6			6	6			6	6	OAD5'		6	36	AR	L	36
7	PRST'		7	7	P		7	7	OAD6'		7	37	AA		37
8	SPARE		3	8	W		8	8	OAD7'		8	38	C		38
9	-6V		9	9	AL	BH	9	9	SPARE	RETURN	9	39	T	BU	39
10	+5V		10	10	AY		10	10	KEY	KEY	10	40	AH		40
11	+12V		11	11	BX		11	11	SPARE	RETURN	11	41	CJ		41
12	SPARE		12	12	CM	CU	12	12	UIN0'		12	42	CV	CA	42
13	OUT0'		13	13	DB		13	13	UIN1'		13	43	CR		43
14	OUT1'		14	14	CD		14	14	UIN2'		14	44	BL		44
15	OUT2'		15	15	BP	AT	15	15	UIN3'		15	45	AP	K	45
16	OUT3'		16	16	BB		16	16	UIN4'		16	46	Z		46
17	OUT4'		17	17	AC		17	17	UIN5'		17	47	B		47
18	OUT5'		18	18	N	V	18	18	UIN6'		18	48	S	AW	48
19	OUT6'		19	19	E		19	19	UIN7'		19	49	AF		49
20	OUT7'		20	20	AK		20	20	UIN8'		20	50	BE		50
21	OUT8'		21	21	AX	BW	21	21	UIN9'		21	51	BT	CX	51
22	OUT9'		22	22	BF		22	22	UIN10'		22	52	CH		52
23	OUT10'		23	23	CL		23	23	UIN11'		23	53	CP		53
24	OUT11'		24	24	DA	CC	24	24	UIN12'		24	54	BZ	BA	54
25	OUT12'		25	25	CT		25	25	UIN13'		25	55	BK		55
26	OUT13'		26	26	BN		26	26	UIN14'		26	56	AN		56
27	OUT14'		27	27	AS	M	27	27	UIN15'		27	57	Y	A	57
28	OUT15'		28	28	AB		28	28	UIN16'		28	58	J		58
29	OUT16'		29	29	D	BV	29	29	DSCRU'		29	59	R	AV	59
30	+5V	RETURN	30	30	U		30	30	SPARE	RETURN	30	60	AE		60

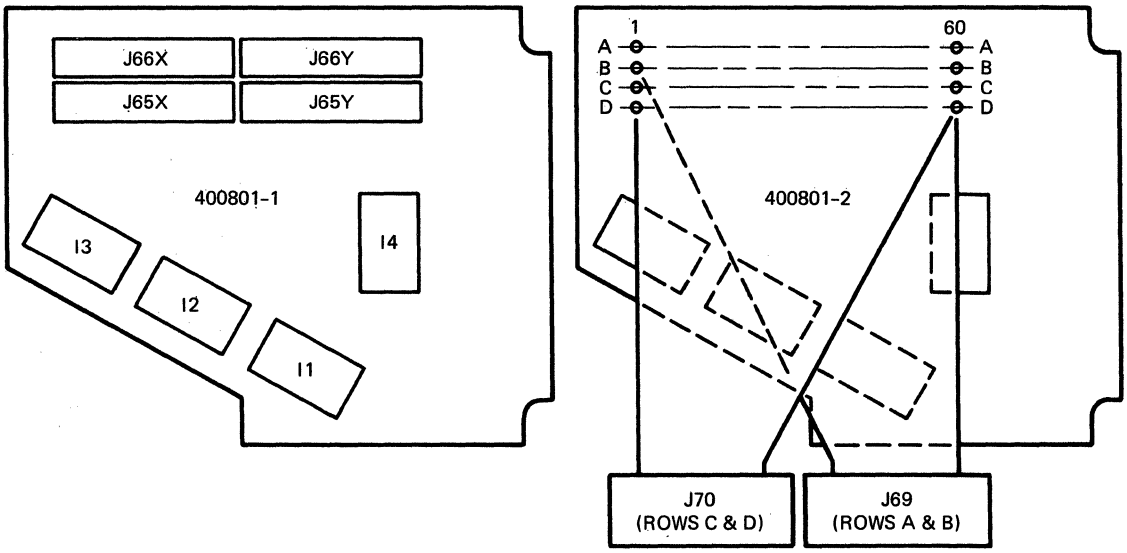
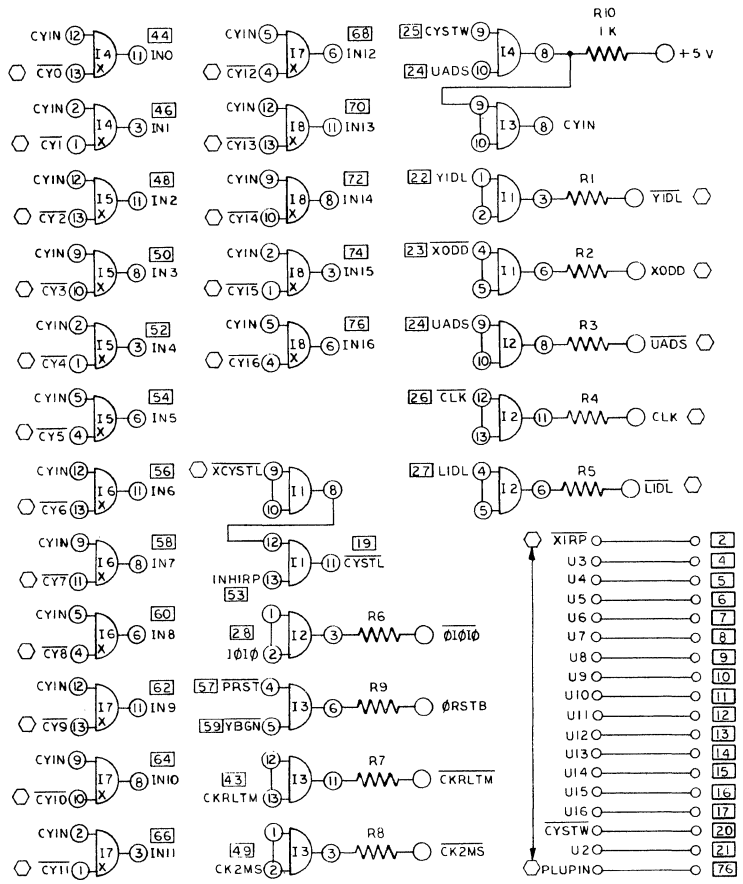


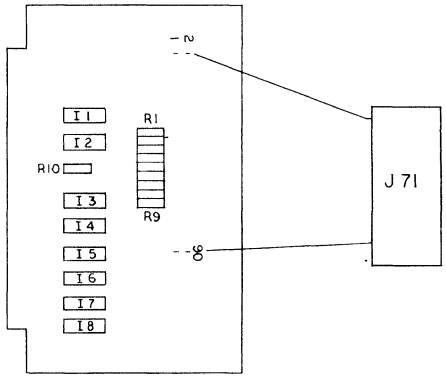
Figure A-5. CPU I/O Connector Interface (Sheet 2 of 2)



FROM CIRCUIT CARD HOLE NO.	SIGNAL	TO ELCO CONN. PIN NO.
1	XIRP'	JJ
3	U3	(v)
5	U4	V
7	U5	(r)
2,4,6,8	RETURN	(d)
9	U6	D
11	U7	K
13	U8	(f)
15	U9	Z
10,12,14,16	RETURN	F
17	U10	CC
19	U11	(j)
21	U12	(m)
23	U13	NN
18,20,22,24	RETURN	(t)
25	U14	HH
27	U15	(C)
29	U16	U
31	CYSTL'	C
26,28,30,32	RETURN	(x)
33	CYSTW'	N
35	U2	E
37	YIDL'	Y
39	XODD	BB
34,36,38,40	RETURN	J
41	UADS'	MM
47	OIOIO'	FF
43	CLK	T
45	LIDL'	H
42,48,44,46	RETURN	(s)
55	CY0'	B
57	CY1'	X
59	CY2'	(r)
61	CY3'	AA
56,58,60,62	RETURN	(w)
63	CY4'	EE
65	CY5'	(v)
67	CY6'	(L)
69	CY7'	S
64,66,68,70	RETURN	M
71	CY8'	F
73	CY9'	A
75	CY10'	W
77	CY11'	(e)
72,74,76,78	RETURN	LL
79	CY12'	(h)
81	CY13'	(z)
83	CY14'	KK
85	CY15'	DD
80,82,84,86	RETURN	(b)
87	CY16'	(k)
89	PLUPIN	(a)
49	CKRLTM'	R
51	CK2MS'	(u)
53	ØRSTB	(p)
88,90,50,52,54	RETURN	L

LOCATION	J. 24	
BACK	FRONT	
GROUND	XIRP'	2
---	U3	4
U4	U5	6
U6	U7	8
U8	U9	10
U10	U11	12
U12	U13	14
U14	U15	16
U16	---	18
CYSTL'	CYSTW'	20
U2	YIDL	22
XODD'	UADS	24
CYSTW	CLK'	26
LIDL	IOIO	28
---	---	30
---	---	32
---	---	34
---	---	36
---	---	38
---	5.0 V.	40

41	---	5.0 V.	42
43	CKRLTM	IN0	44
45	---	IN1	46
47	---	IN2	48
49	CK2MS	IN3	50
51	---	IN4	52
53	INHIRP'	IN5	54
55	---	IN6	56
57	PRST'	IN7	58
59	YBGN'	IN8	60
61	---	IN9	62
63	---	IN10	64
65	---	IN11	66
67	---	IN12	68
69	---	IN13	70
71	---	IN14	72
73	---	IN15	74
75	PLUPIN	IN16	76
77	---	---	78
79	GROUND	---	80



3. ⬡ DENOTES J71 CONN.
2. I1-I3 901011, I4-I8 901006.
1. R1-R9 999101, R10 999102.
NOTES: UNLESS OTHERWISE SPECIFIED.

Figure A-6. CPU DMA/IRP Connector

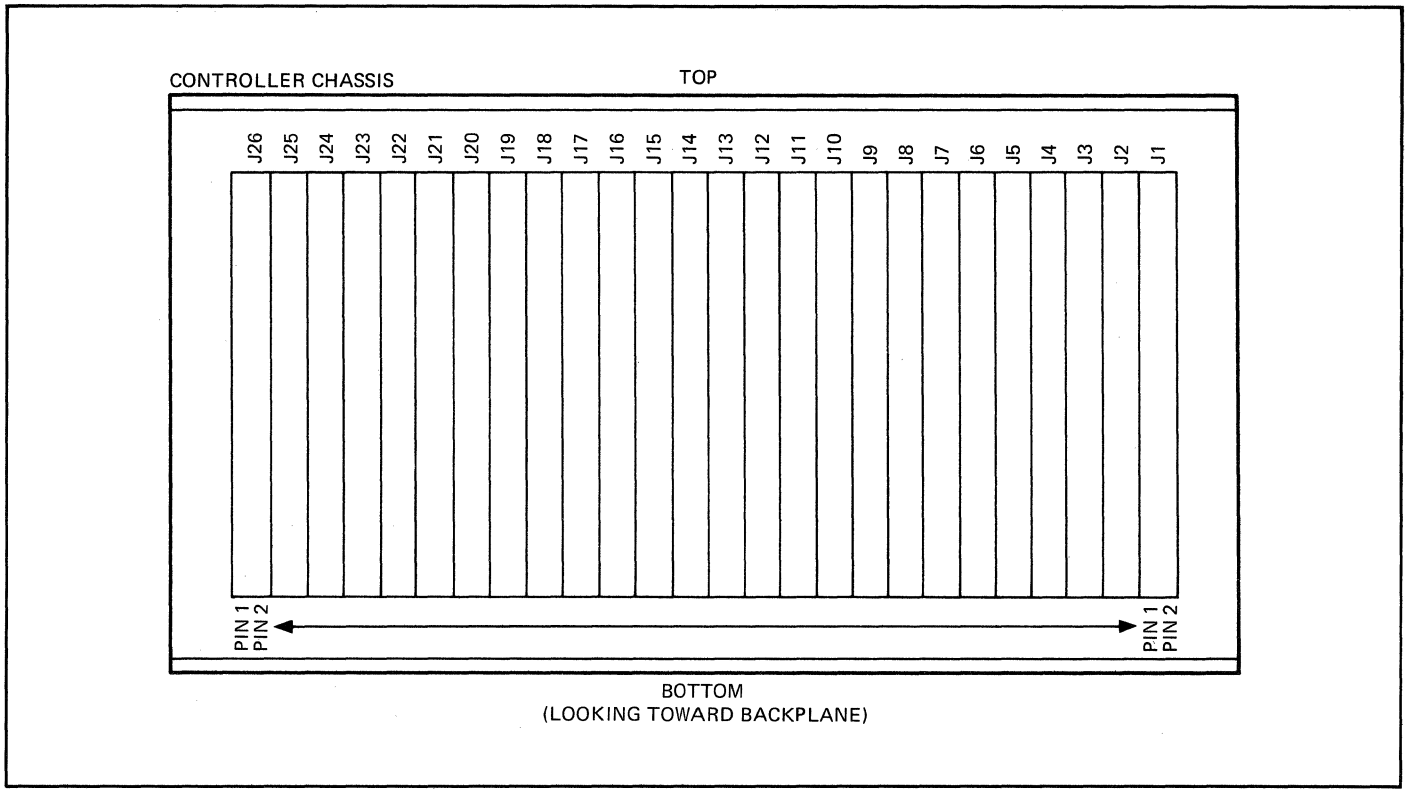


Figure A-7. Controller Chassis