REMEX

TECHNICAL MANUAL

DISKETTE SUBSYSTEM

MODELS: RFS2410, RFS2420
RFS4810, RFS4820

Peripheral Products

Ex-Cell-O Corporation

TECHNICAL MANUAL

DISKETTE SUBSYSTEM

MODELS: RFS2410, RFS2420
RFS4810, RFS4820

IMPORTANT INFORMATION

Changes to the equipment which are made between manual printings are listed in an addendum at the rear of the manual. As a convenience, a list of change pages is given as the last page in the manual. It is recommended that each of these pages be marked "Refer to Addendum" so that these changes can be identified.

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FOR YOUR SAFETY

Before undertaking any maintenance procedure, whether it be a specific trouble-shooting or maintenance procedure described herein or an exploratory procedure aimed at determining whether there has been a malfunction, read the applicable section of this manual and note carefully the

and

contained therein.

The equipment described in this manual contains voltages hazardous to human life and safety and may contain mechanical components capable of inflicting personal injury. The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to the electrical and mechanical hazards and thus prevent personal injury and damage to equipment.

This equipment generates, uses and radiates radio frequency energy and if not installed and used in accordance with the instruction manual, (shielded interface cabling recommended) may cause radio communications interference. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 or FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct this interference.

WARRANTY

SELLER warrants to the original BUYER only that the products will be free from defects in material or workmanship for the following periods, whichever is applicable: (i) Software and firmware products, thirty (30) days from date of shipment; (ii) Punch mechanism products, ninety (90) days from date of shipment; (iii) Flexible disk drives and disk system products, one hundred eighty (180) days from date of shipment; (iv) All other paper tape products, one (1) year from date of shipment; and (v) All other products, ninety (90) days from date of shipment. Any product, or part thereof, which under normal operating conditions proves defective in material or workmanship within the time period applicable to such product, as determined by an inspection by SELLER, will be repaired or replaced, at SELLER'S option, free of charge provided BUYER: (i) Promptly notifies SELLER of the defect; (ii) Returns the defective product to SELLER, transportation prepaid; and (iii) Establishes that the product has been properly installed, maintained, and operated in accordance with SELLER'S instructions or the instructions contained in its operations or maintenance manuals and within the limits of normal usage. SELLER'S warranty as to software and firmware shall be void and of no effect if changes or additions have been made to the software or firmware (or if the software or firmware has been adapted by the BUYER) to serve a function not within the system specifications of SELLER.

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SECTION I

GENERAL DESCRIPTION

1.1 EQUIPMENT DESCRIPTION

This manual has been prepared to assist the user in interfacing, installing, operating and maintaining the RFS2400 and RFS4800 series of Flexible Disk Subsystems. See Figure 1-1. The difference between the RFS2400 and RFS4800 is that the former reads and writes on one side only and the latter reads and writes on both sides. See Section 1.9 and Table 1-3 for a description and listing of the various model numbers.

The subsystem utilizes a built-in microprocessor which controls a single chip LSI formatter and additional SSI/MSI control logic with a REMEX-built flexible disk drive including read/write and control electronics. It offers total media compatibility with the IBM 3740 Data Entry System, the IBM 3540 Diskette I/O unit and the IBM systems 32 and 34 in which diskettes can be read and/or written interchangeably. Having a 1,022K byte, double density (IBM specified MFM) formatted storage capacity for a 26 sector

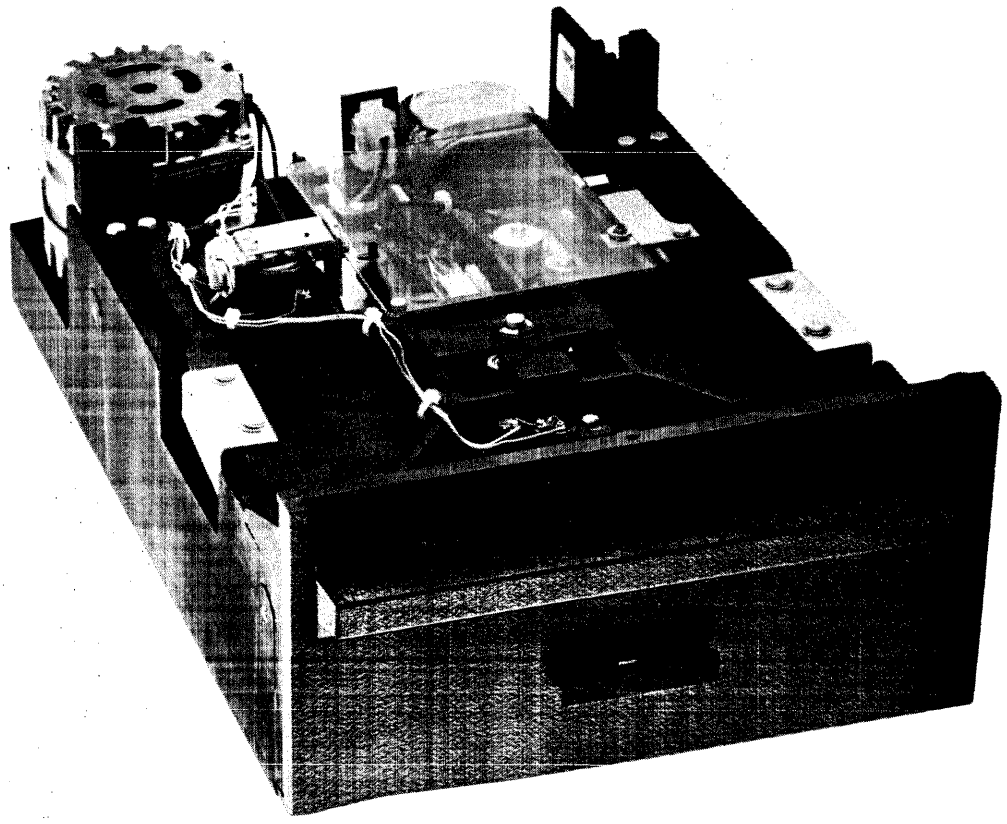


Figure 1-1. RFS4810 Flexible Disk Subsystem. The RFS4820/2410/2420 are identical in appearance in this view.

format when using both sides (1,177K bytes for 15-sector format or 1,255K bytes for 8-sector format), the subsystem provides an ideal random access storage device for microprocessor or minicomputer systems.

The disk drive is a small, portable, direct access storage device which accepts a removable flexible diskette as the storage medium. The drive mechanism consists of a belt driven spindle, spindle motor, read/write head, a split band stepping motor drive mechanism to position the read/write head for track accessing, light emitting diodes and phototransistors for index sensing and write protected media sensing. The printed circuit board provides all the required data signal processing and electronic control functions.

Magnetic data is written on or read from the diskette surface by a read/write head which is positioned to concentric tracks on the diskette surface by means of the stepper motor. The diskette spindle is belt driven at 360RPM by the spindle motor.

The RFS2400 and RFS4800 Series are available in two basic configurations: The RFS2410 or 4810 is the basic master unit with controller and the RFS 2420 or 4820 is the slave unit which contains only drive circuits and read/write electronics. Up to three slaves may be controlled by a single master. Table 1-3 gives the complete model numbers and designation meanings.

1.1.1 RFS48X0 AND 24X0 FEATURES

All units are compatible with the IBM 3740 data entry system, the IBM 3540 diskette I/O unit and the IBM system 32 and 34. Read/write/erase head geometry is identical to that in the IBM diskette drives and the mechanism for positioning the head meets the precise requirements of track location, thereby allowing complete diskette interchangeability.

Interfacing is greatly simplified since only 15 signal lines are used. Eight of these are bidirectional lines which transfer data, status, diskette address and command information. One line is used to control data direction on the 8-bit bidirectional bus. Two lines are used to control the data transfer on the data bus in a handshake mode. Two lines are used to transmit busy and error conditions. One other line is used to unconditionally reset the system.

Fully automatic features include data block transfers, diskette formatting, copy function, head load, track seek, sector search, sector sizing, density switching, and software bootstrap.

Unit select allows bussing of one master and up to three slave drives on a ribbon cable. Unit select circuitry allows the logical unit address of an individual drive to be selected simply by the use of jumper plugs. This feature makes it possible for the user to change a logical drive address without physically interchanging the unit.

An internal buffer is provided to buffer the data transfers between the subsystem and host. The buffer size may be 128, 256, 512 or 1024 bytes as determined by the format being used.

Automatic erase head control eliminates the need for erase gate electronics in the host system.

Gentle media handling is assured by an expandable clutching system. Extended head and media life is made possible by the use of a ceramic head. A "busy" indicator, installed on the front panel, is lit when the head is loaded.

1.2 OPTIONAL EQUIPMENT SUPPLIED

A number of items are available in an optional kit of parts to be used with the disk subsystem for spare parts, installation and maintenance. These are listed in Table 1-1. See Table 7-5 for the REMEX Part numbers for the various Kit of Parts available.

Table 1-1. Optional items available for the RFS4810/4820 and RFS2410/2420 (Kit of Parts)

Item	REMEX Part No.	Quantity RFS2410 RFS4810	Quantity RFS2420 RFS4820
Connector, 34 socket, 3M 3414, (P1)	706510-213	1	-
Connector, 6 pin, Molex 09-50-7061,(P3)	706510-277	1	1
Connector, 26 pin, 3M 3399-6000 (P2)	706510-228	1	1
Connector, Amp 1-480700-0 (P8)	706500-343	1	1
Contact, Female, Molex 08-50-0106 (P3)	706530-137	5	5
Contact, Amp 350550-1 (P8)	706530-176	3	3
Key, Polarizing, 3M 3435-000 (P1,P2)	706540-153	2	1
Key, Polarizing, Molex 15-04-0219 (P3)	706540-149	1	1
Manual	112670-109	1	-

1.3 MAINTENANCE EQUIPMENT REQUIRED BUT NOT SUPPLIED

The maintenance procedures in Section 5 require equipment that is not supplied. This equipment is listed in Table 5-1.

1.4 EQUIPMENT WARRANTY

A statement covering the warranty of this equipment is given on page iii (second page in book). It should be read and understood. All preventive maintenance prodedures must be performed as outlined in Section 5.2. during the warranty period in order that the warranty remain in effect. Any questions arising concerning the warranty should be directed to the REMEX Service Department.

1.5 SPECIFICATIONS

The specifications for the RFS4810/4820/2410/2420 are listed in Table 1-2.

Table 1-2. Specifications for the RFS4810/4820/2410/2420

Characteristic	Specifications				
Capacity/Disk (Double Density)	Format	Standard IBM ①		Modified IBM ②	
		1 Side	2 Side	1 Side	2 Side
	46-Sector ③	447,488	N/A	453,376	906,752
	26-Sector	509,184	1,021,646	512,512	1,025,024
	15-Sector	587,008	1,177,344	591,360	1,182,720
	8-Sector	625,920	1,255,160	630,784	1.261.568
Bytes/Sector	Format	Single Density		Double Density	
	46-Sector ③	—		128	
	26-Sector	128		256	
	15-Sector	256		512	
	8-Sector	512		1024	
Recording Density	Outer Track : 1836 BPI, Single Density 3672 BPI, Double Density Inner Track: 6536 BPI				
Transfer Rate 8-bit byte	Nonbuffered Operation: One byte every 16μs (double density) Buffered Operation: Approximately one byte every 15 to 17 μs, either density.				
Head	Common Read/Write with Tunnel Erase				
Rotational Speed	360RPM ± 2.5%				
Average Latency	83.3 ms				
Access Time	Track to Track: 3ms Settling Time: 15ms Average Access: 91ms, including settling time Maximum Access: 216ms, including settling time				
Head Load Time	35ms				
Number of Tracks	77 each side				
Storage Element	REMEX recommended media only				
Track Density	48 Tracks/Inch				
Temperature	Operating: 40°F to 115°F with media Storage: -30°F to 150°F without media				

① Formatted with Track 00, Side 0, 26 Sector/Trk in Single Density; Track 00, Side 1, 26 Sector/Trk in Double Density.

② Formatted with all tracks double density.

③ This is a unique format that is not specified by IBM.

Table 1-2. Specifications for the RFS4810/4820/2410/2420 continued.

Characteristic	Specifications	
Humidity	Operating: 20 to 80% without condensation. Storage: 5 to 98% without condensation.	
AC Power	100, 115 VAC ± 10%, 50/60Hz ± 0.5 Hz @ 0.4A or 230 VAC ± 10%, 50 Hz ± 0.5 Hz @ 0.2A.	
DC Power Typical	RFD2410/4810 +5Vdc ± 5% @ 1.3A -12Vdc ± 5% @ 0.1A +24Vdc ± 5% @ 0.7A	RFD2420/4820 +5Vdc ± 5% @ 0.5A -12Vdc ± 5% @ 0.1A +24Vdc ± 5% @ 0.5A
Weight	10.5 lbs.	
Outline Dimenisions	See Figure 1-2.	
Reliability	Recoverable Read Error Rate: Less than 1 in 10^9 bits. Unrecoverable Read Error Rate: Less than 1 in 10^{12} bits. Head Life: More than 30,000 hours. Media Life: More than $5x10^6$ passes per track on approved media.	

1.6 DISKETTE

The storage element used is a ferromagnetic coated flexible disk enclosed within a protective plastic jacket. See Figure 1-3 for the one sided diskette and Figure 1-4 for the two sided diskette. The interior of the jacket is lined with a wiping material to clean the disk of contamination. The diskette is always kept in a storage and traveling envelope to further protect the recording surface. Characteristics of the storage element are as follows.

Track Width: 0.014 inch
Track Spacing: 0.02083 inch (48 tracks/inch)
Disk Diameter: 7.875 inches
Envelope Size: 8 X 8 inches

1.7 RECORDING FORMAT

The format of the data recorded on the diskette is the IBM format using 26 sectors, 15 sectors or 8 sectors per track or a special 46 sector non-IBM format. Figure 1-5 shows the IBM track formats. The diskette is organized into 77 separate concentric circular bands called tracks. See Figure 1-3. The outermost track address is 00 and the innermost track address is 76. Each track is divided into contiguous segments called sectors. The first sector after the index hole is assigned an address of 01. The address of the last sector on a track will be equivalent to the number of sectors/track selected. Sectors may be considered as a wedge or pie shapes when a set of sectors is extended over all tracks.

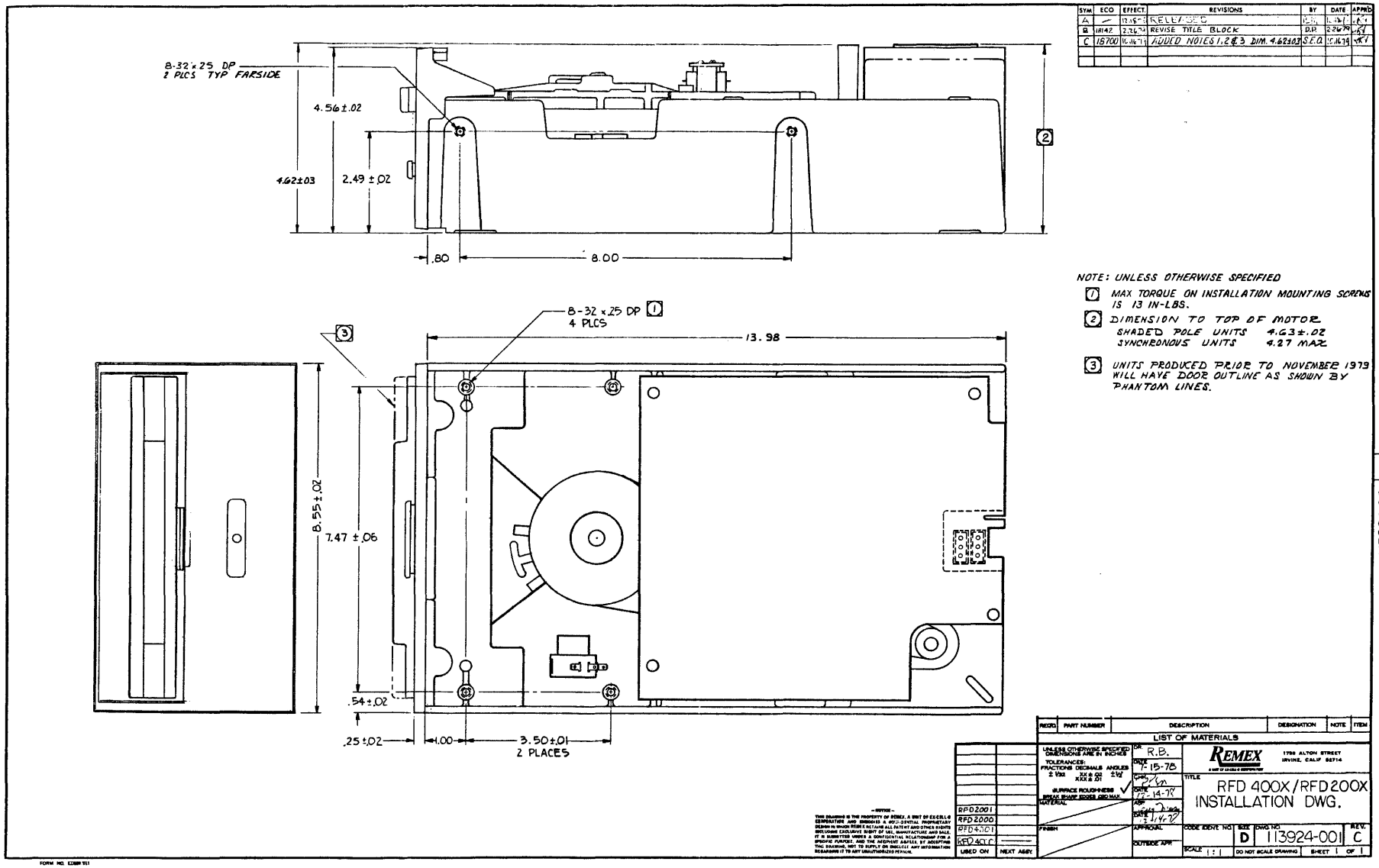


Figure 1-2. Installation Drawing, Model RFS4810/4820/2410/2420.

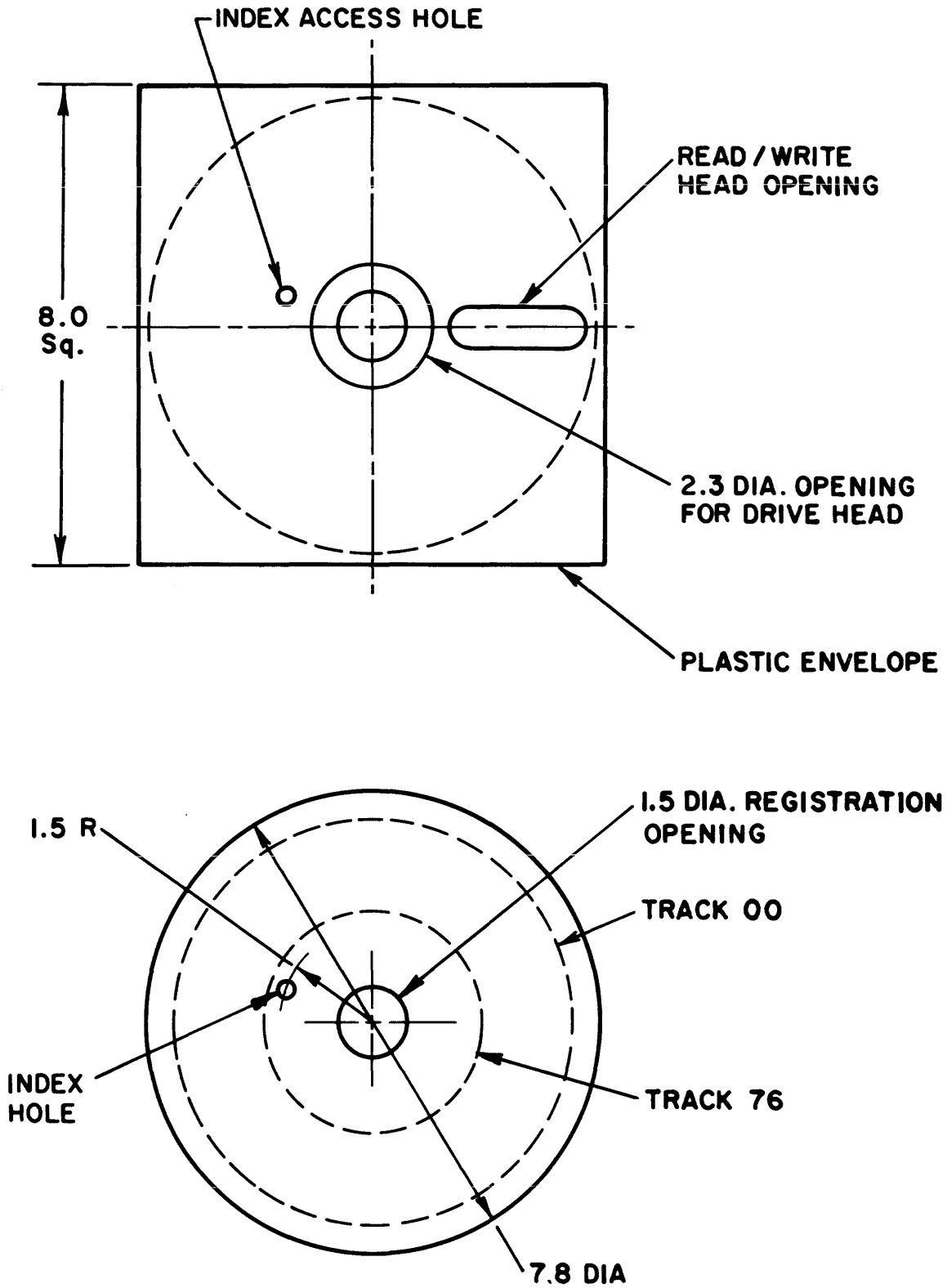
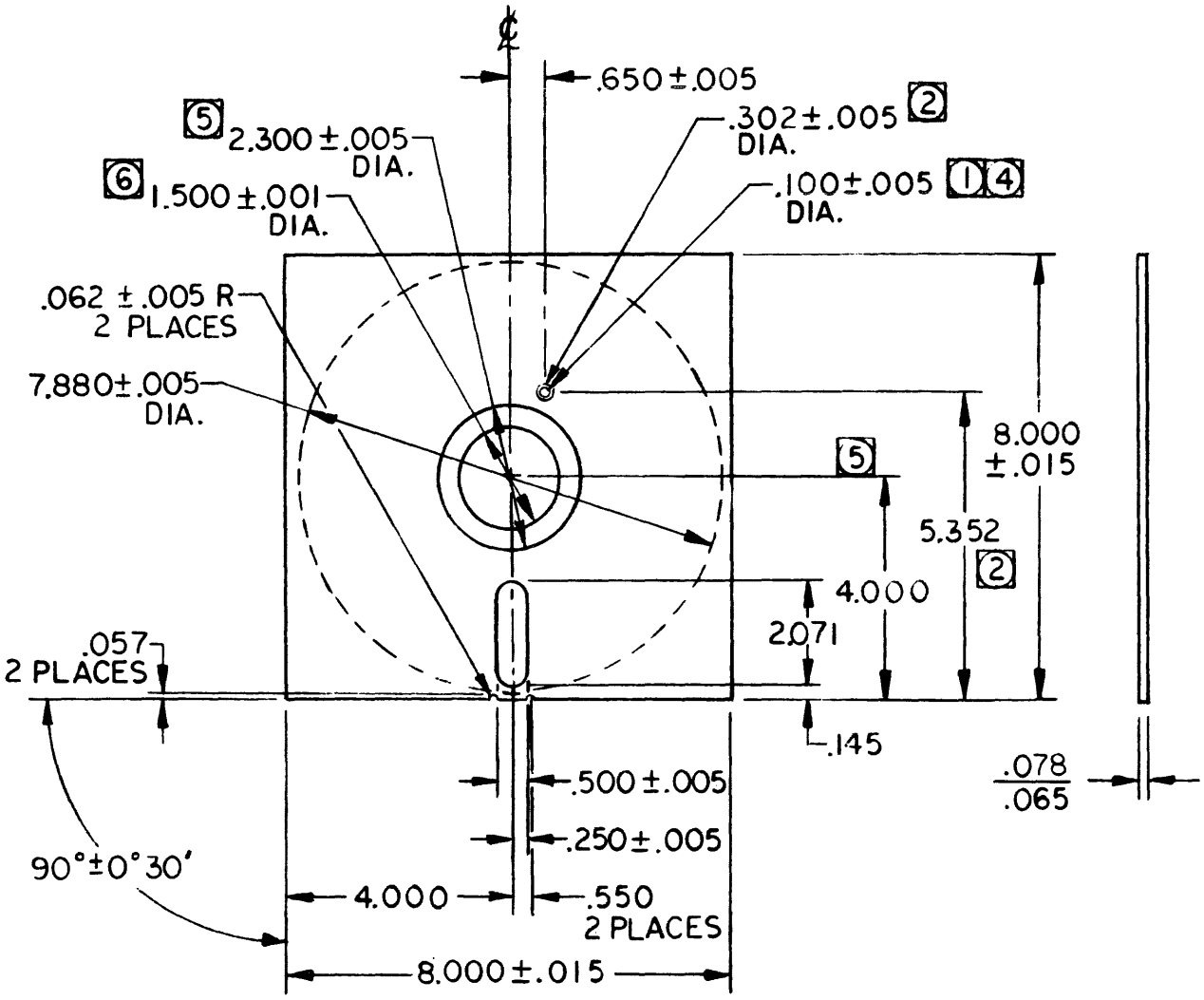


Figure 1-3. Storage Element Physical Dimensions, Single Sided Diskette.



MMC 669

1. INDEX HOLE IN DISK.
2. INDEX HOLE IN JACKET – BOTH SIDES.
3. ALL DIMENSIONS ARE ±.010 INCH UNLESS OTHERWISE INDICATED.
4. CENTER OF MOUNTING HOLE TO CENTER OF INDEX HOLE IS 1.500±.002 INCH.
5. MOUNTING HOLE IN JACKET – BOTH SIDES.
6. MOUNTING HOLE IN DISK.

Figure 1-4. Storage Element Physical Dimensions, Two Sided Diskette.

		SINGLE DENSITY 26 SECTORS		SINGLE DENSITY 15 SECTORS		SINGLE DENSITY 8 SECTORS		DOUBLE DENSITY 26 SECTORS		DOUBLE DENSITY 15 SECTORS		DOUBLE DENSITY 8 SECTORS	
		#BYTES	HEX	#BYTES	HEX	#BYTES	HEX	#BYTES	HEX	#BYTES	HEX	#BYTES	HEX
TRACK INDEX FIELD	PREAMBLE	40 6	FF 00	40 6	FF 00	40 6	FF 00	80 12	4E 00	80 12	4E 00	80 12	4E 00
	TRACK MARK	1	FC CLOCK = D7	1	FC CLOCK = D7	1	FC CLOCK = D7	3 1	C2 (1) FC	3 1	C2 (1) FC	3 1	C2 (1) FC
	GAP 1	26	FF	26	FF	26	FF	50	4E	50	4E	50	4E
SECTOR FIELD	GAP 2	6	00	6	00	6	00	12	00	12	00	12	00
	ADDRESS MARK	1	FE CLOCK = C7	1	FE CLOCK = C7	1	FE CLOCK = C7	3 1	A1 (2) FE	3 1	A1 (2) FE	3 1	A1 (2) FE
	TRACK #	1	01-4C	1	01-4C	1	01-4C	1	01-4C	1	01-4C	1	01-4C
	SIDE #	1	00-01	1	00-01	1	00-01	1	00-01	1	00-01	1	00-01
	SECTOR #	1	01-1A	1	01-0F	1	01-08	1	01-1A	1	01-1A	1	01-08
	SECTOR SIZE = 128 x 2^N	1	N = 00	1	N = 01	1	N = 02	1	N = 01	1	N = 02	1	N = 03
	CRC-PREVIOUS 'Y' BYTES	2	Y = 5 XX	2	Y = 5 XX	2	Y = 5 XX	2	Y = 8 XX	2	Y = 8 XX	2	Y = 8 XX
	GAP 3	11 6	FF 00	11 6	FF 00	11 6	FF 00	22 12	4E 00	22 12	4E 00	22 12	4E 00
	DATA MARK	1	FB(3) CLOCK = C7	1	FB(3) CLOCK = C7	1	FB(3)	3 1	A1(2) FB(3)	3 1	A1(2) FB(3)	3 1	A1(2) FB(3)
	DATA	128	E5	1 255	C4 5E	1 511	C4 5E	256	40	512	40	1024	40
	CRC PREVIOUS 'Z' BYTES	2	Z = 129 XX	2	Z = 257 XX	2	Z = 513 XX	2	Z = 260 XX	2	Z = 516 XX	2	Z=1028 XX
	GAP 4	27	FF	42	FF	58	FF	54	4E	84	4E	116	4E
	REPEAT SECTOR 'M' TIMES	M = 26		M = 15		M = 8		M = 26		M = 15		M = 8	
	TRAILING GAP 5	247	FF	170	FF	311	FF	598	4E	400	4E	654	4E

(1) Missing clock between bits 3 and 4.

(2) Missing clock between bits 4 and 5.

(3) This is F8 for deleted data or IBM calls it "control data" when used on T00 Side 0 Sector 8-26 and T00 Side 1 all Sectors. This is not applicable to the Data Warehouse.

(4) Initialize paramaters are estimated from other formats for which we have IBM Specs.

(5) Track 00 Side 0 is written similar to single density 26 sectors for all formats except data fields are different.

(6) Track 00 Side 1 is written in 26 sector pattern either single or double density to match rest of diskette.

XX = CRC calculated by $1 + x^5 + x^{12} + x^{16}$.

Figure 1-5. IBM Track Format. Hexidecimal Notation Used (X'00') In This Illustration.

The data storage region of a sector is traditionally termed a record. A collection of records is termed a file. The track and sector addresses which define the beginning of a file are called the beginning of extent (BOE) and the terminal track and sector addresses for a file are called the end of extent (EOE). The entire diskette is referred to as a volume. Track 00 is termed an index track and is usually reserved for file management and other descriptive information about the volume.

1.8 MAINTENANCE AND RELIABILITY

This section defines the long term unit reliability and data integrity.

1.8.1 DESIGN LIFE

The drive is designed and constructed, to provide a useful life of 5 years. During the useful life repair or replacement of parts is permitted. The read head is designed for a minimum of 30,000 hours operation.

1.8.2 RECOVERABLE READ ERROR

The recoverable read error rate is less than one error in 10^9 bits.

1.8.3 NON-RECOVERABLE READ ERROR RATE

The non-recoverable read error rate is less than one error in 10^{12} bits read. Errors attributed to the diskette are not included in determining the non-recoverable read error rate.

1.8.4 INTERCHANGEABILITY

The RFS4800 and 2400 series (single density IBM formats) is designed to be media interchangeable with the RFS12X0 subsystem, the RFD4000 and 2000 Series drives, RFD1000 diskette drives, RFD7401 diskette drives, and the following IBM systems: 3741, 3742, 3747, 3540 and Systems 32 and 34.

1.9 MODEL NUMBER DESIGNATION AND OPTIONS

The model number system is used for product identification. It includes a basic model series number which is followed by a virgule (/) and then a six digit number and finally a three digit dash number. The model number is used to code and identify a particular combination of options used in a given product line. This number is printed on the Identification Decal and is located on one of the rear surfaces. Those digits to the left of the virgule are the basic model series of the product line e.g. RFS4810. The six digits to the right and the three dash numbers give the top assembly number of the product. The three digit dash number is unique for any particular combination of options and configurations used in the basic assembly. Table 1-3 lists

the various assemblies possible and a description of option combinations used for each dash number. An X in a model number (as used in many parts of the manual, especially the parts list) denotes any of the letters or digits used in that space is applicable in the situation cited.

Table 1-3. Model Number Configurations

Model Number	Description
RFS2410/814230-001	Standard RFS2410 Master with 110/115 VAC, 50Hz
RFS2410/814230-002	Standard RFS2410 Master with 115 VAC, 60Hz
RFS2410/814230-003	Standard RFS2410 Master with 220 VAC, 50Hz
RFS2410/814230-004	Standard RFS2410 Master with 220 VAC, 50Hz with Special Motor
RFS2420/814231-001	Standard RFS2420 Slave with 110/115 VAC, 50Hz
RFS2420/814231-002	Standard RFS2420 Slave with 115 VAC, 60Hz
RFS2420/814231-003	Standard RFS2420 Slave with 220 VAC, 50Hz
RFS2420/814231-004	Standard RFS2420 Slave with 220 VAC, 50Hz with Special Motor
RFS4810/814235-001	Standard RFS4810 Master with 110/115 VAC, 50Hz
RFS4810/814235-002	Standard RFS4810 Master with 115 VAC, 60Hz
RFS4810/814235-003	Standard RFS4810 Master with 220 VAC, 50Hz
RFS4810/814235-004	Standard RFS4810 Master with 220 VAC, 50Hz with Special Motor
RFS4820/814236-001	Standard RFS4820 Slave with 110/115 VAC, 50Hz
RFS4820/814236-002	Standard RFS4820 Slave with 115 VAC, 60Hz
RFS4820/814236-003	Standard RFS4820 Slave with 220 VAC, 50Hz
RFS4820/814236-004	Standard RFS4820 Slave with 220 VAC, 50Hz with Special Motor

SECTION II

INSTALLATION AND INTERFACE

2.1 UNPACKING

To provide the most protection during transit, specially disigned and reinforced packing cartons are used to ship the REMEX subsystem. When removing the subsystem from the carton, lift with both hands under the unit. Never lift or attempt to carry the unit by any of the covers, door or other delicate parts. Carefully inspect the unit for any apparant damage as soon as it is removed from the carton. In the event the equipment has been damaged as a result of shipping, the carrier and REMEX must be notified as soon as possible.

CAUTION

To prevent magnetization of the head, it is important that during unpacking, installation and operation that the read/write head does not come in contact with stray magnetic fields.

2.2 MOUNTING

The Diskette Subsystem is designed to operate in four positions: on either side, upright (head carriage up) or front panel up. Threaded holes in the mainframe sides and the bottom are provided for either slide or fixed mounting. See Figure 1-2. It should be placed in an environment that does not exceed the ambient temperature specification listed in Table 1-2. If the drive is mounted in the proximity of other heat producing units, a 60 cfm fan must be suitably mounted nearby to ensure sufficient air circulation. I/O cables must not exceed 10 feet in length. Cables between master and slave must not exceed four feet.

2.3 INITIAL ADJUSTMENTS AND JUMPER SELECTIONS

Each subsystem has been accurately adjusted and aligned before leaving the factory. No adjustment or calibration should be required prior to installation or use. Two jumper plugs are supplied on the Drive Card which are used to select the desired unit address. See Figure 7-5 for location of unit select pins on RFS4810 and 2410 and Figure 7-6 for the RFS4820 and 2420. Table 2-1 gives the jumper connections corresponding to the unit number address.

Although the subsystem has the ability to determine the density of the media it's accessing, it takes a slight period of time to switch density. Therefore, provisions have been made on the Master drive P.C. Board to cause it to expect a specific density (single or double). To eliminate that delay,

a jumper between points J and Y causes the drive to expect double density and a jumper between J and H will cause it to expect a single density media format. Points F and G jumpered (using the F to Z jumper) will cause it to expect a single density media format on side 0, track 0 only (to facilitate use of IBM specified dual density formats). The drive is shipped without these points jumpered.

Table 2-1. Jumper Selection for Unit Address

	Master						Slave					
Unit Address	R	P	N	M	L	K	D	E	F	G	H	J
0	—			—				—			—	
1		—		—				—		—		
2	—				—		—				—	
3		—			—		—			—		

2.4 POWER AND SYSTEM CONNECTIONS

Figure 2-1 illustrates the interconnection between the host, power supply, Master drive and Slave drives. The Master drive is the only drive which connects to the Host system and this is done through P1/J1. Figure 2-2 lists the interface pin connections for P1/J1. Table 3-1 lists the detail description for each pin on J1. P2 is connected in parallel from the master to each of the slave drives. D.C. power is applied in parallel to J3 on each drive. The connections for J3 are also given in Figure 2-2. A.C. power is applied in parallel through J8 on each drive (not shown in Figure 2-1). The wiring for J8 is shown in Figures 8-1 and is the same for all types of drives. Figures 2-3 and 2-4 shows the locations of J1, (RFS4810 and RFS2410 ONLY) J2, J3 and J8 for both the Master and Slave drives respectively. Figure 2-5 gives the recommended interface circuits. All mating connectors are provided in the kit of parts (Table 1-1).

CAUTION

Always consult the serial tag and refer to Table 1-3 for proper A.C. voltage and frequency to be used as coded in the model number. Failure to do so could result in damage to the unit. If another A.C. voltage or frequency is required, kits are available as described in Section 2.5.

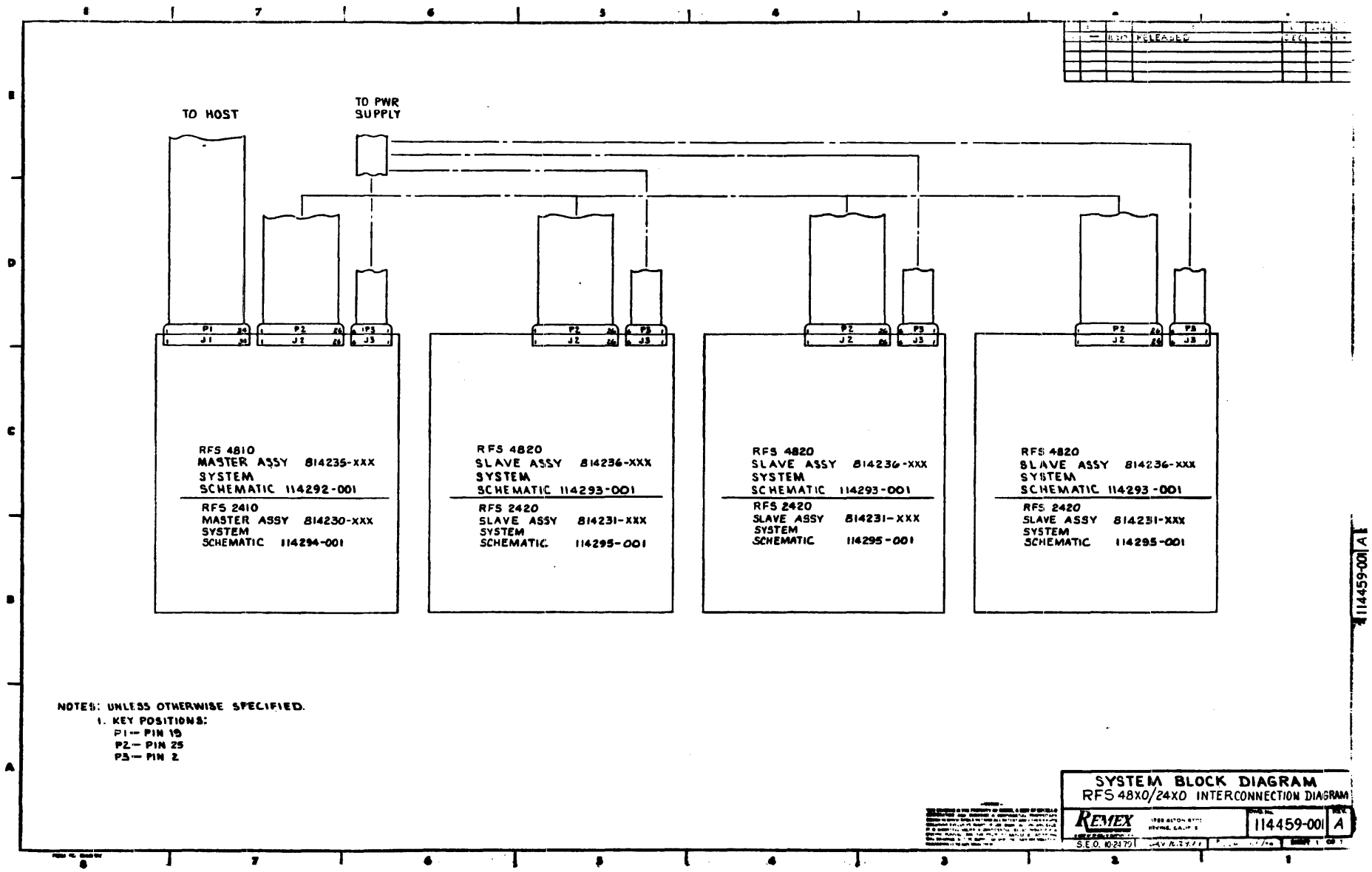


Figure 2-1. Interconnection Diagram, RFS4810 and RFS2410 Subsystem and their respective slave drives.

RFS4810 and RFS2410 units with circuit cards 114101-001, rev. E Assy. or higher allow either - 5V or a variable voltage between - 6 to - 12VDC to be applied to J3-1 depending upon the jumper configurations as given in Table 2-2. RFS4820 and RFS2420 units with circuit card 114181-001, rev. D Assy. or higher also allow these same voltage selections as determined by the jumper configurations given in Table 2-2.

Table 2-2. D.C. Voltage Jumper Configurations

Voltage	Model	Jumper
- 5VDC	RFS4810, RFS2410	Jumper BB and CC
- 5VDC	RFS4820, RFS2420	Jumper P and R
- 6 to - 12VDC	RFS4810, RFS2410	Jumper AA and BB
- 6 to - 12VDC	RFS4820, RFS2420	Jumper N and P

2.5 OPTIONAL VOLTAGES AND FREQUENCIES

Each drive is designed to work on a particular voltage and frequency as described in Table 1-3. In the event a different voltage and/or freqency is required, conversion kits are available which contain the necessary parts and instructions to accomplish the conversion. Conversion Kit RMF0055 (P/N 814389-001) converts 115VAC, 60Hz units (814230-002, 814231-002, 814235-002 and 814236-002) to 220VAC, 50Hz. Conversion Kit RMF0056 (P/N 814394-001) Converts 220VAC, 50Hz units (814230-003, 814231-003, 814235-003 and 814236-003) to 115VAC, 60Hz. The contents of each kit is listed in Table 7-5.

WARNING

Disconnect AC power at J8 before installing any of the conversion kits.

Connector, Pin		Signal
J1-1	———	Bidirectional Data Bus, DAT0*
J1-2	———	Bidirectional Data Bus, DAT1*
J1-3	———	Bidirectional Data Bus, DAT2*
J1-4	———	Bidirectional Data Bus, DAT3*
J1-5	———	Bidirectional Data Bus, DAT4*
J1-6	———	Bidirectional Data Bus, DAT5*
J1-7	———	Bidirectional Data Bus, DAT6*
J1-8	———	Bidirectional Data Bus, DAT7*
J1-9	———	Busy, BUSY*
J1-10	———	Data Transfer Request, DTR*
J1-11	———	Special Command Line, SPCL*
J1-12	———	Spare
J1-13	———	Master Reset, MRST*
J1-14	———	Data Direction Out to Host System, DDOUT*
J1-15	———	Data Transfer Acknowledge, DTAK*
J1-16	———	Error, ERROR*
J1-18 through J1-34	———	OV signal return (except Pin 19, Key).
J3-1	———	- V (See Section 2.4)
J3-2	———	Key
J3-3	———	+ 24VDC
J3-4	———	+ 24V Return
J3-5	———	+ 5VDC
J3-6	———	+ 5VDC Return

Figure 2-2. Host Pin Connections, J1, RFS4810 and RFS2410, and D.C. Power Connections (all drives).

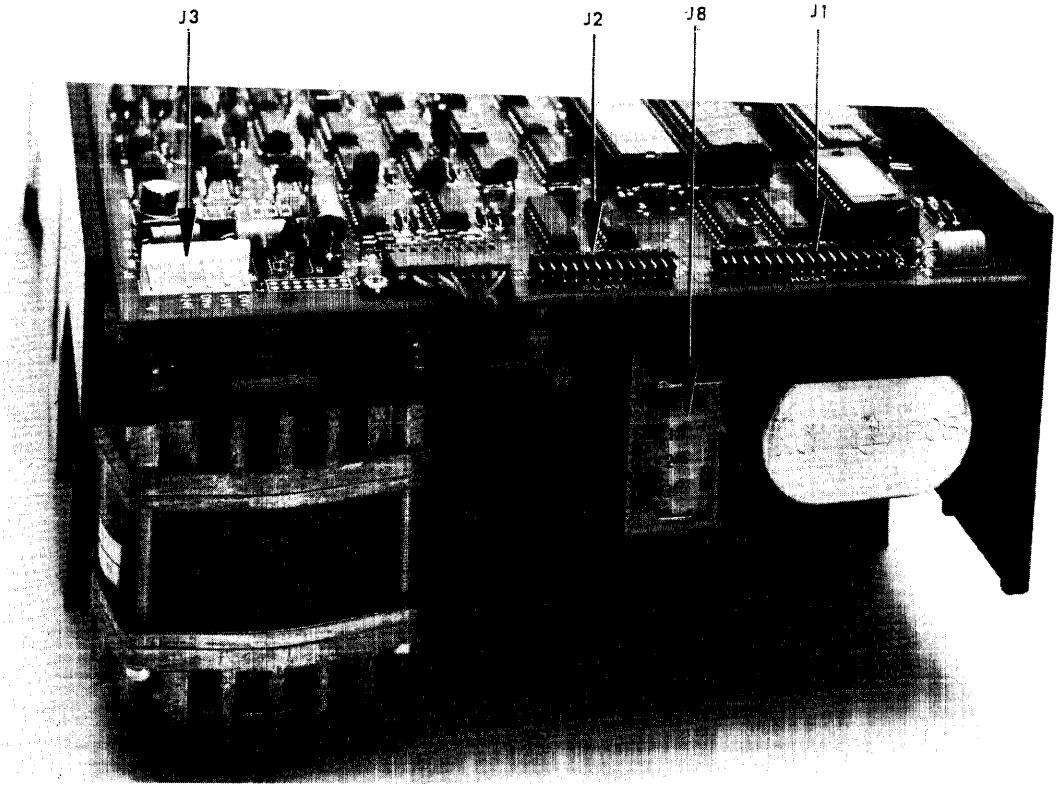


Figure 2-3. Interface Connector Locations, RFS4810 and RFS2410. (Master Drive)

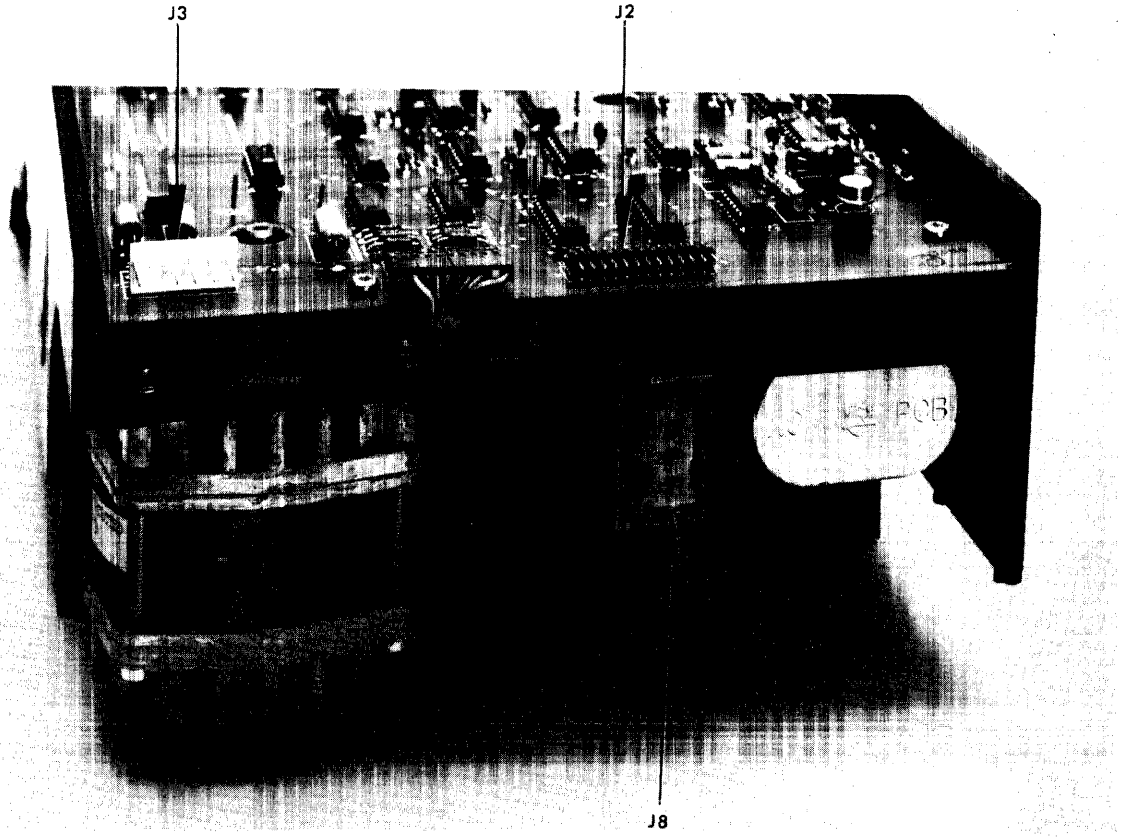
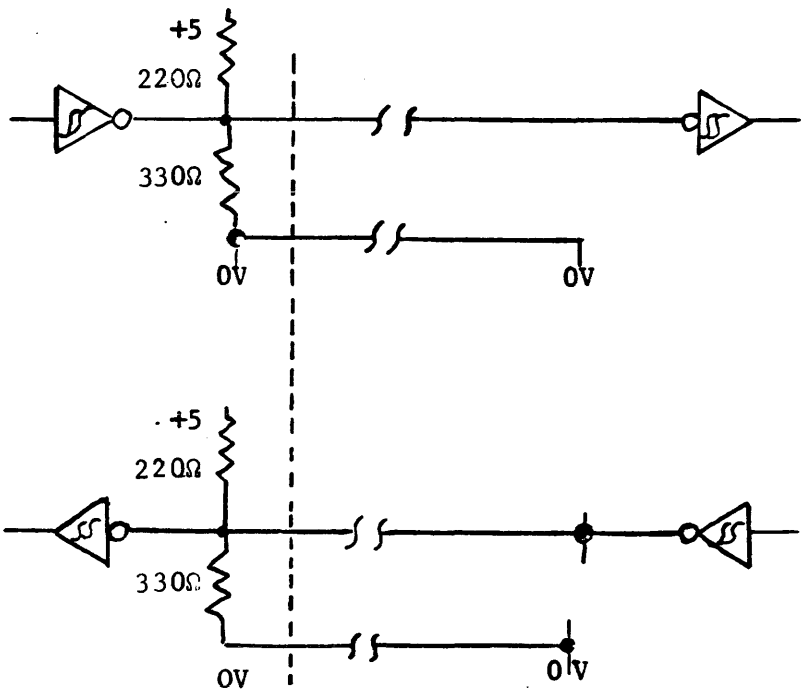


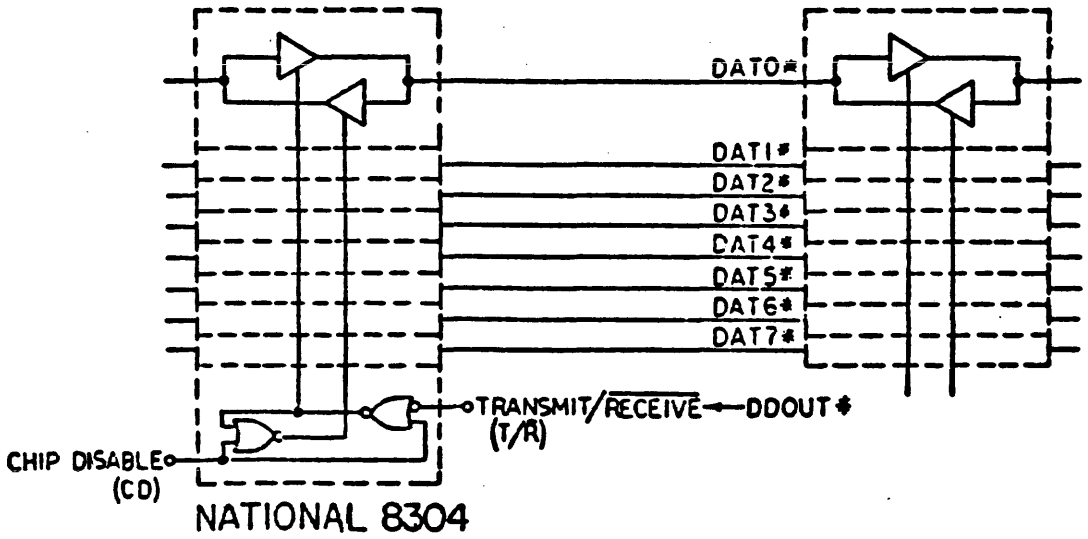
Figure 2-4. Interface Connector Locations, RFS4820 and RFS2420. (Slave Drive)



STATUS AND CONTROL LINES

HOST RFS 2400/4800 SUBSYSTEM

Devices are LS-TTL Tri-state e.g., 74LS240, 74LS243, 8T26A, etc.



HOST RFS 2400/4800

Bi-Directional Data Lines, Recommended Circuitry

Figure 2-5. Recommended Interface Circuits.

SECTION III

OPERATION

3.1 INPUT-OUTPUT SIGNALS

Table 3-1 lists the input, output and power signals which are routed through J1 and J3. Table 3-2 lists the signals which are routed between the Master drive unit and the Slave drive units on J2.

3.2 OPERATOR CONTROLS

The subsystem is fully automatic under direction of a microprocessor controller except for loading and unloading the diskette. A front panel indicator light indicates that the drive is busy. Section 3.3.3. describes the loading and unloading of a diskette.

3.3 START-UP AND DISKETTE LOADING INSTRUCTIONS

The subsystem is designed for ease of operator use since there are no complicated controls and indicators. The following section describes the procedures for loading and operating the diskette subsystem.

3.3.1 POWER UP MODE

Applying AC and DC power to the subsystem can be done in any sequence. However, once AC power has been applied, a 2-second delay must be completed before any Read or Write operation is attempted. This delay is for stabilization of the diskette rotational speed. When DC power is applied, a 90 msec power on reset automatically resets the electronics and inhibits inadvertent writing or erasing on the diskette. Thus, the drive is ready for operation 2 seconds after application of AC power and 90 msec after application of DC power.

3.3.2 DISKETTE HANDLING

The Diskette consists of the flexible disk encased in a plastic jacket. When not in use the Diskette is always stored in a protective envelope. An analogy of this protective storage envelope would be the same as the envelope used to store phonograph records used in your home. The storage

envelope affords the same protection from dust and contaminants. To protect the Diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

a. Return the Diskette to its storage envelope whenever it is removed from file.

b. Store Diskettes vertically.

c. Keep Diskettes away from magnetic fields and from ferromagnetic materials which might cause magnetization. Strong magnetic fields can destroy recorded data on the disk.

d. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the Diskette.

e. Do not write on the Diskette with a lead pencil or ballpoint pen. Use a felt tip pen.

f. Do not smoke while handling the Diskette. Heat and contamination from a carelessly dropped ash can damage the disk.

g. Do not expose Diskettes to heat or sunlight. The read/write head cannot properly track a warped disk.

h. Do not touch or attempt to clean the disk surface. Abrasions and foreign material from the hands may cause loss of stored data.

3.3.3 DISKETTE LOADING/UNLOADING

The following prodedure should be followed when loading or unloading the diskette.

a. Apply AC/DC power to the unit.

b. Open the drive door by depressing the latch.

c. Carefully remove the diskette from its storage envelope.

NOTE

If it is desired to protect the diskette data from inadvertent or accidental erasure and write-over, make sure the notch on the jacket is uncovered. An optional sensor senses the notch and if it is covered writing is allowed; if it is uncovered the write circuitry is disabled.

d. Insert the diskette into the drive. The diskette is inserted with the index hole nearest the operator and the diskette label on the same side as (facing) the door. See Figure 3-1. To load the drive, insert a diskette into the open mouth of the drive until the ejection mechanism is engaged and the door will shut when closed. Close the door to the drive.

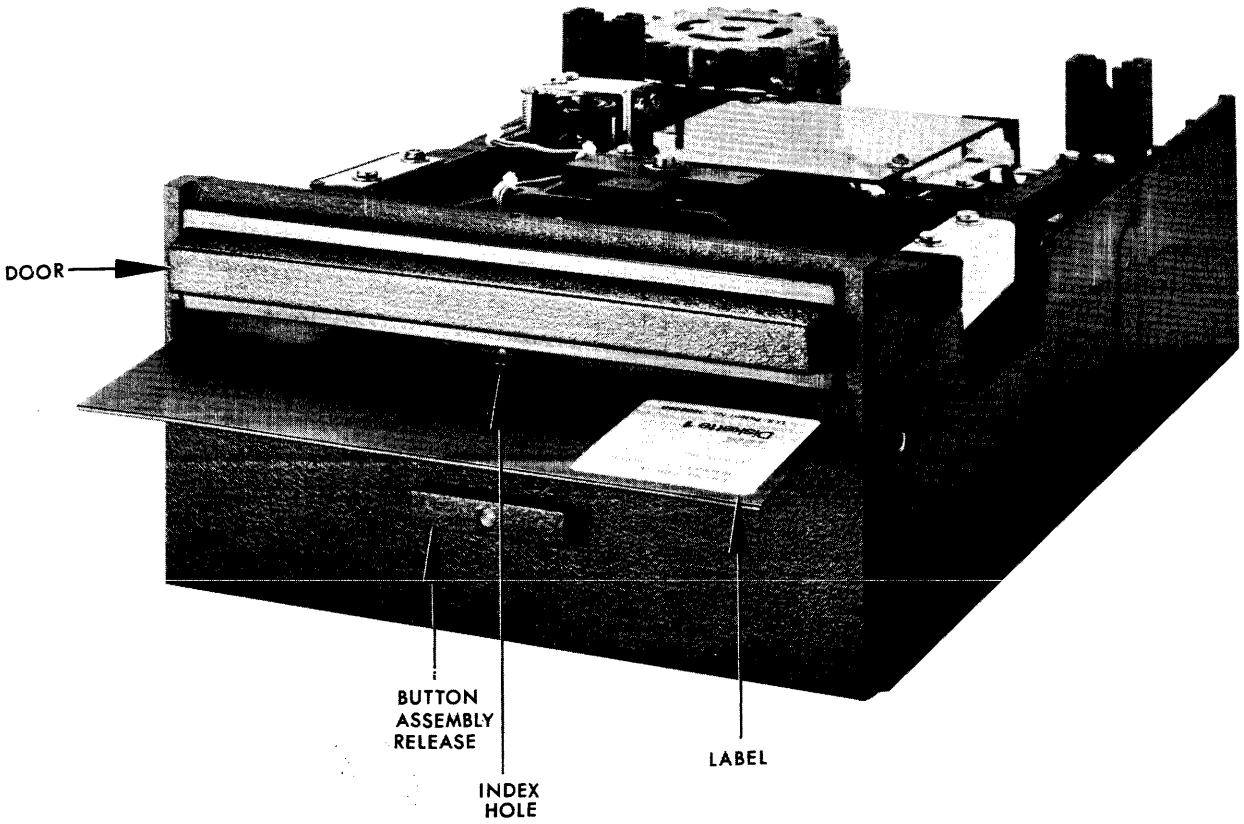


Figure 3-1. Diskette Insertion.

e. The Subsystem may now be operated in any of the modes of operation described in Section 3.4.1 through 3.4.8.

f. To unload the diskette, open the door (when busy light is off), remove the diskette (returning it to its protective storage envelope) and close the door.

Table 3-1. Interface Signals for RFS4810 and 2410.

All signals with an asterick (*) following the signal name are low true (active), i.e., logic 1 = 0V, logic 0 = +2.4V min. Interface signals are of two types: Control and bidirectional data lines. The master to slave interface circuits employ a bus configuration that allows up to three slave units to be bussed together on one cable. Only one subsystem is logically connected to the bus at any given time. Ribbon cable is recommended for interconnection. These cables typically have a characteristic impedance of approximately 100 ohms. The address of the subsystem is determined by jumper plugs on the printed circuit board. The physical position on the slave does not determine the logical address. Recommended maximum cable (host to subsystem master) length is 10 feet. All signals, input and output are referenced with respect to the Master. Thus an input to the master would be either an output from the host or slave depending upon the signal.

	CONNECTOR PIN	DESCRIPTION
HOST INTERFACE	J1-1 through J1-8	Bidirectional Data Bus DAT0* through DAT7*. Used to transmit data, status and commands between host and subsystem. For input to subsystem (DDOUT* high), Data Bus should be asserted prior to or simultaneously with DTAK* active in response to a DTR* active and should be held valid until DTR* goes inactive. For output to host(DDOUT* low) data bus is valid prior to DTR* active and remains valid for 80 ns after receipt of an active DTAK*. DTR* will become inactive after the data bus is invalid.
	J1-9	Busy Output, BUSY*, Active state indicates that the subsystem has received a command and is in the process of executing that command (including illegal commands). Inactive state indicates the subsystem is idle and will accept a command.
	J1-10	Data Transfer Request Output, DTR*. Active signal indicates that the drive subsystem requires data on the data bus for input(DDOUT* high) or has placed data on the bus for output(DDOUT* low). DTR* will become inactive after the data bus is invalad.
	J1-11	Special Command Line SPCL*. This line will abort a multisector operation at the completion of reading/writing of a sector. It must remain active and data transfers must continue until BUSY* goes false.
	J1-12	Spare
	J1-13	Master Reset Input, MRST*. Active signal will cause system to terminate any operation in process, clear all error conditions, raise heads on master and all slaves, and reset the subsystem to an idle state.
	J1-14	Data Direction Out to Host Output, DDOUT*. Data direction signal line controlled by the subsystem to indicate the direction data is being transmitted on the Bidirectional Data Bus DAT0* through DAT7*. Inactive signal indicates data transfer into the drive subsystem. Active signal indicates data transfer to the host.
	J1-15	Data Transfer Acknowledge Input, DTAK*. Active signal from the host acknowledges that data has been placed on or taken from the data bus, depending upon the level of DDOUT* in response to a DTR*.
	J1-16	Error Output, ERROR*. Active signal indicates that one of the following error conditions has occurred: (1) Record not found, (2) CRC Error, (3) Lost Data, (4) Illegal Command, (5) Excess Bad Tracks, (6) Drive not ready when accessed, (7) Attempting to write on a Write Protected Diskette, or (8) Sector with deleted data mark encountered. The specific error condition(s) can be found by a read status command. See Figure 3-2.
	J1-18, J1-20 through J1-34	Zero volt return lines.
	J1-19	Key
	J2	Slave Unit Interface Connector. Internal to subsystem does not require host interface. See Table 3-2 for signal definitions.

POWER	J3-1	-12 VDC
	J3-2	Key
	J3-3	+24 VDC
	J3-4	+24 VDC Return
	J3-5	+5 VDC
	J3-6	+5 VDC Return

Mating Connector for J1 is 3M Company 3414.
Mating Connector for J3 is Molex 09-50-7061 with 08-50-0106 Contacts.
Mating Connector for AC plug is Amp 1-480700 with 3ED550-1 Contacts.

Each non-bidirectional input line has the following characteristics:

Active: 0V to +0.4V
Inactive: +2.5V to +5V

Each non-bidirectional output line has the following characteristics:

Active: 0V to +0.4V
Inactive: 4.7K ohms to +5V
Maximum Current Sink: 24 mA

Table 3-2. Master/Slave Interchange Signals for RFS4820 and RFS2420

Connector Pin	Signal and Description
J2-1	Slave Serial Read Data, SSRDTA*. Active pulse train representing composite clock and data signals being read from the selected slave drive.
J2-2	Slave Track 00, STR00*. Active signal indicates selected slave drive is at track 00 location.
J2-3	Slave Index Pulse, SIP*. Active pulse indicates sensing diskette index hole on selected slave drive.
J2-4	Slave Write Protected Diskette, SWPRT*. Low Active signal indicates selected slave drive contains a Write Protected Diskette in place.
J2-5	Slave Write Gate, SWG. Active signal enables the write logic of the selected slave.
J2-6	Slave Track Greater than 43, STG43. Active signal causes write logic in selected slave head to reduce the write current when writing above track 43 for better resolution and compliance with IBM standards.
J2-7	Slave Write Data, SWD. Active pulse train with composite data and clock for writing on the selected slave diskette.
J2-8	Slave Head Load SHDLD*. Active signal causes the selected slave to load the head onto the diskette.
J2-9	Slave Motor Step SSTEP. Active signal causes selected drive to step one track in direction determined by SDIR.
J2-10	Slave Motor Step Direction Signal SDIR. Low signal causes motor to step toward Track 00; High signal causes motor to step toward Track 76.
J2-11 J2-13	Slave Select Lines, SSEL0* and SSEL1*. Active signals used for drive selection. Slave drives can be jumper connected for unit address 0 through 3.
J2-12	Slave Drive Ready, SDRDY*. Active signal indicates selected slave drive is ready, i.e., diskette is in place and rotating with door closed.
J2-14 through J2-24	OV return.
J2-25	Key
J2-26	Slave Top Head Select, TPHD*. Signal used to select diskette side. Inactive signal indicates side 0. Active signal indicates side 1.

3.4 MODES OF OPERATION

A single 8-bit bidirectional bus is used to transfer all commands, data and status to/from the host. The bus transfer direction is indicated by a single line (DDOUT*). The DTR* and the DTAK* lines are used as handshaking signals between the host and master subsystem. Two additional lines are used to transmit BUSY* and ERROR* status to the host.

3.4.1 I/O TRANSACTION SEQUENCE

All I/O transactions between the subsystem and host are predicated on the following.

a. The first byte transferred to the subsystem while it is in a System Ready state (i.e. BUSY* false and DTR* true) is interpreted as a command. The subsystem will set BUSY* true and DTR* false upon receipt of a command (including invalid commands).

b. The subsystem will determine the direction of data transfer using the DDOUT* line. DDOUT* low indicates data flows to host; DDOUT* high indicates data flow from host.

c. All data transfers are requested by the subsystem by the assertion of DTR*.

d. All data transfers must be acknowledged by the host with a DTAK* in response to a DTR* from the subsystem.

NOTE: Data input or output, to or from the host must precede or occur simultaneously with a DTAK*. Data output from the host must remain valid until DTR* goes false.

e. The Error flag is valid for the preceding operation (i.e., when the subsystem completes an operation and sets BUSY* false and DTR* true).

f. MRST* (Master Reset) will unconditionally abort any operation and set the subsystem to the System Ready state. The The Error flag will not be valid.

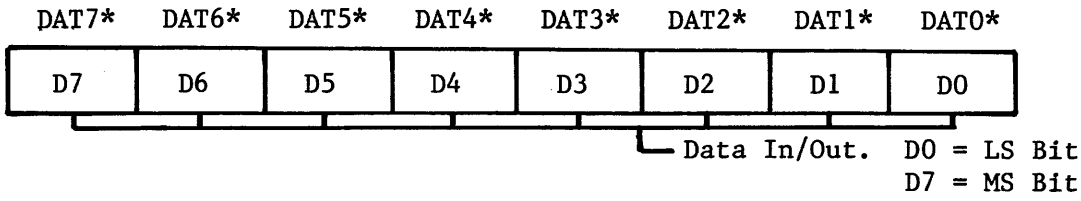
g. When a command has been completed, the subsystem will return to the System Ready state.

Depending upon the command presented by the host, the subsystem will request (and must be supplied with) additional parameters (unit #, track #, sector #, etc,) in the sequence outlined in steps c and d above. Table 3-3 shows the parameters required by each command. Figure 3-2 shows the format of these parameters. Figure 3-3 shows the timing for a Read (05_{16}) command. Sections 3.4.2 through 3.4.11 describe the various modes and commands.

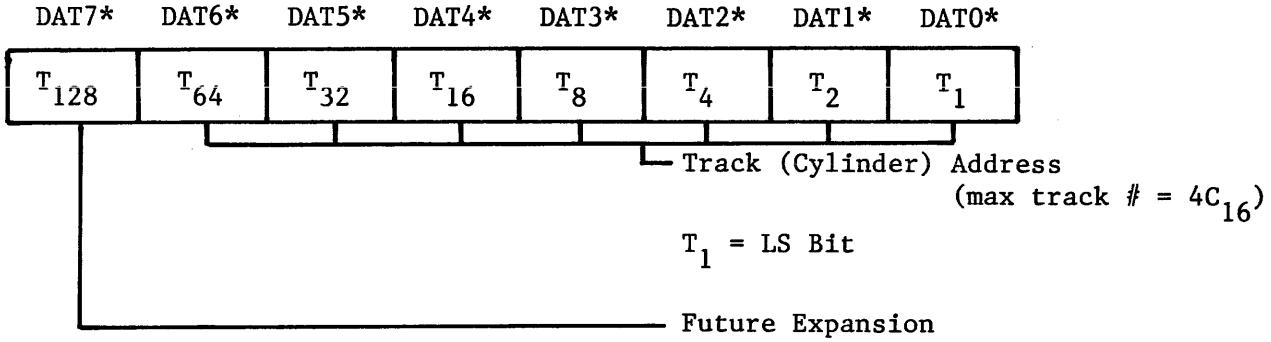
3.4.2 MASTER RESET

This mode is entered whenever the host system asserts the MRST* line low. This signal unconditionally causes the system to terminate any operation it was performing, clear all error status, and then enter the System Ready state.

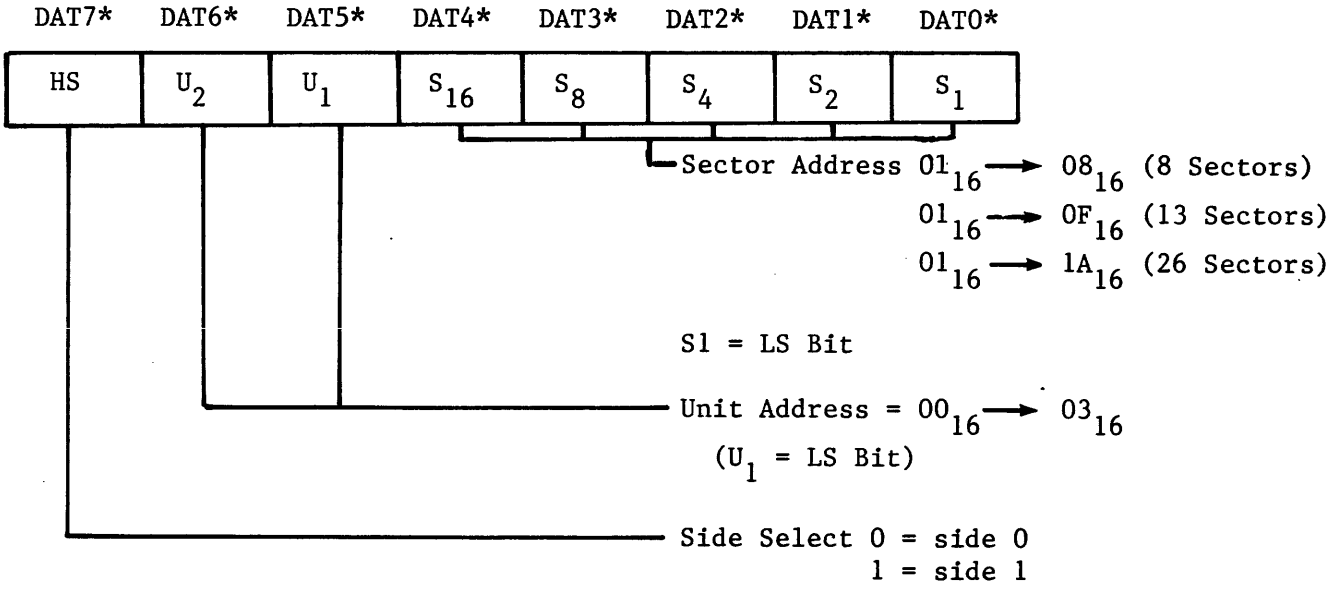
A. DATA BYTE



B. TRACK BYTE



C. UNIT/SECTOR BYTE



See Section 3.4.11 for utilization of 32 to 46 sectors of track feature.

D. COMMAND BYTE

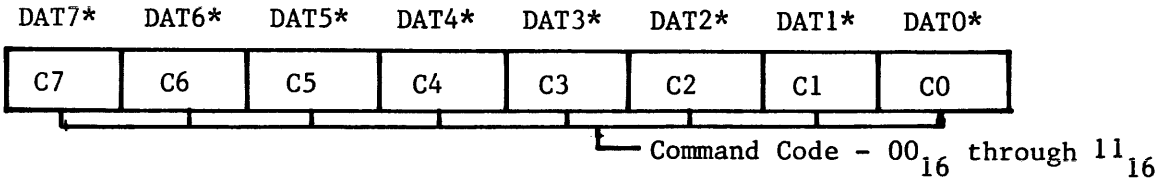


Figure 3-2. Data Formats, Sheet 1 of 3

F. AUXILLARY STATUS

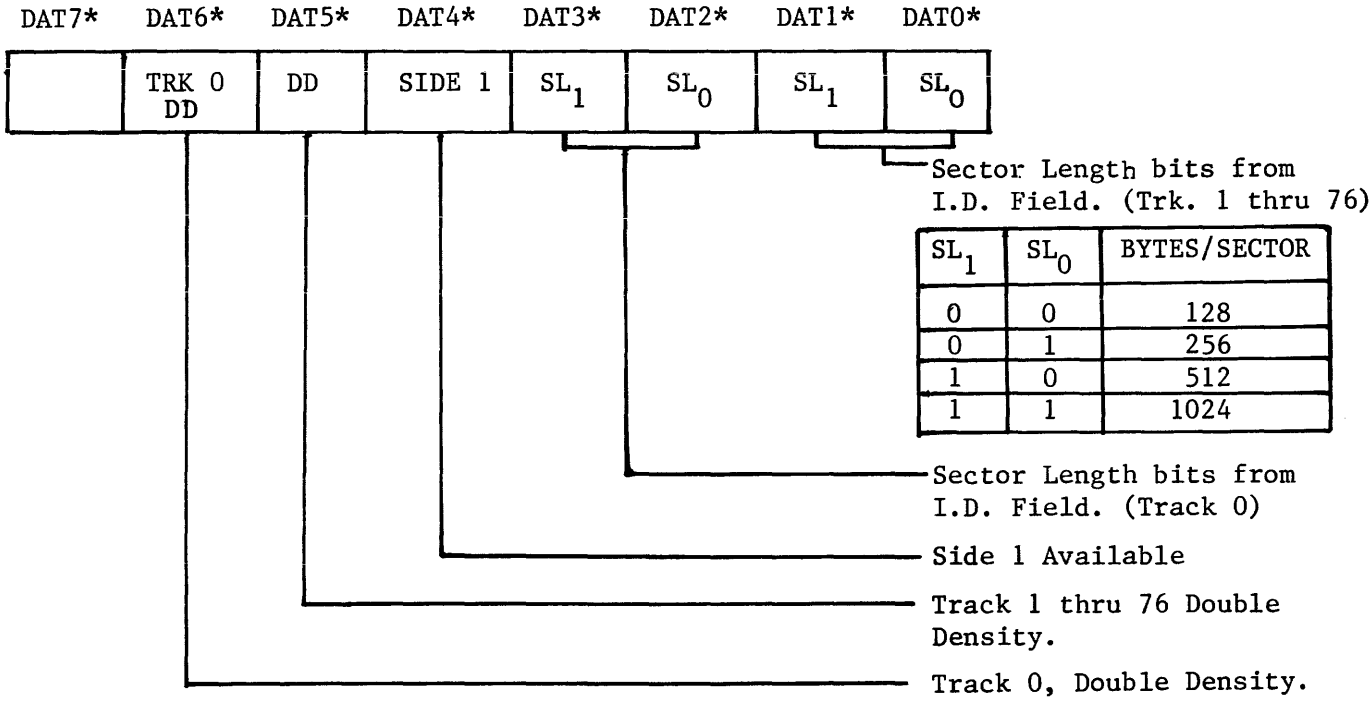


Figure 3-2. Data Bus Format, Sheet 3 of 3(Continued).

E. STATUS

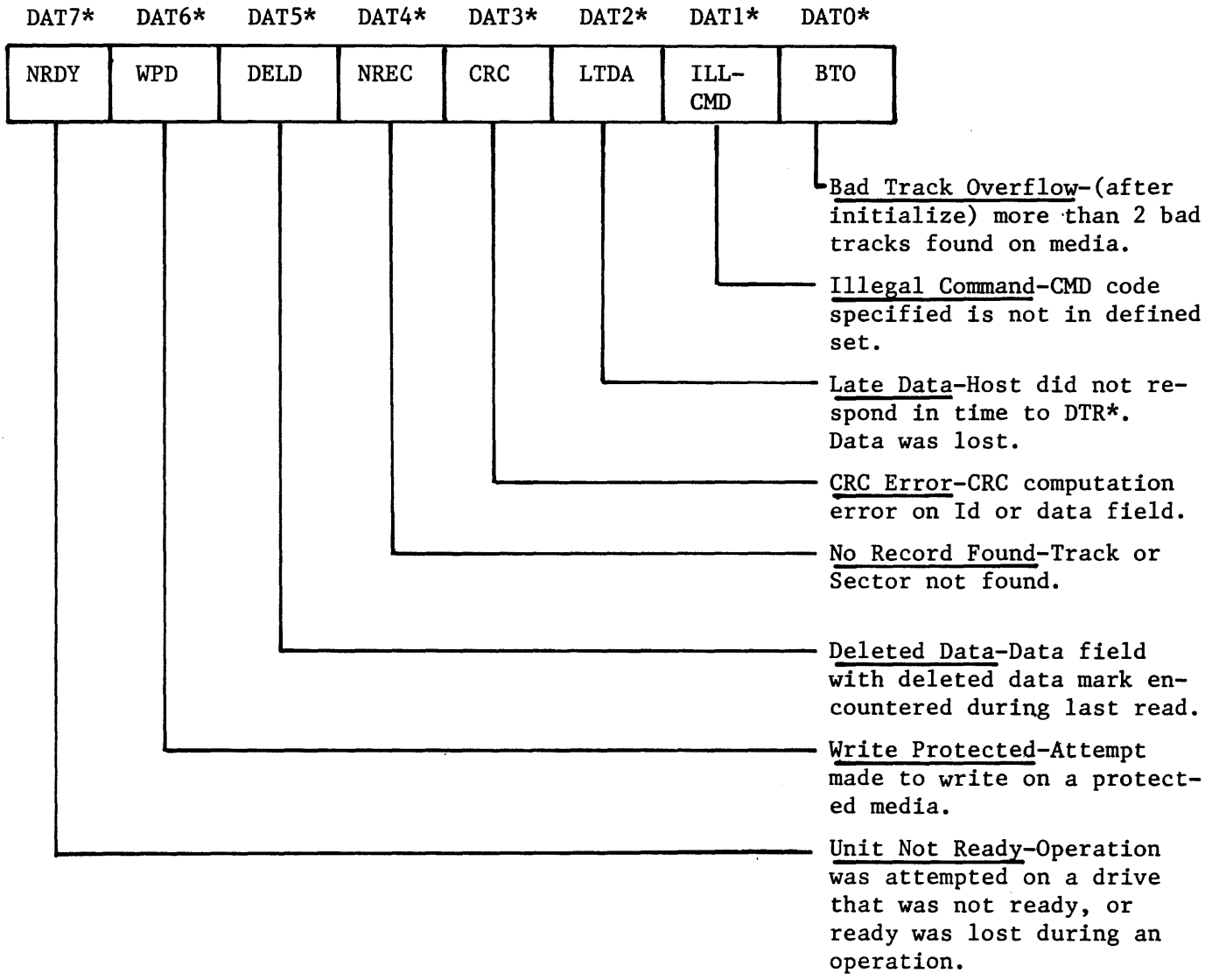


Figure 3-2. Data Bus Format, Sheet 2 of 3.

Table 3-3. Command Summary

BYTE #	COMMAND	DATA FLOW TO	DESCRIPTION
	BOOTSTRAP (BOOT), 00_{16}		
0	00_{16}	Subsystem	Transfers Track 00, Sectors 1 and 2 of unit 0, side 0 to host.
	READ STATUS (RSTS) 01_{16}		
0	01_{16}	Subsystem	Transfers Status to host.
1	Status	Host	
	READ AUXILIARY STATUS, 02_{16}		
0	02_{16}	Subsystem	Transfers Auxiliary Status to Host.
1	Side/Unit	Subsystem	
2	Auxiliary Status	Host	
	LOAD SECTOR COUNT (LDSC), 03_{16}		Load 2 Byte sector count for next operation.
0	03_{16}	Subsystem	Count = 1 to $65,535_{10}$
1	Sector Count MSB	Subsystem	Count = 0 is illegal.
2	Sector Count LSB	Subsystem	Absence of this command will also give a count of 1.
	READ LAST TRACK/SIDE/UNIT/ SECTOR (RADR), 04_{16}		
0	04_{16}	Subsystem	Transfers to Host the Last Track/Side/ Unit/Sector accessed by subsystem.
1	Track	Host	
2	Side/Unit/Sector	Host	
	READ (RD) 05_{16} READ THROUGH BUFFER (RDB), 07_{16}		
0	05_{16} or 07_{16}	Subsystem	Transfers data directly or through buffer to host. No. of sectors transferred depends on previous LDSC. If LDSC is not specified, one sector is read.
1	Track	Subsystem	
2	Side/Unit/Sector	Subsystem	
*	Data	Host	* No of bytes (sectors) specified by LDSC

Table 3-3. Command Summary (Continued).

	COMMAND	DATA FLOW TO	DESCRIPTION
	WRITE (WT), 06_{16} WRITE THROUGH BUFFER (WTB), 08_{16} WRITE WITH DELETED DATA MARK (WTD), 09_{16} WRITE THROUGH BUFFER WITH DELETED DATA MARK (WTDB), $0A_{16}$		
0	06_{16}, 08_{16}, 09_{16}, or $0A_{16}$	Subsystem	Transfers data directly, or through buffer, with or without deleted data mark to subsystem. No. of sectors written depends on previous LDSC. If LDSC is not specified, one sector is written.
1	Track	Subsystem	
2	Side/Unit/Sector	Subsystem	
*	Data	Subsystem	
	COPY (CPY), $0B_{16}$		Copy number of sectors specified by LDSC from source (Track/Side/Unit/Sector) to destination (Track/Side/Unit/Sector).
0	$0B_{16}$	Subsystem	
1	Source Track	Subsystem	
2	Side/Source Unit/Sector	Subsystem	
3	Destination Track	Subsystem	
4	Side/Destination Unit/Sector	Subsystem	
	FORMAT TO IBM SINGLE DENSITY, $0C_{16}$ (TRACK 00 WITH 26 SECTORS),		Formats media as follows: Track 00, Side 0: 26 sectors single density. Track 00, Side 1: 26 sectors single density. Tracks 01-76, sides 1 and 2: 26, 15 or 8 sectors (as specified), single density.
0	$0C_{16}$	Subsystem	
1	Side/Unit/Number Sectors in TK01-TK76	Subsystem	
	FORMAT TO SINGLE DENSITY, $0D_{16}$		Formats media as follows: Tracks 00-76, sides 0 and 1: 26, 15 or 8 sectors (as specified), single density.
0	$0D_{16}$	Subsystem	
1	Side/Unit/Number Sectors in TK00-TK76	Subsystem	
	FORMAT TO IBM DOUBLE DENSITY, $0E_{16}$ (TRACK 00 WITH 26 SECTORS),		Formats media as follows: Track 00, side 0: 26 sectors, single density. Track 00, side 1: 26 sectors, double density. Tracks 01-76, sides 0 and 1: 26, 15 or 8 sectors (as specified), double density.
0	$0E_{16}$	Subsystem	
1	Side/Unit/Number Sectors in TK01-TK76	Subsystem	
	FORMAT TO DOUBLE DENSITY, $0F_{16}$		Formats media as follows: Tracks 00-76, sides 0 and 1: 26, 15 or 8 sectors (as specified), double density.
0	$0F_{16}$	Subsystem	
1	Side/Unit/Number Sectors in TK00-TK76	Subsystem	

* No. bytes (sectors) specified by LDSC

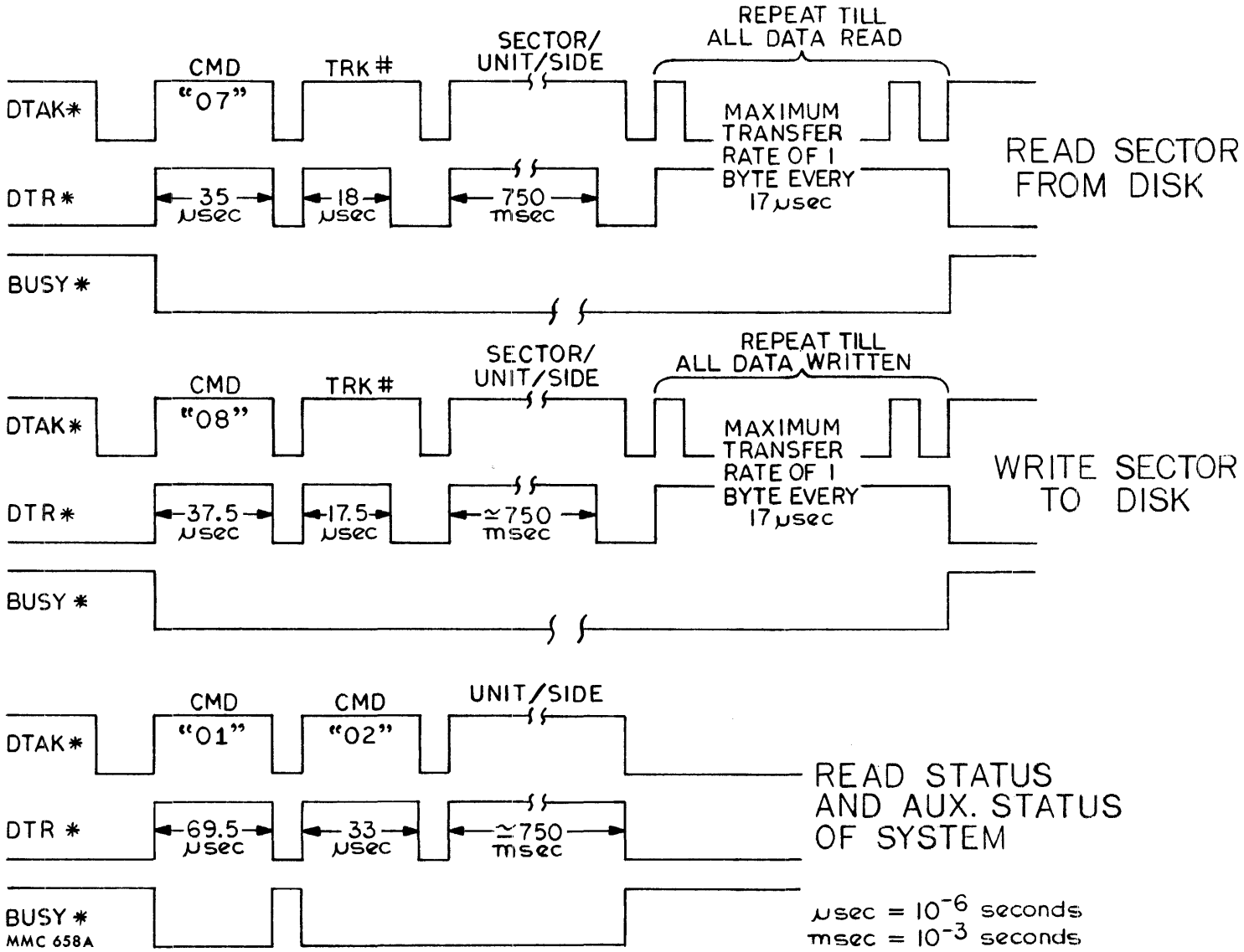


Figure 3-3. Relative Event Sequence for Read (07_{16}) Command, Write (08_{16}) Command, Read Status (01_{16}) and Aux. Status (02_{16}) Command.

3.4.3 SYSTEM READY

In this state, the subsystem is in an idle state waiting for a command from the host. BUSY* is high, DTR* is low, DDOUT* is high and ERROR* may or may not be asserted. When the host sets the DTAK* line, the subsystem will read the data bus, clear the DTR* line, exit System Ready and attempt execution of the specified command.

3.4.4 BOOTSTRAP

This mode is used to transfer data from unit 0, track 00, side 0, sectors 01 and 02 to the host thru the buffer when the subsystem receives a command code of 00_{16} from the host. The subsystem will present each byte to the host as it is requested, for the entire two sectors of data.

3.4.5 READ MAIN AND AUXILIARY STATUS

Read Main Status mode causes the subsystem to retrieve its primary (ERROR) status byte (item E, Figure 3-2) and send it to the host. This mode is entered when the host transfers a command code of 01_{16}. This byte is valid only if ERROR* was set at the completion of any function except Format. After a format, if ERROR* is not set, Read Status will return the number of Bad Tracks written. A successful Read Status will clear ERROR*.

Read Auxiliary status mode causes the subsystem to assemble the auxilary status byte (item F, Figure 3-2). This mode is entered when the host transfers a command code of 02_{16}. The process is similar to Read Main Status except the host must transfer the desired side and unit to the subsystem with a second byte (see Figure 3-2, item C for side and unit bit definition).

3.4.6 LOAD SECTOR COUNT

Load Sector Count mode will cause the subsystem to request the high and low order bytes, respectively, of the desired number of sectors to be transferred or copied. Use of this command is optional. Without this command the subsystem will default to a single sector transfer or copy. This mode is entered when the host transfers a command code of 03_{16}.

For multiple sector operations, the subsystem will automatically access the next contiguous sector and will continue to the last sector in the track. It will then access sector 1 of the next track on the same side.

NOTE

Any multiple sector transfer (including "copy" must be of identical sector sizes. An encounter of a different sector size will return an error status of 12_{16}.

3.4.7 READ LAST TRACK/SIDE/UNIT/SECTOR

Read last track/side/unit/sector mode will cause the subsystem to send the last accessed track # and side/unit/sector (two bytes or three bytes if

sector $\geq$ 32), respectively, to the host. This mode is entered when the host transfers a command code of 04_{16}.

3.4.8 READ DATA

Read Data mode will cause the subsystem to request a track# byte and a side/unit/sector byte. It will find the requested sector and transfer it to the host. This mode is entered when the host transfers a command code of 05_{16} for read data without buffer or 07_{16} for read data with buffer. 05_{16} transfers data directly from the disk to the host at a rate of one byte every 16µs (double density) while 07_{16} stores the data in the subsystem's buffer and transfers it to the host asynchronously. Multiple contiguous sectors may be transferred by preceeding the command with the optional Load Sector Count Command.

3.4.9 WRITE DATA

Write mode will cause the subsystem to request a track# byte and a side/unit/sector byte from the host. It will then find the requested data and transfer it to the host. This mode is specified by command codes of 06_{16}, 08_{16}, 09_{16} and $0A_{16}$. The 06_{16} code defines a normal write operation without a buffer, the 08_{16} code specifies a normal write operation with a buffer, the 09_{16} code is the same as 06_{16} and $0A_{16}$ is the same as 08_{16} except the Sector Data Mark (transparent to the user) will be a $F8_{16}$ instead of FB_{16}. During subsequent reads of a Deleted Data Select, this causes the ERROR* to be set and the Deleted Data bit to be set in the Status byte. A write operation without a buffer requires that the host transfer data at a rate of one byte every 16 µsec (double density) while the use of the buffer allows the transfer rate to be totally dependent on the host and may proceed at a much slower rate. Multiple contiguous sectors may be transferred by preceeding the command with the optional Load Sector Count Command.

3.4.10 COPY

Copy mode will cause the subsystem to request a track# byte and a side/unit/sector byte for the start of the source data to be copied and the track* byte and the side/unit/sector byte for the start of the destination of the copied data. This mode is entered by a $0B_{16}$ command from the host. Copy continues until the number of sectors (number specified in the Load Sector Count) have been copied or until an error condition occurs. Copy can be made from one part of a diskette to another, but the host must insure no unintentional overlay of source and destination data occurs. Multiple contiguous sectors may be transferred by preceeding the command with the optional Load Sector Count Command.

NOTE

An attempt to copy beyond the last sector of the source or destination media will return an error status of 3_{16}.

3.4.11 FORMAT

Format mode will cause the subsystem to request from the host a byte of data which specifies the number of sectors per track (bits 0-4); the logical unit address (bits 5 and 6) and the side (bit 7). Only the specified side of the media will be formatted to allow different formats on each side or preserve data on a side. This mode is entered when a code of OC_{16}, OD_{16}, OE_{16} or OF_{16} is received from the host. OC_{16} and OD_{16} are used with single density formats and OE_{16} and OF_{16} are used with double density formats. The difference in the commands is that each code specifies a unique format to which the media is initialized. Command OC_{16} will cause the entire media to be formatted in single density with track 00, sides 0 and 1 formatted in 26 sectors of 128 bytes each. Tracks 01 through 76 may be formatted into 26 sectors of 128 bytes each, 15 sectors of 256 bytes each or 8 sectors of 512 bytes each depending upon whether 26, 15 or 8 has been entered in the sector portion of the side/unit/sector byte. Command OD_{16} is the same as OC_{16} except all tracks are formatted into 26, 15 or 8 sectors.

Command OE_{16} will cause track 00, side 0 to be formatted in 26 sectors of 128 bytes each, single density and track 00, side 1 to be formatted in 26 sectors 256 bytes each, double density. Tracks 01 through 76 on both sides are formatted into 26 sectors of 256 bytes, 15 sectors or 512 bytes, or 8 sectors of 1024 bytes each, double density, depending on whether a 26, 15 or 8 has been entered in the sector portion of the side/unit/sector byte. Command OF_{16} is the same as OE_{16} except all tracks are formatted in 26, 15 or 8 sectors, double density.

Format mode is entered from the System Ready state by a OC_{16}, OD_{16}, OE_{16} or OF_{16} command from the host. The host next places the side/unit/number of-sectors-per-track byte on the data bus. The subsystem inputs the data and begins the operation. Upon completion the subsystem will enter the System Ready state.

A unique (non-IBM) 46 sectors/track, 128 bytes/sector, double density format is available. It should be used with the OF_{16} command only. Because 46 cannot be expressed with the 5 bits normally used to designate the number of sectors/track (format) or sector # (read, write or copy), a provision in the subsystem allows these bits to be zeros which will cause it to request another byte specifying the number of sectors/track(46_{10}) or the desired sector number (32_{10} to 46_{10}). Side and unit bits must be valid in the previous byte. Figure 3-4 shows an example of the command structure for 05_{16} read command by comparing a 26 and a 46 sector format. Figure 3-5 shows the same comparison using a OF_{16} format command.

NOTE

Because of internal timing considerations, the 46 sector/track format is done in a 2 sector interleave (i.e. 1, 24, 2, 25 etc.).

PARAMETER	SECTOR 25 (26 SECTORS/TRACK)	SECTOR 33 (46 SECTORS/TRACK)	
Command	0000/0101	0000/0101	
Track	0000/0010	0000/0010	
Side/Unit/Sector#	Side Unit Sector#: 1 | 01 | 1/1001	Side Unit Sector: 1 | 01 | 0/0000	Sector # = 0 will cause DTR* for sector number in fourth byte.
Sector Number	N/A	0010/0001	

Figure 3-4. Comparison of a Read (05_{16}) command between a 26 sector and 46 sector format. In each case Track 2, Side 1, Unit 1 are selected.

PARAMETER	26 SECTORS/TRACK	46 SECTORS/TRACK	
Command	0000/1111	0000/1111	
Side/Unit/#Sector	Side Unit#: 1 | 01 | 1/1010	Side Unit#: 1 | 01 | 0/0000	#Sectors = 0 will cause DTR* for number of sectors in third byte.
Number of Sectors	N/A	0010/1110	

Figure 3-5. Comparison of a OF_{16} format command between a 26 sectors/track and 46 sectors/track format. In each case, side 1 and unit 1 are selected.

3.4.12 READ READY STATUS ①

This mode is entered by transferring a command code of 10_{16} after all read/write heads are unloaded (approximately 600 msec after a disk access or when "Busy" goes false after a "Master Reset"). The "Read Ready" command will also unload the head; but the "Ready Status" returned will represent the previous head "Unloaded" status (i.e., execute "Read Ready" to terminate head load time-out and unload immediately, then execute again to get current "Ready Status"). The command is similar to the"Read Status"except that it transfers the current "Ready" status (media inserted and rotating) of all drives in the least significant four bits and the "Ready Changed" status in the four most significant bits. The ready status (LS 4 bits) indicates that a drive is not ready (i.e., either no media in place or the

① These commands are available only with Z36 chip (P/N 114259-001) revision E or higher. Refer to P.C. Card assembly. The revision letter is marked on the chip.

media is not rotating or the door is not closed), by setting it's respective bit in the status byte. The "Ready Changed" status bits indicate a change has occurred in the "Ready Status" since the last time this command was executed (the corresponding "Ready" bit has changed at least once). The "Ready Changed" bits are reset after each "Read Ready" access. The "Ready Changed" bits are considered invalid after a "POWER-ON" or master reset and must be initialized by executing the "Read Ready" command. The following command structure is used:

Byte	Command								Data Flow To
0	MS			10_{16}				LS	Subsystem
1	Unit 3	Unit 2	Unit 1	Unit 0	Unit 3	Unit 2	Unit 1	Unit 0	Host

Ready Changed Bits
1 = Status Changed

Ready Bits
1 = Not Ready

3.4.13 SPECIAL MAINTENANCE COMMANDS ①

Command 11_{16} is a special function command that facilitates the mechanism alignment and is useful when making certain mechanical and electrical tests. The command byte is followed by two additional bytes as follows:

Byte #	Command	Data Flow To
0	11_{16}	Subsystem
1	Track #	Subsystem
2	Side/Unit/Sector (Sector bits ≠ 0)	Subsystem

This command will cause the selected unit to step the head to track 00, load the head, and then step to the physical track specified by byte 1. The head will remain loaded to allow monitoring of the read amplifier signals. While in this mode, the system will accept additional single byte transfers, interpret them as track numbers and reposition the head. A track # byte greater than 76_{10} will cause an exit from this command. Upon exit, the track 0 bit (bit 2) and the write protected bit (bit 6) are set if either condition is true, and may be accessed using a Read Status command.

Upon exit, the head will remain positioned over the previously selected track. Reissuing the 11_{16} command and substituting FC_{16}, FD_{16}, FE_{16} or FF_{16} in the track # byte instead of the track # will cause the subsystem to perform additional functions which are helpful in certain maintenance procedures. Byte 2 which includes side/unit/sector (sector ≠ 0) must also be included. FC_{16}, FD_{16}, FE_{16} and FF_{16} perform the following functions:

① This command is available only with Z36 chip (P/N 114259-001) revision E or higher. Refer to P.C. Card assembly. The revision letter is marked on the chip.

FC - Head Bounce. This command loads and unloads the head repeatedly on the previously accessed track. The duration of each load and unload is approximately 225 msec. This command is useful in checking head settling time by triggering an oscilloscope on the head load signal and measuring the time until the amplitude modulation subsides.

FD - 2 μsec. Pulse. This command will write pulses at 2 μsec intervals on the previously accessed track.

FE - 4 μsec. Pulse. This command will write pulses at 4 μsec intervals on the previously accessed track.

NOTE

After writing, the subsystem remains in the track positioning mode i.e., additional single byte transfers are interpreted as track #'s and the head is repositioned. No writing is performed. Exit this mode by transferring a track # byte greater than 76_{10}.

FF - Head Clean (or Step). This command moves the head to track 00, loads the head and them steps at a rate of approximately 300 msec. per step out to track 76_{10}. This command is useful when checking head settling time after a step or when using a head cleaning diskette.

3.4.14 POWER DOWN MODE

During D.C. power down when +5V drops below +4.3V, all write circuitry is deactivated to prevent inadvertent writing on or erasing of the diskette.

3.5 ERROR DETECTION AND CORRECTION

3.5.1 WRITE ERROR

If a data error occurs during a write operation, and is detected on the next revolution by doing a read operation, commonly called a "write check", to correct the error, another write operation must be done. If the write operation is not successful after 4 attempts have been made, that sector or track should be labeled defective and writing should be attempted on an alternate track. If the error still persists, the Diskette should be considered defective and discarded.

3.5.2 READ ERROR

Most errors that occur will be "soft" errors' that is by performing an error recovery procedure the data will be recovered.

Soft errors are usually caused by:

a. Airborne contaminants that pass between the read/write head and the disk. These contaminants will generally be removed by the cartridge self-cleaning wiper.

b. Random electrical noise which usually lasts for a few micro-seconds.

c. Small defects in the written data and/or track not detected during write operation which may cause a soft error during a read.

The following prodedures are recommended to recover from the above mentioned soft errors:

1. Reread the sector 10 times or until such time as the data is recovered.

2. If data is not recovered after using Step 1, access an adjacent track in the same direction previously moved, then return to the desired track.

3. Repeat Step 1.

4. If data is not recovered, the error is not recoverable.

Errors attributed to the Diskette will not be included in determining the Non-Recoverable Read Error Rate.

3.6 INITIAL CHECKOUT

This procedure should be used to determine that the subsystem is operational. The procedure assumes that the unit is installed and the I/O and power cables are connected.

a. Apply AC power to unit and visually check that the spindle rotates.

b. Apply a write command to the unit with a non-write protect-ed diskette inserted and write a sector of data.

c. Read back the sector of data written in step b and confirm no data errors.

d. Remove command signals and AC power from unit.

SECTION IV

THEORY OF OPERATION

4.1 BLOCK DIAGRAM DESCRIPTION

The RFS4810 and 2410 master drives and RFS4820 and 2420 slave drives are designed as a peripheral subsystem to be attached to or made a part of a host system. Figure 2-1 shows the interconnection between the host, the master and up to three slave units. All interfacing is between the host and the master. In turn, the master drive controls the slave units as directed by the host.

The master drive has the following functional characteristics: (1) the ability to accept 8-bit data parallel bytes and place them into a 26, 15 or 8 sector format, (2) to receive and generate control signals, (3) position the read/write head to selected tracks on both the master and slave and (4) write or read data from either its own diskette or from a diskette in one of the slave units. Figure 4-1 shows the functional block diagram for the RFS4810 and RFS 4820 units. Items contained only on the RFS4820 only are so indicated. The block diagram for the RFS2410 and RFS2420 is identical except for only one read head.

Both the master and slave drives are composed mainly of the following items: diskette drive mechanism, head positioning mechanism, head load actuator, safety and control electronics, read/write electronics, and the read/ write head itself.

4.1.1 DISKETTE DRIVE MECHANISM

A belt drive system which uses a synchronous motor assembly is used to rotate the diskette spindle at 360 rpm. By changing the pulley and belt, either 50 or 60 Hz power can be accommodated. A registration cone, centered on the face of the spindle, positions the diskette and a clamp which moves in conjunction with the door latch handle fixes the diskette to the registration cone.

4.1.2 HEAD POSITIONING MECHANISM

A split band/stepper motor system is used to position the read/write head(s). The two phase stepper motor assembly is set up so that each 3.6^{o} rotation of the stepper moves the read/write precisely on track.

4.1.3 READ/WRITE HEAD

The head used in the RFS4800 and 2400 series is a read/write head with tunnel erase and the contact surface is made of a ceramic material designed for maximum head life and minimum head and diskette wear. When loaded the head is in direct contact with the diskette and has been designed to obtain maximum signal transfer to and from the magnetic surface.

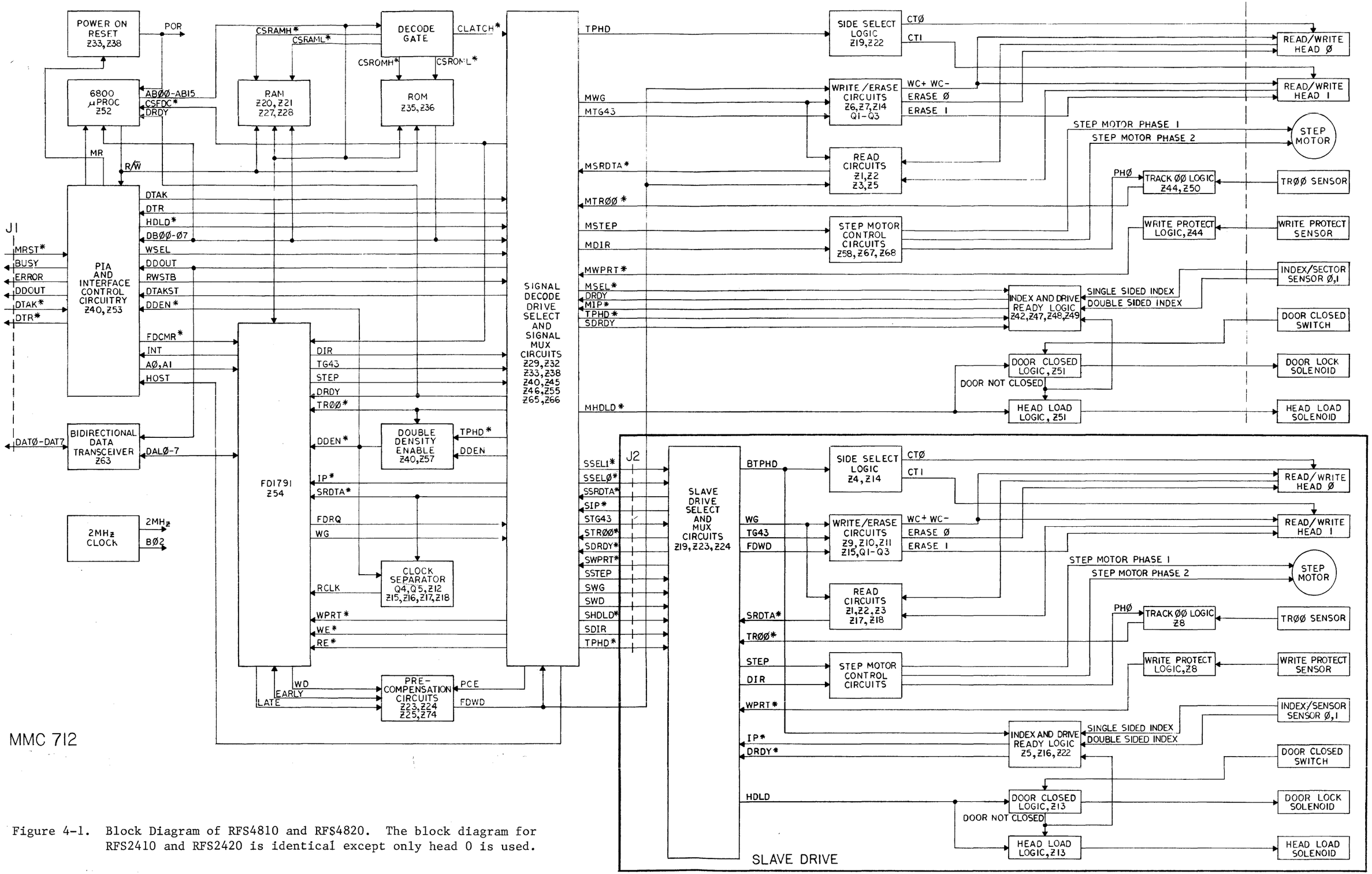
The tunnel erase gaps are part of the complete head but trail the read/write gap. Their function is to trim the read/write track width to 13 mil typical. This is to insure diskette interchangeability as well as IBM compatibility.

4.1.4 ELECTRONICS

Figure 4-1 combines the block diagrams of both the master and the slave. The indicated blocked area shows the slave; the remaining area of the drawing shows the signal flow and block diagram for the master. Both drives contain the control electronics which operate the head load solenoid, stepper motor, read/write circuits and change the analog head signals into a digital output. In addition, each slave contains a drive select circuit which allows commands and data to be received and/or sent provided that drive has been selected. The master drive is the more complicated since it additionally contains the 6800 microprocessor and associated RAM and ROM modules, the interfacing circuitry to the host, the FD1791 formatter and the multiplexing circuits which select either the master drive or one of the slave drives.

Section 3.4 describes the various command codes which are applied from the host to the master drive via the DAT0*-DAT7* data lines. A microprocessor system, consisting of an MC6800, one or two PROM's, four 2114 RAM's, one MC6821 PIA (Peripheral Interface Adapter) is used to decode these commands and generate the necessary control signals to the FD1791 formatter chip. The FD1791 provides signals for controlling the selected drive electronics and for transferring read/write data between the drive and the rest of the system.

A group of circuits labeled Drive Select and Signal Mux circuits are used to select either the master drive or one of the slave drives. Physical drive selection is controlled by the microprocessor system and jumpers. All input/output signals to and from the drives are routed through a multiplexer arrangement. If a slave drive is selected, the signals are applied in parallel to all slave drives. The SSEL0 and SSEL1 select signals activate the chosen drive circuits and only that drive recognizes the control signals from the master and transmits the output signals back to the master. Depending upon the drive selected, the control signals from the FD1791 are then routed to that drive and the input signals from that drive are applied to the FD1791. Signals to and from the other drives are inhibited since only one slave drive can be active at one time.



MMC 712

Figure 4-1. Block Diagram of RFS4810 and RFS4820. The block diagram for RFS2410 and RFS2420 is identical except only head 0 is used.

4.1.5 SYSTEM MNEMONICS

Data and control lines are identified with abbreviations or mnemonic terms to indicate the function or identity of the signal. Table 4-1 lists these terms in alphabetical order and gives the full names, origin (sheet and zone coordinates) and a brief description of their function.

4.2 FUNCTIONAL DESCRIPTION

The following paragraphs describe the functional operation of the electronics in the master and slave drives. In some cases functional block diagrams are used to illustrate circuit operation. When references are made to the schematic, the sheet and zone number are included to enable the reader to easily and quickly find the specific referenced component or logic element. The schematic sheet and zone references appear as parenthetic suffixes. E.g., the unit number select pins R,P,N,M,L and K for the master drive is located on Figure 8-5 at (9E6 and 9D6) i.e., sheet 9, zones E6 and D6. Before proceeding with the theory section, it is recommended that reader review the command codes given in Section 3.

4.2.1 MICROPROCESSOR SYSTEM

The microprocessor (μP) system consists of an MC6800 μP, four 1024 x 4 - bit static 2114 RAM's, one 4K or two 2K x 8 ROM's or erasable PROM's and one MC6821 PIA (Peripheral Interface Adapter). Working in conjunction with the microprocessor system is the FD1791 controller which is described in Section 4.2.2. The use of the microprocessor has considerably reduced the amount of software overhead required in the host system by taking over many of the operational functions. To set up a starting location, to transfer data to or read data from the media, the host system presents the command byte and the desired side/unit/track and sector in the following 2 bytes. It will locate that sector thru all the necessary steps: Read ID, CRC checks and retry operations until the desired track and sector are found. It will also notify the host in the event it cannot locate the requested track or sector.

The MC6800 is a bidirectional, bus-oriented 8-bit parallel processor with 16-bit addressing capability. The processor interfaces to the other elements via the on-chip control lines. Z62 on sheet 6 of Figure 8-5 is used to decode address lines AB02 thru AB15 into signals which select the high RAM (CSRAMH*) the low RAM (CSRAML*), high PROM (CSROMH*), the low PROM (CSROML*) or a latch (CLATCH*) which provides the control signals to various elements of the drive and PIA. Complete descriptions covering the μP, RAM, PROM and PIA are beyond the scope of this manual but are available from the manufacturer's literature.

One of three types of PROMs is used depending upon availability. PROMs 2532 and 2732 are 32K PROMs and the 2516 or 2716 are 16K PROMs. Z35 and Z36 are both used with the 2516 or 2716. Only Z36 is used with the 2732 or 2532 PROMs. Because of the different pin connections, different jumper configurations are used with each type of PROM as shown in the Table on sheet 7 of Figure 8-5.

The RAM is a 2114 static Random Access Memory organized as 1024 x 4 bits and used as the internal buffer. Four of these are used in the system, two for Data Bus DB00-DB03 and two for DB04 through DB07. These are shown on sheet 7 of Figure 8-5 as Z21, Z22, Z27 and Z28. Pin 10 of each RAM ($R/\overline{W}$) is tied to the μP $R/\overline{W}$ (6B5) and determines whether data is read from the RAM (high) or written into the RAM (low). As described later, two of the RAMs (Z20 and Z21) are used to store data from the PROMs during certain portions of the program.

The PIA 6821 chip is used to interface the μP with the drive and host and to control and transfer data. The one used in this system is shown as Z53 on sheet 6 of Figure 8-5. The PIA has two independent sides, each side consisting of an 8-bit data register and two control lines. The 16 data lines total may be programmed by the processor to be either input or output lines in any configuration. The four control lines can be programmed in numerous ways to act as outputs, edge triggered interrupt inputs and handshake type lines.

The system clock is generated by an 8 MHz crystal, Y1(6E3), which works in conjunction with an MC 6875 clock generator, Z37. Outputs ϕ_1 and ϕ_2 at pins 15 and 13 respectively, of Z37 are non-overlapping 2MHz clock signals required by the 68B00 microprocessor. The 4 MHz output at Z37-5 is divided down through F/F Z35 at pin 5 and used throughout the system for timing. At certain times in the program, it is required to read data from the PROM's at the double density rate. Because the PROMs which are employed are too slow to keep up with the high clock rate, during these portions of the program, the clock is slowed down to 1MHz. This is accomplished by the CSROMH* or CSROML* signal which are ORed at Z31-6 and applied to pin 9 of AND gate Z31 (6D3). The resulting OV output at Z31-8 is applied to Z37-6 causing the clock output to slow down to 1MHz. The data from the PROMs during this time are transferred slowly to the RAMs which are later used at the higher rate. When CSROMH* or CSROML* goes false, the clock generator is switched back to the higher 2MHz rate.

4.2.2 FD1791 CONTROLLER DESCRIPTION

The master drive makes use of the FD1791 Floppy Disk Controller, Z54, sheet 8 of Figure 8-5. This chip works in conjunction with the microprocessor to generate all the required control signals to position the read/write head to the desired track, to assemble the write data into the serial format, and to decode the data read from the diskette into 8-bit parallel data for presentation to host system. The internal operation of the FD1791 is beyond the scope of this manual but can be obtained from the manufacturer's literature. Only the external signals as they relate to the subsystem electronics are described below. These include eight Data Access lines, DAL, and other associated control signals used to accomplish the interfacing between the host and drive.

Data, Status and Control bytes are transferred into or out of the FD1791 by means of the DAL lines. These lines may contain data or are coded as described in Table 3-3, depending upon the operational mode. They are enabled as outputs by CSFDC* (pin 3) and RE* (pin 4) going low and are

enabled as input receivers when CSFDC* and WE* (pin 2) go low. If both RE* and WE* are high, the DAL lines are in a high impedance state. CSFDC*, is the output from the DB01 Data Bus line which is stored in the Z29 F/F (see Figure 8-5, sheet 9). The origin of WE* and RE* is described in Sections 4.2.3 and 4.2.4.

Data transfer into or out of the FD1791 is accomplished with CSFDC* true plus either RE* true during a read operation or WE* true during a write operation. A1 (pin 6) and A0 (pin 5) are used to address various registers in the FD1791 chip as follows:

A1	A0	RE*	WE*
0	0	Status	Command
0	1	Track	Track
1	0	Sector	Sector
1	1	Data	Data

A1 and A0 are outputs of the PIA chip (Z53-9 and Z53-8; 6D6). Data Request, FDRQ (Z54-38; 8C5) is set high in read when an assembled serial byte is ready for transfer to the host or buffer. FDRQ is cleared after data has been transferred. During write operations, FDRQ is taken true after the Data Register is empty and requires a new byte. It is reset when the Data Register is loaded with new data. FDRQ must be serviced before the next transfer is required (generally 16 μsec) or an error occurs which sets the Lost Data bit in the Status Register.

INTRQ (Z54-39) is activated upon completion of an operation or interruption of an operation due to an error condition. It remains set until a new operation is requested.

A 2MHz square wave clock is required at Z54-24 to control the internal timing and to clock some external flip-flops. A crystal oscillator, Y1 and its associated components produce the required 2 MHz square wave. A 8 MHz crystal is used but the Z37 clock generator is used to divide the frequency by two and Z32 further divides it by two to obtain 2MHz.

During write mode, the Write Gate (WG) output at Z54-30 is true allowing current to flow into the Read/Write head. The first data byte must be loaded into the Data register in response to a Data Request before the WG signal can be activated. This is done as a precaution against erroneous writing. The write data (WD) appears at pin 31. Writing is inhibited when the Write Protect* input (Z54-36) is low, in which case any write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set.

4.2.3 DIRECT MODE DATA FLOW OPERATION

In this mode, during read or write, data is transferred directly between the host and the FD1791. The processor only controls the data flow by use of the HOST*, DDOUT*, and CSFDC* lines and determines when the operation is complete by interrogation of the INTRQ* line.

4.2.3.1 Direct Read Operation

In this mode of operation the FD1791 provides data directly to the host via the DAT0* - DAT7* interface lines, through the Z63 Bidirectional Transceiver (8E7) via the DAL0* - DAL7* lines.

The sequence begins with the microprocessor sending the appropriate track and sector address data to the FD1791 via the PIA on the DB00 - DB07 and DAL0* - DAL7* lines. When the selected drive has located the proper track, INTRQ signals the microprocessor. The microprocessor sends a Read command to the FD1791 and then sets up the HOST* line (9C4), the CFSDC* line (9C4), and the DDOUT line (9C4) via Z29 (9C7) latch. The requested data is then read from the diskette, assembled by the FD1791 and placed one byte at a time on the DAL0* - DAL7* lines. The reading and 9 clock generation circuits are described in Section 4.2.7.

When a byte is ready for transmission, the FD1791 places the FDRQ signal (Z54-38) true (8C5). This signal is used to clock the Z32 flip-flop at pin 11 (9B6) since HOST* is true. The resulting Q output at pin 9 is applied through the Z46 OR gate at pin 1 and then delayed for five clock pulses at the Z45 shift register (9B3). The resulting DTR output at Z45-10 is then fed to the host via Z64-11 (6D7). Pin 3 of Z46 (9B5) is also used to place RE* true (WSEL is set low previously causing Z39-6 to be high). RE* is used to enable the output lines on the FD1791. The delay between RE* and DTR allows the data lines on the FD1791 to set up and be valid before the host accepts them. The host responds by reading data from the lines and setting DTAK true. DTAK is applied through J1-15 to Z64-13 (6D8) and out Z64 at pin 7 (6D7). It is then applied to Z40-1 (9B6) which resets Z32 at pin 13. RE* is then taken false (high) after which data can no longer be considered valid. This cycle is then repeated for each byte of data to be transferred.

If more than one sector is to be transferred the microprocessor will automatically address the next sector when data transfer from the present sector is complete. This will continue until all requested data is transferred.

4.2.3.2 Direct Write Operation

In write mode, a similar sequence to that described for read in Section 4.2.3.1 occurs except WSEL is true. FDRQ goes true when the FD1791 is ready to accept data. This sets Z32-9 high and generates a delayed DTR as described in Section 4.2.3.1. The host responds to the DTR by placing data on the line and setting DTAK true. DTAK resets Z32 which takes DTR false five clock cycles later and fires the Z33 one-shot at pin 5 (9B6). The resulting 460-500 ns DTAKST signal turns on WE* at Z38-6 which enables FD1791 at pin 2 (8C6). DTR is delayed to allow data to be valid for a short period after the trailing edge of WE*. FDRQ is then taken false while data is being assembled. When FD1791 is ready for the next byte to be transferred, FDRQ is taken high and the sequence is repeated. The

assembled data is applied to the Drive Select and Signal Mux Circuits via the WD line to the precompensation circuits at Z25-4 (11C8). The output of the precompensation circuits is the FDWD signal which is sent to the master and slave drives. The drive selected then writes the data.

4.2.4 BUFFER DATA FLOW OPERATION

Commands 08_{16} and $0A_{16}$ allow data to be transferred from the host to the buffer and then to the diskette. Command 07_{16} is the reverse in that data is read from the diskette, stored in the buffer and then transferred to the host. The following sections described these two operations. In addition a description of the copy operation is also included since it consists of both buffer read and write operations.

4.2.4.1 Buffer Write Operations

When a 08_{16} or a $0A_{16}$ command is recognized, the processor through the PIA generates a RWSTB signal at Z53-19 (6C6) which is applied to the OR gate at Z46-2 (9B5). The resulting signal at Z46-3 is fed to the shift register at Z45-1 (94B) where it is delayed for five clock pulses. The resulting DTR output at Z45-10 is fed to the host via Z64-11 (6D7). The host responds to the DTR by placing data on the line and setting DTAK* true. When DTAK goes high it fires Z33 one-shot at pin 5 (9B6). The resulting 460-500 ns DTAKST signal is used to signal the microprocessor that data is present. The subsystem accepts the data and clears DTR*. Data enters the system on the DAT0* - DAT7* lines, into the Bidirectional Transceiver Z63, thru the PIA via DAL0* - DAL7* lines and into the RAM by way of the DB00-DB07 lines. Another RWSTB is then generated and the sequence is repeated until a full sector is read in or the buffer fills.

When the sector is complete the microprocessor places the appropriate track and sector address on the DB00 - DB06 lines. The PIA transfers this data via the DAL0* - DAL7* lines to the FD1791. A search is then made for the proper track and sector. When the desired track and sector have been located by the selected drive, the FD1791 signals the processor via the INTRQ lines. The processor then causes a byte of data to be transferred from the RAM to the FD1791 using the same flow path as just described for the track and sector. In addition, the processor causes the WSEL and RWSTB lines to go high and sets the A1 and A0 lines to the selected state. RWSTB sets Z46-8 (9A5) high which places WE* true causing the FD1791 to read in the data. After WE* goes true, RWSTB goes false.

When data has been taken, the FD1791 places FDRQ true at Z54-38 (8C5) which is then applied to Z31-2 (9B6). Since HOST* is false and CSFDC is high, Z31-12 goes high. This fires the Z33 one-shot at pin 4, generating the Data Transfer Acknowledge Strobe, DTAKST, which indicates to the PIA at Z53-18 (6C6) that data has been taken.

The data is then formatted and put into serial form by the FD1791 which places it out on the WD line (8B5). The data is then recognized by the selected drive where it is written in the specified sector. (Write Circuits

are described in Section 4.2.8). When the FD1791 is ready for the next byte, FDRQ again goes true. This cycle continues until a full sector has been written at which time FDRQ no longer goes true. When the sector is complete, the Interrupt Request, INTR at Z54-39 (8B5) goes true to let the processor know that present routine is complete. Another sector is then transferred from the buffer or host and the process is repeated until all sectors specified in Load Sector Count Command have been written.

4.2.4.2 Buffer Read Operation

When a 07_{16} command is recognized, the processor loads the command as described for the Buffer Write Operation. The sequence begins with the microprocessor placing, in order, the appropriate track and sector address on the DB00 - DB07 line. The PIA transfers this data via the DAL0* - DAL7* lines to the FD1791. A search is then made for the proper track and sector. When the desired track and sector have been located by the appropriate drive, the data in that sector is transferred from the drive via the MSDTA* (master serial data) or SSRDTA (slave serial data) line depending upon the drive selected. The Mux Circuits select the serial data (SRDATA) at either pin 9 or 12 of Z55 and routes it to the clock generator circuit. This circuit is contained on sheet 10 and used to generate the serial clock (RCLK) from the SRDATA signal. These signals are applied to the FD1791 at pins 26 and 27, respectively (8C6). The FD1791 then converts the data into 8-bit parallel form.

When the first byte of data has been assembled by the FD1791, it sets FDRQ true. FDRQ generates DTAKST as described in Section 4.2.4.1. When the PIA sees DTAKST, RWSTB is generated which places Z46-3 (9B5) high and causes RE* to go low. The data is then transferred from the DAL0* - DAL7* lines thru the PIA and into the RAM via the DB00 - DB07 lines. RWSTB is then removed. After the data has been taken, FDRQ goes false and the next byte of data is assembled. When the byte is ready, FDRQ again goes true and the process is repeated until the entire sector has been transferred into the RAM. At that time no more FDRQ's are generated and the INTRQ line goes true to indicate the routine is complete.

When data is ready to be transferred to the host, the processor sets RWSTB true which generates a delayed DTR as previously described. It also transfers the data from the RAM to the PIA over the DB00 - DB07 lines, to the Bidirectional Transceiver via the DAL0* - DAL7* lines and out to the host on the DAT0* - DAT7* lines. When the host has taken the data it responds with a DTAK. DTAK then generates DTAKST which tells the processor to place another byte on the lines. This sequence continues until the entire sector or buffer has been transferred. The next sector (if sector count $\neq 0$) is then loaded into the RAM and the process is repeated until all sectors specified in the Load Sector Count Command (03_{16}) have been transferred.

4.2.4.3 Copy Operation

An $0B_{16}$ command allows a number of sectors as specified in the Load Sector Count Command (03_{16}) to be moved from one specified source to a specified destination. In this operation, the same sequences described in Sections 4.2.4.1 and 4.2.4.2 are followed except no data (other than the commands) is transferred between the host and subsystem. The operation begins by locating the selected drive, track and sector. The first sector is read by the selected drive and transferred to the RAM as described in Section 4.2.4.2 for a buffer read operation. When the buffer is full or sector is complete, the processor directs a buffer write operation with the data from the RAM transferred to the first sector of the destination. This sequence is the same as the buffer wirite operation described in Section 4.2.4.1. The copy sequence continues until all the specified sectors have been transferred. It is the function of the host to insure that no unintentional overlay of data occurs.

4.2.5 FORMAT OPERATION

Command codes of $0C_{16}$, $0D_{16}$, $0E_{16}$ and $0F_{16}$ are used by the host to format a diskette depending upon format requirements. The difference in the four formats is described in Section 3.4.10. In this sequence the processor uses a program stored in the (P)ROM and places data on the DB00 - DB07 lines. The data is transferred thru the PIA to the FD1791 via the DAL0* - DAL7* lines. The operation is similar to the buffer write operation described in Section 4.2.4.1 except data originates from the preprogrammed ROM rather that the RAM.

4.2.6 DRIVE SELECT AND SIGNAL MUX CIRCUITS

Data and control signals for the various electromechanical drive functions originate from or flow to the FD1791. These signals include TR00*, IP*, WPRT*, TG43, DIR, STEP and WG. One other signal from the PIA, HDLD* is also used. These signals are all applied to or come from the buffer and line driver Z65 and Z66 or to (from) latch Z55 where they are routed to (or from) either the master drive or the parallel slave drives via J2. See Figure 8-5, sheet 9. The A pins of Z55 are inputs and the Y pins are outputs. Similarly, the D pins of Z66 and Z65 are inputs amd the Q pins are outputs. Either Z66 or Z65 and Z55 are selected depending upon whether the master or a slave is selected.

The unit select circuitry for the master drive is made at pins K, L, M, N, P and R as shown in the table on page 9 of Figure 8-5. The jumpers are arranged so that a given combination of pins 16 and/or 19 of Z29 and pins 11 and/or 3 of Z56 will cause Z46-11 to go high depending upon the unit number selected. For unit 0, R and P are jumpered and so are M and L which applies Z29, pins 15 and 16 directly to Z46, pins 13 and 12. Pin 11 or Z46 or its inversion at Z56-13 is used to route the drive control signals to either the master (Z46-11 is high) or the other slave units (Z46-11 low). Incoming signals are similarly accepted from the slave or master depending upon the unit selection made. When the slave signals are

selected, they are applied to all slaves in parallel. A similar jumper arrangement on each slave drive allows the transfer of signals between the master and only the selected slave drive. Signals SSELI* and SSELO* are used to select the particular slave.

4.2.7 READ CIRCUITS AND CLOCK GENERATOR

Figure 4-2 gives a block diagram for the read and write circuits. Figure 8-5, sheet 3 gives the schematic for the read circuits. When the diskette is being read, magnetized bits of prerecorded data are sensed by the selected read/write head. Either CT0 or CT1 from the Side Select logic (3B2) applies 0V to the selected head during read. The signal received from the head is in the form of a sine wave. This signal is amplified by Z5, filtered by the L1-L4 network (TP2, TP3) and differentiated by Z1. See Fig. 4-3. The differentiated signal is then applied to the zero cross-over detector Z2, pins 5 and 6 which generate a negative going pulse at pin 10 of approximately 800ns whenever a flux transition is sensed on the diskette. The pulses at pin 10 are used to clock F/F Z3 at pin 11 (3C3). The alternate Q and $\overline{Q}$ outputs at pins 9 and 8 trigger respective 150 $\pm$ 30ns one-shots at Z4-5 and Z4-11. The $\overline{Q}$ outputs from the one-shots are then gated at pins 4 and 5 of the Z11 OR gate, and inverted at Z26-11. This is the Master Serial Read Data (MSRDTA*) which is applied to the multiplex circuits shown on sheet 9. The output of the multiplex circuit is SRDTA* which is applied to the FD1791.

SRDTA* is also applied to the clock generator circuit shown on sheet 10 of Figure 8-5. Since double density applications contain no clock pulses in the data stream, this phase lock oscillator is used to generate the clock (RCLK) which will envelope the data. Z18 is a voltage controlled oscillator (VCO) which operates nominally at 4 MHz. Its output is divided by Z16 and in turn used to generate RCLK at Z17-1. Z12, Z15, Q4 and Q5 are used to track the frequency variations of the data pulses due to variations in the media rotation and, in turn, regulate the frequency of the VCO.

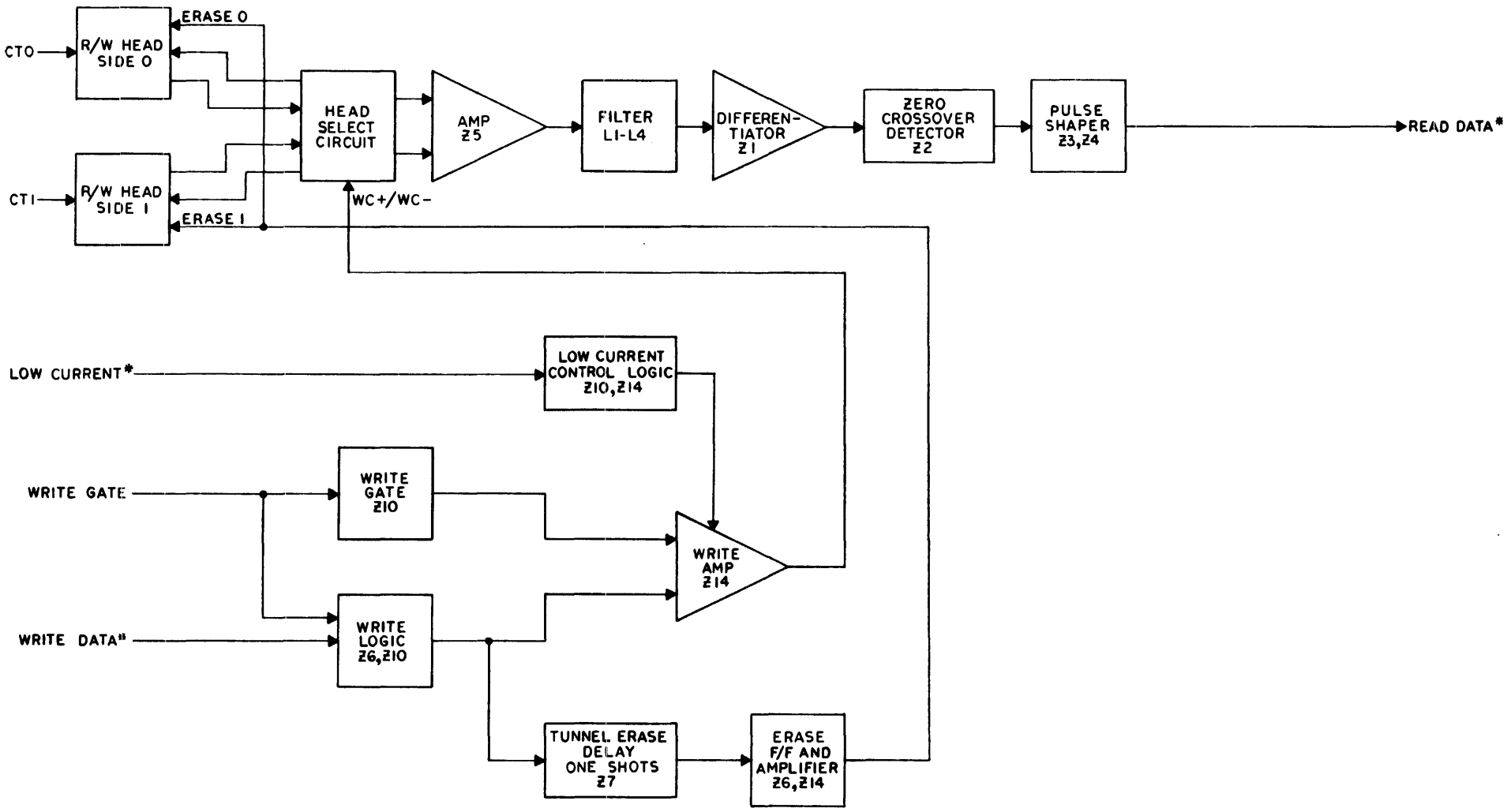


Figure 4-2. Read/Write/Erase Block Diagram.

4.2.8 WRITE CIRCUITS

Data to be written is generated by the FD1791 at pin 31 (8B5) as the WD signal. This signal is applied to the precompensation circuit shown on sheet 11 of Figure 8-5. Precompensation of write data compensates for the bit shift tendencies of data during read when double density schemes are employed. The FD1791 contains an algorithm which determines if each bit is to be shifted early, late or no shift at all. Along with each WD signal, the FD1791 may also generate an EARLY or LATE output which indicates the direction of the compensated bit shift. The EARLY or LATE signals enable F/F's Z74 which are clocked by WD and whose outputs are used by the data selector/multiplexer Z23 as described in the next paragraph.

The WD signal is also applied to the 0.9 to 1.0 μs one-shot, Z25 at pin 4 (11C8). The positive going Q output at pin 6 is applied through gates Z26 and causes the 150-250 ns one-shot at Z25-12 to fire. This one-shot is generally set for 170 ns. At the end of the 170 ns, Z25-9 goes high but since Z26-4 is still high, the one-shot is retriggered and continues oscillating in this manner for approximately 1 μs, i.e., until Z25-6 goes false. Pin 10 of Z25 is applied to the shift register Z24, causing pins 3, 4 and 5 to consecutively go true. Pin 3 is the Write Data Early (WDE), pin 4 is the Write Data On Time (WDOT), and pin 5 is the Write Data Late (WDL). These signals are then applied to the Data Selector/Multiplexer where, one of the inputs is selected depending upon whether B LATE or B EARLY or neither one is selected. The selected WD signal is then placed for the Flexible Disk Write Data (FDWD) output when the Precompensation Enable (PCE) signal is true. At the end of the 1μs one-shot, the shift regular at pin 9 is reset by Z25-6 going low. The precompensation circuits then wait for the next WD signal and its corresponding EARLY or LATE signal and the cycle is repeated.

The circuits which control the data and clock information to be written on the disk are shown in a block diagram in Figure 4-2 and on sheet 4 of Figure 8-5. Incoming composite write data (FDWD) is applied to pin 11 of the write F/F Z6 (4C6). The leading edge of each pulse in the write data stream triggers the F/F causing it to change state. Each output from the F/F at pins 9 and 8 controls identical drive amplifiers, Z14 at pins 2 and 6, respectively. As the F/F changes states, current is driven through one-side of the read/write head and then the other by means of the WC+ and WC- lines. When the F/F is set Z6-9 goes high and Z10-2 goes low causing current to flow in the WC+ line; When the F/F is reset, Z6-8 is high and Z10-4 is low causing current to flow in the WC- line. The F/F is enabled when the reset line at Z6-13 is high. This line is tied to the Write Gate* signal. If the signal goes false (high), the F/F will be held in the reset state and writing will be inhibited.

Z14 at pin 8 (4D3) provides constant current for the two write amplifiers Z14-1 and Z14-7. A 10mA peak-to-peak write current is used when writing

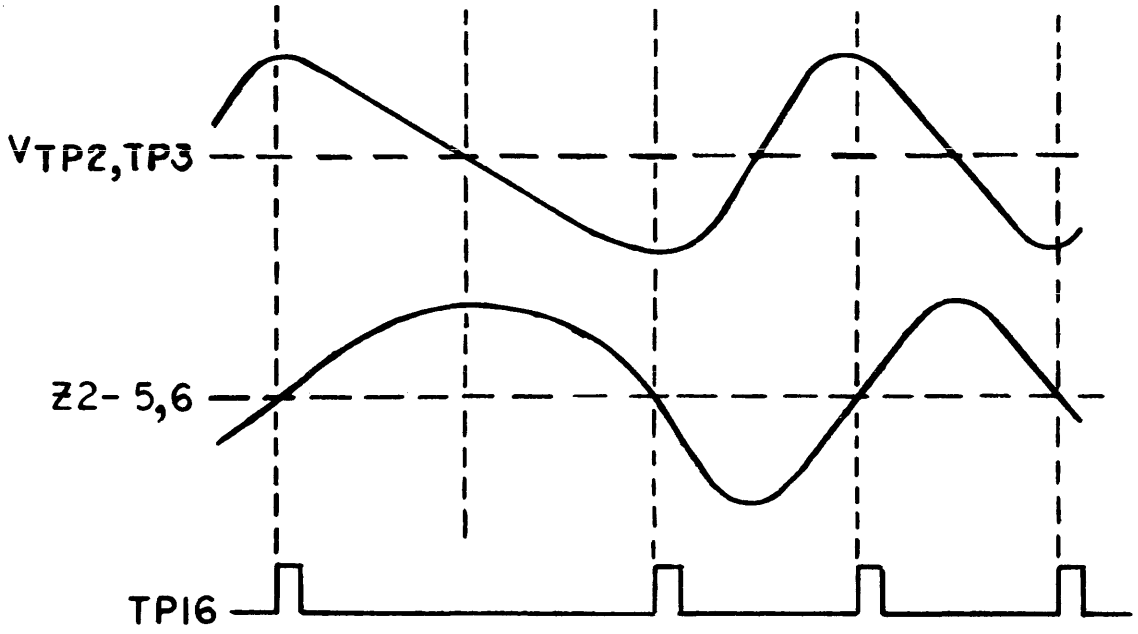


Figure 4-3. Read Circuit Timing Diagram.

on tracks 1-43. At this time the MTG43 input at Z10-5 is false (low), causing Z10-6 to be high. Current supply is essentially thru R34 to Z14-10. When writing on tracks 44-76, MTG becomes true causing Z10-6 to drop to OV. CR13 then becomes forward biased, shunting some current away from Z14-10. This results in a write current drop from 10mA peak-to-peak to 7mA. If MWG goes false, Z10-12 goes high which turns off Z14 at pin 9.

Q1, Q2 and Q5 serve to monitor the +5V supply and if it drops below +3.9Vdc, the write amplifiers and the erase amplifier are shut off. When power is first turned on, Q3 is shut off until the voltage reaches approximately +3.9Vdc. With Q3 off, Q1 is on causing OV to be applied to the anodes of CR9 and CR10, thereby inhibiting writing. Q2 is also on causing OV to be at Z11-12 (4B3) and thus inhibiting erasing. When the +5V level goes above +3.9Vdc, Q3 turns on and Q1 and Q2 turn off thereby enabling the write and erase circuits.

4.2.9 ERASE CIRCUITS

The erase element functions as a tunnel erase; i.e., it erases the area on both sides of the Read/Write track rather than the track itself. In this manner, the track is trimmed on both sides as the track is being written which eliminates stray interference between tracks. This also insures interchangeability between diskettes and drives. The erase gaps are located 0.036" behind the read/write gap.

The erase current must be turned on shortly after write data is present. Circuits controlling the automatic erase as shown on sheet 4 of Figure 8-5, zones B5, B4 and B3 and in Block Diagram form, Figure 4-2. When the first bit is to be written, the write flip-flop is set and Z6-9 goes high. On the second bit, the F/F is reset, Z6-9 goes low and triggers the 470-630µs delay one-shot at Z7-5. The Q output at Z7-6, in turn, triggers the 157-217 µsec delay one-shot at Z7-12. When Z7-9 again goes high it triggers the Z6 erase F/F causing pin 5 to go high. Since Z11-12 is high (providing power is up to operating level; see Section 4.2.8), Z11-11 will go low and turn on the erase amplifier at Z14-13. Z7-5 is a retriggerable one-shot which stays on as long as Z6-9 keeps changing states. When write data is no longer present, Z7-6 will be reset after the 470-630 µsec time out period. When Z7-6 goes low it resets F/F Z6 at pin 1 causing the erase amplifier to shut off. Thus it is seen at the beginning of a write operation, the erase current is delayed 157-217 µsec and at the end of write, the erase current remains on for 470-630 before turning off.

4.2.10 STEP MOTOR DRIVE CIRCUITS

The step motor control circuits are shown on page 5 of Figure 8-5. A two stage counter composed of the two Z58 flip-flops is used to produce four combinations of drive current through the motor phases. The counter is stepped with each MSTEP pulse. The direction of counting and, in turn, the in or out direction of the motor is determined by the MDIR line. Both signals are outputs from the FD1791. A high MDIR signal causes the motor to move the head in toward track 76 and a 0V level causes the motor to move the head out toward track 00.

The motor phases are driven by the Z67, Z68 amplifiers depending upon the state of the counter. Examining Z68, pins 4 and 5 first, when Q at Z58-6 is low, (Z68-4 is low) the associated transistor is shut off. Pins 5, 10, (1) and 1 are always high. This turns on Z67 at pin 11 causing current to flow out pin 10 through step motor phase 1, through the power resistor mounted on the chassis, through CR22, into Z68-9 to 0V (Z68-11 is high at this time causing its associated amplifier to be on). When Z58-5 is reset and goes low, Z68 is turned off at pin 11 and turned on at pin 4. Current flow through the Step Motor Phase is now reversed, coming from Z67-15, through the resistor and winding and CR24 and into Z68-6 to 0V. Figure 4-4 shows the timing diagram and the current flow paths for the various configurations of counter outputs. A mechanical damper is used to adjust the settling time of the motor after each step.

4.2.11 INDEX SECTOR CIRCUITS

Figure 8-5 , sheet 12 shows the schematic for the sector and index circuitry. A combination of a light emitting diode (LED) and photo sensor is used to sense the index and sector holes. When a hole in the diskette passes the sensor, a pulse is emitted an sensed by the Schmitt trigger Z42 at pins 8 an 12 for Index sensor 0 and pins 2 and 6 for Index sensor 1. The Schmitt trigger converts the hole sensor signals into a negative going

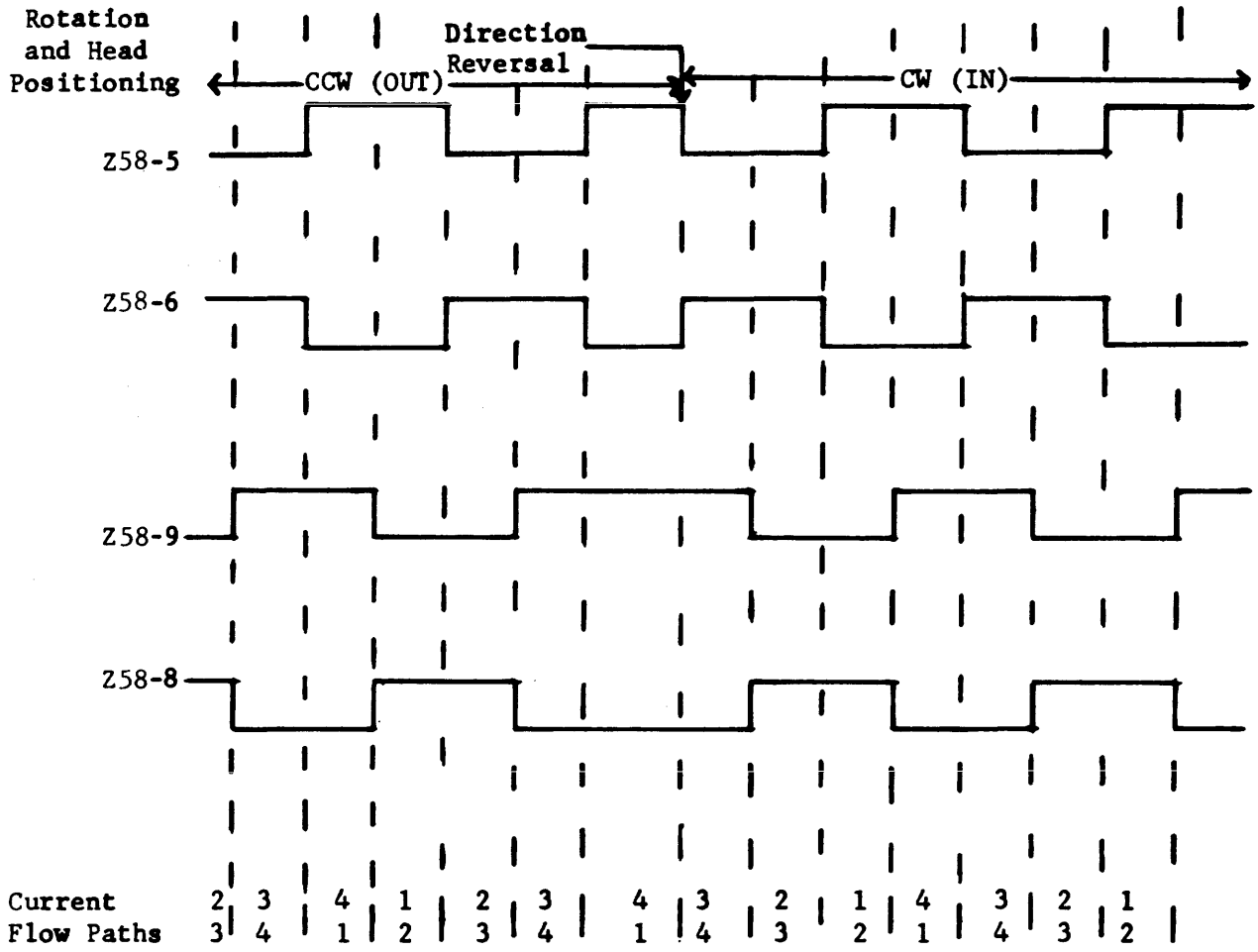


Figure 4-4. Stepper Motor Energizing Sequence.

pulse at standard TTL logic levels. Each Schmitt trigger output is fed to a 180-200ms one-shot, Z49. These are retriggerable so that each revolution keeps the one-shots fired. The single side index output at Z49-10 is gated with MSEL and TPHD* to give a true DRDY signal. Output Z49-6 is gated with MSEL to give DRDY. In the event a slave drive has been selected, the SDRDY from the slave is gated with MSEL* to give DRDY. The negative going output from Z42-9 and Z42-5 are also applied to Z48, pins 9 and 10 as a negative OR gate to give the MIP* signal.

4.2.12 WRITE PROTECT AND TRACK 00 CIRCUITS

The write protect circuit is shown on Figure 8-5, sheet 12. The uncovered write protect notch in the diskette jacket is sensed by the combination of a light emitting diode (LED) and photo sensor. When the uncovered notch is sensed, a dc level is applied to the Write Protect Schmitt trigger, Z44 pins 2 and 6 (12D7). This Schmitt trigger converts the notch sensor signal into the negative going MWPRT* signal. This signal is applied to the multiplex circuits shown on sheet 9. Similarly the TR00 switch is sensed by Z44-12, is inverted at Z50-10 and applied to the multiplex circuits.

4.2.13 POWER ON RESET AND MASTER RESET CIRCUITS

The Power On Reset (POR) and Master Reset Circuits are shown on sheet 6 of Figure 8-5 (6D2). When a Master Reset from the host is given at J1-13 (6D8), pin 18 of Z64 (6D7) and pin 11 of Z33 (6D2) go low. This triggers the 10-12 μs one-shot, Z33, causing Z38-10 to go low. In turn Z38-8 goes high (POR) and Z38-11 goes low (POR*) which resets various logic functions on the card. The POR and POR* signals are also generated when power is first turned on. When power is applied and reaches its operating level, pin 14 of Z37 (6E4) remains low for a short period of time causing Z38-8 to go high and Z38-11 to go low.

4.3 SLAVE DRIVE CIRCUITS

Figure 8-6 gives the schematic for the 114181-001 circuit card used on the slave drive. As noted in Section 4.2, most of the circuits are identical to those described for the master drive. Sheet 2 gives the read circuitry and the resultant SRDTA*. The write circuitry is shown on sheet 3. Sheet 4 gives the step motor circuitry. Sheet 5 contains the unit select circuitry which enables the transfer of signals between slave multiplex circuits and the master drive. The unit select circuitry which decodes the SSEL0* and SSEL1* lines is identical to the master drive. Sheet 6 shows the formation of the TR00*, WPRT*, DRDY*, and IP* signals which are the same as the master drive. The door lock and head load solenoid circuits are also the same.

Table 4-1. Signal Mnemonics

SIGNAL	SOURCE	DEFINITION
A0, A1	6D6	Address Bits 0 and 1. These are PIA outputs used to address the various registers within the FD1791.
AB00- AB11	6A1	MPU Address Bit 00-11. Microprocessor address lines used to address the various logic and memory chips.
B/EARLY	11C5	Buffered Early. Output from the Early F/F used to select early data in the pre-compensation circuits.
B/LATE	11B5	Buffered Late. Output from the Buffered F/F used to select late data in the pre-compensation circuits.
CLATCH*	6C1	Control Latch. Decoded signal from the microprocessor address lines used to enable the Z29 latch which stores the MPU Data Bus lines and, in turn, certain control signals.
CSFDC CSFDC*	9C4	FD1791 Chip Select. Decoded signals from the microprocessor data bus lines which enable the FD1791 controller.
CSRAMH* CSRAML*	6B1 6C1	High and Low RAM Chip Select. Decoded signal from the microprocessor address lines used to enable the RAM chips Z20 and Z21 (low) and Z27 and Z28 (high).
CSROMH*	6C1	ROM (HIGH) Chip Select. Decoded signal from the microprocessor address lines used to enable the high ROM, Z36.
CSROML*	6C1	ROM (LOW) Chip Select. Decoded signal from the microprocessor address lines used to enable the low ROM, Z35.
CT0, CT1	3B1	Center Tap 0,1. Used to enable Read/Write Head 0 or 1.
DAL0*- DAL7*	6C8	Data Bus Bits 0 - 7. Used to transfer data, status and commands among the FD1791, PIA, and Bidirectional Data Transceivers.
DB00- DB07	6E8	Microprocessor Data Bus 00 - 07. Used to transmit data, status and commands among the PIA, RAM, ROM's and microprocessor.
DDEN DDEN*	9C1 8D1	Double Density Enable. Signal which indicates drive is set for double density coding.
DDOUT	9C4	Data Direction Out. Decoded signal from the microprocessor data bus lines which when true indicates that data is flowing from subsystem to host.
DIR	8C4	Direction of Read Step. +5V signal causes head to move in; 0V causes head to move out.
DRDY	12D3	Drive Ready. Input to the FD1791 which indicates the selected drive has a disk rotating.
DTAK*	6D7	Data Transfer Acknowledge. Input from the host equipment which acknowledges that data has been placed on or taken from the data bus depending upon the operation.
DTAKST	9B4	Data Transfer Acknowledge Strobe. Input to PIA which indicates data has been taken (or received).
DTR	6D7	Data Transfer Request. True signal indicates that the drive subsystem requires data or has placed data on the data bus depending upon the operation.
EARLY	8D5	Write Data Early. Output from the FD1791 which is used to select the early data from the precompensation circuit.
ERASE 0,1	4B2 4A2	Erase Head 0,1. Output to the erase head 0 or 1 which causes it to energize.
FDCMR*	6D7	Floppy Disk Chip Master Reset. Output from PIA used reset the FD1791 chip.
FDWD	11D3	Floppy Disk Write Data. This is WD signal which has been precompensated.
FDRQ	8C4	FD Chip Data Transfer Request. Output from the FD1791 requesting a data transfer.
HDLD*	6B6	Head Load. Output from Head Load circuit which energizes the Head Load Solenoid.
HOST*	9C4	Host. Signal from the microprocessor data bus line which indicates data transfer to the host is required.
INTR	8B3	Interrupt Request. Output from FD1791 which is set at the completion or termination of any operation and is reset when a new command is loaded.
IP*	9E5	Index Pulse. True signal indicates index hole in the media has been sensed.
LATE	8D5	Write Late Data. Output from the FD1791 which is used to select late data from the precompensation circuit.
MDIR	9D4	Master Direction. Same as DIR except specifically for the master drive.
MHDLD*	9D4	Master Drive Head Load. Same as HDLD* except specifically for the Master or Slave drive.
MIP	12B3	Master Drive Index Pulse. Same as IP* except specifically applies to the Master or Slave drive.

Table 4-1. Signal Mnemonics (Continued).

SIGNAL	SOURCE	DEFINITION
MIP	12B3	Master Drive Index Pulse. Same as IP* except specifically applies to the Master or Slave drive.
R/W	6A1	Microprocessor Read/Write. Output from the microprocessor used to select direction of data transfer on MPU data bus.
MR*	6D7	Master Reset. Output from master reset circuit used to reset all logic.
MSEL* MSEL	9E4 9E4	Master Select. Output from unit select circuit which indicates Master drive has been selected.
MSRDTA*	3C1	Master Drive Serial Data. Same as SRDTA* except specifically applies to Master Drive.
MSTEP	9D4	Master Drive Step. Same as Step except specifically applies to Master Drive.
MTG43	7D4	Master Drive Track Greater Than 43. Same as TG43 except specifically applies to Master Drive.
MTR00*	12E6	Master Drive Track 00. Same as TR00 except specifically applies to Master Drive.
MWG	9D4	Master Drive Write Gate. Same as WG except specifically applies to Master Drive.
MWPRT	12D6	Master Drive Write Protect. Same as WPRT except specifically applies to Master Drive.
PCE	9D7	Precompensation Enable. Signal used in the precompensation circuit to enable the multiplexer which selects early, on time or late data.
PHO	5A3	Motor Phase Zero. Output from the motor control circuit which indicates the motor is at the zero configuration.
POR* POR	6D1	Power On Reset. Signal used to reset various logic circuitry when power is turned on. POR indicates power is up to operating level.
RCLK	10B2	Read Clock. Read clock generated by phase lock loop clock generator.
RE*	9A4	FD1791 Read Enable. Input to the FD1791 which allows data, status or commands from the chip to the DAL0* - DAL7* lines.
R/W + R/W -	6A1	Read/Write Head Signal. Signal applied to the read/write head for writing or taken from the head during reading.
RWSTB	6C7	Read/Write Strobe. Output signal from the PIA used to strobe Read/Write logic during internal data transfer.
SRDTA*	9E5	Serial Data. Composite serial data from the selected drive which is applied to the FD1791.
SDRY	9C4	Slave Drive Ready. Output from slave drive indicating ready status.
STEP	8C4	Step. Output from the FD1791 which is applied to the selected drive during a stepping sequence.
TG43	8B5	Track Greater than 43. Output from the FD1791 that informs the selected drive that the Read/Write head is positioned between tracks 44-76 and is used to reduce the head current during write mode.
TPHD	9D7	Top Head. Signal from the microprocessor data bus which indicates head is indicated.
TR00*	9E5	Head On Track 00. Signal which indicates the head of the selected drive is at Track 00.
WC+ WC-	4C2	Write Current. Output from the write circuit which is applied to the Read/Write head.
WD	8B5	Write Data. Output from the FD1791 which contains both clock and data bits in the proper format. The data is then switched to either the master or a slave drive as required.
WE*	9A4	Write Enable. Input to the FD1791 which allows data, status or commands to be written onto the DAL0* - DAL7* lines.
WG	8B5	Write Gate. Output from the FD1791 which enables the write circuits on the selected drive.
WPRT*	9E5	Write Protect. Signal indicates the selected drive is write protected and terminates a write command in the FD1791.
WSEL	6C7	Write Mode Select. Output from the PIA which selects either the RE* or WE* signal.
8MHz 2MHz	6E3 6D1	8 and 2MHz Clock. Output from the clock circuit used to time the FD1791 and the microprocessor.

SECTION V

MAINTENANCE

5.1 GENERAL

The REMEX Diskette Drive has been designed to keep maintenance as simple and infrequent as possible. Table 5-1 lists the maintenance equipment required for the various procedures. Section 5.2 and Table 5-2 contain the recommended inspection and maintenance procedures. The remaining sections describe the required adjustment procedures. Replacement procedures are given in Section 6.

Table 5-1. Maintenance Equipment Required

Item	Quantity
Alignment Diskette, Dysan 360 for RFS24X0 as P/N 114584-001.	1
Alignment Diskette, Dysan 360/2A for RFS48X0 as P/N 114584-002.	1
*Dual Trace Oscilloscope, DC to 10 MHz	1
*Torque Driver	1
*Voltmeter, Digital 0-0.1 mA, 0-100 mVdc, 0-10M ohm, 0-100 Vdc, 100K impedance or greater.	1
Taptite Driver #4. Torx Part Number TX-09 (REMEX P/N 716056-125)	1
Taptite Driver #6. Torx Part Number TX-15 (REMEX P/N 716056-126) Taptite Driver #4 and #6 are also available from Apex Machine and Tool, Dayton, Ohio	1
Synthetic Oil, REMEX P/N 716004-232	1

*These Items not available from REMEX

5.2 MAINTENANCE PROCEDURES

Under normal circumstances preventive maintenance is not required for the drive. If severely dirty environments are encountered, an occasional cleaning of the drive may be performed to assure continued reliable performance. If a drive malfunctions, it is recommended that it be inspected and cleaned as described below.

Visual inspection is the first step in any maintenance operation. Always look for corrosion, dirt, wear, binds and loose connections. Noticing these items may save downtime later. Inspection and preventive maintenance operations are listed in Table 5-2. These should be performed at 12 month intervals or after 6000 power on hours. During normal maintenance, only those operations listed on the chart should be performed. Details on adjustments

and service checks are found in Section 5.3. Observe all safety precautions. Cleanliness cannot be overemphasized in the maintenance of the drive.

CAUTION

Do not lubricate the drive except as specifically directed. Oil will allow dust and dirt to accumulate.

5.2.1 READ/WRITE HEAD CLEANING

5.2.1.1 Read/Write Head Cleaning, RFS48X0 Only

On the RFS48X0, REMEX does not recommend touching or cleaning the Read/Write head. In addition, when maintaining the system the following caution should be observed.

CAUTION

It is important when performing maintenance on the RFS48X0 drive that the heads are not touched or disturbed. Certain maintenance procedures give instructions to place a piece of clean paper between the heads to make sure they don't come into contact with each other when working in that vicinity. Do not smoke or permit dirt or lint in this area or any other area of the drive.

5.2.1.2 Read/Write Head Cleaning, RFS24X0 Only

On the RFS24X0 only, the head should be cleaned only when signs of oxide build-up are present. The following procedure is recommended. Refer to Figure 7-1 for reference designations.

a. Retract the carriage to Track 00.

b. Remove all power and control signals by disconnecting P1/J1, P5/J5 and P8/J8.

c. Remove the Head Shield (57) by removing screw (J) and nut (KK).

d. Inspect the face of the head for reddish-brown oxide deposits. Clean head only if deposits are present.

CAUTION

Do not smoke while cleaning. Do not touch the face of the head with your fingers. Do not leave residue or lint on the head face. Trapped residual particles can result in the loss of a head and/or a scored diskette.

f. Check Head Pad Cartridge (MM) for trapped oxide particles. Replace pad if oxide or dirt is present or if excessively worn. See Section 5.4.3.

g. Perform the reverse of steps c and b.

Table 5-2. Inspection and Maintenance procedures.

Part	Inspection	Procedure
Actuator Band and Capstan	Inspect for cleanliness	Clean all oil and dust if necessary
Read/Write Head (RFD200X only)	Oxide Build-Up	Clean head ONLY IF NECESSARY. See Section 5.2.1.2.
Head Pad Cartridge (RFD2000 and RFD2001 only)	Excessive Wear	Replace if excessively worn or once each 6000 hours of operation. See Section 5.4.3.
Belt	Frayed or weakened areas.	Replace belt as described in Section 6.3.
Diskette Carrier	Diskette loads into drive without interference and door latches correctly.	Replace carrier assembly if required. See Section 6.9.
Base	Inspect for cleanliness.	Clean dust from base and check for loose screws and wires. Check all conditions.

5.2.2 TROUBLESHOOTING

Troubleshooting is presented in the form of a chart, Table 5-3, which should be consulted whenever diskette drive performance is unsatisfactory. The chart is divided into three columns: Indication, the way in which the malfunction becomes evident; Probable Cause, the possible reason or reasons for the malfunction; and Remedy, the manner in which the malfunction may be corrected.

The equipment described in this manual contains hazardous voltages capable of inflicting personal injury. These voltages appear at the AC connector, J8, and at the motor capacitor (59). The cautionary and warning notes are included in this manual to alert operator and maintenance personnel to these possible hazards.

5.3 ELECTRICAL ADJUSTMENTS

It is recommended, in most cases, that the unit be returned to the factory or an authorized REMEX service center for repair and adjustment of the carriage (read/write head) or the split band/stepper motor assemblies. If customer maintenance is to be performed, the following procedures are to be followed. These procedures give an outline which describe the steps to take and the desired results. In some cases, the method of performing a particular step or function is not explicit because of the many possible host equipment variations. It is also possible that some host systems and companion software may not be compatible and that a test fixture or special test set-up will be required.

Power should be applied with spindle motor rotating before diskette is inserted for all the following checks and adjustments.

Table 5-3. Troubleshooting Chart.

Indication	Probable Cause	Remedy
1. No output data, any track	1. No data written on a write protected diskette.	1. Check to make sure diskette was not write protected when writing occurred.
	2. Drive not addressed properly.	1. Check Unit/Sector Select Code to make sure proper unit select code is used in Data format. See Figure 3-2. 2. Check jumper wire to make sure unit select jumper is set for desired unit number.
	3. Wrong Commands issued.	1. Check Section 3.4 for modes of operations and signals issued.
	4. Read circuitry malfunctions.	1. Replace drive card.
	5. RE* signal not being generated.	1. Check Z38-3 and associated logic for true RE* signal.
	6. HDLD* signal not being generated.	1. Check Z53-39 for presence of HDLD* during a read operation.
2. Output present on all but a couple of tracks.	1. Defective diskette.	1. If more than two tracks are defective, replace diskette.
3. No data being written; data present from host equipment.	1. Write protect diskette being used.	1. Check to make sure diskette is not write protected.
	2. Wrong Commands issued. Drive not addressed properly.	1. Check Section 3.4 for modes of operation and signal issued. See Figure 3-2 for Data Bus Formats.
	3. Drive Not Ready.	1. Check Z56-7 to make sure DRDY signal is true. If not true check to make sure a diskette is inserted properly and index holes have been recognized.
	4. Fault condition present.	1. Check Status Code for fault condition and correct.
	5. Media not in or rotating properly.	1. Belt broken. Replace belt if required. See Section 6.4. 2. Check to see that media is in and rotating and that index pulses are present. 3. Index alignment incorrect. See Section 5.3.3.

Table 5-3. Troubleshooting Chart (Continued)

Indication	Probable Cause	Remedy
3. No data being written; data present from host equipment, (Cont.)	6. Head Solenoid or circuitry faulty.	1. Check head solenoid and associated circuitry for proper operation.
	7. WE* signal not being generated.	1. Check Z38-6 for presence of WE* signal during write operation.
4. Incorrect data being read.	1. Read/Write head dirty.	1. Clean head as described in Section 5.2.1 (RFS24X0 Only).
	2. Track alignment not correct.	1. Perform Section 5.3.1 and readjust as required.
	3. Data being read from wrong track.	1. Check to see that host equipment is processing track location properly. 2. Check step circuitry. See Indication 6.
	4. Track 00 alignment not correct.	1. Check to see that Z50-10 (MTR00*) is 0V when head is at track 00. Perform Section 5.3.2 if required.
	5. Circuit Malfunction.	1. Check data circuitry on drive card for proper operation.
	6. Head Pad worn (RFS24X0 Only).	1. Check for excessive wear of head pad cartridge and replace as required. See Section 5.4.3.
5. No Index or Sector Pulses.	1. Index sensor dirty.	1. Check index sensor and clean if required.
	2. Index sensor faulty.	1. Check for index sensor output at TP13 for side 0 or TP12 for side 1 and replace sensor if required.
	3. Index circuitry faulty.	1. Check index circuitry for proper operation and replace card if faulty.

Table 5-3. Troubleshooting Chart (Continued)

Indication	Probable Cause	Remedy
6. Head does not step.	1. Step* command not present.	1. Check Z54-15 for proper signal from the FD1791.
	2. Wrong Commands issued.	1. Check Section 3.4 for modes of operation and signals issued.
	3. Drive not ready.	1. Check drive for rotating media and proper unit select jumpers.
	4. Step circuitry faulty.	1. Check step circuitry for proper operation and replace card if required.
	5. Step motor faulty.	1. Check step motor for proper operation and replace if faulty.
7. Head steps in wrong direction.	1. Direction Select line not set properly.	1. Check Direction Select input at Z54-16 for proper output signal.
	2. Direction control logic faulty.	1. Check direction control logic on card and replace card if required.

h. The remaining procedures must be followed if the brake tension screw was adjusted or if the alignment is to be checked. These procedures must be performed if stepper motor , band assembly or carriage assembly has been moved or replaced.

i. Insert the alignment diskette into the drive. Allow 2 minutes for the diskette to warm up (drive selected and power applied).

CAUTION

Do not allow the drive to write with the alignment diskette inserted. This will destroy the alignment signals on the diskette.

j. Select side 0.

k. Step the drive to track 00 and then seek at a 3 msec rate to track 38. On the RFS4800 this can be done using the 11_{16} command.

l. Using a dual trace oscilloscope connect channel 1 to TP 13 (Master) or TP 1 (Slave) (Index 0) and channel 2 to TP 2 (Master) or TP 5 (Slave) (RD AMP*). Trigger the scope on TP 13 (Master) or TP 1 (Slave) for head 0 and TP 12 (Master) or TP 2 (Slave) for head 1 (Index Pulse). Set the time base for 20 msec/division and set the zero reference at the bottom of the screen so only the top half of the two cat-eye patterns are present. See Figure 5-1B. At this point the amplitude of the two signals may not be the same.

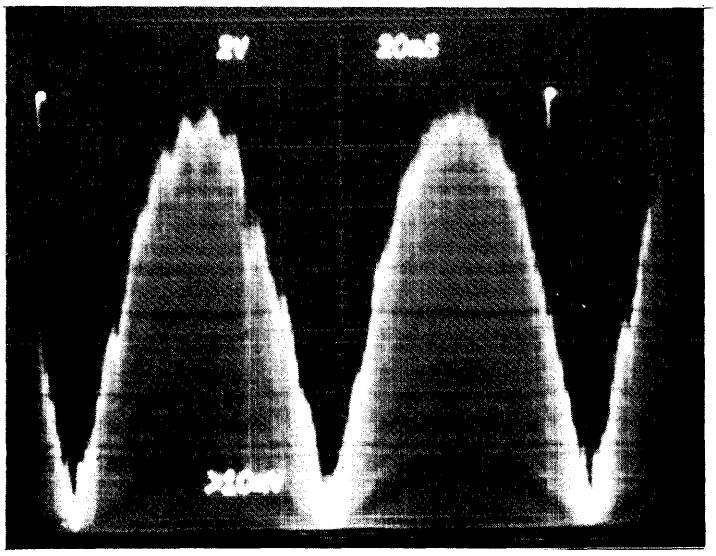


Figure 5-1B. Alignment of Track 38 Showing Equal Cat-Eye Halves.

m. Return the carriage to track 00 and then back to track 38. Record the percentage difference between the heights of the two cat-eyes. Cat-eye A is defined as the one on the left and cat-eye B is on the right as marked in Figure 5-1B. If A > B the difference is positive; if A B, the difference is negative. The percentage is figured as follows: if A is larger than (A-B)/A; if B is larger than (A-B)/B. See Figure 5-1C which illustrates a + 25% difference.

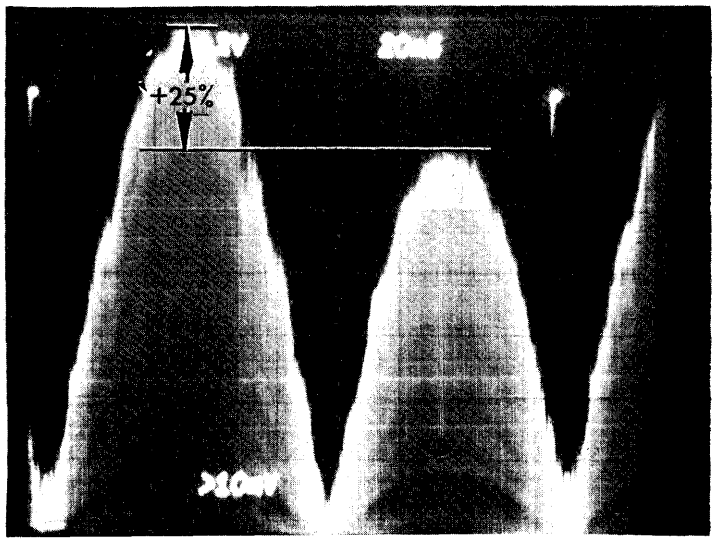


Figure 5-1C. Seek Measurement Showing a + 25% Difference.

n. Step to track 39 and then back to 38. Record the % difference at track 38.

o. Step to track 37 and then back to 38. Record the % difference at track 38.

p. Step to track 76 and then back to 38. Record the % difference at track 38.

q. Check the step (l, m, n or o) with the most positive reading.

r. Switch between head 0 and head 1 and observe the cat-eyes.

s. Select the more positive head (head 0 or head 1). The two cat-eyes of this head must be within ± 30%. If this is not the case, perform steps t through z.

t. Remove the alignment diskette to allow access to screws BB (Figure 7-1). Remove the Head Shield (Item 57, Figure 7-1) and loosen two screws BB just enough to be able to slide the motor assembly. Partially tighten screw BB nearest the door. Use a torque driver with tork #15 tip.

5.3.1 RADIAL TRACK ALIGNMENT

The following procedure is used when performing the radial track alignment:

a. Stabilize the alignment diskette to constant ambient conditions for a period of 24 hours. For the RFS24X0 use REMEX P/N 716083-002 and for either the RFS48X0 or RFS24X0 use REMEX part number 716083-006.

b. Stabilize the drive for 2 hours, minimum, warm up (i.e., power applied and drive selected).

c. Insert a test diskette (not the alignment diskette). Select the drive and allow diskette to turn for two minutes. Write an all "00" pattern on all tracks of side 0.

d. Using a dual trace oscilloscope, connect channel 1 to Z58-3 (Master) or Z24-2 (Slave) (Step Signal) and channel 2 to TP2 (Master) or TP5 (Slave) (RD AMP*). Set the time base for 5 msec/division. Set the trigger for positive trigger on channel 1.

e. Using single step pulses at least 30 milliseconds apart, read all tracks while observing the scope. The amplitude of channel 2 must be > 90% stable within 18 msec of the leading edge of the step pulse on channel 1. See Figure 5-1A.

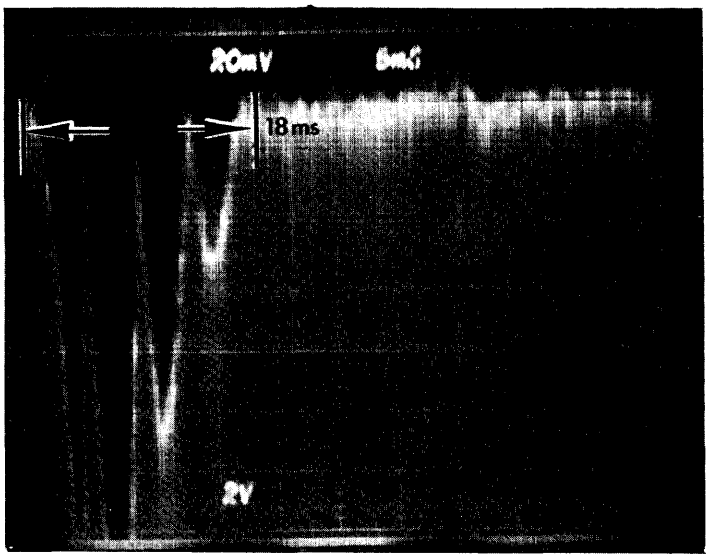


Figure 5-1A. Step settle measurement.

f. If the conditions of step e are not present, adjust the brake tension screw (Item VV, Figure 7-1) to bring it within the 18 msec maximum.

g. On the RFS48X0, repeat steps c, d, e and f for side 1.

u. Insert the alignment diskette back into the drive.

v. Repeat steps m, n, o, p and q. Switch between side 0 and side 1 and select the more positive head.

w. Slide the stepper motor assembly in the appropriate direction until the two cat-eyes are within ± 4% of the same height.

x. Remove the alignment diskette and tighten screws BB.

y. Insert the alignment diskette and repeat steps m, n, o, p and q. Check that the more positive head is between ± 30%. Some error will occur due to the diskette removal. This should be of no concern.

z. Verify step settle time is correct by repeating steps d through f.

5.3.2 TRACK 00 SWITCH AND MECHANICAL STOP ADJUSTMENT

The following procedure describes the alignment of Track 00 switch and must be performed any time the stepper motor assembly, carriage assembly (read/write head) or track 00 sensor is replaced. Refer to Figure 7-1 for letter and number reference designations.

a. Check Track Alignment procedure 5.3.1 and perform alignment if required.

b. Insert a Dysan 360/2A into the RFS48X0 or a Dysan 360 into the RFS24X0.

c. Step to Track 06. At Track 06, J6-4 should be low and J6-5 should be high. If not, repeat step a.

d. Monitor Track 00 Optical Switch signal at Z44-8.

e. Step to Track 02, 01 and 00. The Track 00 Optical Switch signal should be high at track 02 and low at 01 and 00. If this is not the case, loosen the screw (R) which holds the Track 00 Bracket (36) and move the bracket until these conditions exist. Do not loosen screw (S) which holds the Optical Switch (56) to the Bracket (36).

CAUTION

The Track 00 Bracket should be parallel to the guide rail. Interference with the head load bail when energized or the carrier when the door is closed must be avoided.

f. Step to Track 76 and back to Track 00. The Damper (53) should be set so that the operator does not hear the Pulley on the Carriage hit the stops on the Damper at either Track 76 or Track 00.

g. If this is not the case loosen screw AA and rotate the damper slightly so that the conditions in step f are met. Tighten screw (AA) only enough to keep the damper from moving. Excessive torque could cause the Track Alignment to go out of adjustment.

5.3.3 INDEX ALIGNMENT

The following procedure describes the alignment of the index sensor assembly and must be performed any time the index sensor is replaced. Refer to Figure 7-1 for number and letter reference designations.

a. Insert a Dysan 360/2A alignment diskette into the drive.

b. Select side 0.

c. Position the carriage to Track 1 and perform a read operation.

d. Trigger an oscilloscope on the negative going edge of the Index* pulse at TP13. Observe TP2 or TP3 on the scope.

e. The time period between the leading edge of the Index* pulse and the occurrence of the first data pulse shall be 200 ± 100 microseconds. See Figure 5-2. When checking the index alignment, the time period stated can be 200 ± 100 µsec. When performing the alignment, the adjustment is made for 200 ± 50 µsec.

f. If the conditions of step e are not present, slightly loosen the screw (Item U, Figure 7-1) which holds the single-sided Sensor (47) and move the Sensor slightly until the conditions of step e are present.

g. Tighten the screw.

h. Step the carriage to Track 76 and repeat steps d, e, and f as required.

i. Reinsert the diskette several times and ensure that the adjustment made in step f is 200 ± 50 microseconds.

j. This and subsequent steps apply to TP12, the two-sided Sensor (48), and screw (T). Select Side 0 and perform a read operation.

k. With oscilloscope triggered on negative going edge of TP12 the data pulse on TP2 should occur at 200µsec ± 100 µsec. (See Figure 5-2).

l. Repeat step k after selecting Side 1.

m. If both k and l do not result in data pulses at 200µsec ± 100 µsec. it is necessary to adjust two sided Index Sensor (48).

n. Loosen screw (T) and move Sensor (48) until data pulses for both Side 0 and Side 1 occur at 200µsec ± 50 µsec. Tighten the screw.

NOTE

The checking (step k and l) and adjusting (step n) tolerances are different to allow for alignment diskette and temperature variations.

o. Remove the alignment diskette.

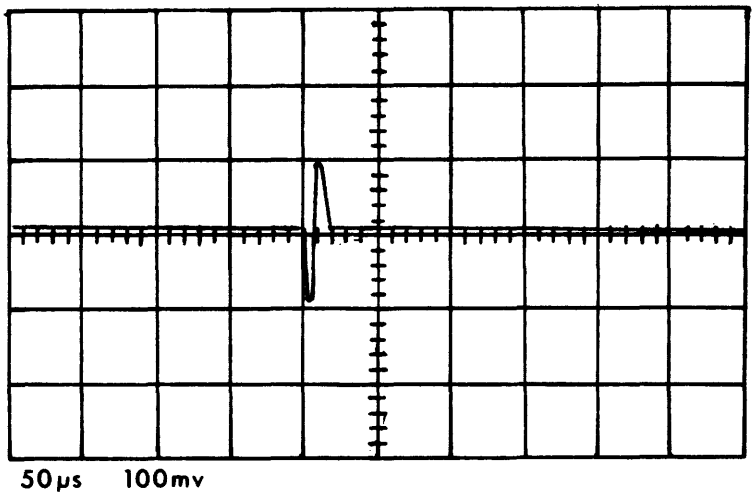


Figure 5-2. Waveforms - Index/Sector Adjustment.

5.3.4 WRITE PROTECT ADJUSTMENT

The following procedure describes the adjustment of the optical write protect switch and must be performed any time the write protect switch is replaced. Refer to Figure 7-1 for number and reference disignations.

a. Insert a write protected (slotted) diskette into the drive.

b. Using an oscilloscope, observe Z44-2 and insure that the signal reaches a peak of 3V minimum.

c. Insert a non-write protected (non-slotted or slot covered with opaque tape) diskette into the drive.

d. Z44-2 should be less than 0.7V.

e. If the conditions of step b and d do not exist loosen the screw (EE) which holds the Write Protect Switch Assy. (28) and adjust the switch in the slot provided until conditions are met.

CAUTION

Make sure the write protect switch does not prevent easy insertion of the diskette into the drive. If it does the write protect switch is too close to the front of the drive.

f. As a check try to perform a write operation with a Write Protected Diskette in the drive. Observe Z44-5 on the circuit card. In order to inhibit writing, this point must be at 3.2V.

5.3.5 R1 CROSSOVER DETECTOR INPUT DC BALANCE ADJUSTMENT

The following steps must be taken to eliminate switching noise into this system:

a. Connect the two leads of a digital voltmeter to TP4 and TP5. The DVM leads should be as short as possible and of equal length.

b. Disconnect P3/J3 and P4/J4 and ground pin 1 and 3 on both J3 and J4.

c. Measure the DC voltage between TP4 and TP5. It should be OV ± 6mV. If not, adjust R1 so that the voltage is 0 ± 3mV.

d. Remove the voltmeter leads.

5.3.6 READ CLOCK GENERATOR ADJUSTMENTS (RFS4810 and RFS2410 ONLY)

The following procedure adjusts R40 and R60 in the Clock Generator Circuits.

a. Inhibit SRDTA* pulses at Z17-6 and 9 by removing the unit select jumpers (unit address ≠0) and the jumpers across F-G and J-H. Disconnect the slave cable at P2/J2.

b. Perform a Master Reset or a Power On Reset.

c. Place a voltmeter between TP7 and TP1 (OV).

d. Adjust R60 as follows:

	If	Then
1.	C28 = 22pf and Z18 = 74LS324	Adjust R60 to 1.5 volts
2.	C28 = 15pf and Z18 = 74LS324	Adjust R60 to 1.0 volts
3.	C28 = 200pf and Z18 = 74LS624	Adjust R60 to 3.2 volts

e. Place an oscilloscope between Z17-1 (RCLK) and TP1.

f. Adjust R40 for a 1.04 μsec RCLK half-cycle in double density mode. If RCLK frequency is too low (greater than 1.04 μsec half-cycle), step d3 may be adjusted up to 3.4V as required.

g. Remove the oscilloscope and voltmeter and replace the jumpers on P2/J2.

5.3.7 WRITE PRECOMPENSATION ADJUSTMENT (RFS4810 and RFS2410 ONLY)

The following adjustment is required for R63 in the precompensation circuit.

a. This circuit is adjusted with WD data pulses present. Place the drive in a mode of operation which will allow data to be written.

b. Place one probe of a dual sweep oscilloscope at TP10 and the other probe at TP9. Place the ground probe at TP1.

c. Adjust R63 for a 160 to 170 ns time period between the positive going edges of TP9 & TP10.

5.4 MECHANICAL ADJUSTMENTS

Proper operation depends upon maintaining accurate adjustments. No adjustments are required when a new unit is first installed. However, when operational performance is unsatisfactory or when parts are replaced, it may be necessary to perform certain mechanical adjustments.

5.4.1 LATCH PLATE/CARRIER ADJUSTMENT

The following procedure adjusts the clearance between the diskette guide rails and bottom of the carrier. This adjustment should be made whenever the Carrier Assembly or the Latch Plate Assembly is removed or replaced. See Figure 7-1 for number and letter disignations.

a. Remove all power and control signals by disconnecting P1/J1, P5/J5 and P8/J8.

b. Open the front door and remove any diskette which may be present.

c. Lay a 0.125 $\pm$ 0.005 metal shim on the diskette guide rails. This shim should be long enough to span the two guide rails (approximately 8 inches).

d. Close the door and check to see that the carrier is in contact with the metal shim when the door is fully closed. There should also be an end play of between .010 - .030 on Clutch shaft (21).

e. If the door does not close properly or if there is a gap between the carrier and shim, loosen the three screws (Item D, Figure 7-1) which hold the Latch Plate (Item 41, Figure 7-1) and adjust the Latch Plate until the conditions of step d are met. Tighten screws (D).

f. Open the front door and remove the shim.

g. Perform the reverse of step a.

5.4.2 DISKETTE LOAD ARM ADJUSTMENT

The following adjustment sets the distance between the Diskette Load Arm (16) and the Head Load Arm on the carriage assembly. See Figure 7-1 for number and letter reference designations.

a. Insert diskette and close door. Apply power to the unit and place the unit in a mode of operation (See Sect.3.4.13) so that the Head Load Solenoid is energized.

b. Remove the Head Shield (57).

c. Move carriage so head is in track 00 position (closest to rear of drive).

NOTE

It is important that during this procedure that caution be taken to protect the read/write heads and that no objects or dirt come in contact with the heads.

d. Measure the air gap between the lip of the Diskette Load Arm and the arm on the carriage assembly. This should be .018 to .023. See Figure 5-3.

e. If this is not the case, loosen the two screws (L) which hold the Diskette Load Arm (16) to the Diskette Load Bracket (17) and move the Load Arm until the conditions of step d are satisfied.

f. Repeat steps c, d & e with head at track 76 position (closest to the front of drive).

g. Deenergize the solenoid and measure the rise in the Diskette Load Arm which should be between 0.020 and 0.030 inch.

h. If this is not the case adjust screw (GG) until the conditions of step e are met.

i. Replace the Head Shield (57).

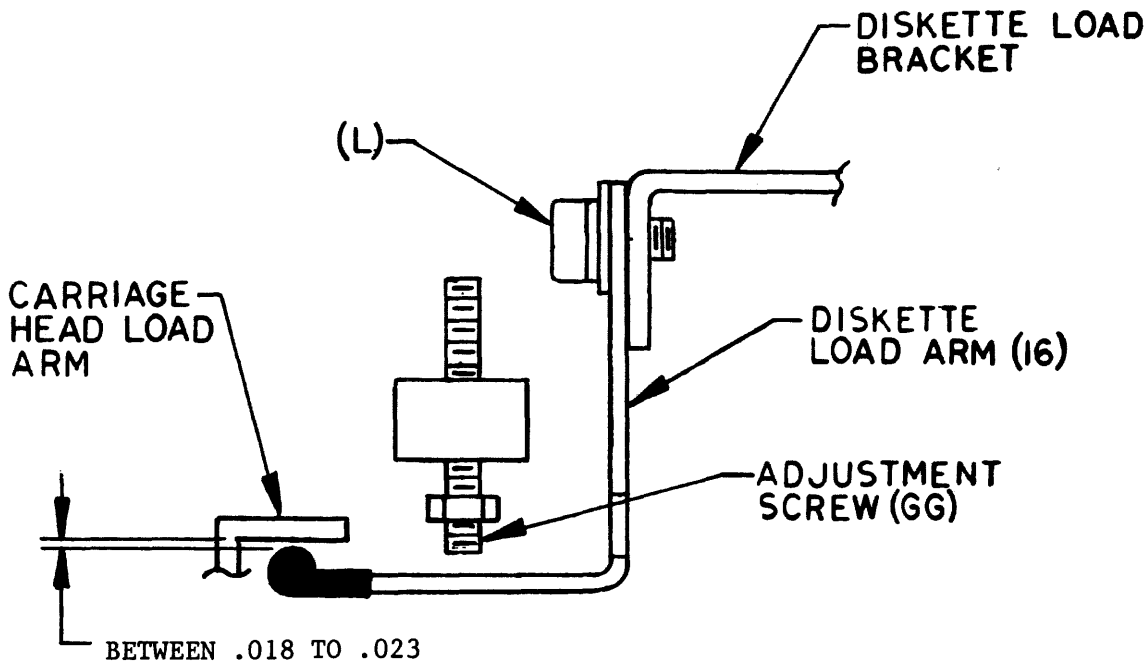
5.4.3 HEAD PAD CARTRIDGE ASSEMBLY REPLACEMENT (RFS24X0 ONLY)

The head pad cartridge assembly (REMEX P/N 112800-001) should be replaced if excessive wear occurs or once every 6000 hours of operation, which ever comes first. The following procedure is recommended. Refer to Figure 7-1 for callout designations.

a. Remove all power and control signals by disconnecting P1/J1, P5/J5 and P8/J8.

b. Loosen the Head Pad Cartridge (MM). It is not necessary to remove the screw entirely, only enough to align the flat side of the cartridge with the flat of the hole. Remove the cartridge.

c. Replacement is the reverse of steps b and a.



MMC 685

Figure 5-3. Diskette Load Arm Adjustment. All Number and Letter Designations Refer to Item Called Out in Figure 7-1.

5.4.4. END-STOP ADJUSTMENT (RFS24X0 ONLY)

The following procedure is recommended for adjusting the end-stops on the RFS24X0 only.

a. Step the carriage to track 00.

b. Insert a 0.012" gauge between the end stop on the carriage and guide rod and the inner carriage frame.

c. Slide the end stop gently against the gauge and secure the stop in this position.

d. Verify a 0.010" minimum clearance between the end stop and the carriage.

e. Repeat steps a, b and c for track 76. Verify that a minimum clearance of 0.010" exists between the carriage and end stop.

f. Repeat steps a, b and c until a 0.010" minimum clearance is reached for both tracks 00 and 76.

SECTION VI

PARTS REPLACEMENT

6.1 GENERAL

REMEX maintains service facilities at its manufacturing location and at sevice centers in major population areas for repair or replacement or components for their products. It is recommended that one of these centers be contacted for assistance in case of equipment malfunction. For the locations of service facilities in any area, contact REMEX at the address listed on the title page of the manual. Please direct inquiries to the attention of the Service Department.

When any parts require replacement or disassembly, the procedures below should be followed closely. In many cases, it is recommended that parts be replaced at a subassembly level rather that as a detail part. Because of the special tools and alignment equipment needed and the time and labor involved it is generally more economical to repair at this level with a prealigned and assembled part rather than at the more detailed level. The warnings and cautions are included to protect personnel and equipment. Notes are included to assist pesons unfamiliar with the equipment. Before attempting any procedure, all instructions for that disassembly should be read and understood.

Replaceable items recommended as spare parts are listed in Table 7-1. All system components are identified in Section VII of this manual along with illustrations showing part locations.

WARNING

Potentially dangerous line voltage is applied to components within this equipment. If adjustments must be performed with power applied, these point must be located and avoided. High voltage can be accidentally contacted at connector J8. Always remove power before disconnecting internal plugs and removing the card.

Figure 7-1 should be folded out from Section VII during these procedures and should prove very helpful in replacing various assemblies. Figures 7-2 through 7-4 also show the location of various parts and assemblies. Circled numbers in Figure 7-1 identify parts listed in Table 7-2 and circled letters refer to various hardware items referred to in the following procedures.

6.2 PRINTED CIRCUIT CARD REPLACEMENT

The following procedure is recommended when replacing the printed circuit card assembly. Refer to Figure 7-1 for letter and number designations.

a. Remove all mating connectors from P.C. Card.

b. Remove all taptite screws which hold the Printed Circuit Card (PCI) to the Mainframe casting.

c. Installlation is the reverse of steps b and a . Replacement cards are prealigned and no adjustments on the circuit card should be required.

6.3 MOTOR DRIVE BELT REPLACEMENT

The following procedure is recommended when replacing the drive belt.

a. Follow prodedure of 6.2 to remove printed circuit board.

b. Slide the belt (Item 1, Figure 7-1) off the Drive and Motor pulleys.

c. Replacement is the reverse of steps b and then a. Before reapplying A.C. power, manually rotate the pulleys to make sure the belt is properly installed on the pulleys.

6.4 DRIVE MOTOR ASSEMBLY REPLACEMENT

When replacing the 114166-001 or 114167-001 drive motor assembly it is recommended that the entire assembly including the connector and grounding strap be replaced. Refer to Figure 7-1 for letter and number designations.

a. Follow procedure of 6.2 to remove Printed Circuit Board.

b. Slide the belt off the Drive and Motor pulleys.

c. Remove the three 8-32 taptite screws (UU) and washers which hold the 114166-001 and 114167-001 Drive Motor Assembly (7) to the mainframe.

d. Remove the 6-32 taptite screw which holds the grounding lug to the Mainframe. Note the installation of the grounding lug so that it is replaced correctly.

e. Remove the connector from the bracket.

f. On assemblies 114166-001 and 114167-001 it is also necessary to remove the two 6-32 Taptite screws (Z) which hold the Capacitor Bracket (2) to the Mainframe and remove the Capatitor (59). The Capacitor is part of the Drive Motor Assembly and should be changed with the Motor.

g. Install the new Motor Assembly to performing the reverse of steps f, e, d, c, b and then a.

6.5 HUB PULLEY REPLACEMENT

The following procedure is recommended when replacing the Hub Pulley. Refer to Figure 7-1 for letter and number designations

a. Remove the Drive Belt. See Section 6.3.

b. Loosen the two set screws (V) which hold the Hub Pulley (46) to the Hub Assembly (38) and remove the Hub Pulley.

c. Install the new Hub Pulley by performing the reverse of steps b and then a.
Caution: Pulley should clear rib of Mainframe by approximately .060.

6.6 INDEX L.E.D. ASSEMBLY REPLACEMENT

The following procedure is recommended when replacing the Index L.E.D. Housing assembly. Refer to Figure 7-1 for letter and number designations.

a. Remove the printed circuit card as in Section 6.2.

b. Unsolder the red and orange wires on the index L.E.D. housing (20).

c. Loosen the 6-32 screw (PP) which holds the Index L.E.D. Housing (20) to the Carrier Assembly and remove the Index L.E.D. Housing.

d. Install the new Index L.E.D. Housing Assembly by performing the reverse of steps c, b and then a.

e. Perform Section 5.3.3.

6.7 TRACK 00 OPTICAL SWITCH REPLACEMENT

The following procedure is recommended when replacing the Track 00 Optical Switch (56). Refer to Figure 7-1 for letter and number designations.

a. Remove the printed circuit card as in Section 6.2.

b. Slide off the red, brown, orange and black wires from the Optical Switch (56). Note the terminal locations for each wire so they can be replaced correctly.

c. Remove the two 4-40 taptite screws (S) which hold the Track 00 Optical Switch to the Track 00 Bracket (36).

d. Replacement os the reverse of steps c, b and then a.

e. Perform Section 5.3.2.

6.8 EXPANDING CLUTCH ASSEMBLY REMOVAL

The expanding clutch (15) can be removed either when the carrier assembly is removed or by the following procedure. See Figure 7-1 for number and letter reference designations.

a. Remove all power and control signals from the drive by disconnecting P1/J1, P5/J5 and P8/J8.

b. Remove two screws (F) which hold the carrier assembly to the Latch Plate (32). This will allow the carrier to raise enough to permit the expanding clutch to drop down.

c. Remove the Retaining Ring (23) and drop the Spring (26), Shim (24), Pin (21) and Expanding Clutch (15) down from the bottom.

d. Reassembly is the reverse of steps c, b and then a. When reassembling the items in step c, make sure there is an end play in the clutch shaft of between .010 and .030 inch.

6.9 CARRIER ASSEMBLY REPLACEMENT

Many items on the carrier including the Diskette Brackets (9,10), Carrier Eject Assembly (11,12,13), portions of the Head Load Solenoid Assembly (16,17,18), Index Housing L.E.D. Assembly (20) and Write Protect Switch Assembly (28 and 29) can be changed without removing the Carrier Assembly. See Figure 7-1 for callouts. However, to gain access to certain items on the Mainframe, the carrier must be removed. The following procedure is recommended when removing the Carrier Assembly:

a. Remove all power and control signals by disconnecting P1/J1, P5/J5 and P8/J8. Remove the Head Shield (57).

b. Unsolder the blue and violet wires which attach to the Head Load Solenoid (18).

c. Slide the four wires off the Write Protect Optical Switch (29). Identify the wires for correct replacement.

d. Remove the Index L.E.D. Housing Assembly (20). See Section 6.6.

e. Protect the read/write heads by inserting a non-abrasive sheet of paper between the heads.

f. Remove the two screws (K) which hold the Disk Load Bracket (17) to the Solenoid (18). The Diskette Load Arm (16) will be attached. Do not disturb the two screws (L) which hold the Diskette Load Arm (16) to the Disk Load Bracket (17).

g. Remove two screws (F) which hold the Carrier to the Latch Plate (32) at the front of the Drive.

h. Remove four screws (FF) which hold the Carrier Spring to the Mainframe (37). These screws are accessable through the two Cover Supports (58).

i. The Carrier Assembly is now free.

j. To replace the Expanding Clutch Assembly (15) remove the Retaining Ring (23) and drop the Spring (26), Shim (24), Pin (21), and Expanding Clutch (15) down from the bottom.

k. Reassembly is the reverse of steps j, i, h, g, f, e, d, c, b and then a. When reassembling the items in step J make sure there is an end play in the clutch shaft of between .010 and .030 inch.

l. Perform Sections 5.3.4, 5.4.1 and 5.4.2.

6.10 SINGLE SIDED AND TWO SIDED INDEX SENSOR ASSEMBLIES REPLACEMENT

The Single Sided Index Sensor Assembly (47) and the Two Sided Index Sensor Assembly (48) are used in conjunction with the Index L.E.D. Housing Assembly (20). Refer to Figure 7-1 for letter and number designations. The following procedure is recommended when replacing the Single Sided or the Two Sided Sensor Assembly:

a. Retract the head to track 00 to insure sufficient room to perform this procedure.

b. Remove all power and control signals to the drive by disconnecting P1/J1, P5/J5 and P8/J8.

c. Loosen the single 6-32 Taptite screw (T or U) which holds either sensor to the Mainframe (37). On some units it may be necessary to remove the P.C. card to gain access to these screws.

d. Remove the two screws (F) which hold the Carrier to the Latch Plate (32) at the front of the drive. This will provide room to move the Single or Two Sided Sensor to the left and give space for unsoldering.

e. Unsolder the black and white wires attached to the Single Sided Sensor (47) or unsolder the gray and violet wires attached to the Two Sided Sensor Assembly (48). Note the wire locations so they can be replaced on the same terminals.

f. Replacement is the reverse of steps d, c and then b.

g. Perform Section 5.3.3.

6.11 DRIVE HUB REPLACEMENT

The following procedure is required when replacing Drive Hub (38). Refer to Figure 7-1 for number and letter designations. When ordering a new Drive Hub, it is recommended that the Upper Bearing (34) and the Lower Bearing (33) be replaced at the same time.

a. Follow procedure 6.3 to remove Drive Belt(1).

b. Follow procedure 6.8 to remove the Carrier Assembly, steps a through i.

c. Remove the two set screws (V) which hold the Pulley Hub (46) to the Drive Hub (38) shaft. Use care not to lose the parts since these items are spring loaded (49). Note the order of assembly (from top to bottom, items 38 , QQ, 34, 33, RR, 49 and 46) so that they are replaced in the same manner. Replace also the Upper Bearing (34) and the Lower Bearing(33).

d. Replacement is the reverse of steps c, b and then a.

6.12 HEAD LOAD SOLENOID REPLACEMENT

The following procedure is recommended when replacing the Head Load Solenoid. Refer to Figure 7-1 for letter and number designations.

a. Remove the Carrier Assembly. Refer to Procedure 6.9.

b. Remove the two 4-40 screws (K) which hold the Solenoid (18) to the Disk Load Bracket (17). Do not disturb the two screws (L) which hold the Diskette Load Arm (16) to the Disk Load Bracket (17).

c. Remove the brass 6-32 x 3/8 screw (Q) which holds the solenoid (18) to the Carrier. Make sure the brass screw (P/N 709221-306) is used during replacement.

d. If the spring on the new solenoid is different than the old spring, replace the solenoid spring with the old spring (P/N 114384-001). Later model units have the spring included as part of the solenoid.

e. Replacement is the reverse of steps d, c, b and then a.

f. Check Adjustment Prodedure 5.4.2.

6.13 CARRIAGE ASSEMBLY REPLACEMENT (RFS4800 ONLY)

When replacing the Carriage Assembly, order P/N 114745-002. Included with the Carriage Assembly are instructions for replacement.

6.14 CARRIAGE ASSEMBLY REPLACEMENT (RFS2400 ONLY)

The following describes the replacement of the carriage assembly (item 6, Figure 7-1).

See Figures 6-1 and 7-1 for part and hardware callouts. Figure 6-1 applies to the RFS2400 carriage assembly.

CAUTION

Great care must be taken when replacing the carriage assembly. The band is very delicate and must not be crimped or dented in any way. This procedure should only be made if the user has the facilities to realign the drive as given in Sections 5.3.1, 5.3.2 and 5.3.3. The entire procedure should be read and understood first before attempting the actual disassembly.

a. Remove the P.C. Card by performing Section 6.2.

b. Remove the plastic head shield (item 57, Figure 7-1) by removing screw J (Figure 7-1) its nut and washer and nut KK (Figure 7-1) and the cable clamp (item 3, Figure 7-1).

c. Cut two ties holding the head cables to the chassis (both sides).

d. Remove the band clamp (item 5, Figure 6-1) from the pulley.

CAUTION

Do not attempt to remove the band pulley.

e. Unhook the band spring from the roll pin (Item 10, Figure 6-1). This allows the band assembly to be loose around the pulley.

CAUTION

Use care so as not to bend or dent the band assembly. It will be reinstalled on the new carriage assembly.

f. Loosen the two guide rod clamps (item 4, Figure 7-1) by loosening the two screws (item SS, Figure 7-1). This allows removal of the guide rods (item 51, Figure 7-1) from the carriage assembly.

g. Carefully slide the guide rods out of the carriage assembly and out the rear of the drive.

CAUTION

Use care in handling the guide rods. Do not drop or damage them in any way.

h. Carefully lift the band up and off the pulley and remove the carriage assembly from the chassis.

i. On a bench, carefully remove the two screws, nut plate and band clamp (Items 15, 17, 4, Figure 6-1).

j. The new carriage assembly is 114240-002 and is identical to the one being replaced except for the absence of the band assembly, the two band clamps, and band pulley and the associated hardware. Also included with the carriage assembly is the 114497-001 damper spring (item 55, Figure 7-1) to be replaced on the stepper motor assembly. Install the band assembly with spring on the new carriage assembly by performing the reverse of step i.

CAUTION

Make sure band is parallel with the upper edge of the carriage assembly.

k. Replace damper spring (item 55, Figure 7-1) on the stepper motor assembly with new spring, part number 114497-001.

l. Insert the head cables through the hole in the chassis.

m. Make a loop in the band and line up the band clamp screw (item 16, Figure 6-1) with the hole in band assembly and install the band clamp (item 5 , Figure 6-1). Tighten the screw only lightly to allow pulley to self align under belt tension.

n. Install the band spring on the roll pin (Item 10, Figure 6-1).

o. Install the guide rods, rotate guide rod clamps and tighten. Make sure the end of the guide rods are flush with the hold down area on the chassis.

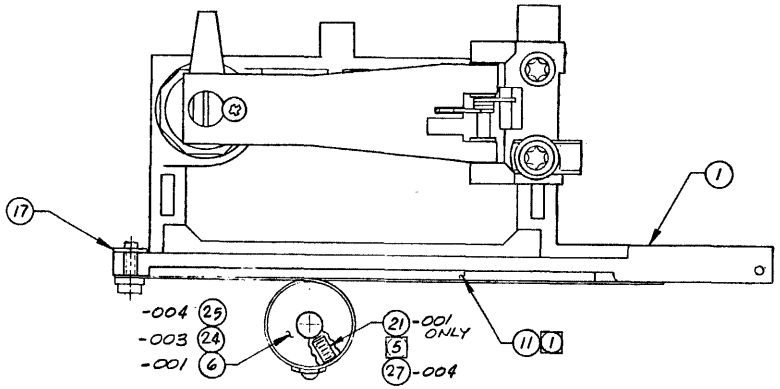
p. Move the carriage assembly back and forth on the guide rods to make sure the band moves without binding. If binding occurs, loosen the band clamp screw (Item 16, Figure 6-1) and if necessary, the two screws (Item 15, Figure 6-1) which hold the band assembly to the carriage. Move the carriage back and forth and align the band assembly until no binding occurs. Tighten all screws.

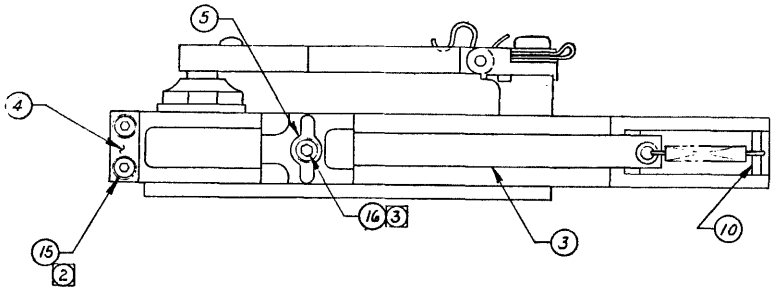
q. Tywrap the cables on the P.C. board side of the chassis.

r. Replace the P.C. board by performing the reverse of step a.

s. Tywrap the head cables on the top of the chassis, making sure that the cable does not interfer with the carriage assembly or the A.C. plug.

t. Realign the drive by performing Section 5.3.1, 5.3.2 and 5.3.3.





SYM	ECO	EFFECT.	REVISIONS	BY	DATE	APPR'D
A	—		RELEASED	S.E.O.	3.1.79	PM
B	18252	4.3.79	ITEM 1 WAS 114239-001	S.E.O.	4.3.79	HK
C	18363	5.15.79	SEE ECO	S.E.O.	5.15.79	HK
D	18469	6.28.79	SEE ECO	S.E.O.	6.28.79	HK
E	18568	7.25.79	SEE ECO	S.E.O.	7.28.79	HK
F	18790	11.13.79	ITEM 13 WAS 709930-403	PLM	11.13.79	HK
G	18815	11.30.79	CHANGED ITEM 11 FOAM PAD TO DAMPER	S.E.O.	11.30.79	HK
H	18818	12.21.79	ITEM 13 WAS 71000-110, ADDED NOTE 8	PLM	12.21.79	HK
J	19123	6.17.80	SEE ECO	S.E.O.	6.17.80	HK
K	19373	10.21.80	ADDED -003 REQUIREMENTS	O.P.	10.21.80	HK
L	19418	3.10.81	SEE ECO	S.E.O.	3.10.81	HK
M	19821	6.16.81	ADDED -004 REQUIREMENTS	O.P.	6.16.81	HK

REQD 004	REQD 003	REQD 002	REQD 001	PART NUMBER	DESCRIPTION	DESIGNATION	NOTE	ITEM
					LIST OF MATERIALS			
1	—	—	—	713000-138	SCREW-SET 6-32x3/16 (BRASS TIP)			28
								27
1	—	—	—	113300-004	PULLEY-BAND			26
—	1	—	—	113300-002	PULLEY-BAND			25
								24
								23
								22
—	—	—	1	713060-703	SET SCREW, 4-40×3/16 LG.		5	21
—	—	1	—	114497-001	SPRING-DAMPER			20
								19
								18
1	1	—	1	114416-001	NUT PLATE			17
1	1	—	1	709940-302	SCREW-BUTTON HD, 1-72×1/8 LG.		3	16
2	2	—	2	709930-405	SCREW-SOC CAP HD, 2-56×5/16 LG.		2	15
								14
								13
								12
1	1	1	1	114471-001	DAMPER-CARRIAGE		1	11
1	1	1	1	713710-006	ROLLPIN-.062 DIA. x .500 LG			10
—	—	1	—	114575-001	OPERATION SHEET: CARRIAGE REPLACEMENT INSTRUCTIONS			9
								8
								7
—	—	—	1	113900-001	PULLEY-BAND			6
1	1	—	1	113931-001	CLAMP-BAND (DRIVE)			5
1	1	—	1	113932-001	CLAMP-BAND (CARRIAGE)			4
1	1	—	1	114376-001	BAND ASSY			3
								2
1	1	1	1	114624-001	CARRIAGE SUB ASSY			1

NOTES: UNLESS OTHERWISE SPECIFIED.

1. INSTALL ITEM 11 IN RECESS PROVIDED ON CARRIAGE (BEHIND BAND AND ALIGNED WITH WIDTH OF BAND.
2. SNUG BUT DO NOT TIGHTEN ITEM 15, 2 PLCS.
3. SNUG BUT DO NOT TIGHTEN ITEM 16. ALLOW PULLEY TO SELF ALIGN UNDER BELT TENSION.
4. INSTALL SET SCREW BUT DO NOT GO PAST SHAFT HOLE. TO BE TIGHTENED ON NEXT ASSY.
5.
6.
7.
8.
9. -002 ASSY FOR SPARE PARTS SALES & SERVICE REQUIREMENTS ONLY.

USED ON	NEXT ASSY.
RFS2410	814230-*
RFS2420	814231-*
RFD2000	814257-*
RFD2000	814258-*

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES: FRACTIONS ±1/32 DECIMALS XX ± .02 XXX ± .01 ANGLES ±1/2
SURFACE ROUGHNESS BREAK SHARP EDGES .020 MAX. ✓
MATERIAL —
FINISH —

DR. S.E.O. DATE 1.24.79
CHK. P.M. DATE 3.16.79
APP. P.M. DATE 3.16.79
APPROVAL
OUTSIDE APP.

REMEX — A UNIT OF EX-CELL-O CORPORATION — 1733 ALTON STREET IRVINE, CALIF 92714

TITLE: CARRIAGE ASSEMBLY

CODE IDENT. NO. | SIZE C | DWG. NO. 114240-* | M

SCALE 2:1 | DO NOT SCALE DRAWING | SHEET 1 OF 1

FORM No. ED 603/011

114240-* M

Figure 6-1. Carriage Assembly 114240, RFS2400.

SECTION VII

PARTS LIST

7.1 GENERAL

This section lists the electronic and mechanical parts used on the RFS4810, RFS4820, RFS2410 and RFS2420. Standard hardware items are not listed. Model number identification is given in Section 1.8. To obtain correct parts, the model number must be obtained from the identification tag located on the unit.

Indented items are part of the assembly under which they are indented and the quantity of these items are per each assembly. Reference designations refer to the parts illustrated in Figures 7-1 through 7-4. The designations in Figures 7-2 through 7-4 are the same for the parts illustrated in Figure 7-1. The reference designations include a figure number and a part designation number which appears on that figure to locate the part. All electronic components are identified by letter-number combinations such as S1 and T1. Mechanical parts are identified by number only. Reference designations in parenthesis are associated with the parenthetical item. These items are generally individual items and not part of the referenced assembly, but are related back to the associated item for ease of location and association. Tables 7-6 and 7-7 contain the printed circuit card components for the master and slave cards, respectively.

All parts are available from REMEX Spares Order Desk, 1733 Alton St., P.O. Box C-19533, Irvine, Ca 92713.

7.2 KIT OF PARTS

The kit of parts is used for installation and maintenance. Refer to Table 1-1 for the listing.

7.3 RECOMMENDED SPARE PARTS

Tables 7-1 and 7-2 lists the recommended spare parts. It is important when ordering spare parts, that the model number be identified and the spare parts be ordered accordingly.

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-1. Recommended Spare Parts List, RFS4810/814235-00X and RFS4820/814236-00X.

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Belt, Drive, Top Assemblies 824235-002, 814236-002. 60Hz	716001-107	1	1
Belt, Drive, Top Assemblies 814235-001, 003, 004 814236-001, 003, 004, 50 Hz	716001-108	1	1
Carriage Assembly	114745-002	1	6
Housing, Index L.E.D. Assembly	113948-001	1	20
Motor Assembly, Drive, Top Assemblies 814235-001, 814236-001, 115 VAC, 50Hz	114166-001	1	7
Motor Assembly, Drive, Top Assemblies 814235-002, 814236-002, 115 VAC, 60Hz	114166-002	1	7
Motor Assembly, Drive, Top Assemblies 814235-003, 814236-003, 220 VAC, 50Hz	114167-001	1	7
Motor Assembly, Drive, Top Assemblies 814235-004, 814236-004, 220 VAC, 50Hz	114167-003	1	7
Motor, Subassembly, Stepper	113945-001	1	39
Printed Circuit Card Assembly, Drive Assemblies, Master 814235-001 thru -003	114101-001	1	PC1
Printed Circuit Card Assembly, Slave 814236-001 thru -003	114181-001	1	PC1
Release, Button Assembly with LED	114244-001	1	44
Solenoid, Head Load, REMEX Specification	715067-114	1	18
Solenoid, Front Panel	715067-112	1	45
Switch, Door Open, SPDT, Micro Switch IDM79MNA6943	715059-194	1	S1
Switch Assembly, Write Protect	114086-001	1	29

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-2. Recommended Spare Parts List, RFS2410/814230-00X and RFS2420/814231-00X.

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Belt, Drive, Top Assemblies, 814230-002, 814231-002, 60Hz	716001-107	1	1
Belt, Drive, Top Assemblies 814230-001,003,004 814231-001,003,004, 50 Hz	716001-108	1	1
Carriage Assembly	114240-004	1	6
Head Pad Cartridge Assembly	112800-001	1	MM
Housing, Index LED Assembly	113948-001	1	20
Motor Assembly, Drive, Top Assemblies 814230-001, 814231-001, 115 VAC, 50Hz	114166-001	1	7
Motor Assembly, Drive, Top Assemblies 814230-002, 814231-002, 115 VAC, 60Hz	114166-002	1	7
Motor Assembly, Drive, Top Assemblies 814230-003, 814231-003, 220 VAC, 50Hz	114167-001	1	7
Motor Assembly, Drive, Top Assemblies 814230-004, 814231-004, 220 VAC, 50Hz	114167-003	1	7
Motor, Subassembly, Stepper	113945-001	1	39
Printed Circuit Card Assembly, Drive Assemblies, Master, 814230-001 thru -003	114101-001	1	PC1
Printed Circuit Card Assembly, Drive 814231-001 thru -003	114181-001	1	PC1
Release, Button Assembly with LED	114244-001	1	44
Solenoid, Head Load, REMEX Specification	715067-114	1	18
Solenoid, Front Panel	715067-112	1	45
Switch, Door Open, SPDT, Micro Switch IDM79MNA6943	715059-194	1	S1
Switch Assembly, Write Protect	114086-001	1	29

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-3. Parts List RFS4810 and RFS4820

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
RFS4810/814235-001	814235-001	1	Ref.
RFS4810/814235-002	814235-002	1	Ref.
RFS4810/814235-003	814235-003	1	Ref.
RFS4810/814235-004	814235-004	1	Ref.
RFS4820/814236-001	814236-001	1	Ref.
RFS4820/814236-002	814236-002	1	Ref.
RFS4820/814236-003	814236-003	1	Ref.
RFS4820/814236-004	814236-004	1	Ref.
Unless specifically noted, the following subassemblies apply to all models:			
. Belt, Drive, 814235-002 and 814236-002 Only, 60Hz	716001-107	1	1
. Belt, Drive, 814235-001, 003, 004 and 814236-001, 003, 004 Only, 50 Hz	716001-108	1	1
. Cable Assembly, External Write Protect	114605-001	1	
. Cable Tie, Panduit PLT3S	715040-167	1	2
. Cable Tie, Panduit PLT1M-MP	715040-146	4	
. Clamp, Guide Rod	113926-001	2	4
. Clamp, Head Cable, Weckesser 1-8/4	715040-152	1	5
. Carriage Subassembly	114745-002	1	6
. . Except for the items listed below the entire carriage, subassembly, should be replaced as a complete assembly.			
. . Band, Assembly	114770-001	1	
. . Pulley, Band	113900-004	1	
. Decal Identification	114985-001	1	
. Decal, UL Recognized	114128-001	1	
. Decal, CSA	114719-001	1	
. Disk Friction	114649-001	1	
. Drive Motor Assembly, 814235-001 and 814236-001 Only, 115 VAC, 50Hz	114166-001	1	
. . Except for the following parts, it is recommended that this item be replaced as a complete assembly.			

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-3. Parts List RFS4810 and RFS4820 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. Drive Motor Assembly, Cont'd			
. . Boot, Insulation	715091-124	1	
. . Bracket, A.C. Connector	113929-001	1	(J8),35
. . Capacitor, 2 µf, 370 VAC	702458-205	1	59
. . Pulley, 50 Hz	112819-004	1	52
. Drive Motor Assembly, 814235-002 and 814236-002, 115 VAC, 60 Hz	114166-002	1	
. Subassembly is same as 114166-001, except:			
. . Pulley, 60 Hz	112819-002	1	52
. Drive Motor Assembly, 814235-003 and 814236-003 Only, 220 VAC, 50 Hz	114167-001	1	7
. . Except for the following parts it is recommended that this item be replaced as a complete assembly:			
. . Boot, Insulation	715019-124	1	
. . Bracket, A.C. Connector	113929-001	1	(J8),35
. . Capacitor, 2 µf, 370 VAC	702458-205	1	59
. . Pulley, Drive Motor, 6 mm Shaft or	112819-005	1	52
. . Pulley, Drive Motor, 5/16" Shaft	112819-004	1	52
. Drive Motor Assembly, 814235-004 and 814236-004	114167-003	1	7
. . Except for the following parts, it is recommended that this item be replaced as a complete assembly.			
. . Boot, Insulation	715019-124	1	
. . Bracket, A.C. Connector	113929-001	1	(J8),35
. . Capacitor, 2 µf, 370 VAC	702458-205	1	59
. . Pulley	112819-005	1	52
. Flexible Disk Drive Subassembly	114247-001	1	Ref.
. . Clamp, Anchor	715040-164	4	8
. . Carrier Assembly	114248-001	1	Ref.
. . . Except for the following parts, it is recommended that this item be replaced as a complete assembly:			
. . . Bracket, Diskette Lift, Left	115007-001	1	9

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-3. Parts List RFS4810 and RFS4820 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. . Carrier Assembly, Cont'd			
. . . Bracket, Diskette Lift, Right	115007-002	1	10
. . . Carrier Eject Assembly	114344-001	1	
. . . . Carrier, Eject	113915-002	1	11
. . . . Roll Pin	713730-005	1	12
. . . . Spring	114427-001	1	13
. . . Expanding Clutch Assembly	112747-001	1	15
. . . Head Load Solenoid Assembly	114085-001	1	
. . . . Arm, Diskette Load	114150-001	1	16
. . . . Bracket, Disk Load	114088-001	1	17
. . . . Pad, Diskette Load	112761-001	1	50
. . . . Solenoid, REMEX Spec.	715067-114	1	18
. . . Pin, Clutch	114273-001	1	21
. . . Pin, Roll, Spring	713710-006	1	22
. . . Ring, Retaining, Truarc 5133-25	715025-136	1	23
. . . Shim, Bearing, Allied Devices AD3080	715030-226	1	24
. . . Spring, Carrier	113922-001	2	25
. . . Spring, Compression, Associated Spring Co. C0360-040-0620M	714090-151	1	26
. . . Spring, Eject Carrier	113921-001	1	27
. . . Switch Assembly, Write Protect	114086-001	1	
. . . . Housing	113918-001	1	28
. . . . Switch, Optical	704214-016	1	29
. . Door, Latch Plate Assembly	114249-001	1	
. . . Door	114079-001	1	30
. . . Pad, Foam, 3/16" x 1/2" x 5.10"	114989-001	1	31
. . . Plate, Latch	114156-001	1	32
. . Harness Assembly, Flexible Disk Drive	113947-001	1	(P2)
. . . Except for the items listed below it is recommended that the Harness Assembly be replaced as a complete assembly.			
. . . Connector, 34 pin, black Amp 3-87456-0	706510-335	1	P2
. . . Connector, 5 pin, Amp 87499-9	706510-336	1	P7

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-3. Parts List RFS4810 and RFS4820 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. . Harness Assembly, Cont'd			
. . . Contact, Amp 87667-5	706530-179	28	(P2,P7)
. . . Contact, Berg 75374-004	706530-181	9	
. . . Housing, Index LED Assembly	113948-001	1	20
. . . Key, Polarizing, Amp 87077	706540-158	2	(P2,P7)
. . . Resistor, 62 ohm, 10W	701020-005	2	R1,R2
. . . Sensor, Single Sided Assembly	114075-001	1	47
. . . Sensor, Two-Sided Assembly	114076-001	1	48
. . . Terminal, Push-On	715005-143	7	
. . Main Frame Subassembly	114246-001	1	
. . . Bearing, Lower, New Hamp. SFR 1883PPK251122	714000-141	1	33
. . . Bearing, Upper, Nippon Miniature Bearing, R-4ZZRA3P15LG-20	714000-125	1	34
. . . Bracket, AC Connector	113929-001	1	(J8) 35
. . . Bracket, Track 00 Assembly	114094-001	1	Ref.
. . . . Bracket	114153-001	1	36
. . . . Optical Switch	704214-016	1	56
. . . Frame, Main	113937-001	1	37
. . . Hub, Drive (when ordering new drive hub, also order Bearing, Lower and Bearing, Upper)	113934-001	1	38
. . . Motor Assembly, Stepper	113944-003	1	Ref.
. . . . Step Motor Subassembly	113945-001	1	39
. . . . Motor Plate Assembly	114675-001	1	60
. . . Panel Assembly, Front	114245-001	1	
. . . Except for the items listed below, it is recommended that the Panel Assembly be replaced as a complete assembly.			
. . . . Catch	113909-001	1	40
. . . . Latch Assembly	114096-001	1	41
. . . . Panel	114078-001	1	43
. . . . Release, Button Assembly and LED	114244-001	1	44
. . . . Solenoid, 12 VDC, REMEX Spec.	715067-112	1	45
. . . Pulley, Hub	112818-002	1	46
. . . Spring	714090-146	1	49

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-3. Parts List RFS4810 and RFS4820 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. . Main Frame Subassembly, Cont'd			
. . . Switch, Door Open, SPDT, Micro Switch IDM79MNA6943	715059-194	1	S1
. . Shield Assembly, Lower Head	114398-001	1	
. Guide Rod	113904-002	2	51
. Printed Circuit Card Assembly 814235-001 thru -004	114101-001	1	PC1
. Printed Circuit Card Assembly 814236-001 thru -004	114181-001	1	PC1
. Shield, Head, Assembly	114638-001	1	57
. Support, Corner	114171-001	2	58

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-4. Parts List RFS2410 and RFS2420

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
RFS2410/814230-001	814230-001	1	Ref.
RFS2410/814230-002	814230-002	1	Ref.
RFS2410/814230-003	814230-003	1	Ref.
RFS2410/814230-004	814230-004	1	Ref.
RFS2420/814231-001	814231-001	1	Ref.
RFS2420/814231-002	814231-002	1	Ref.
RFS2420/814231-003	814231-003	1	Ref.
RFS2420/814231-004	814231-004	1	Ref.
Unless specifically noted, the following subassemblies apply to all models:			
. Belt, Drive, 814230-002 and 814231-002 Only, 60Hz	716001-107	1	1
. Belt, Drive, 814230-001, 003, 004 and 814231-001, 003, 004 Only, 50 Hz	716001-108	1	1
Cable Assembly, External Write Protect	114605-001	1	
. Cable Tie, Panduit PLT3S	715040-167	1	2
. Cable Tie, Panduit PLT1M-MP	715040-146	1	3
. Clamp, Guide Rod	113926-001	2	4
. Clamp, Head Cable, Weckesser 1-8/4	715040-111	1	5
. Carriage Subassembly	114240-004	1	6
. . Except for the items listed below, the entire Carriage, Subassembly, should be replaced as a complete assembly.			
. . Band, Assembly	114378-001	1	
. . Head Pad Cartridge Assembly	112800-001	1	
. . Pulley, Band	113900-002	1	
. Decal, Product Identification	114985-001	1	
. Decal, UL Recognized	114128-001	1	
. Decal, CSA	114719-001	1	
. Disk, Friction	114649-001	1	
. Drive Motor Assembly, 814230-001 and 814231-001, Only 115 VAC	114166-001	1	7
. . Except for the following items, it is recommended that this item be replaced as a complete assembly.			

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-4. Parts List RFS2410 and RFS2420 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. Drive Motor Assembly, Cont'd			
. . Boot Insulation	715019-124	1	
. . Bracket, A.C. Connector	113929-001	1	(J8),35
. . Capacitor, 2 µf, 370 VAC	702458-205	1	59
. . Pulley, 50 Hz	112819-004	1	
. Drive Motor Assembly 814230-002 and 814231-002, 115 VAC, 60 Hz	114166-002	1	
. . Subassemblies are the same as 114166-001 except:			
. . Pulley 60 Hz	112819-002	1	52
. Drive Motor Assembly, 814230-003 and 814231-003 Only, 220 VAC, 50 Hz	114167-001	1	7
. . Except for the following items it is recommended that this item be replaced as a complete assembly:			
. . Boot, Insulation	715019-124	1	
. . Bracket, A.C. Connector	113929-001	1	(J8),35
. . Capacitor, 2 µf, 370 VAC	702458-205	1	59
. . Pulley Drive Motor, 6 mm Shaft or	112819-005	1	52
. . Pulley Drive Motor, 5/16" Shaft	112819-004	1	52
. Drive Motor Assembly, 814230-004 and 814231-004	114167-003	1	7
. . Except for the following items it is recommended that this item be replaced as a complete assembly:			
. . Boot, Insulation	715019-124	1	
. . Bracket, A.C. Connector	113929-001	1	(J8),35
. . Capacitor 2 µf, 370 VAC	702458-205	1	59
. . Pulley	112819-005	1	52
. Flexible Disk Drive Subassembly	114247-001	1	Ref.
. . Clamp Anchor	715040-164	4	8
. . Carrier Assembly	114248-001	1	
. . . Except for the following parts, it is recommended that this item be replaced as a complete assembly:			
. . . Bracket, Diskette Lift, Left	115007-001	1	9
. . . Bracket, Diskette Lift, Right	115007-002	1	10
. . . Carrier Eject Assembly	114344-001	1	
. . . . Carrier, Eject	113915-002	1	11
. . . . Roll Pin	713730-005	1	12

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-4. Parts List RFS2410 and RFS2420 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. . Harness Assembly, Cont'd			
. . . Sensor, Two-Sided Assembly	114076-001	1	48
. . . Terminal, Push-On	715005-143	7	
. . Main Frame, Subassembly	114246-001	1	
. . . Bearing, Lower, New Hamp. SFR1883PPK25/122	714000-141	1	33
. . . Bearing, Upper, Nippon Miniature R-4ZZRA3P15LG-20	714000-125	1	34
. . . Bracket, AC Connector	113929-001	1	(J8) 35
. . . Bracket, Track 00 Assembly	114094-001	1	Ref.
. . . . Bracket	114082-001	1	36
. . . . Optical Switch	704214-016	1	56
. . . Frame, Main	113937-001	1	37
. . . Hub, Drive (when ordering new drive hub, also order Bearing, Lower and Bearing, Upper).	113934-001	1	38
. . . Motor Assembly, Stepper	113944-003	1	Ref.
. . . . Step Motor Subassembly	113945-001	2	39
. . . . Motor Plate Assembly	114675-001	1	60
. . . Panel Assembly, Front	114245-001		
. . . . Except for the items listed below, it is recommended that the Panel Assembly be replaced as a complete assembly.			
. . . . Catch	113909-001	1	40
. . . . Latch Assembly	114096-001	1	41
. . . . Panel	114078-001	1	43
. . . . Release, Button Assembly	114244-001	1	44
. . . . Solenoid, 12 VDC, REMEX Spec.	715067-112	1	45
. . . Pulley, Hub	112818-002	1	46
. . . Spring	714090-146	1	49
. . . Switch, Door Open, SPDT, Micro Switch IDM79MNA943	715059-194	1	S1
. Guide Rod	113904-002	2	51
. Printed Circuit Card Assembly (814230-001 thru -003)	114101-001	1	PC1
. Printed Circuit Card Assembly (814236-001 thru -003)	114181-001	1	PC1

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-4. Parts List RFS2410 and RFS2420 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. Shield, Head, Assembly	114638-001	1	57
. Stop, Carriage	114677-001	1	
. Support, Corner	114171-001	2	58

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-4. Parts List RFS2410 and RFS2420 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
. . . Carrier Eject Assembly, Cont'd			
. . . . Spring	114427-001	1	13
. . . Expanding Clutch Assembly	112747-001	1	15
. . . Head Load Solenoid Assembly	114085-001	1	
. . . . Arm, Diskette Load	114150-001	1	16
. . . . Bracket, Disk Load	114088-001	1	17
. . . . Pad, Diskette Load	112761-001	1	50
. . . . Solenoid, REMEX Spec.	715067-114	2	18
. . . Pin, Clutch	114273-001	1	21
. . . Pin, Roll, Spring	713910-006	1	22
. . . Ring, Retaining, Truarc 5133-25	715025-136	1	23
. . . Shim, Bearing, Allied Devices AD3080	715030-226	1	24
. . . Spring, Carrier	113922-001	2	25
. . . Spring, Compression, Associated Spring Co. C0360-040-0620M	714090-151	1	26
. . . Spring, Eject Carrier	113921-001	1	27
. . . Switch Assembly, Write Protect	114086-001	1	
. . . . Housing	113918-001	1	28
. . . . Switch, Optical	704214-016	1	29
. . Door, Latch Plate Assembly	114249-001	1	
. . . Door	114079-001	1	30
. . . Pad, Foam, 3/16" x 1/2" x 5.10	114989-001	1	31
. . . Plate, Latch	114156-001	1	32
. . Harness Assembly, Flexible Disk Drive	113947-001	1	(P2)
. . . Except for the items listed below it is recommended that the Harness Assembly be replaced as a complete assembly.			
. . . Connector, 34 pin, black, Amp 3-87456-0	706510-335	1	P2
. . . Connector, 5 pin, Amp 87499-9	706510-336	1	P7
. . . Contact, Amp 87667-5	706530-179	28	(P2,P7)
. . . Contact, Berg 75374-004	706530-181	9	
. . . Housing, Index, LED Assembly	113948-001	1	20
. . . Key, Polarizing, Amp 87077	706540-158	2	(P2,P7)
. . . Resistor, 62 ohm, 10W	701020-005	2	R1,R2
. . . Sensor, Single Sided Assembly	114075-001	1	47

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-5. Miscellaneous and Optional Parts.

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Kit of Parts, RFS4810/2410, See Table 1-1	114306-001	1	
Kit of Parts, RFS4820/2420, See Table 1-1	114307-001	1	
Kit of Parts, RFS4810/2410, See Table 1-1 Contents are identical to 114306-001 except delete manual.	114306-002	1	
Connector, 2 pin, Amp 530153-2 (Used as jumpers when connecting customer installed options)	706510-314		
Conversion Kit, RMF0055	814389-001	1	
. Converts 814230-002, 814231-002 814235-002 and 314236-002 to 220VAC, 50 Hz			
. Belt, Drive	716001-108	1	
. Decal, Identification	716018-113	1	
. Drawing, Instruction	114393-001	1	
. Motor Assembly	114167-001	1	
. Pulley, Drive	112819-004	1	
Conversion Kit, RMF0056	814394-001		
. Converts 814230-003, 814231-003, 814235-003 and 814236-003, from 220VAC, 50Hz to 115VAC, 60Hz.			
. Belt, Drive	716001-107	1	
. Instruction Drawing	114390-001	1	
. Identification Decal	716018-113	1	
. Motor Assembly	114166-002	1	
. Pulley, Drive	112819-002	1	
Conversion Kit, RMF058	814403-001	1	
. Converts 814230-002, 814231-002, 814235-002 & 814236-002 from 115VAC, 60Hz to 115VAC, 50Hz			
. Belt, Drive	716001-108	1	
. Decal, Identification	716018-113	1	
. Drawing, Instruction	114405-001	1	
. Pulley, Drive	112819-004	1	
Conversion Kit, RMF059	814404-001	1	
. Converts 814230-001, 814231-001, 814235-001 and 814236-001 from 115VAC, 50Hz, to 115VAC, 60Hz.			
. Belt, Drive	716001-107	1	
. Decal, Identification	716018-113	1	
. Drawing, Instruction	114406-001	1	
. Pulley, Drive	112819-002	1	

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Table 7-6. Printed Circuit Card Assembly Master Card, 114101-001.

The following parts list was written for the G assembly and the P schematic revision. Subsequent changes are contianed on a P.C. Card Change Record Form contained in the addemdum.

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Capacitor, 1000pf, 100V, Dipped Mica, El Menco DM15-102J	702124-102	2	C1,C6
Capacitor, 39 pf, 300V, Dipped Mica, El Menco DM5	702123-390	2	C2,C7
Capacitor, 0.01µf, 25V, Ceramic Disk, Automation Components AC1-Z5V-103Z-25V	702137-103	40	C3,4,15,16,19 20,24-27,31,32, 34-39,41,44-46, 50-55, 57-59, 62-68, 83,85
Capacitor, 22pf, 300V, Dipped Mica El Menco DM5CC220J	702123-220	3	C5,9, 43
Capacitor, 0.056µf, 100V, Metallized Mylar, Electrocube 217A1B563K Ceramic	702181-563	1	C8
Capacitor, 0.01µf, 200V, Type CK06	702128-103	2	C10,C14
Capacitor, 0.1µf, 50V, Metallized Polyester, Elpac Z5R 104K	702180-104	1	C11
Capacitor, 0.22µf, 35V, Polarized Solid Tantalum, Sprague 196D224X9035JA1	702396-224	2	C12, C13
Capacitor, 10µf, 25V, Solid Tantalum, Polarized, Sprague 196D106X9025KA1	702395-106	2	C17,18
Capacitor, 47µf, 6.3V, Electrolytic, Matsushita ECE-AXXV476L	702366-476	5	C21,C22,C40, C79,C84
Capacitor, 0.01µf, 100V, Metallized Mylar, IMBXP7B103X	702181-103	1	C23
Capacitor, 200pf, 300, Dipped Mica, El Menco DM5CC201J	702123-201	1	C28
Capacitor, .22µf, 50V, Ceramic, Monolythic Sprague Type 7C	702131-224	9	C29,C30,C33, C76-78,C81,82,88
Capacitor, 100pf, 200V, Ceramic, Type CK05	702128-101	2	C42,C47
Capacitor, 0.001µf, 100 V, Metallized Mylar, Electrocube 217A1B102K	702181-102	1	C48
Capacitor, 1µf, 35V Sprague 196D105X9035HA1	702396-105	1	C49
Capacitor, 47µf, 25V, Electrolytic, Sprague 501D476F025XX	702641-476	1	C56
Capacitor, 15µf, 15V Sprague 196D156X9015JA1	702394-156	2	C60,C61
Capacitor, 10µf, 50V, Electrolytic, Sprague Type TE	702372-106	1	C70
Capacitor, 10µf, 25V, Electrolytic, Matsushita ECE-AXXV106L	702366-106	1	C80
Capacitor, 82pf, 300V, Dipped Mica, El Menco DM5CC820J	702123-820	1	C87
Choke, 33µH, ± 5%, DINK-33	702500-125	2	L1,L2
Choke, 150µH, ± 5%, RFC-S-33	702500-126	5	L3-L7
Choke, 4.7µH	702500-128	1	L8

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM (IF PRESENT) AT THE REAR OF THE MANUAL FOR POSSIBLE PART NUMBER CHANGES.

Table 7-6. Printed Circuit Card Assembly Master Card, 114101-001 (Continued).

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Connector, 34 pin, Circuit Assembly Corp. CA-D34RSP100-230-090	706500-346	1	J1
Connector, 26 pin, Circuit Assembly Corp. CA-D26RSP100-230-090	706500-345	1	J2
Connector, 6 pin, Molex 09-88-2061	706500-347	1	J3
Connector, 6 pin, Molex 22-12-2061	706500-295	2	J4,J5
Connector, 10 pin, Amp 1-87233-0	706500-340	1	J6,J7
Connector, 34 pin, Amp 1-87230-7	706500-335	1	J8
Crystal, 8MHz, Cal Crystal HC-18/8.0MHz	703800-111	1	Y1
Diode, FDH6666	704000-110	16	CR1-CR13, CR15,16,19
Diode, 5.1V Zener, IN751A	704010-116	1	CR14
Diode, 3.6V Zener, IN747A	704010-126	1	CR17
Diode, IN4003	704005-137	6	CR18,20-24
I.C. Package 592	704520-145	2	Z1,Z5
I.C. Package 8T20	704610-172	1	Z2
I.C. Package 74LS74	704620-074	6	Z3,Z6,Z16, Z32,Z58,Z74
I.C. Package 96LS02	704621-004	5	Z4,Z7,Z25, Z33,Z49
I.C. Package 7406	704600-111	1	Z10
I.C. Package 74LS00	704620-000	7	Z11,13,22,26, 38,40,48
I.C. Package 74LS293	704620-293	2	Z12,Z34
I.C. Package Q2T2905	704202-113	1	Z14
I.C. Package 74LS145	704620-145	1	Z15
I.C. Package 74LS02	704620-002	1	Z17
I.C. Package 74LS624	704620-624	1	Z18
I.C. Package 75462	704600-160	2	Z19,Z51
I.C. Package 2114	704810-130	4	20,21,27,28
I.C. Package 74LS151	704620-151	1	Z23
I.C. Package 74LS164	704620-164	2	Z24,Z45
I.C. Package 74LS273	704620-273	1	Z29
I.C. Package 74LS10	704620-010	1	Z31
I.C. Package Programmed 2532	114259-001	1	Z36
I.C. Package 6875	704810-133	1	Z37
I.C. Package 74LS04	704620-004	2	Z39,Z50
I.C. Package 74LS32	704620-032	2	Z41,Z46
I.C. Package 556	704520-134	2	Z42,Z44
I.C. Package, Resistor 10K	701900-007	1	Z43
I.C. Package 74LS54	704620-054	1	Z47
I.C. Package 68B00	704810-132	1	Z52
I.C. Package 68B21	704810-124	1	Z53
I.C. Package FD1791-2	704810-141	1	Z54
I.C. Package 74LS244	704620-244	1	Z55
I.C. Package 74LS368	704620-368	1	Z56

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Table 7-6. Printed Circuit Card Assembly Master Card, 114101-001 (Continued).

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
I.C. Package 74LS86	704620-086	1	Z57
I.C. Package, Programmed 82S103	114260-001	1	Z62
I.C. Package 8304	704621-001	1	Z63
I.C. Package 74LS240	704620-240	1	Z64
I.C. Package 74LS373	704620-373	2	Z65,Z66
I.C. Package ULN2074B	704900-111	1	Z67
I.C. Package UHP407	704900-110	1	Z68
I.C. Package 78L12	704520-144	1	Z69
I.C. Package 7905	704520-137	1	Z72
I.C. Package 78L05	704520-139	1	Z73
Resistor, 33K, 1/4W, ±5%	701003-333	2	R2,R3
Resistor, 2.2K, 1/4W, ±5%	701003-222	13	R4-R7,R22,R37, R43,R62,R65, R67,R79,R84,R96
Resistor, 5.1K, 1/4W, ±5%	701003-512	2	R8,R18
Resistor, 221 ohm, 1/8W, ±1%	701202-210	3	R9,R10,R54
Resistor, 75 ohm, 1/4W, ±5%	701003-750	3	R11,R12,R53
Resistor, 1.5K, 1/4W, ±5%	701003-152	3	R13,R14,R35
Resistor, 150 ohm, 1/4W, ±5%	701003-151	4	R15,R19,R49,R52
Resistor, 24K, 1/4W, ±5%	701003-243	3	R16,R17,R68
Resistor, 10 ohm, 1/4W, ±5%	701003-100	5	R20,21,77,78
Resistor, 51K, 1/4W, ±5%	701003-513	1	R23
Resistor, 10K, 1/8W, ±1%	701201-002	2	R24,R25
Resistor, 5.62K, 1/8W, ±1%	701205-621	2	R26,R27
Resistor, 1.33K, 1/8W, ±1%	701201-331	2	R28,R31
Resistor, 1K, 1/8W, ±1%	701201-001	2	R29,R30
Resistor, 18K, 1/4W, ±5%	701003-183	2	R32,R61
Resistor, 12.1K, 1/8W, ±1%	701201-212	1	R33
Resistor, 866 ohm, 1/8W, ±1%	701208-660	1	R34
Resistor, 1K, 1/4W, ±5%	701003-102	11	R36,38,39,46-48, 82,83,92,93,97
Resistor, 10K, 1/4W, ±5%	701003-103	11	R41,42,45,50, R64,66,73,74, R85,94,95
Resistor, 43 ohm, 1/2W, ±5%	701004-430	1	R44
Resistor, 1.8K, 1/4W, ±5%	701003-182	1	R51
Resistor, 470 ohm, 1/4W, ±5%	701003-471	2	R57
Resistor, 27 ohm 1/4W, ±5%	701003-270	1	R56
Resistor, 240 ohm, 1/4W, ±5%	701003-241	1	R55, R58
Resistor, 82 ohm, 1/4W, ±5%	701003-820	1	R59
Resistor, 100 ohm, 1/4W, ±5%	701003-101	4	R69-R72
Resistor, 68 ohm, 2W, ±1%	701050-102	1	R75
Resistor, 100 ohm, 2W, ±1%	701050-101	1	R76

P.C. CARD CHANGE RECORD

CARD ASSY NO. 114101-001
SCHEMATIC NO. 114102-001

SCH REV	ASSY REV	FAB REV	DESCRIPTION OF CHANGE
E	E	D	Changed Z72 from 79M05 to 7905, P/N 704520-137; changed Z48 from 74LS08 to 74LS00, P/N 704620-000; added connector sockets Y, J, Z, F, AA, BB. A special adapter P.C. Assembly is used in place of Z37 when the I.C. Package 6875 is not available. When this assembly is used, Y1 and C49 are removed. See Sheet 13 for schematic. Deleted C69 and added C85, 0.01 µf, 25V, P/N 702137-103. Added R94, Resistor 2.2K 1/4W, ± 5%. On sheet 3, zones B8, C8 tied J5-5 to CT0* and J4-4 to CT1*; on sheet 6, zone E7, E8 added R94, C85. Added TP22 (10B2) and TP21 (11D3). Sheet 12 changed locations of jumpers V, W, X. An option -5V or -6V to -12V input can be used at J3-1. A jumper table on sheet 12 shows the connections for jumper AA, BB and CC depending upon the input of -V.
F	E_1	D	On sheet 8, replaced Z54 with FD1791-02, P/N 704810-141. All connections are the same except pin 33 ties to + 5V through resistor R95, 10K, P/N 701003-103. On sheet 6, tie Z37, pin 1 to ground through a 22 pf, 300V capacitor C86, P/N 702123-220.
G	E_2	D	On sheet 6 added P.C. Adapter Card 114541-001. Added C86. Transferred Y1 and Z37 from 114101-001 card to 114541-001 card.
H	E_3	D	On page 8-21/8-22, Figure 8-5, Sheet 6 of 13, Zone E7 change reference designation R94 to R96. On sheet 4 of 13, Figure 8-5 change R23 from 47K to 51K, 1/4W, ± 5%, P/N 701003-513. Make these changes also to Table 7-6, page 7-15.
J	E_4	D	On page 8-29/8-30 and pages 7-13, 7-14 and 7-15 make the following changes: Z18 changes from 74LS324 to 74LS624, P/N 704620-624: C28 changes from 22 pf to 75 pf, P/N 702123-750; R56 changes from 27 ohm to 10 ohm, P/N 701003-100; R58 changes from 470 ohm to 270 ohm, P/N 701003-271; R59 changes from 27 ohm to 180 ohm, P/N 701003-181.
K	E_5	D	C28 changes from 75 pf to 200 pf, P/N 702123-201; R59 changes from 180 ohm to 82 ohm, P/N 701003-820; R55 and R58 changes from 470 and 270 ohm, respectively to 240 ohm, each, P/N 701003-241; R56 changes from 10 ohm to 27 ohm.
L	E_6	D	Changes incorporated from K level since K was never released. On sheet 8, Z41-12 connect to Z34-4 instead of Z34-5. Pin Z34-5 now is not connected.

P.C. CARD CHANGE RECORD

CARD ASSY NO. 114101-001
SCHEMATIC NO. 114102-001

SCH REV	ASSY REV	FAB REV	DESCRIPTION OF CHANGE
M	F	E	Removed adapter card and incorporated its components into circuit card:
			R97, C88, C87, Y1. L8, I.C. package 6875. See Table 7-6.
M	F_1	E	F_1 assembly revision did not affect schematic or parts list.
N	F_2	E	On sheet 12, R75 changed to ± 1%, P/N 701050-102;
			R76 changed to ± 1%, P/N 701050-101.
			Capacitor, C56, changed to 47 µf, 25V, ± 20% Polar, P/N 702641-476.
P	G	F	Added Connector Socket DD-EE P/N 706510-314;
			Added Terminal Post DD, EE, FF, P/N 706530-175;
			Changed schematic, sheet 6, Zone C4 to add DD, EE and FF.
			These terminals used in production test.

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM (IF PRESENT) AT THE REAR OF THE MANUAL FOR POSSIBLE PART NUMBER CHANGES.

Table 7-6. Printed Circuit Card Assembly Master Card, 114101-001

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Resistor, 39K, 1/4W, ±5%	701003-393	2	R80,R81
Resistor, 3.3K, 1/4W, ±5%	701003-332	6	R86-R91
Resistor, Variable, 50K, Spectrol 64W503T000	701676-503	2	R1,R60
Resistor, Variable, 10K, Spectrol 64W103T000	701676-103	2	R40,R63
Socket, Connector, Berg 65474-001	706510-314	8	PR,ML,TU,WV, YJ,ZF,AA-BB, DD-EE
Socket, I.C., 18 pin, Robinson Nugent ICA-183-SG	706515-147	4	Z20,21,27,28
Socket, I.C., 40 pin, Robinson Nugent ICN-406-S4-T	706515-139	4	Z30,52-54
Socket, I.C., 24 pin, Robinson Nugent ICN-246-S4-T	706515-137	2	Z35,Z36
Socket, I.C., 28 pin, Robinson Nugent ICN-286-S4-T	706515-138	1	Z62
Terminal, Post Amp 85931-6	706530-144	42	TP1-8,10, 12-16,19-22 F-FF
Transistor, NPN, 2N4401	704203-114	4	Q1,2,3,5
Transistor, PNP, 2N4403	704202-108	1	Q4

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-7. Printed Circuit Card Assembly: Slave Card, 114181-001

The following parts list was written for the H assembly and the J schematic revision. Subsequent changes are contained on a P.C. Card Change Record Form contained in the addendum.

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Capacitor, 0.01 µf,100V, Metallized Mylar, IMBXP7B103X	702181-103	3	C1,C3,C31
Capacitor, 0.1 µf, 50V, Metallized Mylar, IMBXP7B104X	702181-104	1	C2
Capacitor, 0.22 µf, 35V, Polarized Sprague 196D224X9035JA1	702396-224	2	C4,C5
Capacitor, 1000 pf, 100V, Dipped Mica, El Menco DM15-102J	702124-102	2	C6,C7
Capacitor, 39 pf, 300V, Dipped Mica, El Menco DM5	702123-390	2	C8,C9,
Capacitor, 0.01 µf, 25V, Ceramic Disc Automation Components AC1-Z5V-103Z-25V	702137-103	24	C10,11,15,18,19, 20,23-25,27-30, 32,35,37,39,41-46,51
Capacitor, 10 µf, 25V, Solid Tantalum, Polarized, Sprague 196D1D6X9025KA1	702395-106	2	C13,C14
Capacitor, 0.22 µf, 50V, Ceramic, Monolythic, Sprague Type 7C	702131-224	3	C16,C17,C50
Capacitor, 15 µf, 15V Sprague 196D156X9015JA1	702394-156	2	C21,C22
Capacitor, 47µf, 25V, Electrolytic Sprauge 501D476F025XX	702641-476	1	C26
Capacitor, 0.056 µf, 100V, Metallized Mylar, Electrocube 217A1B563K	702181-563	1	C33
Capacitor, 1µf, 35V Sprague 196D105X9035HA1	702396-105	1	C34
Capacitor, 47 µf, 6.3V, Electrolytic Matsushita ECE-AXXV476L	702366-476	4	C36,C48,C52 C53
Capacitor, 10 uf, 50V, Electrolytic, Sprague Type TE	702372-106	1	C47
Capacitor, 10 µf, 25V, Electrolytic Matsushita ECE-AXXV106L	702366-106	1	C49
Capacitor, 22 pf, 300V, Dipped Mica, El Menco DM15-102J	702123-220	2	C38,C40
Choke, 150 µH, ± 5%, RFC-S-33	702500-126	5	L1,L2,L5-L7
Choke, 33 µH, ± 5%, DINK-33	702500-125	2	L3,L4
Connector, 34 pin, Amp 1-87230-7	706500-335	1	J1
Connector, 26 pin, Circuit Assembly Corp. CA-D26RSP100-230-090	706500-345	1	J2
Connector, 6 pin, Molex 22-12-2061	706500-295	2	J3,J4
Connector, 6 pin, Molex 09-88-2061	706500-347	1	J5
Connector, 10 pin, Amp 1-87233-0	706500-340	1	J6,J7

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-7. Printed Circuit Card Assembly: Slave Card, 114181-001 (Continued)

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Diode, FDH6666	704000-110	18	CR1-9,11,12, 14,15,19,20-23
Diode, 5.1V, Zener IN751A	704010-116	1	CR10
Diode, IN4003	704005-137	6	CR17,18,24-27
Diode, 3.6V, Zener IN747A	704010-126	1	CR28
I.C. Package 592	704520-145	2	Z1,Z2
I.C. Package 8T20	704610-172	1	Z3
I.C. Package 75462	704600-160	2	Z4,Z13
I.C. Package 96LS02	704621-004	3	Z5,Z15,Z18
I.C. Package 556	704520-134	2	Z6,Z8
I.C. Package, Resistor 10K	701900-007	1	Z7
I.C. Package, Q2T2905	704202-113	1	Z9
I.C. Package 7406	704600-111	1	Z10
I.C. Package 74LS74	704620-074	3	Z11,Z17,Z20
I.C. Package 74LS04	704620-004	1	Z12
I.C. Package 74LS00	704620-000	1	Z14
I.C. Package 74LS08	704620-008	1	Z16
I.C. Package 7404	704600-010	1	Z19
I.C. Package 74LS86	704620-086	1	Z21
I.C. Package 74LS02	704620-002	1	Z22
I.C. Package 74LS244	704620-244	1	Z23
I.C. Package 74LS373	704620-373	1	Z24
I.C. Package ULN20748	704900-111	1	Z25
I.C. Package UHP407	704900-110	1	Z26
I.C. Package 7905	704520-137	1	Z27
Resistor, 10K, 1/8W, ± 1%	701201-002	2	R1,R3
Resistor, 5.62K, 1/8W, ± 1%	701205-621	2	R2,R4
Resistor, 10 ohm, 1/4W, ± 5%	701003-100	2	R5,R7
Resistor, 150 ohm, 1/4W, ± 5%	701003-151	4	R6,13,32,33
Resistor, 221 ohm, 1/8W, + 1%	701202-210	3	R8,R9,R31
Resistor, 75 ohm, 1/4W, ± 5%	701003-750	3	R10,R11,R63
Resistor, 33K, 1/4W, ± 5%	701003-333	2	R14,R15
Resistor, 1.5K, 1/4W, ± 5%	701003-152	3	R16,R17,R23
Resistor, 2.2K, 1/4W, ± 5%	701003-222	5	R18,R49,R54, R55,R58
Resistor, 24K, 1/4W, ± 5%	701003-243	2	R19,R52
Resistor, 12.1K, 1/8W, ± 1%	701201-212	1	R20
Resistor, 866 ohm, 1/8W, ± 1%	701208-660	1	R21
Resistor, 1K, 1/4W, ± 5%	701003-102	5	R22,R37 R44,R45,R50
Resistor, 18K, 1/4W, ± 5%	701003-183	1	R24

NOTE: WHEN ORDERING SPARE PARTS, CONTACT REMEX SPARES ORDER DESK AND REFERENCE COMPLETE MODEL AND SERIAL NUMBER OF UNIT. ALWAYS REFER TO ADDENDUM AT THE REAR OF THE MANUAL (IF APPLICABLE) FOR POSSIBLE PART NUMBER CHANGES.

Table 7-7. Printed circuit Card Assembly: Slave Card, 114181-001 (Continued).

Description and Manufacturer's Part No.	REMEX Part No.	Quantity	Reference Designation
Resistor, 10K, 1/4W, ± 5%	701003-103	5	R25,R26,35,40, 64
Resistor, 1.33K, 1/8W, ± 1%	701201-331	2	R27,R29
Resistor, 1K, 1/8W, ± 1%	701201-001	2	R28,R30
Resistor, 43 ohm, 1/2W, ± 5%	701004-430	1	R34
Resistor, 1.8K, 1/4W, ± 5%	701003-182	1	R36
Resistor, 39K, 1/4W, ± 5%	701003-393	2	R38,R39
Resistor, 100 ohm, 1/4W, ± 5%	701003-101	4	R41-R43, R48
Resistor, 100 ohm, 2W, ± 1%	701050-101	1	R46
Resistor, 68 ohm, 2W, ± 1%	701050-102	1	R47
Resistor, 51K 1/4W, ± 5%	701003-510	1	R51
Resistor, 47K, 1/4W, ± 5%	701003-473	1	R53
Resistor, 5.1K, 1/4W, ± 5%	701003-512	2	R56,R57
Resistor, 3.3K, 1/4W, ± 5%	701003-332	4	R59-R62
Resistor, Variable 50K, Spectrol 64W503T000	701676-503	1	R12
Socket, Connector, Berg 65474-001	706510-314	5	AB,EF,GH,KL,NP, J-N, P, R
Terminal, Post, Amp 85931-6	706530-144	29	TP1-TP14,A-C,K, L,M,N,P,R
Transistor, 2N4401	704203-114	3	Q1-Q3

P.C. CARD CHANGE RECORD

CARD ASSY NO. 114181-001
SCHEMATIC NO. 114182-001

SCH REV	ASSY REV	FAB REV	DESCRIPTION OF CHANGE
C	D	D	Changed R56 and R57 from 8.2K to 5.1K, 1/4W, ± 5%, P/N 701003-512. Changed C38 and C40 from 39 pf to 22 pf, 300V, P/N 702123-220. Change P/N of C2 from 702181-104 to 702180-104. Changed Z27 from 79M05 to 7905, P/N 704520-137. Added connector P/N 706510-134 for N, P. Added Terminal post 706530-175 for N, P, and R. On sheet 6, an optional -5V or -6 to -12V input can be used at J5-1. A jumper table on sheet 6 shows the connections for jumpers N, P, and R depending upon the input at J5-1. On sheet 2, tied J3-5 to CT0* and J4-4 to CT1*.
D	E	D	On page 8-41/8-42, Figure 8-6, Sheet 3 of 6, Change R51 from 47K to 51K, 1/4W, ± 5%, P/N 701003-513. Also change Table 7-7, page 7-19.
D	E_1	D	No schematic or component changes.
E	E_2	D	On sheet 5 Z22-10 was connected directly to Z24-11. Z16 pins 4,5,6 and Z19; pin 12 and 13 were spares.
F	E_3	D	Changed R46 from 100 ohm, 2W, ± 5%, P/N 701014-101 to 100 ohm, 2W, ± 1%, P/N 701050-101. Changed R47 from 68 ohm, 2W, ± 5%, P/N 701014-680 to 68 ohm, 2W, ± 1%, P/N 701050-1,2. Change C26 from 100 µf, 25V, P/N 702641-107 to 47 µf, 25V, P/N 702641-476.
G	F	F	Updated fab revision by including previous change.
H	G	F	Changed Z-19 from 74LS14, P/N 704620-014, P/N 704600-110.
J	H	G	Changed terminal post A, B, C, K, L, M, N, P and R from 706530-170 to 706530-175.

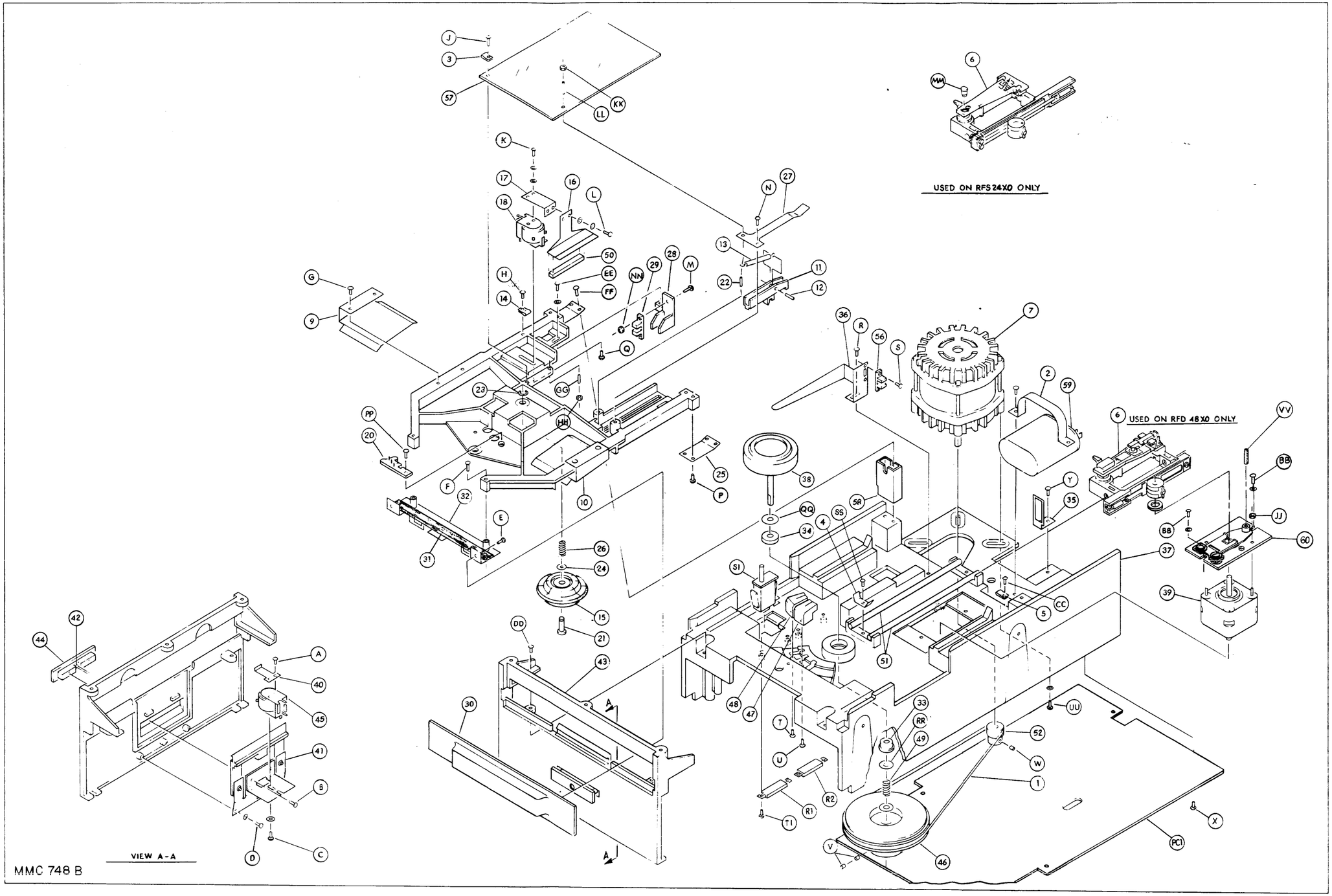


Figure 7-1. Exploded View of RFS48X0 and RFS24X0.

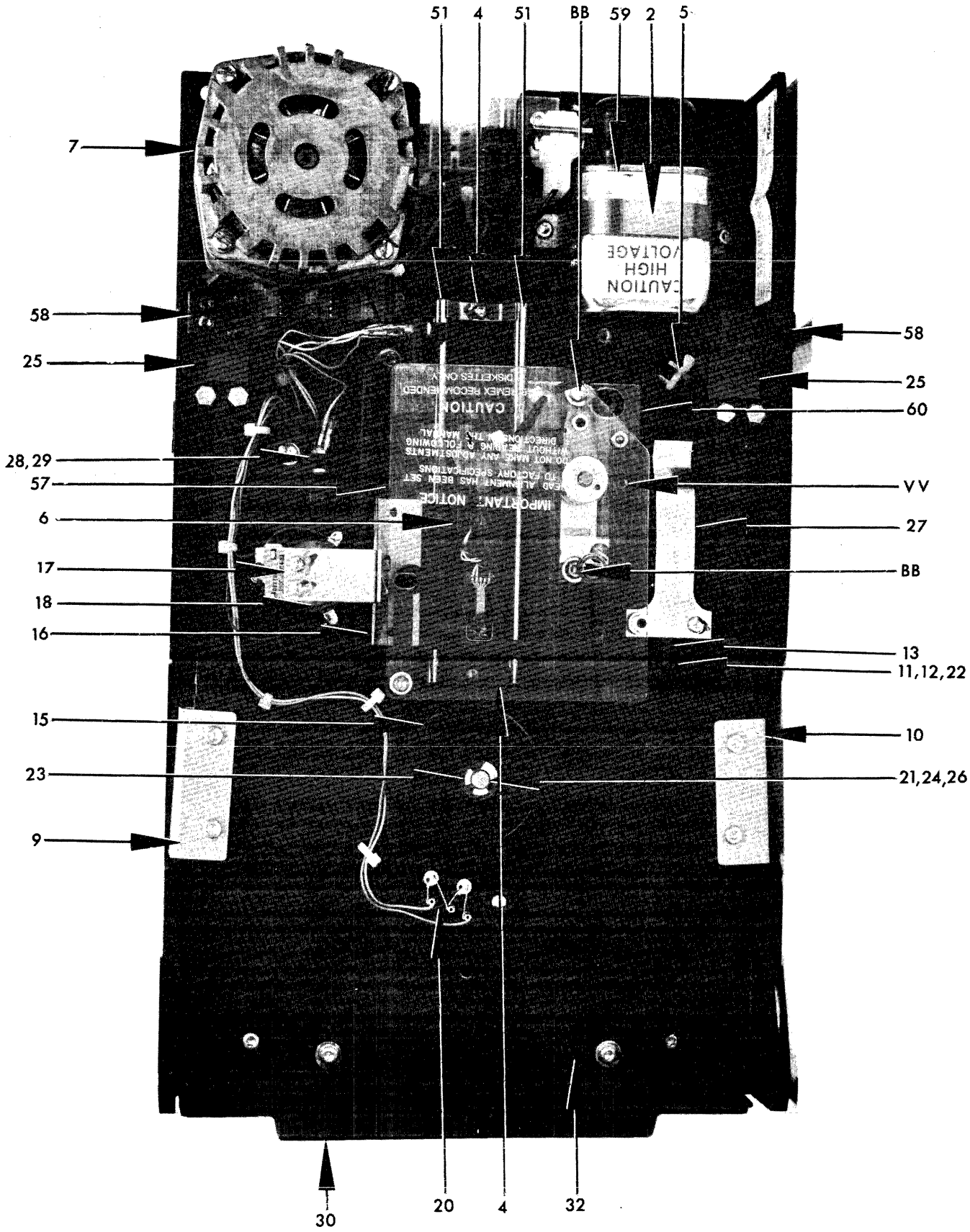


Figure 7-2. Top View, RFS4810/4820.

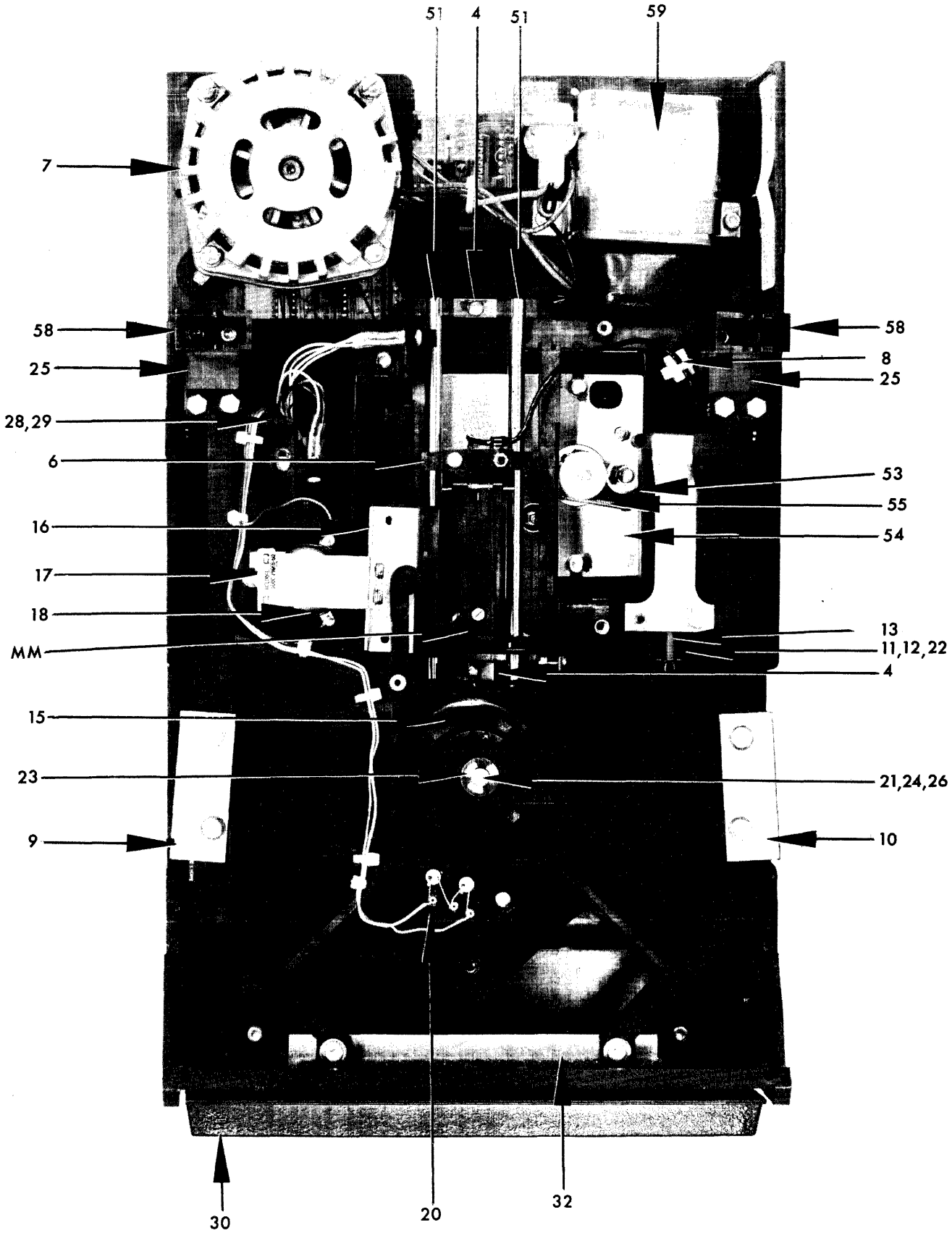


Figure 7-3. Top View, RFS2410/2420.

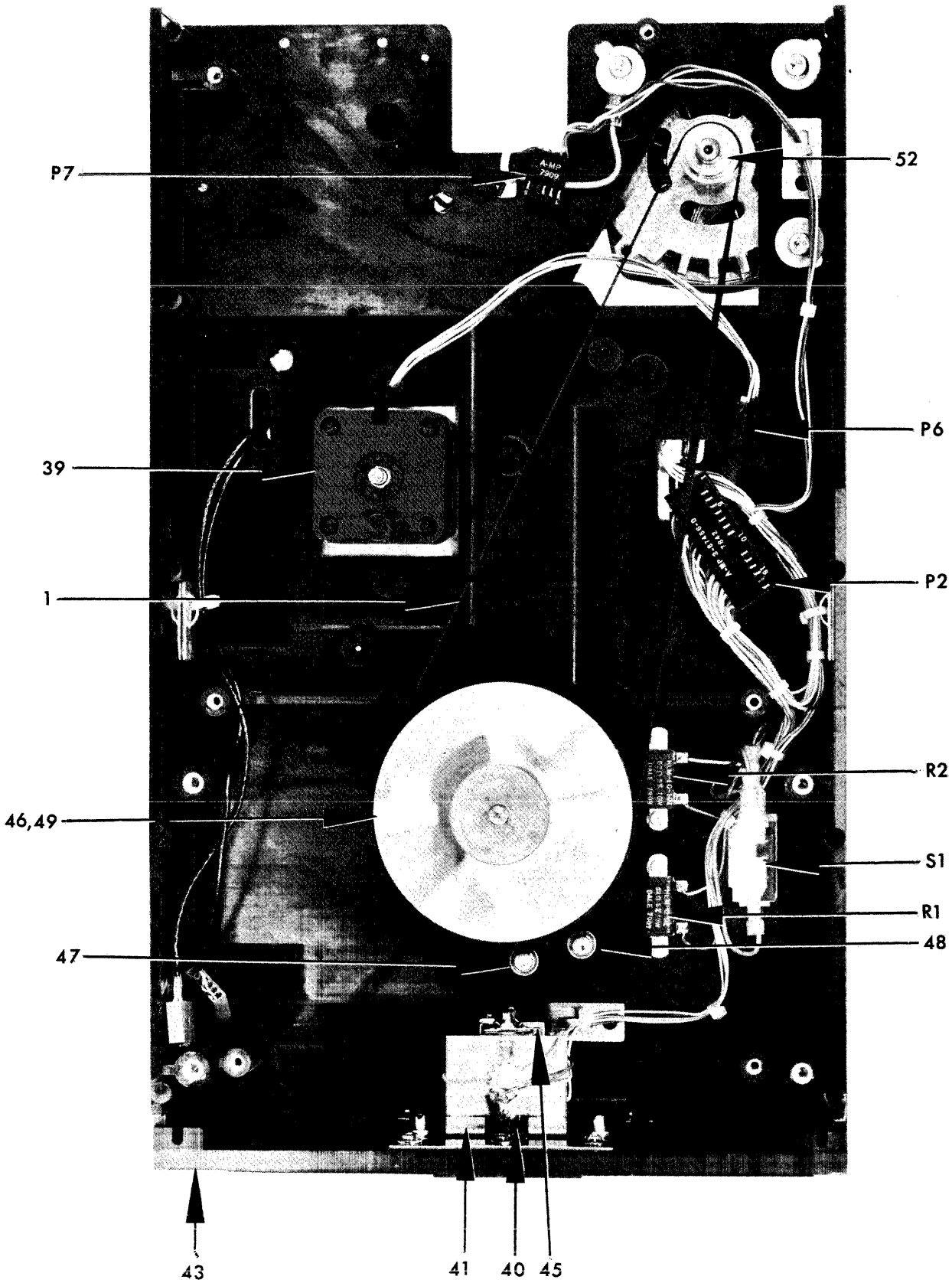


Figure 7-4. Bottom View with P.C. Card Removed.

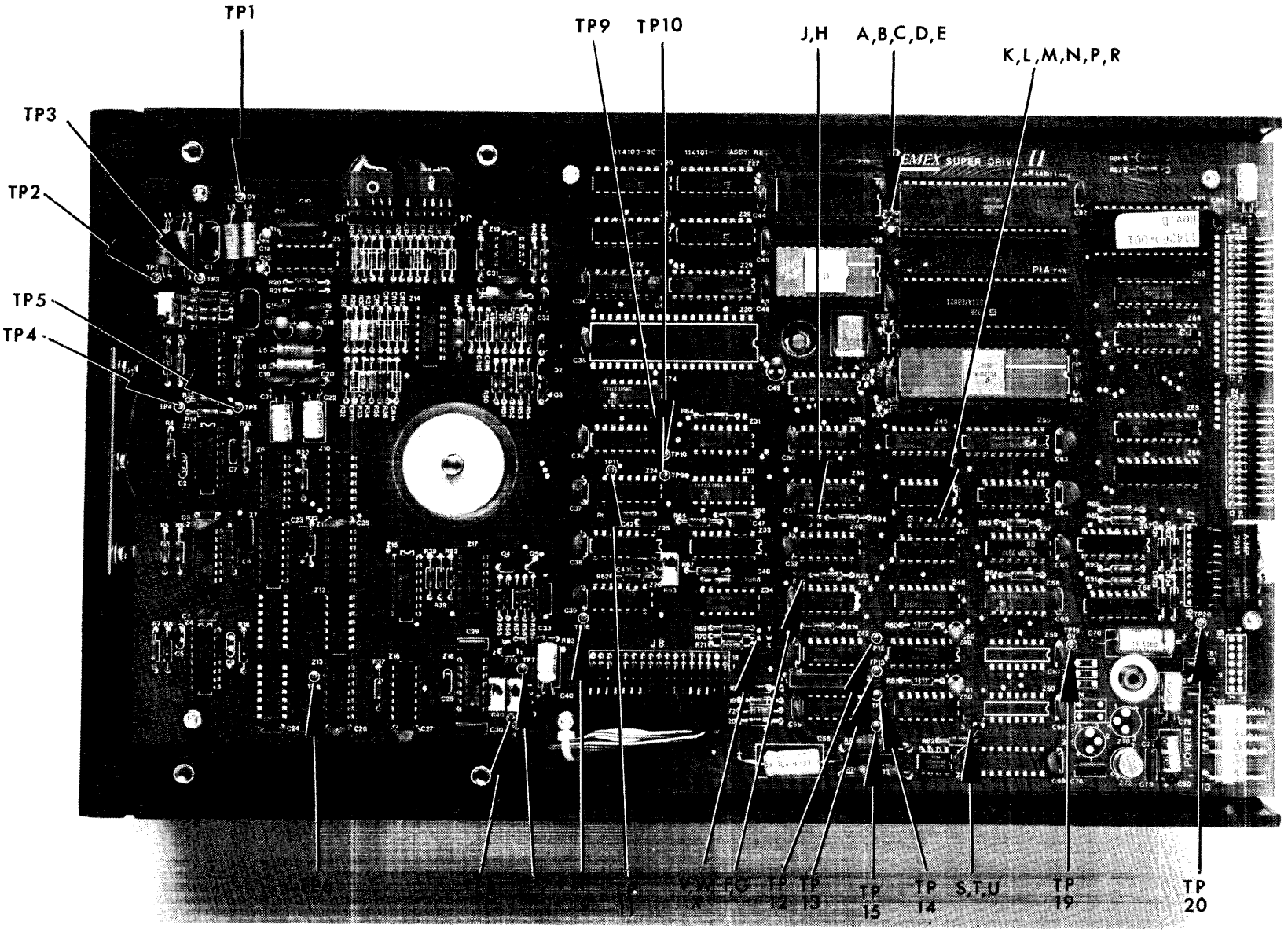


Figure 7-5. View of Master P.C. Card (RFS4810/2410).

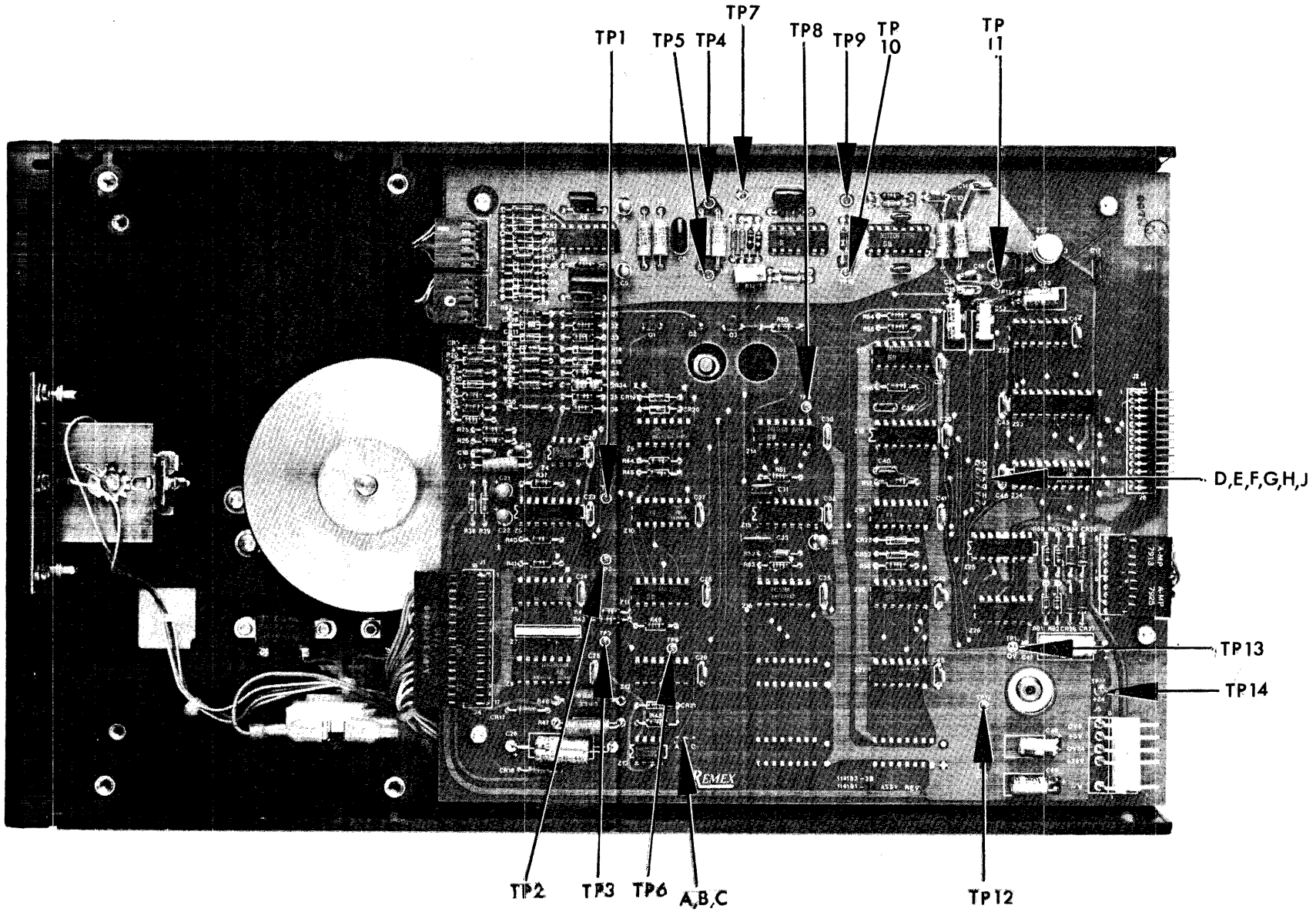


Figure 7-6. View of Slave P.C. Card (RFS4820/2420).

SECTION VIII

SCHEMATICS

8.1 GENERAL

The following schematics are represented in this section:

Figure 8-1, System Schematic RFS4810
Figure 8-2, System Schematic RFS4820
Figure 8-3, System Schematic RFS2410
Figure 8-4, System Schematic RFS2420
Figure 8-5, Schematic, Master Card Assembly 114101-001.
Figure 8-6, Schematic, Slave Card Assembly 114181-001.

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
A	—	5-23-78	RELEASED	A.D.	5-23-78	KY.
B	19154	7.7.80	ADDED EXT. WRT. PROTECT CONN	ESP	7.7.80	KY
C	19420	11.18.80	SEE ECO	S.E.O	11.18.80	KY

FLEXIBLE DISK DRIVE CARD ASSY -114101-001
SCHEM.-114102-001
P.C.ASSY-814235-*

J2

SSRDTA *	1	
STR00 *	2	
SIP *	3	
SWPRT *	4	
SWG	5	
STG43	6	
SWD	7	
SHOLD *	8	
SSTEP	9	
SDIR	10	
SSELO *	11	
SDRDY *	12	
SSELI *	13	
	14	
0V	↕	
	24	
KEY	25	
TPHD *	26	

J1

1	DATO *	
2	DAT 1 *	
3	DAT 2 *	
4	DAT 3 *	
5	DAT 4 *	
6	DAT 5 *	
7	DAT 6 *	
8	DAT 7 *	
9	BUSY *	
10	DTR *	
11	SPARE	
12	SPARE	
13	MRST *	
14	DDOUT *	
15	DTAK *	
16	ERROR *	
17	NC	
18	0V	
19	KEY	
20	0V	
↕		
34		

NOTES: UNLESS OTHERWISE SPECIFIED
1. REFERENCE ASSEMBLY DWG NO. 814235-*
2. SYMBOL * INDICATES LOW TRUE SIGNAL.
[3] J8 AC POWER CONNECTOR ON DRIVE AND NOT PART OF CARD J8.

FLEXIBLE DISK DRIVE CARD ASSEMBLY 114101-001
SCHEMATIC 114102-001
P.C. ASSY. 814235-*

P2 J8

INDEX Φ — RED, BLK, WHT
INDEX 1 — VIO, GRY, ORN
TRACK 00 — WHT/RED, WHT/YEL, WHT/ORN, WHT/BRN
WRITE PROTECT — RED, BRN, ORN, BLK
L.E.D. (IN USE) — GRN, YEL
HEAD LOAD SOLENOID — BLU, VIO
DOOR LOCK SOLENOID — WHT, GRY
DOOR OPEN SWITCH — S1, NC, NO, GRN, BRN, BLU
EXTERNAL WRITE PROTECT CONN. — +5V, GRY; EXT. WRT. PROTECT, BLU

RED	3	
BLK	7	
WHT	6	
VIO	8	
GRY	9	
ORN	20	
WHT/RED	5	
WHT/YEL	15	
WHT/ORN	14	
WHT/BRN	22	
RED	4	
BRN	16	
ORN	17	
BLK	21	
GRN	34	KEY
YEL	33	
BLU	31	
VIO	32	
WHT	30	KEY
GRY	29	
GRN	13	
BRN	28	
BLU	12	
GRY	19	KEY
BLU	1	

J6 P6 — M2 STEP MOTOR WINDINGS

BLU	5	
RED	3	PHASE 1
WHT	1	KEY
YEL	2	PHASE 2
	4	

J7 P7 — R1 62Ω 10W POWER RESISTOR; R2 62Ω 10W POWER RESISTOR

RED	2	
YEL	5	
ORN	4	KEY
BRN	3	
	1	

J5 P5 — HEAD 0

RED	6	
WHT	1	
YEL	2	
	4	KEY
BLK	3	
SHIELD	5	

J4 P4 — HEAD 1

RED	6	
WHT	1	
YEL	2	
	5	KEY
BLK	3	
SHIELD	4	

J3

1	-V	
2	KEY	
3	+24V	
4	0V24	
5	+5V	
6	0V5	

J8 [3]

A.C. POWER — 1, 2 GRN, 3 — AC MTR M1

DWG NO. 114292-001 REV. C

Figure 8-1. System Schematic, RFS4810. 112670-109C 8-3/8-4

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
A	—	5-23-7[illegible]	RELEASED	A.D.	5-23-7[illegible]	[illegible]
B	915[illegible]	7-[illegible]-8[illegible]	ADDED EXT. WRT. PROTECT CONN.	E.C.	7-7-80	[illegible]
C	1942[illegible]	5-28-80	SEE ECO	S.E.O.	11.18.80	[illegible]

FLEXIBLE DISK DRIVE CARD
ASSY 114181-001
SCHEM-114182-001
P/O ASSY-114236-*

J2

SSRDTA *	1
STR00 *	2
SIP *	3
SWPRT *	4
SWG	5
STG43	6
SWD	7
SHOLD *	8
SSTEP	9
SDIR	10
SSELO *	11
SDRDY *	12
SSELI *	13
0V	14 ↕ 24
KEY	25
TPHD *	26

FLEXIBLE DISK DRIVE CARD
ASSEMBLY 114181-001
SCHEMATIC 114182-001
P.O ASSY 814236-*

P2 J1

INDEX Φ — RED, BLK, WHT
INDEX 1 — VIO, GRY
ORN

TRACK 00 — WHT/RED, WHT/YEL, WHT/ORN, WHT/BRN

WRITE PROTECT — ORN, BRN, ORN, BLK

LED. (IN USE) — GRN, YEL

HEAD LOAD SOLENOID — BLU, VIO

DOOR LOCK SOLENOID — WHT, GRY

DOOR OPEN SWITCH — S1, NC, NO, GRN, BRN, BLU

EXTERNAL WRITE PROTECT CONN. — +5V (GRY), EXT. WRT. PROTECT (BLU)

KEY

J6 P6 — M2

5	BLU
3	RED
1	WHT
2	YEL
4	

KEY

PHASE 1
PHASE 2
STEP MOTOR WINDINGS

J7 P7

2	RED
	YEL
5	
4	ORN
3	
1	BRN

KEY

R1 62Ω 10W — POWER RESISTOR
R2 62Ω 10W — POWER RESISTOR

J3 P3

6	RED
1	WHT
2	YEL
4	
3	BLK
5	SHIELD

KEY

HEAD 0

J4 P4

6	RED
1	WHT
2	YEL
5	
3	BLK
4	SHIELD

KEY

HEAD 1

J5

1	-V
2	KEY
3	+24V
4	0V24
5	+5V
6	0V5

KEY

J8 [3]

A.C. POWER — 1, 2 GRN, 3 — AC MTR M1

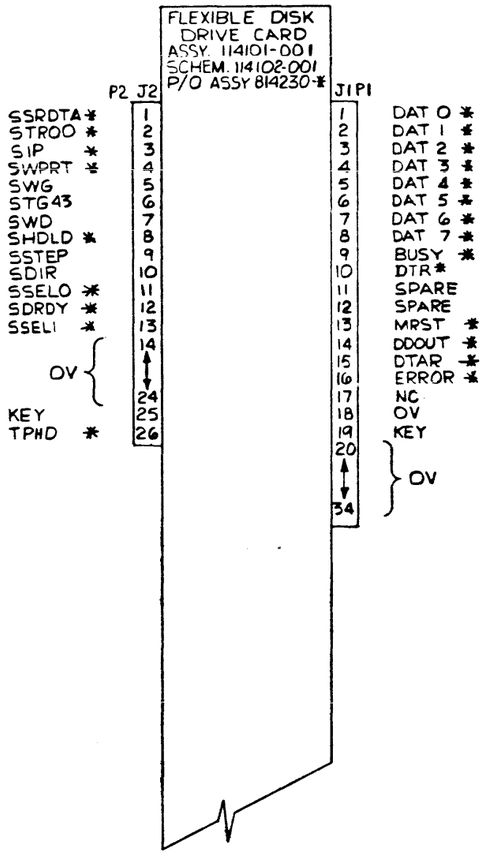
NOTE: UNLESS OTHERWISE SPECIFIED
1. REFERENCE ASSEMBLY DWG NO. 814236-*.
2. SYMBOL * INDICATES LOW TRUE SIGNAL.
[3] J8 AC POWER CONNECTOR ON DRIVE AND NOT PART OF CARD.

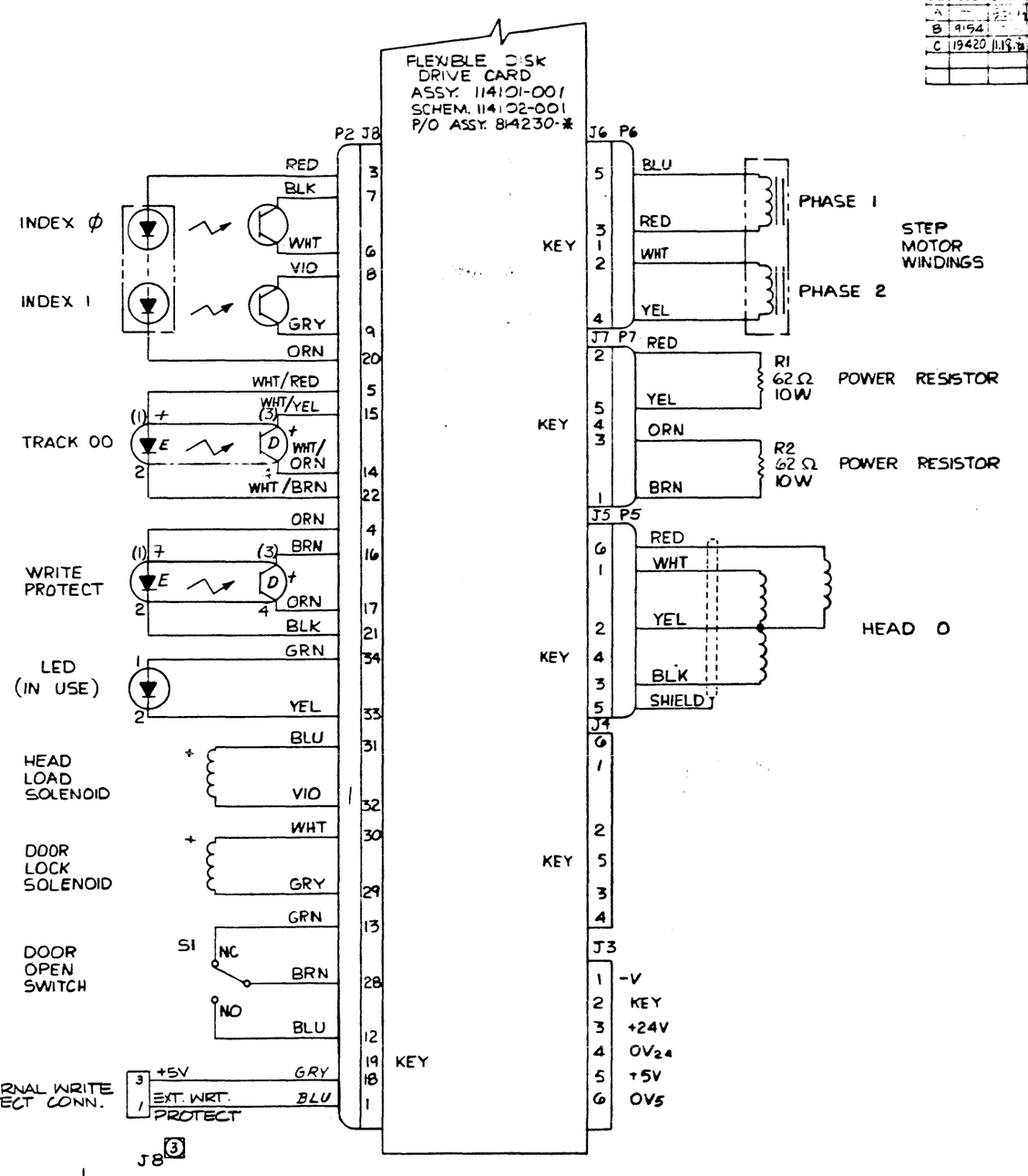
DWG NO. 114293-001 REV. C

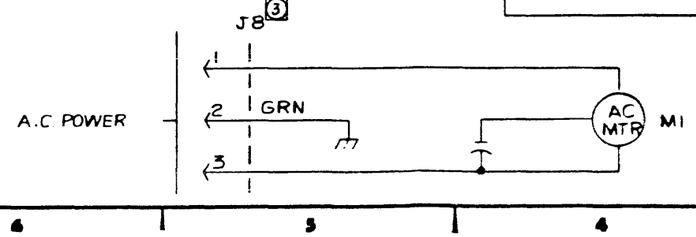
FORM NO. ED638/582

Figure 8-2. System Schematic, RFS4820. 112670-109C 8-5/8-6

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
A	—	—	RELEASED	D P		
B	9154	—	ADDED EXT WRT PROTECT CONN'S.			
C	19420	11.15.78	SEE ECO	S.E.O.	11.15.78	







NOTE: UNLESS OTHERWISE SPECIFIED

1. REFERENCE ASSEMBLY DWG. Nº 814230-*.
2. SYMBOL * INDICATES LOW TRUE SIGNAL.
3. J8 AC POWER CONNECTOR ON DRIVE AND NOT PART OF CARD J8.

DWG. No. 114294-001 REV. C

Figure 8-3. System Schematic, RFS2410. 112670-109C 8-7/8-8

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
A	—	6.23.74	RELEASED	C.P.	6.23.74	[illegible]
B	18154	7.7.76	ADDED EXT WRT PROTECT CONN.	[illegible]	7.7.76	[illegible]
C	19420	11.18.20	SEE ECO	S.E.C.	11.18.20	[illegible]

FLEXIBLE DISK DRIVE CARD
ASSY. 114181-001
SCHEM. 114182-001
P/O ASSY 84231-*

J2

SSRDTA *	1
STROO *	2
SIP *	3
SWPRT *	4
SWG	5
STG43	6
SWD	7
SHDLD *	8
SSTEP	9
SDIR	10
SSELO *	11
SDRDY *	12
SSELI *	13
OV	14 ↕ 24
KEY	25
TPHD *	26

FLEXIBLE DISK DRIVE CARD
ASSY. 114181-001
SCHEM. 114182-001
P/O ASSY 84231-*

P2 J1

INDEX φ: RED, BLK, WHT
INDEX 1: VIO, GRY, ORN
TRACK 00: WHT/RED, WHT/YEL, WHT/ORN, WHT/BRN
WRITE PROTECT: ORN, BRN, ORN, BLK
LED (IN USE): GRN, YEL
HEAD LOAD SOLENOID: BLU, VIO
DOOR LOCK SOLENOID: WHT, GRY
DOOR OPEN SWITCH: GRN, S1 NC, BRN, NO, BLU
EXTERNAL WRITE PROTECT CONN.: +5V GRY, EXT. WRT PROTECT BLU

RED	3
BLK	7
WHT	6
VIO	8
GRY	9
ORN	20
WHT/RED	5
WHT/YEL	15
WHT/ORN	14
WHT/BRN	22
ORN	4
BRN	16
ORN	17
BLK	21
GRN	34
YEL	33
BLU	31
VIO	32
WHT	30
GRY	29
GRN	13
BRN	28
BLU	12
GRY	19
BLU	18
	1

KEY

J6 P6

5	BLU
3	RED
1	WHT
2	WHT
4	YEL

PHASE 1, PHASE 2 — STEP MOTOR WINDINGS

J7 P7

2	RED
5	YEL
4	ORN
3	BRN
1	

R1 62Ω 10W POWER RESISTOR
R2 62Ω 10W POWER RESISTOR

J3 P3

6	RED
1	WHT
2	YEL
4	BLK
3	SHIELD
5	

HEAD 0

J4

6	
1	
2	
5	
3	
4	

J5

1	-V
2	KEY
3	+24V
4	OV_{24}
5	+5V
6	OV_5

J8 [3]

1	
2	GRN
3	

A.C. POWER — AC MTR — M1

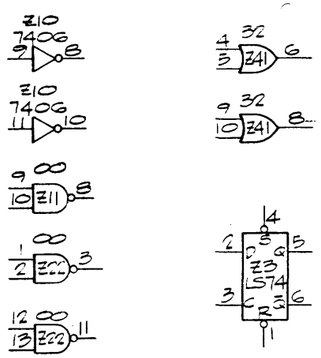
NOTE: UNLESS OTHERWISE SPECIFIED
1. REFERENCE ASSEMBLY DWG. Nº 814231-*
2. SYMBOL * INDICATES LOW TRUE SIGNAL.
[3] J8 AC POWER CONNECTOR ON DRIVE AND NOT PART OF CARD.

Figure 8-4. System Schematic, RFS2420.
112670-109C 8-9/8-10

DWG NO. 114295-001 REV. C

DESIGNATION	ALT USED	NOT USED
CAPACITOR	C88	-89
C-CORE	L8	
CRYSTAL	Y1	
DIODE	CR24	
RESISTOR	R97	
TRANSISTOR	Q5	
I.C. PACKAGE	Z74	

SPARES



REVISION STATUS CONT.			REVISION STATUS		
FAB	SCH	ASSY	FAB	SCH	ASSY
D	H	E_3	A	-	-
D	J	E_4	B	A	A
D	K	E_5	B	B	B
D	L	E_6	C	C	C
E	M	F	C	D	D
E	M'	F_1	D	E	E
E	N	F_2	D	F	E_1
P	P	G	D	G	E_2

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
-	[illegible]	[illegible]	RELEASED [illegible]	[illegible]	[illegible]	[illegible]
-	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
-	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
D	[illegible]	[illegible]	SEE ECO	REK	[illegible]	[illegible]
E	[illegible]	[illegible]	SEE ECO	[illegible]	[illegible]	[illegible]
F	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
G	19117	6-11-80	[illegible]	[illegible]	[illegible]	[illegible]
H	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
J	19280	6-24-80	[illegible]	[illegible]	[illegible]	[illegible]
K	19321	9-20-80	CHANGED VALUES OF C22, A55, 56, 58, 59	S.E.O.	9-20-80	[illegible]
L	19374	10-3-80	SHEET 8: Z34 QB, QC CONN	S.E.O.	10-3-80	[illegible]
M	9317	11-3-80	REVISED PER ECO	S.E.O.	11-3-80	[illegible]
M'	T/C	11-14-80	CORRECTE DRV STATUS-'E' FAB HAS 'D' FAB	D.G.M.	11-14-80	[illegible]

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
N	19473	1-15-81	[illegible]	[illegible]	[illegible]	[illegible]
P	19701		ADDED TEST JUMPER DD-EE ON SH 6	[illegible]	[illegible]	[illegible]

NOTE: (CONTINUED)

	+5V	0V
38. Z4, 7, 25, 33, 49 (9LS02) 704621-004	16	8
39. Z63 IS (8304) 704621-001	20	10
40. Z53 IS (68B21) 704810-123.	20	1
41. Z54 IS (FD179-02) 704810-141 PIN 40 IS +12V.	21	20
42. Z20, 21, 27, 28 ARE (2114 (300ns)) 704810-130.	18	9
43. Z52 IS (68B00) 704810-132.	8	1 & 21
44. Z37 IS (6875) 704810-133.	16	8
45. Z30 IS (INS8250) 704810-134.	40	20
46. Z68 IS (UHP407) 704900-110.	14	7
47. Z67 IS (ULN 2074B) 704900-111.		
48. CR1-13, 15, 16, 19 ARE (FDH6666) 704000-110.		
49. CR18, 20-24 ARE (IN4003) 704005-137.		
50. CR14 IS (IN751A) 5.1V ZENER 704010-116.		
51. CR17 IS (IN747A) 3.6V ZENER 704010-126.		
52. Q1, 2, 3, 5 ARE NPN (2N4401) 704203-114.		
53. Q4 IS PNP (2N4403) 704201-108.		
(F4) 54. Z36 IS (PROM) 114259-001 (PRGM'D 2532) FOR STANDARD CONFIGURATION. FOR ALTERNATE PROM CONFIGURATION SEE TABLE, SHEET 7.	24	12
55. Z62 IS 114260-001. (PRGM'D 82S103)	28	14
56. UNUSED DESIGNATIONS ARE: TP17 AND TP18.		
57. Y1 IS 703800-111 CRYSTAL, 8MHZ.		

NOTE: UNLESS OTHERWISE SPECIFIED—

1. REFERENCE DRAWING- ASSY 114101-*.
2. SIGNAL ADDRESS IS AS FOLLOWS: SHEET NUMBER-HORIZONTAL ZONE-VERTICAL ZONE.
3. AN ASTERISK FOLLOWING SIGNAL NOMENCLATURE INDICATES A LOW (0V) TRUE.
4. RESISTORS ARE IN OHMS 1/4W ±5%.

	+5V	0V
		1
5. Z43 IS 701900-007.		
6. Z14 IS (Q2T2905) 704202-113.	-	-
7. Z42, 44 ARE (556) 704520-134.	14	7
8. Z69 IS (78L12) 704520-144.	-	-
9. Z1, 5 ARE (592) 704520-145. PIN 5 IS -5V.	10	-
10. Z72 IS (7905) 704520-137.	-	-
11. Z71 IS (78M08) 704520-140.	-	-
12. Z70 IS (79M08) 704520-152.	-	-
13. Z73 IS (78L05) 704520-139.	-	-
14. Z10 IS (7406) 704600-111.	14	7
15. Z19, 51 ARE (75462) 704600-160.	8	4
16. Z2 IS (8T20) 704610-172.	14	7
17. Z60 IS (75188) 704610-174. PIN 1 IS -8V. PIN 4 IS +8V.	-	7
18. Z59 IS (75189) 704610-175.	14	7
19. Z11, 13, 22, 26, 38, 40 ARE (74LS00) 704620-000.	14	7
20. Z17 IS (74LS02) 704620-002.	14	7
21. Z39, 50 ARE (74LS04) 704620-004.	14	7
22. Z48 IS (74LS132) 704620-132.	14	7
23. Z31 IS (74LS10) 704620-010.	14	7
24. Z41, 46 ARE (74LS32) 704620-032.	14	7
25. Z47 IS (74LS54) 704620-054.	14	7
26. Z3, 6, 16, 32, 58, 74 ARE (74LS74) 704620-074.	14	7
27. Z57 IS (74LS86) 704620-086.	14	7
28. Z15 IS (74LS145) 704620-145.	16	8
29. Z23 IS (74LS151) 704620-151.	16	8
30. Z24, 45 (74LS164) 704620-164.	14	7
31. Z64 IS (74LS240) 704620-240.	20	10
32. Z55 IS (74LS244) 704620-244.	20	10
33. Z29 IS (74LS273) 704620-273.	20	10
34. Z12, 34 ARE (74LS293) 704620-293.	14	7
35. Z18 IS (74LS624) 704620-624.	14	7
36. Z56 IS (74LS368) 704620-368. PIN 1 & 15 ARE 0V.	16	8
37. Z65, 66 ARE (74LS373) 704620-373.	20	10

DWG NO. 114102-001 REV P

Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 1 of 12 8-11/8-12

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1			

SIGNAL INDEX

SIGNAL	DEFINITION	SOURCE	LOCATION
A0	ADDRESS BIT 0 (FD CHIP)	6D6	8B6
A1	ADDRESS BIT 1 (FD CHIP)	6D6	8B6
AB00	MPU ADDRESS BIT 00	6A1	7E8 13E8
AB01	01		13E8
AB02	02		13E8
AB03	03		
AB04	04		
AB05	05		
AB06	06		
AB07	07		
AB08	08		
AB09	09		
AB10	10		
AB11	MPU ADDRESS BIT 11	6A1	7E8 13E8
BØ2	BUFFERED Ø2	6D1	6B7
B EARLY	BUFFERED EARLY	11C5	11D4
B LATE	BUFFERED LATE	11B5	11D4
CLATCH*	CONTROL LATCH	6C1	9C8
CSACE*	ASYNCHRONOUS COMMUNICATION ELEMENT CHIP SELECT	6C1	13D7
CSFDC*	FD CHIP SELECT	9C4	6B6 8B5 8C6
CSRAMH*	RAM (HIGH) CHIP SELECT	6B1	7E6
CSRAML*	RAM (LOW) CHIP SELECT	6C1	7E6
CSROMH*	ROM (HIGH) CHIP SELECT	6C1	6D3 7D6
CSROML*	ROM (LOW) CHIP SELECT	6C1	6D3 7D8
CT0*	CENTER TAP 0	3B1	3C8
CT1*	CENTER TAP 1	3B1	3B8
DAL0*	DATA LINE BIT 0	6C8	8D4
DAL1*	1		
DAL2*	2		
DAL3*	3		
DAL4*	4		
DAL5*	5		
DAL6*	6		
DAL7*	DATA LINE BIT 7	6C8	8D4
DB00	MPU DATA BIT 00	6E8	7B8 13D8 9D8
DB01	01		
DB02	02		
DB03	03		
DB04	04		
DB05	05		
DB06	06		
DB07	MPU DATA BIT 07	6E8	7B8 13D8 9D8
DENSW	DENSITY SWITCH	9C7	8D1
DDEN*	DOUBLE DENSITY ENABLE	8D1	6D6 8B6 10D8
DDOUT	DATA DIRECTION	9C4	6D7 8D7
DIR	DIRECTION (STEP)	8C4	9D4 9D5
DRDY	DRIVE READY	12D3	6B6 8C6
DTAK	DATA TRANSFER ACKNOWLEDGE	6D7	9B7
DTAKST	DATA TRANSFER ACKNOWLEDGE STROBE	9B4	6C7
DTR	DATA TRANSFER REQUEST	6D7	9B3
EARLY	WRITE EARLY DATA	8D5	11B6

SIGNAL	DEFINITION	SOURCE	LOCATION
ERASE 0	ERASE HEAD 0	4B2	3D8
ERASE 1	ERASE HEAD 1	4A2	3C8
FDCMR*	FLOPPY DISK CHIP MASTER RESET	6D7	8B8
FDWD	FLOPPY DISK WRITE DATA	11D3	3C3 3D3 4C7 9D4
FDRQ	FD CHIP DATA TRANSFER REQUEST	8C4	9C7
HDLD*	HEAD LOAD	6B6	9D5 9D4
HOST*	ENABLE HOST / DRIVE COMMUNICATION	9C4	6D7 8D7
INT	INTERRUPT	8B3	6C7
IP*	INDEX PULSE	9E5	8C4 8C6
LATE	WRITE LATE DATA	8D5	11B5
MDIR	STEP DIRECTION (MASTER)	9D4	5E8
MHDLD*	MASTER DRIVE HEAD LOAD	9D4	12C3
MIP*	MASTER DRIVE INDEX PULSE	12B3	9E4
MR	MASTER RESET	6D7	6E2
MSEL	MASTER SELECT	9E4	12D5
MSEL*	MASTER SELECT	9E4	12D5
MSRDTA*	MASTER DRIVE SERIAL DATA	3C1	9E4
MSTEP	MASTER DRIVE 'STEP'	9D4	5E8
MTG43	MASTER DRIVE TRACK GREATER THAN 43	9D4	4D7
MTR00*	MASTER DRIVE TRACK 0 STATUS	12E6	9E4
MWG	MASTER DRIVE WRITE GATE	9D4	3C4 4E7
MWPRT*	MASTER DRIVE WRITE PROTECT	12D6	9E4
PCE	PRECOMPENSATION ENABLE	9D7	11D4
PH0	MOTOR PHASE ZERO	5A3	12E7
POR	POWER ON RESET	6D1	13B7
POR*	POWER ON RESET	6D1	4B5 5D7 6D5 6D7 9C7 9D6 8B8

SIGNAL	DEFINITION	SOURCE	LOCATION
RCLK	READ CLOCK	10B2	8C6
RE*	READ ENABLE (FD CHIP)	9A4	8C6
R/$\overline{W}$	READ/WRITE	6A1	7E6 13B7 (2 PLC'S)
RWSTB	READ WRITE STROBE	6C7	9B7
SDRDY	SLAVE DRIVE READY	9C4	12D5
SRDTA*	SERIAL DATA	9E5	8C6 10D4
STEP	STEP MOTOR HIGH VOLTAGE	8C4	9D4 9D5
TG43	TRACK GREATER THAN 43	8B5	9D4 9D5
TPHD	TOP HEAD	9D7	3B3
TPHD*	TOP HEAD	9D6	8D4 12D5 12C4
TR00*	TRACK 00 STATUS	9E5	8C6 8D4
WC −	WRITE CURRENT	4C2	3D8
WC +	WRITE CURRENT	4C2	3D8
WD	WRITE DATA	8B5	11C8 11B6
WE*	WRITE ENABLE (FD CHIP)	9A4	8C6
WG	WRITE GATE	8B5	9D4 9D5
WPRT*	WRITE PROTECT	9E5	8C6
WSEL	WRITE SELECT	6C7	9A7
2 MHZ	2 MHZ CLOCK	6D1	13E5 8B5
8 MHZ	8 MHZ CLOCK	6E3	9B4

DWG No. 114102-001 REV P

Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 2 of 12 8-13/8-14

FORM NO. ED0.902

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
			SEE SHEET 1			

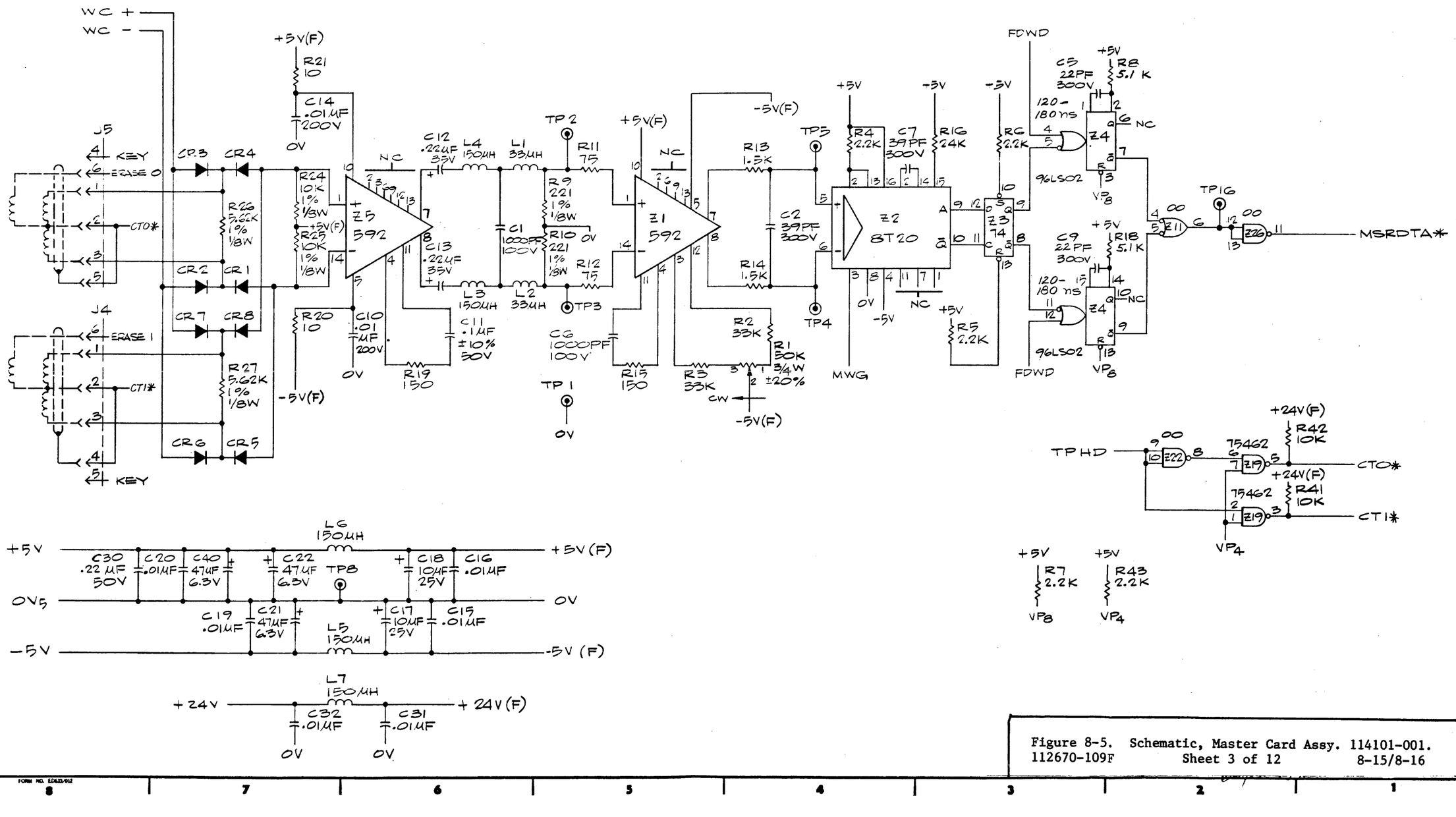


Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 3 of 12 8-15/8-16

DWG NO. 114102-001 REV P

FORM NO. ED633/012

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1			

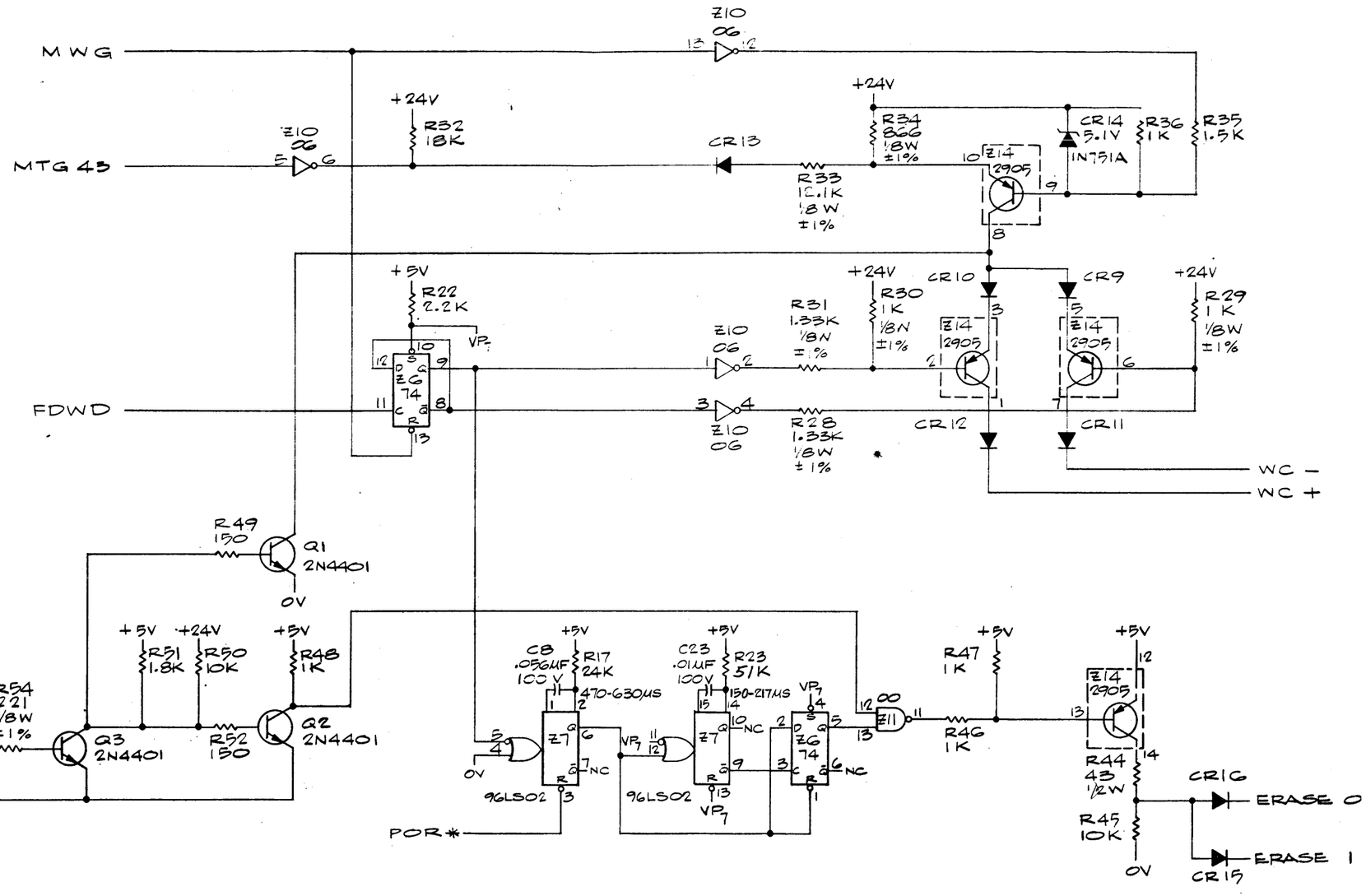


Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 4 of 12 8-17/8-18

DWG No. 114102-001 REV. P

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APP'D
			SEE SHEET 1			

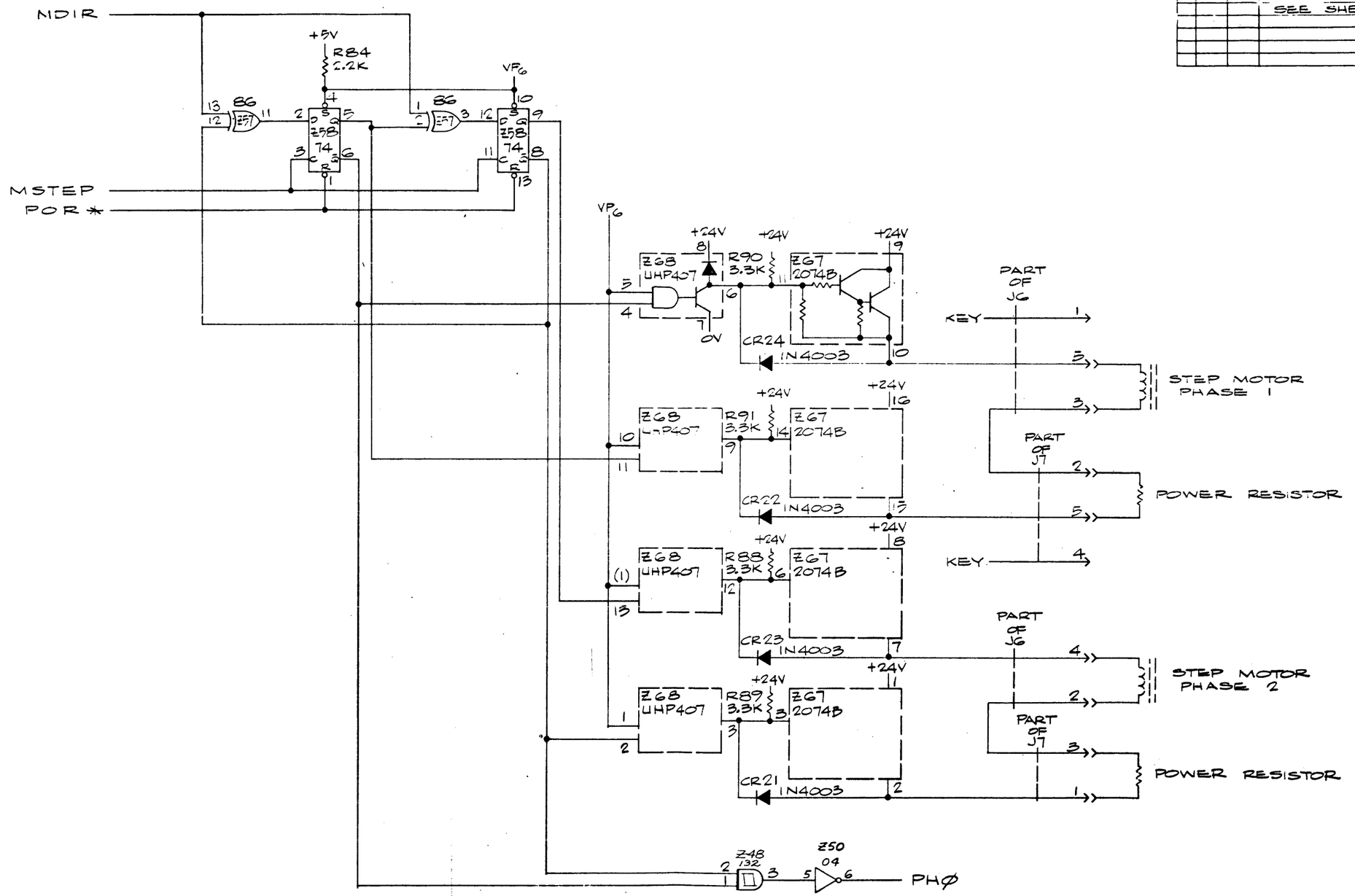


Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 5 of 12 8-19/8-20

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1.			

7800-C7 MPU DATA BUS

PART OF J1

Z64 240

HOST*

KEY NC

Z53 68B21

Z52 68B00

Z62 (825103)

DATA LINE BUS

DAL 0 * — DAL 7 *

CIRCUIT INTERUPT JUMPER FOR TEST

VP2 VP1 VP3

MPU READ/WRITE — R/W

MPU ADDRESS BUS — AB00-AB11

PIACS

POR *

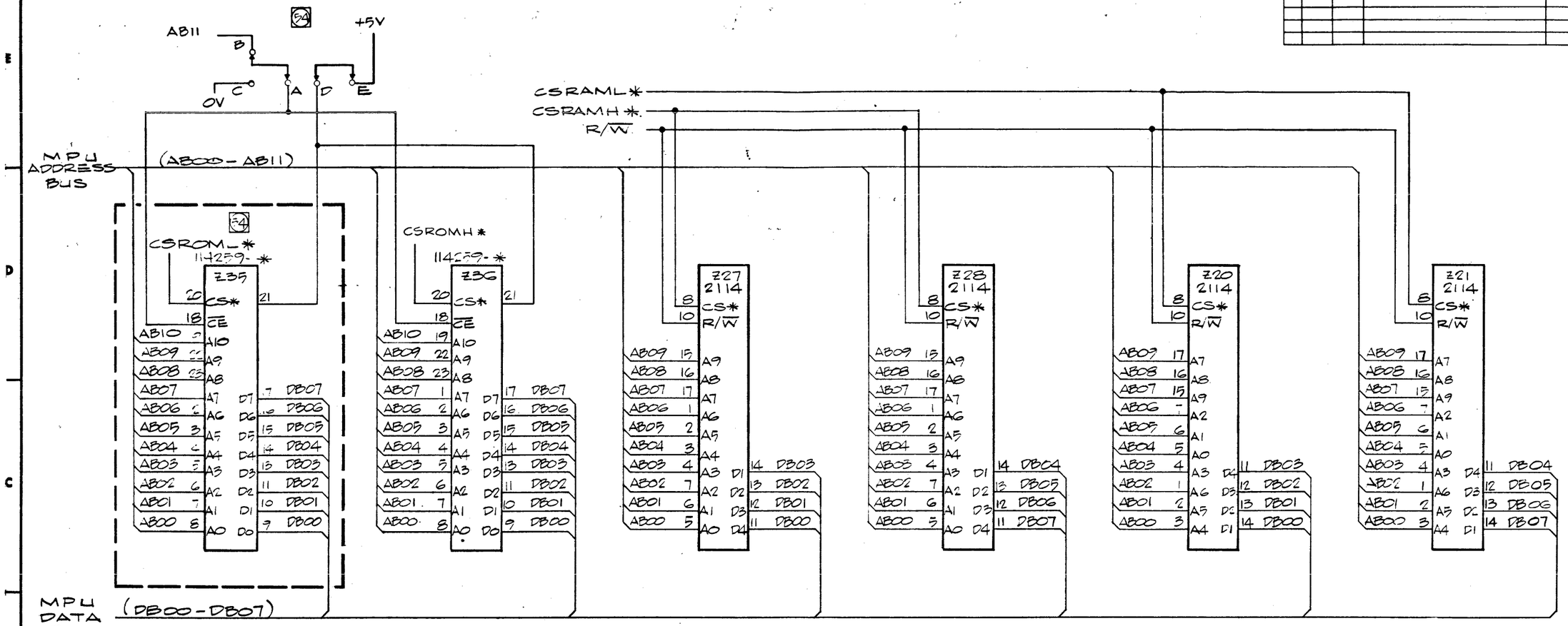
POR 2 MHZ BØ2

CSRAML *
CSACE *
CLATCH *
CSROMH *
CSROML *
CSRAMH *

Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 6 of 12 8-21/8-22

DWG NO. 114102-001 REV P

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
			SEE SHEET 1			



STANDARD -001 ASSEMBLY CONFIGURATION IS SHOWN.
FOR STANDARD AND ALTERNATE CONFIGURATIONS
SEE TABLE:

(54)	ASSY DASH NO.	PROM REQUIRED Z35	PROM REQUIRED Z36	JUMPER CONFIGURATION C	A	B	D	E
STANDARD	-001 ASSY	NONE	(2532) 114259-001		●	●	●	●
ALTERNATE 1	-001 ASSY	NONE	(2732) 114259-002	●	●	●	●	
ALTERNATE 2	-001 ASSY	(2516 OR 2716) 114259-003	(2516 OR 2716) 114259-004	●	●		●	●

Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 7 of 12 8-23/8-24

SYM	ECO	EFFECT.	REVISIONS	BY	DATE	APP'D
			SEE SHEET 1			

SIDE 0 TRACK 0 DENSITY	JUMPER G	F	Z
SINGLE DENSITY	•	•	
SAME AS TRK 1 THRU 76		•	•

DENSITY FORMAT	JUMPER H	J	Y
SINGLE	•	•	
DOUBLE		•	•

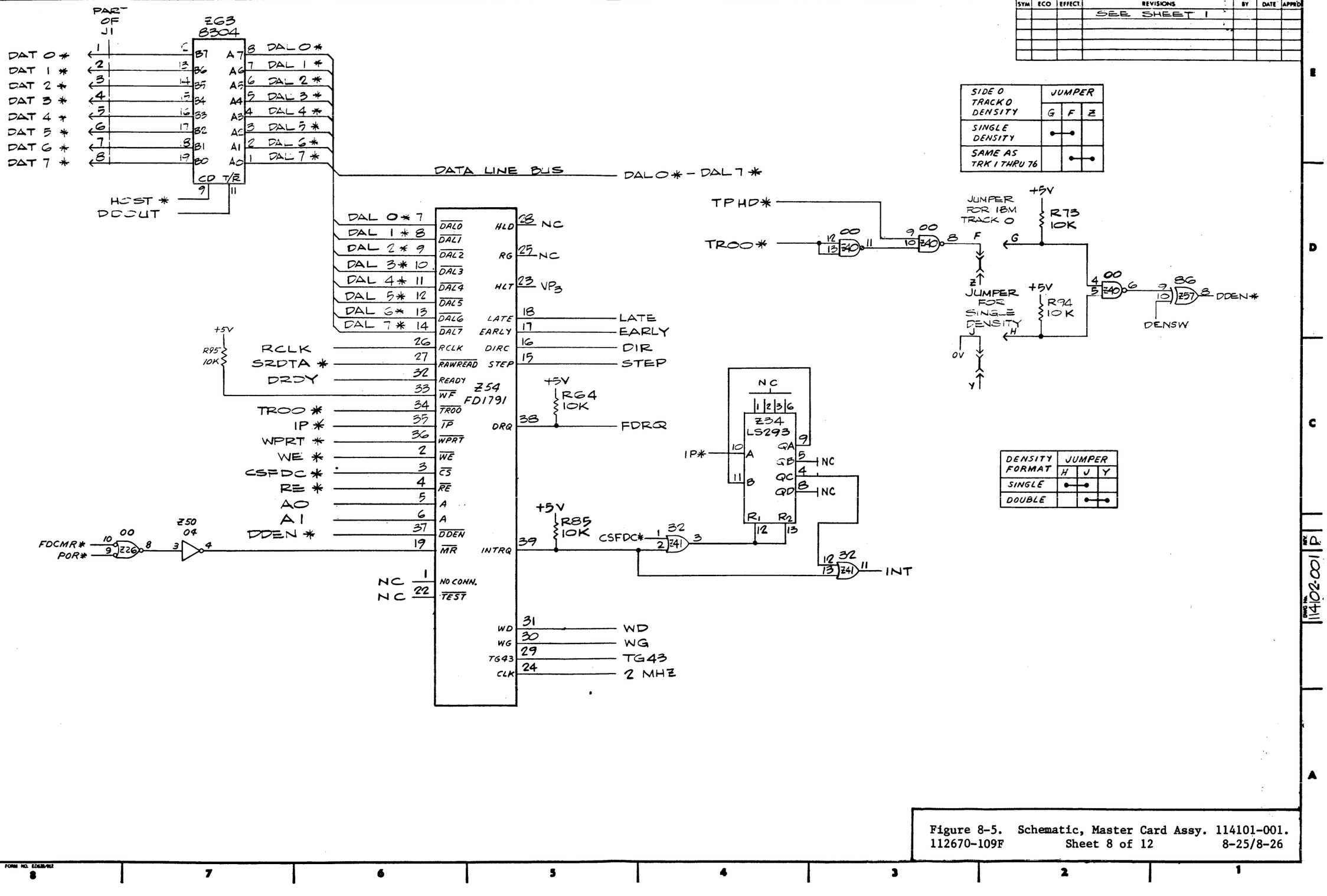


Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 8 of 12 8-25/8-26

SYM	ECO	EFFECT.	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1			

UNIT SELECT	JUMPER					
	C	D	N	M	L	K
0	•	•		•	•	
1		•	•	•	•	
2	•	•			•	•
3		•	•		•	•

Z55 244
SRDTA *
TROO *
IP *
WPRT *
WPRT *
IP *
TROO *
SRDTA *
MSRDTA *
MTROO *
MIP *
MWPRT *
MSEL *
MSEL

J2
SWPRT *
SIP *
STROO *
SSRDTA *

Z66 373
WG
TG43
NC
HDLD *
NC
NC
DIR
STEP
MWG
MTG43
NC
MHDLD *
NC
NC
MDIR
MSTEP

Z65 373
WG
TG43
FDWD
HDLD *
NC
NC
DIR
STEP
SWG
STG43
SWD
SHDLD *
NC
NC
SDIR
SSTEP

32 Z46
Z56 368
Z48 132
Z48 132
POR *
PCE
R
P
N
M
L
K
OV
OV1

MPU DATA BUS (DB00 - DB07)
Z29 273
DB07
DB06
DB05
DB04
DB03
DB02
DB01
DB00
CLATCH *
POR *
TPHD
TPHD *
DENSW
DDOUT
CSFDC *
HOST *
FDRQ
DTAK
RWSTB
WSEL
SSEL 1 *
SSEL 0 *
SDRDY *
DTAKST
RE *
WE *
KEY
14-24
OV

Z56 368
Z56 368
Z56 368
Z56 368
Z56 368
Z39 04
Z39 04
Z39 04
Z39 04
Z39 04
Z31 10
Z32 74
Z33 96LS02
C47 100PF 200V
+5V
R66 10K
460-500nS
VP2
VP1
VP3
NC
00
240
32
238
R83 1K
Z49 164
QA
QB
QC
QD
QE
QF
QG
QH
A
B
CLK
CLR
8MHZ
DTR

Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 9 of 12 8-27/8-28

DWG NO. 114102-001 REV P

FORM NO. EDM8/82

SYM	ECO	EFFECT.	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1			

DDEN *

Z11 00

+5VR

R40 10K 3/4 W ±20%

C28 200pf 3KV

TP6

TP7

Z18 624

4MHZ (NOM)

NC

0V

+5VR

R60 50K 3/4 W ±20%

CW

0V

Z13 00

Z16 74

NC

Z12 293

NC

Z15 145

SRDTA *

+5V

R39 1K

R38 1K

NC

Z17 02

-5V

R92 1K

R55 240Ω

Q4 4403

R57 ±Ω

Q5 4401

0V

R59 82Ω

R58 240Ω

C33 .22uF 50V

R56 27Ω

0V

VP5

Z16 74

NC

TP22

RCLK

Z13 00

Z17 02

+5V

R37 2.2K

VP5

+24V

R93 1K

Z73 78L05

C29 .22MF 50V

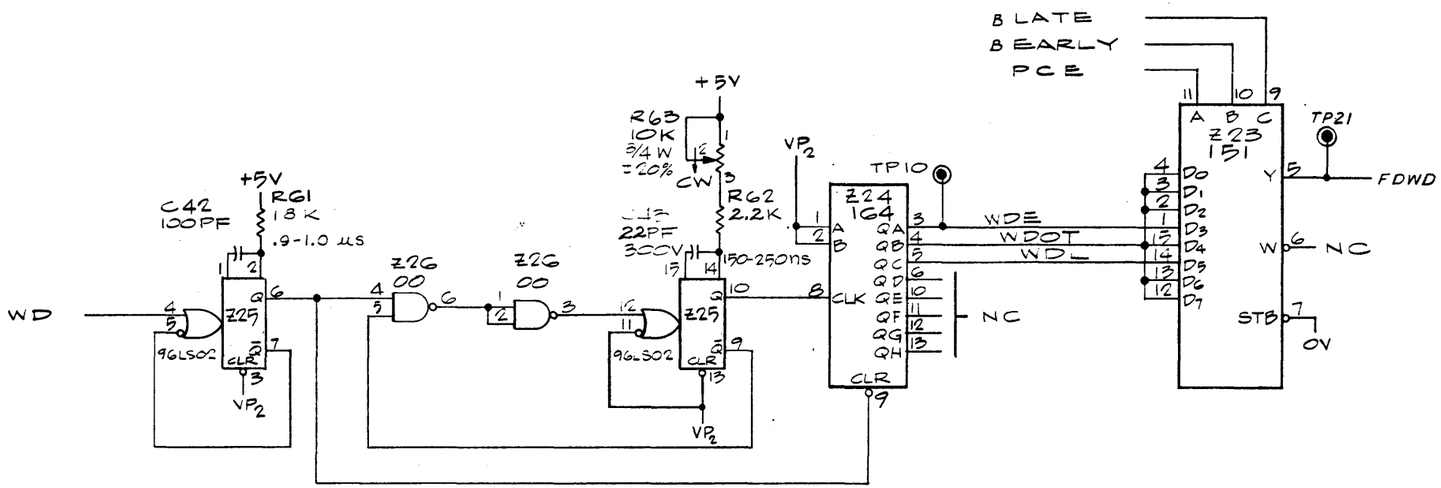
+5VR

0V

Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 10 of 12 8-29/8-30

DWG NO. 114102-001 REV P

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1			



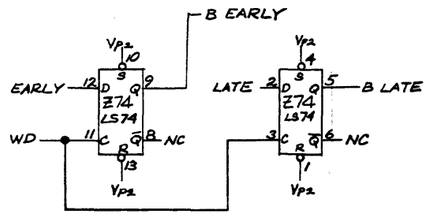


Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 11 of 12 8-31/8-32

DWG No. 114102001 REV P

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1			

PART OF J8

TR00 SW

+5V

R71 100

EXTERNAL WRITE PROTECT

WRITE PROTECT SENSOR

R70 100

LED

SINGLE SIDED INDEX

R69 100

LED

DOUBLE SIDED INDEX

PH∅

Z50 04

MTR00*

TP15

Z44 556

Z43 10K

NC

TP14

MWPRT*

Z42 556

TP13

TP12

R74 10K

Z48 132

Z57

MIP*

AA BB CC

U3

-V

Z72 7905

C80 10µF 25V

C78 .22µF 50V

C76 .22µF 50V

KEY

+24V

Z69 78L12

C70 10µF 50V

C82 .22µF 50V

C81 .22µF 50V

+12V

OV24

TP20

+5V

C79 47µF 6.3V

C84 47µF 6.3V

C77 .22µF 50V

.01µF

C34, 24-27, 34-39, 41, 44-46, 50-55, 57-59, 62-68, 83.

TP19

OV5

SINGLE/DOUBLE HEAD ENABLE	JUMPER V	W	X
RFS 4810	●	●	
RFS 2410		●	●

-V	JUMPER AA	BB	CC
-5V		●	●
-6V TO -12V	●	●	

Z47 74LS54

SDRDY

MSEL*

NC

MSEL

TPHD*

NC

CG1 15 µF 15V

R81 39K

96LS02

Z49

180-200ms

CG0 15 µF 15V

R80 39K

TPHD*

U V W X

Z50 04

MHDLD*

Z56 368

DRDY

PART OF J8

NC

+5V

R82 1K

DOOR NOT CLOSED

75462

CR18 IN4003

+24V

DOOR LOCK SOLENOID

DOOR LOCK SOLENOID	JUMPER CONFIGURATION J	T	S
ENABLE	●		
DISABLE		●	

S

75462

CR19

R72 100

+5V

+ LED

- LED

+24V

C56 47µF 25V ±20%

CR20 IN4003

HEAD LOAD SOLENOID

R76 100±1% 2W

R75 68±1% 2W

KEY

OV

DWG No. 114102-001 REV P

FORM NO. ED633/812

Figure 8-5. Schematic, Master Card Assy. 114101-001.
112670-109F Sheet 12 of 12 8-33/8-34

DESIGNATION	LAST USED
CAPACITOR	C54
DIODE	CR28
INTEGRATED CKT	Z67
RESISTOR	R64
TRANSISTOR	Q3
CHOKE	L1

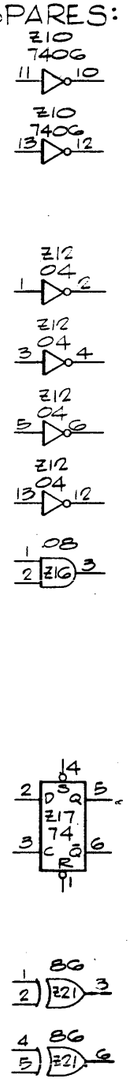
REVISION STATUS CONT.			REVISION STATUS		
FAB	SCH	ASSY	FAB	SCH	ASSY
D	E	E_2	A	–	–
D	F	E_3	B	A	A
E	–	–	C	B	B
F	G	F	C	B'	C
F	H	G	C	C	C_1
F	H	G_1	D	C'	D
G	J	H	D	C'	D'
			D	D	E
			D	D	E_1

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
A	–	3.13.79	RELEASED	JL	3.9.79	
B	19556	7.27.79	NSHM - ADDED JUMPER WIRES	D.G.M.	7.27.79	
B'	R/C	11.13.79	REVISED REVISION STATUS	M.M.	11.13.79	
C	19567	3.4.80	SEE ECO	REK	3.7.80	
C'	R/C	7.11.80	UPDATE REV. STATUS, REF ECO 19167	D.M.	7.14.80	
D	19255	8.14.80	SH 3, ZONE B4, R57 WAS 47K	D.G.M.	8.14.80	
E	19475	12.17.80	SEE ECO	D.G.M.	12.17.80	
F	19493	1.13.81	CHANGED R48, R47 AND C26; ADDED C54	D.G.M.	1.13.81	
G	19700	4.13.81	REVISED REV STATUS.	D.G.M.	4.13.81	
H	19768	5.15.81	SHTS 1 NOTE 19 WAS (74LS74) 704620-074 SHEET 5, RE-IDENTIFIED Z19 AS 7406 & PARTS	S.E.O.	5.15.81	
J	20202	—	UPDATED REVISION STATUS	D.G.M.		

SIGNAL INDEX

SIGNAL	DEFINITION	SOURCE	LOCATION
BTPHD	BUFFERED TOP HEAD	2B1	6D4
BTPHD*	BUFFERED TOP HEAD	3C6	2B2
CTO*	CENTER TAP 0	2B1	2C8
CT1*	CENTER TAP 1	2B1	2B8
DIR	DIRECTION (STEP)	5C6	4E7
DRDY*	DRIVE READY	6C3	5D6
ERASE 0	ERASE 0	3B2	2D8
ERASE 1	ERASE 1	3A2	2C8
FDWD	FLOPPY DISK WRITE DATA	5D6	2C3 2D3 3C7
HDLD*	HEAD LOAD	5C6	6C3
IP*	INDEX PULSE	6B3	5E6
PHO	PHASE ZERO	4A4	6E7
POR*	POWER ON RESET	5A6	3B5 4D7 5C7
SRDTA*	SERIAL DATA	2C1	5E6
STEP	STEP PULSE	5D6	4E7
TG43	TRACK GREATER THAN 43	5D6	3D7
TR00*	TRACK 00	6E6	5D6
WC –	WRITE CURRENT	3C2	2D8
WC +	WRITE CURRENT	3C2	2D8
WG	WRITE GATE	5C6	2C4 3E7
WPRT*	WRITE PROTECT	6D6	5D6

SPARES:



NOTE: UNLESS OTHERWISE SPECIFIED –

1. REFERENCE DRAWING - ASSY 114181-*.
2. THE THREE CHARACTER ADDRESS IS AS FOLLOWS: SHEET NUMBER - HORIZONTAL ZONE - VERTICAL ZONE
3. AN ASTERISK FOLLOWING SIGNAL NOMENCLATURE INDICATES THE COMPLEMENTARY FUNCTION.
4. RESISTORS ARE IN OHMS 1/4W ±5%.

		+5V	0V
5.	Z7 IS 701900-007.	6	1
6.	Z9 IS (Q2T 2905) 704202-113.		
7.	Z6, 8 ARE (556) 704520-134.	14	7
8.	Z1, 2 ARE (592) 704520-145. PIN 10 +5V. PIN 8 -5V.		
9.	Z27 IS (7905) 704520-137.		
10.	Z10 IS (7406) 704600-111.	14	7
11.	Z4, 13 ARE (75462) 704600-160.	8	4
12.	Z3 IS (8T20) 704610-172.	14	7
13.	Z14 IS (74LS00) 704620-000.	14	7
14.	Z22 IS (74LS02) 704620-002.	14	7
15.	Z12 IS (74LS04) 704620-004.	14	7
16.	Z16 IS (74LS08) 704620-008.	14	7
17.	Z19 IS (7404) 704600-110.	14	7
18.	Z11, 17 AND 20 ARE (74LS74) 704620-074	14	7
19.	Z21 IS (74LS86) 704620-086.	14	7
20.	Z23 IS (74LS244) 704620-244.	20	10
21.	Z24 IS (74LS373) 704620-373.	20	10
22.	Z5, 15 AND 18 ARE (96L502) 704621-004.	16	8
23.	Z26 IS (UHP407) 704900-110.	14	7
24.	Z25 IS (ULN 2074B) 704900-111.		
25.	CR1-9, 11, 12, 14, 15, 19, 20, 21, 22, 23 ARE (FDH6666) 704000-110.		
26.	CR17, 18, 24-27 ARE (1N4003) 704005-137.		
27.	CR10 IS (1N751A) 704010-116.		
28.	CR28 IS (1N747A) 704010-126. (3.6 V ZENER)		
29.	Q1, 2, 3 ARE (2N4401) 704203-114.		

DWG NO. 114182-001 REV. J

Figure 8-6. Schematic, Slave Card Assy. 114181-001.

FORM NO. EDS8/82

SYM	ECO	REVISIONS	BY	DATE	APP'D
		SEE SHEET 1			

WC +
WC -
J3
KEY
ERASE 0
CTO*
J4
ERASE 1
CT1*
KEY
CR6 CR5 CR7 CR8 CR2 CR1 CR3 CR4
R4 5.62K 1% 1/8W
R2 5.62K 1% 1/8W
+5V(F)
R5 10
C1 .01 MF 200V
OV5
R3 10K 1% 1/8W
R1 10K 1% 1/8W
R7 10
C3 .01 MF 200V
-5V(F)
E1 592
NC
C5 .22MF 35V
C4 .22MF 35V
L1 150UH
L2 150UH
L3 33UH
L4 33UH
C6 1000PF 100V
R8 221 1% 1/8W
R9 221 1% 1/8W
R11 75
R10 75
TP5
TP4
C2 .1MF ±10% 50V
RG 150
C7 1000 PF 100V
TP7
OVE
R13 150
E2 592
+5V(F)
-5V(F)
R16 1.5K
R17 1.5K
R15 33K
R14 33K
R12 50K 3/4W 20%
CW
TP9
TP10
WG
C9 39PF 300V
R18 2.2K
C8 39PF 300V
R19 24K
Z3 8T20
OV5
-5V
NC
+5V
R54 2.2K
R55 2.2K
VP3
Z17 74
C40 22PF 300V
R57 5.1K
120-180ns
FDWD 96LS02
Z18
NC
VP3
C38 22PF 300V
R56 5.1K
120-180ns
FDWD 96LS02
Z18
NC
VP3
TP8
Z14
SRDTA*

+5V
+5V(F)
C51 .01MF
C53 47MF 6.3V
C52 47MF 6.3V
L6 150UH
C14 10MF 25V
C11 .01MF
OV5
C15 .01MF
C36 47MF 6.3V
C13 10MF 25V
C10 .01MF
L5 150UH
-5V
-5V(F)

+24V
+24V(F)
C18 .01MF
C19 .01MF
OV24

+24V(F)
R25 10K
75462
BTPHD*
CTO*
+24V(F)
R26 10K
75462
Z14
CT1*
VP1
BTPHD

114182-001 REV

Figure 8-6. Schematic, Slave Card Assy. 114181-001.

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPD
			SEE SHEET 1			

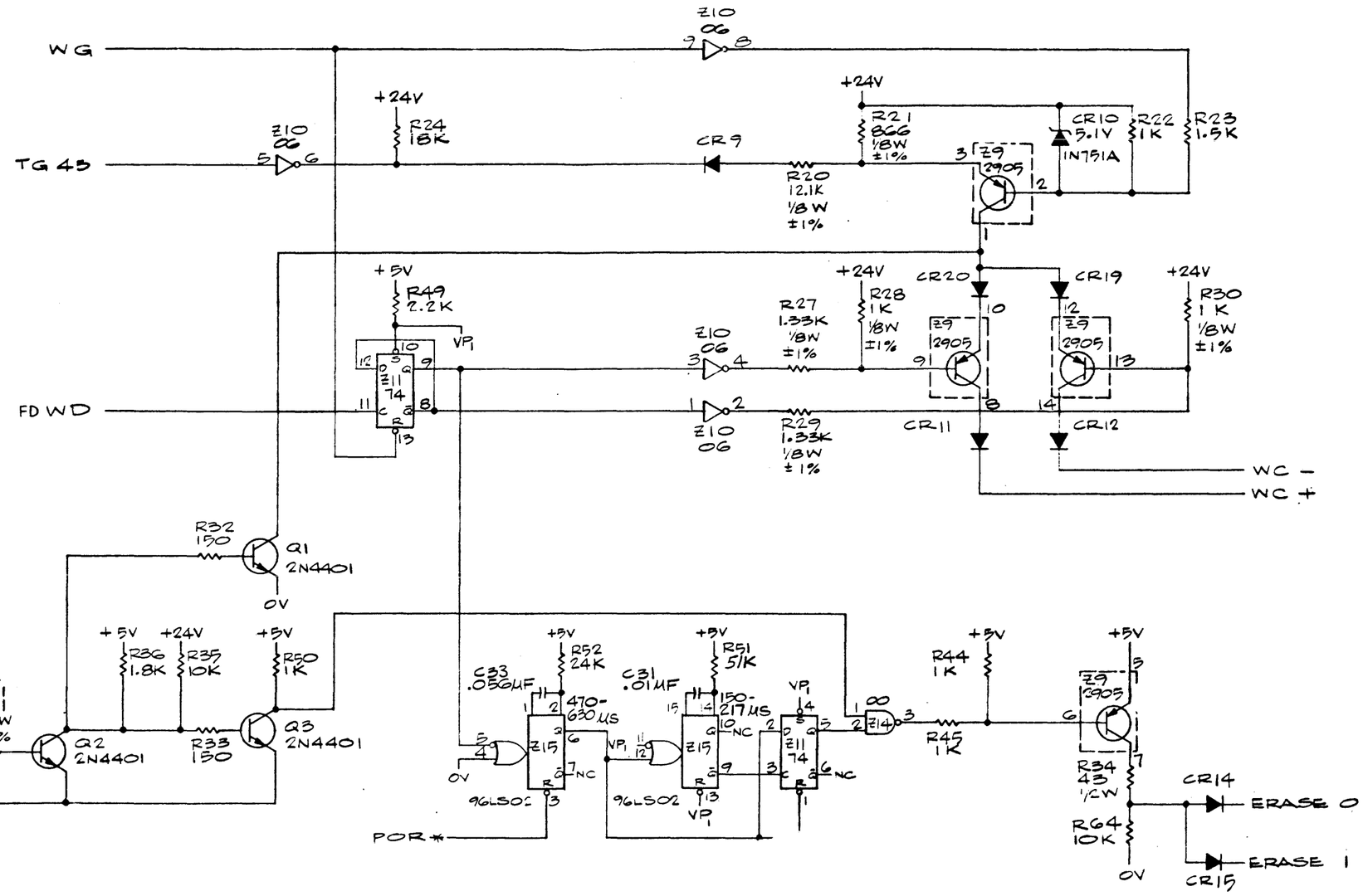


Figure 8-6. Schematic, Slave Card Assy. 114181-001.

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPD
			SEE SHEET 1			

DIR

STEP

POR*

+5V

R58 2.2K

Z21 7486 ECO

Z20 7486

VP2

Z16 UHP407

R62 3.3K

Z25 2074B

+24V

CR26 IN4003

KEY

PART OF J6

STEP MOTOR PHASE 1

PART OF J7

POWER RESISTOR

Z26 UHP407

R60 3.3K

CR24 IN4003

Z26 UHP407

R61 3.3K

CR27 IN4003

STEP MOTOR PHASE 2

Z26 UHP407

R59 3.3K

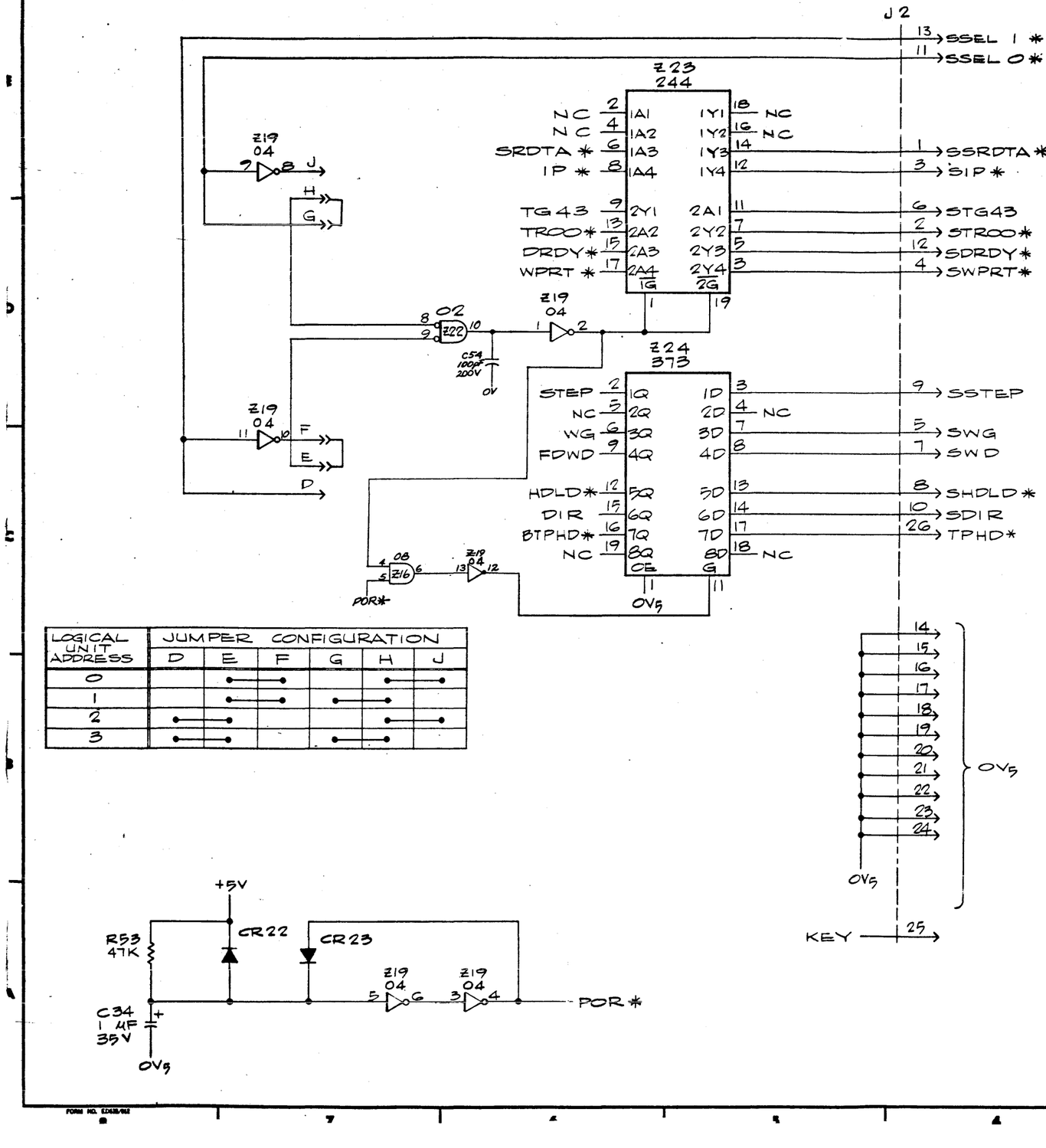
CR25 IN4003

Z16

PHØ

Figure 8-6. Schematic, Slave Card Assy. 114181-001.

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPR'D
			SEE SHEET 1			



LOGICAL UNIT ADDRESS	JUMPER CONFIGURATION					
	D	E	F	G	H	J
0		—			—	—
1		—		—	—	
2	—	—			—	—
3	—	—		—	—	

Figure 8-6. Schematic, Slave Card Assy. 114181-001.

DWG No. 114182001 REV J

SYM	ECO	EFFECT	REVISIONS	BY	DATE	APPRD
			SEE SHEET 1			

PART OF J1

TR00 SW 14 — +5V — R43 100 — 5 — 22 — 18 — +5V — 0V

EXTERNAL WRITE PROTECT

WRITE PROTECT SENSOR 17 — +5V — R42 100 — 16 — LED 4 — 21 — 0V

SINGLE SIDED INDEX 6 — +5V — R41 100 — 7 — LED 3

DOUBLE SIDED INDEX 9 — +5V — 8 — 20 — 0V

PH Ø

Z12 04

TP6 — TR00*

Z5 96LS02 — NC — 180-200ms

Z7 10K — 0V

TP3 — WPRT*

Z8 — NC

TP1

Z6 — NC

TP2

Z9 — NC — R40 10K

C21 15µF 15V — R38 39K

C22 15µF 15V — R39 39K

BTPHD

Z22

HDLD* — Z12 04

DRDY*

IP*

Z16

J5

−V 1 — KEY 2 — +24V 3 — 0V24 4 — +5V 5 — 0V5 6

C49 10µF 25V — C17 .22µF 50V — Z27 7905 — C16 .22µF 50V — −5V

TP11 — TP12 — TP13 — TP14

C47 10µF 50V — C48 47µF 6.3V — C20 23-25 27-30 32 33 37 39 41-46 .01µF 25V — C50 .22µF 50V

−V	JUMPER		
	N	P	R
−5V		●	●
−6V TO −12V	●		

DOOR LOCK SOLENOID	JUMPER CONFIGURATION		
	A	B	C
ENABLE	●	●	
DISABLE		●	●

PART OF J1

+5V — R37 1K — 13 — DOOR NOT CLOSED

7 — 7406 — 6 — Z13 — 5 — CR18 IN4003 — +24V — 30 (+) / 29 (−) — DOOR LOCK SOLENOID

NC (PINS 2, 10, 11, 12, 23, 24, 25, 26, 27)

A — B — C — 0V

+5V — 34 — + LED

2 — 7406 — 1 — Z13 — 3 — CR21 — R48 100 — 33 — − LED

+24V — C26 47µF 25V ±20% — CR17 IN4003 — 31 (+) / 32 (−) — HEAD LOAD SOLENOID

R46 100±1% 2W — R47 68±1% 2W

KEY — 19

28 — 0V24

114182-001 REV J

Figure 8-6. Schematic, Slave Card Assy. 114181-001.

Ex-Cell-O Corporation

REMEX DIVISION