PUNCH DRIVER BOARD ASSEMBLY, E-569344

TDG-378

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GENERAL INFORMATION

1.1 INTRODUCTION

Punch driver board assembly, E-569344, illustrated in Figure 3.1, has been designed to operate the various tape punches manufactured by Litton ABS. Jumper points, located on the punch board, permit deactivation of those functions not required by a specific punch model. Section 1 of this manual describes the basic operation, physical description and electrical characteristics of the punch driver board. Section 2 contains a detailed functional description of the hybrid circuits employed. A parts catalog is included as Section 3 of this manual.

1.2 BASIC OPERATION AND USE

The punch driver board assembly converts information taken from the data source into signals which activate the feed, index, and punch solenoids. The data source controls the direction of tape feed and the holes to be punched. In addition, the punch driver board generates an IN-PROCESS signal to the data source whenever it is operating on previous information given, or an excess tape tension or out-of-tape condition exists.

1.3 PHYSICAL DESCRIPTION

The punch driver board assembly measures 4-5/8 inches by 6-1/4 inches and weighs approximately four ounces. It is connected to an AMP-44 pin edge connector (AMP part 582358-2), or equivalent.

1.4 ELECTRICAL CHARACTERISTICS

The electrical characteristics of the punch driver board assembly are listed in the following table of specifications.

INTEGRATED CIRCUIT-PUNCH DRIVE ELECTRONICS INTERFACE SPECIFICATIONS

ELECTRICAL CHARACTERISTICS:

LOGIC LEVELS A signal logic level is designated true or high when the voltage level is between +2.4 and +5 volts; false or low when the voltage level is between -0.5 and +0.4 volts. Rise and fall time shall be less than 200 nanoseconds. Minimum pulse width is five microseconds. Maximum frequency is limited to the shaft rotation rate of the punch model employed.

CURRENT SINKCurrent sink for all input signals is equalAND SOURCEto -3.2ma (two TTL's). Current source is
equal to an open condition.

OUTPUT LOGIC SIGNAL:

IN PROCESS (BUSY)

Output signal (pin Z) - used to indicate a busy condition. This signal may be activated by an external circuit or internally by the logic when the punch is processing data. Usually externally controlled by a tape tension or out-of-tape switch. A true or high signal indicates the punch is busy. A low signal indicates the punch is ready for a new punch cycle. Current sink for the IN PROCESS signal is equal to -12.8ma (8 TTL's) and current source is equal to 320ma. A low input at pin X causes the IN PROCESS signal to go high.

INPUT LOGIC SIGNALS:

The following signals are controlled by either the data source or external circuits.

START PROCESS

Input signal (pin 22) - The positive-going leading edge of this signal initiates a new punch cycle. This signal must not be generated until the IN PROCESS signal has been low for more than five microseconds. Minimum separation between pulses must be five microseconds.

FEED DIRECTION

Input signal (pin Y) - used to specify forward or reverse feed (high-forward, low-reverse). A change in the FEED DIRECTION signal is permitted only when the IN PROCESS signal is low and before a new START PROCESS signal occurs.

NOTE: Punch operations are enabled only during forward feed.

DATA OUTPUT Channels 1 thru 8 Input signals (pins V, U, T, S, P, N, L, J) - a true or high indicates a hole is to be punched. The data inputs must be <u>valid</u> within 100 microseconds after the <u>START PRO-</u> CESS signal and remain valid until the IN PROCESS signal goes low.

TAPE FEED

TAPE TENSION + OUT-OF-TAPE Input signal (pin 17) - a low input will cause the punch to generate leader. This signal is usually generated via a manually operated switch external to the board.

Input signal (pin X) - a low input will generate an IN PROCESS signal. The signal is usually generated via a switch whenever the punch is out of tape or the tape has exceeded a predetermined tension.

INPUT LOGIC SIGNALS WITH JUMPER OPTIONS:

The following signals are controlled either by jumpers on the punch board or by external circuits when jumpers are removed.

Three of the inputs to the punch driver board assembly are used to inhibit a particular function and can be enabled by installation of jumpers. With the jumper removed, a high input signal to the circuit will inhibit the function.

PARITY INHIBIT
LEADER signal (pin -1) - a low input will generate leader tape with a punched hole on channel five. Normally used in parity applications. Install jumper J3 to punch holes in channel five when feeding leader.
INDEX INHIBIT V
CARD IN POSITION (pin -2) - used to indicate the use of a prepunched card. A high input inhibits the index punch from punching the already prepunched cards. Install jumper J2

to punch index holes when feeding media.

CARD HOLE signal (pin -3) - a high input signal will inhibit punching and feed the media until the signal goes low. Install jumper Jl to punch data when feeding media.

The fourth jumper, J4, is installed when it is desired to connect signal ground to ac ground.

Capacitor C5 is also optional and, when installed, provides ac bypass between ac ground and signal ground. Normally capacitor C5 is not used when jumper J4 is installed.

POWER REQUIREMENTS:

VOLTAGE REGULATION

CURRENT DRAIN

Voltage variations, including ripple, do not exceed \pm 10% of the +24vdc and \pm 5% of the +5vdc.

Average current drain for the +24vdc is 0.6a with maximum current at 1.2a for ten milliseconds (this is a worst possible case, i.e., punching all holes at full speed). Average current for the +5vdc is 0.4a with a maximum continuous current of 0.5a.

Three grounds are utilized. They are as follows:

- 1. <u>Chassis Ground</u>: This ground is brought into the board on pin 12. Normally there is no connection to this ground on the board. Optionally, a jumper position is available to connect this ground to the signal ground.
- Signal Ground: This ground is the return for the I.C. level signals and the +5 volt supply brought into the board on pin 9.
- 3. <u>Solenoid Ground</u>: This ground provides the return for solenoid currents to the +24V supply brought into the board on pin 20.

For proper operation, all three grounds must be connected together at one point near the data source power supply.

GROUNDING

FUNCTIONAL OPERATION

2.1 GENERAL

The punch driver board assembly interfaces with the various switches and solenoids to control tape feed, index, and punch operations.

The board electronics can be divided into the following functional circuits:

Timing Pulse Generator Forward Drive and Punch Control Reverse Drive Control Feed and Punch Control Circuit

The Timing Pulse Generator utilizes the timing wheel solenoid to generate a square wave signal which is applied to the forward drive and punch control and the reverse drive control.

The Forward Drive Control consists of the forward flipflop FFl and driving components which energize the forward feed and index punch solenoids, L9 and L11, respectively.

The Reverse Drive Control consists of reverse flipflop FF2 and driving components which energize reverse feed solenoid, L10.

The Feed and Punch Control Circuit consists of the feed control flipflop FF3 and the punch control flipflop FF4. The feed control flipflop enables the forward and reverse drive control circuits.

The Punch Control flipflop enables the eight data punch drive components. The circuit controls the punching of holes into the tape.

2.2 TIMING PULSE GENERATOR

When the timing disc at one end of the input shaft interrupts the magnetic flux produced by current flow through the timing pulse generator, a timing pulse is generated. The pulse coil is mounted adjacent to the timing disc and its load coil is mounted to the same side frame.

Current flow through the load coil maintains the pulse generator at a nominal voltage level. Induction establishes a magnetic field whose

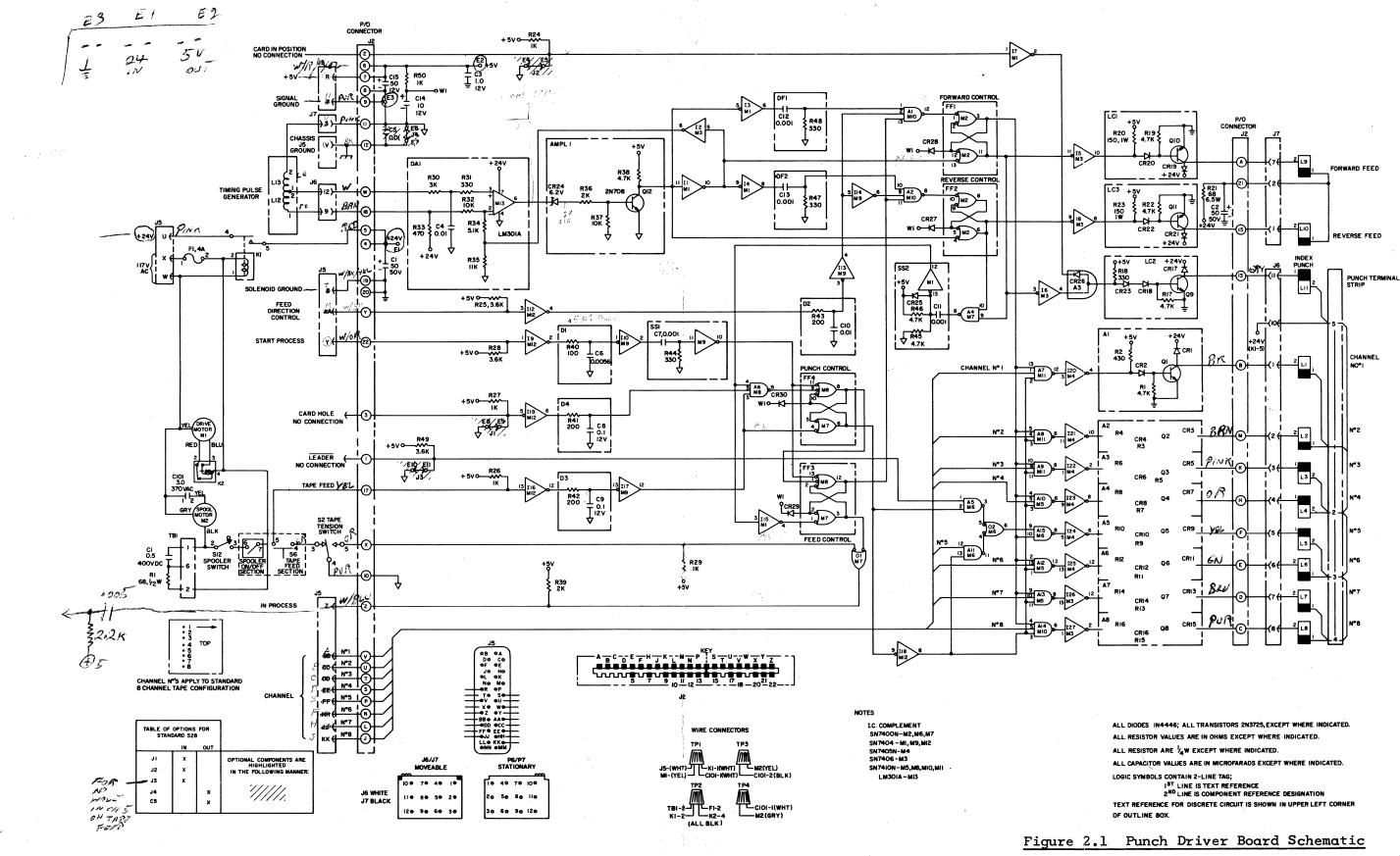
flux lines pass through the timing disc, the input shaft and the side frame to form a complete loop. Any interruption of the flux path changes the intensity of the magnetic field and produces a transient voltage level shift in the form of a positive or negative-going spike.

The edge of the timing disc comes closer to the pulse coil at an input shaft setting of 180 to 360 degrees than it does between zero and 180 degrees. At zero, the gap increases and the resultant collapse of the magnetic field induces a voltage in the pulse generator which tends to maintain the direction of current flow; thus, a positive-going spike results. When the timing disc reaches 180 degrees, the disc surface suddenly increases, the gap between the disc and pulse generator decreases, and the magnetic field builds up rapidly, thereby producing a negative-going spike.

These positive and negative spikes are applied to differential amplifier DA1, Figure 2.1. A positive spike, occurring at zero degrees, with respect to the timing disc, causes a difference between the inputs to DA1 to result in a positive output voltage. A negative spike, occurring at 180 degrees, causes a negative voltage at the output of DA1. These output voltage levels are converted into logic levels via amplifier AMPL 1 and fed back via I1 and I2 to sustain the latching action of the circuit. This results in a square wave output at AMPL 1 and its complement at the output of Il. The square wave from AMPL 1 is inverted by I3 and leading edges are differentiated via DFl to form positive spikes. These sample gate Al, which is the input control gate to the forward control flipflop FTL. Positive spikes are inverted by the gate to set FF1 when the feed control flipflop, FF3, is set and the direction control indicates forward drive. The forward feed flipflop is reset by the trailing edge of the output from Il. The output from Il is also inverted at I4 and differentiated at DF2 to form positive spikes which are 180 degrees out of phase with the output of DF1. These spikes sample gate A2 which is the input control gate to the reverse feed flipflop FF2. Positive spikes are inverted by the gate to set FF2 when the feed control flipflop FF3 is set and the feed direction control line indicates reverse drive. The reverse feed flipflop is reset by the trailing edge of the output from AMPL 1.

2.3 FORWARD DRIVE AND PUNCH CONTROL

Forward drive and index punching is controlled by the state of the forward feed flipflop FF1. The zero output level is applied via I5 to level changer LC1 and via 16 to level changer LC2. When FF1 is set, the outputs of LC1 and LC2 go to ground to energize the forward feed solenoid and the index punch solenoid, respectively. The output of 16 is applied via gate A3. This gate is always enabled when jumper J2 is in place. Removal of J2 allows the electronics to inhibit index punching in punches which handle cards. A card in position signal at pin 2 is inverted via I7 to inhibit gate A3 and block drive signals to the index punch solenoid.



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The one output from FF1 is applied to the data punch enabling gates in the feed and punch control circuit.

2.4 REVERSE FEED CONTROL

Reverse feed is controlled by the state of the reverse flipflop FF2. The zero output level is applied via I8 to level changer LC3. When FF2 is set, the output of LC2 goes to ground to energize the reverse feed solenoid.

2.5 FEED AND PUNCH CONTROL CIRCUIT

The feed and punch control circuit operates in response to the start process signal during automatic operation. During manual operation, the circuit operates in response to the tape feed switch signal.

2.6 AUTOMATIC OPERATION

When a start process signal is received, it is applied via Dl and IlO, for an 0.5usec delay. The delayed leading edge triggers single shot SS1 to generate a negative pulse which sets the feed control flipflop FF3 and the punch control flipflop FF4 0.5 useconds after the arrival of the start process signal. The feed control flipflop then partially enables the control gates to the forward and reverse flipflops. Full enabling of either gate is determined by the feed direction control signal at pin Y. When the feed direction control is high, inverter I12, in conjunction with delay D2 and inverter I13, provides a high level to enable gate Al. When the feed direction control is low, inverter I14 provides a high level to enable gate A2. The feed control flipflop resets when either the forward or reverse feed flipflop is resetting. The zero output from both FF1 and FF2 are applied to gate A4, which produces a -Ve going output when either FF1 or FF2 is resetting. This output triggers SS2 to form a reset pulse, via I15, for the feed control flipflop.

When the feed control flipflop is set, the prime output is applied via gate 01 to form the in process signal. This in process signal is also generated when the tape tension switch indicates either tension in the tape, or absence of tape.

When the punch control flipflop is set, its prime output (now low) partially enables gates A7 through Al4, via inverter Il8. These gates receive the data pulses for punching. These gates are also partially enabled by the one output of the forward feed flipflop FF1. When a hole is to be punched, all inputs to the gate are high resulting in a low output, which, via an inverter and level changer, energizes the corresponding punch solenoid.

2.7 MANUAL OPERATION

Manual operation is controlled by the tape feed switch. When depressed, a low level signal is applied at pin 17 which, via Il6, D3 and Il7, resets the punch control flipflop FF4. The true output, going low, sets the feed control flipflop FF3. Tape is continuously advanced and index holes are punched as long as the tape feed switch is held closed.

In addition to index holes, a leader can be punched in channel 5 by removal of jumper J3. This is accomplished as follows: With FF4 in the reset state, its prime output is high and enables gate A5. With jumper J3 removed, the second input to A5 is controlled by the external signal at pin 1. With gate A5 satisfied, its output, via gate O2, satisfies gate A15 to turn on the channel 5 solenoid drive circuit.

When the tape feed switch is opened, the signal at pin 17 goes high. This signal, via Il6, D3 and Il7, enables gate A6. The input to gate A6 at pin 5 is always held high by the presence of jumper Jl.

When single shot SS2 emits a pulse, it is gated through A6 to set FF4, and is applied through I15 to reset FF3.

Removal of jumper Jl allows use of the input at pin 3 as a card hole indicator. In this case, when a card hole is sensed, the input goes low and, via I19 and D4, partially enables gate A6.

2.8 OPTIONAL +5 VOLT REGULATED POWER SUPPLY

The optional power supply, Figure 2.2, consists of an integrated circuit regulator and a series pass power transistor. When the load voltage increases, it is reflected back to the regulator which decreases the output voltage via the power transistor. This degeneration of the regulator maintains the output at a constant level of +5vdc.

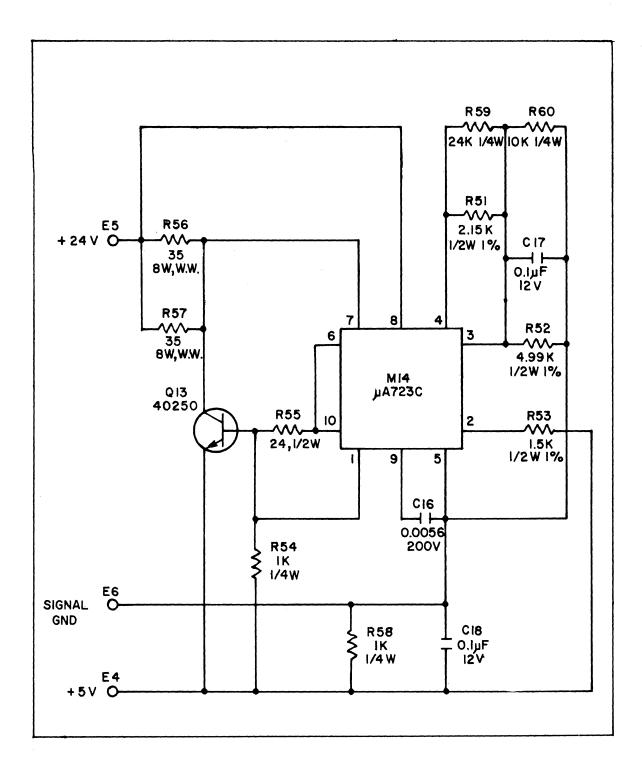


Figure 2.2 +5 Volt Regulated Power Supply Schematic

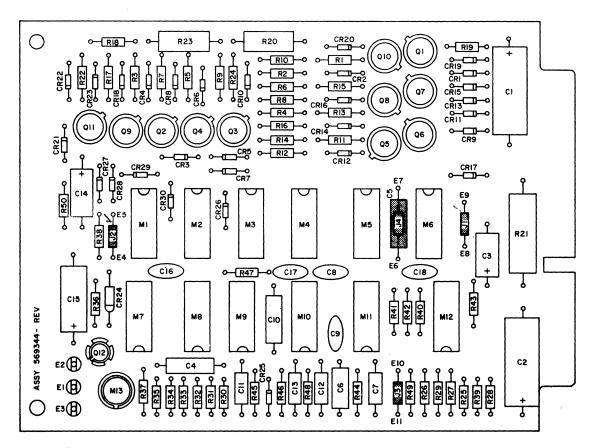
PARTS LIST

PUNCH DRIVER BOARD ASSEMBLY FIGURE 3.1

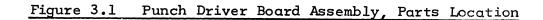
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REF. DES.	PART NO.	DESCRIPTION	QTY.
1	E-560051	Marking - Punch Board	1
2	E- 588420	Solder Terminals-Cambion 1969-2	3
3	E-596291	Transipad	11
4	E-596459	Transipad	1
5	E-596460	Transipad	1
6	E-592252	Jumper	4 *
C1, 2	E-586221-13	50µf, 50V, Elect. Capacitor	2
C3	E-586219-1	luf, 12V, Elect.	1
C4, 10	E-586217-13		2.
7 C5	E-586217-13	0.01µf, 200V, Film	1 *
C6	E-586217-10	0.0056µf, 200V, Film —	1
C7, 12, 13, 11	E-586217-1	0.001µ1f, 200V, Film	4
C8; 9; 16, 17; 18-	E-586190	0.luf, 12V, Disc.	5
C14	E-586219-8	10µf, 12V, Elect.	1
C15/	E-586219-13	50µf, 12V, Elect. Capacitor	1
010		• • •	
CR1- ^ CR23,	- E - 580077	1N4446 Diode 636 \$	29
CR25 -CR30			
	-E-580043	6.2V, 5% Zener Diode	. 1
M1, 9, 12	E-585060	Hex Inverter SN7404 $(2)^{30}$	3
M2, 6, 7	E-585007-0	Quad 2 Input Positive NAND 30 Gate - SN7400N	3
M3	E-585047	High Level Inverter SN7406 μ^3	1
M4./	E-585061	Hex Inverter w/open collector output SN7405N	1
M5, 8,	E-585008-0	Triple 3 Input Positive NAND	4
10, 11/	•	Gate SN7410N	· •
M13	E-585058	Operational Amplifier LM301A 30	1
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	PART NO.	DESCRIPTION	QTY.
Q12	E-581093 E-581089 E-582711-472	Transistor 2N3725 Transistor 2N7089 ²⁰ Resistor 4.7K, 1/4W, Prec. Film, 5%	11 1 14
45" and 46	E-582711-431	Resistor 430Ω, 1/4W,	8
R18, 31, 44, 47, 48-	E-582711-331	Resistor 330Ω, 1/4W,	5
R20, 23 R21		Resistor 150 Ω , 1W, Prec. Film, 5% Resistor 68 Ω , 6.5W, WW, 5% Resistor 1K, 1/4W, Prec. Film, 5%	2 1 5.
R25, 28, 49 R30 R32, 37 R33 R34	E-582711-101	Resistor 3.6k, $1/4W$, Resistor 3K, $1/4W$, Resistor 10K, $1/4W$, Resistor 470 Ω , $1/4W$, Resistor 5.1K, $1/4W$, Resistor 11K, $1/4W$, Resistor 2K, $1/4W$, Resistor 100 Ω , $1/4W$, Resistor 200 Ω , $1/4W$, Prec. Film, 5%	3- 1 2- 1 1 1 2- 1 3



OPTIONAL

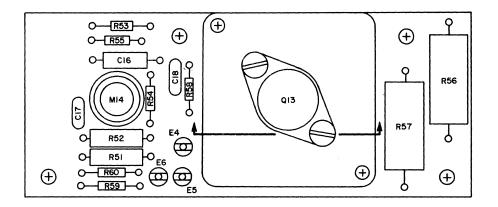


PARTS LIST

+5 VOLT REGULATED POWER SUPPLY FIGURE 3.2

ITEM OR REF. DES.	PART NO.	DESCRIPTION	QTY.
4 5 6 7 8 9 10 11	E-560052 E-588420 E-588419 E-594028-8 E-595804-6 E-595800-6 E-592015 E-592143 E-592143 E-592016 E-596760 E-588295	PC Board, Marked Solder Terminal (E4, 5, 6) Heat Dissipator (Astrodyne #2300-005A01A) Pan Hd.Mach.Screw, 6-32x0.500 lg. Lockwasher, Ext. Tooth, #6 Machine Nut, Hex, 6-32 Wire, #18 AWG, RED Wire, #18 AWG, RED Wire, #18 AWG, OR Wire, #18 AWG, BLK Transipad Washer, Shoulder, Nylon	1 3 1 2 2 2 A/R A/R A/R 1 2
	E-592403 E-586217-10 E-586190 E-585043	Heat Sink Compound, Silicon Capacitor, 0.0056µf, 200vdc, Film Capacitor, 0.1µf, 12vdc, Disc IC, Voltage Regulator (Fairchild µA723C)	A/R 1 2 1
R54, 58 R55 R56, 57 R59	E-581051 E-582720-232 E-582720-267 E-582720-217 E-582711-102 E-582712-240 E-582719-013 E-582711-273 E-582711-103	Transistor (40250) Resistor, 2.15K \pm 1%, 1/2W, Film Resistor, 4.99K \pm 1%, 1/2W, Resistor, 1.5K \pm 1%, 1/2W, Resistor, 1K \pm 5%, 1/4W, Resistor, 24 Ω , \pm 5%, 1/2W, Film Resistor, 35 Ω , \pm 5%, 8W, WW Resistor, 27K \pm 5%, 1/4W, Film Resistor, 10K \pm 5%, 1/4W, Film	1 1 1 2 1 2 A/R * A/R *

* R59 and R60 are used to bring output voltage to within 5V ± 5%. (R59 lowers voltage, R60 increases voltage.)



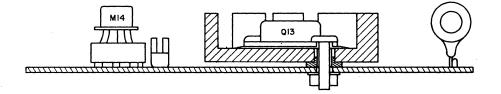


Figure 3.2 +5 Volt Regulated Power Supply, Parts Location

528 PUNCH DESCRIPTION

4.1 DESCRIPTION

The 528 Punch is a desk top unit and punches eight-channel paper or mylar tape. The unit utilizes an integrated circuit punch drive board to control tape feed, index punching and data punching.

Connection to the unit is at the rear via a 34-pin connector.

The unit is equipped with a tape supply drawer and rewinder unit. Controls associated with the unit are a tape feed spooler on/off switch (S6), tape tension switch (S2), and spooler tension switch (S12).

4.2 OPERATION

The unit requires 117vac for spooler and punch motor operation and connection to the +24 volt dc source. The fused 117vac input operates relay Kl. Closure of relay Kl connects +24vdc to the punch drive board. The required +5vdc power can be supplied externally (J5-R) or by the optional +5 volt regulated power supply.

Automatic punching is controlled by the start process (J5-Y) and feed direction control (J5-AA) levels from an external data source. The in process signal (J5-2) is generated during punch operations or when tape is out or in tension.

4.3 CONTROLS

The only manual control is the three-position rocker switch on the left front of the unit. The mid-position is off. When depressing the upper section of the switch, a tape feed signal is generated which advances the tape. This is a momentary type position and must be held to advance tape. When depressing the lower section of the switch, power is applied to the spooler motor via the closed spooler tension switch. The spooler tension switch closes when the tape being taken up is not under tension.