XEROX

Xerox Data Systems
Technical Information

APPENDIX A

MODEL 7900

DEVICE SUBCONTROLLER

XDS 98 03 63A August 1969

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XDS 98 03 63A August 1969

XDS

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INTRODUCTION

This appendix contains a detailed description of the Model 7900 device subcontroller (DS), designed and developed by Xerox Data Systems, El Segundo, California.

To provide a comprehensive physical and functional description of the equipment and its system application, information is presented in the following sectional format:

Section A-I contains general information about the device subcontroller and the computer system in which it functions. The general information includes physical descriptions, performance specifications, and operating characteristics.

Instructions for operating, controlling, and programming the equipment are provided in Section A-II.

Section A-III contains a detailed functional analysis of the circuit configurations used in the device subcontroller. In this section, logic explanations are augmented by logic diagrams, timing diagrams, and data flow charts. Logic diagrams are in conformity with MIL-STD-806B (XDS modified).

Recommended procedures for testing and maintaining the equipment are provided in Section A-IV.

Section A-V lists the drawings and documents that are referenced but not contained in this manual.

Documents that provide application data for integrated circuit logic modules used in the extended device subcontroller are included in Section A-VI.

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A-I. CHARACTERISTICS AND ORGANIZATION

This section contains a general description of the device subcontroller, and also includes a physical description, functional description and operating characteristics.

A1-1 EQUIPMENT DESIGNATIONS

In a system configuration, the device subcontroller is functionally related to a peripheral device via the device controller, and to an XDS Sigma Computer via the input/output processor. These units are referred to throughout the text by the following designations:

DS = Device Subcontroller

DC = Device Controller

IOP = Input/Output Processor for Sigma Computer

CPU = Central Processing Unit of Sigma Computer

A1-2 GENERAL DESCRIPTION

As a part of the peripheral device controller for the computer system, the DS provides the following system requirements:

(a) All cable drivers and cable receivers required to connect the eight-bit data path interface.

(b) Logic required to determine priority during Acknowledge Service Call (ASC) and Acknowledge Interrupt (AIO) operations.

(c) Eight address selection switches and logic for comparing the switch outputs against the device number presented by the IOP during Start Input/Output (SIO), Halt Input/Output (HIO), Test Input/Output (TIO), and Test Device (TDV) operations.

(d) Service Connect flip-flop (FSC).

(e) Remote-controlled relay logic to regulate interconnection between the DS, DC, and I/O interface during a Power ON - Power OFF sequence.

A1-3 OPERATION

The DS, used in conjunction with a DC, controls a device whose number is determined by the position of the eight address selection toggle switches.

A1-4. PHYSICAL DESCRIPTION

The device subcontroller consists of nine logic modules mounted in a standard 5.25-inch by 19-inch rack, as shown in figure A1-1. Slots 23 through 32 are wired to accept the DS modules.

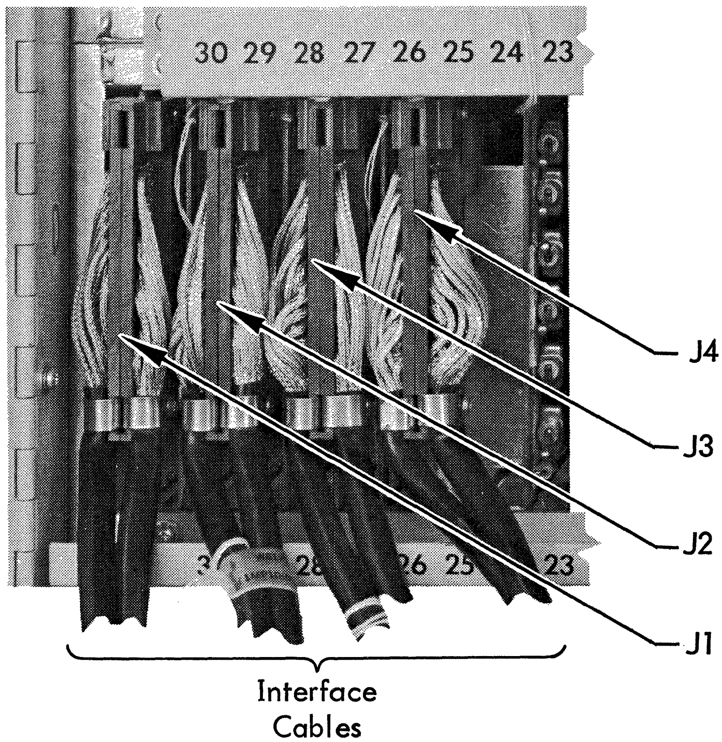


Figure A1-1. Device Subcontroller Logic Modules, Installed

A1-5. LOGIC MODULES

The XDS T-Series IC (integrated circuit) digital logic modules that constitute the DS module complement, are described in Table A1-1. Modules AT10, AT11, and AT12 are connected to signal cables from the IOP, and the priority cable from the IOP connects to module AT17. The remaining modules perform various DS functions.

A1-6. DS TO IOP INTERCABLING

The DS is connected to the IOP through four interface cables, including three signal cables and one priority cable. A simplified illustration of the intercabling scheme is shown in figure A1-2.

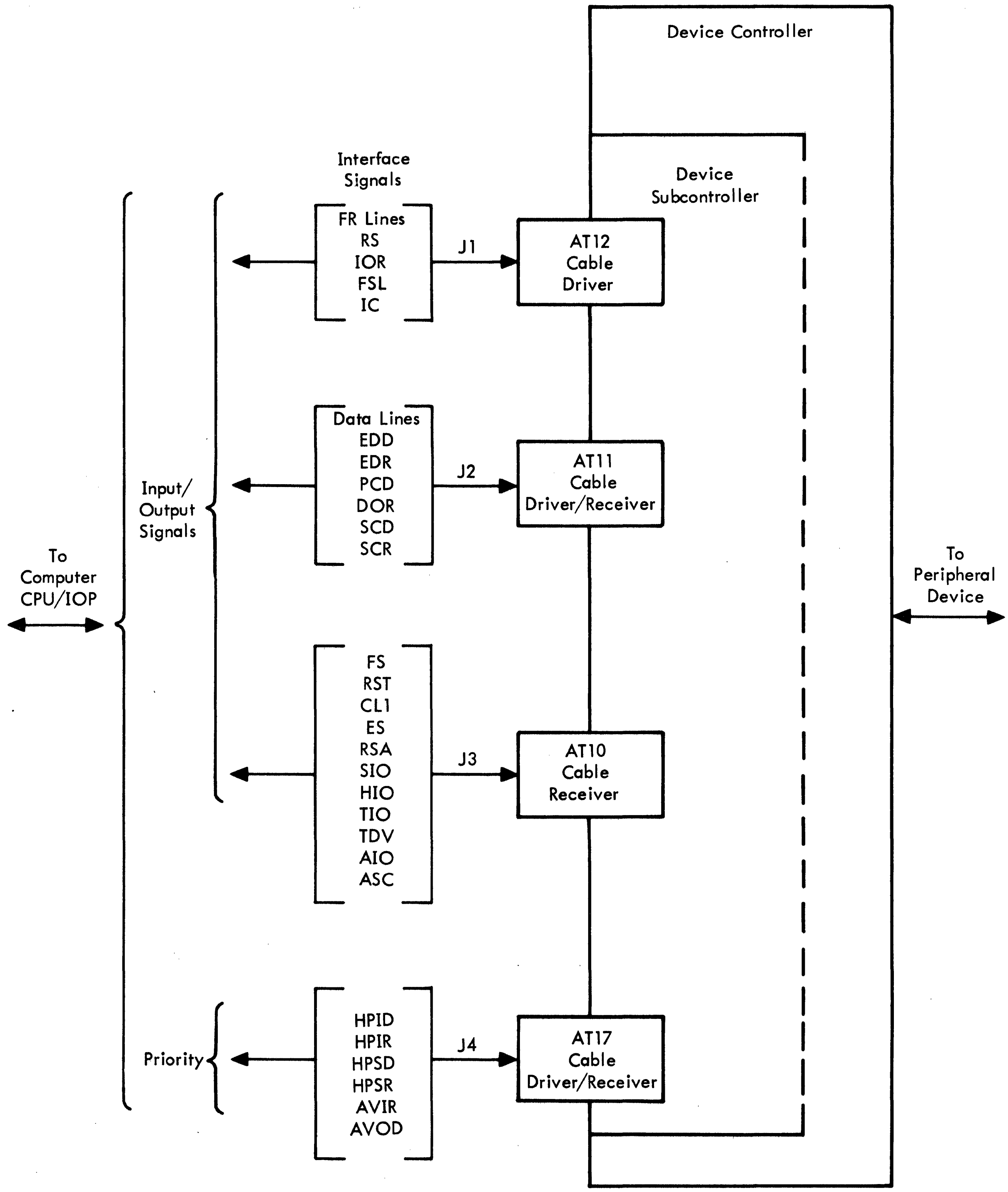


Figure A1-2. IOP-DS-DC Intercabling Diagram

Table A1-1. DS Logic Modules

Type	Description	Location(s)	Quantity
AT10	Line Receiver	28	1
AT11	Cable Driver/Receiver	30	1
AT12	Cable Driver	32	1
AT17	Cable Driver/Receiver	26	1
LT24	Logic Element	27	1
LT25	Logic Element	23	1
LT26	Switch Comparator	24	1
LT41	Logic Element	29	1
LT43	Logic Element	31	1
		Total	9

Each interconnecting cable contains 14 shielded conductors. The shielded conductors (used as transmission lines) are each terminated into a characteristic impedance of 33 ohms at both ends. Electrical characteristics of a typical transmission line are described in Table A1-2.

Table A1-2. Transmission Line Characteristics

Characteristic	Specification
Characteristic Impedance	33 ohms
DC Resistance (Conductor)	23 milliohms per foot
DC Resistance (Shield)	10 milliohms per foot
Inductance	50 nanohenries per foot
Capacitance	50 picofarads per foot
Signal Delay	1.4 nanoseconds per foot

The four I/O cables are connected to logic modules on the DS by bolting the cable connector assemblies to the modules. Connection details are shown in figure A1-3. Module connectors P2 and P3 consist of 14 alphanumeric terminal pairs. P2 terminals are numbered 1 through 14. Each P2 terminal is connected through the module card to the P3 terminal on the opposite side of the card. P3 terminals are designated A through R, with letters I, O, and Q omitted. Pin designations on each cable connector match the terminal designations on the modules.

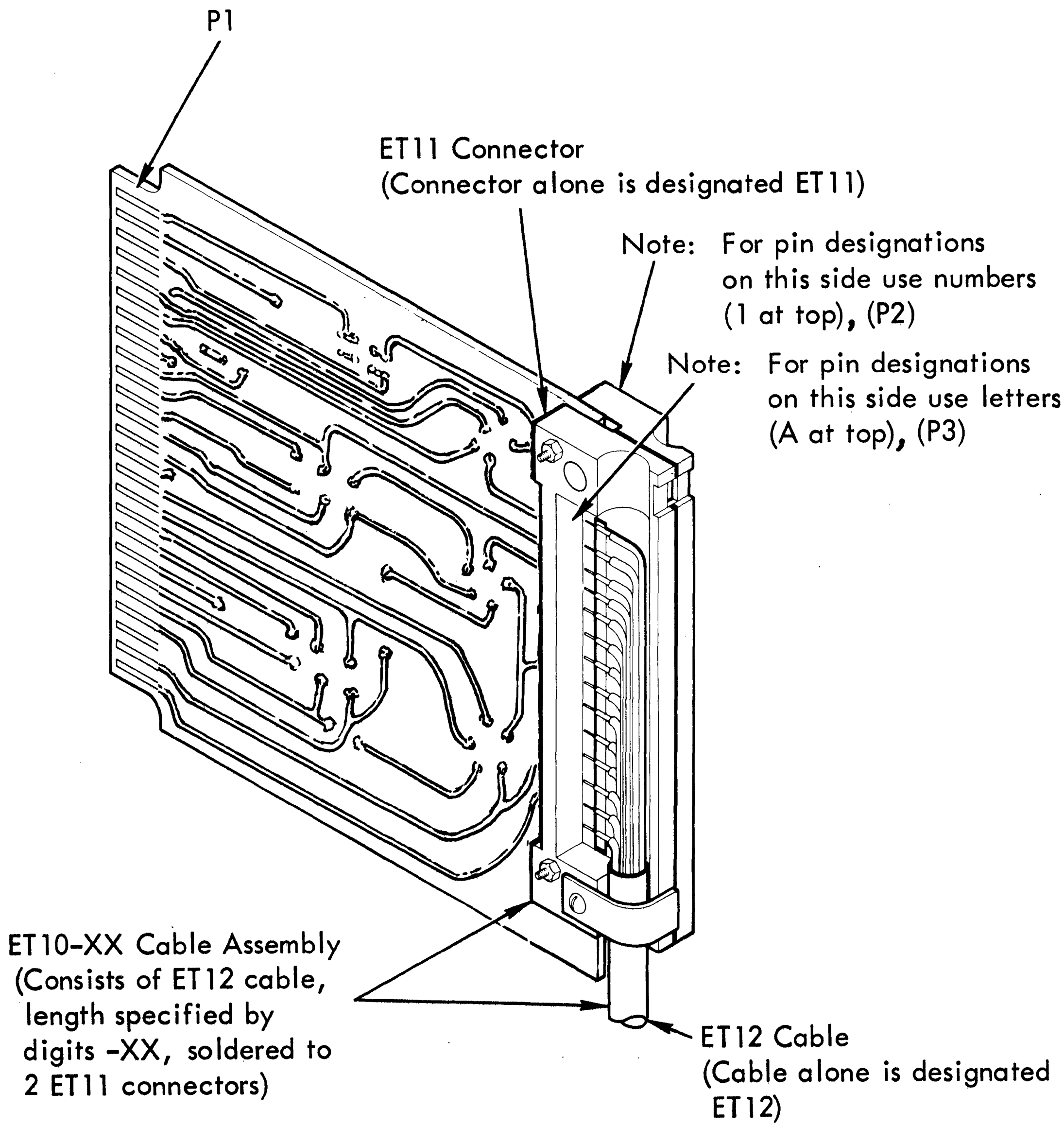


Figure A1-3. I/O Cable Connections to DS Logic Modules

Note

On Cable Driver/Receiver AT17, module location 26, terminal 4 on P2 and terminal D on P3 are not connected to terminals on the opposite side of the module card.

The I/O cables are connected to the following modules on the DS chassis:

Cable J1 to Cable Driver AT12 at location 32.

Cable J2 to Cable Driver/Receiver AT11 at location 30.

Cable J3 to Line Receiver AT10 at location 28.

Cable J4 to Cable Driver/Receiver AT17 at location 26.

Table A1-3 is an I/O signal location chart on which is listed the name and location of each signal that appears at the input and output terminals of the logic modules to which the interface cables are attached. Connectors P2 and P3 consist of the paired I/O terminals; connector P1, located at the opposite end of the module, plugs directly into the module receptacle on the DS chassis, at the indicated location.

The device subcontroller is a subassembly of the device controller. Receptacles for the DS logic modules are physically located on one of the DC chassis.

A1-7 FUNCTIONAL DESCRIPTION

The DS functions as a device subcontroller, enabling the transfer of data between the IOP and a single device, via the device controller.

Device selection is controlled by eight toggle switches. The selection switches are mounted on an LT26 Switch Comparator module, located in slot 24 on the DS chassis.

Communication between the IOP and the DS is established through transmission lines that exhibit the characteristics described in Table A1-2. Signal levels at the transmission lines are characterized as follows:

(a) A logical ONE (1) is transmitted at a voltage level of +2 volts dc, indicating low impedance at the cable driver output.

(b) A logical ZERO (0) is transmitted at a voltage level of 0 volts dc, indicating high impedance at the cable driver output.

The circuit configuration of the switch comparator module (LT26) enables an eight-bit address to be generated and applied to the function response lines during AIO and ASC functions. The comparator module also provides the required logic to allow the contents of the data lines to be compared with the eight switch settings during input and output operations.

Table A1-3. DS I/O Signal Locations

I/O Connector (P2, P3) Terminals	Module AT12 Location 32			Module AT11 Location 30			Module AT10 Location 28			Module AT17 Location 26		
	Cable J1	Connector P1		Cable J2	Connector P1		Cable J3	Connector P1		Cable J4	Connector P1	
	Signal	Signal	Pin	Signal	Signal	Pin	Signal	Signal	Pin	Signal	Signal	Pin
01, A	FR7	FR7D	02	DA7	DA7D	02	RST	RSTR	06	HPI	HPID	35
					DA7R	06					HPIR	06
02, B	FR6	FR6D	01	DA6	DA6D	01	CL1	CL1R	04	HPS	HPSD	33
					DA6R	04					HPSR	04
03, C	FR5	FR5D	09	DA5	DA5D	09	ES	ESR	10			
					DA5R	10						
04, D	FR4	FR4D	03	DA4	DA4D	03	RSA	RSAR	08	(4)AVI	AVIR	08
					DA4R	08				(D)AVO	AVOD	29
05, E	FR3	FR3D	12	DA3	DA3D	12	SIO	SIOR	13			
					DA3R	13					INI	07
06, F	FR2	FR2D	15	DA2	DA2D	15	HIO	HIOR	18			
					DA2R	18					NINI	15
07, G	FR1	FR1D	19	DA1	DA1D	19	TIO	TIOR	20			
					DA1R	20					INC	11
08, H	FR0	FR0D	23	DA0	DA0D	23	TDV	TDVR	22			
					DA0R	22					NINC	09
09, K	RS	RSD	25	DAP	DAPD	25	AIO	AIOR	27			
					DAPR	27					PT18S	17
10, L	IOR	IORD	33	ED	EDD	33	ASC	ASCR	34			
					EDR	34						
11, M	FSL	FSLD	35	PC	PCD	35	FS	FSR	36			
12, N				DOR	DORD	37						
13, P	IC	ICD	39	SC	SCD	39						

In response to a service request from the device controller, the DS establishes communication paths between the IOP and the DC. When the service connection is verified by the DS, data transfer begins.

The DS receives an interrupt call from the DC when an interrupt is required, and sends the call to the CPU. The DS receives an acknowledgment from the CPU and supplies the DC with the information required to implement the appropriate function.

A1-8 POWER REQUIREMENTS

The nine logic modules that constitute the DS require the following dc operating power:

+8v at 1.6 amps

-8v at 0.3 amps

+4v at 2.0 amps

A-II. OPERATION AND PROGRAMMING

A2-1 GENERAL OPERATING INFORMATION

The nine-module portion of the device subcontroller when used in conjunction with a device controller contains the required interface logic for effecting a two-way information exchange between the input/output processor (IOP) of an XDS Sigma computer and a selected peripheral device, via applicable circuits in the device controller.

During an I/O operation, logic circuits in the DS are used to implement signal transfer functions in response to requests from the IOP and the device controller. Signal flow between the IOP and the controlled device is shown in simplified form in figure A2-1.

Information contained in this section includes descriptions of functions performed by the DS, relating each function to the appropriate I/O operation. Significant signals are listed, and the functional application of each signal is described. Also described in this section are the applications and implementation of I/O instructions that initiate and control the interchange of information within the system.

A2-2 INITIAL OPERATION

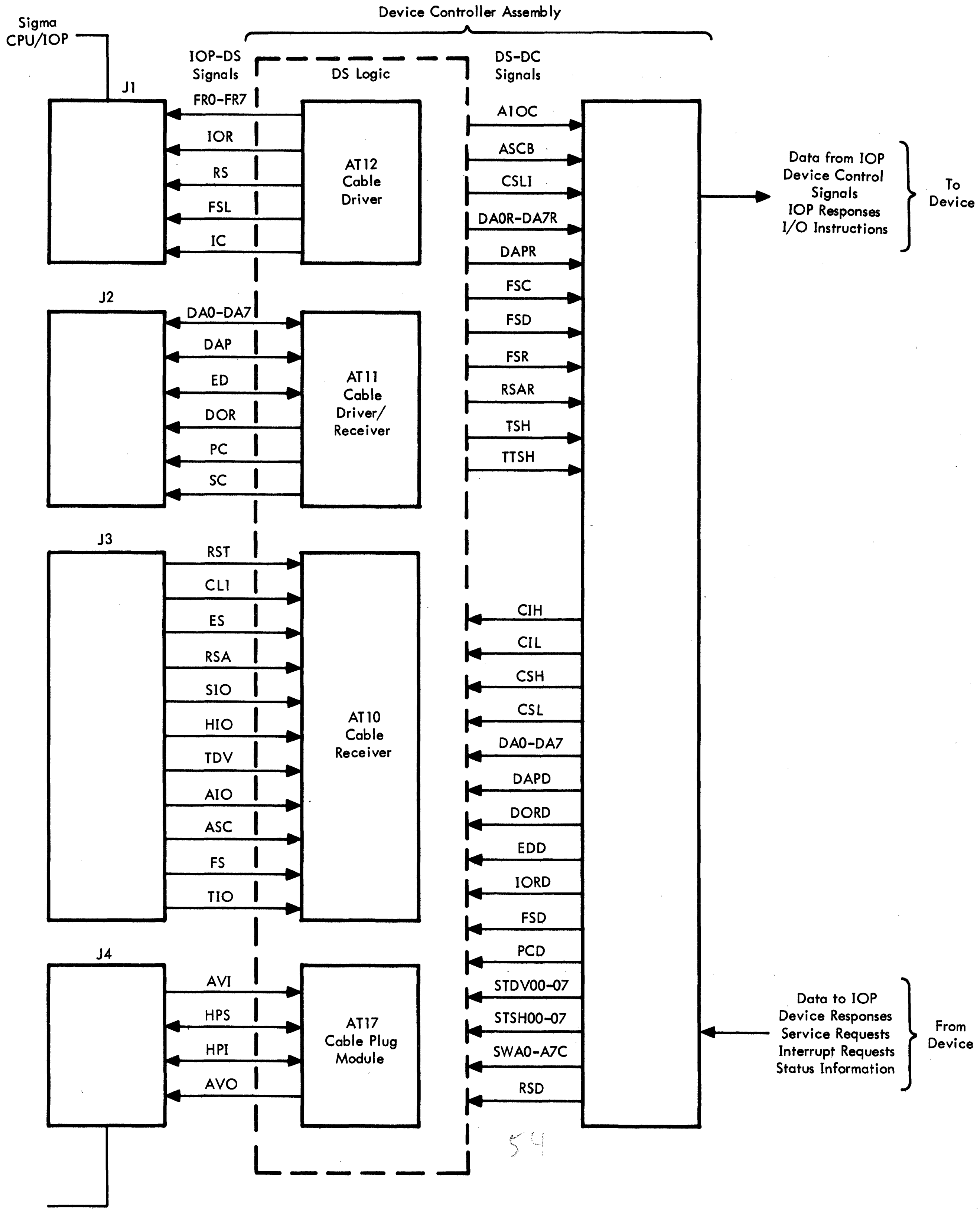
Preparatory to the transfer of information, signal paths must be established between the IOP and the device controller. A toggle switch, in conjunction with a pair of sequence relays, enables the required IOP-DC interconnection to be effected, and allows power to be applied to the device controller in a transient-free manner.

A2-3 ON-OFF SEQUENCE CONTROL

During ON-OFF sequencing, power to the device controller is applied through contacts on the sequence relays, as described in paragraph A2-2. Relay contact positions are determined by the state (energized or deenergized) of the relay coil, which is in series with the toggle switch. The configuration of the sequence relay circuit is controlled by the remote toggle switch, as shown in figure A2-2.

A2-4 CONNECT/DISCONNECT TIMING

When the DS is to be connected to the IOP interface, the sequence relay control switch must be ON and a ground source must be applied to the connect/disconnect circuit. The switch is positioned to OFF to disconnect the DS from the IOP. The order in which the connect/disconnect signals are applied is illustrated in the timing diagram in figure A2-3.



Note: Signals represented mnemonically in this illustration are defined in Table 2-1

Figure A2-1. Interface Signal Paths

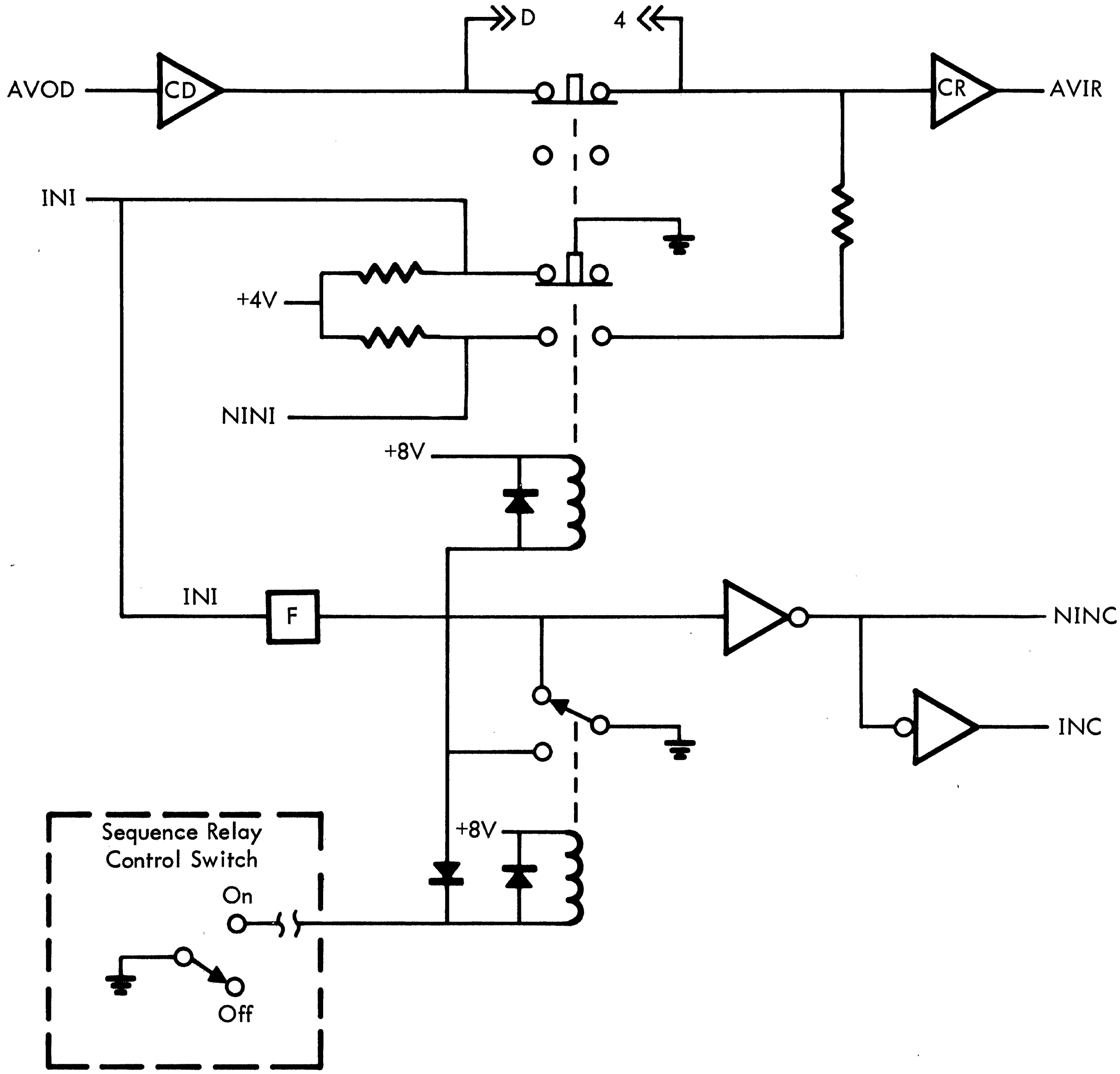
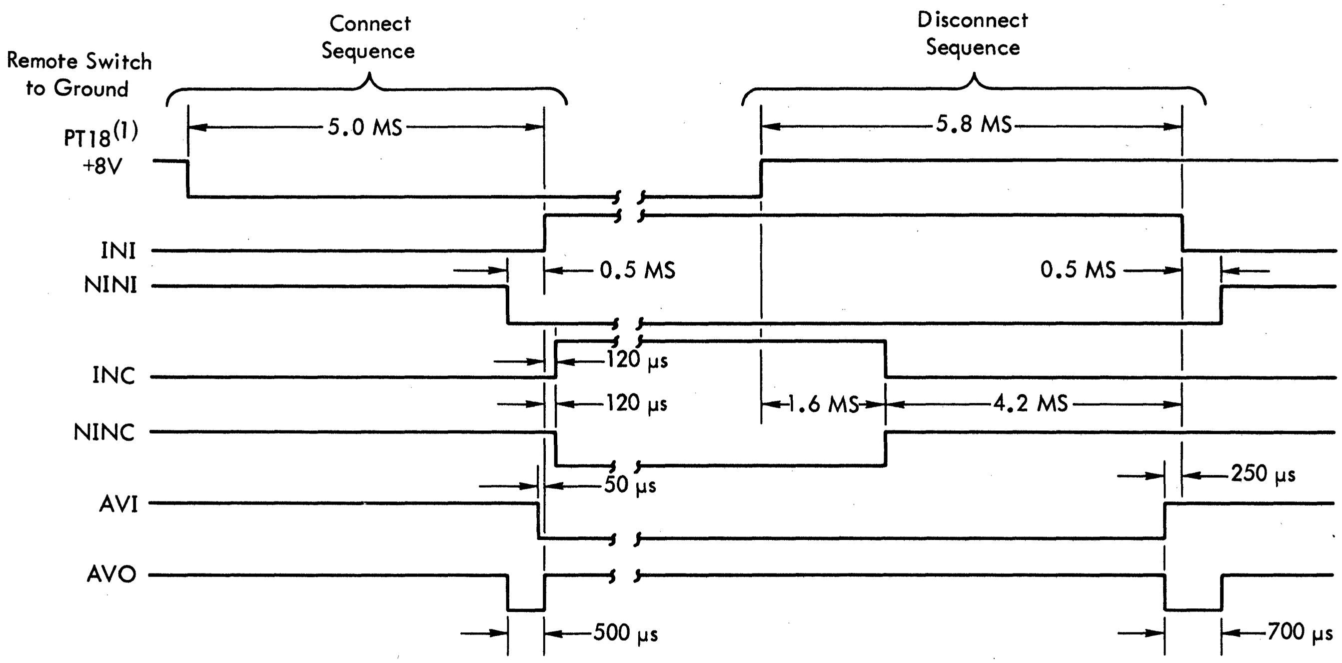


Figure A2-2. ON-OFF Sequence Circuit Configuration

A2-5 CONNECT/DISCONNECT PROCEDURE

The connect procedure is executed in the following sequential manner:

(a) As indicated in figure A2-3, signal NINI is grounded through a set of sequence relay contacts about 4.5 milliseconds after the control switch is placed in the ON position.



Note: (1) PT18 is controlled by switch on LT25 Logic Module, Slot 23.

Figure A2-3. Connect/Disconnect Sequence Timing Diagram

(b) Signals AVI and AVO are shorted together through a set of normally-closed contacts as long as the relay coil remains deenergized. The short is removed about 450 microseconds after NINI is grounded.

(c) Signal INI becomes True about 50 microseconds later or about 5.0 milliseconds after the toggle switch is turned ON.

(d) Approximately 50 microseconds after INI reaches the True state, signal INC becomes True and signal NINC is grounded.

When signals INI and INC are both True, the DC is connected to the IOP interface and the service call, interrupt call, and cable driver lines become active.

To disconnect the DS from the IOP, the sequence relay control switch is placed in the OFF position. This action removes the ground return for the sequence relay coils, causing the relays to become deenergized. The following sequence of events, timed as indicated in figure A2-3, occurs when the control switch is turned OFF:

(a) Approximately 1.6 milliseconds after the switch is turned OFF, all service and interrupt calls to the IOP are inhibited. This effect is achieved by grounding signal INC and allowing NINC to go True through relay and transistor logic.

(b) About 3.95 milliseconds after INC is grounded, signals AVI and AVO are shorted together through a set of sequence relay contacts.

(c) Signal INI is grounded through a set of sequence relay contacts about 4.2 milliseconds after INC is grounded.

(d) About 0.5 milliseconds after INI is grounded, signal NINI is allowed to become True.

The grounding of signal INI drives the inputs of all the DS cable drivers False, effectively isolating the IOP from the device controller. At this time, signal lines AVI and AVO are shorted together, enabling the DS to be physically connected to the priority cable of the IOP interface without interfering with the operation of the priority cable.

A2-6 INTERFACE SIGNALS

The origin, destination, and function of each signal that affects the transfer of information between the IOP, DS, and DC are defined in Table A2-1.

Table A2-1. System Interface Signals

Signal Name	Signal Path		Signal Description and Application
	From	To	
AIO	IOP	DS	Acknowledge Interrupt Function Indicator - IOP/DC Interface
AIOC	DS	DC	Defines period when the controller should apply interrupt status, condition codes, and device number to IOP. Also can be used in conjunction with FSR (trailing edge) to reset interrupt call request CIL and CIH.
NAIOC	DS	DC	Inverse of AIOC
AIOM	DS	DS	Indicates that an AIO will be accepted when AVIR is received.
NAIOM	DS	DS	Inverse of AIOM
AIOR	DS	DS	Output from AIO Receiver
NAIOR	DS	DS	Inverse of AIOR
ASC	IOP	DS	Acknowledge Service Call Function Indicator
ASCB	DS	DS	True when ASC occurs and device has priority. When ASCB is True, flip-flop FSC is set by falling edge of signal FSR.

Table A2-1. System Interface Signals (Cont)

Signal Name	Signal Path		Signal Description and Application
	From	To	
ASCM	DS	DS	Indicates that an ASC will be accepted when AVIR is received.
NASCM	DS	DS	Inverse of ASCM
ASCR	DS	DS	Output of ASC receiver
NASCR	DS	DS	Inverse of ASCR
AVI	IOP	DS	Priority signal, Available Input, routed sequentially through each controller from highest priority to lowest priority. This signal, when received by a controller, indicates that all higher priority controllers have not accepted the Function Indicator.
AVIR	DS	DC	Output of AVI receiver
AVO	DS	IOP	Priority signal, Available Output, which is generated when a Function, is not accepted. AVO becomes AVI into the next lower priority controller.
AVOD	DS	DS	Input to AVO cable driver. Cable driver output is shorted to AVI receiver input when controller power is off.
BSYC	DS	DS	Defines period, during ASC or AIO function, when the device address is placed on function response lines FR0-FR7 by the DS.
CIH	DC	DS	CIH is supplied by the device controller, when a high priority interrupt is required.
CIL	DC	DS	CIL is supplied by the controller when a high or low priority Interrupt Call is required.
CL1	IOP	DS	1 mHz clock (500 nsec high, 500 nsec low)
CL1R	DS	DC	Output of CL1 receiver
CSH	DC	DS	CSH is supplied by the controller when a high priority service call is required.
CSL	DC	DS	CSL is supplied by the controller when a high or low priority Service Call is required.
CSLI	DS	IOP	NFSC with delayed falling edge

Table A2-1. System Interface Signals (Cont)

Signal Name	Signal Path From	To	Signal Description and Application
DA0-DA7	IOP, DS	DS, IOP	Bidirectional data lines between the I/O system and the DS
DA0D-DA7D	DS	DS	Input to DA0-DA7 cable drivers
DA0R-DA7R	DS	DS	Output of DA0-DA7 receivers. These lines handle Order Output, Terminal Order, and data transfer from IOP.
NDA0R-NDA7R	DC	DS	Inverse of DA0R-DA7R
DAP	IOP, DS	DS, IOP	Bidirectional ODD parity lines between the IOP and DS
DAPD	DC	DS	Data parity input to DAP cable driver
DAPR	DS	DC	Output of DAP receiver
DCA	DS	DS	Indicates that the contents of DA0-DA3 equal the toggle switch outputs SWA0-SWA3. This signal is clamped false when FSC is true.
NDCA	DS	DS	Inverse of DCA
DCA47	DS	DS	Indicates that the contents of DA4-DA7 equals the toggle switch outputs SWA4-SWA7.
DOR	DC	IOP	DATA/ORDER line during service, and condition code during function acknowledgment. Line is high when Order is active.
DORD	DC	DS	Input to DOR cable driver
DORR	DS	DC	Output of DOR receiver
ED	IOP, DS	DS, IOP	Bidirectional End Data line. Indicates last data or order byte is being transmitted.
EDD	DC	DS	Input to ED cable driver
EDR	DS	DC	Output of ED receiver
ES	IOP	DS	End Service line. Indicates last byte of service is being transmitted. This signal is used to reset flip-flop FSC.
ESR	DS	DC	Output of ES receiver

Table A2-1. System Interface Signals (Cont)

Signal Name	Signal Path From	Signal Path To	Signal Description and Application
FR0-FR7	DS	IOP	Function Response lines. Status information is applied to these lines during SIO, HIO, TIO, and TDV functions with the "device number" being applied during AIO and ASC functions.
FR0D-FR7D	DS	DS	Input to FR0-FR7 cable drivers
FS	IOP	DS	Function Strobe. Indicates that the Function Indicator lines are stable.
FSD	DC	DS	Function Strobe delayed "as required" by the controller.
FSR	DS	DC	Output of FS receiver
FSRC	DS	DC	Defines FSR · NFSC
FSL	DS	IOP	Function Strobe Leading Acknowledge. Indicates that Function Response lines, Condition Code lines, etc. may be strobed by the IOP.
FSLD	DS	DS	Input to FSL cable driver
FSC	DS	DS	Service Connect flip-flop. Indicates, when set, that the controller is connected for service.
NFSC	DS	DS	Inverse of FSC
FSCL	DS	DS	Extends RSARC until FSC falls
HIO	IOP	DS	HIO Function Indicator (Halt I/O)
HIOR	DS	DC	Output of HIO receiver
HPI	DS	IOP	High Priority Interrupt. This line is high if any controller is requesting high priority interrupt.
HPID	DS	DS	Input to HPI cable driver
HPIL	DS	DS	Latch circuit that holds the condition of HPI during an AIO function.
HPIR	DS	DS	Output of HPI receiver
NHPIL	DS	DS	Inverse of HPIL

Table A2-1. System Interface Signals (Cont)

Signal Name	Signal Path		Signal Description and Application
	From	To	
HPS	DS	IOP	High Priority Service. This line is high if any controller is requesting high priority service.
HPSD	DS	DS	Input to HPS cable driver
HPSL	DS	DS	Latch circuit that holds the condition of HPS during an ASC function.
HPSR	DS	DS	Output of HPS receiver
NHPSL	DS	DS	Inverse of HPSL
IC	DS	IOP	Interrupt Call. This line is high if any controller is generating an Interrupt Call.
ICD	DC	DS	Input to IC cable driver
INC	DS	DC	Inhibits new service and interrupt calls through sequence relay contacts when controller power is Off.
NINC	DS	DC	Inverse of INC
INI	DS	DS	Clamped to ground through sequence relay contacts when controller power is Off. High when DC power is On.
NINI	DS	DS	Clamped to ground through sequence relay contacts when DC power is On. High when DC power is Off.
IOR	DS	IOP	I/O line during service and condition code during function acknowledgment. Line is high when Output is active.
IORD	DC	DS	Input to IOR cable driver
LIH	DS	DS	Latch circuit that holds the condition of CIH during the AIO function.
LIL	DS	DS	Latch circuit that holds the condition of CIL during the AIO function.
LSH	DS	DS	Latch circuit that holds the condition of CSH during the ASC function.
LSL	DS	DS	Latch circuit that holds the condition of CSL during the ASC function.

Table A2-1. System Interface Signals (Cont)

Signal Name	Signal Path From	Signal Path To	Signal Description and Application
N008	PS	DS	Minus 8-volt line
PC	DS	IOP	Parity Check line. If high during a Request Strobe, the IOP will check the Data lines, DA0-DA7, and DAP for correct ODD parity.
PCD	DC	DS	Input to PC cable driver
PT18	DC	DS	Represents a signal from controller that opens a ground return line prior to any voltages decaying below a safe limit.
PT18S	DS	DS	Represents the term, PT18, after being routed through a toggle switch in the DS. This permits manual simulation of the power OFF condition. PT18S is High if power supply fails. When PT18S is high, cable driver inputs are grounded and peripheral system is disconnected from I/O system.
RS	DS	IOP	Request Strobe. Indicates that associated signal lines are stable and requests data transfer between IOP and device during a service cycle.
RSA	IOP	DS	Request Strobe Acknowledge indicates that RS may be dropped. RSA terminates after each byte exchange during a service cycle.
RSAR	DS	DC	Output of RSA Receiver. Conveys IOP response to request strobe.
RSARC	DS	DC	Repeats RSAR, except at End Service, at which time RSARC latches until FSC resets.
RSD	DC	DS	Input to RS cable driver
RST	IOP	DS	I/O Reset line. The controller must initialize all circuits when this signal is high.
RSTR	DS	DC	Output of RST receiver
NRSTR	DS	DC	Inverse of RSTR
SC	DS	IOP	Service Call. This line is high if any controller is generating a Service Call.
SCD	DS	DS	Input to SC cable driver

Table A2-1. System Interface Signals (Cont)

Signal Name	Signal Path From	To	Signal Description and Application
SCR	DS	DS	Output of SC receiver
SIO	IOP	DS	SIO Function Indicator (Start I/O)
SIOR	DS	DS	Output of SIO receiver
STDV00-STDV07	DC	DS	Status lines provided by the controller during TDV function.
STSH00-STSH07	DC	DS	Status lines provided by controller during TIO, SIO, HIO functions.
SWA0-SWA7	DC	DS	Output of the eight "device number" toggle switches applied to response lines during AIO and ASC functions.
NSWA0-NSWA7	DC	DS	Inverse of SWA0-SWA7
TDV	IOP	DS	TDV Function Indicator (Test Device)
TDVR	DS	DS	Output of TDV receiver
TIO	IOP	DS	TIO Function Indicator (Test I/O)
TIOR	DS	DS	Output of TIO receiver
TSH	DS	DS	Defines DCA (TIOR + SIOR + HIOR)
TTSH	DS	DC	Defines TIOR + TDVR + SIOR + HIOR
Abbreviations:	DC	Device Controller	
	DS	Device Subcontroller	
	IOP	Input/Output Processor (or CPU in the absence of an IOP)	
	PS	Power Supply	

A2-7 INPUT/OUTPUT CHARACTERISTICS

The I/O interface, which forms the communication link between the computer input/output processor (IOP) and the device controller, is compatible with the XDS Sigma Series computers. One interface, providing an eight-bit data path, is associated with each IOP in the system.

A device controller, of which the DS is a part, is connected between the IOP interface and each peripheral device. As many as 32 device controllers may be connected to one IOP interface by time-sharing the eight-bit data path. When more than one controller is used in the system, the first DC is connected directly to the IOP interface, while the second controller is connected to the first in a parallel manner. Subsequent controllers are added in the same manner to form a parallel chain, thereby requiring only one set of interconnecting cables between the controller-device network and the IOP interface.

In the XDS Sigma 2 computer the IOP is physically integrated within the central processing unit (CPU), and is capable of maintaining 20 simultaneously active communication channels. The basic Sigma 2 computer word consists of 16 bits, which are divisible into two eight-bit bytes. Two words may be combined to form a 32-bit doubleword, which is accessed by the address of its most significant word.

XDS computers Sigma 5 and Sigma 7 are each capable of maintaining as many as 256 simultaneously active communication channels. The basic computer word in both the Sigma 5 and the Sigma 7 consists of 32 bits, which are divisible into two 16-bit halfwords or four 8-bit bytes. Two words may be combined to form a 64-bit doubleword, with the most significant word occupying bit positions 0 through 31.

The operational descriptions in this manual are especially applicable to a system in which a "single device" controller is interfaced with an XDS computer. References to the IOP apply to the portion of the CPU in which IOP functions are performed.

A2-8 COMMAND DOUBLEWORDS

During an input/output operation, the I/O channel registers contain an I/O Control Doubleword (IOCD) which includes an address, byte count, flags, and in the Sigma 5/7, an order. Sigma 2 orders are in the data list.

The word or byte address designates the memory location for the next byte of data.

The byte count indicates the number of bytes to be transmitted in the I/O operation. Refer to the appropriate computer reference manual for flag meaning and usage.

A2-9 OPERATIONAL STATUS BYTE FORMAT

The peripheral device associated with the controller is assigned a number manually selected by a switch within the controller. The device number identifies the selected device, and defines the I/O channel that controls the device.

A2-10 ADDRESS SELECTION

Eight toggle switches on an LT26 Switch Comparator module are used for device controller address selection, while two equivalent detection circuits compare the switch settings against the IOP output address during SIO, HIO, TIO, and TDV operations. Switch locations are shown in figure A2-4.

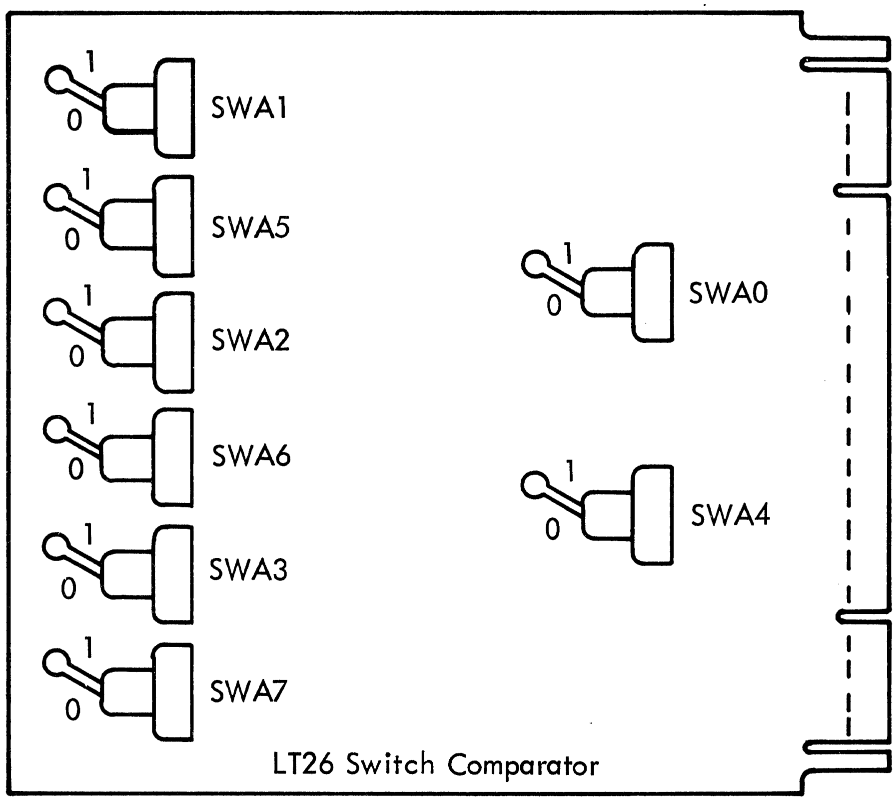


Figure A2-4. Comparator Module LT26, Switch Locations

A2-11 BIT CODING SUMMARY

The allocation of bit positions zero through seven of the I/O channel register during data exchange functions, is summarized in Table A2-2.

A2-12 DEVICE ORDERS

When a device is started for an input/output operation, the device requests an order from the I/O system. A device order consists of an eight-bit byte, which is transmitted to the device under control of the channel to which the device is attached. Orders that the device may accept include Write, Read, Control, Sense, Read Backward, Transfer in Channel, and Stop. The device order coding format is shown in Table A2-3. The following are device order operational descriptions.

Write. The Write order causes the DC to initiate an output operation. In response to controller output requests, the IOP transmits bytes from memory to the device. The output operation normally continues until data chaining is completed and the byte count is reduced to zero.

Table A2-2. Bit Codings for Data Exchanges

Function/Instruction	I/O* Line	I/O Bit Positions 0	1	2	3	4	5	6	7	DOR (NCC1)	IOR (NCC2)
SIO, HIO, TIO, TDV	DA	Device controller address									
SIO, HIO, TIO	FR	Interrupt pending	00 = D ready 01 = D not operational 10 = D unavailable 11 = D busy		Device automatic	Device unusual end (last operation)	00 = DC ready 01 = DC not operational 10 = DC unavailable 11 = DC busy		0	Address recognition	SIO: SIO successful HIO: DC was not busy when HIO occurred TIO: SIO can be accepted
TDV	FR	Rate error								Address recognition	Abnormal condition does not exist
AIO	DA		Device end							AIO acknowledged	DC error or fault does not exist
AIO	FR	Device controller address									
Order in	DA	Trans. error	Incorrect length	Chaining modifier	Channel end	Unusual end				1	0
Terminal order	DA	Interrupt	Count done	Command chain	IOP halt						
Order out (even command word bits 0-7) Control	DA	M	M	M	M	M	M	1	1	1	1
Write		M	M	M	M	M	M	0	1		
Read		M	M	M	M	M	M	1	0		
Read back		M	M	M	M	1	1	0	0		
Sense		M	M	M	M	0	1	0	0		
TCH		X	X	X	X	1	0	0	0		
Stop		1	0	0	0	0	0	0	0		
Odd command (word bits 0-7)		Data chain	Interrupt at count = 0	Command chain	Interrupt at channel end	Halt on transmission error	Interrupt at unusual end	Suppress incorrect length	Skip		

*DA = data lines; FR = function response lines. Status supplied by the device controller on the function response lines and data lines must remain stable while function strobe acknowledge is true.

Read. The Read order causes the device to initiate an input operation, during which bytes are transmitted from the device to memory. Reading continues until the device generates channel end or the byte count is reduced to zero.

Read Backward. The Read Backward order, which can be executed on certain Sigma peripheral devices, causes the initiating device to start operation in a backward direction, transmitting bytes in reverse order. The backward-transmitted bytes are stored in memory in an ascending order, similar to the transmission that results from a Read order. Thus, the record appears in memory in reverse sequence from its originally transmitted order.

Control. Special device operations are initiated by the Control order. For some operations, the Control order specifies the entire operation. During a magnetic tape operation, for example, the Control order initiates rewind, backspace record, backspace file, spare record, and similar operations. Individual functions are specified by the unique modifier bits of the Control order.

Table A2-3. Device Order Coding Format

	Data Lines							
	DA0R	DA1R	DA2R	DA3R	DA4R	DA5R	DA6R	DA7R
Write	M	M	M	M	M	M	0	1
Read	M	M	M	M	M	M	1	0
Control	M	M	M	M	M	M	1	1
Sense	M	M	M	M	0	1	0	0
Read Backward	M	M	M	M	1	1	0	0

Definition:

M = Modifier unique to DC

Sense. Upon receipt of a Sense order, the device transmits one or more bytes of information describing its current operational status. These status bytes are stored in memory. The type of status information transmitted is a function of the device.

A2-13 DEVICE INTERRUPTS

All device controllers are capable of generating device interrupts. The execution of an AIO instruction causes the device with the highest priority to be identified to the program. The device generates interrupts upon IOP request or DC request.

A2-14 INPUT/OUTPUT INSTRUCTIONS

The computer CPU initiates and controls I/O operations by using instructions SIO, TIO, TDV, HIO, and AIO. With the exception of AIO, all I/O instructions require a device number to address the I/O device being controlled. The result of each instruction is shown by overflow and carry indicators on the Sigma 2 computer control panel, and CC1 and CC2 indicators on the Sigma 5/7 computer control panel.

A2-15 SIO INSTRUCTION

The SIO (Start Input/Output) instruction initiates an input or output operation with the device selected by the I/O address. The overflow or CC1 indicator is set to 1 if the device number is not recognized by the I/O system. The carry or CC2 indicator is set to 1 if the SIO instruction cannot be accepted by the selected device. When the number is recognized by a device, status information is returned from the device. The significance of the results displayed on the overflow/CC1 and carry/CC2 indicators during an SIO instruction is explained in Table A2-4.

Table A2-4. Status Indications for SIO

Indicator Display		Significance of Indicator Display
Overflow CC1	Carry CC2	
0	0	I/O address recognized and SIO accepted
0	1	I/O address recognized; SIO not accepted
1	1	I/O address not recognized

A2-16 TIO INSTRUCTION

Instruction TIO (Test Input/Output) elicits similar responses from the device as does SIO, but the device is neither started nor advanced to the busy state. Significance of the indicator display that results from TIO is explained in Table A2-5. When the device number is recognized, the device status byte is returned.

Table A2-5. Status Indications for TIO

Indicator Display		Significance of Indicator Display
Overflow CC1	Carry CC2	
0	0	I/O address recognized and SIO can be accepted
0	1	I/O address recognized; SIO cannot be accepted
1	1	I/O address not recognized

A2-17 TDV INSTRUCTION

Instruction TDV (Test Device) is used to obtain specific information about the device. The device, upon recognizing the device number, returns its device status byte. The significance of TDV indications is detailed in Table A2-6.

A2-18 HIO INSTRUCTION

Instruction HIO (Halt Input/Output) causes the device identified to stop operating immediately, without regard for the type of program being executed at the time. Device recognition causes status information to be sent from the device. The significance of each indication for HIO is explained in Table A2-7.

Table A2-6. Status Indications for TDV

Indicator Display		Significance of Indicator Display
Overflow CC1	Carry CC2	
0	0	I/O address recognized
0	1	I/O address recognized and device-dependent condition exists
1	1	I/O address not recognized

Table A2-7. Status Indications for HIO

Indicator Display		Significance of Indicator Display
Overflow CC1	Carry CC2	
0	0	I/O address recognized and DC not busy
0	1	I/O address recognized and DC busy at time of halt
1	1	I/O address not recognized

A2-19 AIO INSTRUCTION

Instruction AIO (Acknowledge Input/Output Interrupt) is used to recognize an interrupt generated by an I/O device. In response to AIO, the highest-priority device identifies itself and returns both its status and its device number. If interrupts are pending, the highest-priority device clears its pending interrupt and the device status and device number is returned. The significance of the display exhibited on the status indicators for AIO is explained in Table A2-8.

Table A2-8. Status Indications for AIO

Indicator Display		Significance of Indicator Display
Overflow CC1	Carry CC2	
0	0	Normal interrupt recognition
0	1	Unusual interrupt recognition
1	1	No interrupt recognition

A2-20 I/O STATUS INFORMATION

The distribution and state of bits in positions 0 through 7 device status byte indicate the operational status of the device controller and the peripheral device during the execution of the five input and output instructions.

A2-21 STATUS INDICATORS

The status indicators, located on the Sigma 2 control panel, and CC1 and CC2 indicators, located on the Sigma 5/7 control panel, are set to display the system response to the current I/O instruction.

A2-22 DEVICE STATUS BYTE

When correlation exists between the device number programmed and a peripheral device, the Device Status Byte of the selected device is returned.

The AIO instruction does not require the device number because a function of this instruction is to obtain the number of the device that triggered the I/O interrupt level.

A2-23 Function of Device Status Byte

The current operation state of the device and the device controller is indicated by the position and state of bits within the eight-bit Device Status Byte. Conditions indicated by the various bit allocations are defined in Table A2-9.

A2-24 Significance of Status Indicators

For instructions SIO, TIO, and HIO the status indicators have the following significance:

(a) Device Interrupt Pending. Bit 0 indicates by a 1 (true) or a 0 (false) whether the device has generated an interrupt signal that has not yet been acknowledged. A new I/O operation cannot be initiated on the device until the pending interrupt signal has been acknowledged by means of an AIO instruction, or until the device has been reset as the result of an HIO instruction.

(b) Device Condition. Bits 1 and 2 define which of the four possible conditions the device is in, while bits 5 and 6 provide the same information about the device controller. In a single-device controller, the device condition and the controller condition are identical. If the device and controller are ready and no device interrupt is pending, an SIO instruction can be accepted and acted upon. If the device and controller are not operational, an SIO instruction cannot be accepted and operator intervention is required to initiate an operation. The indication that the device

Table A2-9. Device Status Byte Bit Allocation

Input/Output Instruction	Bit Position and State 0	1	2	3	4	5	6	7	Device and Controller Status Indication
SIO, HIO, TIO	1	-	-	-	-	-	-	-	Device interrupt pending
	-	0	0	-	-	-	-	-	Device ready
	-	0	1	-	-	-	-	-	Device not operational
	-	1	0	-	-	-	-	-	Device unavailable
	-	1	1	-	-	-	-	-	Device busy
	-	-	-	0	-	-	-	-	Device Manual
	-	-	-	1	-	-	-	-	Device Automatic
	-	-	-	-	1	-	-	-	Device unusual end
	-	-	-	-	-	0	0	-	Device controller ready
	-	-	-	-	-	0	1	-	Device controller not operational
	-	-	-	-	-	1	0	-	Device controller unavailable
	-	-	-	-	-	1	1	-	Device controller busy
SIO, HIO, TIO	-	-	-	-	-	-	-	-	Unassigned
TDV, AIO	1	-	-	-	-	-	-	-	Unique to the Selected Peripheral Device
	-	1	-	-	-	-	-	-	
	-	-	1	-	-	-	-	-	
	-	-	-	1	-	-	-	-	
	-	-	-	-	1	-	-	-	
	-	-	-	-	-	1	-	-	
	-	-	-	-	-	-	1	-	
TDV, AIO	-	-	-	-	-	-	-	1	

and controller are busy denotes an SIO instruction has been accepted and the ensuing I/O operations has not been completed.

(c) Device Mode. Bit 3, the mode status indicator, is 1 if the device has been cleared for operation and the START switch has been actuated to place the device in the automatic mode. A mode status indication of 0 denotes the device is in the manual mode and operator intervention is required to effect operation. A device that is ready can accept an

SIO instruction while in the manual mode, but operation cannot begin until the device is placed in the automatic mode.

(d) Unusual End Termination. Bit 4 is set to 1 if the previous operation on the peripheral device resulted in an unusual end; otherwise, bit 4 is reset to 0.

A2-25 Device Number Loading

In addition to the Status returned, instruction AIO causes the device number to be returned to identify the controller in question.

A2-26 INSTRUCTION IMPLEMENTATION IN DS

The DS contains nine logic modules. All functions required to transfer information between the Sigma IOP and a peripheral device are implemented extensively by logic circuits within the DS and DC.

A2-27 INPUT TO IOP VIA DATA LINES

The data lines are used to convey input data, Order In information, and interrupt acknowledgment signals to the IOP. Signals from the peripheral device and device controller are implemented within the DS and are strobed into appropriate data lines for transmission to the IOP.

A2-28 OUTPUT FROM IOP VIA DATA LINES

Data lines DA0 through DA7 may be used as desired for transmitting IOP output information to cable receivers. Receiver output lines DA0R through DA7R are also connected to address selection circuits on a comparator module.

A2-29 IOP INPUT VIA FUNCTION RESPONSE LINES

Start, Halt, and Test instructions are sent to the peripheral device through the DS, which is a part of the device controller. Instruction TIO asks for general I/O status information, while TDV is a request for status information from the device. Eight Function Response lines that are connected between the DS and the IOP deliver the requested status information from the device and the device controller to the IOP, via the DS.

A2-30 Controller Responses to SIO, HIO, and TIO

Instructions SIO, HIO, and TIO are sent to the device controller, causing the current interrupt status, device status, and device controller status to be reported to the IOP via the Function Response lines, FR0D-FR7D.

A2-31 Test Device Responses

When the IOP raises the test device function indicator, status information from the device is received by the DS. The DS gates this information onto the Function Response lines for transmission to the IOP.

A2-32 Responses from Selected Device

Outputs from eight device selection toggle switches on the comparator module are routed to a logic module LT24. Upon receipt of instruction AIO or ASC, the device-number comparator signals are strobed through Function Response lines to the IOP. Each device-number bit is assigned to a specific line for transmission to the IOP.

A2-33 TERMINATION OF I/O OPERATIONS

The device controller, which initiates input/output operations, also controls the termination of operations. Various conditions that will induce the controller to inhibit normal signal flow within the system are described in this subsection.

A2-34 Channel End

At the completion of the transfer phase of an operation, when the interchange of information between the IOP and the device has ceased, Channel End is reported to the IOP via an Order Input. The specific operation and type of device involved determine the time at which Channel End occurs. After Channel End, the device is usually ready to accept another cycle of instructions.

A2-35 Device End

The completion of an I/O operation at an I/O device causes Device End to be reported to the IOP by devices that do not have the capability to enter the ready state immediately after reporting Channel End, without command chaining. In this category are fully buffered devices that must remain Busy for a relatively long time after Channel End; and devices that must perform rewind, search, and similar control functions while logically disconnected from the associated control unit. Device End is reported to the IOP (CPU) by a device-generated interrupt call. When an interrupt call is generated at Device End, Bit 1 of the ensuing AIO status indicates Device End.

A2-36 Unusual End

When a device must leave the Busy state prematurely during an I/O operation, Unusual End occurs. This condition is reported to the IOP by an Order Input via a data line. Unusual End may also be sensed as status by instructions SIO, HIO, or TIO. Both the IOP and the I/O device are capable of initiating Unusual End.

The device initiates Unusual End as follows:

(a) An existing condition in the device or DC that warrants termination of the current I/O operation causes the device controller to inhibit succeeding Data In, Data Out, and Order Out requests.

(b) If data transfer has not begun when the unusual condition occurs, e.g., when an invalid order has been received, the controller immediately reports Unusual End and enters the Ready state.

(c) In the event data transfer has begun, the controller reports both Unusual End and Channel End, and enters the Ready state. The presence of a Command Chain bit is ignored at the Terminal Order following Channel End reporting.

(d) While Command Chaining, if the device must cease operation after Channel End has been reported, and before another Order has been requested, the device controller will report Unusual End and enter the Ready state.

The IOP presents an IOP Halt bit during a Terminal Order, to initiate Unusual End. The Halt bit causes the controller to perform the sequence described in steps (a) through (c) of the preceding paragraph.

If an error condition is sensed by the IOP during a Channel End Order Input, IOP Halt is presented during the following Terminal Order. The device controller does not report Unusual End to the IOP at this time, because all interrupts associated with Unusual End are presented by the IOP, coincident with IOP Halt. The device controller ignores the presence of Command Chaining and enters the Ready state.

A2-37 Instruction HIO

The receipt of an HIO Function Indicator causes a currently busy device to inhibit subsequent service requests and enter the Ready state. A status byte, presented to the CPU coincident with the HIO, reveals the operational status of the device. The Interrupt Pending condition is reset at this time.

A2-38 Input/Output Reset

When the I/O Reset signal is true, the device controller and devices are directed to clear all Service Calls, Error Indicators, and registers. In the absence of conditions which indicate a non-operational state, the controller and devices enter the Ready state, in anticipation of the next I/O operation.

A-III. PRINCIPLES OF OPERATION

A3-1 INTRODUCTION

This section contains logical descriptions of the functions performed by the DS in fulfilling its assignment as intermediary between the computer IOP and the device controller. Logic diagrams, timing diagrams, and data flow charts are integrated with the text to provide a comprehensive functional description of DS logic configurations. Symbology in the logic diagrams conforms to MIL-STD-806B, as modified by XDS. The overall logic diagram (figure A3-22) is located at the end of this section.

Circuit components mounted on the nine integrated circuit modules provide: (1) cable drivers and receivers to connect the eight-bit data path interface; (2) priority-determining logic for use during input/output and service call acknowledgments; (3) selection switches and associated logic for comparing switch outputs to the device number input from the IOP during SIO, HIO, TIO, and TDV operations; (4) a service-connect flip-flop; (5) the required relay logic for controlling interconnection between the DS and the IOP-DC interface during power ON, power OFF operations; and (6) standard gates, buffers, inverters, and special logic elements for implementing various DS functions.

A3-2 GENERAL I/O SEQUENCE

After a peripheral device has been started by the main computer, the general sequence in which information is transferred between the IOP and the device (via the DS and the device controller) is as follows:

(a) A service request is sent from the DC to the IOP.

(b) The IOP acknowledges the request and establishes lines of communication between the computer and the peripheral device by connecting to the device controller through the DS.

(c) While connected to the IOP, the DC requests (1) Data Out (DOUT), (2) Data In (DIN), (3) Order Out (OOUT), or (4) Order In (OIN) to define the type of transfer operation desired.

(d) During the period when the IOP and the DC are interconnected, up to four bytes of data or one byte of control information may be exchanged, in addition to a terminal order (TO) byte.

Information is transmitted between the DS and the IOP via three signal cables and one priority cable. At the DS, each I/O cable is connected to a logic module. A simplified diagram of logic functions performed within the DS is shown in figure A3-1, while figure A3-2 shows typical timing.

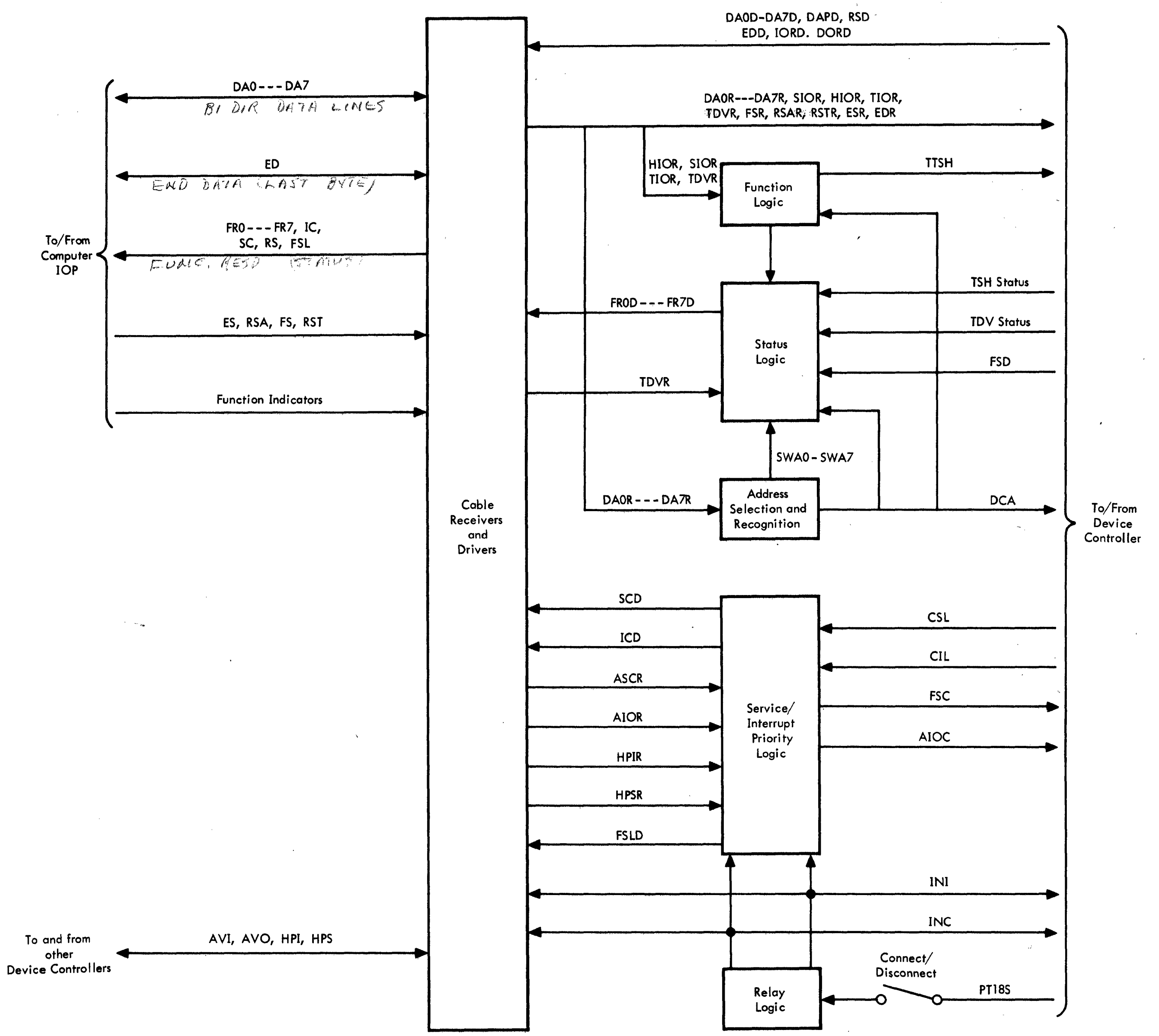


Figure A3-1. Device Subcontroller, Simplified Functional Block Diagram

A3-3. INTERFACE CONNECT LOGIC

The procedure for interconnecting the IOP and the device controller is described in Section A-II. As the timing diagram in figure A2-3 indicates, the controller is connected to the IOP interface when signals INI and INC become True. This condition allows the service call, interrupt call, and cable driver lines to become active.

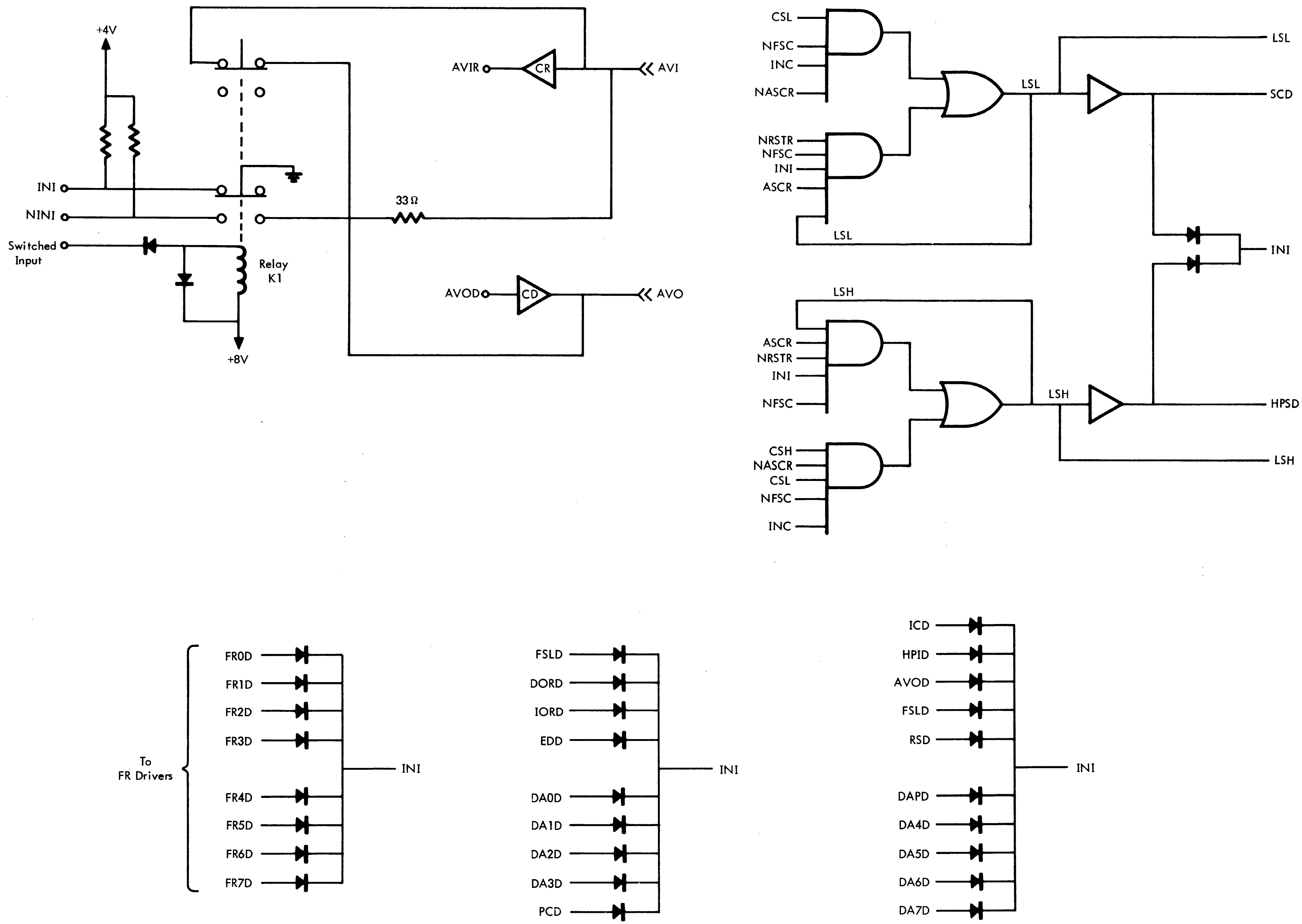


Figure A3-3. Circuit Implementation of Clamp Signal INI

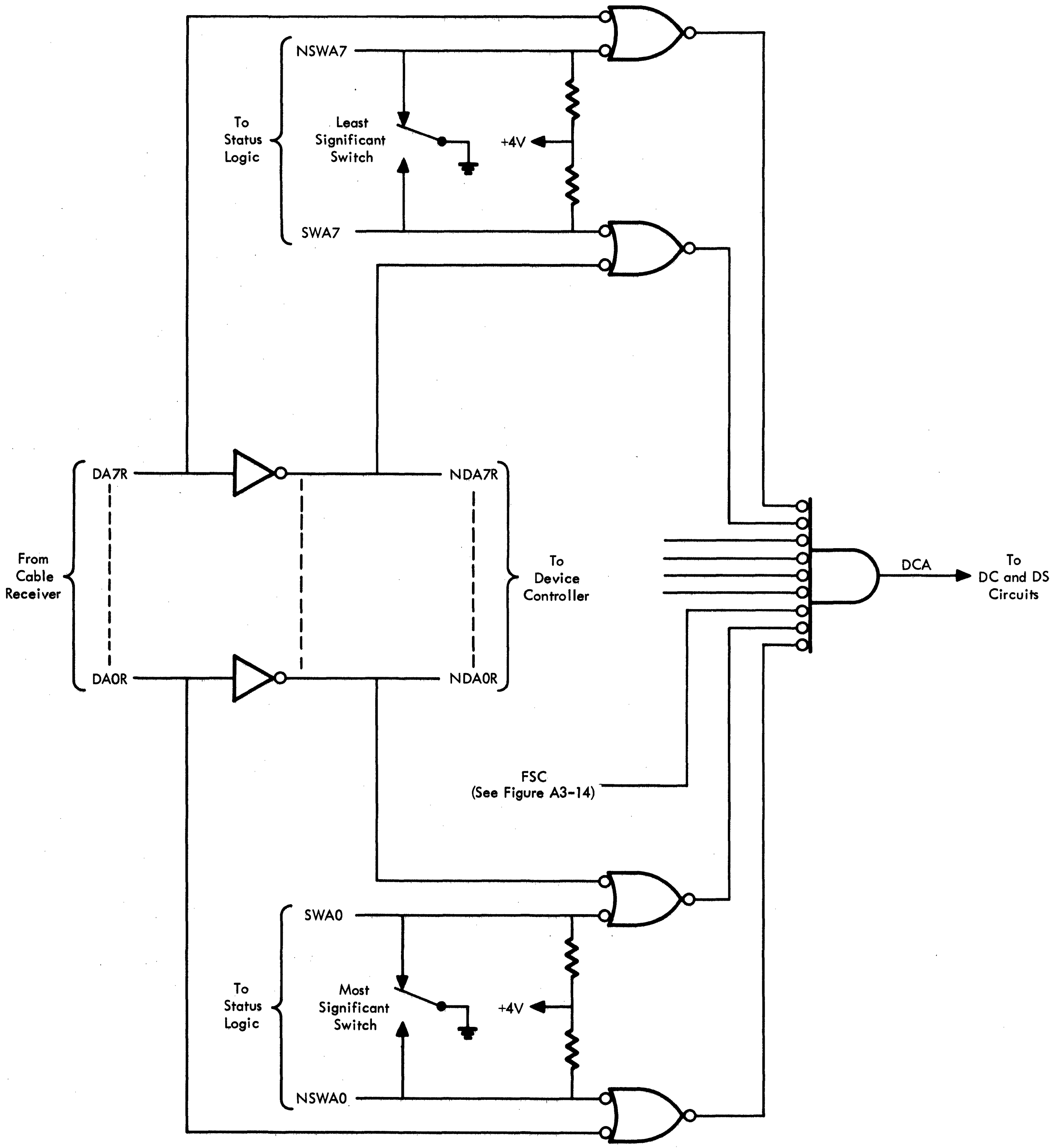


Figure A3-4. Address Selection and Recognition, Simplified Logic Configuration

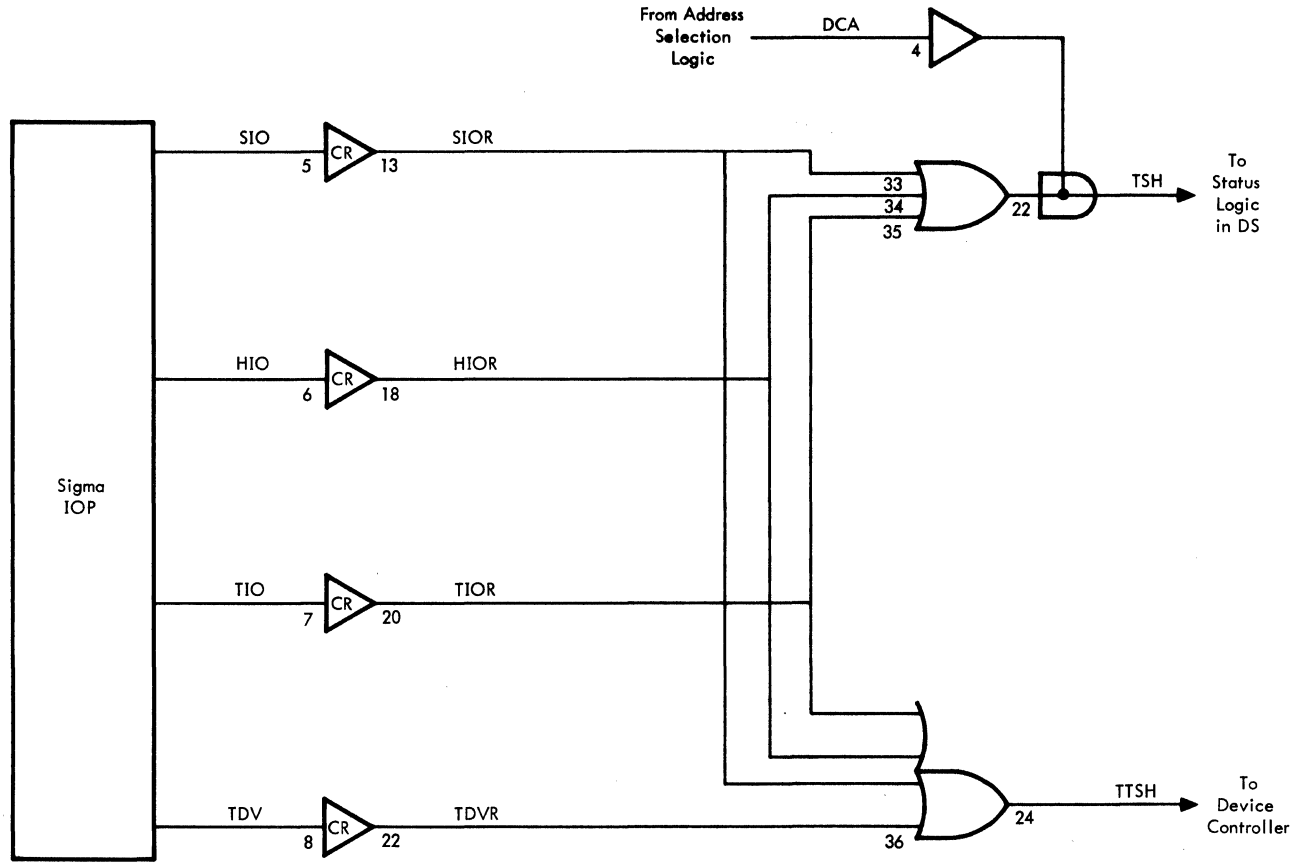


Figure A3-5. Derivation of Function Logic Terms TSH and TTSH

from the controller via the FR lines is determined by the current computer instruction. Function strobe delay term FSD is supplied by the controller when status is applied to the FR lines by function strobe FS. When signal FS falls, delay term FSD is dropped.

The status logic, shown in simplified form in figure A3-7, places status information on the FR lines for transmission to the IOP during three unique functions, each of which is controlled by a separate set of eight AND gates that are enabled one set at a time. The functions performed by the status logic are as follows:

(a) In response to a TDV function indicator, TDV status information is provided to the I/O system.

(b) The FR lines carry TSH status information to the I/O system in response to an SIO, HIO, or TIO function indicator.

(c) During an AIO or an ASC function, the peripheral device address is transmitted to the I/O system.

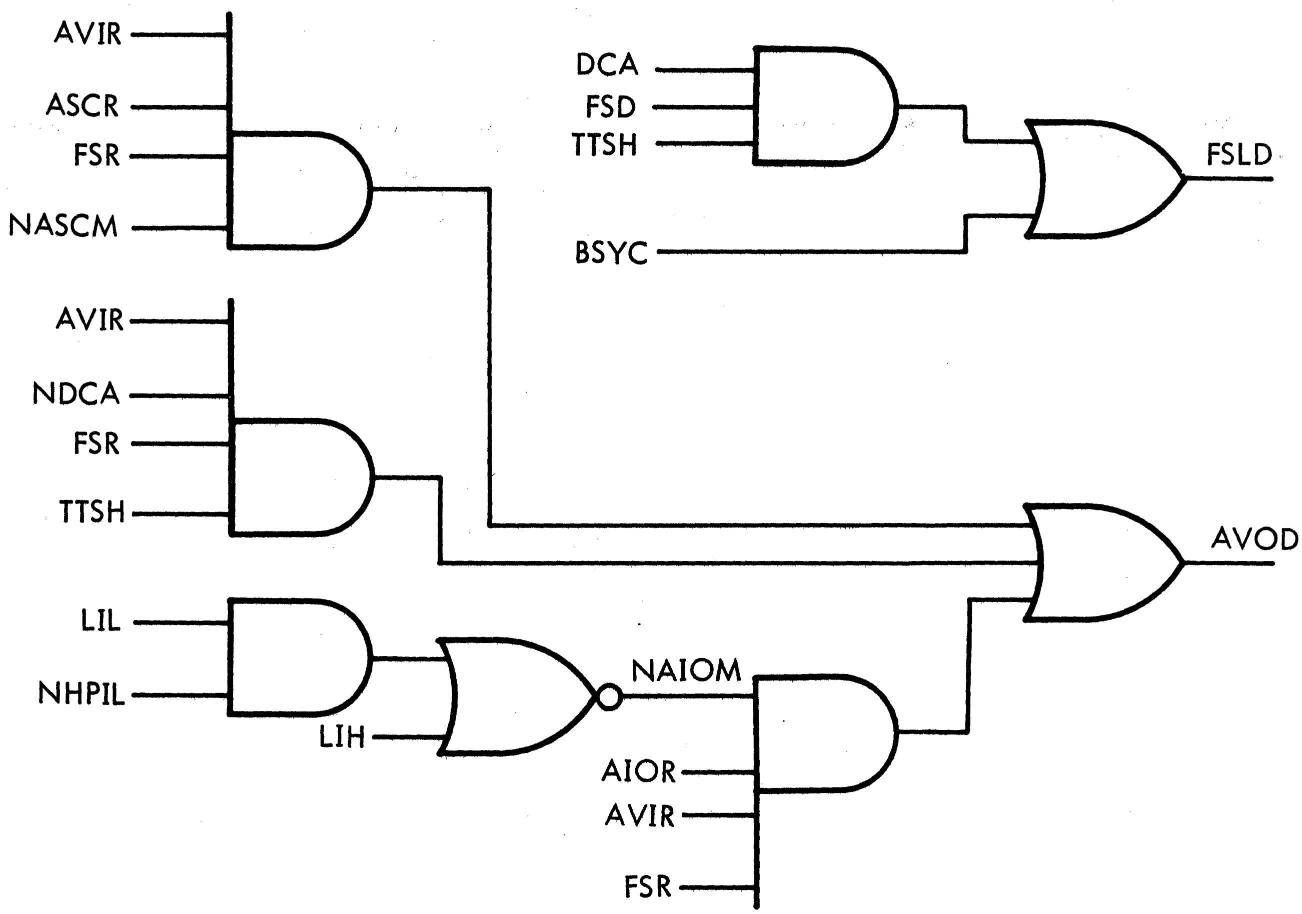


Figure A3-6. Terms AVOD and FSLD, Simplified Logic Diagram

Table A3-1 described the status information that is placed on each FR line during the three applicable functions, and defines the logic equations that are related to each function.

A3-9 I/O DATA INTERCHANGE LOGIC

Data is interchanged between the computer IOP and a group of cable drivers and receivers via nine data lines in a 14-conductor interconnecting cable. The drivers and receivers provide the signal amplification and impedance matching that is required between the I/O system and circuits in the DS and the device controller.

The logic implementation of a typical I/O data line is illustrated in figure A3-8. The data exchange procedure is as follows:

(a) During an SIO, HIO, TIO, or TDV function, the IOP addresses a device controller via data lines DA0 through DA7.

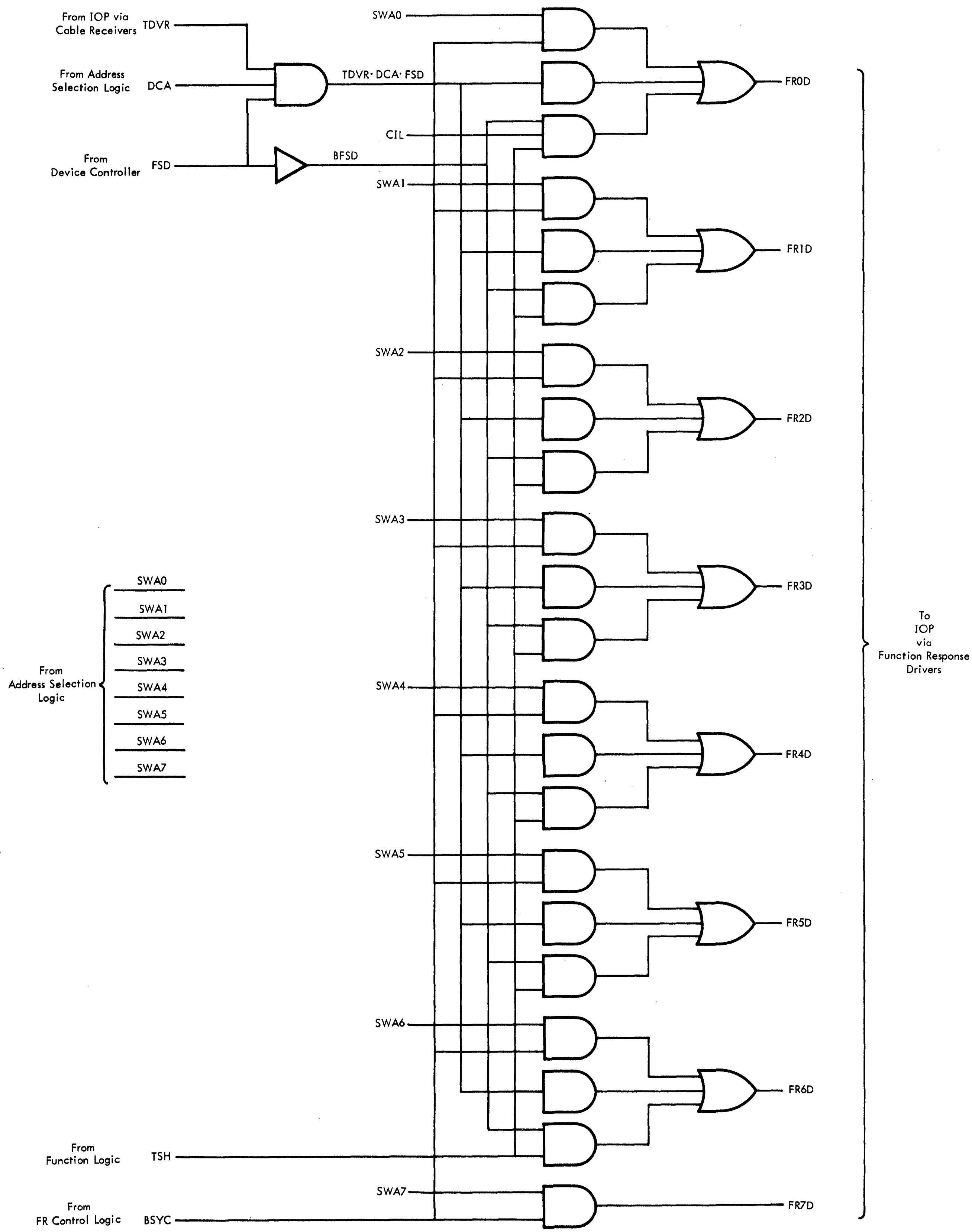


Figure A3-7. Status Logic, Simplified Logic Diagram

Table A3-1. Status Information Returned to IOP on FR Lines

Function Response Line	Logic Equation	Applicable Instruction: SIO, TIO, HIO	TDV	AIO/ ASC	Status Information
FR0D	BSYC · SWA0			X	Device Number MSB
	+STDV00 · (TDVR · DCA · FSD)		X		Rate Error
	+TSH · BFSD · STSH00	X			Interrupt Pending
	(BSYC=AIOM · AIOR · FSD · AVIR +ASCM · FSR · ASCR · AVIR)				
FR1D	BSYC · SWA1			X	Device Number MSB – 1
	+STDV01 · (TDVR · DCA · FSD)		X		Device End
	+TSH · BFSD · STSH0I	X			Device Status
FR2D	BSYC · SWA2			X	Device Number MSB – 2
	+STDV02 · (TDVR · DCA · FSD)		X		Test Device Response
	+TSH · BFSD · STSH02	X			Device Status
FR3D	BSYC · SWA3			X	Device Number MSB – 3
	+STDV03 · (TDVR · DCA · FSD)		X		TDV Response
	+TSH · BFSD · STSH03	X			Device Automatic
FR4D	BSYC · SWA4C			X	Device Number LSB + 3
	+STDV04 · (TDVR · DCA · FSD)		X		TDV Response
	+TSH · BFSD · STSH04	X			Device Unusual End
FR5D	BSYC · SWA5C			X	Device Number LSB + 2
	+STDV05 · (TDVR · DCA · FSD)		X		TDV Response
	+TSH · BFSD · STSH05	X			Device Controller Status
FR6D	BSYC · SWA6C			X	Device Number LSB + 1
	+STDV06 · (TDVR · DCA · FSD)		X		TDV Response
	+TSH · BFSD · STSH06	X			Device Controller Status
FR7D	BSYC · SWA7C			X	Device Number LSB
	+STDV07 · (TDVR · DCA · FSD)		X		TDV Response
	+TSH · BFSD · STSH07	X			Device Controller Status

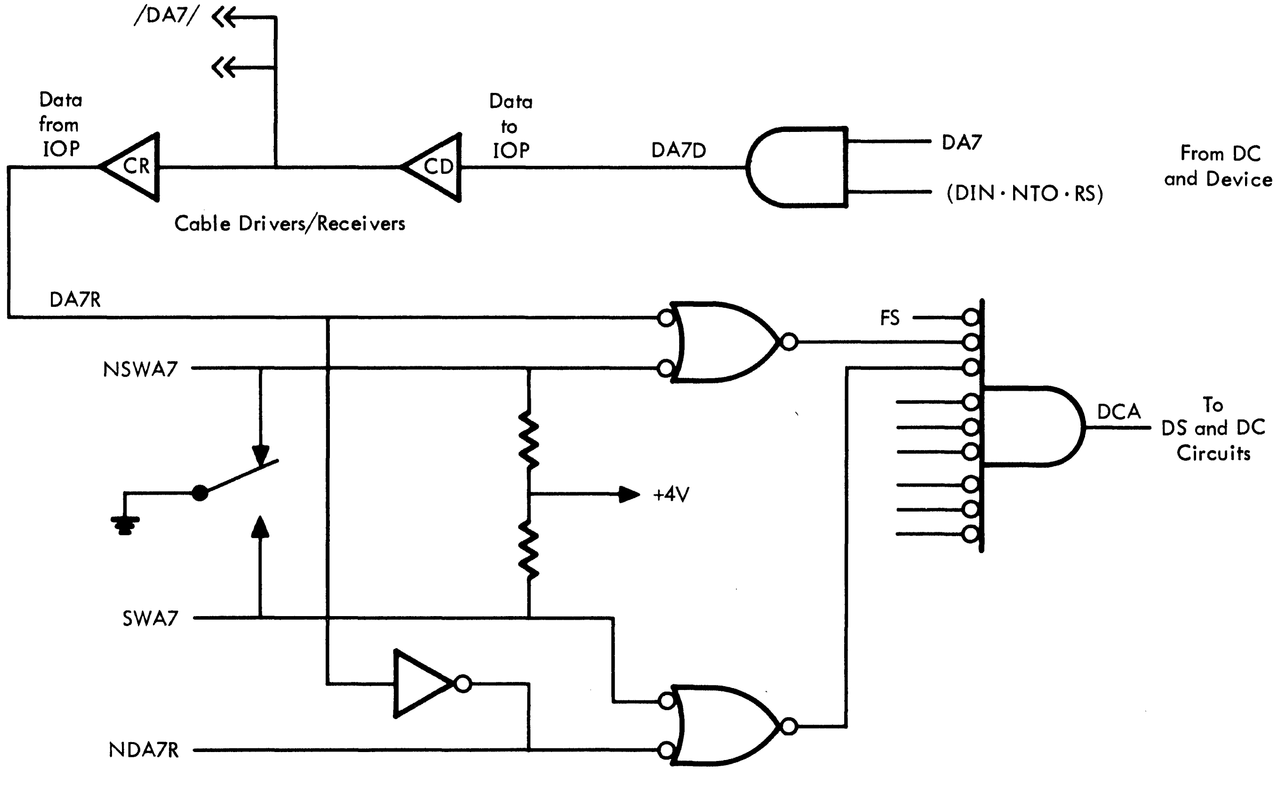


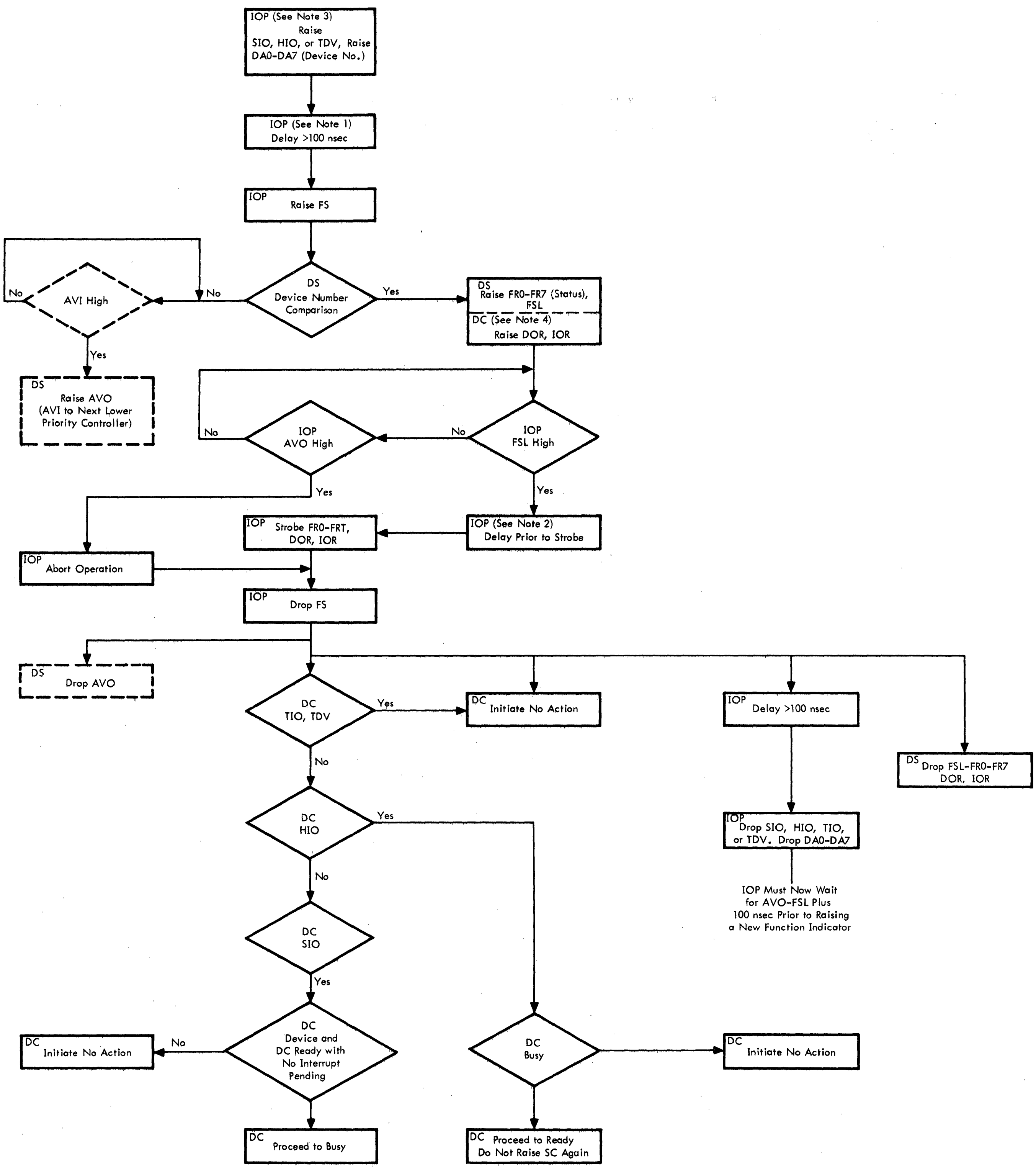
Figure A3-8. Logic Implementation of Typical I/O Data Line

(b) The address from the IOP is amplified by the cable receivers and sent to the address selection logic (described in paragraph A3-5) where it is compared with the address programmed by the toggle switches in the address selection network.

(c) If the two addresses coincide, term DCA, used as an enable term in the DS and the DC, is generated, allowing the data to be transmitted to the appropriate circuits in the DS and the device controller.

(d) Address selection terms SWA0 through SWA7 are also applied to the status logic, as shown in figure A3-7, and are used to supply the device address in response to an AIO or an ASC function indicator.

(e) Input data for the IOP arrives at the cable drivers from the device and device controller as signals DA0D through DA7D. The cable drivers then transmit the data to the IOP via data lines DA0 through DA7. Information transferred during specific functions is defined in Table A3-2. Signal flow during SIO, HIO, TIO, and TDV functions is shown in figure A3-9.



Notes:

1. For signals arriving from IOP, all timing is measured at output of Device Controller Cable Receiver.
2. Before strobing input signals lines after receiving FSL or RS signal, IOP must compensate for worst-case signal description caused by cables, IOP receivers, IOP logic, plus 60 nsec.
3. Only one function indicator (SIO, HIO, TIO, TDV, AIO, or ASC) can be high at any time.
4. DOR and IOR represent condition codes NCC1 and NCC2 respectively at this time. Raise IOR (NCC2) only if applicable.
5. AVI to the highest priority device controller is always high.

Figure A3-9. Signal Flow During SIO, HIO, TIO, and TDV Operations

Table A3-2. Information Transmitted to IOP Via Data Lines

Data Lines	Applicable Instruction			Signal Description
	Data In	Order In	AIO Response	
DA0D	X			Data MSB
		X		Transmission Error
			X	Rate Error
DA1D	X			Data MSB - 1
		X		Incorrect Length
			X	Device End
DA2D	X			Data MSB - 2
		X		Chaining Modifier
			X	AIO Response
DA3D	X			Data MSB - 3
		X		Channel End
			X	AIO Response
DA4D	X			Data LSB + 3
		X		Unusual End
			X	AIO Response
DA5D	X			Data LSB + 2
		X		Unused
			X	AIO Response
DA6D	X			Data LSB + 1
		X		Unused
			X	AIO Response
DA7D	X			Data LSB
		X		Unused
			X	Order Out Stop Interrupt

A3-10 PRIORITY LOGIC

Priority logic circuits are provided in the DS to gate service and interrupt requests between the device and device controller and the I/O system. When a request is acknowledged by the I/O system, the service and interrupt logic must determine the priority and generate the required signals to initiate the appropriate circuit responses.

A3-11 SERVICE FUNCTION LOGIC

The service function is initiated by an SIO from the IOP, in response to which the controller requests service by raising signal CSL. Circuit LSL in the DS latches CSL and service call line SC follows. The IOP acknowledges the service call by raising signal ASC, followed by function strobe FS. The sequence continues in the following order:

(a) The raising of ASC causes terms LSL, LSH, and HPSL to be latched.

(b) When FS becomes True, the DS samples LSL, LSH, HPSL, and AVI, to determine if ASC can be accepted.

(c) If ASC cannot be accepted because HPSL has been raised by a lower priority device controller, line AVO is shuttled to the next lower priority DC.

(d) If ASCM is True, denoting ASC can be accepted, the DS drops AVOD and raises FSL.

(e) Service connect flip-flop FSC is set by ASCB, which is driven True by ASCM.

(f) When flip-flop FSC is set, LSL is inhibited and service call SC is dropped.

(g) Flip-flop FSC is reset by end service signal ES.

A simplified diagram of service function logic is shown in figure A3-10; service cycle timing is shown in figure A3-11.

A3-12 Implementation of the ASC Function

The controller raises the term, CSL, when a Service Call is required. The DS latches CSL during an ASC Function by latch circuit LSL.

For high priority Service Calls, the controller must provide term CSH, which is latched by DS latch circuit LSH. Again, the controller must provide both CSL and CSH for high priority Service Calls. The Service Call line, SC, follows LSL. The High Priority Service line, HPS, follows LSH.

The IOP, seeing SC raised, will eventually acknowledge by raising the ASC Function Indicator. At this time the DS will latch the condition of LSL, LSH, and HPSL (HPSL continuously monitors the state of the High Priority Interrupt line HPS).

When the IOP raises the Function Strobe, FS, the highest priority DS examines LSL, LSH and HPSL to determine if the ASC may be accepted. If the ASC cannot be accepted (not required

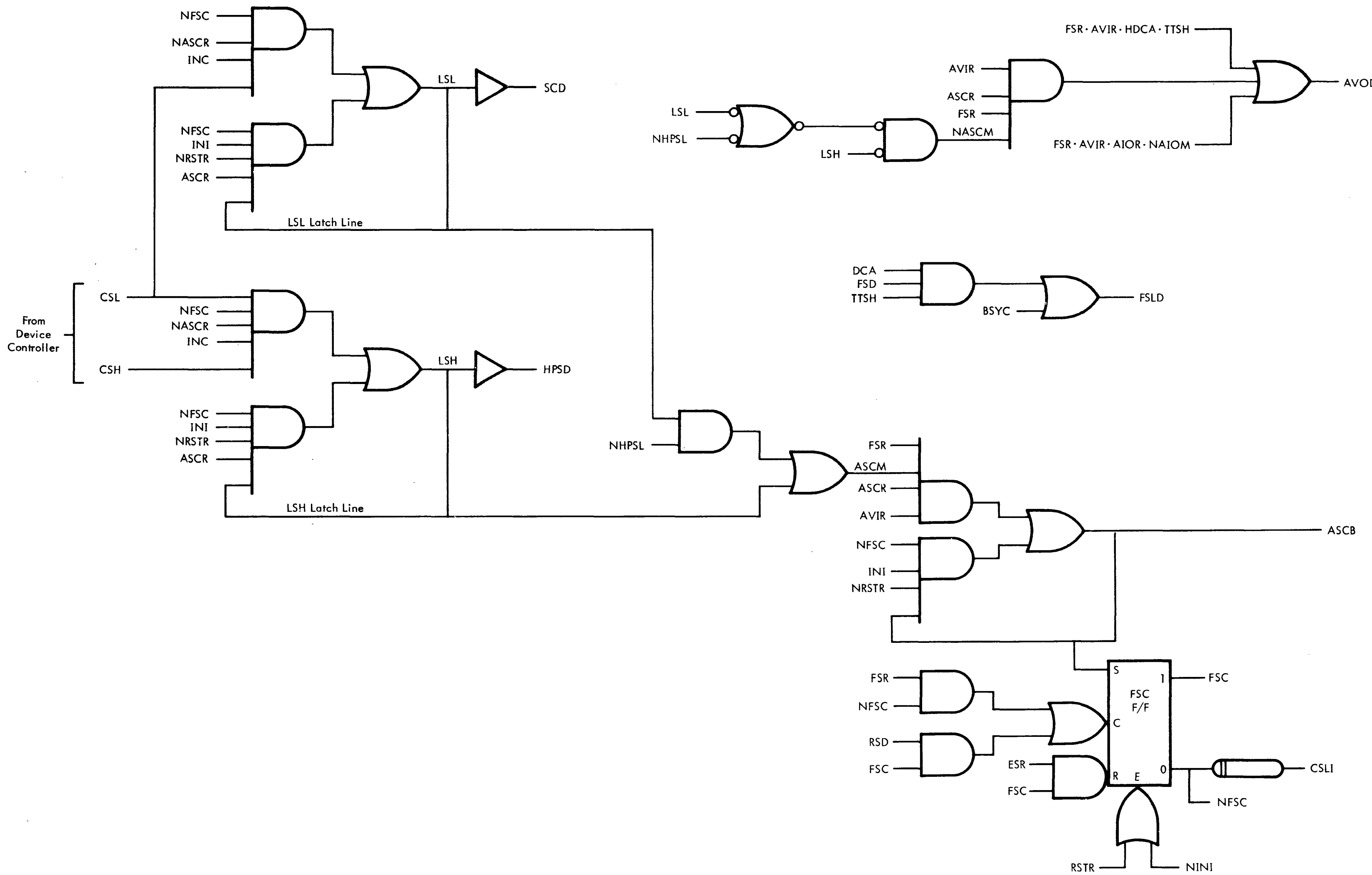


Figure A3-10. Service Function Priority Logic, Simplified Logic Diagram

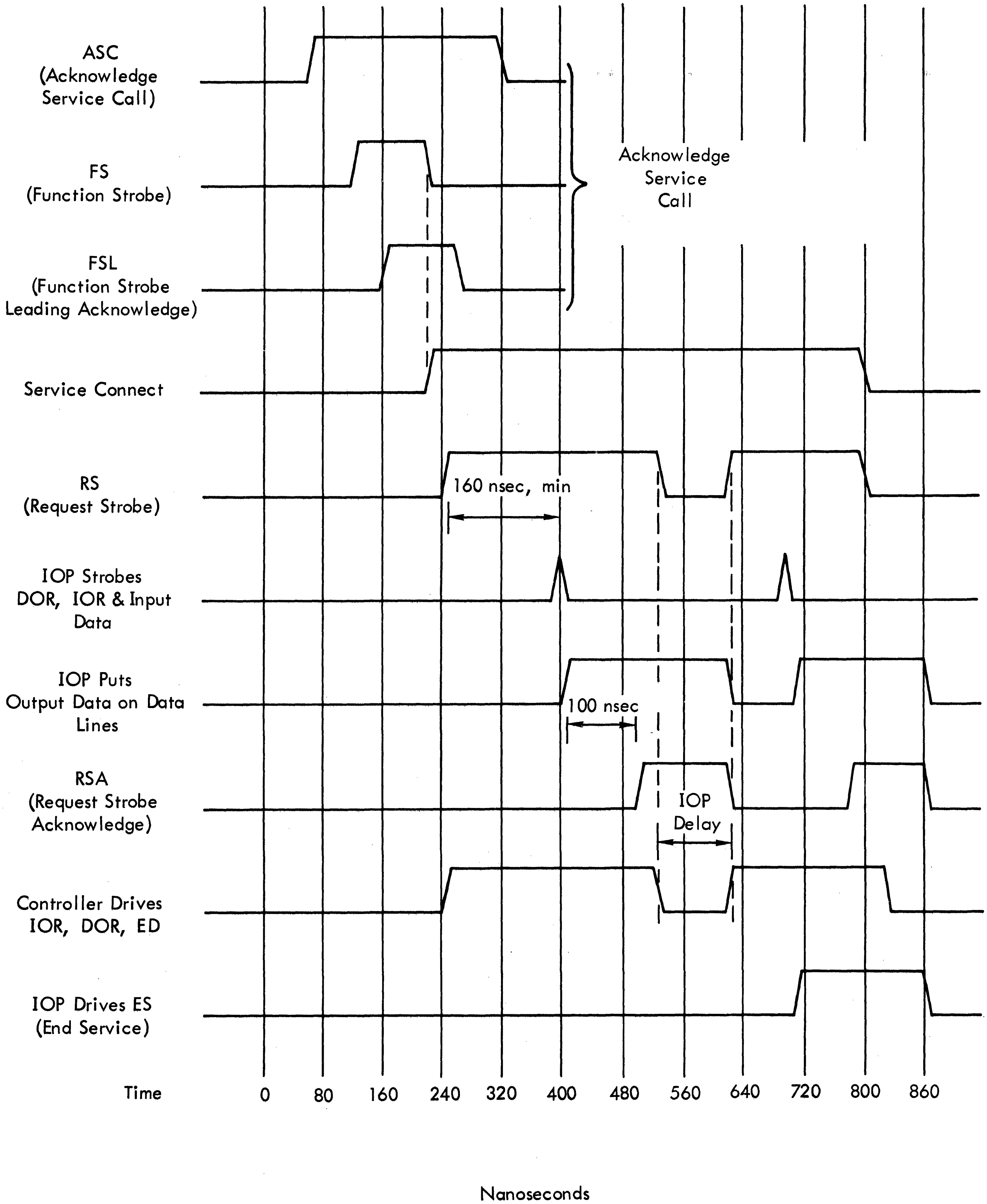


Figure A3-11. Service Cycle Timing Diagram or a lower priority controller has raised the High Priority Service Line), the Available Out line, AVO, is sent to the next lower priority controller. The action of sequentially sending AVO from higher priority controllers to lower priority controllers continues until the DS finds ASCM true. At this point AVOD is inhibited and FSL is raised. The controller places its device number on the function response lines at this time for the transmission of information to the IOP. The DS supplies the required gating for the four most significant bits. The information strobed onto the FR lines is defined in Table A3-1.

Figure A3-12 contains a diagram of ASC signal flow preparatory to the establishment of a service connection. Table A3-3 lists the 16 communication lines between the IOP and the DS that are active during a service cycle.

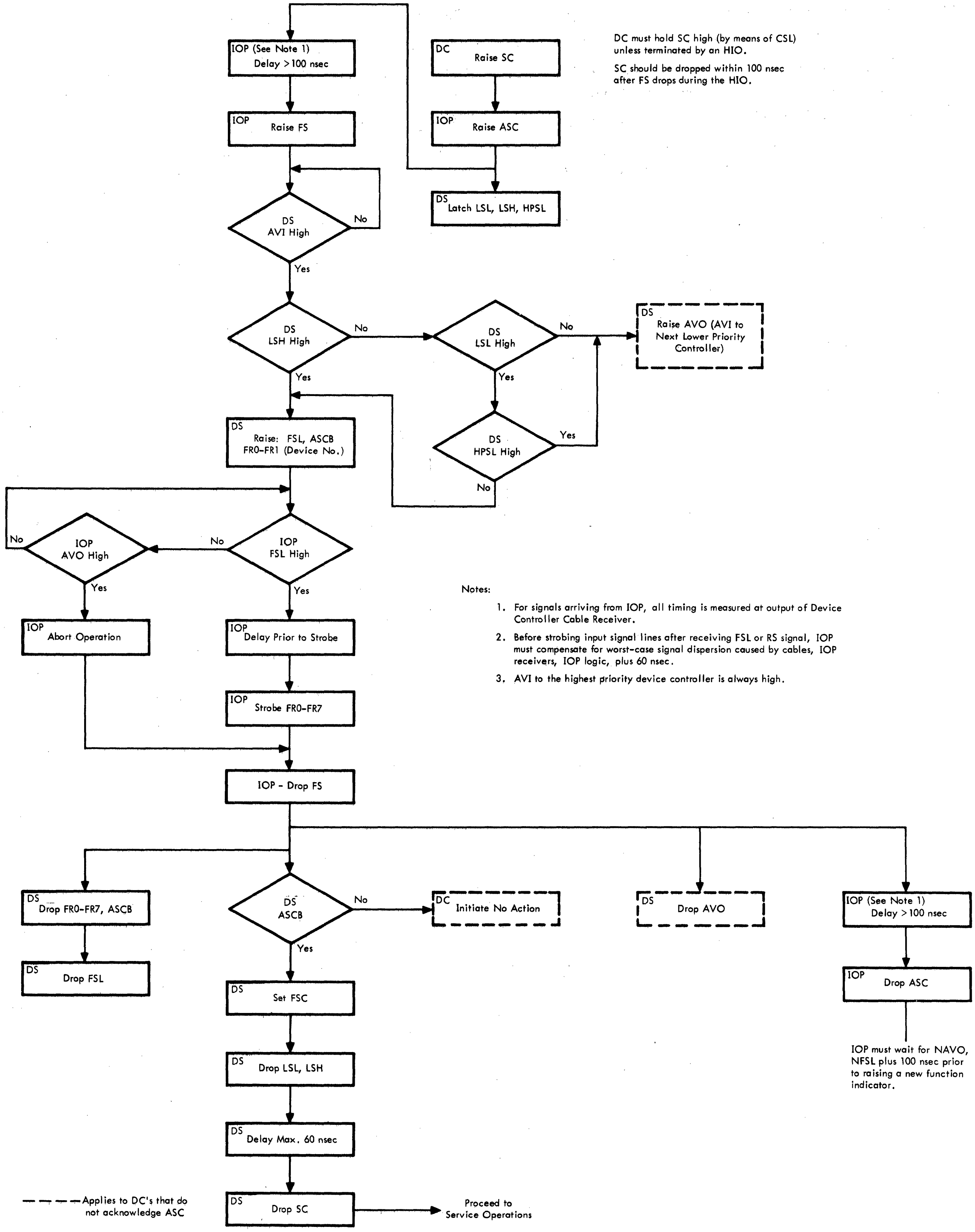
A3-13 Service Connect Flip-Flop

When the IOP receives signal FSL at a high level, Function Strobe FS is dropped. The falling edge of FS sets flip-flop FSC.

After term FSC becomes True, the controller raises request strobe RS and controls the coding of signals DOR and IOR, as shown in Table A3-4, to specify the type of information that is to be exchanged.

Table A3-3. Service Cycle Interface Signals

Mnemonic Name	Signal Description
RS	Request Strobe
RSA	Request Strobe Acknowledge
DOR	Data-Order Request
IOR	Input-Output Request
ED	End Data
ES	End Service
DA0 | | DA7	Data Lines
DAP	Data Parity
PC	Parity Check



Notes:

1. For signals arriving from IOP, all timing is measured at output of Device Controller Cable Receiver.
2. Before strobing input signal lines after receiving FSL or RS signal, IOP must compensate for worst-case signal dispersion caused by cables, IOP receivers, IOP logic, plus 60 nsec.
3. AVI to the highest priority device controller is always high.

Figure A3-12. ASC Signal Flow Diagram (Prior to Service Connection)

Table A3-4. Coding of Control Signals DOR and IOR

DOR	IOR	Operation
0	0	Data Input
0	1	Data Output
1	0	Order Input
1	1	Order Output

A3-14 Service Connect Sequence

When the type of operation has been specified by the coding of DOR and IOR, the following sequence occurs:

(a) If an input operation is specified, the DC puts data on the Data lines via the DS. The DC may drive signal PC if parity checking in the IOP is needed. Signal PC is generated by a cable driver.

(b) The IOP generates signal RSA in response to request strobe RS. If an output operation is specified, output data is strobed onto the lines after a 100 nanosecond delay. Signal RSA follows after an additional 100 nanosecond delay.

(c) The controller releases RS when RSA is received. At this point, output data is strobed during an output operation.

(d) After RS is released by the DC, the IOP releases RSA. Another RS may then be generated, depending on the state of signals ED and ES, the coding of which is defined in Table A3-5.

(e) If the current data exchange is to be the last one, the DC may drive ED when it generates RS. The DC is only allowed to discontinue issuing RS signals when ES becomes True. Ordinarily, if the IOP senses the ED is True, the IOP drives ES True with the same timing as the output data, notifying the controller that service is complete. Also, the IOP may drive ED True, with or without ES, to terminate the data exchange portion of the service cycle.

(f) When the IOP has control information (other than OOUT) to transmit to the DC, a terminal order signal (TO) is used. When the DC senses that ED is True and ES is False, one more RS signal is generated so that TO may be received. The timing for this additional TO subcycle is identical to all others; the TO data timing is the same as OOUT or DOUT. During TO, signal ES is driven True by the IOP. The service function is complete following a terminal order.

Table A3-5. Coding of Control Signals ED and ES

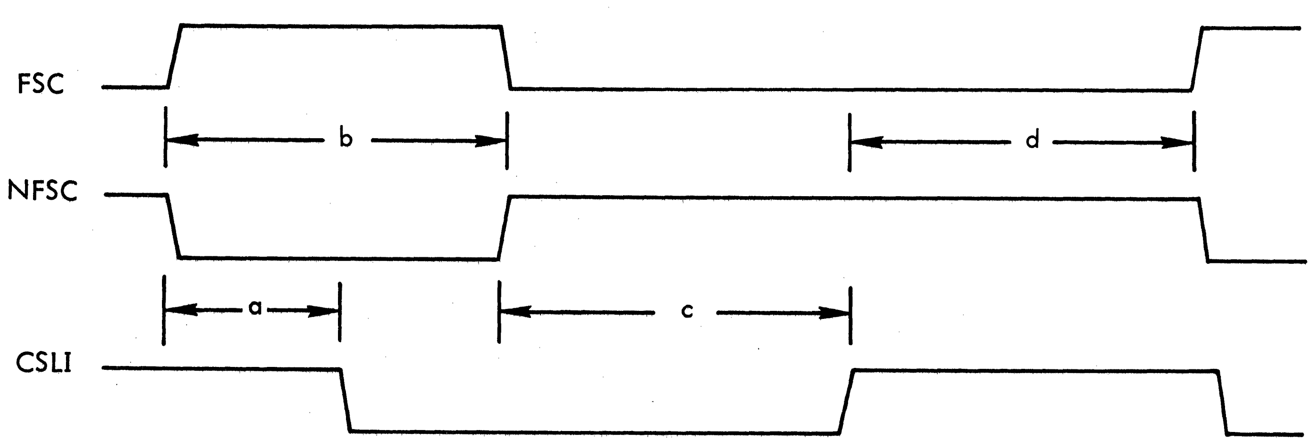
ED	ES	Description
0	0	More data to follow; DC must generate at least one more RS signal.
1	0	This is last data byte; one more RS required to get the TO.
X	1	Either last byte with no TO to follow, or TO itself. In either case, service is complete after this subcycle.

A3-15 RESETTING FLIP-FLOP FSC

Signal FSC is ANDed with signal ESR from the end service receiver and gated into the reset input of the service connect flip-flop causing output NFSC to be generated. Signals RSTR and NINI are ORed into the erase gate as direct reset signals.

Reset output signal NFSC is fed to a special time delay circuit from which delayed reset signal CSLI is generated. The timing relationship between signals NFSC and CSLI is shown in figure A3-13.

Flip-Flop FSC Output Signal Timing



a = 50 nanoseconds, max.
b = 100 nanoseconds, min.
c = 100 to 350 nanoseconds
d = 100 nanoseconds, min.

Figure A3-13. Service Connect Delay Timing

Logic circuits involved in the service connect operation are illustrated in simplified form in figure A3-14.

Signal RSARC, the logical evolution of which is shown in figure A3-14, is sent to an inverter. The inverted signal, NRSARC, is used to prevent switching transients from appearing on the RS line if flip-flop FSC resets slowly (70 nanoseconds, maximum).

A3-16 INTERRUPT FUNCTION

When an interrupt call is required, the device controller raises CIL, which is used for low priority interrupt calls. As shown in the simplified interrupt function logic diagram, figure A3-15, term CIL is generated by a flip-flop. During an AIO function, term CIL is held True by Latch circuit LIL. CIL must also be set for high priority interrupt calls along with CIH.

For high priority calls, the DC supplies term CIH, which is latched by circuit LIH. Term LIL is followed by interrupt call line IC and high priority interrupt line HPI follows term LIH.

During an AIO function, the signal flow for which is shown in figure A3-16, the interrupt logic is implemented as described in the following sequence:

(a) When the CPU acknowledges Interrupt Call, the IOP raises the AIO Function Indicator. At this time, the DS latches the condition of terms LIL, LIH, and HPIL, which monitors the state of high priority interrupt line HPIL.

(b) Function Strobe FS is raised by the IOP and the DS examines LIL, LIH, and HPIL to determine if the AIO may be accepted. In multicontroller systems, if the AIO cannot be accepted by the addressed controller, Available Out signal AVO is sent to the next lower priority controller as AVOD.

(c) Available Input term AVIR, which is always True in a "single device controller" system, is only True at the DC in a multicontroller system after all higher priority controllers have passed along Available Output term AVO. Thus, AVO starts from the highest priority DC and samples each controller in a descending order. When AVO arrives at a controller where a True AIOM is encountered, AVO is inhibited and function strobe leading acknowledge signal FSL is raised.

The following sequence of events completes the AIO function:

(a) The DS supplies term AIOC, indicating that Interrupt Call is being acknowledged.

(b) The controller holds CIL and CIH True until the DS raises AIOC.

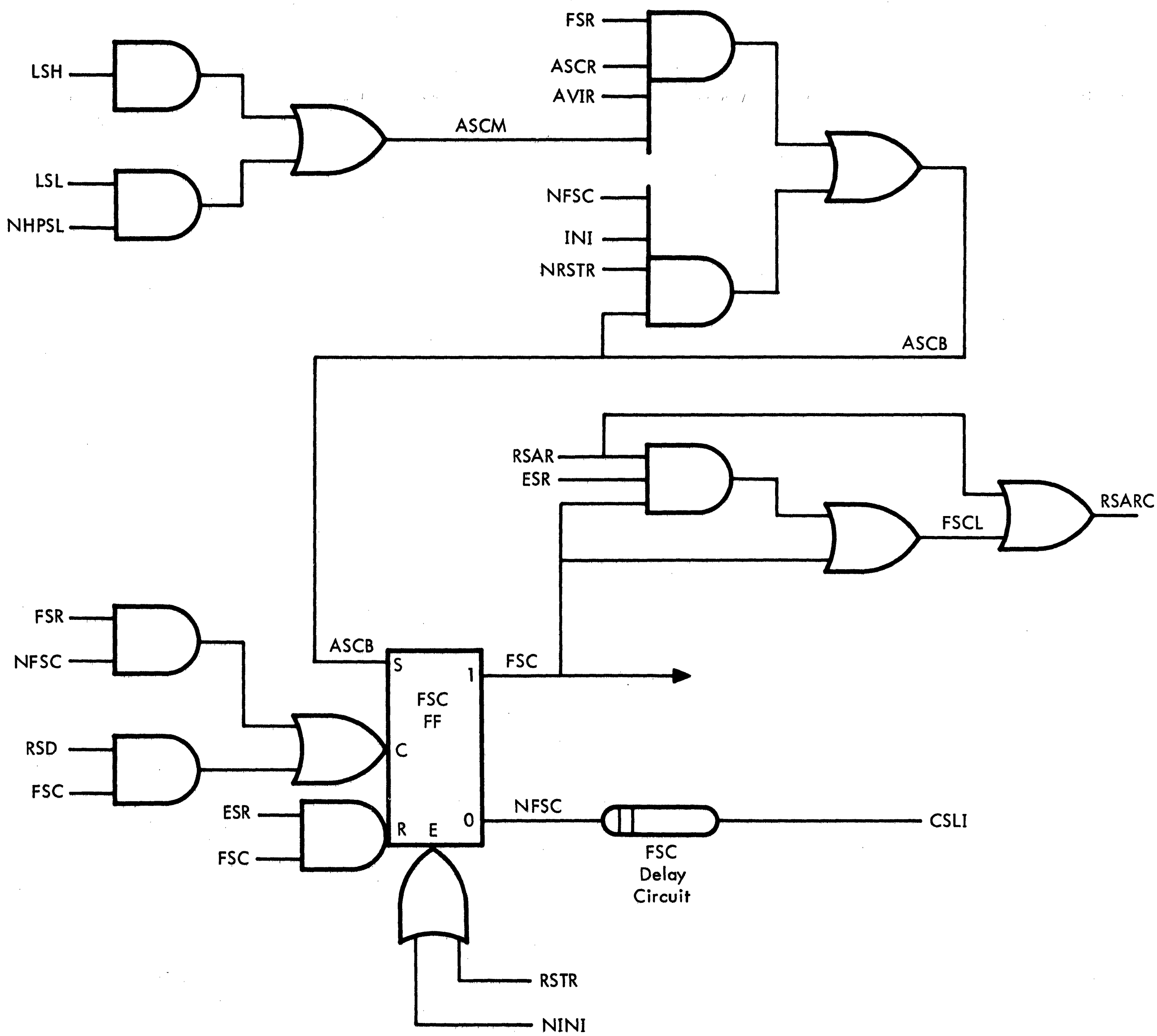


Figure A3-14. Service Connection Circuits, Logic Diagram

(c) The controller uses AIOC in conjunction with FSR to reset CIL, CIH, and any interrupt indicators that are currently set.

(d) The controller provides status and condition codes while AIOC is high.

(e) When FSL is returned to the IOP at a high level, function strobe FS is dropped. About 100 nanoseconds later, the IOP drops term AIO, to complete the function.

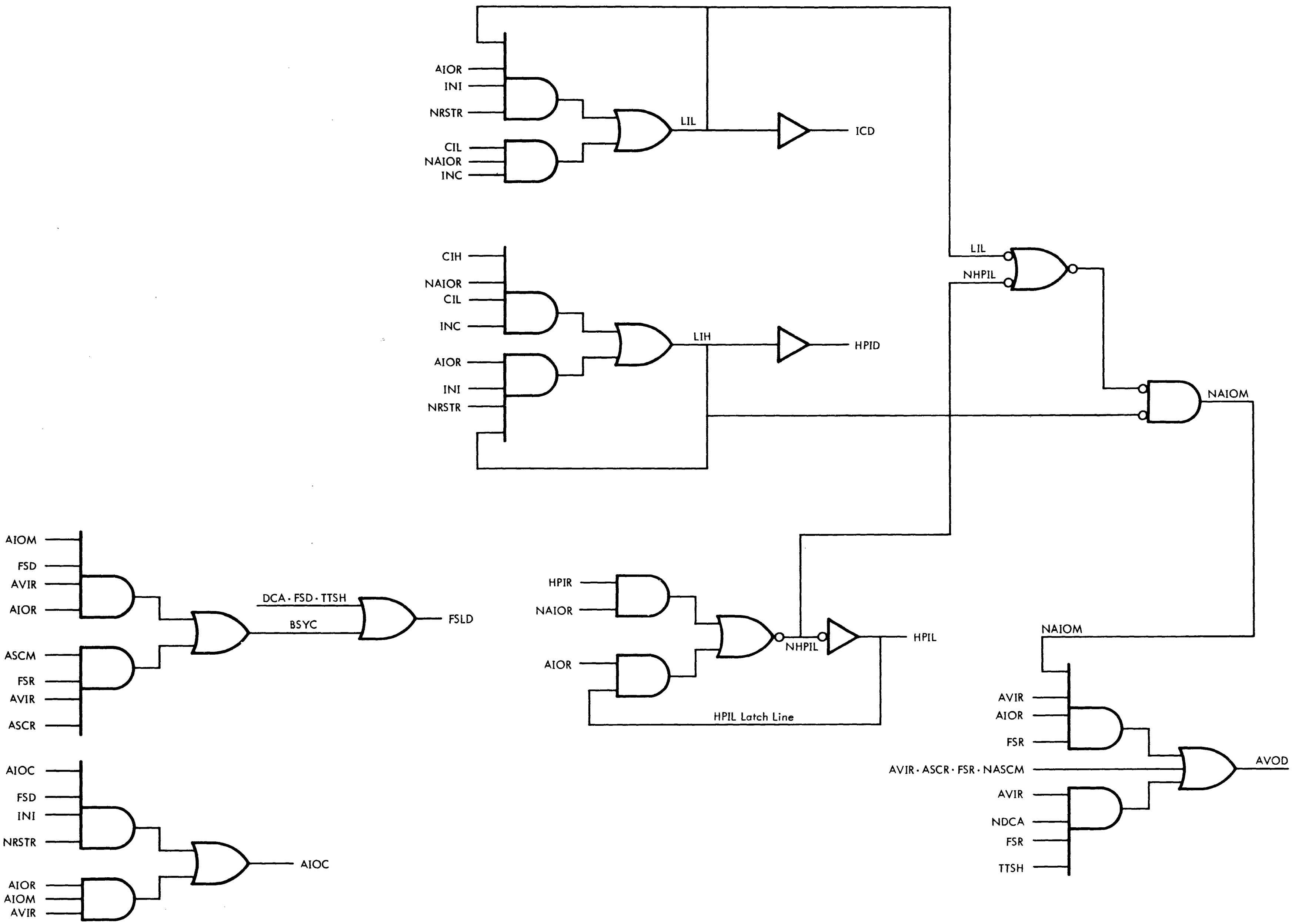
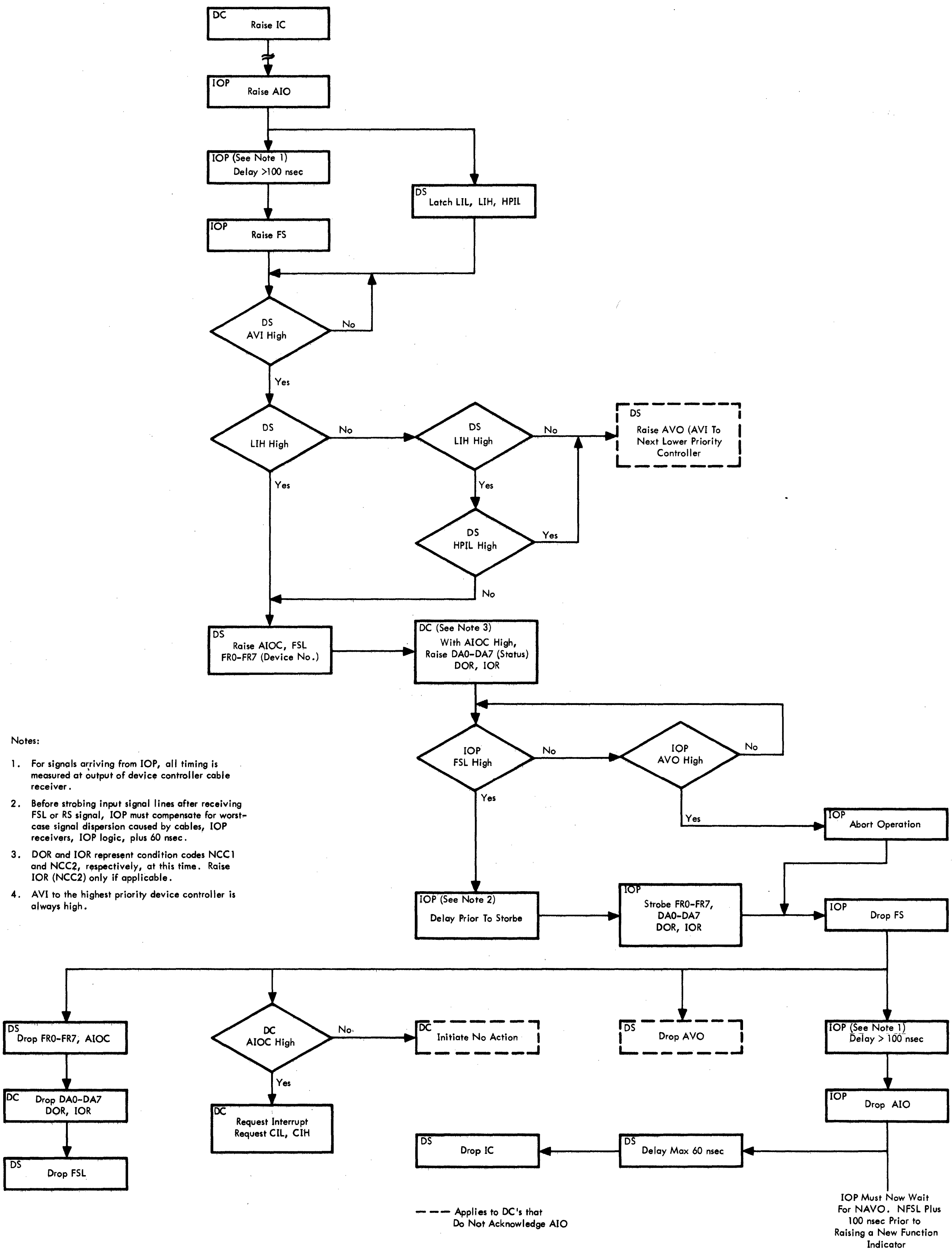


Figure A3-15. Interrupt Function, Simplified Logic Diagram



Notes:

1. For signals arriving from IOP, all timing is measured at output of device controller cable receiver.
2. Before strobing input signal lines after receiving FSL or RS signal, IOP must compensate for worst-case signal dispersion caused by cables, IOP receivers, IOP logic, plus 60 nsec.
3. DOR and IOR represent condition codes NCC1 and NCC2, respectively, at this time. Raise IOR (NCC2) only if applicable.
4. AVI to the highest priority device controller is always high.

Figure A3-16. AIO Signal Flow Diagram

A3-17 DATA INPUT AND OUTPUT CONTROL

Signal flow during a Data Input and Data Output operation's are shown in figure A3-17 and 3-18, respectively.

A3-18 ORDER OUTPUT IMPLEMENTATION

The function of an Order Output service cycle is to obtain the first (or subsequent) command doubleword from the CPU main memory and (1) store the new byte count in IOP fast memory; (2) store the new memory byte address in IOP fast memory; (3) store the eight IOP control flags in IOP fast memory; and (4) pass the new order along to the device controller.

A3-19 Order Output Sequence (Sigma 5 and Sigma 7 Only)

The sequence of operations that transpires when the controller requests OOUT during command chaining (when a Sigma 5 or Sigma 7 computer is used) is as follows:

(a) Subsequent to processing the last data byte in or out, the IOP issues a TO that specifies count done, if data chaining is not requested. If data chaining is called for, the DC is not cognizant of the request, nor is the controller aware that the byte count has gone to zero and has been set to a new nonzero value by data chaining.

(b) The controller performs an OIN specifying channel end.

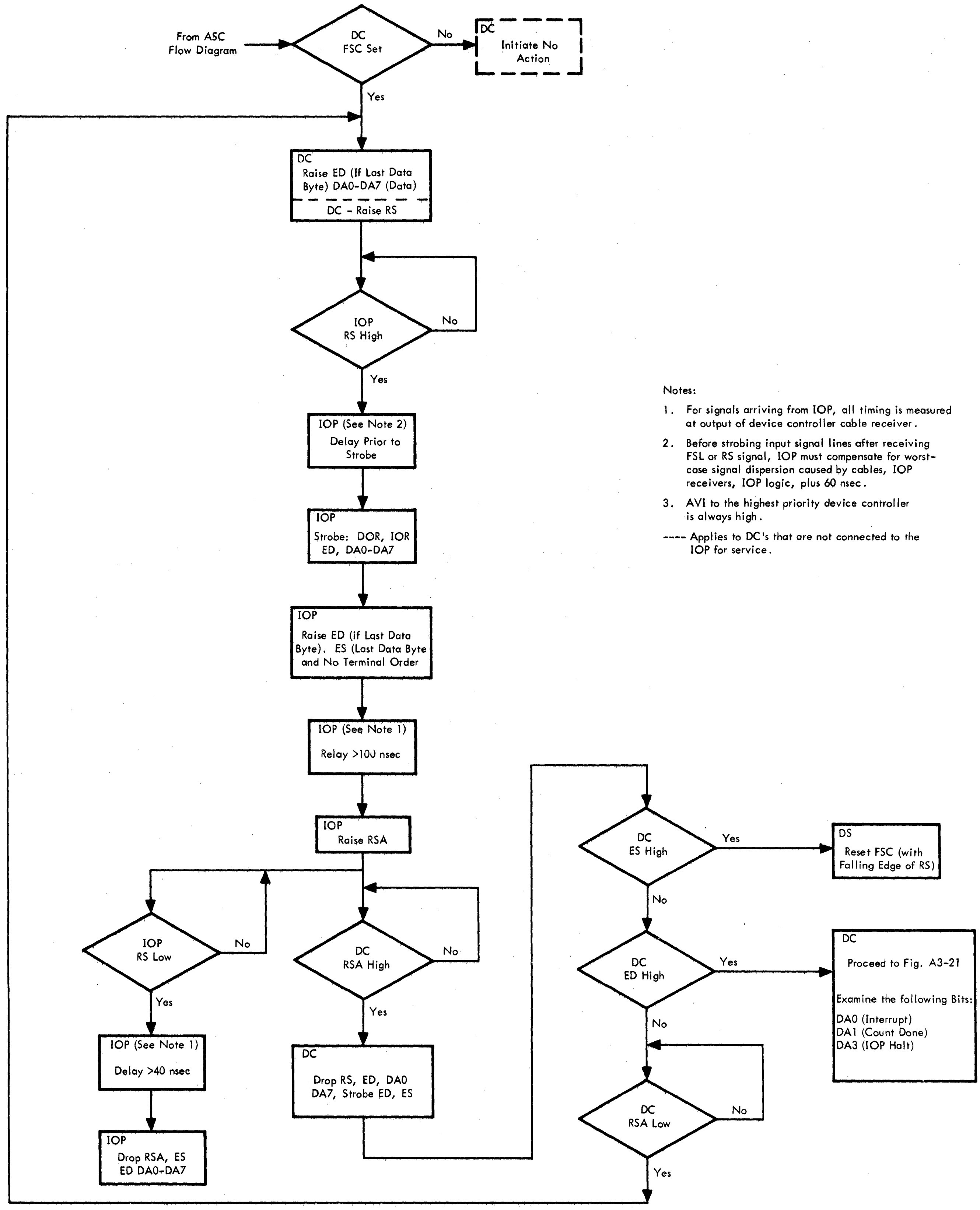
(c) In the TO following OIN, a bit designates whether command chaining is to be performed. The CC bit is present during each TO, but is inspected by the controller only after the OIN that specifies channel end. If bit CC is not set, the controller returns to the ready condition, requiring another SIO instruction to restart. If CC is set, the DC requests OOUT on the next service cycle and begins another operational sequence.

The significance of information placed on the Data lines during OOUT is defined in Table A2-4.

Signal flow during an OOUT operational sequence is shown in figure A3-19.

A3-20 ORDER INPUT IMPLEMENTATION

The Order Input service cycle allows the controller to communicate certain control information to the IOP, via the DS. OIN information is placed on the Data lines by the DS when the controller brings up request strobe RS. Signal flow during the OIN function is shown in figure A3-20.

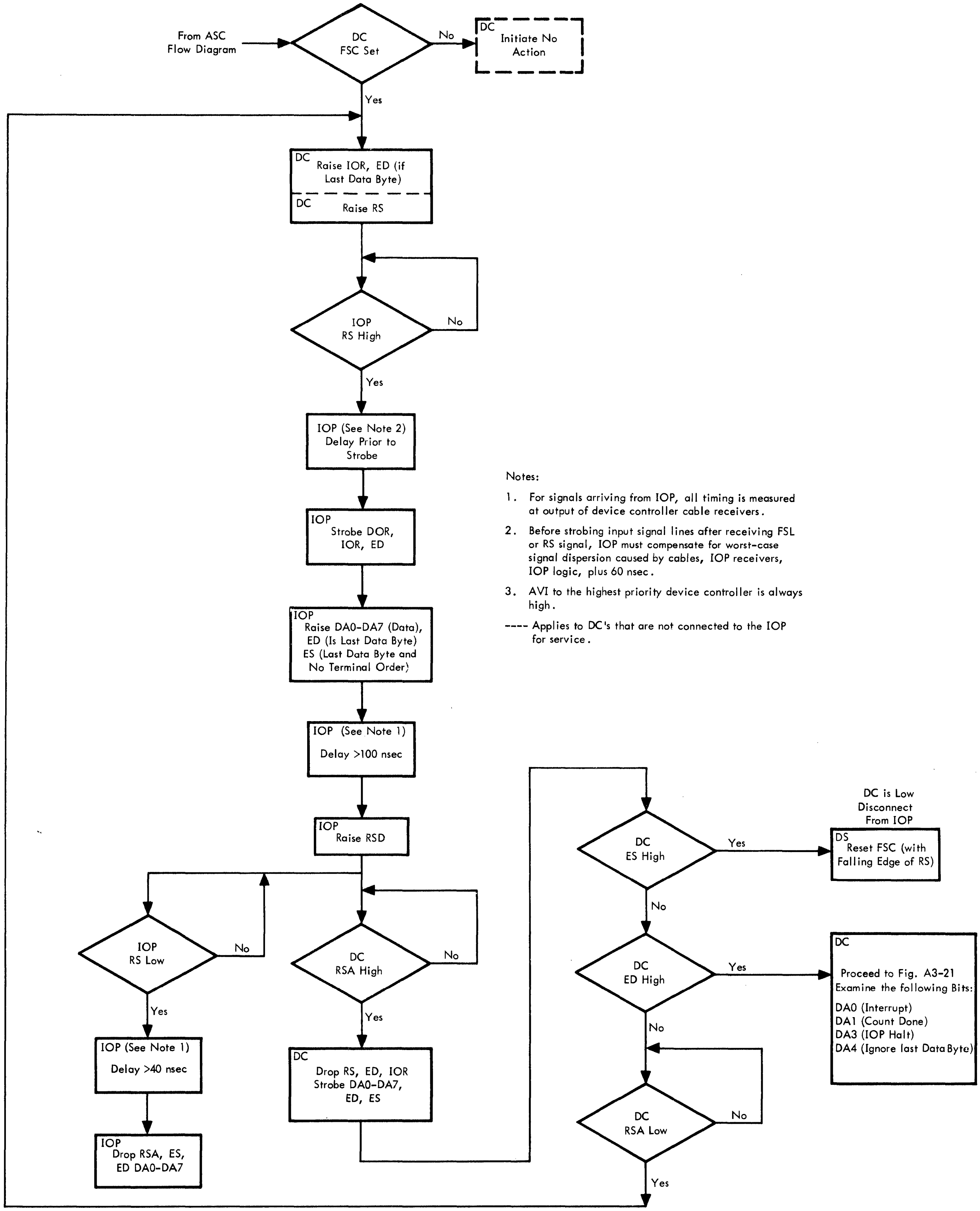


Notes:

1. For signals arriving from IOP, all timing is measured at output of device controller cable receiver.
2. Before strobing input signal lines after receiving FSL or RS signal, IOP must compensate for worst-case signal dispersion caused by cables, IOP receivers, IOP logic, plus 60 nsec.
3. AVI to the highest priority device controller is always high.

---- Applies to DC's that are not connected to the IOP for service.

Figure A3-17. Data Input, Signal Flow Diagram

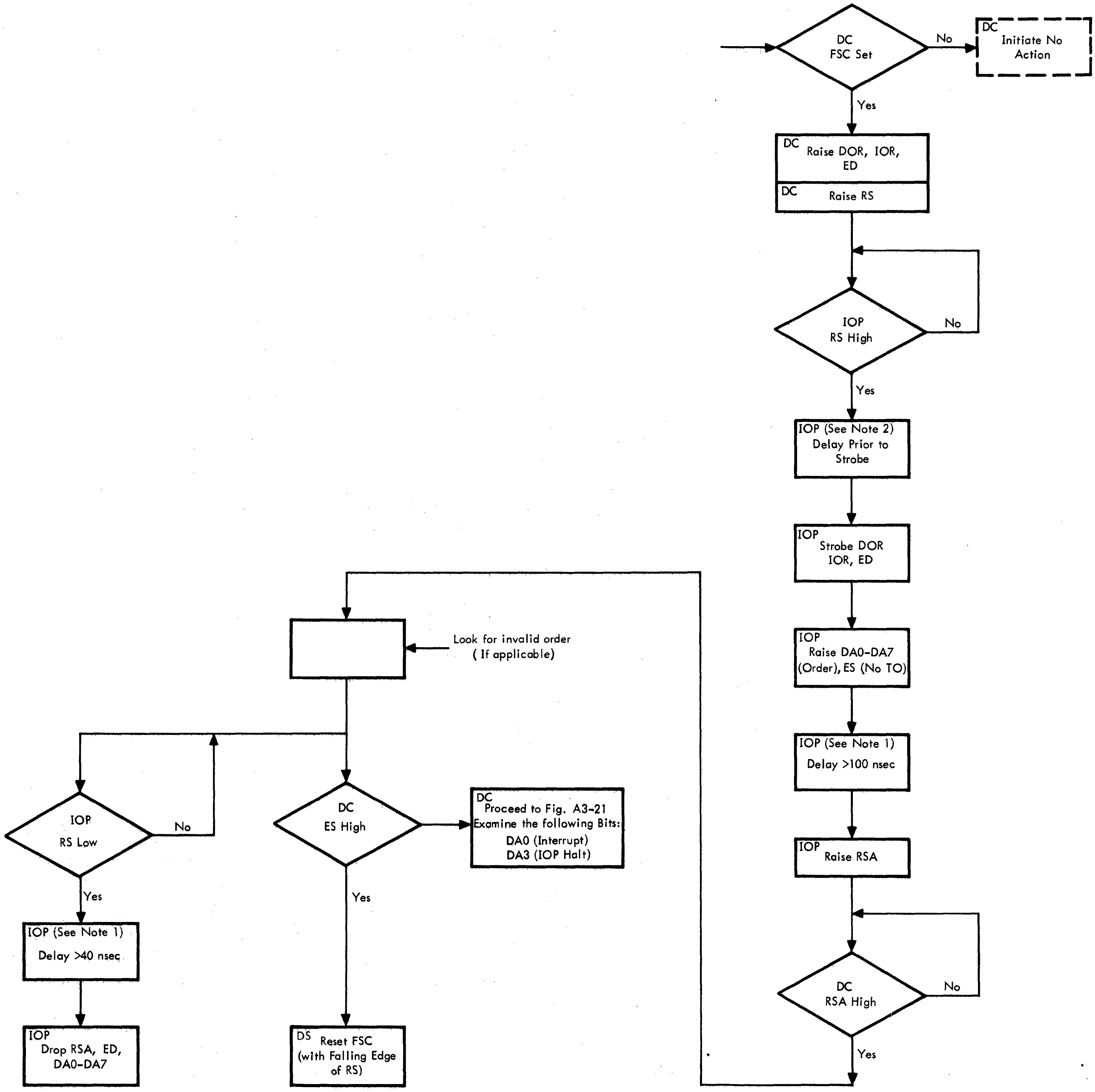


Notes:

1. For signals arriving from IOP, all timing is measured at output of device controller cable receivers.
2. Before strobing input signal lines after receiving FSL or RS signal, IOP must compensate for worst-case signal dispersion caused by cables, IOP receivers, IOP logic, plus 60 nsec.
3. AVI to the highest priority device controller is always high.

---- Applies to DC's that are not connected to the IOP for service.

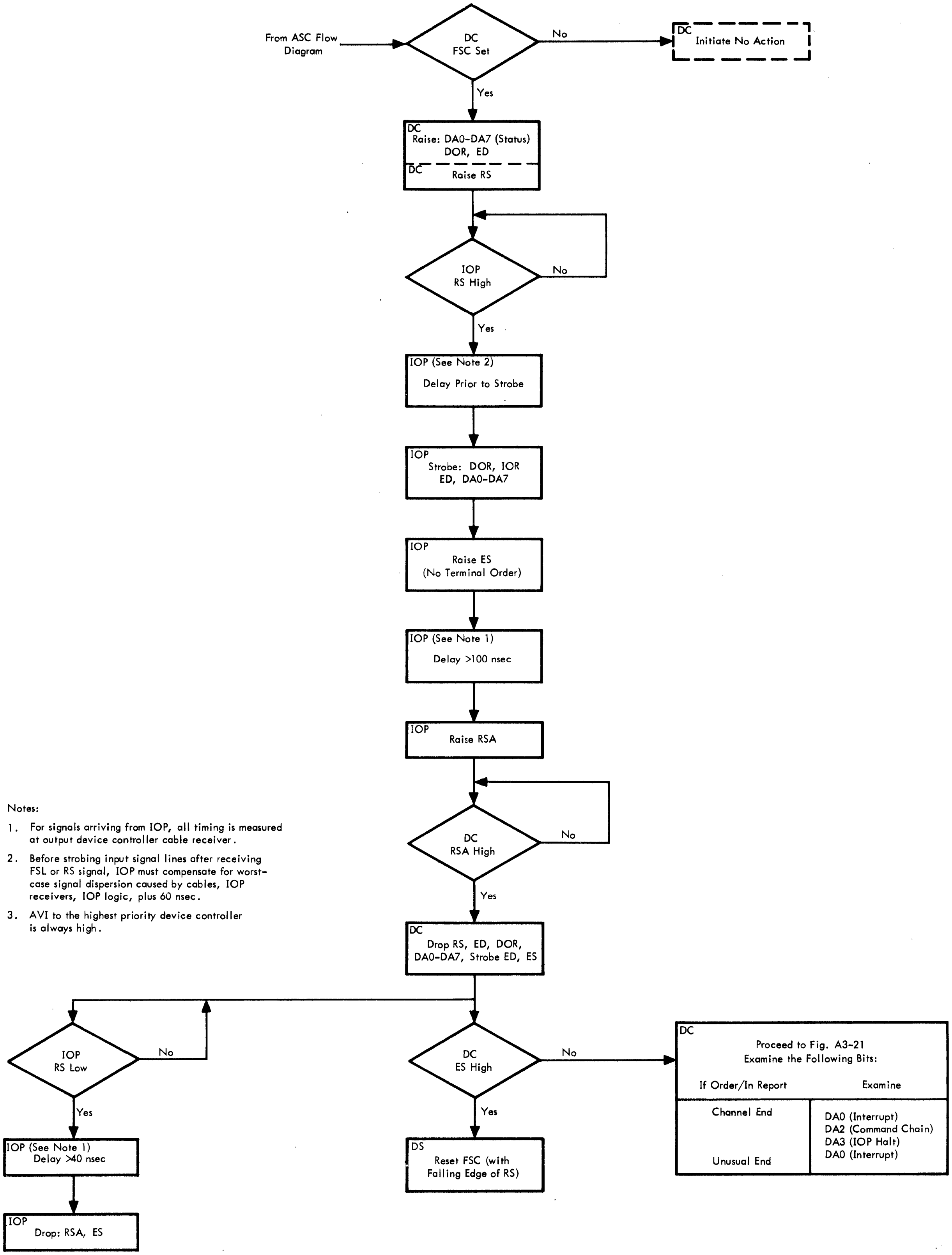
Figure A3-18. Data Output, Signal Flow Diagram



Notes:

1. For signals arriving from IOP, all timing is measured at output of device controller cable receiver.
2. Before strobing input signal lines after receiving FSL or RS signal, IOP must compensate for worst-case signal dispersion caused by cables, IOP receivers, IOP logic, plus 60 nsec.
3. AVI to the highest priority device controller is always high.

Figure A3-19. Order Output, Signal Flow Diagram



Notes:

1. For signals arriving from IOP, all timing is measured at output device controller cable receiver.
2. Before strobing input signal lines after receiving FSL or RS signal, IOP must compensate for worst-case signal dispersion caused by cables, IOP receivers, IOP logic, plus 60 nsec.
3. AVI to the highest priority device controller is always high.

Figure A3-20. Order Input, Signal Flow Diagram

A3-21 TERMINAL ORDER IMPLEMENTATION

A Terminal Order (TO) is a data transmission from the IOP to the device controller. A TO may conclude certain other data exchanges. Terminal Orders are used during DOUT, DIN, OOUT, and OIN operations. The DIN and DOUT cycles may consist of more than one byte. The end data line, ED, may be controlled by both the IOP and the DC, so either may determine the number of bytes exchanged during a service cycle. For example, the DC may ask for a four byte cycle, but operations may be aborted by the IOP if the IOP needs to transmit a TO immediately.

The IOP may issue a TO for any of the following reasons:

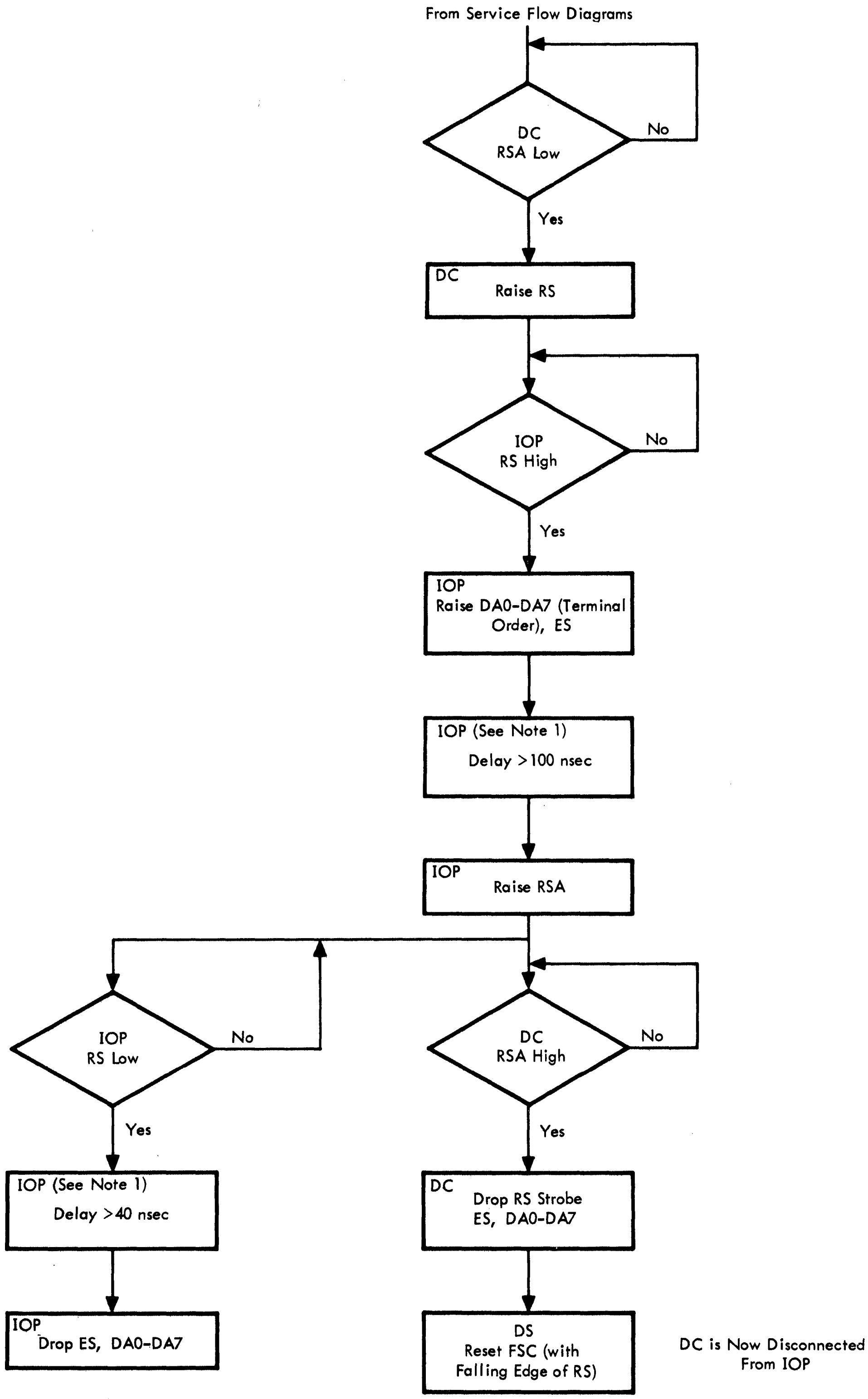
(a) To request the generation of an Interrupt request by the DC.

(b) To signal count done to the DC.

(c) To signal IOP Halt. In conjunction with this, the controller may be instructed to ignore the last byte of data. Signal flow during the execution of a TO is shown in figure A3-21.

A3-22 OVERALL LOGIC DIAGRAM

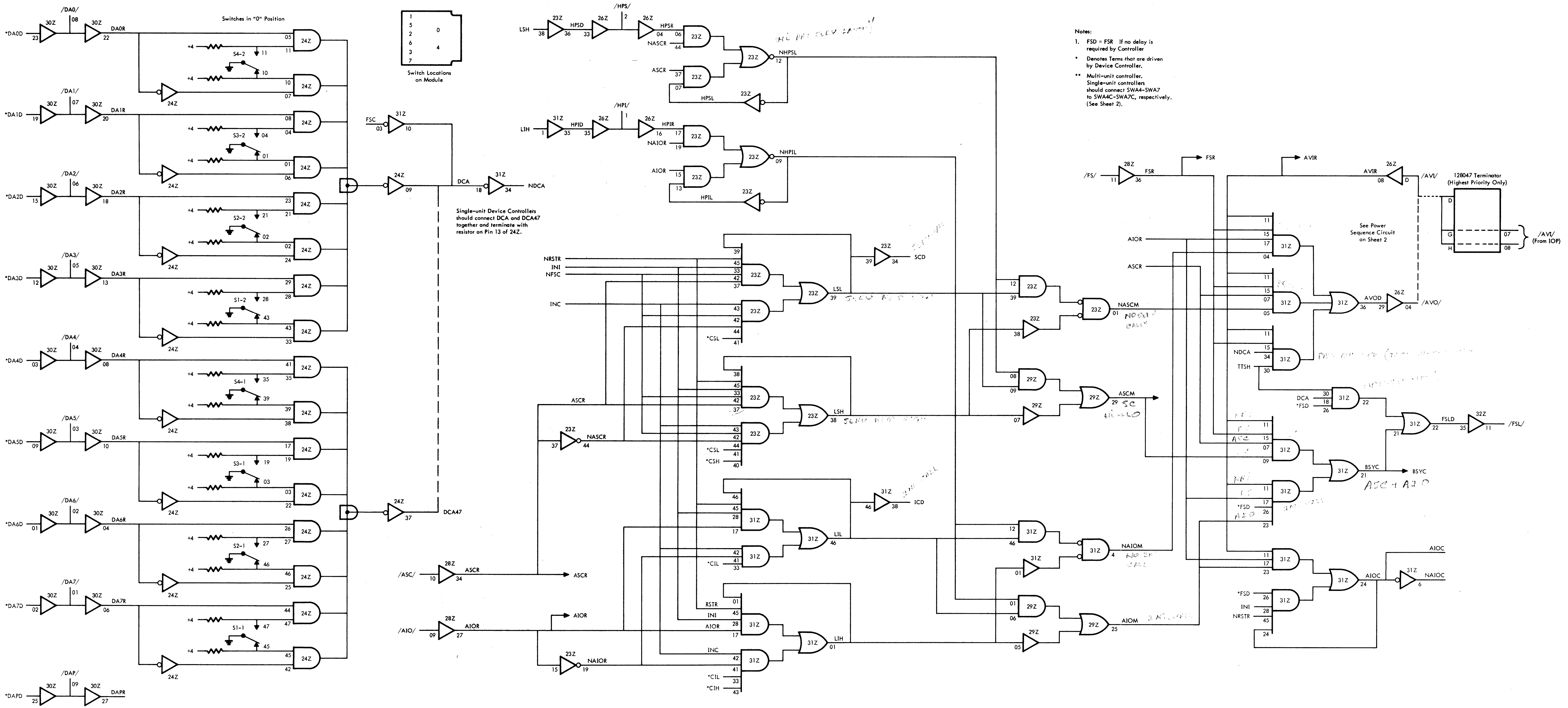
The overall logic diagram of the Model 7900 Device Subcontroller is shown in figure A3-22.



Notes:

1. For signals arriving from IOP, all timing is measured at output of device controller cable receiver.
2. AVI to the highest priority device controller is always high.

Figure A3-21. Terminal Order, Signal Flow Diagram



Notes:

1. FSD = FSR If no delay is required by Controller

* Denotes Terms that are driven by Device Controller.

** Multi-unit controller. Single-unit controllers should connect SWA4-SWA7 to SWA4C-SWA7C, respectively. (See Sheet 2).

Figure A3-22. Model 7900 Device Subcontroller, Logic Diagram (Sheet 1 of 2)

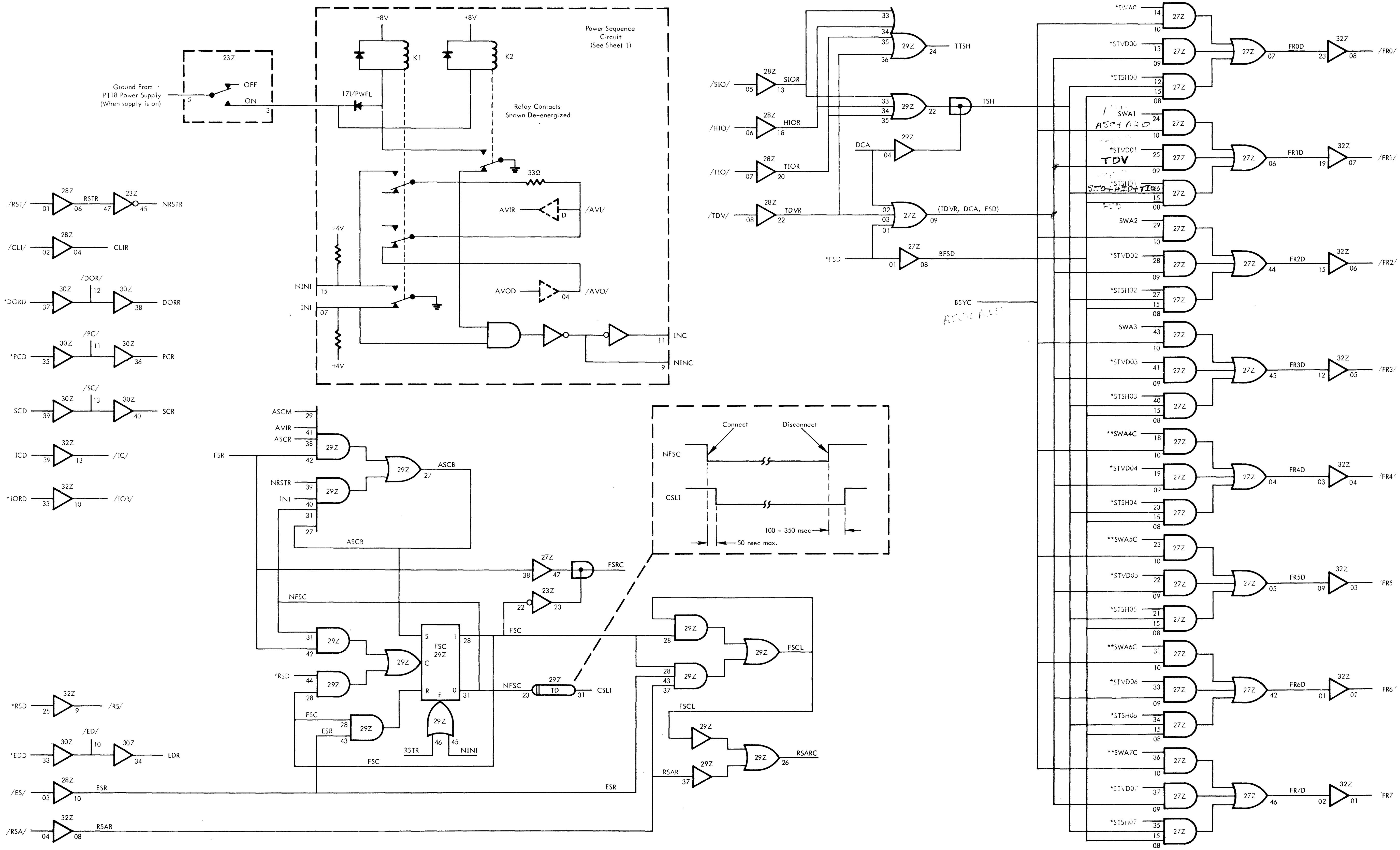


Figure A3-22. Model 7900 Device Subcontroller, Logic Diagram (Sheet 2 of 2)

A-IV. INSTALLATION AND MAINTENANCE

A4-1 INSTALLATION

The nine DS logic modules are installed in slots 23 through 32 on the bottom module rack of the associated device controller chassis. Figure A4-1 is a placement chart showing module locations in a device controller chassis. Documentation supplied with the device controller provides complete installation data for the DC, including intercabling details.

A4-2 MAINTENANCE

The absence of moving parts in the DS obviates the need for mechanical maintenance. Performance evaluation tests for individual logic modules are described in documents listed in Section A-VI of this manual.

A4-3 DIAGNOSTIC PROGRAMS

Diagnostic routines have been developed by XDS for exercising the device controller and subcontroller under simulated operating conditions. The XDS publication numbers of several typical test programs are listed in Section A-V of this manual.

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
AT12	LT43	AT11	LT41	AT10	LT24	AT17		LT26	LT25																						

Figure A4-1. DS Module Placement

A-V. REFERENCE DATA

A5-1 GENERAL

This section lists drawings and documents related to the Model 7900 Device Subcontroller. Reference documents are listed in Table A5-1.

Table A5-1. Model 7900 Device Subcontroller
Reference Documents

Drawing or Publication Number	Title
133021	Assembly, Device Subcontroller
133022	Specification, Design
133023	Installation Drawing
127040	Chart, Module Location
127042	Pin List
127043	Equations Logic

The publications listed in Table A5-2 contain descriptions of XDS Sigma computers, optional features, systems applications, and related equipment.

Table A5-2. Sigma Systems Documentation

Title	XDS Publication No.
Sigma Computer Systems, Interface Design Manual	900973
Sigma 2 Computer, Technical Manual	900630
Sigma 2 Computer, Reference Manual	900964
Sigma 2 CPU, Documentary Supplement (Model 8001)	65-78-S07
Sigma 2 Symbol, Reference Manual	901051
Sigma 2 Stand-Alone Systems, Operations Manual	901047
Sigma 5 Computer, Reference Manual	900959
Sigma 5 Computer, Technical Manual	901172
Sigma 5/7 1400 Series Simulator, General Information	647708
Sigma 5/7 Stand-Alone Systems, Operations Manual	901053
XDS Sigma: New Techniques in Computer Development	640604
Sigma 7 Computer, Reference Manual	900950
Sigma 7 Computer, Technical Manual (4 volumes)	901060
Sigma 7 Basic Control Monitor, Reference Manual	900953
Sigma 7 FORTRAN IV-H, General Information	647217
Sigma System Interface Units (SIU)	642801
Sigma Data Communications Equipment	643311
Sigma Keyboard Printers, Models 7010/7011, Reference Manual	900974
Sigma 7-Track Mag Tape Systems, Models 7361/7362/7371/7372, Reference Manual	900978
Sigma Graph Plotters, Models 7530/7531, Reference Manual	901194
IC Digital Logic Modules, T Series, Description and Specifications	645103

Table A5-3 lists the titles and XDS publication numbers of several diagnostic programs that are used to exercise Sigma computer systems.

Table A5-3. Typical Sigma Diagnostic Programs

Title	XDS Publication No.
Diagnostic Program Manual, Sigma 2 Line Printer Test	901159
Diagnostic Control Program, Sigma 2 Peripheral Devices	900839
Diagnostic Program Manual, Sigma 2 Paper Tape Reader/ Punch System Test	901151
Diagnostic Controlled Program, Sigma 5/7 Computer Peripheral Devices	900712
Diagnostic Program Manual, Sigma 5/7 Paper Tape Reader/Punch System Test	901122

A-VI. MODULE DATA SHEETS

A6-1 INTRODUCTION

This section of the manual is devoted to information concerning the T series modules employed in the logic circuits. Included are descriptions, component placement drawings, logic and schematic drawings, and parts lists.

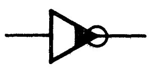
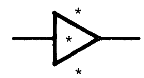
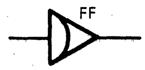
The module data sheets, listed in Table A6-1 for the standard Model 7900 Subcontroller are reproduced in the subsequent pages of this section of the manual.

The logic diagrams presented on the module data sheets employ XDS logic, as contrasted with the MIL-STD-806B logic presented in other portions of this manual. Accordingly, figure A6-1 is provided as a means of translating the XDS logic into the more familiar MIL-STD-806B logic.

Table A6-1. Module Data Sheets

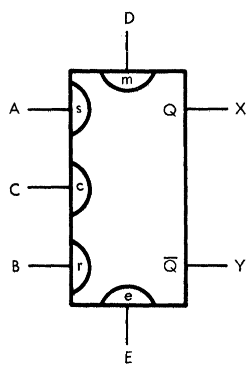
Module	Title
AT10	Cable Receivers
AT11	Cable Receivers/Drivers
AT12	Cable Drivers
AT17	Cable Drivers/Receivers
LT24	Logic Elements
LT25	Logic Elements
LT26	Logic Elements
LT41	Logic Elements
LT43	Logic Elements

OTHER AMPLIFIERS

XDS SYMBOLS	MIL-STD-806B EQUIVALENT
 Interface Cable Driver (on AT14 Module);  Interface Cable Receiver (on AT15 Module)	 *Letter is placed inside, above, or Below Symbol to denote function
 Clock Driver;  Interface Buffer;  Emitter Follower (on DT12/13 Modules)	

XDS IC FLIP-FLOP

XDS SYMBOLS



Signal Relationships:

$X = \overline{Y} = D + AD$

(C is falling edge of clock pulse)

$Y = \overline{X} = E + BC\overline{A}$

Terminal Designations

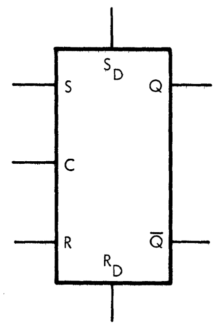
- m = "Mark" input (Unclocked Set input)
- e = "Erase" input (Unclocked Set input)
- s = Set input (Must be Clocked)
- r = Reset input (Must be Clocked)
- c = Clock input (Falling edge of Clock is used)
- Q = Set output
- $\overline{Q}$ = Reset Output

Truth Table

Period n		n+1
s	r	Q
0	0	Q^n
0	1	0
*1	0	1
*1	1	1

*Note the unique characteristic of the XDS flip-flop: the set input, when True, always causes the Q output to go True (when clocked), regardless of the state of the reset input. Mark and erase inputs, however, always override set and reset inputs. When both mark and erase are True simultaneously both outputs are False until one input goes False; the flip-flop then assumes the state determined by the other input, which was True last. Inputs must be wired False (grounded) when not used. Reset input is wired True (left open) in set-True-overrides-reset applications.

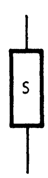
MIL-STD-806B EQUIVALENT



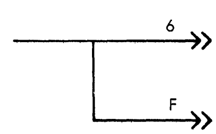
Terminal Designators:

- S_D = set direct (equivalent to XDS m)
- R_D = reset direct (equivalent to XDS e)
- S = set (equivalent to XDS s)
- R = reset (equivalent to XDS r)
- C = clock (equivalent to XDS c)
- Q = 1 output
- $\overline{Q}$ = 0 output

TERMINATORS

XDS SYMBOL	MIL-STD-806B EQUIVALENT
 Line Terminator (absorbs 5 Unit Leads)	

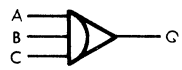
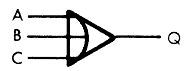
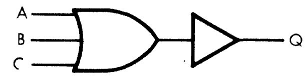
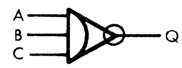
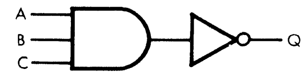
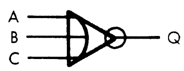
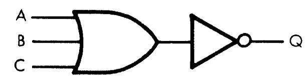
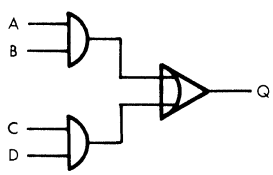
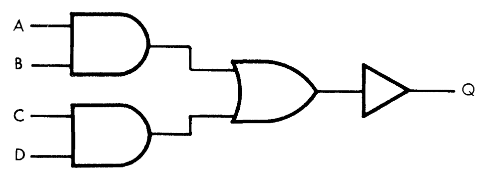
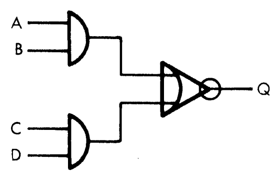
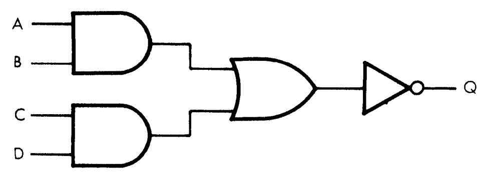
CABLE CONNECTORS



Front Edge Cable Connectors

Figure A6-1. Conversion of XDS Logic to MIL-STD-806B Logic (Sheet 1 of 3)

GATES COMBINED WITH LOGIC AMPLIFIERS

	XDS SYMBOLS		MIL-STD-806B EQUIVALENT
Buffered AND Gate (BAND)		$Q = A \cdot B \cdot C$	
Buffered OR Gate		$Q = A + B + C$	
NAND Gate		$\overline{Q} = A \cdot B \cdot C$ or $Q = \overline{A \cdot B \cdot C}$ or $Q = \overline{A}+\overline{B}+\overline{C}$	
NOR Gate		$\overline{Q} = A + B + C$ or $Q = \overline{A + B + C}$ or $Q = \overline{A} \cdot \overline{B} \cdot \overline{C}$	
Buffered AND/OR Gate		$Q = AB + CD$	
Inverted AND/OR Gate (AND/NOR)		$\overline{Q} = AB+CD$ or $Q = \overline{AB+CD}$ or $Q = (\overline{A}+\overline{B})(\overline{C}+\overline{D})$	

LOGIC FUNCTIONS FORMED AT OUTPUTS

A T Series feature is the Logic Function created when two or more Amplifiers or Flip-Flops are tied directly together. The rule is that any element having a false output will cause all outputs connected together to be false.

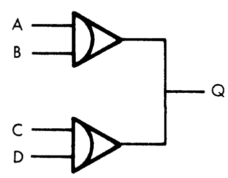
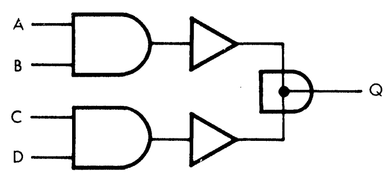
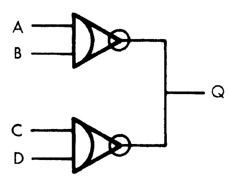
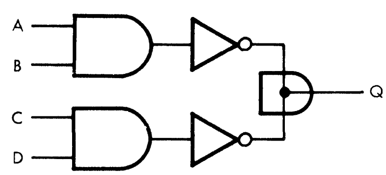
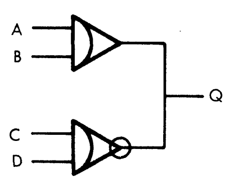
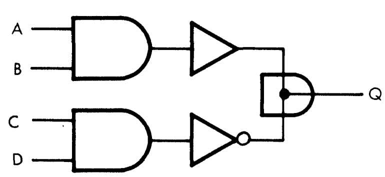
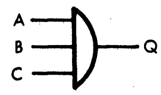
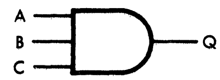
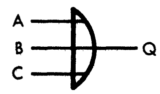
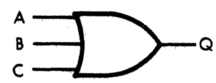
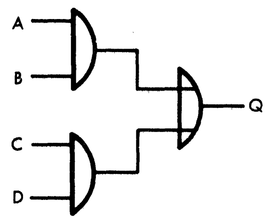
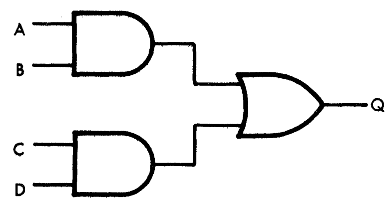
XDS SYMBOLS		MIL-STD-806B EQUIVALENT
	$Q = A \cdot B \cdot C \cdot D$ or $\overline{Q} = \overline{A}+\overline{B}+\overline{C}+\overline{D}$	
	$Q = (\overline{AB})(\overline{CD})$, or $Q = (\overline{A}+\overline{B})(\overline{C}+\overline{D})$, or $\overline{Q} = AB+CD$	
	$Q = (AB)(\overline{CD})$ or $Q = AB(\overline{C}+\overline{D})$	

Figure A6-1. Conversion of XDS Logic to MIL-STD-806B Logic (Sheet 2 of 3)

GATES WITHOUT LOGIC AMPLIFIERS

	XDS SYMBOLS		MIL-STD-806B EQUIVALENT
AND Gate		$Q = A \cdot B \cdot C$	
OR Gate		$Q = A + B + C$	
AND/OR Gate		$Q = A \cdot B + C \cdot D$	

LOGIC AMPLIFIERS

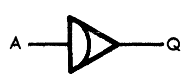
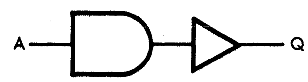
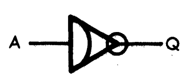
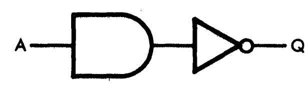
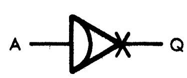
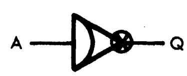
	XDS SYMBOLS			MIL-STD-806B EQUIVALENT
Buffer			$Q = A$	
Inverter			$\overline{Q} = A$ or $Q = \overline{A}$	
Without pull-up resistor on the Module	 Buffer	 Inverter		Pull-up resistors connected externally add note to symbol shown above

Figure A6-1. Conversion of XDS Logic to MIL-STD-806B Logic (Sheet 3 of 3)

SDS XDS Xerox Data Systems
Formerly
Scientific Data Systems

MODULE DATA SHEET

CABLE DRIVERS AND RECEIVERS

AT10,AT11,AT12

AT10, ASSY NO. 123018; AT11, ASSY NO. 123019; AT12, ASSY NO. 124629

These modules provide for high speed transmission and reception of logic level changes via a 33 ohm cable system, over distances up to 200 feet. The same modules can be used with a 93 ohm cable system and the ET24 BNC Connector Tray for distances up to 3,000 feet.

A cable of 14 individually shielded conductors can be clamped to either side of the front edge of one of these modules to mate with etch terminals. A second 14-conductor cable can be clamped to the other side of the front edge. Corresponding terminals on opposite sides of the front edge are connected together through the card. Thus two shielded 14-conductor cables (or 1 cable and a Model ET13 dummy load) can be connected to each module, as shown in Figure 1, below.

The Model ET11 cable connector must be used, and Model ET12 cable is recommended. Model ET10 and ET14 cable/connector assemblies are available. (See catalog 64-51-15).

One module type contains 14 identical cable receivers (AT10), one contains 14 drivers (AT12), while the third (AT11) has 14 pairs of driver-receiver circuits, each of which share a common pair of front-edge connectors (Fig. 3). The AT11 module reduces rack space and cable requirements in 2-way non-simultaneous communication by combining drivers and receivers on one card.

The AT10, AT11, and AT12 modules are electrically compatible with the similar AJ10, AJ11, and AJ12 modules, and provide a convenient method of interfacing T Series logic with J Series logic. There is a logical inversion in going through an AJ driver-receiver chain, but no inversion in going through the AT chain.

Cable Driver Circuit

The cable driver circuit is an emitter follower which accepts standard T Series logic level input and converts level changes to nominal 0v and +2v logic level output without inversion.

Driving capability depends on cable attenuation, which is a function of cable length. Input to cable driver must be standard T Series 0v to +4v logic levels. Back panel logic wiring at cable driver input should not exceed 18 inches. A line terminating resistor may not be connected to the input line. Any number of cable drivers can be connected to the same cable, but only one can be raised to the True level at any given time, since output voltages are additive.

Cable Receiver Circuit

The cable receiver circuit detects an input signal greater than nominal +.54v threshold. Output drive capability is 14 unit loads. The output signal is logically identical with the input signal. As many as 25 cable receivers can be connected to the same cable because input current and capacitance are so low. All receivers connected to the cable are activated simultaneously by the signal on the cable.

INSTALLATION CONSIDERATIONS

An AT10, AT11, or AT12 module requires only 1 module space provided that adjacent modules in the mounting case are not also cable driver/receivers. Another type of module may be placed between each pair of AT modules so that no space is wasted.

In any system which uses cables between cabinets, the logic ground and power ground of all cabinets must be properly interconnected independently of the cable shield. Otherwise the cable shield acts as a ground return if it offers the lowest impedance path between the two separate ground systems. Noise pulses traveling down the shield between the two grounds can couple to the logic signal line and cause improper triggering at the receivers.

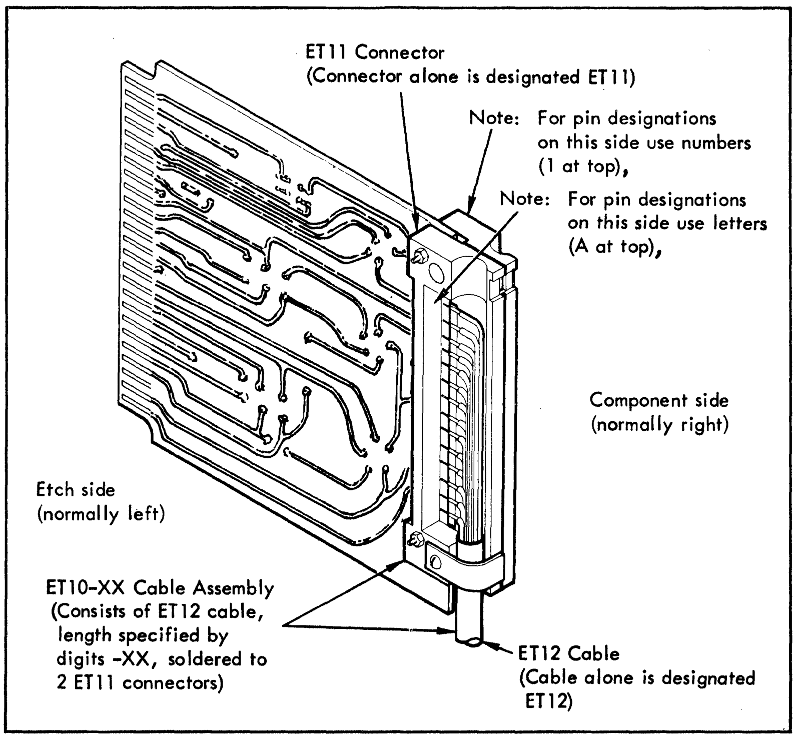


Fig. 1. AT12 Module, Showing The Several Cable And Connector Options

Publication Number 901211C
Revised Jan. 15, 1969

SPECIFICATIONS AND LOGIC DIAGRAMS

Max. Operating Frequency	10 Mc	Input Capacitance	8 pf max.
Internal Circuit Delay	20 nsec typical 40 nsec worst case	Max. No. Receivers per Cable	25
Input Logic Levels	Nom. 0v and +2v	Switching Threshold	+.54 volts ±.1v
Permissible Input Voltage Range	-1.5v to +4.4v	Output Drive Capability	14 Unit Loads (53.2 ma)
Input Current Required	50 μa per receiver input max.		

AT10

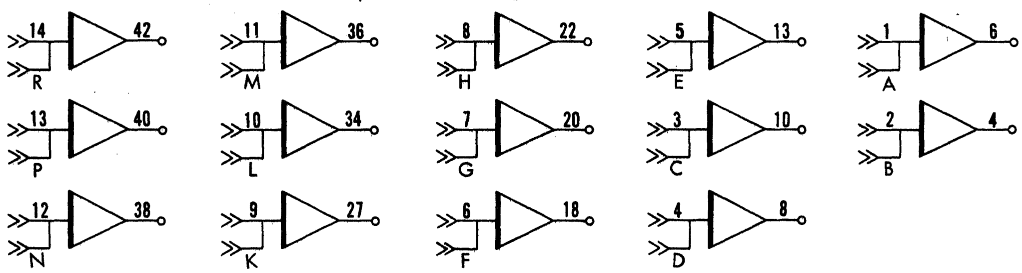


Fig. 2. Logic Diagram, AT10 Cable Receivers

Specifications: Drivers, same as Model AT12; Receivers, same as Model AT10

AT11

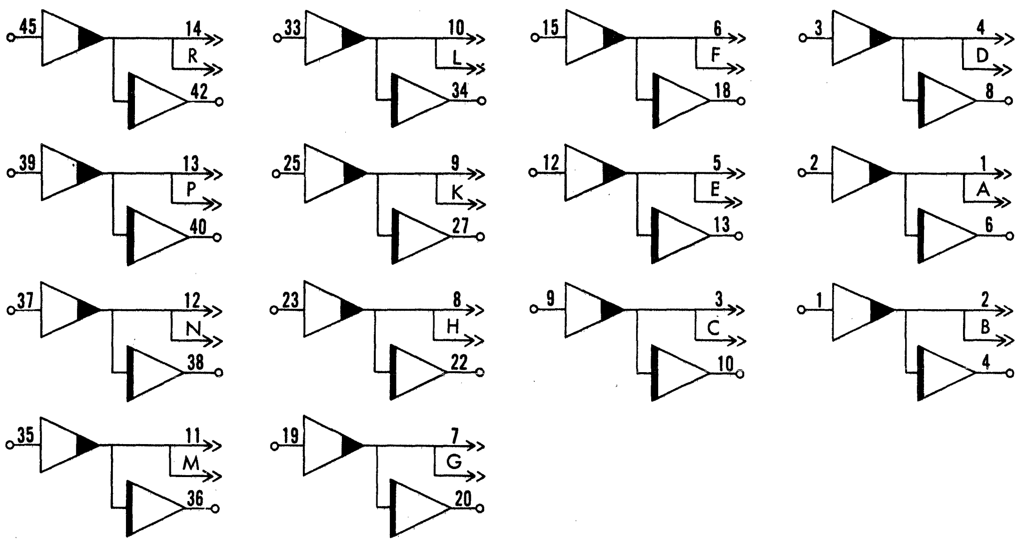


Fig. 3. Logic Diagram, AT11 Cable Drivers/Receivers

Max. Operating Frequency	10 Mc	Output Logic Levels	Nominal 0v and +2v
Internal Circuit Delay	5 nsec typical, 10 nsec worst case	Output Loading	Output must be loaded with 16.5 ohms to ground; load should be two 33 ohm cables in parallel or one 33 ohm cable and one 33 ohm dummy load (see ET10, ET11, ET12, ET13 module data sheet)
Input Logic Levels	Nominal 0v and +4v		
Permissible Input Voltage Range	-2v to +4v		
Input Current Required	9 Unit Loads (34.2 ma max.)		
Input Wiring Restrictions	No line terminator in parallel with input; No more than 18 in. wire to input		

AT12

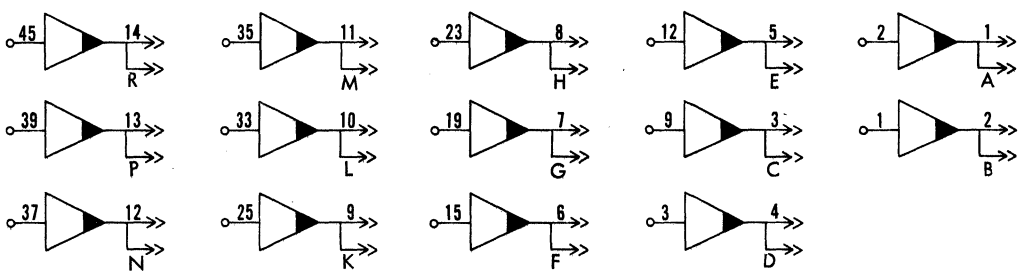


Fig. 4. Logic Diagram, AT12 Cable Drivers

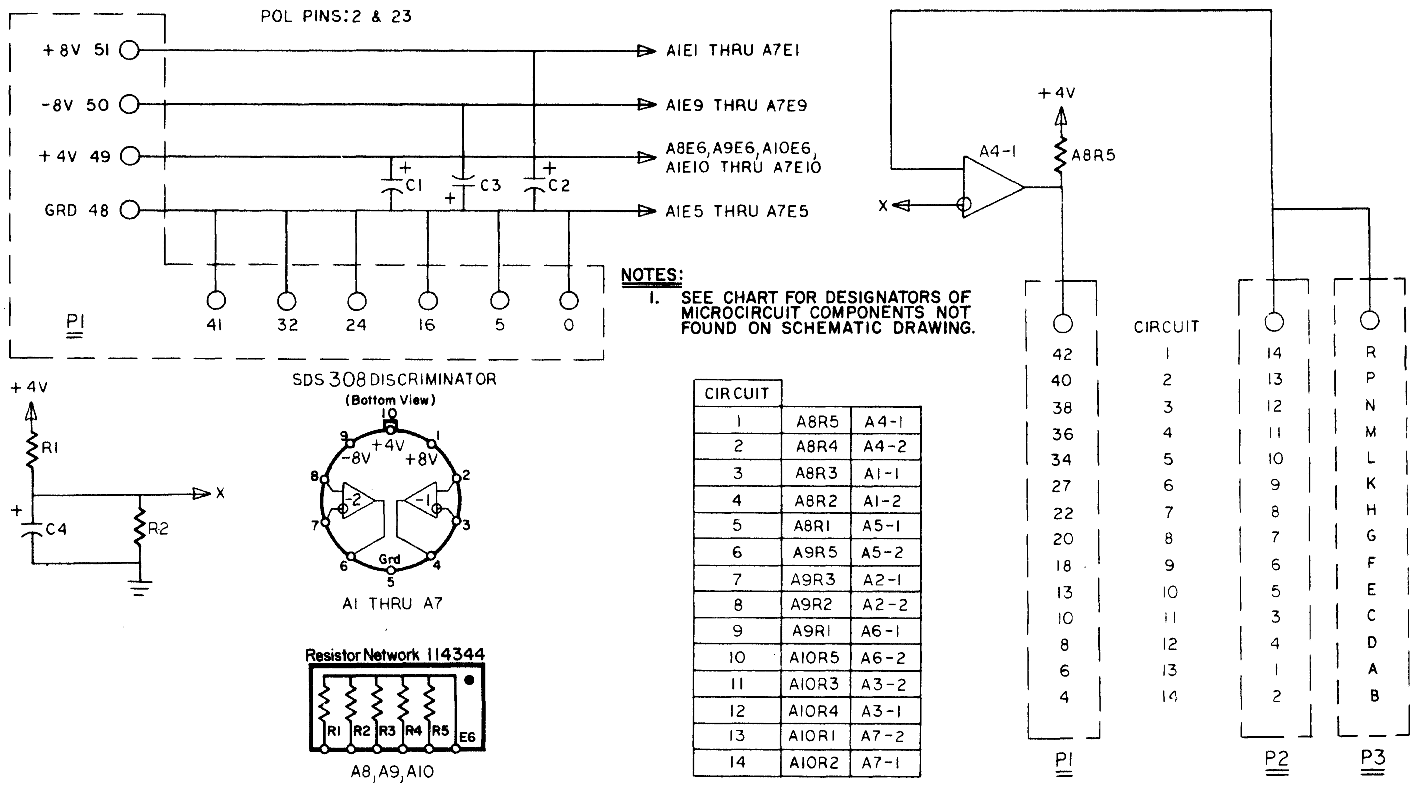
Power and Dissipation Specifications

POWER

Model	+8v	-8v	+4v Av. *	+4v Max.	Max. Dissipation
AT10	100 ma	100 ma	178 ma	230 ma	2.5 watts
AT11	485 ma	100 ma	878 ma	1.8 amp	4.5 watts
AT12	400 ma	0	700 ma	1.4 amp	4.0 watts

* Requirement for average system, based on 50% duty cycle.

MODEL AT10 SCHEMATIC



NOTES:

1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.

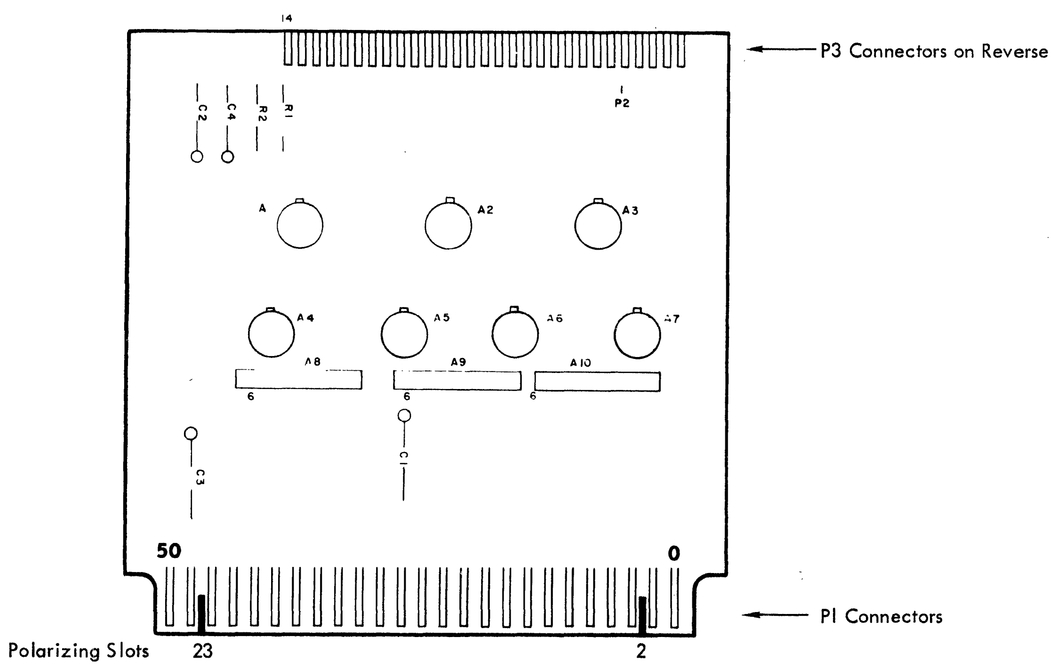
CIRCUIT		
1	A8R5	A4-1
2	A8R4	A4-2
3	A8R3	A1-1
4	A8R2	A1-2
5	A8R1	A5-1
6	A9R5	A5-2
7	A9R3	A2-1
8	A9R2	A2-2
9	A9R1	A6-1
10	A10R5	A6-2
11	A10R3	A3-2
12	A10R4	A3-1
13	A10R1	A7-2
14	A10R2	A7-1

P1	CIRCUIT	P2	P3
42	1	14	R
40	2	13	P
38	3	12	N
36	4	11	M
34	5	10	L
27	6	9	K
22	7	8	H
20	8	7	G
18	9	6	F
13	10	5	E
10	11	3	C
8	12	4	D
6	13	1	A
4	14	2	B

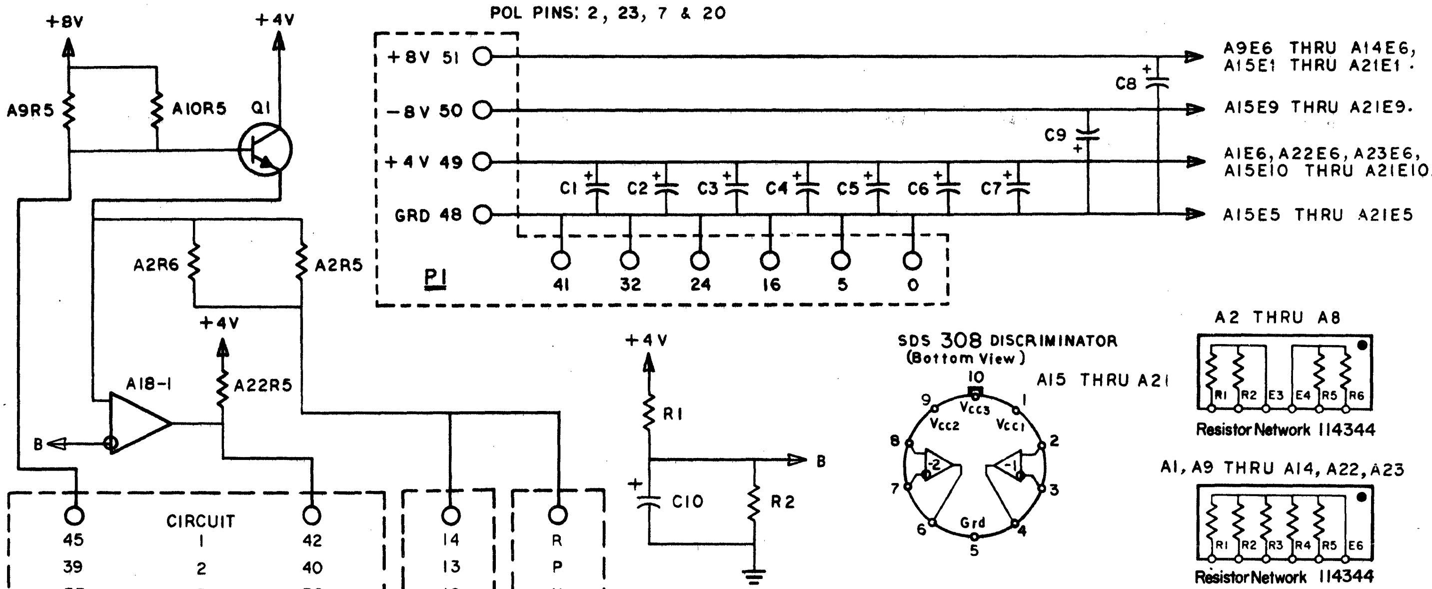
MODEL AT10 PARTS LIST

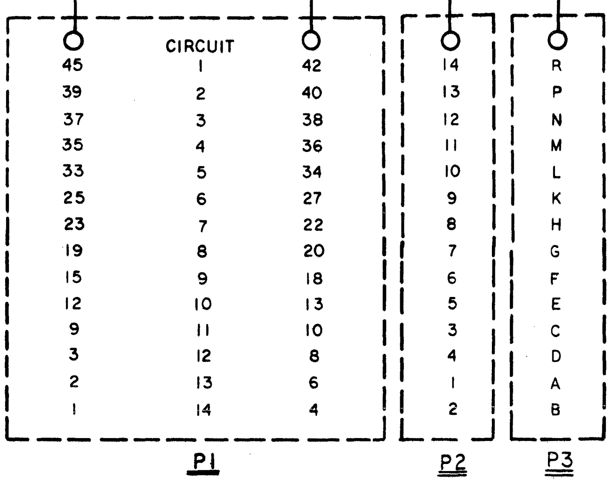
Item		Description	Designator	Qty.
1	Integrated Circuit	SDS 308	A1 thru A7	7
2	Capacitor, Tantalum	2.7 mfd ±20%, 15v	C1 thru C4	4
3	5-Resistor Network	560 ohms ±5%, 1/4 watt	A8 thru A10	3
4	Resistor, Film	158 ohms ±1%, 1/8 watt	R1	1
5	Resistor, Film	30.1 ohms ±1%, 1/8 watt	R2	1

MODEL AT10 SCREEN



MODEL AT11 SCHEMATIC





CIRCUIT	P1		P1	P2	P3
1	45		42	14	R
2	39		40	13	P
3	37		38	12	N
4	35		36	11	M
5	33		34	10	L
6	25		27	9	K
7	23		22	8	H
8	19		20	7	G
9	15		18	6	F
10	12		13	5	E
11	9		10	3	C
12	3		8	4	D
13	2		6	1	A
14	1		4	2	B

NOTES:

1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.

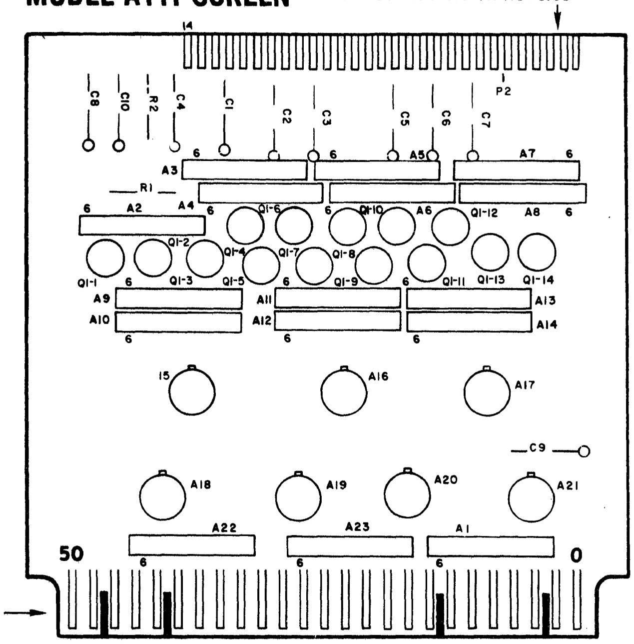
CIRCUIT						
1	A9R5	A10R5	A2R6	A2R5	A22R5	A18-1
2	A9R4	A10R4	A2R2	A2R1	A22R4	A18-2
3	A9R3	A10R3	A3R6	A3R5	A22R3	A15-1
4	A9R2	A10R2	A4R6	A4R5	A22R2	A15-2
5	A9R1	A10R1	A3R2	A3R1	A22R1	A19-1
6	A11R5	A12R5	A4R1	A4R2	A23R5	A19-2
7	A11R4	A12R4	A5R6	A5R5	A23R3	A16-1
8	A11R3	A12R3	A6R6	A6R5	A23R2	A16-2
9	A11R1	A12R1	A5R2	A5R1	A23R1	A20-1
10	A13R5	A14R5	A6R2	A6R1	A1R5	A20-2
11	A13R4	A14R4	A7R1	A7R2	A1R4	A17-1
12	A13R3	A14R3	A8R1	A8R2	A1R3	A17-2
13	A13R2	A14R2	A7R6	A7R5	A1R2	A21-1
14	A13R1	A14R1	A8R5	A8R6	A1R1	A21-2

MODEL AT11 PARTS LIST

Item		Description	Designator	Qty.
1	Integrated Circuit	SDS 308	A15 thru A21	7
2	Transistor	SDS 217	Q1	14
3	Capacitor, Tantalum	2.7 mfd ±20%, 15v	C1 thru C10	10
4	5-Resistor Network	33 ohm ±5%, 1/4 watt	A2 thru A8	7
5	5-Resistor Network	560 ohms ±5%, 1/4 watt	A1, A9 thru A14, A22, A23	9
6	Resistor, Film	158 ohms ±1%, 1/8 watt	R1	1
7	Resistor, Film	30.1 ohms ±1%, 1/8 watt	R2	1

MODEL AT11 SCREEN

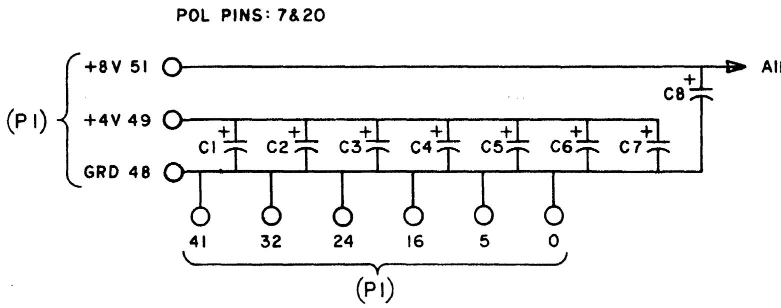
P3 Connectors on Reverse

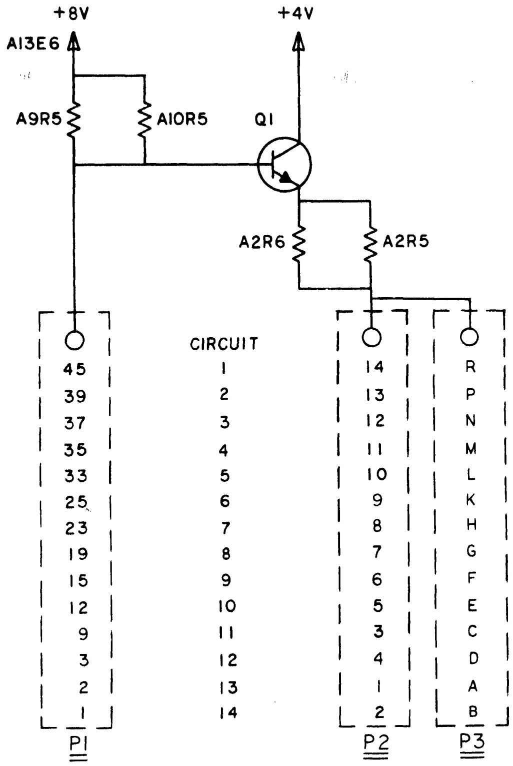


P1 Connectors

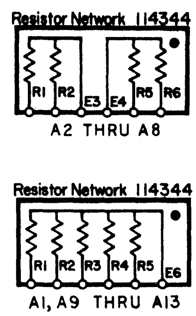
Polarizing Slots 23 20 7 2

MODEL AT12 SCHEMATIC





CIRCUIT				
1	A9R5	A10R5	A2R6	A2R5
2	A9R4	A10R4	A2R2	A2R1
3	A9R3	A10R3	A3R6	A3R5
4	A9R2	A10R2	A4R6	A4R5
5	A9R1	A10R1	A3R2	A3R1
6	A11R5	A12R5	A4R1	A4R2
7	A11R4	A12R4	A5R6	A5R5
8	A11R3	A12R3	A6R6	A6R5
9	A11R1	A12R1	A5R2	A5R1
10	A13R5	A1R5	A6R2	A6R1
11	A13R4	A1R4	A7R1	A7R2
12	A13R3	A1R3	A8R1	A8R2
13	A13R2	A1R2	A7R6	A7R5
14	A13R1	A1R1	A8R5	A8R6

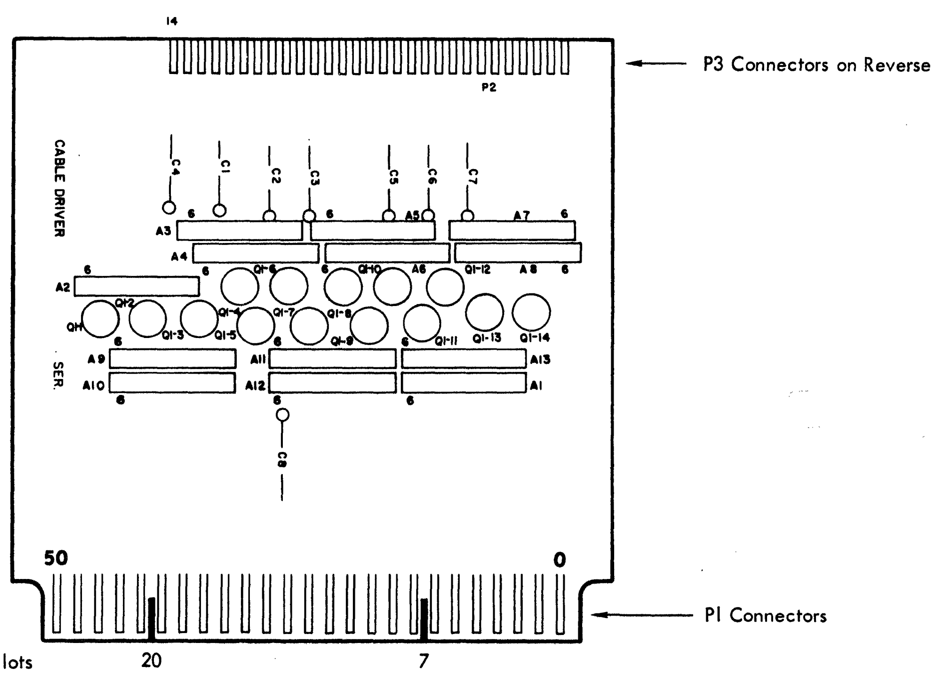


NOTES:
1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.

MODEL AT12 PARTS LIST

Item		Description	Designator	Qty.
1	Transistor	SDS 217	Q1	14
2	Capacitor, Tantalum	2.7 mfd ±20%, 15v	C1 thru C8	8
3	5-Resistor Network	33 ohms ±5%, 1/4 watt	A2 thru A8	7.
4	5-Resistor Network	560 ohms ±5%, 1/4 watt	A1, A9 thru A14	6

MODEL AT12 SCREEN



Printed in U.S.A.

SPECIAL PURPOSE LOGIC MODULE FOR SDS MODEL 7900 DEVICE SUBCONTROLLER

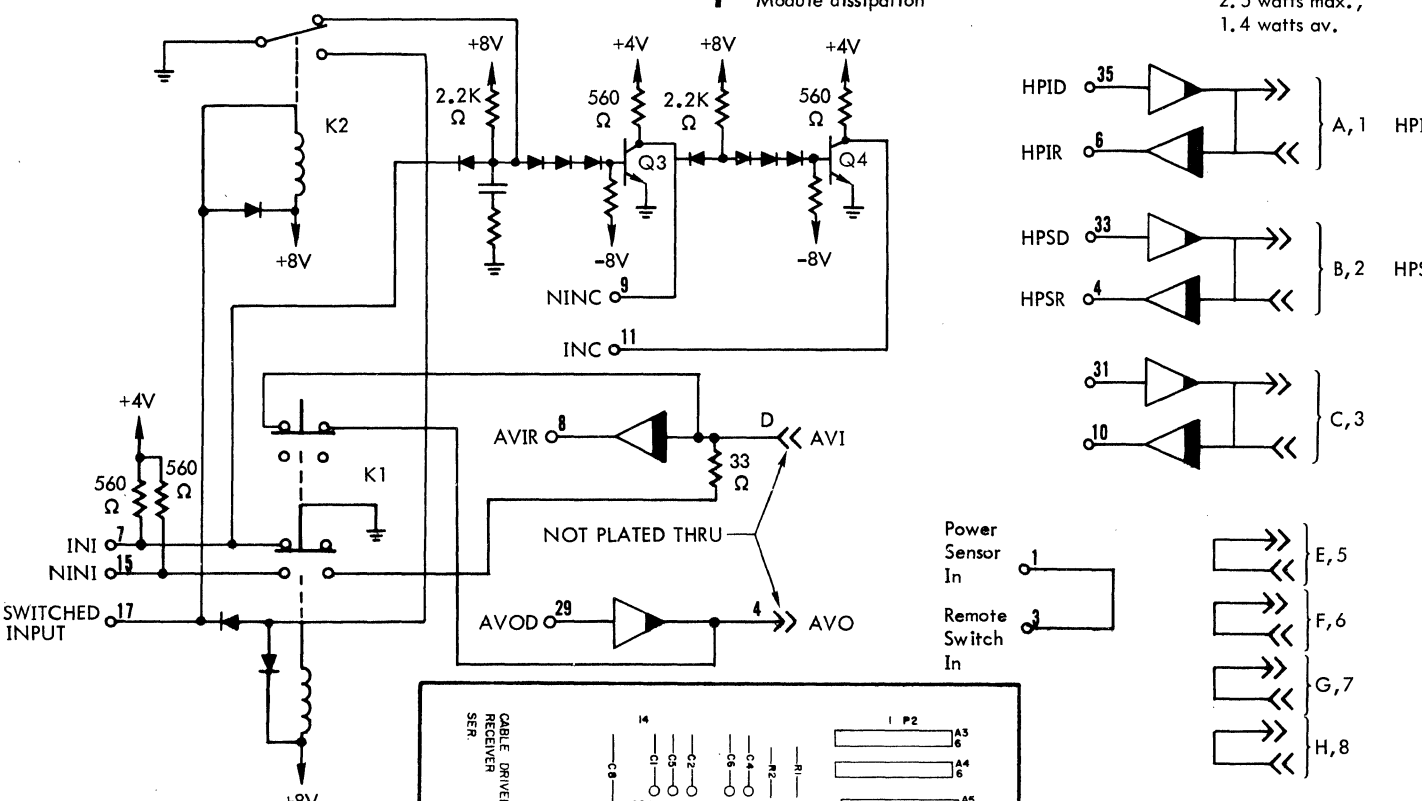
AT17

The AT17 is a special purpose module designed to function as part of the SDS Model 7900 Device Subcontroller (DS). It contains circuitry that includes relays, cable drivers, and receivers, which performs a portion of the DS function. The DS provides circuitry for connecting and disconnecting a Device Controller (DC) from a Sigma Computer IOP interface in a transient free manner when power is applied or removed from the Device Controller.

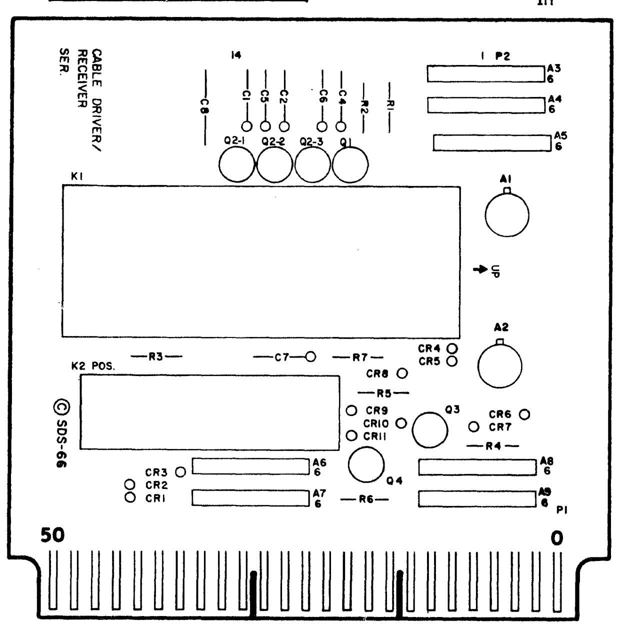
For detailed principles of operation refer to SDS Publication No. 900973, "SDS Sigma Computer Systems, Interface Design Manual", Section 3. The latter publication gives a timing diagram and definitions of signal functions.

The AT17 module occupies two card slots.

Maximum Operating Frequency of cable driver and receiver circuits (refer to AT10, AT11, AT12 data sheet for other specifications)	10 Mc
Relay Coil K1 must-operate current	120 ma max.
Relay K1 operate time	4.5 millisec typical
K1 Contact rating	limited by circuit (see schematic)
Relay Coil K2 must-operate current	30 ma max.
Relay K2 operate time	4.5 millisec. typical
K2 contact rating	limited by circuit (see schematic)
+4 volt supply	550 ma max. 285 ma av.
+8 volt supply	300 ma
-8 volt supply	50 ma
Module dissipation	2.5 watts max., 1.4 watts av.



MODEL AT17 SCREEN

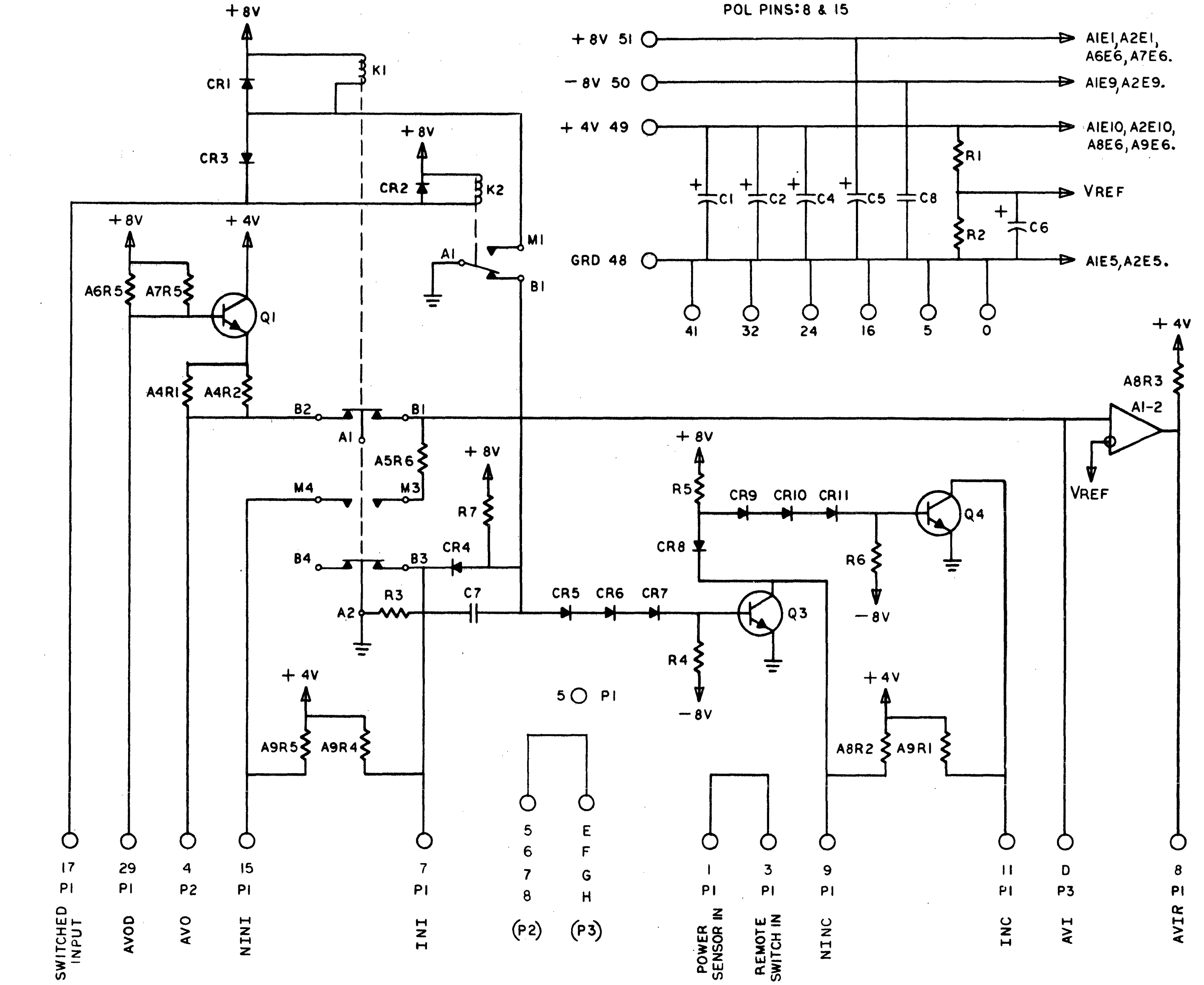


Note: Symbol —o is used to indicate back panel pin. Symbols —>> and —<< are used to indicate front edge cable connectors.

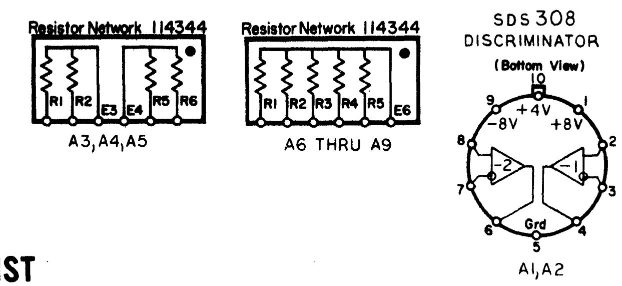
Polarizing Slots 15 8

Publication Number 901248A

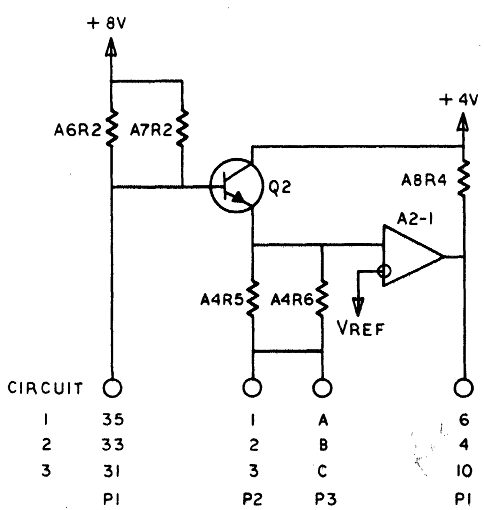
MODEL AT17 SCHEMATIC



NOTES:
1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.



CIRCUIT						
1	A6R2	A7R2	A4R5	A4R6	A8R4	A2-1
2	A6R3	A7R3	A3R5	A3R6	A8R5	A2-2
3	A6R4	A7R4	A3R1	A3R2	A9R2	A1-1



MODEL AT17 PARTS LIST

Item	Description		Designators	Qty.
1	Integrated Circuit	SDS 308	A1, A2	2
2	5-Resistor Network	33 ohms, ±5%, 1/4W	A3, A4, A5	3
3	5-Resistor Network	560 ohms, ±5%, 1/4W	A6, A7, A8, A9	4
4	Capacitor, Tantalum	2.7 MFD, ±20%, 15V	C1, C2, C4, C5, C6	5
5	Capacitor, Tantalum	.56 MFD, ±20%, 15V	C7	1
6	Capacitor, Mylar	.01 MFD, ±10%, 80V	C8	1
7	Diode	1N4154	CR1 thru CR11	11
8	Transistor	2N3013 or 2N2369	Q3, Q4	2
9	Transistor	2N3013	Q1, Q2	2
10	Relay	CX DP DK-MK Adams/Westlake MWB2645	K1	1
11	Relay	BP SPDT, Mercury Bridging, Adams/Westlake AWCA 16126	K2	1
12	Resistor, Film	120 ohms, ±5%, 1/4W	R1	1
13	Resistor, Film	43 ohms, ±5%, 1/4W	R2, R3	2
14	Resistor, Film	15K ohms, ±5%, 1/4W	R4, R6	2
15	Resistor, Film	910 ohms, ±5%, 1/4W	R5, R7	2

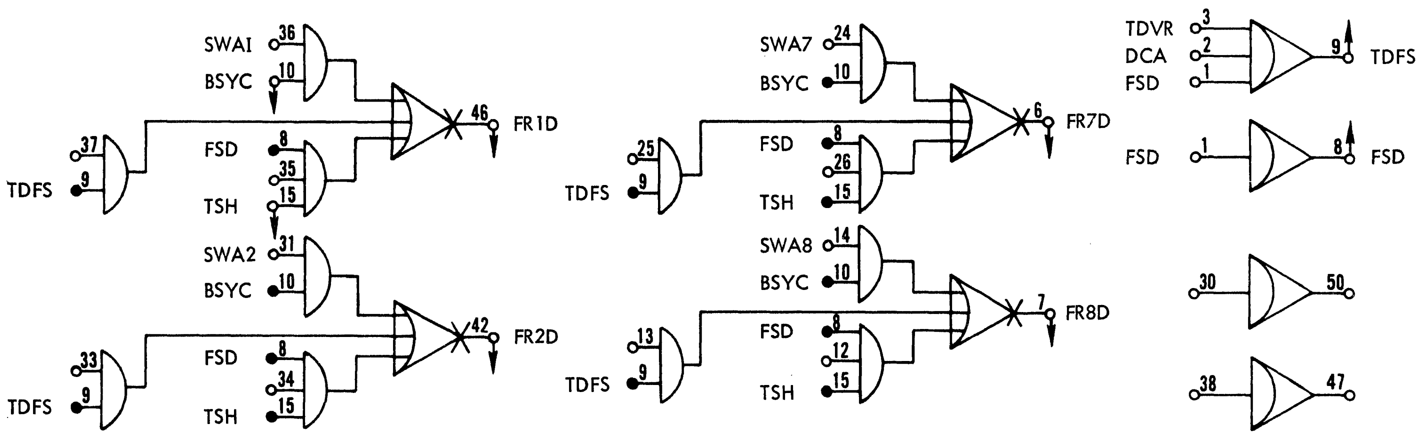
SPECIAL PURPOSE LOGIC MODULE FOR SDS MODEL 7900 DEVICE SUBCONTROLLER

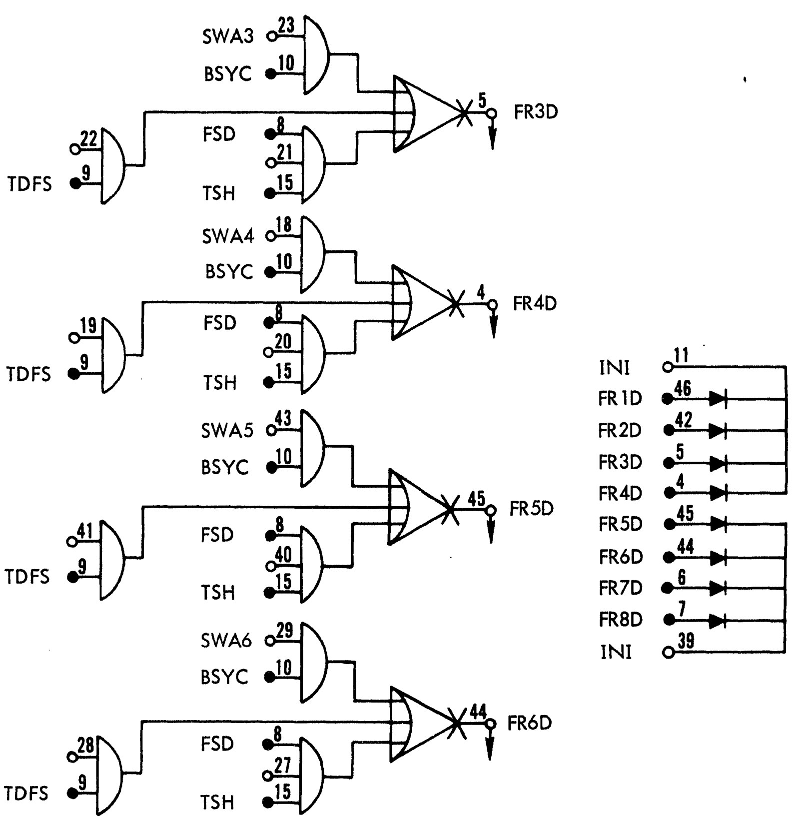
LT24

The LT24 is a special purpose module designed to function as part of the SDS Model 7900 Device Subcontroller. It contains eight buffered AND/ORs, one buffered 3-input AND, three straight-through buffers, and eight clamp diodes. The AND/OR inputs and the clamp diodes are extensively interconnected on the module, as shown in the logic diagram, to perform the special logic functions required.

Detailed principles of operation and definitions of logic terms are given in the SDS Sigma Interface Design Manual, SDS Publication No. 900973, Section 3.

Maximum Operating Frequency	10 Mc
Input Logic Levels	Logic 1: +4v Logic 0: 0v
Output Logic Levels	Logic 1: +4v Logic 0: 0v
Fan-out	Pins 46, 42, 5, 4, 45, 44, 6, 7: 13 unit loads when pins 11 and 39 are properly connected to signal INI (pin 7) on AT17 module. Pins 8 and 9: 6 unit loads ea. Pins 47 and 50: 14 unit loads ea.
Load imposed by inputs	Pins 10 and 15: 8 unit loads All others: 1 unit load ea.
Circuit Delay (each amplifier)	18 nsec typical 30 nsec worst case
+8 Volt Supply	95.2 ma
+4 Volt Supply	119 ma
Module Dissipation	1.24 watts

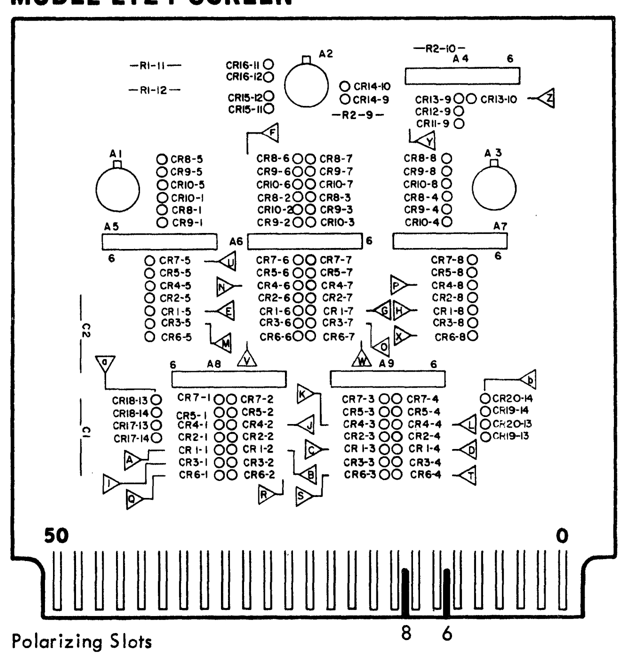




Notes:

1. Common connections on module are shown with arrow and numbered solid dot
2. X on output indicates that a load resistor (pull-up resistor) is not connected to the output.

MODEL LT24 SCREEN

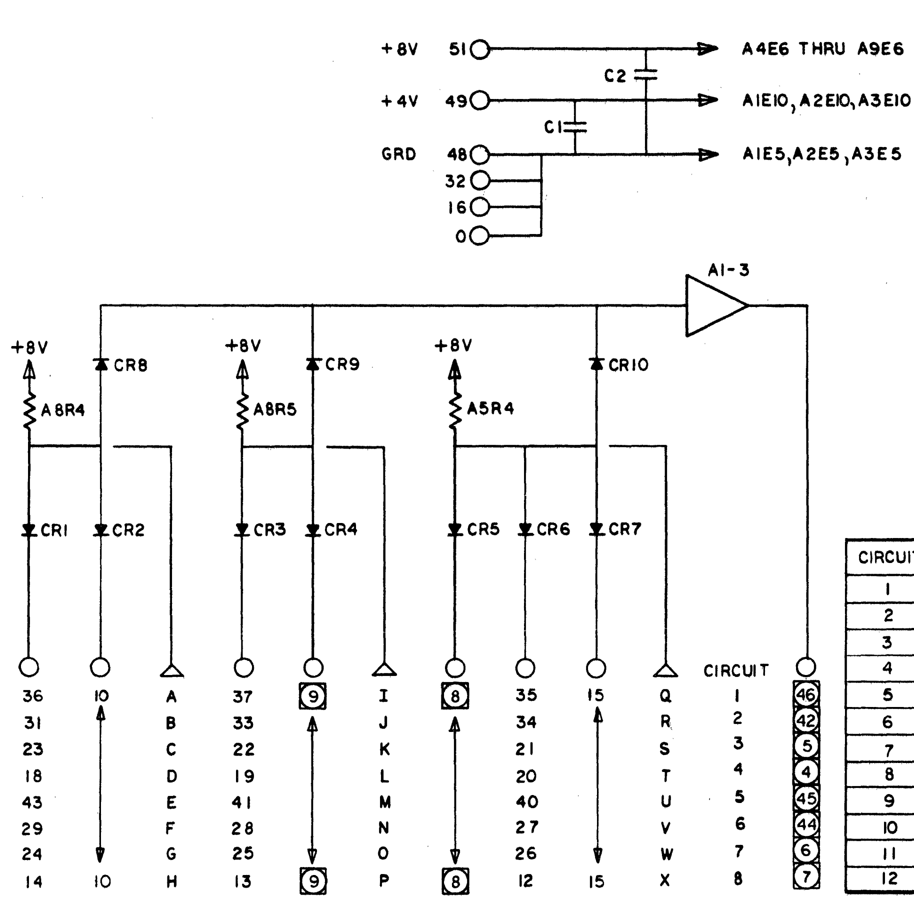


Polarizing Slots

Publication Number 901249A

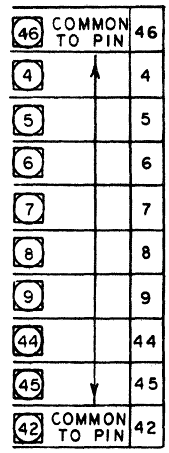
MODEL LT24 SCHEMATIC

POL PINS: 6 & 8



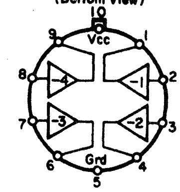
NOTES:

1.



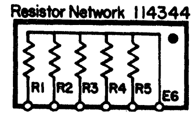
2. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.

SDS 306 BUFFER
(Bottom View)



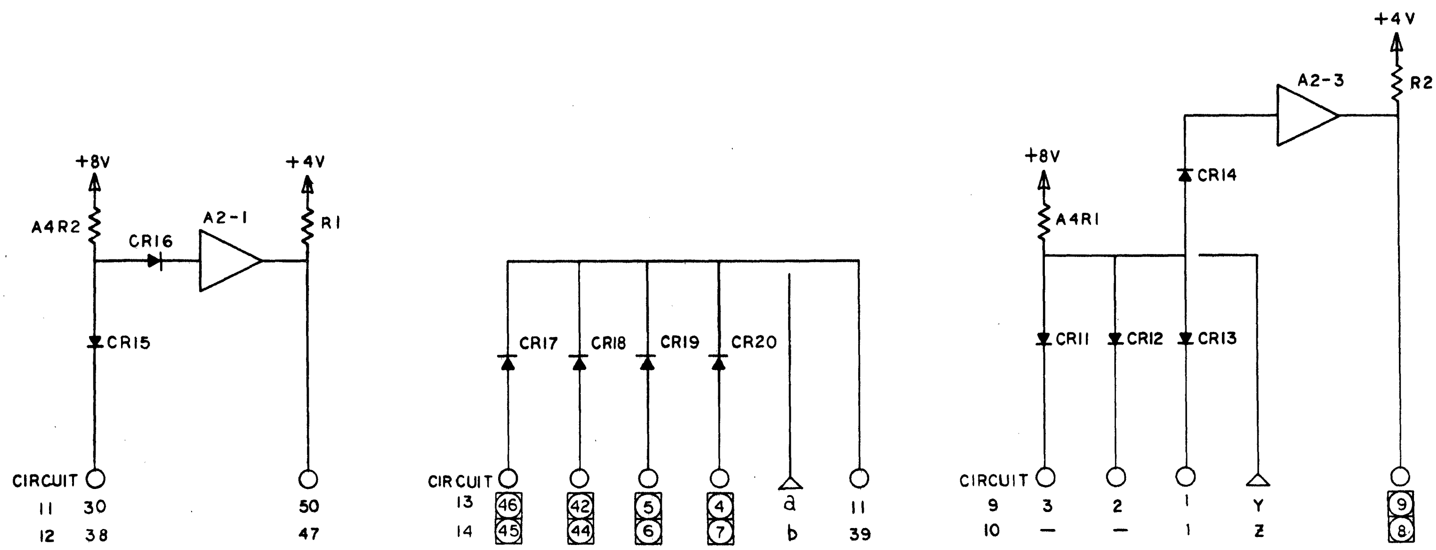
A1, A2, A3

Resistor Network 114344



A4 THRU A9

CIRCUIT								
1	A8R4	A8R5	A5R4			A1-3		
2	A8R3	A8R2	A8R1			A1-1		
3	A9R3	A9R2	A9R1			A3-4		
4	A9R4	A9R5	A7R5			A3-2		
5	A5R3	A5R2	A5R1			A1-4		
6	A6R3	A6R2	A6R1			A1-2		
7	A6R4	A6R5	A7R1			A3-3		
8	A7R4	A7R3	A7R2			A3-1		
9				A4R1			A2-3	
10				A4R5			A2-4	
11					A4R2			A2-1
12					A4R3			A2-2



MODEL LT24 PARTS LIST

Item	Description	Designators	Qty.
1	Integrated Circuit, Buffer SDS 306	A1, A2, A3	3
2	Diode, Switching, 1N4154	CR1 thru CR20	98
3	Capacitor, Mylar .01 MFD ±10%, 80v	C1, C2	2
4	5-Resistor, Network 2.2K ±5%, 1/4W	A4 thru A9	6
5	Resistor, Film 560 ohms ±5%, 1/4 W	R1, R2	4

SPECIAL PURPOSE LOGIC MODULE FOR SDS MODEL 7900 DEVICE SUBCONTROLLER

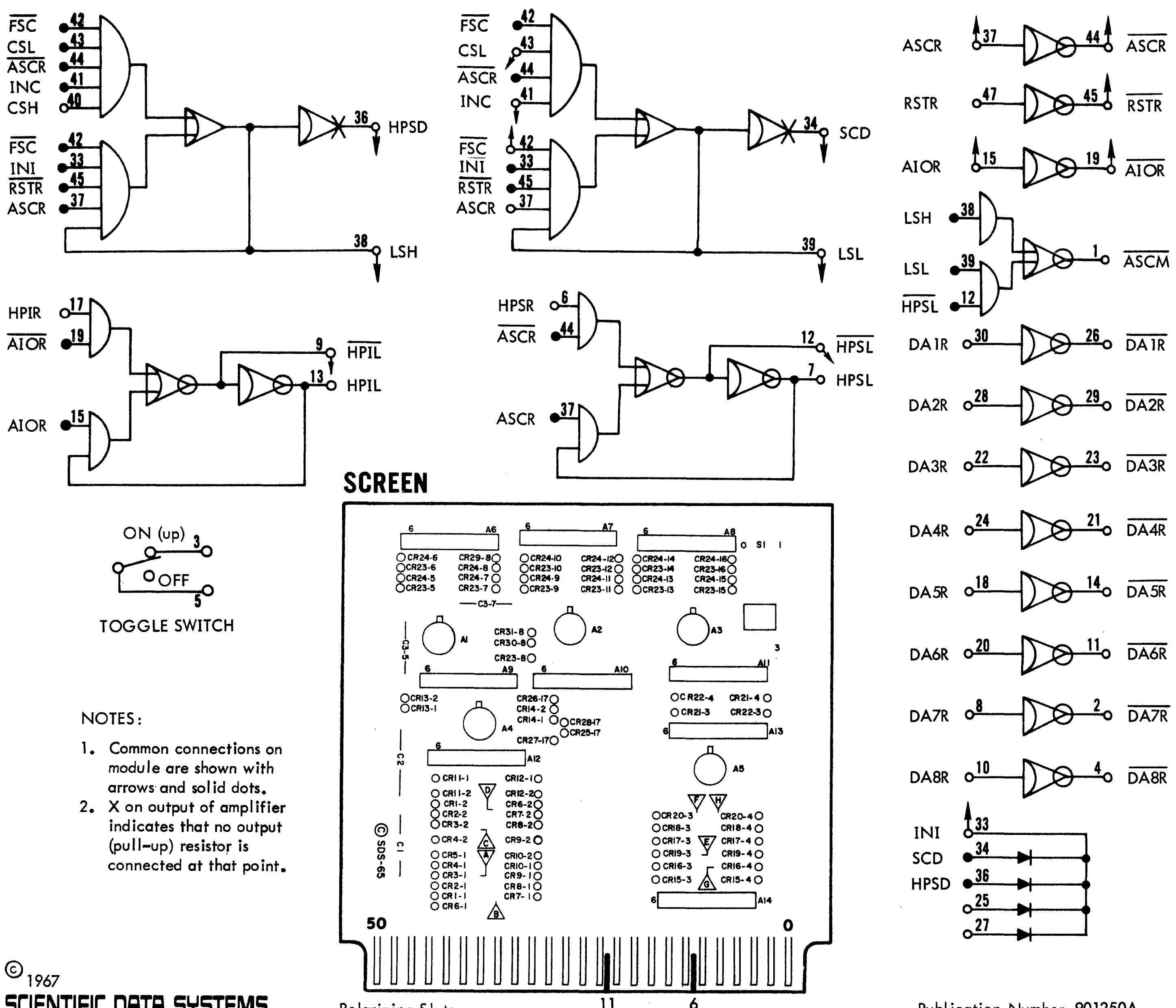
LT25

The LT25 is a special purpose module designed to function as part of the SDS Model 7900 Device Subcontroller. It contains four buffered latch circuits with AND/OR inputs, eleven inverters, one AND/OR-inverter gate, a manual toggle switch, and four clamp diodes. The circuits are extensively interconnected on the module as shown in the logic diagram.

Detailed principles of operation and definitions of logic terms are given in Section 3 of the SDS Sigma Interface Design Manual, SDS Publication No. 900973.

SPECIFICATIONS

Maximum Operating Frequency	10 Mc
Input Logic Levels	Logic 1: +4v Logic 0: 0v
Output Logic Levels	Logic 1: +4v Logic 0: 0v
Fan-out	Pins 12, 15, 19, 34, 36, 38, 39: 13 unit loads when pin 33 is connected to INI (pin 7) on AT17 module. Pin 44: 11 unit loads Pin 45: 12 unit loads All other outputs: 14 unit loads
Load imposed by inputs	Pins 37, 42: 4 unit loads ea. Pins 41, 43: 2 unit loads ea. All other pins except 3, 5: 1 unit load ea. (Pins 3 and 5 are toggle switch)
Circuit Delay (each amplifier)	18 nsec typical 30 nsec worst case
+8 Volt Supply	85 ma
+4 Volt Supply	301 ma
Module Dissipation	1.88 watts

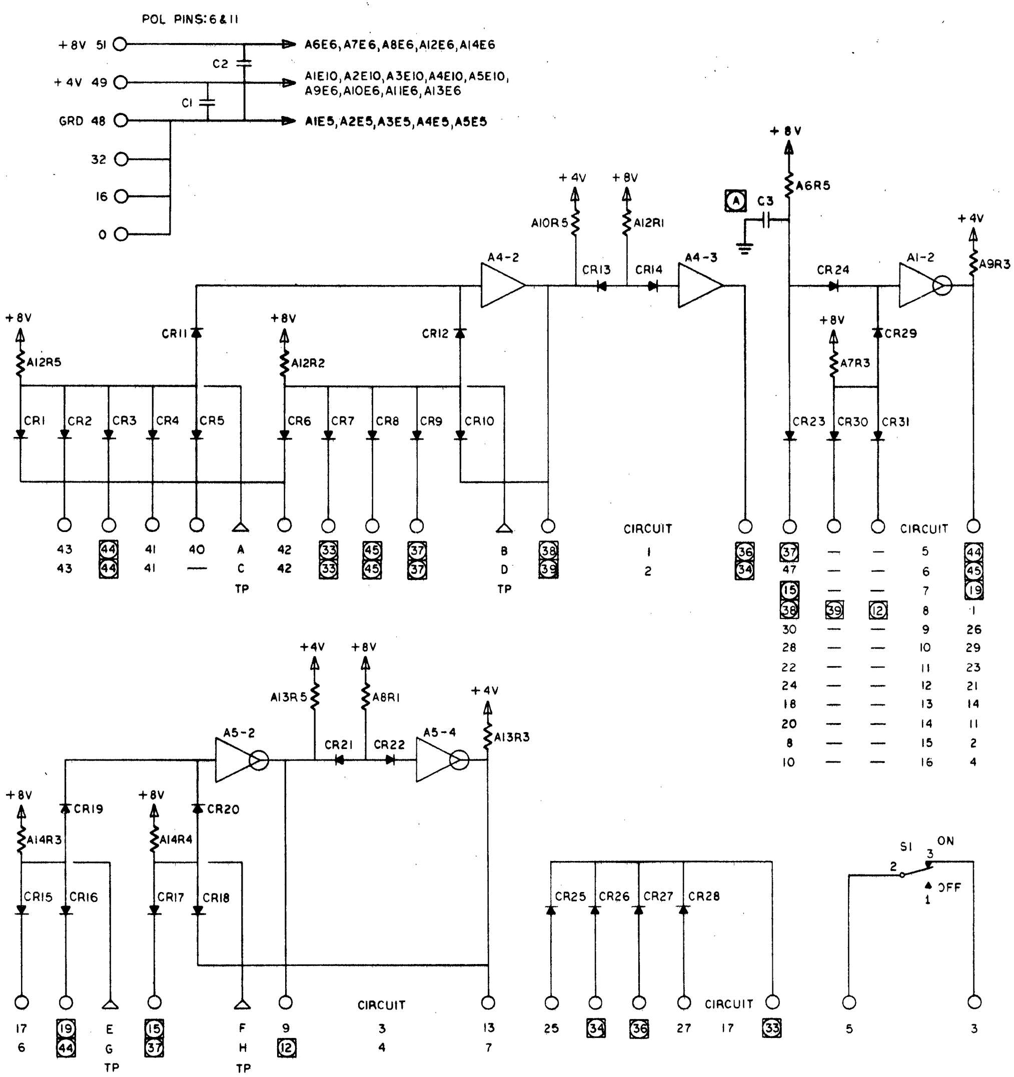


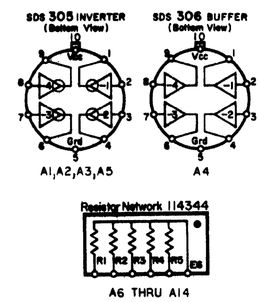
NOTES:

1. Common connections on module are shown with arrows and solid dots.
2. X on output of amplifier indicates that no output (pull-up) resistor is connected at that point.

Publication Number 901250A

MODEL LT25 SCHEMATIC





CIRCUIT							
1	A12R5	A12R2	A10R5	A12R1	A4-2	A4-3	
2	A12R4	A12R3	A9R5	A6R1	A4-1	A4-4	
3	A14R3	A14R4	A13R5	A8R1	A13R3	A5-2	A5-4
4	A14R2	A14R1	A13R1	A14R5	A13R4	A5-3	A5-1
5	A6R5	A9R3	A1-2				
6	A6R4	A9R4	A1-1				
7	A6R2	A9R2	A1-3				
8	A6R3	A9R1	A1-4				
9	A7R5	A10R3	A2-2				
10	A7R4	A10R4	A2-1				
11	A7R1	A10R2	A2-3				
12	A7R2	A10R1	A2-4				
13	A8R5	A11R4	A3-2				
14	A8R4	A11R5	A3-1				
15	A8R2	A11R2	A3-3				
16	A8R3	A11R3	A3-4				

NOTES:

1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.
2. A C3 APPEARS ON CIRCUITS 5 & 7 ONLY.
3. SYMBOL 12 INDICATES COMMON TO PIN 12, SYMBOL 15 INDICATES COMMON TO PIN 15, ETC.
4. FOR REPLACEMENT PARTS LIST, SEE SHEET 2.

MODEL LT25 PARTS LIST

Item	Description		Designators	Qty.
1	Integrated Circuit, Inverter	SDS 305	A1, A2, A3, A5	4
2	Integrated Circuit, Buffer	SDS 306	A4	1
3	Diode, Switching	1N4154	CR1 thru CR31	74
4	Capacitor, Mylar	.01 MFD ±10%, 80vdc	C1, C2	2
5	Capacitor, Polystyrene	22PFD ±1PF, 125vdc	C3	2
6	5-Resistor, Network	2.2K ±5%, 1/4 W	A6, A7, A8, A12, A14	5
7	5-Resistor, Network	560 ohms ±5%, 1/4W	A9, A10, A11, A13	4
8	Switch, Toggle, Printed Circuit, SPDT	Arrow-Hart Model TS-3PC	S1	1

SWITCH COMPARATORS | LT26

SSY NO. 126982

The LT26 module contains eight switch comparator gates, NORed together in two sets of four. A switch comparator compares the logical state of a signal with the state of a manual toggle switch, as illustrated in Figure 2.

This type of circuit is often used as an address comparator, to detect when the address set into the switches is present. For instance in the example of Figure 3, when the incoming binary pattern equals the pattern stored in the switches the output of the NOR gate goes True. With the two NOR outputs tied together, an eight bit number can be detected. Another use is limit detection. Upper and lower limits of four bits each can be detected and the signals used to activate correction devices.

Note that a 220 ohm terminating resistor must be connected to NOR gate output (see Fig. 3) since no 560 ohm pull-up is present. Usually both NOR outputs can be connected to the same 220 ohm resistor. Additional terminators are available on the module for conveniently terminating logic lines in accordance with the T Series backpanel wiring rules.

Note also that the eight inverters on the card can be used independently, as shown in Figure 4.

Maximum Operating Frequency	10 Mc
Circuit Delay	60 nsec worst case (2 amplifiers in series)
Input Logic Levels	Logic 1: +4v Logic 0: 0v
Output Logic Levels	Logic 1: +4v Logic 0: 0v
Fan-out (each output)	16 Unit Loads without terminator. One 220 ohm terminator requires 5 Unit Loads.
Load imposed by each input term	1 Unit Load
+8 Volt Supply	82 ma
+4 Volt Supply	273 ma
Module Dissipation	1.75 watts max.

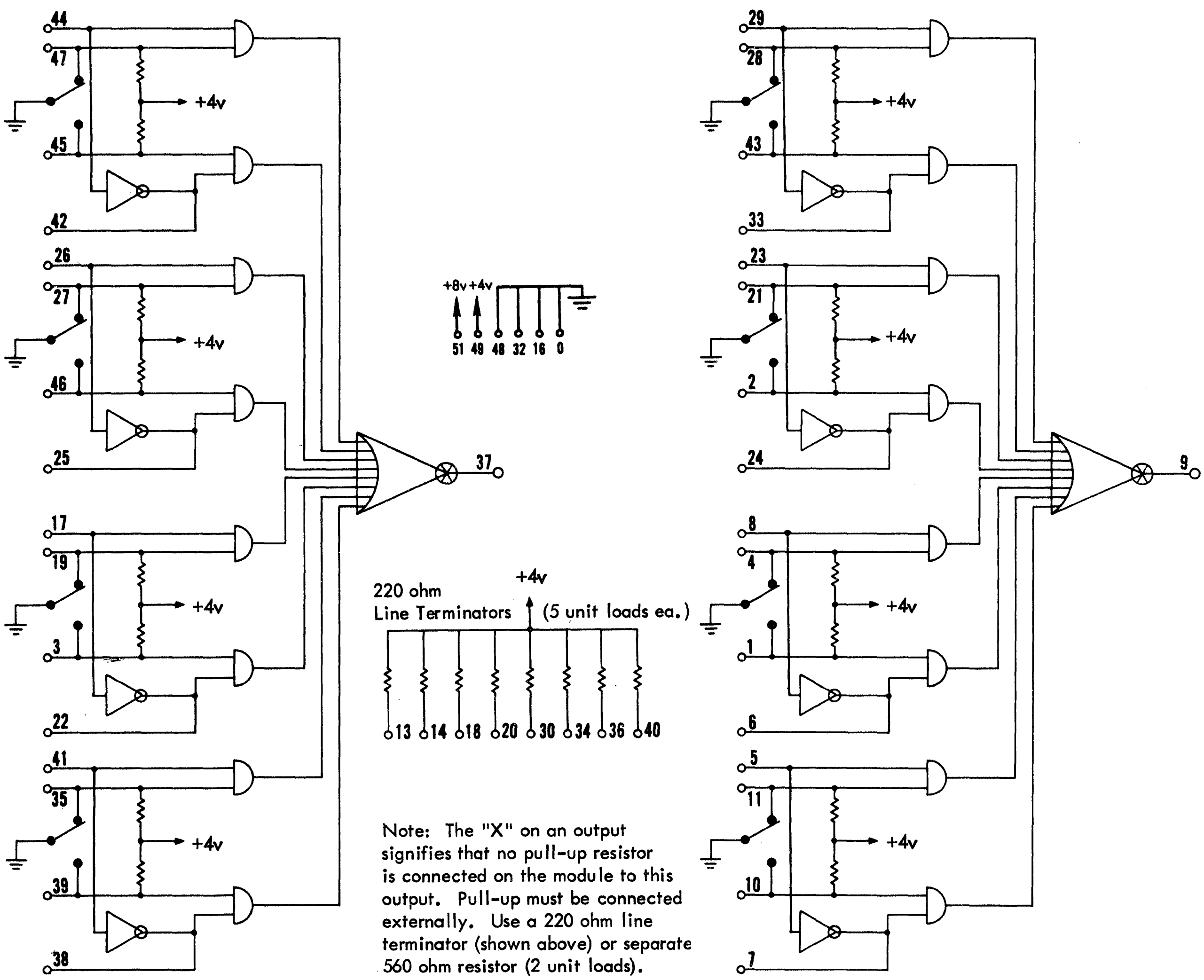


Figure 1. LOGIC DIAGRAM, LT26

Publication No. 901246

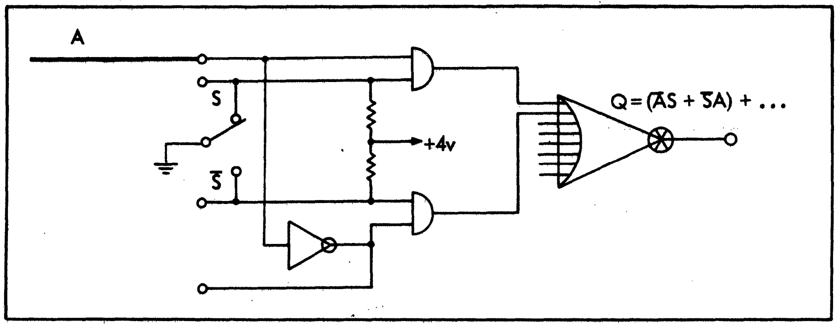


Figure 2. Single Switch Comparator, Typical Input Connection

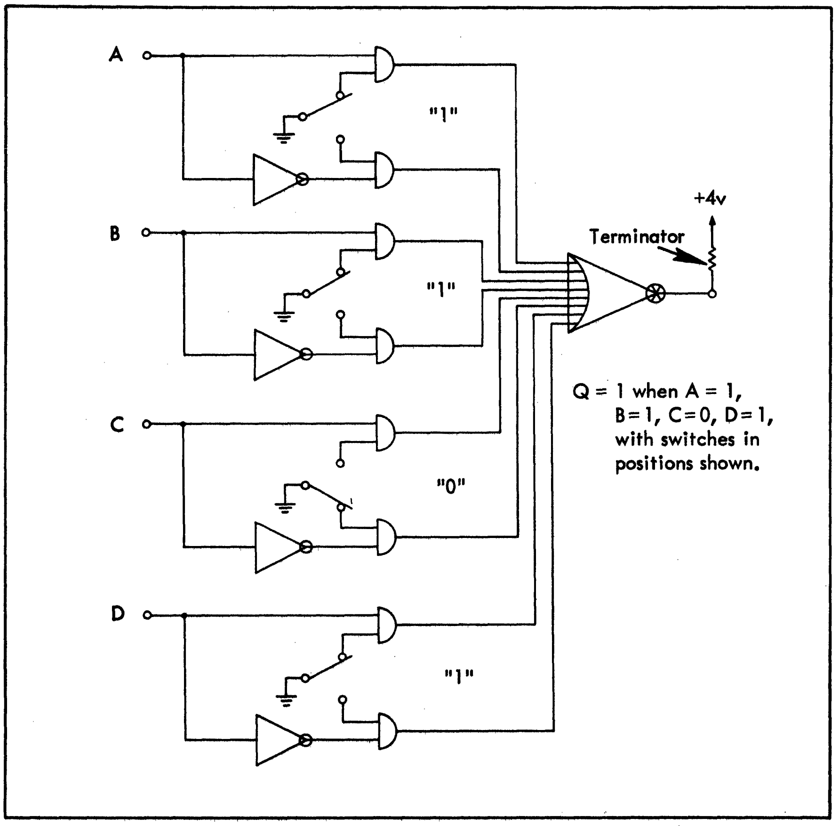


Figure 3. Detecting Equivalence Between Switches And
4-bit input (simplified circuit diagram).

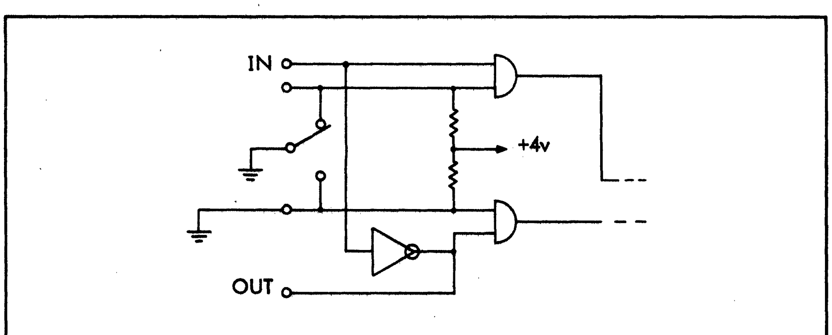
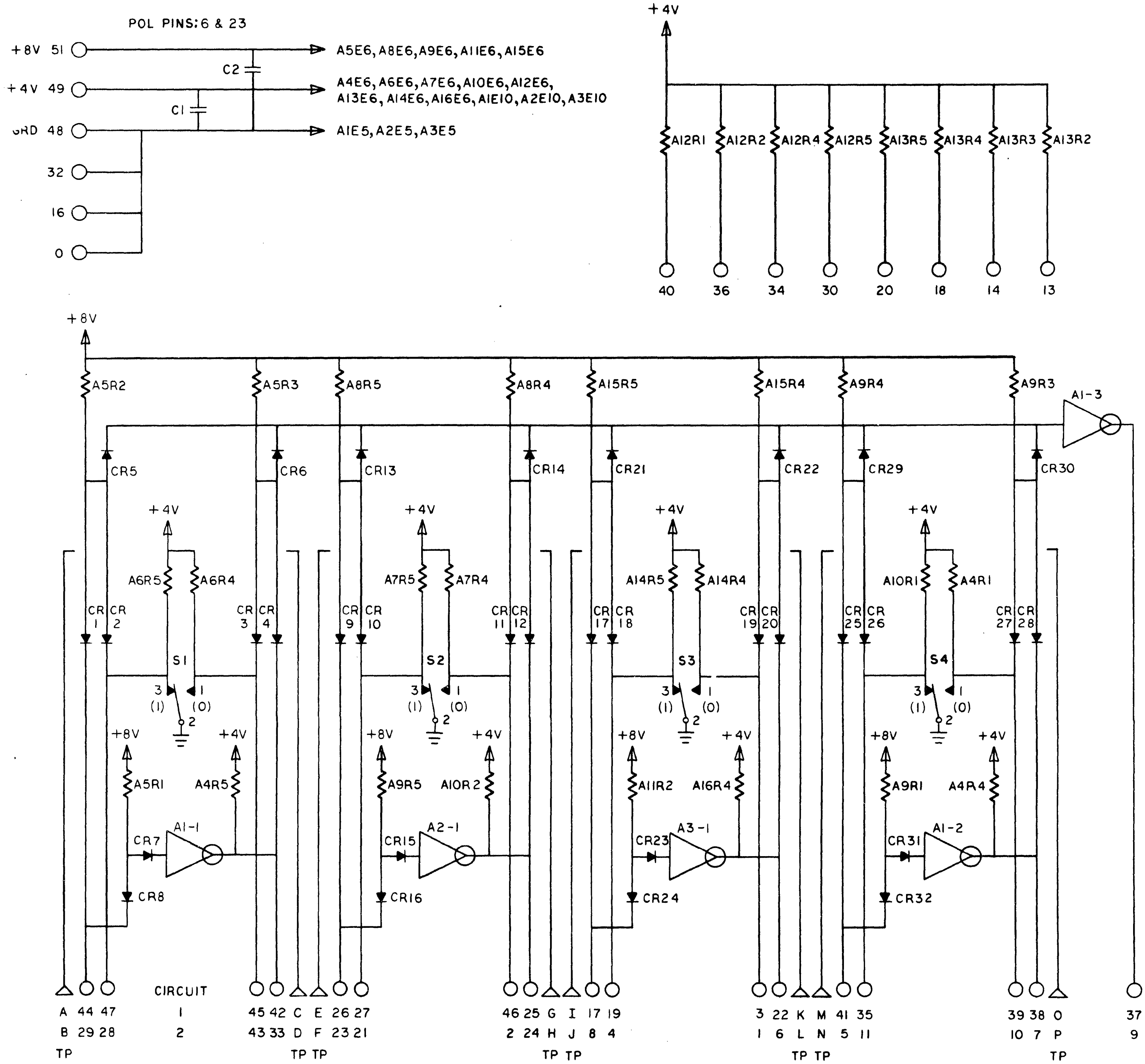


Figure 4. Independent Use Of Inverter

Model LT26 Schematic

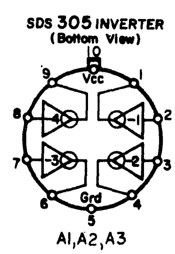


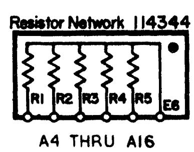
CIRCUIT																		
1	A5R2	A5R3	A8R5	A8 R4	A15R5	A15R4	A9R4	A9R3	A6R5	A6R4	A7R5	A7R4	A14R5	A14R4	A10R1	A4R1	A5R1	A4R5
2	A5R5	A5R4	A8R2	A8R3	A15R2	A15R3	A11R4	A11R3	A6R2	A6R3	A7R2	A7R3	A14R1	A14R2	A10R5	A16R5	A9R2	A4R2

1	A9R5	A10R2	A11R2	A16R4	A9R1	A4R4	A1-3	A1-1	A2-1	A3-1	A1-2
2	A11R5	A10R4	A15R1	A16R2	A11R1	A16R1	A3-2	A1-4	A2-4	A3-4	A3-3

NOTES:

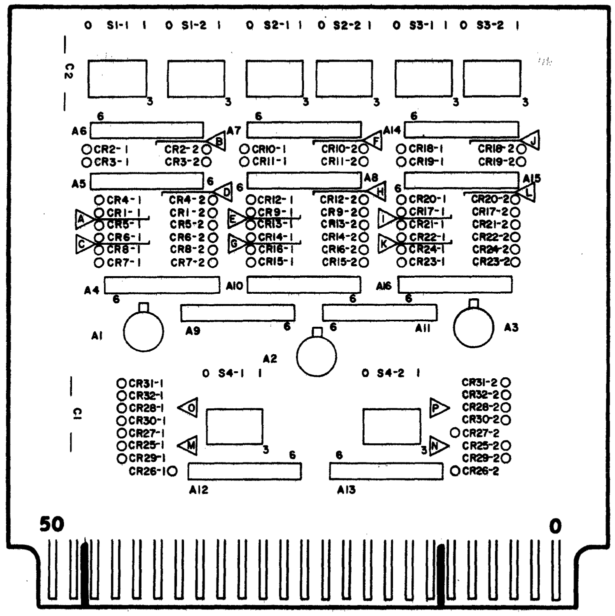
1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.
2. FOR REPLACEMENT PARTS LIST, SEE SHEET 2 ("A" SIZE).





SDS 901246

MODEL LT26 SCREEN



Polarizing Slots 23 6

MODEL LT26 PARTS LIST

Item	Description	Designators	Qty.
1	Integrated Circuit Inverter SDS 305	A1, A2, A3	3
2	Diode, 1N4154	CR1 thru CR32	64
3	Capacitor, Mylar, 0.01µf ±10%, 80v	C1, C2	2
4	5-Resistor Network, 2.2K ohms ±5%, 1/4 W	A5, A8, A9, A11, A15	5
5	5-Resistor Network, 560 ohms ±5%, 1/4 W	A4, A6, A7, A10, A14, A16	6
6	5-Resistor Network, 220 ohms ±5%, 1/4 W	A12, A13	2
7	Switch, Toggle, Printed Circuit, SPDT, Arrow-Hart TS-3PC	S1 thru S4	8

SDS XDS Xerox Data Systems Formerly Scientific Data Systems

MODULE DATA SHEET

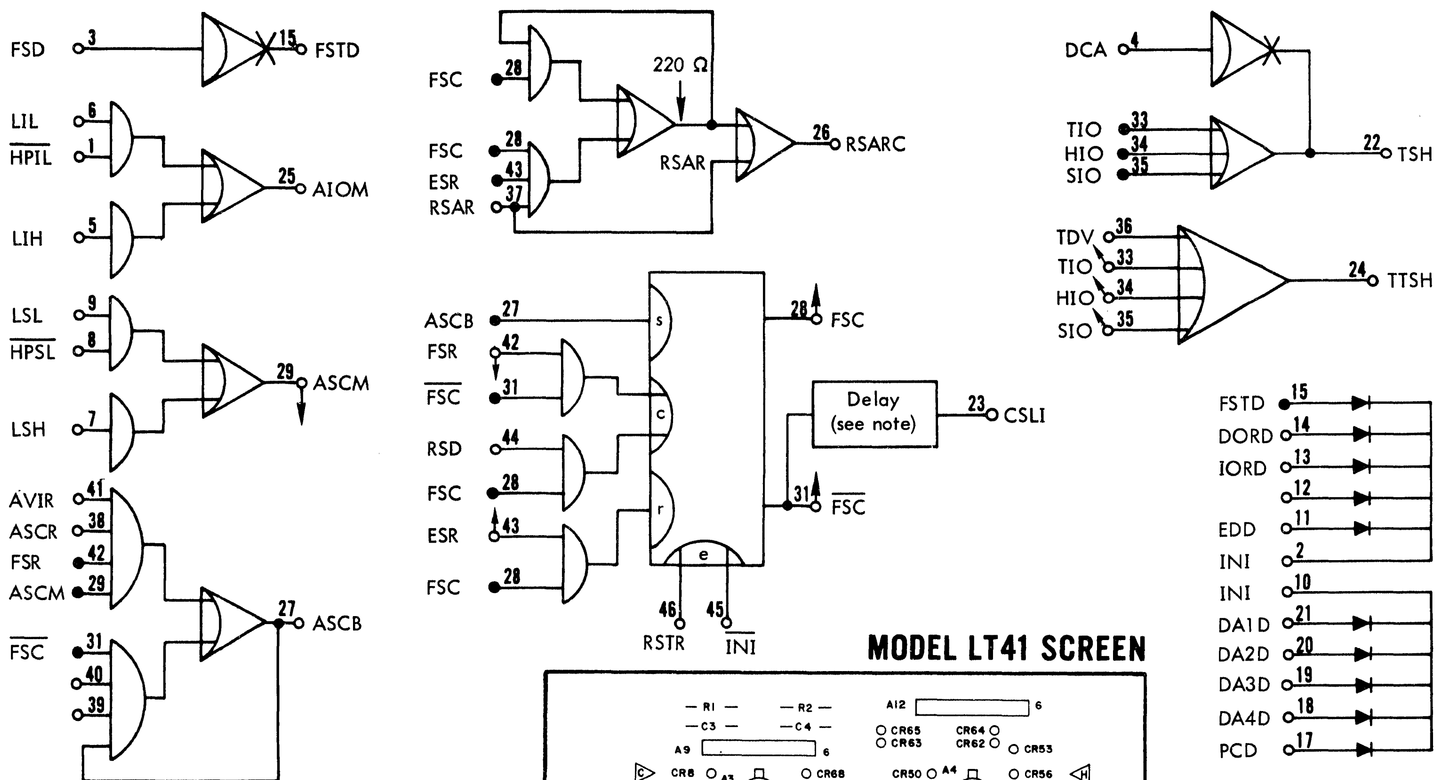
SPECIAL PURPOSE LOGIC MODULE FOR SDS MODEL 7900 DEVICE SUBCONTROLLER

LT41

The LT41 is a special purpose module designed to function as part of the SDS Model 7900 Device Subcontroller. It contains three buffered AND/OR circuits, two buffered latched AND/OR circuits, two buffers, one clocked flip-flop with gated inputs and a delay circuit on one output, ten clamp diodes, and two OR circuits. The circuits are extensively interconnected on the module as shown in the logic diagram.

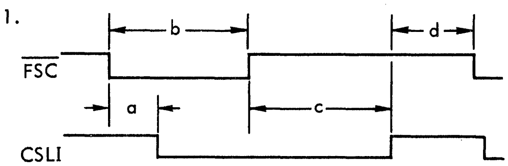
Detailed principles of operation and definitions of logic terms are given in Section 3 of the SDS Sigma Interface Design Manual, SDS Publication No. 900973.

Maximum Operating Frequency	10 Mc
Input Logic Levels	Logic 1: +4v Logic 0: 0v
Output Logic Levels	Logic 1: +4v Logic 0: 0v
Fan-out	Pin 29: 13 unit loads Pin 31: 12 unit loads Pin 28: 10 unit loads pin 15: (when connected to INI, pin 7 of AT17 module) 13 unit loads All others: 14 unit loads
Load imposed by inputs	Pins 33, 34, 35, 42, 43: 2 unit loads each. All others: 1 unit load
Circuit Delay (each amplifier, except for the delay circuit on the flip-flop, which is as specified)	18 nsec typical 30 nsec worst case
Circuit Delay (flip-flop)	40 nsec typical 60 nsec worst case
+8 Volt Supply	74 ma
+4 Volt Supply	192 ma
Module Dissipation	1.86 watts



Notes:

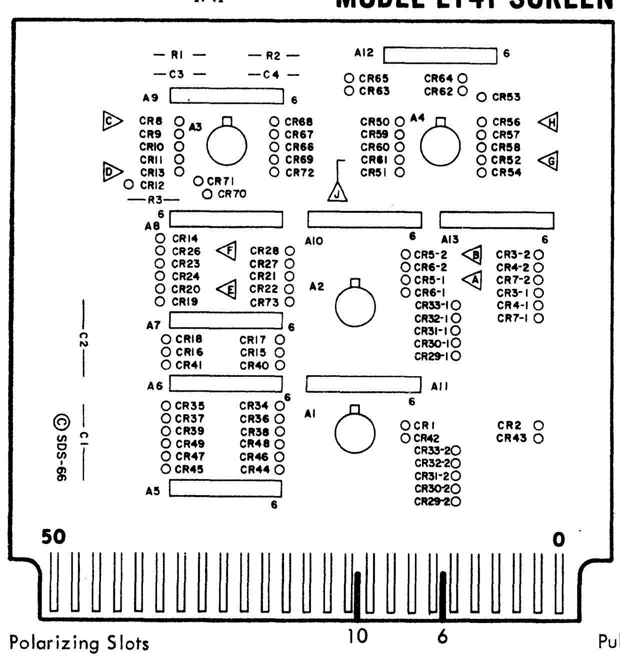
1.



a = 50 nsec max.
b = 100 nsec min
c = 100 nsec min, 350 nsec max.
d = 100nsec min

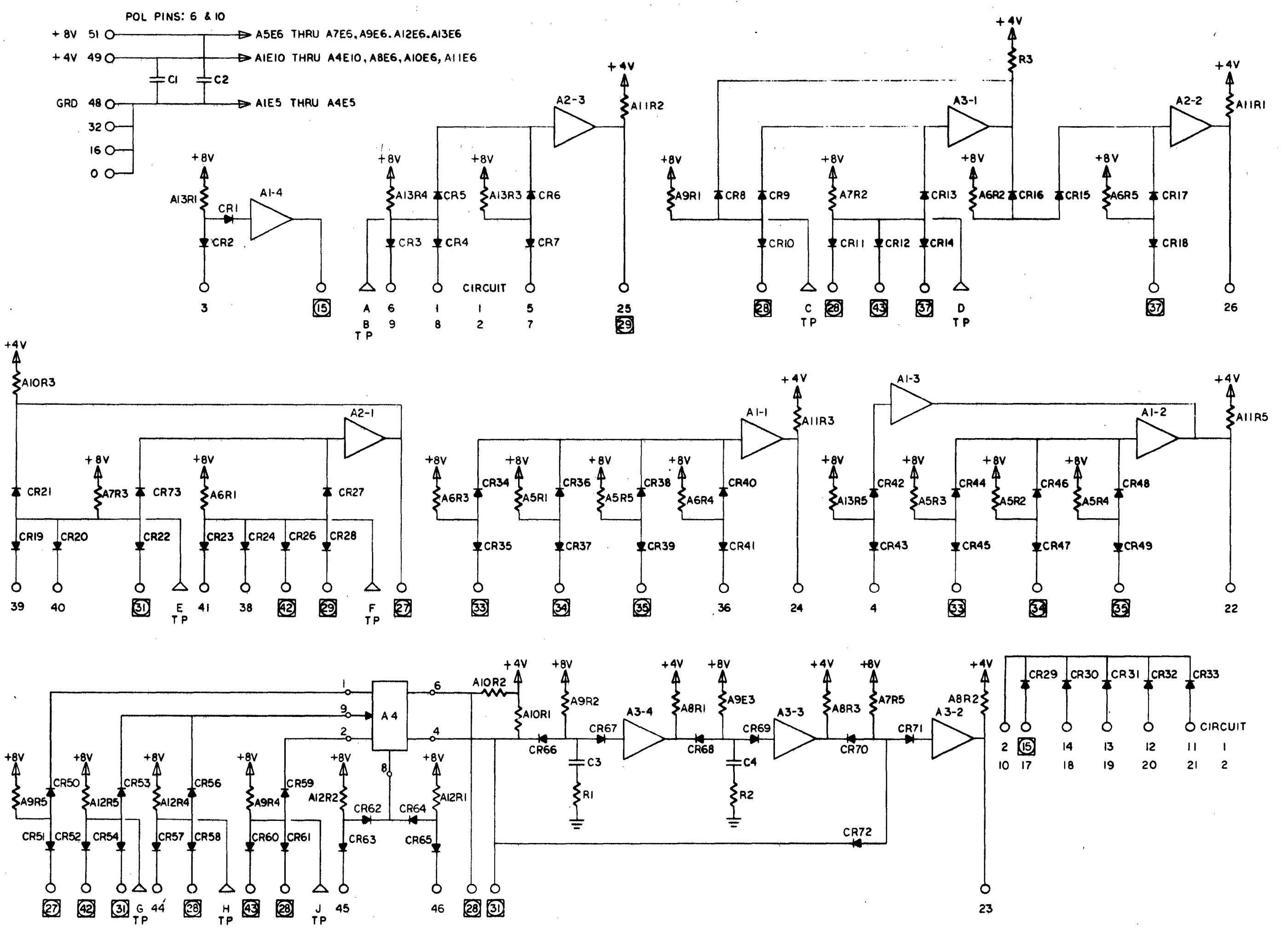
2. Common connections on module are shown with arrows and solid dots.
3. X on output of amplifier indicates that no output (pull-up) resistor is is connected at that point

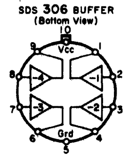
MODEL LT41 SCREEN



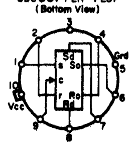
Polarizing Slots

Publication Number 901251A

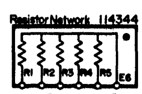



SDS 306 BUFFER (Bottom View)

A1, A2, A3


SDS 307 FLIP-FLOP (Bottom View)

A4



A5 THRU A13

NOTES:

1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.
2. FOR REPLACEMENT PARTS LIST SEE SHEET 2, ("A" SIZE).
3. 15 COMMON TO PIN 15, 43 COMMON TO PIN 43, ETC.

CIRCUIT				
1	A13R4	A13R3	A11R2	A2-3
2	A13R2	A12R3	A10R4	A2-4

MODEL LT41 PARTS LIST

Item	Description		Designators	Qty.
1	Integrated Circuit, Buffer	SDS 306	A1, A2, A3	3
2	Integrated Circuit, Flip-Flop	SDS 307	A4	1
3	5-Resistor Network	2.2K ohms, ±5%, 1/4W	A5, A6, A7, A9, A12, A13	6
4	5-Resistor Network	560 ohms, ±5%, 1/4W	A8, A10, A11	3
5	Capacitor, Mylar	.01MFD, ±10%, 80V	C1, C2	2
6	Capacitor, Polystyrene	100 PFD, ±2.5%, 125V	C4, C3	2
7	Diode, Silicon Switching	1N4154	CR1 thru CR24, CR26 thru CR54 CR56 thru CR73	81
8	Resistor, Film	33 ohms, ±5%, 1/4W	R1, R2	2
10	Resistor, Film	220 ohms, ±5%, 1/4W	R3	1

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MODULE DATA SHEET

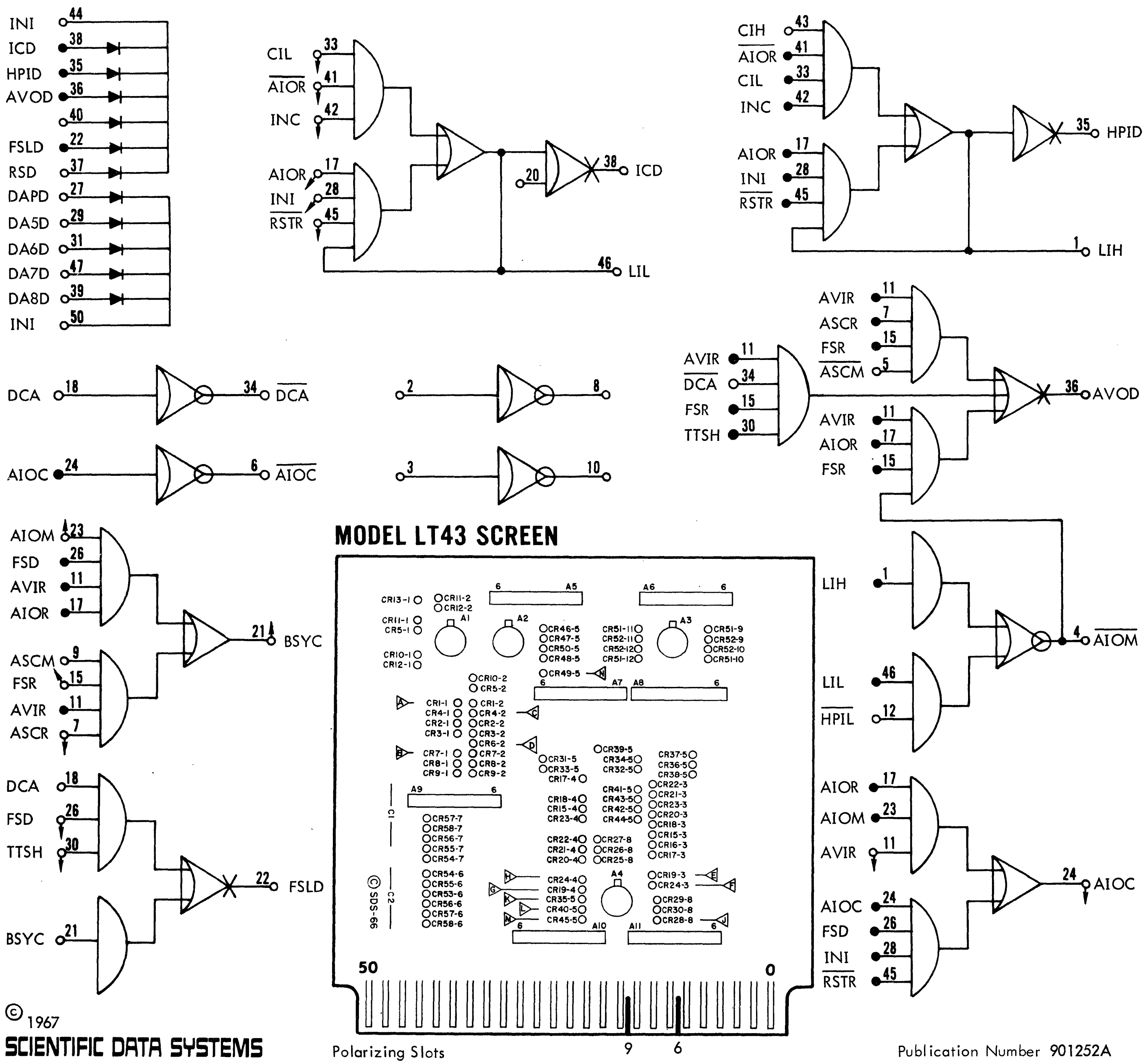
SPECIAL PURPOSE LOGIC MODULE FOR SDS MODEL 7900 DEVICE SUBCONTROLLER

LT43

The LT43 is a special purpose module designed to function as part of the SDS Model 7900 Device Subcontroller. It contains four buffered AND/OR gates, one inverted-output AND/OR gate, two buffered latched AND/OR circuits, four inverters, and eleven clamp diodes. The circuits are extensively interconnected on the module as shown in the logic diagram.

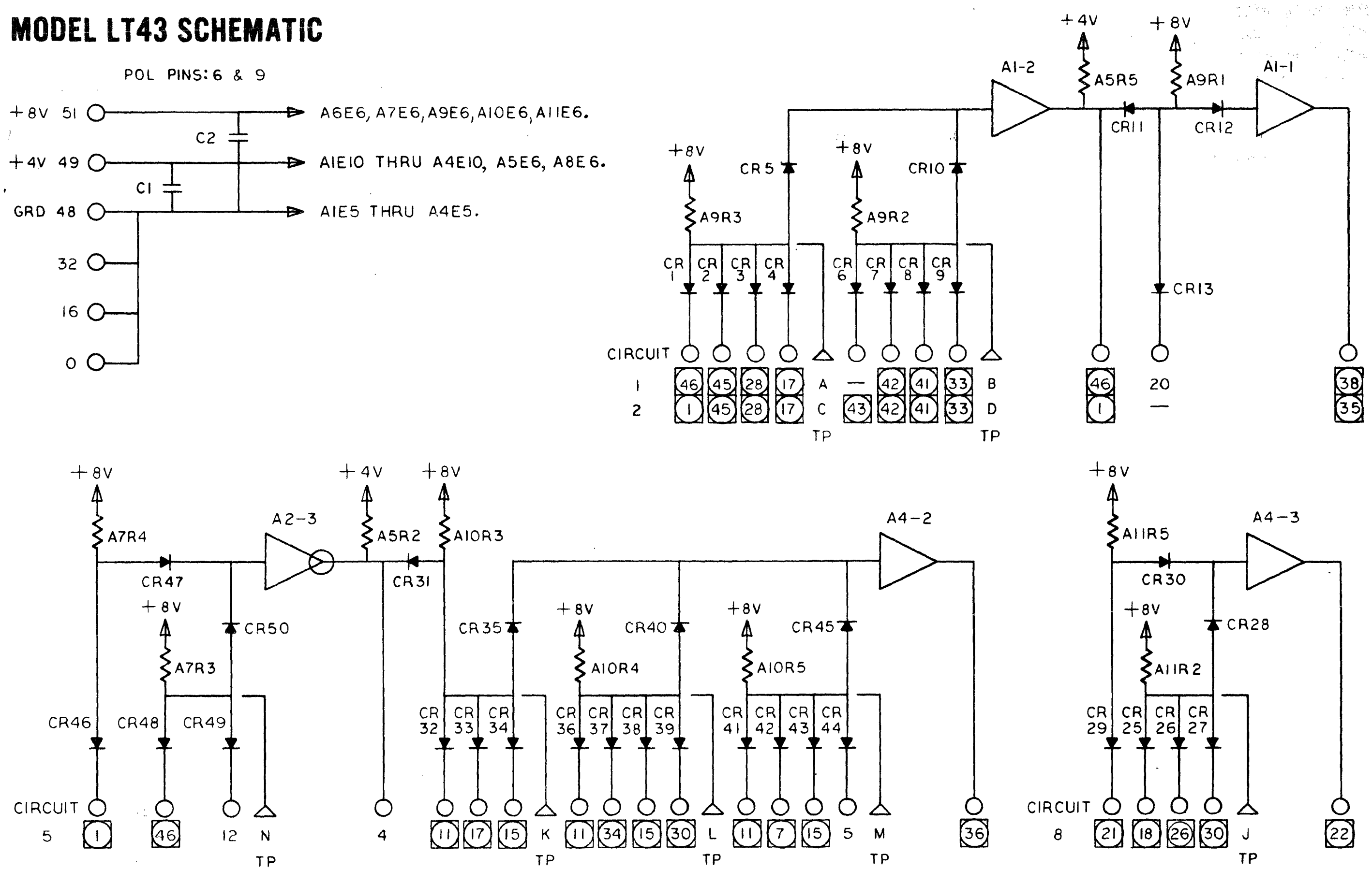
Detailed principles of operation and definitions of logic terms are given in Section 3 of the SDS Sigma Interface Design Manual, SDS Publication No. 900973.

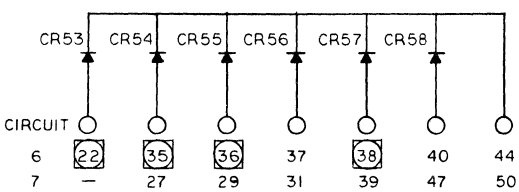
Maximum Operating Frequency	10 Mc
Input Logic Levels	Logic 1: +4v Logic 0: 0v
Output Logic Levels	Logic 1: +4v Logic 0: 0v
Fan-out	Pins 1, 4, 21, 22, 35, 36, 38, 46: 13 unit loads Pin 24: 12 unit loads All others: 14 unit loads
Load imposed by inputs	Pin 11: 6 unit loads Pin 17: 5 unit loads Pin 15: 4 unit loads Pins 26, 28, 45: 3 unit loads Pins 7, 23, 30, 33, 41, 42: 2 unit loads All others: 1 unit load
Circuit Delay (each amplifier)	18 nsec typical 30 nsec worst case
+8 Volt Supply	65 ma
+4 Volt Supply	205 ma max.
Module Dissipation	1.33 watts max.



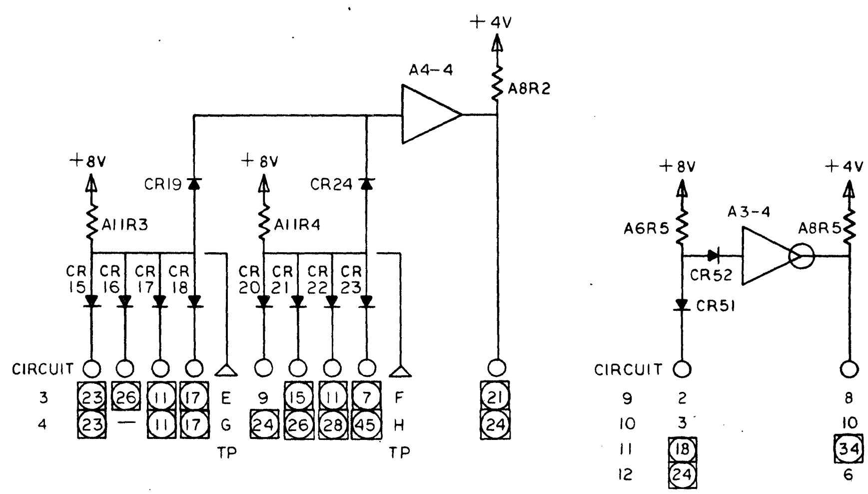
Publication Number 901252A

MODEL LT43 SCHEMATIC



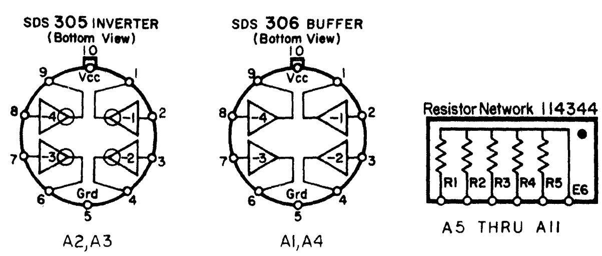


CIRCUIT						
1	A9R3	A9R2	A5R5	A9R1	A1-2	A1-1
2	A7R5	A9R5	A5R4	A6R1	A1-3	A1-4
3	A11R3	A11R4	A8R2	A4-4		
4	A10R2	A10R1	A8R1	A4-1		
9	A6R5	A8R5	A3-4			
10	A6R4	A8R4	A3-3			
11	A7R1	A5R1	A3-1			
12	A7R2	A8R3	A3-2			



NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE CHART FOR DESIGNATORS OF MICROCIRCUIT COMPONENTS NOT FOUND ON SCHEMATIC DRAWING.
2. 1 COMMON TO PIN 1, 46 COMMON TO PIN 46, ETC.



MODEL LT43 PARTS LIST

Item	Description		Designators	Qty.
1	Integrated Circuit, Buffer	SDS 306	A1, A4	2
2	Integrated Circuit, Inverter	SDS 305	A2, A3	2
3	5-Resistor, Network	560 ohms, ±5%, 1/4 W	A5, A8	
4	5-Resistor, Network	2.2K ±5%, 1/4 W	A6, A7, A9, A10, A11	5
5	Diode, Silicon Switching	1N4154	CR1 thru CR13 CR15 thru CR58	88
6	Capacitor, Mylar	.01 MFD, ±10%, 80v	C1, C2	2

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