ST4096

OEM MANUAL

Seagate

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INTRODUCTION

The Seagate ST4096 disc drive provides OEMs and system integrators with over 80 megabytes of formatted capacity in a shock-resistant full-height package. The ST4096 is designed for multi-user multi-tasking systems, engineering workstations or local storage in multi-user networks. Systems needing frequent and rapid data access will benefit from the fast access time and high storage capacity per cylinder. The ST4096 is ideal for these applications in either rugged industrial or quiet office environments.

High-reliability is assured through the use of LSI and surface-mount devices. Seagate's head-positioning system uses a dedicated-servo surface and a unique continuous position feedback for unequaled recording performance. The heads are automatically positioned and locked over the dedicated head shipping zone at power-down. Seagate's internally developed and produced voice-coil actuator and carbon-overcoated, sputtered thin-film media provide a cost-effective fast-access storage solution for multi-user systems.

Our manufacturing facilities have been designed and located exclusively for high-volume production and testing of disc drives. Seagate's ongoing commitment to vertical integration assures availability of the latest technology at the same consistent quality and lowest possible cost. Every stage of the production process is tightly controlled by highly refined procedures. Our proprietary final test and burn-in system continuously verifies our goals of volume production with rigorous quality control.

1.0 SPECIFICATION SUMMARY

DRIVE CAPACITY 1.1

UNFORMATTED CAPACITY 1.1.1

Per Drive:	95.99 Megabytes
Per Cylinder:	93,744 Bytes
Per Track:	10,416 Bytes

FORMATTED CAPACITY 1.1.2

Per Drive:	80.22 Megabytes
Per Cylinder:	78,336 Bytes
Per Track:	8,704 Bytes
Per Sector:	512 Bytes
Sectors per Track:	17

PHYSICAL ORGANIZATION 1.1.3

Tracks:	9,216
Cylinders:	1,024
Read/Write Heads:	9
Servo Heads	1
Discs:	5

ACCESS TIME DEFINITION AND TIMING 1.2

Access time is defined as the time from the leading edge of the first Step pulse received to SEEK COMPLETE (including carriage settling). The period between Step pulses must be between 3μsec and 70μsec.

Average access time is measured over a 341-track seek (one-third stroke).[1] The calculation assumes the following:

1. Step pulses are issued at a 13μsec rate*
2. Nominal temperature and power
3. The average is taken from an inward one-third stroke, plus an outward one-third stroke.

*Access time will be degraded at step rates greater than 20μsec.

Track-to-Track:	6.0msec max.
Average:	30.0msec max. [1]
Maximum Seek:	65.0msec max. [1]
Latency:	8.33msec nominal

FUNCTIONAL SPECIFICATIONS 1.3

Rotational Speed:	3,600 RPM ± 0.5%
Recording Density:	9,792 BPI
Flux Density:	9,792 FCI
Track Density:	1,031 TPI
Interface:	ST412
Recording Method:	MFM
Data Transfer Rate:	5.0 Megabits/second

1. Buffered-Seek

1.4 PHYSICAL SPECIFICATIONS

Height:	3.25 ± .01 inches (82.55 ± .25mm)
Width:	5.75 $^{+.00}_{-.02}$ inches (146.05 $^{+.00}_{-.51}$ mm)
Depth:	8.00 inches max. (203.2mm)
Weight:	6.5 lbs (2.95Kg)

1.5 RELIABILITY SPECIFICATIONS

MTBF:	15,000 Power-on Hours [2]
PM:	Not Required
MTTR:	30 Minutes
Service Life:	5 Years

1.5.1 READ ERROR RATES

Recoverable Read Errors:	1 per 10^{10} bits read [3]
Nonrecoverable Read Errors:	1 per 10^{12} bits read [4]
Seek Errors:	1 per 10^{6} seeks

1.5.1.1 BIT JITTER

Bit jitter reduction determines the relationship between the leading edge of READ DATA and the center of the data window.

The specified Read error rates are based on the following bit jitter specification: The data separator must provide at least -40 dB of bit jitter reduction at 2F with an offset error of less than 1.5nsec shift from the center of the data window.

1.5.2 MEDIA DEFECTS

A media defect is a Read error when data, which has been correctly written, cannot be recovered within 16 retries.

A printout will be provided with each drive shipped listing the location of any defect by head, cylinder, sector and byte. It will also specify the number of bytes from the Index pulse. [5]

There will be no more than nine (9) defects per R/W surface and eighty-one (81) total per drive. A single defect may be up to 16 bits long. Cylinder Ø will be free of defects.

1.6 ENVIRONMENTAL SPECIFICATIONS

1.6.1 AMBIENT TEMPERATURE

Operating:	50°F to 113°F (10°C to 45°C)
Nonoperating:	-40°F to 140°F (-40°C to 60°C)

1.6.2 TEMPERATURE GRADIENT

Operating:	18°F/hr (10°C/hr) max.
Nonoperating:	Below condensation

2. Typical usage at 25°C at sea level. Calculated per Mil. Spec. handbook 217.
3. Recoverable within 16 retries
4. Not recoverable within 16 retries
5. Based on a 32-sector 256 byte/sector format

RELATIVE HUMIDITY 1.6.3

Operating:	8 to 80% noncondensing
Maximum Wet Bulb:	78.8°F (26°C) noncondensing
Nonoperating:	5 to 90% noncondensing

ALTITUDE LIMITS 1.6.4

Operating:	-1,000 ft to 10,000 ft
Nonoperating:	-1,000 ft to 30,000 ft

OPERATING SHOCK 1.6.5

Maximum shock without incurring nonrecoverable errors: 10 G's [6,7]

OPERATING VIBRATION 1.6.6

Maximum vibration, at the following frequencies, without incurring nonrecoverable errors:[7]

FREQUENCY	VIBRATION
5 — 17Hz Displacement (double amplitude)	0.036″
17 — 150Hz Acceleration (peak-to-peak)	0.55 G
200 — 500Hz Acceleration (peak to peak)	0.25 G
500 — 200Hz Acceleration (peak-to-peak)	0.25 G
150 — 17Hz Acceleration (peak-to-peak)	0.55 G
17 — 5Hz Displacement (double amplitude)	0.036″

NONOPERATING SHOCK 1.6.7

Maximum shock without incurring physical damage or degradation in performance: 35G's [7,8,9]

NONOPERATING VIBRATION 1.6.8

Maximum permitted vibration, at the following frequencies, without incurring physical damage or degradation in performance:[7,8]

FREQUENCY	VIBRATION
2—200 Hz	1.0 G (peak to peak)
200—2 Hz	1.0 G (peak to peak)

6. 11msec half-sine wave shock pulse.
7. Input levels at the drive mounting screws. Drive mounted in an approved orientation.
8. Heads positioned in the shipping zone
9. 12.3msec square-wave shock pulse (ΔV=166.6 inch/sec)

1.7 DC POWER REQUIREMENTS

Power may be applied or removed in any sequence without loss of data or damage to the drive.

+12VDC:	
Voltage Tolerance (inc. ripple):	± 5% Seeking ± 10% Nonseek
Maximum Current at Power-on/Seeking:	4.0 Amp
Seeking:	2.5 Amps typ. [10]
Nonseeking:	1.5 Amps typ. [11]
+5VDC:	
Voltage Tolerance (inc. ripple):	± 5% Both seek and nonseek conditions
Maximum Current at Power-on:	1.5 Amps [10]
Seeking:	1.5 Amps typ. [10]
Nonseeking:	1.5 Amps typ. [11]
Power:	
Maximum:	37.5 Watts typical[10]
Nonseeking:	25.5 Watts typical[11]

1.7.1 INPUT NOISE RIPPLE

The maximum permitted ripple is 100mV (peak-to-peak) on either +12VDC or +5VDC measured on the host system power supply across the following equivalent resistive loads:

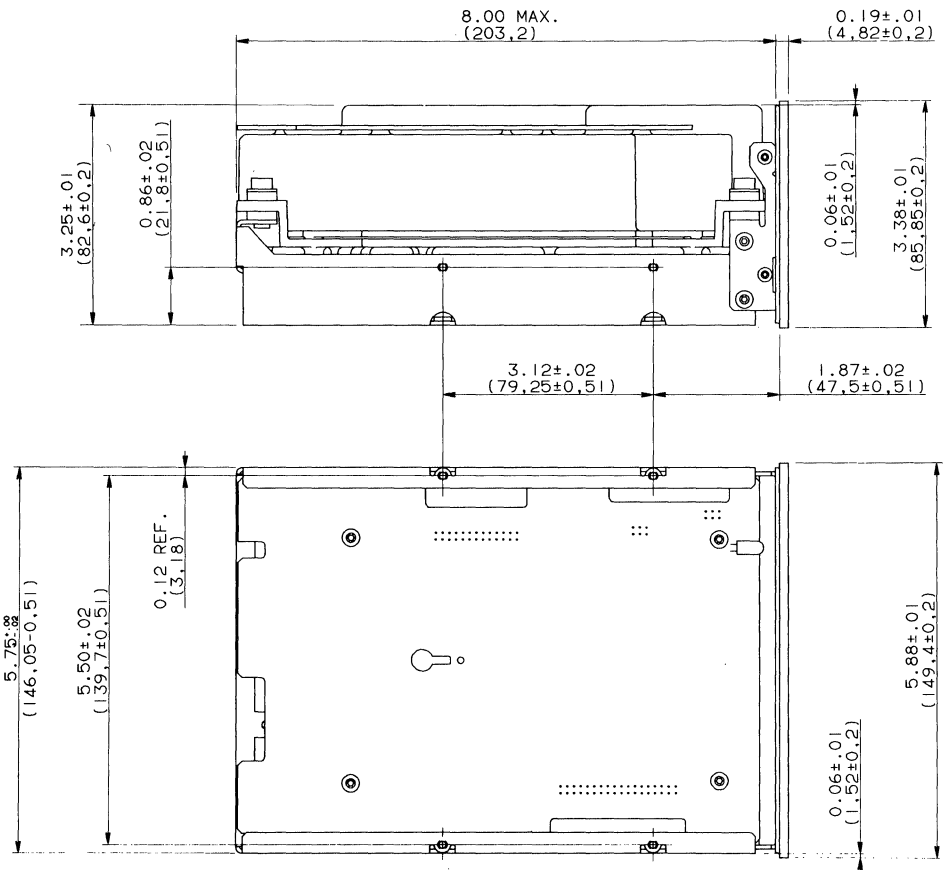
+ 12 Volts: 8Ω
+ 5 Volts: 3Ω

1.7.2 INPUT NOISE FREQUENCY

20MHz max. on both the +12 and +5 Volt lines

10. Measured under the following standard operating conditions:
    1. 25°C ambient temperature
    2. Sea level
    3. Nominal voltages applied
    4. Spindle rotating, drive seeking with buffered one-third stroke followed by two revolutions of non-seek time.
11. Measured under the following standard operating conditions:
    1. 25°C ambient temperature
    2. Sea level
    3. Nominal voltages applied
    4. Spindle rotating and drive not seeking

FIGURE 1: ST4096 Mounting Dimensions



Dimensions are in inches (mm).

MOUNTING REQUIREMENTS 1.8

The ST4096 may be mounted in the following orientations:

Horizontal:	Spindle motor down
Sides:	Left or right

Refer above to *Figure 1* for mounting dimensions.

The drive should not be tilted front to back, in any position, by more than ±5°. For optimum performance the drive should be formatted in the same orientation as it will be mounted in the host system.

SHOCK MOUNTING RECOMMENDATION 1.8.1

It is recommended that any external shock mounts between the drive and the host frame be designed so that the composite system has a vertical resonant frequency of 25Hz or lower. A minimum clearance of 0.050 inch should be allowed around the entire perimeter of the drive to allow for cooling airflow and motion during mechanical shock or vibration.

1.8.2 HANDLING AND STATIC-DISCHARGE PRECAUTIONS

After unpacking, and prior to system integration, the drive is exposed to potential handling and ESD hazard.

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

It is strongly recommended that the drive always rest on a padded surface until the drive is mounted in the host system.

1.8.3 SHIPPING ZONE

Upon power-down, the carriage will automatically move to the shipping zone and the carriage lock will engage. All portions of the head/slider assembly will park inboard of the maximum data cylinder. When power is applied, the lock will automatically disengage and the heads will recalibrate to Track Ø.

The heads may also be parked by issuing a seek command to cylinder 1,024. If the heads are parked while the power is still applied, and Step pulses are then issued, the lock will disengage and the drive will recalibrate to Track Ø.

2.0 ST4096 HOST/DRIVE INTERFACE

This section details the physical specifications of the host/drive interface connectors. Connector dimensions and pin assignments follow under each section. Refer to *Figure 7* for an overall view of the drive interface connectors.

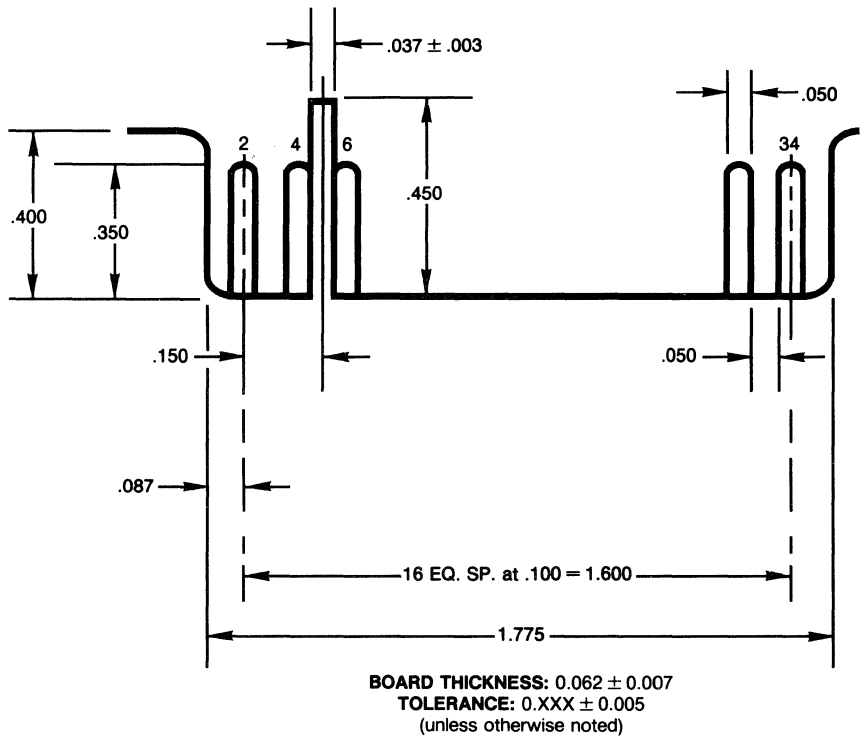
CONTROL / STATUS SIGNALS PCB EDGE-CONNECTOR, J1 2.1

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Control and status signals between the host and the drive are transmitted through a 34-pin PCB edge- connector, J1. *Figure 2* below indicates connector dimensions and *Table 1* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 3*.

J1 pins are numbered 1 through 34 with the even pins located on the component side of the PCB. All odd pins are ground. A key slot is provided between Pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J1 is AMP ribbon connector part number 88373-3.

FIGURE 2: J1 Connector Dimensions



GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	-HEAD SELECT 2^3
3	4	-HEAD SELECT2^2
5	6	-WRITE GATE
7	8†	-SEEK COMPLETE
9	10†	-TRACK Ø
11	12†	-WRITE FAULT
13	14	-HEAD SELECT 2^0
15	16	-RECOVERY MODE
17	18	-HEAD SELECT 2^1
19	20†	-INDEX
21	22†	-READY
23	24	-STEP
25	26	-DRIVE SELECT 1
27	28	-DRIVE SELECT 2
29	30	-DRIVE SELECT 3
31	32	-DRIVE SELECT 4
33	34	-DIRECTION IN
†STATUS ENABLED WITH DRIVE SELECT		

TABLE 1: J1 Host / Drive Pin Assignments

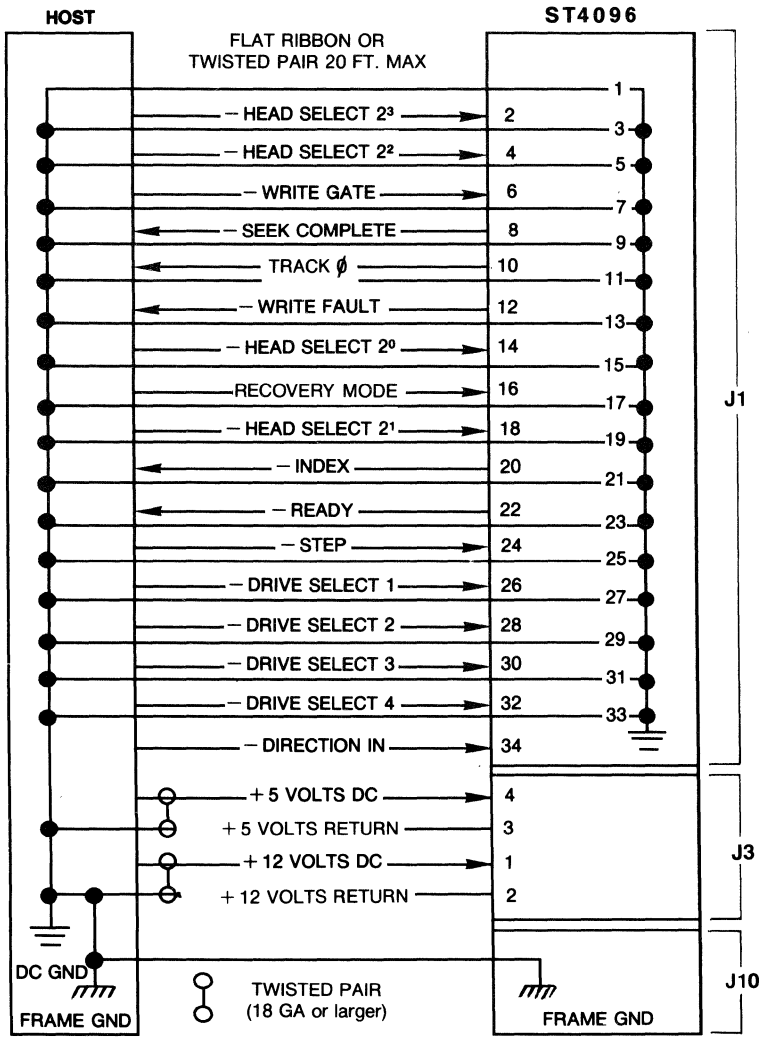


FIGURE 3: Control / Status Signals

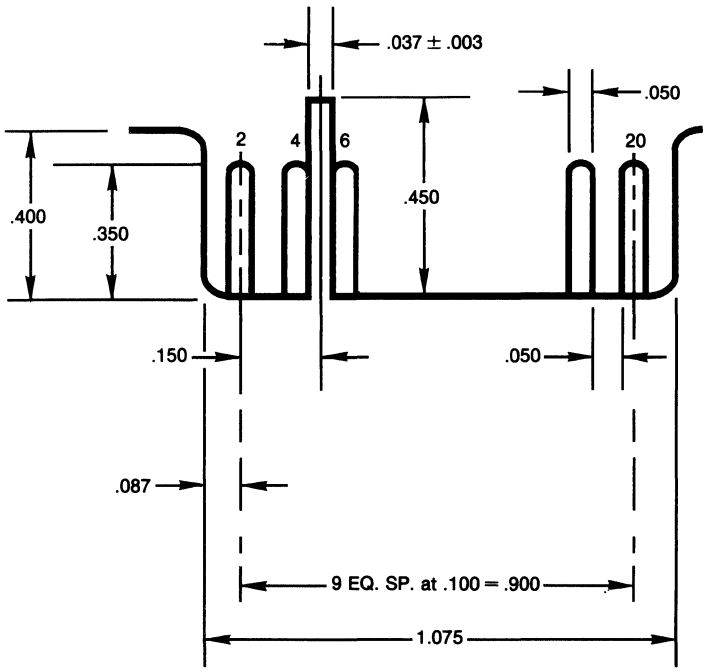
DATA SIGNALS, PCB EDGE-CONNECTOR, J2 2.2

Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

Read/Write data signals are received and transmitted over a 20-pin PCB edge-connector, J2. *Figure 4* below indicates connector dimensions and *Table 2* lists the pin assignments. A host/drive interconnection is illustrated in *Figure 5*.

J2 pins are numbered 1 through 20 with the even pins located on the component side of the PCB. A key slot is provided between Pins 4 and 6. Pin 2 is labeled. The recommended mating connector for J2 is AMP ribbon connector, part number 88373-6.

FIGURE 4: J2 Connector Dimensions

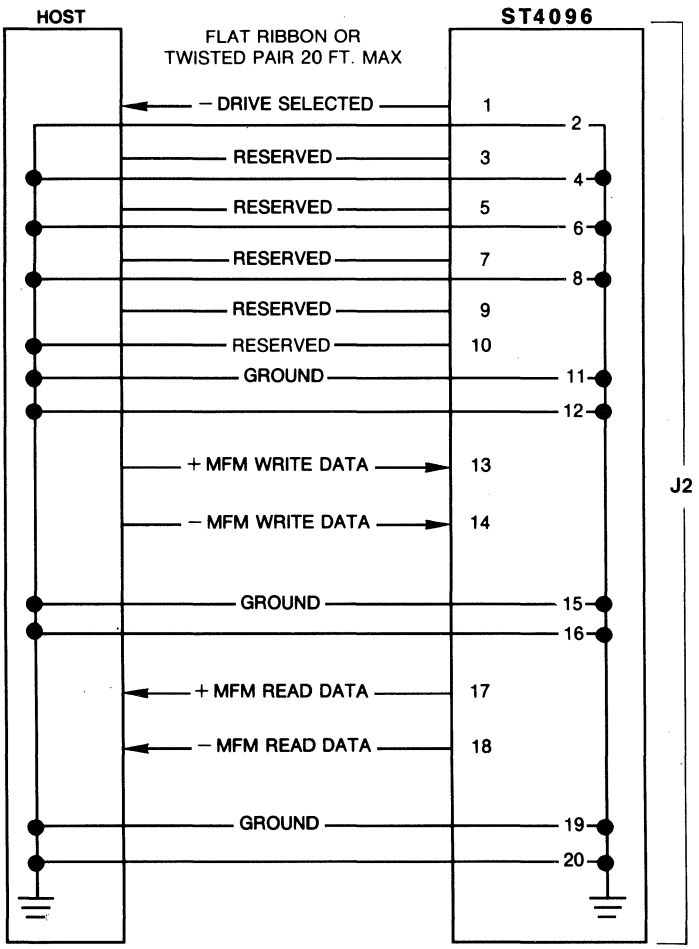


BOARD THICKNESS: 0.062 ± 0.007
TOLERANCE: 0.XXX ± 0.005
(unless otherwise noted)

TABLE 2:
J2 Host / Drive
Pin Assignments

GROUND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	-DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED
10	9	RESERVED
12	11	GROUND
	13	+ MFM WRITE DATA
	14	− MFM WRITE DATA
16	15	GROUND
	17	+ MFM READ DATA
	18	− MFM READ DATA
20	19	GROUND

FIGURE 5:
Status Signals



DC POWER CONNECTOR, J3 2.3

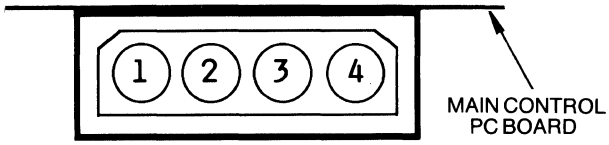
Do not touch the PCB edge-connectors, board components or the printed circuit cable without observing static-discharge precautions. Handle the drive by the frame only.

DC power is transmitted from the host to the drive via the power connector J3. J3 is a 4-pin AMP "Mate-N-Lock" connector, AMP part number 350211-1. The recommended mating connector is AMP part number 1-480424-0.

Applications using cable lengths less than five feet, may use #18AWG wire and AMP 61314-4 strip pins.

For applications requiring cable lengths greater than five feet, #14AWG wire is recommended using AMP 61117-4 strip pins.

FIGURE 6: DC Power Connector and Pin Assignments



PIN	POWER
1	+12 VOLTS
2	+12 VOLTS RETURN
3	+5 VOLTS RETURN
4	+5 VOLTS

FRAME GROUNDING LUG, J10 2.4

J10 is an AMP "Faston," part number 61761-2. It is located on the frame between and below the host/drive interface connectors. The recommended mating connector is AMP part number 62187-2. Refer below to *Figure 7.*

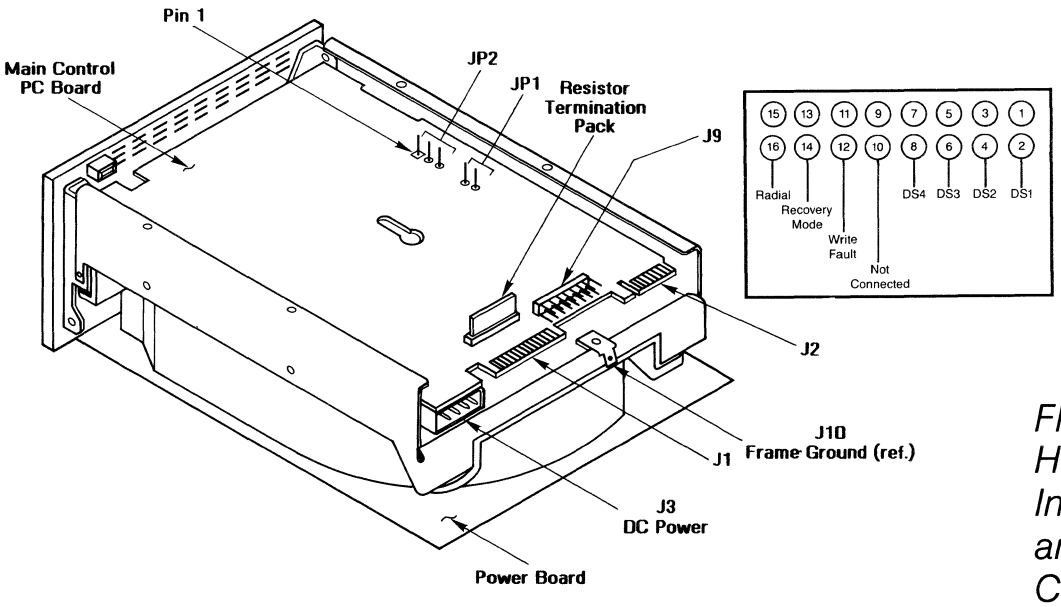


FIGURE 7: Host / Drive Interface and Drive Configuration

3.0 DRIVE CONFIGURATION

The ST4096 may be configured for specific system requirements. These options are detailed in *Sections 3.1* though *3.5*.

DRIVE CONFIGURATION SHUNT, J9 3.1

J9 is a 16-pin right-angle shunt located midway between J1 and J2. Use the provided shorting blocks to enable the DRIVE SELECT lines and any required option. *Figure 7* illustrates J9 and indicates Pin 1.

DRIVE SELECT 3.2

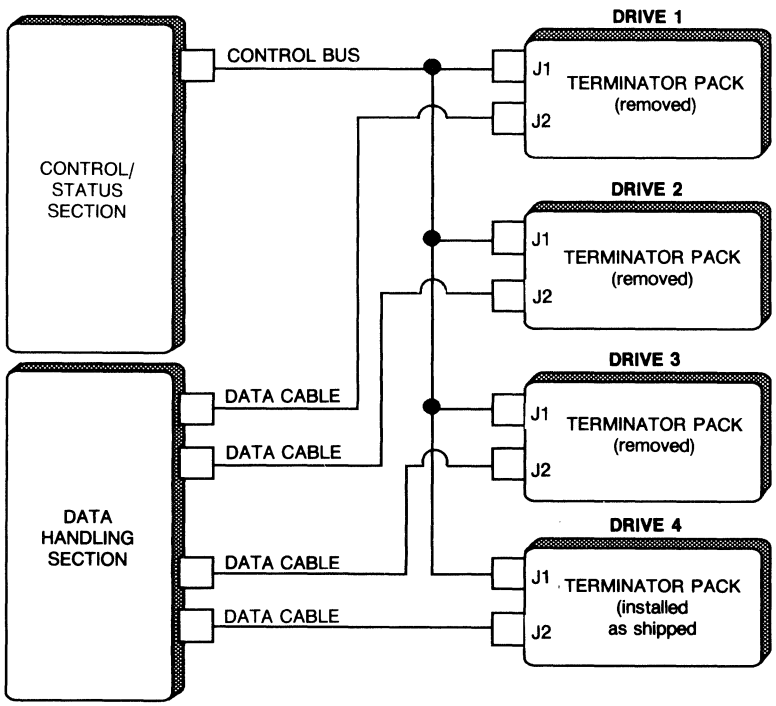
The DRIVE SELECT line enables the controller to select and address the drive. Control cable interface options use either a Daisy-Chain or Radial configuration.

Pins 1-2 shorted enable DRIVE SELECT 1
Pins 3-4 shorted enable DRIVE SELECT 2
Pins 5-6 shorted enable DRIVE SELECT 3
Pins 7-8 shorted enable DRIVE SELECT 4

DAISY-CHAIN 3.2.1

Each drive in the chain must be selected as either Drive Select 1,2,3 or 4, so that only one DRIVE SELECT line activates a device. The last drive in the chain must have a 220/330Ω resistor termination pack installed on the PCB. Refer to *Figure 7* for the termination pack location.

FIGURE 8: Daisy-Chain Configuration



3.2.2 RADIAL

The Radial option is enabled by shorting pins 15 and 16 at J9. Drives configured to this option are always selected and respond to all control signals issued on the attached control cable. The resistor termination pack must remain installed on each radially-connected drive. *Figure 9* illustrates a host/drive Radial configuration.

The LED activity light, if installed, will not light with the Radial option.

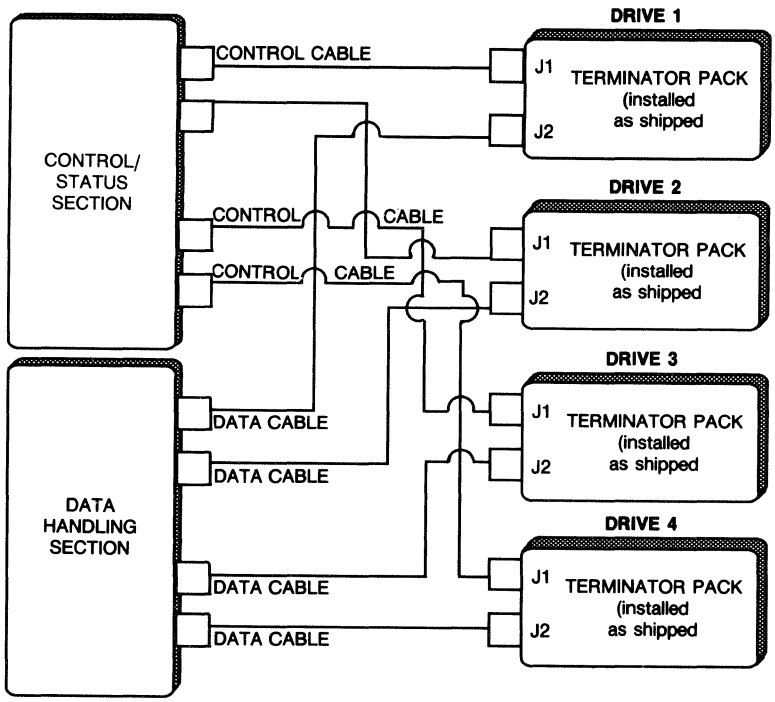


FIGURE 9: Radial Configuration

WRITE FAULT LATCH OPTIONS CONNECTORS, JP2 and J9 3.3

These options allow the user to configure the WRITE FAULT reset to specific system requirements.

JP2 has three jumper pins, and is located on the Main Control PCB. *Figure 7* illustrates JP2 and indicates pin-1. J9 is located midway between the PCB edge-connectors (see *Section 3.1*).

STANDARD: Pins 1 and 2 shorted at JP2
WRITE FAULT will be cleared when Write Gate is false. A WRITE FAULT will only occur when Write Gate is True.

LATCHED: Pins 2 and 3 shorted at JP2
This option will maintain WRITE FAULT True after Write Gate goes False and is recommended for controllers that do not edge-detect WRITE FAULT.

The latched operation has two configurations which are provided at the J9 shunt, pins 11 and 12.

1. **No jumper at J9:** The WRITE FAULT signal can only be cleared by a power-off/on cycle. Use of this option in conjunction with the DC-Unsafe option is not recommended.
2. **Pins 11-12 shorted at J9:** The WRITE FAULT signal can be cleared by de-selecting the drive. When the drive is de-selected, and the fault condition is corrected, the WRITE FAULT signal will be false.

DC-UNSAFE OPTION, JP1 3.4

JP1 has two jumpers, and when shorted, a DC-Unsafe condition will cause a WRITE FAULT signal to be sent to the interface. Use *Figure 7* to locate JP1. Refer to *Section 5.6* for a more detailed discussion of WRITE FAULT.

RECOVERY MODE 3.5

The ST4096 may be configured to the Recovery Mode option by shorting pins 13 -14 at J9. This option enables the R/W heads to microstep. This repositioning option may be used after the controller has completed its retry options on a Read error.

4.0 CONTROL INPUT SIGNALS

The control signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing.

The signals to be multiplexed are WRITE GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, HEAD SELECT 2^3, DIRECTION IN, RECOVERY MODE and STEP. These lines are terminated with a removable 220/330Ω resistor pack.

The multiplexing signals are DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, and DRIVE SELECT 4. These lines are terminated in a single fixed 220/330Ω resistor pack.

Control signals are transmitted across the driver/receiver combination illustrated below in *Figure 10.* Control input signals are activated in accordance with the following specifications:

True:	0.0 Volts DC to 0.4 Volts DC at I = -48mA max.
False:	2.5 Volts DC to 5.25 Volts DC at I = +250μA (open collector)
Termination:	220/330Ω resistor pack

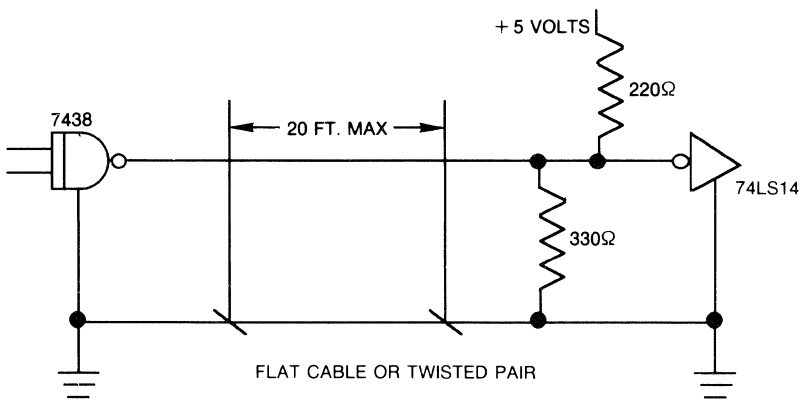


FIGURE 10: Control Signals Driver/Receiver Combination

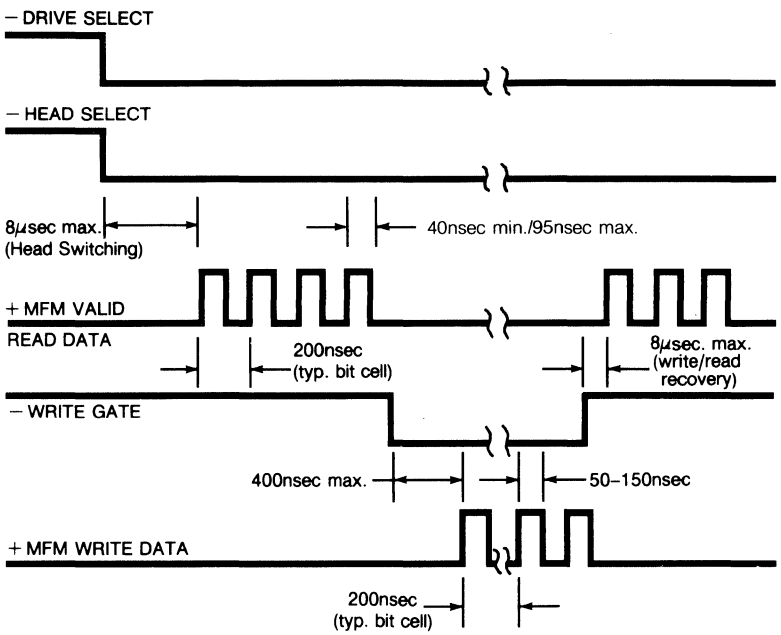
4.1 HEAD SELECT 2^0, 2^1, 2^2, 2^3

These signals allow the selection of each Read/Write head in a binary code sequence. The lines are numbered 0 through 3. HEAD SELECT line 2^0 is the least significant line. When all HEAD SELECT lines are high on the interface, Head 0 is selected. Refer below to *Figure 11* for HEAD SELECT timing.

4.2 WRITE GATE

The active state of this signal, or low level, enables data to be written to the disc. When inactive, or high, this signal enables data to be transferred from the drive and enables Step pulses to move the heads.

FIGURE 11:
Read/Write Timing



NOTE: Heads may not be switched while WRITE GATE is active.

STEP 4.3

The STEP signal is a 2μsec to 10μsec pulse that initiates R/W head motion. The number of pulses issued determines distance traveled. The rate of Step pulses determines the access method.

If the period between pulses is from 3μsec to 70μsec, the access method will be Buffered-Seek. Slow-Step is employed if the period between pulses is greater than or equal to 3msec.

DIRECTION IN must be stable 100nsec before the leading edge of the first step pulse and remain stable for 100nsec after the last pulse in a string of Step pulses. Step pulses issued between 70μsec and 3msec may be lost.

If excessive Step pulses are issued which would cause a seek inward beyond Cylinder 1,023 or outward beyond Cylinder Zero, the drive will enter the Auto-Truncation mode.

BUFFERED SEEK 4.3.1

To minimize access time, pulses may be issued at an accelerated rate and buffered in a counter. Initiation of a seek starts immediately after the first pulse is received. Head motion occurs during pulse accumulation, and the seek is completed following receipt of all pulses.

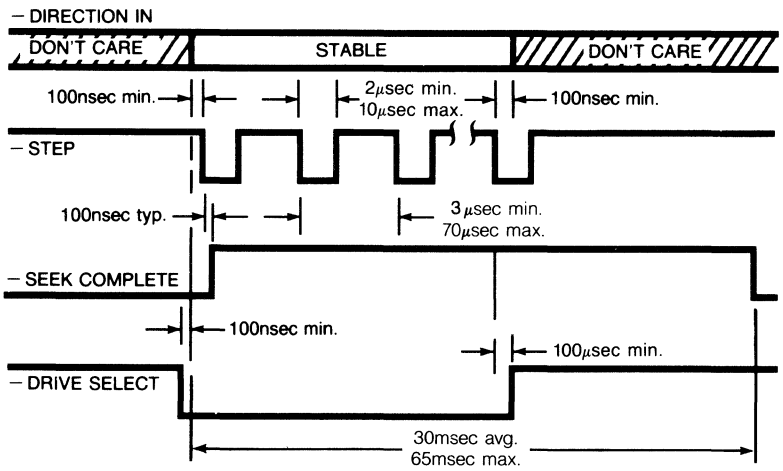
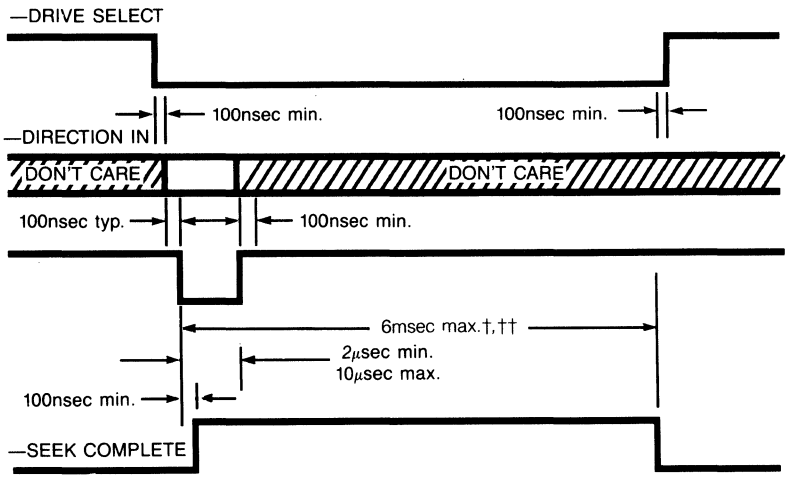


FIGURE 12: Buffered-Seek Timing

4.3.2 SLOW-STEP

In a single-track mode, the servo motor is settled and SEEK COMPLETE is issued 6msec max. after the leading edge of the Step pulse.



† Assumes drive maintains velocity at incoming pulse rate.
†† For multiple-track, time depends on length of seek.

FIGURE 13: Single-Track Seek Timing

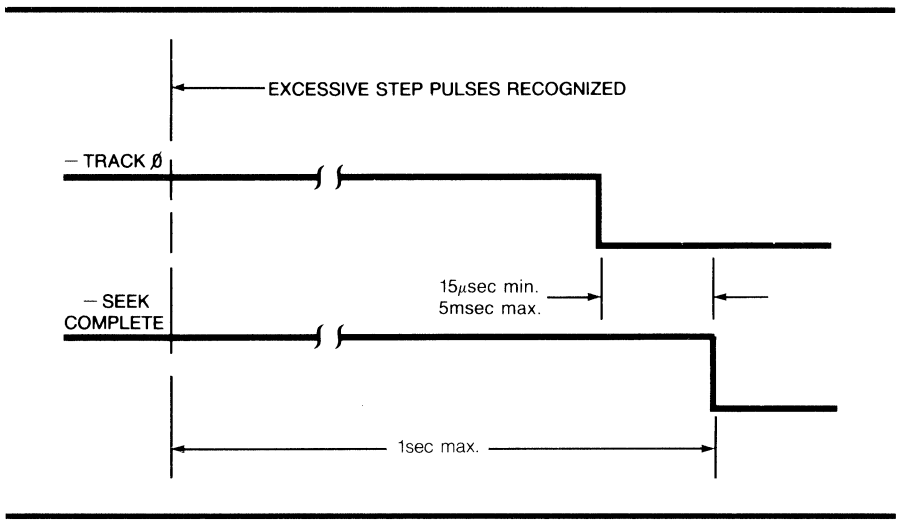
AUTO-TRUNCATION 4.3.3

The drive will enter the Auto-Truncation mode if the controller issues an excessive number of Step pulses, which would place the R/W heads outward beyond Track Ø or inward beyond Cylinder 1,023.

With Auto-Truncation active, the drive disallows additional pulses, takes control of the servo motor and recalibrates the heads to Track Ø.

CAUTION: If the controller is still issuing Slow-Step pulses after the ST4096 issues SEEK COMPLETE from Auto-Truncation mode, the drive will either reenter Auto-Truncation mode with DIRECTION IN false, or step the remaining cylinders with DIRECTION IN true.

FIGURE 14: Auto-Truncation Timing



SEEK RETRY 4.3.4

Seek-Retry is an internally generated seek command and is implemented by the drive to enhance seek performance.

If the drive detects an off-track condition, or the seek cannot be completed, the drive will recalibrate the heads to Track Ø and retry the seek. All writing is inhibited during retry.

If the target track is still not achieved, or the seek was not completed, the drive will set WRITE FAULT true, and READY and SEEK COMPLETE false. WRITE FAULT will remain active until the condition which caused the fault is corrected and the reset is completed.

DIRECTION IN 4.4

DIRECTION IN defines the direction the Read/Write heads will move when the STEP line is pulsed. With DIRECTION IN true, each pulse causes the heads to move one cylinder inward toward the spindle.

When DIRECTION IN is false, each pulse causes the heads to move one cylinder outward toward Track Ø.

DRIVE SELECT 4.5

The DRIVE SELECT line is activated by the controller to select and address the drive.

4.6 RECOVERY MODE

RECOVERY MODE is initiated by the controller asserting the RECOVERY MODE line true at the interface. This changes the STEP line to a microstep function after 100nsec. A Step pulse will now cause SEEK COMPLETE to go false 100nsec after the drive receives the pulse. The drive then microsteps off-track using the optimum algorithm, allowing 8msec for the R/W heads to settle and then takes the SEEK COMPLETE line true.

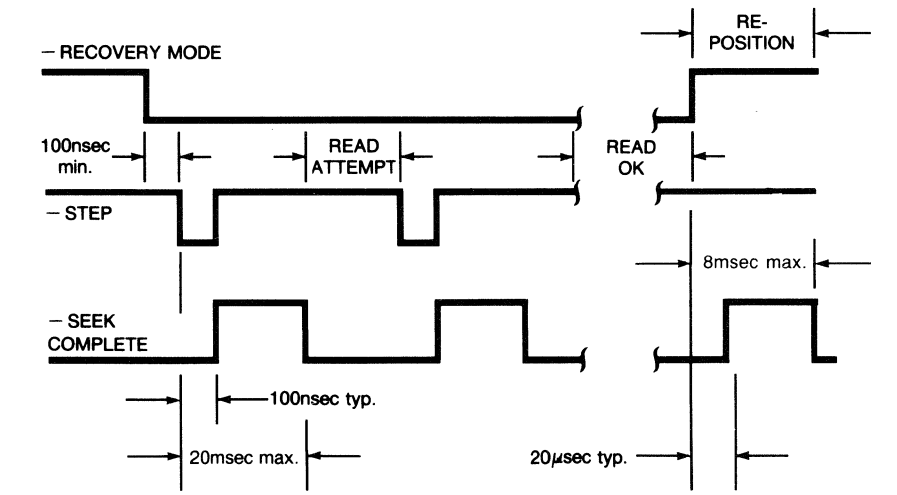


FIGURE 15: Recovery Mode

The controller may then attempt to read data. If data is not read correctly, the controller may issue an additional Step pulse. Up to eight separate microstep algorithms may be accessed before the sequence is repeated.

When data is read correctly, the controller exits RECOVERY MODE by taking the line false at the interface. The drive then returns the heads to the nominal position by asserting SEEKING COMPLETE false, waiting 8msec for head settling and then asserting SEEK COMPLETE true. All writing is inhibited while RECOVERY MODE is true.

5.0 CONTROL OUTPUT SIGNALS

The control output signals are gated to the interface when selected. The control output signals are DRIVE SELECTED, INDEX, TRACK Ø, READY, SEEK COMPLETE and WRITE FAULT.

DRIVE SELECTED 5.1

DRIVE SELECTED is a status signal transmitted over J2, which informs the host system of the selection status of the drive. The signal is driven by a TTL open collector. The signal goes true on the interface only when the device is configured as described in *Sections 3.1-3.2,* and the appropriate DRIVE SELECT line is activated by the host system.

INDEX 5.2

This signal is provided by the drive once each revolution (16.67msec nominal) to indicate the beginning of a track. Normally this signal is at a high level and makes the transition to low to indicate INDEX. Only the transition from high to low, or the leading edge, is valid.

During power-on, INDEX is not available until the heads have moved out of the shipping zone.

TRACK Ø 5.3

This signal indicates a low level (true) only when the Read/Write heads are positioned at Cylinder Zero (the outermost track).

Track Ø is the only cylinder that provides interface recognition. The drive is designed to recalibrate to Track Ø during power-on and Auto-Truncation operations.

Track Ø may also be accessed via conventional Buffered-Seek and Slow-Step modes. After Track Ø is true, no actions may be taken by the controller until SEEK COMPLETE is also true.

READY 5.4

This signal, when true together with SEEK COMPLETE, indicates that the drive is ready to Read, Write or Step and that all control input signals are valid. When this line is high, all reading, writing and stepping are inhibited. The maximum time after power-on for READY to be true is 20 seconds.[12]

During the power-up sequence, READY remains false until:

1. The recalibration to Track Ø is complete
2. Spindle speed is stable within ± 0.5% of nominal
3. Drive initialization routines are complete
4. DC voltages are within tolerance.

12. The specified 20 seconds max. time interval is calculated from the point that the power supply voltages are within the ±5% voltage tolerance.

5.5 SEEK COMPLETE

This signal goes to a low level (true) on the interface when the Read/Write heads have settled on the final track at the end of a seek. Seeking, reading or writing should not be attempted when SEEK COMPLETE is false. SEEK COMPLETE goes false in the following cases:

1. When a recalibration sequence is initiated (by drive logic) at power-on.
2. 100nsec (typical) after the leading edge of a Step pulse.
3. If either +5 or +12 Volts are detected as unsafe.
4. It the drive attempts a Seek-Retry after settling on a track.
5. At the beginning and end of a RECOVERY MODE operation

5.6 WRITE FAULT

This signal notifies the host system that a condition exists at the drive which, if not detected, would cause improper writing on the disc.

With DRIVE SELECT active, and one of the following conditions true, the WRITE FAULT signal will be issued to the interface and Write Current will be inhibited.

1. Write Gate true with no Write Current flowing to the head
2. Write Current to the heads with no Write Gate
3. DC-Unsafe jumper option enabled

Any of the following conditions will cause Write Current to be inhibited when Write Gate is true:

1. Multiple heads selected
2. No head selected
3. SEEK COMPLETE false
4. READY false
5. DC-Unsafe true
6. A Step pulse is received

WRITE FAULT will remain active until the condition which caused the fault is corrected and the reset is completed.

6.0 POWER-ON SEQUENCE

The application of DC power initiates a sequence which starts the spindle motor, regulates its speed, steps the Read/Write heads to Track Ø and issues READY and SEEK COMPLETE sequentially to terminate the sequence.

READY and SEEK COMPLETE are issued to the interface when the drive is available to accept commands. Upon power-up the drive is available to accept commands 20 seconds max. after the power supply voltages maintain the specified tolerances.

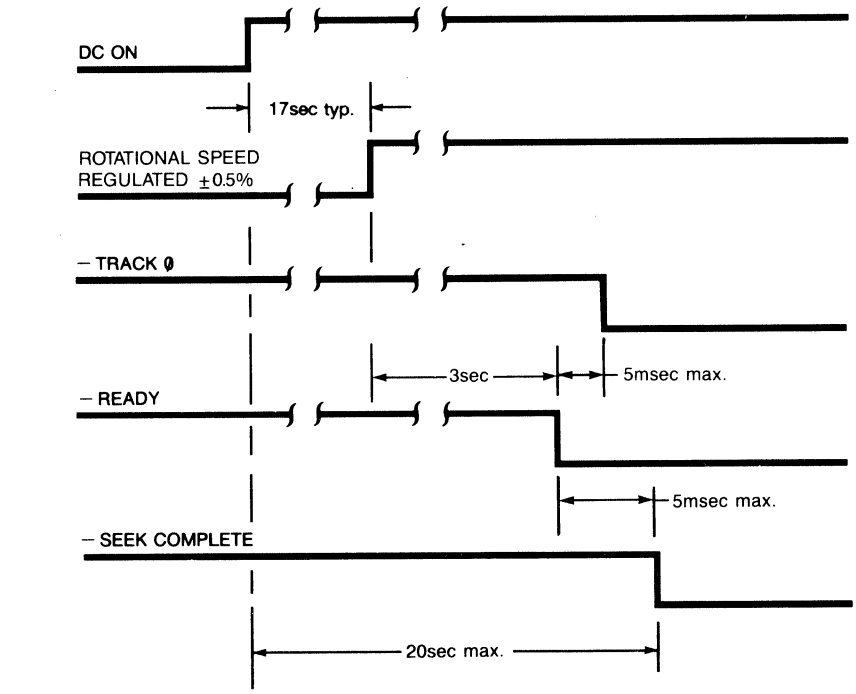


FIGURE 16: Typical Power-On Sequence

7.0 DATA TRANSFER LINES

Two pairs of balanced signals are used for the transfer of data: MFM WRITE DATA and MFM READ DATA. All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed.

These lines are provided at the J2 connector. Refer below to *Figure 17* for the driver/receiver combination used for data transfer signals.

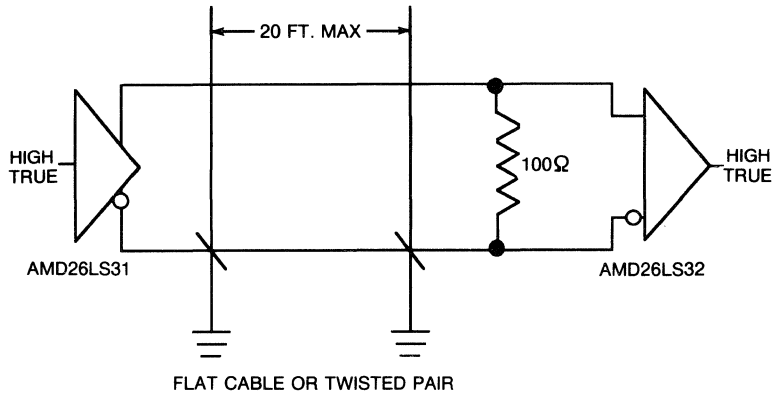


FIGURE 17: Data Signal Driver/Receiver Combination

7.1 MFM WRITE DATA

WRITE DATA is transmitted by a differential pair which defines the transitions to be written on the disc. The +MFM WRITE DATA line going more positive than the -MFM WRITE DATA line is the active transition. This signal must be driven to an inactive state when in READ mode.

7.1.1 PRECOMPENSATION

The ST4096 does not require precompensation.

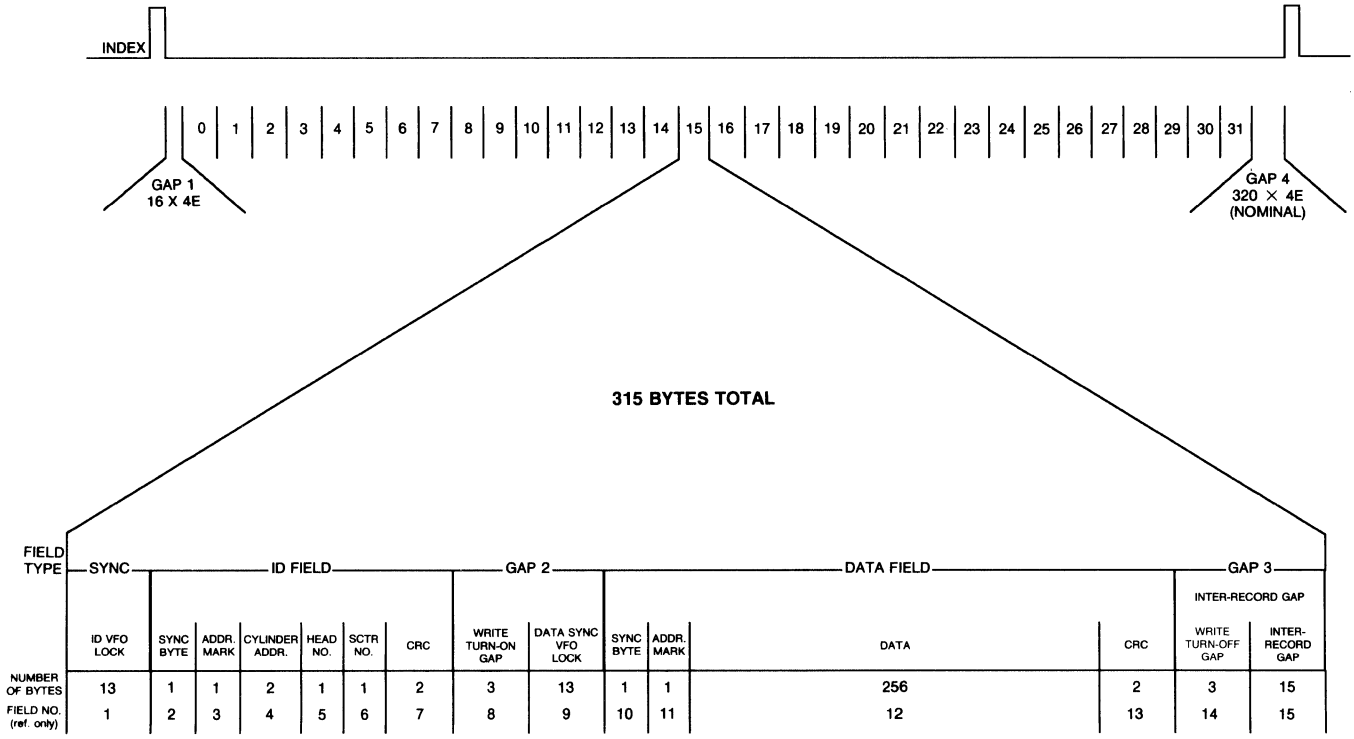
7.1.1.1 REDUCED WRITE CURRENT

The ST4096 does not require the host system to specify a cylinder to begin applying reduced Write Current. This function is managed internally by the MPU.

7.2 MFM READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system by a differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the -MFM READ DATA line represents a flux reversal on the track of the selected head.

Appendix 1:32 Sector, 256 Byte/Sector Format Example



Reference Number	Number of Bytes	Field Name	Field Description
1	13	ID VFO LOCK	A field of all zeros to sync the VFO for the ID
2	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows
3	1	ADDRESS MARK	"FE" Hex defining that ID field data follows
4	2	CYLINDER ADDRESS	A numerical value in Hex defining the detent position of the acuator
5	1	HEAD NUMBER	A numerical value in Hex defining the head selected
6	1	SECTOR NUMBER	A numerical value in Hex defining the sector for this section of the rotation
7	2	CRC	Cyclic Redundancy Check information used to verify the validity of the ID field information just read
8	3	WRITE TURN-ON GAP	Zeros written during format to isolate the write splice created. This field assures valid reading of field number 7 and allows the 13 bytes required for Data VFO lock.
9	13	DATA SYNC VFO LOCK	A field of all zeros to sync the VFO for the data field
10	1	SYNC BYTE	"A1" Hex with a dropped clock to notify the controller that data follows
11	1	ADDRESS MARK	"F8" Hex defining that user data follows
12	256	DATA	This area available for user data
13	2	CRC	Cyclic Redundancy Check information used to verify the validity of the user data field information just read
14	3	WRITE TURN-OFF GAP	Zeros written during update to isolate the write splice created. This field assures valid reading of field number 13 and allows the 13 bytes required for VFO lock for the ID field of the next sector.
15	15	INTER-RECORD GAP	A field of all zeros which acts as a buffer between sectors to allow for speed variation

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