NOTES ON SA-10 INSTALLATION

1. Check carefully that no physical damage has occurred.

2. Check that 11 plugs into the wire-wrap panel are properly seated. Insert the clock crystal plug in 1B33 -- see attached sketch.

3. Check for shorts across outputs of both power supplies: on any DEC connector, pin A2 is +5V, pin B2 is -6.5V, pin C2 is ground. Normally, the +5V will measure about 5 ohms to ground, the -6.5V about 40 ohms.

4. Apply power to unit. If power plug is of the wrong type, power cord coding is: Green, frame ground; White, neutral; Black, hot.

5. Turn on circuit breaker on rear door and check for +5V and -6.5V at DEC rack.

6. Turn off and unplug unit before cabling to CPU. CPU power should also be off.

7. I/O and memory bus connections are as follows:

AB5-6	Mem. Cable 2 (data bits) IN
AB7-8	Mem. Cable 2 OUT
AB13-14	Mem. Cable 1 (address and control) OUT
AB15-16	Mem. Cable 1 IN
AB21-22	I/O Cable 2 (control) IN
AB23-24	I/O Cable 2 OUT
AB29-30	I/O Cable 1 (data bits) OUT
AB31-32	I/O Cable 1 IN

Note that the relative positions of the cables 1 and 2 are opposite to that on most DEC devices. IN and OUT designations are arbitrary and may be swapped if desired for better cable routing. If the SA-10 is at either end of the KI-10 I/O bus, -15 volt power is not available for the terminators in the SA-10 and should be taken from a nearby device. Most configurations will work if the terminator tabs are connected together but not to a power source.

If an MX-10 multiplexor is used on the SA-10 memory port, remove the W990 from A19 and replace with the multiplexor control cable. The W990 is not interchangable with the one in DF-10s. If the SA-10 is not at the end of the multiplexor bus, remove the G703s from slots AB5, AB6, AB15 and AB16 and replace with cables to the next device.

9. The frame of the SA-10 should be grounded in the same manner as any PDP-10 I/O device.

9. The memory port should be set to receive the request on "immediate" if the SA-10 is set up for KA10 bus; otherwise on "fast".

10. Set the base address to the desired value with the DIP switch on the wire-wrap panel. Switches 1 through 7 correspond to bits 25 through 31 respectively. Pressing the top of the switch, labelled "off", corresponds to a 1.

11. Power up the system including the SA-10 and read in the properly configured diagnostic. Start the program at BEG. It should loop until manual stopped. If it stops at ERROR 3, the SA-10 is probably inaccessible. Check I/O cabling and power. CONI 2T4 should give a one in bit 17 if the unit is properly connected. An ERROR 8 stop probably indicates inaccessibility to memory. An ERROR 10 stop is probably a memory cable or port problem. Other errors are likely to be SA-10 faults.

12. If less than 256K of memory is available, open location ADRHI with DDT and type in the highest available address. Start the program at CMT. This should also loop until manually stopped, counting through all available memory addresses. If it returns to DDT or prints an error message, check memory cabling and port.

13. Connect the controllers to the SA-10. Each BUS or TAG cable has a black end and a gray (or brown) end. The black end plugs into the SA-10 and the gray end into the "IN" connector. The terminators supplied with the SA-10 plug into the "OUT" connectors. Note that a black connector always mates with a gray connector.

14. The SA-10 does not support the EPO cable, so a jumper must be installed at the controller to permit it to power up. A ground connection to the controller frame should also be made.

15. The controller address should be set to the desired value, which must agree with the assignment in the diagnostic.

16. If a tape controller is to be tested, skip to step 20.

17. Mount formatted scratch packs on drives to be tested, leaving others stopped. If no formatted packs are available, use virgin packs and proceed with step 18 until a "No Record Found" error is obtained, then format the packs (step 19) and return to step 18.

18. Start the program at DSKT. It will print the size of memory, list the drives off-line, and then start read/write testing. If all drives are listed as off-line, note whether there is a noticeable delay before the off-line message prints out. If so, the selection path is not continuous. Perhaps the BUS and TAG cables are swapped or the wrong channel is being used. If the off-line message comes quickly, there is a select error; check the controller address and make sure that it is enabled to the proper channel. If one or more drives are found online, they will be run and errors printed as encountered. Summaries are printed every 15 minutes. If no errors other than correctable data check are found for one hour, the subsystem should be usable on-line.

19. To format a pack, set the desired drive to unit 0. With DDT,

set location FMTM as desired: 0= write data records only, 1 = write record zero and data records, -1 = write home address, record zero and data records. Start the program at FMT. Either "Formatter Done" or "Error" will be printed. On error the sense bytes should give a clue to the trouble. The progress can be monitored by setting the address switches to 5 and turning on exec paging, which will set the current CCHH in the memory indicators.

20. Make sure the tape control is set for 24 sense bytes.

21. Ready a scratch tape (ring in) on the drive to be tested. If not drive 0, open location TDEV with DDT and type in the controller and drive address.

22. Start the program at QTT. If all is well the program will write, backspace and read all the way down the tape, printing a summary at the end. Any errors found will also be printed. Five passes with nothing but a few errors should indicate readiness for on-line operation. If the program hangs in a loop, check that the proper subchannel is being used and that the bus and tag cables are not interchanged. If a "Select Error" occurs, check that the proper channel is enabled and that the contents of TDEV agree with the controller address. If "Intervention Required" occurs, check that the drive address is correct, and that the drive is on-line and ready. On other errors, the sense bytes should provide a clue.

SAIO Notes

People to contact
Systems Concepts - Stuart Nelson
Fred Wright
ADP - Tom Kurkowski

16 x 512 microcode

Need to know device code & base address

+5v for logic
-6.5v for level inverters

Bus in
Bus out } 8 bits + P

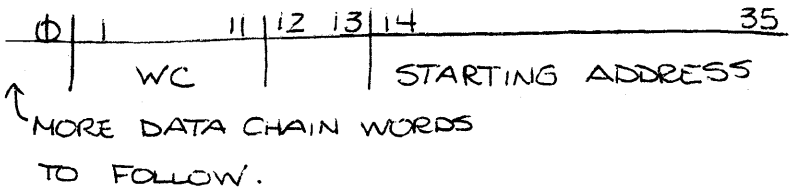
High rate feature uses data in / data out } instead of { service in / service out

Base address is where a channel goes in physical memory to fetch the initial command

SAIO is started by setting "GO" bit for a channel with a CONO.

When finished processing a command list the SAIO will store status & will set a flag (1 per channel)

DATA CHAIN POINTS TO AN ARGUMENT

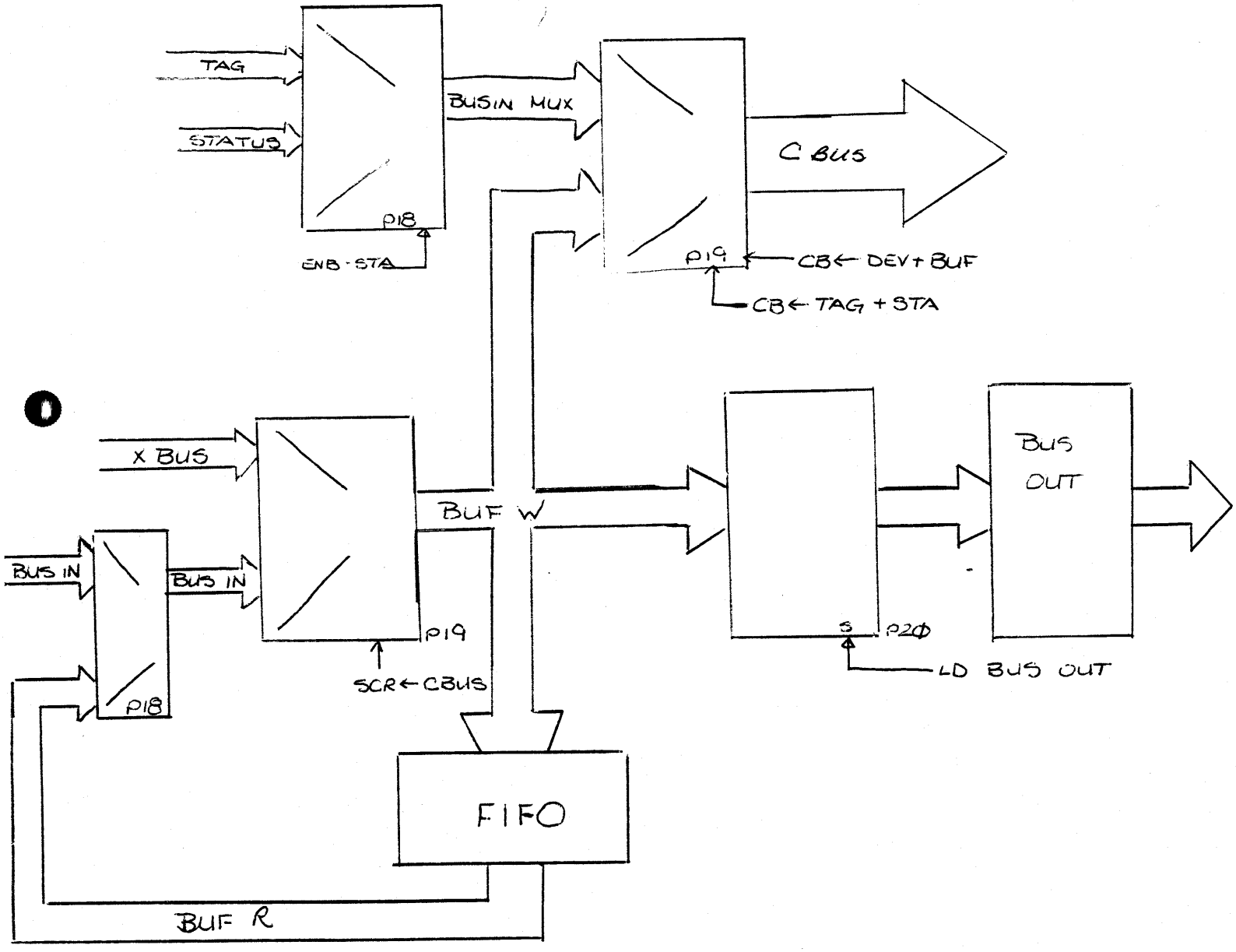


BASE ADDRESS SET WITH DIP SWITCHES
* FOUR WORDS PER CHANNEL
IE. BASE ADD 760

CH 0
- 760 - INITIAL COMMAND
- 761 - STATUS WD 1
- 762 - STATUS WD 2.
- 763 - N/U

STATUS WORDS STORED AT BASE ADDRESS + 4 x CHAN # + 1 OR + 2

FIFO DATA PATHS



CR1	CR8	CR9	CRØ	CR11	LD-ADR-OP(LOW)	DST-BUF-OP(LOW)	BUS-OUT←CBUS(LOW)	WRT-REG-B4L	WRT-REG-B3L	WRT-REG-B2L	WRT-REG-B1L	WRT-REG-BØL
A4	A3	A2	A1	AØ	F7	F6	F5	F4	F3	F2	F1	FØ
0	0	0	0	0	1	1	1	0	0	0	0	0
		↓							↓			
0	1	1	1	1	1	1	1	0	0	0	0	0
1	0	0	0	0	1	1	1	0	0	0	0	1
1	0	0	0	1	1	1	1	0	0	0	1	0
1	0	0	1	0	1	1	1	0	0	1	0	0
1	0	0	1	1	1	1	1	0	1	0	0	0
1	0	1	0	0	1	1	1	1	0	0	0	0
1	0	1	0	1	1	1	0	0	0	0	0	0
1	0	1	1	0	1	0	1	0	0	0	0	0
1	0	1	1	1	1	0	1	0	0	0	0	0
1	1	0	0	0	1	1	1	0	0	0	0	0
1	1	0	0	1	1	1	1	0	0	0	0	0
1	1	0	1	0	1	1	1	0	0	0	0	0
1	1	0	1	1	1	1	1	0	0	0	0	0
1	1	1	0	0	0	1	1	0	0	0	0	0
1	1	1	0	1	1	1	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0	0
1	1	1	1	1	1	1	1	0	0	0	0	0

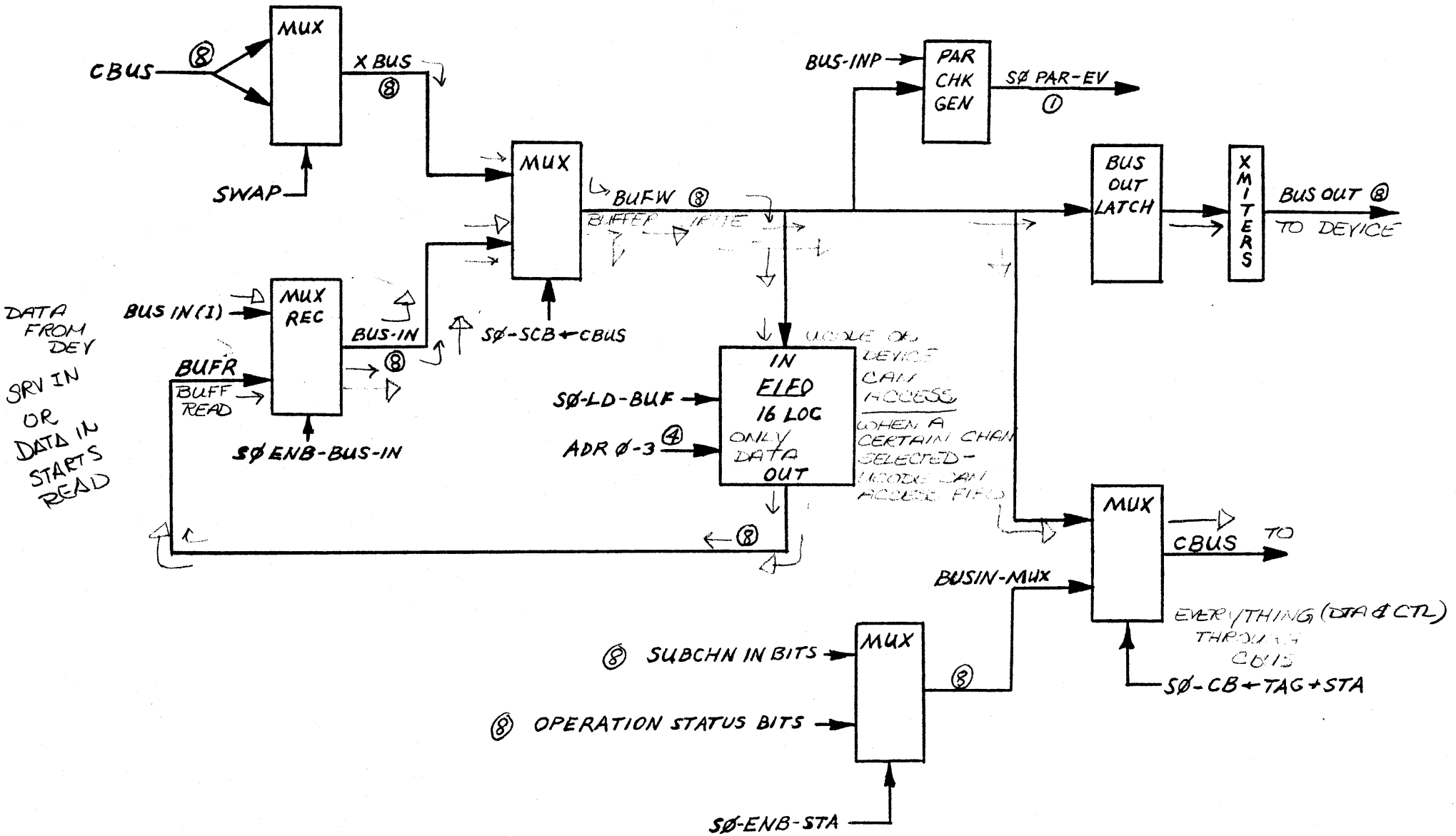
PROM #2Ø 1C29

GROUND	ADR-SEL	-MEM GO B	CR6	CR7		DECR(B2)	DECR(B1)	ADR-CRY-CMPL (LOW)	ADR-CRY-ENB (LOW)	ADRSEL 1 (B2) (LOW)	ADRSEL 1 (B1) (LOW)	ADRSEL Ø (B2) (LOW)	ADRSEL Ø (B1) (LOW)	
A4	A3	A2	A1	AØ		F7	F6	F5	F4	F3	F2	F1	FØ	ADRIN MUX SEL
0	0	0	0	0		0	0	0	0	0	0	0	0	3
0	0	0	0	1		0	0	0	0	0	0	0	0	3
0	0	0	1	0		0	0	0	0	0	0	0	0	3
0	0	0	1	1		0	0	0	0	0	0	0	0	3
0	0	1	0	0		0	0	1	0	1	1	1	1	0
0	0	1	0	1		0	0	1	0	1	1	1	1	0
0	0	1	1	0		0	0	1	0	1	1	1	1	0
0	0	1	1	1		0	0	1	0	1	1	1	1	0
0	1	0	0	0		0	0	1	0	1	1	1	1	0
0	1	0	0	1		1	1	0	0	1	1	1	1	0
0	1	0	1	0		0	0	0	1	1	1	0	0	2
0	1	0	1	1		0	0	0	1	0	0	0	0	3
0	1	1	0	0		0	0	1	0	1	1	1	1	0
0	1	1	0	1		0	0	0	1	0	0	1	1	1
0	1	1	1	0		0	0	0	1	1	1	0	0	2
0	1	1	1	1		0	0	0	1	0	0	0	0	3
1	0	0	0	0		0	0	0	0	0	0	0	0	
		↓							↓					
1	1	1	1	1		0	0	0	0	0	0	0	0	

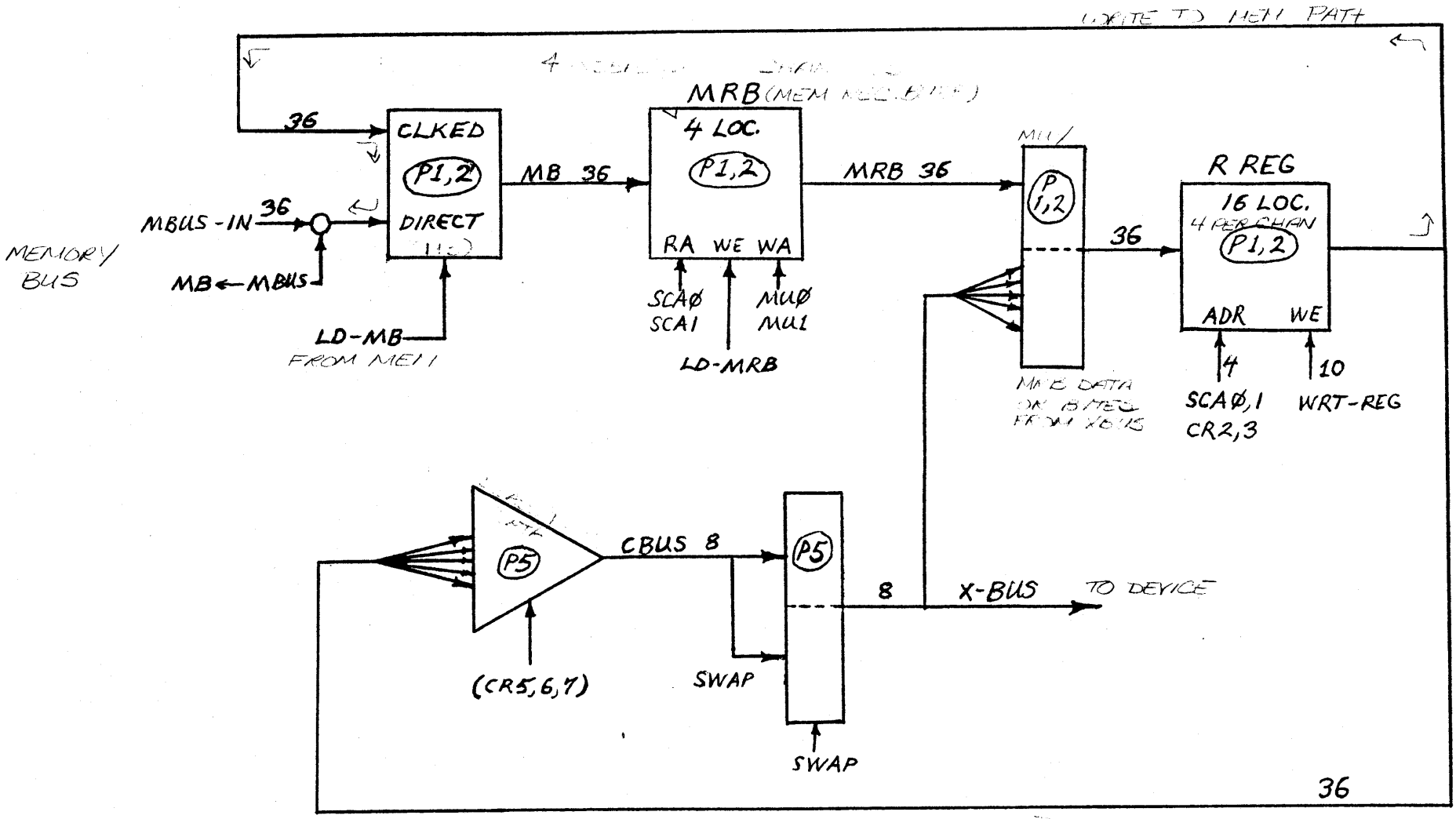
PROM #21 2A13 P4

A4	A3	A2 (CR9)	A1 (CR10)	A0 (CR11)	F7 (WRT-REG-B4R)	F6 (WRT-REG-B3R)	F5 (WRT-REG-B2R)	F4 (WRT-REG-B1R)	F3 (WRT-REG-B0R)
0	0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	1	0
0	0	0	1	0	0	0	1	0	0
0	0	0	1	1	0	1	0	0	0
0	0	1	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0
0	1	0	0	1	0	0	0	0	1
0	1	0	1	0	0	0	0	1	0
0	1	0	1	1	0	0	1	0	0
0	1	1	0	0	0	1	0	0	0
0	1	1	0	1	0	0	0	0	0
		↓					↓		
1	0	1	0	0	0	0	0	0	0
1	0	1	0	1	1	1	1	1	1
1	0	1	1	0	0	0	0	1	0
1	0	1	1	1	0	0	0	0	0
		↓					↓		
1	1	1	1	1	0	0	0	0	0

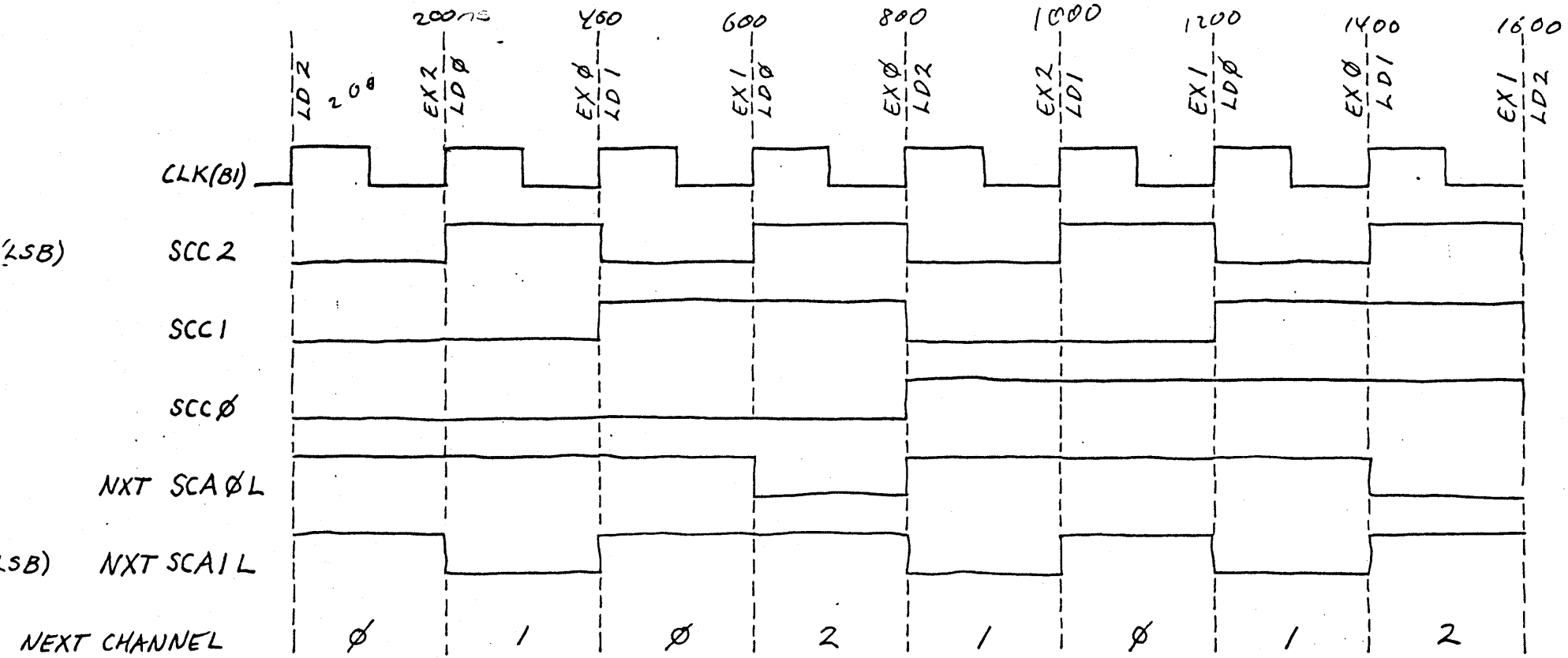
PROM #22 1A24 P9

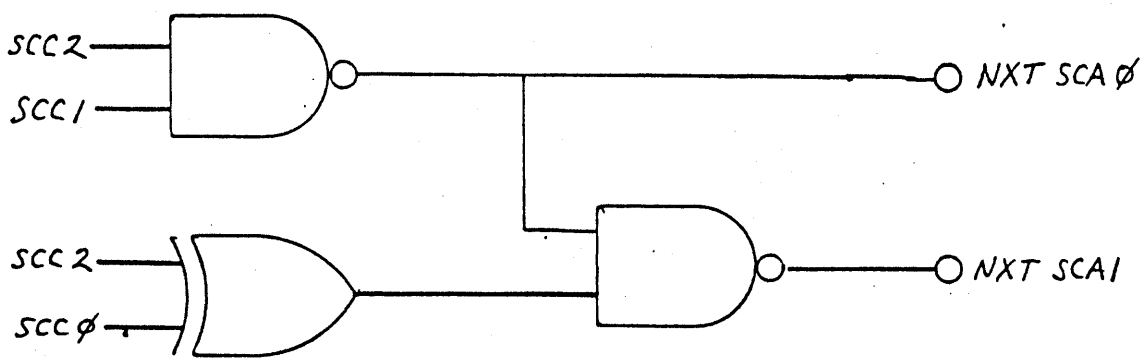


CHANNEL BUSES



MEMORY DATA BUSES





2 CHANNEL TIMING

GLOSSARY

The numbers refer to the drawing sheets.

ACKN	12	memory bus multiplexor (MX10) acknowledge
ADDR13-35	3	latches hold A reg outputs stable while they are being written
ADR.CR4	9	XANC microinstruction with bit 4 true
ADR.CR5	9	XANC microinstruction with bit 5 true
ADR-CRY-CMPL	4	ADR carry complement (for decrementing)
ADR-CRY-ENB	4	ADR carry enable
ADR-HLT-SW	15	address halt switch
ADR-IGN-SW	15	address ignore switch
ADRIN13-35	4	multiplexed input to the A registers
ADR-SEL	9	-CR0.CR1, XANC instruction
ADRSEL0-1	4	select source for ADRIN bus
AS6-15	15	address select switches
AS=IAR	15	IAR matches console address switches
BADR25-31	4	switches control base address
BRANCH	11	when true, low order bit of IAR is complemented
BUF-BRANCH	10	buffer reference branch because data transfer finished
BUF-DUMMY	10	an attempt to take a FIFO cycle somehow inhibited
BUF-HANG	10	microcode hang until FIFO IS AVAILABLE
BUF-OP	10	FIFO reference, source or destination
BUS-OUT<CBUS	9	destination is BUS OUT register
BUSY	10	
BUSY-SY	10	
BYTE-MODE	10	BYTE MODE, selected by SCA number
CBUS0-7	5 and 19	main 8-bit data path
CBUS<B0-3	9	source field is 00xx
CBUS<B4-5	9	source field is 001x
CBUS<DEV	9	source field is 10xx
CLEN	14	clock enable
CLK(B1)	14	
CLK(B1)-	14	
CLK(B2)	14	
CLK(B2)-	14	
CLK(B3)	14	
CLK(B4)	14	
CLK0	14	Clock gated with CLEN
CLKT1	14	
CLR-MB-LT	12	clear MB (left)
CLR-MB-RT	12	clear MB (right)
CLR-STA-S0	9	clear operation status bits, subchannel 0
CLR-STOP	14	clears STOP-RQ
CLR-TAG-S0	9	clear subchannel tags, subchannel 0
CON27-32	13	IO BUS bits saved from last CONO
CONDB	15	console condition flip-flop
CONT(NO),(NC)	15	continue switch

CONT	14	continue after clock stop
CR0-15	(7) 53	register where microinstructions are decoded
CRD0-15	53	and 128, 3-state bus that is the input to CR
CROBAR	12	from power supply sequencer
CRY16	4	carry out of incrementor bit 16
CRY20	4	" " " " 20
CRY24	4	" " " " 24
CRY28	4	" " " " 28
CRY32	4	" " " " 32
DECR	4	controls incrementor to decrement
DEV-DONE	10	"DEV-DONE" signal gated from the appropriate subchannel
DEV-DONE-SY	10	
DEV-MATCH	11	same device address in block multiplexor mode
DAIG16-35	5 and 6	20-bit diagnostic bus
DIAG-ON-BUS	13	set one clock after RD-DIAG; gates IO BUS drivers
DIAG-SEL-A,B	15	controls gating to DIAG bus
DIAG-SEL1-2	15	controls gating to DIAG bus
DST-BUF-OP	9	destination is subchannel FIFO
DST=7	9	Destination field = 7, referring to subchannel FIFO with byte halves swapped
EXT-FN	9	-CR0.-CR1.-CR2.-CR3
EXT-SENSE	6	response from external mystery device
FIX-WC	10	signal used to increment WC if final word is not completely filled
FLG-WRT-RQ	13	remembers CONO to set or reset flag
HI0	13	+3 volts to panel 0
HI1	12	+3 volts to panel 1
HI2	12	+3 volts to panel 2
HOLD-ADDR	14	enable to A reg holding latch
IAR6-15	(7)53	Instruction Address Register, 4x10 RAM
IAR7-14	8	IAR inverters
IARB6-15	(7)53	value of IAR for this instruction
IGN-SPLIT-BYTE	10	attempt to move split byte in byte mode is treated as a no-op
INCR13-35	4	five 4-bit partial sums of A+1
INCR-WC	10	automatic increment of word count
INTR	13	PDP-10 interrupt--channel or memory error
IOB<STAT	13	gates IO BUS drivers
IOBUS26-35	41	from IO BUS receivers
IO-DAT16-35	6	to IO BUS drivers for CONI or DATAI
IO-FLG-WRT	13	flag set or reset due to CONO--clocked ff
JAM-CR	11	CR is to be loaded from special source
LC-SW-COND	15	light control switch
LC-SW-MEM	15	" " "
LD-ADR	9	signal used to load an A register
LD-ADRA-E	4	controlled by LD-ADDR and preceeding carries
LD-ADR-OP	9	destination is an A register
LD-CR	11	
LD-IAR12-15	11	

LD-IAR6-7	11	
LD-IAR8-11	11	
LD-LR	15	load the lights register
LD-MA	12	load MA from A reg--memory cycle
LD-MB-LT	12	load MB (left) from R reg--memory cycle
LD-MB-RT	12	(right)
LD-MRB	12	MB to MRB at end of memory cycle
LD-STA-S0	9	load operation status bits, subchannel 0
LD-TAG-S0	9	load subchannel tags, subchannel 0
LITIG-35	6	20 light drivers
LITE-SEL0-2	15	display selection switches
LOC	7	D.C. voltage from power sequencer to be connected to PWR ON to bring power up
MA14-35	3	memory address register
MADR<MA	12	gate address to memory
MB0-19	1	memory buffer register
MB20-35	2	memory buffer register
MBD32-35	2	data to be stored in bottom half-byte of word
MB<MBUS-LT	12	catch fetch data
MB<MBUS-RT	12	(right)
MBP	1	parity bit for MB
MB-PAR-A	1	parity on MB0-11
MB-PAR-B	1	parity on MB12-23
MB-PAR-C	1	parity on MB24-35
MB-PAR-EV	1	MB (including MBP) has even parity
MBUS<MB-LT	12	strobe pulse to level shifters, memory data left half
MBUS<MB-RT	12	strobe pulse to level shifters, memory data right half, and control signals
MC-ADR-ACK	12	Address Acknowledge from cable receiver
MC-ADR-ACK-IN	12	latch remembers ADR-ACK
MC-ADRA	12	ADR-ACK to this unit
MC-BUS-DONE	12	done with memory bus
MC-BUSY	12	memory interface busy--subsequent references will hang
MC-CONTIN	12	catches PDP-10 acknowledgement of SA-10A memory error
MC-DONE-SYNC	12	follows MC-BUS-DONE, clocked
MC-ENB	12	MX10 says this is our memory cycle
MC-ERROR	12	memory error: parity or NX-MEM
MC-FINISH	12	signal which resets MC-BUSY
MC-NXM	12	non-existent memory error
MC-PAR-ERR	12	bad parity on a fetch
MC-REQ-CYC	12	memory cycle request
MC-SET-DONE	12	sets MC-BUS-DONE on write or NX-MEM
MC-WRRQ	3	marks memory cycle as a write
MC-WRT-DONE	12	write done--forms trailing edge of pulses to memory
MC-ZAP	12	abort memory cycle
MEM-GO	12	begin memory cycle
MEM-GO-A	12	memory cycle very likely

MEM-GO-HANG	12	hang because memory interface busy
MHZ10 10MHZ	14	=10Mhz
MHZ5 5MHZ	14	=5Mhz
MPX-CLR	12	abort signal to MX10 multiplexor
MRB0-19	1	memory read buffer RAMs
MRB20-35	2	memory read buffer RAMs
MRB-HANG	11	hang due to fetch not yet compleye
MTR-OUT	13	metering out signal to device controllers. True if a CONI (to any device) has occurred in last 24 msec.
MU0-1	3	remember which channel started current memory cycle
MU0(B1)	3	
MU1(B1)	3	
MWATCH	3	marks memory cycle for console display
NXMS	12	memory busy for 200 usec = non-existent memory
NXT-SCA0-1	(7)53	govern which channel will execute next
OPR-GROUP	9	-CR0.-CR1
PANIC	11	subchannel has received DISCONNECT
PI1-7	13	interrupt lines to PDP-10
PIA0-2	13	IO-BUS33-35 from last CONO: interrupt channel
POR	300,12	power on reset from power supply sequencer
PWRON	12	signal to power sequencer for turn-on
RCBA0-2	9	address lines for those multiplexors which gate REG bits to the right half of CBUS
RCBE	9	REG CBUS enable to multiplexors
RD-DIAG	13	clock-synchronous DATAI
READ-OK	10	word count not yet reached on this channel
READ-OK-SY	10	
READS-DONE	10	word count not yet reached
REG0-19	1	outputs of R reg RAMs
REG20-35	2	outputs of R reg RAMs
REG36-39	2	outputs of TDS RAMs
REG<CBUS	9	everything but a 36-bit wide source
REG<MRB	9	source field is 1101
REM	12	signal to power sequencer for remote turn-on
REQN	12	memory bus multiplexor (MX10) request
RESET	13	
ROMEH	8	enable line for high-addressed half of PROM array
ROMEL	8	enable line for low-addressed half of PROM array
RST	13	POR + IO-RESET
RSTA	13	condition for complete SA-10A reset
RST-SYNC	13	governs reset of RESET
SO-ADR-OUT	20	ADDRESS OUT
SO-BOR<CBUS	21	transfer CBUS to BUS OUT register
SO-BUF-CYC-REQ	21	flip-flop set by SERVICE IN or DATA IN

SO-BUF-EMP	21	subchannel FIFO is empty
SO-BUF-ENB	20	buffer enabled, a subchannel tag
SO-BUF-HLT	21	buffer halt--device done or no more data
SO-BUFRO-7	19	subchannel buffer outputs
SO-BUFWO-7	19	subchannel buffer inputs
SO-BUS-IN	18	eight bits plus parity from control unit
SO-BUS-IN-PERR	21	bad parity from control unit
SO-BUSIN-MUX	18,19	eight-bit bus in subchannel onto which may be gated tags or status
SO-BUS-OUT	20	eight bits plus parity to control unit
SO-BUSY	13	subchannel 0 BUSY (or GO) flag
SO-BYTEM	21	BYTE MODE--subchannel status bit
SO-CB-DEV+BUF	21	gate device or buffer to CBUS
SO-CB-TAG+STA	21	gate tags or status to CBUS
SO-CBUS<DEV	21	gate device BUS IN TO CBUS
SO-CLK	21	
SO-CLKA	21	
SO-CMD-OUT	20	COMMAND OUT
SO-CTRL-ERR	21	subchannel status bit
SO-DEV-BUF-AVL	21	FIFO available to device
SO-DEV-BUF-CYC	21	device buffer cycle
SO-DEV-DONE	21	branch condition from subchannel: Status in or not Operational in
SO-DEV-LST	21	the last buffer cycle was taken for the device end
SO-DSC-IN	18	DISCONNECT IN from control unit
SO-DSI-ACK	21	true for one clock after SO-DEV-BUF-CYC
SO-DTA-IN	18	DATA IN from control unit (High-Speed Transfer Feature)
SO-DTA-OUT	20	DATA OUT to control unit (response to DATA IN)
SO-DTA-OUT-A	21	
SO-ENB-BUS-IN	21	enable BUS IN through receivers
SO-ENB-STA	21	enable status bits through multiplexor
SO-HLD-OUT	20	HOLD OUT
SO-INT-EN	13	subchannel 0 interrupt enable flag
SO-INT-STA0-1	21	subchannel status bits
SO-OPL-OUT	20	OPERATIONAL OUT
SO-PANIC	21	control unit is bewildered--causes jump to microcode 0004
SO-PAR-EV	19	even parity on data byte
SO-PROG-INT	21	subchannel status bit
SO-PTRS-EQ	19	the FIFO is either full or empty if the pointers are equal
SO-SCB<CBUS	21	gate CBUS to buffer
SO-SEL	21	SCA register pointing to channel 0
SO-SEL-ERR	21	subchannel status bit
SO-SEL-OUT	20	SELECT OUT
SO-SRV-IN	18	SERVICE IN from control unit
SO-SRV-OUT	20	SERVICE OUT to control unit--response to SERVICE IN
SO-SRV-OUT-A	21	

S0-STA-FLG	13	subchannel 0 status flag
S0-STA-IN	18	STATUS IN
S0-STA-RQ	13	subchannel 0 status request flag
S0-SUP-OUT	20	SUPRESS OUT
S0-SW	15	channel select switch
S0-UC-BUF-AVL	21	FIFO available to microcode
S0-UC-BUF-CYC	21	microcode buffer cycle
S0-UC-W-BUF-CYC	21	microcode write buffer cycle
S0-WRT	20	WRITE (data to device), a subchannel tag
***Preceeding signals are specific to subchannel 0. To ***generalize to subchannel n, add 2n to page number.		
SA0-CONO-CLR	13	first pulse of a CONO
SA0-DATAO-CLR	13	first pulse of a DATAO
SA0-SEL	13	PDP-10 selects SA-10 on I/O bus
SCA0,1	(7) 53	subchannel active
SCA0(B1)	(7) 53	
SCC0-2	(7) 53	major cycle counter
SCH-RST	13	subchanne reset, clocked
SCH-RST-CLR	13	jams a GOTO into CR
SCH-RST-RQ	13	remembers subchannel reset CONO
SCOPE-SYNC	15	
SC-SEL-SW	10	NXT lines match a switch-selected channel
SEL-R3		CR2.CR3
SRC-BUF-OP	9	source field is 1110 (FIFO)
SRC-BUF-OP1	9	source field is 1111 (FIFO with byte halves swapped)
STA-FLG	10	
STA-FLG-SY	10	
STA-RQ	10	
STA-RQ-SY	10	
STATUS-INT	13	PDP-10 interrupt from channel
STOP-RQ	14	stop request from CONO
SW-COND	15	console switch conditions met
SW-STOP	15	clock stop for console switches
SWAP	9	byte halves of CBUS are to be swapped as they are gated to XBUS
TIMER	11	12.2 usec waveform
UC-BUF-AVL	10	subchannel FIFO available to microcode
UC-BUF-CYC	10	microcode buffer cycle
UC-FLG-WRT	9	-CR0.-CR1.-CR2.CR3
UCLK	14	ungated clock
WC-OC	3	MSB of ADDR used to signify WC negative
WRT-FLGS-A	13	write BUSY and STATUS REQUEST flags
WRT-FLGS-B	13	write STATUS and INTERRUPT ENABLE flags
WRT-REG-B0L-B4L	9	write pulses to R register destination bytes 0-4, left four bits
WRT-REG-B0R-B4R	9	write pulses to R register destination bytes 0-4, right four bits
XBUS0-7	5	eight bit data path equal either to CBUS, or to CBUS with right and left halves swapped

```
 H
A short list of SA-10 commands:

#A      basic channel test for subchannel #

##,#B   write or update BAT blocks on subchannel #
               (will ask for more information) (UWP(##)=-1)

##,#C   check disk drives on subchannel # control unit ## (read only test)
               (default control unit device code = 300)

##,#D   disk test for drives on subchannel # control unit ##
               (default control unit device code = 300)
               (UWP=0 maintenance cyl only  UWP=-1 all cyl)
               (writes on packs)

#E      set right half of 'switches' (if zero don't exit on error)
                1=suppress error typeout
                2=ring bell instead of error typeout
                4=enter DDT on error
      (default) 10=stop test, return to command scanner if error

###,##,#F format drive ## on subchannel # (UWP(##) must be -1)
               ###=mode for FMTM
                 0=normal mode
                 1=write RO
                 2=write RO and HA
               if pack was previously an RP06 pack use mode=2

##,#Gsingle cylinder seek routine on drive ##, channel #

H       print this text

#I      zero to set flag to run interference chan prog during disk & tape test
               (zero is normal case)

J       select channel and units to be made available for testing.
         (option: ##,#J - ##=unit, #=channel (null=0))

##,#K   seek test for disk drives on subchannel # control unit ##
               (doesn't write on packs)

#L      set left half of 'switches' (cause STATIC to loop on err # routine)
               (octal test number)

#M      memory test using subchannel

##,#N   loop selecting device ## on subchannel #

#P      line printer test for subchannel #

Q       report SA-10 crystal frequency

#R      print internal registers for subchannel #

S       static test. internal test of SA-10 (old BEG)

##,#T   quick tape test for drive ## on subchannel #

##,#U   set 'use whole pack' state to ## for drive # (0=maint cyls only)
               (## not specified means -1)

##,##V   verify disk surfaces on drives on subchannel #
               (UWP must be -1 for all drives to be tested)
               (writes on packs)

W       report controller configuration

X       exit to EDDT

##,#Y   fast reliability test for disk drives on subchannel # control unit ##
               (writes on packs)

##,#Z   read and reset error counters for device ## on subchannel #

=
```