BCC-500 CHIO MULTIPLEXER - IMP INTERFACE

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THE CHIO/IMP INTERFACE IS A FULL DUPLEX BIT-SERIAL UNIT PYSICALLY LOCATED IN THE CHIO MULTIPLEXER. IT IS LOGICALLY DIVIDED INTO A CHIO-TO-IMP AND A IMP-TO-CHIO SECTION. EACH SECTION CONTAINS A 8-BIT SIFT REGISTER (AND CONTROL LOGIC), ONE OF WHICH IS FOR SHIFITING BITS TO THE CHIO FROM THE IMP AND THE OTHER FOR SHIFTING BITS FROM THE CHIO TO THE IMP.

IN GENERAL, THE COMMUNICATION IN EITHER DIRECTION WORKS AS FOLLOWS: WORDS OR BYTES ARE TAKEN ONE AT A TIME FROM THE SENDER'S MEMORY AND TRANSFERRED BIT SERIALLY ACROSS THE INTERFACE TO THE RECEIVER, WHERE THEY ARE REASSEMBLED INTO WORDS OR BYTES OF THE APPROPRIATE LENGTH AND STORED INTO MEMORY. THE IMP STORES AND FETCHES 16 BITS AT A TIME, THE CHIO ONLY 8. THE TRANSMISSION THUS CONSISTS OF A BIT TRAIN CONTAINING NO SPECIAL INDICATIONS OF WORD BOUNDARIES BUT DELAYED OCCASIONALLY WHILE THE SENDER FETCHES, OR THE RECEIVER STORES. THE HIGH-ORDER BIT OF EACH WORD IS TRANSMITTED FIRST.

CHIO/IMP HANDSHAKING

BIT TRANSFER IS ASYCHRONOUS, THE TRANSMISSION OF EACH BIT BEING CONTROLLED BY A READY-FOR-NEXT-BIT, THERE'S-YOUR-BIT HANDSHAKING FEATURE. EACH BIT IS TRANSFERRED ONLY WHEN BOTH SENDER AND RECEIVER INDICATED PREPAREDNESS. THIS PERMITS EITHER THE SENDER OR THE RECEIVER TO HOLD UP THE TRANSMISSION BETWEEN ANY TWO BITS IN ORDER TO TAKE AS MUCH TIME AS NECESSARY TO GET A NEW WORD OR BYTE IN OR OUT OF MEMORY, OR TO ACTIVATE AN INTERRUPT ROUTINE THAT SETS UP NEW INPUT OR OUTPUT BUFFERS. NEITHER THE SENDER NOR THE RECEIVER EXPECT THAT THE TRANSMISSION SHOULD TAKE PLACE AT A PRE-DETERMINED BIT RATE AND EACH ARE ABLE TO ACCEPT ARBITRARY DELAYS INTRODUCED BY THE OTHER AT ANY POINT IN THE BIT TRAIN.

THE INTERFACE USES A FOUR-WAY HANDSHAKE. IN THE FOUR-WAY HANDSHAKE THE RECEIVER AWAITS THE DROPPING OF THERE'S-YOUR-BIT BEFORE RAISING READY-FOR-NEXT BIT. A FULL CYCLE OF THE FOUR-WAY HANDSHAKE WORKS AS FOLLOWS: THE IMP READIES THE NEXT DATA BIT AND THE THERE'S-YOUR-IMP BIT SIGNAL IS SENT TO THE INTERFACE (1ST CABLE TRANSIT) THE INTERFACE TAKES IN THE BIT AND NOTIFIES THE IMP BY DROPPING READY-FOR-NEXT-IMP BIT (2ND CABLE TRANSIT). THE IMP RESPONDS BY DROPPING THE THERE'S-YOUR-IMP BIT SIGNAL (3RD TRANSIT) AND AFTER THE INTERFACE HAS NOTED THIS, THE READY-FOR-NEXT-IMP BIT SIGNAL CAN BE TURNED BACK ON (4TH CABLE TRANSIT), REGISTERING PREPAREDNESS FOR A NEW BIT.

THE IMP ITSELF USES A TWO-WAY HANDSHAKE, WHEN IT RECEIVES FROM THE INTERFACE THE ACTION IS AS FOLLOWS: THE INTERFACE READIES THE NEXT DATA BIT AND THE THERE'S-YOUR-HOST BIT SIGNAL IS SENT TO THE IMP (1ST CABLE TRANSIT). THE IMP TAKES IT IN AND NOTIFIES THE INTERFACE BY DROPPING READY-FOR-NEXT-HOST BIT (2ND CABLE TRANSIT). INSTEAD OF WAITING FOR THIS SIGNAL TO PROPAGATE TO THE INTERFACE AND THE RESULTANT DROPPING OF THERE'S-YOUR-HOST BIT TO RETURN, THE IMP HOLDS READY-FOR-NEXT-HOST BIT OFF FOR AT LEAST ONE MICROSECOND AND THEN TURNS IT BACK ON.

THE TWO-WAY HANDSHAKE IS SUBJECT TO A COUPLE OF RACE CONDITIONS AND THEREFORE THE IMP PUTS IN THE LONG DELAY. SINCE OUR CHIO INTERFACE IS LOCATED FAIRLY CLOSE TO THE IMP, THE TIME DELAYS INVOLVED IN THE EXTRA TWO CABLE TRANSITS ARE STILL SMALL AND THEREBY THE LINK IS FASTER WHILE STILL BEING INTERLOCKED SAFELY. THE FOUR-WAY HANDSHAKE IS THE SAME PROTOCOL THAT IS USED BY THE LINK TO THE HP 2100.

DETAILED THEORY OF OPERATION

IMP-TO-CHIO COMMUNICATION

FIRST LET'S CONSIDER THE SECTION THAT RECEIVES BITS FROM THE IMP, AND ASSUME THE CHIO HAS JUST READ IN A BYTE SO THAT THE SHIFT REGISTER IS EMPTY. AS LONG AS THE SHIFT REGISTER IS NOT FULL AND THE THERE'S-YOUR-IMP BIT IS FALSE THE RECEIVER ASSERTS READY-FOR-NEXT-IMP BIT. WHEN THE IMP RAISES THE THERE'S-YOUR-IMP BIT LINE IT PRIMES THE PULSE SYCHRONIZER (74120), WHICH THEN PASSES THE NEXT K2 TICK AS RECEIVE

BIT CLOCK (RBC). THIS WILL MAKE THE SHIFT SIGNAL BECAUSE THE AND OF RBC AND NOT PAD AND NOT FULL WILL BE TRUE. THE IMP DATA BIT WILL BE SHIFTED INTO THE 8-BIT SHIFT REGISTER (74164) AND THE COUNT OF BITS ASSEMBLED SO FAR WILL BE INCREMENTED BY ONE (7493). READY-FOR-NEXT-IMP BIT DROPPED WHEN THERE'S-YOUR-IMP BIT CAME TRUE--SIGNALLING THE IMP THAT THE CHIO INTERFACE WAS ACCEPTING THE BIT, AND TO READY THE NEXT BIT. THIS PROCESS REPEATS UNTIL AFTER THE SEVENTH BIT IS SHIFTED INTO THE RECEIVER. AT THIS POINT THE AND GATE ON THE OUTPUTS OF THE COUNTER GOES HIGH IDICATING THE NEXT BIT IS THE LAST ONE. WITH THE ARRIVAL OF THE EIGHTH BIT THE SHIFT REGISTER FULL FF IS SET BY THE SHIFT SIGNAL. SINCE THE FULL FF IS SET, EVEN THO THE THERE'S-YOUR-IMP BIT DROPS THE READY-FOR-NEXT-IMP BIT DOES NOT COME BACK UP UNTIL AFTER THE CHIO READS IN THE BYTE AND THUS RESETS THE FULL FF. AS EACH BIT IS SHIFTED IN THE LAST-IMP-BIT LINE IS SAMPLED. IF IT IS TRUE INDICATING THE END OF AN IMP PACKET THE REST OF THE 8-BIT BYTE MUST BE PADDED OUT WITH ZERØ'S. THE SAMPLED LAST-IMP-BIT SETS THE PAD FF. PAD BEING TRUE PASSES K2 TICKS AS SHIFT PULSES AS LONG AS FULL IS NOT TRUE, AND FORCES ZERO'S INTO THE SHIFT REGISTER. THE READY-FOR-NEXT-IMP BIT CANNOT BE ASSERTED WHILE PAD IS TRUE, AND SO THE IMP IS FORCED OT WHILE AWAY THE TIME UNTIL THE SHIFT REGISTER IS FILLED AND THE BYTE IS READ IN BY THE CHIO.

CHIO-TO-IMP COMMUNICATION

SUPPOSE THE CHIO IS INITIATING TRANSFER OF A NEW BYTE OF ONE TO EIGHT BITS TO THE IMP. THE POT DIRECTED TO THE INTERFACE LOADS AN 8 BIT SHIFT REGISTER (74165), INITIALIZES THE BIT COUNTER (74191), SETS THE TRANSMIT SHIFT REGISTER FF (74279) AND THE HOST BIT AVAILABLE FF

(74H74).

HOST BIT AVAILABLE IS AND'ED WITH READY-FOR-NEXT-HOST BIT TO PRODUCE THERE-IS-YOUR-HOST BIT--THE SIGNAL THAT THE HOST DATA OUT LINE HAS A NEW BIT FOR THE IMP.

WHEN THE IMP READS IN THE HOST BIT IT DROPS READY-FOR-NEXT-HOST BIT, THIS RESULTS IN THE THERE'S-YOUR-HOST BIT GOING DOWN, AND STARTS THE LOGIC IN MOTION TO SHIFT THE NEXT BIT OUT FOR THE IMP BECAUSE THE NEXT K2 CLOCK PULSE AFTER READY-FOR-NEXT-HOST BIT FALLS WILL BE PASSED BY THE PULSE SYCHRONIZER (74120). THE TRANSMIT BIT CLOCK (TBC) RESETS HOST-BIT-AVAILABLE--SO THAT THERE-IS-YOUR-HOST BIT WILL STAY LOW UNTIL A NEW DATA BIT IS MADE AVAILABLE. HOST BIT NOT AVAILABLE AND TRANSMIT REGISTER FULL 'AND' TO ALOW THE NEXT K2 TO SHIFT THE OUTPUT SHIFT REGISTER (74165) AND SET THE HOST BIT AVAILABLE FF. CONSEQUENTLY THERE'S-YOUR-HOST BIT WILL BE SENT TO THE IMP AS SOON AS READY-FOR-NEXT-HOST BIT IS ASSERTED. AT WORST IT TAKES THE INTERFACE 300 NS TO SHIFT THE NEXT BIT OUT IF THE TRANSMIT SHIFT REGISTER IS STILL FULL.

AT THE SAME TIME THE SHIFT REGISTER IS ROTATED ONE THE BIT COUNTER IS DECREMENTED BY ONE. WHEN THE BIT COUNT REACHES ONE THE LAST HOST BIT SIGNAL IS ALSO ASSERTED ALONG WITH THERE-IS-YOUR-HOST BIT IF THE LAST BYTE MARKER BIT WAS SET WHEN THE BYTE WAS LOADED BY THE CHIO. THE TRANSMIT SHIFT REGISTER FULL FF IS RESET SO THAT AFTER THE LAST BIT OF THIS BYTE IS TAKEN (READY-FOR-NEXT-HOST BIT GOES DOWN) THE SHIFT PROCEDURE WILL BE BLOCKED UNTIL THE CHIO REFILLS THE SHIFT REGISTR WITH ANOTHER OUTPUT BYTE.

THE BIT COUNT MAY LOGICALLY BE ANY NUMBER BETWEEN ONE AND EIGHT. NOTING THAT EIGHT WILL BE THE COUNT MOST OFTEN USED, AND THAT A BIT COUNT OF ZERO DOESN'T MAKE SENSE, A ZERO COUNT FIELD FORCES THE

COUNT TO EIGHT. THUS THE DEFAULT FIELD IS HOPEFULLY THE MOST USEFUL ONE. IT ALSO SAVES ONE VERY VALUABLE CONNECTOR PIN.

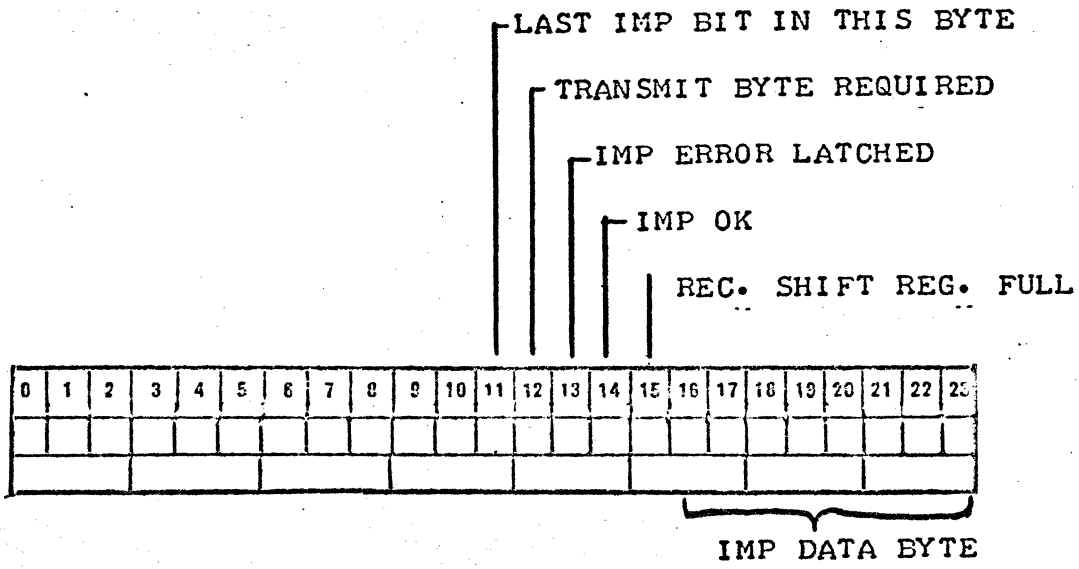
INTERFACE-CHIO COMMUNICATION

THE INTERFACE IS TREATED IN THE CHIO MPXR AS ALMOST A STANDARD HIGH-SPEED MODEM. MODEM NUMBER 6 IS NOT IN THE MPXR, SO ITS ADDRESS IS USURPED FOR THE INTERFACE. THE COMMUNICATION WITH THE HIGH-SPEED MODEMS IS COVERED IN CHUCK THACKER'S CHIO MULTIPLEXER SPECIFICATION NCHIO/S-17.1, PAGE 5. THE ADDRESSING FOR INPUT AND OUTPUT TRANSFERS IS EXACTLY AS DISCRIBED, WITH THE DEVICE ADDRESS BEING 4B7+1Ø6. THE FORMAT OF THE DEVICE ADDRESS IS AS FOLLOWS:

BIT:	MEANING:
Ø	1 TO SPECIFY I/O HARDWARE
1	1 FOR INPUT, Ø FOR OUTPUT
2-15	NOT INTERPRETED
16	IF THIS BIT IS ON AND BIT 1 IS ON THEN THE RECEIVER DATA AND STATUS BITS ARE ALL CLEARED AFTER READING.
17-23	1Ø6B TO SPECIFY THE INTERFACE

THE DIFFERENCES ARE IN THE ASSIGNMENT OF BITS IN THE I/O WORDS TRANSFERRED. WE DISCUSS THAT NEXT.

THE BITS OF THE E2 BUS THAT ARE READ ONTO THE Y BUS ARE INTERPRETED AS:

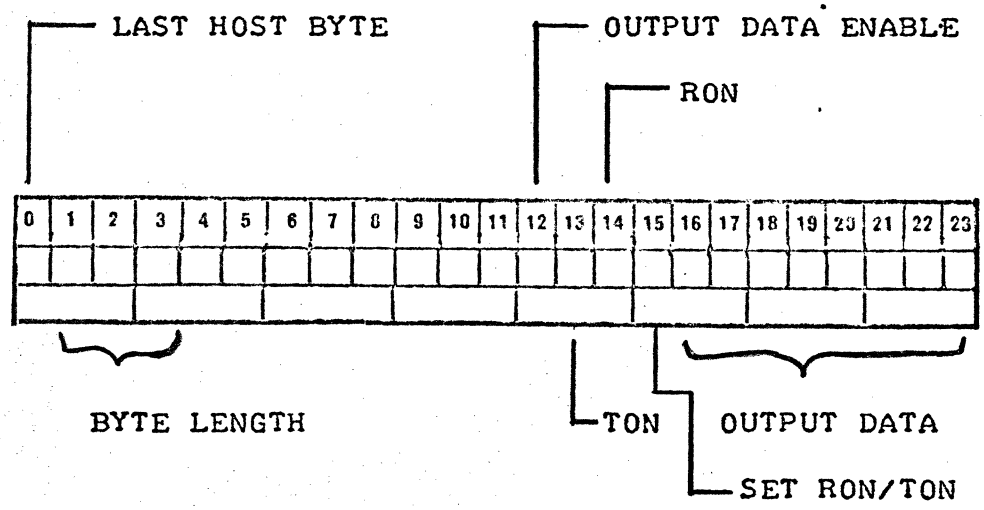


IF THE RECEIVER ON (RON) CONTROL BIT IS SET, THEN ATTENTION 2 WILL BE SENT TO THE CHIO WHENEVER THE RECEIVE SHIFT REGISTER IS FULL. IF ATTENTIONS ARE DISABLED THEN THE INTERFACE MAY BE HANDLED BY TESTING ON THE REC. SHIFT REG. FULL STATUS BIT. RON AND REC. SHIFT REG. FULL MAY COME ON IN EITHER ORDER TO SET ATTN 2.

IMP OK AND IMP ERROR LATCHED WILL BE DISCUSSED LATER.

CHIO-INTERFACE COMMUNICATION

DATA FOR THE IMP AND CONTROL FOR THE INTERFACE IS LOADED INTO THE INTERFACE BY AN ALERT - POT SEQUENCE. THE ALERT ADDRESS MAY BE EITHER 105B OR 305B--THE 16 BIT IS NOT USED. THE BITS THAT ARE PRESENTED ON THE Z BUS DURING THE POT ARE USED AS FOLLOWS:



DATA AND CONTROL FIELD LOADING IS SEPARATELY ENABLEABLE BY BITS 12 AND 15 RESPECTIVELY. THEY MAY BE BOTH ON (AS WHEN OUTPUTTING THE FIRST OR LAST BYTE SAY) OR NEITHER ON (AS WHEN A POT IS DONE SOLELY TO MAINTAIN THE HOST OK TIMER TO THE IMP, TO BE DISCUSSED LATER).

THE TRANSMIT ON BIT (14) INTERACTS WITH THE TRANSMIT SHIFT REGISTER FULL FLAG IN EXACTLY THE SAME WAY AS WAS COVERED FOR RON IN SENDING ATTENTION 2 TO THE CHIO.

WHEN IN THE MIDDLE OF TRANSFERRING A PACKET SAY OUT TO THE IMP ALL THAT IS NEEDED IS TO PUT A RIGHT JUSTIFIED 8-BIT BYTE ON THE Z BUS, MERGE IN A 400B AND POT TO EFFECT A DATA LOAD AFTER THE ALERT.

IMP & HOST OK SIGNALS

THERE IS A SET OF RELAY CONTACTS IN BOTH THE IMP AND CHIO INTERFACE THAT MAY BE INTERROGATED TO DETERMINE THE HEALTH OF THE OTHER PROCESSOR. THE IMP OK PAIR WILL BE SHORTED BY THE RELAY WHEN 1) THE CABLE CONNECTING THE CARDS IS IN PLACE. 2) THE POWER IS ON TO THE TIP/IMP AND 3) WHEN THE PROGRAM IN THE IMP IS HEALTHY ENOUGH TO GOOSE A TIMER EVERY SO OFTEN. WHEN THERE DOES EXIST SUCH CONTINUITY A SIGNAL CALLED IMP OK IS MADE ON THE CHIO INTERFACE WHICH HAS THE FOLLOWING USE. THE THERE'S-YOUR-IMP BIT AND THE READY-FOR-NEXT-HOST BIT SIGNALS FROM THE IMP CAUSE THE INTERFACE TO INITIATE ACTIVITY IN SHIFTING BITS INTO OR OUT OF THE LINK. THE IMP OK SIGNAL IS USED TO GATE THESE TERMS SO THAT NO SHIFTS ARE DONE UNLESS THE IMP IS UP, AND THEREFORE THEY ARE MEANINGFUL AND NOT POSSIBLY JUST NOISE.

ON THE HOST SIDE THE RELAY CONTACTS ARE HELD CLOSED BY A ONE SECOND TIMER, WHICH IS TRIGGERED BY ANY POT OR PIN ACTIVITY DIRECTED TO THE INTERFACE. THESE MAY BE EITHER REALLY I/O COMMANDS IN RUNNING THE LINK, OR THEY MAY BE "DUMMY" COMMANDS SOLELY FOR THE PURPOSE OF HOLDING THE TIMER CLOSED. THAT IS POTS WITH BOTH DATA AND CONTROL ENABLE BITS OFF, OR PINS WITH BIT 16 IN THE ALERT OFF. WHEN BRINGING UP THE CONNECTION AND CLOSING THE RELAY THERE NO DOUBT WILL BE CONTACT BOUNCE. ASIDE FROM THE PROGRAMMING OF NOP'S ETC. FOR PROPER HANDLING, THERE ALSO IS A SECOND TIMER IN THE HARDWARE. IT IS STARTED BY THE SIGNAL CLOSING THE HOST READY RELAY, AND ITS JOB IS TO GATE THE THERE'S-YOUR-HOST BIT AND READY-FOR-NEXT-IMP BIT, SO THAT THEY CAN NOT BE ASSERTED UNTIL THE HOST OK IS STEADY AT THE IMP INTERFACE. THERE

IS ALSO A LATCH THAT LOOKS AT THE IMP OK SIGNAL, AND IS READ IN AS A STATUS BIT ON EACH PIN. THIS BIT SAYS THAT THE IMP HAS DROPPPED OUT, SOMETIME BETWEEN THE TIME LAST READ AND NOW. THE IMP OK STATUS BIT TELLS THE PRESENT STATUS OF THE IMP OK RELAY CONTACTS-READINESS TEST.

HARDWARE AND CONSTRUCTION DETAILS

THE CHIO-IMP INTERFACE IS CONSTRUCTED ON A SINGLE SMALL KLUDGE CARD TO BE PLUGGED INTO THE CHIO MPXR. IT REQUIRES ABOUT 36 IC'S, AND THE CARD CAN HOLD 42. SINCE AN AMP RIBBON CABLE CONNECTOR TAKES A LOT OF REAL ESTATE, THE CABLE IS THEREFORE TERMINATED IN A 25 PIN CINCH DB-25S CONNECTOR MOUNTED ON THE BACK EDGE OF THE CARD. THIS IS 3/4 INCH HIGH SO THE CARD OUGHT TO BE WIRED UP FOR SLOT 12 TO GIVE ENOUGH CLEARANCE. THE INTERFACE LOGICALLY IS CLEAN, BUT THE CABLE... THE IMP INTERFACE MANUAL CALLS FOR A SHIELDED CABLE OF 20 AWG OR LARGER WIRES, WITH AN IMPEDANCE OF 120 OHMS. THEIR DIFFERENTIAL LINE DRIVERS ARE CAPABLE OF PUTTING 18 MA INTO THE LINE. I PROPOSE WE USE SN75110 DIFFERENTIAL LINE DRIVERS ALTHOUGH THEY CAN ONLY SWITCH 12 MA INTO THE LINE. FURTHER THAT WE USE THE SAME KIND OF CABLE AS WILL BE USED IN THE HP-CHIO LINK AND THE LINE PRINTER CABLES. THIS WOULD MEAN A 13 PAIR CABLE VISE A 12 PAIR SHIELD CABLE. THE CHARACTERISTIC IMPEDANCE WOULD BE AROUND 80 OHMS, SO THE TERMINATORS SHOULD BE ADJUSTED AT BOTH ENDS. THE CABLE CONNECTOR MAPPING BETWEEN THE CINCH DB-25P AND THE AMPHENOL SERIES 48 AT THE IMP IS:

CINCH	AMPHENOL	SIGNAL
1	1	LAST IMP BIT
2	2	
3	3	IMP DATA
4	4	
5	5	THERE'S-YOUR-IMP BIT
6	6	
7	7	READY-FOR-NEXT-HOST BIT
8	8	
9	9	SPARE
10	10	
11	11	HOST MASTER READY
12	12	
13	13	IMP READY TEST
14	14	
15	15	SPARE
16	16	
17	17	READY-FOR-NEXT-IMP BIT
18	18	
19	19	THERE'S-YOUR-HOST BIT
20	20	
21	21	LAST HOST BIT
22	22	
23	23	HOST DATA
24	24	
25	31	GROUND

THE ASSERTED LOGIC SIGNAL DRIVES THE ODD-NUMBERED CONNECTOR OF THE PAIR POSITIVE, THE EVEN TO NEGATIVE.

ALSO MOUNTED ON THE REAR EDGE ABOVE THE CINCH CONNECTOR WILL BE 2 RED AND 2 GREEN LED'S. THEY WILL BE ON READY-FOR-NEXT-IMP BIT, THERE'S-YOUR-IMP BIT, READY-FOR-NEXT-HOST BIT AND THERE'S-YOUR-HOST BIT. WHILE ACTUALLY INSTALLED TO AMUSE AND PACIFY THE CHILD IN US, THEY CAN BE RATIONALIZED AS BEING USEFUL IN QUICKLY INDICATING ANY "DEATHLY EMBRACES"--ESPECIALLY DURING INITIAL DEBUGGING.

WIRE WRAP CHANGES

SINCE THE INTERFACE REQUIRES ONE MORE SIGNAL PIN THAN IS AVAILABLE ON THE REGULAR MODEM CARD SLOTS, A NEW SLOT, A012 MUST BE WIRED UP FOR IT. IT IS LOGICALLY ADDRESSED AS MODEM #6 THO SO THE ADDRESS LINES ARE WIRED UP AS:

TO:	FROM:	NAME:
A12-14	A16-14	SCPT6'
A12-15	A16-15	DAPT6'

ALL OF THE OTHER SIGNALS ARE WIRED TO A012 FROM A017 EXCEPT FOR THE FOLLOWING WHICH ARE NOT NEEDED ON THE INTERFACE:

PIN:	SIGNAL:	
A17-5	XZ(10)	REQUEST TO SEND
A17-17	XE2(10)'	CLEAR TO SEND
A17-13	XE2(9)'	CARRIER DETECT
A17-20	GND	NICE TO KEEP, BUT NO CAN
A17-33	XE2(13)'	TRANSMIT ERROR

INSTEAD THOSE PINS ARE WIRED UP AS:

TO:	FROM:	NAME:
A12-5	A30-39	Z(Ø)'
A12-13	A25P-25	Z(3)'
A12-17	A25P-26	Z(2)'
A12-2Ø	A21-1Ø	-5 VOLTS
A12-33	A3Ø-Ø3	Z(1)'

THE UP-DOWN TERMINATION OF Z(Ø)' SHOULD BE REMOVED FROM THE DEVICE ADDRESS CARD.

SOCKET LIST FOR CHIO-IMP INTERFACE

MPXR SLOT A012

PIN:	SIGNAL:
A12-01	GND
A12-02	GND
A12-03	XZ(13)
A12-04	XZ(14)
A12-05	XZ(0)'
A12-06	XZ(15)
A12-07	DA16'
A12-08	XZ(23)
A12-09	XZ(22)
A12-10	XZ(21)
A12-11	XZ(20)
A12-12	XZ(19)
A12-13	XZ(3)'
A12-14	SCPT6'
A12-15	DAPT6'
A12-16	XTREQ'
A12-17	XZ(2)'
A12-18	XRREQ'
A12-19	XE2(11)'
A12-20	-5 VOLTS

A12-21	GND
A12-22	XE2(13)'
A12-23	XNRQ
A12-24	XE2(23)'
A12-25	XE2(22)'
A12-26	XE2(21)'
A12-27	XE2(20)'
A12-28	XE2(19)'
A12-29	XE2(18)'
A12-30	XE2(17)'
A12-31	XE2(16)'
A12-32	XE2(12)'
A12-33	XZ(1)'
A12-34	XE2(14)'
A12-35	XE2(15)'
A12-36	XZ(18)
A12-37	XZ(17)
A12-38	XZ(16)
A12-39	OUTPUT'
A12-40	XZ(12)
A12-41	K2'
A12-42	XINPUT'
A12-43	VCC
A12-44	VCC