D6-50005

AMPEX

35 sheets

update completed 4/24/75

	C	B	A
32			
31		LINE TERMINATOR (B3Ø)	
30	D5Ø (23) D51 (P1)	DATA IN Ø-13 (B29) (12 = PØ)	D5Ø (23) D51 (P1)
29	D46 (19) D47 (2Ø) D48 (21) D49 (22)	GROUND BUS	D46 (19) D47 (2Ø) D48 (21) D49 (22)
28	D42 (15) D43 (16) D44 (17) D45 (18)	DATA IN 14-25 (25 = P1)	D42 (15) D43 (16) D44 (17) D45 (18)
27	D38 (PØ) D39 (12) D4Ø (13) D41 (14)	DATA OUT LINE DRIVER Ø-25	D38 (PØ) D39 (12) D4Ø (13) D41 (14)
26	D34 (Ø8) D35 (Ø9) D36 (1Ø) D37 (11)	POSITIVE LOGIC B DO 2Ø-25 (MIX UPPER/LOWER)	D34 (Ø8) D35 (Ø9) D36 (1Ø) D37 (11)
25	D3Ø (Ø4) D31 (Ø5) D32 (Ø6) D33 (Ø7)	PLB DO Ø-19 (MIX UPPER/LOWER)	D3Ø (Ø4) D31 (Ø5) D32 (Ø6) D33 (Ø7)
24	D26 (ØØ) D27 (Ø1) D28 (Ø2) D29 (Ø3)	PL DO 18-25 & 44-51 (MIX STACKS)	D26 (ØØ) D27 (Ø1) D28 (Ø2) D29 (Ø3)
23	D24 (23) D25 (P1)	PL DO 9-17 & 35-43 (MIX STACKS)	D24 (23) D25 (P1)
22	D2Ø (19) D21 (2Ø) D22 (21) D23 (22)	PL DO Ø-8 & 26-34 (MIX STACKS)	D2Ø (19) D21 (2Ø) D22 (21) D23 (22)
21	D16 (15) D17 (16) D18 (17) D19 (18)	PL	D16 (15) D17 (16) D18 (17) D19 (18)
20	D12 (PØ) D13 (12) D14 (13) D15 (14)	PL MAR 12 LATCH	D12 (PØ) D13 (12) D14 (13) D15 (14)
19	D8 (Ø8) D9 (Ø9) D1Ø (1Ø) D11 (11)	STROBE CONTROL	D8 (Ø8) D9 (Ø9) D1Ø (1Ø) D11 (11)
18	D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)	READ TIMING	D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)
17	DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)	WRITE TIMING	DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)
16	CORE STACK B	DRIVE CONTROL	CORE STACK A
15	J4-28: MAR 12 @ +5.		J4-28: MAR 12 @ GND.
14	RØ(22) = Ø	YS ADDRESS REGISTER BITS 1Ø, 11, 12	RØ(22) = 1
13		YD AR BITS 13, 14, 15	
12		XS AR BITS 16, 17, 18	
11	XS6-TP8 B12 XS7-TP9 B12	XD AR BITS 19, 2Ø, 21	XS6-TP8 B12 XS7-TP9 B12
10	XS4-TP6 B12 XS5-TP7 B12	PARITY TEST CAPAR LATCH	XS4-TP6 B12 XS5-TP7 B12
9	XS2-TP4 B12 XS3-TP5 B12	PARITY GENERATOR DATA BITS	XS2-TP4 B12 XS3-TP5 B12
8	XSØ-TP2 B12 XS1-TP3 B12		XSØ-TP2 B12 XS1-TP3 B12
7	YS6-TP8 B14 YS7-TP9 B14	HEATSINK FOR V_{TH} PROTECTION ZENER.	YS6-TP8 B14 YS7-TP9 B14
6	YS4-TP6 B14 YS5-TP7 B14		YS4-TP6 B14 YS5-TP7 B14
5	YS2-TP4 B14 YS3-TP5 B14		YS2-TP4 B14 YS3-TP5 B14
4	YSØ-TP2 B14 YS1-TP3 B14		YSØ-TP2 B14 YS1-TP3 B14
3	XDØ-XD7 (TP B11) YDØ-YD7 (TP B13)		XDØ-XD7 (TP B11) YDØ-YD7 (TP B13)
2	X CURRENT SOURCE		X CURRENT SOURCE
1	Y CURRENT SOURCE	CURRENT CONTROL MASTER POT. A1 A2 C1 C2	Y CURRENT SOURCE
	C	B	A

DATA LOWER (rows 30–24): J4-46: RDUL @ +5. RØ(23) = Ø

DATA UPPER (rows 23–17): J4-46: RDUL @ GND. RØ(23) = 1

PC CARD PINS 1A THRU 4ØA ARE NUMBERED 1-4Ø
PC CARD PINS 1B THRU 4ØB ARE NUMBERED 51-9Ø
J1 CONNECTOR PINS ARE NUMBERED AS FOLLOWS:

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	BB	CC	DD
1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15	16	17	18	19	2Ø	21	22	23	24	25	26	27	28	29	3Ø

O	RELEASED			
NO.	DESCRIPTION	DATE	DRAWN	APPROVED

REVISIONS

The Aloha System BCC-500

TITLE: AMPEX CORE LAYOUT

DATE: -3 DEC 1974

SHEET 1 OF 4

L Ø1104.Ø

Slot	A	B	C
32	A	B	C
31		LINE TERMINATOR (B30)	
30	D5Ø (23) D51 (P1)	DATA IN Ø-13 (B29) (12 = PØ)	D5Ø (23) D51 (P1)
29	D46 (19) D47 (2Ø) D48 (21) D49 (22)	GROUND BUS	D46 (19) D47 (2Ø) D48 (21) D49 (22)
28	D42 (15) D43 (16) D44 (17) D45 (18)	DATA IN 14-25 (25 = P1)	D42 (15) D43 (16) D44 (17) D45 (18)
27	D38 (PØ) D39 (12) D4Ø (13) D41 (14)	DATA OUT LINE DRIVER Ø-25	D38 (PØ) D39 (12) D4Ø (13) D41 (14)
26	D34 (Ø8) D35 (Ø9) D36 (1Ø) D37 (11)	POSITIVE LOGIC B DO 2Ø-25 (MIX UPPER/LOWER)	D34 (Ø8) D35 (Ø9) D36 (1Ø) D37 (11)
25	D3Ø (Ø4) D31 (Ø5) D32 (Ø6) D33 (Ø7)	PLB DO Ø-19 (MIX UPPER/LOWER)	D3Ø (Ø4) D31 (Ø5) D32 (Ø6) D33 (Ø7)
24	D26 (ØØ) D27 (Ø1) D28 (Ø2) D29 (Ø3)	PL DO 18-25 & 44-51 (MIX STACKS)	D26 (ØØ) D27 (Ø1) D28 (Ø2) D29 (Ø3)
23	D24 (23) D25 (P1)	PL DO 9-17 & 35-43 (MIX STACKS)	D24 (23) D25 (P1)
22	D2Ø (19) D21 (2Ø) D22 (21) D23 (22)	PL DO Ø-8 & 26-34 (MIX STACKS)	D2Ø (19) D21 (2Ø) D22 (21) D23 (22)
21	D16 (15) D17 (16) D18 (17) D19 (18)	PL	D16 (15) D17 (16) D18 (17) D19 (18)
20	D12 (PØ) D13 (12) D14 (13) D15 (14)	PL MAR 12 LATCH	D12 (PØ) D13 (12) D14 (13) D15 (14)
19	D8 (Ø8) D9 (Ø9) D1Ø (1Ø) D11 (11)	STROBE CONTROL	D8 (Ø8) D9 (Ø9) D1Ø (1Ø) D11 (11)
18	D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)	READ TIMING	D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)
17	DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)	WRITE TIMING	DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)
16	CORE STACK A	DRIVE CONTROL	CORE STACK B
15	J4-28: MAR 12 @ GND. RØ(19) = Ø		J4-28: MAR 12 @ +5. RØ(19) = 1
14		YS ADDRESS REGISTER BITS 7, 8, 9	
13		YD AR BITS 1Ø, 11, 12	
12		XS AR BITS 13, 14, 15	
11	XS6-TP8 B12 3 / XS7-TP9 B12 7	XD AR BITS 16, 17, 18	XS6-TP8 B12 3 / XS7-TP9 B12 7
10	XS4-TP6 B12 1 / XS5-TP7 B12 5	PARITY TEST CAPAR LATCH	XS4-TP6 B12 1 / XS5-TP7 B12 5
9	XS2-TP4 B12 2 / XS3-TP5 B12 6	PARITY GENERATOR DATA BITS	XS2-TP4 B12 2 / XS3-TP5 B12 6
8	XSØ-TP2 B12 Ø / XS1-TP3 B12 4		XSØ-TP2 B12 Ø / XS1-TP3 B12 4
7	YS6-TP8 B14 3 / YS7-TP9 B14 7	HEATSINK FOR V_{TH} PROTECTION ZENER.	YS6-TP8 B14 3 / YS7-TP9 B14 7
6	YS4-TP6 B14 1 / YS5-TP7 B14 5		YS4-TP6 B14 1 / YS5-TP7 B14 5
5	YS2-TP4 B14 2 / YS3-TP5 B14 6		YS2-TP4 B14 2 / YS3-TP5 B14 6
4	YSØ-TP2 B14 Ø / YS1-TP3 B14 4		YSØ-TP2 B14 Ø / YS1-TP3 B14 4
3	XDØ-XD7 (TP B11) Ø,4,2,6,1,5,3,7 / YDØ-YD7 (TP B13) Ø,4,2,6,1,5,3,7		XDØ-XD7 (TP B11) Ø,4,2,6,1,5,3,7 / YDØ-YD7 (TP B13) Ø,4,2,6,1,5,3,7
2	X CURRENT SOURCE	CURRENT CONTROL MASTER POT. A1 A2 C1 C2	X CURRENT SOURCE
1	Y CURRENT SOURCE		Y CURRENT SOURCE

DATA LOWER J4-46: RDUL @ +5. RØ(23)=Ø

DATA UPPER J4-46: RDUL @ GND. RØ(23)=1

NOTE: (nn) IN DATA BIT DESIGNATION INDICATES A PROCESSOR M-BUS BIT POSITION. PØ & P1 ARE DATA PARITY BITS. THE CORE BOX EXPECTS EVEN DATA PARITY AND ODD ADDRESS PARITY.

							B5			B4			B3			B2			B1			B		
RØ	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15	16	17	18	19	2Ø	21	22	23
FM							A1	A2	A3	A4	A5	A6	A7	A8	A9	A1Ø	A11	A12	A13	A14	A15	A16	A17	A18
MAR						(LSB)		Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12				
								YS			YD			XS			XD							

STACK SELECT — MODULE SELECT — QUADRANT SELECT — RDUL

J: ØØ
K: Ø1
L: 1Ø
M: 11

NOTE: THE CORE BOX NEVER SEES RØ(ØØ) THRU RØ(Ø6), RØ(2Ø) THRU RØ(22).

NUMBERS ABOVE ARE OCTAL REPRESENTATIONS OF RESPECTIVE RØ BITS. EG. SLOT C11, XS6, NUMBER 3: RØ(13) = Ø, RØ(14) = RØ(15) = 1

.Ø RELEASED

REVISIONS

The Aloha System BCC-500

AMPEX CORE
FAST MEMORY - FULL

Slot	C	B	A
31		LINE TERMINATOR (B3Ø)	
3Ø	D5Ø (23), D51 (P1)	DATA IN Ø-13 (B29) (12 = PØ)	D5Ø (23), D51 (P1)
29	D46 (19), D47 (2Ø), D48 (21), D49 (22)	GROUND BUS	D46 (19), D47 (2Ø), D48 (21), D49 (22)
28	D42 (15), D43 (16), D44 (17), D45 (18)	DATA IN 14-25 (25 = P1)	D42 (15), D43 (16), D44 (17), D45 (18)
27	D38 (PØ), D39 (12), D4Ø (13), D41 (14)	DATA OUT LINE DRIVER Ø-25	D38 (PØ), D39 (12), D4Ø (13), D41 (14)
26	D34 (Ø8), D35 (Ø9), D36 (1Ø), D37 (11)	POSITIVE LOGIC B DO 2Ø-25 (MIX UPPER/LOWER)	D34 (Ø8), D35 (Ø9), D36 (1Ø), D37 (11)
25	D3Ø (Ø4), D31 (Ø5), D32 (Ø6), D33 (Ø7)	PLB DO Ø-19 (MIX UPPER/LOWER)	D3Ø (Ø4), D31 (Ø5), D32 (Ø6), D33 (Ø7)
24	D26 (ØØ), D27 (Ø1), D28 (Ø2), D29 (Ø3)	PL DO 18-25 & 44-51 (MIX STACKS)	D26 (ØØ), D27 (Ø1), D28 (Ø2), D29 (Ø3)
23	D24 (23), D25 (P1)	PL DO 9-17 & 35-43 (MIX STACKS)	D24 (23), D25 (P1)
22	D2Ø (19), D21 (2Ø), D22 (21), D23 (22)	PL DO Ø-8 & 26-34 (MIX STACKS)	D2Ø (19), D21 (2Ø), D22 (21), D23 (22)
21	D16 (15), D17 (16), D18 (17), D19 (18)	PL	D16 (15), D17 (16), D18 (17), D19 (18)
2Ø	D12 (PØ), D13 (12), D14 (13), D15 (14)	PL MAR 12 LATCH	D12 (PØ), D13 (12), D14 (13), D15 (14)
19	D8 (Ø8), D9 (Ø9), D1Ø (1Ø), D11 (11)	STROBE CONTROL	D8 (Ø8), D9 (Ø9), D1Ø (1Ø), D11 (11)
18	D4 (Ø4), D5 (Ø5), D6 (Ø6), D7 (Ø7)	READ TIMING	D4 (Ø4), D5 (Ø5), D6 (Ø6), D7 (Ø7)
17	DØ (ØØ), D1 (Ø1), D2 (Ø2), D3 (Ø3)	WRITE TIMING	DØ (ØØ), D1 (Ø1), D2 (Ø2), D3 (Ø3)
16	CORE STACK B	DRIVE CONTROL	CORE STACK A
15	J4-28: MAR 12 @ +5		J4-28: MAR 12 @ GND
14	RØ(19) = 1	YS ADDRESS REGISTER BITS 7, 8, 9	RØ(19) = Ø
13		YD AR BITS 1Ø, 11, 12	
12		XS AR BITS 13, 14, 15	
11	XS6-TP8 B12 3; XS7-TP9 B12 7	XD AR BITS 16, 17, 18	XS6-TP8 B12 3; XS7-TP9 B12 7
1Ø	XS4-TP6 B12 1; XS5-TP7 B12 5	PARITY TEST CAPAR LATCH	XS4-TP6 B12 1; XS5-TP7 B12 5
9	XS2-TP4 B12 2; XS3-TP5 B12 6	PARITY GENERATOR DATA BITS	XS2-TP4 B12 2; XS3-TP5 B12 6
8	XSØ-TP2 B12 Ø; XS1-TP3 B12 4		XSØ-TP2 B12 Ø; XS1-TP3 B12 4
7	YS6-TP8 B14 3; YS7-TP9 B14 7	HEATSINK FOR V_{TH} PROTECTION ZENER	YS6-TP8 B14 3; YS7-TP9 B14 7
6	YS4-TP6 B14 1; YS5-TP7 B14 5		YS4-TP6 B14 1; YS5-TP7 B14 5
5	YS2-TP4 B14 2; YS3-TP5 B14 6		YS2-TP4 B14 2; YS3-TP5 B14 6
4	YSØ-TP2 B14 Ø; YS1-TP3 B14 4		YSØ-TP2 B14 Ø; YS1-TP3 B14 4
3	XDØ-XD7 (TP B11) Ø,4,2,6,1,5,3,7; YDØ-YD7 (TP B13) Ø,4,2,6,1,5,3,7		XDØ-XD7 (TP B11) Ø,4,2,6,1,5,3,7; YDØ-YD7 (TP B13) Ø,4,2,6,1,5,3,7
2	X CURRENT SOURCE		X CURRENT SOURCE
1	Y CURRENT SOURCE	CURRENT CONTROL MASTER POT. A1 A2 C1 C2	Y CURRENT SOURCE

DATA LOWER J4-46: RDUL @ +5. RØ(23) = Ø (slots 17–3Ø, column C)

DATA UPPER J4-46: RDUL @ GND. RØ(23) = 1 (slots 17–23, column C)

NUMBERS ABOVE ARE OCTAL REPRESENTATIONS OF RESPECTIVE RØ BITS. EG. SLOT C11, XS6, NUMBER 3: RØ(13) = Ø, RØ(14) = RØ(15) = 1.

NOTE: (nn) IN DATA BIT DESIGNATION INDICATES A PROCESSOR M-BUS BIT POSITION. PØ & P1 ARE DATA PARITY BITS. THE CORE BOX EXPECTS EVEN DATA PARITY AND ODD ADDRESS PARITY.

							B5			B4			B3			B2			B1			B		
RØ	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15	16	17	18	19	2Ø	21	22	23
FM							A1	A2	A3	A4	A5	A6	A7	A8	A9	A1Ø	A11	A12	A13	A14	A15	A16	A17	A18
MAR							(LSB)	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12				
								YS			YD			XS			XD							

J: ØØ
K: Ø1
L: 1Ø
M: 11

STACK SELECT
MODULE SELECT
QUADRANT SELECT
RDUL

NOTE: THE CORE BOX NEVER SEES RØ(ØØ) THRU RØ(Ø6), RØ(2Ø) THRU RØ(22).

RELEASED			
REVISIONS			
The Alpha System BCC-500	AMPEX CORE	FAST MEMORY - FULL	
4719	2	4	LØ11Ø4.Ø

B	A
LINE TERMINATOR (B30)	D50 (23) D51 (P1)
DATA IN Ø-13 (B29) (12 = P0)	
GROUND BUS	D46 (19) D47 (20) D48 (21) D49 (22)
DATA IN 14-25 (25 = P1)	D42 (15) D43 (16) D44 (17) D45 (18)
DATA OUT LINE DRIVER Ø-25	D38 (1-Ø) D39 (12) D40 (13) D41 (14)
POSITIVE LOGIC B DO 20-25 (MIX UPPER/LOWER)	D34 (Ø8) D35 (Ø9) D36 (1Ø) D37 (11)
PLB DO Ø-17 (MIX UPPER/LOWER)	D3Ø (14) D31 (15) D32 (16) D33 (17)
PL DO 18-25 & 44-51 (MIX STACKS)	D26 (Ø2Ø) D27 (Ø21) D28 (Ø22) D29 (Ø23)
PL DO 9-17 & 35-43 (MIX STACKS)	D24 (23) D25 (P1)
PL DO Ø-8 & 26-34 (MIX STACKS)	D2Ø (19) D21 (2Ø) D22 (21) D23 (22)
TL	D14 (15) D17 (16) D18 (17) D19 (18)
TL	D12 (P0) D13 (12) D14 (13) D15 (14)
MAR 12 LATCH STROBE CONTROL	D8 (Ø8) D9 (Ø9) D10 (1Ø) D11 (11)
READ TIMING	D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)
WRITE TIMING	DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)
DRIVE CONTROL	CORE STACK A
YS ADDRESS REGISTER BITS 20, 8, 9	J4-28: MAR 12 @ GND. RØ(19) = Ø
YD AR BITS 10, 11, 12	
XS AR BITS 13, 14, 15	
XD AR BITS 16, 17, 18	XS6-TP5 B12 XS7-TP9 B12 3 7
PARITY TEST	XS4-TP6 B12 XS5-TP7 B12 1 5
CAFAR LATCH	XS2-TP4 B12 XS3-TP5 B12 2 6
PARITY GENERATOR DATA BITS	XSØ-TP2 B12 XS1-TP3 B12 Ø 4
HEATSINK FOR V_{TH} PROTECTION ZENER	YS6-TP8 B14 YS7-TP9 B14 3+Ø 3+1
	YS4-TP6 B14 YS5-TP7 B14 1+Ø 1+1
	YS2-TP4 B14 YS3-TP5 B14 2+Ø 2+1
	YSØ-TP2 B14 YS1-TP3 B14 Ø+Ø Ø+1
	XDØ-XD7 (TP B11) Ø4,2,6,1,5,3,7 YDØ-YD7 (TP B13) Ø4,2,6,1,5,3,7
	X CURRENT SOURCE Y CURRENT SOURCE

C
D50 (23) D51 (P1)
D46 (19) D47 (20) D48 (21) D49 (22)
D42 (15) D43 (16) D44 (17) D45 (18)
D38 (1Ø) D39 (12) D40 (13) D41 (14)
D34 (Ø8) D35 (Ø9) D36 (1Ø) D37 (11)
D3Ø (Ø4) D31 (Ø5) D32 (Ø6) D33 (Ø7)
D26 (ØØ) D27 (Ø1) D28 (Ø2) D29 (Ø3)
D24 (23) D25 (P1)
D20 (19) D21 (2Ø) D22 (21) D23 (22)
D16 (15) D17 (16) D18 (17) D19 (18)
D12 (P0) D13 (12) D14 (13) D15 (14)
D8 (Ø8) D9 (Ø9) D10 (1Ø) D11 (11)
D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)
DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)
CORE STACK B
J4-28: MAR 12 @ +5. RØ(19) = 1
XS6-TP8 B12 XS7-TP9 B12 3 7
XS4-TP6 B12 XS5-TP7 B12 1 5
XS2-TP4 B12 XS3-TP5 B12 2 6
XSØ-TP2 B12 XS1-TP3 B12 Ø 4
YS6-TP8 B14 YS7-TP9 B14 3+Ø 3+1
YS4-TP6 B14 YS5-TP7 B14 1+Ø 1+1
YS2-TP4 B14 YS3-TP5 B14 2+Ø 2+1
YSØ-TP2 B14 YS1-TP3 B14 Ø+Ø Ø+1
XDØ-XD7 (TP B11) Ø4,2,6,1,5,3,7 YDØ-YD7 (TP B13) Ø4,2,6,1,5,3,7
X CURRENT SOURCE Y CURRENT SOURCE

DATA LOWER
J4-46: RDUL @ +5. RØ(23) = Ø

DATA UPPER
J4-46: RDUL @ GND. RØ(23) = 1

NOTE: (nn) IN DATA BIT DESIGNATION INDICATES A PROCESSOR M-BUS BIT POSITION. PØ & P1 ARE DATA PARITY BITS. THE CORE BOX EXPECTS EVEN DATA PARITY AND ODD ADDRESS PARITY.

	B5			B4			B3			B2			B1			B		
RØ	Ø	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
FM	A1								A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
MAR	(MARØ = LSB)								1	2	3	4	5	6	7	8	9	10
									YS		YD			XS			XD	

	B																		
RØ	18	19	20	21	22	23													
FM	A13	A14	A2	A15	A17	A16													
MAR	11	12	Ø																
			YS		J(L)=Ø														

STACK SELECT
MODULE SELECT
QUADRANT SELECT
RDUL

NOTE: THE CORE BOX NEVER SEES RØ(Ø8) THRU RØ(17), RØ(21) & RØ(22).

SWITCHES ON MASTER PANEL FOR ENTRY OF J OR L & K OR M.

NUMBERS ABOVE ARE OCTAL REPRESENTATIONS OF RESPECTIVE MAR BITS. FOR SLOT C11, XS6 NUMBER 3: RØ(13) = Ø, RØ(14) = RØ(15) = 1
3+Ø : 3 IN BITS 8&9, Ø IN BIT 2Ø

NO	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

REVISIONS

The Aloha System BCC-500

DESIGNED
DES. CHK'D
DRAWN Tim
DWG CHK'D

TITLE: AMPEX CORE
FAST MEMORY-HALF
PROJECT

4719

SHEET 3 OF 4

NO. LØ1104.Ø

C	B	A	
			32
	LINE TERMINATOR (B3Ø)		31
D5Ø (23) D51 (P1)	DATA IN Ø-13 (B29) (12 = PØ)	D5Ø (23) D51 (P1)	30
D46 (19) D47 (2Ø) D48 (21) D49 (22)	GROUND BUS	D46 (19) D47 (2Ø) D48 (21) D49 (22)	29
D42 (15) D43 (16) D44 (17) D45 (18)	DATA IN 14-25 (25 = P1)	D42 (15) D43 (16) D44 (17) D45 (18)	28
D38 (PØ) D39 (12) D4Ø (13) D41 (14)	DATA OUT LINE DRIVER Ø-25	D38 (PØ) D39 (12) D4Ø (13) D41 (14)	27
D34 (Ø9) D35 (Ø9) D36 (1Ø) D37 (11)	POSITIVE LOGIC B DO 2Ø-25 (MIX UPPER/LOWER)	D34 (Ø8) D35 (Ø9) D36 (1Ø) D37 (11)	26
D3Ø (Ø4) D31 (Ø5) D32 (Ø6) D33 (Ø7)	FLB DC Ø-19 (MIX UPPER/LOWER)	D3Ø (Ø4) D31 (Ø5) D32 (Ø6) D33 (Ø7)	25
D26 (ØØ) D27 (Ø1) D28 (Ø2) D29 (Ø3)	PL DO 18-25 & 44-51 (MIX STACKS)	D26 (ØØ) D27 (Ø1) D28 (Ø2) D29 (Ø3)	24
D24 (23) D25 (P1)	PL DO 9-17 & 35-43 (MIX STACKS)	D24 (23) D25 (P1)	23
D2Ø (19) D21 (2Ø) D22 (21) D23 (22)	PL DO Ø-8 & 26-34 (MIX STACKS)	D2Ø (19) D21 (2Ø) D22 (21) D23 (22)	22
D16 (15) D17 (16) D18 (17) D19 (18)	PL	D16 (15) D17 (16) D18 (17) D19 (18)	21
D12 (PØ) D13 (12) D14 (13) D15 (14)	PL MAR 12 LATCH	D12 (PØ) D13 (12) D14 (13) D15 (14)	20
D8 (Ø8) D9 (Ø9) D1Ø (1Ø) D11 (11)	STROBE CONTROL	D8 (Ø8) D9 (Ø9) D1Ø (1Ø) D11 (11)	19
D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)	READ TIMING	D4 (Ø4) D5 (Ø5) D6 (Ø6) D7 (Ø7)	18
DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)	WRITE TIMING	DØ (ØØ) D1 (Ø1) D2 (Ø2) D3 (Ø3)	17
	DRIVE CONTROL		16
CORE STACK B		CORE STACK A	15
J4-28: MAR 12 @ +5. RØ(22) = Ø	YS ADDRESS REGISTER BITS 1Ø,11,12	J4-28: MAR 12 @ GND. RØ(22) = 1	14
	YD AR BITS 13,14,15		13
	XS AR BITS 16,17,18		12
XS6-TP8B12 4 / XS7-TP9B12 Ø	XD AR BITS 19,2Ø,21	XS6-TP8B12 4 / XS7-TP9B12 Ø	11
XS4-TP6B12 6 / XS5-TP7B12 2	PARITY TEST / CAPAR LATCH	XS4-TP6B12 6 / XS5-TP7B12 2	10
XS2-TP4B12 5 / XS3-TP5B12 1	PARITY GENERATOR DATA BITS	XS2-TP4B12 5 / XS3-TP5B12 1	9
XSØ-TP2B12 7 / XS1-TP3B12 3		XSØ-TP2B12 7 / XS1-TP3B12 3	8
YS6-TP8B14 4 / YS7-TP9B14 Ø	HEATSINK FOR V_{TH} PROTECTION ZENER	YS6-TP8B14 4 / YS7-TP9B14 Ø	7
YS4-TP6B14 6 / YS5-TP7B14 2		YS4-TP6B14 6 / YS5-TP7B14 2	6
YS2-TP4B14 5 / YS3-TP5B14 1		YS2-TP4B14 5 / YS3-TP5B14 1	5
YSØ-TP2B14 7 / YS1-TP3B14 3		YSØ-TP2B14 7 / YS1-TP3B14 3	4
XDØ-XD7 (TP B11) 7,3,5,1,6,2,4,Ø X CURRENT SOURCE / YDØ-YD7 (TP B13) 7,3,5,1,6,2,4,Ø		XDØ-XD7 (TP B11) 7,3,5,1,6,2,4,Ø Y CURRENT SOURCE / YDØ-YD7 (TP B13) 7,3,5,1,6,2,4,Ø	3
Y CURRENT SOURCE	CURRENT CONTROL MASTER POT. A1 A2 C1 C2	Y CURRENT SOURCE	2
			1

DATA LOWER J4-46: RDUL @ +5. RØ(23) = Ø

DATA UPPER J4-46: RDUL @ GND. RØ(23) = 1

								B5		B4			B3			B2			B1			B		
RI	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	13	14	15	16	17	18	19	2Ø	21	22	23
MAR										(LSB)	Ø	1	2	3	4	5	6	7	8	9	1Ø	11	12	
											YS			YD			XS			XD				
																	STACK SELECT						RDUL	

NOTE: (nn) IN DATA BIT DESIGNATION INDICATES A PROCESSOR M-BUS BIT POSITION. PØ & P1 ARE DATA PARITY BITS. THE CORE BOX EXPECTS EVEN DATA PARITY AND ODD ADDRESS PARITY.

NOTE: THE CORE BOX NEVER SEES RØ(ØØ) THRU RØ(Ø9).

NUMBERS ABOVE ARE OCTAL REPRESENTATIONS OF RESPECTIVE RØ BITS. J4 SLOT C11 XS6 JUMPER 4: RØ(16) = 1 RØ(17) = RØ(18) = Ø

Ø	RELEASED		
NO.	DESCRIPTION	DATE	DRAWN / APPROVED

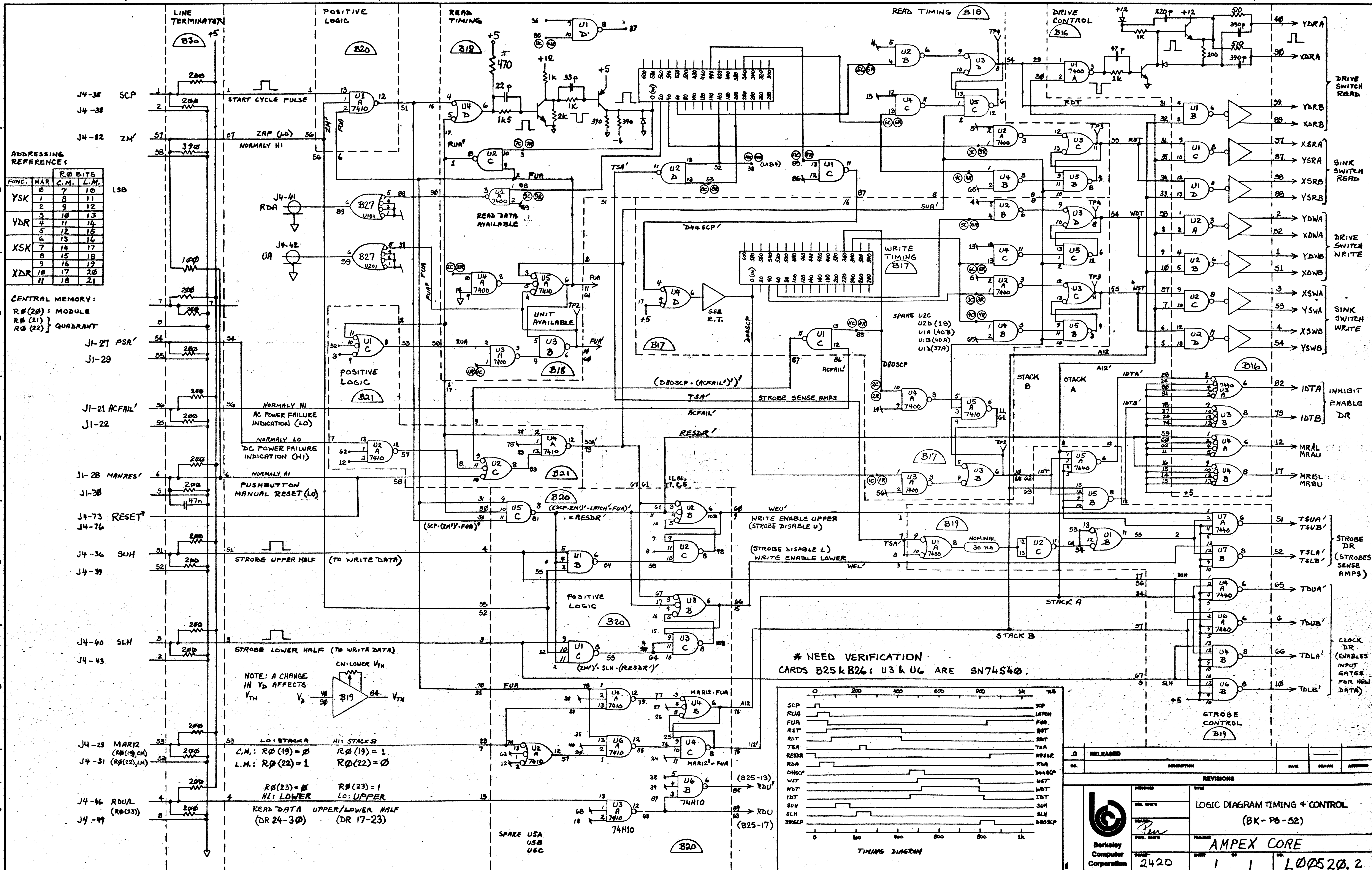
REVISIONS

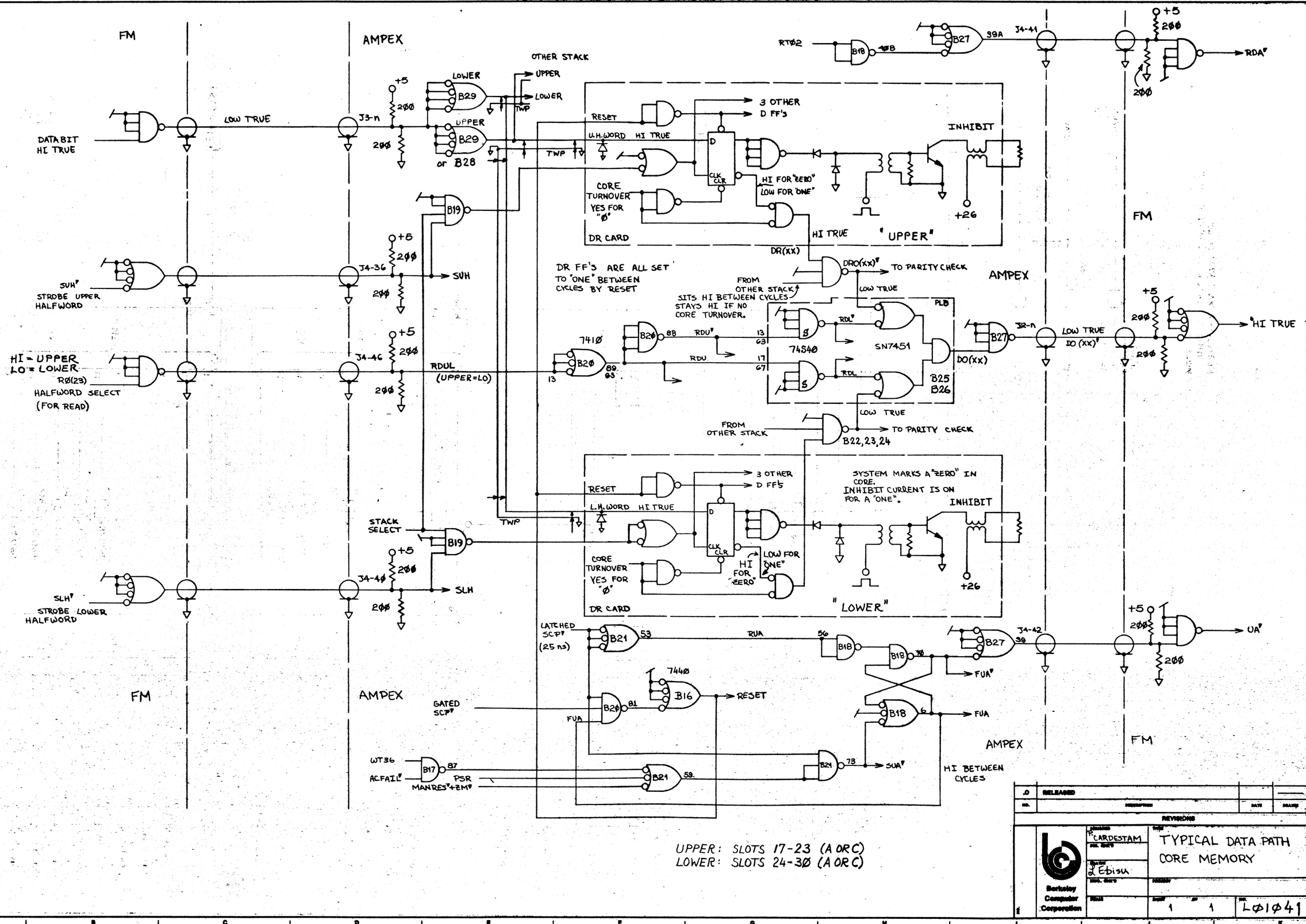
The Alpha Systems BCC-500

TITLE: AMPEX CORE LOCAL

DRAWN: Tuc

4719 SHEET 4 OF 4 NO. LØ11Ø4.Ø


LINE TERMINATOR
POSITIVE LOGIC
READ TIMING
READ TIMING (B18)
DRIVE CONTROL (B16)
START CYCLE PULSE
ZAP (LO)
NORMALY HI
ADDRESSING REFERENCE:
CENTRAL MEMORY:
RØ(20): MODULE
RØ(21) RØ(22) QUADRANT
READ DATA AVAILABLE
UNIT AVAILABLE
WRITE TIMING (B17)
DRIVE SWITCH READ
SINK SWITCH READ
DRIVE SWITCH WRITE
SINK SWITCH WRITE
INHIBIT ENABLE DR
STROBE DR (STROBES SENSE AMPS)
CLOCK DR (ENABLES INPUT GATES FOR NEW DATA)
STROBE CONTROL (B19)
NORMALY HI AC POWER FAILURE INDICATION (LO)
NORMALY LO DC POWER FAILURE INDICATION (HI)
NORMALY HI PUSHBUTTON MANUAL RESET (LO)
STROBE UPPER HALF (TO WRITE DATA)
STROBE LOWER HALF (TO WRITE DATA)
WRITE ENABLE UPPER (STROBE DISABLE U)
(STROBE DISABLE L) WRITE ENABLE LOWER
STROBE SENSE AMPS
NOTE: A CHANGE IN VD AFFECTS VTH
LO: STACK A HI: STACK B
C.M.: RØ(19) = Ø RØ(19) = 1
L.M.: RØ(22) = 1 RØ(22) = Ø
RØ(23) = Ø HI: LOWER RØ(23) = 1 LO: UPPER
READ DATA UPPER/LOWER HALF (DR 24-3Ø) (DR 17-23)
SPARE U5A U5B U6C
* NEED VERIFICATION
CARDS B25 & B26: U3 & U6 ARE SN74S40.
TIMING DIAGRAM
LOGIC DIAGRAM TIMING & CONTROL (BK-PB-52)
AMPEX CORE
Berkeley Computer Corporation
2420
L00520.2
REVISIONS
RELEASED



NO.	RELEASED	DATE	DRAWN	APPROVED
.0				

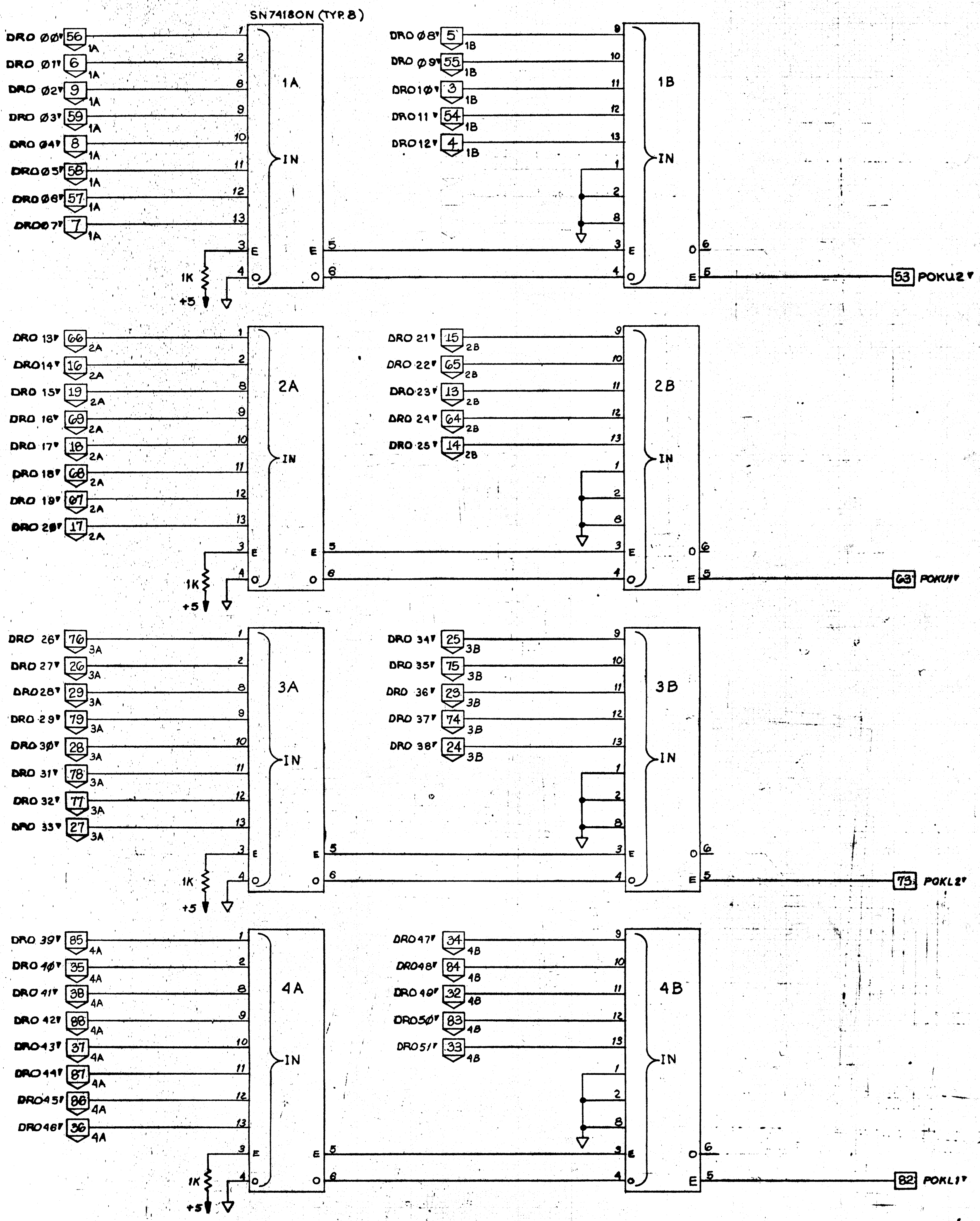
REVISIONS

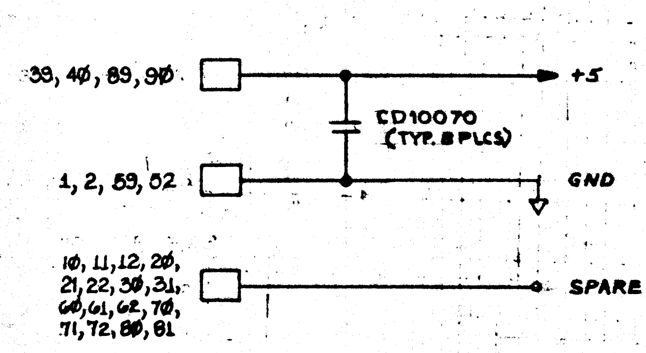
Berkeley Computer Corporation

DESIGNED P. LARDESTAM
DRAWN L. Ebisu

TYPICAL DATA PATH IN CORE MEMORY

SIZE 1 SHEET 1 DWG. NO. L-Ø1Ø41.2





NOTE
UNLESS OTHERWISE SPECIFIED ALL RESISTORS ARE 1/8W 10%

L00519

Berkeley Computer Corporation

DESIGNED J. PRICE
DRAWN G BONAWITZ 4-28-70
4/28/70

TITLE DATA PARITY GENERATOR

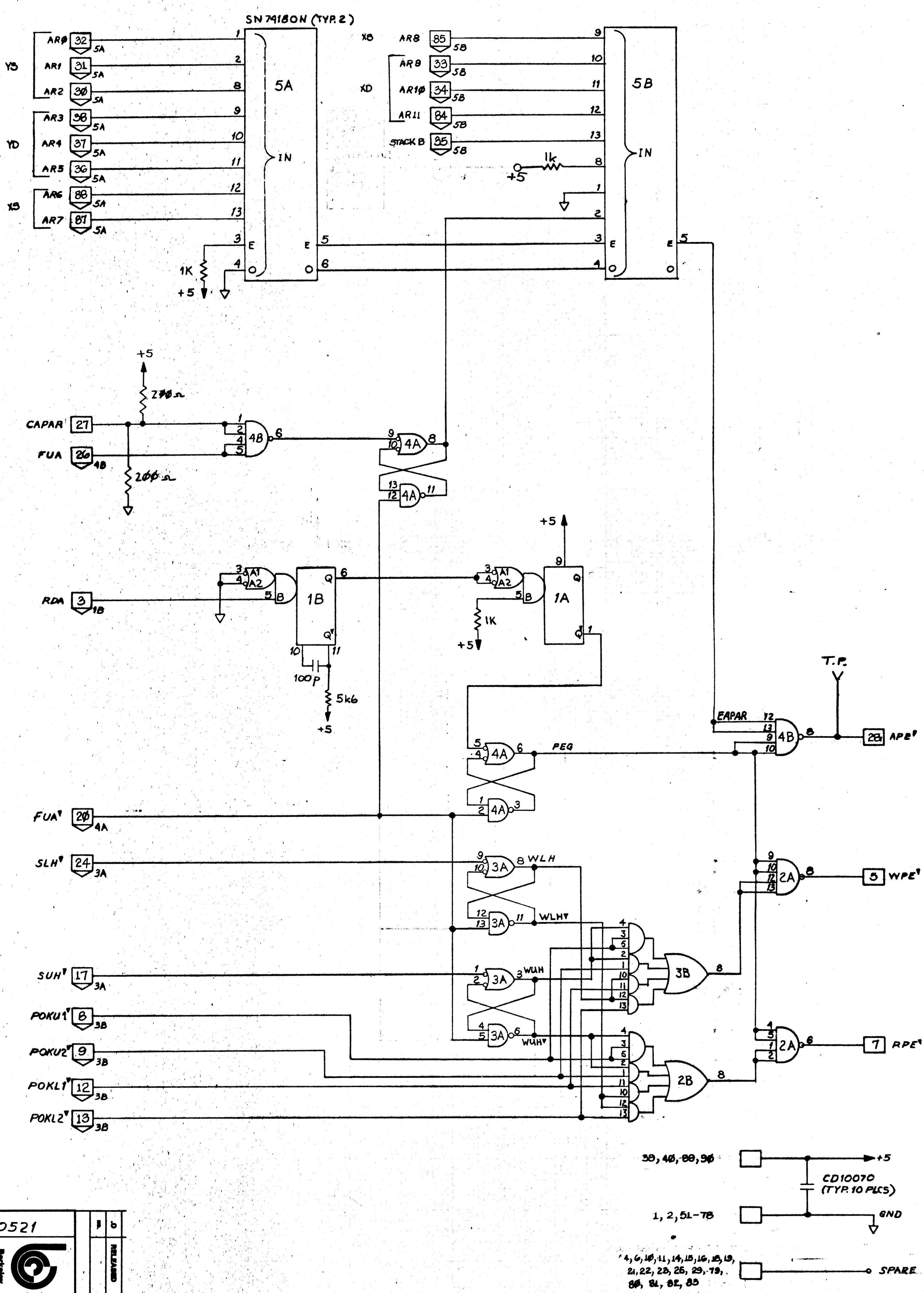
PROJECT FIRST USED ON CORE MEMORY

SHEET 1 OF 1

NO. L00519 .2

REVISIONS

B9



NOTE:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 10%

L00521

Berkeley Computer Corporation

DESIGNED J. PRICE
DRAWN 4/23/70 G. BONAWITZ
DWG. CHK'D 4/28/70

TITLE PARITY TESTER

PROJECT FIRST USED ON M1 CORE MEMORY

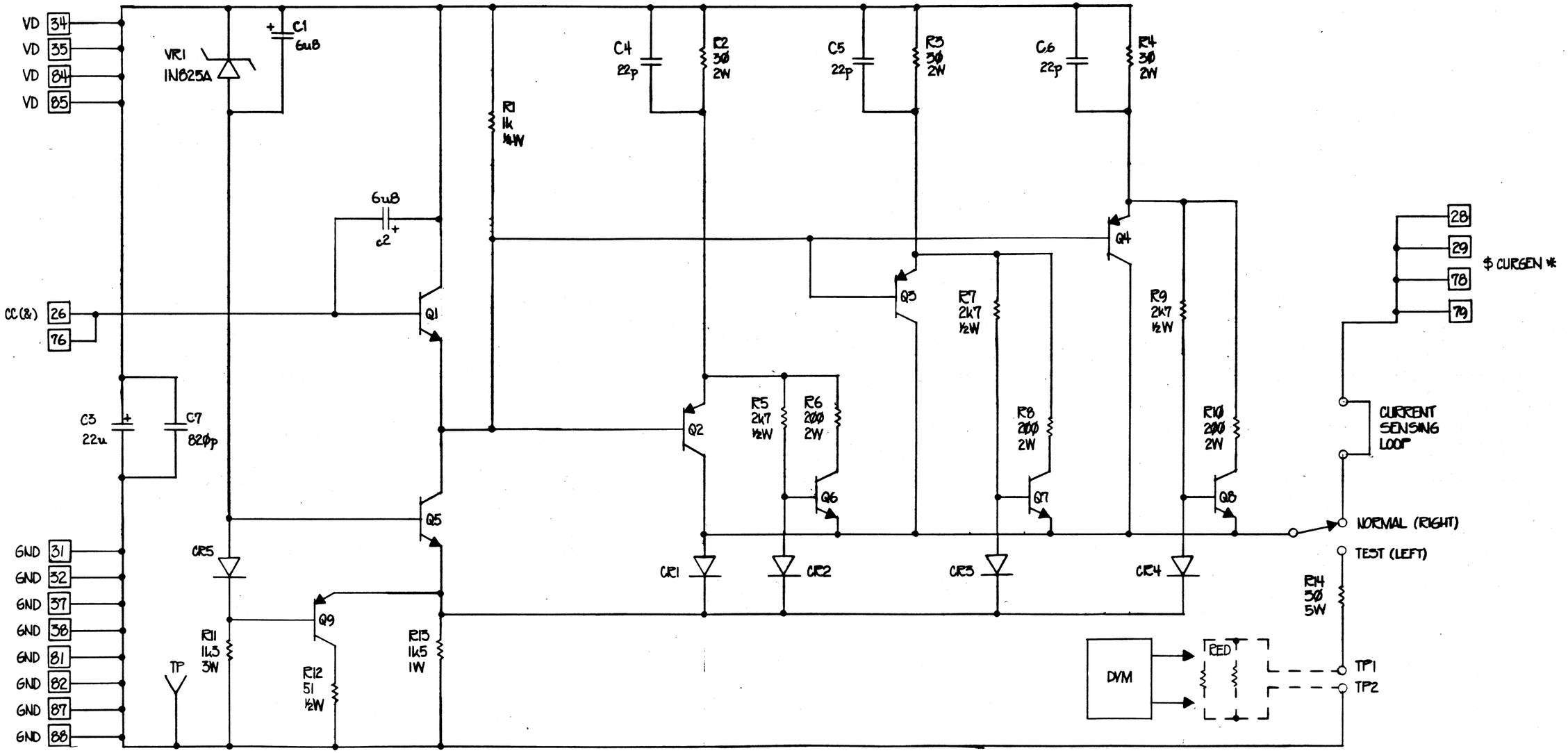
SHEET 1 OF 1

NO. L00521 . 2

REVISIONS

RELEASED

B10



SLOT	&	$	*
A1	A1	Y	A
A2	A2	X	A
C1	C1	Y	B
C2	C2	X	B

NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

REVISIONS

The Aloha System BCC-500

DESIGNED

ENGR. CHG'D

DRAWN: F. YOSHIOKA

ENGR. CHK'D: Ken

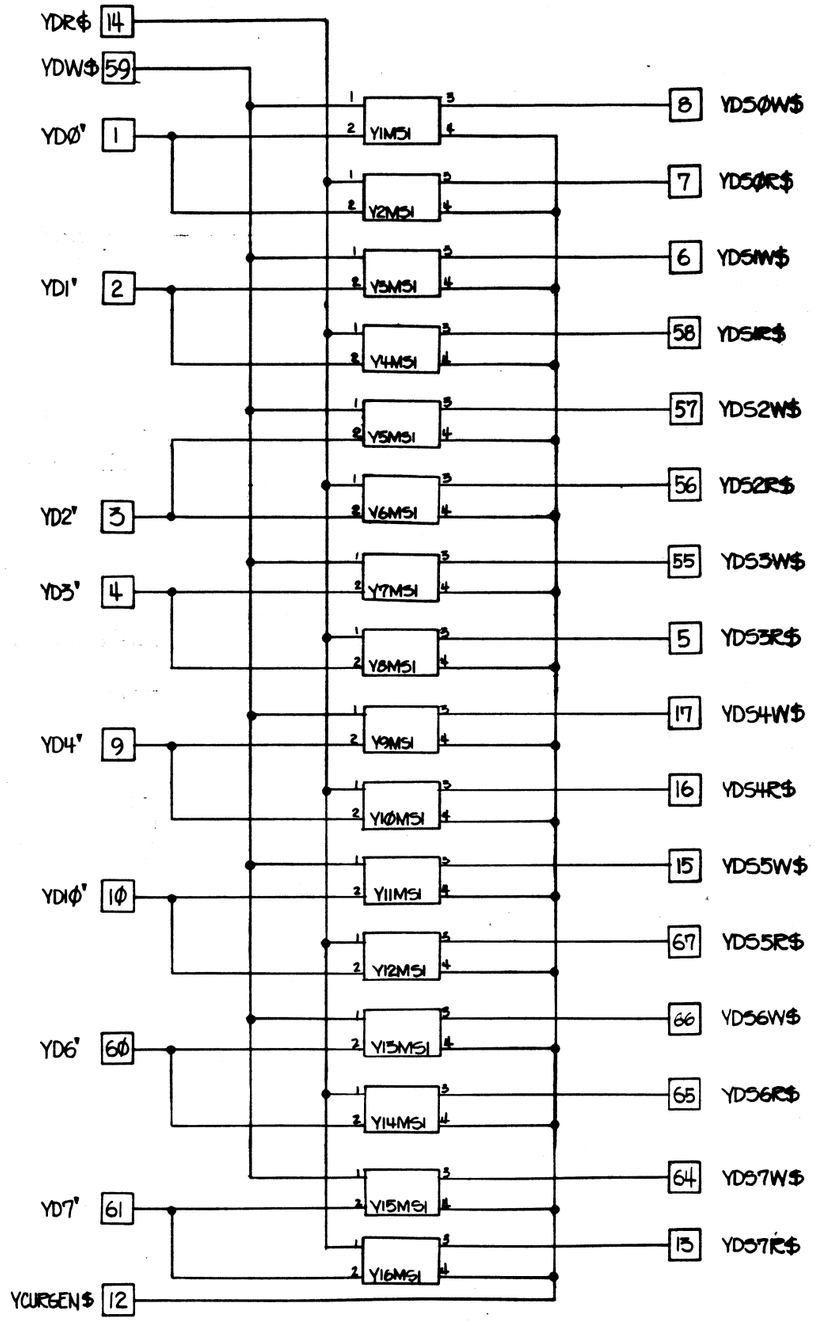
DATE: 3 DEC 1974

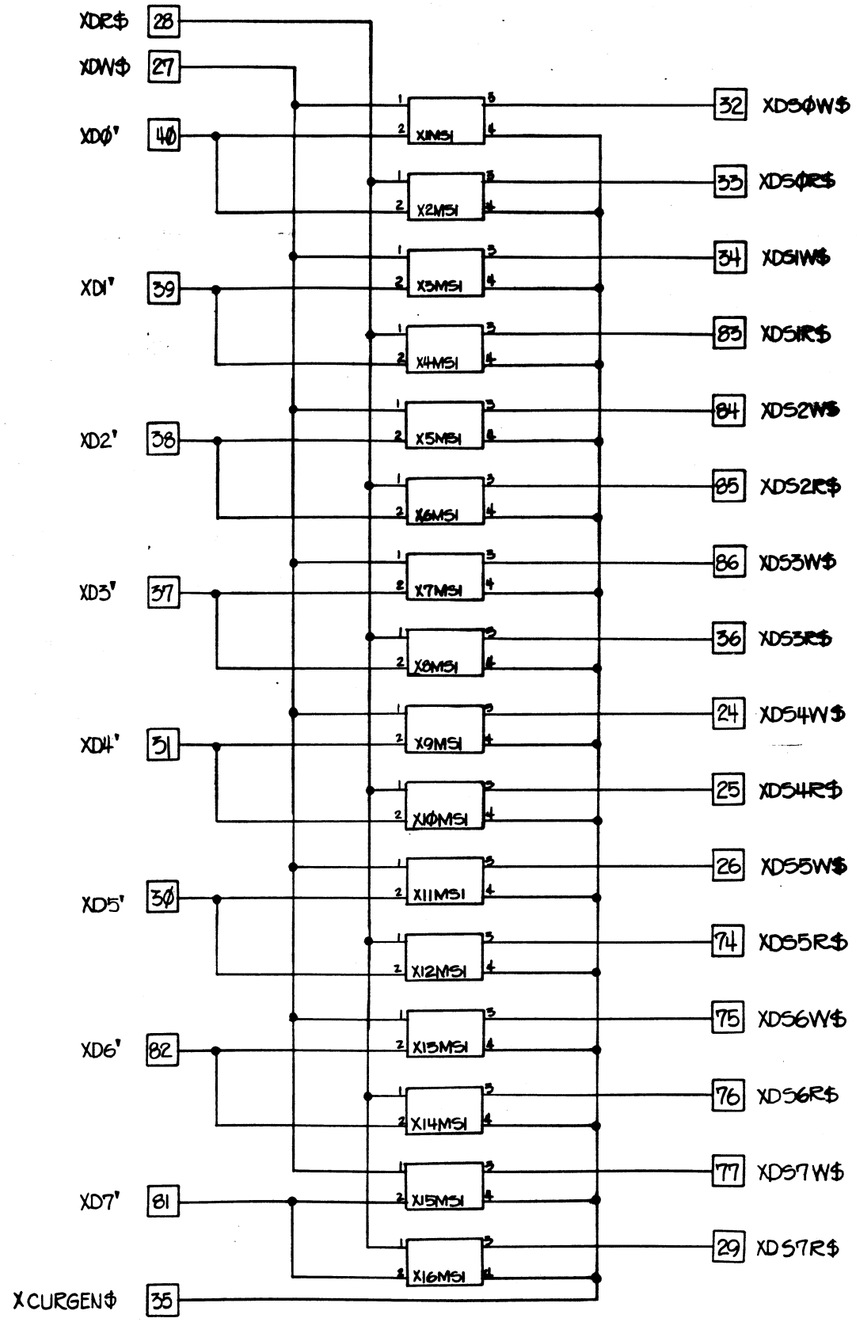
TITLE: CURRENT SOURCE

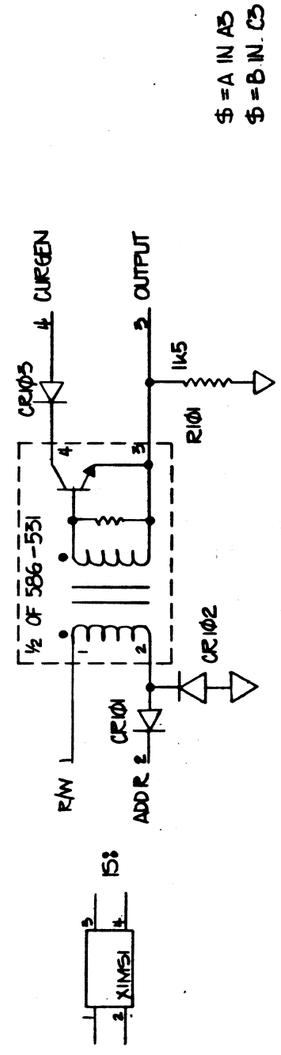
PROJECT: AMPEX A1, A2, C1, C2

SHEET | OF |

DR. LØ1ØØØ.Ø







.0	RELEASED			
NO.	DESCRIPTION	DATE	DRAWN	APPROVED

REVISIONS

The Aloha System BCC-500

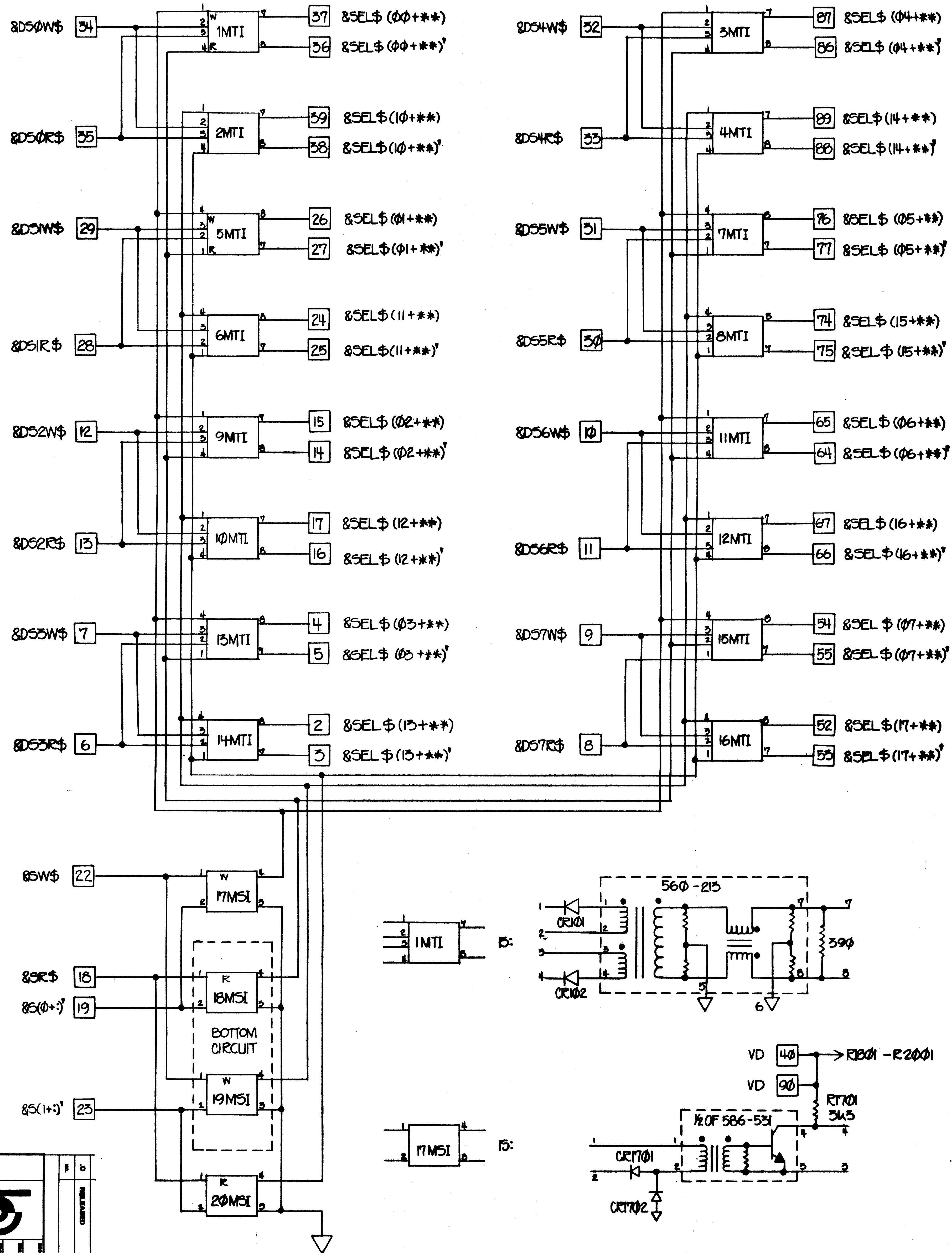
DESIGNED
DES. CHK'D
DRAWN F. YOSHIOKA
PROG. CHK'D Steve
APPROVED - 3 DEC 1974

TITLE: DRIVE SWITCH

PROJECT: AMPEX A3 OR C3

SHEET 1 OF 1

DWG. NO. LØ1Ø91.Ø



& = Y ON A4 - A7
C4 - C7
& = X ON A8 - A11
C8 - C11

$ = A ON A4 - A11
$ = B ON C4 - C11

** = 00 ON A4, A8, C4, C8
20 A5, A9, C5, C9
40 A6, A10, C6, C10
60 A7, A11, C7, C11

: = 0 ON A4, A8, C4, C8
2 A5, A9, C5, C9
4 A6, A10, C6, C10
6 A7, A11, C7, C11

1, 20, 21
51, 70, 71

The Aloha System BCC-500

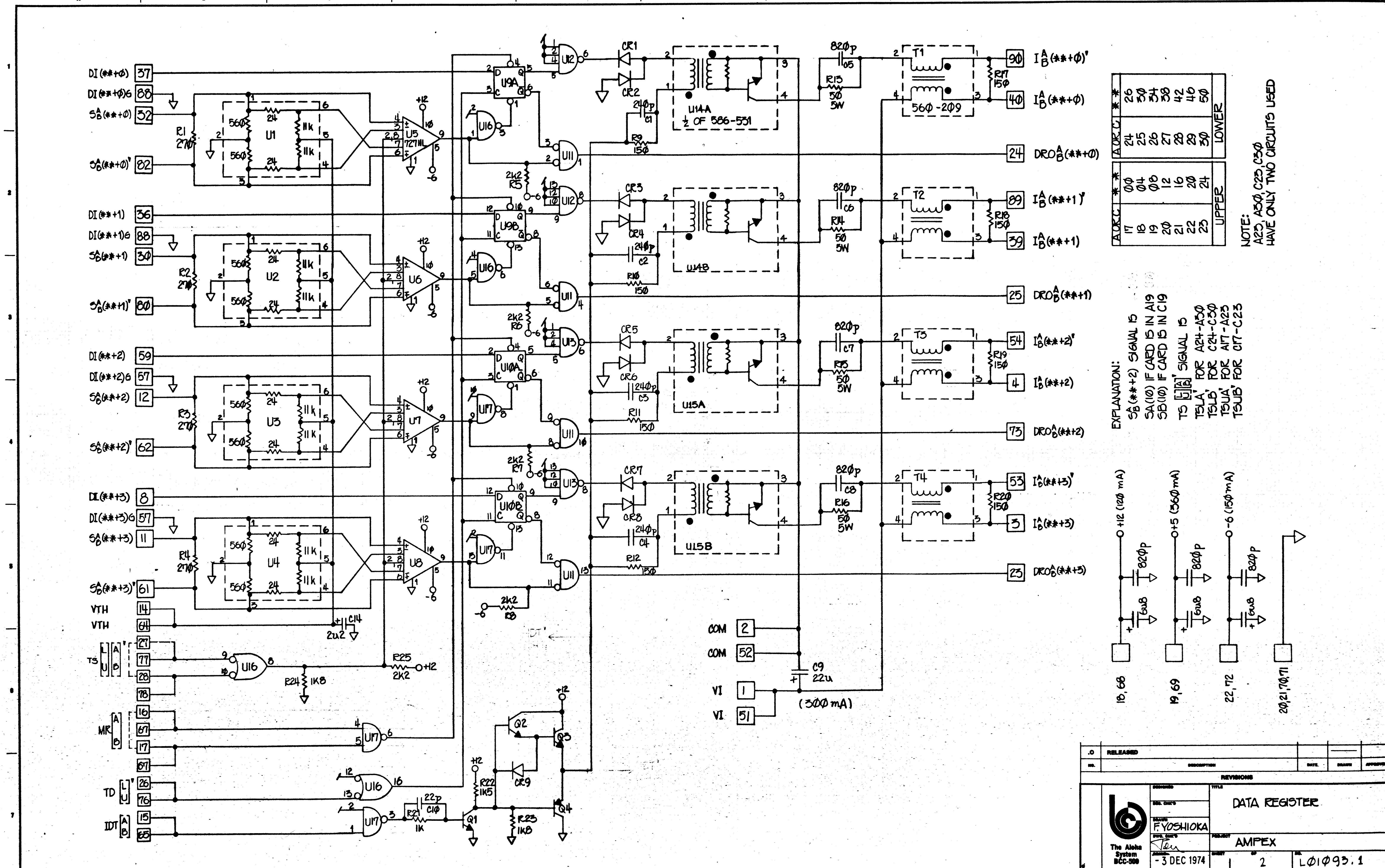
F. YOSHIOKA

- 3 DEC 1974

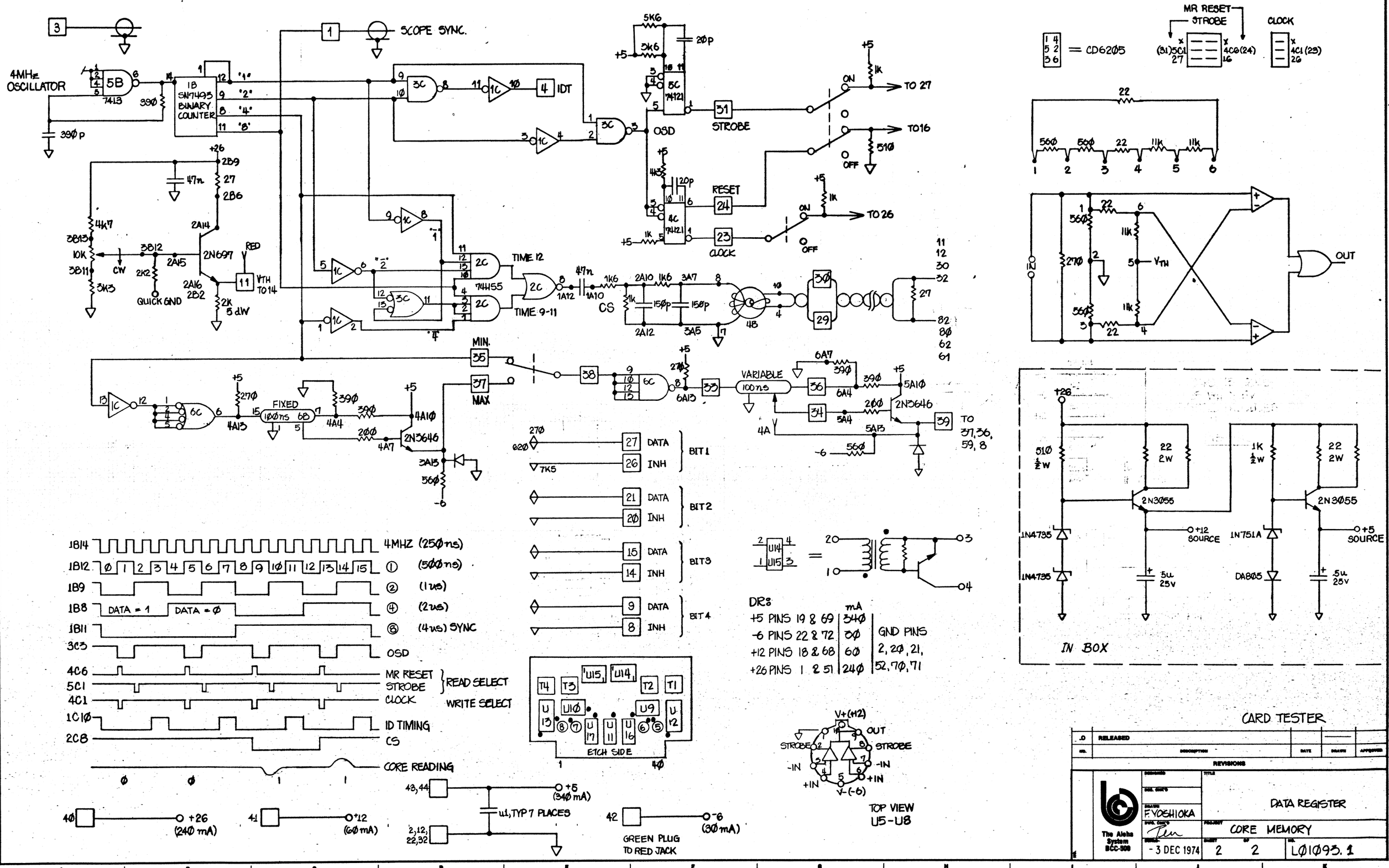
STACK DECODER

AMPEX A4-A11 C4-C11

L01092.0



DI(**+0) 37
DI(**+0)6 88
SA B(**+0) 32
SA B(**+0)' 82
DI(**+1) 36
DI(**+1)6 88
SA B(**+1) 30
SA B(**+1)' 80
DI(**+2) 59
DI(**+2)6 57
SA B(**+2) 12
SA B(**+2)' 62
DI(**+3) 8
DI(**+3)6 57
SA B(**+3) 11
SA B(**+3)' 61
VTH 14
VTH 64
TS
MR
TD
IDT
U1 U2 U3 U4 U5 U6 U7 U8
U9A U9B U10A U10B U11 U12 U13 U16 U17
U14A ½ OF 586-531
U14B U15A U15B
T1 T2 T3 T4
560-209
I A B(**+0)' 90
I A B(**+0) 40
DRO A B(**+0) 24
I A B(**+1)' 89
I A B(**+1) 39
DRO A B(**+1) 25
I A B(**+2)' 54
I A B(**+2) 4
DRO A B(**+2) 73
I A B(**+3)' 53
I A B(**+3) 3
DRO A B(**+3) 23
COM 2
COM 52
VI 1
VI 51
C9 22u
(300 mA)
+12 (120 mA) 18, 68
+5 (360 mA) 19, 69
-6 (150 mA) 22, 72
20, 21, 70, 71
A OR C | ** LOWER: 24 26, 25 30, 26 34, 27 38, 28 42, 29 46, 30 50
A OR C | ** UPPER: 17 00, 18 04, 19 08, 20 12, 21 16, 22 20, 23 24
NOTE:
A25, A50, C25, C50
HAVE ONLY TWO CIRCUITS USED
EXPLANATION:
SA B(**+2) SIGNAL 15
SA(10) IF CARD 15 IN A19
SB(10) IF CARD 15 IN C19
TS [L U][A B]' SIGNAL 15
TSLA' FOR A24-A50
TSLB' FOR C24-C50
TSUA' FOR A17-A23
TSUB' FOR C17-C23
RELEASED
REVISIONS
The Aloha System BCC-500
F.YOSHIOKA
3 DEC 1974
DATA REGISTER
AMPEX
1 2
L01093.1



CARD TESTER

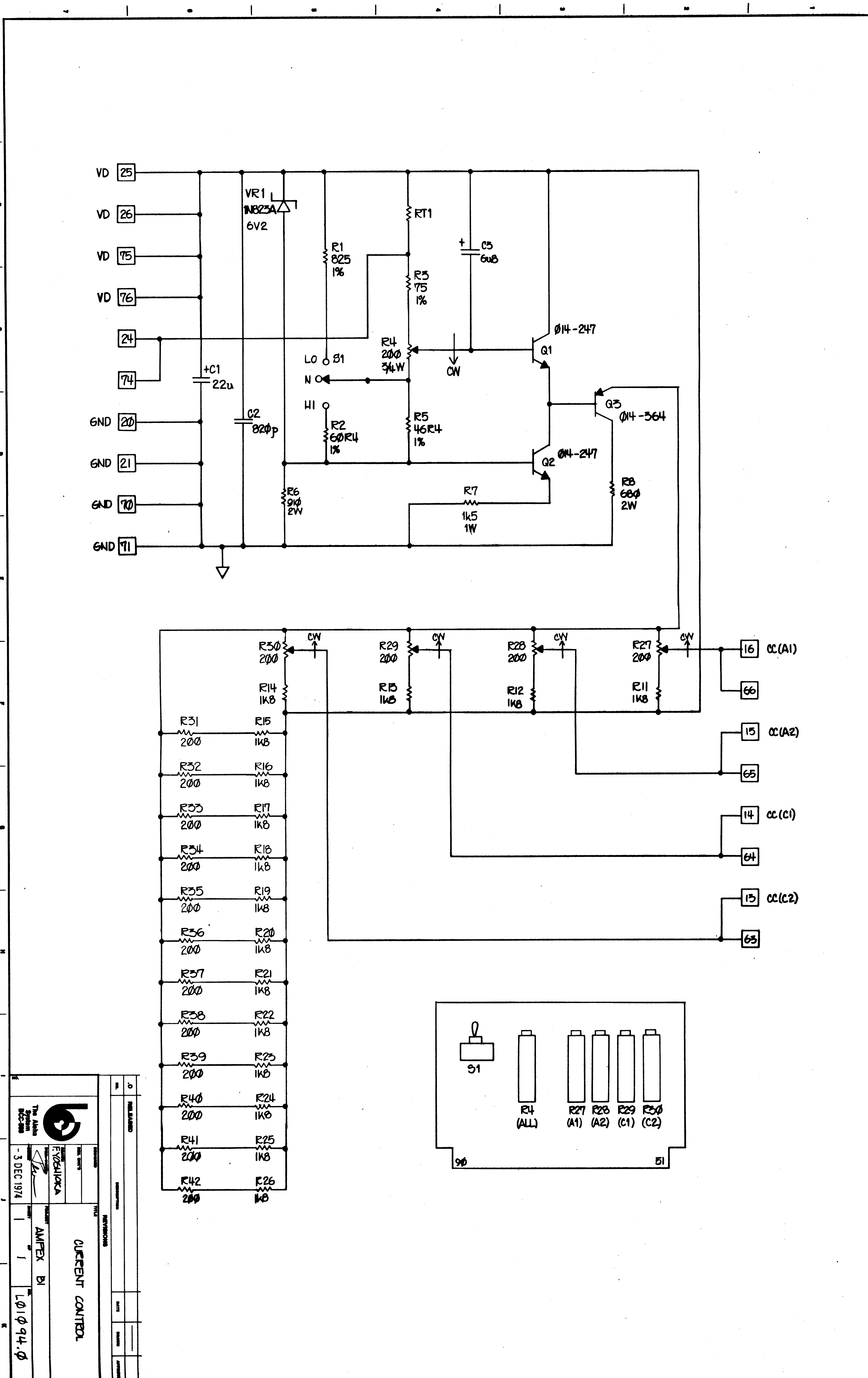
NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

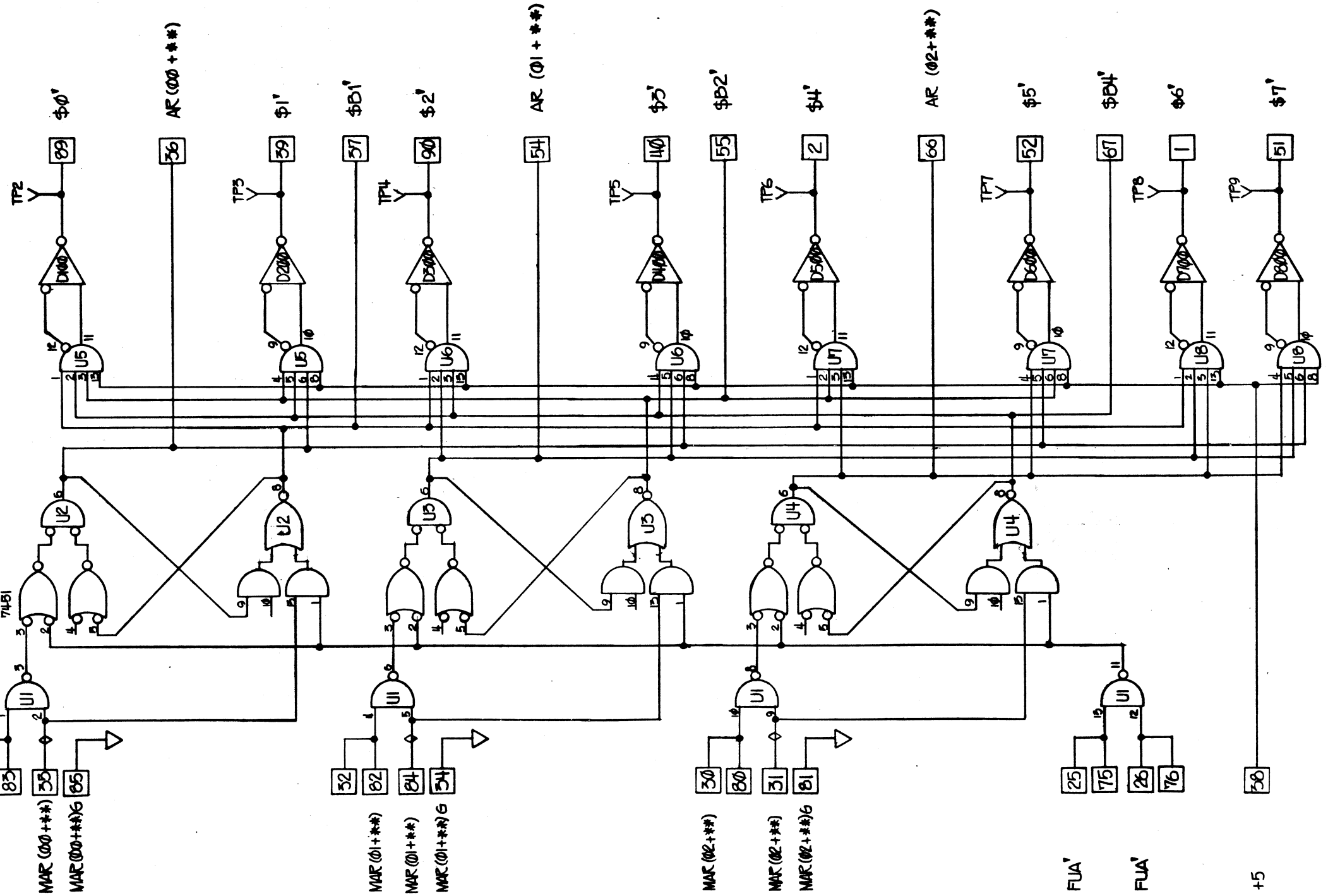
REVISIONS

The Aloha System BCC-500

DESIGNED
DES. CHK'D
DRAWN F. YOSHIOKA
PHYS. CHK'D
ENGR.
- 3 DEC 1974

TITLE
DATA REGISTER
PROJECT
CORE MEMORY
SHEET 2 OF 2
NO. LØ1Ø93.1


VD 25
VD 26
VD 75
VD 76
24
74
GND 20
GND 21
GND 70
GND 71
+C1 22u
C2 820p
VR1 1N823A 6V2
R6 910 2W
R1 825 1%
LO S1
N
HI
R2 60R4 1%
RT1
R3 75 1%
R4 200 3/4W
R5 46R4 1%
CW
+ C5 6u8
Q1 014-247
Q2 014-247
Q3 014-364
R7 1k5 1W
R8 680 2W
R30 200
R29 200
R28 200
R27 200
CW
R14 1K8
R13 1K8
R12 1K8
R11 1K8
16 CC(A1)
66
15 CC(A2)
65
14 CC(C1)
64
13 CC(C2)
63
R31 200
R15 1K8
R32 200
R16 1K8
R33 200
R17 1K8
R34 200
R18 1K8
R35 200
R19 1K8
R36 200
R20 1K8
R37 200
R21 1K8
R38 200
R22 1K8
R39 200
R23 1K8
R40 200
R24 1K8
R41 200
R25 1K8
R42 200
R26 1K8
S1
R4 (ALL)
R27 (A1)
R28 (A2)
R29 (C1)
R30 (C2)
90
51
The Alpha System BCC-998
F.YOSHIOKA
-3 DEC 1974
CURRENT CONTROL
AMPEX B1
1 of 1
L01094.0
REVISIONS
RELEASED



NO.	DESCRIPTION	DATE	DRAWN	APPROVED
Ø	RELEASED			

REVISIONS

The Aloha System BCC-500

DESIGNED
ENGR. CHK'D
DRAWN F. YOSHIOKA
PROG. CHK'D
APPROVED

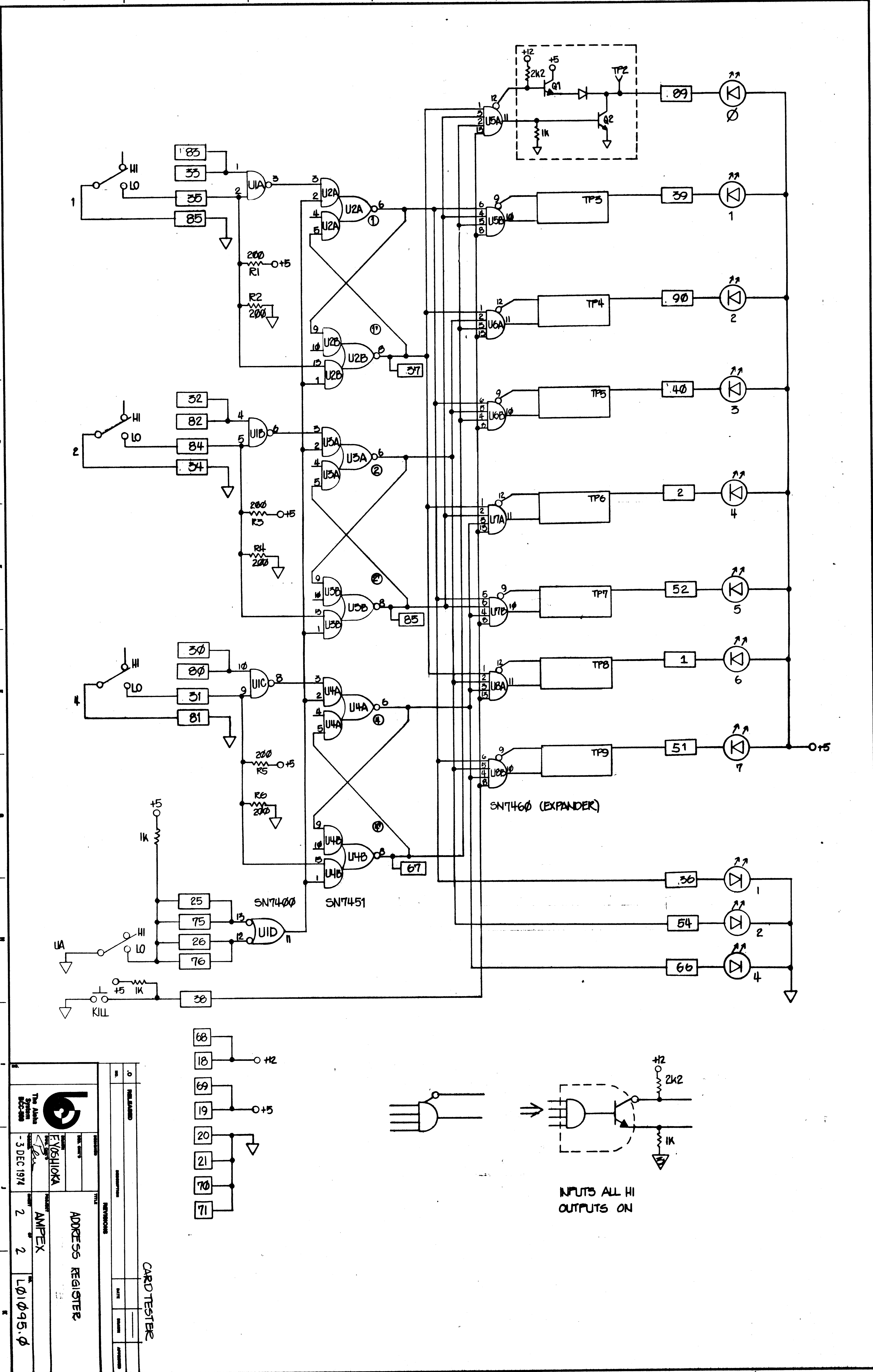
- 3 DEC 1974

TITLE: ADDRESS REGISTER

PROJECT: AMPEX B11, B12, B13, B14

SHEET 1 OF 2

NO. L0Ø95.Ø



The Aloha System BCC-500

F. YOSHIOKA

-3 DEC 1974

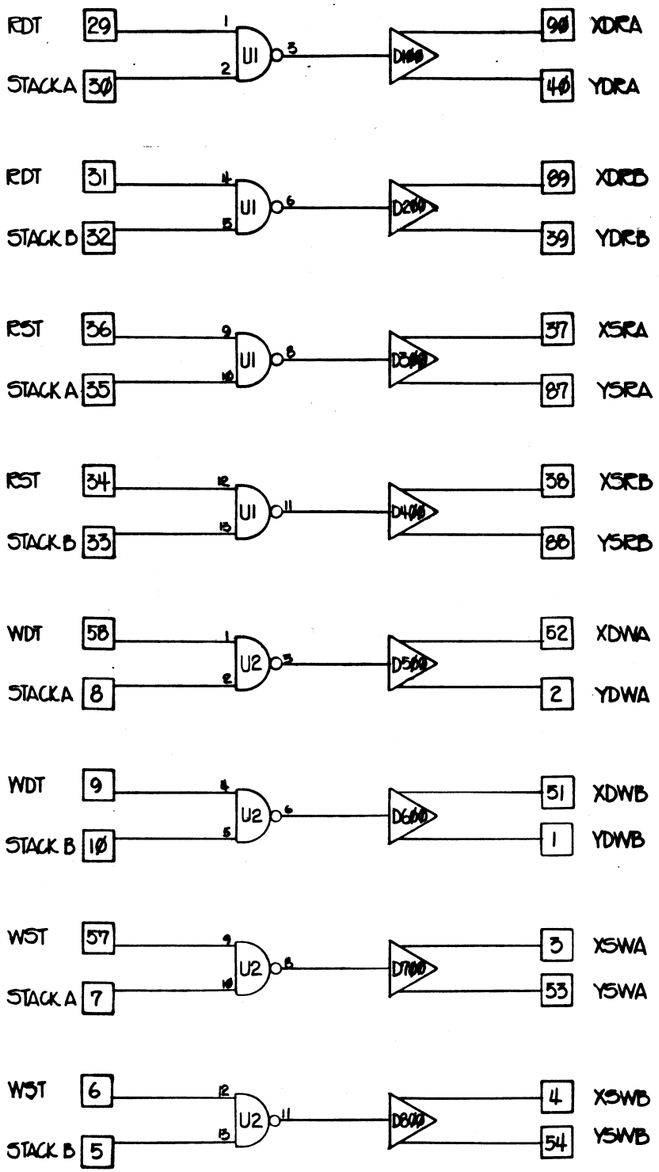
AMPEX

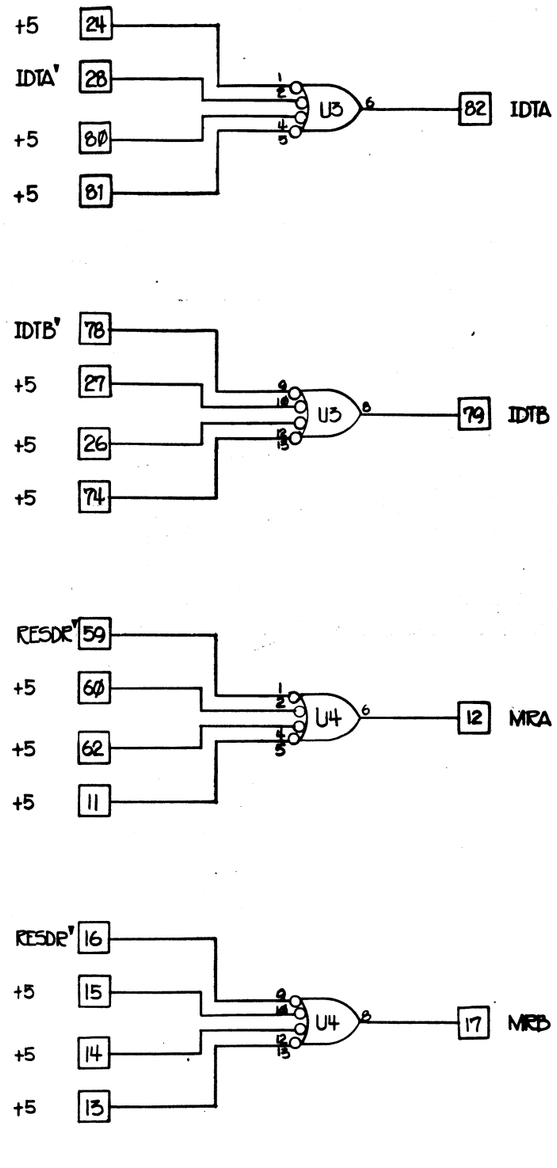
ADDRESS REGISTER

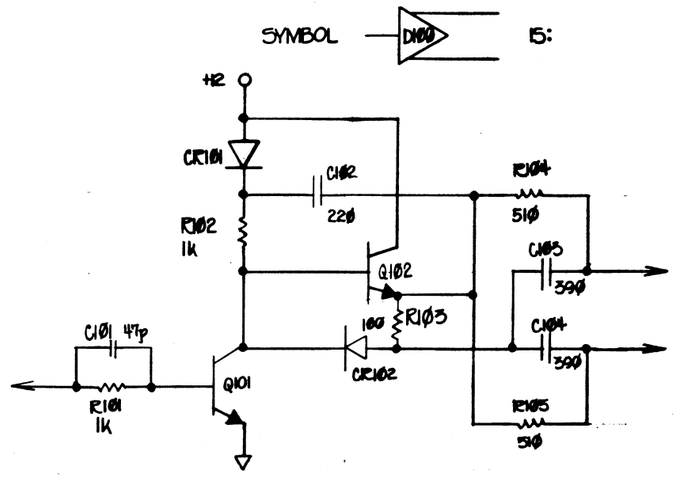
CARD TESTER

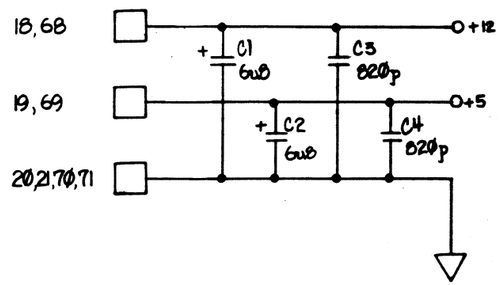
2 of 2

L01095.0









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.0	RELEASED			

REVISIONS

The Aloha System BCC-500

DESIGNED

DRAWN F. YOSHIOKA

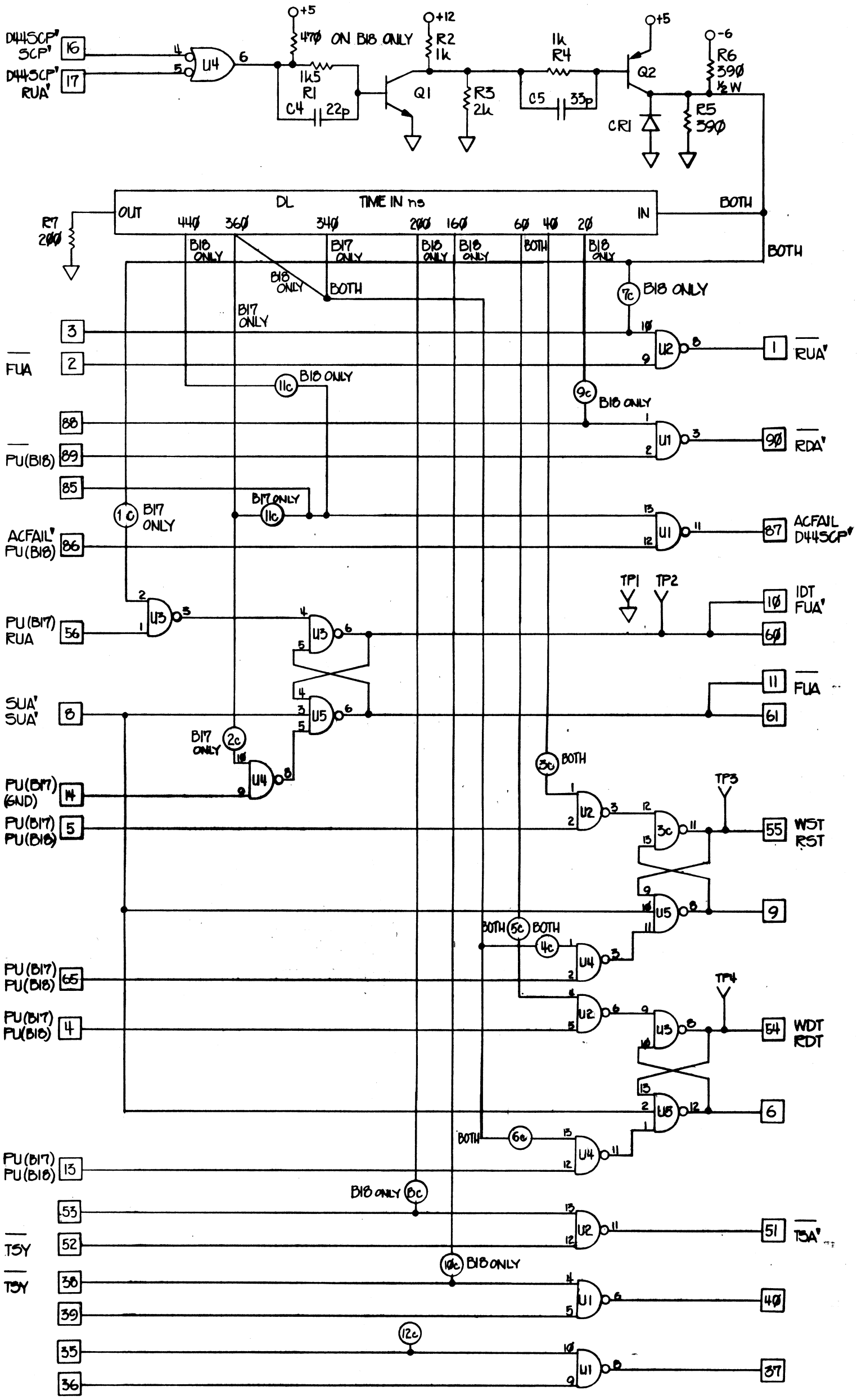
DATE - 3 DEC 1974

TITLE DRIVE CONTROL

PROJECT AMPEX B16

SHEET 1 OF 1

DWG. L01096.0



The Aloha System BCC-500

F. YOSHIOKA

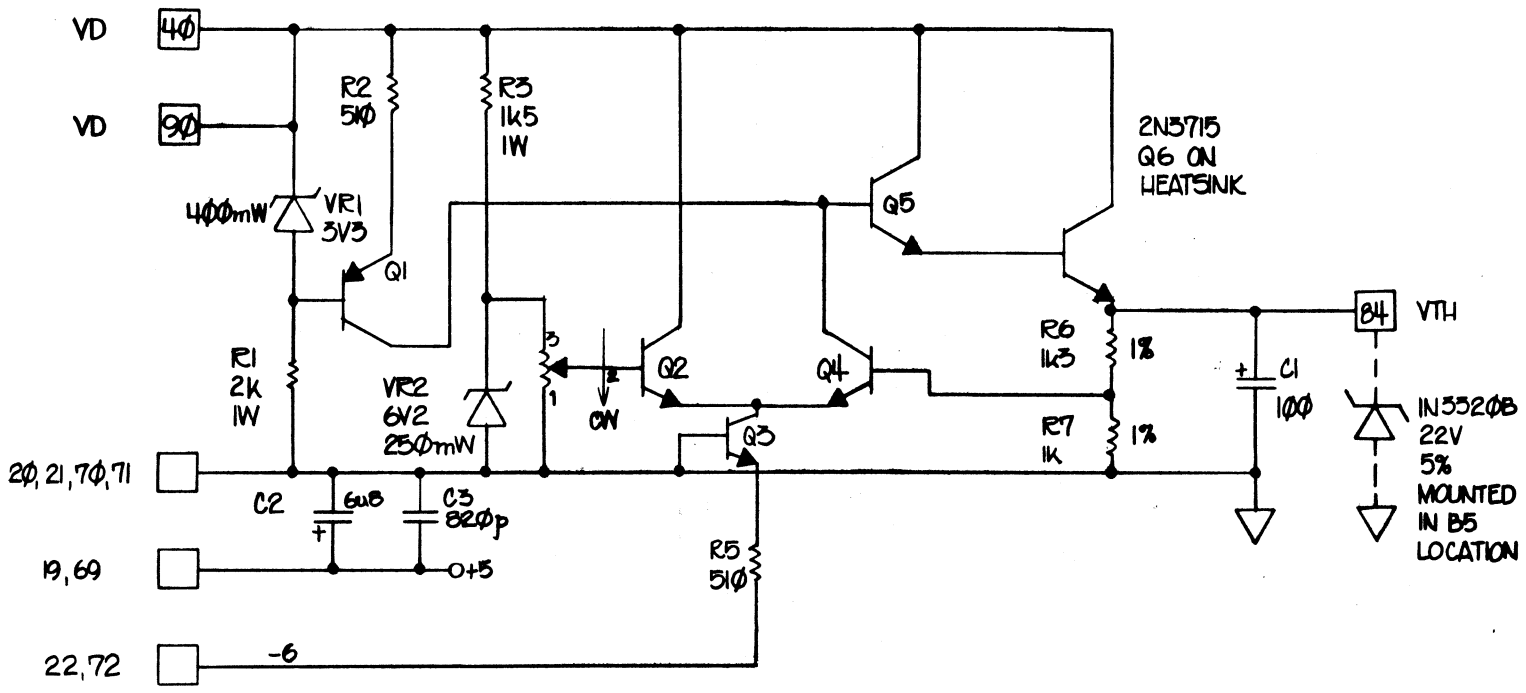
- 3 DEC 1974

TIMING

AMPEX B17 WRITE, B18 READ

L010.7.0

RELEASED



The Alpha System BCC-500			
DRAWN F. YOSHIOKA			
- 3 DEC 1974			
SIZE			
L01Ø98			

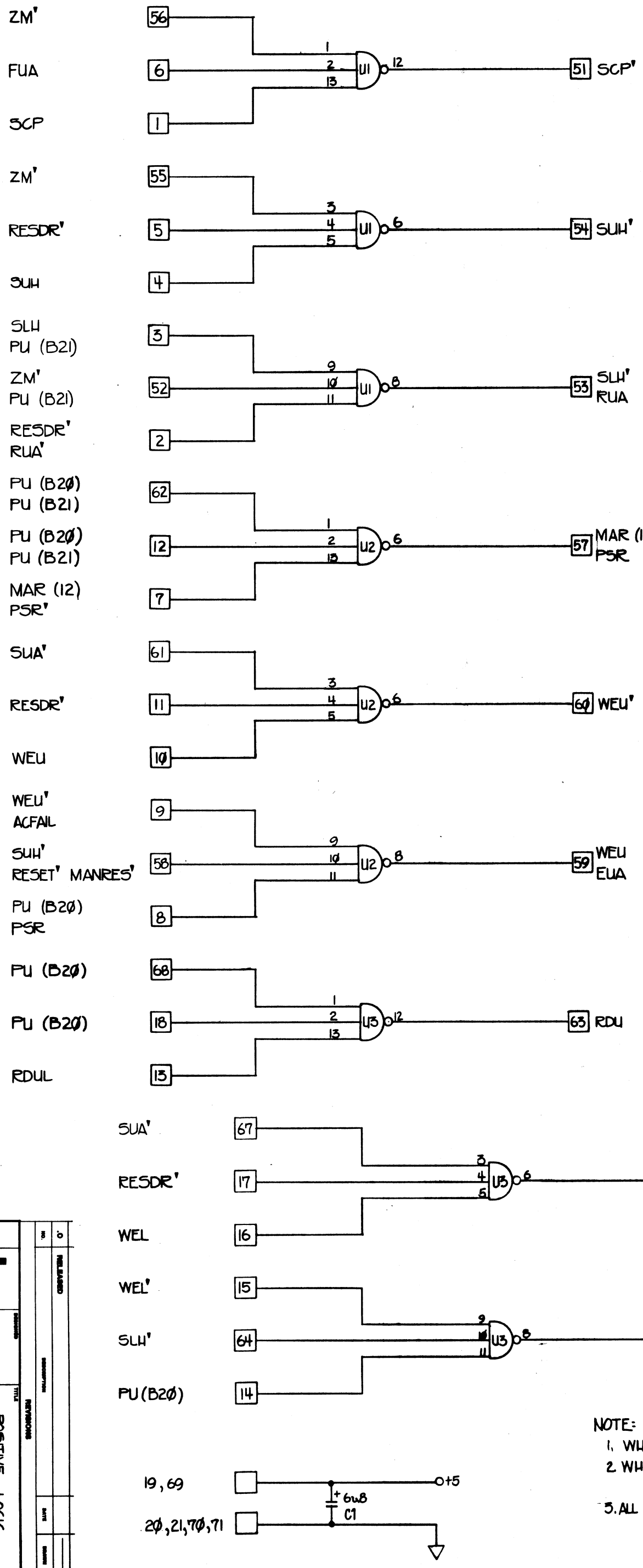
TITLE: STROBE CONTROL

PROJECT: AMPEX B19

SHEET 1 OF 1

NO.	DESCRIPTION	DATE	DRAWN	APPROVED
Ø	RELEASED			

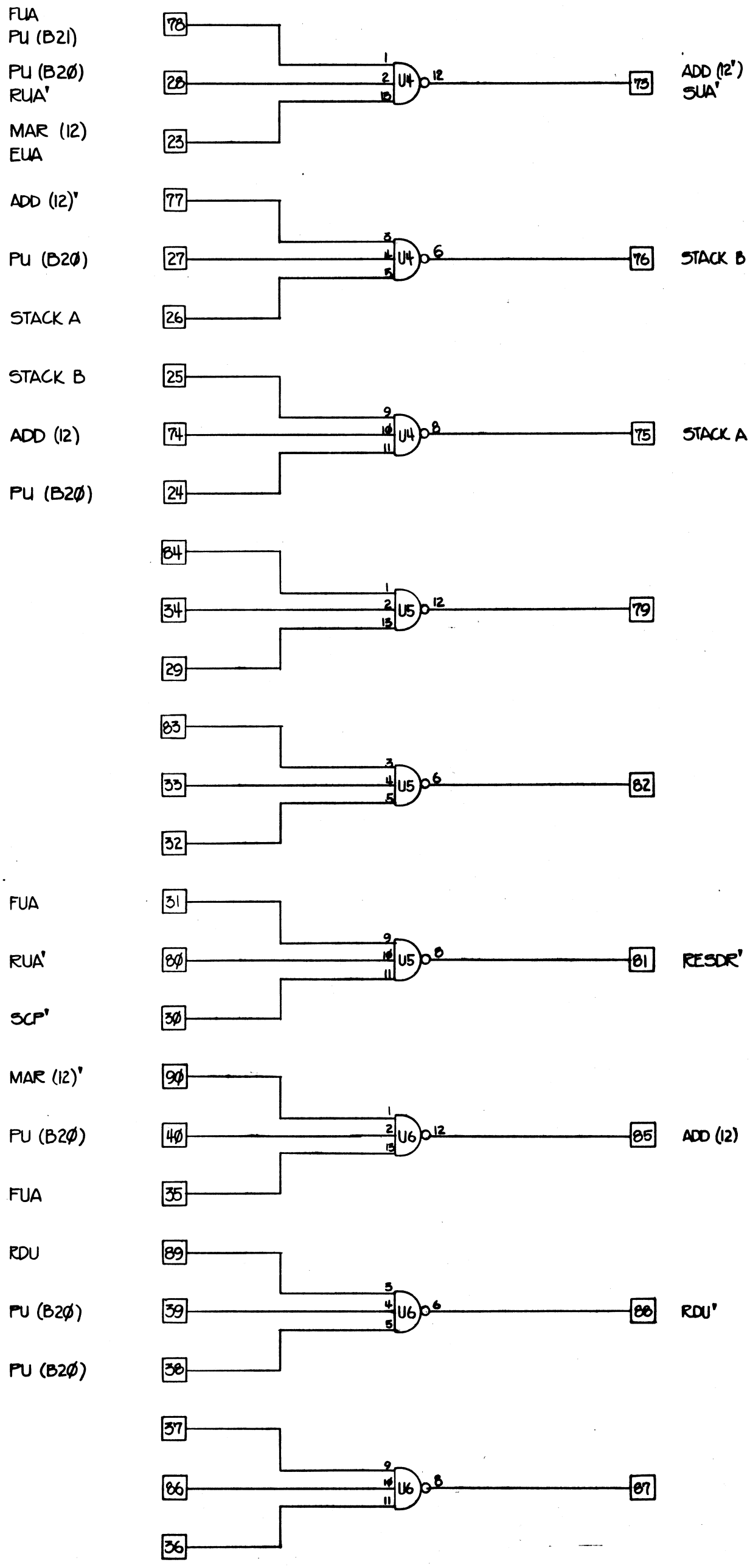
REVISIONS



NOTE:

1. WHEN SINGLE NAME B2Ø ONLY
2. WHEN DOUBLE NAME B2Ø TOP
   B21 BOTTOM
3. ALL MICROCIRCUITS ARE SN 741Ø

The Akhin System BCC-500	
DRAWN F.YOSHIOKA	
- 3 DEC 1974	
SHEET 1 OF 2	
PROJECT AMPEX B2Ø B21	
TITLE POSITIVE LOGIC CONTROL CIRCUITS	
DWG. NO. L01Ø99.Ø	
REVISIONS NO. .0 RELEASED	



.0	RELEASED	9/16/74	
NO.	DESCRIPTION	DATE	DRAWN / APPROVED

REVISIONS

The Alpha System BCC-500

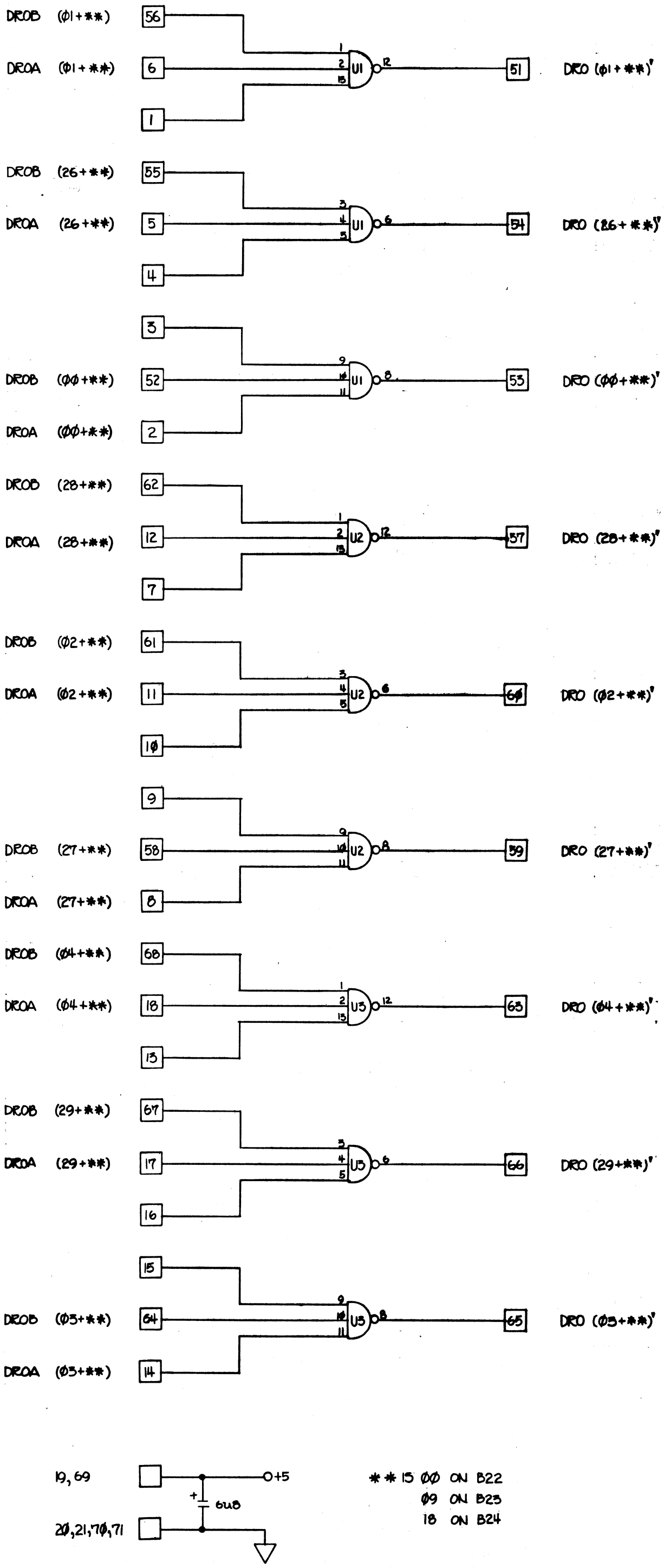
DRAWN F.YOSHIOKA
ENGR. CHK'D
ENGR. CHK'D
APPROVED
DATE - 3 DEC 1974

TITLE: POSITIVE LOGIC CONTROL CIRCUITS

PROJECT: AMPEX B2Ø B21

SHEET 2 OF 2

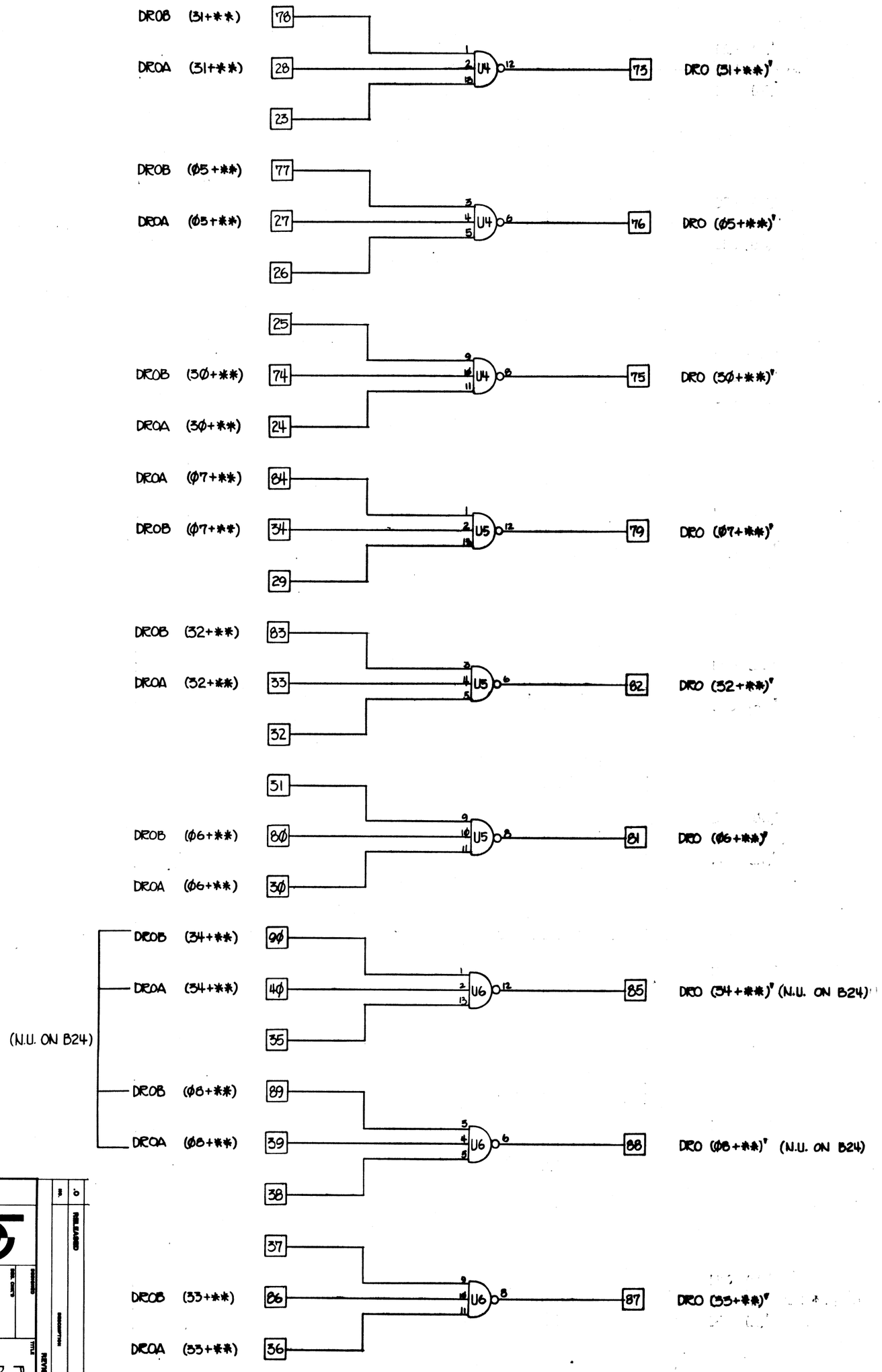
DR. L01099.Ø



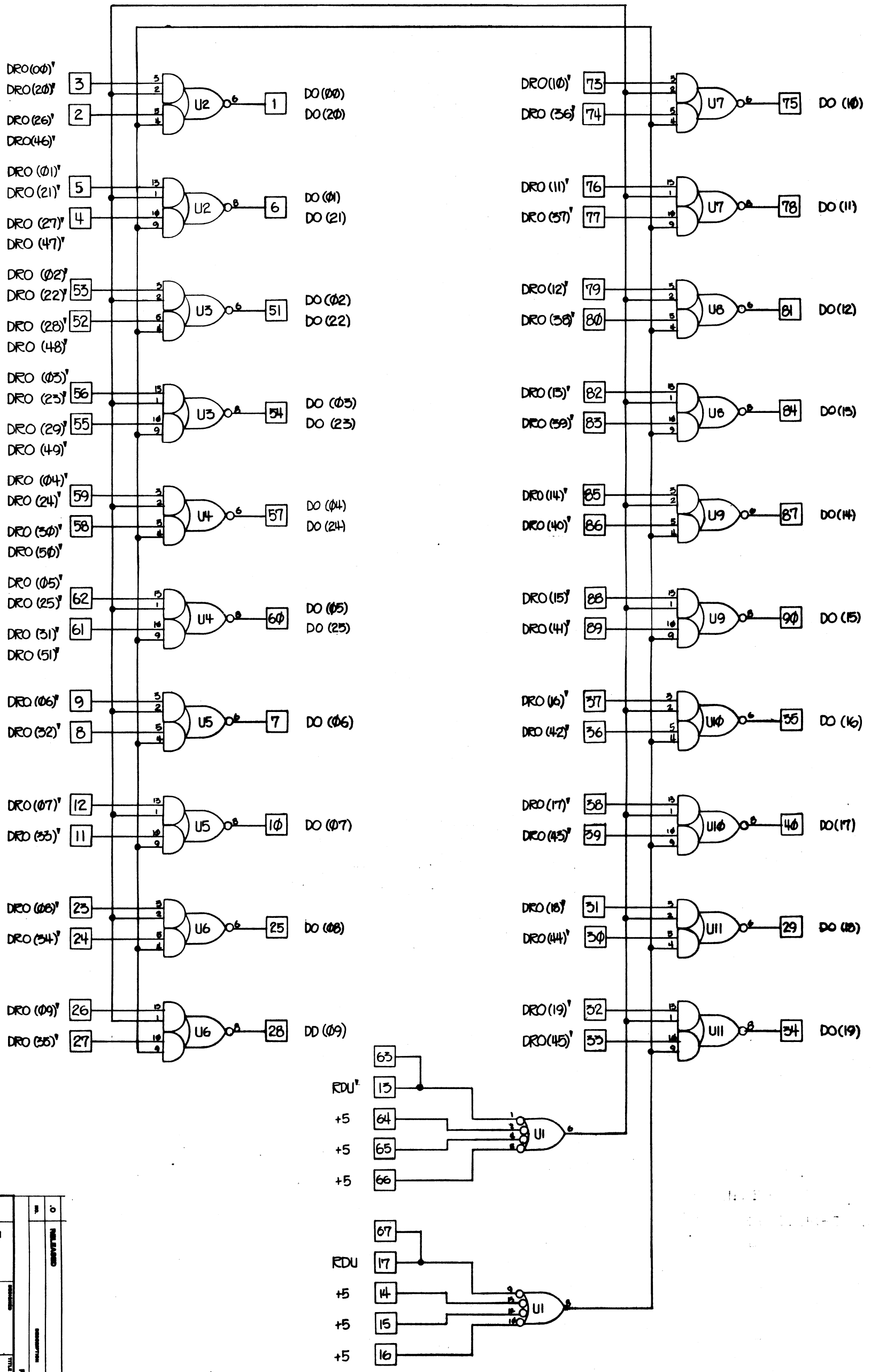
DRAWN	F.YOSHIOKA	The Alpha System DEC-20	
CHECKED			
APPROVED	- 3 DEC 1974		
SHEET	1 OF 2	PROJECT	AMPEX B22, B23, B24
SIZE	L Ø11 Ø Ø . Ø	TITLE	POSITIVE LOGIC DATA MIXING BY STACK

REVISIONS LATEST REVISION 9/20/74

NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

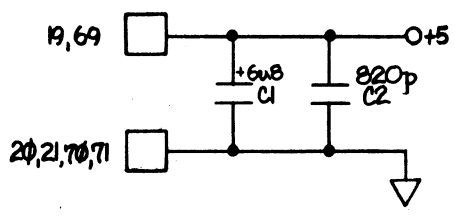


The Ampex System 800	
DRAWN F.YOSHIOKA	SEAL CHK'D
DATE - 3 DEC 1974	
SHEET 2 OF 2	
DWG. NO. LØ11ØØ.Ø	
PROJECT AMPEX B22, B23, B24	
TITLE POSITIVE LOGIC DATA MIXING BY STACK	
REVISIONS LATEST REVISION 9/20/74	
.0 RELEASED	

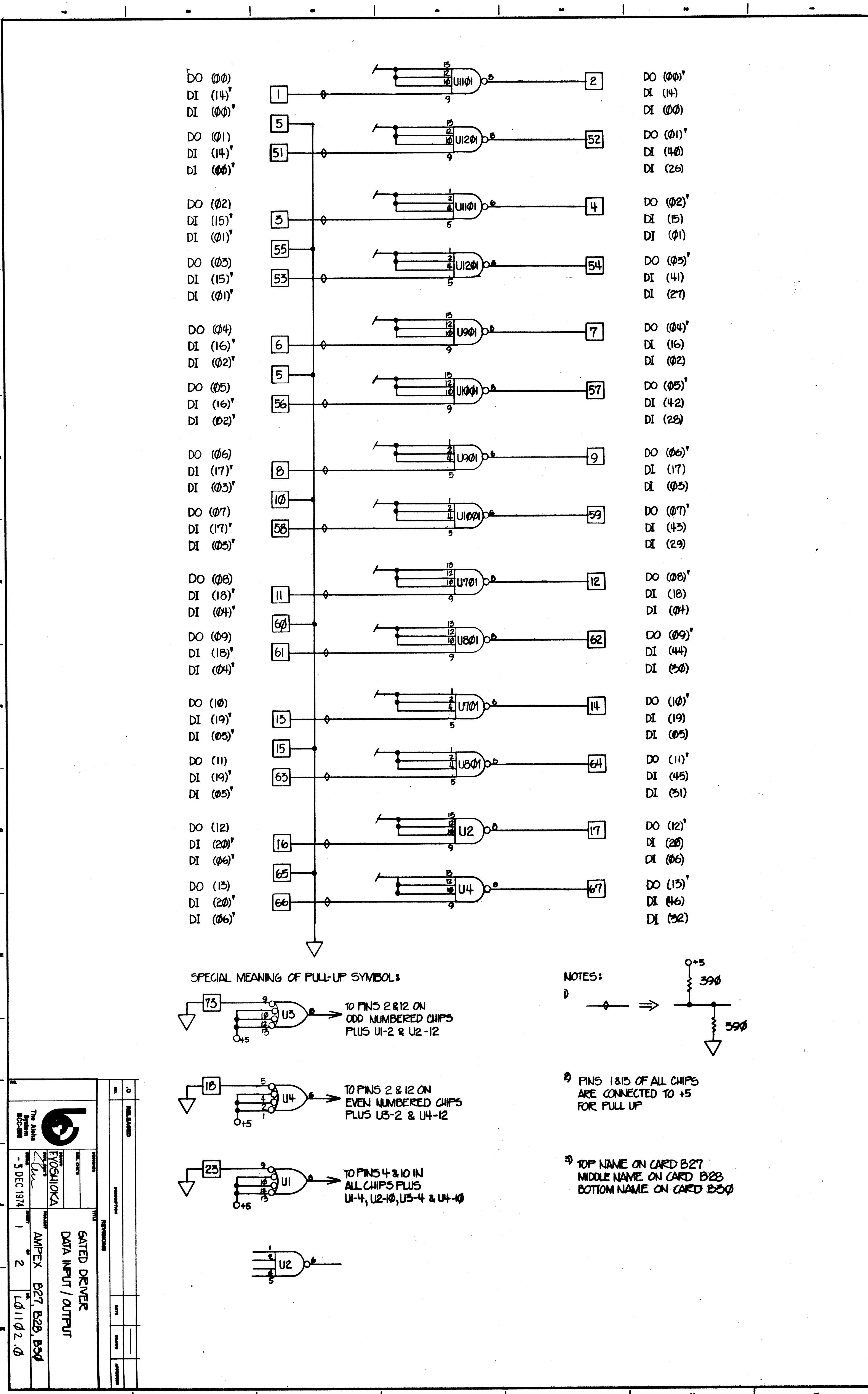


NOTE:

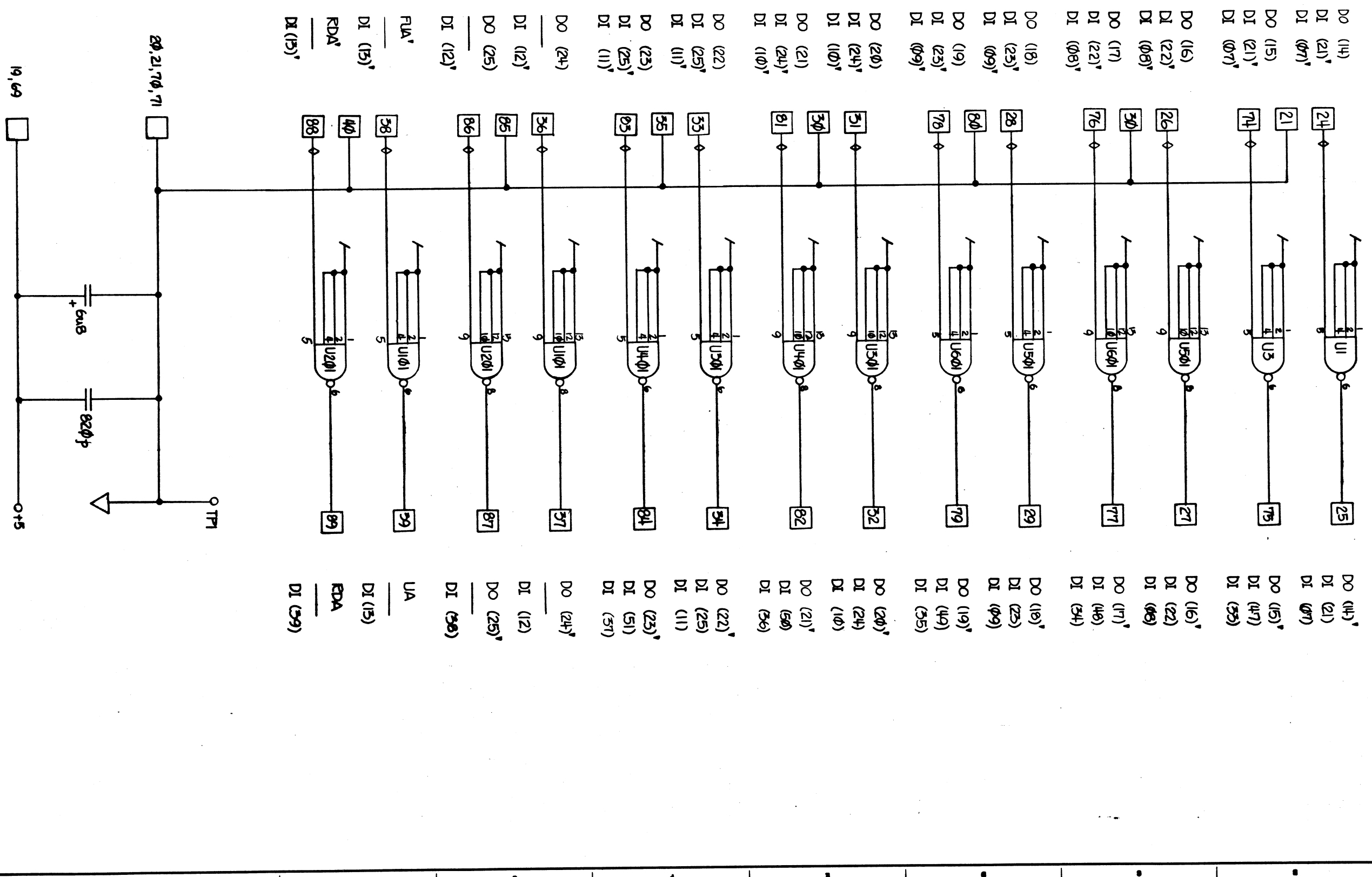
1. WHEN SINGLE NAME B25 ONLY
2. WHEN DOUBLE NAME B25 TOP
   B26 BOTTOM
3. ALL MICROCIRCUITS ARE SN7451
   EXCEPT U1 WHICH IS SN74540



The Alpha System BCC-500			.0 RELEASED
DRAWN F.YOSHIOKA			
- 3 DEC 1974			
SIZE B	SHEET 1 OF 1	PROJECT AMPEX B25, B26	TITLE POSITIVE LOGIC B DATA U/L MIXING
		DWG. L0110101.0	



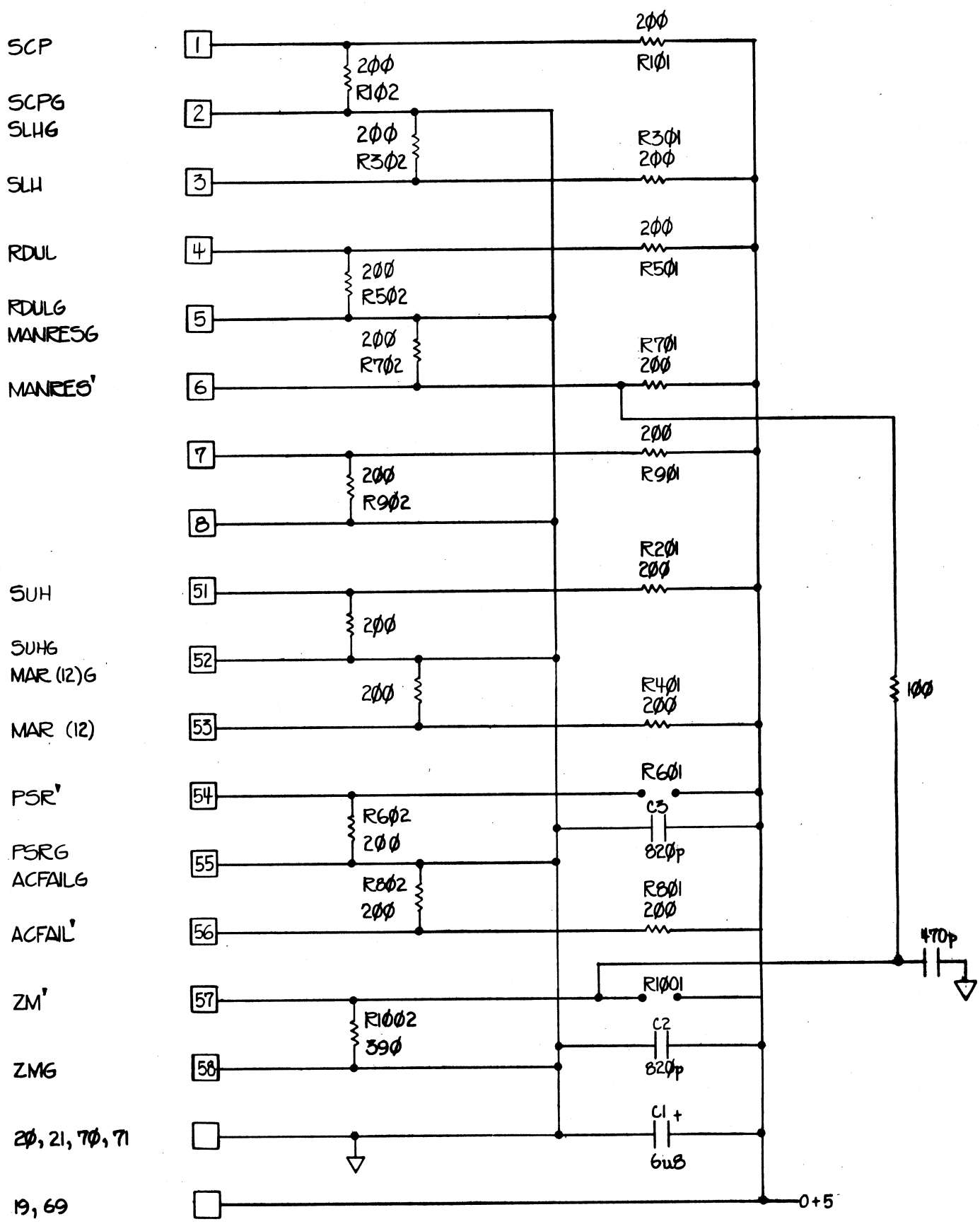
DO (ØØ)
DI (14)'
DI (ØØ)'
DO (Ø1)
DI (14)'
DI (ØØ)'
DO (Ø2)
DI (15)'
DI (Ø1)'
DO (Ø3)
DI (15)'
DI (Ø1)'
DO (Ø4)
DI (16)'
DI (Ø2)'
DO (Ø5)
DI (16)'
DI (Ø2)'
DO (Ø6)
DI (17)'
DI (Ø3)'
DO (Ø7)
DI (17)'
DI (Ø3)'
DO (Ø8)
DI (18)'
DI (Ø4)'
DO (Ø9)
DI (18)'
DI (Ø4)'
DO (1Ø)
DI (19)'
DI (Ø5)'
DO (11)
DI (19)'
DI (Ø5)'
DO (12)
DI (2Ø)'
DI (Ø6)'
DO (13)
DI (2Ø)'
DI (Ø6)'
U11Ø1
U12Ø1
U9Ø1
U1ØØ1
U7Ø1
U8Ø1
U2
U4
DO (ØØ)'
DI (14)
DI (ØØ)
DO (Ø1)'
DI (4Ø)
DI (26)
DO (Ø2)'
DI (15)
DI (Ø1)
DO (Ø3)'
DI (41)
DI (27)
DO (Ø4)'
DI (16)
DI (Ø2)
DO (Ø5)'
DI (42)
DI (28)
DO (Ø6)'
DI (17)
DI (Ø3)
DO (Ø7)'
DI (43)
DI (29)
DO (Ø8)'
DI (18)
DI (Ø4)
DO (Ø9)'
DI (44)
DI (3Ø)
DO (1Ø)'
DI (19)
DI (Ø5)
DO (11)'
DI (45)
DI (31)
DO (12)'
DI (2Ø)
DI (Ø6)
DO (13)'
DI (46)
DI (32)
SPECIAL MEANING OF PULL-UP SYMBOL:
U3
TO PINS 2 & 12 ON ODD NUMBERED CHIPS PLUS U1-2 & U2-12
U4
TO PINS 2 & 12 ON EVEN NUMBERED CHIPS PLUS U3-2 & U4-12
U1
TO PINS 4 & 10 IN ALL CHIPS PLUS U1-4, U2-1Ø, U3-4 & U4-1Ø
+5
NOTES:
1)
390
39Ø
2) PINS 1 & 13 OF ALL CHIPS ARE CONNECTED TO +5 FOR PULL UP
3) TOP NAME ON CARD B27
MIDDLE NAME ON CARD B28
BOTTOM NAME ON CARD B3Ø
The Aloha System BCC-500
F. YOSHIOKA
-3 DEC 1974
GATED DRIVER
DATA INPUT / OUTPUT
AMPEX B27, B28, B3Ø
1 OF 2
LØ11Ø2.Ø
REVISIONS
RELEASED



NO.	REVISIONS	DATE	BY	APPROVED
A	RELEASED			

TITLE	GATED DRIVER DATA INPUT / OUTPUT
DRAWING	F105H10KA
PROJECT	AMPEX B27, B28, B50
DRAWN	
DESIGNED	
CHECKED	
APPROVED	
DATE	- 3 DEC 1974
SHEET	2 OF 2
SIZE	B
FSCM NO.	80009
DWG NO.	L011Ø2 .Ø

The Alpha System BCC-080



.0	RELEASED				
NO.	DESCRIPTION		DATE	ENGRG	APPROVED

REVISIONS LATEST REVISION 9/16/74

TITLE: LINE TERMINATOR

DRAWN: F.YOSHIOKA

PROJECT: AMPEX B31

SHEET 1 OF 1

DWG. NO. L0110503

DATE: 3 DEC 1974

The Alpha System BCC-500

BRACKET

F,H,W, CC — COM — 7

E,J,V,DD D,S — COM — 6

G,R — -6 — 5

B,N — +5 — 4

A,M — +12 — 3

K,L — +26 — 2

T,Y — +33 — 1

3Ω, 25W — COM

1.5Ω x 4A = 6V

-6V

3Ω, 25W — COM

2Ω, 25W

2Ω, 25W — +12V

.4Ω x 13 = 5.2V

2Ω, 25W — +5

2Ω, 25W

2Ω, 25W

VI (26V)

4A

5Ω 175W

3Ω 100W — COM

3Ω x 4A = 12V — +12

3Ω 100W

25Ω 100W

8.3Ω x 4A = 33V — +VD

25Ω 100W — +33V

25Ω 100W

12K1, 1%

82K, 10%, ¼W

51K1 5% ¼W

100m 35V

2N2905

15K 5% ¼W

820, 10% 1W

2Ω, 30W RE715 GE2000 RH 50

SCR 2N2575

1K43, 1%

2K2, 10% ¼W

2K2, 10% ¼W

2u2

1N748A, 3V9

1K, 10% 1W

COM

TB (SMALL)

Z — 6

X — 5

BB — 4

AA — 3

C — 2

+5 — 1

REMOTE ON

MAINRES'

PSR'

AC FAIL

NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

REVISIONS

The Aloha System BCC-500

DESIGNED

ENG. CHK'D

DRAWN F.YOSHIOKA

DOC. CHK'D

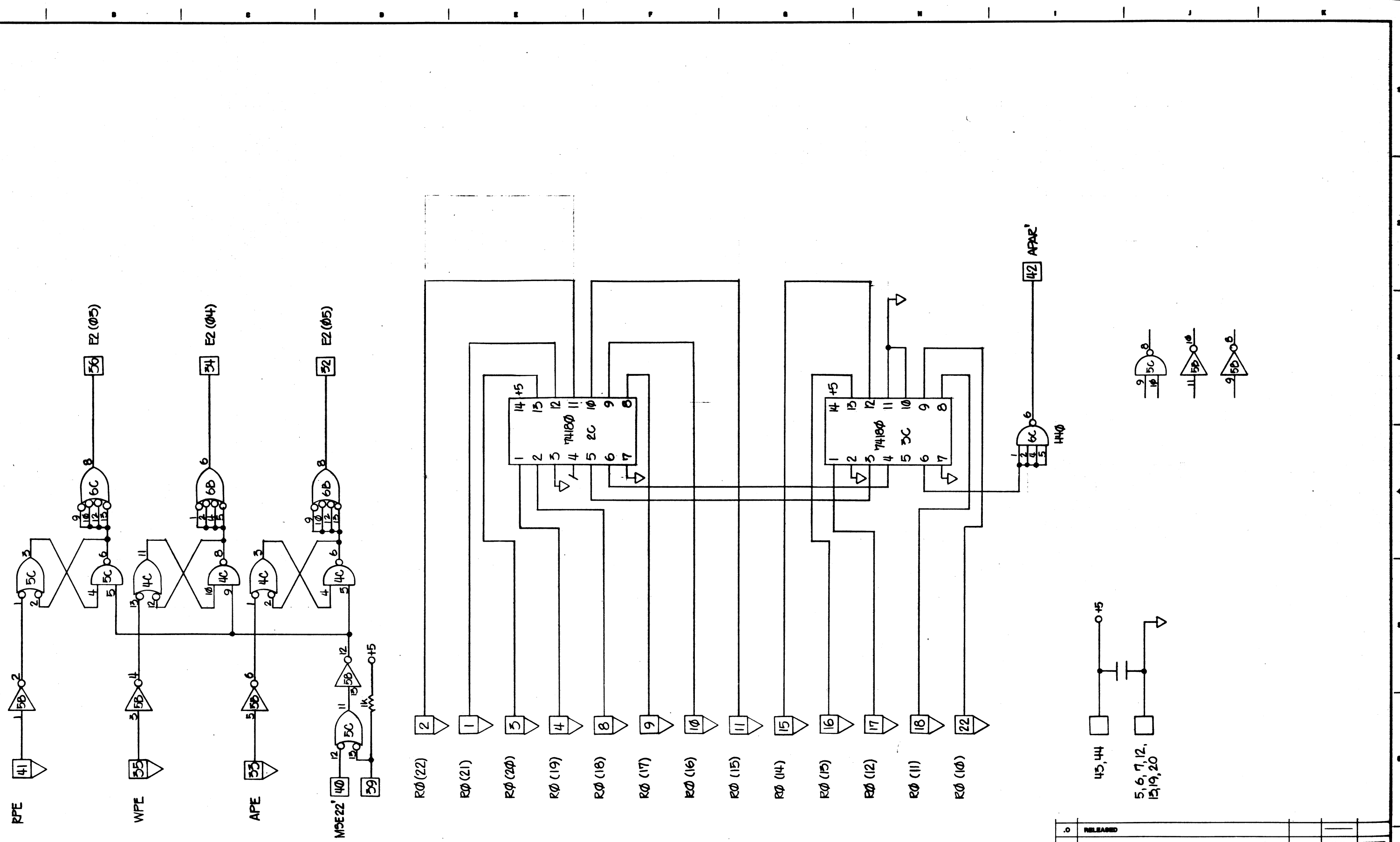
DATE - 3 DEC 1974

TITLE SUPPLY DUMMY LOAD AMPEX CORE PWR

PROJECT AMPEX

SHEET 1 OF 1

NO. LØ1105.Ø

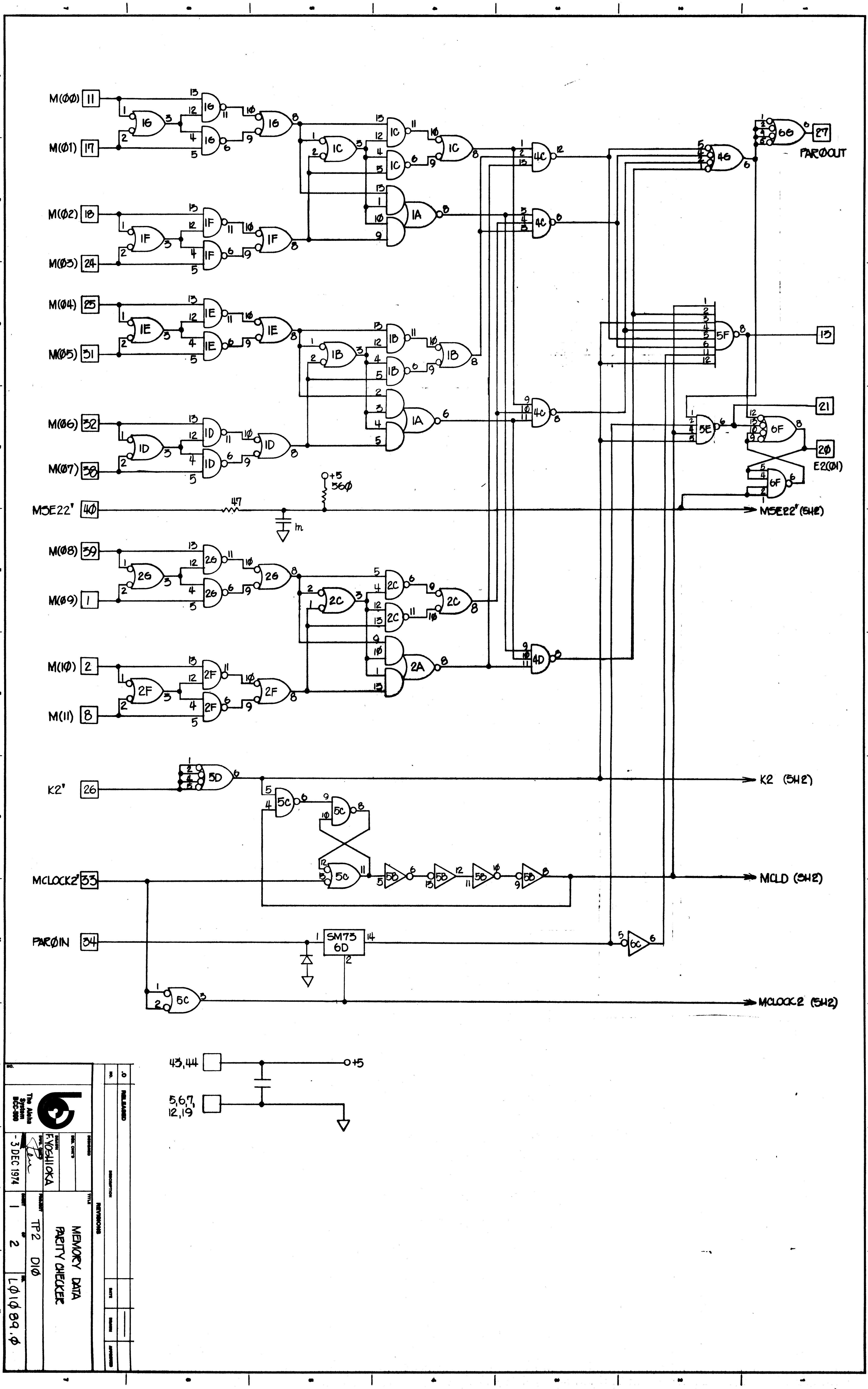


NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

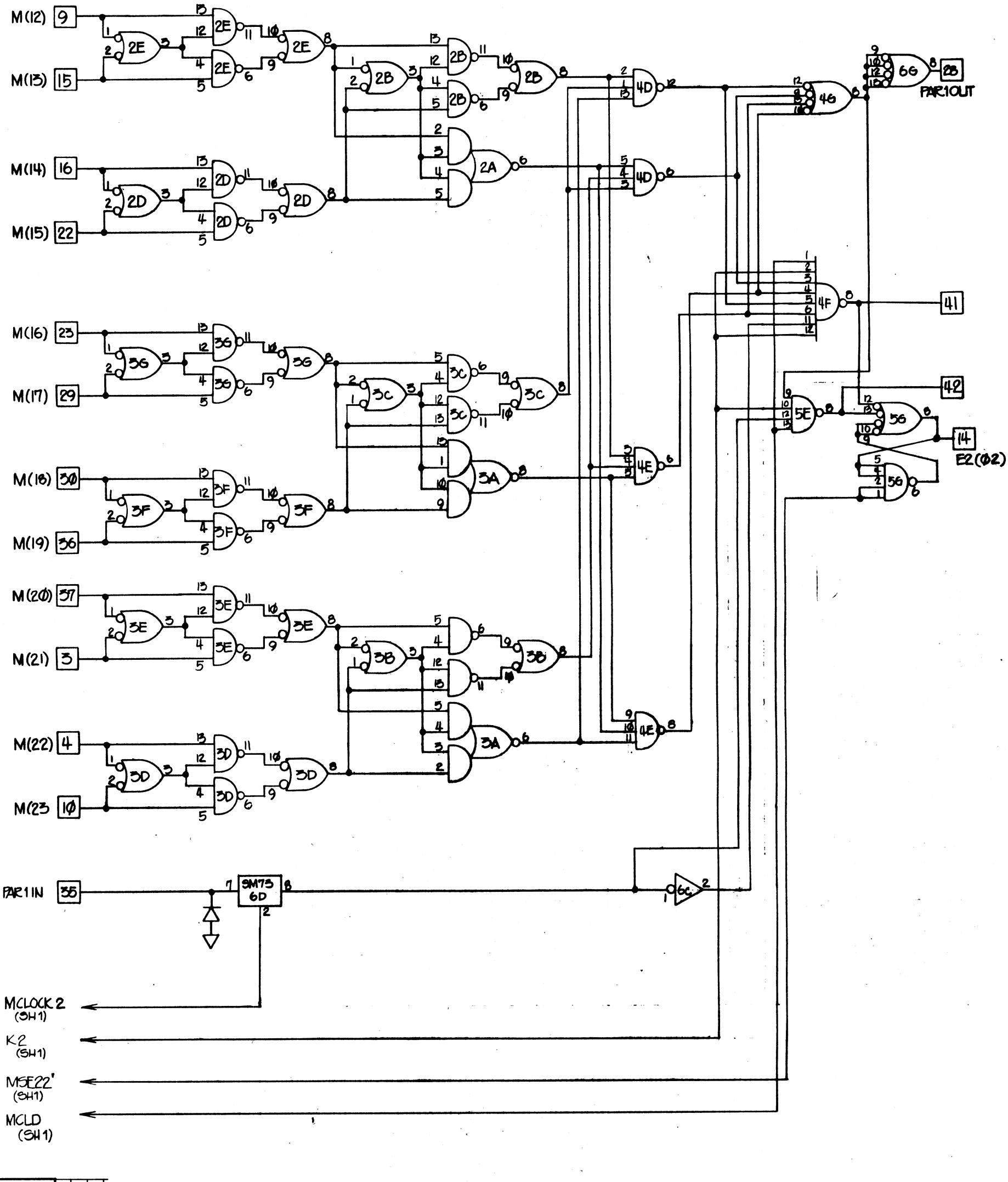
REVISIONS

DESIGNED	
DES. CHK'D	
DRAWN	F. YOSHIOKA
DWG. CHK'D	
APPROVED	- 3 DEC 1974
TITLE	MEMORY ADDRESS PARITY
PROJECT	TP2 D9
SHEET	1 OF 1
DWG. NO.	LØ1Ø88.Ø

The Aloha System BCC-500



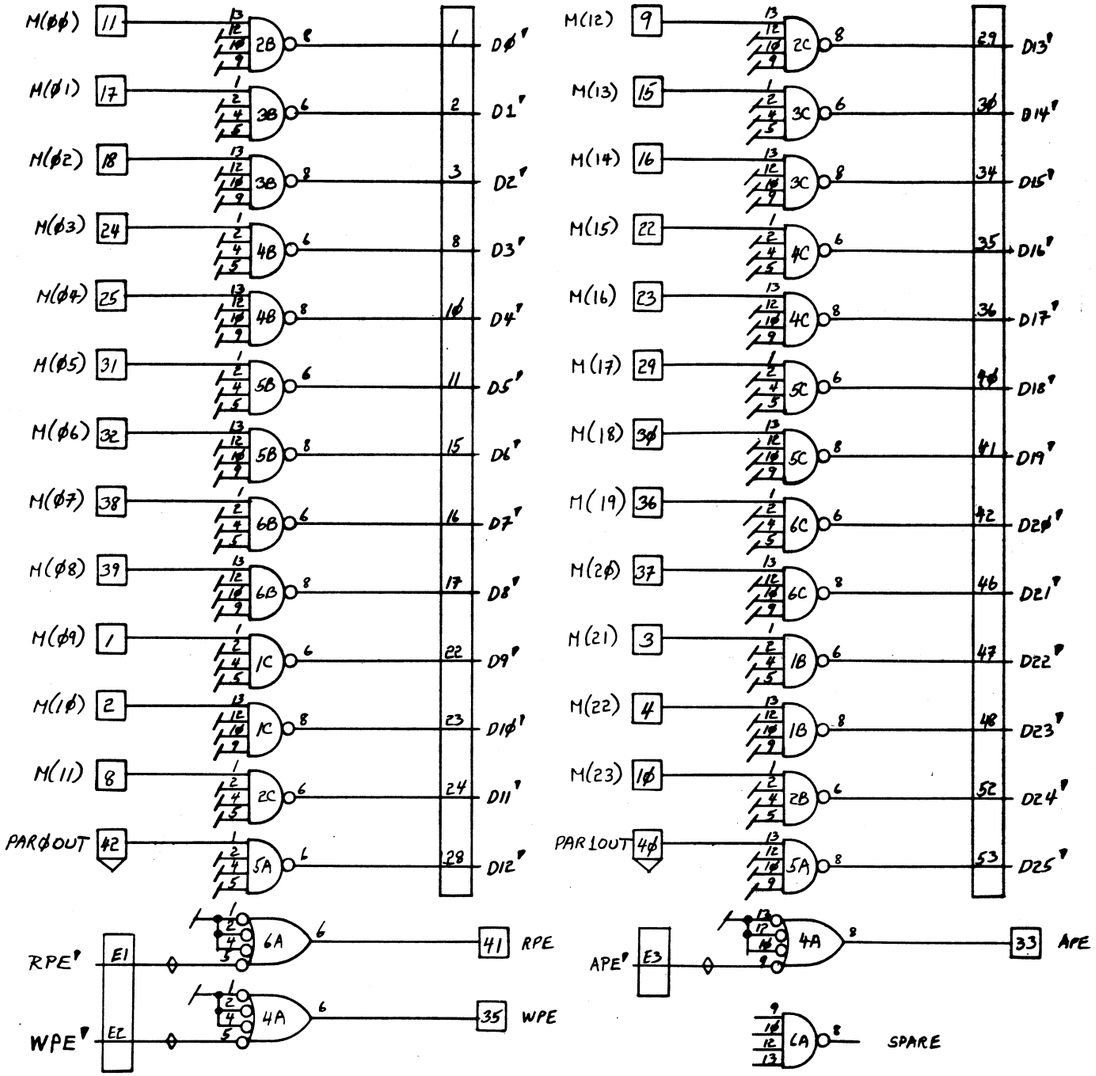
M(ØØ) 11
M(Ø1) 17
M(Ø2) 18
M(Ø3) 24
M(Ø4) 25
M(Ø5) 31
M(Ø6) 32
M(Ø7) 38
MSE22' 4Ø
47
+5
56Ø
M(Ø8) 39
M(Ø9) 1
M(1Ø) 2
M(11) 8
K2' 26
MCLOCK2' 33
PARØIN 34
SM73
6D
27
PARØOUT
13
21
2Ø
E2(Ø1)
MSE22' (5H2)
K2 (5H2)
MCLD (5H2)
MCLOCK2 (5H2)
43,44
+5
5,6,7,
12,19
The Aloha System BCC-500
F. YOSHIOKA
-3 DEC 1974
MEMORY DATA
PARITY CHECKER
TP2 D1Ø
1
2
LØ1Ø89.Ø
REVISIONS

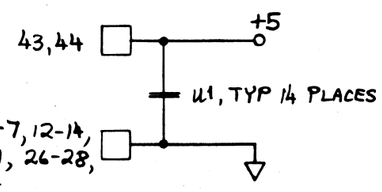


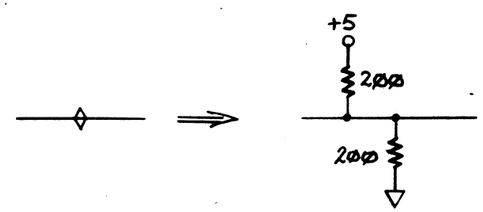
The Alpha System DEC-339	DRAWN F.YOSHIOKA - 3 DEC 1974	TITLE MEMORY DATA PARITY CHECKER	.0 RELEASED
	DES. ENGR.	PROJECT TP2 DIØ	
	APPR. ENGR.	SHEET 2 OF 2	DWG. LØ1ØØ9.Ø

REVISIONS

NO.	DESCRIPTION	DATE	DRAWN	APPROVED







E3 APE' (PIN 73) — 54 — 53 D25' — (73)

52 D27' — 48 D23' — 47 D22'

46 D21' — 42 D2Ø' — 41 D19'

65 — 75 — 74

58 — 67 — 66

E4 — 6Ø — 59

4Ø D18'
(34) D15'

EDGE PINS ←

E1 RPE' (PIN 75) — 17 D8' — 16 D7'

15 D6' — 11 D5' — 1Ø D4'

8 D3' — 3 D2' — 2 D1'

28 D12' — 36 D17' — 35 D16'

22 D9' — 3Ø D14' — 29 D13'

E2 WPE' (PIN 74) — 24 D11' — 23 D1Ø'

1 DØ'

⇒ CABLE

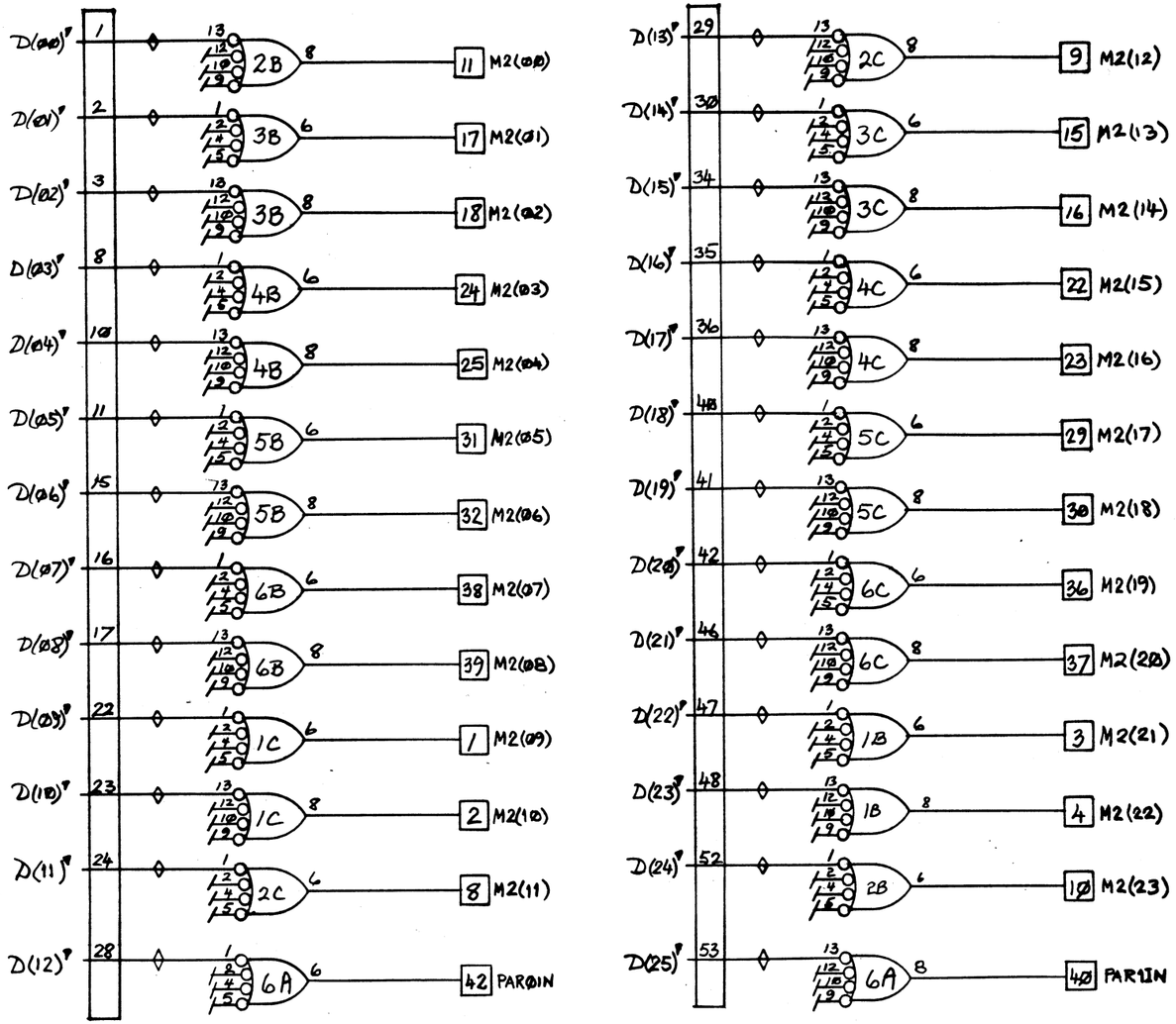
NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

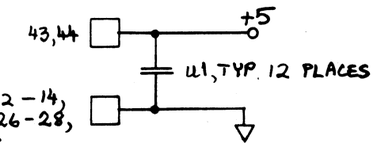
REVISIONS

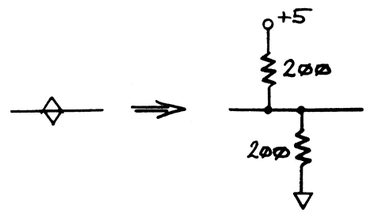
The Aloha System BCC-800

DESIGNED CARDESTAM
DES. CHK'D
DRAWN HATSUYAMA
ENGR. CHK'D
SCALE

TITLE LOCAL MEMORY DATA OUT CABLE CARD
PROJECT TP2 DØ11
SHEET 1 OF 1
NO. LØ11Ø6.Ø







E3 54 53 D(25)▼ (73)

52 D(24)▼ 48 D(23)▼ 47 D(22)▼

46 D(21)▼ 42 D(20)▼ 41 D(19)▼

65 75 74

58 67 66

E4 60 59

40 D(18)▼
(34) D(15)▼

EDGE PINS ←

E1 17 D(08)▼ 16 D(07)▼

15 D(06)▼ 11 D(05)▼ 10 D(04)▼

8 D(03)▼ 3 D(02)▼ 2 D(01)▼

28 D(12)▼ 36 D(17)▼ 35 D(16)▼

22 D(09)▼ 30 D(14)▼ 29 D(13)▼

E2 24 D(11)▼ 23 D(10)▼

1 D(00)▼

⇒ CABLE

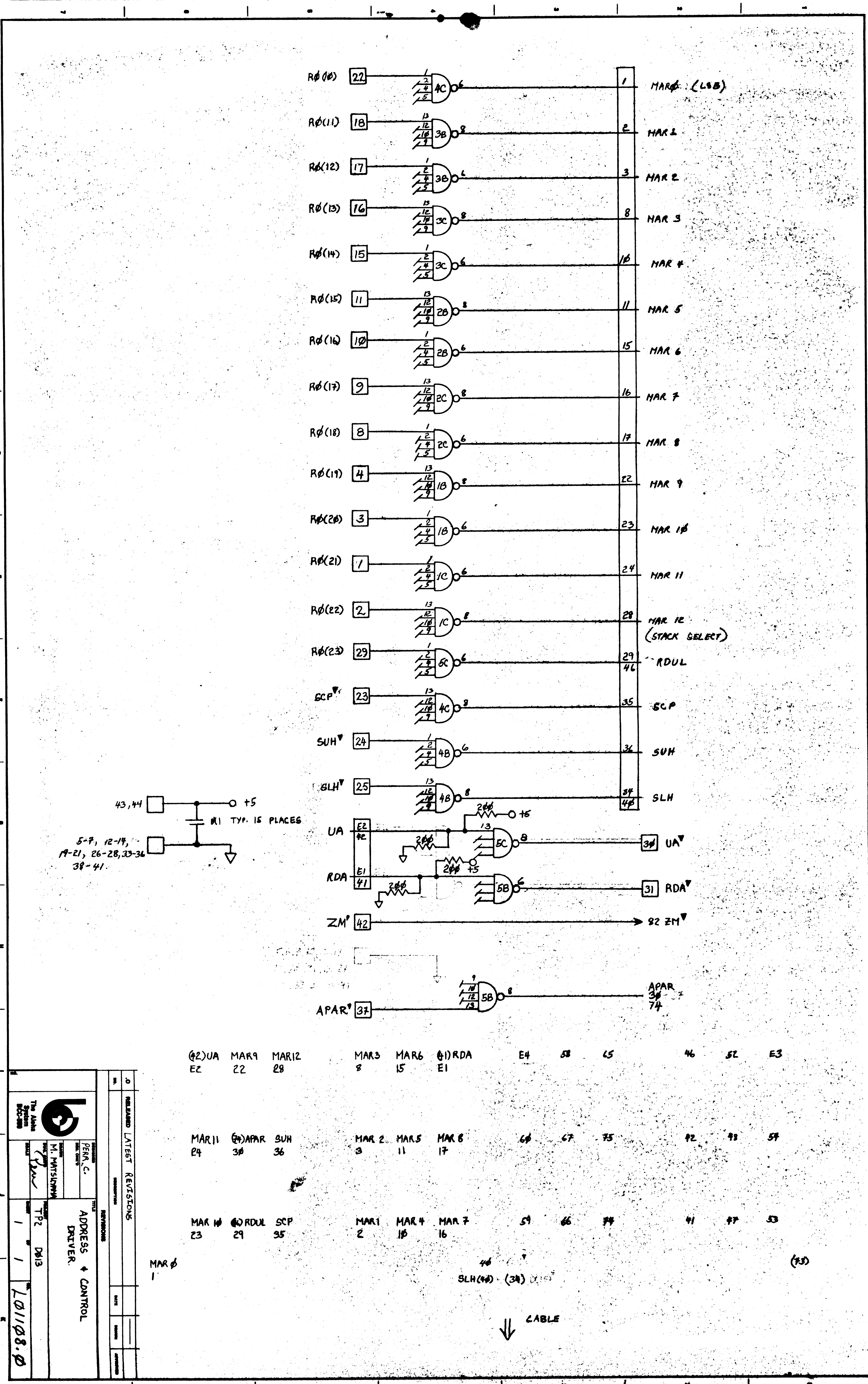
NO.	DESCRIPTION	DATE	DRAWN	APPROVED
.0	RELEASED			

REVISIONS

The Aloha System BCC-500

DESIGNED: CARDESTAM
DRAWN: MATSUYAMA
PROJECT: TP2 D012
SCALE:
SHEET 1 OF 1
SIZE: L01107.00

TITLE: LOCAL MEMORY DATA BACK CABLE CARD


RØ(1Ø) 22 4C 6 1 MARØ (LSB)
RØ(11) 18 3B 8 2 MAR 1
RØ(12) 17 3B 6 3 MAR 2
RØ(13) 16 3C 8 8 MAR 3
RØ(14) 15 3C 6 1Ø MAR 4
RØ(15) 11 2B 8 11 MAR 5
RØ(16) 1Ø 2B 6 15 MAR 6
RØ(17) 9 2C 8 16 MAR 7
RØ(18) 8 2C 6 17 MAR 8
RØ(19) 4 1B 8 22 MAR 9
RØ(2Ø) 3 1B 6 23 MAR 1Ø
RØ(21) 1 1C 6 24 MAR 11
RØ(22) 2 1C 8 28 MAR 12 (STACK SELECT)
RØ(23) 29 5C 6 29 46 RDUL
SCP 23 4C 8 35 SCP
SUH 24 4B 6 36 SUH
SLH 25 4B 8 34 4Ø SLH
43,44 +5
C1 TYP. 15 PLACES
5-7, 12-14, 19-21, 26-28, 33-36 38-41.
UA E2 42 2ØØ +5 5C 8 3Ø UA
RDA E1 41 2ØØ +5 5B 6 31 RDA
ZM 42 82 ZM
APAR 37 5B 8 APAR 3Ø 74
(42)UA E2
MAR9 22
MAR12 28
MAR3 8
MAR6 15
(41)RDA E1
E4 58 65 46 52 E3
MAR11 24
(24)APAR 3Ø
SUH 36
MAR 2 3
MAR5 11
MAR 8 17
6Ø 67 75 42 48 54
MAR 1Ø 23
(46)RDUL 29
SCP 35
MAR1 2
MAR 4 1Ø
MAR 7 16
59 66 74 41 47 53
MAR Ø 1
46
SLH(4Ø) (34)
(73)
CABLE
The Aloha System BCC-500
RELEASED LATEST REVISIONS
PERR, C.
M. MATSUKAWA
ADDRESS + CONTROL DRIVER.
TP2 D013
1 1
LØ11Ø8.Ø