

RACK C

RACK B

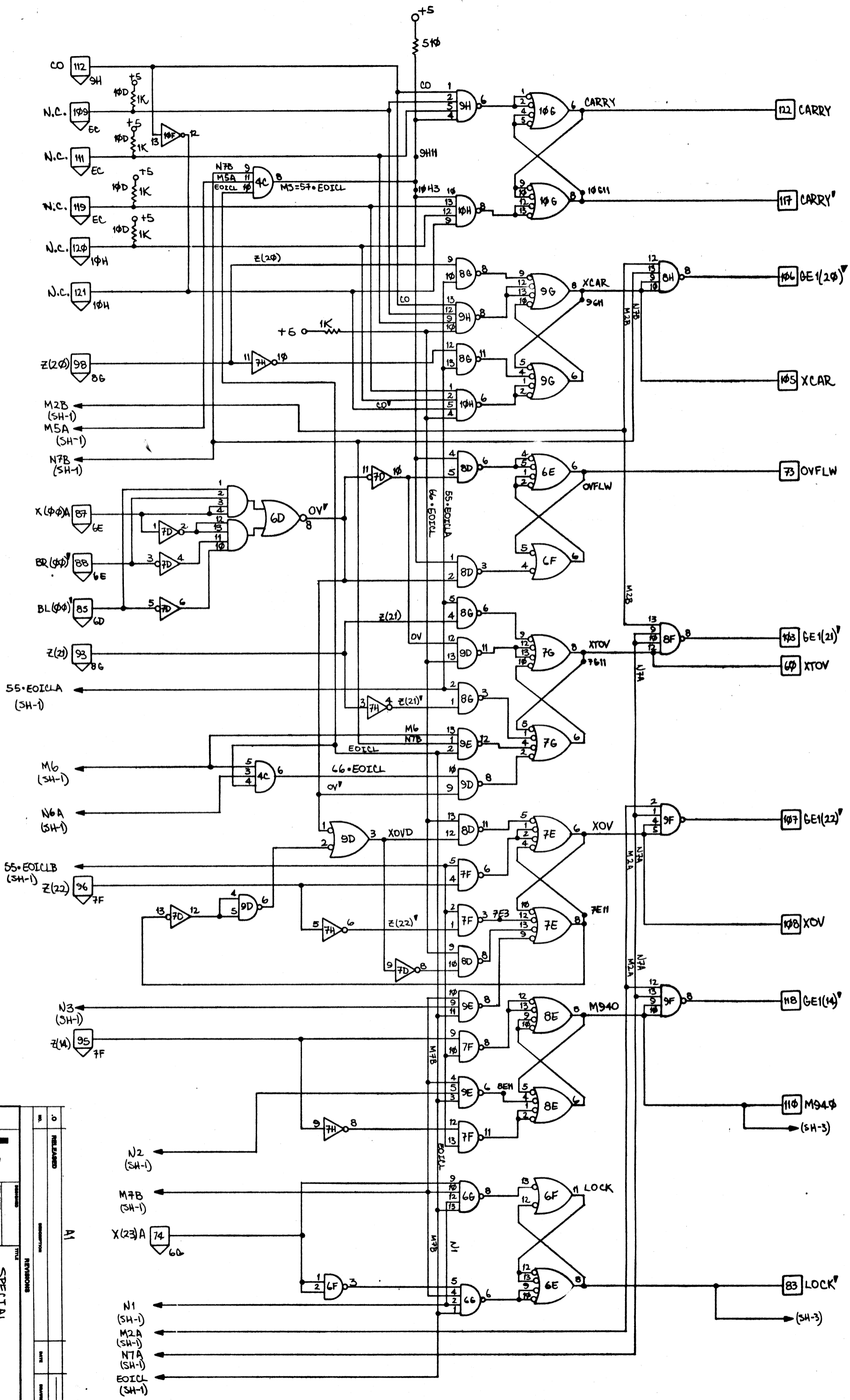
RACK A

33	ITR, CPU 0	ROM 20	I/O INTERFACE	33
32	CTR, CPU 0	ROM 21	SCRATCH PAD (00-15)	32
31	UNG CABLE	ROM 22	HOLDING REG (16-23)	31
30	UNG	ROM 23	CYCLER/ADDER (16-23)	30
29	CTR, CPU 1	ROM 24	M0Z REGISTER (16-23)	29
28	ITR CPU 1	ROM 25	MUL REGISTER	28
27	UNG CLOCK	ROM 26	MUL REGISTER	27
26		ROM 27	MUL REGISTER	26
25		ROM 00	MULT CONT	25
24		ROM 01	IFU DATA & REG	24
23		ROM 02	IFU MAR - PAR	23
22		ROM 03	IFU CONTROL	22
21		ROM 04	IFU NJR	21
20		ROM 05	SCRATCH PAD (00-15)	20
19		ROM 06	HOLDING REG (00-15)	19
18		ROM 07	CYCLER/ADDED (00-15)	18
17		I-REGISTER I5	M0Z REGISTER (00-15)	17
16		I-REGISTER I4	MAP REGISTER #2	16
15		I-REGISTER I3	MAP REGISTER #1	15
14		I-REGISTER I2	MAP CONTROL #3	14
13		I-REGISTER I1	MAP CONTROL #2	13
12		I-REGISTER I0	MAP CONTROL #1	12
11		ROM 10	SCRATCH PAD (00-07)	11
10		ROM 11	HOLDING REG (00-07)	10
9		ROM 12	CYCLER/ADDER (00-07)	9
8		ROM 13	M0Z REGISTER (00-07)	8
7		ROM 14	0105 REGISTER	7
6		ROM 15	CONTROL LOGIC	6
5		ROM 16	REQ STROBE/ BP	5
4		ROM 17	BRANCH COND #1	4
3	LOCAL CONTROL, CPU 0	ROM 30	BRANCH COND #2	3
2		ROM 31	SPECIAL FUNCTIONS #1	2
1	LOCAL CONTROL, CPU 1	ROM 32	SPECIAL FUNCTIONS #2	1

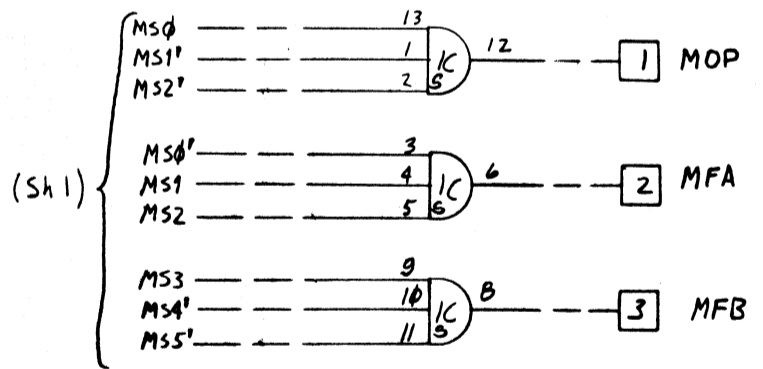
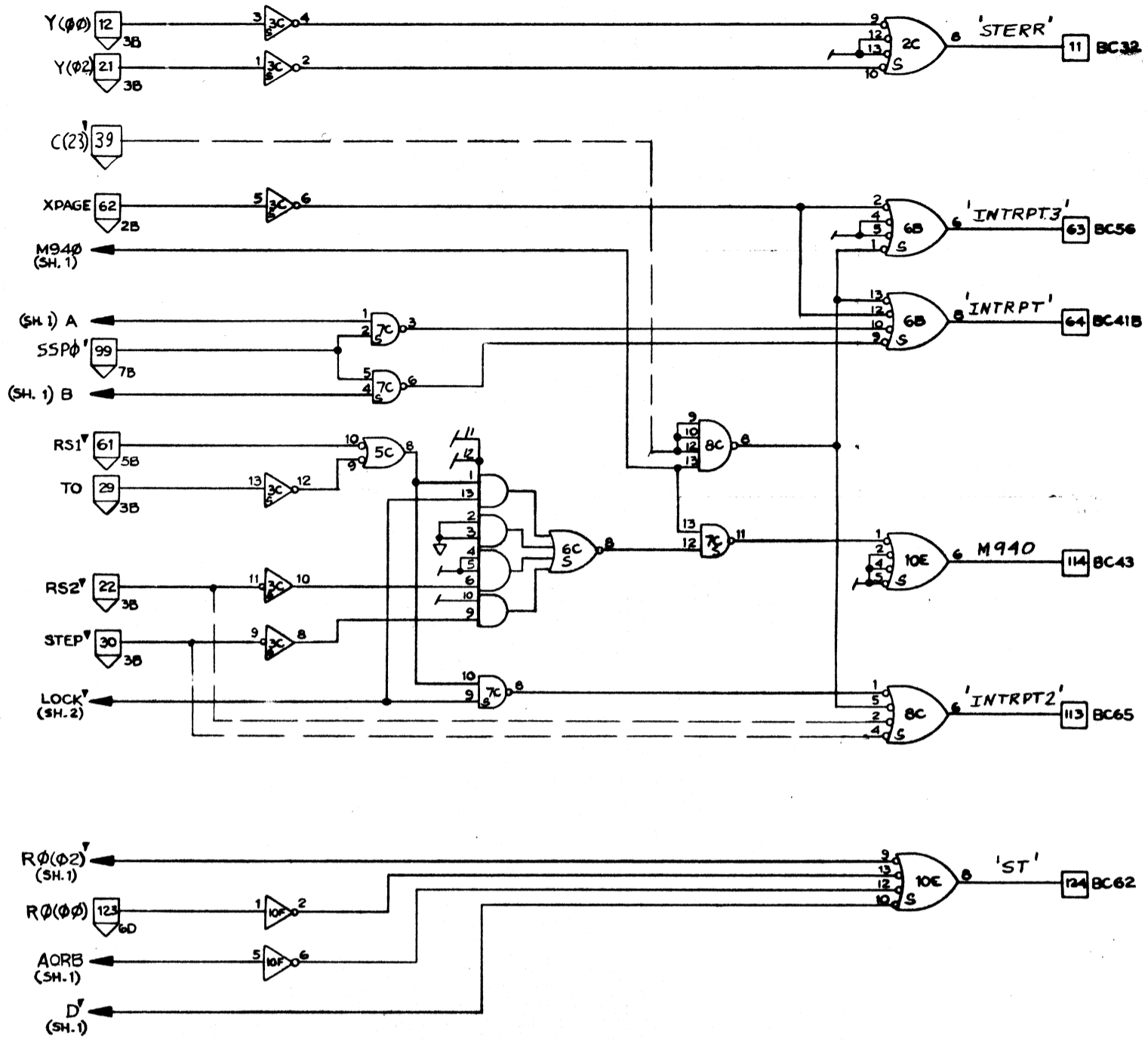
NOTE

CPU 0 IS TOP
CPU 1 IS BOTTOM

L01039.1	DESIGNED	DATE		9/9/74	DRAWN	APPROVED
	DRAWN E. YOSHIOKA	REVISIONS		CPU 1.5 BACK PANEL		
The Aloha System BCC-500	SCALE	SHEET	OF	NO.		

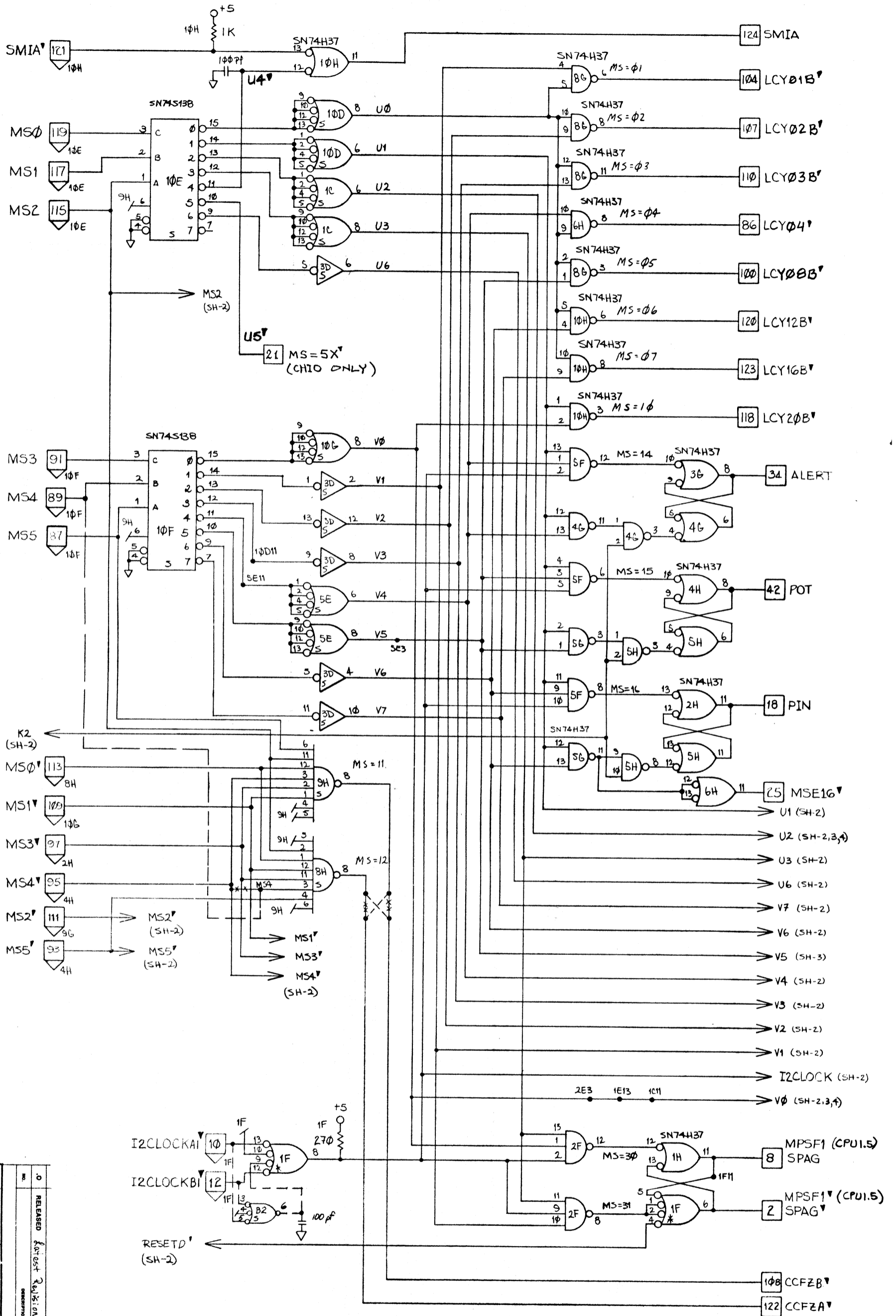


RELEASED DATE: _____ BY: _____	TITLE: SPECIAL FUNCTIONS #2 PART: CPU 4.5 REV: 2 3 L00436, H
REVISIONS NO. _____ DATE _____ BY _____ APPROVED _____	AUTHORITY: _____ APPROVED: _____

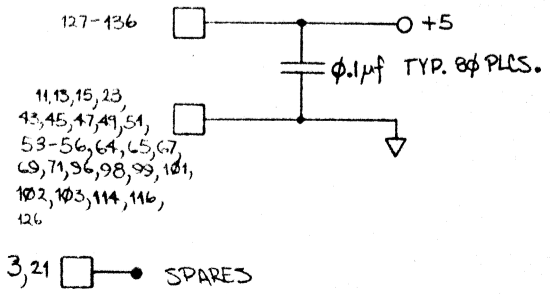


A1

L00436		REVISIONS	
		DATE	APPROVED
DESIGNED BY	DATE	DATE	DATE
NAME: R/Z/T/G	DATE: 2/21/70	DATE:	DATE:
NAME: DON ROBBINS	DATE:	DATE:	DATE:
SPECIAL FUNCTIONS: 2		DATE:	DATE:
FIRST USED ON: M1 CPU 1.5		DATE:	DATE:
REVISION: 3	DATE: 3	DATE:	DATE:
L00436		DATE:	DATE:



NOTES:
 1. UNLESS SPECIFIED:
 ALL RESISTORS ARE 1/8 W. 10% CARB. COMP.
 ALL CAPACITORS ARE CD10070
 2.



The Alpha System BCC-500

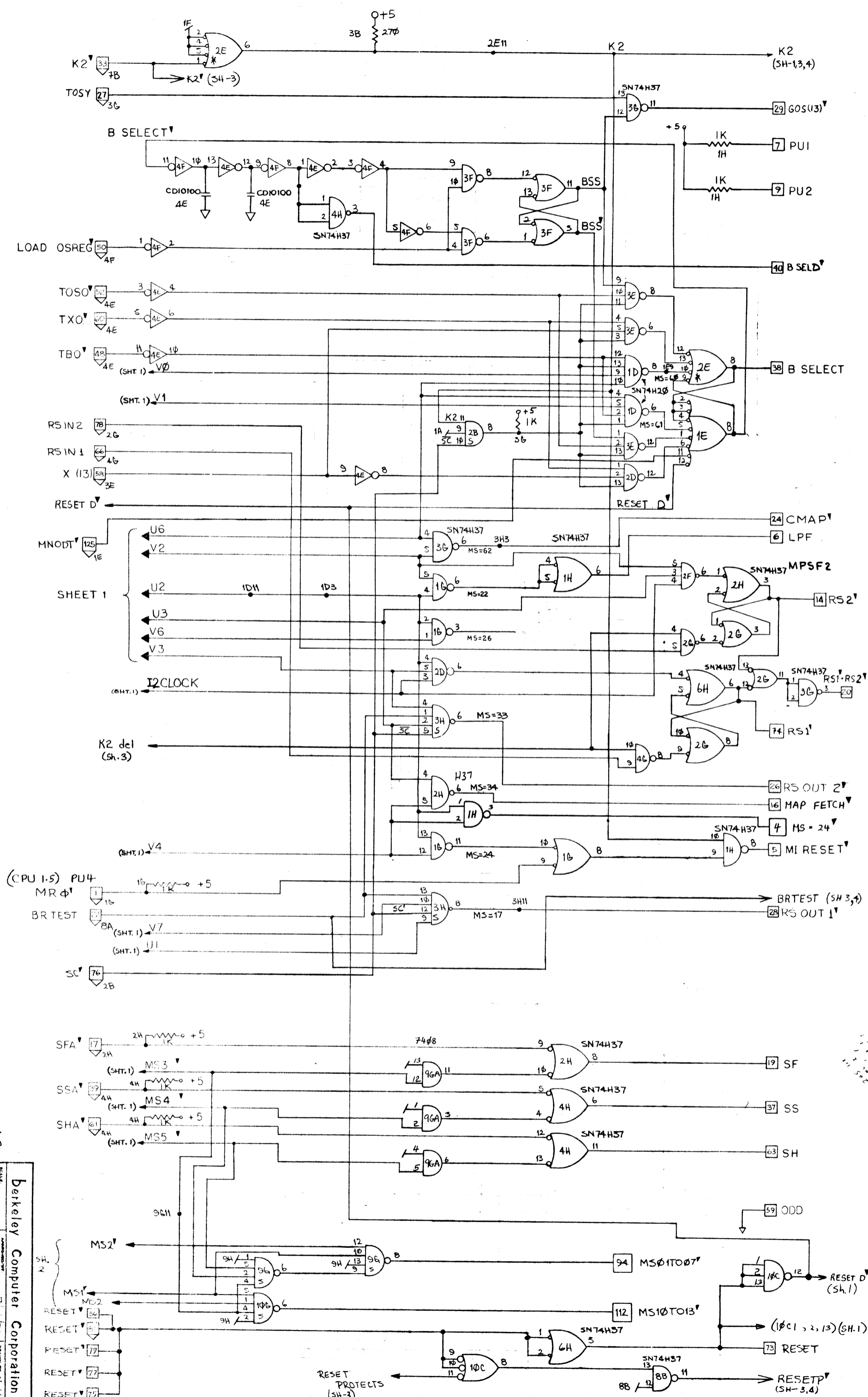
DESIGNED BY: A.B. GOODRICH
 DRAWN BY: E. ELKHA
 CHECKED BY: [Signature]
 PROJECT: MICROPROCESSOR
 SHEET: 1 OF 4
 NO. L00242.4

SPECIAL FUNCTIONS #1

DATE: [Blank]
 DRAWN: [Blank]
 APPROVED: [Blank]

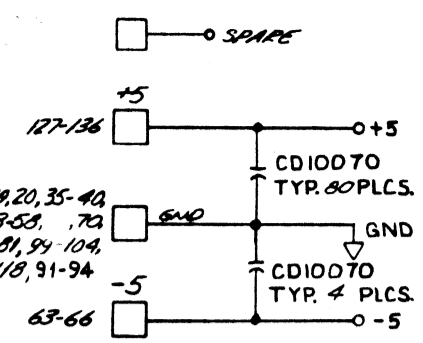
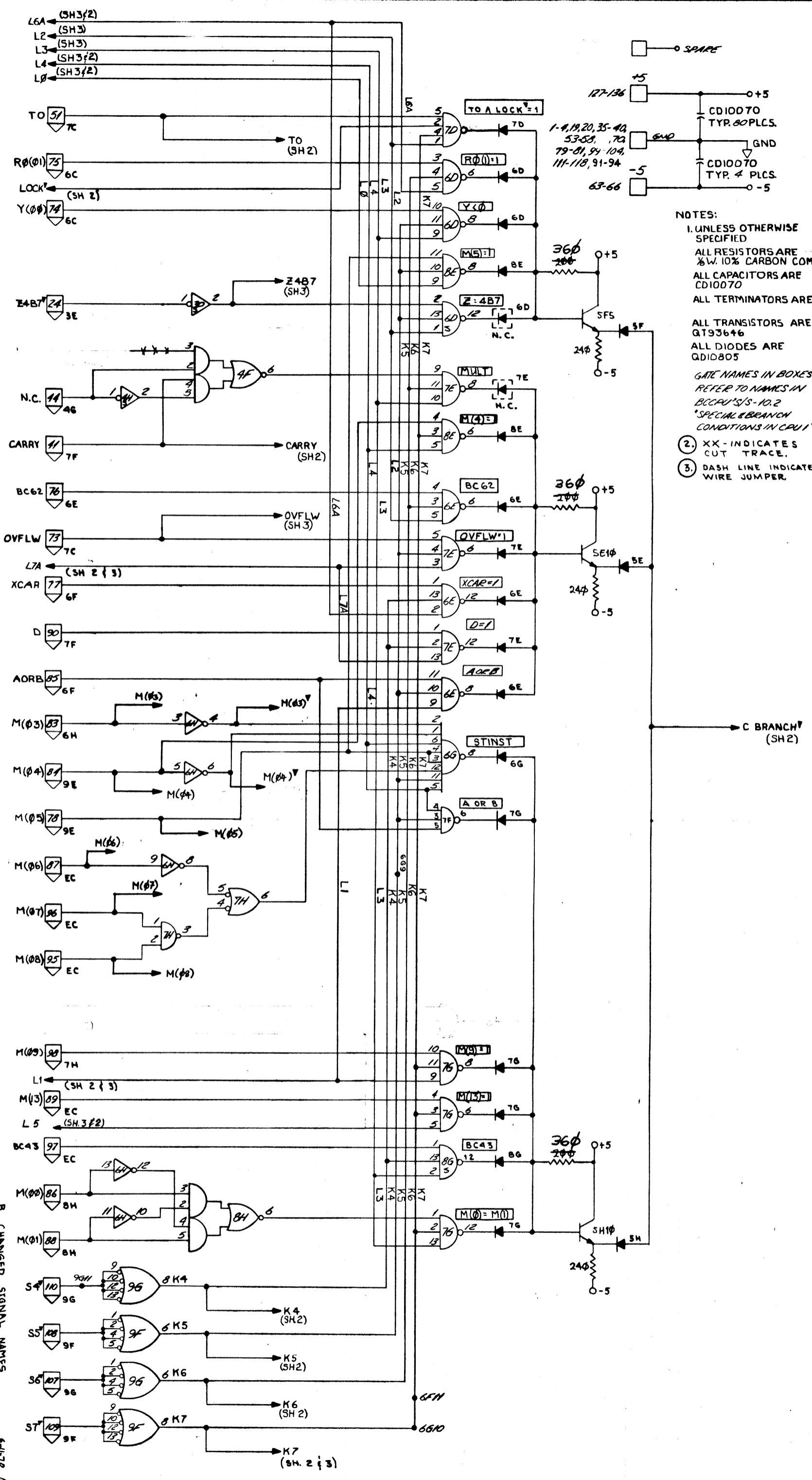
NO.	DESCRIPTION	DATE	DRAWN	APPROVED
0	RELEASED Latest Revisions 7/14/74			
REVISIONS				

A2



Berkeley Computer Corporation
 SPECIAL FUNCTIONS #1
 DATE: 7/15/74
 DRAWN BY: J. J. J.
 CHECKED BY: J. J. J.
 MICROPROCESSOR
 47 L00292.4
 SH 2 OF 4

A2



NOTES:

- UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W. 10% CARBON COMP.
ALL CAPACITORS ARE CD10070
ALL TERMINATORS ARE
- ALL TRANSISTORS ARE QT93646
ALL DIODES ARE QD10805
- GATE NAMES IN BOXES REFER TO NAMES IN BCCPU'S/S-10.2 "SPECIAL BRANCH CONDITIONS IN CPU 1"
- XX - INDICATES CUT TRACE.
- DASH LINE INDICATES WIRE JUMPER.

A3

L000435

0 RELEASED

B CHANGED SIGNAL NAMES

6-11-70 MM

REVISIONS

DATE

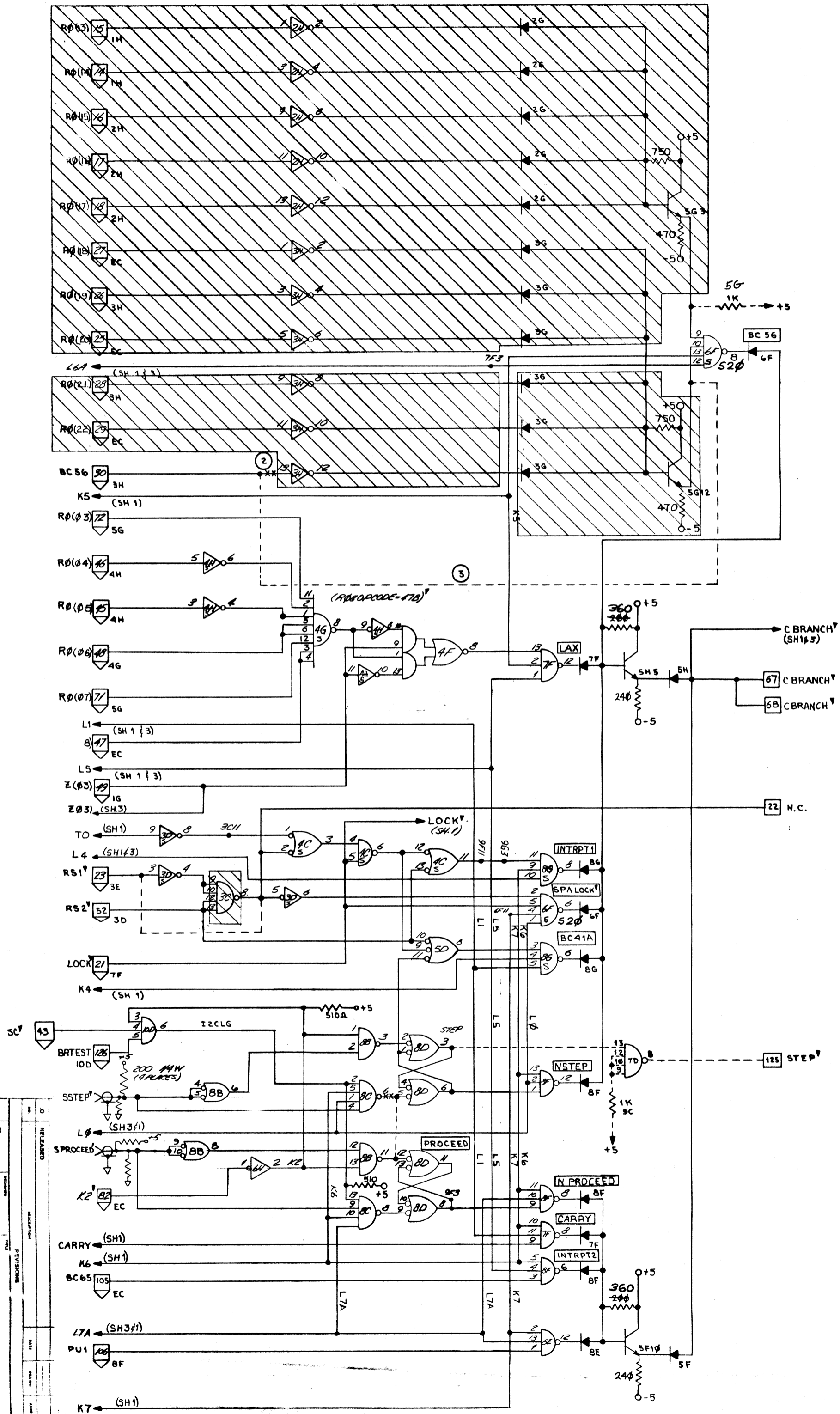
BY

APPROVED

BRANCH CONDITIONS *2

FIRST USED ON M1 CPU-15

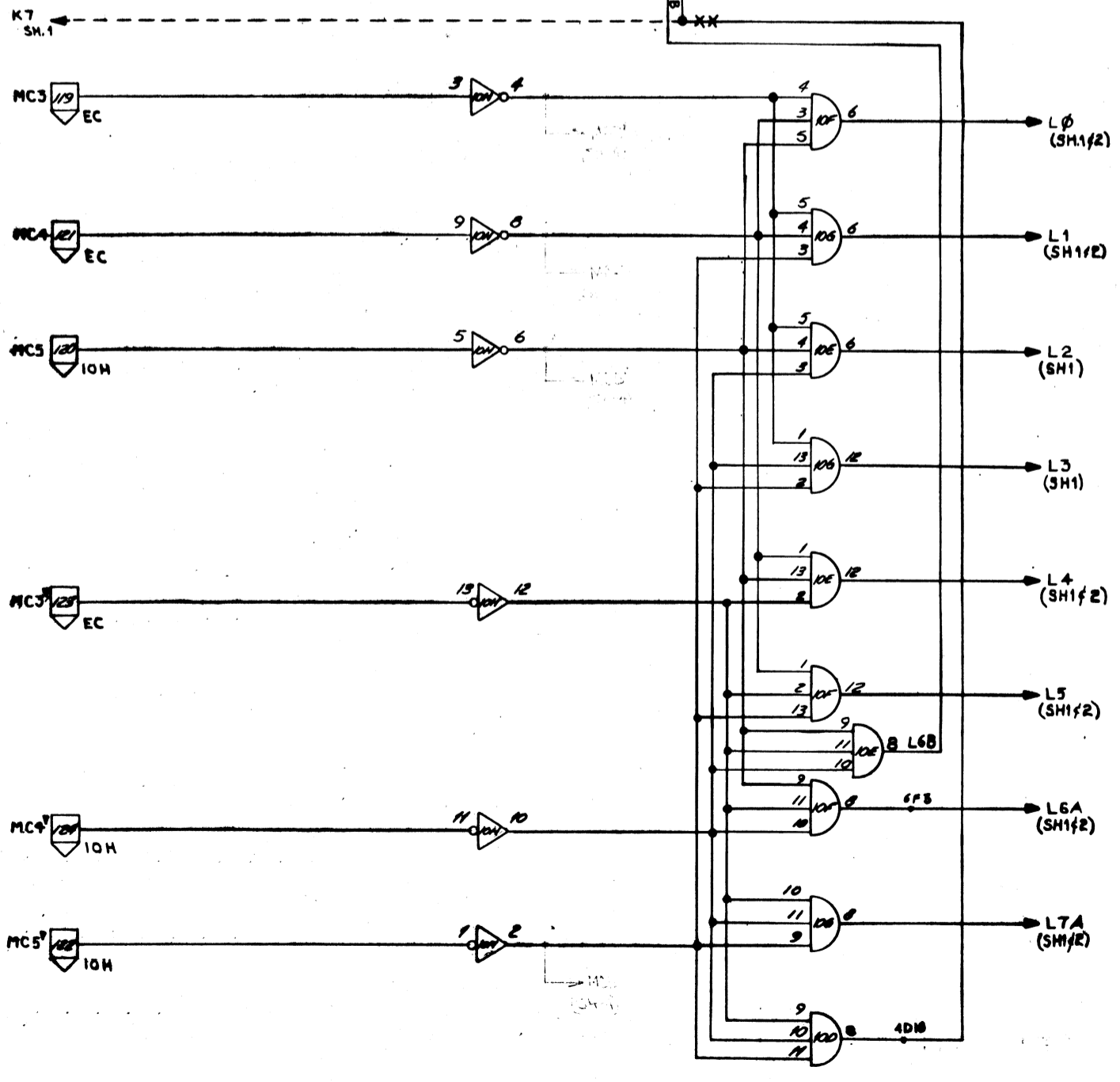
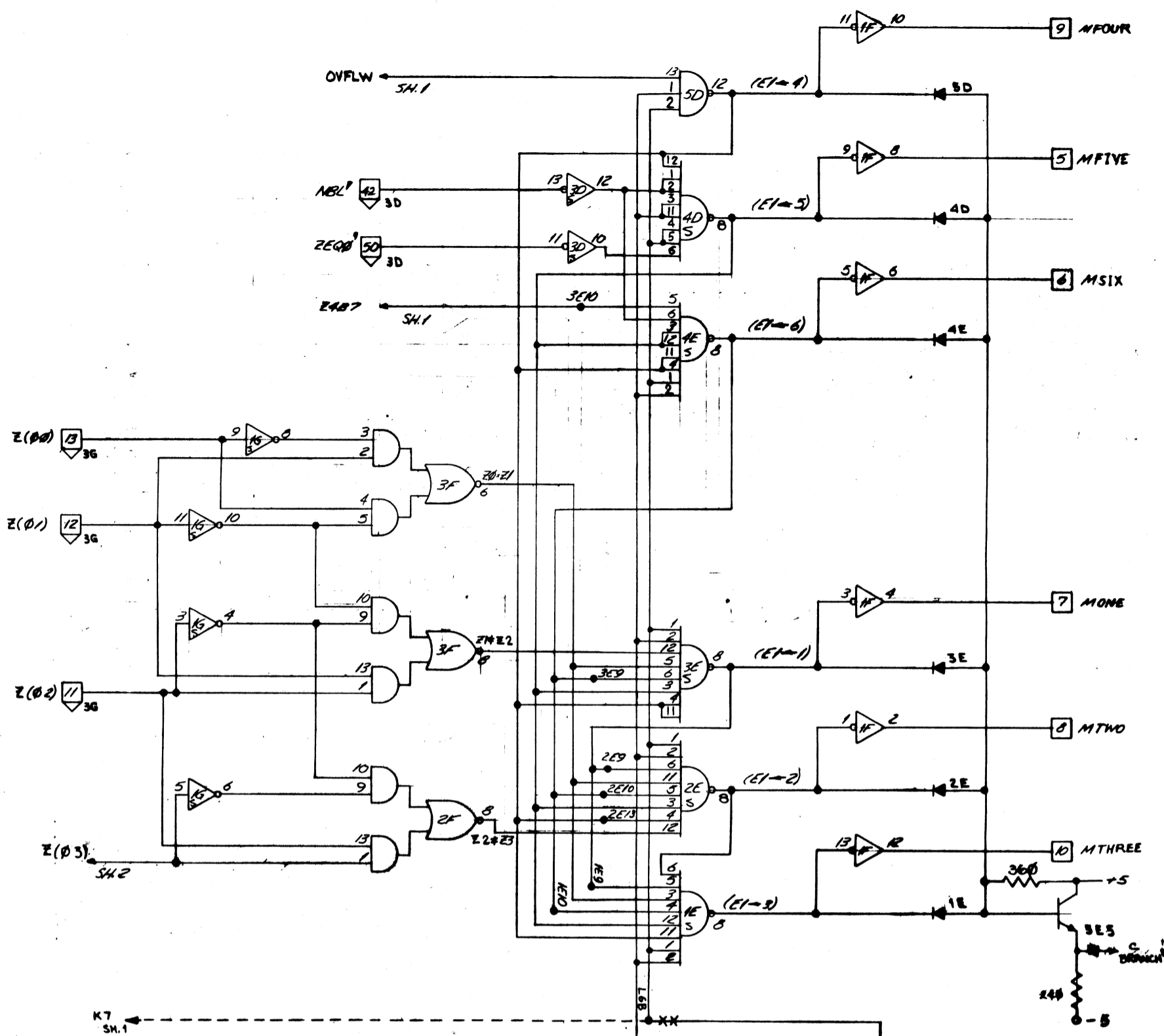
1 3 L00435 .9E



L00435
 RELEASED
 CPU BRANCH CONDITIONS #2
 FIRST USED ON M1 CPU-1.5
 L00435

REV	DATE	DESCRIPTION
1		
2		
3		

CPU BRANCH CONDITIONS #2
 L00435



A3

L00435

Computer Corporation

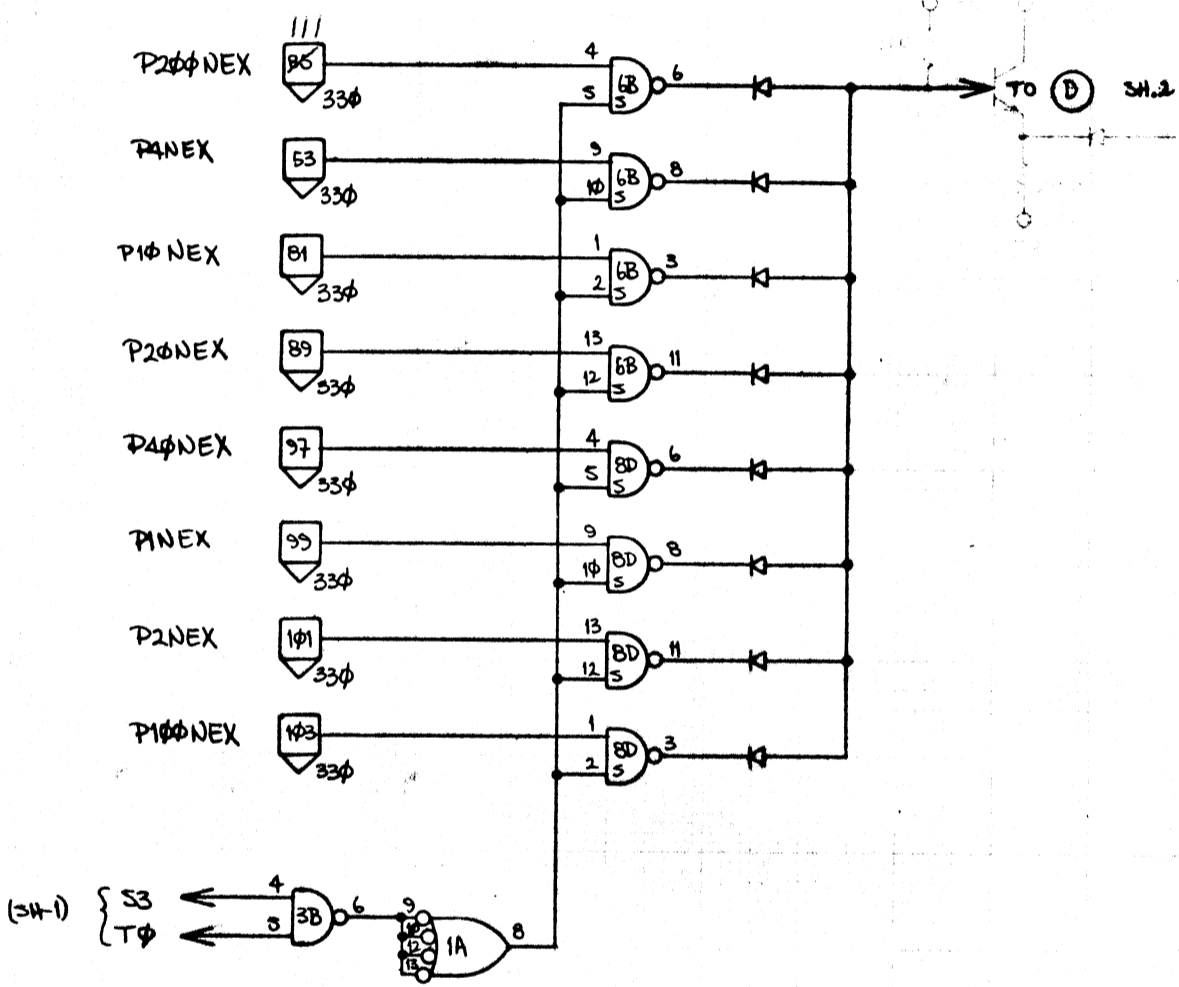
BRANCH CONDITIONS 2

FIRST USED ON M1 CPU-15

3 3 L00435

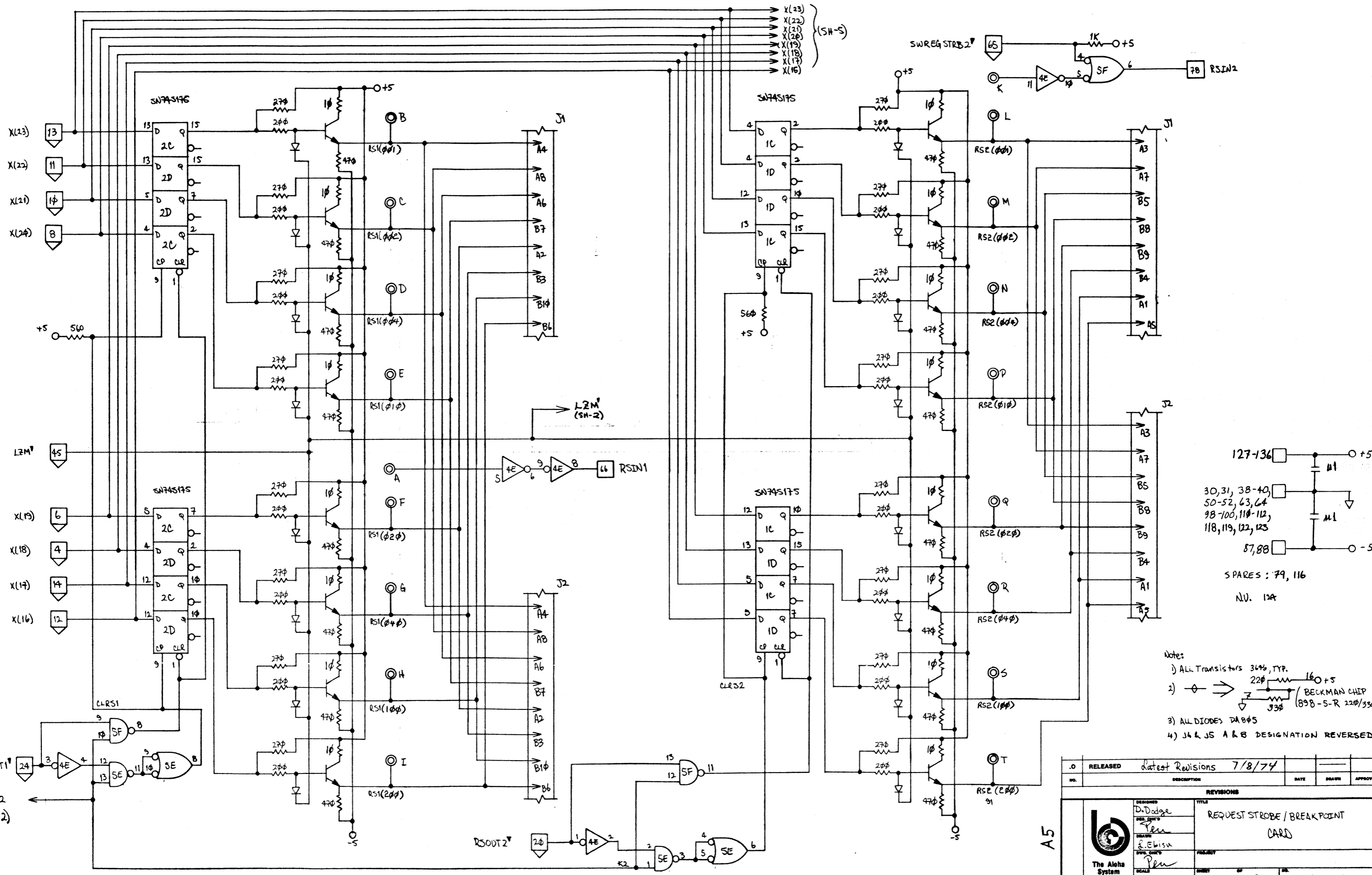
0	RELEASED	LATEST REVISIONS	12/8/74
1			
2			
3			

A3



A4

0		RELEASED
DATE		
BY		
REVISIONS		
REV	DATE	DESCRIPTION
3	5	CPU ILS
		D. Dodge R. E. S. A. BRANCH CONDITIONS #1
3 5 L00437		



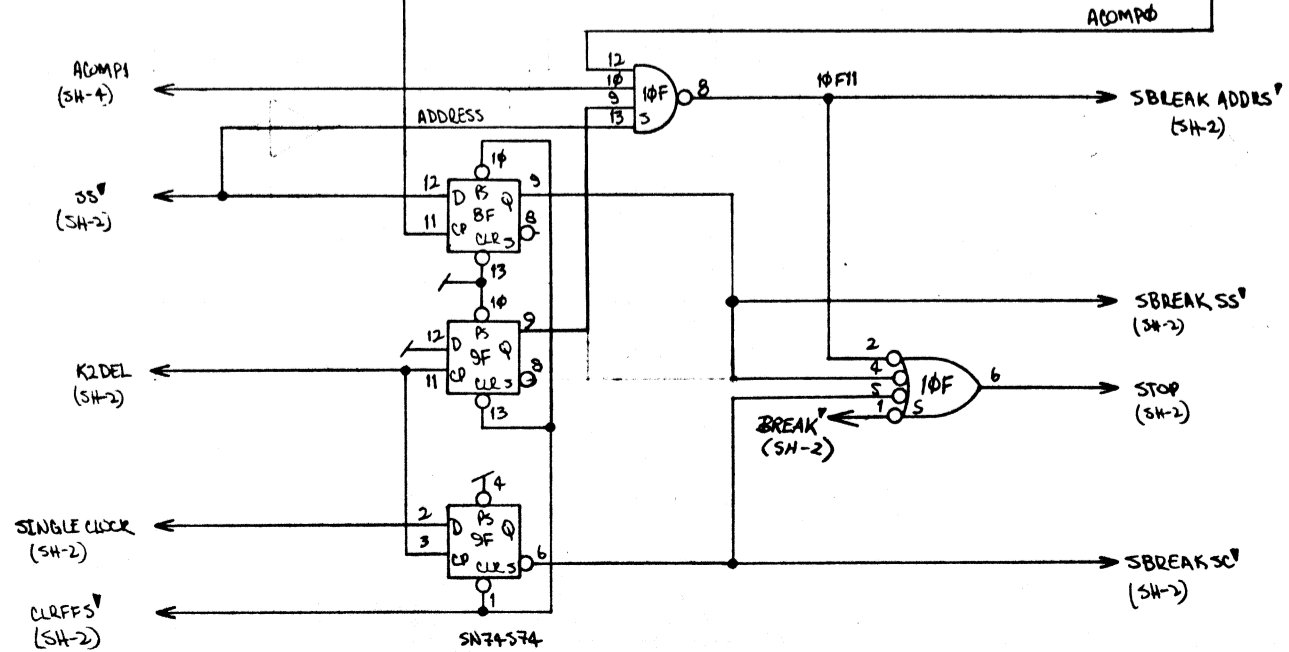
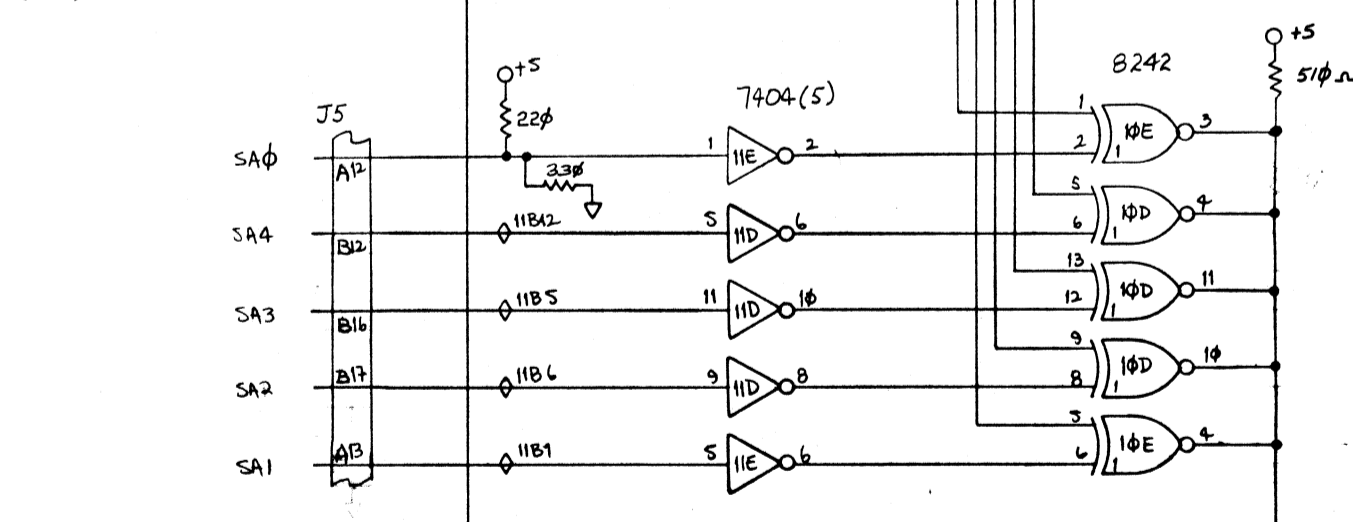
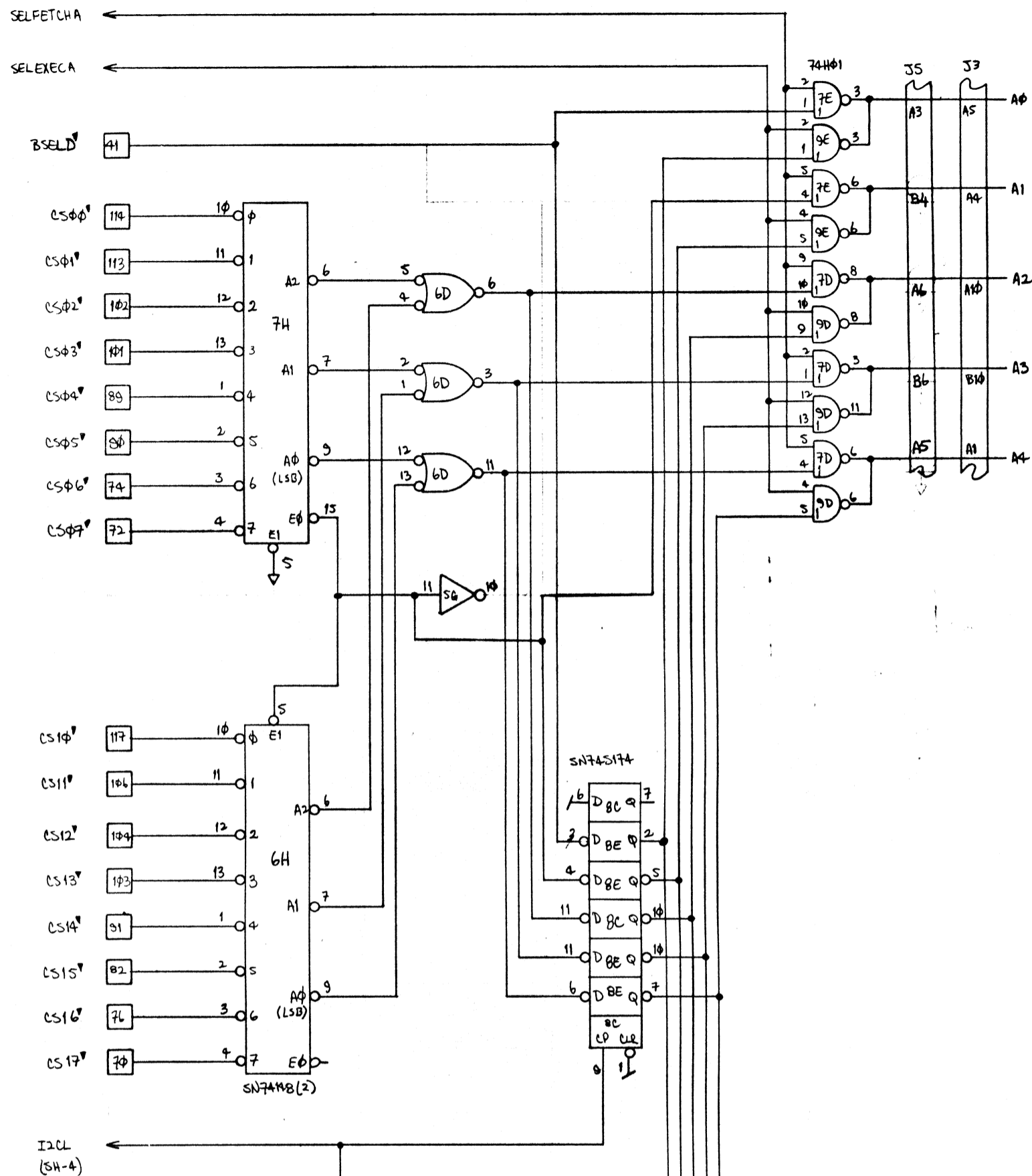
127-136 □ — +5
 30, 31, 38-40, □
 50-52, 63, 64 □
 98-100, 110-112, □
 118, 119, 122, 123 □
 87, 88 □ — -5

SPARES: 79, 116
 N.Y. 12A

- Note:
- 1) ALL TRANSISTORS 36%, TYP.
 - 2) $\phi \rightarrow$ $\begin{matrix} 22\phi & \text{---} & 160 + 5 \\ \text{---} & \text{---} & \text{---} \\ 7 & \text{---} & 33\phi \end{matrix}$ (BECKMAN CHIP 89B-5-R 220/330)
 - 3) ALL DIODES DA805
 - 4) J4 & J5 A & B DESIGNATION REVERSED.

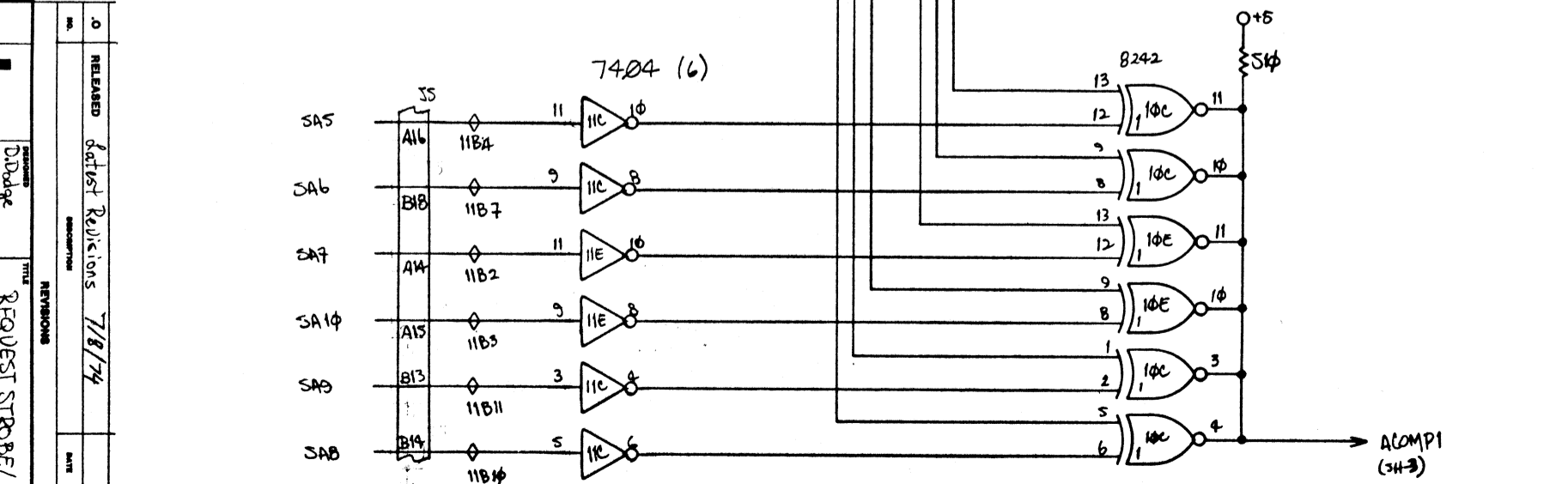
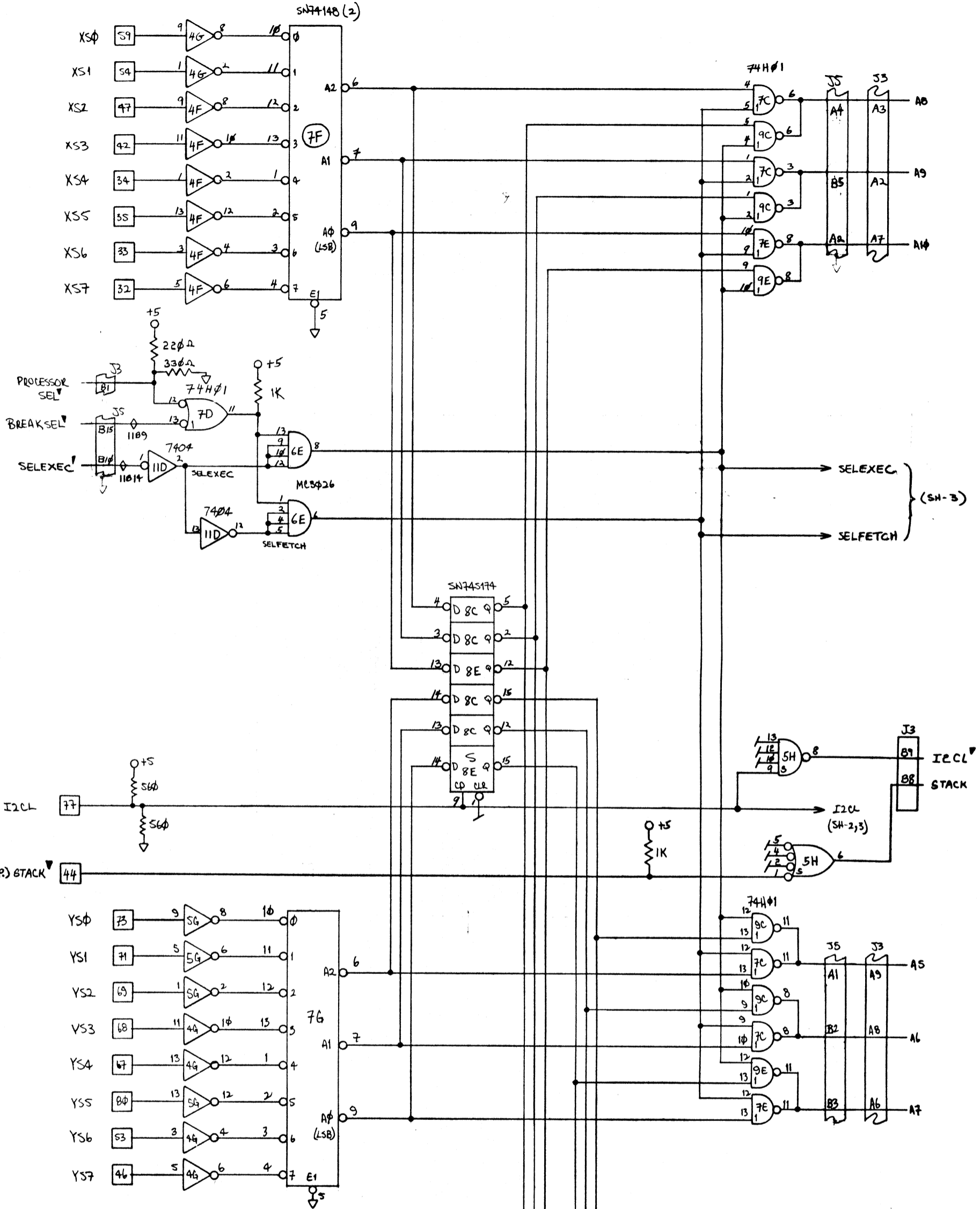
.0	RELEASED	Latest Revisions	7/8/74		
NO.		DESCRIPTION	DATE	DRAWN	APPROVED
REVISIONS					
DESIGNED		TITLE			
D. Dodge		REQUEST STROBE/BREAKPOINT CARD			
DRAWN		PROJECT			
E. Elvish					
CHECKED		SHEET			
P. Pen		1 OF 5			
SCALE		Lφ1066.1			

A5



A5

	RELEASED Request Revisions 7/8/74
D. Dodge R. E. BISHA	TITLE REQUEST STROBE/ BREAKPOINT CARD
3 5	DATE L01/066.1



A5

The Alpha System BCC-500

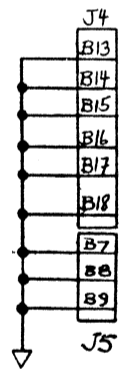
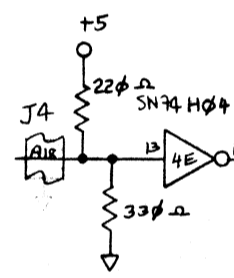
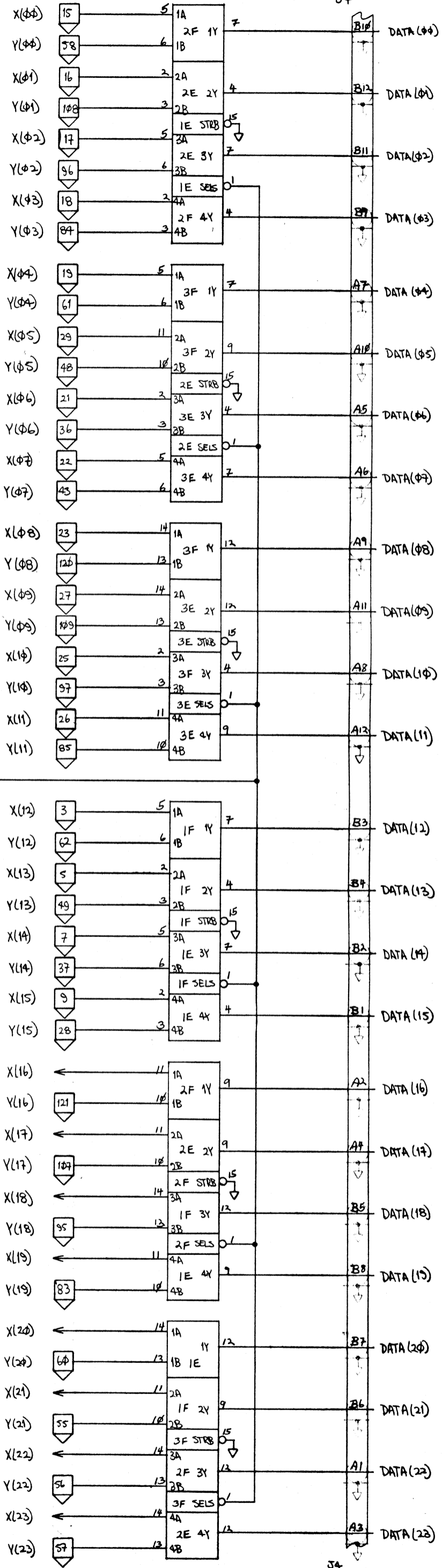
RELEASED
 Latest Revisions 7/8/74

REQUEST STROBE/
 BREAKPOINT
 CARD

4 5
 LP/1066.1

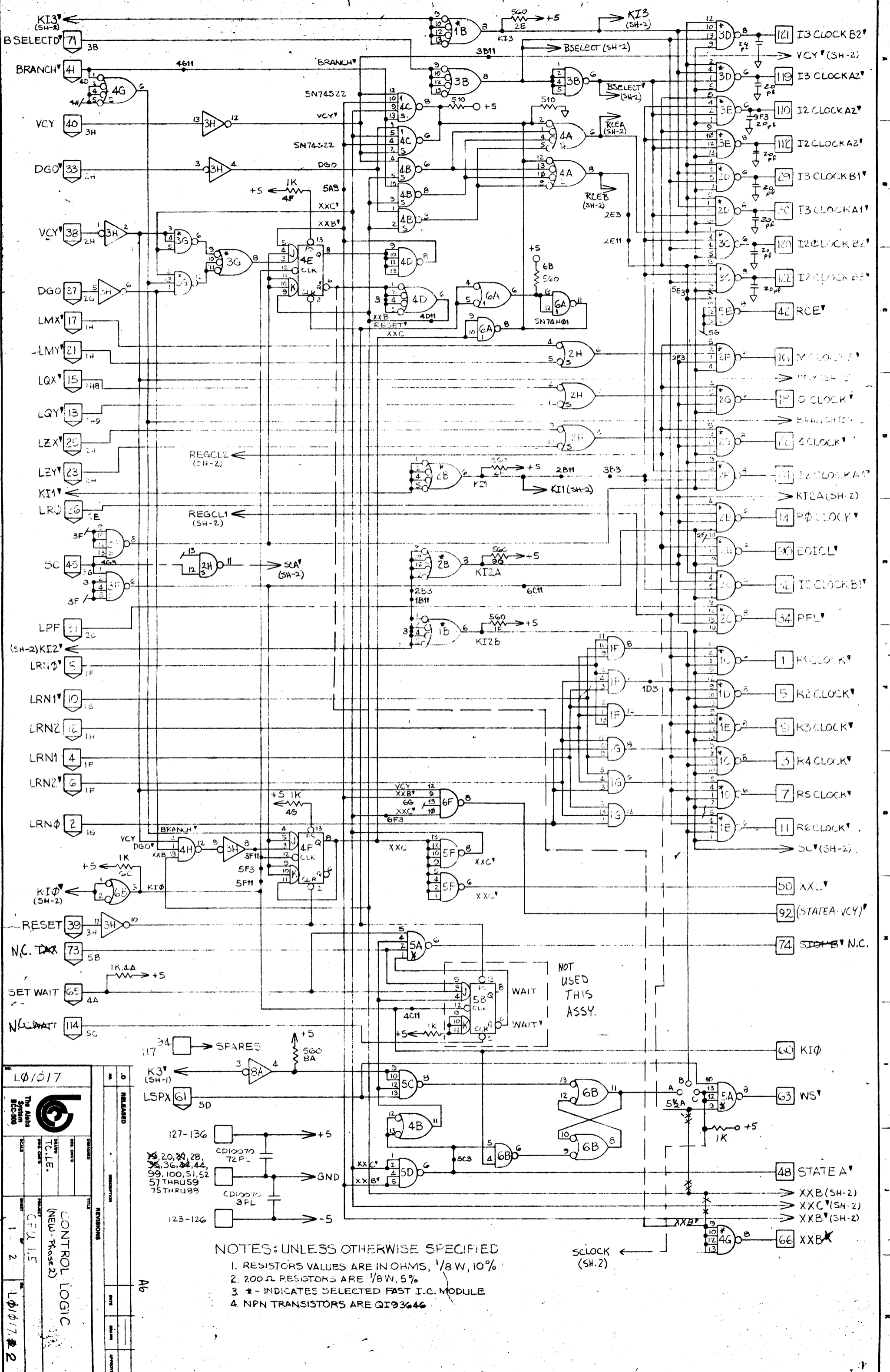
3N74157

J4



A5

		RELEASED <i>K-test Revisions</i> 7/8/74	
D. D. Duke & E. E. E. E.	TITLE REQUEST STROBE/BREAK POINT CAED	DATE 5 5	APPROVED Lp/066.1

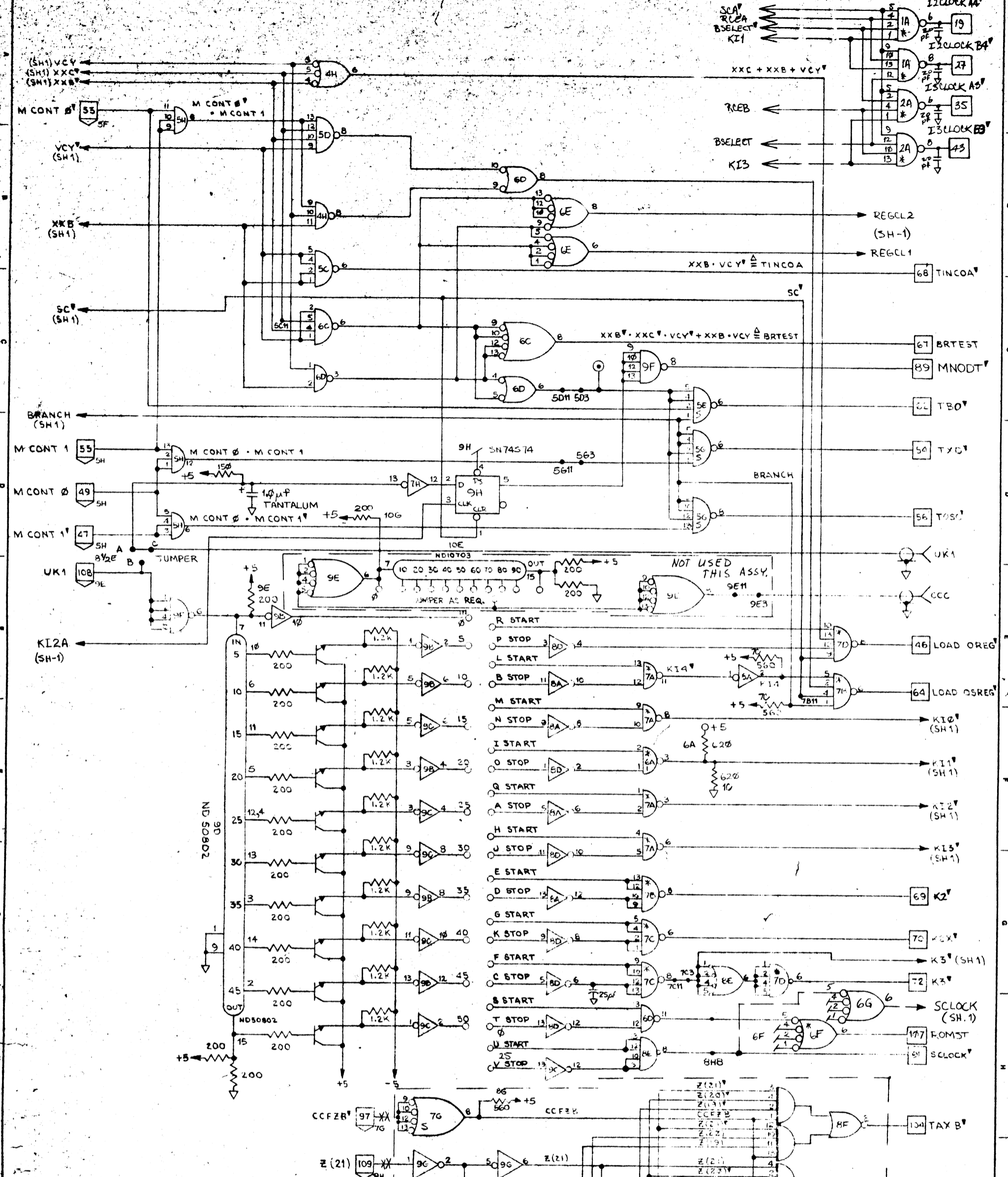


L01017	
THE ALBION SYSTEM BCC-500	
SCALE	REVISIONS
DATE	NO.
DESCRIPTION	DATE
DESIGNED BY	APPROVED BY
CHECKED BY	
DATE	
CONTROL LOGIC (NEW - Phase 2)	
REVISED	DATE
1	
2	
L01017-2	

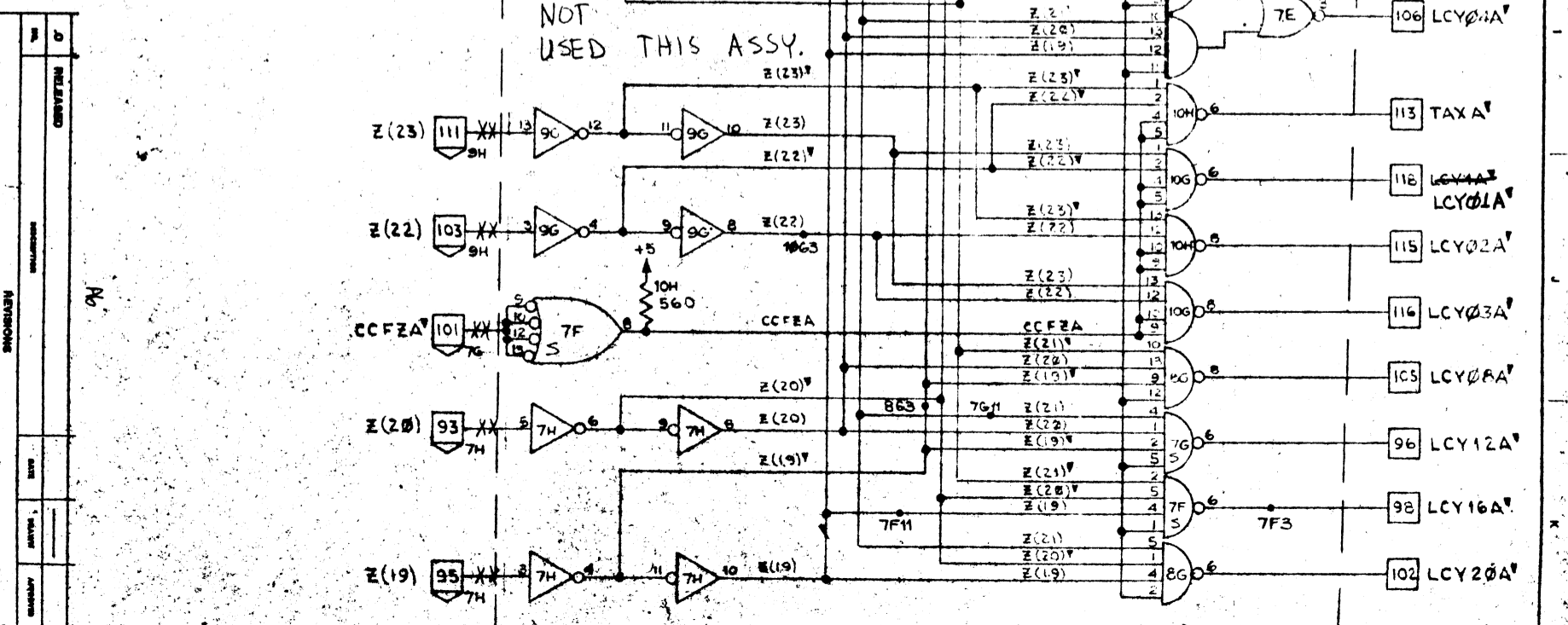
127-136	CD10070 72 PL	+5
20, 24, 28, 36, 44, 99, 100, 51, 52, 57 THRU 59, 75 THRU 89	CD10070 3 PL	GND
123-126		-5

NOTES: UNLESS OTHERWISE SPECIFIED
 1. RESISTORS VALUES ARE IN OHMS, 1/8 W, 10%
 2. 200Ω RESISTORS ARE 1/8 W, 5%
 3. * - INDICATES SELECTED FAST I.C. MODULE
 4. NPN TRANSISTORS ARE Q193646

SCLOCK (SH.2)

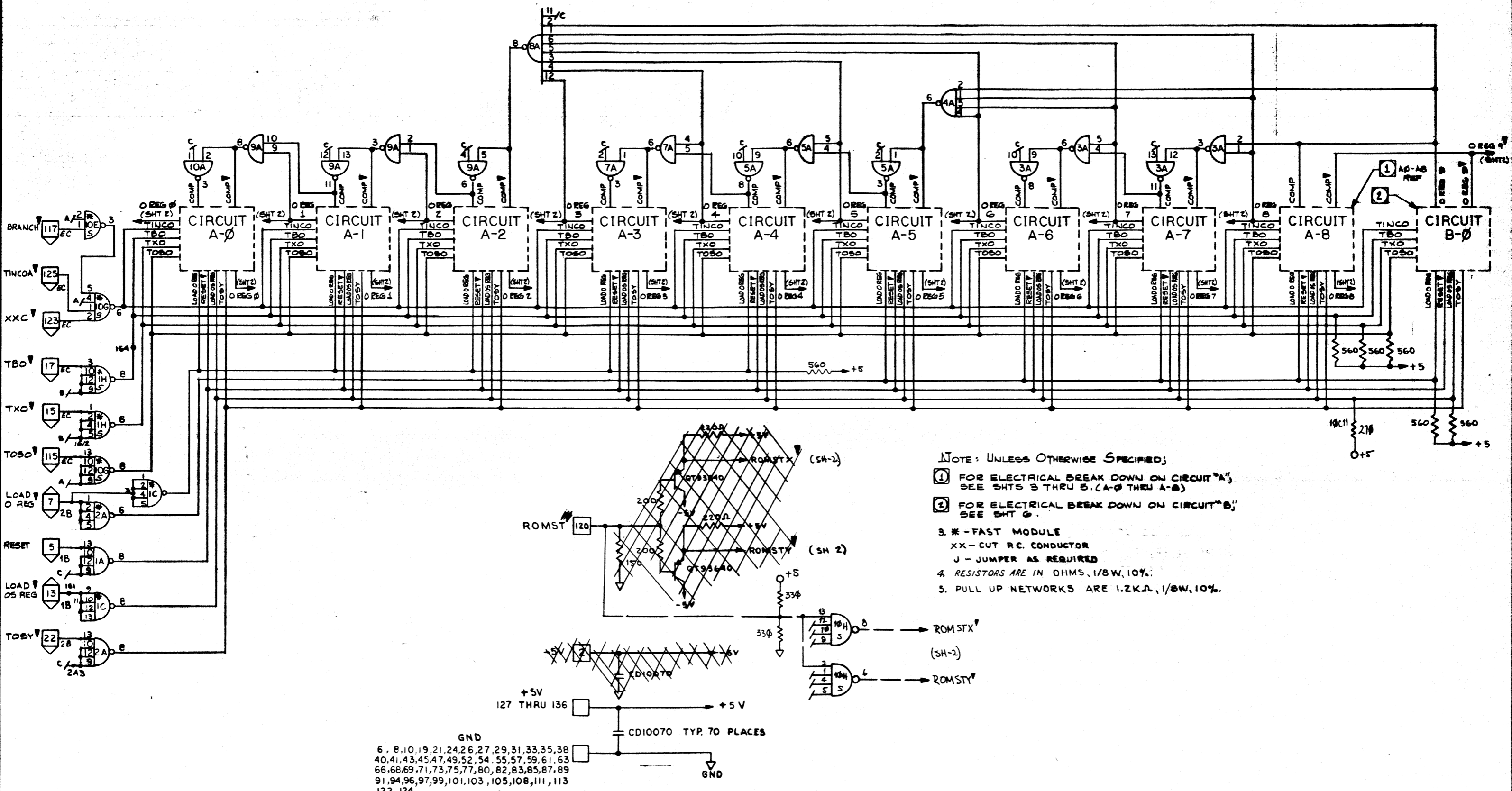


L01017	
CONTROL LOGIC (NEW-Phase 2) CPU 15	
2	2
L01017#2	



NOT USED THIS ASSY.

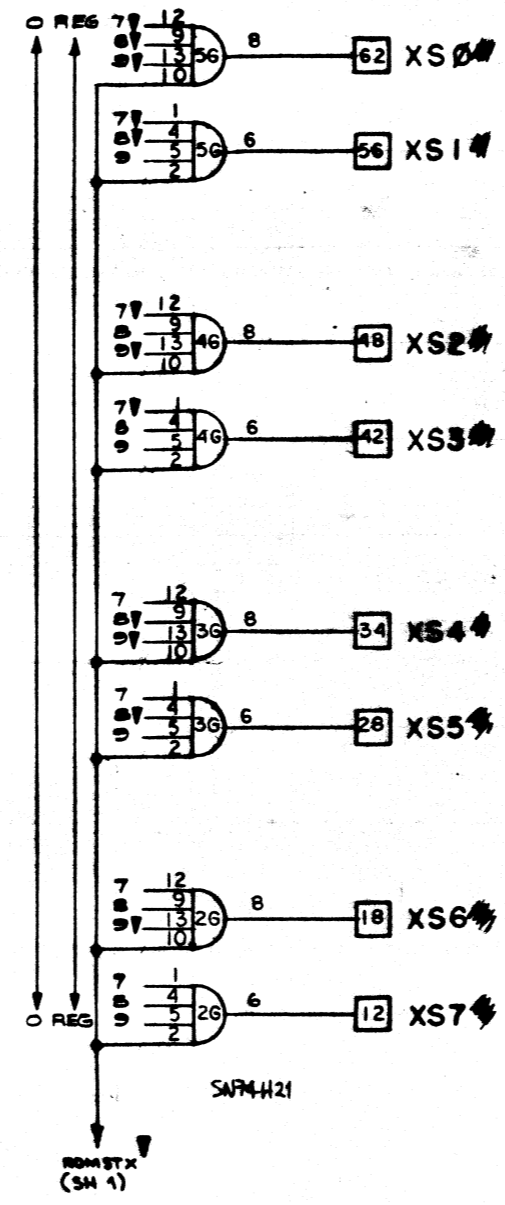
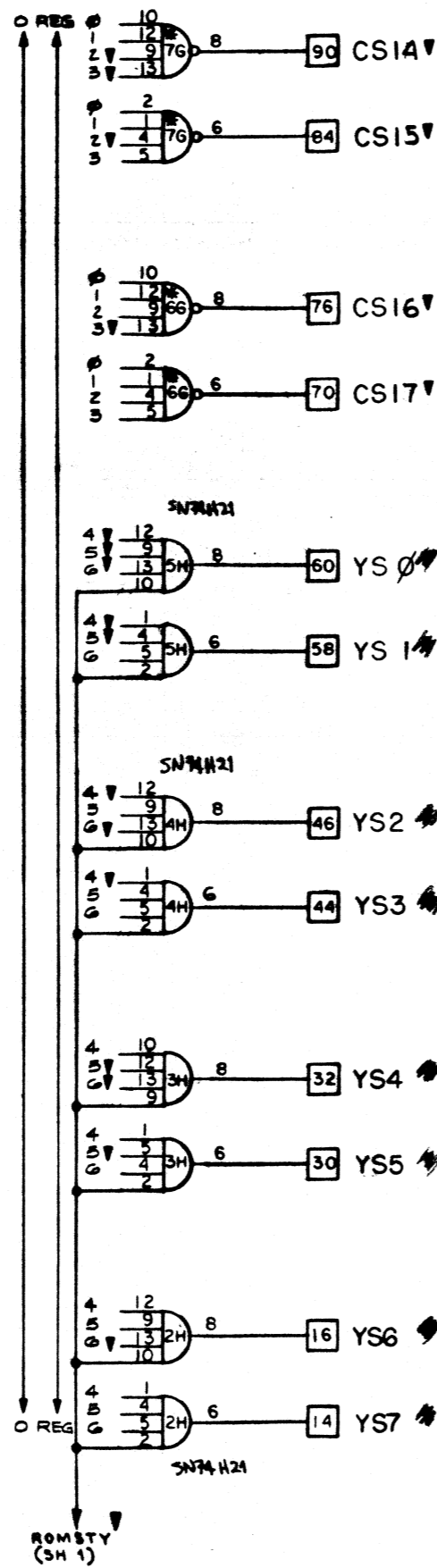
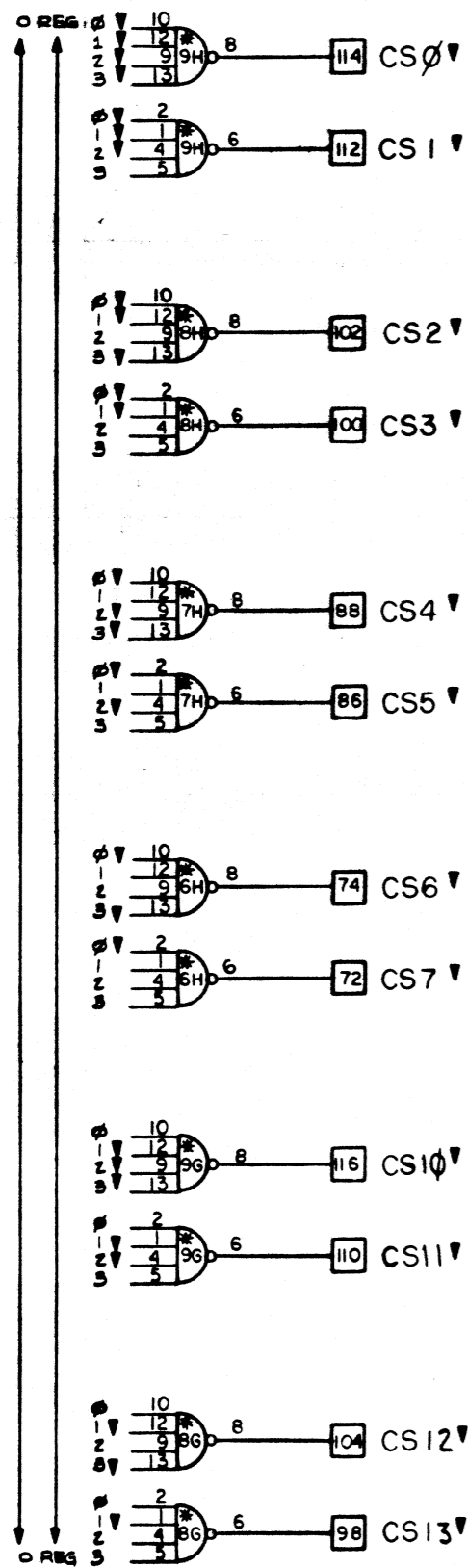
NOT USED THIS ASSY.



- NOTE: UNLESS OTHERWISE SPECIFIED;
- ① FOR ELECTRICAL BREAK DOWN ON CIRCUIT "A", SEE SHTS 3 THRU 5. (A-0 THRU A-8)
 - ② FOR ELECTRICAL BREAK DOWN ON CIRCUIT "B", SEE SHT 6.
 - 3. * - FAST MODULE
 - XX - CUT R.C. CONDUCTOR
 - J - JUMPER AS REQUIRED
 - 4. RESISTORS ARE IN OHMS, 1/8W, 10%.
 - 5. PULL UP NETWORKS ARE 1.2K Ω , 1/8W, 10%.

A7

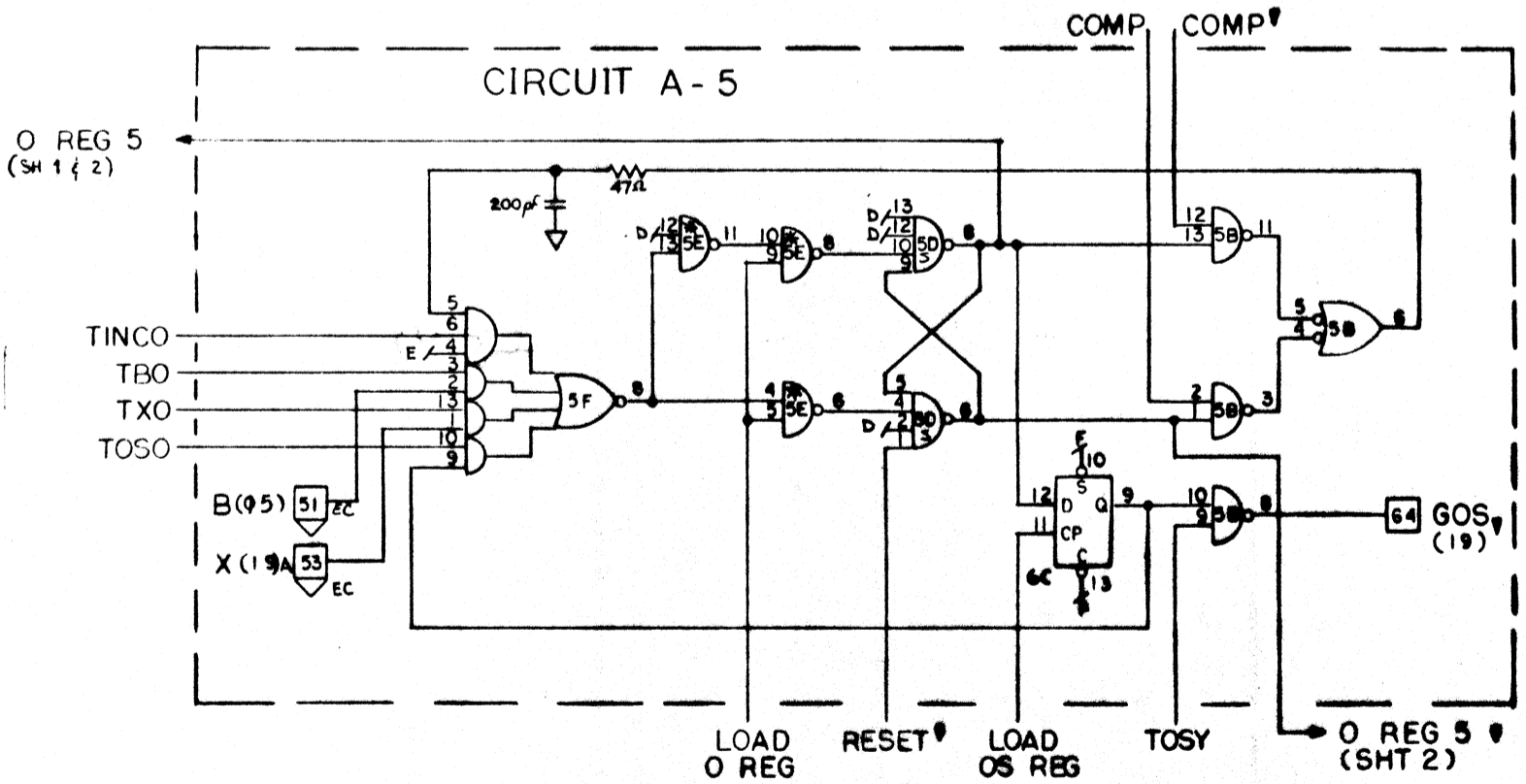
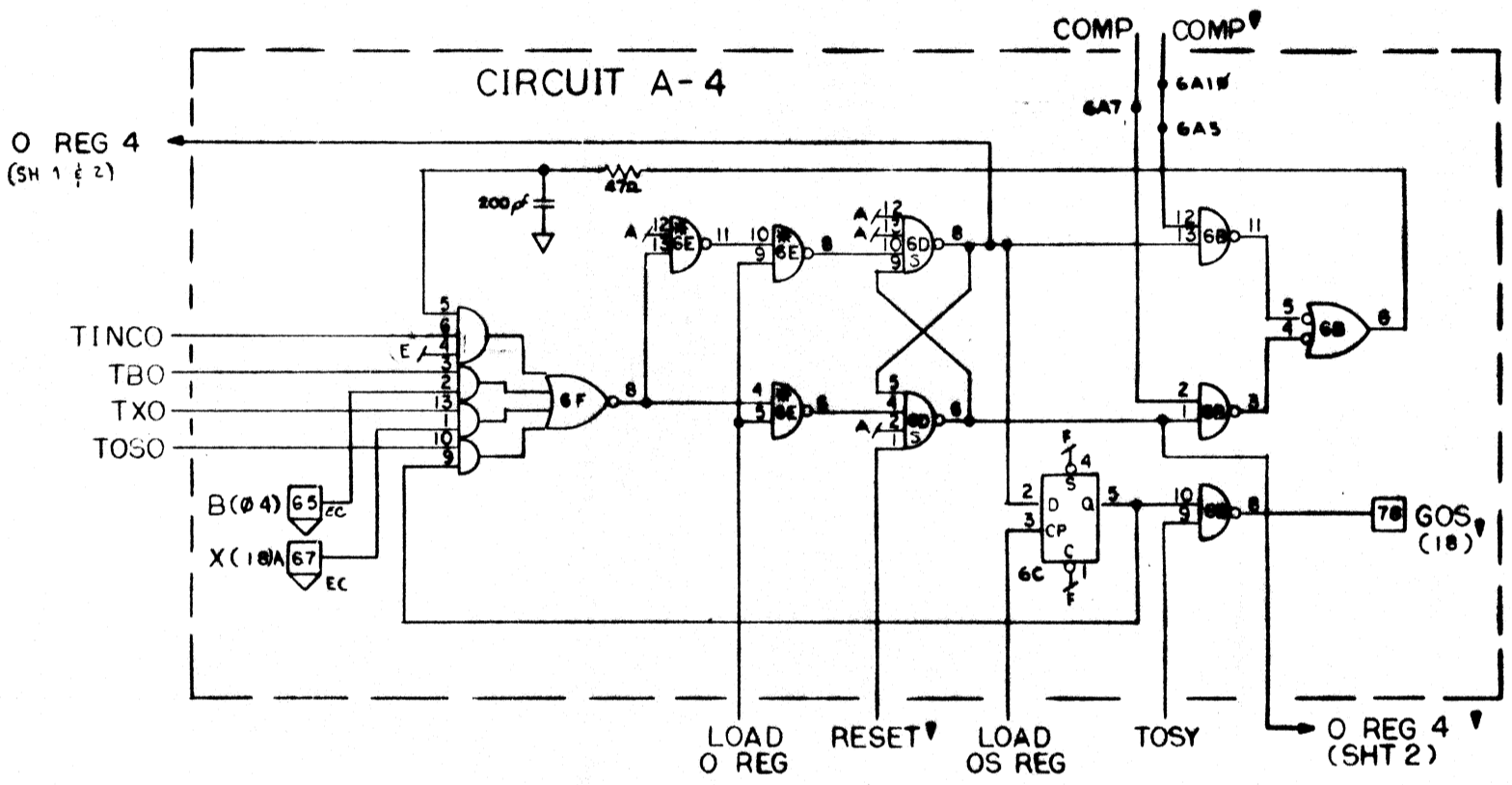
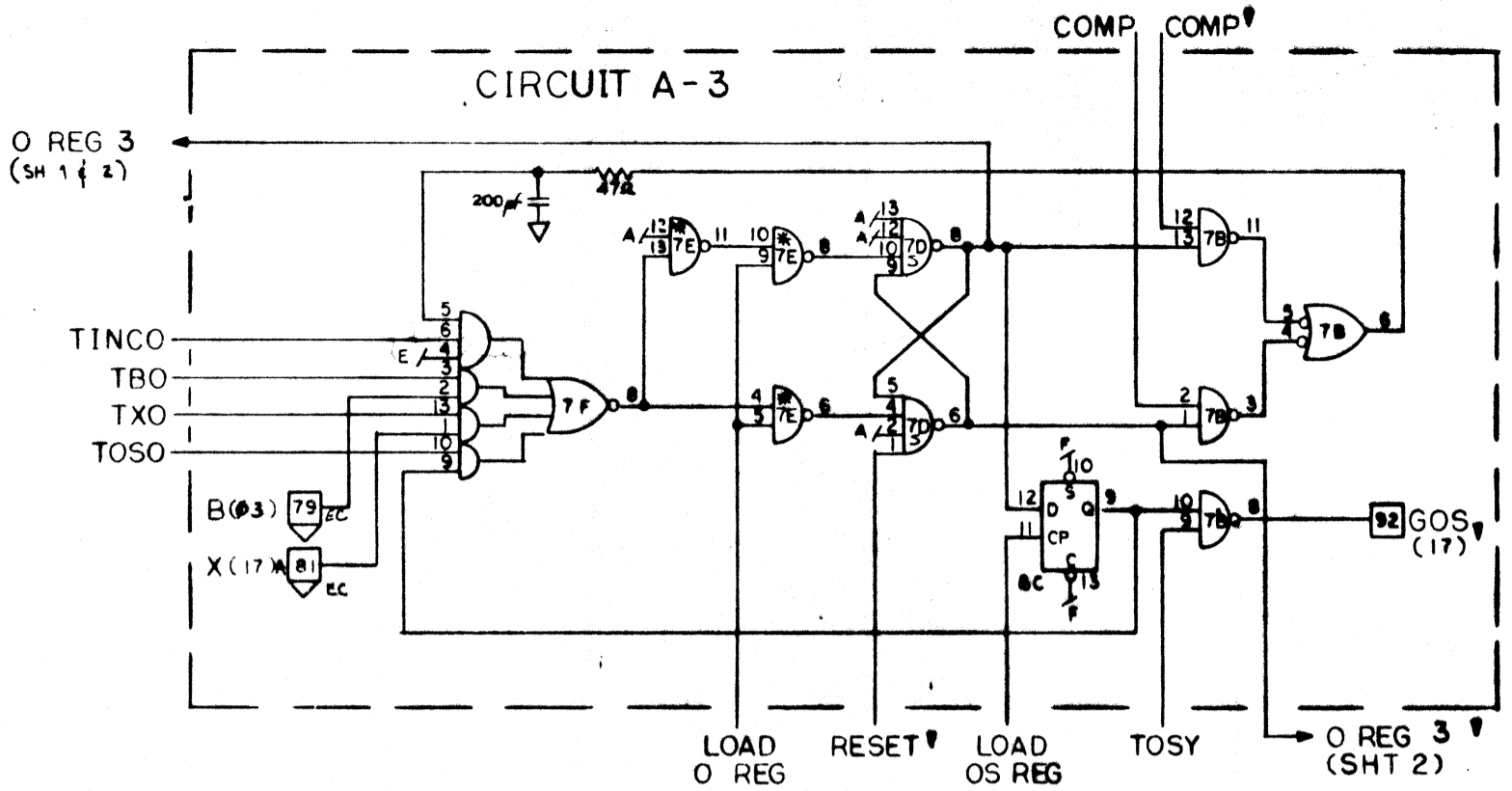
Berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: P. B. M.
DATE:	REVISION:	
TITLE: 0 & OS REGISTER		
PROJECT: FIRST DESIGN DCC & MS CPU.5	DRAWING NUMBER: L00245.4	



A7

berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: <i>REB</i>
DATE:		REVISED:
TITLE: O & OS REGISTER		
PROJECT: FIRST USED ON DCC & MICROLE		DRAWING NUMBER L00245.1

SH 2 OF 6



Berkeley Computer Corporation

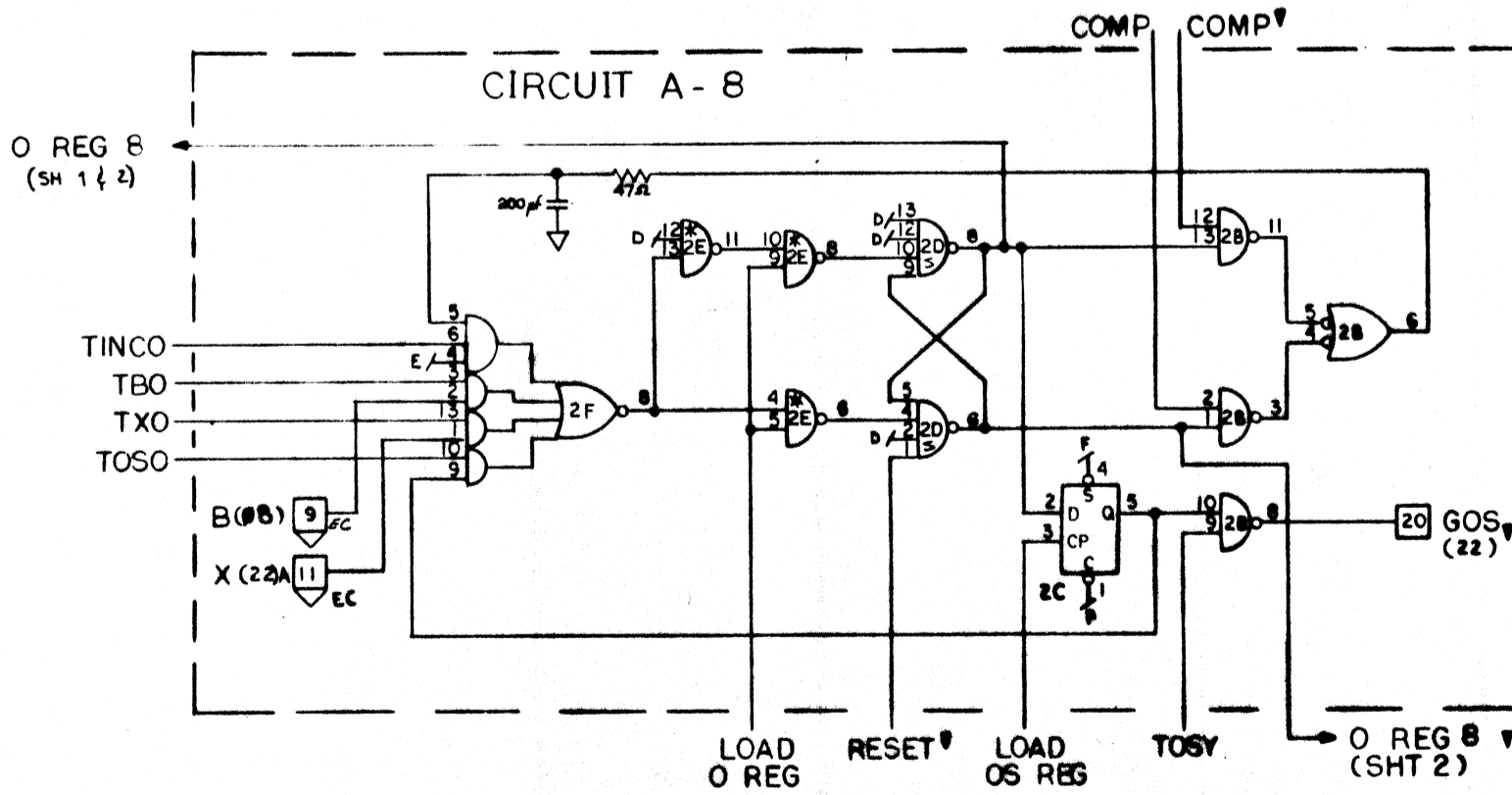
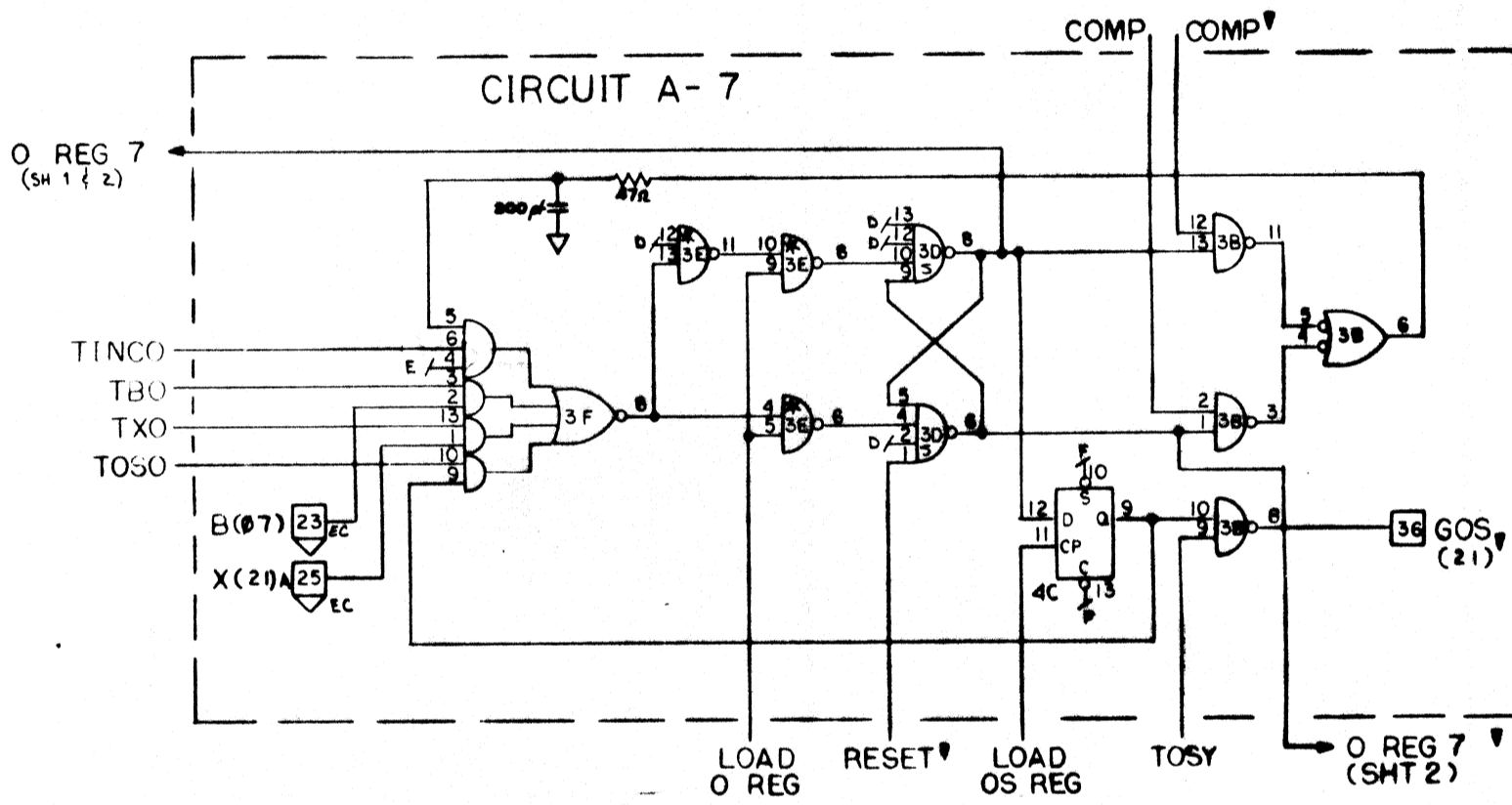
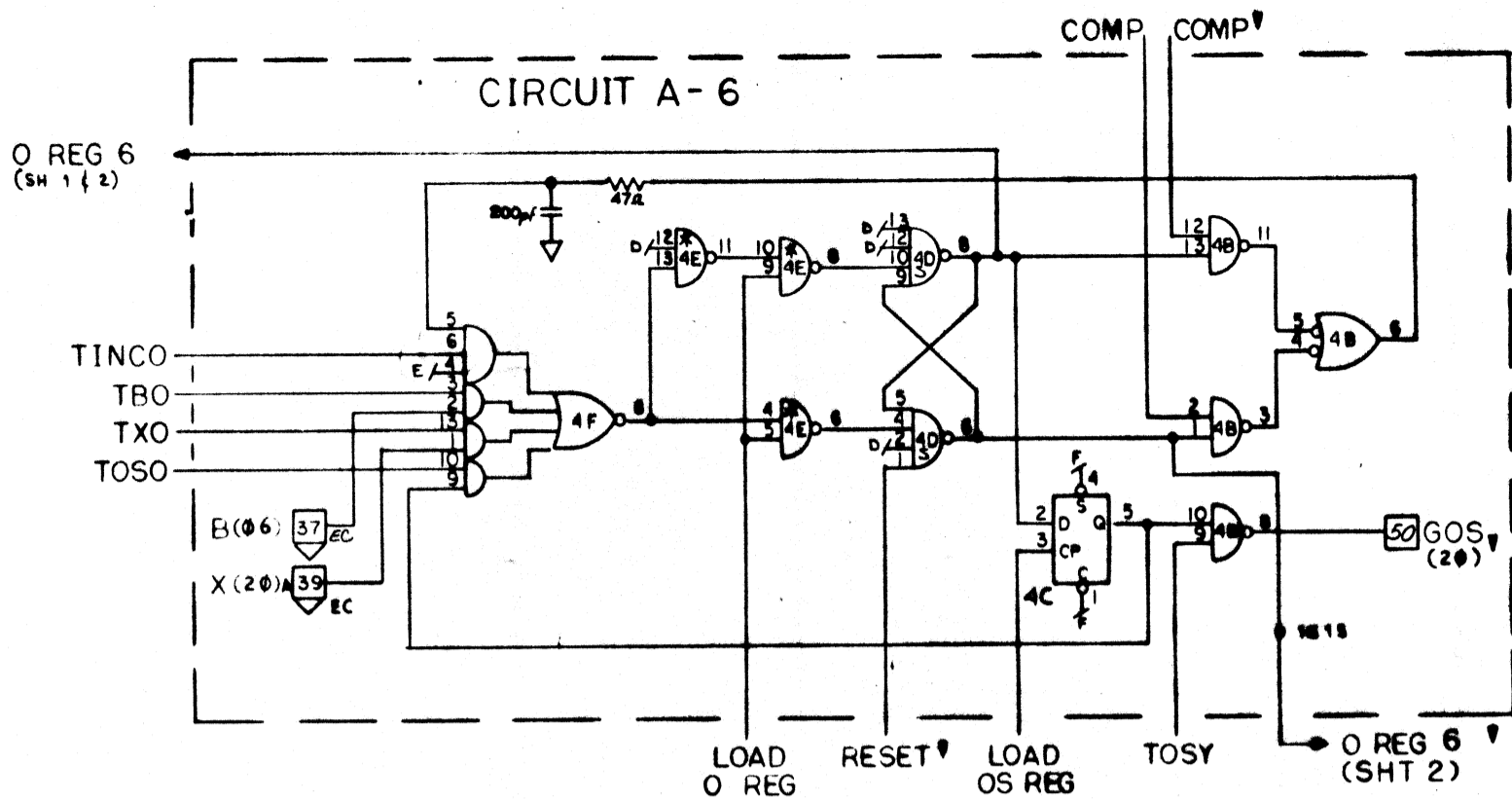
DATE: NONE
APPROVED BY: [Signature]
REVIEWED: [Signature]

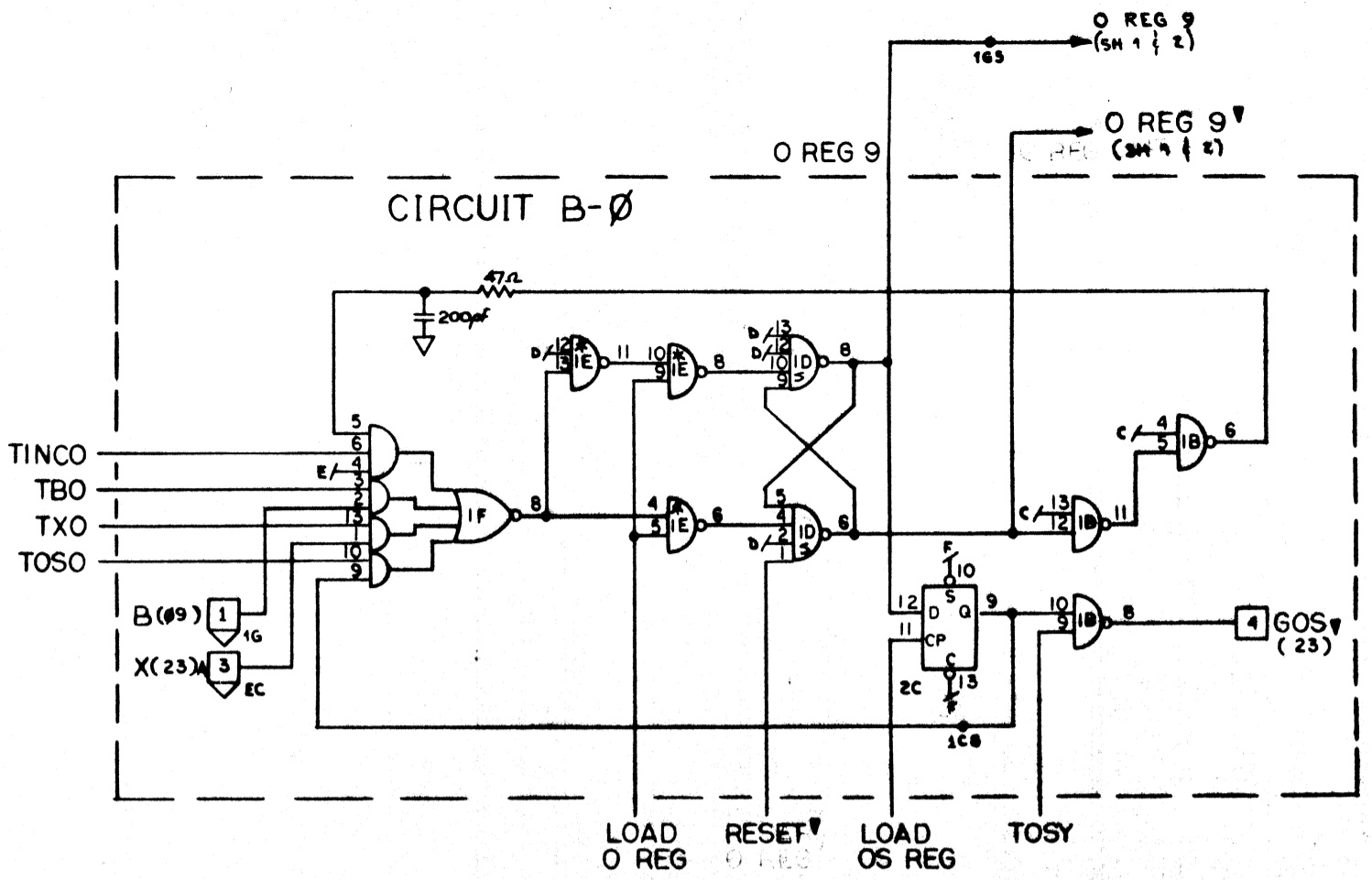
TITLE: O & OS REGISTER

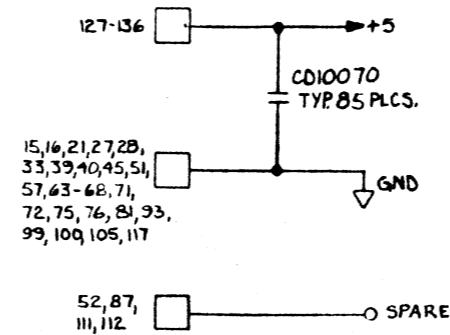
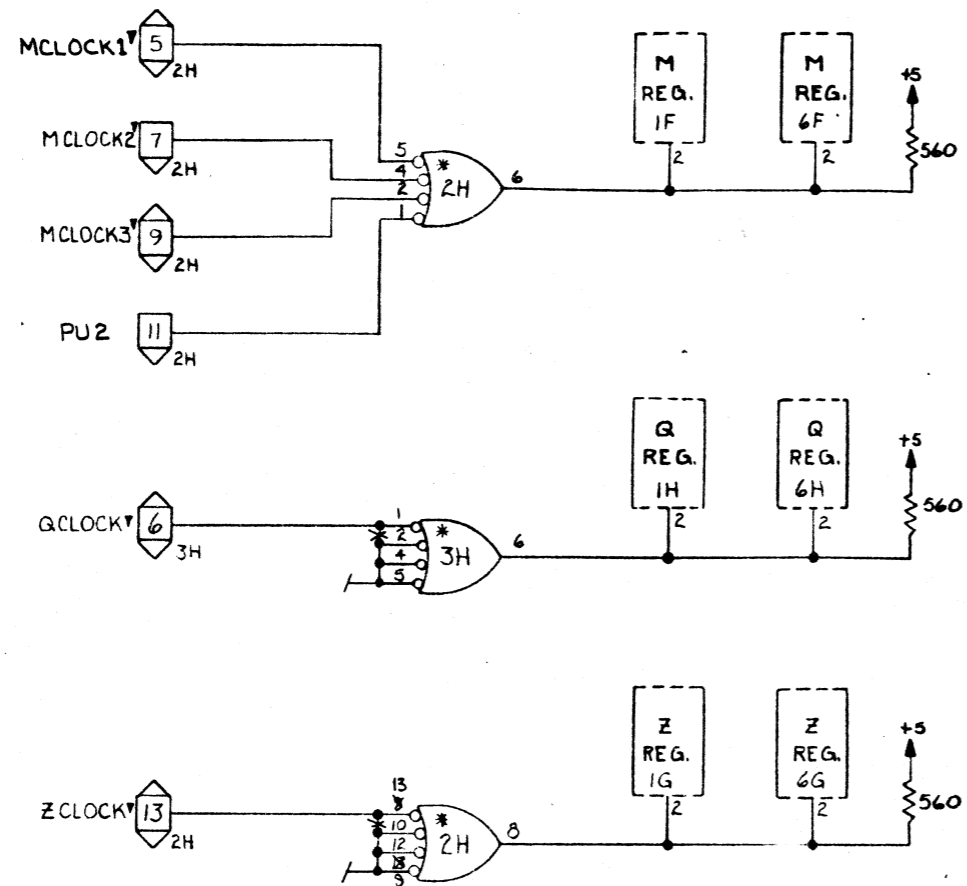
PROJECT: CONTROL LOGIC
CDD & ANALOGS

DATE: 10/24/65

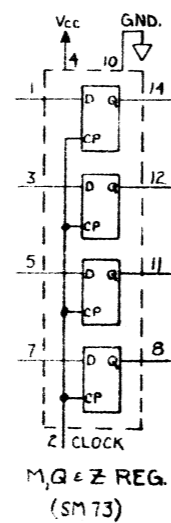
SH 4 OF 6







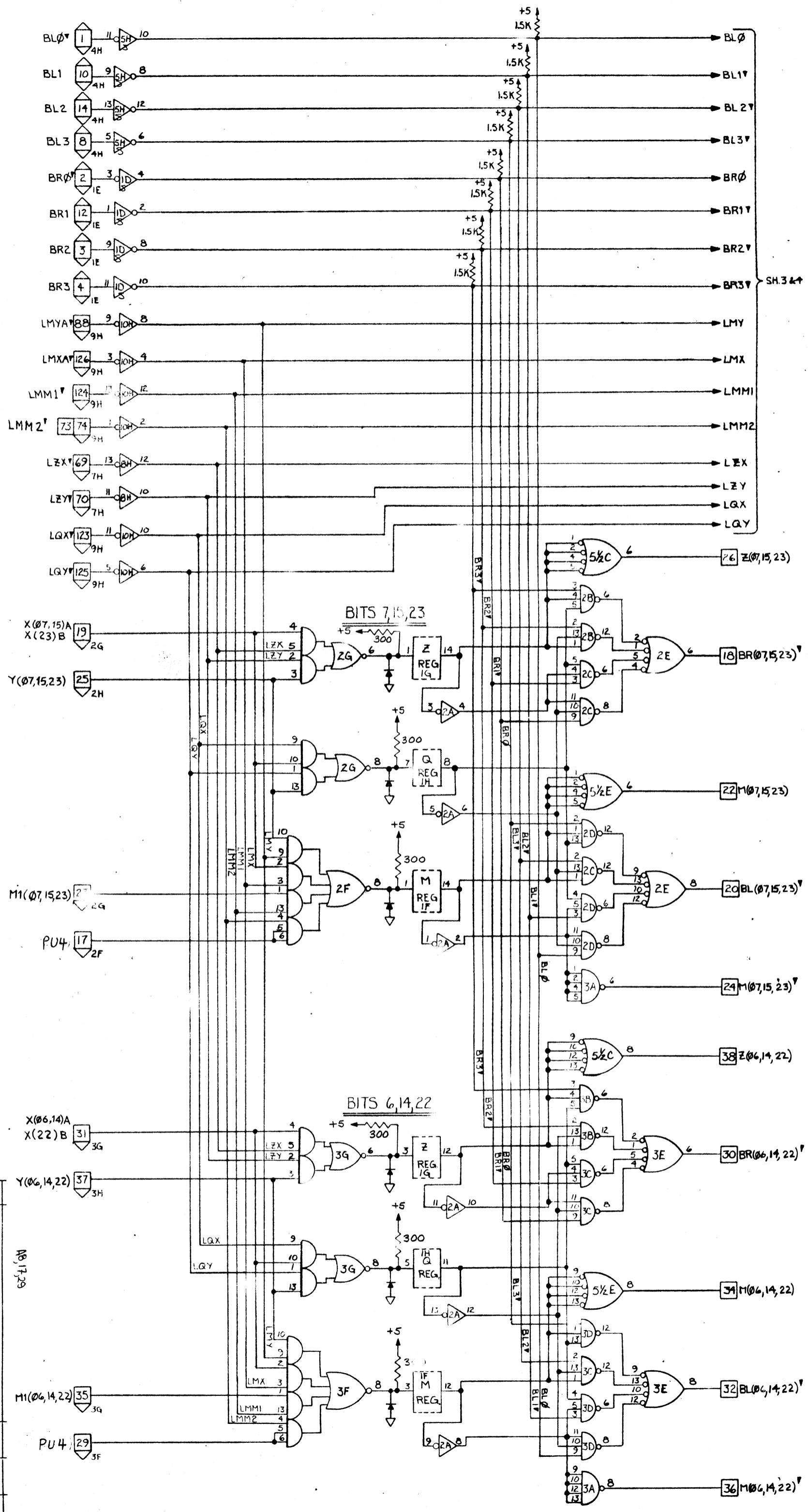
NOTES:
 UNLESS OTHERWISE SPECIFIED:
 1. RESISTORS ARE 1/8W, 10%, CARBON COMP.
 2. * INDICATES FAST MODULE.
 3. DIODES ARE DABOS's.



AB (00-07)
 A17 (08-15)
 A29 (16-23)

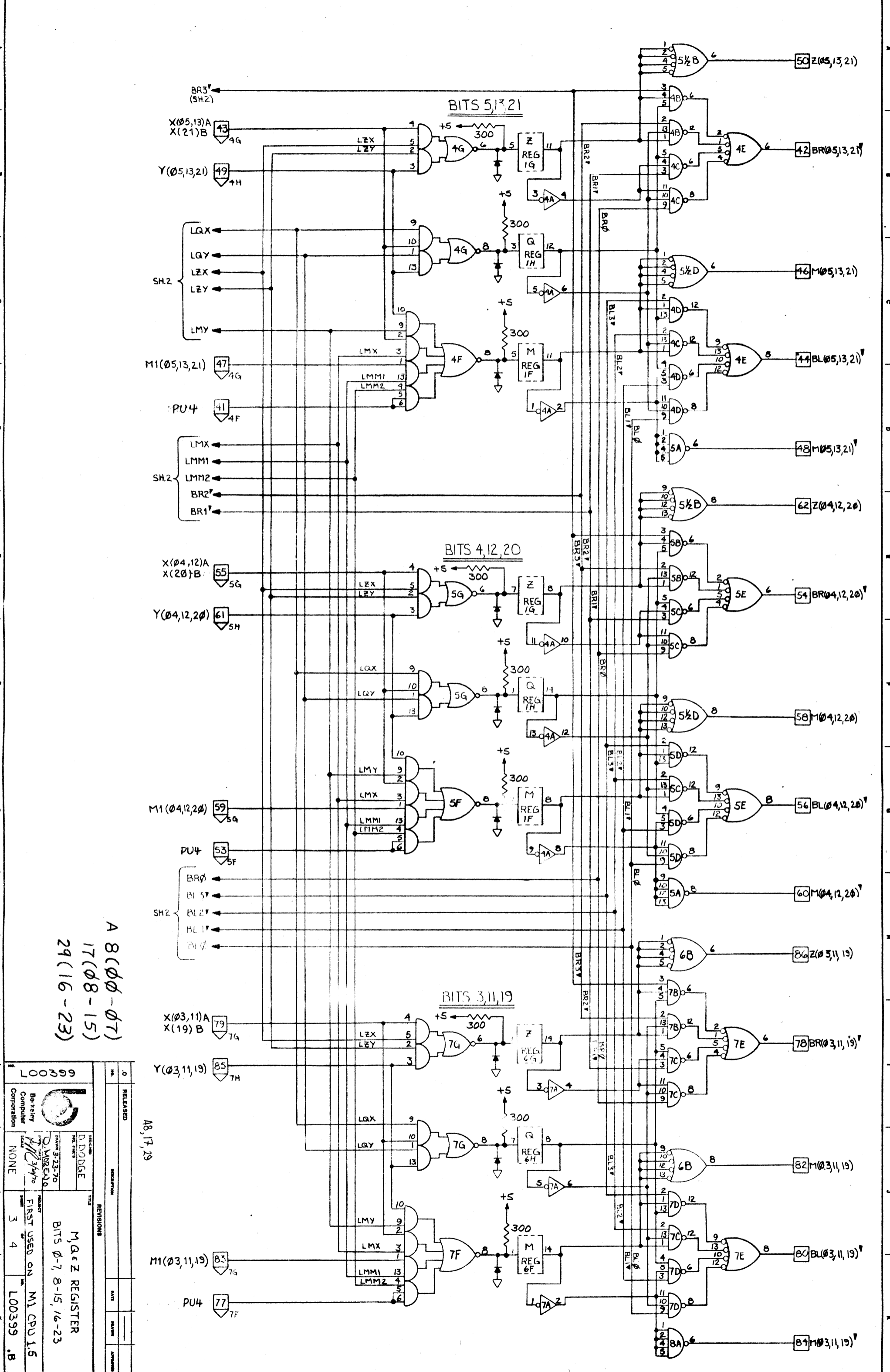
AB, 17, 29

B CHANGED SIGNAL NAMES		6-10-70	M.M.
NO.	DESCRIPTION	DATE	DRAWN APPROVED
REVISIONS			
66007 L00399	DESIGNED D. DODGE	TITLE M, Q & Z REGISTER	
	DRAWN 3-23-70 D. MORENO	BITS 0-7, 8-15, 16-23	
Berkeley Computer Corporation	SCALE NONE	FIRST USED ON M1 CPU 1.5	NO. OF SHEETS 4
		NO. L00399 .B	



A 8 (00-07)
 17 (08-15)
 29 (16-23)

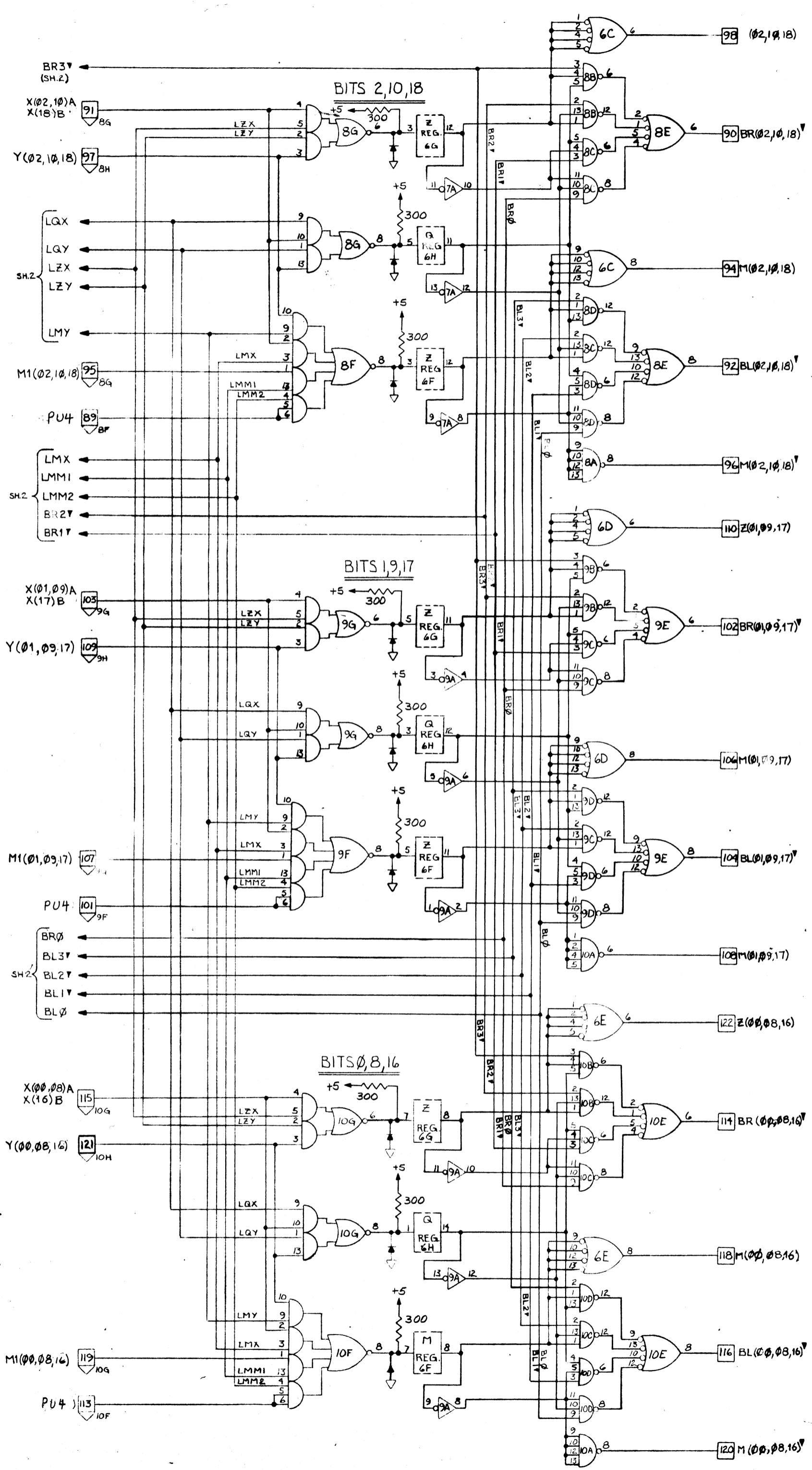
L00399		DESIGNED BY	DA WOODGE
Berkley Computer Corporation		DATE	3-23-70
NONE		REVISIONS	1. M.O.R.E.S.O.
2		PRODUCT	FIRST USED ON M1 CPU 1.5
4		TITLE	BITS 0-7, 8-15, 16-23
L00399 .B		NO.	
		RELEASED	
		REVISIONS	
		DATE	
		NAME	
		APPROVED	



A 8(00-07)
 17(08-15)
 29(16-23)

A8, 17, 29

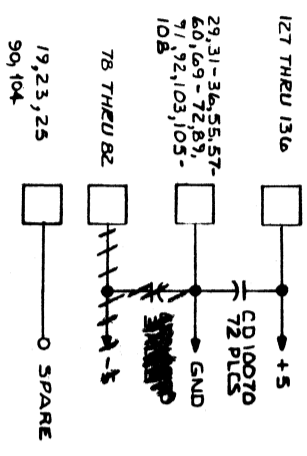
L00399		REVISED	DATE	BY	REASON
		RELEASED			
D. DODGE DATE: 3-23-70 BY: M. M. M. M. NONE		REVISIONS	DATE	BY	REASON
FIRST USED ON M1 CPU 1.5 BITS 0-7, 8-15, 16-23		1			
L00399 .B		2			



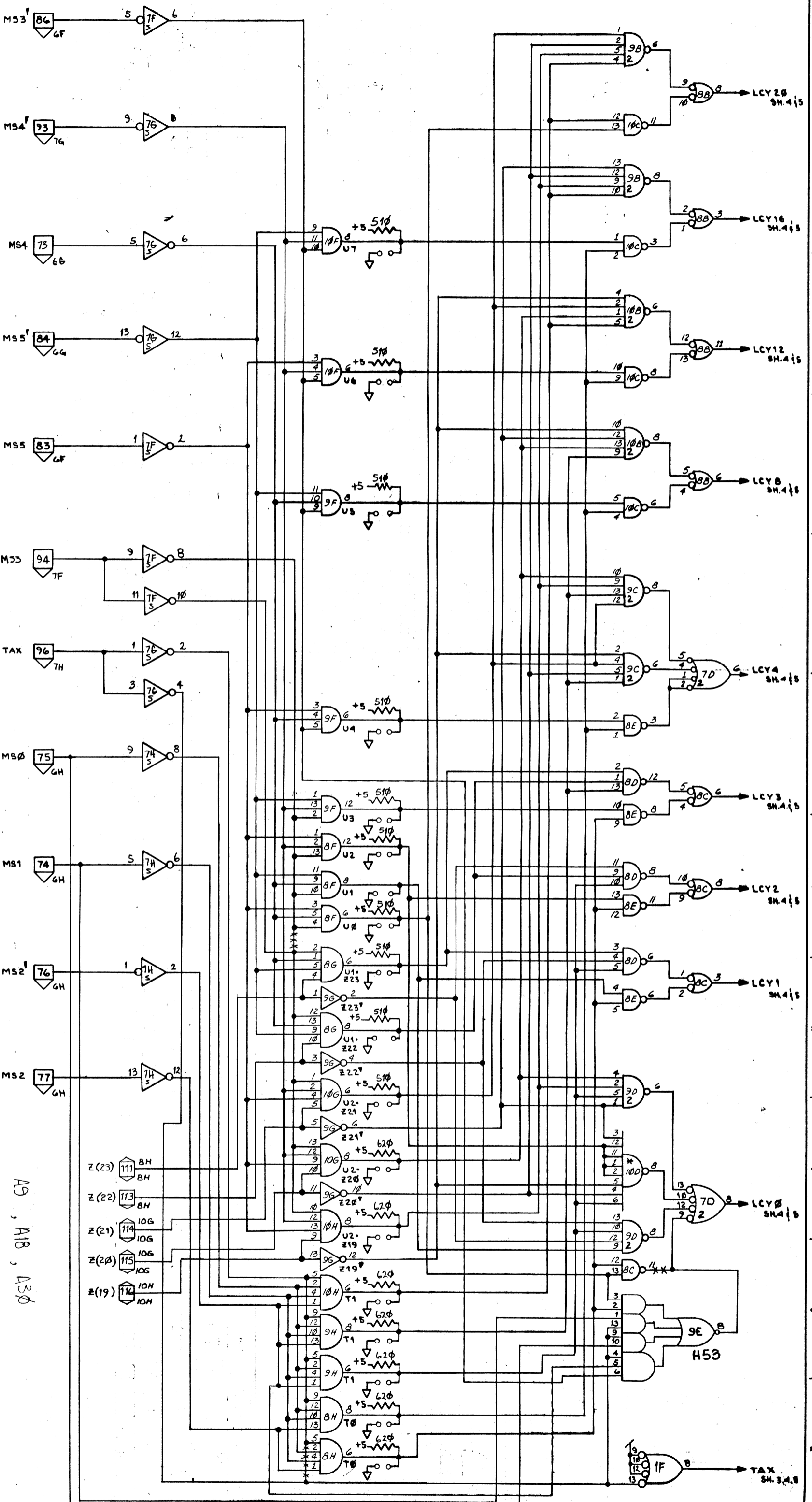
AB (00-07)
 17 (08-15)
 29 (16-23)

L00399		0	RELEASED	AS, 17, 29
 BERKLEY COMPUTER CORPORATION	DESIGNED BY	DODGE	REVISIONS	
	DATE			
	REVISED	3-23-70		
	BY	NOREDO		
	SCALE	NONE		
	FIRST USED ON	M1 CPU 1.5		
	SCALE	4 4		
	PROJECT	L00399.B		
M, Q & Z REGISTER BITS 0-7, 8-15, 16-23				

NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTOR VALUES ARE IN OHMS
 2. ALL TRANSISTOR VALUES ARE IN OHMS
 3. * INDICATES SELECTED FAST I.C. MODULES.
 4. 200Ω RESISTORS ARE 5% 1/8W

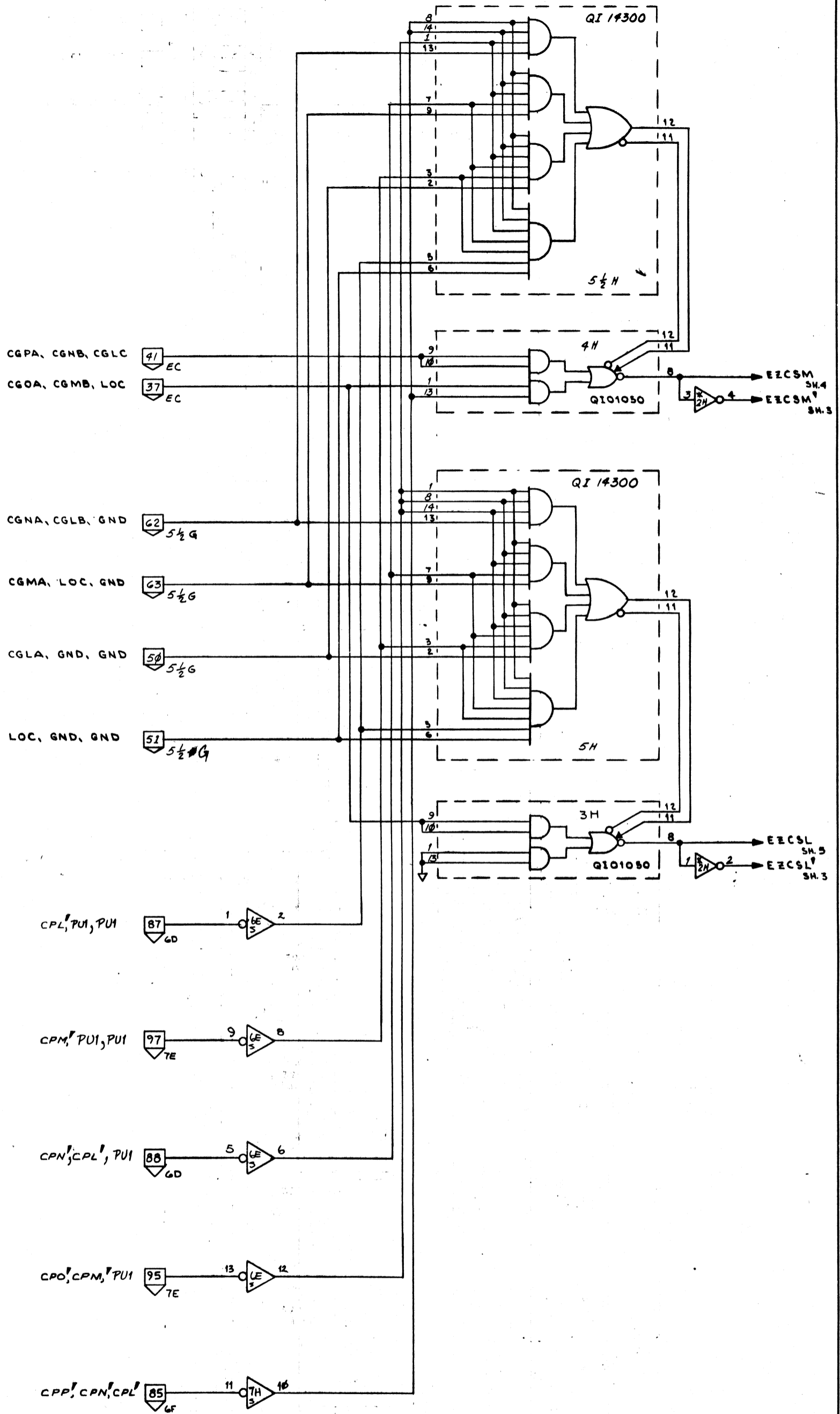


A9 (00-07)
 A18 (08-15)
 A30 (16-23)
 A9 (00-07)
 A18 (08-15)
 A30 (16-23)



PCN #016 REMOVED 150Ω PULL UP FROM SH1		8-10-70	M/M
CHANGED SIGNAL NAMES		6-10-70	M/M
RELEASED			
M. M. BROTHMAN		CYCLER/ADDER, BITS	
DATE: 5/21/70		(0-7), (8-15), (16-23)	
REV. 1		FIRST USED ON M1 CPU-1.5	
L00431		L00431	

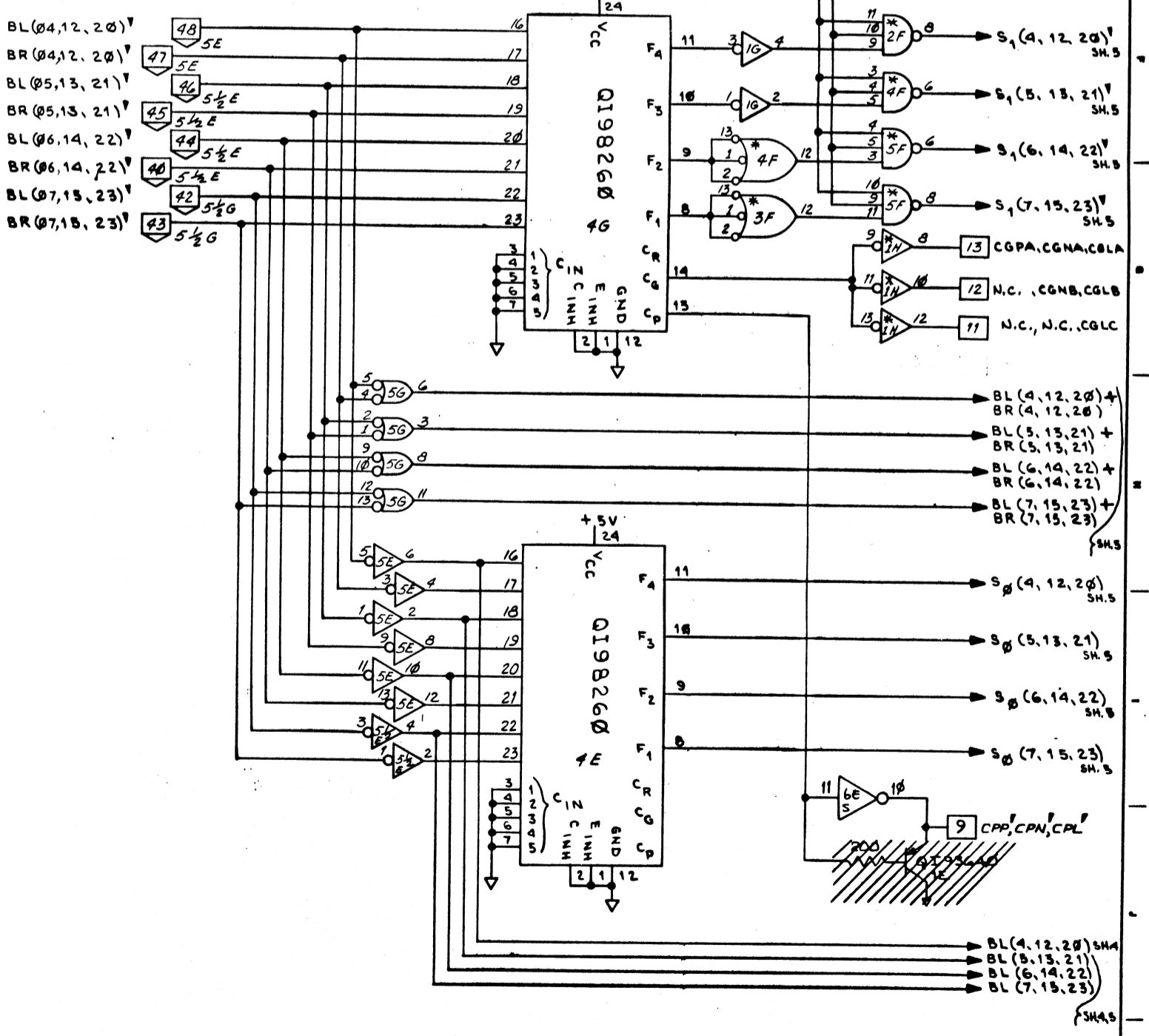
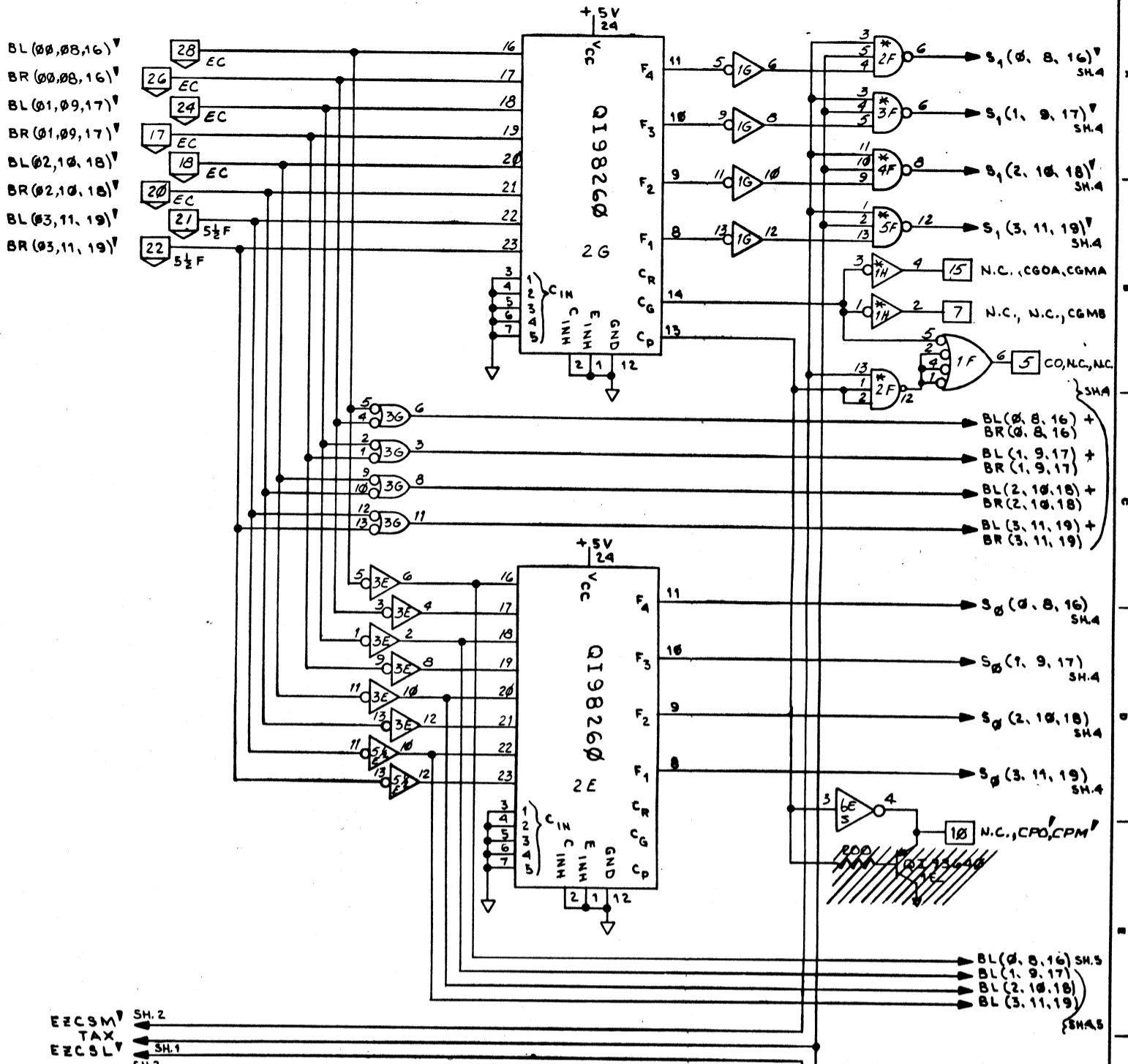
A9, A18, A30



A9 (ØØ-Ø7)
 18 (Ø8-15)
 3Ø (16-23)

A9, A18, A3Ø

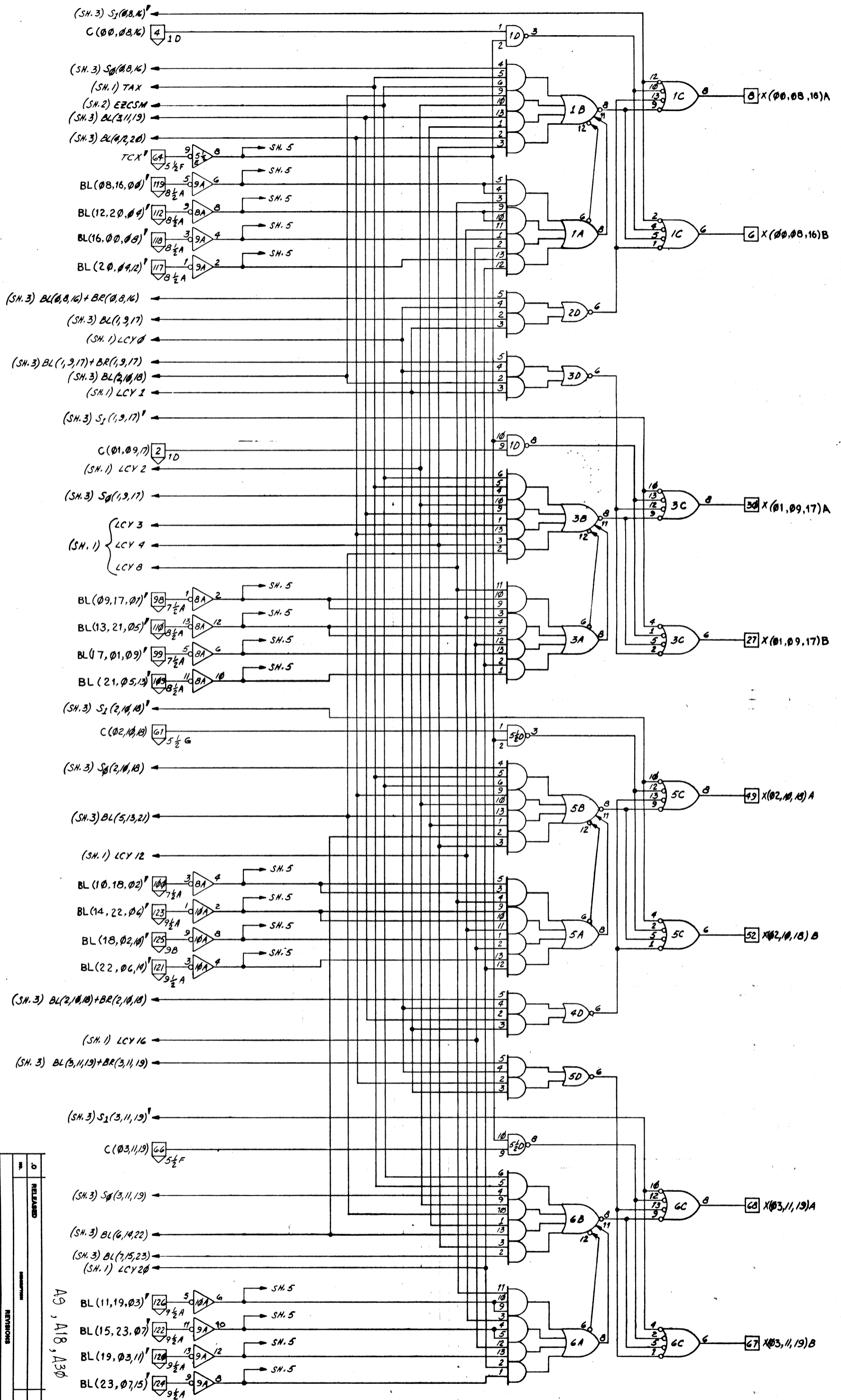
L00431		REVISION		DATE	
RELEASED		LANSFUTN11		5/23/70	
NO.		REVISED		DATE	
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3		4		5/23/70	
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A9 (0-07)
 10 (01-15)
 30 (16-23)

A9, A18, A30

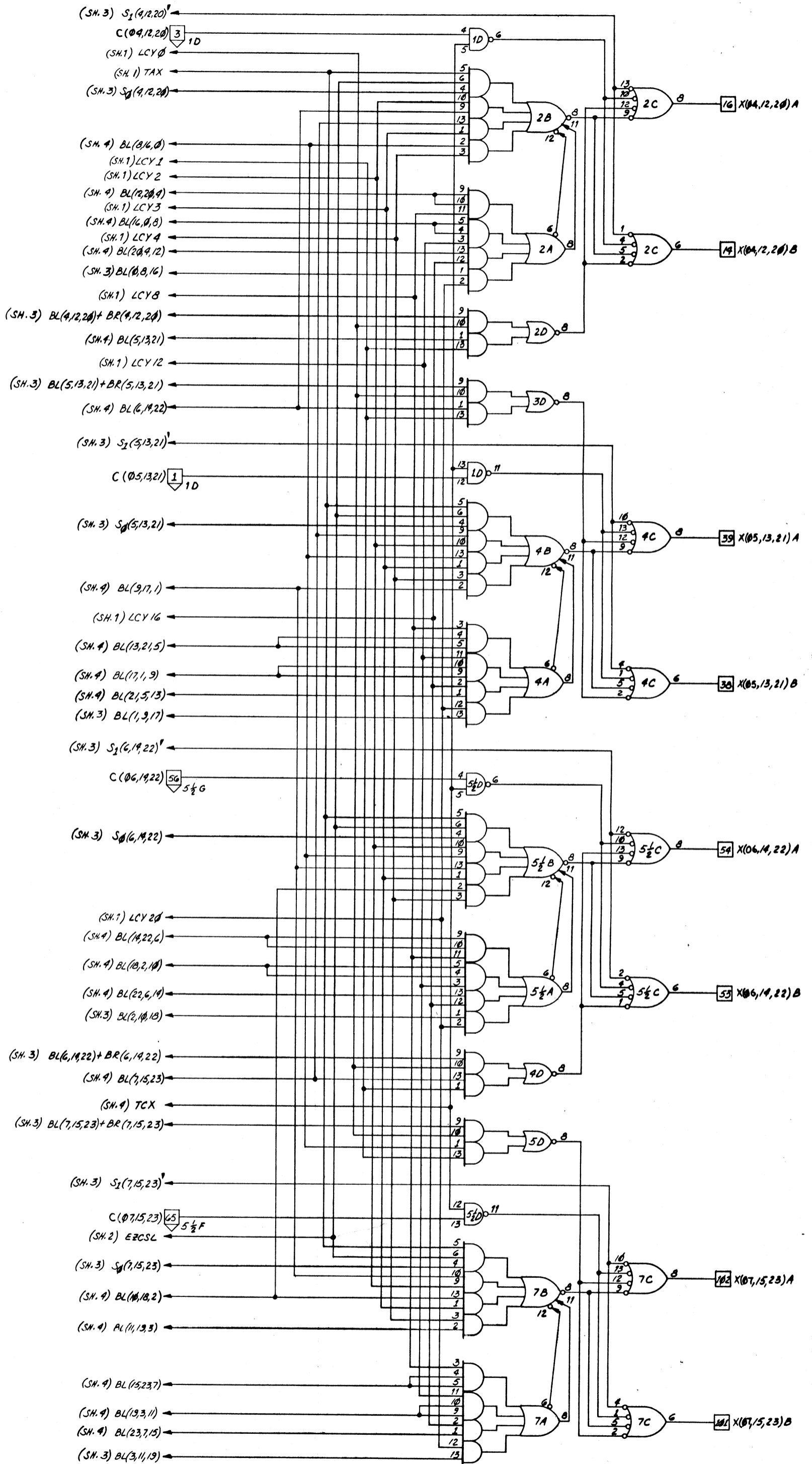
L00431		RELEASED	
Berkeley Computer Corporation 2000 UNIVERSITY AVENUE BERKELEY, CALIF. 94720		M. INDUSTRIAL 1000 UNIVERSITY AVENUE BERKELEY, CALIF. 94720	
CYCLER/ADDER, BITS (0-7), (8-15), (16-23)		FIRST USED ON M1 CPU-1.5	
3 5		L00431 DE	



A9 (00-07)
 18 (08-15)
 30 (16-23)

A9, A18, A30

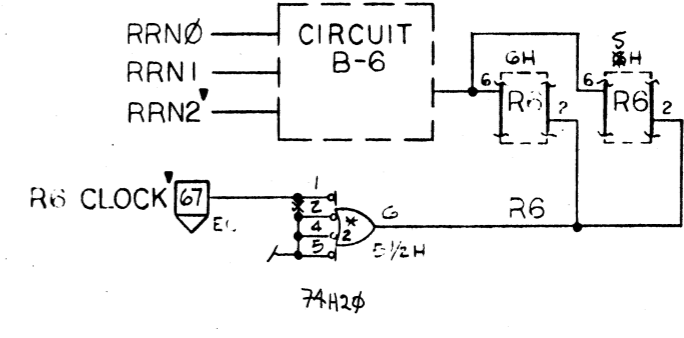
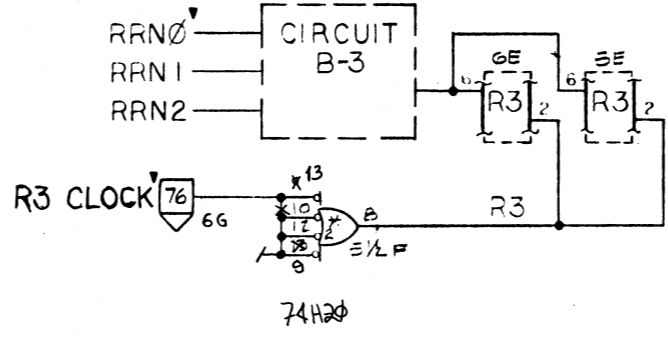
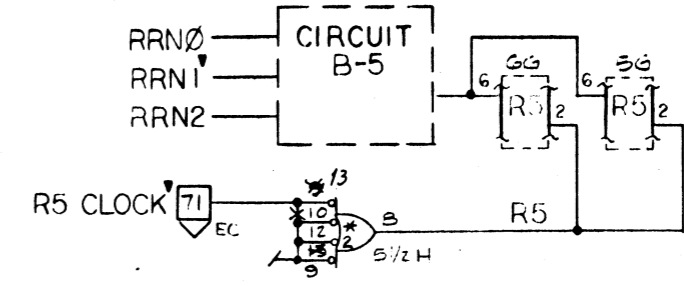
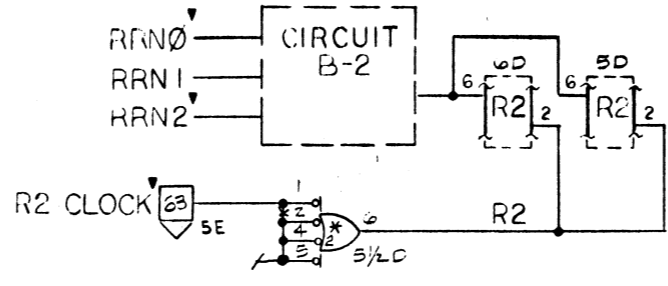
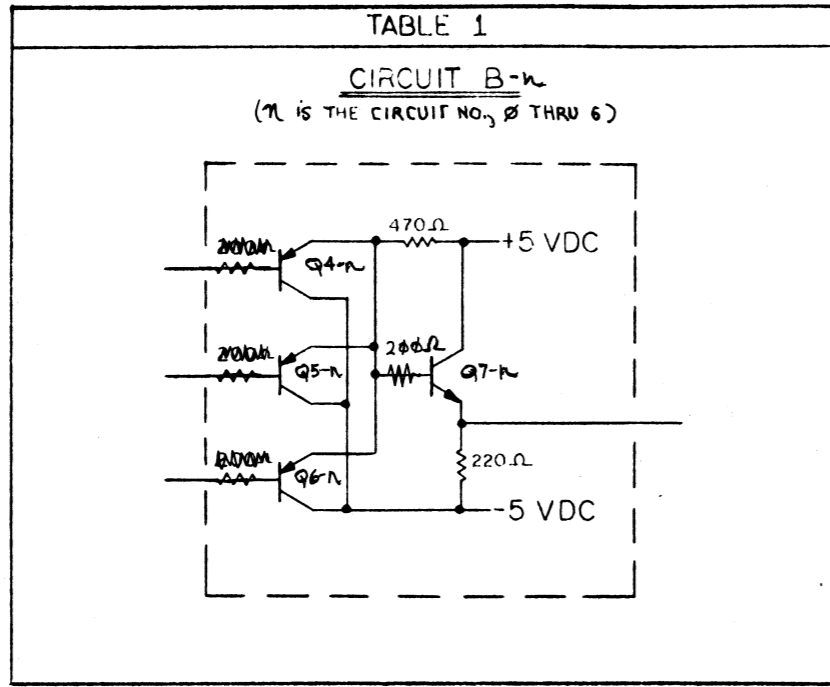
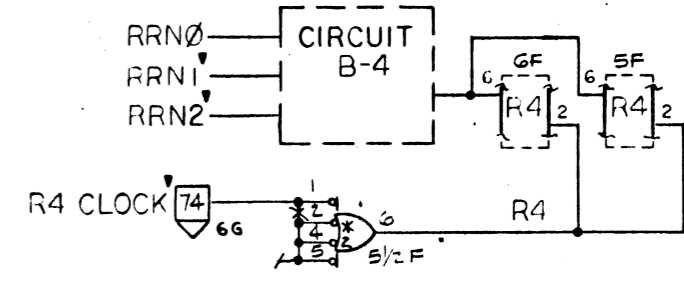
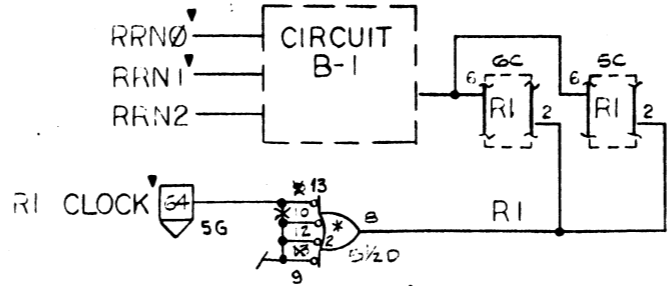
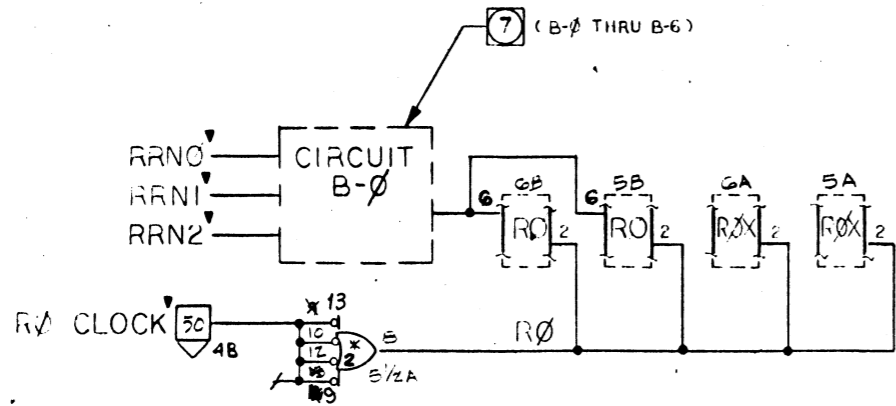
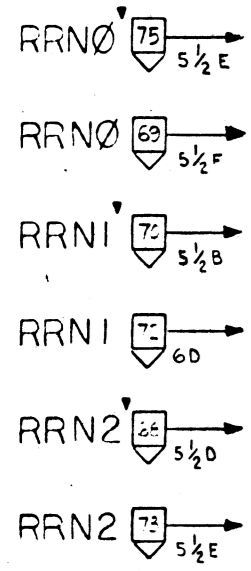
100431		RELEASD
		N. MARSTON DATE: 5/24/70 TIME: 4:30 MAKE: 30
CYCLER/ADDER BITS (0-7), (8-15), (16-23)		TITLE: CYCLER/ADDER PART: 100431 REV: 5
FIRST USED ON M1 CPU 1.5		DATE: 5/24/70 TIME: 4:30 MAKE: 30



A 9 (00-07)
 18 (08-15)
 30 (16-23)

A9, A18, A30

L00431		RELEASED	
BERKELEY COMPUTER CORPORATION 2015 SHILTON AVENUE BERKELEY, CALIF. 94704		M. M. ROTUNDA 1000 UNIVERSITY AVENUE BERKELEY, CALIF. 94704	
DATE: 3/25-2 FILE: 00-1-2-2 BY: M. M. ROTUNDA		TITLE: CYCLER/ADDER BITS (0-7), (8-15), (16-23)	
FIRST USED ON MI CPU 1.5		NO. 5 L00431 .D	



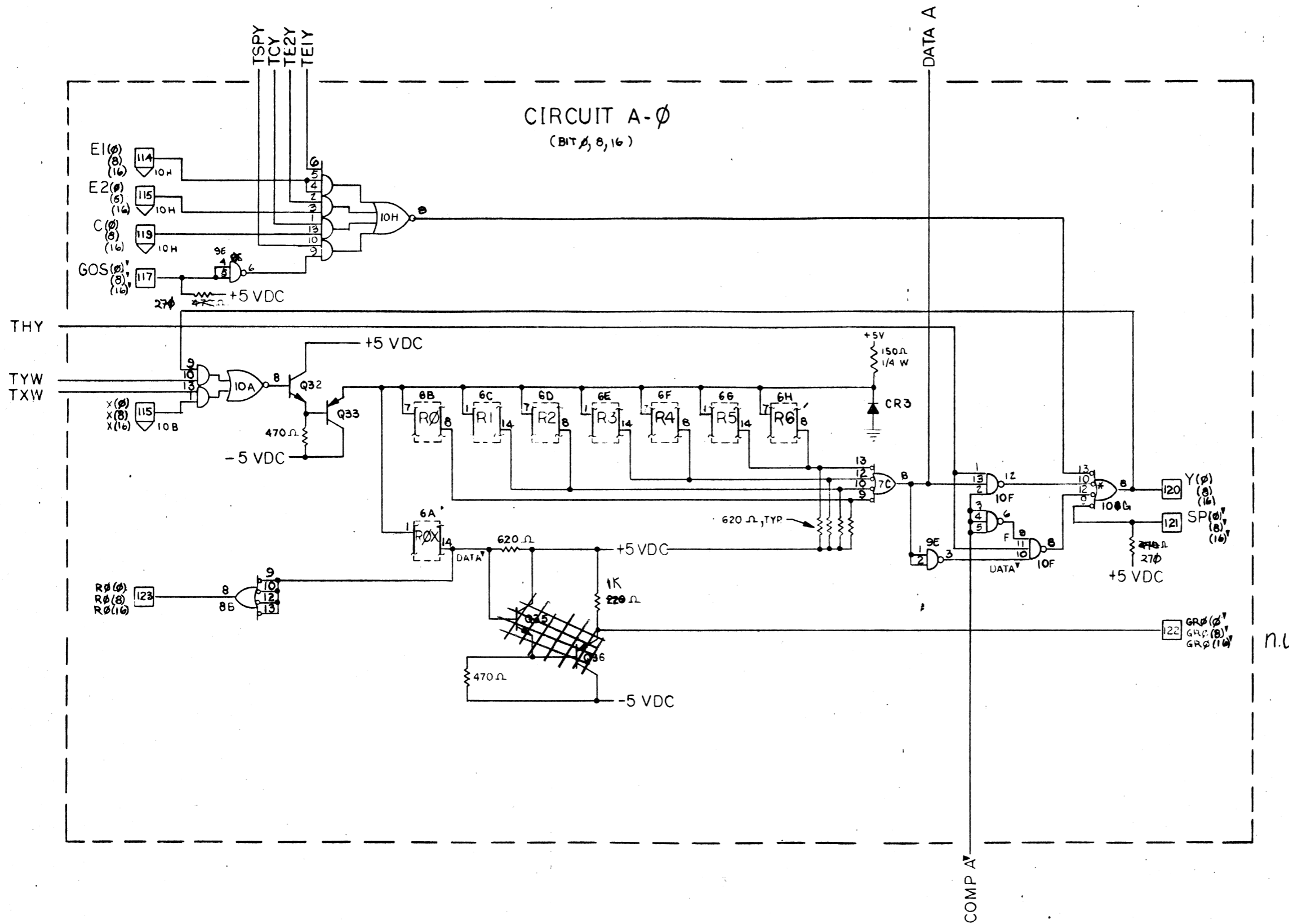
A 10(00-07)
19(08-15)
31(16-23)

A10, 19, 31

berkeley Computer Corporation

SCALE: NONE	APPROVED BY:	DRAWN BY: R. BOW
DATE: 18 JULY 69		REVISED 12/9/69 HC
TITLE: HOLDING REGISTER		
FIRST USED ON MI CPU 1.5		DRAWING NUMBER: L00400

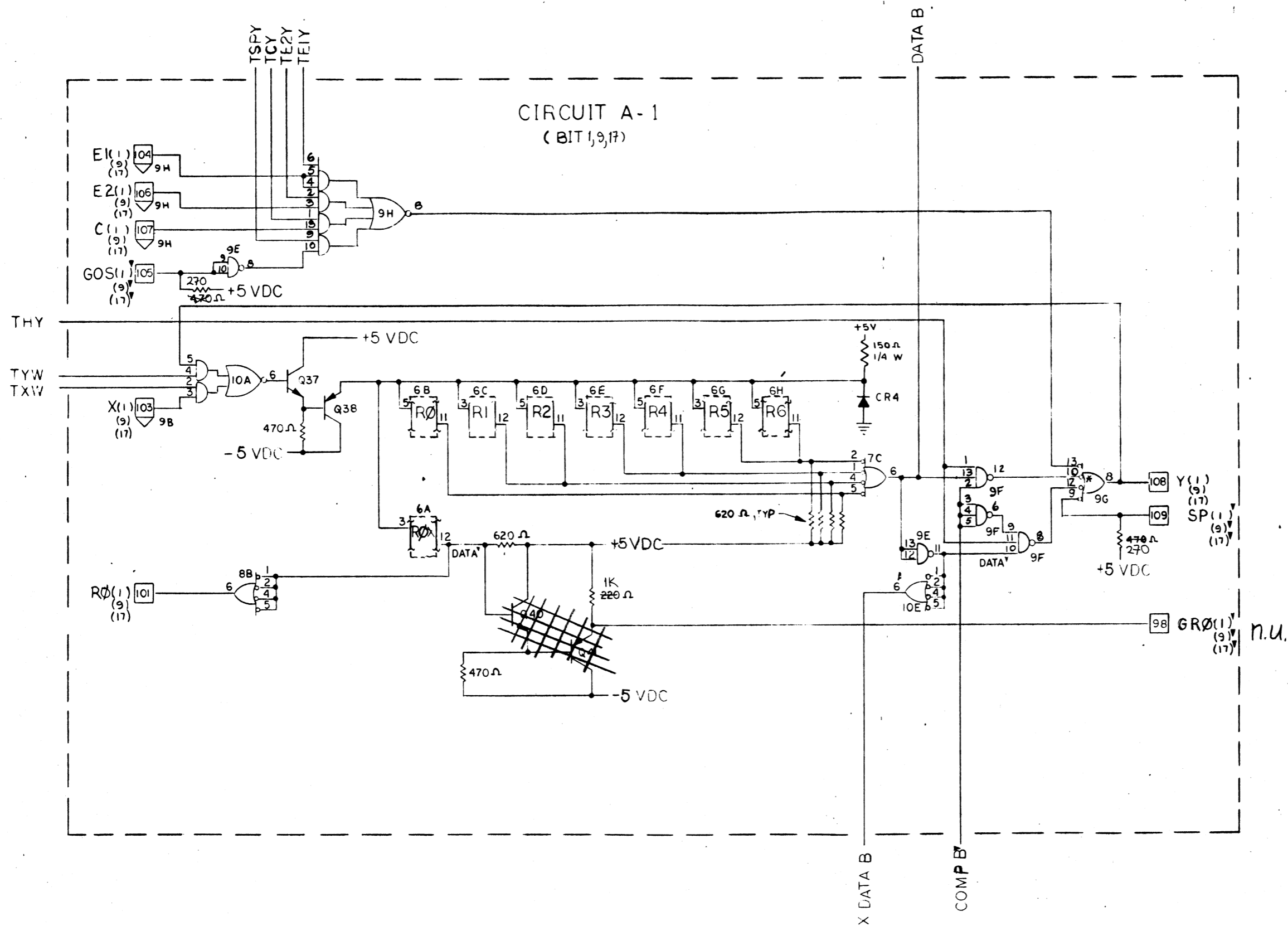
SH 2 OF 1



A10, 19, 31

A10 (00-07)
19 (08-15)
31 (16-23)

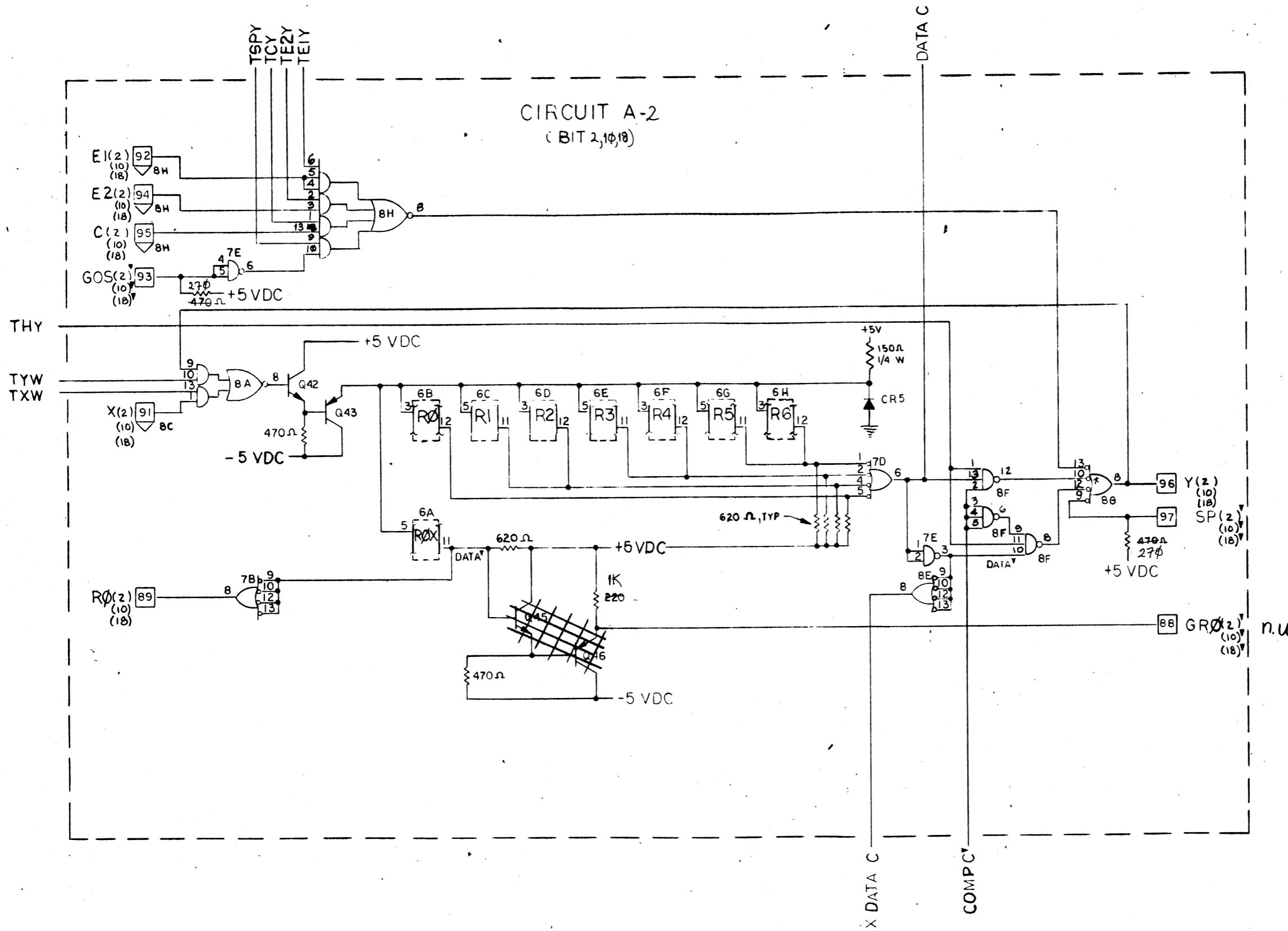
berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: E.B. BEN
DATE: 19 JULY 69		REVISED: 12-9-69
HOLDING REGISTER		
FIRST USED ON MI CPU 1.5	DRAWING NUMBER	LOW 400 3
SH 3 OF 10		



A1Ø (ØØ-Ø7)
 19 (ØØ-15)
 31 (16-23)

A1Ø, 19, 31

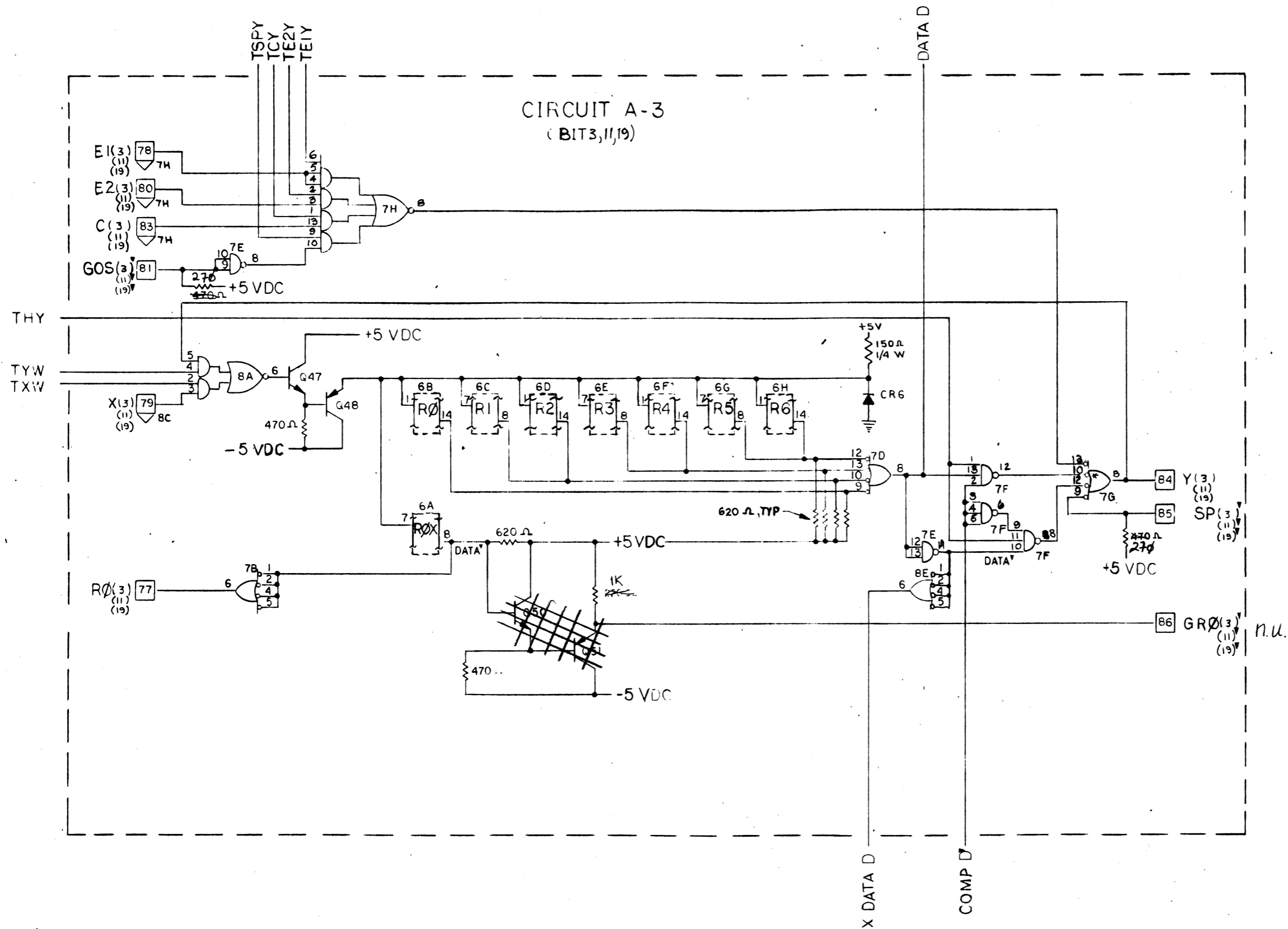
berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: <i>RSN</i>
DATE: 16 JULY 69		REVISED: 12-9-69 H.C.
HOLDING REGISTER		
FIRST USED ON MI CPU 1.5	DRAWING NUMBER: LOU 400.D	



A 10 (00-07)
19 (08-15)
31 (16-23)

A10, 19, 31

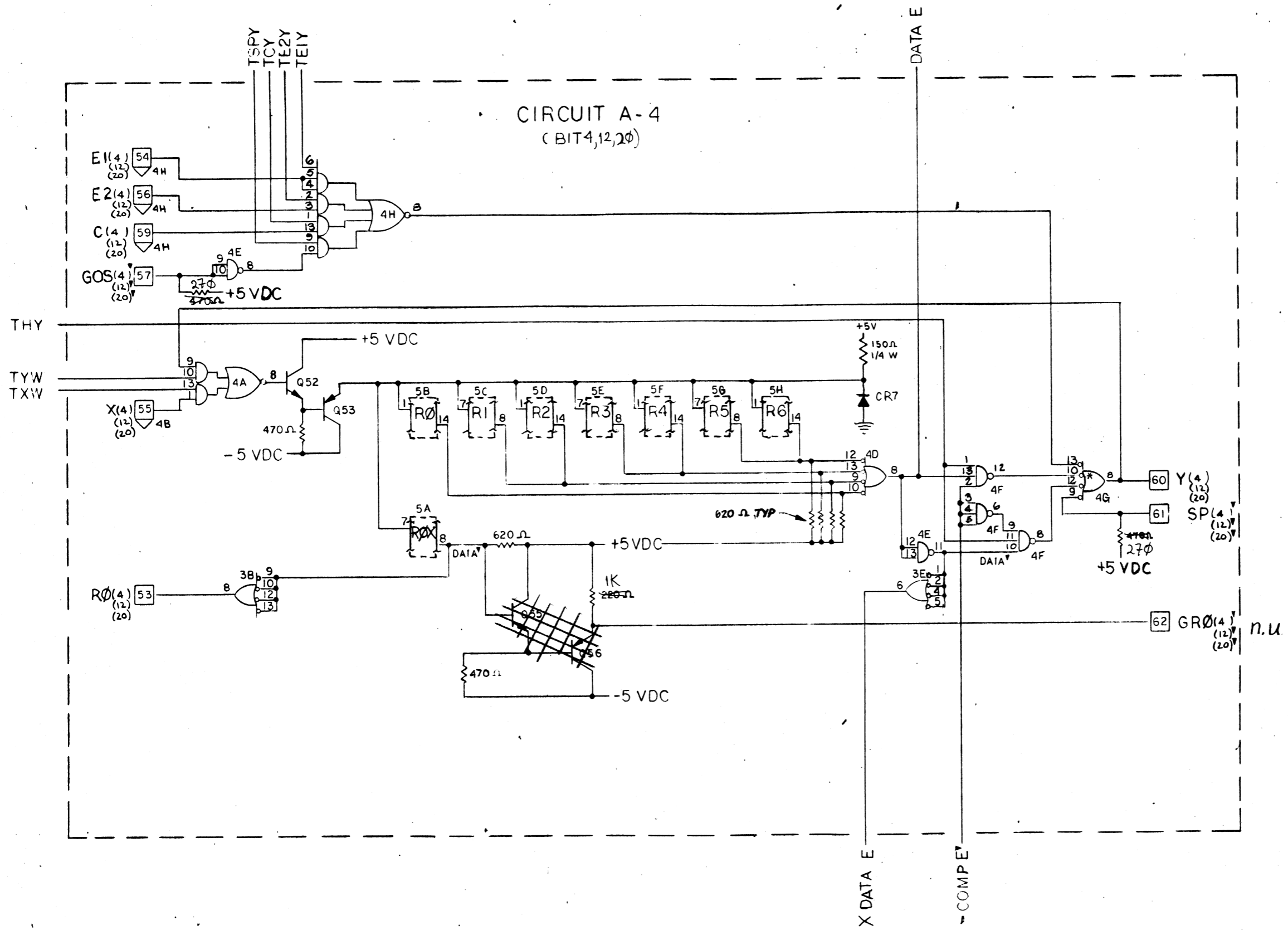
Berkeley Computer Corporation		
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DATE: 19 JULY 69		REVISED 12/9/69 H.C.
HOLDING REGISTER		
FIRST USED ON M1 CPU 1.5	DRAWING NUMBER: L00400.0	



A 10 (00-07)
 19 (08-15)
 31 (16-23)

A10, 19, 31

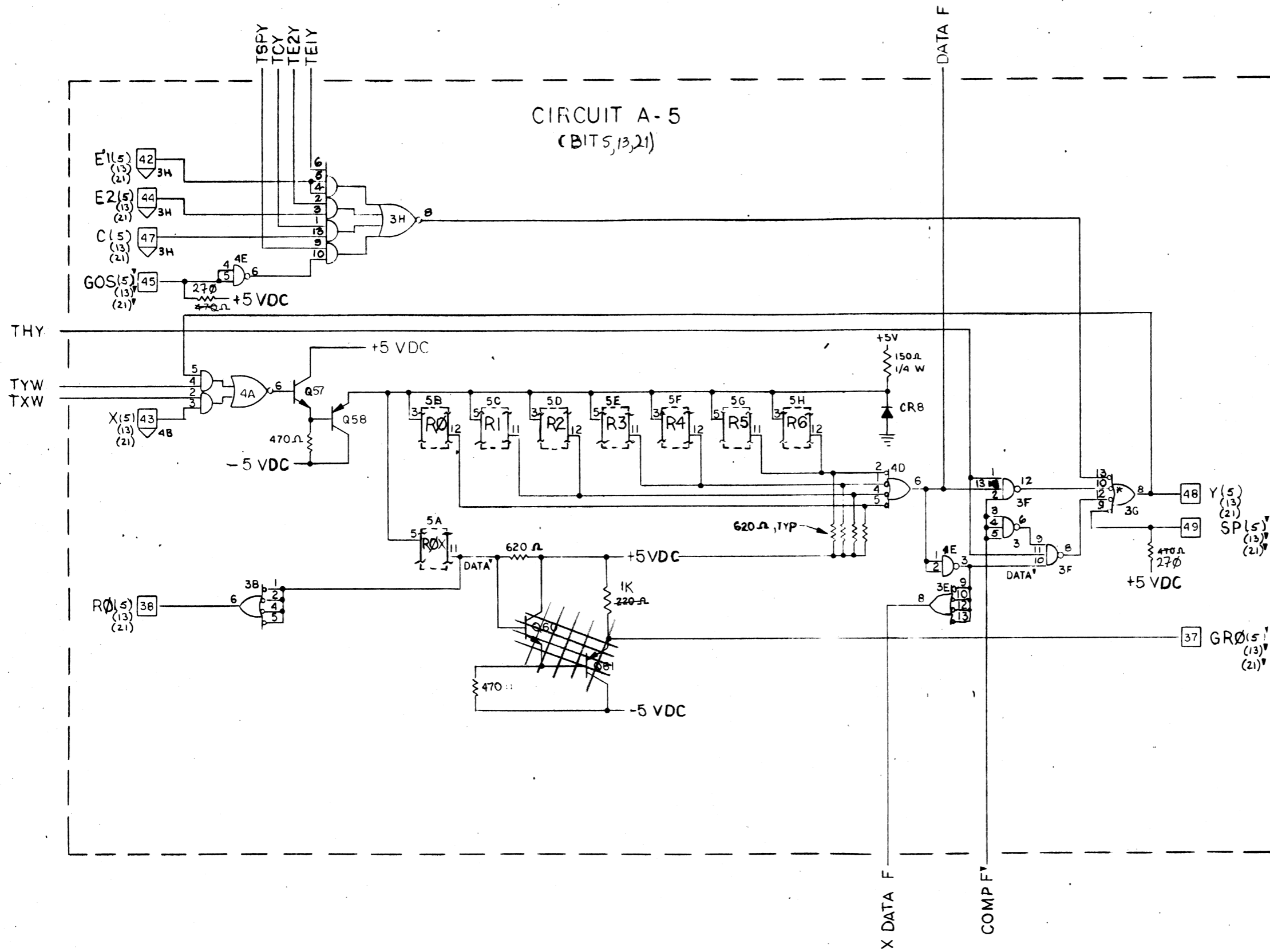
berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: P. J. ...
DATE: 16 JULY 69		REVISED: 12/9/69
HOLDING REGISTER		
FIRST USED ON M1 CPU 1.5	DRAWING NUMBER: LCC400.1	



A 10 (00-07)
19 (08-15)
31 (16-23)

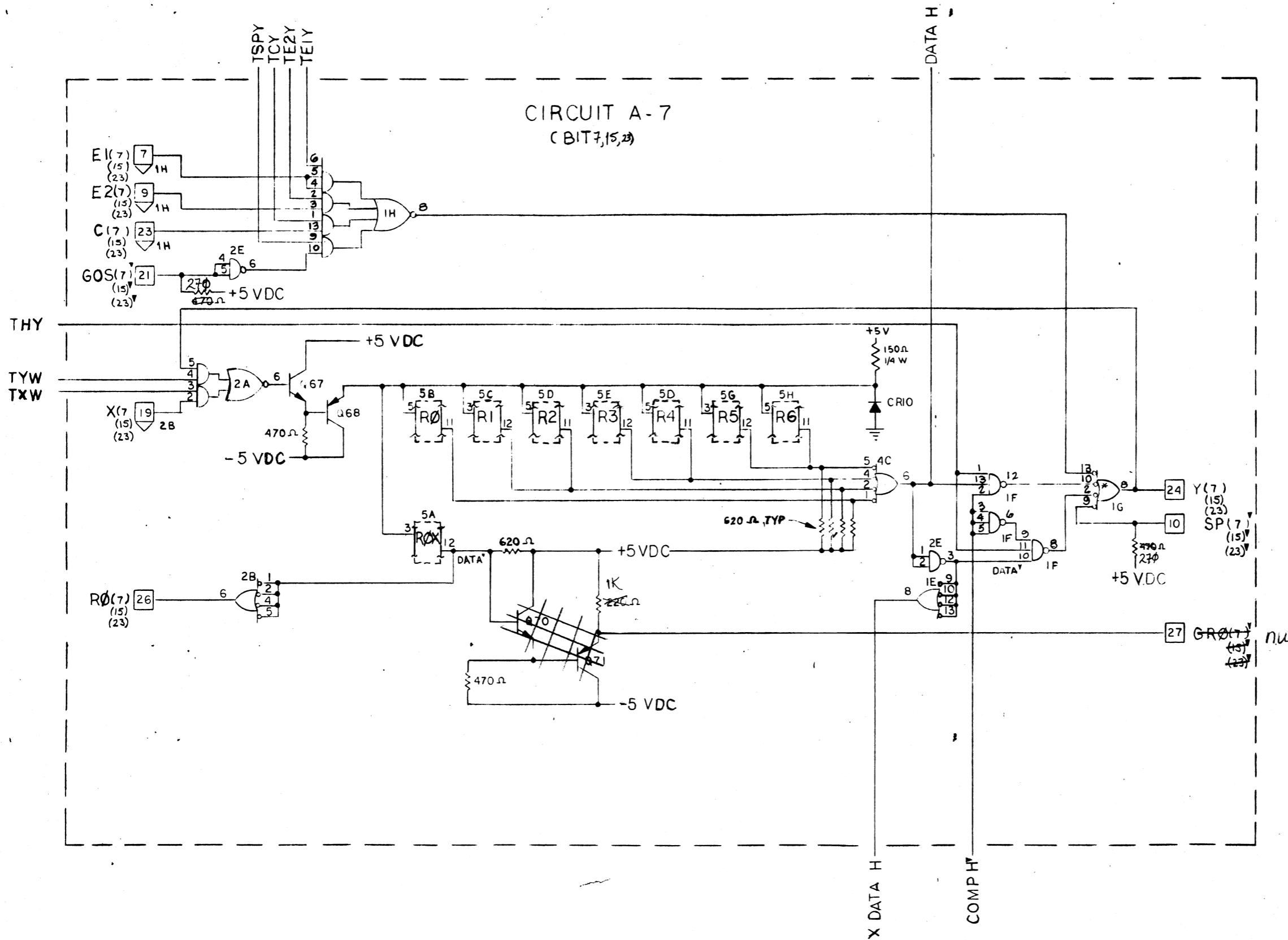
410, 19, 31

Berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: E.S.V.
DATE: 15 JULY 69		REVISED: 7/9/69 H.C.
HOLDING REGISTER		
FIRST USED ON MI CPU 1.5	DRAWING NUMBER: L00400.0	



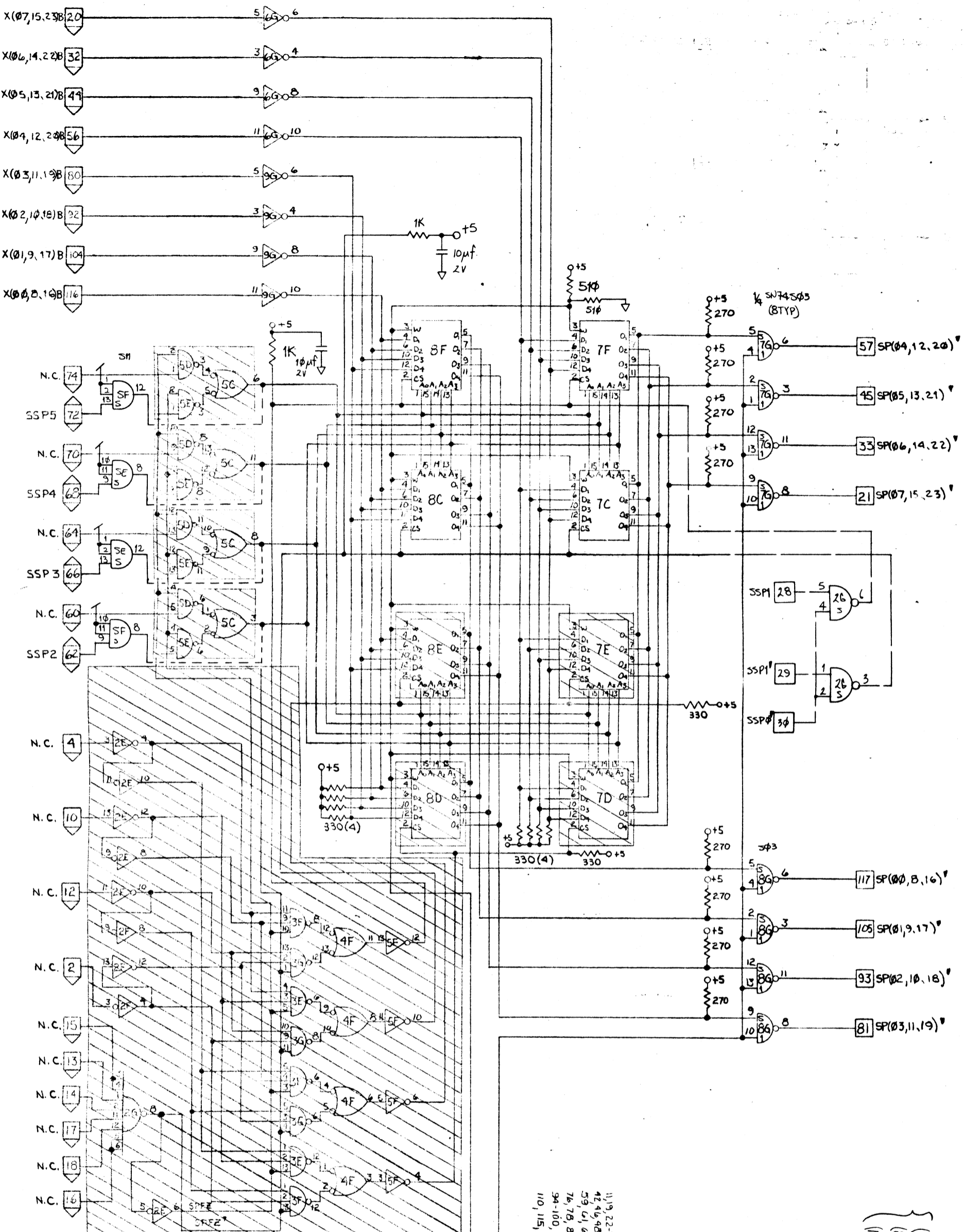
A10, 19, 31

Berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: R.F.
DATE: 15 JULY 69		REVISED: 12/9/69 A.C.
HOLDING REGISTER		
FIRST USED ON MICR PULS	DRAWING NUMBER: L00400	



A10, 19, 31

Berkeley Computer Corporation		
SCALE: NONE	APPROVED BY:	DRAWN BY: <i>EC</i>
DATE: 17 JULY 69		REVISED H.C. 12/9/69
HOLDING REGISTER		
FIRST USED ON MI CPU 1.5	DRAWING NUMBER L00400.D	



LO0447

Berkeley Computer Corporation

DATE: 03/3/70

SCALE: NONE

PROJECT: 32 WORD SCRATCHPAD

REVISED: 1

REVISED BY: M1 CPU-1.5

NO. 1

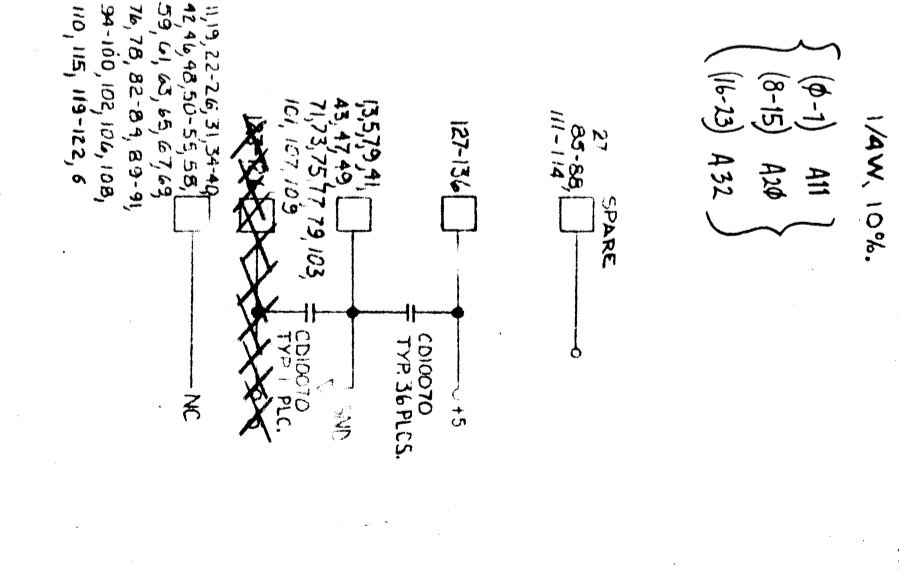
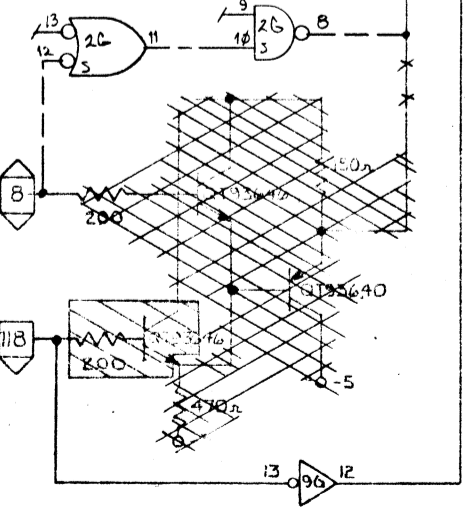
REVISED BY: L00447 C

B. CHANGED SIGNAL NAMES

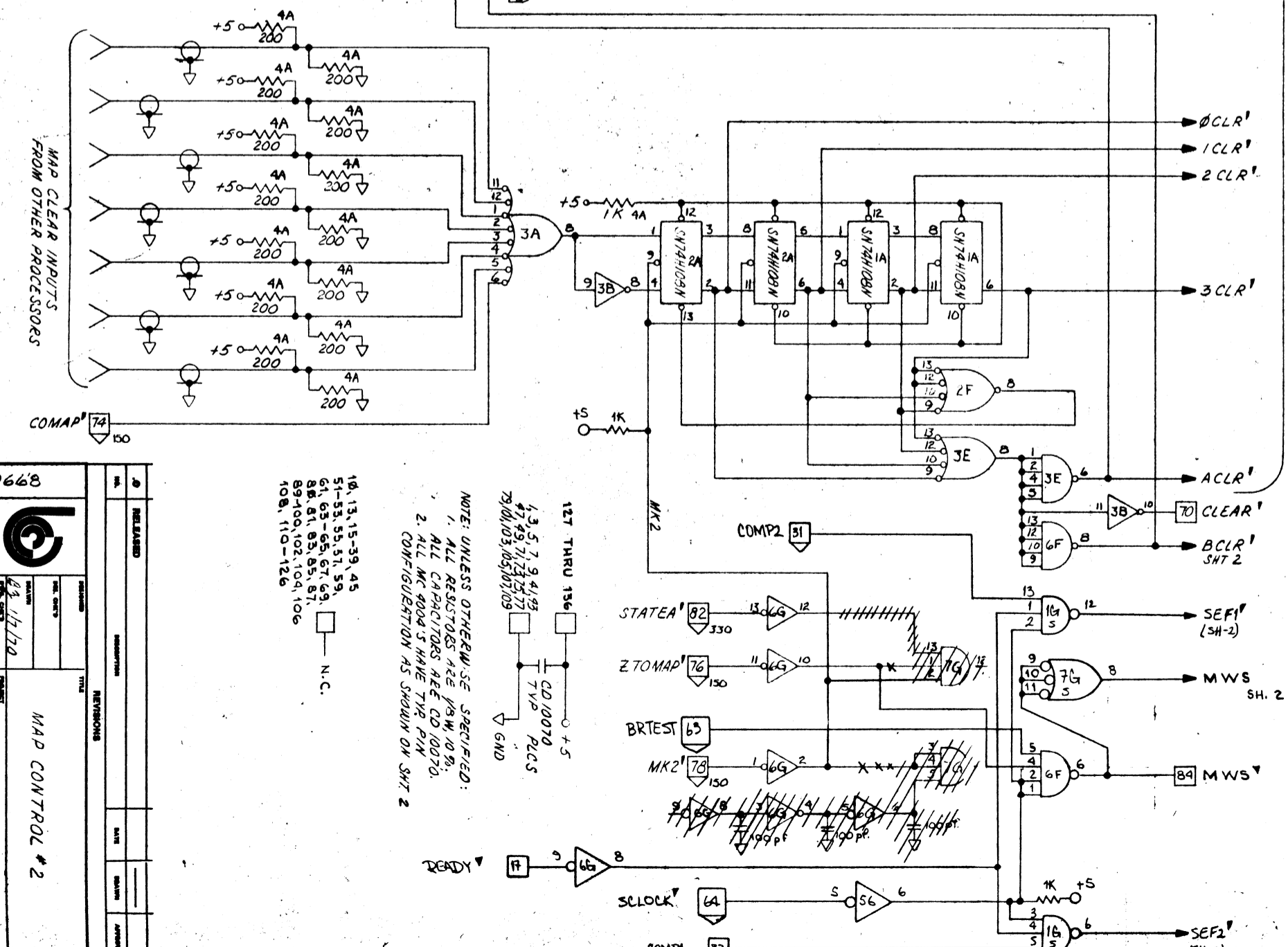
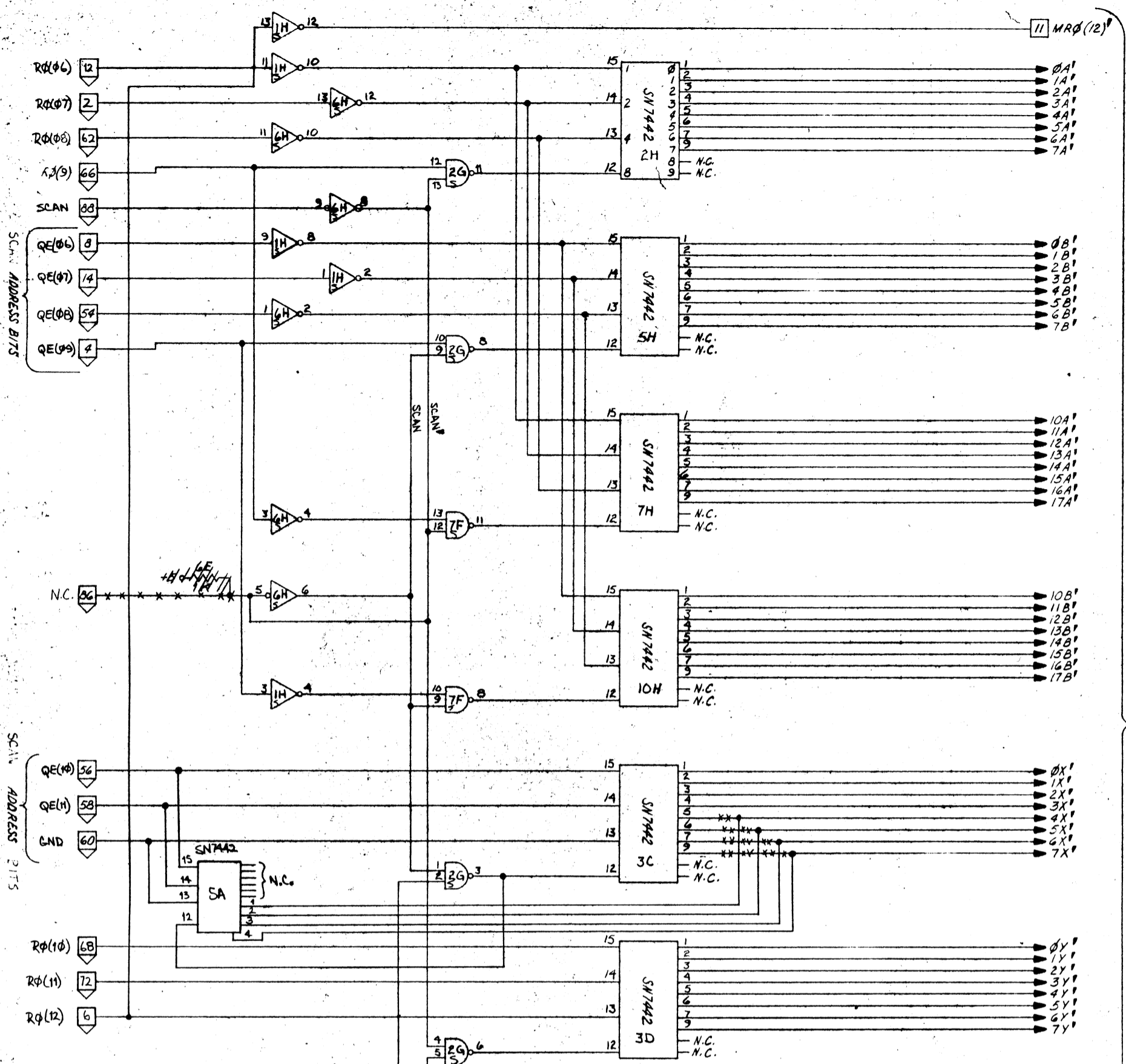
NO.	RELEASED	DESCRIPTION	REVISION	DATE	NAME	APPROVED
1				6-10-70	MM	

32 WORD SCRATCHPAD
BITS (0-23)
32 (16-23)

A 11 (00-07)
20 (08-15)
32 (16-23)



NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCE VALUES ARE IN OHMS,
1/4W, 10%.



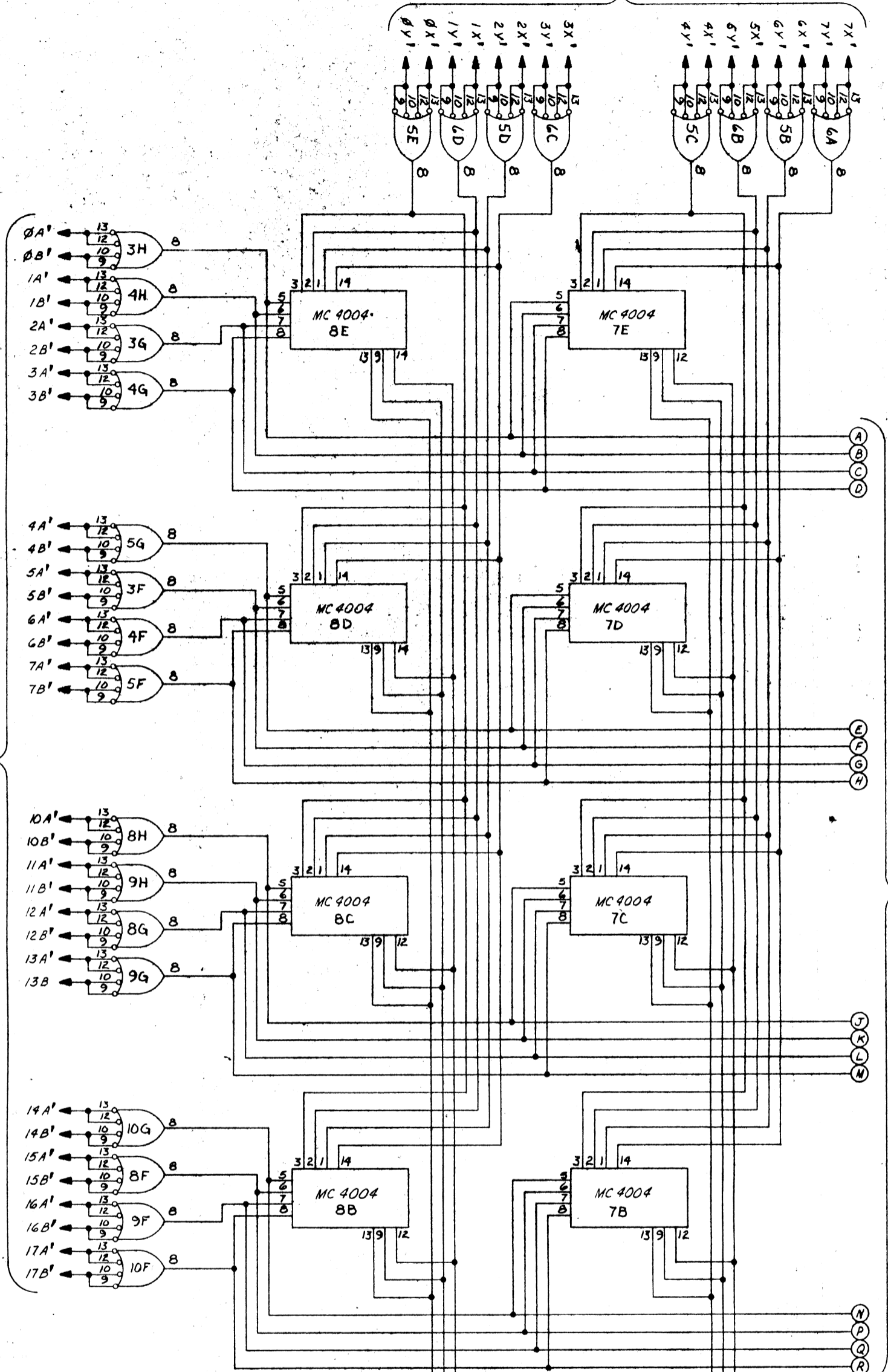
# 100668		RELEASED	
Berkeley Computer Corporation			
DATE	REV. NO.	ISSUED	BY
03/17/70	4-1-70		
FIRST USED ON M1 CPU-1.5			
MAP CONTROL # 2			
L00668.C			

NOTE: UNLESS OTHERWISE SPECIFIED:
 1. ALL RESISTORS ARE 1/8W, 10%.
 2. ALL CAPACITORS ARE CD 10070.
 3. ALL MC 9004'S HAVE TYP. PIN CONFIGURATION AS SHOWN ON SHT 2

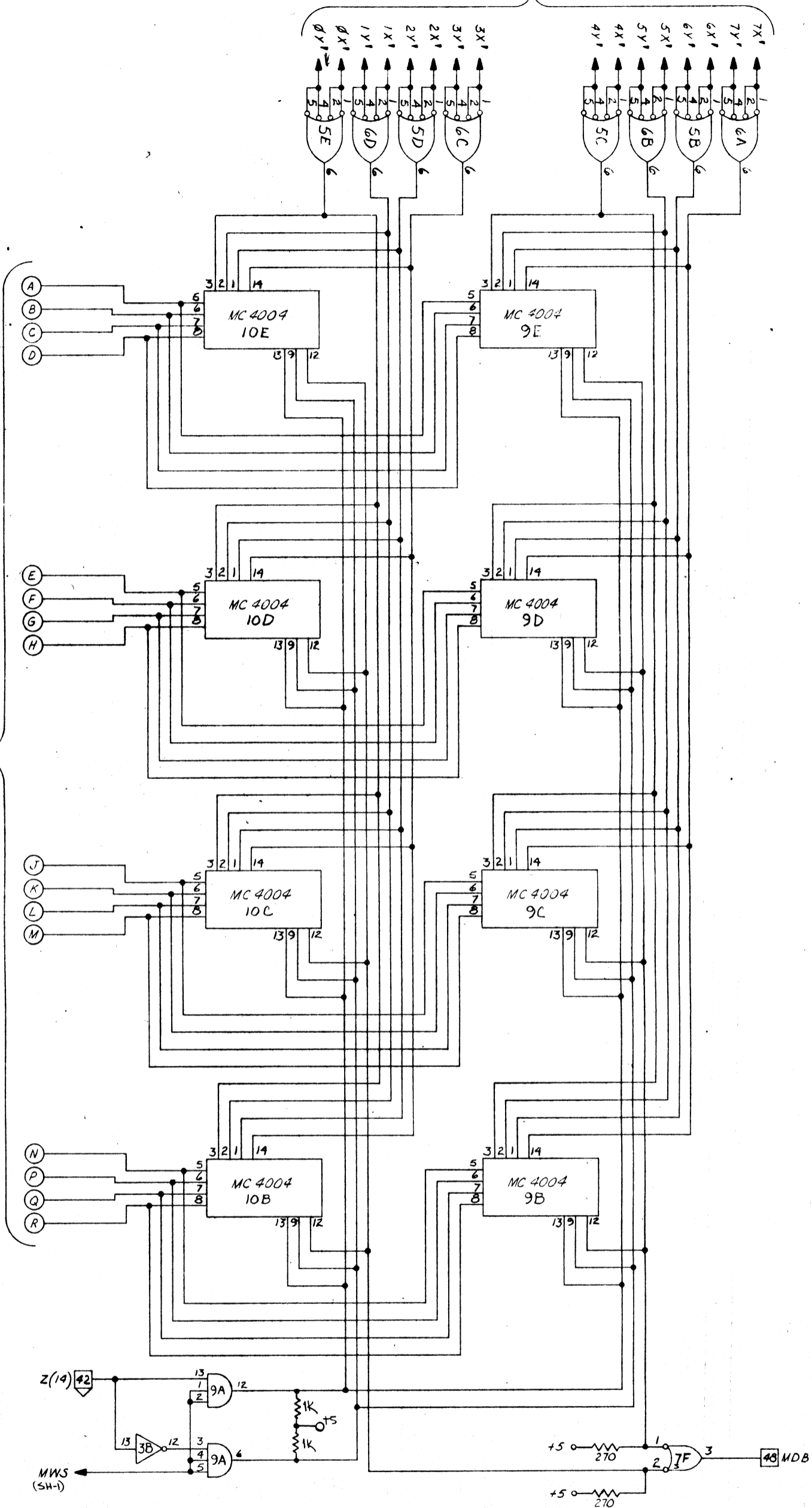
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 101, 103, 105, 107, 109,
 108, 110, 112, 6

1, 3, 5, 7, 9, 41, 43,
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127 TRU 156
 CD 10070
 TYP. PLCS
 +5
 GND



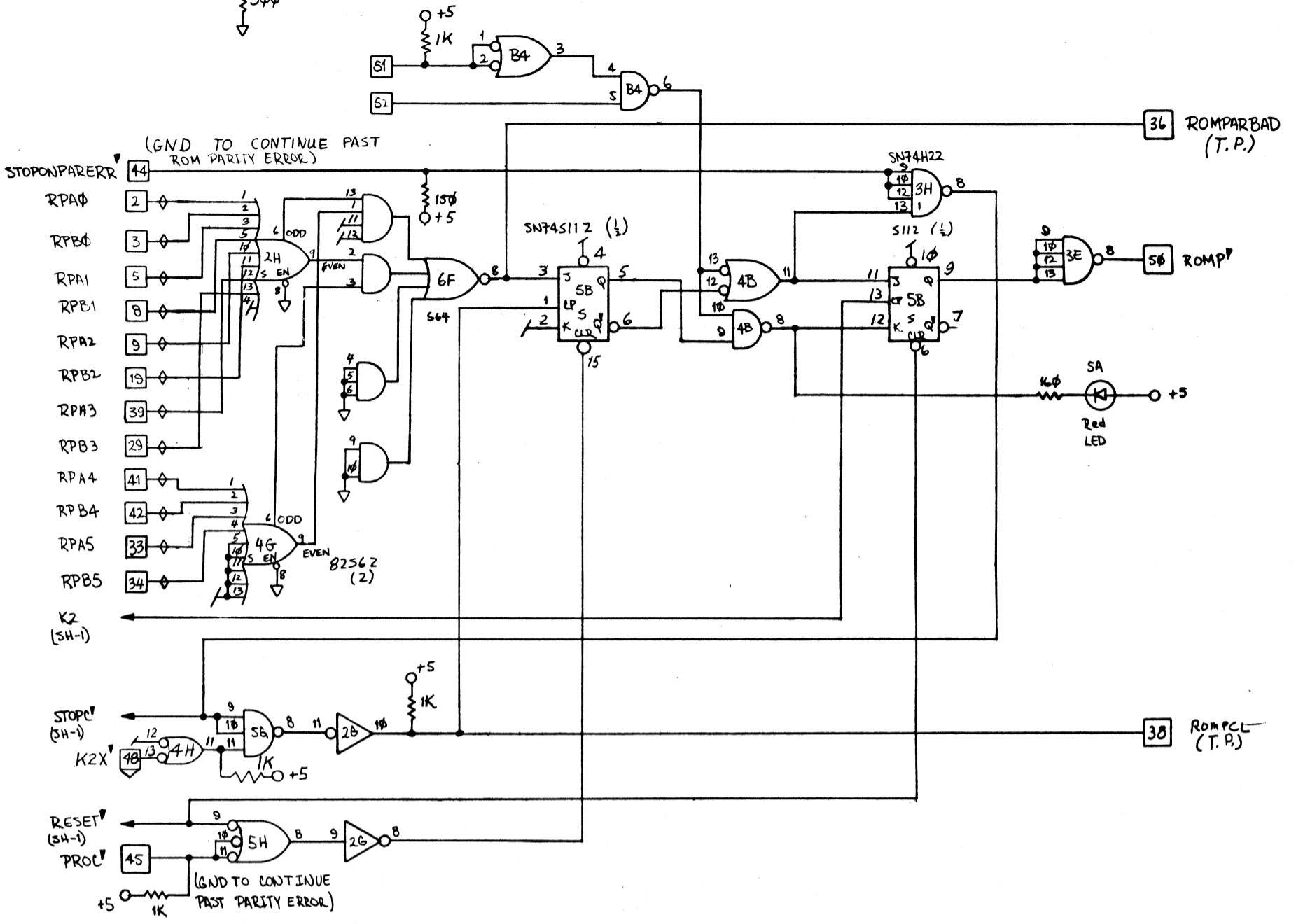
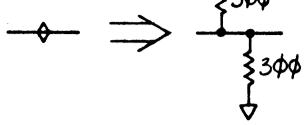
100868		RELEASSED	
 Berkeley Computer Corporation		TITLE: MAP CONTROL # 2	
DATE: 6/17/70	REV. CHG'S: 3	DESIGNER: MWS	APPROVER: SHT 1
DATE: 4-1-70	REV. CHG'S: 4	DESIGNER: MWS	APPROVER: SHT 1
PROJECT: FIRST USED ON M1 CPU-15		PART NO: 100868 . 2	



SHEET #3

L00665			
BERKLEY Computer Corporation		RELEASED DATE: 1/17/72 BY: [Signature] FOR: [Signature]	
REVISIONS NO. 4 DATE: 4/4/72 BY: [Signature]		TITLE MAP CONTROL # 2	
PRODUCT FIRST USED ON M1 CPD-1.5		PART NO. L00668 . C	

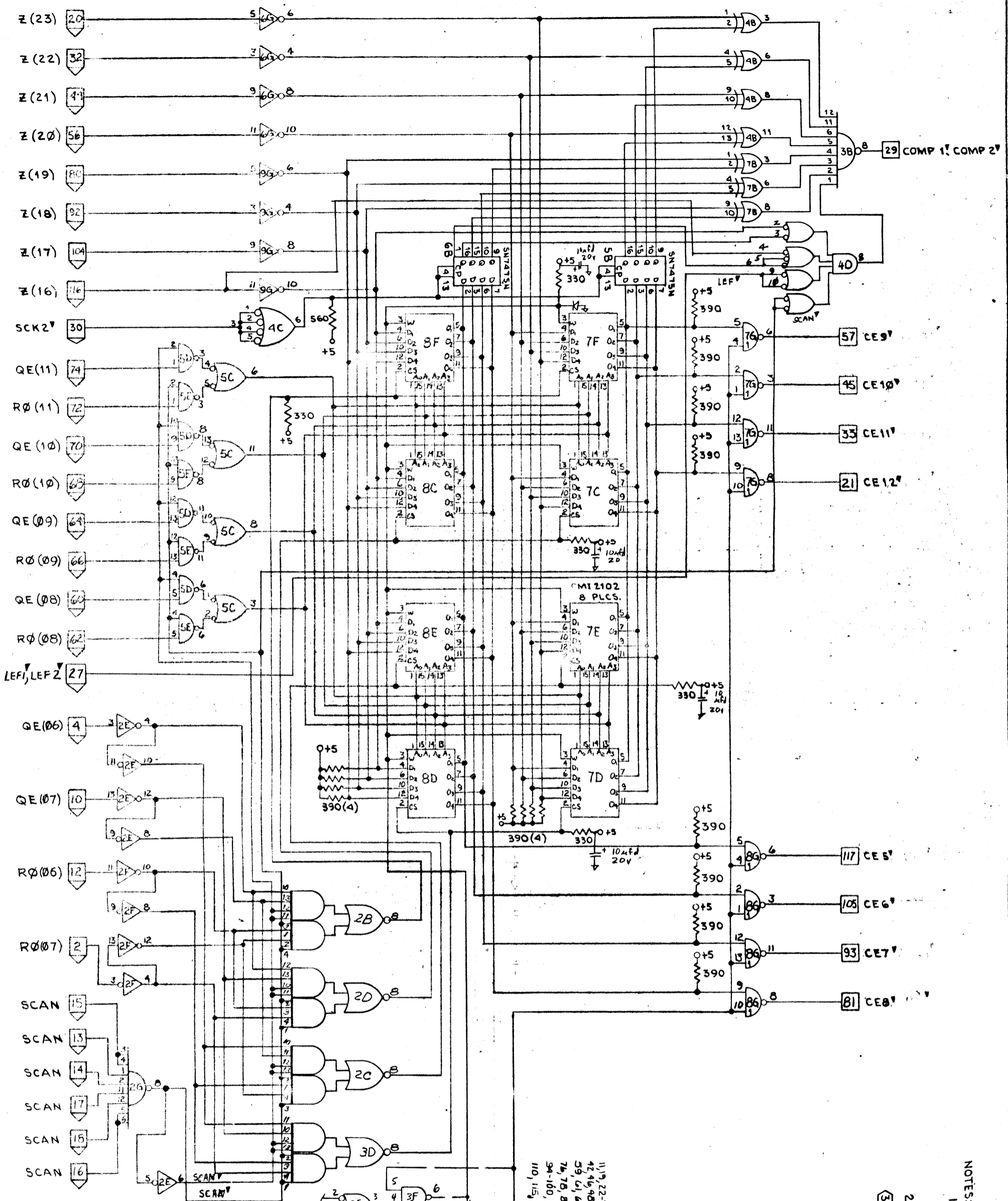
Note:



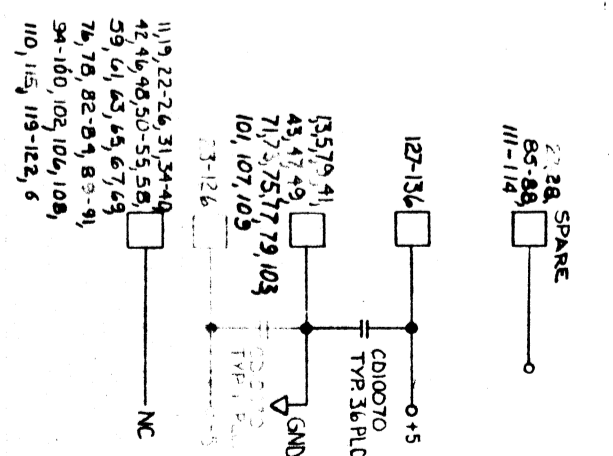
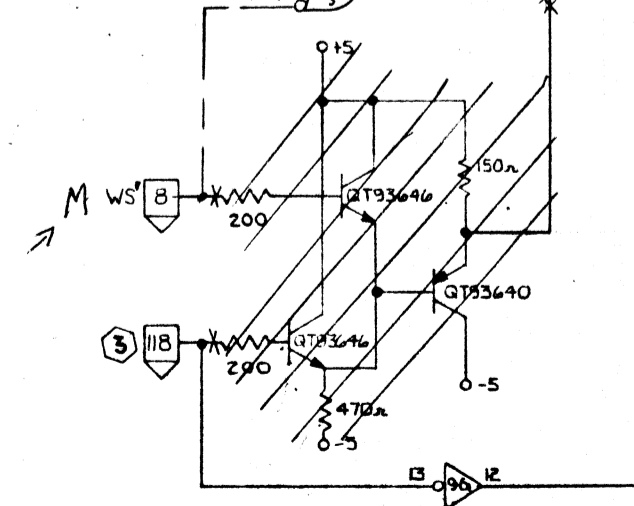
AM

more current returns
669.1 missing

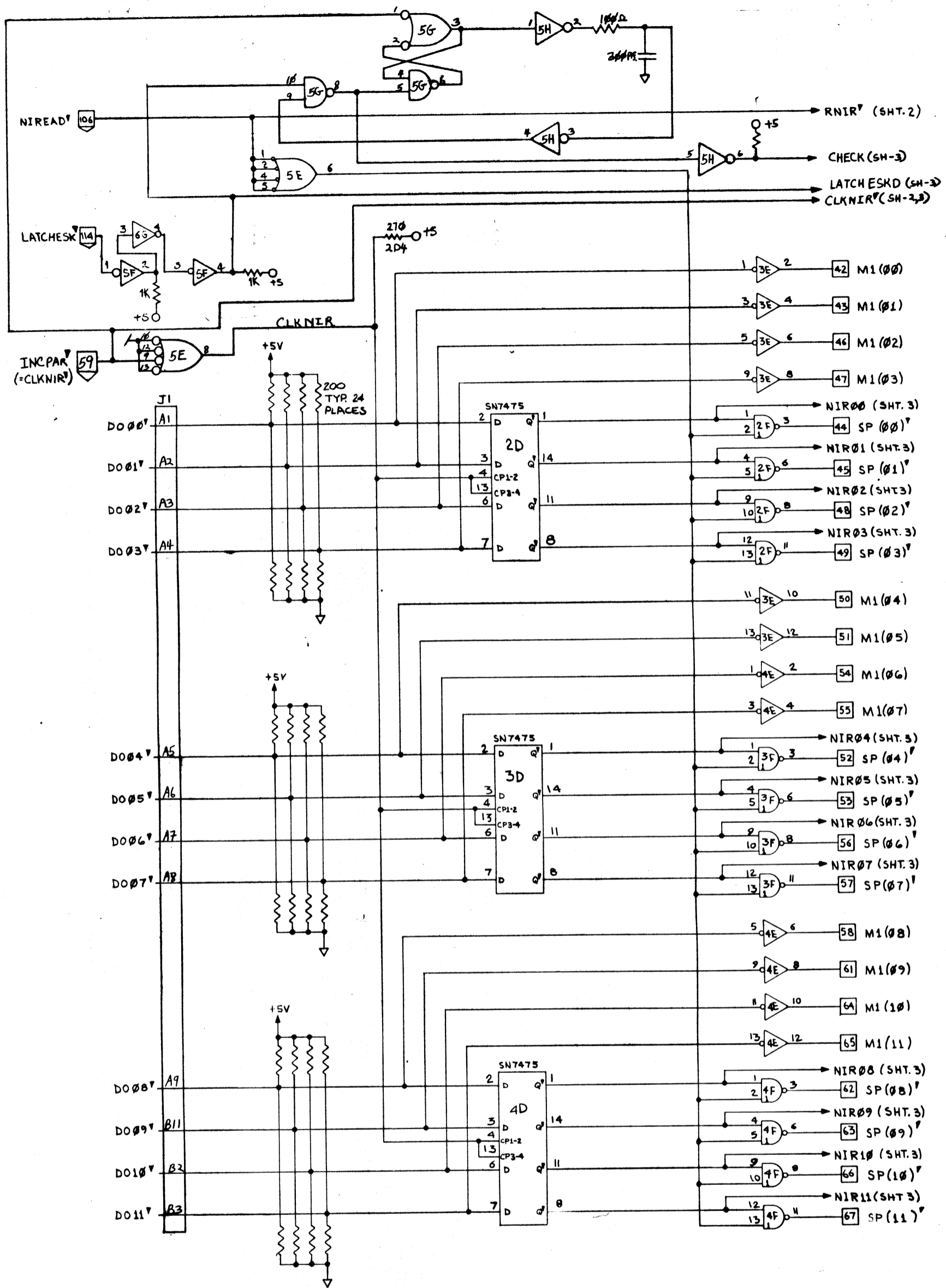
DESIGNED D. Dodge DRAWN R. E. BISON CHECKED SCALE 2 2 L66669.C	TITLE MAP CONTROL #3 PROJECT M1 CPU1.5 REV. 2 2
REVISIONS 1 RELEASED LATEST REVISIONS 4/26/74 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20	DATE DRAWN APPROVED



L00384			
DATE	REVISED	DESCRIPTION	TITLE
7-22-70	DW	MAP REGISTER #1 & #2	
5-10-70	MW		
C SWITCHED INPUTS TO 4B & 7B B CHANGE SIGNAL NANTES			
A15, A16 7-22-70 DW 5-10-70 MW			
MAP REGISTER #1 & #2 FIRST USED ON M1 CPU-15			
L00384			



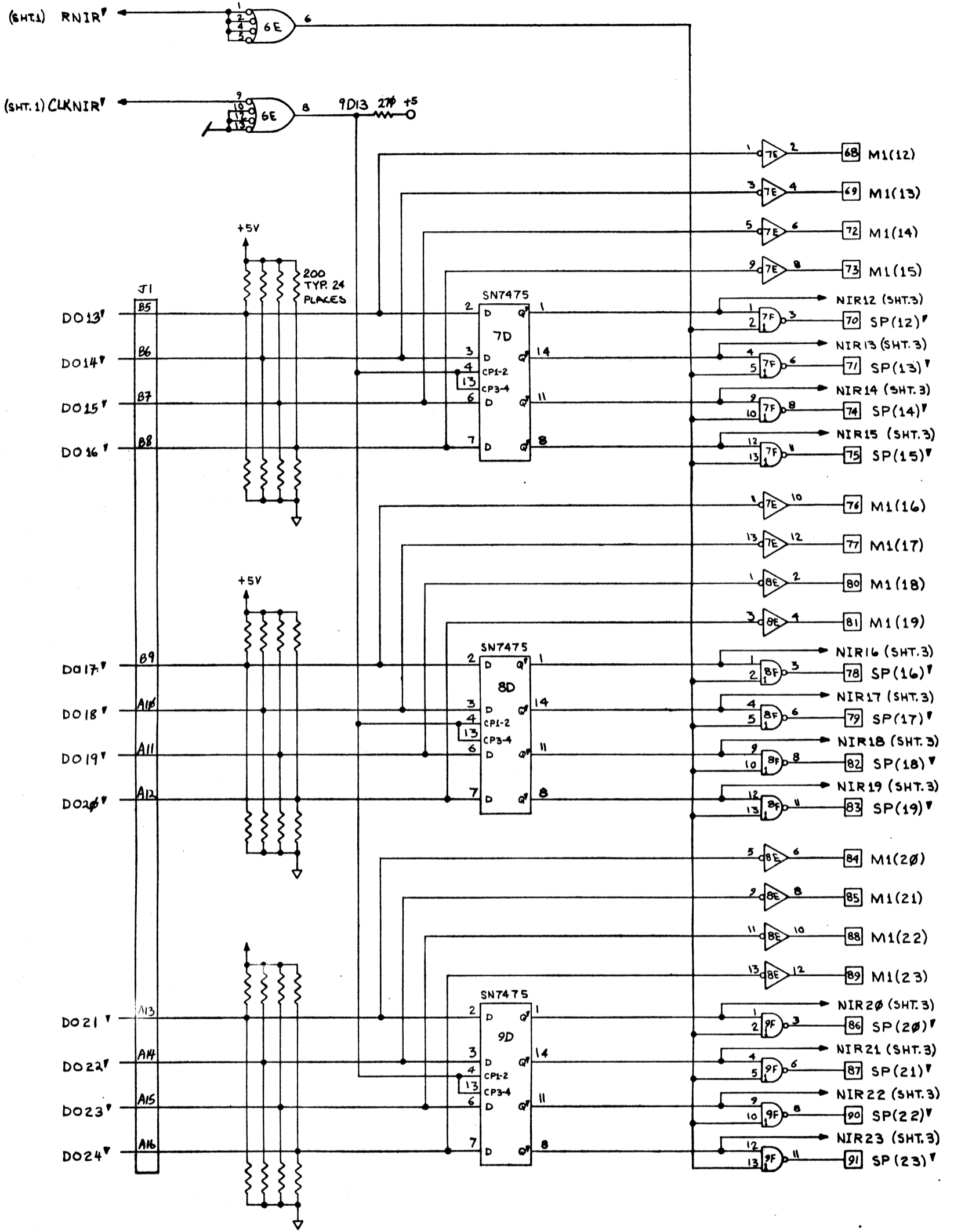
NOTES: UNLESS OTHERWISE SPECIFIED,
 1. ALL RESISTANCE VALUES ARE IN OHMS,
 1/4W, 10%.
 2.
 ③ MAP REGISTER #1 (A15) - R0 (12)
 MAP REGISTER #2 (A15) - MR0 (12)



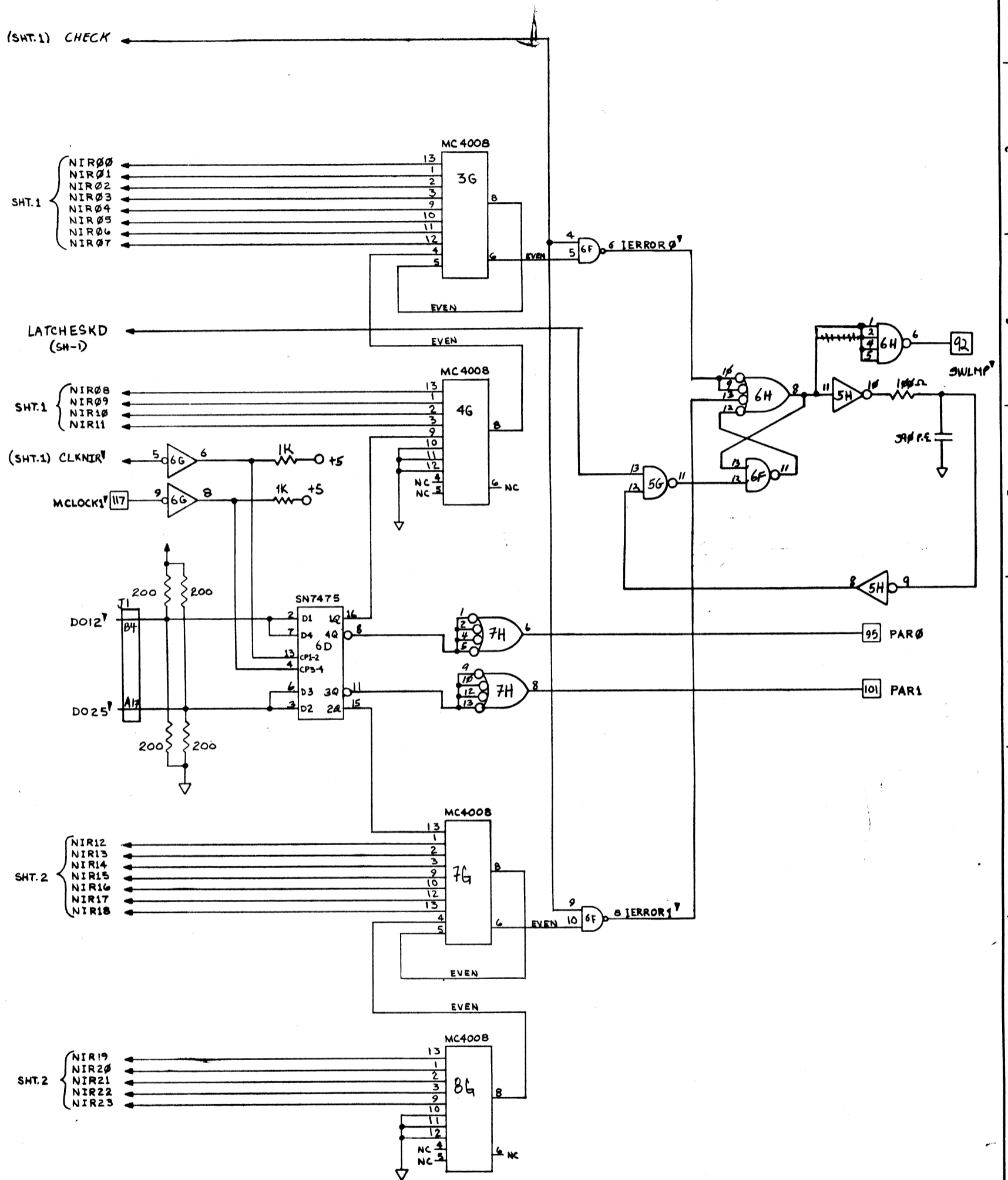
LDMARROA ⁸
 LDMARY ¹⁵
 LDMARROB ³²

127-136 □ TYPICAL PLCS. +5V
 □ CD10070 GND.
 1, 2, 19, 20, 39
 40, 3, 4, 5, 6, 93
 94, 96, 97, 98, 121
 122, 123, 124 NOTES:
 64, 100, 119, 120
 1. UNLESS OTHERWISE SPECIFIED
 ALL RESISTORS ARE 200-Ω 1/8W, 10% CARBON COMP.

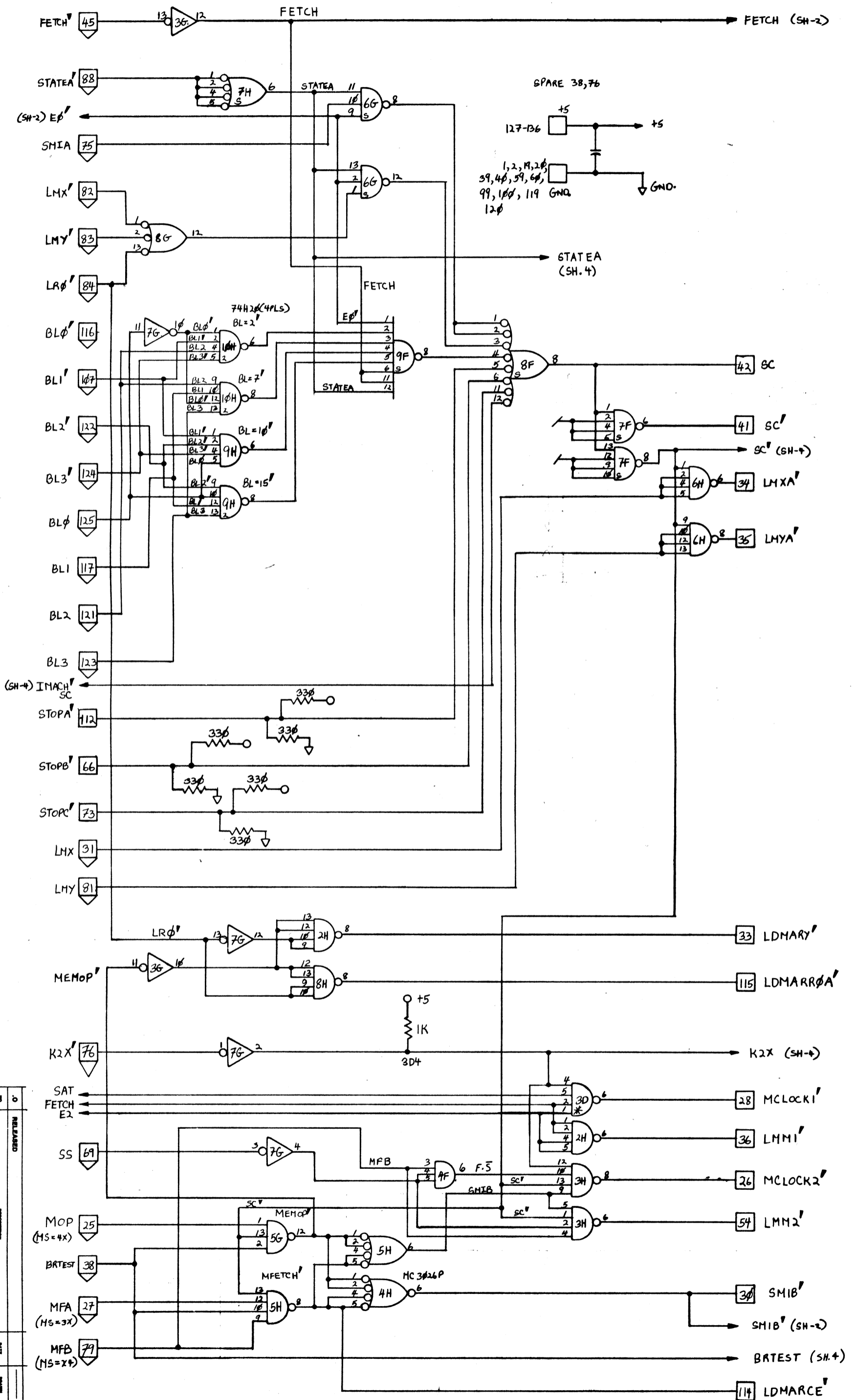
L00664		REVISION	
Berkeley Computer Corporation		1	3
THACKER		IFU NIR & DATA RECEIVER	
ALM 6-18-70		CPU 1.5	
L00664 .3		A21	



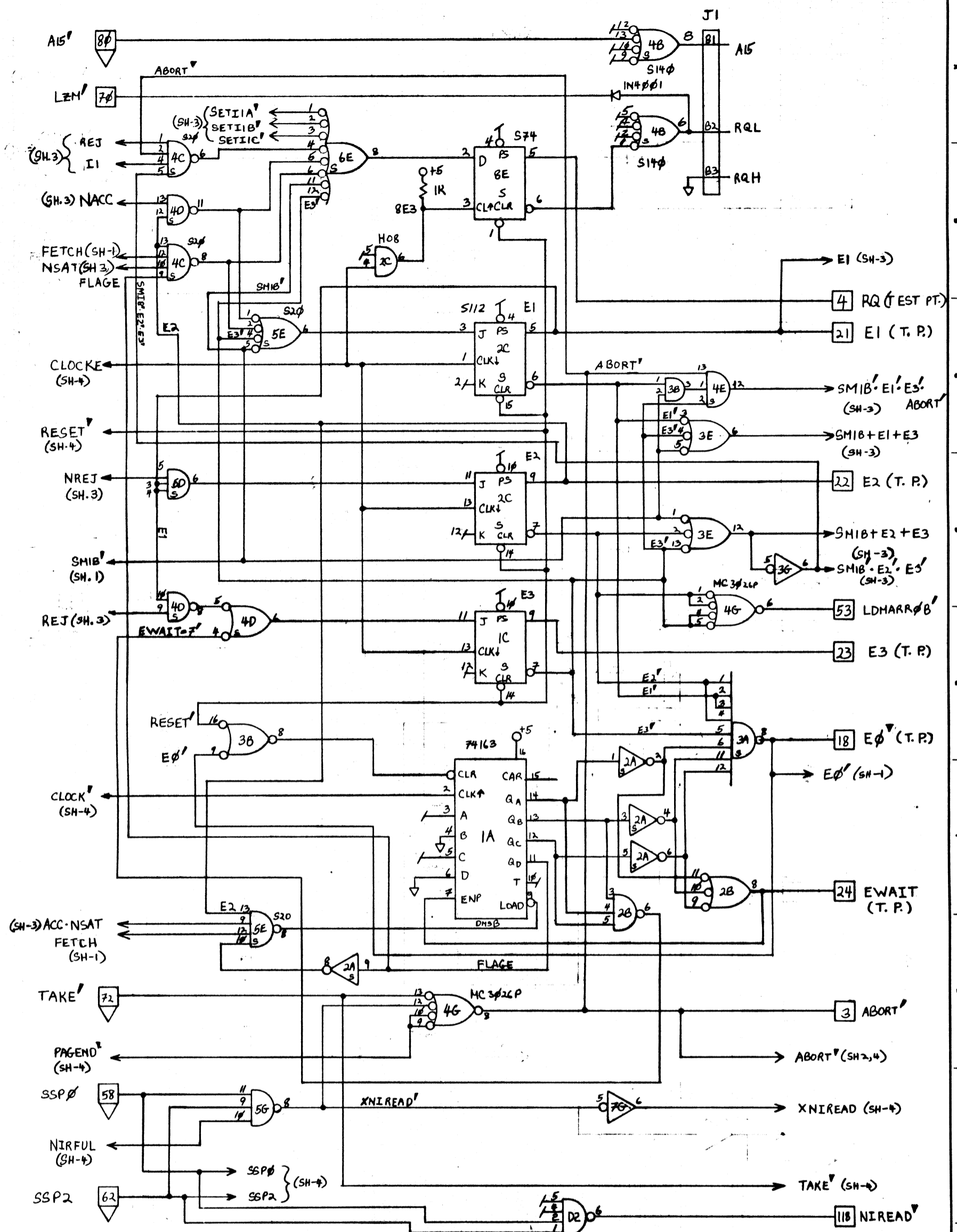
L00664	
THACKER ALM C-18-70 2	IFU NIR & DATA RECEIVER CPU1.5 A21 3
RELEASED DATE BY APPROVED	REVISIONS DATE BY APPROVED



00		L00664	
RELEASED LATEST REVISIONS 1/25/74			
DESIGNED BY THAKER		TITLE IFU NIR & DATA RECEIVER	
DRAWN BY ALM C-1870		REVISIONS	
CHECKED BY		3	
APPROVED BY		3	
DATE		L00664 . 3	
MATERIAL		CPU1.5	
PARTS FIRST USED ON		A21	
SCALE			
BERRY Computer Corporation			



L00663
 The Alpha System BCC-500
 D. JODGE
 M. MATSUYAMA
 A22
 IFU CONTROL
 1 4
 L00663.3



L0663

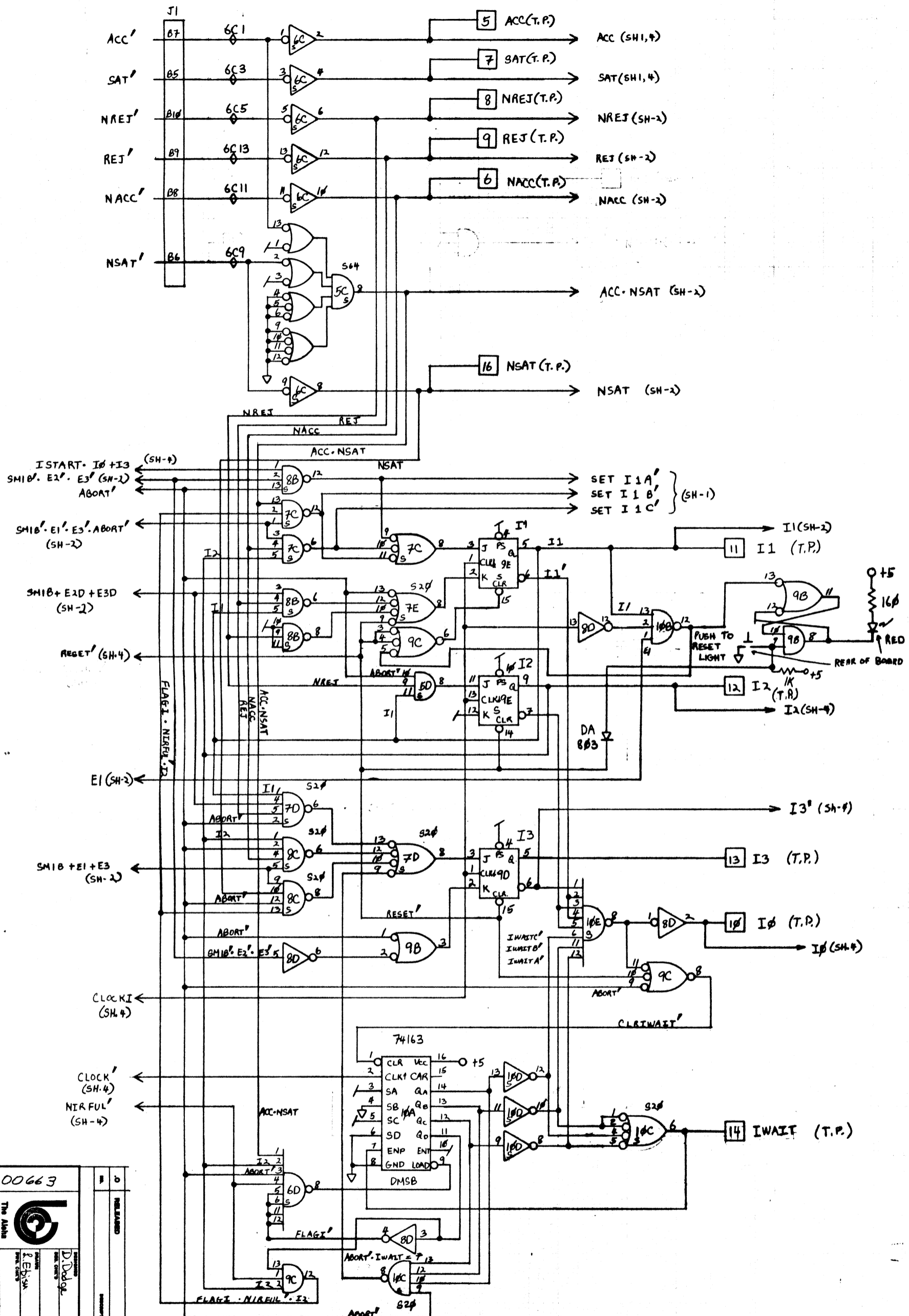
The Alpha System BCC-800

D. DODGE
M. MATSUMURA

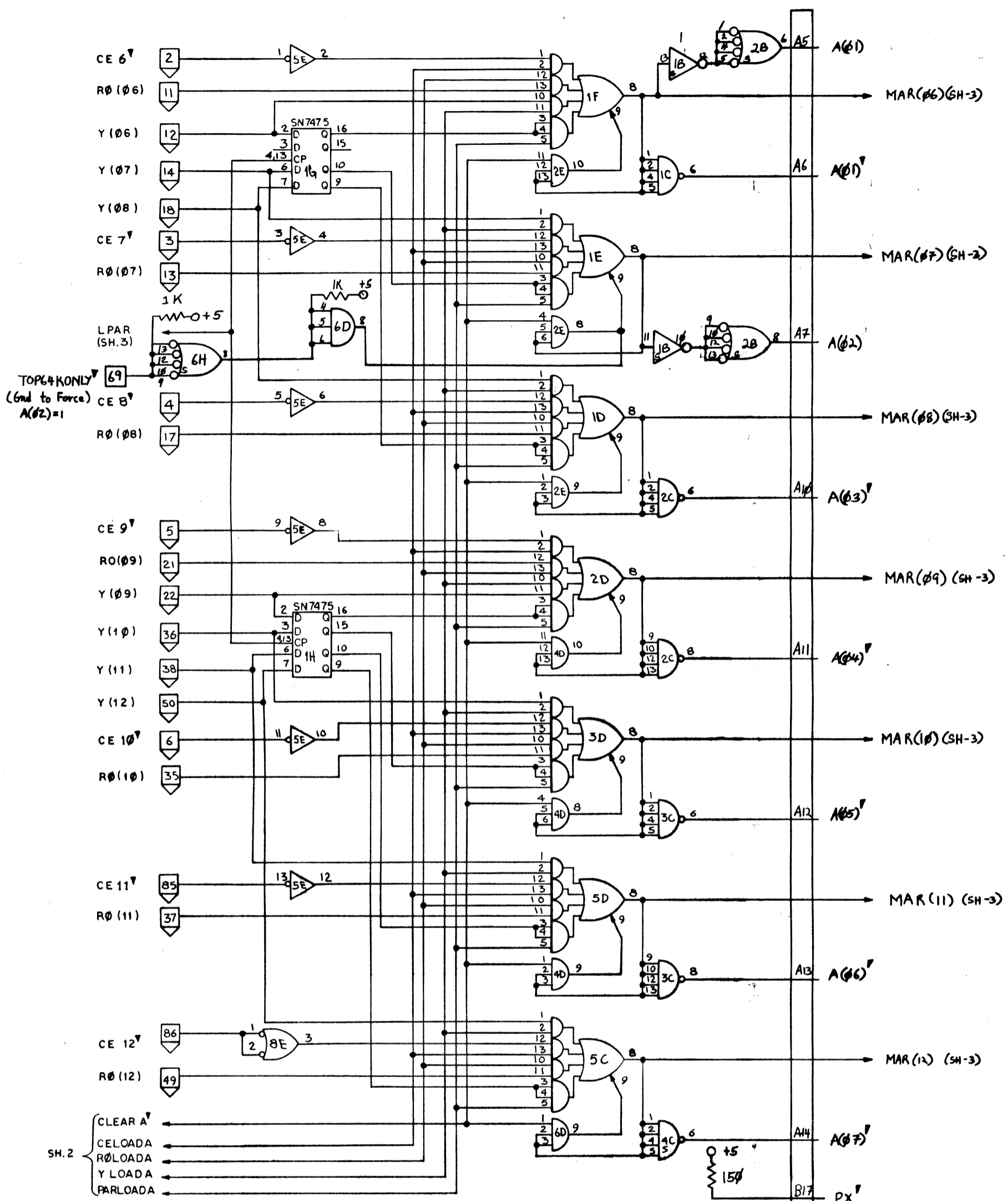
IFU CONTROL

2 4 L0663.3

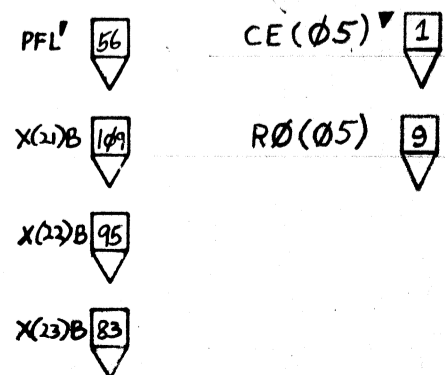
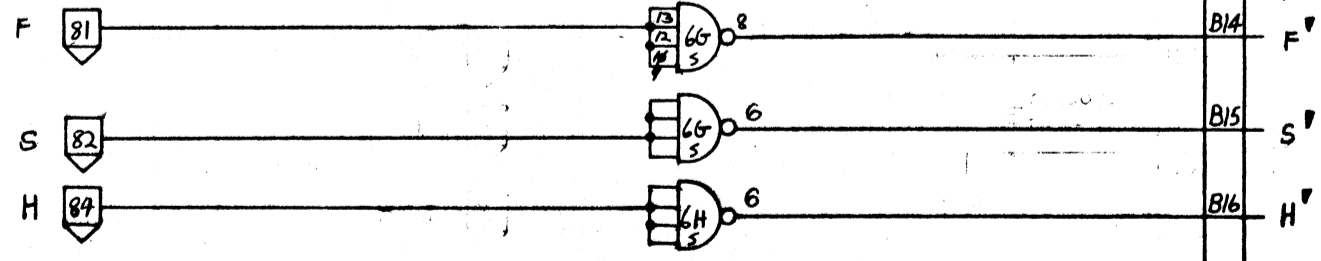
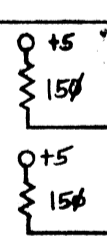
SSP1'	61	M(16)	92	M(21)	87	M(14)	94	M(10)	98	M(06)	104	M(02)	109
SSP3'	63	M(17)	91	M(22)	86	M(13)	95	M(09)	101	M(05)	105	M(01)	110
SSP4'	64	M(18)	90	M(23)	85	M(12)	96	M(08)	102	M(04)	106	M(00)	111
SSP5'	65	M(19)	89	M(15)	93	M(11)	97	M(07)	103	M(03)	108		



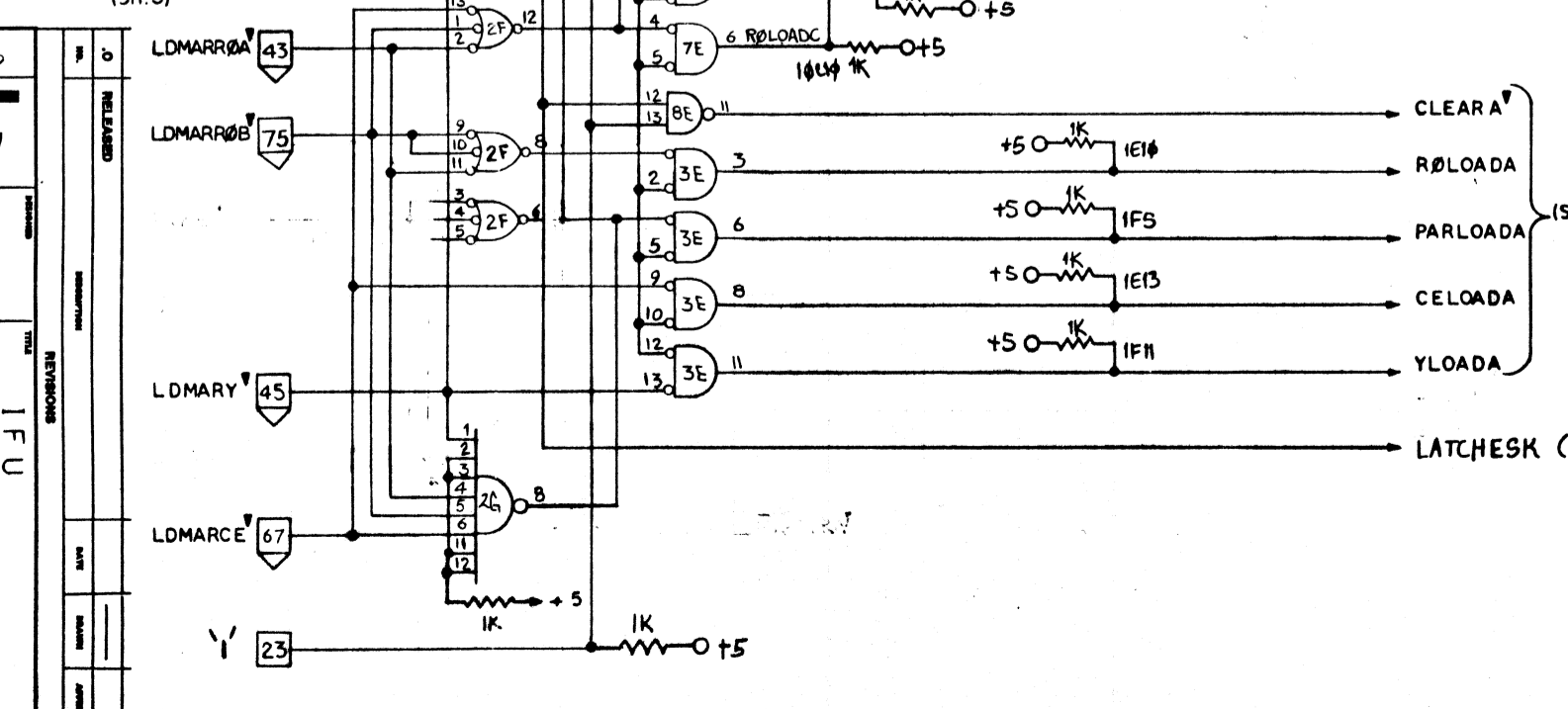
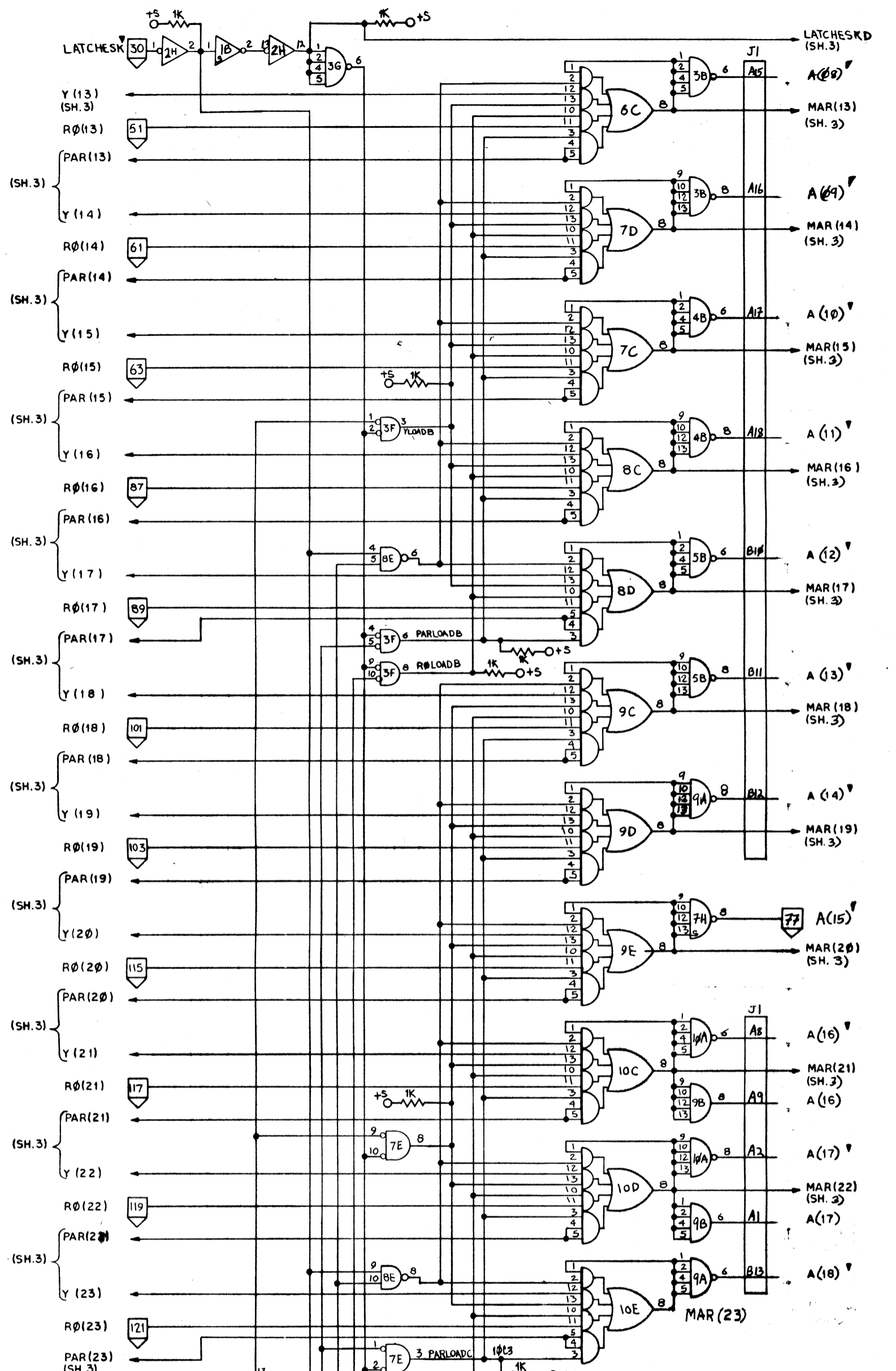
L00663		b	
The Alpha System REC-200		RELEASED	
D. Dodge		DATE	
REVISION		DRAWN	
3 4		CHECKED	
A32		APPROVED	
IFU CONTROL		TITLE	
L00663.3		PART	



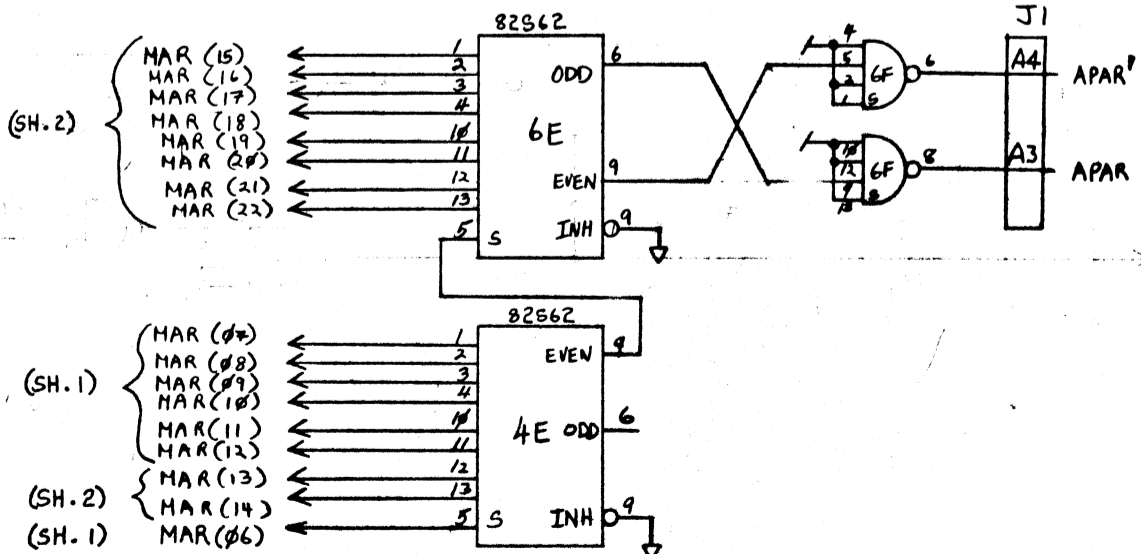
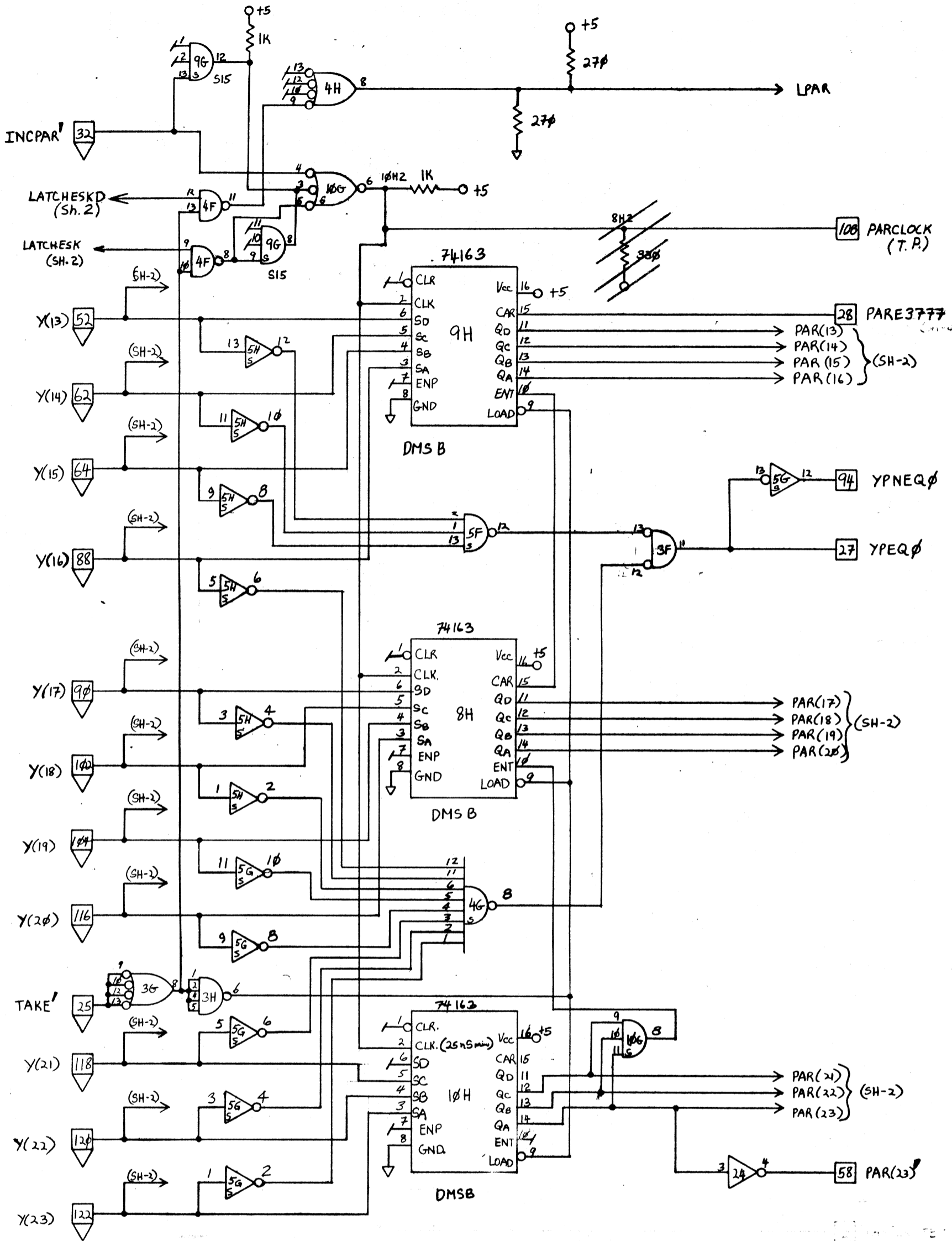
SH.2
 CLEAR A
 CELOADA
 R0LOADA
 YLOADA
 PARLOADA



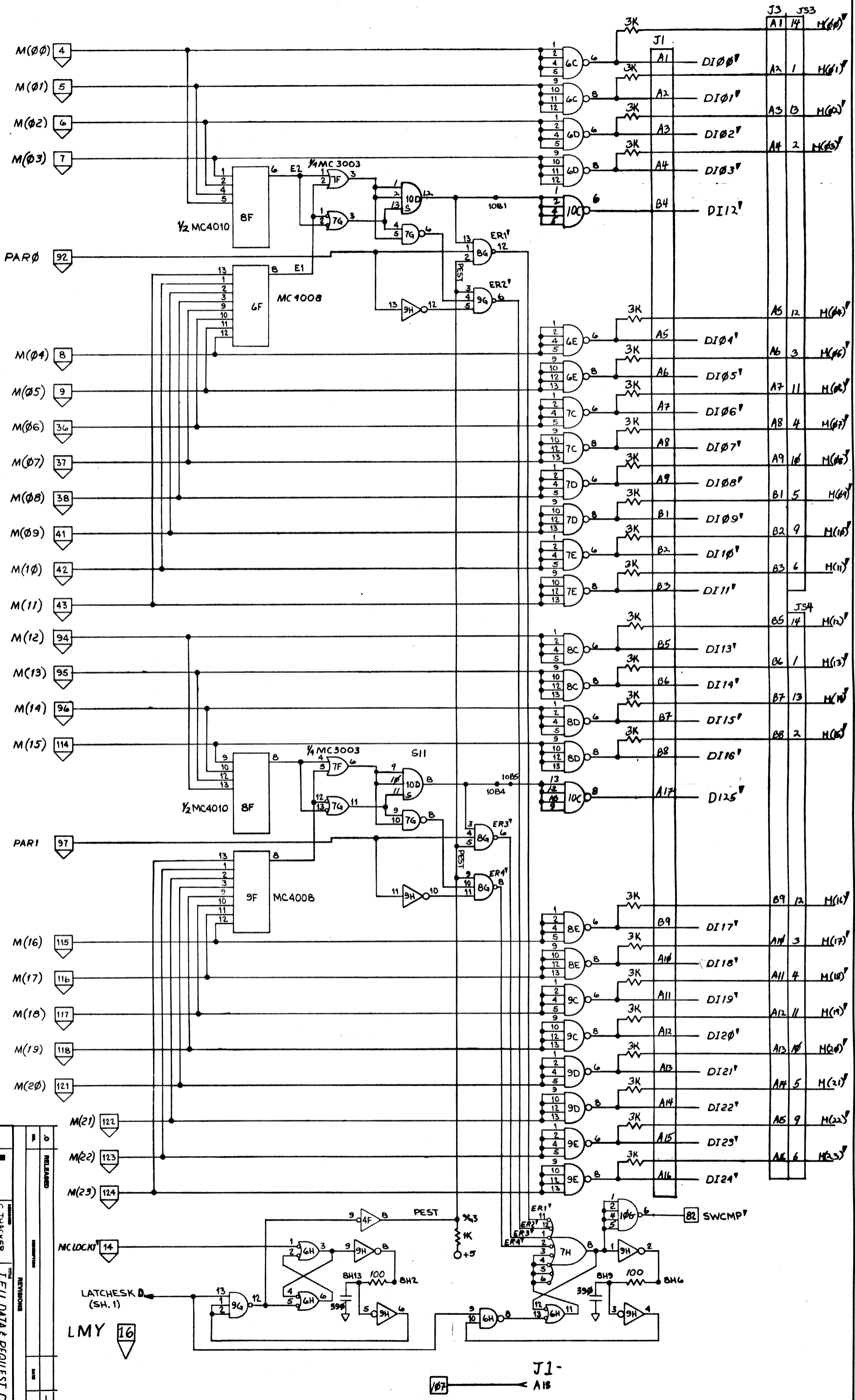
L00666		Q	RELEASED
		DATE	
SCALE	NONE	REVISIONS	
DATE	6-19-70	BY	
DESIGNER	M/M	CHECKED	
MAR-PAR A23		APPROVED	
FIRST USED ON CPU 1.5			
NO.	1		
REV.	3		
NO.	L00666		



L00666		REVISED
	DATE	REVISED
	DATE	REVISED
NONE	DATE	REVISED
2	DATE	REVISED
3	DATE	REVISED
I F U MAR - PAR A 23 FIRST USED ON CPU 15 L00666.4		



L00666	
DESIGNED BY	D. DODGE
DESIGNED BY	M. MATSUMURA
DATE	3 3
REV	3
REV	L00666-04
IFU MAR PAR	



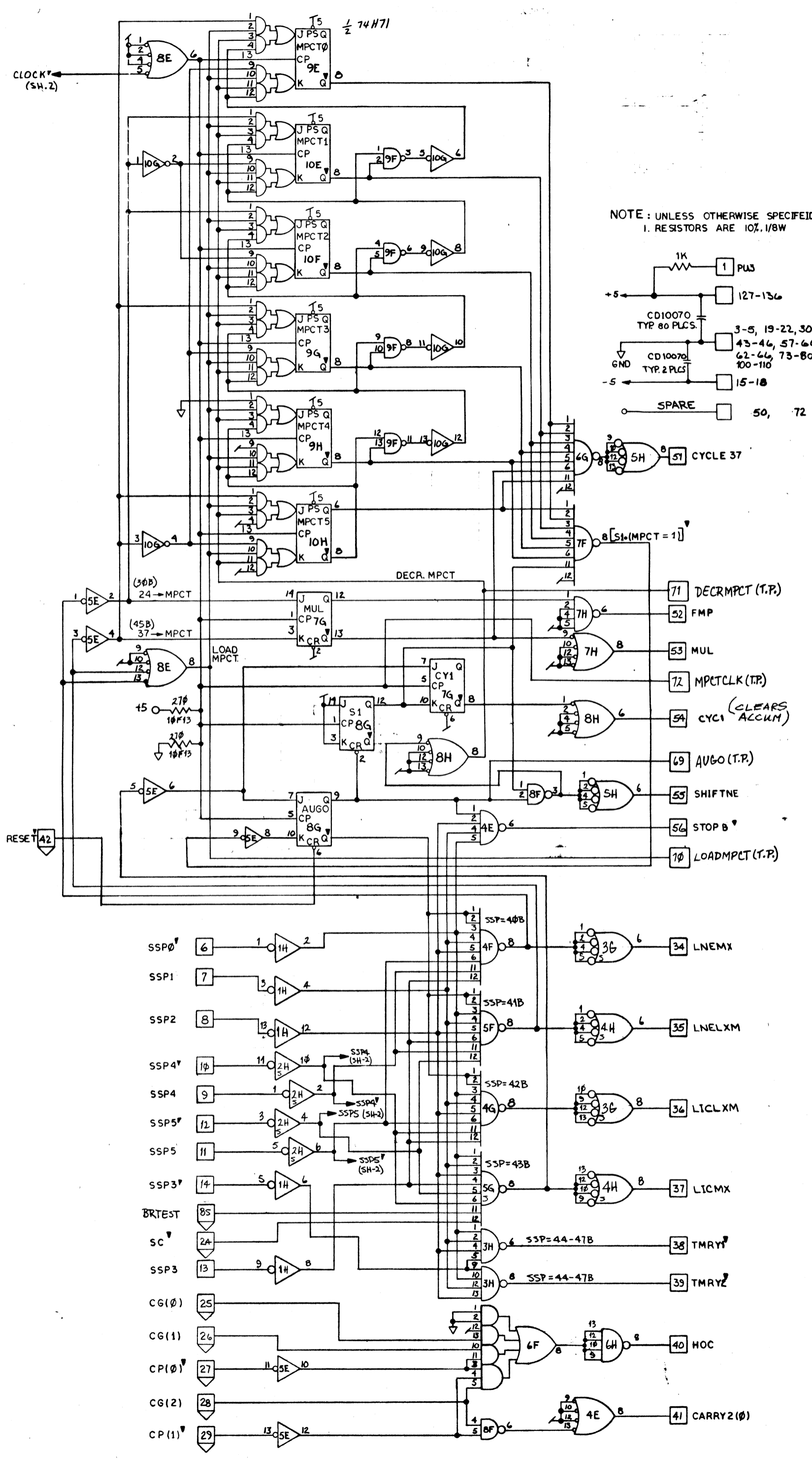
L00665
 Berkeley
 Computer
 Corporation
 C. THACKER
 6-18-70
 BOWMAN/WZ
 FIRST USED ON CPU1.5, M1 A24
 L00665 .3

REVISION	1	RELEASED
DATE		
BY		
APPROVED		

IFU DATA REQUEST DRIVER

LMY 16

J1-
A18

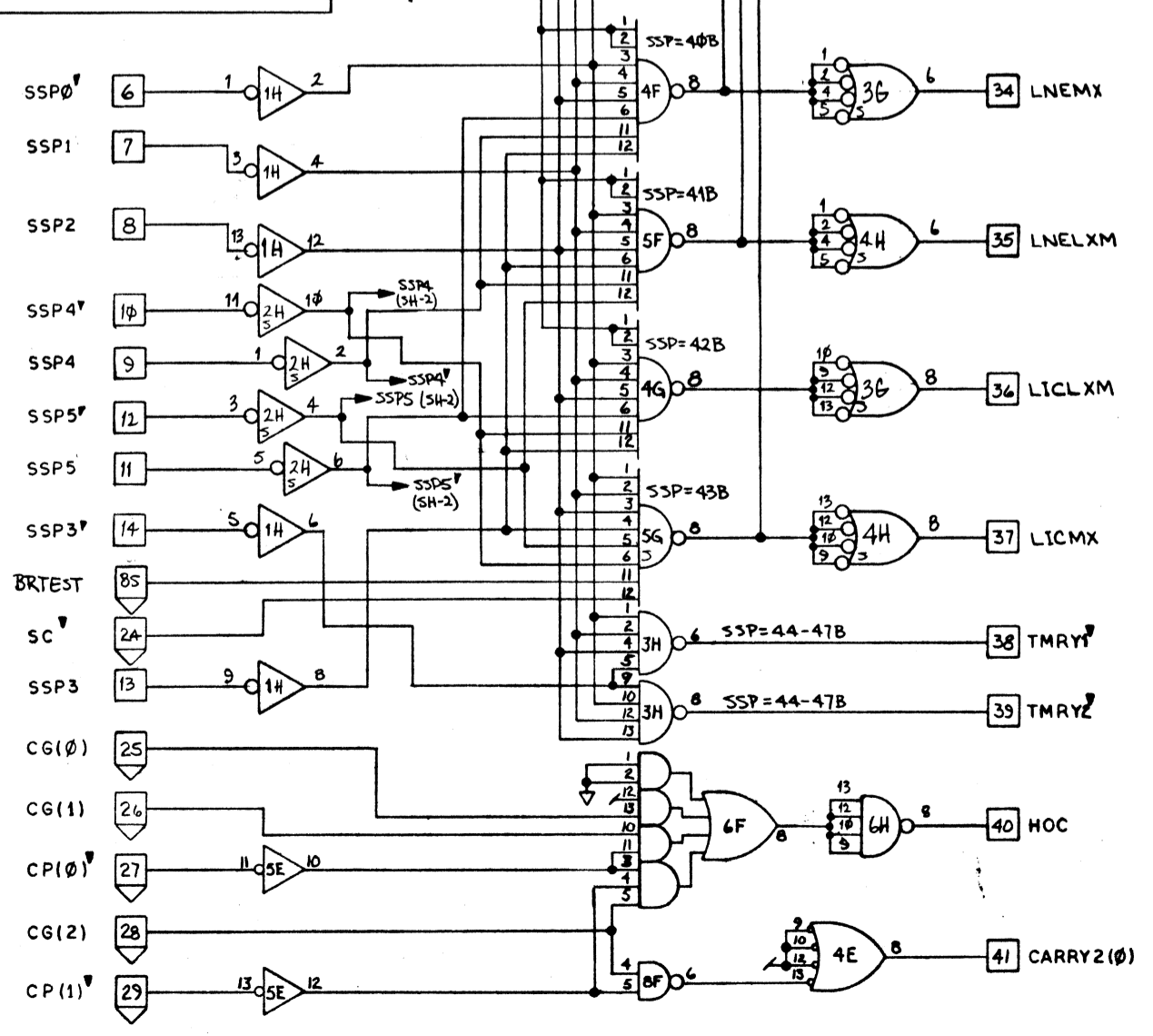


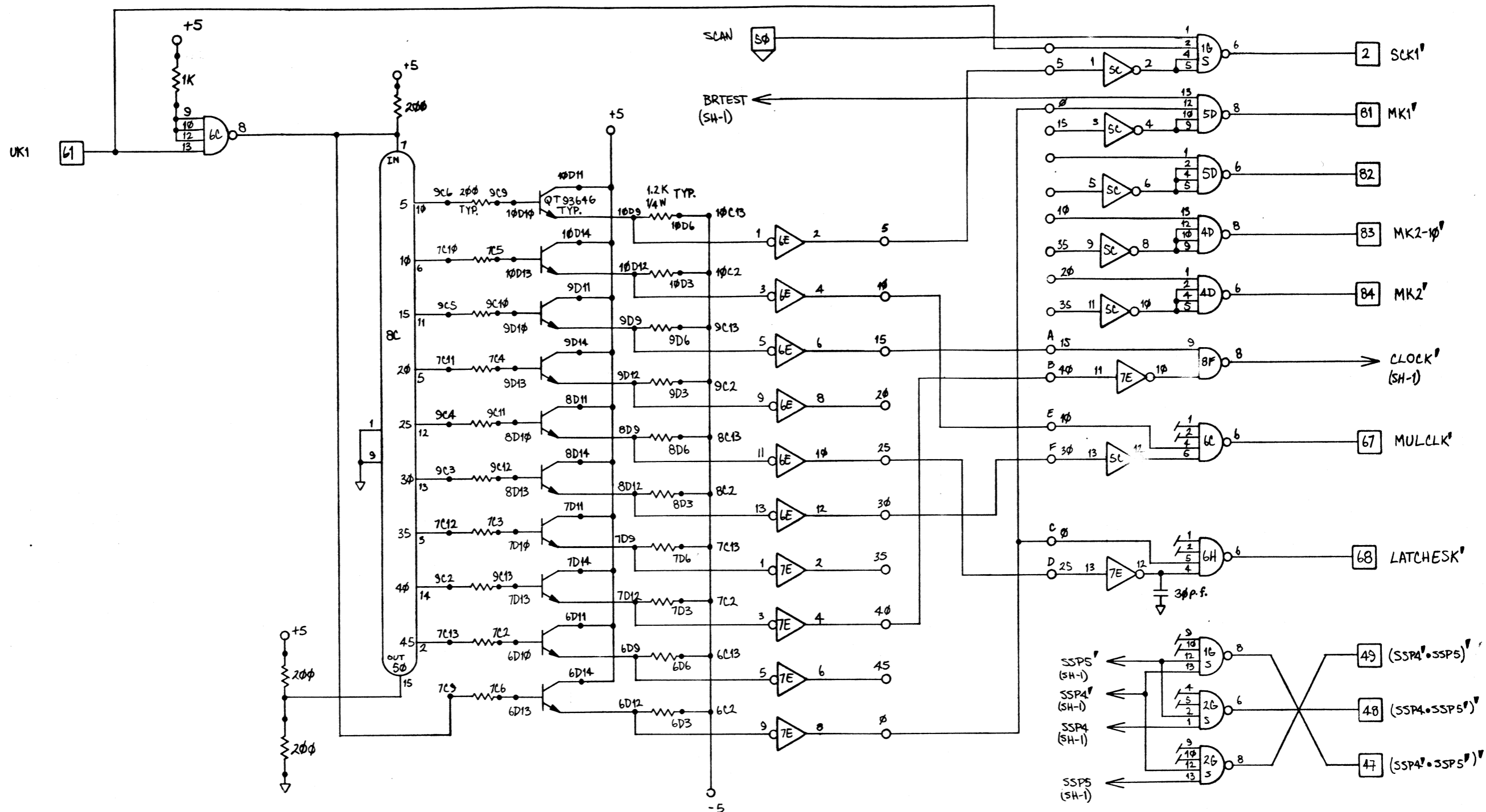
NOTE: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE 10% 1/8W

1K 1 PWS
+5 127-136
CD10070 TYP 80 PLCS 3-5, 19-22, 30-33, 43-46, 57-60, 62-66, 73-80, 100-110
GND CD10070 TYP 2 PLCS 15-18
-5 SPARE 50, 72

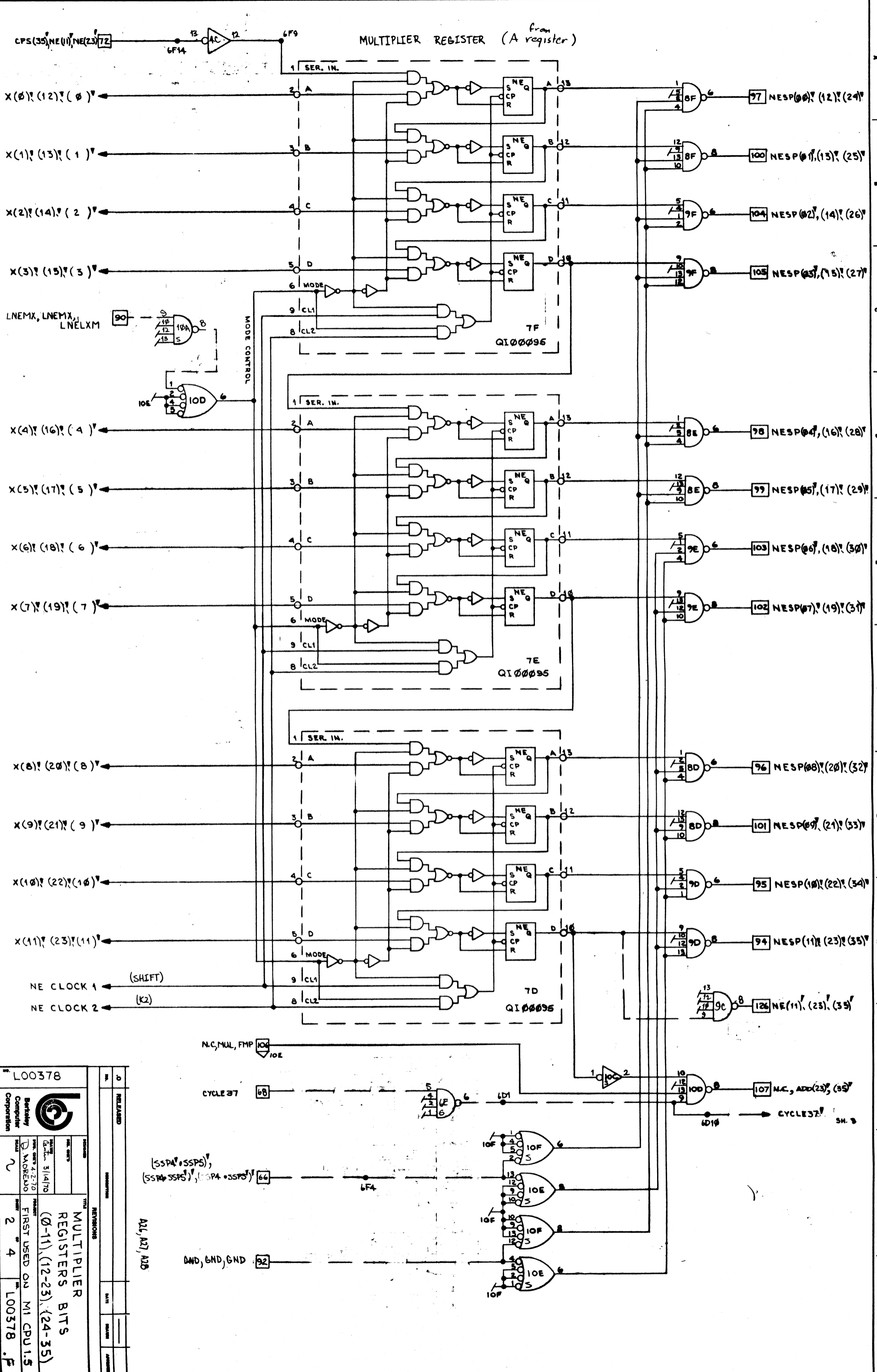
L00670		REVISIONS	
		N. COHLER DATE: 3/13/70 SCALE: 1/16"	
NONE FIRST USED ON M1 CPU 15 L00670 .C		TITLE: MULTIPLIER CONTROL	

0	RELEASED	DATE:	APPROVED:
1		DATE:	APPROVED:
2		DATE:	APPROVED:





.O RELEASED		DATE	DRAWN	APPROVED
NO.	DESCRIPTION			
REVISIONS				
DESIGNED	N. COHLER	TITLE		
DES. CHK'D		MULTIPLIER CONTROL		
DRAWN	J. EBISA	PROJECT		
DWG. CHK'D		ON M1 LPU 1.5		
SCALE	REVISED	SHEET	2 OF 2	NO. LΦ670.C



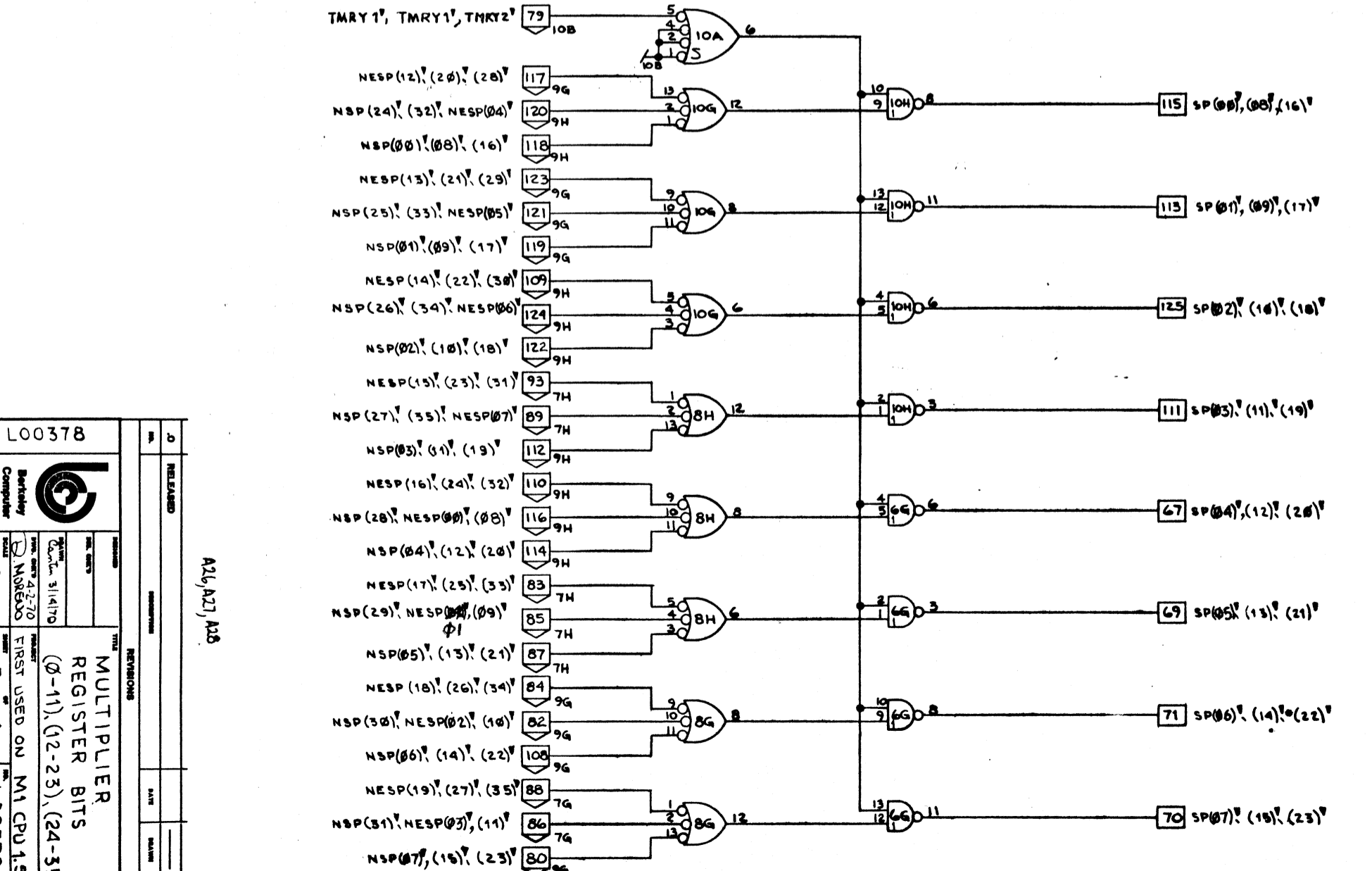
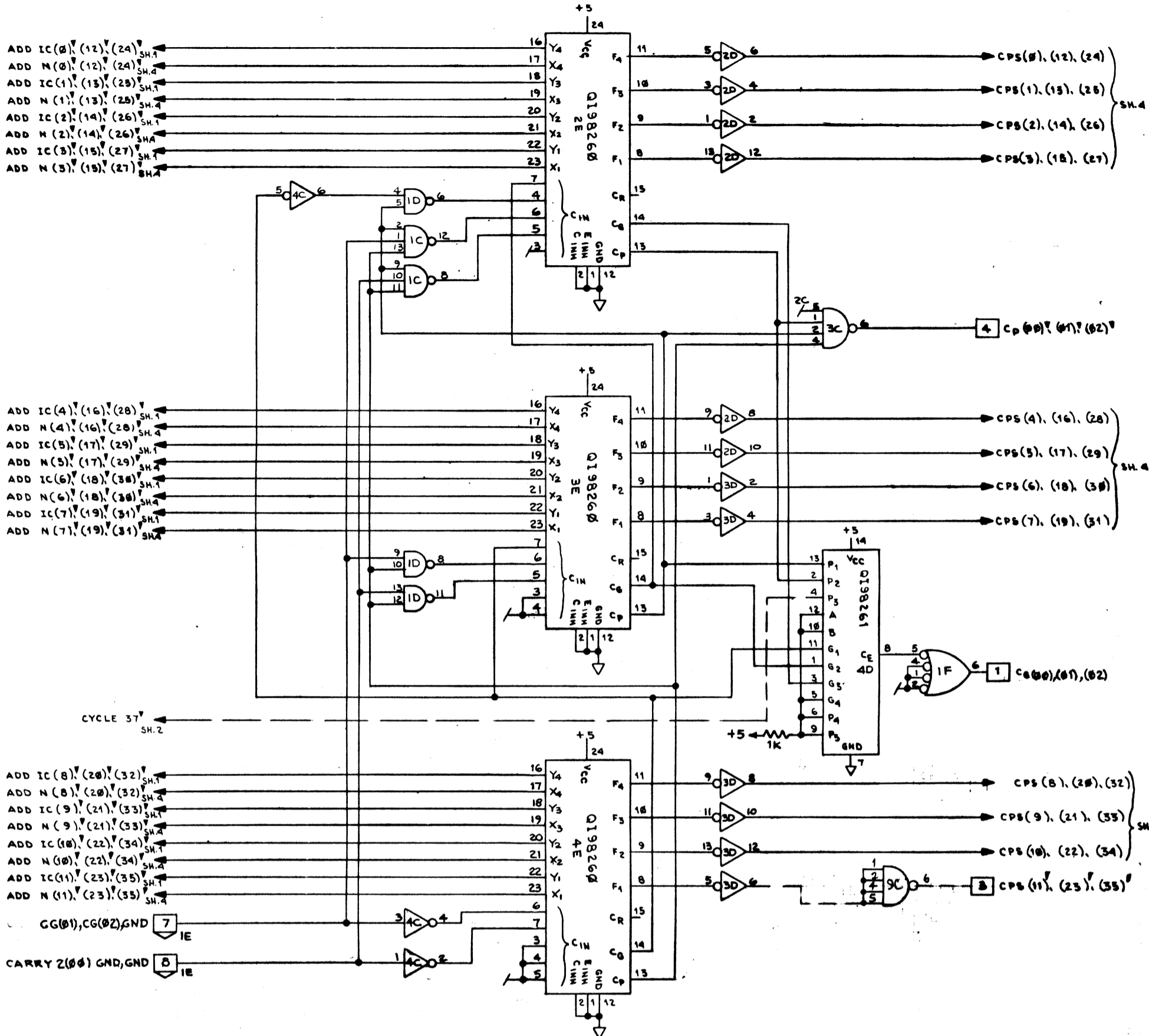
L00378		0	RELEASED
		1	REVISION
BERKELEY COMPUTER CORPORATION		2	DATE
DATE: 3/14/70 REV. 4-2-70 MADREDO		3	REVISION
TITLE: MULTIPLIER REGISTERS BITS (0-11), (12-23), (24-35)		4	DATE
FIRST USED ON: M1 CPU 1.5		5	REVISION
L00378		6	DATE

A4L, A27, A28

(SSPA + SSPB),
(SSPA + SSPB), (SSPA + SSPB)

DND, GND, GND

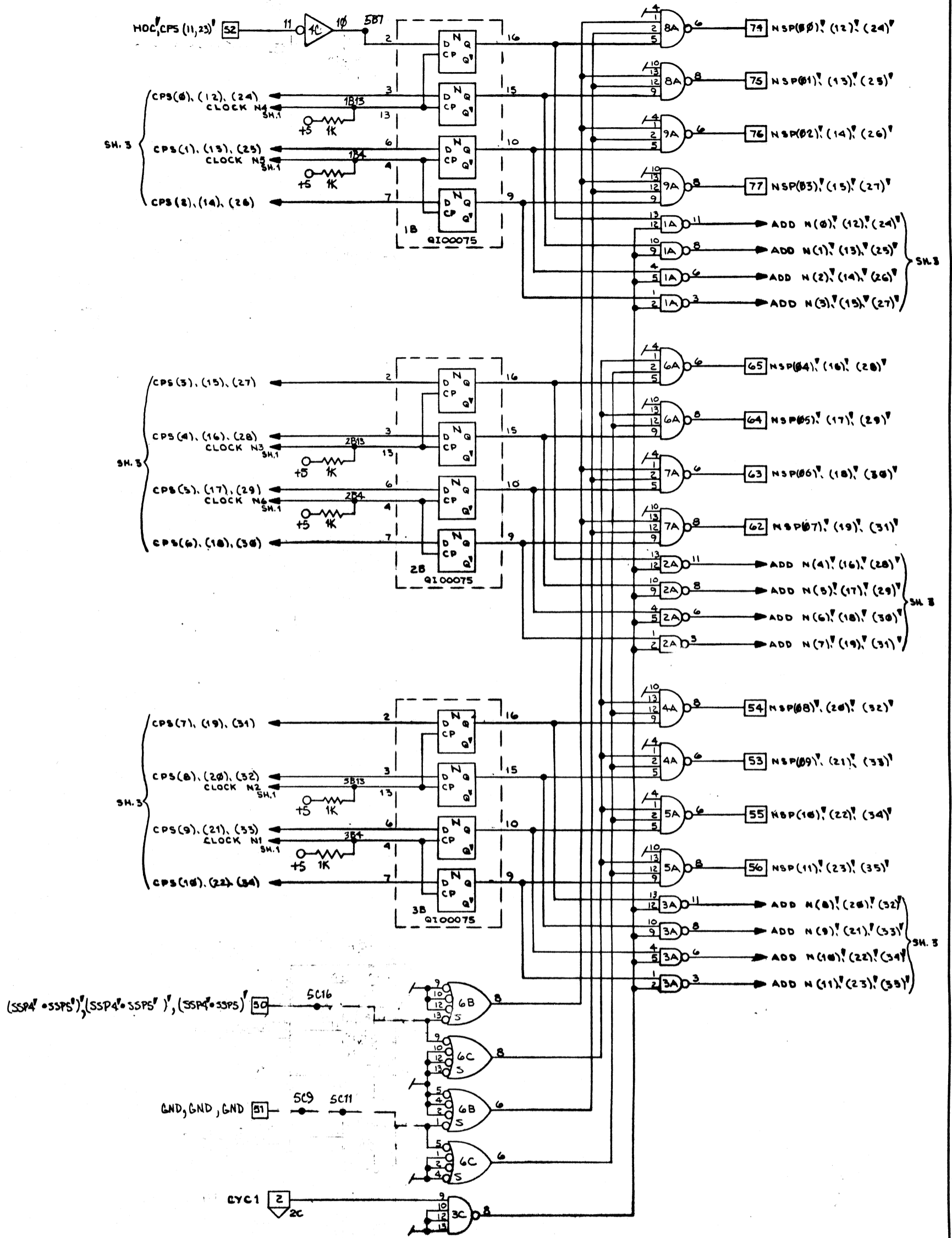
SH. 3



L00378
 RELEASED
 BATTERY COMPUTER CORPORATION
 MODEL 4-2-70
 PART 314170
 FIRST USED ON M1 CPU 15
 L00378

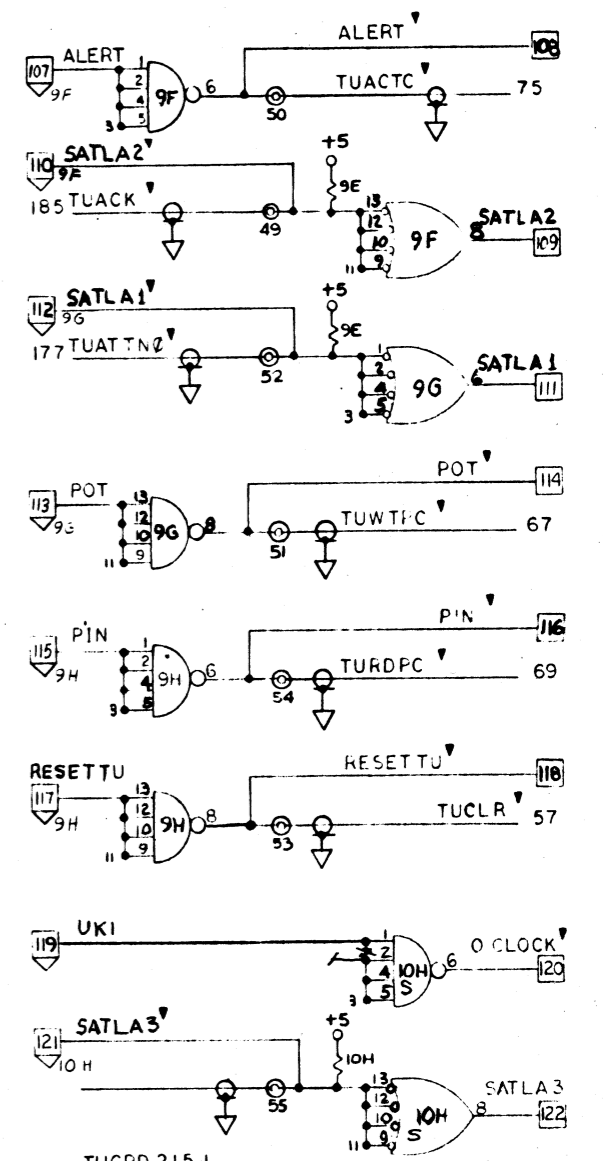
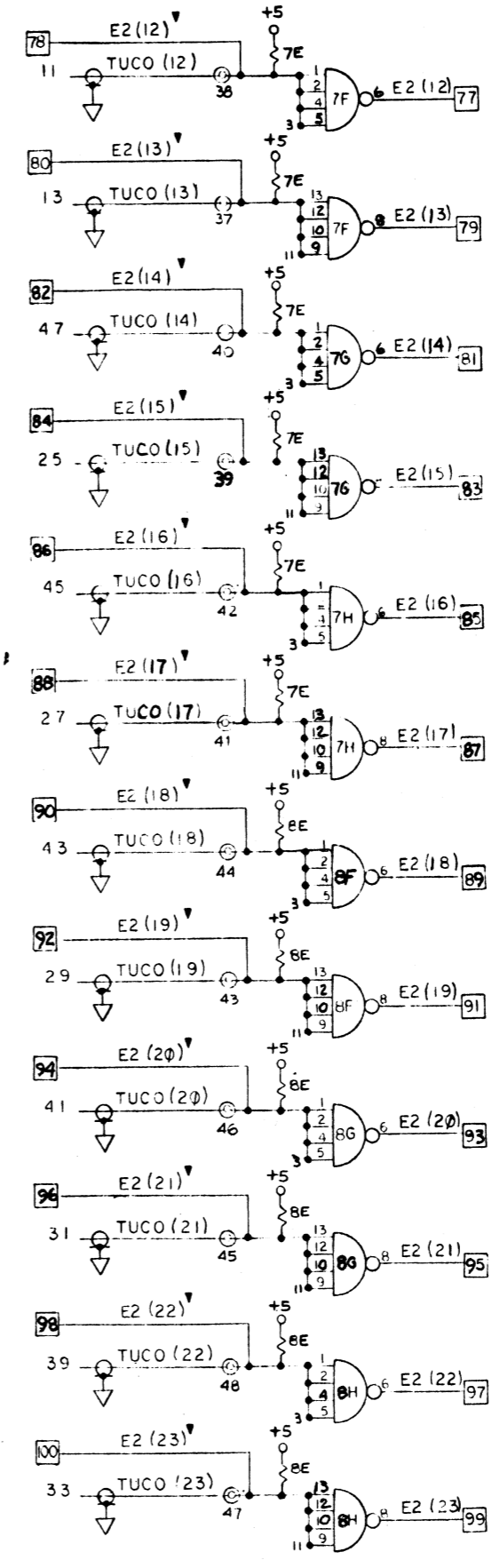
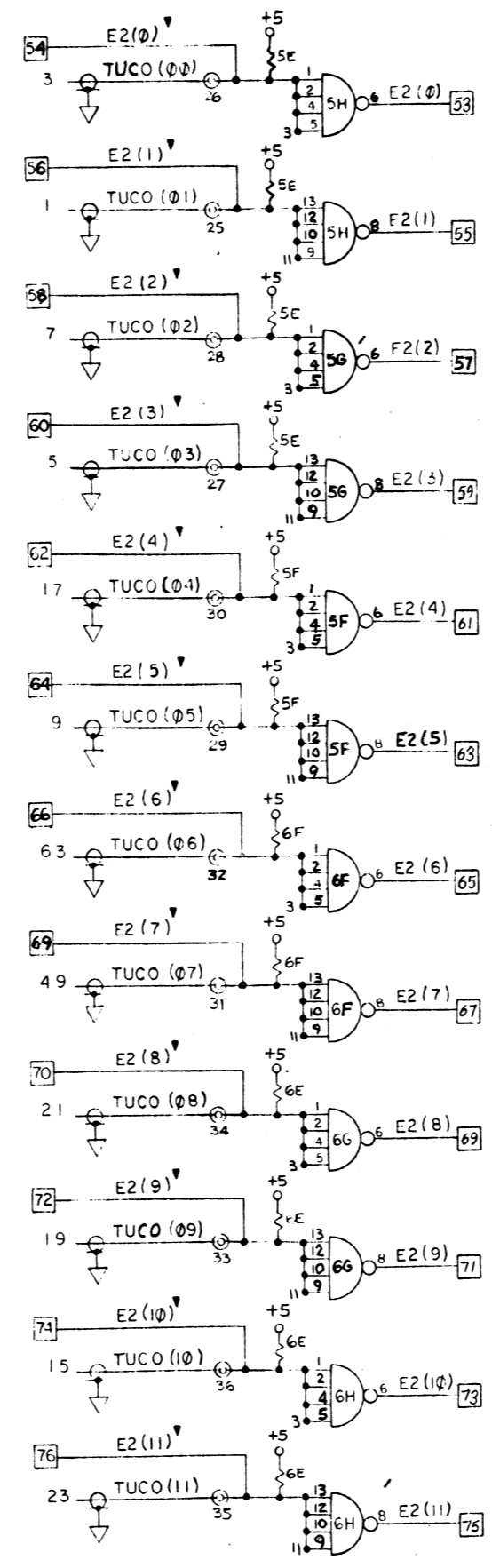
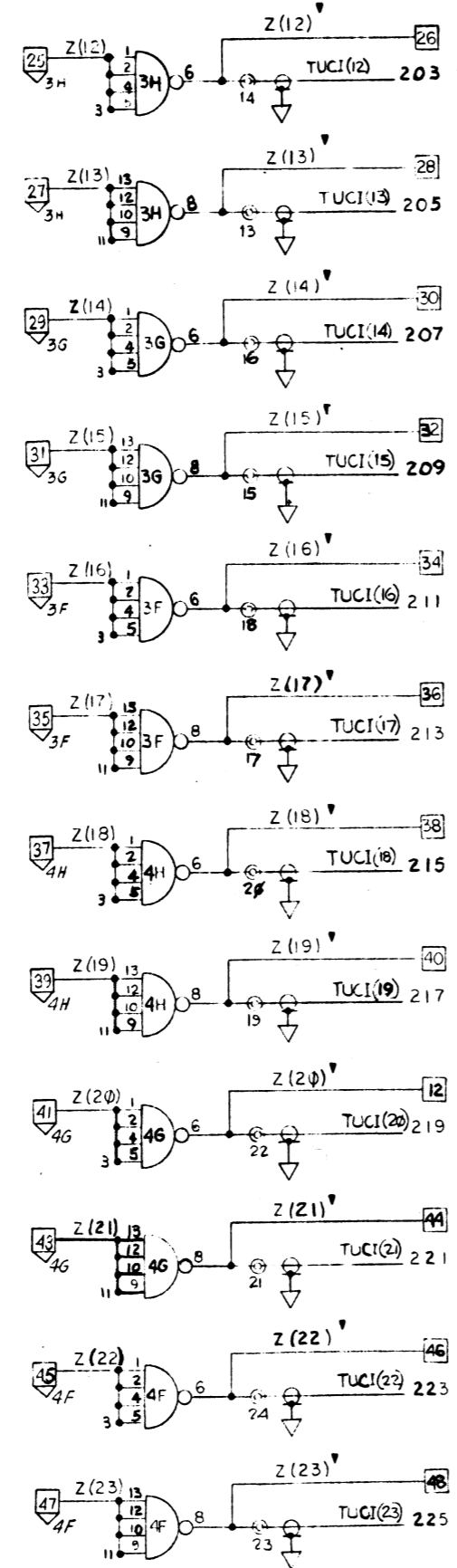
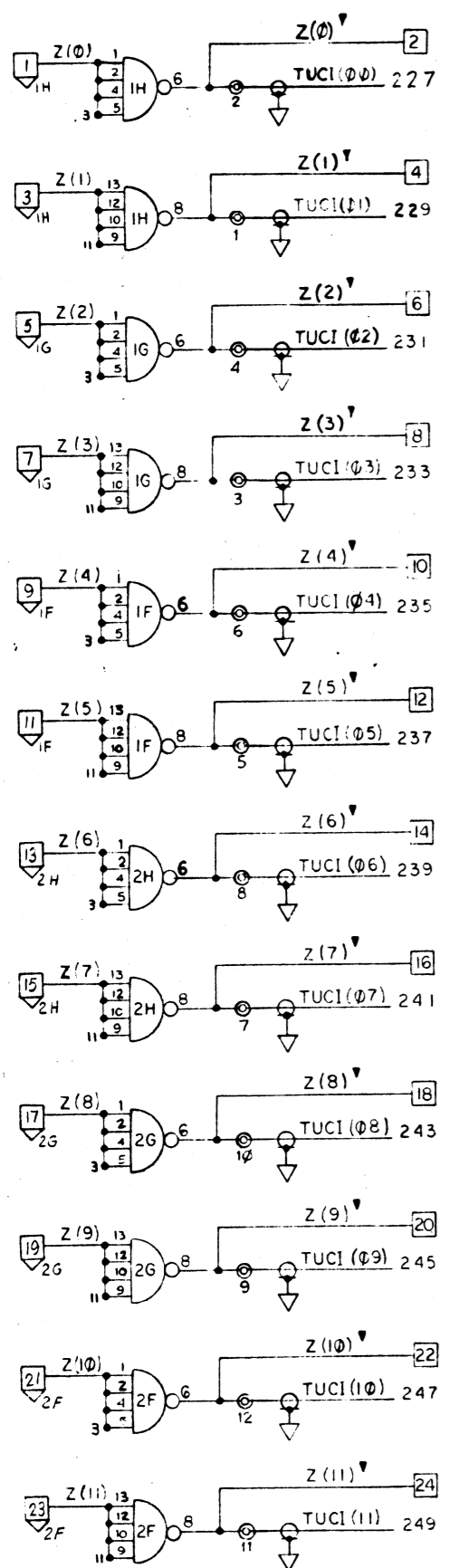
TITLE: MULTIPLIER REGISTER BITS
 PARTS: 3, 4
 A26, A27, A28

SUM REGISTER



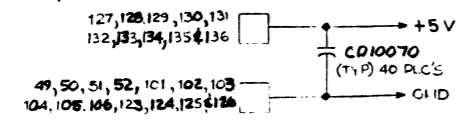
L00378		REVISED	
		DATE: _____ BY: _____ CHECKED: _____ APPROVED: _____	
TITLE: MULTIPLIER REGISTERS BITS (0-11), (12-23), (24-35)	PART NO.: M1 CPU 1.5	DATE: 4 4	PART NO.: L00378 .F

A26, A27, A28



35 TUGRD 215-1
 37 TUGRD 215-2
 77 TUGRD-3
 79 TUGRD-4
 TUIM
 1/4" SHIELD BRAID IN CABLE.
 AMC

NOTE:
 1. CABLES SHOWN CONNECT TO BRYANT TSU'S, WHEN THIS CARD IS USED AS THE I/O INTERFACE, THEY ARE NOT MOUNTED. ALL NR'S AT CABLE ENDS ARE FEED THROUGHS ON CABLE CARD 'A' (ASSEMBLY NR 70072B-7), TO WHICH THE COAXIAL CABLES ARE CONNECTED.
 2. UNLESS OTHERWISE SPECIFIED:
 ALL IC'S ARE TYPE SN7411N Q101040
 ALL RESISTORS ARE 200Ω 1/8W
 ALL TERMINATORS ARE

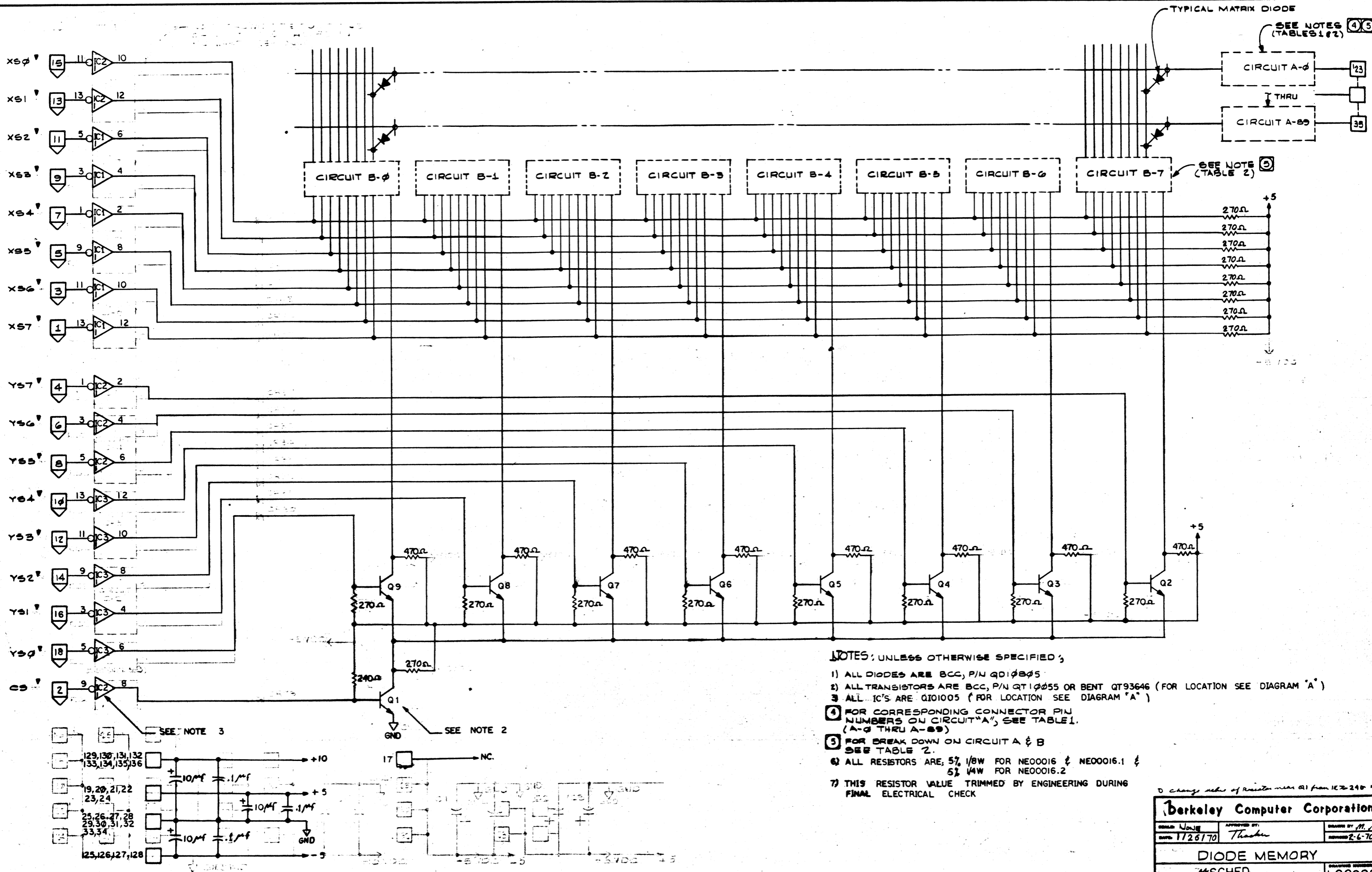


A33

berkeley Computer Corporation

SCALE:	APPROVED BY:	DRAWN BY: M.M.
DATE: 9-4-69		REVISED:
I/O INTERFACE CARD		
FIRST USED ON M1 μSCH	DRAWING NUMBER L00251.E	

SH 1 of 1



TYPICAL MATRIX DIODE
SEE NOTES (TABLES 1 & 2) 4 5

SEE NOTE 5 (TABLE 2)

- NOTES: UNLESS OTHERWISE SPECIFIED;
- 1) ALL DIODES ARE BCC, P/N QD10B05
 - 2) ALL TRANSISTORS ARE BCC, P/N QT10055 OR BENT QT93646 (FOR LOCATION SEE DIAGRAM "A")
 - 3) ALL IC'S ARE Q101005 (FOR LOCATION SEE DIAGRAM "A")
 - 4) FOR CORRESPONDING CONNECTOR PIN NUMBERS ON CIRCUIT "A", SEE TABLE 1. (A-0 THRU A-89)
 - 5) FOR BREAK DOWN ON CIRCUIT A & B SEE TABLE 2.
 - 6) ALL RESISTORS ARE: 5% 1/8W FOR NE00016 & NE00016.1 & 5% 1/4W FOR NE00016.2
 - 7) THIS RESISTOR VALUE TRIMMED BY ENGINEERING DURING FINAL ELECTRICAL CHECK

Change value of resistor near Q1 from 1K to 240Ω

Berkeley Computer Corporation

DESIGN NAME	APPROVED BY	DRAWN BY M.M.
DATE: 1/26/70	Thacker	REVISED 2-6-70
DIODE MEMORY		DRAWING NUMBER
SCHED.		L00298.0

TABLE 1		
"A" CIRCUIT	CONN PINS	REMARKS
A-0	123	
1	124	
2	120	
3	122	
4	121	
5	119	
6	116	
7	118	
8	117	
9	115	
10	112	
11	114	
12	113	
13	111	
14	108	
15	109	
16	107	
17	104	
18	106	
19	105	
20	103	
21	100	
22	102	
23	101	
24	99	
25	96	
26	98	
27	97	
28	95	
29	92	
30	94	
31	93	
32	91	
33	88	
34	89	
35	87	
36	84	
37	86	
38	83	
39	85	
40	82	
41	81	
42	80	
43	79	
44	78	
45	77	
46	75	
47	72	
48	74	
49	73	
50	71	
51	68	
52	70	
53	69	
54	67	
55	64	
56	66	
57	65	
58	63	
59	62	
60	60	
61	61	
62	59	
63	56	
64	58	
65	57	
66	55	
67	52	
68	54	
69	53	
70	51	
71	48	
72	50	
73	49	
74	47	
75	44	
76	46	
77	45	
78	43	
79	40	
80	42	
81	41	
82	39	
83	36	
84	38	
85	37	
86	35	

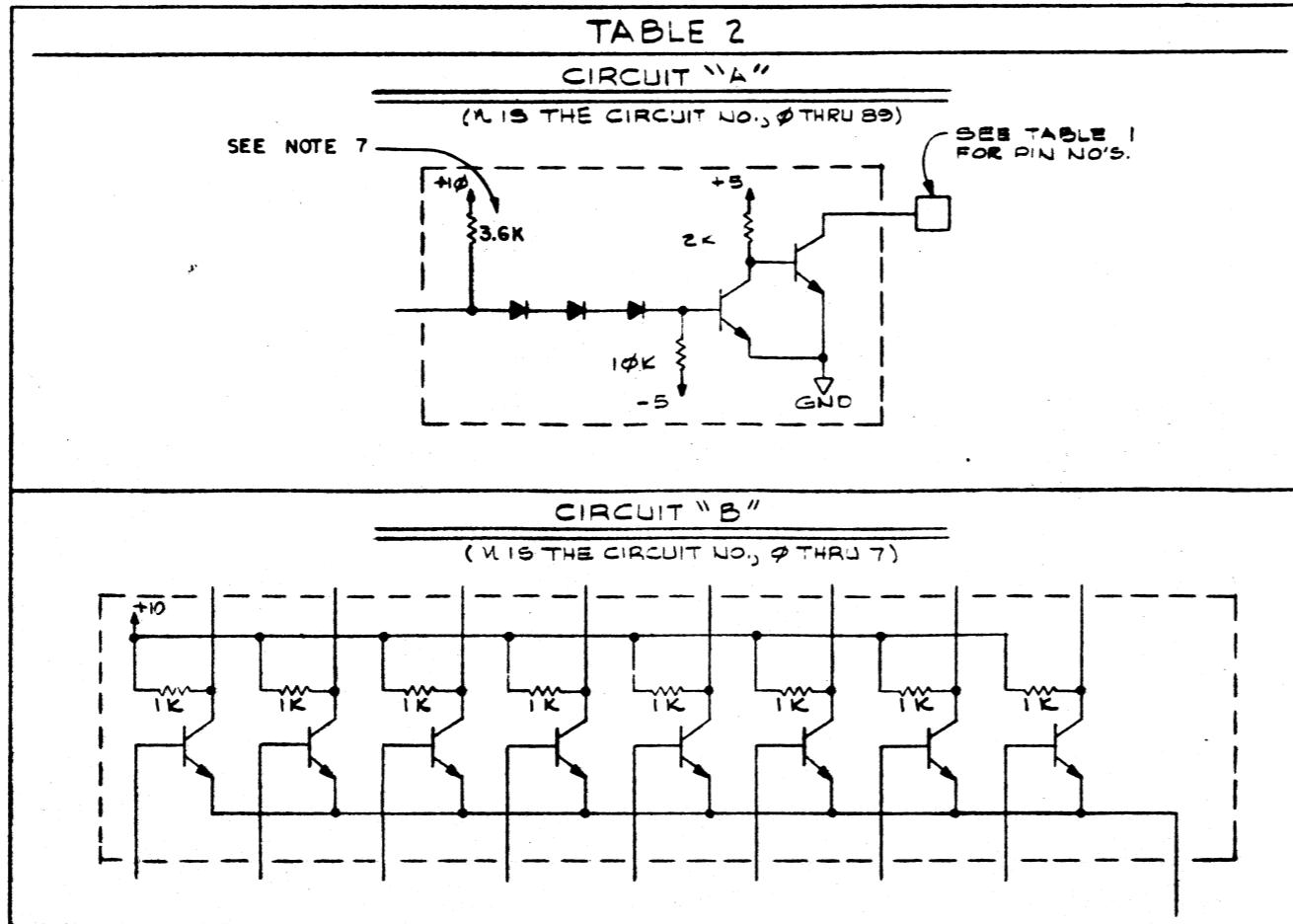
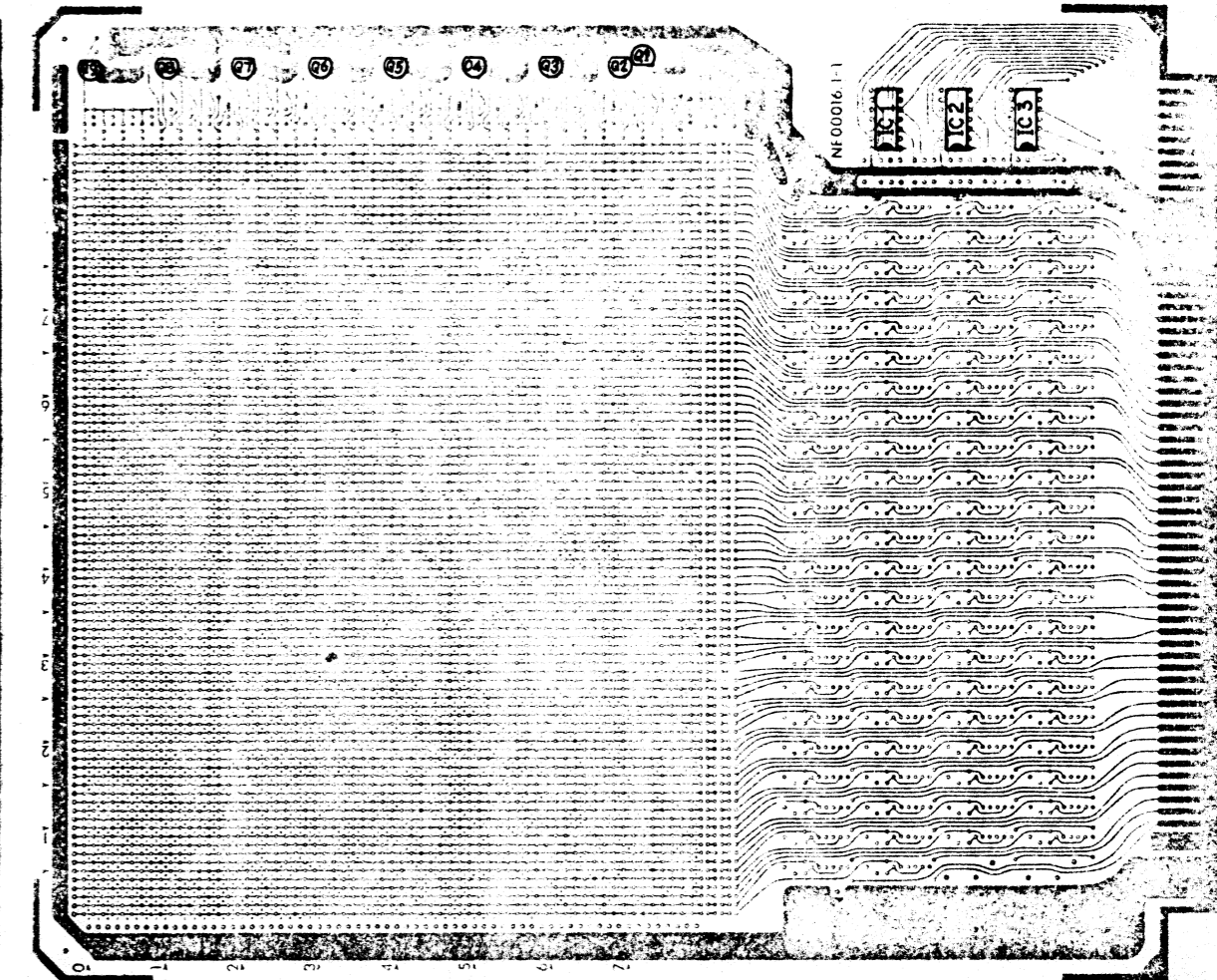
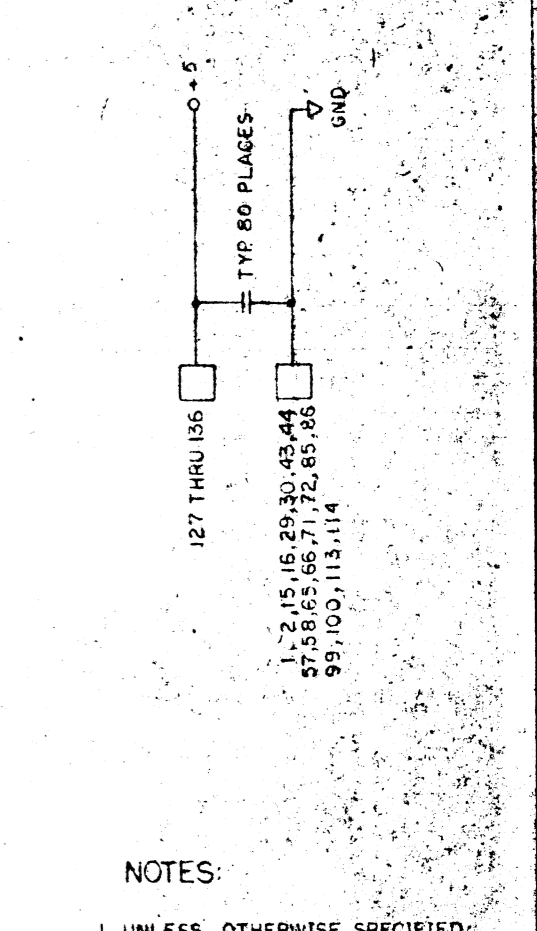
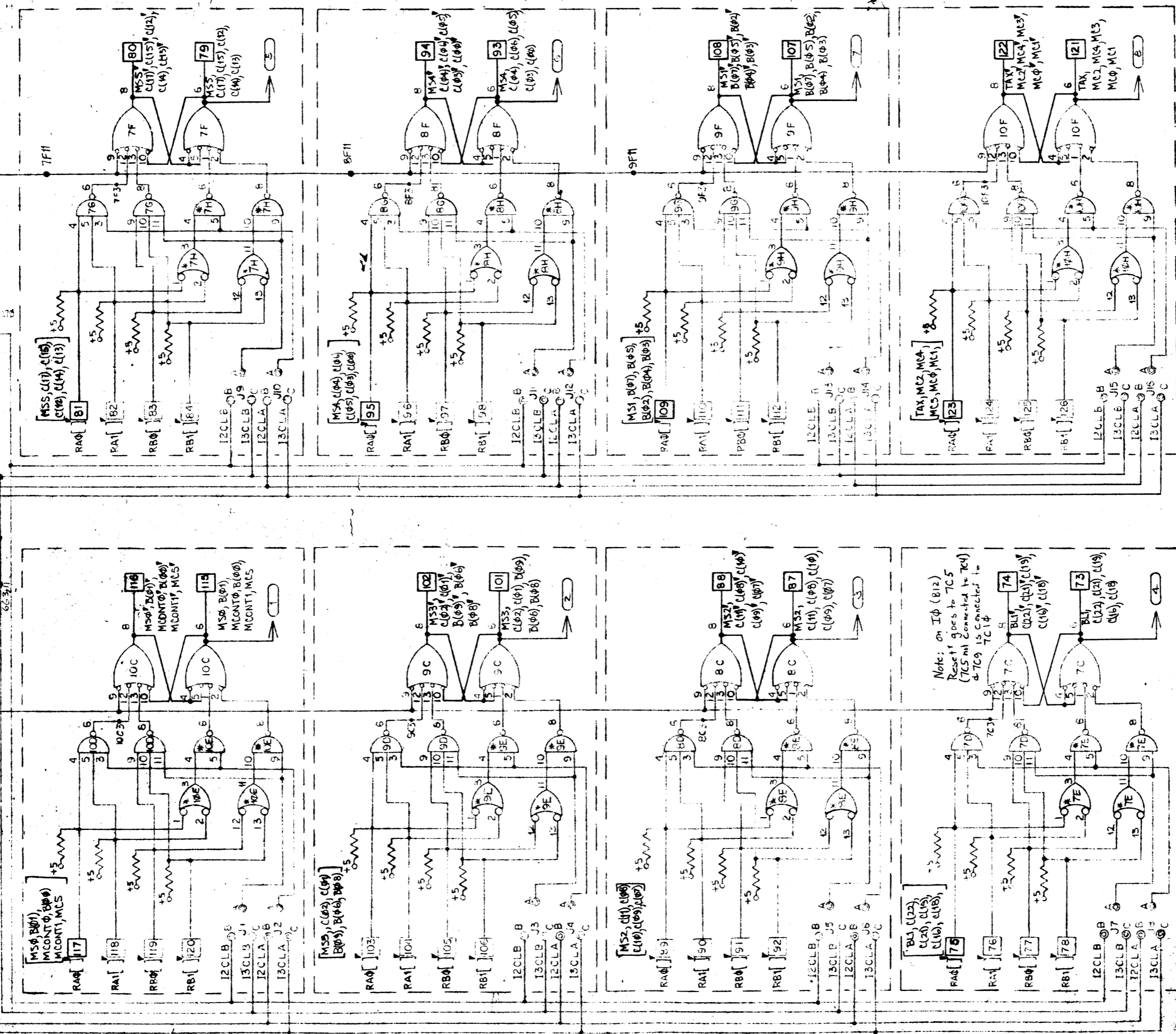
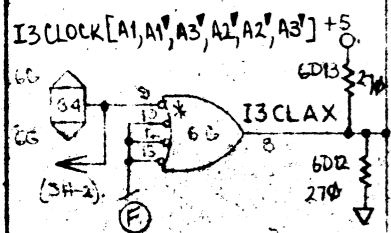
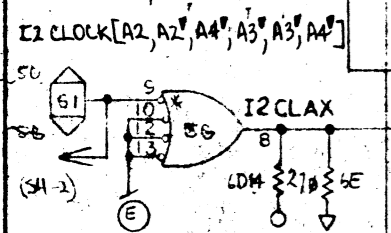
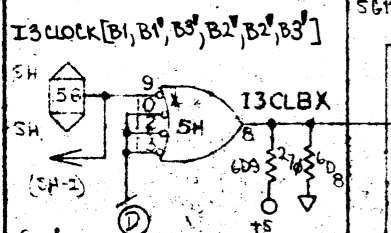
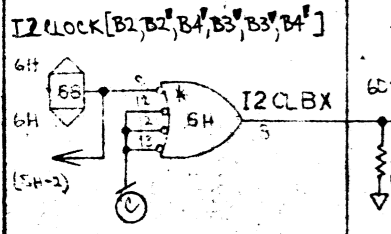
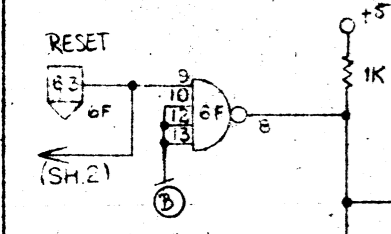


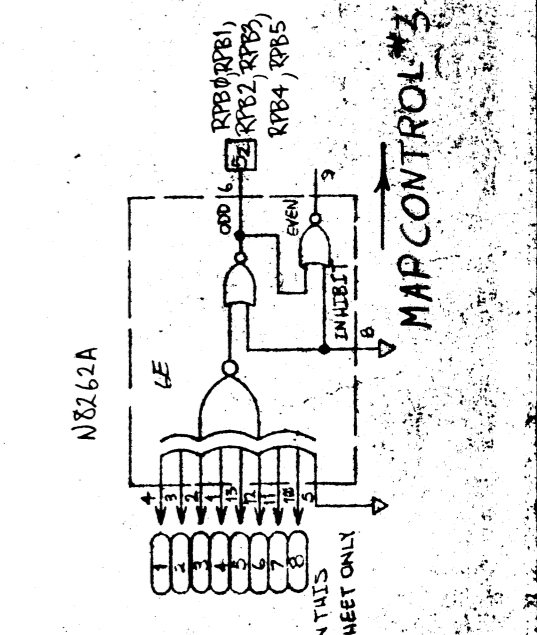
DIAGRAM "A"



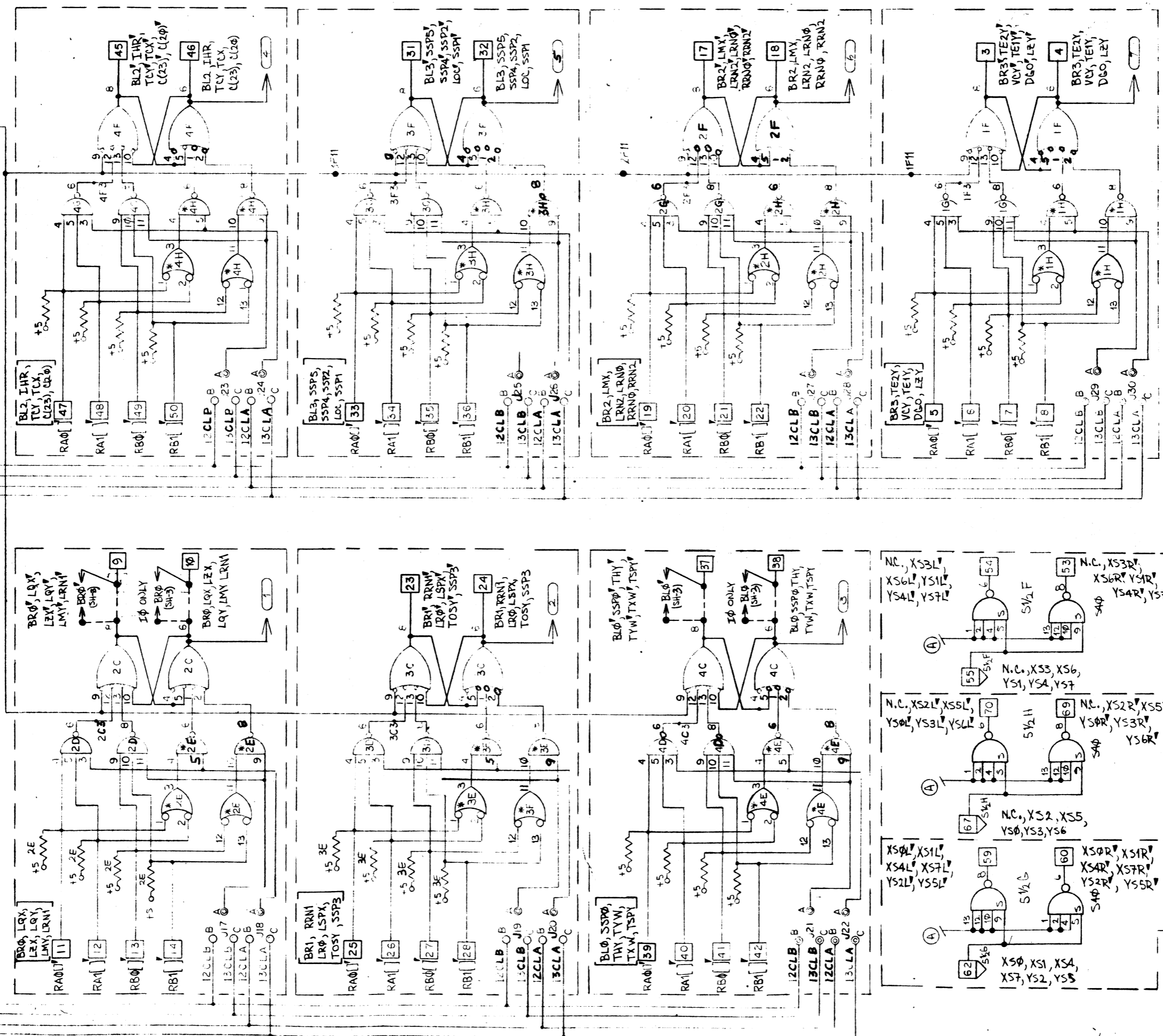
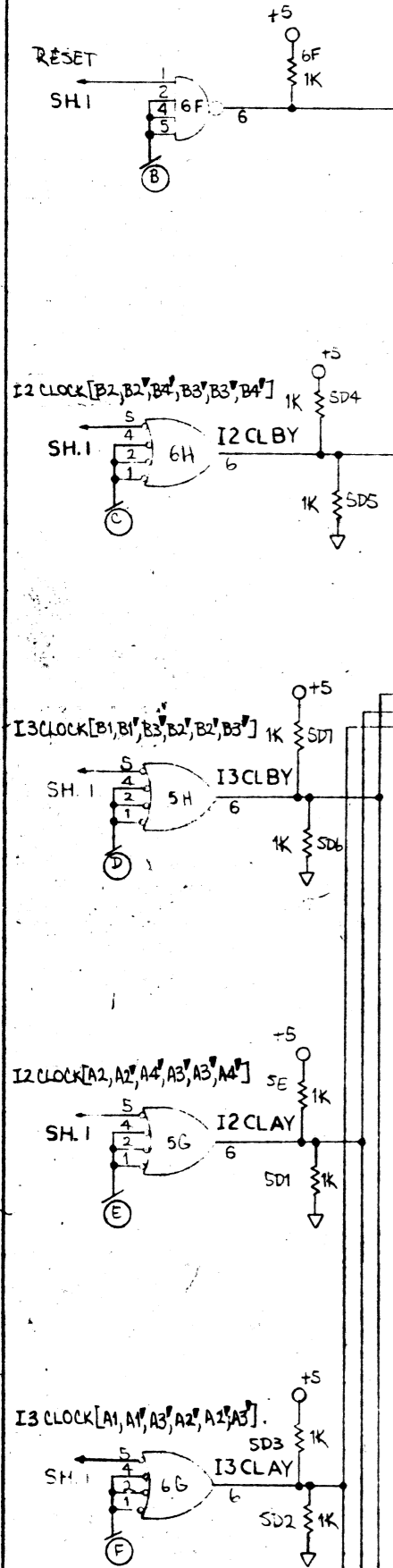
Berkeley Computer Corporation		
DATE: 1/26/70	APPROVED BY: <i>Thacker</i>	DRAWN BY: <i>M.M.</i>
DIODE MEMORY		REVISED: 2-6-70
MSCHED.		DRAWING NUMBER: L00298.D
SHT 3 OF 2		



NOTES:
 1. UNLESS OTHERWISE SPECIFIED:
 RESISTORS ARE RC27210
 CAPACITORS ARE CD10P70
 TRANSISTORS ARE Q193640
 2. * - FAST I.C. MODULES
 3. J - JUMPER AS REQUIRED



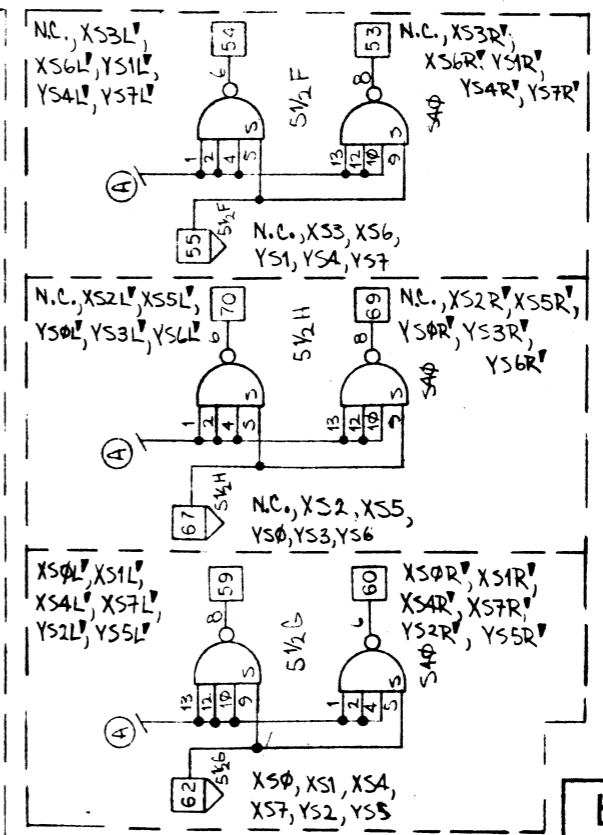
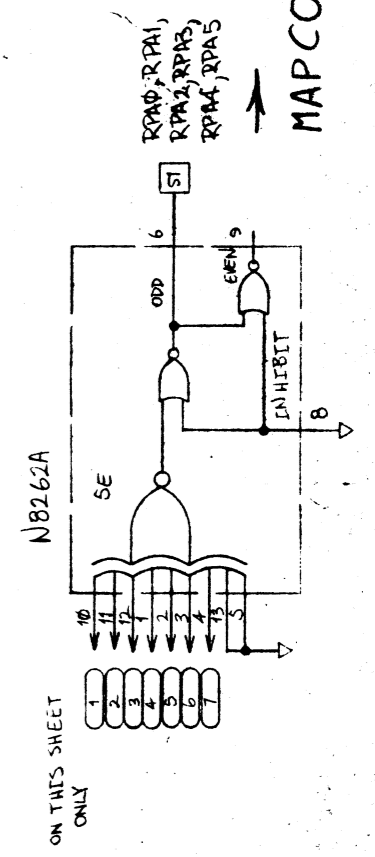
DATE	7 AUG 69	DESIGNED BY	GSA
REVISED	1-8-70	DRAWING NUMBER	L00392C
I REGISTER (10, 11, 12, 13, 14, 15)		MASTER CPU 1.5	
SHEET ONLY		SHEET 1 OF 3	



- Notes:
- (A) 5 1/2 H
 - (B) 6 F
 - (C) 6 H
 - (D) 5 H
 - (E) 5 H
 - (F) 6 C

PULL-UP LOCATIONS

MAP CONTROL #3



Berkeley Computer Corporation

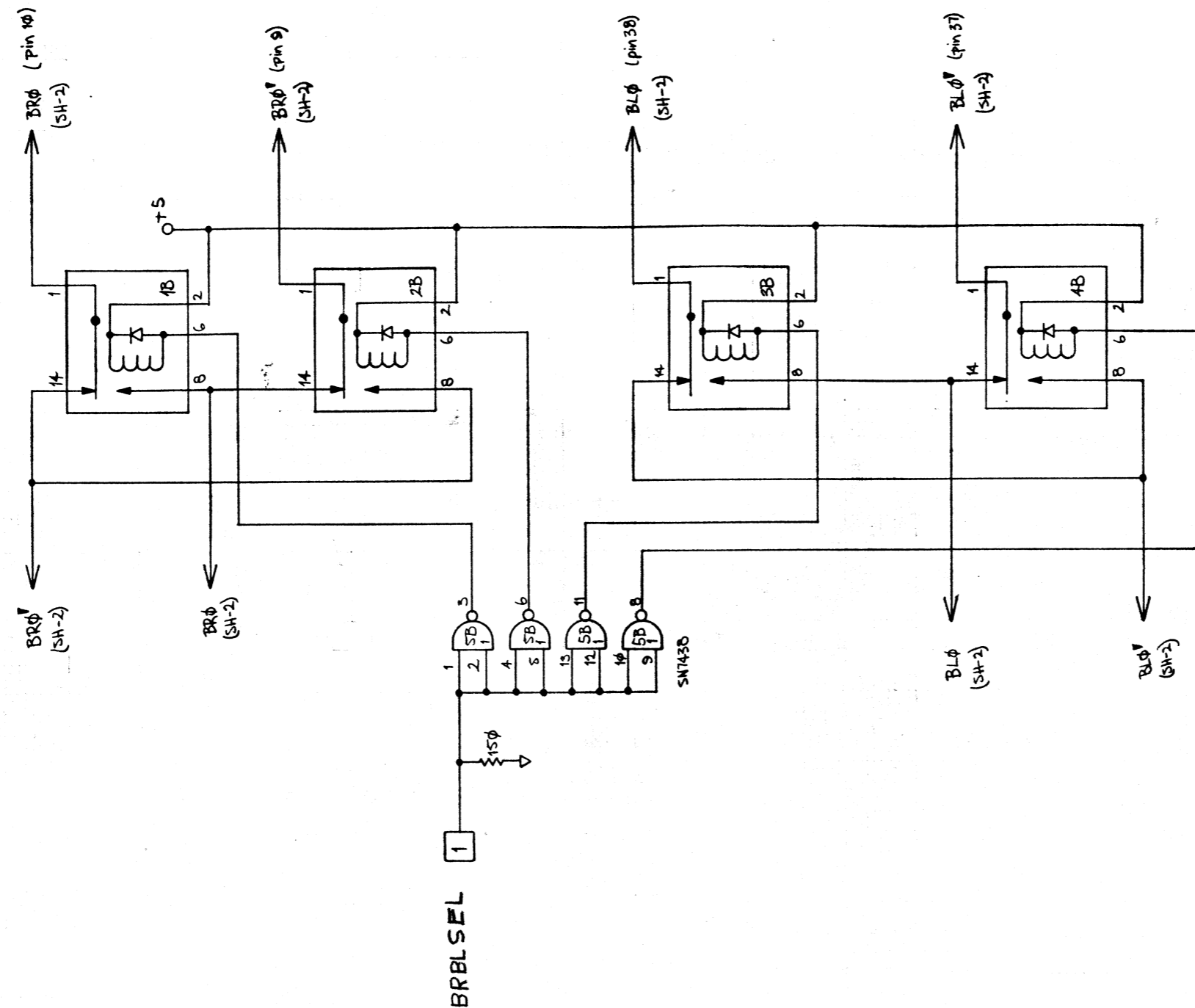
SCALE: _____ APPROVED BY: _____ DRAWN BY: GCA

DATE: 7 AUG 69 REVISED: 1-8-70

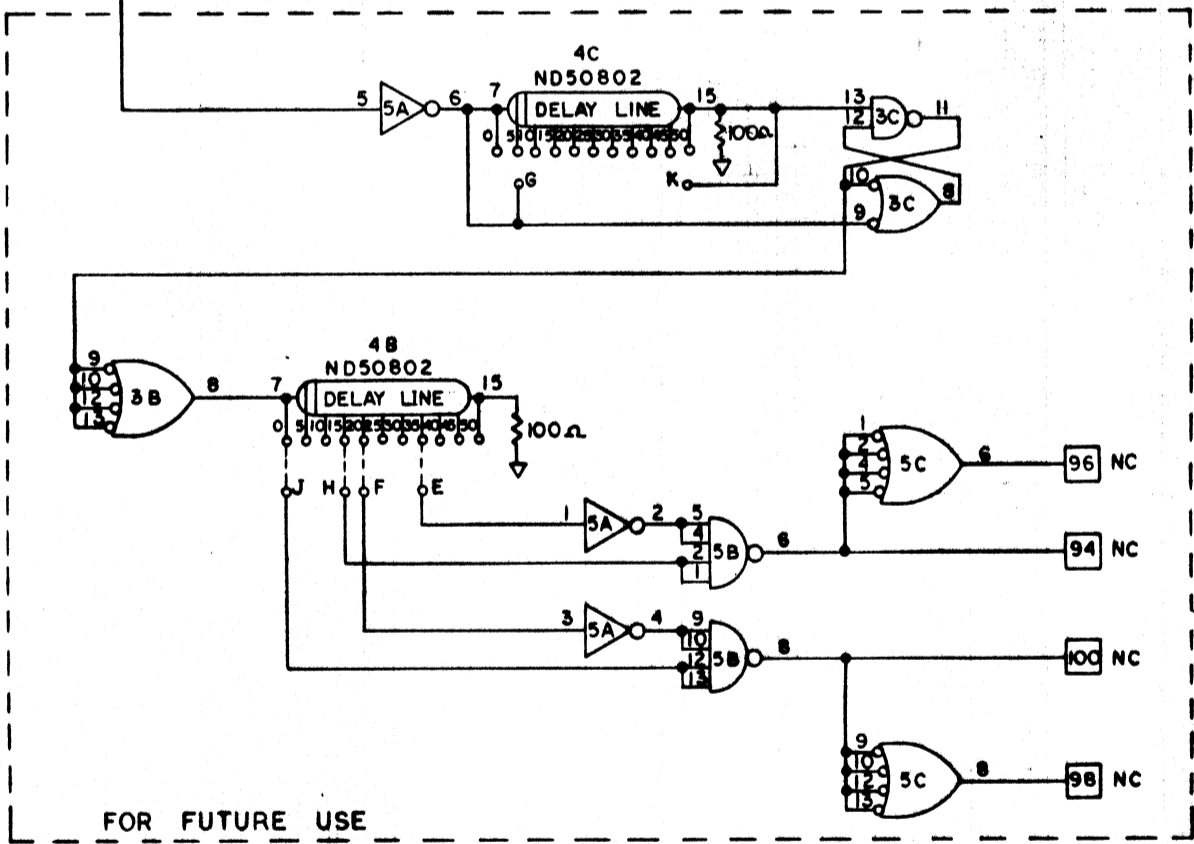
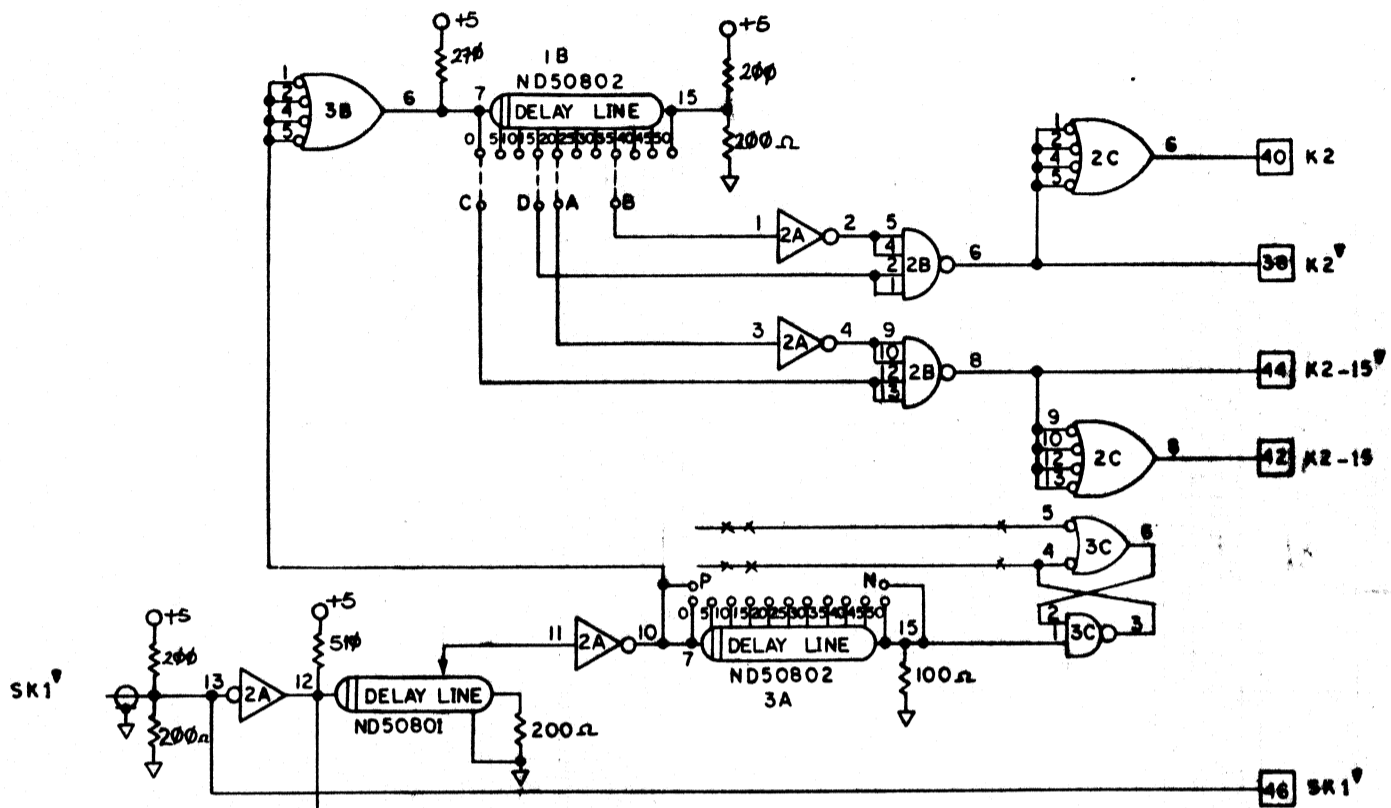
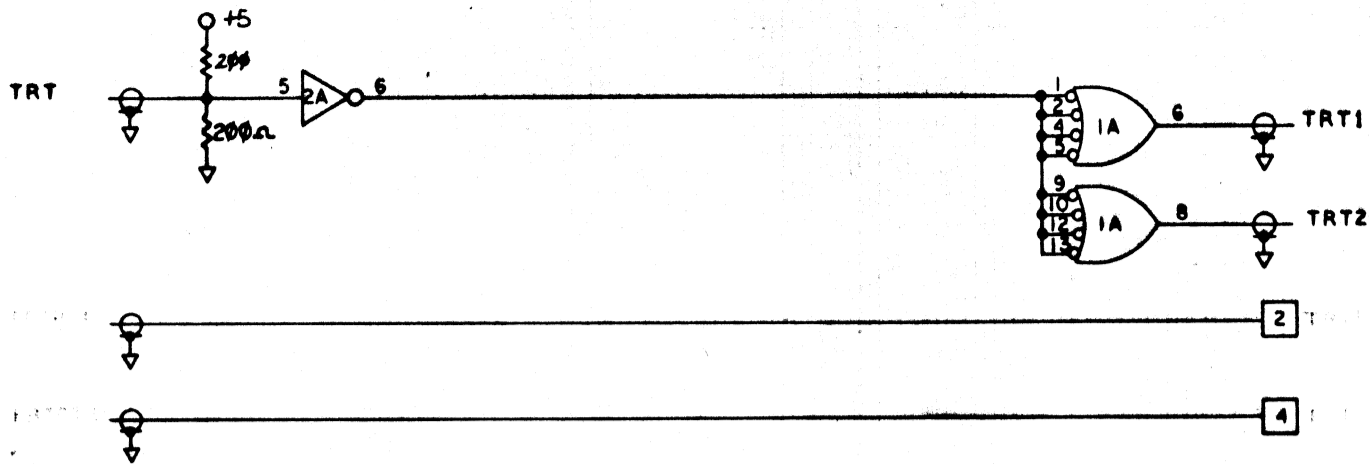
I REGISTER (10, 11, 12, 13, 14, 15)

MASTER CPU 15

DRAWING NUMBER: L00392C



DESIGNED	D. Dodge		
DRAWN	R. Edisa		
PROJECT	MASTER	CPU 1.5	
SHEET	3	3	NO. L00392.C



6, 8, 10, 12, 14, 16, 18, 20, 21, 22, 37, 39, 41, 43, 45, 47-50, 52, 54, 56, 58, 60, 62, 64, 66, 68, 70, 72, 74-80, 85-92, 102, 104, 106, 108-110, 125, 126

127-136

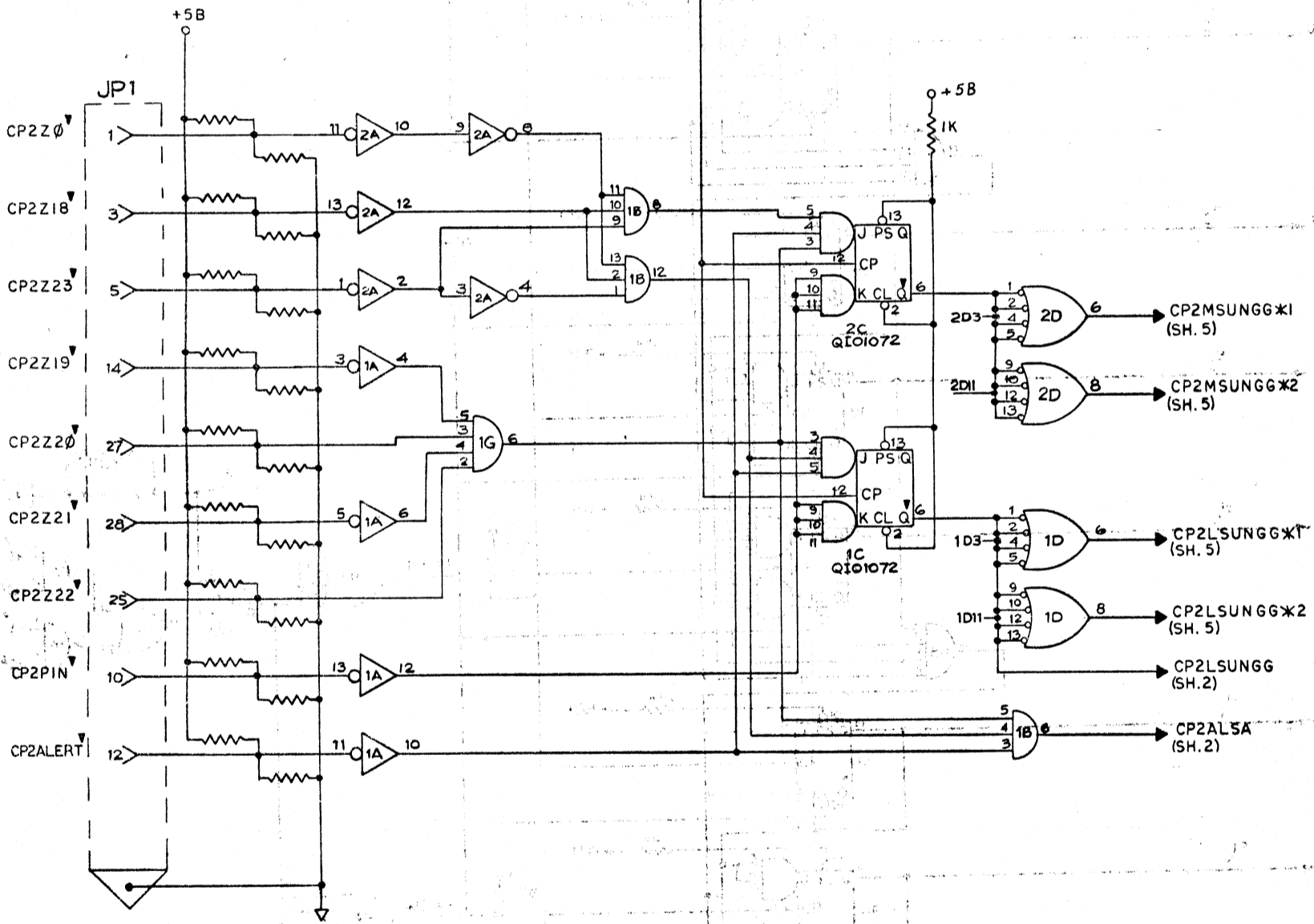
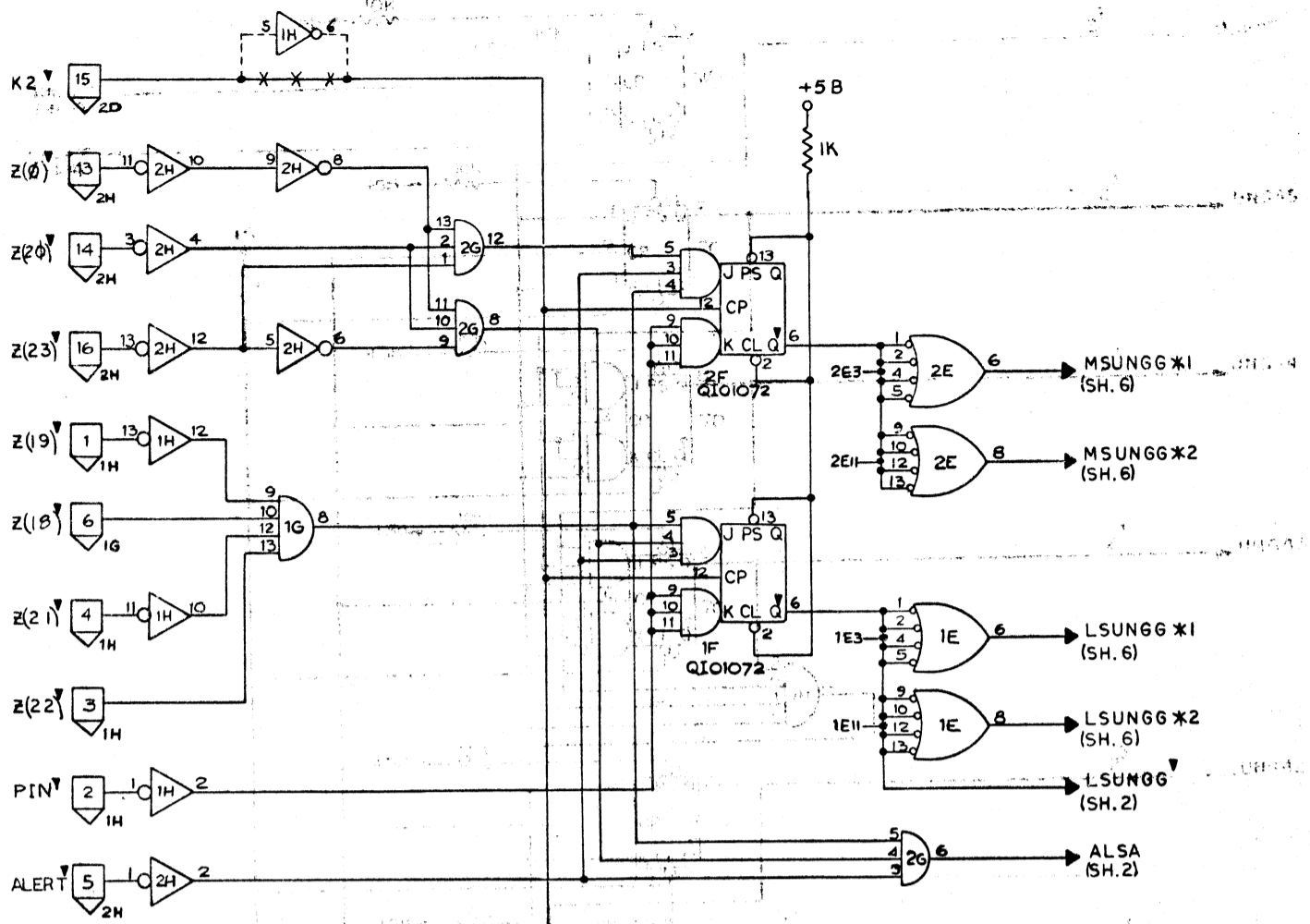
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, 73, 93, 95, 97, 99, 101, 103, 105, 107.

23-36, 81-84, 111-124

NOTE: UNLESS OTHERWISE SPECIFIED
1. RESISTORS ARE 10%, 1/4W, CARB. COMP.

LC0557		REVISION	
Berkeley Computer Corporation		ST. DUNSMORE	
DATE: 5/1/70		DATE: 5/1/70	
REVISED BY: M. J. MOORE		REVISED BY: M. J. MOORE	
NONE		FIRST USED ON M1-SR.	
L00557.0		UNG. CLOCK	

C27



6010007

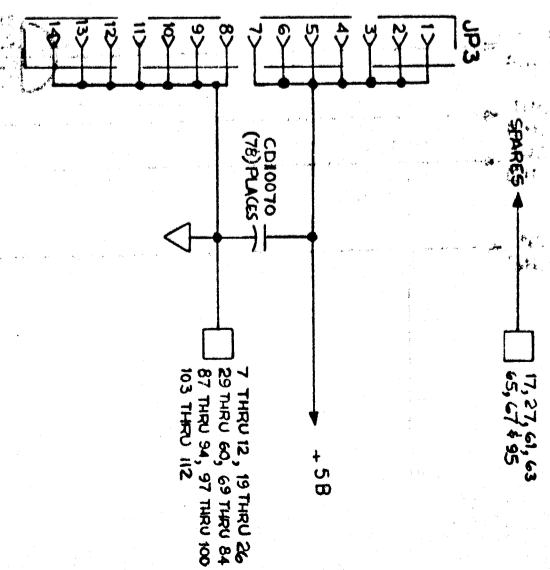
S. DINSMORE
 G. AZALINA
 NONE
 CPU
 1 6 L000109J/F

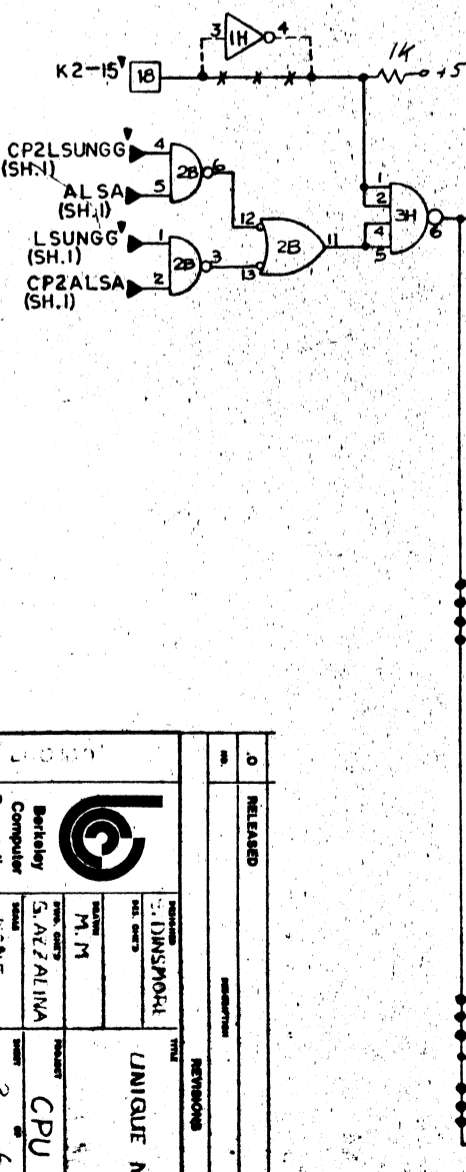
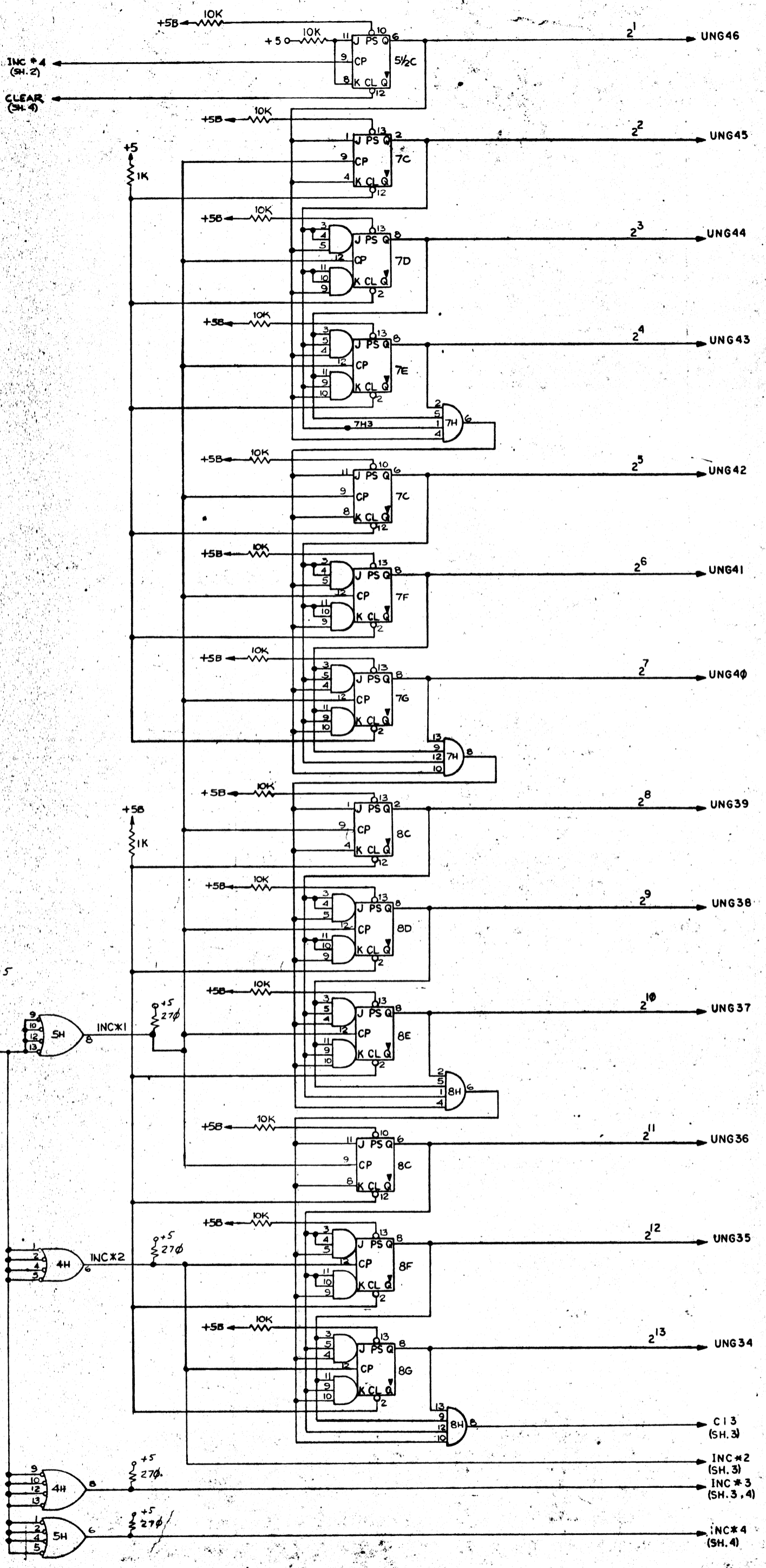
CPU 1 A33 1.5 C30

UNIQUE NAME GENERATOR (11NG)

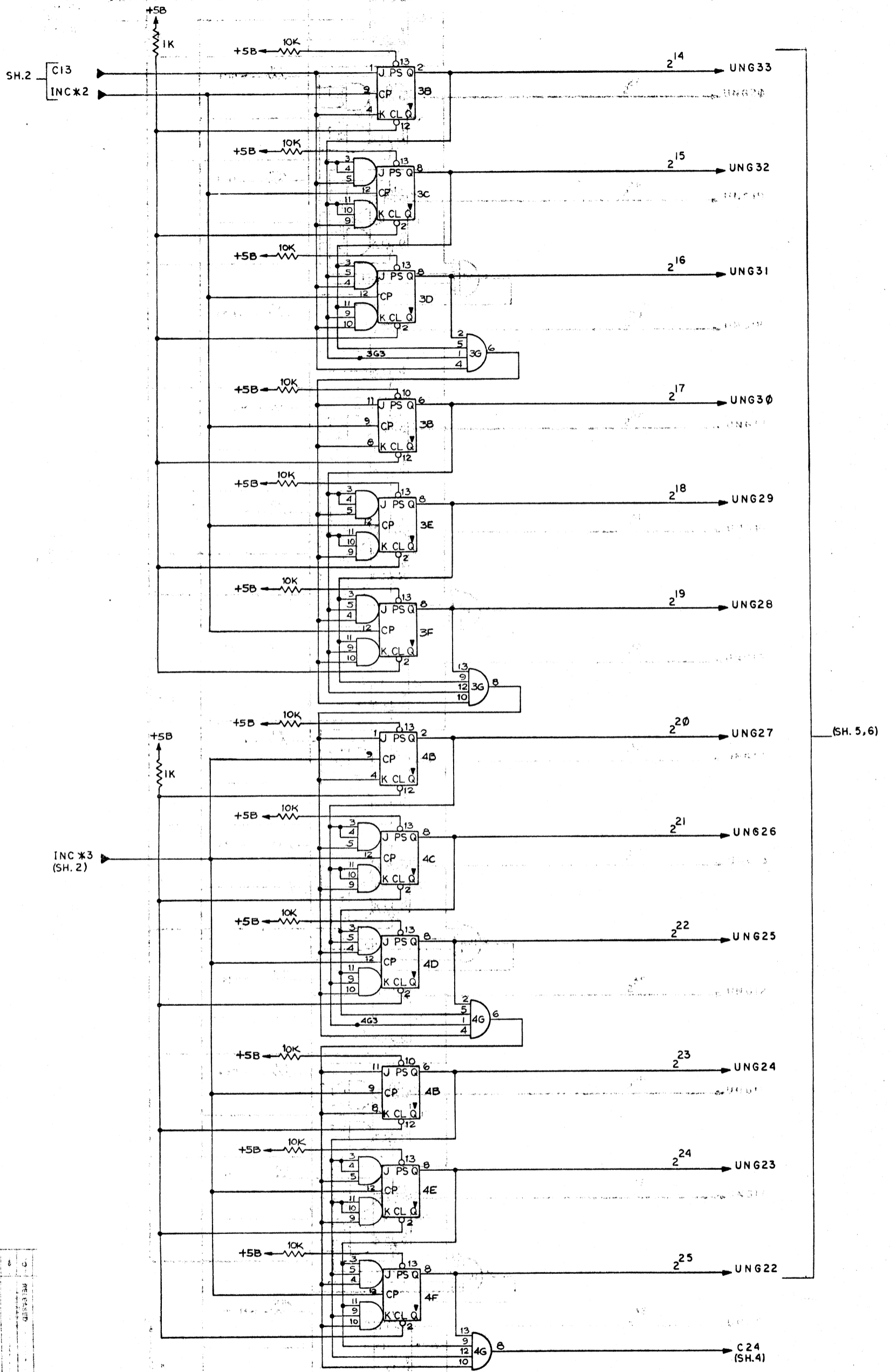
NOTES:

1. UNLESS OTHERWISE SPECIFIED, ALL RESISTORS ARE 180 Ω, 1/8W, CARBON, 5% ARE CD10070 CAPACITORS ARE CD10070
2. Vcc FOR ALL IC'S IS +5B, SUPPLIED BY CABLE.





		RELEASED DATE: _____ BY: _____
PROJECT: UNIQUE NAME GENERATOR (CPU) DRAWING NO: 2-6 REVISION: 1	DESIGNED BY: DMSPH CHECKED BY: SAZALINA DATE: _____	TITLE: UNIQUE NAME GENERATOR (CPU) PART: LOGIC



00109

REVISIONS

DATE

BY

DESCRIPTION

EXTENSIONS

UNIQUE NAME GENERATOR (UNG)

MM

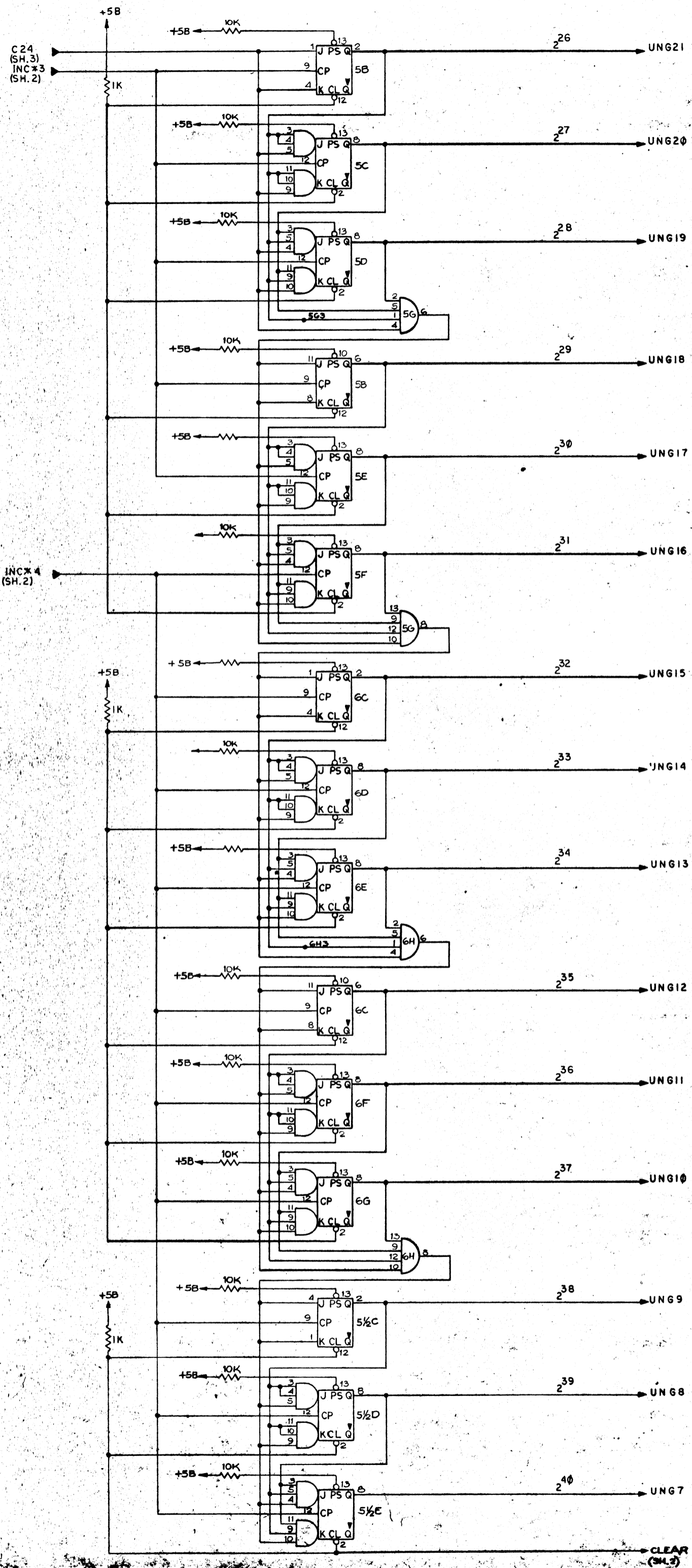
GAZZALINA

CPU

3

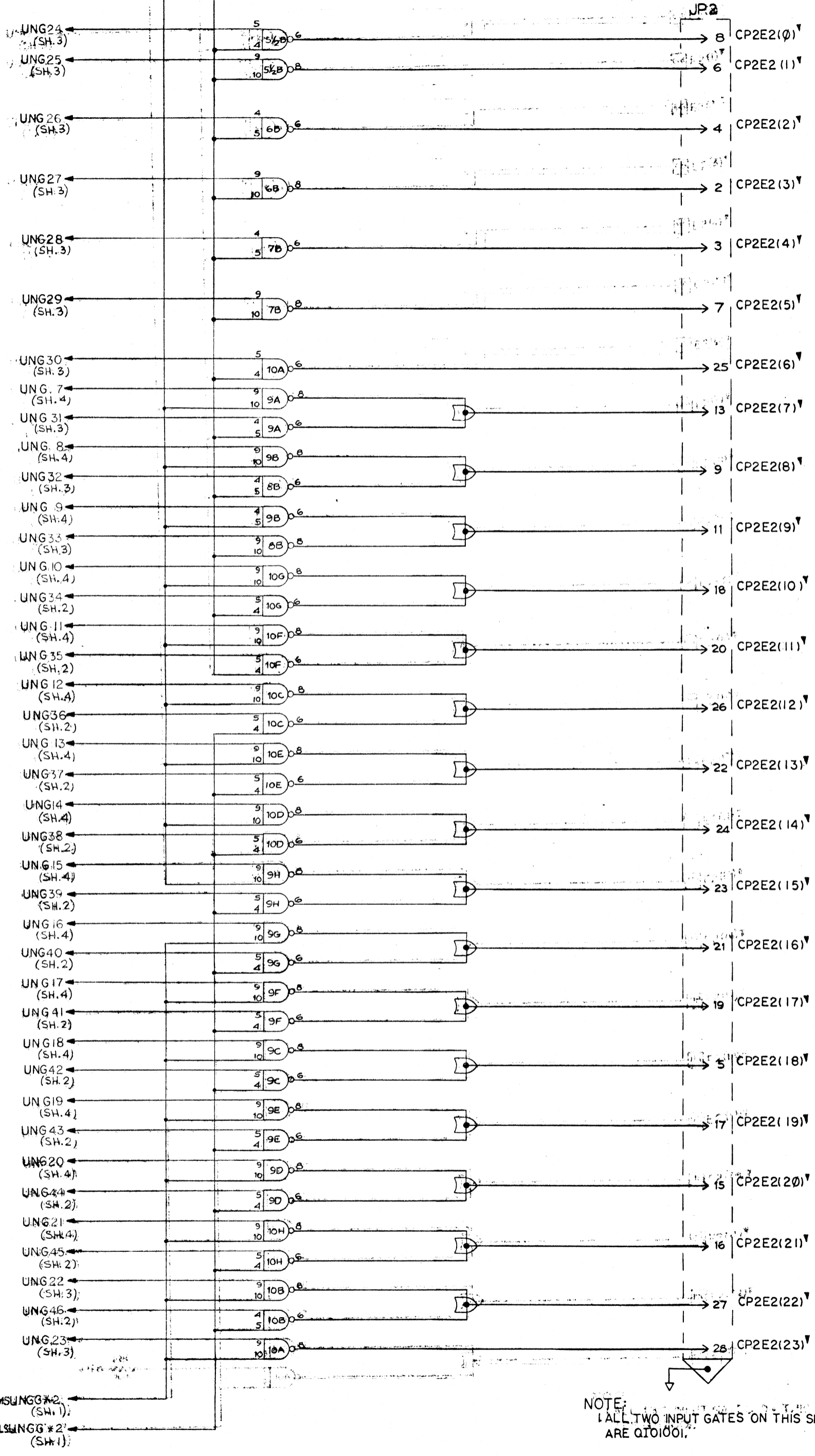
6

00109



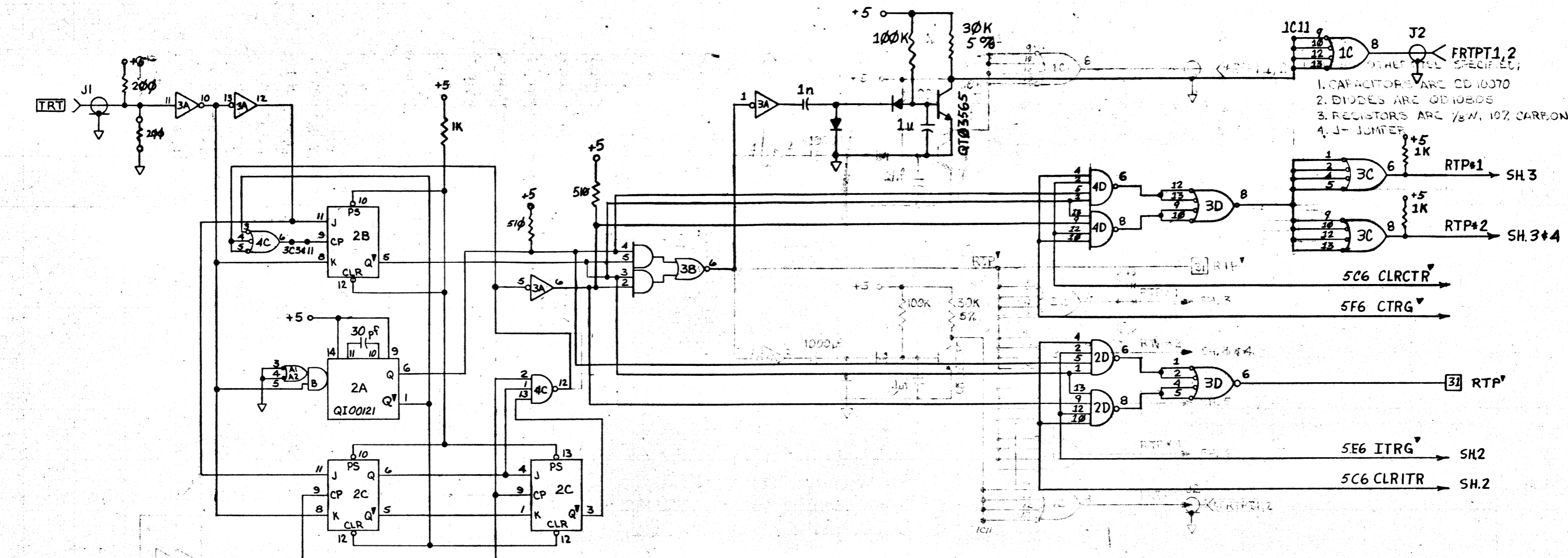
LOGIC		RELEASED	
		ENGINEERING S. LINSCHME DATE: 1/11/64 BY: GAZZALINI	
TITLE UNIGUT NAME GENERATOR (UNIG)	PART CPU	QUANTITY 4	DRAWING NO. LOGIC
PROJECT NONE	REVISION NONE	DATE 1/11/64	BY GAZZALINI

CP2LSUNGG*1
 CP2MSUNGG*1

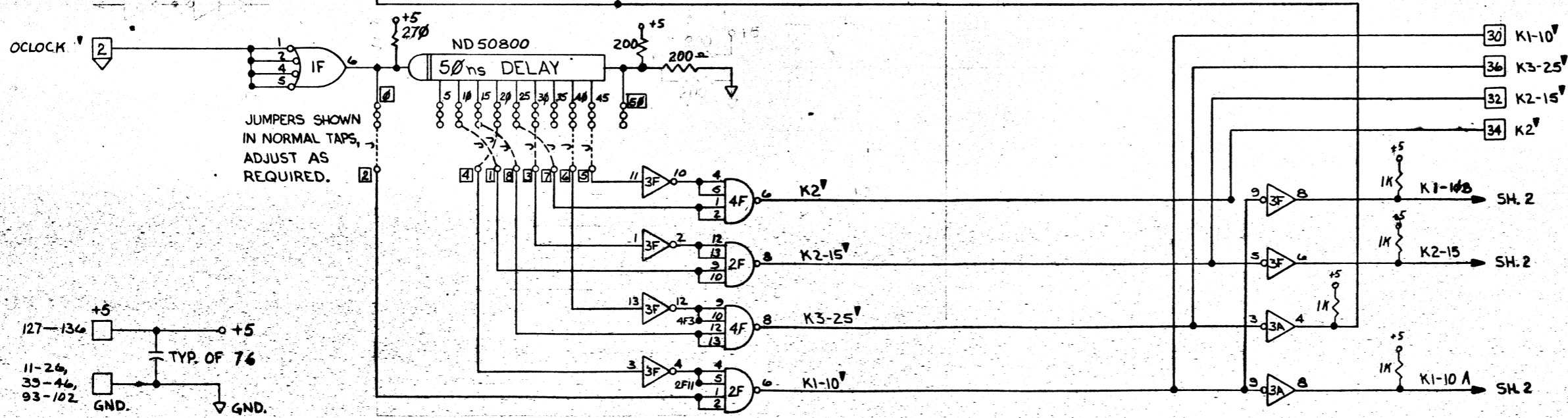


NOTE:
 ALL TWO INPUT GATES ON THIS SHEET
 ARE Q10101.

Berkeley Computer Corporation
 CPU
 UNIQUE NAME GENERATOR (UNG)
 LCO109

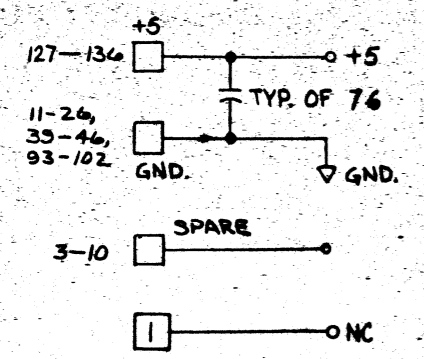


- UNLESS OTHERWISE SPECIFIED;
1. CAPACITORS ARE CD10070
 2. DIODES ARE QD10805
 3. RESISTORS ARE 1/8W, 10% CARBON
 4. J- JUMPER



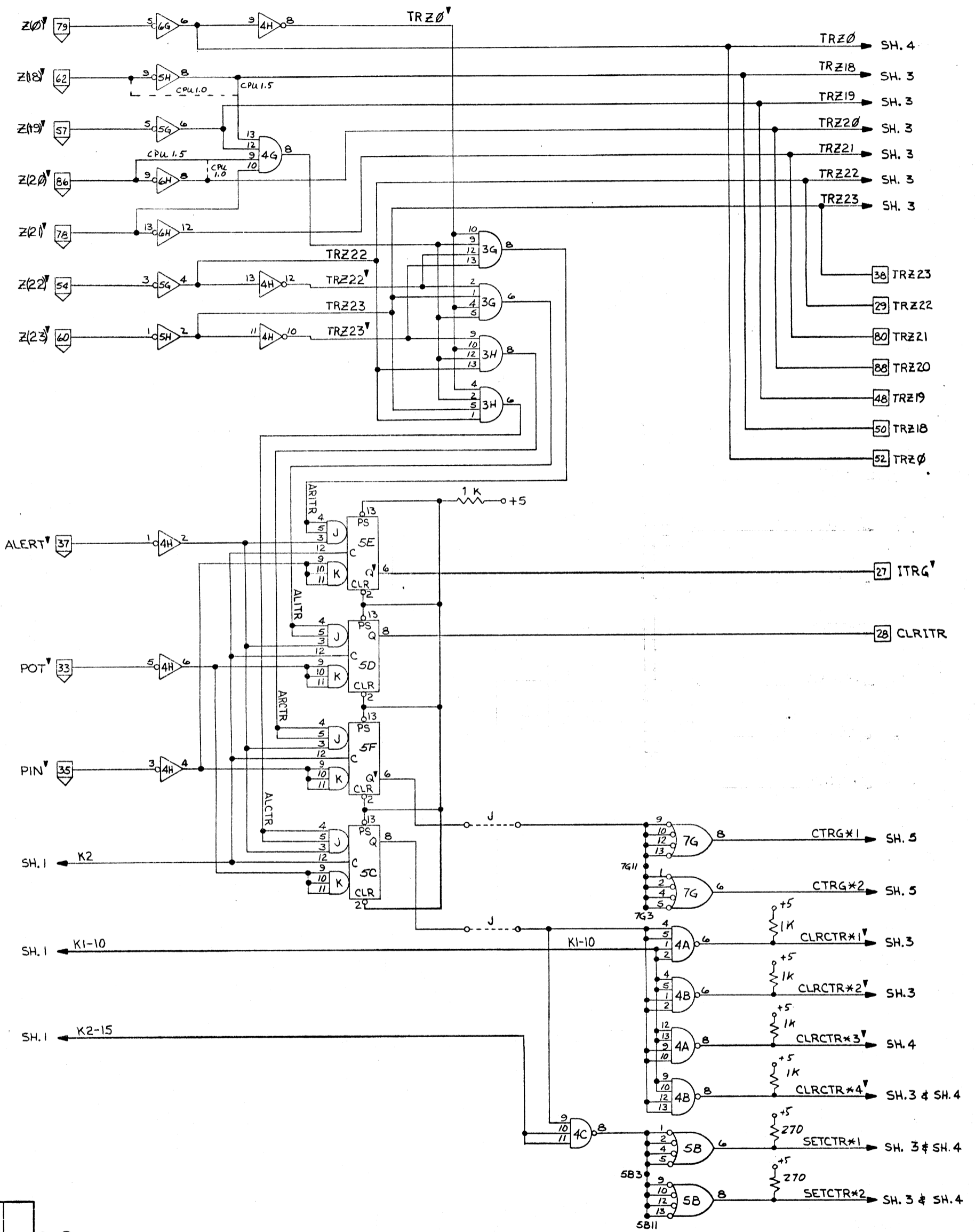
- 30 K1-10 (RESETS ITR/CTR)
- 36 K3-25 (MAKES RTP)
- 32 K2-15 (LOADS ITR/CTR - ALSO MAKES TD)
- 34 K2 (MAKES LOAD/READ GATES)

- NOTES:
1. CAPACITATORS ARE CD10070
 2. DIODES ARE QD10805
 3. RESISTORS ARE 1/8W, 10% CARBON
 4. J- JUMPER



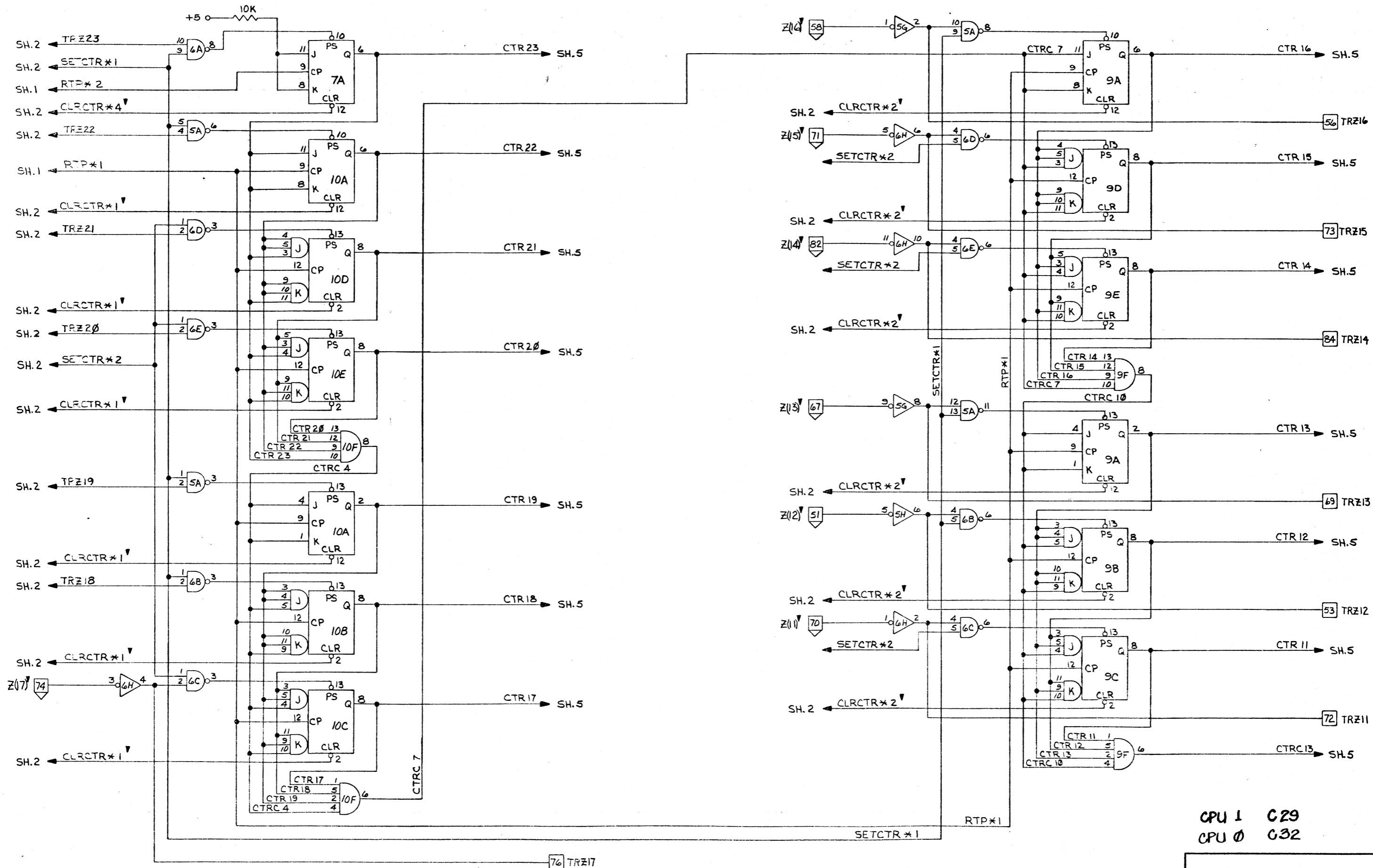
CPU 1 029
CPU 0 032

DATE: 9-26-69	APPROVED BY:	DESIGNED BY: DM
COMPUTE TIME REGISTER (CTR)		REVISED 10-7-69
CPU # 1		DRAWING NUMBER: L00084.6



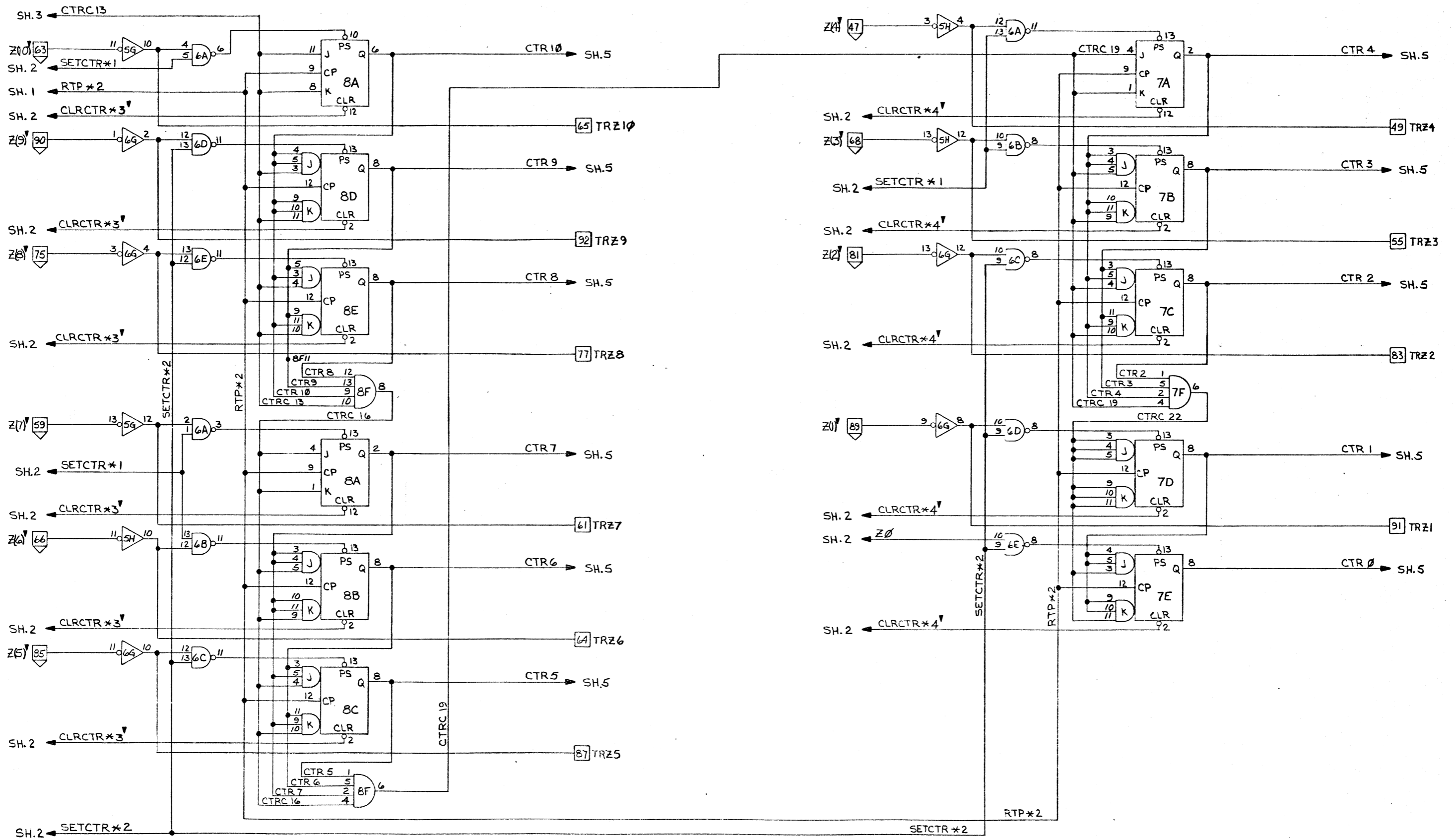
SHEET 2 OF 5

SCALE NONE	APPROVED BY
DATE 9-24-69	DRAWN BY
REVISION 10-7-69	REVISION
DRAWING NUMBER L00084	
CPU # 1	
COMPUTE TIME REGISTER (CTR)	
CPU 1 C29	
CPU 0 C32	



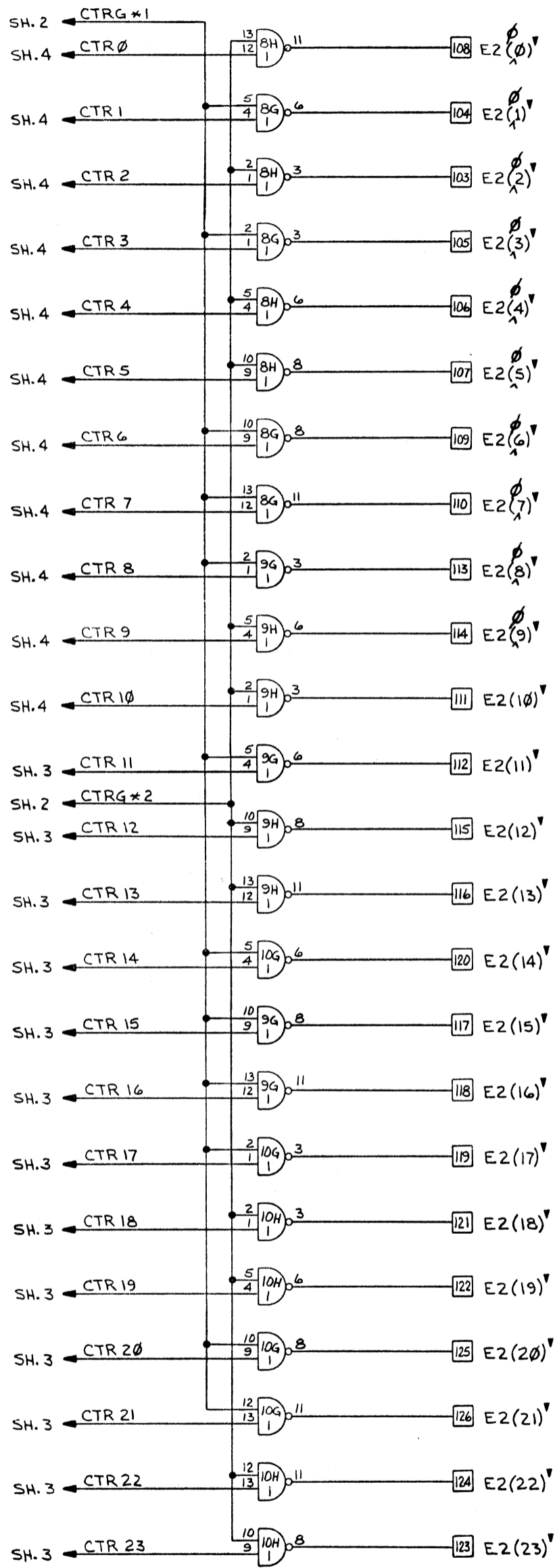
CPU 1 C29
CPU 0 C32

SCALE: NONE	APPROVED BY:	DRAWN BY: <i>[Signature]</i>
DATE: 9-30-69		REVISED 10-7-69
COMPUTE TIME REGISTERS (CTR)		
CPU # 1	DRAWING NUMBER	1.00084.1



CPU 1 C29
CPU 0 C32

SCALE: NONE	APPROVED BY:	DRAWN BY: DM
DATE: 10-1-69		REVISED: 10-7-69
COMPUTE TIME REGISTER (CTR)		
CPU# 1		DRAWING NUMBER: L00084



L 00084

DATE: 10-7-69
BY: D. MORENO

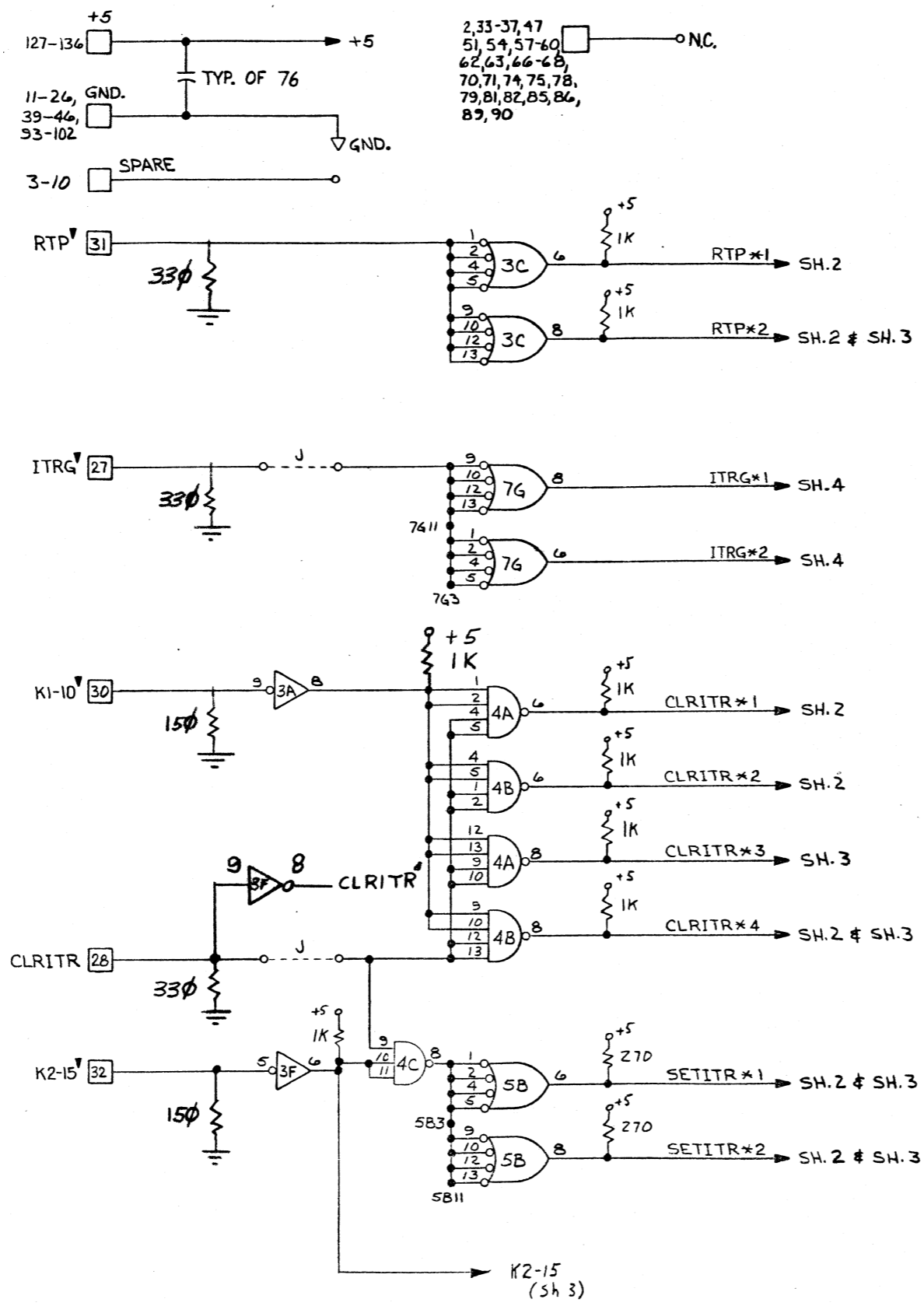
COMPUTE TIME REGISTER (CTR)
CPU # 1

NONE 5 5 L00084. 6

CPU 1 C29
CPU 0 C32

NOTES

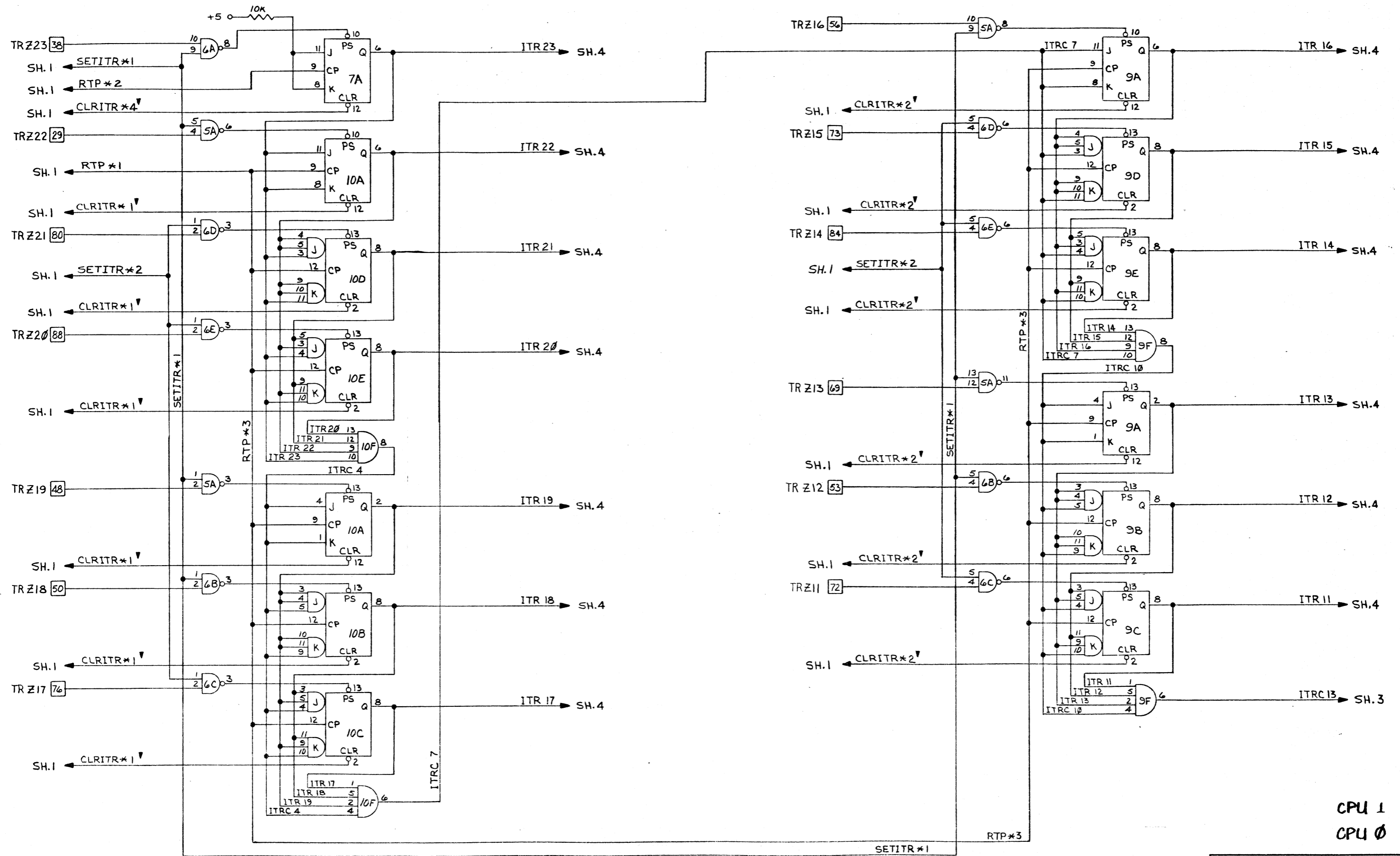
- UNLESS OTHERWISE SPECIFIED;
- 1. CAPACITORS ARE CD 10070
- 2. RESISTORS ARE 1/8W, 10% CARBON
- 3. J - JUMPER



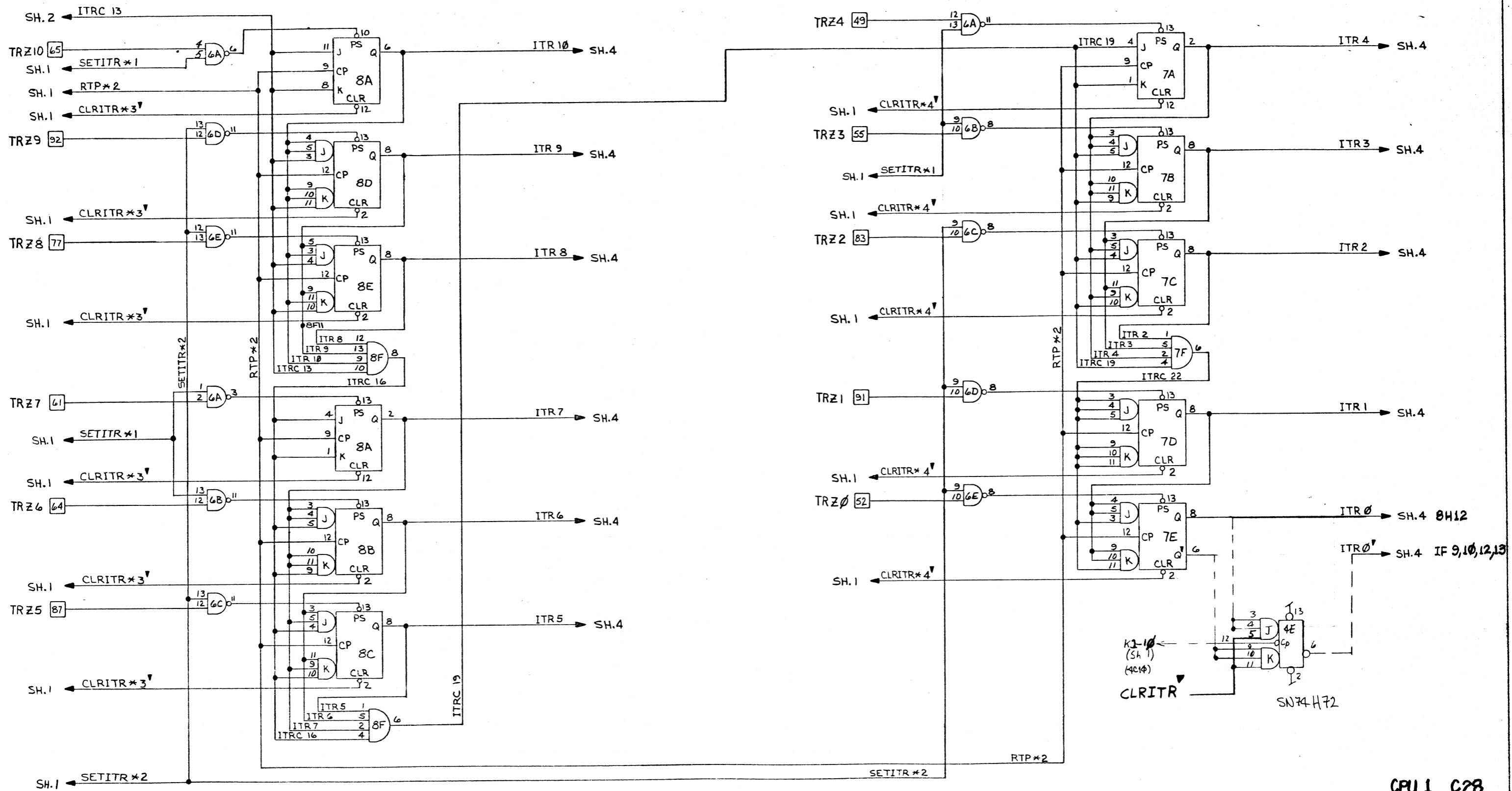
CPU 1 C28
CPU 0 C33

CPU 1 A32 1.5 C28, C32

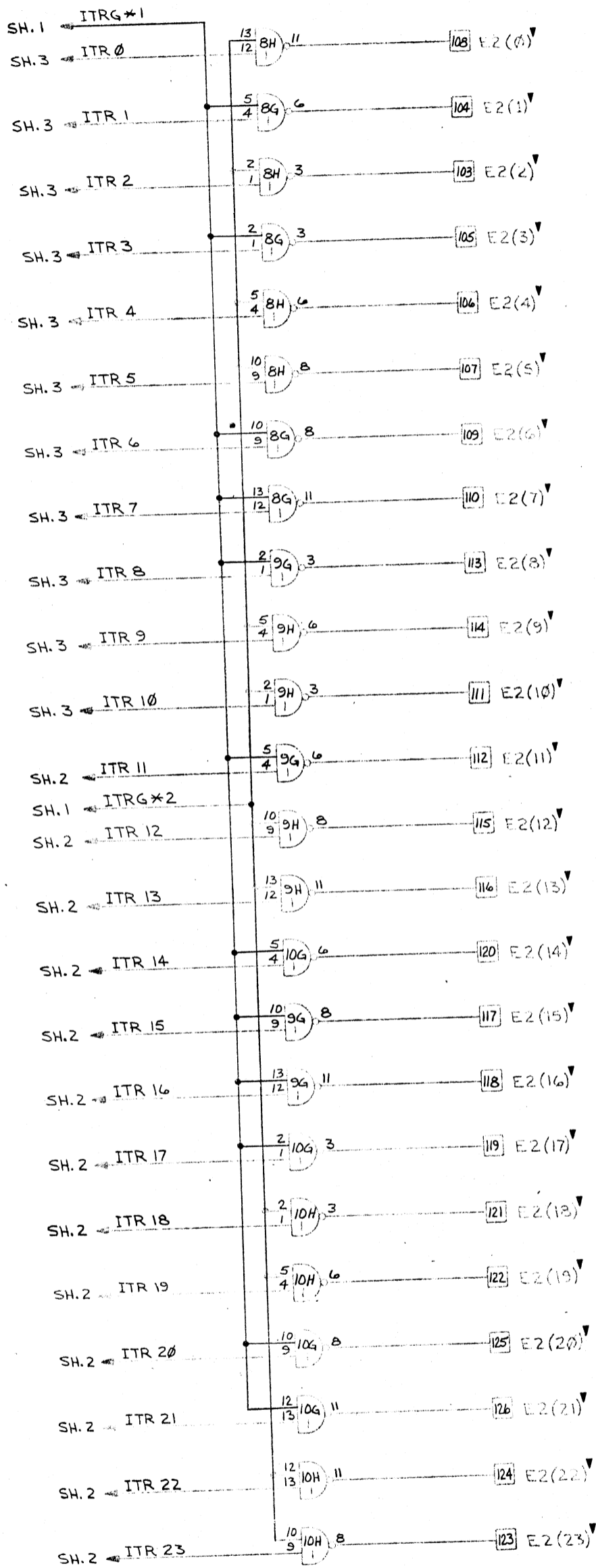
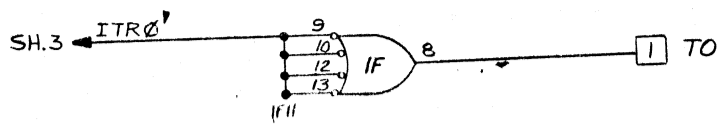
0	DATE	DATE	DATE	DATE
REVISIONS				
100108	REV	DESCRIPTION	DATE	BY
	1	INTERVAL TIME REGISTER (ITR)	10-7-69	D. MORENO
	2	CPU		
	3	NONE	1	4
			100108	E



SCALE: NONE	APPROVED BY:	DRAWN BY: DJM
DATE: 10-7-69		REVISED:
INTERVAL TIME REGISTER (ITR)		
CPU		DRAWING NUMBER: L00108



NO.	RELEASED	DESCRIPTION	DATE	BY	APPROVE
REVISIONS					
NO.	DATE	DESCRIPTION			
1	16-7-63	D. MORENO			
INTERVAL TIME REGISTER (ITR)					
PROJECT			CPU		
SHEET			3 4		
L00108			L00108.E		



L00108

CPU 1
CPU 0

INTERVAL TIME REGISTER (ITR)

CPU 1
CPU 0

10-7-69
D.MORENO
NONE 4 4 L00108