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DATE

TECHNICAL MEMORANDUM

TITLE: GUIDELINES FOR HARDWARE PERFORMANCE MONITORING, INCLUDING TEST POINT LIBRARI, OF 1100/80 SYSTEMS.

ABSTRACT: This memorandum presents information pertinent to the Hardware Performance Monitoring of 1100/80 Systems. Areas addressed are; specifications required of hardware monitoring equipment, probe installation and removal procedures, plugboard logic signal manipulation and test point library.

DESCRIPTORS: 1100/80 Systems, Hardware Performance Monitoring, Test Point Library.

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PROJ. NO.

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1.0 INTRODUCTION

The purpose of this Technical Memorandum is twofold. One, to outline the Development position regarding Hardware Performance Monitoring of 1100/80 Systems. Secondly, to provide hardware monitoring instrumentation information for the 1100/80 Computer System. The system units instrumented for monitoring are the Processing Units, the Storage Interface Units (SIU's), and the Input/Output Units (IOU's).

Items addressed are as follows:

- Specifications required of Hardware Monitoring Equipment to be connected to 1100/80 Systems.
- Probe Installation/Removal Procedures.
- Hardware Monitoring Instrumentation Information.
- 1100/80 System Hardware Monitoring Test Point Library.

2.0 APPLICABLE DOCUMENTS

- 1100/80 Product Description S-70140
- 1100/80 Equipment Specifications
  - Type 3032 Processing Unit SA01093
  - Type 3033 Input/Output Unit SA01469
  - Type 7022 Storage Interface Unit SA01465
  - Type 7039 Storage Interface Unit SA01640
- 1100/80 System Hardware Monitoring Test Points - drawing #4198497.

3.0 HARDWARE MONITORING EQUIPMENT SPECIFICATIONS

It is recommended that Hardware Monitoring Equipment meet the following specifications to be connected to 1100/80 Systems.

Probes

For absolute freedom of probe placement (driving source and/or loads) probes should have:

- A minimum impedance of 50K ohms.
- A maximum capacitance of 10 pf.

If probe placement is restricted to driving or source pin connections, specifications can be relaxed to :

- A minimum DC resistance of 5K ohms.
- A maximum capacitance of 30 pf.

Pulse Width

Equipment should be capable of responding to a pulse width of:

- 8 nsec. for clock signals.
- 25 nsec. for other signals.

All signals specified in the Test Point Library (Section 6.0) are signals other than clock signals.

Operating Frequency

Equipment should be capable of operating at a frequency of 20 Mhz.

Pulse Amplitude

Equipment should be capable of responding to a pulse amplitude changes of 600 mv. or greater.

4.0 PROBE INSTALLATION REMOVAL PROCEDURES

The following probe installation and removal procedures are recommended where Univac has the maintenance contract or the system is leased.

- Probes should be installed/removed during dedicated system time.
- Site Customer Engineers (CE's) should install/remove all probes, or
- Site CE's should approve and supervise the installation/removal of all probes.
- Qualified Univac personnel should be permitted to install/remove probes.
- Frequent removal and re-installation of probes should be discouraged.

4.1 Testing After Probe Installation or Probe Removal

It is recommended that Diagnostic Software be run on all modules after probes have been installed or removed. This will help identify problems that could result from the probe installation or removal process.

If a module(s) experiences intermittent problems after probes are connected, it is recommended that margin tests be run on said module(s). If a module fails the margin tests, probes should be removed one at a time, and the margin tests rerun until the problem probe(s) and corresponding test point(s) and net(s) are isolated. This information should be forwarded to the Tech Support home office permitting the initiation of corrective action.

5.0 HARDWARE MONITORING INSTRUMENTATION INFORMATION

The performance monitoring of the 1100/80 System is accomplished by using hardware monitoring equipment such as the Compress Dynaprobe or Tesdata systems. This equipment must be capable of meeting the specifications as described in Section 3.0 of this document. The monitoring signal must be a source point on a signal that is terminated through 50 ohms to the minus two (-2) volt bus.

The equipment used for in-house monitoring is the Tesdata MS88 System. This equipment provides the means of sampling the specific 1100/80 signals, performing logic manipulation, and storage of monitored data. The Tesdata equipment is also capable of performing on-line data reduction and report generation. Univac has modified the MS88 System with two sets of 16 high-speed counters and a 1024x32 bit high speed buffer. These modifications greatly expand the monitoring or collection of data by other types of hardware monitoring equipment as long as the equipment meets the requirements of Section 3.0 of this document.

The hardware monitoring task is accomplished by generating a unique logic plugboard for the collection to be taken and placing the monitor probes within the 1100/80 System units. The installation of the monitor probes requires the use of extreme care and caution plus some familiarization of the 1100/80 System unit cabinet layout. The procedures as outlined in Section 4.0 of this document must also be met.

ECL logic is used within the 1100/80 processor and SIU cabinets, and TTL logic is used within the IOU cabinet. The placement of the probe varies with the monitoring equipment used. The placement must be followed by the calibration of the probe and varification of the signal received at the monitor.

The Tesdata probes should be calibrated to 4.6 volts at the concentrator. The red lead is used on the ground back panel pin (21) on any 1100/80 connector and the black lead is used on the signal pin for ECL circuitry.

The Comress Dynaprobe probes should be adjusted to minus 1.3 (-1.3) volts threshold at the logic plugboard. The black probe lead is connected to the ground back panel pin (21) on any 1100/80 connector, and the red lead is used on the signal pin for ECL circuitry.

The ECL logic levels are:

high level = -0.8 volts
low level = -1.8 volts

The TTL logic levels are:

high level = 0.0 volts
low level = -4.0 volts

On the Tesdata plugboard the high level is the false signal and the low level is the true signal level.

The Comress Dynaprobe plugboard, the high level is the true signal level and the low level is the false signal level.

Examples of the logic performed by the logic plugboard on such signals as the CPU Busy, Instructions Executed, and other collection signals are shown in Section 5.1.

The output of the logic elements is sent to the Tesdata collectors. The collectors use the signal in either a map, count, or time mode. The time mode operation is where the signal enables a counter to be incremented at a predetermined rate. The map mode configuration maintain counts of predetermined parameters and time periods. In the count mode, each positive going edge of the signal is counted.

5.1 Plugboard Logic Signal Manipulation

The following paragraphs describe the logic performed by the logic plugboard with the Tesdata equipment. This logic manipulates monitored 1100/80 System signals into desired signals for use in determining the various performance parameters. The performance parameters are recorded on magnetic tape for later reduction or report generation purposes.

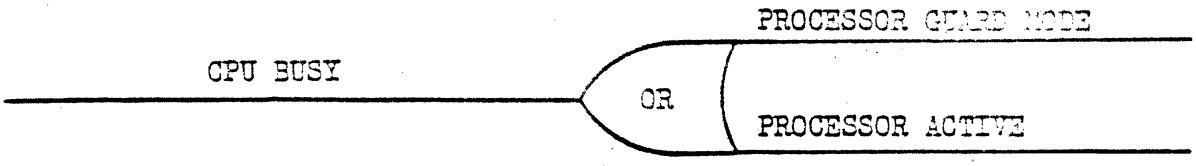
5.1.1 CPU Busy Time

The CPU Busy parameter is the processor time spent doing useful work (i.e., not in the EXEC idle loop). This parameter is determined with the probe monitored Processor Guard Mode signal, ORed with a probe monitored Processor Active signal. The 1100/80 Processor Guard Mode signal is a logic signal generated within each processor by the setting of the PSR register D2 flip flop. This signal is generated whenever the Guard Mode or User Mode of operation is to be executed.

The Processor Active signal (or not EXEC idle) is derived from the Block Transfer instruction (F22.X=0) execution. This signal is generated during the execution of approximately eleven instructions while the processor is in the idle loop. The idle loop method of determining the CPU Busy parameters introduces a small amount of error (approx. 4%) in the actual system performance.

In the near future, a possible improvement in measuring the processor busy will be accomplished by using the PSR register D30 bit, or another specific bit for idle designation. The setting of PSR bit D30 during the idle loop provides a more accurate Processor Active signal. The implementation of this approach requires a change in the Executive Program.

The logic used to determine CPU busy is as follows:



The CPU Busy signal is sent to a collector where it is used in the time mode. This time is used to determine the amount of time the processor is not idle. The CPU Busy signal is also used with other logic elements to generate CPU Busy, Instruction Counts, and CP overlap time, etc.

5.1.2 CPU Guard Mode (User) Time

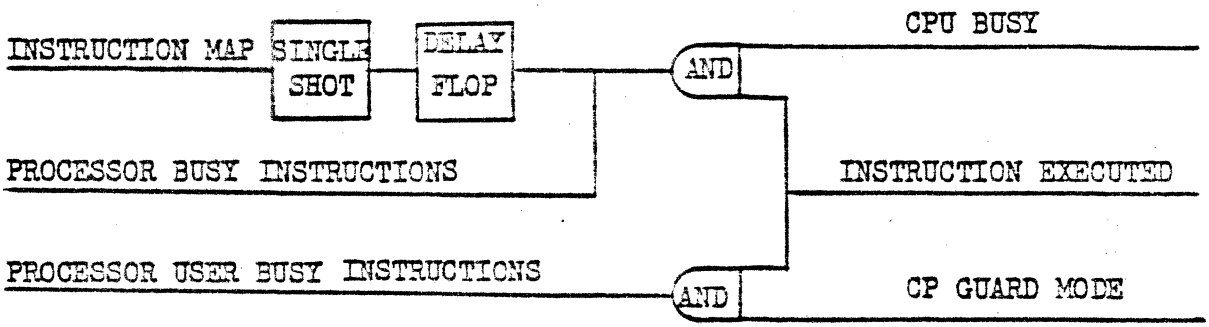
The CPU User time parameter is the time the processor spends doing User Program executions. This parameter is determined by the 1100/80 Processor Guard Mode signal (PSR D2 Set).

The signal is patched directly to a collector where it is used in the time mode. This signal is also used in other logic elements within the plugboard to generate additional User parameters.

5.1.3 Instruction Executed

The Instruction Executed signal is used to count the number of instructions executed while the processor is Busy, and also while the processor is in the Guard Mode (User). Other logic elements within the plugboard use the Instruction Executed signal for strobing other counters and for mapping capabilities.

The logic used to generate these parameters is as follows:



The Processor Busy and User instruction count signals both are sent to collectors where an accumulated count is maintained for the monitoring period. The instruction mapping signal is sent to a collector which is used in the collector map mode configuration.

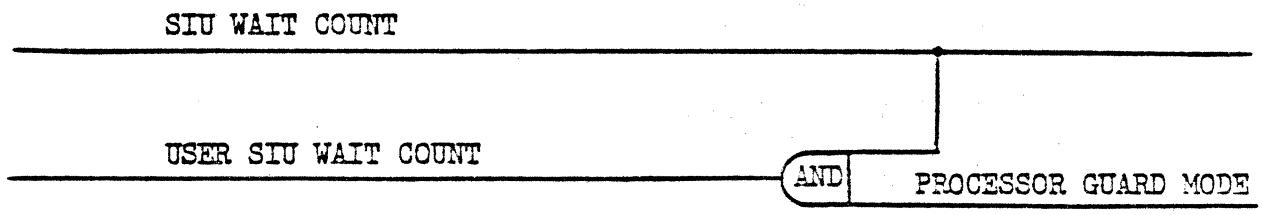
5.1.4 SIU Wait Count

The Storage Interface Unit (SIU) Wait Count is a signal generated by the 1100/80 processor whenever an SIU conflict is encountered. The conflict may be caused by the I/O, SIU Miss, 2nd CPU instruction, or operand port request pending; and disrupting the processor execution sequence.

A specifically designed 50 nanosecond pulse, the SIU Wait Count signal, is the output of a divide by 16 logic network within the 1100/80 equipment. Thus, the resultant 50 nanosecond pulse is the sixteenth 50 nanosecond wait cycle plus encountered by the processor. This signal represents a processor accumulated delay of 800 nanoseconds.

The SIU Wait Count signal is sent to a collector for maintaining the count of total SIU conflicts the processor encounters. The signal is also ANDed with the Processor Guard Mode signal to generate a User SIU Conflict signal. This represents a User delay of 800 nanoseconds for each count.

The logic used to generate this parameter is as follows:



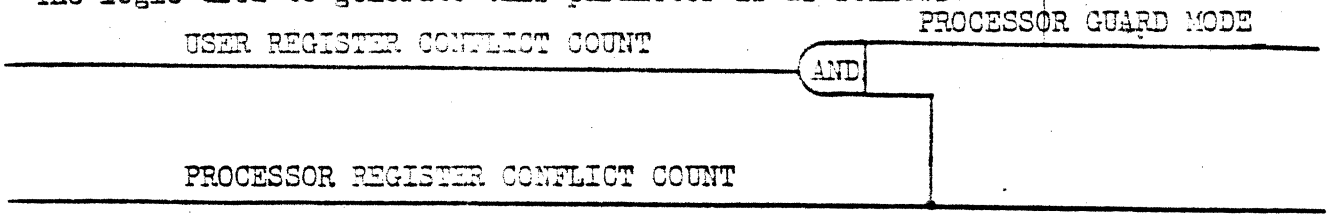
5.1.5 Register Conflict Count

The Register Conflict Wait Count is a signal generated by the 1100/80 processor whenever a conflict is encountered at the General Register Stack interface. This signal also represents the time a processor uses to re-fetch an instruction, whenever the original fetch was modified by skips or branches, etc.

Like the SIU Wait Count, the Register Conflict Count is the output of a divide by 16 logic network. Thus, the 50 nanosecond pulse represents the accumulation of sixteen 50 nanoseconds conflict time periods and a processor delay of 800 nanoseconds.

The Register Conflict Count signal is sent to a counter to maintain a count of the total register conflicts the processor encounters. The signal is also ANDed with the Processor Guard Mode signal to generate the User Register Conflict count. This signal then represents a User delay time of 800 nanoseconds for each count recorded.

The logic used to generate this parameter is as follows:



5.1.6 Storage Requests Count - 9222 TYPE SIU

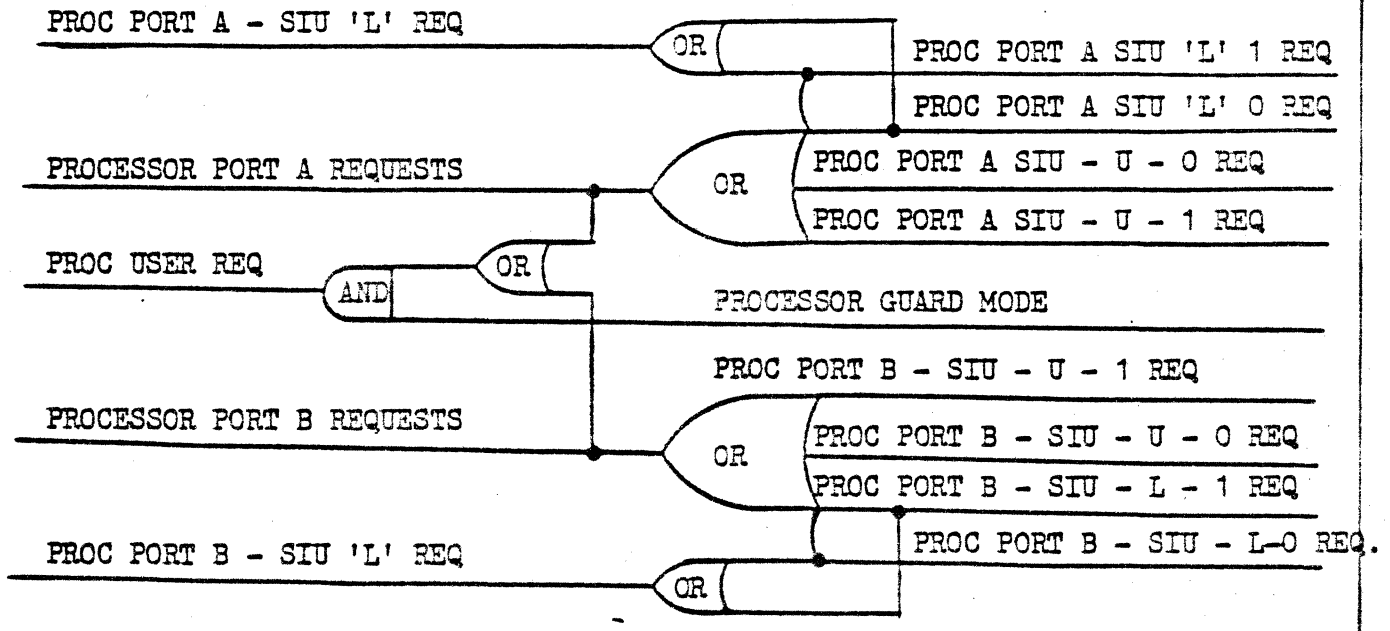
The Storage Request Counts are the results of using the Requestor Acknowledge pulses in each Storage Interface Unit (SIU). These acknowledge signals are sent by the referenced SIU to the Requestor to signify that the SIU has accepted this request. The acknowledges are issued for both the Odd Address, Segment 0, and the Even Address, Segment 1 sections of the SIU.

5.1.6.1 CPU Storage Requests

The CPU Request Counts are generated in the logic plugboard by ORing the SIU acknowledge pulses for each processor. The four input OR logic element is used, thus, the acknowledge pulses are grouped into instruction requests, Port A; and data requests, Port B. A two input logic OR element is used to generate the SIU lower instruction request or data request counts.

The User mode counts per processor are generated by ANDing the processor Guard Mode signal with the ORed processor Port A and Port B Request counts.

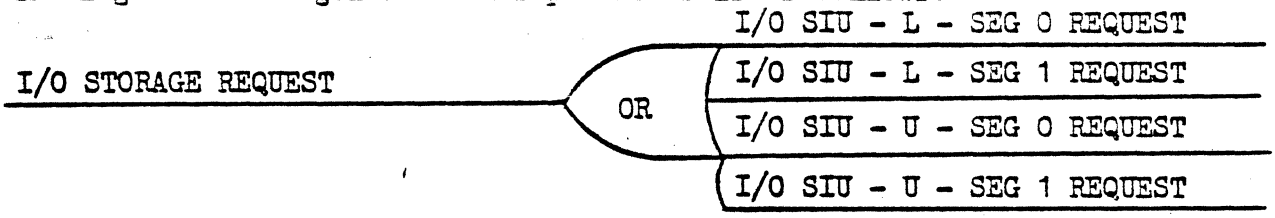
The following is an illustration of the logic used to generate the various counts for a processor. Each output of the logic is sent to a collector.



5.1.6.2 I/O Storage Request Counts

The I/O Storage Request counts are generated in the same manner as the CPU storage request. The SIU acknowledge pulses are ORed together for an I/O unit to produce the storage counts. The output of the logic plugboard is sent to a counter.

The logic used to generate this parameter is as follows:

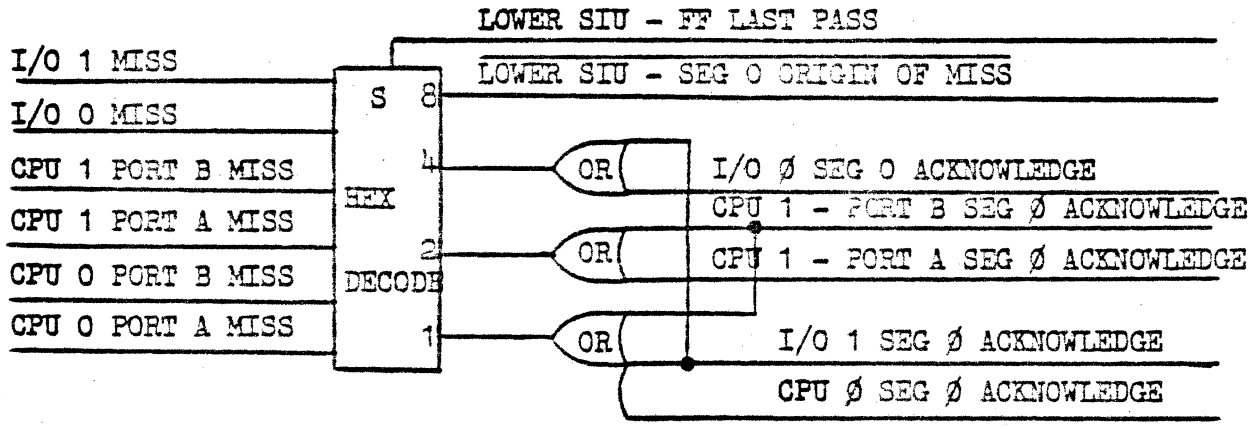


5.1.7 SIU Reference Misses – 7022 Type SIU

The Storage Interface Unit (SIU) Reference Miss parameter is a significant factor to system performance. To accomplish the counting of the SIU misses, the SIU provides the FF Last Pass signal to signify the completion of accepting the Backing Store data. This data was requested due to a data miss in the SIU. Another signal is the FF Segment 0 Origin of miss, which signifies that Segment 0 of that SIU is the originator of the Miss Data request to the Backing Store. The use of these two signals and the Segment Acknowledge pulse identifies the Requestor that encountered the missed data anomaly.

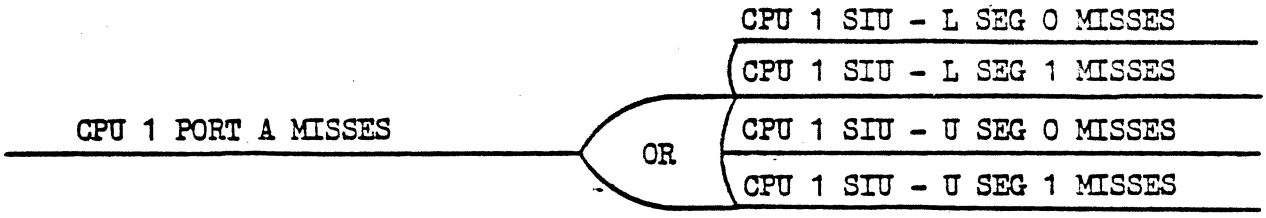
A hex-decoder logic element in the logic plugboard is used to isolate the specific requestor that encountered the SIU miss. A hex-decoder for each segment of either SIU is required to accomplish this requestor selection.

The following logic illustrates the selection of Segment 0 of the SIU lower Missed Data requestor. The false, Segment 0 origin of miss, signal enables the translation of 1 of 6 requestor acknowledge active pulses. The outputs of the hex-decoders are used with additional logic before going to the counters.



The output of the four hex-decoders are ORed together for each of the six requestors to enable the counting of the data misses.

The following logic illustrates the typical ORing used for the determination of the CPU instruction misses, Port A; CPU operand misses, Port B; and I/O misses.

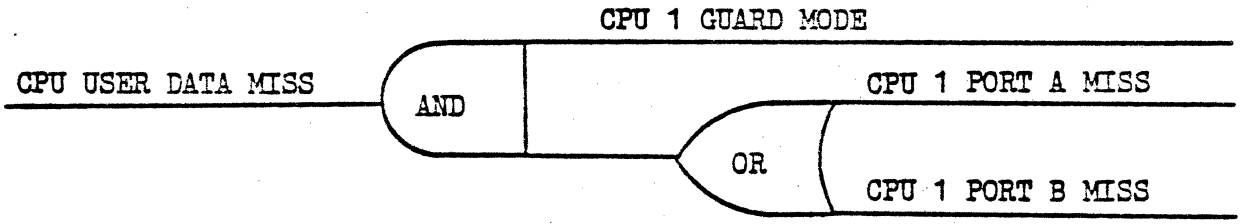


The output of the OR element is sent to the collector counters for data recording.

5.1.7.1 CPU User SIU Misses

The output of both Port A and Port B misses for each CPU ORed together and ANDed with the CPU Guard Mode Signal to enable counting the User Data misses.

The following logic accomplishes this parameter:



5.1.8 Other Processor Signals Monitored

The previously described monitor parameters, used some logic manipulation before routing the signal to the collectors. The following signals are monitored and routed directly to the collectors. These parameters may be counted by the counters, or used in a map mode.

5.1.8.1 CPU Total Interrupt's

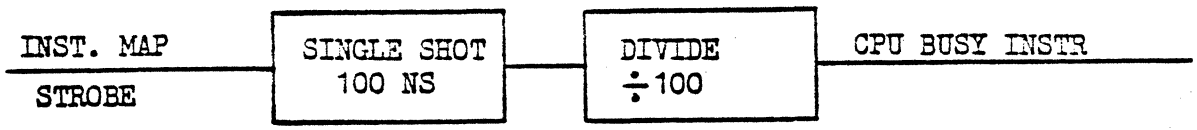
The counting of the number of interrupts a processor actually honors uses the Sequence IN22 signal in the processor. This signal is generated by the processor during Sequence 2 of the Interrupt Routine, regardless of the type of interrupt.

5.1.8.2 Function Code Map

The accomplishment of mapping the instruction types executed by a processor uses the Instruction Register F2 flip flops. The outputs of bits 26 thru 35 of the F2 register are routed directly from the monitor probe input directly to the collector input. The collector is used in the map mode.

To accomplish the mapping, a strobe pulse is required to gate the collector. This signal is derived by using the CPU Busy instruction parameter and dividing this signal by 100 and using a one shot logic element to product a 100 nanosecond pulse to strobe the collector.

The logic used to generate this parameter is as follows:



Thus, the resultant instruction map is actually a map of every 100th instruction executed.

5.1.9 I/O Unit Monitoring

The hardware performance monitoring of the input output section of the 1100/80 System shall be accomplished in a manner similar to the previously discussed processor monitoring. The performance monitoring shall consist of monitoring the I/O signals that are addressable on a channel basis.

The I/O unit consists of an I/O Control Module and up to four channel modules. The Channel Modules may be a word channel, a byte channel or a block multiplexer channel module type.

The Word Channel Module consists of up to four 30 to 36 bit word channels, each interfacing with a Peripheral Control Unit. The Byte Multiplexer Channel Module is a single channel consisting of up to eight subchannels each capable of controlling eight Peripheral Subsystem Control Units. The Block Multiplexer Channel Module is a single channel consisting of up to 132 subchannels each capable of controlling eight Peripheral Subsystem Control Units.

An I/O expansion feature is available which adds up to four additional Channel Modules. Hardware monitoring of the expansion feature is not discussed in this document, although the approaches discussed would be applicable to the expansion Channel Modules.

5.1.9.1 I/O Storage Monitoring

The monitoring of the I/O unit to Storage Interface may become as detailed as desired with the test points provided in the "1100/80 System Hardware Monitoring Test Points" document drawing #4198497.

The overall I/O requests, and number of misses may be derived as previously described in Paragraph 5.1.6.2 and 5.1.7 of this document.

The following paragraphs describe a method of obtaining memory request parameters on a channel basis.

5.1.9.1.1 I/O Storage Requests

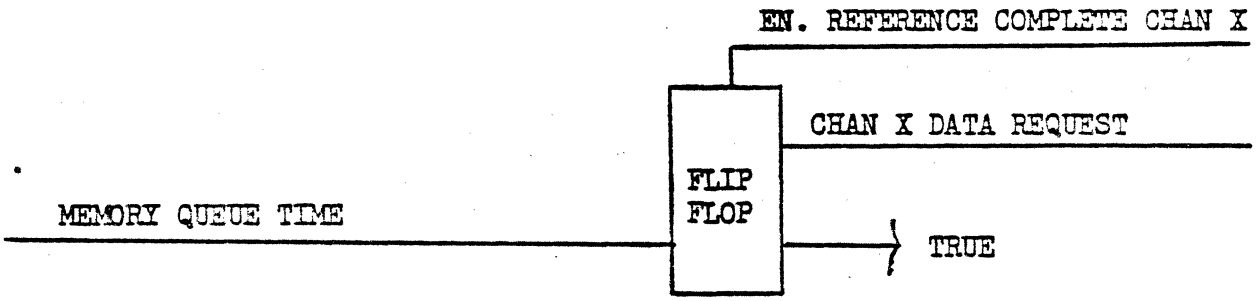
The I/O Storage Request parameters may be determined by using the Channel Data Request signal. This signal is unique for each channel and also one signal for the Control Module.

These signals may be routed directly to a collector to count the number of requests made.

5.1.9.1.2 I/O Memory Queue

To establish the I/O Memory Queue time parameters, the Channel Data Request signal is used to set a flip flop. The Enable Reference Complete signal is used to clear the flip flop. Both of these signals are unique for a channel and also one signal for the Control Module. The output of the flip flop is routed directly to a collector, where it is used in the time mode.

The logic used is as follows:

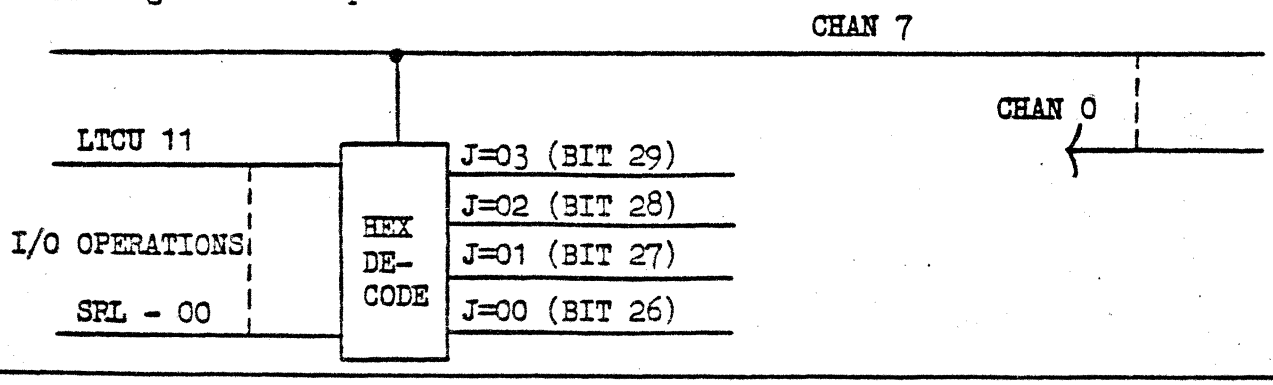


The Average Queue time is derived from the accumulated queue time divided by the number of storage references made.

5.1.9.2 I/O Operation

The I/O Operation monitoring shall consist of capturing and counting the executions of I/O instructions by the processors. The translation of the various operations or functions shall be undertaken on a channel basis; the processor initiate I/O signal is used to strobe the hex-decoder, and is also routed to a counter to accumulate the count of total operations per processor.

The logic used to perform the translation is as follows:



The output of the logic is sent to the various collectors for mapping or counting purposes. If additional or more detailed monitoring is required, the use of the supplied test points in document #4198497 may be used. These test points may be used as direct collector inputs, as the count of Interrupt Requests etc., or to perform logic manipulation of the signals.

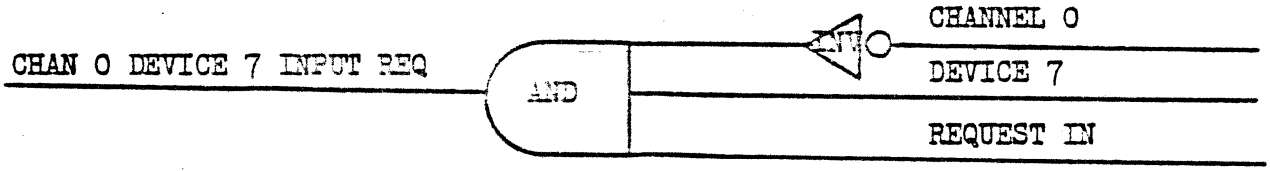
5.1.9.3 I/O Control Module to Channel Module Monitoring

The I/O Control Module to Channel Module interface monitoring shall consist of channel or device addressable parameters. These parameters may consist of operation or function distributions, interrupts, storage requests or the mapping of channel or device activity.

5.1.9.3.1 Byte and Block Channel

The Byte and Block Channels consist of a multiplexed interface and is usually on channel 00, and channel 01. The channels utilize an input and an output data bus to communicate to peripheral control units. To monitor a specific subchannel or device requires the use of the channel or device register bits and using these signals as enables or logic inputs to AND, OR, logic elements.

An example of Device 7 on channel Ø input request would use logic similar to the following:



5.1.9.3.2 Word Channel Module

The Word Channel Module consists of up to four parallel 30/36 bit channels. Additional channels may be added by use of the expansion capability of the 1100/80 System. The monitoring and test points included in this document only addressed the non-expanded interface. The test points in Section 6 have been selected to be used for monitoring on a channel basis.

The monitoring may consist of counting the individual channel requests acknowledges, or also on a composite or total number of interrupt requests. To count the number of input, output or external interrupt requests would require the selection of the individual channels test point for the parameter desired and routing it directly to a counter. The signal may also be used to set a FF and the corresponding acknowledge pulse used to clear the FF. This would enable the output of the FF to be used in either the count or time modes to establish queue times.

5.1.10 Additional Monitor Signals

The following signals are available within the system for hardware monitoring. The signals may be combined with the various logic elements available in the logic plugboard. These logic elements are AND, OR, flip flop, Delay Flops, One Shots, Decoders, one 32 bit comparator, Inventors and other type of logic. The logic is configured by using patch cord wires.

5.1.10.1 FF1 Wait A

The FF1 Wait A control signal is associated with an instruction request on Port A of the SIU. The signal is generated by setting a flip flop on the Instruction Request signal. The flip flop is cleared with the SIU acknowledge pulse to the requestor. This signal may be as short as 163 nanoseconds if the data is available in the SIU. This FF1 Wait A signal is used by the processor to control the IG (Instruction Generation) sequences.

5.1.10.2 FF0 Wait B

The FF0 Wait B control signal is identical to the FF1 Wait A, only it is associated with requests made on Port B of the SIU. Port B is usually associated with operand requests. The processor uses the FF0 Wait B signal to control the OG (Operand Generation) sequences. If the FF0 Wait B signal should be set whenever the processor expects operand data, the processor will loop between phase 1 and 4 of the sequence until the Wait FF is cleared. If the operand sequence is looping this causes the instruction sequence to loop also, because the operand sequence is not available to receive the next instruction.

5.1.10.3 Breakpoint Sync Signal

The Breakpoint Sync Signal is generated in the processor whenever the contents of the "P" Register equals the value set in the Breakpoint Register. This signal is generated before the Interrupt is requested to enable use of the signal for measurement purposes with Interrupts disabled.

5.1.11 7038 Type SIU Measurements

5.1.11 . 7039 Type SIU measurements

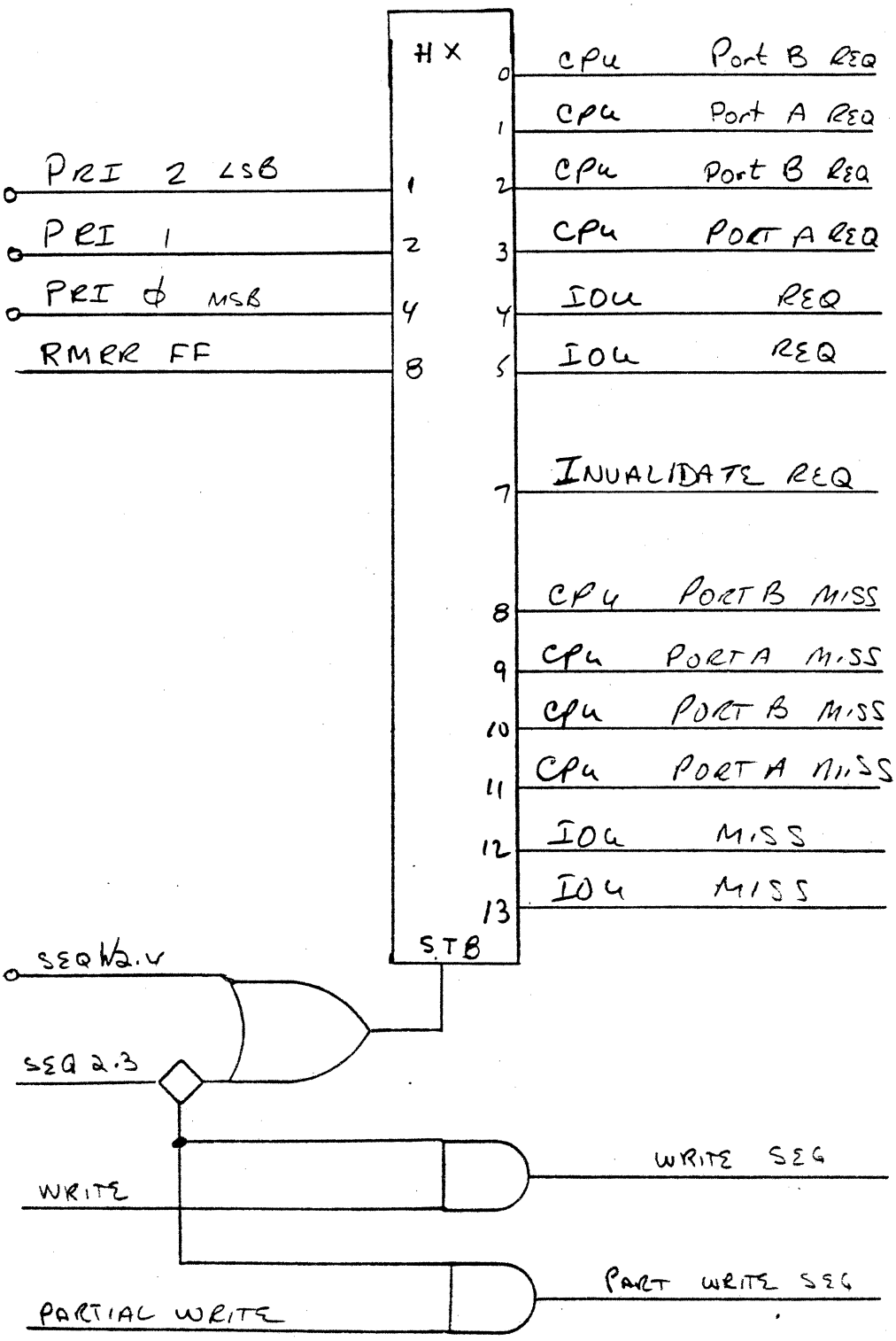
The 7039 Type SIU is used in the 1100/90A systems. This SIU Type is segmented into 4K words of 4 word blocks of intermediate Storage. The 7039 SIU employes a write through method. thus a write function addresses backing store to write the word. Some delay may be encountered for a write function if the 4 word MSI address stack is full.

The 7039 type SIU contains the absolute address register bits per segment. These test points are listed in the test point library section 6.0. of this document. The absolute address allows memory mapping if this feature is desired for hardware monitoring.

5.1.111 Storage Requests and misses

The measurement of the Storage Requests and misses per segment is accomplished by using a Hex decoder logic element. the three priority bits RP000 - RP002 are used to select the requestor and the 1st RMKR FF is used to determine the Read miss that a requestor encounters

The following is an illustration of the logic used to determine the requestor, the requestor encountering a Read miss, the write and partial write functions per SIU segment. There are only 4 Hex decoders available in the logic board, thus only one SIU Cluster or two partial SIU Clusters may be monitored at one time.


HX
PRI 2 LSB
PRI 1
PRI ϕ MSB
RMRR FF
1
2
4
8
STB
0 CPU Port B REQ
1 CPU Port A REQ
2 CPU Port B REQ
3 CPU PORT A REQ
4 IOU REQ
5 IOU REQ
7 INUALIDATE REQ
8 CPU PORT B MISS
9 CPU PORT A MISS
10 CPU PORT B MISS
11 CPU PORT A MISS
12 IOU MISS
13 IOU MISS
SEQ W2.V
SEQ 2.3
WRITE
PARTIAL WRITE
WRITE SEQ
PART WRITE SEQ

6.0 HARDWARE MONITORING TEST POINT LIBRARY

The following test point library contains test point definitions for the 3032 processor (Rev T), 7022 SIU (Rev M), 7039 SIU (Rev J) and 3033 IOU (Rev M). The IOU test points include the Byte Mux Channel Module (Rev M), the Block Mux Channel Module (Rev M), and the 1100 Word Channel Module (Rev M).

The test points defined in the library are only valid for the specified revision level of each system module. Systems containing modules with later revision levels should reference the "1100/80 System Hardware Monitoring Test Points" document, drawing number 4198497. This document contains current and past revision test point definitions for the 7022 and 7039 SIU's, 3032 processor and 3033 IOU.

The test point library was generated and used by the Systems Analysis group in Roseville relative to computer evaluation studies performed by the group. Because the group studies did not involve the utilization of all 1100/80 System test points, the library presents a limited set of test points. Other test points were not documented as they were not identified as being useful, or they were not pertinent to the computer evaluation studies. The library is provided as a convenience for persons wishing to perform hardware monitoring on 1100/80 Systems and is or was not intended to be a total composite list. Other test points may be desired by the monitoring analyst to accomplish his monitoring task and these points will have to be obtained from the corresponding logic drawing. The "1100/80 System Hardware Monitoring Test Points" document (drawing #4198497) will be updated as required to reflect modified or newly used test points.

The nomenclature used in the test point library corresponds to the 1100/80 cabling nomenclature. This nomenclature identifies the test points in connector locations A thru H, whereas the logic diagram identify the P.C. card connector locations as A card connectors, A through D, and E card connectors as A through D.

Figure 6-1 illustrates the logic and test point nomenclature encountered for a Register Type P.C. card used in two locations in the 1100/80 cabinet.

The E card location connector A, corresponds to E test point connector E location, i.e., logic diagram card E32 pin A59 corresponds to test point E32 pin E59. The B card connector corresponds to test point F connector location; the C card connector corresponds to test point G connector location, and the D card connector corresponds to test point H connector location.

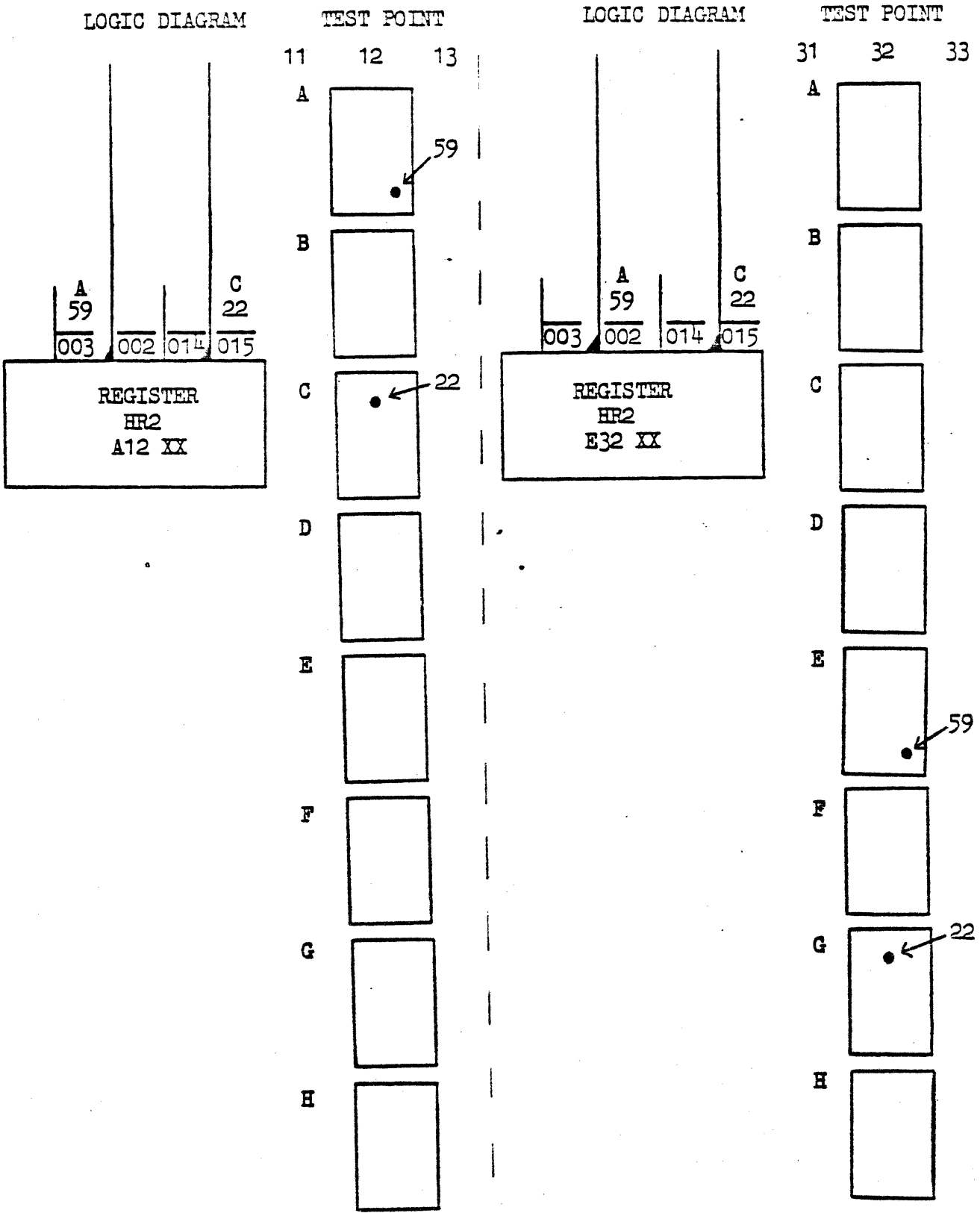


FIGURE 6-1 LOGIC AND TEST POINT NOMENCLATURE

$ TPHMON - 1100/30 TEST POINT LIBRARY - VERSION 26 OCTOBER 1978

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CENTRAL PROCESSOR TEST POINTS

SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
INSTRUCTIONS EXECUTED	M6F	HIGH	A02	A27	C15	-
INSTRUCTIONS EXECUTED	M6F	LOW	A02	A27	C56	-
REGISTER CONFLICT WAIT COUNT	M6I	LOW	A02	A27	A60	-
SIU WAIT COUNT	P6A	LOW	A01	A07	C38	-
GRAB P	R3F	HIGH	A02	A32	A58	-
FFIWAITA	R0D	HIGH	A02	E12	E13	-
FFOWAITB	R0D	HIGH	A02	E04	G52	-
SEQ IN 22 (INTRPT SEQ)	R9A	LOW	A02	A17	A15	-
PROC ACTIVE	S5A	LOW	A02	A15	A58	-
GUARD MODE	S7F	LOW	A02	E25	E49	-
BREAKPOINT SYNC TEST POINT 1	R2D	HIGH	A02	E12	H04	-
**********						
P0 REGISTER						
RP0 23	P0E	HIGH	A02	E29	H10	-
RP0 22	P0E	HIGH	A02	E29	E13	-
RP0 21	P0E	HIGH	A02	E29	H50	-
RP0 20	P0E	HIGH	A02	E29	H17	-
RP0 19	P0E	HIGH	A02	E29	H03	-
RP0 18	P0E	HIGH	A02	E29	G54	-
RP0 17	P0E	HIGH	A02	E29	E41	-
RP0 16	P0E	HIGH	A02	E29	G08	-
RP0 15	P1E	HIGH	A02	E30	E58	-
RP0 14	P1E	HIGH	A02	E30	E54	-
RP0 13	P1E	HIGH	A02	E30	F54	-
RP0 12	P1E	HIGH	A02	E30	F13	-
RP0 11	P1E	HIGH	A02	E30	E15	-
RP0 10	P1E	HIGH	A02	E30	F41	-
RP0 09	P1E	HIGH	A02	E30	G11	-
RP0 08	P1E	HIGH	A02	E30	G55	-
RP0 07	P2D	HIGH	A02	E32	G30	-
RP0 06	P2D	HIGH	A02	E32	G53	-
RP0 05	P2D	HIGH	A02	E32	G12	-
RP0 04	P2D	HIGH	A02	E32	G19	-
RP0 03	P2D	HIGH	A02	E32	H02	-
RP0 02	P2D	HIGH	A02	E32	G17	-
RP0 01	P2D	HIGH	A02	E32	G60	-
RP0 00	P2D	HIGH	A02	E32	G22	-

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CENTRAL PROCESSOR TEST POINTS

SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
F2 REGISTER						
RF2 35	L3A	HIGH	A02	A13	D01	-
RF2 34	L3A	HIGH	A02	A13	D41	-
RF2 33	L3A	HIGH	A02	A13	A56	-
RF2 32	L3A	HIGH	A02	A13	A49	-
RF2 31	L3A	HIGH	A02	A13	A14	-
RF2 30	L3A	HIGH	A02	A13	C45	-
RF2 29	L3A	HIGH	A02	A13	D18	-
RF2 28	L3A	HIGH	A02	A13	D11	-
RF2 27	L3A	HIGH	A02	A13	D09	-
RF2 26	L3A	HIGH	A02	A13	D08	-
RF2 25	L3A	HIGH	A02	A13	B60	-
RF2 24	L3A	HIGH	A02	A13	A11	-
RF2 23	L3A	HIGH	A02	A13	D19	-
RF2 22	L3A	HIGH	A02	A13	D15	-
**********						
D BITS						
RP2 00 (D00)	S7D	HIGH	A02	E25	G47	-
RP2 01 (D01)	S7D	HIGH	A02	E25	G57	-
RP2 02 (D02)	S7D	HIGH	A02	E25	E11	-
RP2 03 (D03)	S7D	HIGH	A02	E25	F26	-
RP2 04 (D04)	S7D	HIGH	A02	E25	F58	-
RP2 05 (D05)	S7D	HIGH	A02	E25	F12	-
RP2 06 (D06)	S7C	HIGH	A02	E25	G51	-
RP2 07 (D07)	S7C	HIGH	A02	E25	G09	-
RP2 08 (D08)	S7C	HIGH	A02	E25	E54	-
RP2 10 (D10)	S7C	HIGH	A02	E25	G45	-
RP2 11 (D11)	S7C	HIGH	A02	E25	E09	-
RP2 12 (D12)	S7C	LOW	A02	E25	G56	-
RP2 13 (D13)	S7C	LOW	A02	E25	G53	-
RP2 14 (D14)	S7B	LOW	A02	E25	E58	-
RP2 15 (D15)	S7B	LOW	A02	E25	E55	-
RP2 16 (D16)	S7B	LOW	A02	E25	F54	-
RP2 17 (D17)	S7B	HIGH	A02	E25	F50	-
RP2 20 (D20)	S7B	HIGH	A02	E25	F01	-
RP2 21 (D21)	S7B	LOW	A02	E25	E20	-
RP2 22 (D22)	S7A	LOW	A02	E25	H47	-
RP2 23 (D23)	S7A	LOW	A02	E25	H44	-
RP2 29 (D29)	S7A	HIGH	A02	E25	F09	-
RP2 30 (D30)	S7A	HIGH	A02	E25	G22	-
RP2 31 (D31)	S7A	HIGH	A02	E25	G14	-
RP2 32 (D32)	S7A	HIGH	A02	E25	E42	-
RP2 33 (D33)	S7A	HIGH	A02	E25	H26	-
RP2 34 (D34)	S7A	HIGH	A02	E25	F56	-
RP2 35 (D35)	S7A	HIGH	A02	E25	F49	-

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SIU TEST POINTS 7022 TYPE SIU

SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
LOWER SIU HALF						
FFMISS IN PROGRESS	H3B	LOW	A03	A06	B06	-
FF SEG 0 ORIGIN OF MISS	H3B	LOW	A03	A06	B09	-
FF LAST PASS	H5H	LOW	A03	A08	A09	-
REQUESTOR ACKNOWLEDGES						
PROCESSOR 0 PORT A SEG 0	B1D	LOW	A04	A25	C01	-
PROCESSOR 0 PORT B SEG 0	B1D	LOW	A04	A25	C44	-
PROCESSOR 0 PORT A SEG 1	E3D	LOW	A03	A25	C01	-
PROCESSOR 0 PORT B SEG 1	E3D	LOW	A03	A25	C44	-
PROCESSOR 1 PORT A SEG 0	B1E	LOW	A04	A25	C13	-
PROCESSOR 1 PORT B SEG 0	B1E	LOW	A04	A25	C16	-
PROCESSOR 1 PORT A SEG 1	E3E	LOW	A03	A25	C13	-
PROCESSOR 1 PORT B SEG 1	E3E	LOW	A03	A25	C16	-
IOU 0 SEG 0	B1D	LOW	A04	A25	D04	-
IOU 0 SEG 1	E3D	LOW	A03	A25	D04	-
IOU 1 SEG 0	B1D	LOW	A04	A25	D07	-
IOU 1 SEG 1	E3D	LOW	A03	A25	D07	-
**********						
**********						
UPPER SIU HALF						
FFMISS IN PROGRESS	H3B	LOW	A01	A06	B06	-
FF SEG 0 ORIGIN OF MISS	H3B	LOW	A01	A06	B09	-
FF LAST PASS	H5H	LOW	A01	A08	A09	-
REQUESTOR ACKNOWLEDGES						
PROCESSOR 0 PORT A SEG 0	B1D	LOW	A02	A25	C01	-
PROCESSOR 0 PORT B SEG 0	B1D	LOW	A02	A25	C44	-
PROCESSOR 0 PORT A SEG 1	E3D	LOW	A01	A25	C01	-
PROCESSOR 0 PORT B SEG 1	E3D	LOW	A01	A25	C44	-
PROCESSOR 1 PORT A SEG 0	B1E	LOW	A02	A25	C13	-
PROCESSOR 1 PORT B SEG 0	B1E	LOW	A02	A25	C16	-
PROCESSOR 1 PORT A SEG 1	E3E	LOW	A01	A25	C13	-
PROCESSOR 1 PORT B SEG 1	E3E	LOW	A01	A25	C16	-
IOU 0 SEG 0	B1D	LOW	A02	A25	D04	-
IOU 0 SEG 1	E3D	LOW	A01	A25	D04	-
IOU 1 SEG 0	B1D	LOW	A02	A25	D07	-
IOU 1 SEG 1	E3D	LOW	A01	A25	D07	-

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SIU TEST POINTS 7039 TYPE SIU

SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
LOWER SIU HALF -CLUSTER 0 - SEGMENT 0 AND 2						
SIU READ MISSES:						
1ST RMRR FF SEG 0	B0D	LOW	A04	A09	B58	-
1ST RMRR FF SEG 2	N0D	LOW	A04	A11	B58	-
LOAD MSI STACK SEG 0	B2H	LOW	A04	A08	A60	-
LOAD MSI STACK SEG 2	B3H	LOW	A04	A10	A60	-
SIU MISSES:						
MEMORY ACK 2 SEG 0	K1H	LOW	A03	A11	C08	-
MEMORY ACK 2 SEG 2	P6H	LOW	A03	E12	G08	-
SIU CYCLES:						
SEQ 23 FF SEG 0	B0C	LOW	A04	A09	C51	-
SEQ 23 FF SEG 2	N0C	LOW	A04	A11	C51	-
SEQ W 24 FF SEG 0	BCC	HIGH	A04	A09	D56	-
SEQ W 24 FF SEG 2	N0C	HIGH	A04	A11	D56	-
SIU HITS:						
CONTROL MATCH SEG 0	B1J	HIGH	A04	A08	A04	-
CONTROL MATCH SEG 2	N1J	HIGH	A04	A10	A04	-
SIU WRITE CONTROL: (AND WITH SEQ 23 FOR WRITE COUNTS						
WRITE SEG 0	B2G	LOW	A04	A07	A53	-
WRITE SEG 2	B2H	LOW	A04	A07	C22	-
PARTIAL WRITE SEG 0	B2G	LOW	A04	A07	A30	-
PARTIAL WRITE SEG 2	B2H	LOW	A04	A07	D16	-
REQUESTOR ACKNOWLEDGES:						
PROCESSOR 0 PORT A SEG 0	B1A	LOW	A04	A08	A15	-
PROCESSOR 0 PORT B SEG 0	B1A	LOW	A04	A08	A54	-
PROCESSOR 0 PORT A SEG 2	N1A	LOW	A04	A10	A15	-
PROCESSOR 0 PORT B SEG 2	N1A	LOW	A04	A10	A54	-
PROCESSOR 1 PORT A SEG 0	B1A	LOW	A04	A08	C17	-
PROCESSOR 1 PORT B SEG 0	B1A	LOW	A04	A08	B54	-
PROCESSOR 1 PORT A SEG 2	N1A	LOW	A04	A10	C17	-
PROCESSOR 1 PORT B SEG 2	N1A	LOW	A04	A10	B54	-
IOU 0 SEG 0	B1A	LOW	A04	A08	C48	-
IOU 0 SEG 2	N1A	LOW	A04	A10	C48	-
IOU 1 SEG 0	B1A	LOW	A04	A08	D50	-
IOU 1 SEG 2	N1A	LOW	A04	A10	D50	-
SIU REQUESTS:						
MSI PRIORITY RP002 SEG 0 (MSB)	B0E	HIGH	A04	A09	B01	-
MSI PRIORITY RP001 SEG 0	B0E	HIGH	A04	A09	B14	-
MSI PRIORITY RP000 SEG 0 (LSB)	B0E	HIGH	A04	A09	C14	-
MSI PRIORITY RP002 SEG 2 (MSB)	B0E	HIGH	A04	A11	B01	-
MSI PRIORITY RP001 SEG 2	B0E	HIGH	A04	A11	B14	-
MSI PRIORITY RP000 SEG 2 (LSB)	B0E	HIGH	A04	A11	C14	-

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SIU TEST POINTS 7039 TYPE SIU

SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
ABSOLUTE ADDRESS SEG 0:						
MSI ADDRS REG RA723	B4E	HIGH	A04	A26	A52	-
MSI ADDRS REG RA722	B4E	HIGH	A04	A26	A14	-
MSI ADDRS REG RA721	B4E	HIGH	A04	A26	B09	-
MSI ADDRS REG RA720	B4E	HIGH	A04	A26	B10	-
MSI ADDRS REG RA719	B4E	HIGH	A04	A26	A48	-
MSI ADDRS REG RA718	B4E	HIGH	A04	A26	A09	-
MSI ADDRS REG RA717	B7F	HIGH	A04	A25	A02	-
MSI ADDRS REG RA716	B7F	HIGH	A04	A25	A46	-
MSI ADDRS REG RA715	B7D	HIGH	A04	A25	A10	-
MSI ADDRS REG RA714	B7D	HIGH	A04	A25	C59	-
MSI ADDRS REG RA713	B7D	HIGH	A04	A25	A08	-
MSI ADDRS REG RA712	B7D	HIGH	A04	A25	C55	-
MSI ADDRS REG RA711	B7D	HIGH	A04	A25	B07	-
MSI ADDRS REG RA710	B5E	HIGH	A04	A23	D09	-
MSI ADDRS REG RA709	B5D	HIGH	A04	A23	B44	-
MSI ADDRS REG RA708	B5D	HIGH	A04	A23	B07	-
MSI ADDRS REG RA707	B6D	HIGH	A04	A24	D05	-
MSI ADDRS REG RA706	B6D	HIGH	A04	A24	D08	-
MSI ADDRS REG RA705	B6D	HIGH	A04	A24	B14	-
MSI ADDRS REG RA704	B6D	HIGH	A04	A24	B15	-
MSI ADDRS REG RA703	B6D	HIGH	A04	A24	C07	-
MSI ADDRS REG RA702	B4E	HIGH	A04	A26	A43	-
MSI ADDRS REG RA701	B5E	HIGH	A04	A23	D43	-
MSI ADDRS REG RA700	B5E	HIGH	A04	A23	D10	-
ABSOLUTE ADDRESS SEG 2:						
MSI ADDRS REG RA723	B4G	HIGH	A04	A26	C17	-
MSI ADDRS REG RA722	B4G	HIGH	A04	A26	D02	-
MSI ADDRS REG RA721	B4G	HIGH	A04	A26	C12	-
MSI ADDRS REG RA720	B4G	HIGH	A04	A26	C14	-
MSI ADDRS REG RA719	B4G	HIGH	A04	A26	D09	-
MSI ADDRS REG RA718	B4G	HIGH	A04	A26	D53	-
MSI ADDRS REG RA717	B7F	HIGH	A04	A25	C49	-
MSI ADDRS REG RA716	B7F	HIGH	A04	A25	C12	-
MSI ADDRS REG RA715	B7E	HIGH	A04	A25	B01	-
MSI ADDRS REG RA714	B7E	HIGH	A04	A25	D07	-
MSI ADDRS REG RA713	B7E	HIGH	A04	A25	C45	-
MSI ADDRS REG RA712	B7E	HIGH	A04	A25	D59	-
MSI ADDRS REG RA711	B7E	HIGH	A04	A25	B16	-
MSI ADDRS REG RA710	B5G	HIGH	A04	A23	A02	-
MSI ADDRS REG RA709	B5D	HIGH	A04	A23	A11	-
MSI ADDRS REG RA708	B5D	HIGH	A04	A23	A12	-
MSI ADDRS REG RA707	B6F	HIGH	A04	A24	A58	-
MSI ADDRS REG RA706	B6F	HIGH	A04	A24	A19	-
MSI ADDRS REG RA705	B6F	HIGH	A04	A24	B22	-
MSI ADDRS REG RA704	B6F	HIGH	A04	A24	B43	-
MSI ADDRS REG RA703	B6F	HIGH	A04	A24	B03	-
MSI ADDRS REG RA702	B4G	HIGH	A04	A26	D03	-
MSI ADDRS REG RA701	B5G	HIGH	A04	A23	D17	-
MSI ADDRS REG RA700	B5G	HIGH	A04	A23	D52	-

SIU TEST POINTS — 7039 TYPE

SIGNAL NAME:	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
UPPER SIU HALF - SEGMENT 4 AND 6						
SIU READ MISSES:						
1ST RMRR FF SEG 4	B0D	LOW	A02	A09	B58	-
1ST RMRR FF SEG 6	N0D	LOW	A02	A11	B58	-
LOAD MSI STACK SEG 4	B2H	LOW	A02	A08	A60	-
LOAD MSI STACK SEG 6	B3H	LOW	A02	A10	A60	-
SIU MISSES:						
MEMORY ACK 2 SEG 4	K1H	LOW	A01	A11	C08	-
MEMORY ACK 2 SEG 6	P6H	LOW	A01	E12	G08	-
SIU CYCLES:						
SEQ 23 FF SEG 4	B0C	LOW	A02	A09	C51	-
SEQ 23 FF SEG 6	N0C	LOW	A02	A11	C51	-
SEQ W 24 FF SEG 4	B0C	HIGH	A02	A09	D56	-
SEQ W 24 FF SEG 6	N0C	HIGH	A02	A11	D56	-
SIU HITS:						
CONTROL MATCH SEG 4	B1J	LOW	A02	A08	A04	-
CONTROL MATCH SEG 6	N1J	HIGH	A02	A10	A04	-
SIU WRITE CONTROL:						
WRITE SEG 4	B2G	LOW	A02	A07	A53	-
WRITE SEG 6	B2H	LOW	A02	A07	C22	-
PARTIAL WRITE SEG 4	B2G	LOW	A02	A07	A30	-
PARTIAL WRITE SEG 6	B2H	LOW	A02	A07	D16	-
REQUESTOR ACKNOWLEDGES:						
PROCESSOR 0 PORT A SEG 4	B1A	LOW	A02	A08	A15	-
PROCESSOR 0 PORT B SEG 4	B1A	LOW	A02	A08	A54	-
PROCESSOR 0 PORT A SEG 6	N1A	LOW	A02	A10	A15	-
PROCESSOR 0 PORT B SEG 6	N1A	LOW	A02	A10	A54	-
PROCESSOR 1 PORT A SEG 4	B1A	LOW	A02	A08	C17	-
PROCESSOR 1 PORT B SEG 4	B1A	LOW	A02	A08	B54	-
PROCESSOR 1 PORT A SEG 6	N1A	LOW	A02	A10	C17	-
PROCESSOR 1 PORT B SEG 6	N1A	LOW	A02	A10	B54	-
IOU 0 SEG 4	B1A	LOW	A02	A08	C48	-
IOU 0 SEG 6	N1A	LOW	A02	A10	C48	-
IOU 1 SEG 4	B1A	LOW	A02	A08	D50	-
IOU 1 SEG 6	N1A	LOW	A02	A10	D50	-
SIU REQUESTS:						
MSI PRIORITY RP002 SEG 4 (MSB)	B0E	HIGH	A02	A09	B01	-
MSI PRIORITY RP001 SEG 4	B0E	HIGH	A02	A09	B14	-
MSI PRIORITY RP000 SEG 4 (LSB)	B0E	HIGH	A02	A09	C14	-
MSI PRIORITY RP002 SEG 6 (MSB)	B0E	HIGH	A02	A11	B01	-
MSI PRIORITY RP001 SEG 6	B0E	HIGH	A02	A11	B14	-
MSI PRIORITY RP000 SEG 6 (LSB)	B0E	HIGH	A02	A11	C14	-

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IOU TEST POINTS

SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
PROCESSOR 0 INTERFACE						
PROCESSOR AVAILABLE	YN1	LOW	A04	B34	29	-
INITIATE I/O	XU0	HIGH	A04	B41	24	-
INTERRUPT REQUEST	YP1	HIGH	A04	A56	64	-
INTERRUPT ACKNOWLEDGE	XU1	HIGH	A04	B41	47	-
CANCEL INTRPT REQUEST	XL1	HIGH	A04	B51	33	-
CANCEL INTRPT ACKNOWLEDGE	XI1	HIGH	A04	B57	61	-
MACHINE CHECK INT REQ CTRL	XF1	HIGH	A04	A46	28	-
MACHINE CHECK ACKNOWLEDGE	XU1	HIGH	A04	B41	65	-
TABLE INTERRUPT REQUEST	YO1	HIGH	A04	A57	19	-
TABLE INTRPT ACKNOWLEDGE	XU1	HIGH	A04	B41	55	-
INTERRUPT ERROR REQUEST	XU0	HIGH	A04	B41	35	-
PROCESSOR 1 INTERFACE						
PROCESSOR AVAILABLE	YN1	LOW	A04	B34	35	-
INITIATE I/O	XU0	HIGH	A04	B41	22	-
INTERRUPT REQUEST	YP1	HIGH	A04	A56	71	-
INTERRUPT ACKNOWLEDGE	XU1	HIGH	A04	B41	45	-
CANCEL INTRPT REQUEST	XL1	HIGH	A04	B51	34	-
CANCEL INTRPT ACKNOWLEDGE	XI1	HIGH	A04	B57	63	-
MACHINE CHECK INT REQ CTRL	XF1	HIGH	A04	A46	23	-
MACHINE CHECK ACKNOWLEDGE	XU1	HIGH	A04	B41	64	-
TABLE INTERRUPT REQUEST	YO1	HIGH	A04	A57	48	-
TABLE INTRPT ACKNOWLEDGE	XU1	HIGH	A04	B41	54	-
INTERRUPT ERROR REQUEST	XU0	HIGH	A04	B41	33	-
SIU LOWER INTERFACE						
STORAGE REQUEST SEG 0 FF	YC0	HIGH	A04	A44	02	-
STORAGE REQUEST SEG 1 FF	YC0	HIGH	A04	A44	12	-
HIT ACKNOWLEDGE FF	YC1	HIGH	A04	A44	65	-
MISS CTRL FF	YC0	HIGH	A04	A44	35	-
SIU UPPER INTERFACE						
STORAGE REQUEST SEG 2 FF	YC0	HIGH	A04	A44	23	-
STORAGE REQUEST SEG 3 FF	YC0	HIGH	A04	A44	34	-
HIT ACKNOWLEDGE FF	YC1	HIGH	A04	A44	64	-
MISS CTRL FF	YC0	HIGH	A04	A44	33	-

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IOU TEST POINTS SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
I/O COMMANDS						
INITIAL LOAD	XC0	LOW	A04	B61	57	-
LOAD TABLE CNTRL WORD (LTCW)	XC0	LOW	A04	B61	55	-
LOAD CHANNEL REGISTER (LCR)	XC0	LOW	A04	B61	42	-
HALT CHANNEL (HCH)	XC0	LOW	A04	B61	43	-
HALT DEVICE (HDV)	XC0	LOW	A04	B61	41	-
TEST SUBCHANNEL (TSC)	XC0	LOW	A04	B61	21	-
TEST I/O (TIO)	XC0	LOW	A04	B61	19	-
START I/O FAST REL (SIOF)	XC0	LOW	A04	B61	17	-
SENSE RELEASE (SRL)	XC0	LOW	A04	B61	16	-
CHANNEL 7 SELECT	XC1	LOW	A04	B61	58	-
CHANNEL 6 SELECT	XC1	LOW	A04	B61	59	-
CHANNEL 5 SELECT	XC1	LOW	A04	B61	54	-
CHANNEL 4 SELECT	XC1	LOW	A04	B61	53	-
CHANNEL 3 SELECT	XC1	LOW	A04	B61	46	-
CHANNEL 2 SELECT	XC1	LOW	A04	B61	36	-
CHANNEL 1 SELECT	XC1	LOW	A04	B61	40	-
CHANNEL 0 SELECT	XC1	LOW	A04	B61	35	-
DEVICE REGISTER BIT D07	XC0	LOW	A04	B61	09	-
DEVICE REGISTER BIT D06	XC0	LOW	A04	B61	13	-
DEVICE REGISTER BIT D05	XC1	LOW	A04	B61	73	-
DEVICE REGISTER BIT D04	XC1	LOW	A04	B61	75	-
DEVICE REGISTER BIT D03	XC1	LOW	A04	B61	80	-
DEVICE REGISTER BIT D02	XC1	LOW	A04	B61	65	-
DEVICE REGISTER BIT D01	XC1	LOW	A04	B61	66	-
DEVICE REGISTER BIT D00	XC1	LOW	A04	B61	72	-
CHANNEL MODULE MEMORY REFERENCES						
CONTROL DATA REQUEST	XK0	HIGH	A04	A60	17	-
CHANNEL 7 DATA REQUEST	WJ0	HIGH	A04	B76	10	-
CHANNEL 6 DATA REQUEST	W10	HIGH	A04	B75	10	-
CHANNEL 5 DATA REQUEST	WH0	HIGH	A04	B74	10	-
CHANNEL 4 DATA REQUEST	WG0	HIGH	A04	B73	10	-
CHANNEL 3 DATA REQUEST	WF0	HIGH	A04	A76	10	-
CHANNEL 2 DATA REQUEST	WE0	HIGH	A04	A75	10	-
CHANNEL 1 DATA REQUEST	WD0	HIGH	A04	A74	10	-
CHANNEL 0 DATA REQUEST	WC0	HIGH	A04	A73	10	-
CONTROL ENABLE REF COMPLT	XB0	HIGH	A04	B60	75	-
CHANNEL 7 ENABLE REF COMPLT	XB1	HIGH	A04	B60	30	-
CHANNEL 6 ENABLE REF COMPLT	XB1	HIGH	A04	B60	29	-
CHANNEL 5 ENABLE REF COMPLT	XB1	HIGH	A04	B60	09	-
CHANNEL 4 ENABLE REF COMPLT	XB1	HIGH	A04	B60	07	-
CHANNEL 3 ENABLE REF COMPLT	XB0	HIGH	A04	B60	70	-
CHANNEL 2 ENABLE REF COMPLT	XB0	HIGH	A04	B60	60	-
CHANNEL 1 ENABLE REF COMPLT	XB0	HIGH	A04	B60	43	-
CHANNEL 0 ENABLE REF COMPLT	XB0	HIGH	A04	B60	40	-

IOU TEST POINTS SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
BYTE AND BLOCK CHANNEL MODULE						
OPERATONAL IN	MM0	HIGH		A02	40	-
ADDRESS IN	MM0	HIGH		A02	64	-
STATUS IN	MM0	HIGH		A02	31	-
SERVICE IN	MM0	HIGH		A02	75	-
REQUEST IN	MM0	HIGH		A02	66	-
SERVICE OUT	ML1	HIGH		A01	64	-
COMMAND OUT	ML1	HIGH		A01	59	-
CHANNEL INACTIVE 2 SEQ	HR2	HIGH		A16	59	-
BUS IN 0	MM0	HIGH		A02	55	-
BUS IN 1	MM0	HIGH		A02	30	-
BUS IN 2	MM0	HIGH		A02	11	-
BUS IN 3	MM0	HIGH		A02	02	-
BUS IN 4	MM0	HIGH		A02	17	-
BUS IN 5	MM0	HIGH		A02	07	-
BUS IN 6	MM0	HIGH		A02	19	-
BUS IN 7	MM0	HIGH		A02	09	-
BUS IN PARITY	MM0	HIGH		A02	23	-
BUS OUT 0	ML0	HIGH		A01	41	-
BUS OUT 1	ML0	HIGH		A01	35	-
BUS OUT 2	ML0	HIGH		A01	04	-
BUS OUT 3	ML0	HIGH		A01	06	-
BUS OUT 4	ML0	HIGH		A01	13.	-
BUS OUT 5	ML0	HIGH		A01	16	-
BUS OUT 6	ML0	HIGH		A01	27	-
BUS OUT 7	ML0	HIGH		A01	24	-
BUS OUT PARITY	ML1	HIGH		A01	47	-

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IOU TEST POINTS

SIGNAL NAME	LOGIC PAGE	LOGIC LEVEL	PANEL LOC.	CARD SLOT	PIN NO.	PROBE NUMBER
WORD CHANNEL MODULE						
MACHINE CHECK FF	CP0	HIGH	A03	B74	23	-
TABLE STATUS REQ. FF	CP1	HIGH	A03	B74	25	-
INTERRUPT ERROR FF	DK1	HIGH	A03	B58	17	-
CHANNEL 0 INPUT ACTIVE FF	OP1	HIGH	A03	B26	79	-
CHANNEL 0 OUTPUT ACTIVE FF	OP1	HIGH	A03	B26	75	-
CHANNEL 1 INPUT ACTIVE FF	OR1	HIGH	A03	B25	79	-
CHANNEL 1 OUTPUT ACTIVE FF	OR1	HIGH	A03	B25	75	-
CHANNEL 2 INPUT ACTIVE FF	OP1	HIGH	A03	B26	59	-
CHANNEL 2 OUTPUT ACTIVE FF	OP1	HIGH	A03	B26	55	-
CHANNEL 3 INPUT ACTIVE FF	OR1	HIGH	A03	B25	59	-
CHANNEL 3 OUTPUT ACTIVE FF	OR1	HIGH	A03	B25	55	-
CHANNEL 0 FUNCTIONS	OA0		A03	B17		
EXTRNAL INTRPT REQUEST FF	"	LOW	"	"	-09	-
INPUT DATA REQUEST FF	"	LOW	"	"	-07	-
OUTPUT DATA REQUEST FF	"	LOW	"	"	-06	-
EXTERNAL FUNC. ACKNOWLEDGE	"	HIGH	"	"	-78	-
INPUT DATA ACKNOWLEDGE	"	HIGH	"	"	-79	-
OUTPUT DATA ACKNOWLEDGE	"	HIGH	"	"	-77	-
CHANNEL 1 FUNCTIONS	OB0		A03	B16		
SAME PIN NUMBERS AS CHANNEL 0						
CHANNEL 2 FUNCTIONS	OC0		A03	B15		
SAME PIN NUMBERS AS CHANNEL 0						
CHANNEL 3 FUNCTIONS	OD0		A03	B14		
SAME PIN NUMBERS AS CHANNEL 0						

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7.0 SUMMARY

In summary, the Hardware Monitoring Equipment Specifications and the Probe Installation/Removal Procedure information is provided as a guideline to maintain and build on the stability of 1100/80 Systems. Problems could potentially be injected into 1100/80 System Modules by hardware monitoring equipment not meeting the defined specifications. The probe installation/removal procedures are recommended to reduce the probability of error resulting from the probe installation or removal process. Testing (Diagnostic Software) is recommended on all modules that have had probes either installed or removed as this will help to identify problems that could result from the probe installation or removal process.

The Hardware Monitoring Instrumentation Information and the Hardware Monitoring Test Point Library are provided as a convenience for persons wishing to conduct or perform hardware monitoring on 1100/80 Systems. As stated in Section 6.0, the test point library contained herein is only valid for the specified revision level of each module and will not be updated. The "1100/80 Hardware Monitoring Test Point" document (drawing #4198497) will be maintained as required to reflect modified or newly used test points for each of the specified system modules.