NAVSHIPS 0967-280-4030

VOLUME III

TECHNICAL MANUAL

for

DIGITAL DATA COMPUTER
CP-642B/USQ-20(V)

SECTIONS 5 THROUGH 7

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SYLVANIA ELECTRONIC SYSTEMS
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DEPARTMENT OF THE NAVY
NAVAL SHIP SYSTEMS COMMAND

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TROUBLESHOOTING

5-1. GENERAL.

The logic troubleshooting concepts for the computer are based on the assumption that the troubles will be exposed while running the maintenance routines. The maintenance routines may be run as a result of observing incorrect operational results or they may be run as part of the preventive maintenance procedure. The maintenance routines (referred to as MROT - Maintenance Routines On Tape) are supplied with documentation containing the flow charts, program data sheets, the actual program, and procedures.

The MROT are such that most transmission paths, registers, designators, and modifiers are checked. Several options are available when JUMP or STOP options are selected. A malfunction can cause an error typeout and stop; the program can continue or it may recycle through the routine detecting the error. The error typeout indicates what type of error exists. In many cases, however, maintenance personnel must be relied upon to pinpoint the fault.

The repair concept consists of replacing the faulty printed circuit module with a known good module and verifying the bad module on a module tester. Usually no attempt is made in the field to repair such items as printed circuit modules, memory core stacks, or memory film stacks.

Troubleshooting the nonlogic circuits, such as the main power supply or console, consists of making voltage and/or resistance checks to determine the faulty component.

This section consists of the procedures for loading, running, and interpreting MROT as well as the test procedures for the nonlogic portions of the computer.

5-2. TEST EQUIPMENT AND SPECIAL TOOLS.

Test equipment and special tools required for effective troubleshooting are listed in table 5-1.

If the input/output jumper cables are not available, they may be fabricated as follows: obtain 32 90-pin input/output jacks and 16 90-conductor cables about 48 inches long. Connect the cables and jacks as indicated in paragraph 2-5f.

A module extender may be fabricated as follows: obtain a 15-pin male module connector and two 15-contact female connectors. Connect the male connector to the female connector with 36-inch lengths of wire (see figure 5-1). Connect the second female connector to the first with six-inch lengths of wire. The first female connector holds the module, and the second provides test points for all pins.

5-3. LOGIC TROUBLESHOOTING.

Troubleshooting the computer logic circuits is generally done by running the maintenance routines on tape (MROT) and interpreting the error typeouts (if any). The logic troubleshooting can take two forms. It may be desirable to run MROT or it could be more advantageous to run a specific instruction.

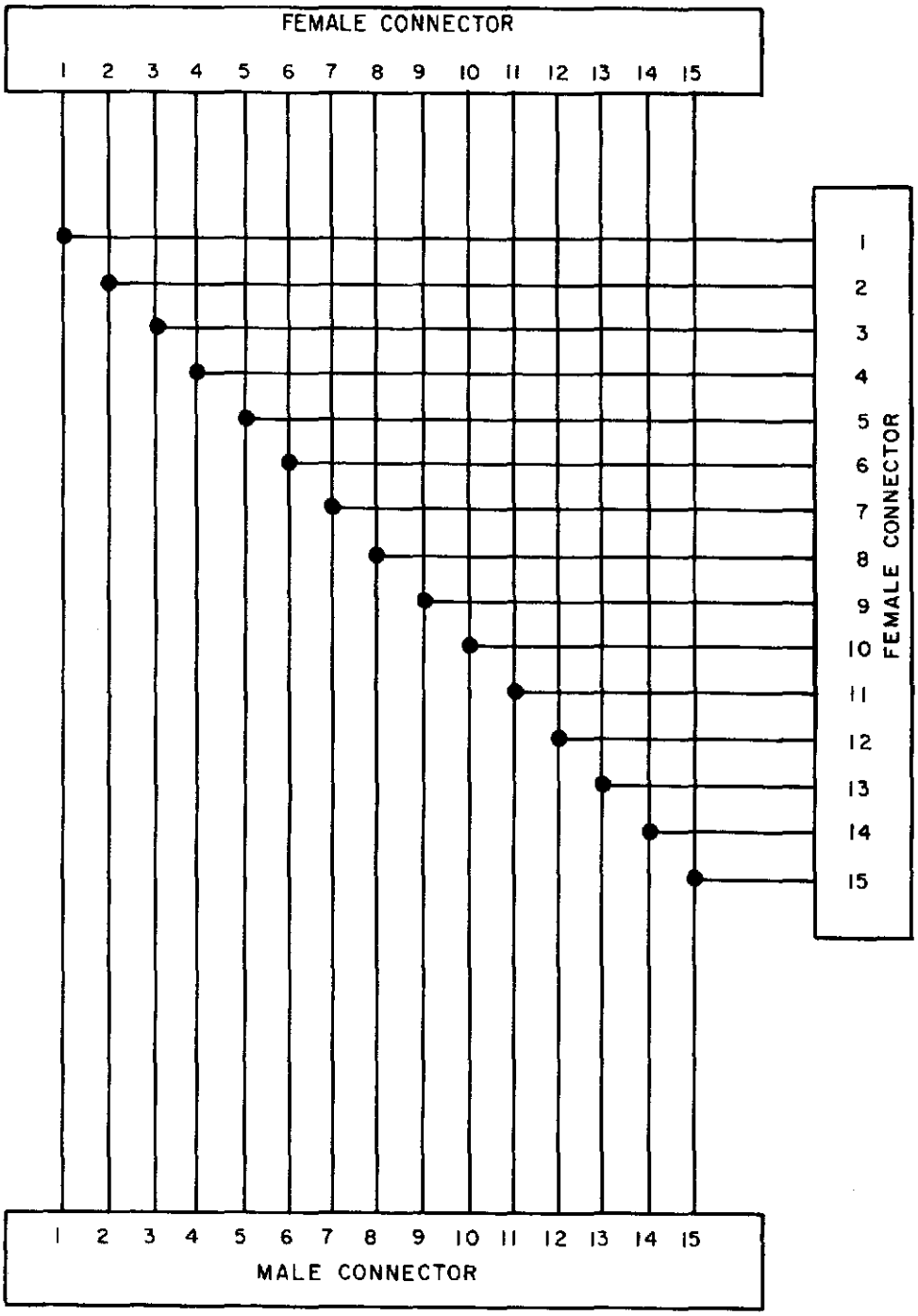


Figure 5-1. Module Extender Schematic

TABLE 5-1. TEST EQUIPMENT AND SPECIAL TOOLS

NOMENCLATURE		FUNCTION
NAME	DESIGNATION	
Multimeter	AN/PSM-4(C)*	Measure AC/DC voltages, currents, and resistances.
Oscilloscope	Tektronix 545*	View waveforms
Dual Channel Pre-Amplifier	Tektronix Type CA*	Two channel input
Current Probe & Termination	Tektronix Type P6016*	View memory current pulses
2 Voltage Probes		View voltage pulses
1 Probe		External sync probe
Tool Set	AN/USM-3*	General purpose
Hand stripper	Ideal Industries No. 45-171*	Strip insulation from wire
Hand Crimper	Aircraft Marine Products No. 47506*	Attach taper pins to wire
Hand Insertion Tool	Aircraft Marine Products No. 380306* with tip No. 394042*	Insert taper pins into connectors
Torque Wrench		Reassemble memory stacks
Module Extender**		
15 pin male module connector (1)	UNIVAC No. 911900	Part of Module Extender
15 pin female module connector (2)	UNIVAC No. 906155	Part of Module Extender
16 I/O Jumper Cables		

* Or equivalent

** See paragraph 5-2 and figure 5-1.

TABLE 5-1. TEST EQUIPMENT AND SPECIAL TOOLS (CONT.)

NOMENCLATURE		FUNCTION
NAME	DESIGNATION	
Wrapping Tool	14R2 (8130-132)	Make wire-wrap connections
Power Pack	503885 (8130-151)	Battery for wrapping tool
Unwrapping Tool		
Dual for 30 ga.	505084 (8130-137)	Unwraps left or right hand wrapped connections
Dual for 20-26 ga.	A31478 (8130-138)	
Bits for		
30 ga. square pin	504221	
30 ga. rect. pin	505561 (8130-144)	
24 or 26 ga.	26263 (8130-121)	Adapts wire wrapping tool to various wire sizes.
Sleeves for		
30 ga. square pin	505350	
30 ga. rect. pin	17611-2 (8130-129)	
24 or 26 ga.	18840 (8130-128)	

Specific instructions can be manually loaded and initiated. The results of the instruction can be checked, and the execution time can be determined with an oscilloscope. This type of testing can prove computer competence or assist in trouble-shooting timing problems that are not tested specifically by MROT. MROT testing consists of loading the routines and selecting the desired options as indicated by the directory typeout portions of MROT. The successful performance of a routine is indicated by a typeout; errors are also indicated by a typeout.

a. GENERAL. - The several MROT available basically consist of ECCLAT, the memory tests, the input/output tests, and others which do not fit into a general category.

These tests are designed to give the highest confidence rating to the computer. They are designed to be followed in any order; some, however, are to follow each other in order. Any individual test can be run to prove the computer competence.

Associated with MROT are error typeouts that occur when an error is detected by the test routine. The error typeout is a terse message indicating what portion of the computer is experiencing trouble. The error typeouts and console indications provide the major clues to isolating a malfunction. The exact trouble may be pin-pointed by proper interpretation of typeout and console indications, or it may be necessary to use an oscilloscope and/or voltmeter to pin-point the trouble.

The maintenance routines contain typeout subroutines that type out messages when an error is detected. The messages indicate what particular computer function is failing. For example:

This message would be typed out if an error occurred during the test that shifts AQ to the left 14 places. The next step would be to refer to the functional schematics and decide which circuits could cause this error. Further testing in the Op Step and/or Phase Step modes will isolate the trouble to a module that must be replaced. Rerunning the test that detected the error will verify that the trouble has been corrected. For example:

XPL TO DL

XXX XXX XXX XXX XXX (X = Binary Number)

XXX XXX XXX XXX XXX

This message indicates an error in the transmission of the complement of X lower (X'L) to D lower. The first 15-bit word is the word that was actually transmitted (error word), and the second 15-bit word is the word that was attempted to be transmitted (test pattern). If corresponding bits are not identical, an error occurred. For example:

XPL TO DL

111 000 111 000 011

111 000 111 000 111

This message indicates that bit 2^2 is being dropped during the transmission. A careful check of the circuits associated with this bit will reveal the fault.

The general procedure for troubleshooting takes the following form:

1) Obtain error indication during operation or preventive maintenance.

2) Load and run the appropriate MROT.

3) Error typeout by MROT.

4) Isolation to section and several possible circuit causes through interpretation of error typeout and console indications.

5) Isolation to a single circuit through interpretation of previous facts and by possible use of test equipment (oscilloscope and/or multimeter).

6) Replacement of faulty component.

7) Rerun the portion of MROT that detected the error (this will prove that the error has been corrected).

8) Resume operation.

If the trouble is isolated to a printed circuit module, it may be desirable to check the module on a module tester.

Use the test equipment and special tools (table 5-1) as indicated by the test procedures given in paragraph 5-3b.

b. MEMORY SECTION TROUBLESHOOTING. - In the memory section, as well as in the other sections of the computer, the troubleshooting procedures are presented primarily to enable personnel to isolate a malfunctioning component. Normal computer troubleshooting techniques are helpful but not necessarily the primary method of solving memory problems. The memories utilize current operated devices. The following paragraphs present several troubleshooting techniques and the associated memory waveforms which will aid in the isolation of memory problems.

NOTE

Do not attempt to adjust the memories until it has been determined whether or not the cause of a memory malfunction is due to a damaged component.

(1) MAIN MEMORY TROUBLESHOOTING.

(a) GENERAL. - If a memory chassis is failing, the trouble can usually be isolated to one of three sections (drive line, inhibit, or sense). If the read and write waveforms are correct, the trouble is probably in the sense or inhibit sections. The inhibit section can be checked by observing the inhibit waveforms for each bit while writing zeros. If these waveforms are correct, the one section remaining, the sense section, is probably at fault. Once a trouble is pin-pointed to a certain section, a block-to-block check of waveforms may be made to pin-point the trouble to a module or component. The following paragraphs present a short review of the functions of these sections.

1. DRIVE LINES. - The drive lines control the application of current that creates the magnetic field which switches the cores to one of two stable states. During the read portion of the memory cycle, all cores receiving coincident current are switched to a "0" unconditionally. During the write portion of the memory cycle, all cores receiving coincident current switch back from a "0" to a "1". An inhibit pulse occurring during this write portion prevents a core from switching to a "1". The drive line circuits can be split into two sections: the read/write transformer and the selector circuits. Read/write transformer translation takes place on each memory chassis and determines which of four X or four Y transformers is selected. The proper selector (one of 32X or 32Y) completes the drive line selection, that is, which X and Y lines are receiving the switching currents. Translation for the proper selector also takes place on each memory chassis.

2. INHIBIT LINES. - The inhibit lines prevent selected cores from being switched to a "1" during the write portion of the memory cycle, if a "0" was sensed during the read portion. Translation for the inhibit lines is accomplished on each memory chassis, and current is switched through the selected inhibit line if the Z register has a "0" for a given bit rather than a "1". Inhibit lines run parallel to either an X or a Y drive line, and the current is in the opposite direction to the drive line current. This effectively cancels half of the drive line current. Thus, coincident current is not obtained for the selected cores, and a "1" is not written.

3. SENSE LINES. - The sense lines thread through each core and detect core flux changes as an induced voltage. If this voltage is 10 millivolts or less, the sense amplifier ignores it. If the voltage is about 50 millivolts, the sense amplifier accepts it as a "1". Since a core requires 0.7 microseconds to switch, a "1" from a switched core occurs later in time than a "0", which occurs only when a core fails to switch. Because of this delay, a 0.2 to 0.3 microsecond strobe pulse is initiated approximately 0.5 microseconds after a read pulse is initiated. The data buffer register can accept inputs from the sense amplifiers only during the duration of the strobe pulse. In this way, "0" noise from the cores is isolated from the data buffer register. The data buffer register feeds the Z register which holds the data obtained from the memory reference. Figure 5-2 shows the timing relationships of the various memory pulses.

(b) PROCEDURES. - The following steps are presented to assist in the isolation of failing circuits in the memory section. Table 5-2 presents tabulated data concerning the circuitry which affects the bits at various addresses. Figure 5-3 illustrates typical waveforms which may be used as a guide to check actual waveforms. Several of the oscillograms presented are abnormal memory waveforms (see

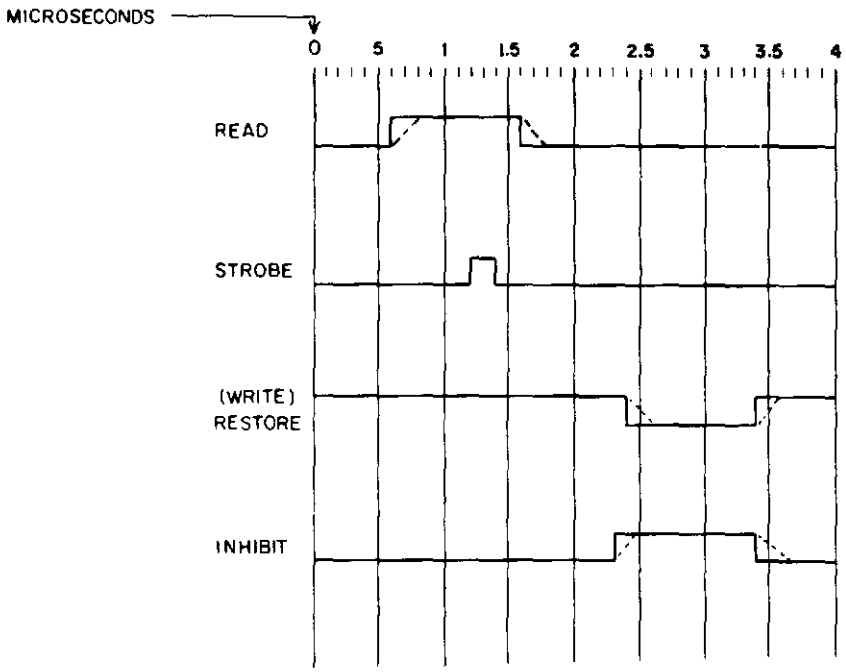


Figure 5-2. Memory Timing Cycle, Idealized Timing Waveform

figure 5-4). The test points used to obtain some of these will be inaccessible when the chassis is plugged in. If the memory chassis above is to be checked, the one to be checked is to be removed if it is possible to obtain access to these signals during actual operation. In this case, however, six of the memory bits will not be available for accessing due to the removed chassis. The following steps are quite basic but they should be checked thoroughly prior to making any adjustments or replacements.

STEP 1. Determine that the proper bits are being sent to the S register, and, in the case of write functions, check that the Z register contains the correct information to be written. Refer to figures 8-95 through 8-99, 8-103, and 8-104.

STEP 2. Determine that the translation is correct. Refer to paragraph 4-2e(2)(d) for an explanation of the translation circuits. Check the read-write drive lines to see if they are properly activated. See the adjustment procedure in paragraph 6-2b(1), if it appears that this is the problem. It is good practice to note the settings prior to any adjustment attempt, in the event that adjusting does not correct the malfunction.

STEP 3. Check the inhibit circuits to determine if this is creating the problem. The inhibit diverters may be either open or shorted; if this happens, a certain bit or block of addresses would contain all ones. Refer to figures 8-105 and 8-106 for inhibit translation and to the waveforms in figure 5-3.

STEP 4. Check the sense output and strobe timing on each chassis. Determine if the output itself is weak or if the timing is off. In either case, adjustments should be made according to paragraph 6-2b(1). Note the settings before attempting any adjustment. If the memory is dropping "1's", the problem may be that the read and write currents are too low. If it is picking up "1's", perhaps the read and write currents are too high, or the inhibit circuits are not functioning. Refer to figure 8-107 for the sense circuit logic. Figure 5-3 shows typical sense output waveforms. In the very remote case that the failure exists within the core plane itself, replace according to paragraph 6-3i.

(2) CONTROL AND BOOTSTRAP MEMORY TROUBLESHOOTING.

(a) GENERAL. - Troubleshooting the memories is so closely linked with the adjustments that the procedures for performing both are contained in paragraph 6-2b(2). However, a valuable program for troubleshooting these memories is the control memory test which is described in paragraph 5-3c(2)(b)1.

(b) LOCATION OF CONTROL MEMORY WORDS. - The control memory as explained in section 4 can store 64 30-bit words. Words 00 through 37 (octal) are stored on planes A4 and A6 (odd bits on A4, even bits on A6). Words 40 through 77 are stored on planes A3 and A5 (odd bits on A3, even bits on A5). Refer to figure 5-5.

c. TESTS

(1) ECCLAT. - The Executive Controlled Computer Logic Acceptance Test (ECCLAT) is an executive controlled program designed to check the logic of the computer. ECCLAT, under control of a main executive program, consists of the following test programs.

(a) J CONTROL TEST. - The function of this program checks the j designator evaluation. Separate test routines have been included for the testing of each j designator.

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
0	00000 - 07777	9A17	93Y00	9J13B	86Y00	9J01C
0	10000 - 17777	9A17	93Y10	9J10F	86Y10	9J02C
0	20000 - 27777	9A17	93Y30	9J25G	86Y20	9H30C
0	30000 - 37777	9A17	93Y20	9J21C	86Y30	9J04C
0	40000 - 47777	9A23	93Y40	9J16B	86Y40	9J05C
0	50000 - 57777	9A23	93Y50	9J13F	86Y50	9J06C
0	60000 - 67777	9A23	93Y70	9J28G	86Y60	9J07C
0	70000 - 77777	9A23	93Y60	9J34C	86Y70	9J08C
1	00000 - 07777	9A18	93Y01	9J13B	86Y01	9J01C
1	10000 - 17777	9A18	93Y11	9J10F	86Y11	9J02C
1	20000 - 27777	9A18	93Y31	9J25G	86Y21	9J03C
1	30000 - 37777	9A18	93Y21	9J31C	86Y31	9J04C
1	40000 - 47777	9A24	93Y41	9J16B	86Y41	9J05C
1	50000 - 57777	9A24	93Y51	9J13F	86Y51	9J06C
1	60000 - 67777	9A24	93Y71	9J28G	86Y61	9J07C
1	70000 - 77777	9A24	93Y61	9J34C	86Y71	9J08C
2	00000 - 07777	9A19	93Y02	9J14B	86Y02	9J01C
2	10000 - 17777	9A19	93Y12	9J11F	86Y12	9J02C
2	20000 - 27777	9A19	93Y32	9J26G	86Y22	9J03C
2	30000 - 37777	9A19	93Y22	9J32C	86Y32	9J04C
2	40000 - 47777	9A25	93Y42	9J17B	85Y42	9J05C
2	50000 - 57777	9A25	93Y52	9J14G	86Y52	9J06C
2	60000 - 67777	9A25	93Y72	9J29G	86Y62	9J07C
2	70000 - 77777	9A25	93Y62	9J35C	86Y72	9J08C
3	00000 - 07777	9A20	93Y03	9J14B	86Y03	9J09C
3	10000 - 17777	9A20	93Y13	9J11F	86Y13	9J10C
3	20000 - 27777	9A20	93Y33	9J26G	86Y23	9J11C
3	30000 - 37777	9A20	93Y23	9J32C	86Y33	9J12C
3	40000 - 47777	9A26	93Y43	9J17B	86Y43	9J13C
3	50000 - 57777	9A26	93Y53	9J14G	86Y53	9J10B
3	60000 - 67777	9A26	93Y73	9J29G	86Y63	9J11B
3	70000 - 77777	9A27	93Y63	9J35C	86Y73	9J12B

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS (CONT.)

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
4	00000 - 07777	9A21	93Y04	9J15B	86Y04	9J09C
4	10000 - 17777	9A21	93Y14	9J12F	86Y14	9J10C
4	20000 - 27777	9A21	93Y34	9J27G	86Y24	9J11C
4	30000 - 37777	9A21	93Y24	9J33C	86Y34	9J12C
4	40000 - 47777	9A27	93Y44	9J18B	86Y44	9J13C
4	50000 - 57777	9A27	93Y54	9J15G	86Y54	9J10B
4	60000 - 67777	9A27	93Y74	9J30G	86Y64	9J11B
4	70000 - 77777	9A27	93Y64	9J36C	86Y74	9J12B
5	00000 - 07777	9A22	93Y05	9J15B	86Y05	9J09C
5	10000 - 17777	9A22	93Y15	9J12F	86Y15	9J10C
5	20000 - 27777	9A22	93Y35	9J27G	86Y25	9J11C
5	30000 - 37777	9A22	93Y25	9J33C	86Y35	9J12C
5	40000 - 47777	9A28	93Y45	9J18B	86Y45	9J13C
5	50000 - 57777	9A28	93Y55	9J15G	86Y55	9J10B
5	60000 - 67777	9A28	93Y75	9J30G	86Y65	9J11B
5	70000 - 77777	9A28	93Y65	9J36C	86Y75	9J12B
6	00000 - 07777	10A17	93Y00	10J13B	86Y00	10J01C
6	10000 - 17777	10A17	93Y10	10J10F	86Y10	10J02C
6	20000 - 27777	10A17	93Y30	10J25G	86Y20	10J03C
6	30000 - 37777	10A17	93Y20	10J21C	86Y30	10J04C
6	40000 - 47777	10A23	93Y40	10J16B	86Y40	10J05C
6	50000 - 57777	10A23	93Y50	10J13F	86Y50	10J06C
6	60000 - 67777	10A23	93Y70	10J28G	86Y60	10J07C
6	70000 - 77777	10A23	93Y60	10J34C	86Y70	10J08C
7	00000 - 07777	10A18	93Y01	10JBB	86Y01	10J01C
7	10000 - 17777	10A18	93Y11	10J10F	86Y11	10J02C
7	20000 - 27777	10A18	93Y31	10J25G	86Y21	10J03C
7	30000 - 37777	10A18	93Y21	10J31C	86Y31	10J04C
7	40000 - 47777	10A24	93Y41	10J16B	86Y41	10J05C
7	50000 - 57777	10A24	93Y51	10JBF	86Y51	10J06C
7	60000 - 67777	10A24	93Y71	10J28G	86Y61	10J07C
7	70000 - 77777	10A24	93Y61	10J34C	86Y71	10J08C

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS (CONT.)

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
8	00000 - 07777	10A19	93Y02	10J14B	86Y02	10J01C
8	10000 - 17777	10A19	93Y12	10J11F	86Y12	10J02C
8	20000 - 27777	10A19	93Y32	10J26G	86Y22	10J03C
8	30000 - 37777	10A19	93Y22	10J32C	86Y32	10J04C
8	40000 - 47777	10A25	93Y42	10J17B	86Y42	10J05C
8	50000 - 57777	10A25	93Y52	10J14G	86Y52	10J06C
8	60000 - 67777	10A25	93Y72	10J29G	86Y62	10J07C
8	70000 - 77777	10A25	93Y62	10J35C	86Y72	10J08C
9	00000 - 07777	10A20	93Y03	10J14B	86Y03	10J09C
9	10000 - 17777	10A20	93Y13	10J11F	86Y13	10J10C
9	20000 - 27777	10A20	93Y33	10J26G	86Y23	10J11C
9	30000 - 37777	10A20	93Y23	10J32C	86Y33	10J12C
9	40000 - 47777	10A26	93Y43	10J17B	86Y43	10J13C
9	50000 - 57777	10A26	93Y53	10J14G	86Y53	10J10B
9	60000 - 67777	10A26	93Y73	10J29G	86Y63	10J11B
9	70000 - 77777	10A26	93Y63	10J35C	86Y73	10J12B
10	00000 - 07777	10A21	93Y04	10J15B	86Y04	10J09C
10	10000 - 17777	10A21	93Y14	10J12F	86Y14	10J10C
10	20000 - 27777	10A21	93Y34	10J27G	86Y24	10J11C
10	30000 - 37777	10A21	93Y24	10J33C	86Y34	10J12C
10	40000 - 47777	10A27	93Y44	10J18B	86Y44	10J13C
10	50000 - 57777	10A27	93Y54	10J15G	86Y54	10J10B
10	60000 - 67777	10A27	93Y74	10J30G	86Y64	10J11B
10	70000 - 77777	10A27	93Y64	10J36C	86Y74	10J12B
11	00000 - 07777	10A22	93Y05	10J15B	86Y05	10J09C
11	10000 - 17777	10A22	93Y15	10J12F	86Y15	10J10C
11	20000 - 27777	10A22	93Y35	10J27G	86Y25	10J11C
11	30000 - 37777	10A22	93Y25	10J33C	86Y35	10J12C
11	40000 - 47777	10A28	93Y45	10J18B	86Y45	10J13C
11	50000 - 57777	10A28	93Y55	10J15G	86Y55	10J10B
11	60000 - 67777	10A28	93Y75	10J30G	86Y65	10J11B
11	70000 - 77777	10A28	93Y65	10J36C	86Y75	10J12B

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS (CONT.)

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
12	00000 - 07777	11A17	93Y00	11J13B	86Y00	11J01C
12	10000 - 17777	11A17	93Y10	11J10F	86Y10	11J02C
12	20000 - 27777	11A17	93Y30	11J25G	86Y20	11J03C
12	30000 - 37777	11A17	93Y20	11J21C	86Y30	11J04C
12	40000 - 47777	11A23	93Y40	11J16B	86Y40	11J05C
12	50000 - 57777	11A23	93Y50	11J13F	86Y50	11J06C
12	60000 - 67777	11A23	93Y70	11J28G	86Y60	11J07C
12	70000 - 77777	11A23	93Y60	11J34C	86Y70	11J08C
13	00000 - 07777	11A18	93Y01	11J13B	86Y01	11J01C
13	10000 - 17777	11A18	93Y11	11J10F	86Y11	11J02C
13	20000 - 27777	11A18	93Y31	11J25G	86Y21	11J03C
13	30000 - 37777	11A18	93Y21	11J31C	86Y31	11J04C
13	40000 - 47777	11A24	93Y41	11J16B	86Y41	11J05C
13	50000 - 57777	11A24	93Y51	11J13F	86Y51	11J06C
13	60000 - 67777	11A24	93Y71	11J28G	86Y61	11J07C
13	70000 - 77777	11A24	93Y61	11J34C	86Y71	11J08C
14	00000 - 07777	11A19	93Y02	11J14B	86Y02	11J01C
14	10000 - 17777	11A19	93Y12	11J11F	86Y12	11J02C
14	20000 - 27777	11A19	93Y32	11J26G	86Y22	11J03C
14	30000 - 37777	11A19	93Y22	11J32C	86Y32	11J04C
14	40000 - 47777	11A25	93Y42	11J17B	86Y42	11J05C
14	50000 - 57777	11A25	93Y52	11J14G	86Y52	11J06C
14	60000 - 67777	11A25	93Y72	11J29G	86Y62	11J07C
14	70000 - 77777	11A25	93Y62	11J35C	86Y72	11J08C
15	00000 - 07777	11A20	93Y03	11J14B	86Y03	11J09C
15	10000 - 17777	11A20	93Y13	11J11F	86Y13	11J10C
15	20000 - 27777	11A20	93Y33	11J26G	86Y23	11J11C
15	30000 - 37777	11A20	93Y23	11J23C	86Y33	11J12C
15	40000 - 47777	11A26	93Y43	11J17B	86Y43	11J13C
15	50000 - 57777	11A26	93Y53	11J14G	86Y53	11J10B
15	60000 - 67777	11A26	93Y73	11J29G	86Y63	11J11B
15	70000 - 77777	11A27	93Y63	11J35C	86Y73	11J12B

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS (CONT.)

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
16	00000 - 07777	11A21	93Y04	11J15B	86Y04	11J09C
16	10000 - 17777	11A21	93Y14	11J12F	86Y14	11J10C
16	20000 - 27777	11A21	93Y34	11J27G	86Y24	11J11C
16	30000 - 37777	11A21	93Y24	11J33C	86Y34	11J12C
16	40000 - 47777	11A27	93Y44	11J18B	86Y44	11J13C
16	50000 - 57777	11A27	93Y54	11J15G	86Y54	11J10B
16	60000 - 67777	11A27	93Y74	11J30G	86Y64	11J11B
16	70000 - 77777	11A27	93Y64	11J36C	86Y74	11J12B
17	00000 - 07777	11A22	93Y05	11J15B	86Y05	11J09C
17	10000 - 17777	11A22	93Y15	11J12F	86Y15	11J10C
17	20000 - 27777	11A22	93Y35	11J27G	86Y25	11J11C
17	30000 - 37777	11A22	93Y25	11J33C	86Y35	11J12C
17	40000 - 47777	11A28	93Y45	11J18B	85Y45	11J13C
17	50000 - 57777	11A28	93Y55	11J15G	86Y55	11J10B
17	60000 - 67777	11A28	93Y75	11J30G	86Y65	11J11B
17	70000 - 77777	11A28	93Y65	11J36C	86Y75	11J12B
18	00000 - 07777	12A17	93Y00	12J13B	86Y00	12J01C
18	10000 - 17777	12A17	93Y10	12J10F	86Y10	12J02C
18	20000 - 27777	12A17	93Y30	12J25G	86Y20	12J03C
18	30000 - 37777	12A17	93Y20	12J21C	86Y30	12J04C
18	40000 - 47777	12A23	93Y40	12J16B	86Y40	12J05C
18	50000 - 57777	12A23	93Y50	12J13F	86Y50	12J06C
18	60000 - 67777	12A23	93Y70	12J28G	86Y60	12J07C
18	70000 - 77777	12A23	93Y60	12J34C	86Y70	12J08C
19	00000 - 07777	12A18	93Y01	12J13B	66Y01	12J01C
19	10000 - 17777	12A18	93Y11	12J10F	86Y11	12J02C
19	20000 - 27777	12A18	93Y31	12J25G	86Y21	12J03C
19	30000 - 37777	12A18	93Y21	12J31C	86Y31	12J04C
19	40000 - 47777	12A24	93Y41	12J16B	86Y41	12J05C
19	50000 - 57777	12A24	93Y51	12J13F	85Y51	12J06C
19	60000 - 67777	12A24	93Y71	12J28G	86Y61	12J07C
19	70000 - 77777	12A24	93Y61	12J34C	86Y71	12J08C

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS (CONT.)

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
20	00000 - 07777	12A19	93Y02	12J14B	86Y02	12J01C
20	10000 - 17777	12A19	93Y12	12J11F	86Y12	12J02C
20	20000 - 27777	12A19	93Y32	12J26G	86Y22	12J03C
20	30000 - 37777	12A19	93Y22	12J32C	86Y32	12J04C
20	40000 - 47777	12A25	93Y42	12J17B	86Y42	12J05C
20	50000 - 57777	12A25	93Y52	12J14G	86Y52	12J06C
20	60000 - 67777	12A25	93Y72	12J29G	86Y62	12J07C
20	70000 - 77777	12A25	93Y62	12J35C	86Y72	12J08C
21	00000 - 07777	12A20	93Y03	12J14B	86Y03	12J09C
21	10000 - 17777	12A20	93Y13	12J11F	86Y13	12J10C
21	20000 - 27777	12A20	93Y33	12J26G	86Y23	12J11C
21	30000 - 37777	12A10	93Y23	12J32C	86Y33	12J12C
21	40000 - 47777	12A26	93Y43	12J17B	86Y43	12J13C
21	50000 - 57777	12A26	93Y53	12J14G	86Y53	12J10B
21	60000 - 67777	12A26	93Y73	12J29G	86Y63	12J11B
21	70000 - 77777	12A26	93Y63	12J35C	86Y73	12J12B
22	00000 - 07777	12A21	93Y04	12J15B	86Y04	12J09C
22	10000 - 17777	12A21	93Y14	12J12F	86Y14	12J10C
22	20000 - 27777	12A21	93Y34	12J27G	86Y24	12J11C
22	30000 - 37777	12A21	93Y24	12J33C	86Y34	12J12C
22	40000 - 47777	12A27	93Y44	12J18B	86Y44	12J13C
22	50000 - 57777	12A27	93Y54	12J15G	86Y54	12J10B
22	60000 - 67777	12A27	93Y74	12J30G	86Y64	12J11B
22	70000 - 77777	12A27	93Y64	12J36C	86Y74	12J12B
23	00000 - 07777	12A22	93Y05	12J15B	86Y05	12J09C
23	10000 - 17777	12A22	93Y15	12J12F	86Y15	12J10C
23	20000 - 27777	12A22	93Y35	12J27G	86Y25	12J11C
23	30000 - 37777	12A22	93Y25	12J33C	86Y35	12J12C
23	40000 - 47777	12A28	93Y45	12J18B	86Y45	12J13C
23	50000 - 57777	12A28	93Y55	12J15G	86Y55	12J10B
23	60000 - 67777	12A28	93Y75	12J30G	86Y65	12J11B
23	70000 - 77777	12A28	93Y65	12J36C	86Y75	12J12B

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS (CONT.)

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
24	00000 - 07777	13A17	93Y00	13J13B	86Y00	13J01C
24	10000 - 17777	13A17	93Y10	13J10F	86Y10	13J02C
24	20000 - 27777	13A17	93Y30	13J25G	86Y20	13J03C
24	30000 - 37777	13A17	93Y20	13J21C	86Y30	13J04C
24	40000 - 47777	13A23	93Y40	13J16B	86Y40	13J05C
24	50000 - 57777	13A23	93Y50	13J13F	86Y50	13J06C
24	60000 - 67777	13A23	93Y70	13J28G	86Y60	13J07C
24	70000 - 77777	13A23	93Y60	13J34C	86Y70	13J08C
25	00000 - 07777	13A18	93Y01	13J13B	86Y01	13J01C
25	10000 - 17777	13A18	93Y11	13J10F	86Y11	13J02C
25	20000 - 27777	13A18	93Y31	13J25G	86Y21	13J03C
25	30000 - 37777	13A18	93Y21	13J31C	86Y31	13J04C
25	40000 - 47777	13A24	93Y41	13J16B	86Y41	13J05C
25	50000 - 57777	13A24	93Y51	13J13F	86Y51	13J06C
25	60000 - 67777	13A24	93Y71	13J28G	86Y61	13J07C
25	70000 - 77777	13A24	93Y61	13J34C	86Y71	13J08C
26	00000 - 07777	13A19	93Y02	13J14B	86Y02	13J01C
26	10000 - 17777	13A19	93Y12	13J11F	86J12	13J02C
26	20000 - 27777	13A19	93Y32	13J26G	86Y22	13J03C
26	30000 - 37777	13A19	93Y22	13J32C	86Y32	13J04C
26	40000 - 47777	13A25	93Y42	13J17B	86Y42	13J05C
26	50000 - 57777	13A25	93Y52	13J14G	86Y52	13J06C
26	60000 - 67777	13A25	93Y72	13J29G	86Y62	13J07C
26	70000 - 77777	13A25	93Y62	13J35C	86Y72	13J08C
27	00000 - 07777	13A20	93Y03	13J14B	86Y03	13J09C
27	10000 - 17777	13A20	93Y13	13J11F	86Y13	13J10C
27	20000 - 27777	13A20	93Y33	13J26G	86Y23	13J11C
27	30000 - 37777	13A20	93Y23	13J32C	86Y33	13J12C
27	40000 - 47777	13A26	93Y43	13J17B	86Y43	13J13C
27	50000 - 57777	13A26	93Y53	13J14G	86Y53	13J10B
27	60000 - 67777	13A26	93Y73	13J29G	86Y63	13J11B
27	70000 - 77777	13A26	93Y63	13J35C	86Y73	13J12B

TABLE 5-2. BIT ASSOCIATED CIRCUITS AND CIRCUIT LOCATIONS (CONT.)

BIT	ADDRESS	CORE PLANE	SENSE AMPLIFIER	LOCATION	INHIBIT	LOCATION
28	00000 - 07777	13A21	93Y04	13J15B	86Y04	13J09C
28	10000 - 17777	13A21	93Y14	13J12F	86Y14	13J10C
28	20000 - 27777	13A21	93Y34	13J27G	86Y24	13J11C
28	30000 - 37777	13A21	93Y24	13J33C	86Y34	13J17C
28	40000 - 47777	13A27	93Y44	13J18B	86Y44	13J13C
28	50000 - 57777	13A27	93Y54	13J15G	86Y54	13J10B
28	60000 - 67777	13A27	93Y74	13J30G	86Y64	13J11B
28	70000 - 77777	13A27	93Y64	13J36C	86Y74	13J12B
29	00000 - 07777	13A22	93Y05	13J15B	86Y05	13J09C
29	10000 - 17777	13A22	93Y15	13J12F	86Y15	13J10C
29	20000 - 27777	13A22	93Y35	13J27G	86Y25	13J11C
29	30000 - 37777	13A22	93Y25	13J33C	86Y35	13J12C
29	40000 - 47777	13A28	93Y45	13J18B	86Y45	13J13C
29	50000 - 57777	13A28	93Y55	13J15G	86Y55	13J10B
29	60000 - 67777	13A28	93Y75	13J30G	86Y65	13J11B
29	70000 - 77777	13A28	93Y65	13J36C	86Y75	13J12B

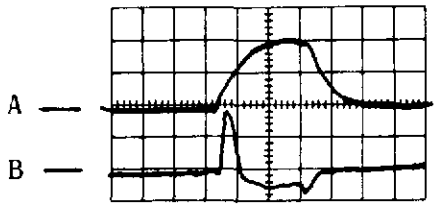
NOTE: In address block 00000 - 07777 addresses 100 - 177 and 540 - 577 are not used in core memory.

(b) K CONTROL TEST. - The function of this program is to test the transmission paths as they are called for by the different k translations. Separate test routines have been included for testing each of the three classes of instructions, the Read, Store and Replace instructions.

(c) COMMAND TEST. - The function of this program is to test the subcommand paths from main control used in the execution of each instruction. In general, the common paths consist of a function code translation, j evaluation, and k designator determination.

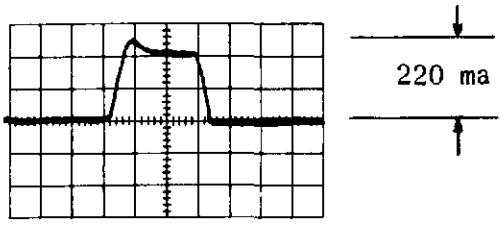
(d) CONTROL TEST. - This program checks the transmission lines associated with the R, B, ZØ, UL and B register, UL and control adder, the SØ and U register, the Z and S register, and the 71 instruction; and it evaluates the b designator in the instruction word.

(e) ARITHMETIC TEST. - The objective of this test is to check interregister transmission lines in the arithmetic section, the arithmetic subtractor, and other matrix operations.



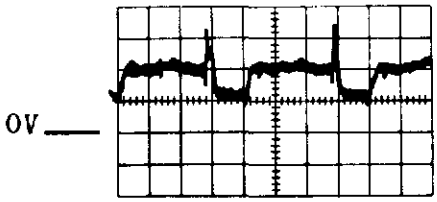
A. INHIBIT CURRENT

1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to .1 VOLTS/CM
   Channel B switch to 15 VOLTS/CM
   TIME/CM switch to .5 usec
   MODE switch to ALTERNATE
2. Connect a jumper between TB05F1 and F3.
3. Connect a P6016 current probe to Channel A input with a P6016 termination and attached to jumper in step 2. Do not ground.
4. Connect a voltage probe to channel B input and attach to TB05F1. Connect shield lead to ground.



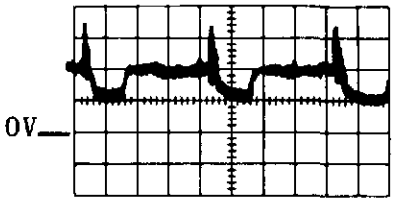
B. INHIBIT CURRENT

1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to .1 VOLTS/CM
   TIME/CM switch to 1 usec
2. Connect a P6016 current probe to Channel A input with a P6016 termination and attach to inhibit line, such as 86Y00 pin 1 which is inaccessible when the chassis is plugged in.



C. X READ DIVERTER OUTPUT

1. Oscilloscope settings using type CA Preamplifier.
   Channel B switch to 5 VOLTS/CM
   TIME/CM switch to 1 usec
2. Connect voltage probe to channel B input and attach to TB6M3.
3. Y diverter outputs are identical.

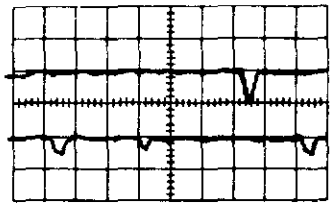


D. X WRITE DIVERTER OUTPUT

1. Oscilloscope settings using type CA Preamplifier.
   Channel B switch to 5 VOLTS/CM
   TIME/CM switch to 1 usec
2. Connect voltage probe to channel B input and attach to TB6M8.
3. Y diverter outputs are identical.

Strobe

Sense

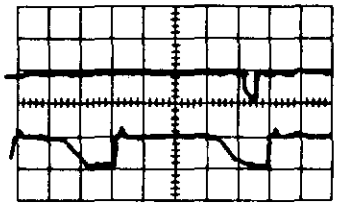


E. STROBE AND SENSE OUTPUT FOR A "0". CYCLING A SINGLE ADDRESS

1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to 5 VOLTS/CM
   Channel B switch to 5 VOLTS/CM
   TIME/CM switch to .5 usec/CM
   MODE switch to ALTERNATE
2. Memory margins on NORMAL.
3. Connect a voltage probe to channel A input and attach to strobe TB05E7 or E8.
4. Connect a voltage probe to channel B input and attach to sense amplifier TB08M1 through M6.

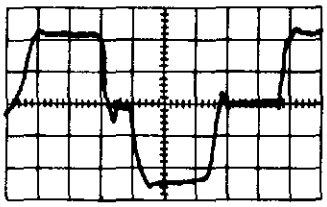
Strobe

Sense



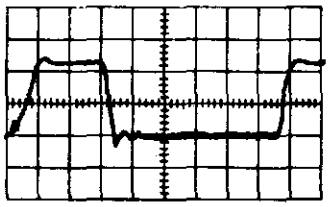
F. STROBE AND SENSE OUTPUT FOR A "1". CYCLING A SINGLE ADDRESS

1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to 5 VOLTS/CM
   Channel B switch to 5 VOLTS/CM
   TIME/CM switch to .5 usec/CM
   MODE switch to ALTERNATE
2. Memory margins on NORMAL.
3. Connect a voltage probe to channel A input and attach to strobe TB05E7 or E8.
4. Connect a voltage probe to channel B and attach to a sense amplifier TB08M1 through M6.



G. X READ-WRITE WAVEFORM

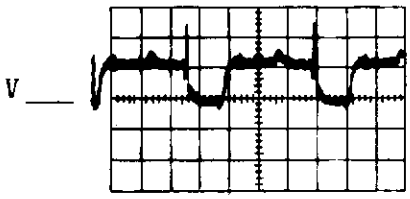
1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to .1 VOLTS/CM
   TIME/CM switch to .5 usec/CM
2. Connect P6016 current probe to Channel A input with a P6016 termination. Attach current probe to several X drive lines on end board.



H. X READ ONLY WAVEFORM

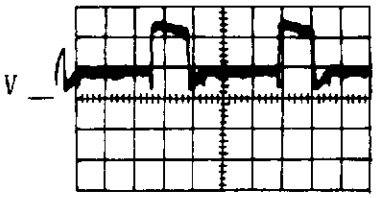
1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to .1 VOLTS/CM
   TIME/CM switch to .5 usec/CM
2. Connect P6016 current probe to a single X drive line on the end board.

Figure 5-3. Main Memory, Typical Waveforms (Cont.)



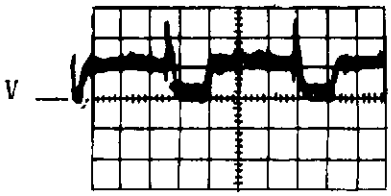
A. SHORTED X DRIVE LINE CYCLING SINGLE ADDRESS

1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to 5 VOLTS/CM
   TIME/CM switch to 1 usec/CM



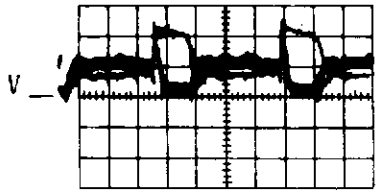
B. OPEN X DRIVE LINE CYCLING SINGLE ADDRESS

1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to 5 VOLTS/CM
   TIME/CM switch to 1 USEC/CM



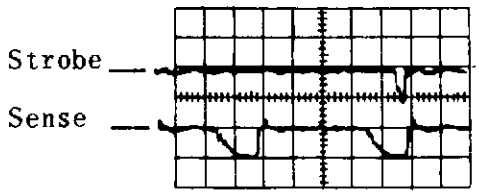
C. SHORTED X DRIVE LINE CYCLING ALL ADDRESSES

1. Oscilloscope settings using type CA Preamplifier
   Channel A switch to 5 VOLTS/CM
   TIME/CM switch to 1 usec/CM



D. OPEN X DRIVE LINE CYCLING ALL ADDRESSES

1. Oscilloscope settings using type CA Preamplifier
   Channel A switch to 5 VOLTS/CM
   TIME/CM switch to 1 usec/CM



E. BAD "1" OUTPUT

1. Oscilloscope settings using type CA Preamplifier.
   Channel A switch to 5 VOLTS/CM
   Channel B switch to 5 VOLTS/CM
   TIME/CM switch to .5 usec/CM

2. Memory margins to NORMAL.

3. Note the width of the output pulse and the fact that the strobe hits on the return swing which occurs too early.

Figure 5-4. Main Memory, Abnormal Waveforms

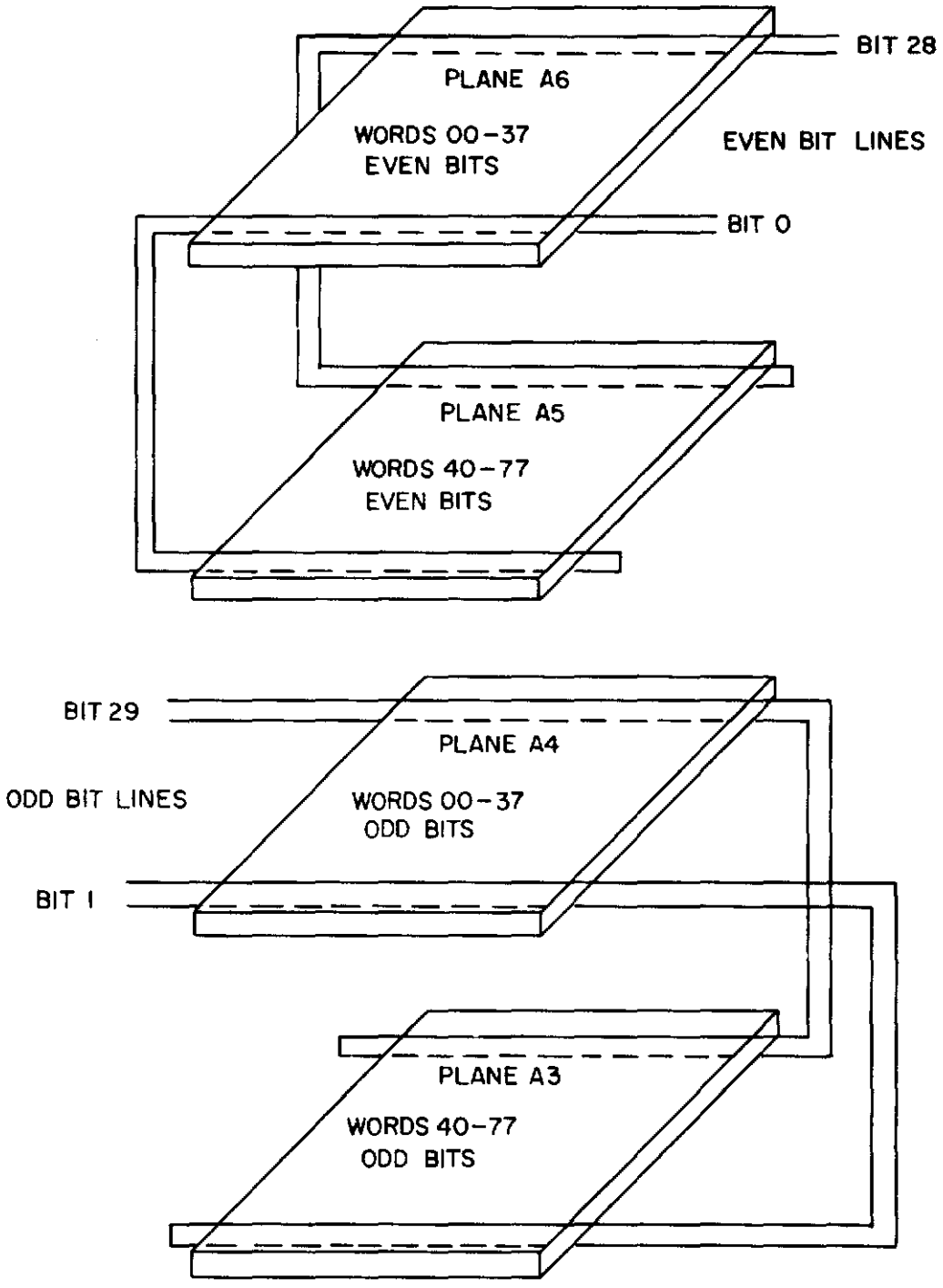


Figure 5-5. Control Memory Words, Diagram of Bit Locations

(f) INPUT/OUTPUT TEST. - The objective of this program is to exercise and test the input/output section of the computer. Separate routines are included to test the various functions in the input/output section such as data transmissions, buffer operation, buffer termination, and external and internally generated interrupts.

(2) MEMORY. - These tests verify that the individual addresses can be manually altered and that the memory is functioning and insensitive to internally generated noise from the worst patterns in the memory. They also verify the core read marginal checking feature and that the memory circuits are capable of operating under the highest possible repetition rate.

(a) MAGNETIC CORE MEMORY.

1. BRAINWASH. - The brainwash program tests the capability of the main memory section of the computer to accept and retain various bit configurations. Seven patterns are used in the test, the final pattern generating the maximum amount of noise in the magnetic core matrix sense winding. The test is diagnostic in that individually failing bits in the memory array are located exactly and associated with a specific test. When using the program, the memory is considered to be divided into two frames of 16,384 bits each. The frames are further divided into quadrants of 4,096 bits each. The program tests each quadrant as an individual memory unit. The division is justified by the fact that each sense winding encompasses a volume of 4,096 bits and each quadrant contains one inhibit line. Because of subdividing the memory when testing, it is possible to locate the program in any of the eight quadrants. The program starts in the second $4,000_8$ addresses of each quadrant of memory and is advanced $10,000_8$ addresses after each test sequence of a quadrant is completed. This permits operating the sense amplifiers in all combinations as well as allowing half pulses to be applied in varying combinations to the memory drive lines.

2. PROGRAM 55. - The 55 program determines the computer's ability to write any pattern of "1's" and "0's" into all core memory locations without using any of the memory addresses. It does not write into control memory. A unique feature of this program is that it can accomplish its duties at any cycle rate.

3. MEMORY CAPACITY TEST. - The memory capacity test checks core memory by causing the quantity stored at each address to be the address itself. Therefore, when read out of memory, the contents would be the same as the address.

4. MAGNETIC CORE CYCLING PROGRAM. - The cycle program permits the checking of a particular word or group of words and its associated circuitry. The program continually reads the same address so that the waveforms can be checked to isolate the malfunctioning circuit.

5. CORE READ MARGINAL CHECK. - The core read marginal check utilizes the brainwash program to check the memory under marginal conditions. By means of switches, the signals to the sense amplifiers are increased in width (low margin) or decreased in width (high margin). With an increase in width, less signal is clipped, and a greater possibility of noise being passed through the amplifier exists. With a decrease in width, more signal is being clipped, and less signal is available to the amplifier; therefore, greater sensitivity is required of the amplifier to pass the signal on.

6. REPETITION RATE TEST. - The repetition rate test establishes that the memory is capable of operating properly at a maximum repetition rate.

(b) CONTROL MEMORY.

1. CONTROL MEMORY TEST. - The control memory test program tests the capability of the control memory of the computer to accept and retain various bit configurations. It also checks the address location capabilities. Four patterns are used to test the memory to hold "1's", to hold "0's" and for crosstalk and complement crosstalk. During the address location test, the content of each address is set to its own address. The test is diagnostic in that failing bits are located and associated with a specific address. The failing address is displayed in Q with the failing bits in the A register. During this test all addresses in control memory are treated as 30-bit operands.

2. CYCLE TIME TEST. - The cycle time test checks the control memory cycle time by measuring the leading edge of a signal and the trailing edge of a signal to see that at 50 per cent amplitude the cycle time is less than 700 nanoseconds.

3. INSTRUCTION FAULT TEST. - The instruction fault test checks that an instruction cannot be read from the control memory.

(3) REAL-TIME CLOCK TEST. - The real-time clock test provides a recognizable indication of each 10-second period that the real-time clock is operating. For each 10-second period that has elapsed while the real-time clock is operative, the characters 10 SEC will be printed. If the real-time clock is inoperative for a 10-second period, the characters CLK INOP will be printed.

(4) INPUT/OUTPUT TEST. - The major I/O test is included in ECCLAT; however, this test exercises the I/O section further for a greater degree of confidence.

(5) INSTRUCTION EXECUTIVE TIME TESTS. - The instruction execution time test checks the ability of the computer to perform arithmetic functions in the prescribed time.

(6) MASTER CLOCK MARGIN TEST. - The master clock margin test checks the ability of the computer to perform any or all of the tests covered in the logic troubleshooting section, under marginal clock conditions. This is achieved by moving the delay modules of the clock and issuing clock pulses of about 120 nanosecond width (normally 150) and thus reducing the clock cycle time to about 540 nanoseconds (normally 680). Running the computer under clock margin will often reveal intermittent troubles or will indicate areas of weakness that could be future trouble-spots.

(7) CONSOLE CONTROL NONLOGIC TESTS. - The console control tests are a program controlled method of checking the switches and pushbutton indicators that control the computer. The various indicators associated with computer control are checked.

d. TEST PROCEDURES. - The test procedures explained in this paragraph consist of two basic operations. They are: first, the step-by-step setup which must be accomplished before specific programs begin, and, second, the step-by-step procedure to insure a valid run of the test programs. In all cases the MROT test setup must be made according to figure 5-6. Any deviations or additions to the setup are given at the beginning of each individual test. Unless otherwise stated the MROT test setup remains for all tests.

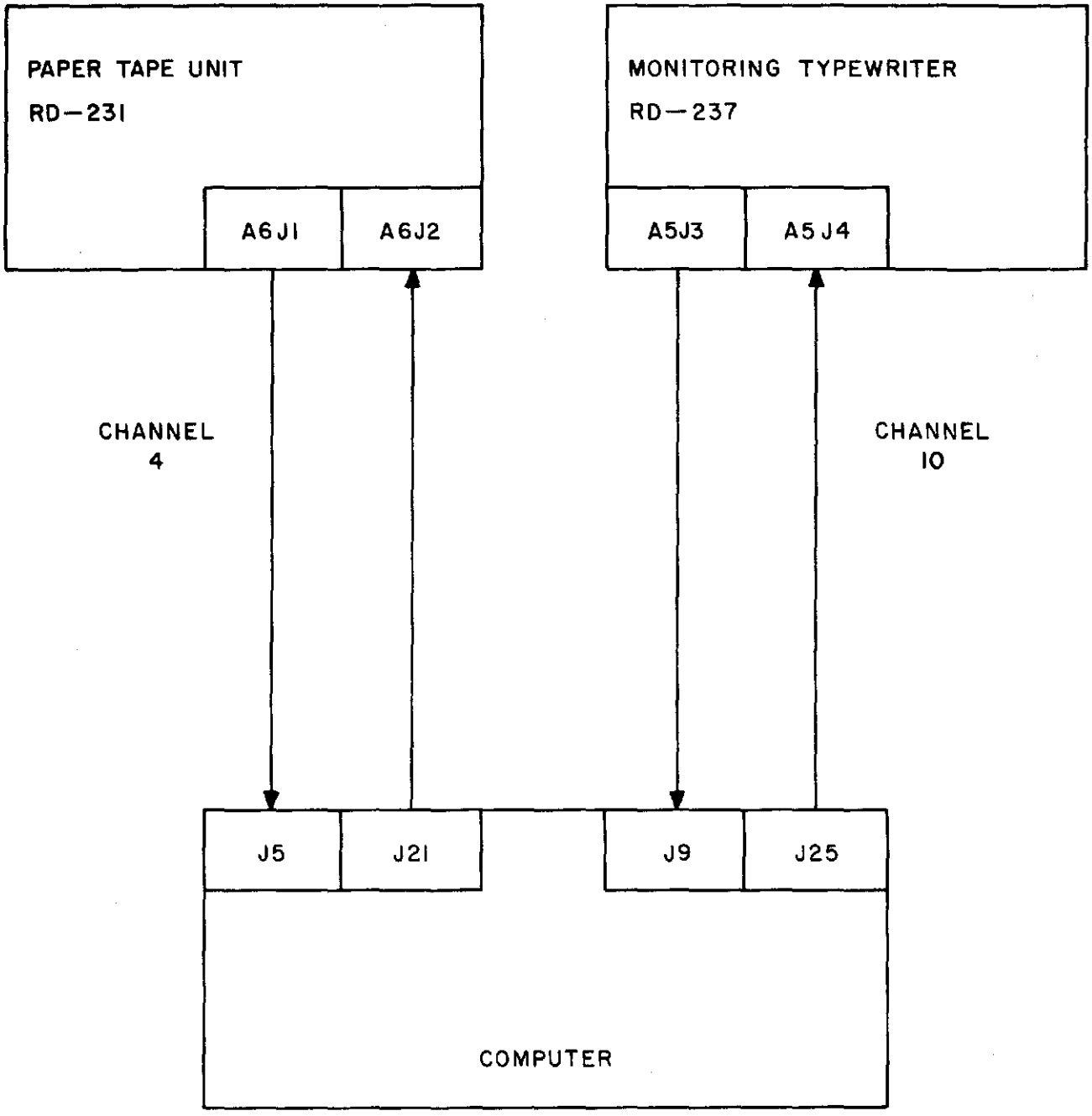


Figure 5-6. MROT Test Setup, Cabling Diagram

NOTE

During the step-by-step procedures, reference is made to "Master clear the computer". Whenever this is stated, it is implied that the computer is not running (stopped). For example, the computer cannot be master cleared under control of the phase step mode or when operating at high speed. Certain procedures require that just the MASTER CLEAR pushbutton be pressed. This does not necessarily master clear the computer.

(1) ECCLAT.

STEP 1. Position the CP-642B/USQ-20(V) Utility Package Load Routine on the paper tape reader.

STEP 2. Master clear the computer.

STEP 3. Press the LOAD MODE indicator-switch.

STEP 4. Press the PROGRAM II indicator-switch.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The utility package load routine enters memory.

STEP 6. Master clear the computer.

STEP 7. Position the ECCLAT program tape on the paper tape reader.

STEP 8. Set the P register to address 00001.

STEP 9. Operate the START-STEP/RESTART switch to the START-STEP position. The ECCLAT program enters the computer starting at address 04000.

STEP 10. Using the input/output jumper cables, jumper all output connectors to all input connectors with the exception of the channel used for the monitoring typewriter. Channels 0 and 1 output must be jumpered to channels 0 and 1 input respectively. All others may be intermixed.

STEP 11. Master clear the computer.

STEP 12. Set the P register to address 04000.

STEP 13. Operate the STOP 5 switch to the up position (refer to step 16).

STEP 14. Operate the START-STEP/RESTART switch to the START-STEP position. The monitoring typewriter types: ECCLAT.

STEP 15. The ECCLAT programs run continuously. To terminate the test, operate the STOP switch to the down position.

STEP 16. If an error occurs, operate the following switches to assist in defining the indications of the program result. Operate the appropriate switch to the up position to acquire the responses as follows:

JUMP 1 - The computer will not repeat the test which failed, but will go on to the next test after the error printout, if possible.

JUMP 2 - The computer repeats an individual test routine.

JUMP 3 - The computer will repeat a main program such as control test.

STOP 5 - The computer stops for visual inspection of registers before the printout in case an error has been detected.

STOP 7 - The computer stops after one execution of the ECCLAT test and is ready to re-execute the complete test.

STOP 4 - The computer will stop after the printout of an error.

STEP 17. Upon successful completion of the test, return the computer to the MROT setup as shown in figure 5-6.

(2) MEMORY TESTS.

(a) MAGNETIC CORE TESTING.

1. BRAINWASH.

STEP 1. Position the utility package load routine on the paper tape reader.

STEP 2. Master clear the computer.

STEP 3. Press the LOAD MODE indicator-switch.

STEP 4. Press the PROGRAM II indicator-switch.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The load routine enters memory.

STEP 6. Master clear the computer.

STEP 7. Position the brainwash program on the paper tape reader.

STEP 8. Set the P register to address 00001.

STEP 9. Operate the START-STEP/RESTART switch to the START-STEP position. The brainwash program enters the computer starting at 05400.

STEP 10. Master clear the computer.

STEP 11. Set the P register to address 05400.

STEP 12. Operate the STOP 5 switch to the up position (refer to step 15).

STEP 13. Operate the START-STEP/RESTART switch to the START-STEP position. The monitoring typewriter types: BRAINWASH. At the end of a complete program cycle through the computer memory the monitoring typewriter types out: END.

STEP 14. The brainwash program will continuously cycle repeating the typeouts (refer to step 13) until terminated. To terminate, operate the STOP 6 switch to the up position.

STEP 15. If an error occurs, operate the following switches to assist in defining the indications of the program results. Operate the appropriate switch to the up position to acquire the response as follows:

JUMP 1 - Eliminates all printouts.

JUMP 2 - Cycles a major subroutine.

JUMP 3 - Cycles the complete brainwash test in the same quadrant.

STOP 5 - Error stop before printout of errors.

STOP 6 - Stop upon entrance to a major subroutine.

STOP 7 - Stop following the move of program from one quadrant to another.

STOP 4 - Any time an error is found in the generator random number (GRN) tests, the computer stops at the beginning of this test. Operating the START-STEP/RESTART switch to START-STEP re-executes the test if an error was detected while moving the program from one quadrant to the next

2. PROGRAM 55

STEP 1. Disable control memory by grounding 5TB11H4.

CAUTION

Be absolutely sure that 5TB11H4 is grounded. Grounding any other pin may cause memory damage.

STEP 2. Master clear the computer.

STEP 3. Press the AF En indicator-switch.

STEP 4. Press the OP STEP MODE indicator-switch.

STEP 5. Set the U register equal to 70 100 77777.

STEP 6. Operate the START-STEP/RESTART switch to the START-STEP position.

STEP 7. Clear U (Do not master clear).

STEP 8. Set the U register equal to 14 030 00000.

STEP 9. Press the RUN MODE switch and operate the START-STEP/RESTART switch to the START-STEP position. When the computer stops, memory is clear.

STEP 10. Master clear.

STEP 11. Set the U register to 70 100 00007.

STEP 12. Press the OP STEP MODE switch and operate the START-STEP/RESTART switch switch to the START-STEP position.

STEP 13. Clear U (Do not master clear).

STEP 14. Set the U register equal to 55 030 00000.

STEP 15. Set the A register to all "1's".

STEP 16. Successive operations of the START-STEP/RESTART switch to START-STEP will store "1's" at consecutive addresses beginning at 00000. High speed operation can be obtained by pressing the RUN MODE switch prior to operating the START-STEP/RESTART switch to the START-STEP position. High speed operation results in "1's" being stored in all addresses. The contents of any address can be checked by using the manual read procedure [see paragraph 3-3e(1)].

STEP 17. Re-establish the repeat mode for the 55 instruction as directed by steps 11 through 15.

STEP 18. Successive operations of the START-STEP/RESTART switch to the START-STEP position will store "1's" and "0's" at alternate memory addresses (all "1's" at 00000, all "0's" at 00001, etc). High speed operation will result in "1's" and "0's", alternately, at all addresses.

STEP 19. Re-establish the repeat mode for the 55 instruction as directed by steps 11 through 15.

STEP 20. High speed operation at this time will result in the following pattern being stored: alternately all "1's" in two consecutive addresses and all "0's" in two consecutive addresses. Continued operation of a repeated 55 results in many different patterns being stored. Careful analysis of events is necessary to determine what data is stored in any address following a repeated 55.

The preceeding steps cause the program to stop when all addresses have been referenced. Continuous cycling can be obtained by operating the DISCONNECT B7 switch to the up position before initiating the repeated 55 instruction.

3. CHECKING MEMORY CAPACITY.

STEP 1. Master clear the computer and depress the Af En indicator pushbutton.

STEP 2. Store 614 00 00000 in address 00000. Refer to paragraph 3-3e(2) for manual store procedures.

STEP 3. Manually set U upper to 70200_8 (Repeat) and set U lower to 77777_8 (Repeat Count).

STEP 4. Press the OP STEP MODE indicator-switch.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. This causes the repeat instruction to set up the repeat mode.

STEP 6. Manually clear the U register.

STEP 7. Manually set U upper to 16730_8 (Store B7 in memory) and U lower to 77777_8 (starting store address). When the computer is started, the repeat mode will be active with r = 12. This causes UL (and therefore Y) to be decreased by one for each execution, and the quantity to be stored at each address to be the address itself.

STEP 8. Press the RUN MODE indicator switch.

STEP 9. Operate the START-STEP/RESTART switch to the START-STEP position. This stores 77777_8 in address 77777_8 and decreases the number and address by one for each execution. The computer enters the program fault condition at the termination of the repeat mode and the FAULT and STOP 4 indicators glow.

STEP 10. Using the manual read procedure [refer to paragraph 3-3e(1)] inspect any memory address. The contents should be the same as the address itself.

4. MEMORY CYCLING TEST.

STEP 1. Master clear the computer.

STEP 2. Press the Af En indicator-switch.

STEP 3. Press the OP STEP MODE indicator-switch.

STEP 4. Operate the DISCONNECT B7 switch to the up position.

STEP 5. Manually set U to 70 000 00001.

STEP 6. Operate the START-STEP/RESTART switch to the START-STEP position.

STEP 7. Manually clear the U register. Do not master clear.

STEP 8. Manually set U to 11 030 XXXXX. (XXXXX indicates the address to be cycled.)

STEP 9. Press the RUN MODE indicator-switch.

STEP 10. Operate the START-STEP/RESTART switch to the START-STEP position. The selected address is being referenced at the maximum rate.

5. CORE READ MARGINAL CHECK.

STEP 1. Run the brainwash program as specified in paragraph 5-3d(2)(a)1.

STEP 2. Using the oscilloscope, observe the width of the pulse signal to each of the six sense amplifiers on each of the memory chassis. The test points utilized are TB8M1 or TB8L1 on chassis A9 through A13. Sync the oscilloscope from 5TB18E8.

STEP 3. Operate the core read MARGINAL CHECK switches to the LOW position. Observe that the pulse signal to the amplifiers is increased in width. The MARGINAL CHECK indicator is lighted.

STEP 4. Operate the core read MARGINAL CHECK switches to the HIGH position. Observe that the pulse signal to the amplifier is decreased in width.

6. REPETITION RATE TEST.

STEP 1. Manually load an arbitrary pattern into a selected memory location [refer to paragraph 3-3e(1) for manual writing procedures].

STEP 2. Master clear the computer.

STEP 3. Press the OP STEP MODE and Af En indicator-switch.

STEP 4. Operate the DISCONNECT B7 switch to the up position.

STEP 5. Manually set the U register to 70 000 00000 and operate the START-STEP/RESTART switch to the START-STEP position.

STEP 6. Manually set the U register to Enter Q, 10 030 XXXXX. (XXXXX is the address selection.)

STEP 7. Press the RUN MODE indicator-switch.

STEP 8. Operate the START-STEP/RESTART switch to the START-STEP position. The computer will repeat the enter Q instruction from the selected address approximately every four microseconds, making the repetition rate of the memory reference 250,000 times per second.

STEP 9. Observe the signal at test point 5TB13C7 with the oscilloscope. Sync the oscilloscope from 5TB18E8.

STEP 10. Allow the computer to run for about 10 minutes to insure that information inserted into the memory location is unaltered. Press the OP STEP MODE indicator-switch to terminate the test.

(b) CONTROL MEMORY.

1. CONTROL MEMORY TEST.

STEP 1. Position the utility package load routine on the paper tape reader.

STEP 2. Master clear the computer.

STEP 3. Press the LOAD MODE indicator-switch.

STEP 4. Press the PROGRAM II indicator-switch.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The load routine enters memory.

STEP 6. Master clear the computer.

STEP 7. Position the control memory test tape (CMADRX) program on the paper tape reader.

STEP 8. Set the P register to address 00001.

STEP 9. Operate the START-STEP/RESTART switch to the START-STEP position. The control memory test program enters the computer starting at address 10000.

STEP 10. Master clear the computer.

STEP 11. Set the P register to address 10000.

STEP 12. Operate the DISCONNECT RTC switch to the up position. (This disables the real-time clock.)

STEP 13. Operate the STOP 5 switch to the up position (Refer to step 16).

STEP 14. Operate the START-STEP/RESTART switch to the START-STEP position. If an error occurs in the computer, a stop 5 occurs. The failing bits will appear in the

A register and the address appears in the Q register. To restart the program operate the START-STEP/RESTART switch to the START-STEP position.

STEP 15. The control memory test cycles continuously until stopped by the operator. To terminate the test, operate the STOP 7 switch to the up position.

STEP 16. If an error occurs, use the following switches to assist in the definition of the malfunction. Operate the appropriate switch to the up position to acquire the responses as follows:

JUMP 1 - Cycles selected major subtest.

NOTE

JUMP 1 should not be selected until the STOP 6 has occurred for the major subtest to be repeated.

JUMP 5 - Error Stop with address displayed in Q and failing bits in A.

STOP 6 - Stop on completion of major subtest.

STOP 7 - Stop at end of completed test.

2. CYCLE TIME TEST.

STEP 1. Master clear the computer.

STEP 2. Set the Q register to 11 030 00100 and press the Af En indicator-switch.

STEP 3. Press the OP STEP MODE indicator-switch.

STEP 4. Set the U register to 14 030 00000 and operate the START-STEP/RESTART switch to the START-STEP position. This stores the instruction in the Q register at address 00000.

STEP 5. Operate the DISCONNECT ADV P switch to the up position.

STEP 6. Master clear the computer.

STEP 7. Operate the START-STEP/RESTART switch to the START position.

STEP 8. Observe test points 8TB11A1 and 8TB11B7 using the oscilloscope. Sync the oscilloscope from 6TB10C1. The control memory cycle time is measured from the leading edge of the signal at 8TB11A1 to the trailing edge of the signal at 8TB11B7. Measured at 50 percent amplitude points, the cycle time should be less than 700 nanoseconds.

3. INSTRUCTION FAULT.

STEP 1. Manually store at address 00100 an 11 030 00100 instruction [refer to paragraph 3-3e(1) for manual writing procedures].

STEP 2. Master clear the computer.

STEP 3. Press the OP STEP MODE indicator-switch.

STEP 4. Set the P register to address 00100 and operate the START-STEP/RESTART switch to the START-STEP position twice. The FAULT indicator will glow, and the U register contains 00 000 XXXXX, indicating that an instruction cannot be read from control memory.

(3) REAL-TIME CLOCK TESTS.

(a) REAL-TIME CLOCK PROGRAMS.

STEP 1. Position the utility package load routine on the paper tape reader.

STEP 2. Master clear the computer.

STEP 3. Press the LOAD MODE and PROGRAM II indicator-switches.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. The load routine enters memory.

STEP 5. Master clear the computer.

STEP 6. Position the real-time clock program on the paper tape reader.

STEP 7. Set the P register to address 00001.

STEP 8. Operate the START-STEP/RESTART switch to the START-STEP position. The RTC program enters the computer starting at address 10000.

STEP 9. Master clear the computer.

STEP 10. Set the P register to address 10000.

STEP 11. Select STOP 7 if it is desirable to stop after the printout of 10 seconds.

STEP 12. Operate the START-STEP/RESTART switch to the START-STEP position. For each 10-second period that the clock is operative, the printout, 10 SEC., occurs on the monitoring typewriter (once only if step 11 is initiated).

STEP 13. Operate the DISCONNECT RTC switch to the up position. For each 10-second period that the clock is inoperative, the printout, CLK INOP, occurs on the monitoring typewriter.

STEP 14. Repeat the operation of the DISCONNECT RTC switch to the up and down position (enable and disable clock) several times and observe the printouts.

(b) INTERNAL ACCURACY CHECK. - Use the oscilloscope to check the output of the RTC interrupt flip-flop (test point 5TB15E5). Since the RTC oscillator frequency is 1024 cps, the period of the waveform should be about 0.9765 milliseconds.

(4) INPUT/OUTPUT EXERCISE.

STEP 1. Using the jumper cables, jumper all output channel connectors to all input connectors with the exception of 4 and 10 which are connected to the monitoring typewriter and the paper tape reader. Channels 0 and 1 must be jumpered to channels 0 and 1 respectively. All others can be intermixed.

STEP 2. Position the utility package load routine on the paper tape reader.

STEP 3. Master clear the computer.

STEP 4. Press the LOAD MODE and PROGRAM I indicator-switches.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The load routine program enters memory.

STEP 6. Master clear the computer.

STEP 7. Position the input/output test program on the paper tape reader.

STEP 8. Set the P register to address 00001.

STEP 9. Operate the START-STEP/RESTART switch to the START-STEP position. The input/output programs enter the computer starting at 05000.

STEP 10. Master clear the computer.

STEP 11. Set the P register to address 05000 for single channel operation or to address 05023 for multiple channel operation.

STEP 12. Operate the START-STEP/RESTART switch to the START-STEP position. The program cycles testing each channel in sequence.

STEP 13. If an error occurs, use the following switches to assist in the definition of the program indications. Operate the appropriate switch to the up position to acquire the responses as follows:

JUMP 1 - Advance to next test after an error.

JUMP 2 - Repeats major subtest.

STOP 5 - Stop before error printout.

STOP 6 - Store before performing each major subtest.

STOP 7 - Stop at completion of test.

STOP 4 - Stop after error printout.

STEP 14. To terminate the test, operate the STOP switch to the down position.

(5) INSTRUCTION EXECUTION TIME TEST.

(a) ADD.

STEP 1. Master clear the computer.

STEP 2. Load the Q register with the instruction, 20 000 00000.

STEP 3. Press the OP STEP MODE and the Af En indicator switches.

STEP 4. Set 14 030 00000 into the U register.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The instruction in Q is now located in memory address 00000.

STEP 6. Operate the DISCONNECT ADV P switch to the up position.

STEP 7. Master clear the computer.

STEP 8. Operate the START-STEP/RESTART switch to the START-STEP position. The computer continuously repeats an add instruction.

STEP 9. Observe time 31T11 at test point 6TB10C3 with the oscilloscope. The time from leading edge to leading edge of the waveshape is eight microseconds plus or minus five percent.

(b) SUBTRACT.

STEP 1. Repeat steps 1 through 9 of paragraph 5-3d(5)(a) except set the Q register with the instruction 21 000 00000 during step 2.

STEP 2. The observed execution time is eight microseconds plus or minus five percent.

(c) MULTIPLY.

STEP 1. Repeat steps 1 through 9 of paragraph 5-3d(5)(a) except set the Q register with the instruction 22 000 00001.

STEP 2. The observed execution time is 32 microseconds plug or minus five percent The completion of this step terminates the short execution time.

STEP 3. Press the OP STEP MODE and Af En indicator-switches.

STEP 4. Set the Q register to 37 777 77777.

STEP 5. Press the RUN MODE indicator-switch.

STEP 6. Operate the START-STEP/RESTART switch to the START-STEP position. The execution time is 52 microseconds plus or minus five percent. The completion of this step terminates the long execution time.

(d) DIVIDE.

STEP 1. Repeat Steps 1 through 9 of paragraph 5-3d(5)(a) except step 2. For Step 2 set the Q register with the instruction 23 000 00001.

STEP 2. The observed time is 52 microseconds plus or minus five percent.

(6) MASTER CLOCK MARGIN TEST.

STEP 1. Move the delay modules according to table 5-3.

STEP 2. Perform any of the tests in this section under the margin conditions.

STEP 3. Replace all delay modules to their original location as soon as the test or tests are completed (refer to table 5-3).

TABLE 5-3. MASTER CLOCK DELAY MODULE FAST/NORMAL LOCATIONS

TERM	ORIGINAL (FROM)	NEW (TO)
72Y01	5J38F	5J39F
72Y02	5J40F	5J41F
72Y03	5J38E	5J38E
72Y04	5J40E	5J41E

(7) CONSOLE CONTROL NONLOGIC TESTS. - The MODE switches, START-STEP/RESTART switch, STOP switch, RESTART SPEED CONTROL, PHASE INDICATOR switches, and all JUMP/STOP switches and indicators are checked with the use of the program tape as follows:

(a) LOAD MODE INDICATOR-SWITCH, PROGRAM I/II SWITCHES

STEP 1. Master clear the computer.

STEP 2. Position the console test program tape on the paper tape reader.

STEP 3. Press the LOAD MODE and PROGRAM II indicator switches.

STEP 4. Operate the STOP 7 switch to the up position.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The tape is read into the computer via the Bootstrap Program II.

STEP 1. Master clear the computer.

STEP 2. Set the P register to 10000 and operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 3. Release the STOP 7 switch.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. The computer cycles waiting for the normal operation of the jump switches.

STEP 5. Operate the STOP 5 switch to the up position.

STEP 6. Operate the JUMP 1 switch to the up position. A STOP 5 occurs.

STEP 7. Release the STOP 5 switch (down position).

STEP 8. Perform steps 1 through 8 the desired number of times.

STEP 9. Release JUMP 1 switch (down position).

STEP 10. Operate the START-STEP/RESTART switch to the START-STEP position. The computer cycles.

STEP 11. Operate the STOP 6 switch to the up position.

STEP 12. Operate the JUMP 2 switch to the up position. A STOP 6 occurs.

STEP 13. Release the STOP 6 switch (down position).

STEP 14. Perform steps 9 through 13 the desired number of times.

STEP 15. Operate the START-STEP/RESTART switch to the START-STEP position. The computer cycles.

STEP 16. Operate the STOP 7 switch to the up position.

STEP 17. Operate the JUMP 3 switch to the up position. A STOP 7 occurs.

STEP 18. Release the STOP 7 switch (down position).

STEP 19. Perform steps 14 through 18 the desired number of times.

STEP 20. Operate the JUMP 1 and 3 switches to the up position. The program exits to executive and a STOP 4 occurs.

STEP 21. Release all JUMP switches (down position).

(c) DISCONNECT B7 SWITCH.

NOTE

Omit steps 1 and 2 if tests are run in consecutive order.

STEP 1. Master clear the computer.

STEP 2. Set the P register to address 10002 and operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 3. Operate the START-STEP/RESTART switch to the START-STEP position.

STEP 4. Observe B7 being displayed in the A register. The number is being counted down.

STEP 5. Operate the DISCONNECT B7 switch to the up position. The A register stops counting down.

STEP 6. Release the DISCONNECT B7 switch (down position). The A register resumes counting.

STEP 7. Operate the JUMP 1 switch to the up position. A STOP 4 occurs.

STEP 8. Release the JUMP 1 switch (down position).

(d) REAL-TIME CLOCK DISCONNECT SWITCH.

NOTE

Omit steps 1 and 2 if tests are run in consecutive order.

STEP 1. Master clear the computer.

STEP 2. Set the P register to address 10003 and operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 3. Operate the START-STEP/RESTART switch to the START-STEP position.

STEP 4. Observe the real-time clock being displayed in the A register.

STEP 5. Operate the DISCONNECT RTC switch alternately to up and down positions (selected and not selected respectively) and observe the A register counting and not counting as the switch is operated (up on counting, and down on not counting).

STEP 6. Operate the JUMP 1 switch to the up position. This allows an exit and a STOP 4 occurs.

STEP 7. Release the JUMP 1 switch (down position).

(e) C REGISTER SWITCHES.

NOTE

Omit steps 1 and 2 if tests are run in consecutive order.

STEP 1. Make sure the I/O jumper cables are not connected on channels 2, 5, 11, and 15. Operate the DISCONNECT RTC switch to the up position.

STEP 2. Master clear the computer.

STEP 3. Set the P register to address 10004 and operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 5. Observe the C register indicators. All bit position indicator switches indicate "0's".

STEP 6. Operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 7. Observe the C register indicators. All bit position indicator switches indicate "1's".

STEP 8. Operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 9. Observe the C register indicators. All bit position indicator switches indicate "0's".

STEP 10. Operate the START-STEP/RESTART switch to the START-STEP position. The program exits and a STOP 4 occurs.

(f) START-STEP/RESTART, RESTART SPEED CONTROL, AND OP STEP MODE SWITCHES AND INDICATOR-SWITCHES.

STEP 1. Master clear the computer.

STEP 2. Press the OP STEP MODE indicator-switch.

STEP 3. Set the P register to address 10000.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. For each action of the START-STEP/RESTART switch, one instruction is executed.

STEP 5. Operate the START-STEP/RESTART switch to the RESTART position. The execution of instructions is controlled by the RESTART SPEED CONTROL switch via the low-speed oscillator.

STEP 6. Rotate the RESTART SPEED CONTROL switch. The execution of instructions varies between 2 and 200 cps depending on the positioning of the switch.

STEP 7. Operate the START-STEP/RESTART switch to the neutral position. The execution of instructions stops.

(g) PHASE STEP MODE INDICATOR-SWITCH, PHASE REPEAT SWITCH, AND PHASE INDICATOR-SWITCHES.

STEP 1. Master clear the computer.

STEP 2. Press the PHASE STEP MODE indicator-switch.

STEP 3. Set the P register to address 10000.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. Consecutive phase pulses (1, 2, 3, and 4) are emitted each time the START-STEP/RESTART switch is operated and the CLOCK PHASE indicators advance one stage, depicting the next phase pulse to be issued.

STEP 5. Operate the START-STEP/RESTART switch to the RESTART position. Consecutive phase pulses are emitted, controlled by the RESTART SPEED CONTROL switch via the low-speed oscillator. The CLOCK PHASE indicators advance one for each phase pulse and depict the next pulse to be issued.

STEP 6. Operate the START-STEP/RESTART switch to the neutral position.

STEP 7. Press the CLOCK PHASE indicator-switch to be repeated and hold.

STEP 8. Operate the PHASE REPEAT switch to the up position. Release the CLOCK PHASE indicator. The selected clock phase is emitted at the normal pulse rate.

STEP 9. Any phase can be selected by repeating step 7.

STEP 10. Operate the PHASE REPEAT switch to the neutral position.

(h) RUN MODE AND RUN INDICATOR-SWITCHES.

STEP 1. Master clear the computer.

STEP 2. Depress the RUN MODE indicator-switch.

STEP 3. Set the P register to address 10000.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The test program runs and the RUN indicator-switch is lighted.

STEP 6. Depress the MASTER CLEAR switch. The program continues to run uninterrupted.

STEP 7. Operate the STOP switch to the down position. The RUN indicator is extinguished.

STEP 8. Manually load, at address 10000, a jump instruction to the beginning program address (61 000 10000) [refer to paragraph 3-3e(1) for manual writing procedure].

STEP 9. Master clear the computer.

STEP 10. Press the Af En indicator-switch.

STEP 11. Operate the AUTOMATIC RECOVERY switch to the center position.

STEP 12. Operate the START-STEP/RESTART switch to the START-STEP position. A fault routine is initiated to address 00000, and the FAULT indicator is lighted. A STOP 4 occurs.

STEP 13. Press the MASTER CLEAR switch. The FAULT indicator is extinguished.

(i) AUTOMATIC RECOVERY TEST.

1. AUTOMATIC RECOVERY SWITCH - UP POSITION.

STEP 1. Master clear the computer.

STEP 2. Set P register to address 10005.

STEP 3. Operate the START-STEP/RESTART switch to the START-STEP position. A STOP 4 occurs.

STEP 4. Position the program tape in the paper tape reader.

STEP 5. Operate the STOP 7 switch to the up position.

STEP 6. Operate the PROGRAM I/II switch to the PROGRAM I position. This switch is located on program control module J35A of chassis A5.

STEP 7. Operate the AUTOMATIC RECOVERY switch to the up position.

STEP 8. Operate the START-STEP/RESTART switch to the START-STEP position. This causes the clearing of the program area. A fault occurs and the FAULT indicator is lighted. This program is read into the computer. A STOP 7 occurs. If verification of program reload is required, any portion of the console test can be redone.

STEP 9. Repeat steps 2 through 8 except operate the PROGRAM I/II switch to the PROGRAM II position (refer to step 6).

STEP 10. Operate the AUTOMATIC RECOVERY switch to the center position.

2. AUTOMATIC RECOVERY SWITCH-CENTER POSITION.

STEP 1. Repeat steps 8 through 10 of preceding paragraph 5-3d(7)(i)1.

STEP 2. Operate the AUTOMATIC RECOVERY switch to the center position.

STEP 3. Operate the START-STEP/RESTART switch to the START-STEP position. A fault sequence is initiated and the preceding instructions loaded by step 1 are executed. The FAULT indicator is lighted and a STOP 4 occurs.

5-4. NONLOGIC TROUBLESHOOTING.

The nonlogic troubleshooting is divided into two groups: power supplies and console.

a. POWER SUPPLIES. - The power required by the computer is divided into four groups: unregulated input power, the regulated input power, main power supply, and the console power supply.

(1) UNREGULATED INPUT POWER. - The unregulated input power requirements are:

FREQUENCY	400 (±5%) cps
VOLTAGE	115 (±10%) VAC (line-to-line)
PHASES	3
POWER	2000 watts

The unregulated power distribution is shown on figure 5-7. Use the AC voltmeter to verify unregulated power application to all necessary circuits (refer also to figures 8-176 and 8-177).

(2) REGULATED INPUT POWER. - The regulated input power is furnished by the PU-655/U motor generator. The regulated input power requirements are:

FREQUENCY	400 (±5%) cps
VOLTAGE	115 (±1%) VAC (line-to-line)
PHASES	3
POWER	2500 watts

The regulated power distribution is shown on figure 5-8. Use the AC voltmeter to verify regulated power application to all necessary circuits (refer also to figures 8-176 and 8-177).

(3) MAIN POWER SUPPLY. - The main power supply provides the DC voltages used by the computer logic and memory circuits (see figure 8-177). The characteristics of the main power supply are listed in table 5-4. Use the DC voltmeter and check the voltages on each chassis. Use the oscilloscope or AC voltmeter to check the ripple voltage for each supply. The difference between the absolute values of the 15-volt supplies should not be greater than 6% of the smaller value.

TABLE 5-4. MAIN POWER SUPPLY CHARACTERISTICS

OUTPUT VOLTS (DC)	TOLERANCE (VOLTS)	RIPPLE (Max P to P)	TEST POINT (EACH CHASSIS)	ADDITIONAL INSTRUCTIONS
-15	-13.5 to -16.5	0.20	J19-M8 to GRD	Measure on any one of chassis A1 through A8
+15	+13.5 to +16.5	0.20	J19-L8 to GRD	Measure on any one of chassis A1 through A8
-4.5	-4.0 to -5.0	0.20	J19-N8 to GRD	Measure on any one of chassis A1 through A8
-15	-13.5 to -16.5	0.20	J8-M8 to GRD	Measure on any one of chassis A9 through A13
+18	+16.2 to +19.8	0.10	J8-L8 to GRD	Measure on any one of chassis A9 through A13
-4.5	-4.0 to -5.0	0.20	J8-N8 to GRD	Measure on any one of chassis A9 through A13
+10*	+9.0 to +11.0 (Adjustable)	0.10	J8-K8 to GRD	Measure on any one of chassis A9 through A13

* Output from voltage regulator located at J37E on each memory chassis (A9 thru A13).

(4) CONSOLE POWER SUPPLY. - The console power supplies produce the voltages for the indicators, switches, and relays on the console. The characteristics of the console power supply are listed in table 5-5. Use the multimeter to measure the output of each supply.

b. CONSOLE CONTROL AND INDICATORS. - The console controls and indicators are tested by operating the controls and observing the results. The following paragraphs are step-by-step procedures for testing all the console controls and indicators.

(1) BLOWER POWER AND COMPUTER POWER.

STEP 1. Operate the BLOWER POWER switch to the ON position. The BLOWER POWER indicator is lighted and the blower is circulating the air inside the computer.

STEP 2. Operate the COMPUTER POWER switch to the ON position. The COMPUTER POWER indicator is lighted. The computer is now energized and the COMPUTER ON TIME meter is registering elapsed time.

STEP 3. Operate the BLOWER POWER switch to the OFF position. Blower power and computer power are both removed, and the indicators are extinguished.

(2) OVERTEMP WARNING.

STEP 1. Remove computer and blower power.

STEP 2. Remove plug P99 from jack J57 and connect pins F and G on P99 together with a jumper wire. This simulates the closing of the overtemperature warning sensor at +46°C (+115°F).

STEP 3. Apply blower power long enough to verify that the OVERTEMP WARNING indicator is lighted and the 400 cycle alarm horn is active.

STEP 4. Press the OVERTEMP WARNING indicator-switch. The 400 cycle alarm horn is silenced, but the OVERTEMP WARNING indicator remains lighted.

TABLE 5-5. CONSOLE POWER SUPPLY CHARACTERISTICS

Output Volts (DC)	Tolerance (Volts)	Test Points	Ripple Volts (Max. P. to P.)
-90.5*	-80 to -100 (peak)	TB1, TB3	---
-54	-48 to -60	TB2, TB3	0.5
-26.5	-23.8 to -29.2	C1-2, TB3	2.5
-15	-13.5 to -16.5	TB4-A7, TB3	2.5

* One-half wave, rectified voltage

STEP 5. Remove blower power from computer.

STEP 6. Remove the jumper wire attached in step 2.

STEP 7. Remove plug P99 from J57. Connect pins D and E on P99 together with a jumper wire.

STEP 8. Operate the BLOWER POWER and COMPUTER POWER switches to the ON position. The indicators are lighted.

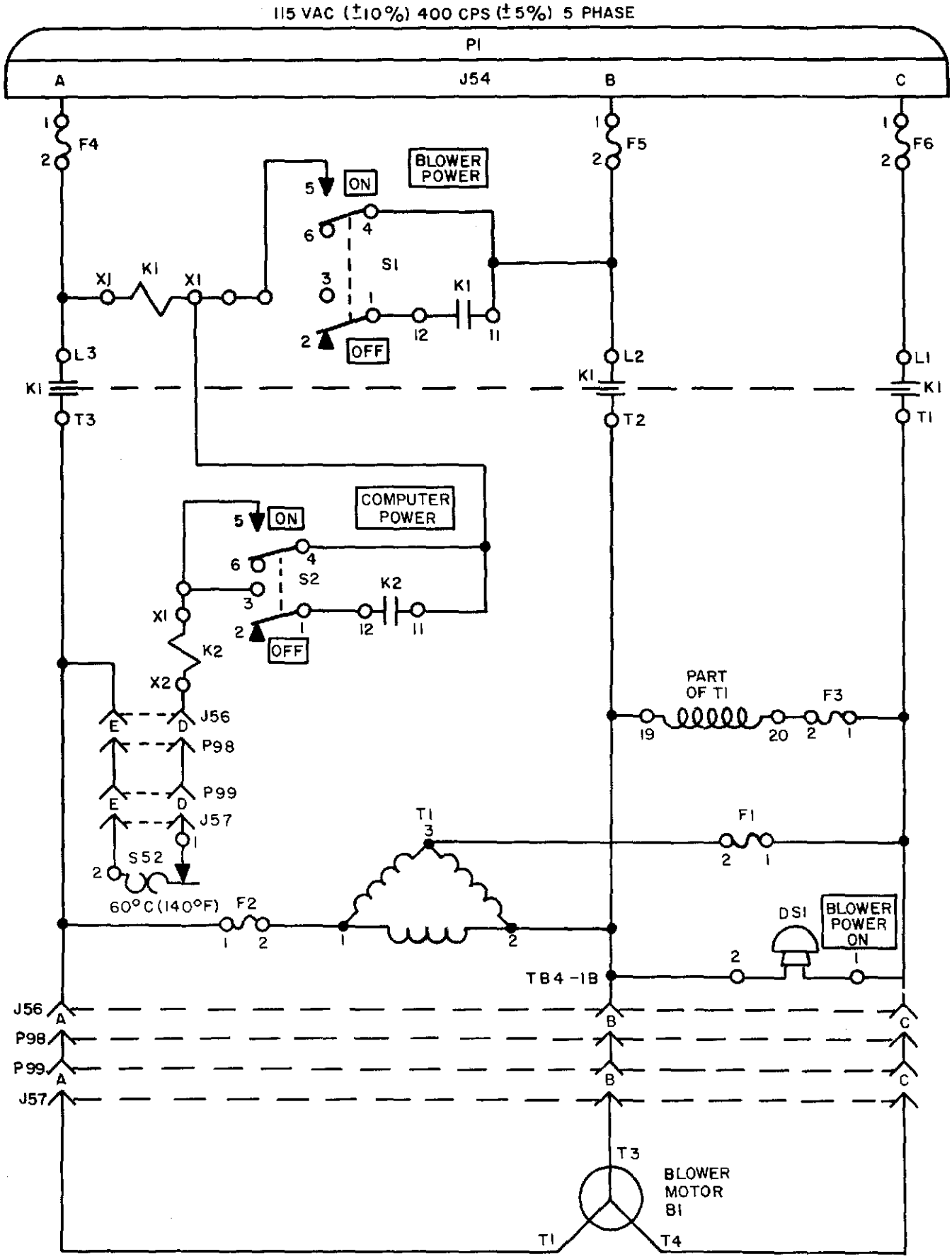


Figure 5-7. Unregulated Primary Power Distribution Diagram

Figure
5-8

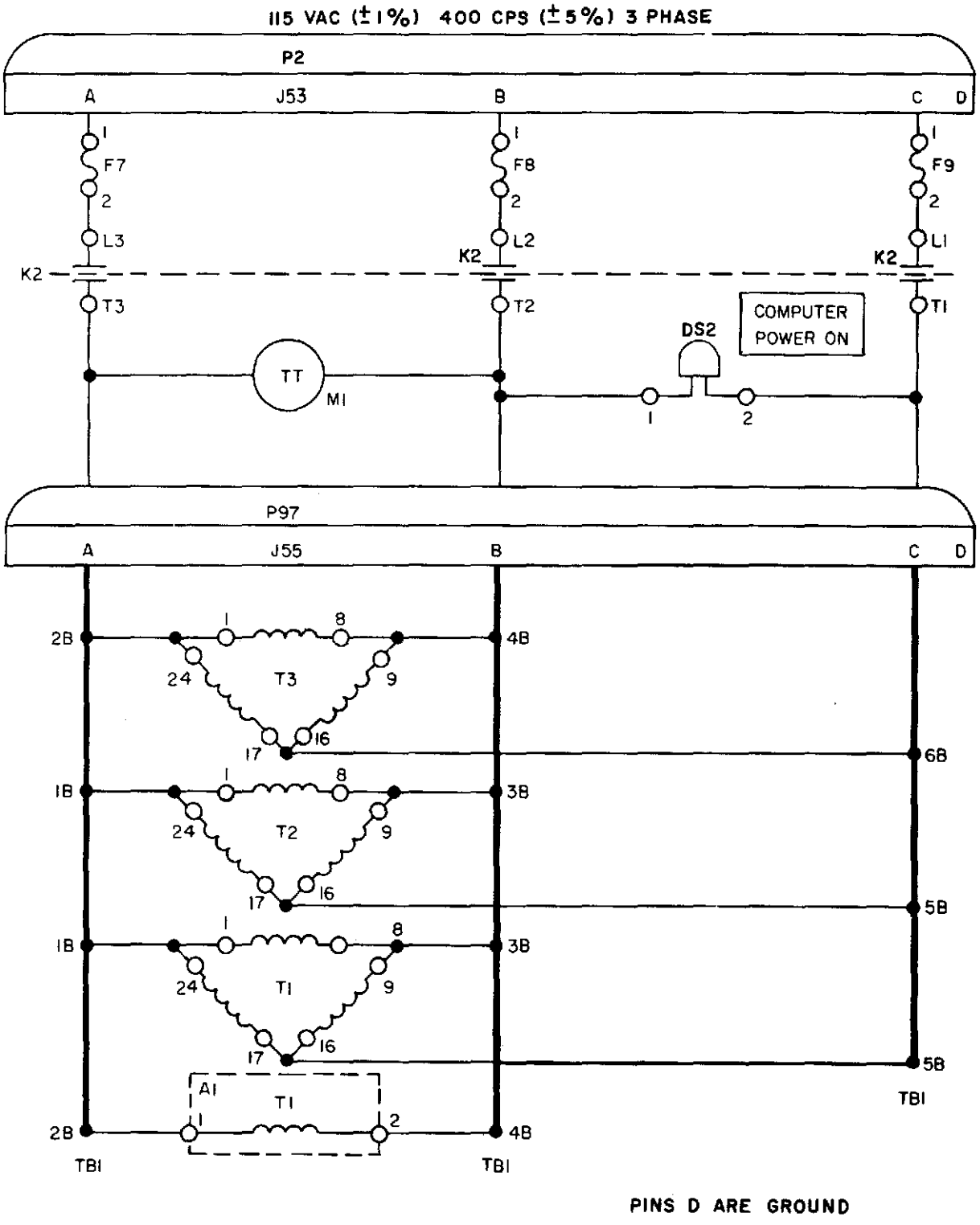


Figure 5-8. Regulated Primary Power Distribution Diagram

STEP 9. Disconnect the jumper connected in step 6. Computer power is removed and the COMPUTER POWER indicator is extinguished. The BLOWER POWER indicator remains lit. This insures that the overtemperature shut-down circuits are operative.

(3) LOCAL CONTROL INDICATORS.

STEP 1. Attach a ground wire to the input to 70Y00 (refer to figure 8-90). This simulates the remote panel being placed "on-line". The LOCAL CONTROL indicator is not lighted. Verify loss of local control by operating several controls and noting that their operation has no effect.

STEP 2. Operate the memory MARGINAL CHECK switch to the HIGH position. Local control is regained and the LOCAL CONTROL indicator lights. Operate the memory MARGINAL CHECK switch to the neutral position. The LOCAL CONTROL indicator is extinguished, and the computer controls are nonoperative. Operate the memory MARGINAL CHECK switch to the LOW position. Local control is regained and the LOCAL CONTROL indicator is lighted. Operate the memory MARGINAL CHECK switch to the neutral position. The LOCAL CONTROL indicator is extinguished and the computer controls are again inoperative.

STEP 3. Repeat step 2 for each memory chassis.

STEP 4. Remove the ground wire attached in step 1.

(4) MARGINAL CHECK INDICATORS. - Repeat step 2 of the preceding test (paragraph 5-4b(3). When the memory MARGINAL CHECK switch is in the high or low position, the MARGINAL CHECK indicator is lighted and the local controls are operative.

(5) FAULT INDICATOR.

STEP 1. Master clear the computer.

STEP 2. Store the instruction word, 61 400 00001, in memory address 00000 [refer to paragraph 3-3e(2) for manual store procedure].

STEP 3. Master clear the computer and depress the Af En indicator-switch.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. This causes the computer to perform the f = 00 instruction (illegal function code); the FAULT indicator glows and the computer is in a STOP 4.

STEP 5. Master clear the computer. The FAULT indicator is extinguished.

STEP 6. Manually set U to 77 000 00000 and press the Af En indicator-switch.

STEP 7. Operate the START-STEP/RESTART switch to the START-STEP position. This causes the computer to perform the f = 77 instruction (the other illegal function code); the FAULT indicator is lighted, and the computer is in a STOP 4.

STEP 8. Repeat step 5.

(6) RUN INDICATOR.

STEP 1. Master clear the computer.

STEP 2. Manually store the two following instructions in addresses 00000 and 00001 [refer to paragraph 3-3e(2) for manual store procedures].

00000	60	100	00001
00001	60	100	00000

STEP 3. Master clear the computer.

STEP 4. Operate the START-STEP/RESTART switch to the START-STEP position. The computer is running at high speed and the RUN indicator is lighted.

STEP 5. Press the RUN indicator-switch. The indicator is extinguished as long as the switch is pressed. Release the switch and the indicator glows.

STEP 6. Operate the STOP switch to the down position.

(7) MASTER CLEAR.

STEP 1. Master clear the computer.

STEP 2. Manually set bit indicators of the following registers and designators: A, Q, X, D, U, P, B, R, K2, K3, R, IN ACK, OUT ACK, IN MON, OUT MON, and IN ACT.

STEP 3. Master clear the computer. All indicators on the console shall be extinguished with the following exceptions: CLOCK PHASE; MARGINAL CHECK; LOCAL; MAIN TIMING Sequence; MODE Controls; PROGRAM I or II; DISCONNECTS, JUMP Selections, and STOP Selections (if selected); and Power Indicators.

STEP 4. Repeat steps 2, 3, and 4 of the preceding paragraph [5-4b(6)].

STEP 5. Press the MASTER CLEAR switch. There is no effect while in the run mode.

STEP 6. Operate the STOP switch to the down position.

STEP 7. Manually store 60 100 00000 in address 00000 and all "0's" in 00002 [refer to paragraph 3-3e(2) for manual store procedure].

STEP 8. Master clear the computer.

STEP 9. Set the P register to 00002.

STEP 10. Operate the START-STEP/RESTART switch to the START-STEP position. The computer performs the illegal function code (f = 00); the FAULT indicator is lighted and the computer continues to run.

STEP 11. Press the MASTER CLEAR pushbutton. The FAULT indicator is extinguished and the computer continues to run. If the MASTER CLEAR switch is pressed while the computer is operating in the run mode, only the Fault II flip-flop (and FAULT indicator) are cleared.

STEP 12. Operate the STOP switch to the down position.

(8) RUN MODE.

STEP 1. Master clear the computer. This automatically selects the run mode, and the RUN MODE indicator is lighted.

STEP 2. Press the OP STEP MODE indicator-switch. The indicator is lighted, and the RUN MODE indicator is extinguished.

STEP 3. Press the RUN MODE indicator-switch. The OP STEP MODE indicator is extinguished; the RUN MODE indicator is lighted.

STEP 4. Repeat steps 2, 3, and 4 of the run indicator test [refer to paragraph 5-4c(6)]. The RUN and RUN MODE indicators are lighted, and the computer is operating in the run mode.

(9) OP STEP MODE.

STEP 1. Master clear the computer.

STEP 2. Load the following instructions in consecutive addresses beginning with address 00000 [refer to paragraph 3-3e(2) for manual load procedures].

```
00000 01000 00004        RSH Q 4
00001 05000 00004        LSH Q 4
00002 02000 00002        RSH A 2
00003 06000 00002        LSH A 2
00004 60100 00000        JP 00000
```

STEP 3. Master clear the computer.

STEP 4. Manually set A lower to 00100 and Q lower to 00100.

STEP 5. Press the OP STEP MODE indicator-switch. The indicator lighted and the RUN MODE indicator extinguishes.

STEP 6. Repeatedly operate the START-STEP/RESTART switch to the START-STEP position. Each operation of the switches causes one instruction to be performed, and the computer stops at Bf. Observe the A and Q register bit indicators to verify that the instructions are being performed.

(10) PHASE STEP MODE.

STEP 1. Master clear the computer.

STEP 2. Press the PHASE STEP mode indicator-switch; the PHASE STEP mode indicator lights, and the RUN MODE indicator is extinguished.

STEP 3. Repeatedly operate the START-STEP/RESTART switch to the START-STEP position. Observe (on the CLOCK PHASE 1, 2, 3, and 4 indicators) that one clock phase is generated each time the START-STEP/RESTART switch is operated.

(11) LOAD MODE.

STEP 1. Master clear the computer.

STEP 2. Press the LOAD MODE indicator-switch; the LOAD MODE indicator is lighted, and the RUN MODE indicator is extinguished.

STEP 3. Operate the START-STEP/RESTART switch to the START-STEP position. The LOAD MODE indicator is extinguished, and the RUN MODE indicator is lighted. This indicates that the load mode has been initiated and is being performed in the high-speed run mode.

(12) AUTOMATIC RECOVERY SWITCH.

STEP 1. Master clear the computer.

STEP 2. Operate the AUTOMATIC RECOVERY switch to the center position.

STEP 3. Manually load address 00000 with 61 400 00000 and address 00001 with all "0's". [Refer to paragraph 3-3e(2) for a manual load procedure].

STEP 4. Master clear the computer.

STEP 5. Set the P register to 00001.

STEP 6. Operate the START-STEP/RESTART switch to the START-STEP position. An illegal function code (f = 00) is performed, a jump to address 00000 is performed, the computer comes to a STOP 4, and the FAULT light is lighted.

STEP 7. Master clear the computer.

STEP 8. Operate the AUTOMATIC RECOVERY switch to the up position.

STEP 9. Set the P register to 00001.

STEP 10. Operate the START-STEP/RESTART switch to the START-STEP position. This causes the illegal function code (f = 00) to be performed and causes the computer to jump to the bootstrap, as indicated by the fact that the computer did not STOP 4 and that the R register contains 00547. It appears as though the computer is stopped, but it is performing the instruction that is stored at 00547.

STEP 11. Return the AUTOMATIC RECOVERY switch to the center position.

(13) PHASE REPEAT.

STEP 1. Master clear the computer.

STEP 2. Press the PHASE STEP MODE indicator-switch.

STEP 3. Operate the PHASE REPEAT switch to the up position.

STEP 4. Press the CLOCK PHASE 1 indicator-switch.

STEP 5. Clock Phase 1 is the only phase being generated and it is being generated at the normal, high speed rate. Depress the other CLOCK PHASE indicators, in turn, and notice that the only clock phase being generated is the phase manually selected.

STEP 6. Operate the PHASE REPEAT switch to the center position.

(14) STOP SWITCH.

STEP 1. Master clear the computer.

STEP 2. Repeat steps 2, 3, and 4 of the RUN indicator test [refer to paragraph 5-4b(6)].

STEP 3. Operate the STOP switch to the down position. The computer stops and the RUN indicator is extinguished.

(15) START-STEP/RESTART SWITCH.

STEP 1. Repeat the run mode, op step mode, phase step mode, and load mode tests to verify that the START-STEP/RESTART switch functions in the START-STEP position.

STEP 2. Repeat steps 1 through 6 of the op step mode test [refer to paragraph 5-4b(9)].

STEP 3. Operate the START-STEP/RESTART switch to the RESTART position. The instructions are being initiated at the rate of the low-speed oscillator.

STEP 4. Rotate the RESTART SPEED CONTROL switch clockwise. The initiation rate of the instruction increases. Rotate the RESTART SPEED CONTROL switch counterclockwise. The initiation rate of the instruction decreases.

STEP 5. Repeat steps 1 and 2 of the phase step mode test [refer to paragraph 5-4c(10)].

STEP 6. Operate the START-STEP/RESTART switch to the RESTART position. The clock phases are being generated at the rate of the low-speed oscillator. Vary the RESTART SPEED CONTROL switch and notice that rate at which the clock phases are generated varies accordingly.

STEP 7. Return the START-STEP/RESTART switch to the neutral position.

STEP 8. Load the following program in addresses 00000 through 00005:

```
00000   12 500 00777
00001   72 500 00003
00002   61 400 00000
00003   70 000 77777
00004   10 000 00000
00005   61 000 00001
```

[Refer to paragraph 3-3e(2) for manual load procedures].

STEP 9. Master clear the computer.

STEP 10. Rotate the RESTART SPEED CONTROL switch fully counterclockwise.

STEP 11. Operate the START-STEP/RESTART switch to the RESTART position. The computer repeatedly comes to a STOP 4 but recovers automatically as controlled by the low-speed oscillator and RESTART SPEED CONTROL switch.

(16) RESTART SPEED CONTROL.

STEP 1. Repeat steps 1 through 4 of the preceding test to verify that the RESTART SPEED CONTROL varies the low-speed oscillator output.

STEP 2. Connect the oscilloscope to test point 5TB18A8. Vary the RESTART SPEED CONTROL switch and observe that the rate varies from about 2 to 200 cycles per second.

(17) STOP.

STEP 1. Repeat steps 2, 3, and 4 of the Run indicator test [refer to paragraph 5-4b(6)]. The computer is running in normal high speed mode.

STEP 2. Operate the STOP switch to the down position. The computer stops operation with Af En set.

(18) DISCONNECT B7.

STEP 1. Master clear the computer.

STEP 2. Manually load the following instructions in addresses 00000 through 00003 [refer to paragraph 3-3e(2) for manual load procedures].

```
00000   12 600 77777    ENT B6
00001   70 000 00007    RPT NI 7
00002   17 640 00000    STR B6 A
00003   61 400 00000    JP 00000 STOP 4
```

STEP 3. Master clear the computer.

STEP 4. Operate the DISCONNECT B7 switch to the up (selected) position.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The computer is repeating the store B6 in A instruction; A lower contains 77777.

STEP 6. Operate the DISCONNECT B7 switch to the down position. The computer repeats the store B6 in A instruction seven times (at high speed) and jumps to address 00000 with a STOP 4. The FAULT indicator is lighted.

(19) DISCONNECT ADV P.

STEP 1. Master clear the computer.

STEP 2. Manually load the following instructions in addresses 00000 through 00003 [refer to paragraph 3-3e(2) for manual load procedures].

00000	10 000 00000	ENT · Q · 00000
00001	10 000 52525	ENT · Q · 52525
00002	11 000 52525	ENT · A · 52525
00003	61 400 00000	JP · 00000 · STOP 4

STEP 3. Master clear the computer.

STEP 4. Operate the ADV P switch to the up (selected) position.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The computer is running at high speed, repeating the Enter Q with "0's" instruction.

STEP 6. Operate the DISCONNECT ADV P switch to the down position. The computer executes the next three instructions and jumps to address 00000 with a STOP 4; Q lower and A lower contain alternate "1's" and "0's".

(20) DISCONNECT RTC. - The DISCONNECT RTC switch is checked during the real-time clock test [refer to paragraph 5-3d(3)].

(21) JUMPS.

STEP 1. Master clear the computer.

STEP 2. Manually load the following instructions in addresses 00000 through 00011 [refer to paragraph 3-3e(2) for manual load procedures].

00000	61 100 00003	JP 1 · 00003
00001	61 200 00005	JP 2 · 00005
00002	61 300 00007	JP 3 · 00007
00003	10 000 77777	ENT Q · 77777
00004	61 400 00000	JP · 00000 · STOP 4
00005	11 000 77777	ENT A · 77777
00006	61 400 00000	JP · 00000 · STOP 4
00007	10 000 52525	ENT Q · 52525
00010	11 000 52525	ENT A · 52525
00011	61 400 00000	JP · 00000 · STOP 4

STEP 3. Master clear the computer.

STEP 4. Operate the JUMP 1 switch to the up (selected) position. The JUMP indicator illuminates.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The computer jumps to address 00000 and comes to a STOP 4. Q lower contains all "1's".

STEP 6. Return JUMP 1 to the down position. Operate the JUMP 2 switch to the up (selected) position.

STEP 7. Operate the START-STEP/RESTART switch to the START-STEP position. The computer jumps to address 00000 and comes to a STOP 4. A lower contains all "1's".

STEP 8. Return JUMP 2 switch to the down position. Operate the JUMP 3 switch to the up (selected) position.

STEP 9. Operate the START-STEP/RESTART switch to the START-STEP position. The computer jumps to address 00000 and comes to a STOP 4. Q lower and A lower contain alternate "1's" and "0's".

STEP 10. Return the JUMP 3 switch to the down position. The JUMP indicator is extinguished.

(22) STOPS.

STEP 1. Master clear the computer.

STEP 2. Manually load the following instructions in addresses 00000 through 00003 [refer to paragraph 3-3e(2) for manual load procedures].

00000	61 500 00001
00001	61 600 00002
00002	61 700 00003
00003	61 400 00000

STEP 3. Master clear the computer.

STEP 4. Operate the STOP 5 switch to the up (selected) position. The STOP indicator is lighted.

STEP 5. Operate the START-STEP/RESTART switch to the START-STEP position. The computer jumps to address 00001 and comes to a STOP 5; the STOP 5 indicator is lighted.

STEP 6. Return the STOP 5 switch to the down position. Operate the STOP 6 switch to the up (selected) position.

STEP 7. Operate the START-STEP/RESTART switch to the START-STEP position. The computer jumps to address 00002 and comes to a STOP 6; the STOP 6 indicator is lighted.

STEP 8. Return the STOP 6 switch to the down position. Operate the STOP 7 switch to the up (selected) position.

STEP 9. Operate the START-STEP/RESTART switch to the START-STEP position. The computer jumps to address 00003 and comes to a STOP 7; the STOP 7 indicator is lighted.

STEP 10. Return the STOP 7 switch to the down position. The STOP indicator is extinguished.

STEP 11. Operate the START-STEP/RESTART switch to the START-STEP position. The computer jumps to address 00000 and comes to a STOP 4; the STOP 4 indicator is lighted.

(23) C REGISTER SWITCHES.

STEP 1. Rotate the two C register switches to the C1, C2, C3 or C4 position.

STEP 2. Manually set random bits of C.

STEP 3. With the oscilloscope, check the flip-flops of C1, C2, C3, or C4 (respectively) to verify that they are set or clear as indicated on the console (refer to figures 8-126 and 8-127 for test point data).

(24) REGISTERS AND DESIGNATORS.

(a) The bits of all the registers and designators except subpriority, main Priority, translators, S, Z, timing sequences, and the g and active sequence designators are tested in the following manner:

STEP 1. Master clear the computer.

STEP 2. Press the indicator-switch for the stage or stages of the registers and/or designators to be tested. The indicators light and remain lit until the CLEAR button for that stage or the particular register is pressed, at which time they extinguish. Verification that the flip-flops have been cleared or set is obtained by checking the appropriate test points with an oscilloscope.

(b) The bits of the g and timing control designators, subpriority, main priority, translators, S and Z registers, timing sequences and subsequences are tested in the following manner:

STEP 1. Master clear the computer.

STEP 2. Press the PHASE STEP MODE indicator-switch.

STEP 3. Press the indicator-switches for the designators. The indicator-switches which are pressed light and remain lit.

STEP 4. Press OP STEP MODE indicator-switch.

STEP 5. Press the MASTER CLEAR switch. All indicators are extinguished except MAIN TIMING and CLOCK PHASE indicators.

STEP 6. Repeat Steps 2 through 5 for each group of bits listed.

(25) MASTER CLOCK. - The Master Clock is checked as follows: Observe with the oscilloscope test points J14C5, J14E5, J14G5, and J14I5 on chassis A5. These are the four clock phases (1, 2, 3, and 4 respectively). The cycle period is approximately 680 nanoseconds. The clock cycle waveform has a period of between 660 and 700 nanoseconds at the 50 percent amplitude points. The clock pulse duration is from 115 to 135 nanoseconds at the 50 percent amplitude points.

SECTION 6

REPAIR

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SECTION 6

REPAIR

6-1. FAILURE, PERFORMANCE, AND OPERATIONAL REPORTS.

NOTE

The Bureau of Ships no longer requires the submission of failure reports for all equipments. Failure Reports and Performance and Operational Reports are to be accomplished for designated equipments (refer to Electronics Installation and Maintenance Book, NAVSHIPS 900,000) only to the extent required by existing directives. All failures shall be reported for those equipments requiring the use of Failure Reports.

6-2. TUNING AND ADJUSTMENT.

a. TEST EQUIPMENT AND SPECIAL TOOLS. - Refer to table 5-1 for test equipment and special tools required.

b. ADJUSTMENTS. - Accessible adjustments on the computer are kept to a minimum. There are no accessible operational adjustments on the logic chassis. The only adjustments which are necessary are those concerned with memories and power supplies. The memory adjustments include procedures for changing the +10 VDC output in the event that the output varies appreciably from the standard.

(1) MAIN MEMORY ADJUSTMENTS. - This section contains the necessary procedures for adjusting the X and Y read and write currents, the inhibit current, the strobe timing and the regulated +10 VDC on each memory chassis.

CAUTION

Do not make any adjustments in the memory unless it has been determined without a doubt that the malfunction is caused by a misadjustment rather than a failing circuit. Refer to paragraph 6-3b.

With the exception of the +10 VDC regulated supplies, all operational adjustments are located on the front of each memory chassis (see figure 6-1). The main memory adjustments for each memory chassis consist of setting the +10 VDC power supply for a nominal inhibit current, adjusting the X and Y read/write currents and finally, to optimize the circuits for minimum noise at the outputs of the sense amplifiers.

The nominal current values which are given in the following procedures are for a core temperature of +25°C (+77°F). A thermistor, located in each core stack, compensates for temperature variations by varying the output of the associated +10 VDC supply. When the core temperature is higher or lower than +25°C (+77°F), the currents must be set inversely proportional to the temperature variation. The approximate change in current for each degree variation is 1.0 to 1.5 milliamperes.

The main memory circuits may be adjusted either by using an oscilloscope and the chassis test points or by using an oscilloscope together with a current probe and a module extender. When possible, it is recommended that the second method be used since the resulting oscilloscope waveforms have a much lower noise content.

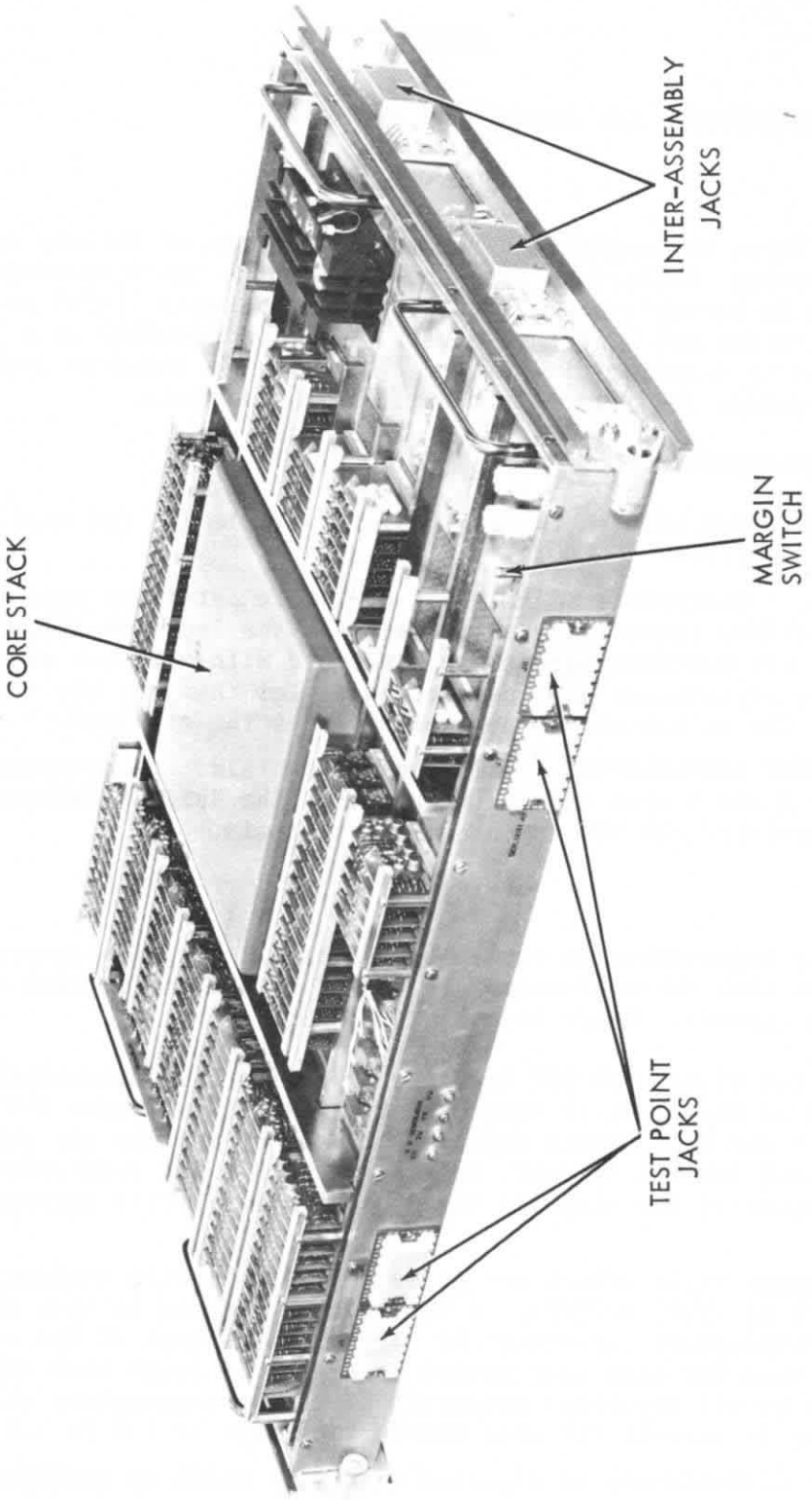


Figure 6-1. Core Memory Chassis

(a) CURRENT ADJUSTMENTS USING CHASSIS TEST POINTS.

STEP 1. Apply power to the computer and run a repeated 55 (f = 55) instruction in the computer using normal operation [refer to paragraph 5-3d(2)(a)2]. Run the computer for 15 to 20 minutes to allow the core temperature to stabilize.

CAUTION

Do not ground the oscilloscope or allow it to touch the computer or any equipment that is grounded.

NOTE

Current waveforms observed during the following steps are measured across a 1 ohm resistor located in the affected modules.

STEP 2. Set up the oscilloscope using AC FAST with EXT TRIG. Use the output from test point 5TB13G7 as the trigger source. Attach two direct probes to the oscilloscope; one probe to the channel A input and the other probe to the ground terminal.

To observe the input inhibit current waveform, connect the two direct probes between any one set of the inhibit test points listed in table 6-1. (Example: TB5J6 - TB5J8.) The amplitude of the inhibit current waveform (see figure 6-2) is dependent upon the output voltage of the +10 VDC power supply.

Adjust the +10 VDC supply to obtain an inhibit current of approximately 220 ma by using R3 located on module J37E (figure 6-1). Because of its location in the chassis, R3 cannot be adjusted while the chassis is in the computer. Therefore, the +10 VDC supply must be adjusted by a trial and error method with the chassis removed.

STEP 3. To adjust the X read current to the nominal value listed in table 6-1, connect the oscilloscope (with the direct probes attached as in step 2) between test points TB6M6 and TB6M8.

Set the XR trimmer resistor for the read current value listed in table 6-2. The X write current is adjusted to the value listed in table 6-2 by connecting the oscilloscope to test points TB6M1 and TB6M3 and adjusting the XW trimmer resistor for the proper value of write current. Figure 6-3 illustrates a typical X read/write waveform.

STEP 4. Repeat the steps for the Y read and write current adjustments using the test points listed in table 6-2. Use trimmer resistors YR and YW for adjusting the currents to the values listed in table 6-2. Figure 6-4 illustrates a typical Y read/write current waveform.

TABLE 6-1. MEMORY TEST POINTS

X READ/WRITE	Y READ/WRITE	INHIBIT CURRENT	SENSE AMPLIFIERS
READ			
TB6M6	TB6L6	TB5J6 - TB5J8	TB7F1
TB6M8	TB6L8	TB5J1 - TB5J3	TB7F2
WRITE			
TB6M1	TB6L1	TB5H6 - TB5H8	TB7F3
TB6M3	TB6L3	TB5H1 - TB5H3	TB7F4
		TB5F6 - TB5F8	TB7F5
		TB5F1 - TB5F3	TB7F6

TABLE 6-2. NOMINAL MEMORY CURRENT VALUES

	CORE MANUFACTURER
	ELECTRONIC MEMORIES INC.
X READ	220 ma
X WRITE	230 ma
Y READ	220 ma
Y WRITE	230 ma
INHIBIT	220 ma

STEP 5. Set the strobe timing so that it is slightly behind the maximum amplitude of the "1" output but at a point which is least susceptible to noise. Strobe adjustment is accomplished by moving the taps on delay line 91Y01 at location J7F. It is necessary to remove the bottom chassis cover to obtain access to the strobe timing. Adjustments must be made by the trial and error method. To set the strobe ahead, attach to a smaller number on the J7F delay line. To set the strobe so that it occurs later, attach to a larger number. Figure 6-5 illustrates a typical relationship between a strobe pulse and a "1" output. The first waveshape on the sense line is caused by the previous write pulse.

STEP 6. Repeat steps 2 through 5 for each memory chassis.

After each memory chassis has been adjusted according to the previous steps, the following steps should be used to make the final adjustments.

STEP 1. Perform the pattern test generating the maximum amount of memory noise in the computer [refer to paragraph 5-3c(2)] .

STEP 2. Set up the oscilloscope using AC FAST with EXT TRIG. Use the output from 5TB13G7 as the trigger source. Measure the output from the sense amplifiers at the test points listed in table 6-1. Measure between the test point and ground.

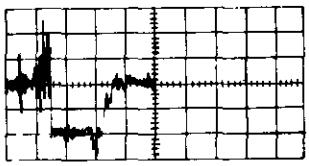
STEP 3. Observe the amount of noise on the waveforms. Figure 6-6 (Noise) illustrates a typical waveform. Readjust the X read/write currents, the Y read/write currents, the inhibit currents, and the +10 VDC for minimum noise. This procedure may be time consuming but must be done carefully and thoroughly. Figure 6-6 (Best Condition) illustrates a typical waveform for the best condition.

STEP 4. Repeat step 3 for each memory chassis.

STEP 5. After all adjustments have been made, check the settings by running memory under marginal conditions. Run with both high and low margins. If there is any failure, repeat step 3 for the failing chassis. Refer to paragraph 4-2e for detailed explanation of the memory system.

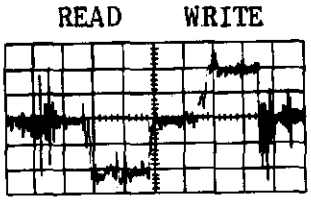
(b) ADJUSTMENTS USING MODULE EXTENDERS.

STEP 1. Apply power to the computer and run a repeated 55 (f=55) instruction in the computer using normal operation, refer to paragraph 5-3d(2)(a)2. Run the computer for 15 to 20 minutes to allow the core temperature to stabilize.



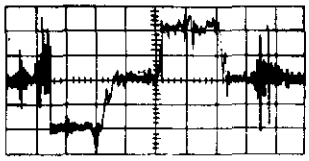
100 ma/cm
0.5 μsec/cm

Figure 6-2. Inhibit Current Waveform



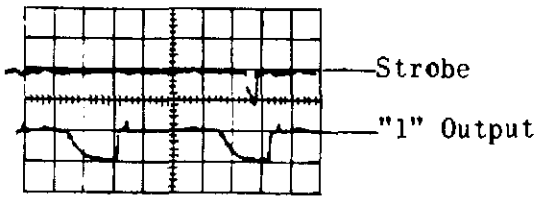
100 ma/cm
0.5 μsec/cm

Figure 6-3. X Read/Write Current Waveform



100 ma/cm
0.5 μsec/cm

Figure 6-4. Y Read/Write Current Waveform



5.0 v/cm
0.5 μsec/cm

Figure 6-5. Strobe Pulse and "1" Output Timing Waveform

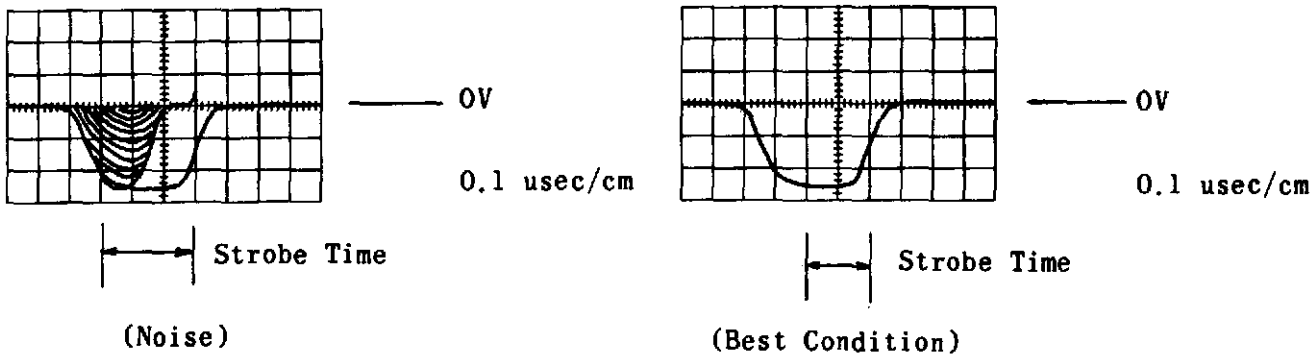


Figure 6-6. Sense Amplifier Outputs Waveform

STEP 2. Set up the oscilloscope using AC FAST with EXT TRIG. Connect the oscilloscope ground to the computer ground and use the output from 5TB13G7 as the trigger source.

STEP 3. Use the module extender to extend one of the inhibit transformer modules. (Example: module J10B, shown on figure 8-106.) There are three pairs of output inhibit lines (pins 1-5, 8-9, 12-13) from each module. Select one pair for the inhibit current test. Clamp a type P6016 current probe and termination across one wire of the selected pair. Note the value of the inhibit current waveform displayed on the oscilloscope. The inhibit current should be approximately 220 ma. The inhibit current amplitude is dependent upon the output from the +10 VDC power supply. The +10 VDC supply is adjusted by using the module extender to extend module J37E and adjusting the module trimmer resistor R3.

STEP 4. The X read and write currents are adjusted to the same value as the inhibit current in the following manner:

1) Extend one of the eight X line selector modules (example - module 9J16G, figure 8-103).

2) Each of the X line selector modules has two outputs (pins 12 and 15) connecting to the stack. Clamp the probe across the both leads extending from pins 12 and 15.

3) Both the read and write current waveforms will be displayed on the oscilloscope during recurring intervals. The read current waveform occurs first, followed after a short interval by the write current waveform. After a longer time

interval the two current waveforms are again displayed. The polarity of the waveforms is immaterial and is dependent upon the manner in which the probe is attached to the leads. (See figures 6-3 and 6-4.)

4) Use the XR and XW trimmer resistors to adjust the X read and write currents to the same value as the inhibit current noted in step 3.

STEP 5. The Y read and write currents are adjusted in the same manner as described in step 3.

1) Extend one of the eight Y line selector modules (example - module J32E, figure 8-104).

2) Connect the current probe across the leads connected to pins 12 and 15. Use the YR and YW trimmer resistors to adjust the Y read and write currents to the same value as the inhibit current noted in step 3.

STEP 6. Repeat steps 2 through 5 for each memory chassis.

STEP 7. Using a regular 10:1 oscilloscope probe with the ground terminal connected to the computer ground, check the output from the sense amplifiers using the test points listed in table 6-1.

Observe the amount of noise on the waveforms. Figure 6-6 (Noise) illustrates a typical waveform. For each X and Y waveform, circuit noise can usually be adjusted to its minimum value by turning the XW and/or YW trimmer controls from 2 to 4 turns in a clockwise direction. In some cases, it may also be necessary to slightly readjust the read currents. Adjusting the circuits for minimum noise must be done thoroughly and carefully.

STEP 8. Repeat step 5 for each memory chassis.

STEP 9. After all adjustments have been made, check the settings by running memory under marginal conditions. Run with both high and low margins. If there is any failure, repeat steps 1 through 6 and 8 for the failing chassis. Refer to paragraph 4-2e for detailed explanation of the memory system.

(2) CONTROL AND BOOTSTRAP MEMORY ADJUSTMENTS. - The principle adjustments to control and bootstrap memory are those concerned with timing. The timing relationship between word and digit current and the duration of each is critical. Also the strobe and reset timing with respect to the sense output is very important. The external sync point to be used for triggering the oscilloscope is 8TB15A1.

CAUTION

Do not make any adjustments to control or bootstrap memory until it has been determined that the cause of a malfunction is due to misadjustment rather than a failing component.

(a) TROUBLESHOOTING AND TIMING. - The two word current generators (WCG) are removed from 8J51C and 8J51D until it has been determined that the inputs to them are correct. Check all bit registers in the SØ register to see if the address information is being received correctly and to determine if all the bit registers in the SØ register are functioning properly. Refer to figures 8-109 and 8-110 to determine the test points to be used to check the SØ register.

(b) WORD CURRENT ADJUSTMENT. - To get proper word current timing and word line selection, the following conditions must exist:

1) Only one word transformer selector may be activated at any time; this is checked on 8TB15J5, 8TB15J4, 8TB15J3, 8TB15J2, 8TB15J1, 8TB1518, 8TB1517, and 8TB1516. A typical word transformer selector output is shown in figure 6-7A. The current as an activated word transformer is shown in figure 6-7B.

2) Only one word current translator may be activated at any time; this is checked by referring to figure 8-110 and test points 8TB15G3, 8TB15G2, 8TB15G1, 8TB15F8, 8TB15F7, 8TB15F6, 8TB15F5, and 8TB15F4.

3) If items 1) and 2) above give the proper results, the word current generators may be replaced in locations 8J51C and 8J51D. The starting time and duration of the word current is controlled by the delay line. Monitor the output voltage of the slowest word current translator or word transformer selector (WTS). With the computer doing a clear/write of control memory address 0, attach the current probe to 8J52D pin 13. The module extender must be used to accomplish this. Move the terminal connected to 8J47B pin 11 along the delay line so that the word current begins 40 nanoseconds after the slowest word current translator or WTS is activated. This must be done by the trial and error method and should result with the tap being at approximately 8J47A pin 12. With the computer doing a clear/write of bootstrap program II address 0, attach the current probe to 8J52C pin 13. The module extender must be used to accomplish this. Move the terminal connected to 8J46B pin 13 along the delay line so that the word current begins 40 nanoseconds after the slowest word current translator or WTS is activated. This must be done by the trial and error method and should result with the tap being at approximately 8J47A pin 13. Temporarily connect the terminal attached to 8J47B pin 15 onto 8J44A pin 10 until the desired duration of the word current is established. Refer to figure 6-8 for a typical word current waveform. With the computer doing a clear/write in the addresses listed in table 6-3, check the word current at the outputs.

(c) BIT TIMING ADJUSTMENT. - The starting time and duration of the bit current is controlled by the delay line timing. The digit current is started as soon as the slowest ZØ flip-flop is activated. With the computer doing a read-restore of either bootstrap or control memory, locate the slowest ZØ flip-flop. This can be determined by writing all ones into the memory and timing one bit waveform against another until the slowest one is obtained. Monitor this flip-flop and attach a current probe to the twisted pair of the corresponding bit generator. Move the terminal attached to 8J47B pin 13 along the delay line so that the digit current starts as soon or slightly after the slowest ZØ flip-flop is set. This is approximately 8J45A pin 8. Temporarily connect the terminal attached to 8J46B pin 9 onto 8J43A pin 6, until the desired duration of the digit current can be established.

With the computer doing a clear-write from address 0, check the digit current for both a "1" and "0" for each bit. Note the slowest bit. The waveforms should be as illustrated in figure 6-9.

(d) ADJUSTING THE WORD CURRENT DURATION. - When the above steps have been successfully completed, it is possible to establish the word current duration. The word current is set to overlap the slowest digit current as shown in figure 6-10. Move the terminal attached to 8J47B pin 15 along the delay line until the word current overlaps the digit current by 50 nanoseconds. This is approximately at tap 8J44A pin 10.

TABLE 6-3. WORD CURRENT TEST POINTS

CONTROL MEMORY ADDRESSES	OUTPUT PINS
0	8J52D - 13
10	8J52D - 10
20	8J52D - 7
30	8J52D - 5
40	8J50D - 13
50	8J50D - 10
60	8J50D - 7
70	8J50D - 5
BOOTSTRAP I ADDRESSES	**OUTPUT PINS**
0	8J50C - 13
10	8J50C - 10
20	8J50C - 7
30	8J50C - 5
BOOTSTRAP II ADDRESSES	**OUTPUT PINS**
0	8J52C - 13
10	8J52C - 10
20	8J52C - 7
30	8J52C - 5

(e) ADJUSTING DIGIT CURRENT DURATION. - When the word current duration has been successfully determined, it is possible to adjust the digit current. The duration of the digit current must be sufficient to overlap any ringing on the word line. Move the terminal connected to 8J46B pin 9 along the delay line until the digit current sufficiently overlaps the ringing. This is approximately 8J43A pin 6. Refer to figure 6-11.

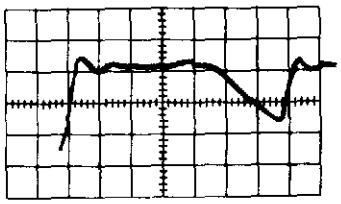
(f) ADJUSTING SENSE OUTPUT. - The sense output occurs during the rise time of the word current. The sense output is observed using the oscilloscope Type CA Preamp in the ADDED ALGEBRAICALLY mode, with the probes on pins 5 and 6 of the sense amplifier. The polarity of the sense output for a "1" or "0" depends upon the address as shown in paragraph 4-2e(3)(d)2. The amplitude, polarity, and duration of the digit noise may vary greatly from sense line to sense line. With the computer doing a clear-write in address 0, check each sense amplifier output. Refer to figures 6-12 and 6-13.

(g) ADJUSTING THE STROBE. - Set the strobe pulse to be coincident with the sense output. The strobe pulse is controlled by the delay line timing. Move the terminals connected to 8J40A pin 15 and 8J39A pin 15 along the delay line until the sense output and strobe pulse are coincident. This is approximately tap 8J46A pin 11. Check the strobe at the locations shown on table 6-4. (See figure 6-14.)

(h) ADJUSTING THE RESET PULSE. - Set the sense amplifier reset so that the sense output is about 200 nanoseconds. Move the terminal connected to 8J47B pin 9 until the sense output is approximately 200 nanoseconds wide which is approximately 8J44A pin 9. Figure 6-15 illustrates a typical waveform.

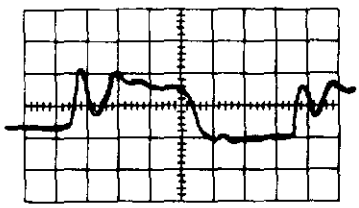
TABLE 6-4. STROBE AND SENSE OUTPUT PIN NUMBERS

STROBE	SENSE OUTPUT
8J41G - 11	8J38F - 6
8J41G - 12	8J38F - 5
8J38A - 11	8J38B - 6
8J38A - 12	8J38B - 5
8J31A - 11	8J31B - 6
8J31A - 12	8J31B - 5
8J33G - 11	8J30F - 6
8J33G - 12	8J30F - 5



A.

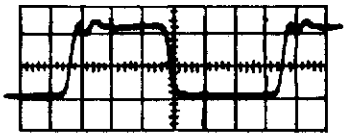
Word Transformer Selector Output
5 volts/cm
100 nsec/cm



B.

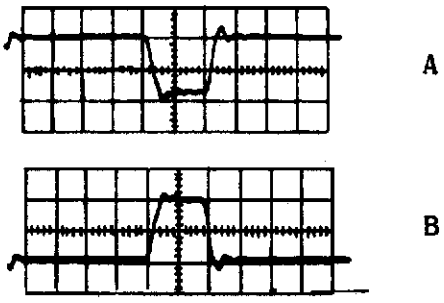
Word Transformer Selector Current
100 ma/cm
100 nsec/cm

Figure 6-7. Word Transformer Selector Waveforms



100 ma/cm
100 nsec/cm

Figure 6-8. Word Current Waveform

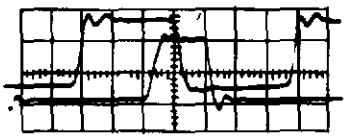


50 ma/cm
100 nsec/cm

A Digit Current to restore a "1"

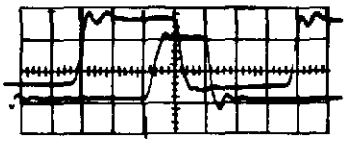
B Digit Current to restore a "0"

Figure 6-9. Digit Current Waveforms



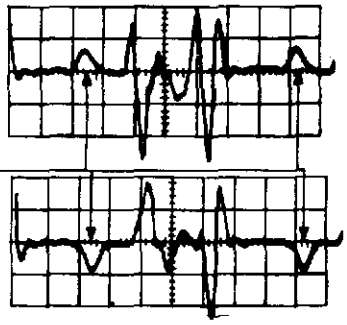
Word Current 100 ma/cm
Digit Current 50 ma/cm
100 nsec/cm

Figure 6-10. Word and Digit Current Waveforms



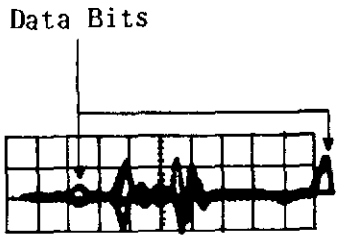
Word Current 100 ma/cm
Digit Current 50 ma/cm
100 nsec/cm

Figure 6-11. Word and Digit Current Timing Waveforms



.5 MV/cm
100 nsec/cm

Figure 6-12. Single Address Sense Output Waveforms



1.0 V/cm
100 nsec/cm

Figure 6-13. All Addresses Sense Output Waveforms

A Strobe pulse normally +2V

B Sense output

Figure 6-14. Strobe and Sense Output Waveform

A Sense Amplifier Output

B Sense Amplifier Reset Pulse

Figure 6-15. Sense Amplifier Reset and Sense Output Waveforms

(i) ADJUSTING THE CURRENT AMPLITUDES. - With the computer doing a clear-write in all film memory addresses, adjust the word current until both polarities of film output signal are a maximum and the output signals are uniform. This is checked using the oscilloscope Type CA Preamp in the ADDED ALGEBRAICALLY mode and checking the signals at pins 5 and 6 of the sense amplifier.

NOTE

If, after adjusting the word currents, the memory is dropping bits, a possible solution may be that the digit bit current is too low. If the memory is picking up bits, a possible solution may be that the digit current is too high. The nominal word current is 240 ma, the digit bit current is 90 ma.

(3) POWER ADJUSTMENTS.

(a) POWER TRANSFORMER. - When the aging of a component or other causes make it necessary to change the primary taps on the power transformers, proceed as follows:

STEP 1. Remove enough of the lower chassis to have access to the main power supply.

STEP 2. Apply a DC meter to the output of the affected supply (refer to figures 8-176 and 8-177).

WARNING

Disconnect input power cables while moving taps. Connect input power cables to check results.

STEP 3. Move the primary taps to bring the DC output within tolerance.

(b) +10 VDC VOLTAGE REGULATOR. - The +10 VDC adjustment on each memory chassis is done with the aid of a module extender. Extend the +10 VDC regulator module (J37E, figure 6-1). Meter the DC output and adjust the potentiometer (R3) for +10 VDC. The core stack should be operating at +25°C (+77°F) for this adjustment. Refer to paragraph 6-2b(1) for exact adjustment procedure.

(c) VOLTAGE SENSORS. - The voltage sensor circuits are adjusted with the trimmer resistors located on the sensor modules.

STEP 1. Turn off the computer.

STEP 2. Slide chassis A5 part way out to provide access to the modules located at J50C and J50D.

STEP 3. Remove the 2880 module at J50C. Plug the module extender into J50C and insert the 2880 module into the module extender. Roll the A5 chassis back into place, leaving the 2880 module accessible for adjustments.

STEP 4. Make provisions for adjusting the regulated power input to the computer. This can be done either at the motor generator set or by inserting a three-phase 400-cycle variable transformer in the line.

STEP 5. Apply power to the computer. Adjust the regulated power to 100 VAC line-to-line.

STEP 6. Connect the multimeter between 5TB16-D8 and ground. Adjust R3 on the 2880 module (see figure 6-150) until the multimeter indicates a voltage change from zero (0) volts to a negative voltage. Make a note of the R3 adjust screw position so that the adjust screw can be visually reset later on. After marking the screw position, return the R3 adjust screw slightly past the point where the indicated voltage returns to zero (0) volts.

STEP 7. Adjust R8 on the 2880 module in the same manner as in step 6; however, leave the R8 adjust screw at the setting where the multimeter indicates a change from zero (0) volts to a negative voltage.

STEP 8. Return the R3 adjust screw to the position noted in Step 6.

STEP 9. Turn off the computer and slide chassis A5 out from the cabinet so as to provide access to J50C. Remove the module extender. Remove the 2880 module from the extender and mark it for later installation in J50C of chassis A5.

STEP 10. Remove the 2890 module at J50D. Plug the module extender into J50D and insert the 2890 module into the extender. Return the A5 chassis to an operational position, leaving the 2890 module accessible for adjustments.

STEP 11. Apply power to the computer; ensure that the regulated power input is 100 VAC line-to-line and that the multimeter is connected as in Step 6.

STEP 12. Adjust R11 on the 2890 module (see figure 6-152) until the multimeter again indicates a change from zero (0) volts to a negative voltage. Leave the R11 adjust screw at the setting where the voltage change occurs.

STEP 13. Turn off the computer. Remove the 2890 module and mark it for later installation in J50D of chassis A5. Remove the module extender and return chassis A5 to its operating position.

STEP 14. The 2880 and 2890 modules on chassis A8 are adjusted in essentially the same manner as described in steps 1 through 13 with the following exceptions.

1) Adjust the regulated input power to 104 VAC line-to-line.

2) Connect the multimeter between 8TB10-M8 and ground.

3) Using the module extender, adjust R3 on the 2880 module (J12F) and observe the settings at which the multimeter indicates a change from zero (0) volts to a negative voltage. Leave the adjust screw at the setting where the voltage change occurs. Repeat the process for the R8 adjustment.

4) Remove the module extender and mark the 2880 module for later installation in J12F.

5) Repeat step 12 for R11 on the 2890 module located at J11G.

STEP 15. Turn off the computer. Replace the 2880 and 2890 modules to their respective chassis locations. Return the chassis to their operating positions and reset the regulated power input to 115 VAC line-to-line.

6-3. REMOVAL, ADJUSTMENT, REPAIR AND REASSEMBLY OF PARTS AND SUBASSEMBLIES.

a. CHASSIS REMOVAL (See figure 6-16). - The removal of a chassis should be done by two people because each logic chassis weighs about 84 pounds and each memory chassis weighs about 60 pounds. Have a clear work area available before removing a chassis. The procedure for removing a chassis is as follows:

STEP 1. Turn off the computer.

STEP 2. Remove the socket wrench from the compartment in the door, and loosen the five fasteners holding the doors closed. Open the doors.

STEP 3. With the square headed socket and ratchet, turn the two connector release shafts, on either side of the chassis (in the sides of the cabinet) in the OPEN direction until the plugs have cleared the jacks on the chassis.

STEP 4. Loosen the chassis locks on both sides of the chassis.

STEP 5. Apply the chassis puller tools over the chassis locks, and carefully slide the chassis out as far as it will go.

STEP 6. With a man on each side of the chassis, depress the chassis release rods on both sides of the chassis. Remove the chassis to the work area.

STEP 7. Replace the chassis by sliding it into the proper slot; secure the chassis locks, and turn the plug drive shafts until firm connection is made with the chassis jacks. The chassis is now operational.

NOTE

Securing the chassis locks first will ensure that the chassis jacks and side plugs will mate properly.

b. PRINTED CIRCUIT MODULE REPLACEMENT. - If the chassis must be removed to expose the printed circuit module to be replaced, remove according to paragraph 6-3a. Replace the module as follows.

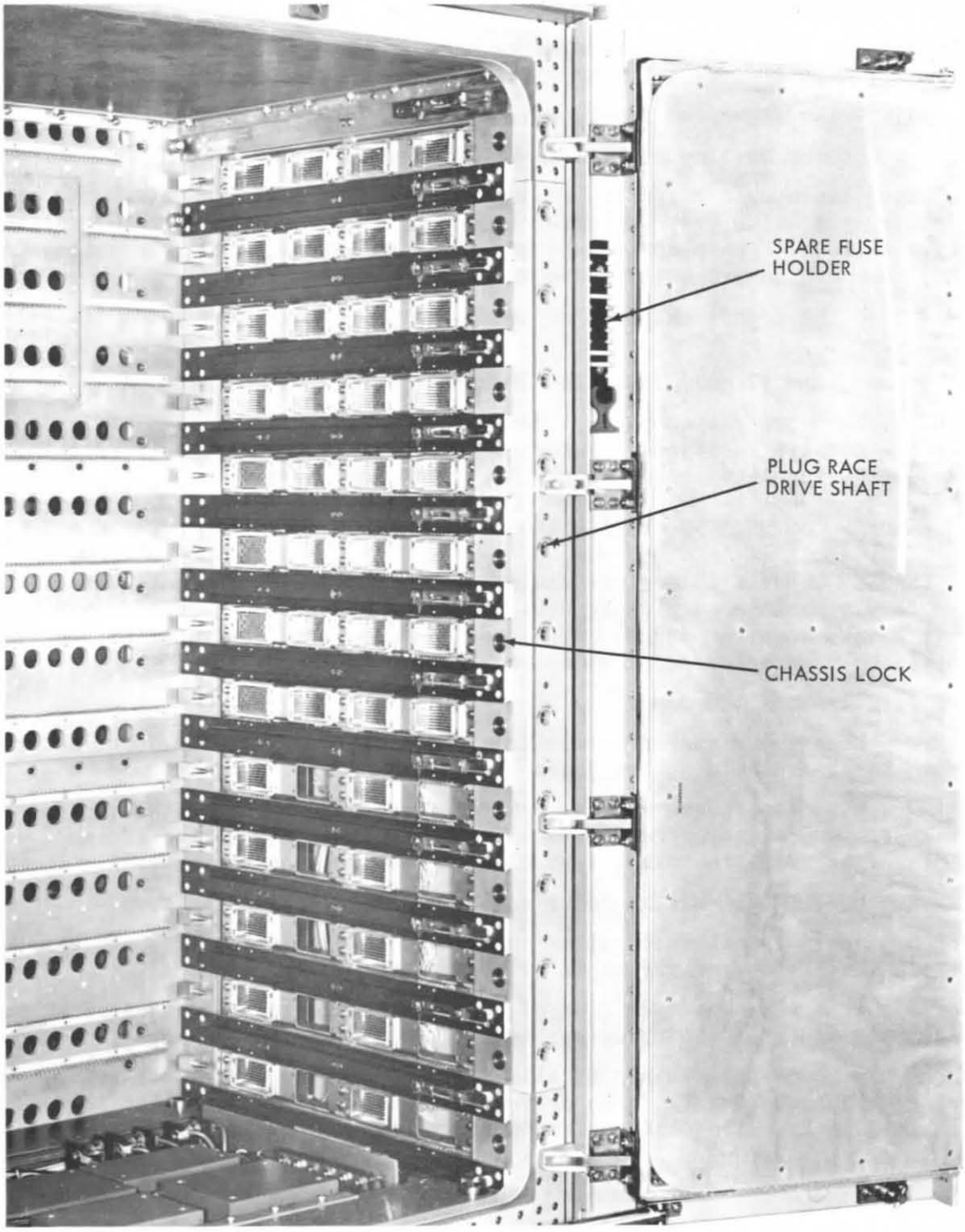


Figure 6-16. Chassis Removal Mechanisms

STEP 1. Release the module hold-down strips.

STEP 2. Remove the module. A gentle, rocking motion will ease removal.

NOTE

The sense amplifiers on chassis A8 have a small, three conductor connector that must be disconnected for removal of the module. It must likewise be reconnected when a new module is inserted.

STEP 3. Replace the module with a known good module.

STEP 4. Secure the module hold-down strips.

STEP 5. Replace the chassis in the computer.

All the module assemblies in the computer and their location on the chassis are color coded according to type number. The colors on the top edge of each card give the last four digits of the module type. The color code used is the standard JAN resistor code. For example, a 2010 module is color coded red, black, brown, and black. A 2030 module is color coded red, black, orange, and black. In this way a cross check can be made between the chassis maps, the functional schematics, and the computer chassis to ensure the correct placement of module assemblies. The figures at the end of this section contain all module schematics and component layouts.

c. REPLACEMENT OF MOVABLE CHASSIS CONNECTORS. - The procedure for replacing the movable chassis connectors is as follows:

STEP 1. Remove the affected chassis (see paragraph 6-3a).

STEP 2. Loosen the 36 screws holding the side panel covering the connector and remove the panel.

STEP 3. With a long nose pliers remove and tag each wire of the connector.

STEP 4. Remove the four screws and nuts holding the connector to the plug rack and remove the connector.

STEP 5. Replace the connector, and reassemble in the reverse order.

d. REPLACEMENT OF CONSOLE POWER SUPPLY PARTS AND ASSEMBLIES. - The power supply for the console indicators is located behind the console panel. Except for transformer T1, the parts in the power supply can be replaced without removing the console power supply chassis from the computer. Transformer T1 is bolted to the chassis from the bottom; therefore, the power supply chassis must be removed to replace T1. Replacement of parts other than transformer T1 is as follows:

STEP 1. Remove power to the computer by disconnecting the input power cables.

STEP 2. Loosen the four screws on the console cover.

STEP 3. Remove the six screws on each side and the 12 screws on the top of the console shroud.

STEP 4. Fold the console cover back over the top, and lift off the console shroud.

STEP 5. Loosen the seven screws holding the console panel and swing the panel down.

STEP 6. Pull out the plugs connected to the back panel in the area of the part to be replaced. Pull the cables forward giving access to the faulty parts.

STEP 7. Remove and tag the wires on the part.

STEP 8. Replace the faulty part, and reassemble in the reverse order.

e. REPLACEMENT OF INPUT/OUTPUT JACKS.

STEP 1. Turn off the computer.

STEP 2. Remove the four screws holding the connector retainer, and pull the connector up and away from the surface.

STEP 3. With a long nose pliers, carefully pull out the wires and tag each wire with the corresponding pin designation.

STEP 4. Use the insertion tool to replace the taper pins in the new connector.

STEP 5. Replace and fasten the connector.

f. REPLACEMENT OF CONSOLE INDICATORS AND SWITCHES.

STEP 1. Turn off the computer power.

STEP 2. Loosen the four screws on the console cover, and fold the cover back over the top.

STEP 3. Loosen the seven screws (two along each side, and five along the top) holding the console panel, and swing the panel down.

STEP 4. Unsolder the wires, or remove the taper pin connectors from the faulty part, carefully tagging each wire. The pin orientation for the various switches and indicators is illustrated in figure 6-17.

STEP 5. From the front panel, unscrew the nut holding the switch or indicator, and remove the part from the rear.

STEP 6. Replace the part, and reassemble in the reverse order.

g. REPLACEMENT OF C SELECTION SWITCH ASSEMBLY.

STEP 1. Repeat the first three steps of paragraph 6-3f.

STEP 2. Remove the four plugs on the back of the C selection switch assembly to be replaced.

STEP 3. Holding the console panel, remove the chains on the sides of the switch assembly, and carefully lower the panel.

CAUTION

The panel must be supported by some means so that the indicators and/or wires are not damaged.

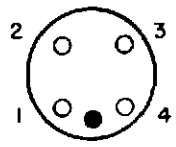
STEP 4. Loosen the Allen set screws, and remove the switch knobs.

STEP 5. Remove the four screws on either side of the switch shafts and the four screws and nuts at the corners of the rectangle formed by the C selection switch area.

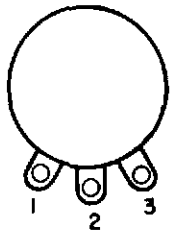
STEP 6. Remove the assembly.

STEP 7. Replace the assembly in the reverse order.

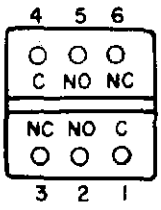
h. MAIN POWER SUPPLY REMOVAL AND REPAIR. - The main power supply is located in the bottom of the cabinet. Except for transformers T1, T2, and T3 and the inductors L1, L2, and L3, which are bolted to the power supply chassis from the bottom,



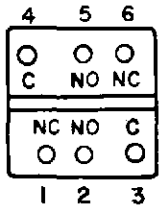
PIN ORIENTATION FOR PUSH-BUTTON SWITCHES AND INDICATORS



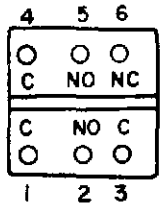
PIN ORIENTATION FOR R1



PIN ORIENTATION FOR S1 & S2



PIN ORIENTATION FOR S15 THRU S18



PIN ORIENTATION FOR S42 THRU S50

Figure 6-17. Console Switches, Diagram of Pin Orientation

the parts and assemblies can be replaced without removing the power supply from the cabinet. Usually the lower six chassis have to be removed to allow sufficient room to work on the power supply. Transformer T1 of assembly A1 is bolted to the bottom assembly plate; therefore, assembly A1 is removed to replace T1. The procedure for removal of the power supply is as follows: (See figure 6-18.)

STEP 1. Remove power to the computer by disconnecting the input power cables.

STEP 2. Remove the lower six chassis according to the procedure in paragraph 6-3a.

STEP 3. Remove and tag the 11 wires going from the power supply to other parts of the computer. There are six connected to TB4, three connected to TB1, one connected to ground stud E1, and one connected to assembly A1.

STEP 4. With a 5/32 inch Allen wrench, remove the 40 cap screws on the periphery of the power supply chassis.

STEP 5. Lift the power supply up and out. Since the power supply weighs approximately 150 pounds, two people are required to lift it out of the cabinet.

STEP 6. Replace the faulty component with a known good component.

STEP 7. Replace the power supply in the reverse order.

i. REPLACEMENT OF CORE STACKS. - The main memory core stacks may be replaced by performing, in order, the following steps. Item numbers refer to callouts on figure 6-19.

STEP 1. Clean a work area and move the memory chassis to the clean area.

STEP 2. Remove the core stack cover (item 1) by removing the 12 screws (item 2) and lifting the cover away from the chassis.

STEP 3. Place the memory chassis on its top and remove the bottom cover plate to expose the wiring.

STEP 4. Disconnect the core stack wiring by unwrapping the wires from the card jack terminals listed in table 6-6. Tag each wire with the card jack coordinates and pin number as listed in table 6-6. When finished, visually inspect the chassis to make certain that all core stack wires have been disconnected from the chassis.

STEP 5. Remove the 12 bolts (item 3) which secure the core stack to the chassis.

STEP 6. The core stack may now be lifted from the chassis.

STEP 7. Install a new core stack by reversing the above procedure.

STEP 8. After installing a new core stack clean the chassis in the area around the stack with a vacuum cleaner and brush to remove ann foreign particles.

STEP 9. Install the chassis in the computer. Apply power to the computer and, by using a 55 test, check to see if any bit positions are failing (refer to paragraph 5-3d(2)(a)(2) for the 55 test).

STEP 10. It may be necessary to readjust the memory following replacement of the core stack. Refer to paragraph 6-2a for adjustment procedures.

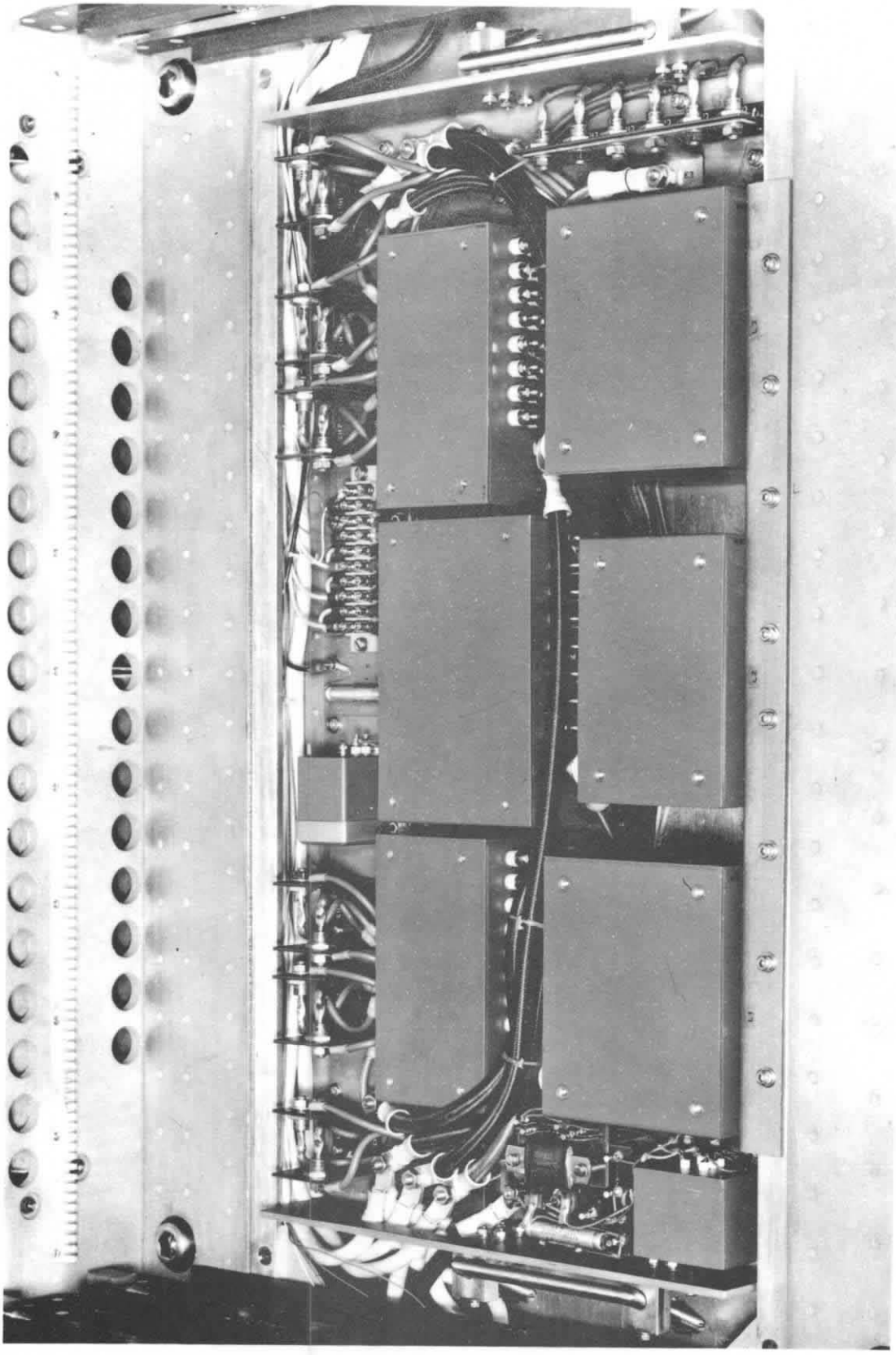
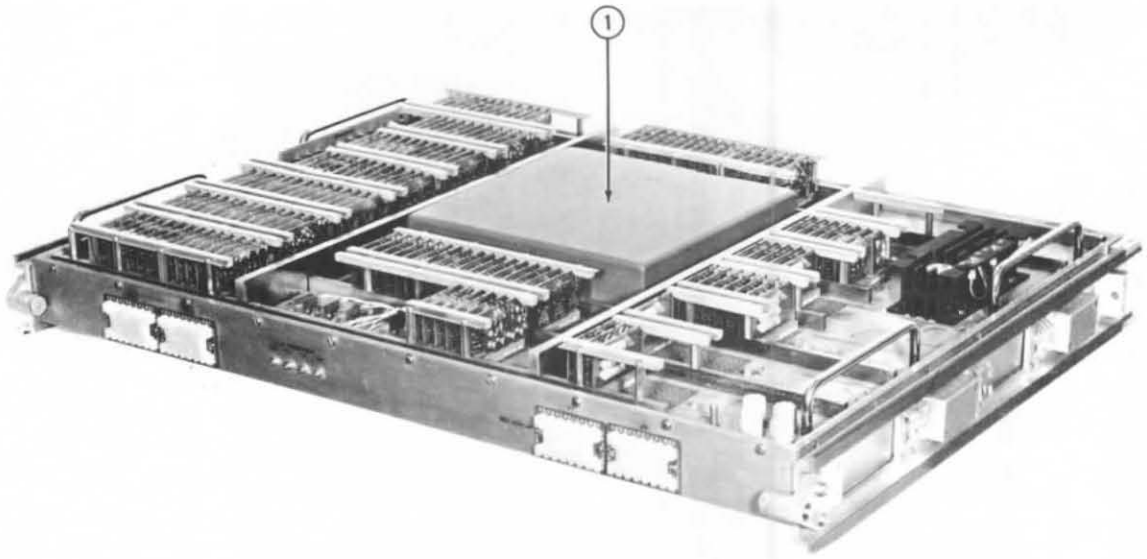


Figure 6-18. Main Power Supply



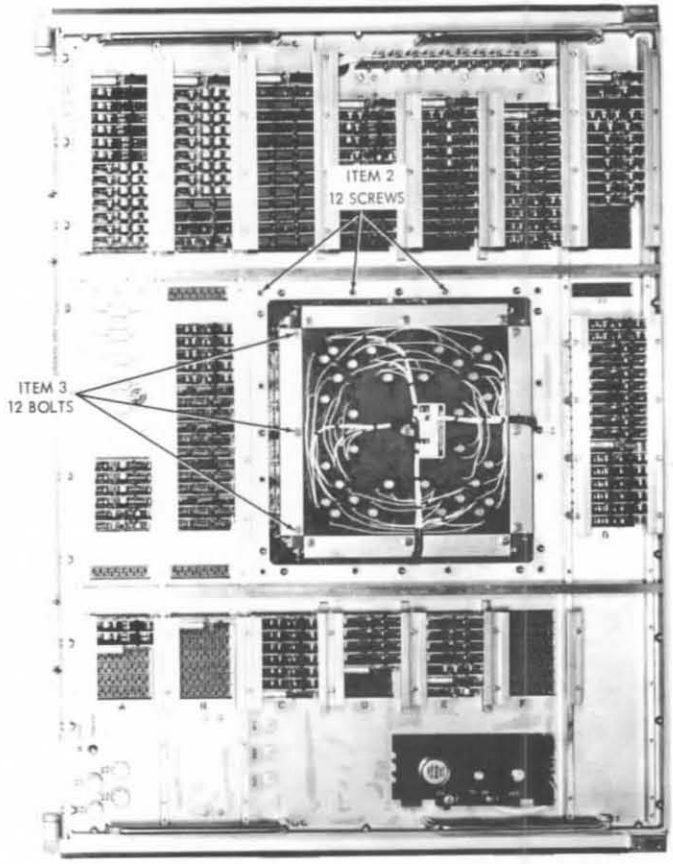


Figure 6-19. Main Memory Chassis, Top and Bottom View

TABLE 6-6. CORE STACK WIRING TERMINATIONS

J 1C- 1	J 7C- 8	J10D- 7	J12C- 9	J14G-12	J21B- 5	J28B- 7	J33C-15
J 1C- 5	J 7C- 9	J10D- 9	J12C-12	J14G-14	J21B- 7	J28G-11	J33D-12
J 1C- 8	J 7C-12	J10E- 5	J12C-13	J14G-15	J21B- 9	J28G-12	J33D-15
J 1C- 9	J 7C-13	J10E- 7	J12D- 5	J15B-11	J21G-12	J28G-14	J33E-12
J 1C-12	J 8C- 1	J10E- 9	J12D- 7	J15B-12	J21G-15	J28G-15	J33E-15
J 1C-13	J 8C- 5	J10F-11	J12D- 9	J15B-14	J22B- 5	J29B- 5	J34C-11
J 2C- 1	J 8C- 9	J10F-12	J12E- 5	J15B-15	J22B- 7	J29B- 7	J34C-12
J 2C- 5	J 8C-12	J10F-14	J12E- 7	J15G-11	J22G-12	J29B- 9	J34C-14
J 2C- 8	J 8C-13	J10F-15	J12E- 9	J15G-12	J22G-15	J29G-11	J34C-15
J 2C- 9	J 8D- 5	J11B- 1	J12F-11	J15G-14	J23B- 5	J29G-12	J34D-12
J 2C-12	J 8D- 7	J11B- 5	J12F-12	J15G-15	J23B- 7	J29G-14	J34D-15
J 2C-13	J 8E- 5	J11B- 8	J12F-14	J16B-11	J23B- 9	J29G-15	J34E-12
J 3C- 1	J 8E- 7	J11B- 9	J12F-15	J16B-12	J23G-12	J30B- 5	J34E-15
J 3C- 5	J 9C- 1	J11B-12	J13B-11	J16B-14	J23G-15	J30B- 7	J35C-11
J 3C- 8	J 9C- 5	J11B-13	J13B-12	J16B-15	J24B- 5	J30B- 9	J35C-12
J 3C- 9	J 9C- 8	J11C- 1	J13B-14	J16G-12	J24B- 7	J30G-11	J35C-14
J 3C-12	J 9C- 9	J11C- 5	J13B-15	J16G-15	J24B- 9	J30G-12	J35C-15
J 3C-13	J 9C-12	J11C- 8	J13C- 1	J17B-11	J25B- 5	J30G-14	J36C-11
J 4C- 1	J 9C-13	J11C- 9	J13C- 5	J17B-12	J25B- 7	J30G-15	J36C-12
J 4C- 5	J 9D- 5	J11C-12	J13C- 8	J17B-14	J25G-11	J31C-11	J36C-14
J 4C- 8	J 9D- 7	J11C-13	J13C- 9	J17B-15	J25G-12	J31C-12	J36C-15
J 4C- 9	J 9D- 9	J11D- 5	J13C-12	J17G-12	J25G-14	J31C-14	J37E-13
J 4C-12	J 9E- 5	J11D- 7	J13C-13	J17G-15	J25G-15	J31C-15	J37E-15
J 4C-13	J 9E- 7	J11E- 5	J13D- 5	J18B-11	J26B- 5	J31D-12	
J 5C- 1	J 9E- 9	J11E- 7	J13D- 7	J18B-12	J26B- 7	J31D-15	
J 5C- 5	J10B- 1	J11F-11	J13D- 9	J18B-14	J26B- 9	J31E-12	
J 5C- 8	J10B- 5	J11F-12	J13E- 5	J18B-15	J26G-11	J31E-15	
J 5C- 9	J10B- 8	J11F-14	J13E- 7	J18G-12	J26G-12	J32C-11	
J 5C-12	J10B- 9	J11F-15	J13E- 9	J18G-15	J26G-14	J32C-12	
J 5C-13	J10B-12	J12B- 1	J13F-11	J19B- 5	J26G-15	J32C-14	
J 6C- 1	J10B-13	J12B- 5	J13F-12	J19B- 7	J27B- 5	J32C-15	
J 6C- 5	J10C- 1	J12B- 8	J13F-14	J19G-12	J27B- 7	J32D-12	
J 6C- 8	J10C- 5	J12B- 9	J13F-15	J19G-15	J27B- 9	J32D-15	
J 6C- 9	J10C- 8	J12B-12	J14B-11	J20B- 5	J27G-11	J32E-12	
J 6C-12	J10C- 9	J12B-13	J14B-12	J20B- 7	J27G-12	J32E-15	
J 6C-13	J10C-12	J12C- 1	J14B-14	J20B- 9	J27G-14	J33C-11	
J 7C- 1	J10C-13	J12C- 5	J14B-15	J20G-12	J27G-15	J33C-12	
J 7C- 5	J10D- 5	J12C- 8	J14G-11	J20G-15	J28B- 5	J33C-14	

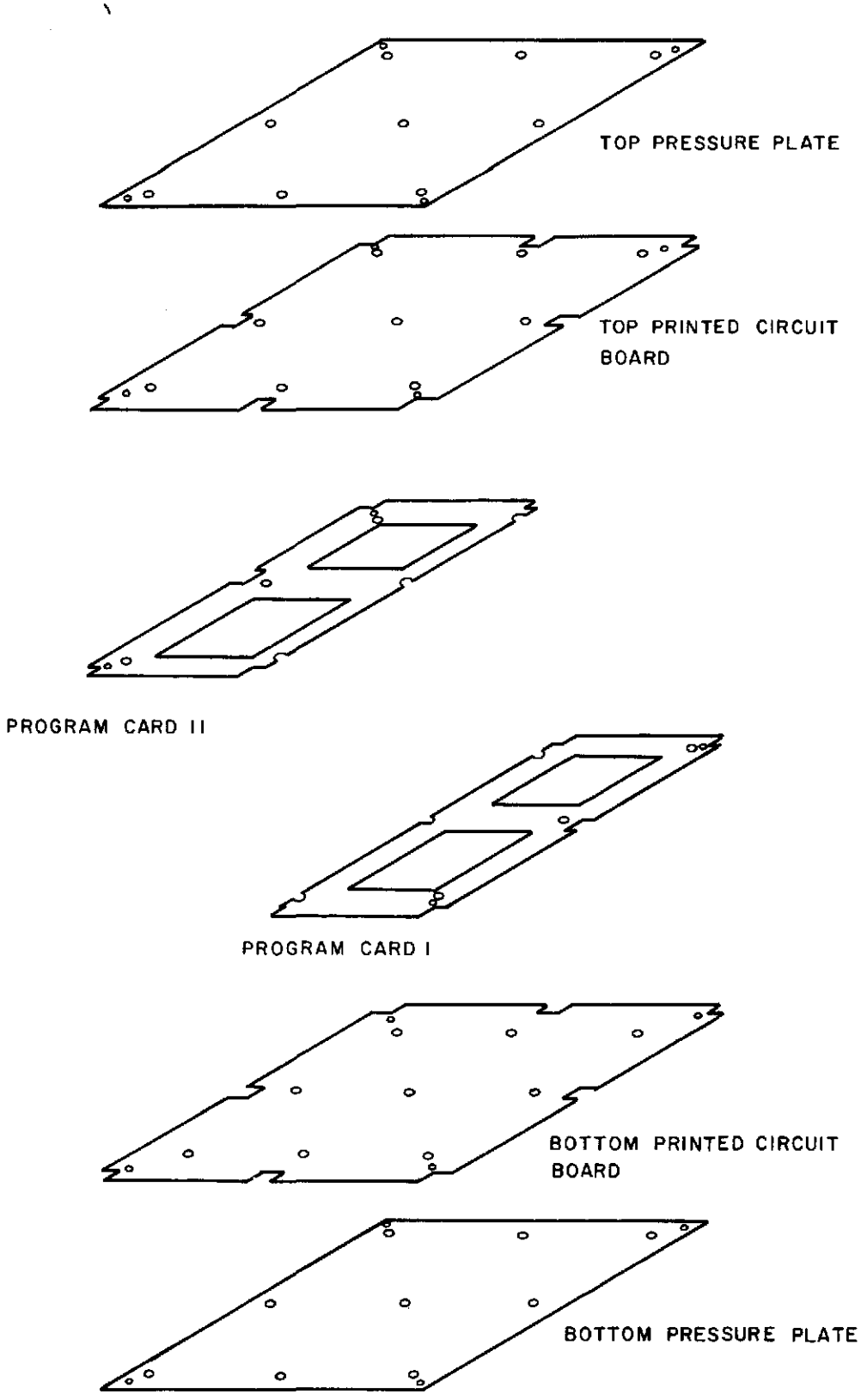


Figure 6-20. Bootstrap Memory Plane

j. REPLACEMENT OF CONTROL MEMORY, THIN-FILM, UNIFLUXOR, OR TRANSFORMER DIODE BOARDS. - The control memory on chassis A8 contains seven planes. The top plane is the bootstrap (Unifluxor) memory. The next four planes are the control memory (thin-film) planes. Below the control memory planes, and accessible from the bottom of the chassis, are two transformer diode boards. The outer transformer diode board selects the bootstrap memory word lines. The inner transformer diode board selects the control memory word lines. The procedure for replacing one of the seven planes is as follows:

STEP 1. Remove the control memory chassis. The removal of a chassis should be done by two people because each logic chassis weighs about 84 pounds and each memory chassis weighs about 60 pounds. Have a clear work area available before removing a chassis. The procedure for removing a chassis is as follows:

STEP 2. Turn off the computer.

STEP 3. Remove the socket wrench from the compartment in the door, and loosen the five fasteners holding the doors closed. Open the doors.

STEP 4. With the square headed socket and rachet, turn the two connector release shafts, on either side of the chassis (in the sides of the cabinet) in the OPEN direction until the plugs have cleared the jacks on the chassis.

STEP 5. Loosen the chassis locks on both sides of the chassis.

STEP 6. Apply the chassis puller tools over the chassis locks, and carefully slide the chassis out as far as it will go.

STEP 7. With a man on each side of the chassis, depress the chassis release rods on both sides of the chassis. Remove the chassis to the work area.

STEP 8. Replace the chassis by sliding it into the proper slot; secure the chassis locks, and turn the plug drive shafts until firm connection is made with the chassis jacks. The chassis is now operational.

NOTE

Securing the chassis locks first will ensure that the chassis jacks and side plugs will mate properly.

STEP 9. Remove the 10 screws holding the top memory cover and the eight screws holding the bottom memory cover; remove the covers.

STEP 10. Remove the six connector hold-down bolts and nuts from the connectors facing the sides of the chassis.

(1) BOOTSTRAP OR CONTROL MEMORY PLANE REPLACEMENT.

STEP 1. Remove the two connector bolts from the connectors facing the front and back of the chassis.

STEP 2. Carefully remove the plug connectors from the periphery of the planes, down to and including the plane to be removed.

STEP 3. Remove the four nuts and washers from the corners of the stack.

STEP 4. Lift the bootstrap memory plane up and off the rods. (If this is the plane to be replaced go to step 7.)

STEP 5. Remove the four nuts from the corners of the stack.

STEP 6. Lift the required number of control memory planes and spacers up and off the rods.

STEP 7. Replace the plane, and reassemble in the reverse order.

NOTE

Torque the plane hold-down nuts to 30 ±3 inch-ounces.

CAUTION

Do not over-torque the connector hold-down bolts.

(2) TRANSFORMER DIODE BOARD REPLACEMENT.

STEP 1. With the bottom of the chassis facing up, remove the four connector hold-down bolts.

STEP 2. Carefully remove the plug connectors from the periphery of the boards.

STEP 3. Remove the four nuts and washers from the corners of the stack.

STEP 4. Lift the boards up and off the rods.

STEP 5. Replace the board, and reassemble in the reverse order.

NOTE

Torque the plane hold-down nuts to 30 ±3 inch-ounces.

CAUTION

Do not over-torque the connector hold-down bolts.

k. REPLACEMENT OF THE BOOTSTRAP MEMORY PROGRAM ELEMENTS. - The bootstrap memory is made so that the two program elements contained within the memory plane can be replaced. Figure 6-20 illustrates the bootstrap memory plane. The procedure for replacing the program elements is as follows:

STEP 1. Remove the bootstrap memory plane in the manner described in paragraph 6-3j.

STEP 2. Place three strips of masking tape over the three rows of sleeve nuts on the bottom of the memory plane. This prevents the nuts from coming out when the screws are removed.

STEP 3. Lay the plane on its bottom surface, and remove the nine screws from the top plane.

STEP 4. Remove the top pressure plate.

STEP 5. Push the sleeve nuts down far enough so that the top printed circuit board and the program elements can be removed.

STEP 6. Remove the top printed circuit board and program elements, and separate them by getting a fingernail between the two surfaces. (The surfaces are held together by a tacky adhesive on the corners.)

STEP 7. Push the sleeve nuts up to their normal position.

STEP 8. Place the new program elements on the plane, and push them down over the sleeve nuts.

STEP 9. Apply a polyester type adhesive (EI Dupont de Nemours & Co. Type IV adhesive) to the corners of the program element.

STEP 10. Place the top printed circuit board on the plane, and push it down over the sleeve nuts.

STEP 11. Place the top pressure plate on the plane, and replace the nine screws.

STEP 12. Remove the masking tape from the bottom of the plane.

1. WIRE-WRAP REPAIR TECHNIQUES.

STEP 1. After locating the wire to be replaced, mark its routing (or draw a sketch of it) because the new wire must take the same path.

STEP 2. Use the proper unwrapping tool to remove the ends of the wire. If the defective wire is wrapped below another wire, the upper wire must also be replaced, so mark its route for exact replacement.

STEP 3. Strip replacement wire with an automatic stripping machine whenever possible; however, hand stripping tools with die type blades, such as "Ideal Strip Machine" or equivalent, can be used.

NOTE

Do not use wire strippers with "V" type blades.

STEP 4. Place routing bullets or spacers over the via terminals to eliminate shorting and tight wires, when forming wire patterns.

STEP 5. Use a non-metallic pointed rod to move adjacent wires from the terminal to be wrapped, when installing wires in a previously wrapped area.

STEP 6. Select proper gun, bit, and sleeve.

STEP 7. Insert stripped end of wire in wire slot provided in the wrapping bit. (When bit is used to produce a "Modified Wrap", a portion of wire insulation also must be inserted into the slot.) Bend wire into insulation relief which is located on a side of the sleeve.

STEP 8. Squarely place wrapping gun over terminal and squeeze the trigger.

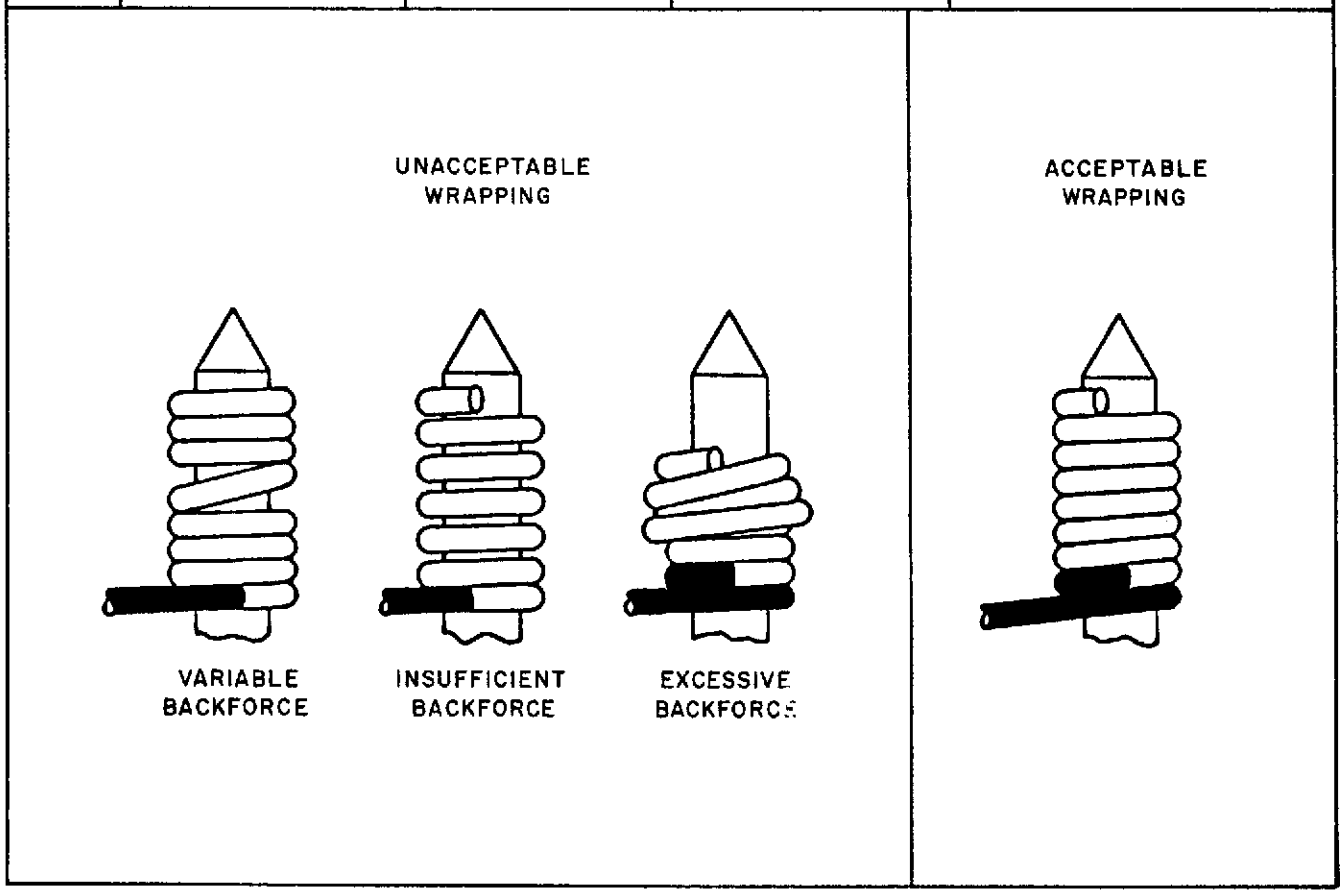
NOTE

Only a momentary squeeze on the trigger is necessary to complete the connection.

To produce acceptably wrapped connections, the back force (pressure exerted by the operator in opposition to the wire wrapping around the terminal) should be approximately one to 1-1/2 pounds; however, this is acquired with experience only. Table 6-5 shows acceptable and unacceptable connections.

TABLE 6-5. WIRE WRAPPING INFORMATION

Wire Guage	Pin Dimension	Strip Length (Inches)	Turns of Bare Wire	Turns of Insulation on Modified Wraps
30	0.025 x 0.025	1-1/8 + 1/8 - 0	8	1/2 to 2
30	0.035 x 0.050	1-5/8 + 1/8 - 0	8	1/2 to 2
26	0.035 x 0.050	1-1/2 + 1/8 - 0	6	1/2 to 2
24	0.035 x 0.050	1-1/3 + 1/8 - 0	5	1/2 to 2
22	0.035 x 0.050	1-1/4 + 1/8 - 0	5	1/2 to 2
20	0.035 x 0.050	1-1/4 + 1/8 - 0	4	1/2 to 2



6-4. OVERALL SCHEMATIC DIAGRAM

The functional schematics in Section 8 together with the wire tabulations in Section 9 and the module schematics in paragraph 6-5 serve as the overall schematic.

6-5. MODULE SCHEMATICS.

Figures 6-21 through 6-152 present the electrical schematics and component layouts for each type of printed circuit module used in the computer. These printed circuit modules are considered non-repair items, and the schematics and component layouts are provided to aid in understanding the overall computer concept.

NOTE

Reference designators are abbreviated. Prefix the designation with the unit number or assembly designation or both.

Component ratings unless otherwise specified:

Resistors: Ohms ±5%, 1/4 Watt
Capacitors: Microfarads +30% - 10%, 50V

 Used on all diodes; band indicates cathode.

Module type numbers are abbreviated. For solder-plated connector prefix the type number with 700. For gold-plated connectors prefix the type number with 422 except the 0210, 1110, 1120, and 1200 types which are prefixed with 25.

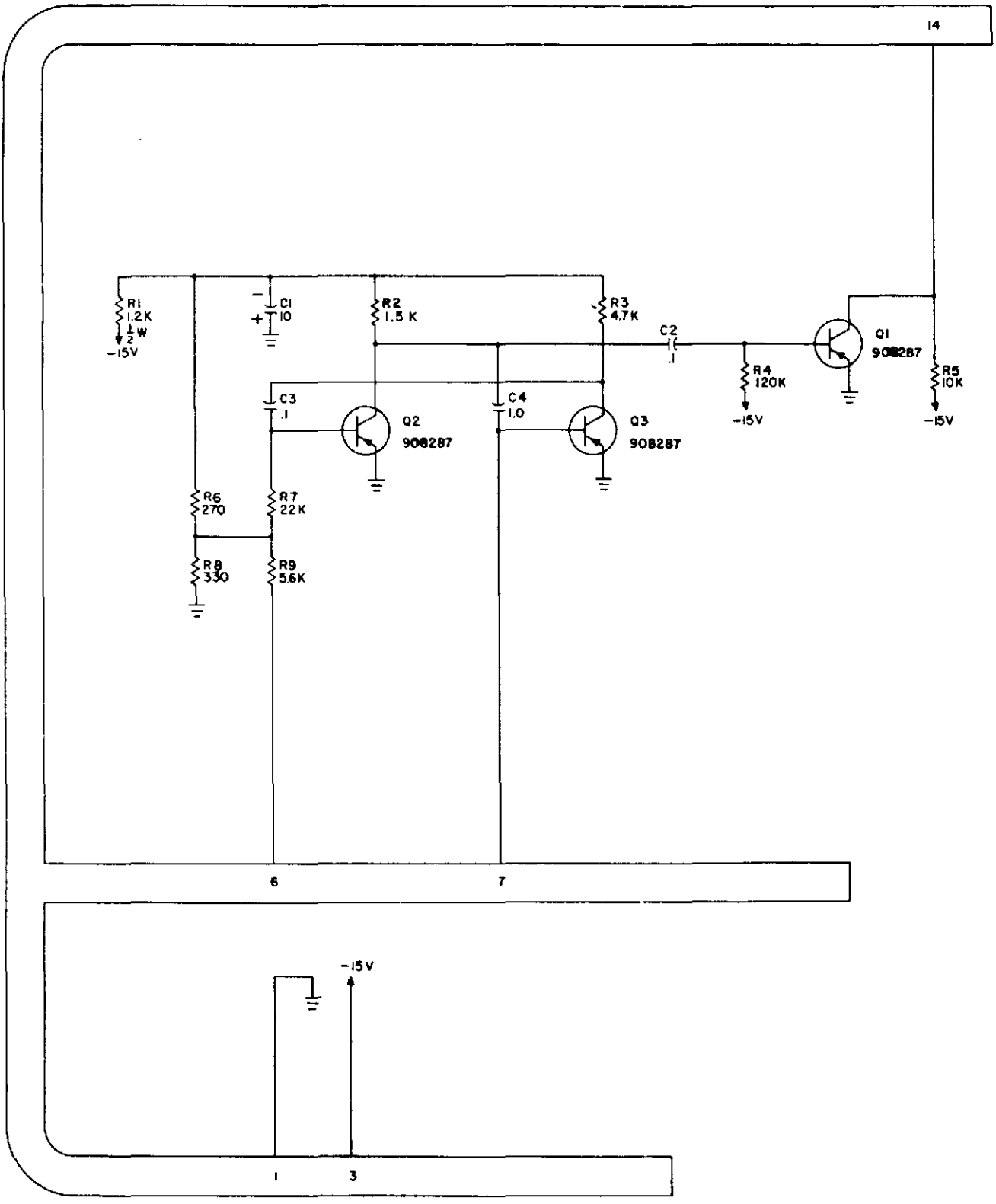


Figure 6-21. Low Speed Variable Oscillator, Module Type 0210, Electrical Schematic

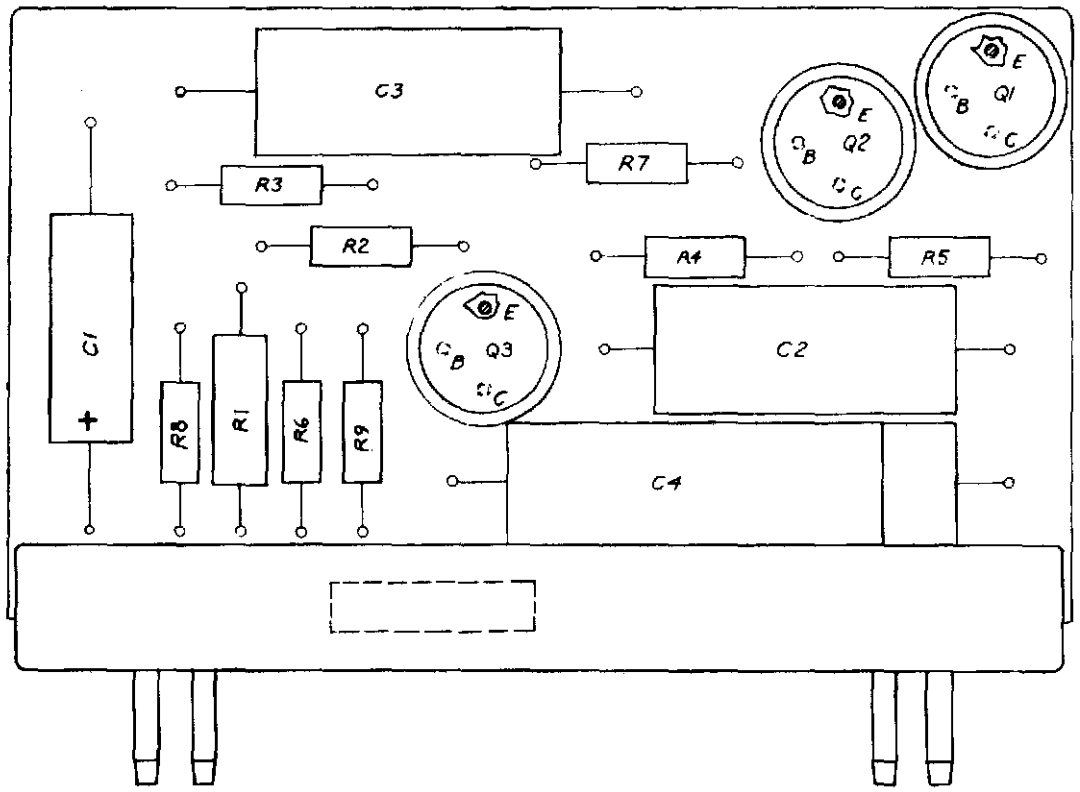


Figure 6-22. Module Type 0210 Component Layout

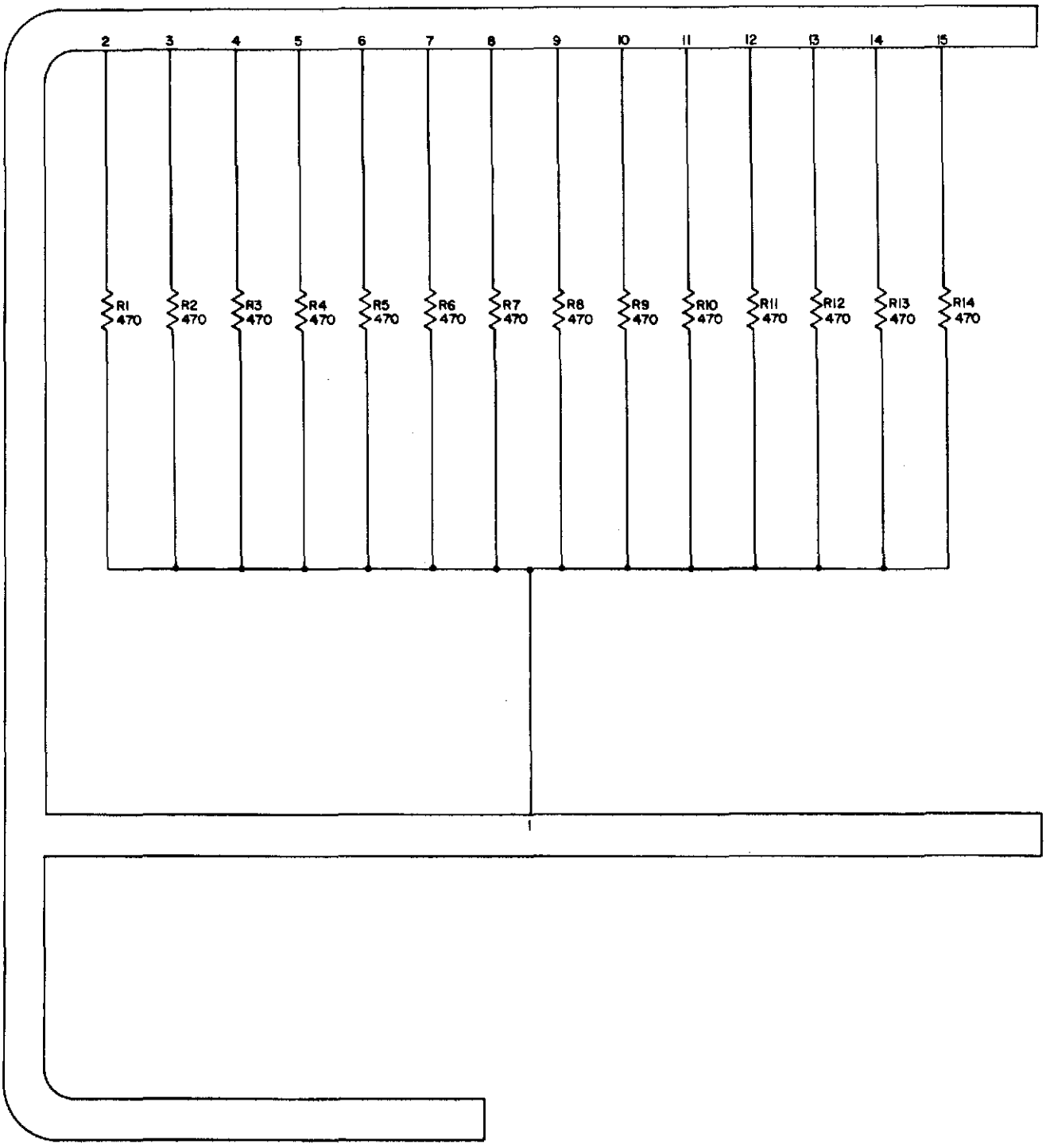


Figure 6-23. Resistor Assembly #6, Module Type 1110, Electrical Schematic

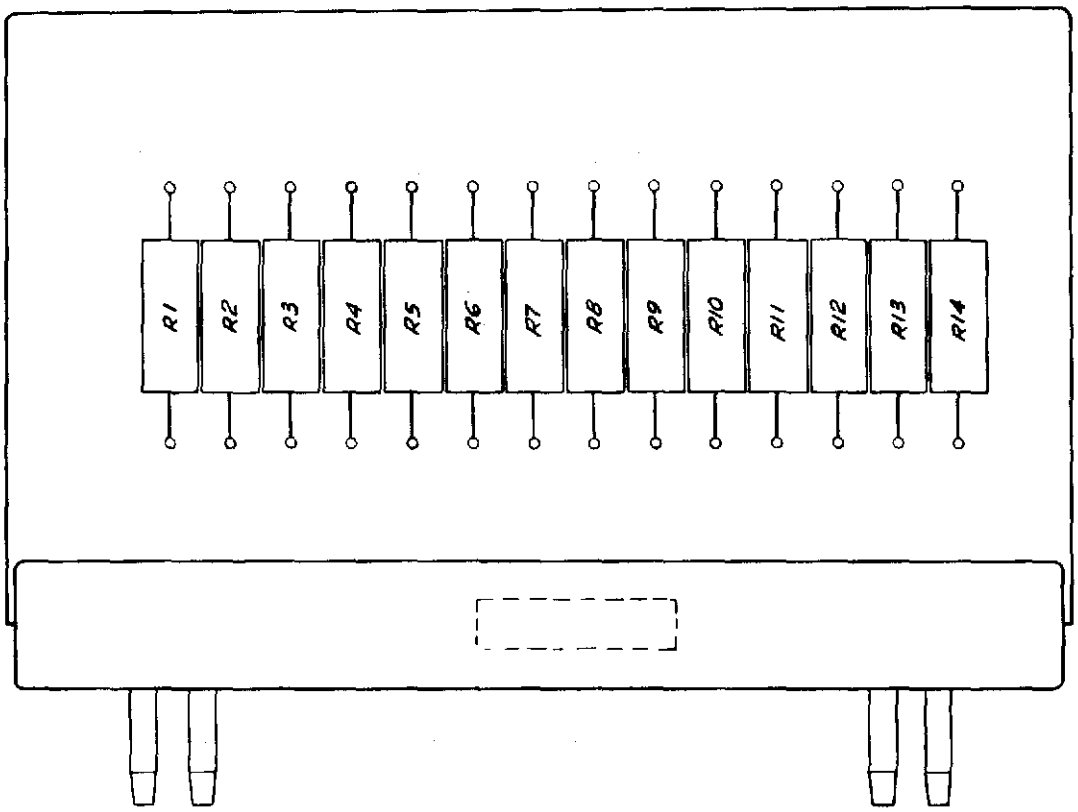


Figure 6-24. Module Type 1110 Component Layout

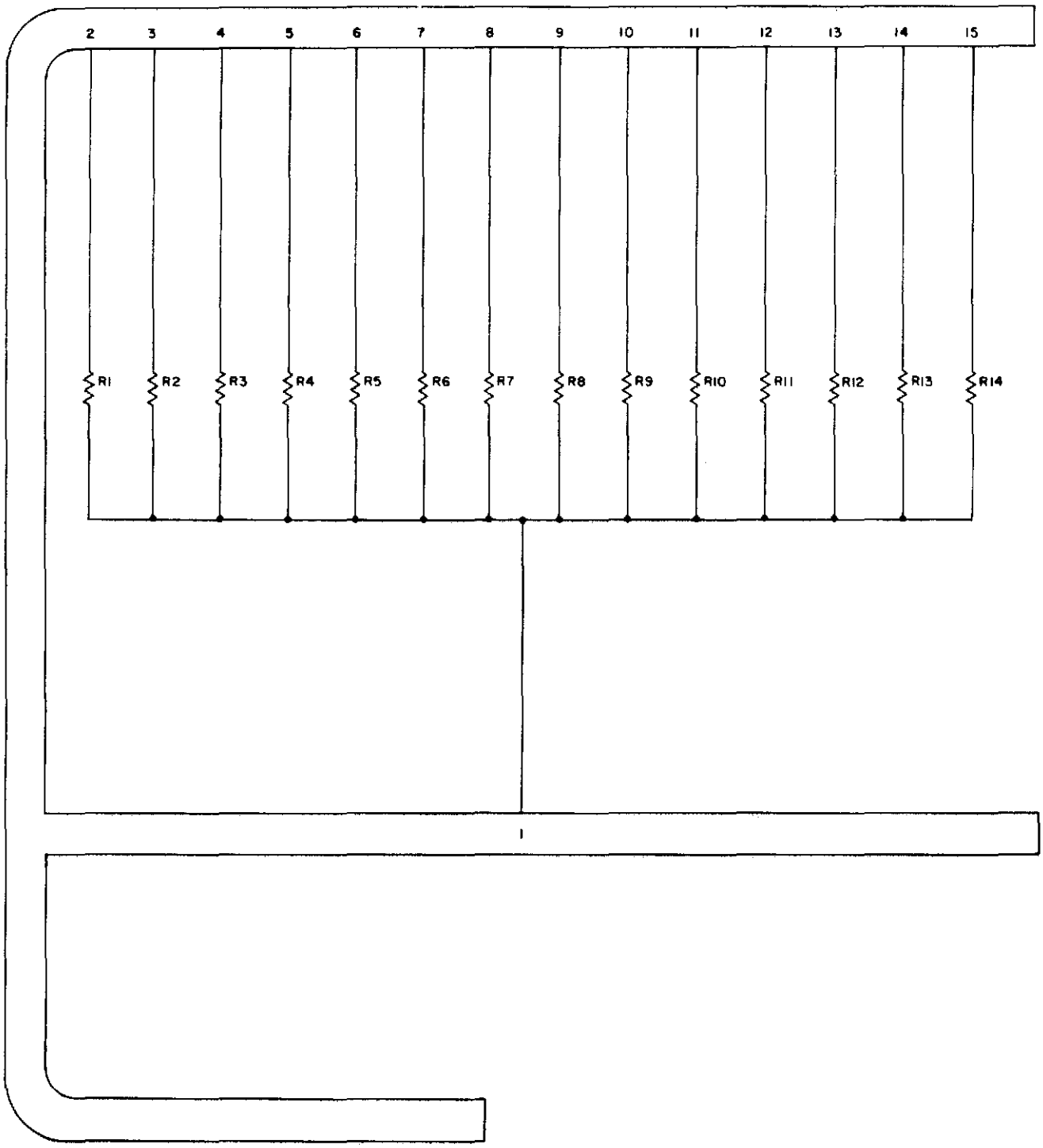


Figure 6-25. Resistor Assembly #7, Module Type 1120, Electrical Schematic

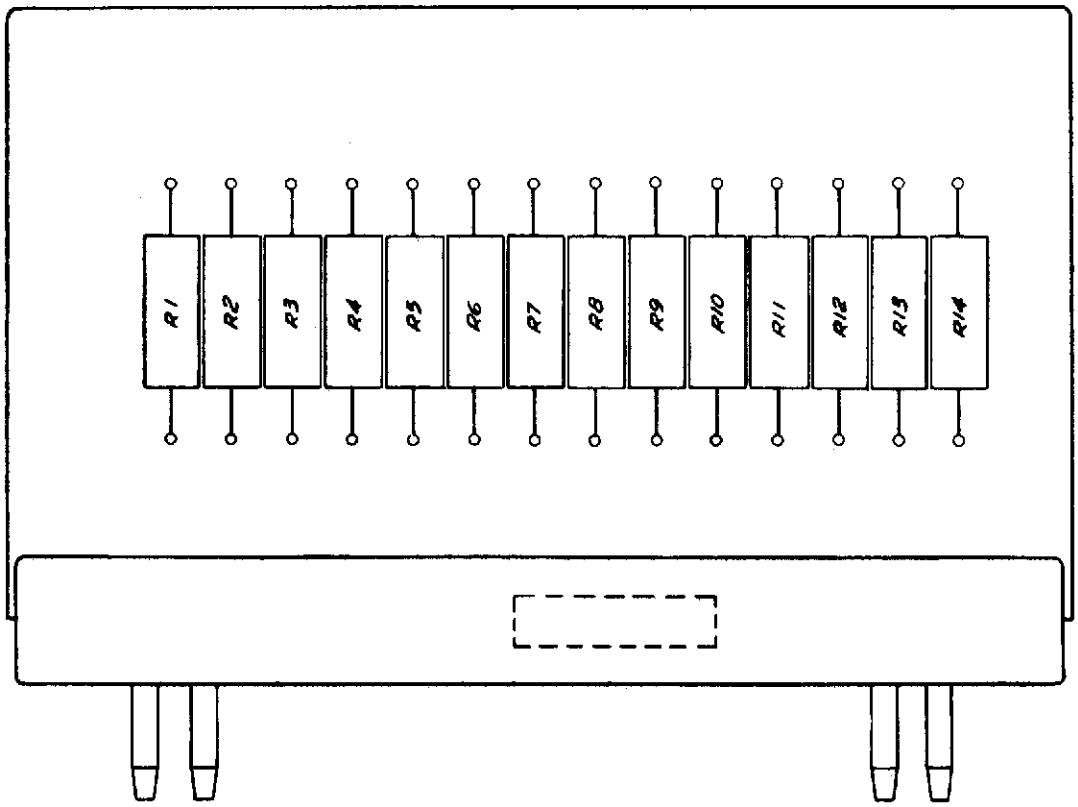


Figure 6-26. Module Type 1120 Component Layout

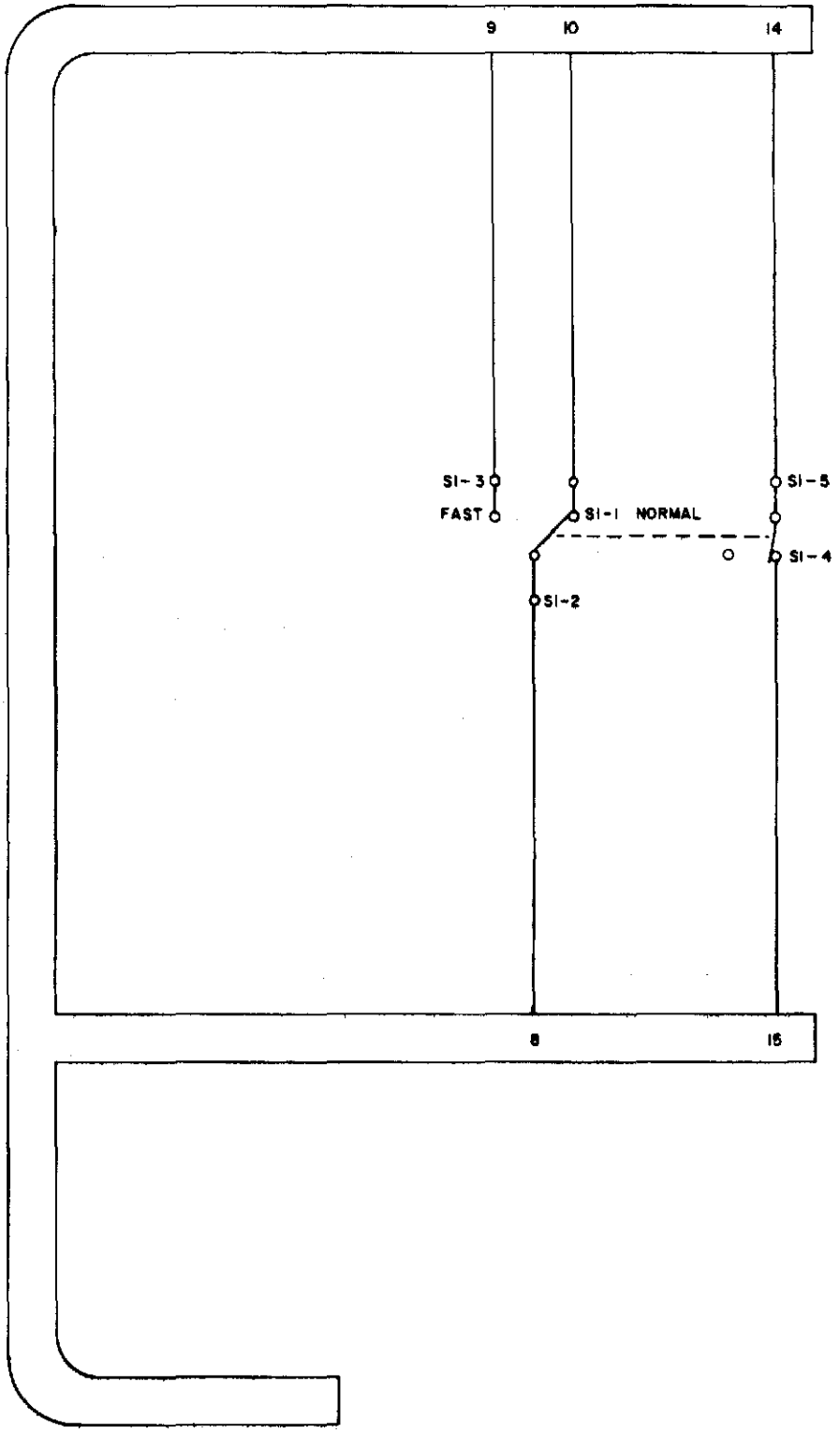


Figure 6-27. Fast/Normal Clock Selector Switch Unit, Module Type 1200, Electrical Schematic

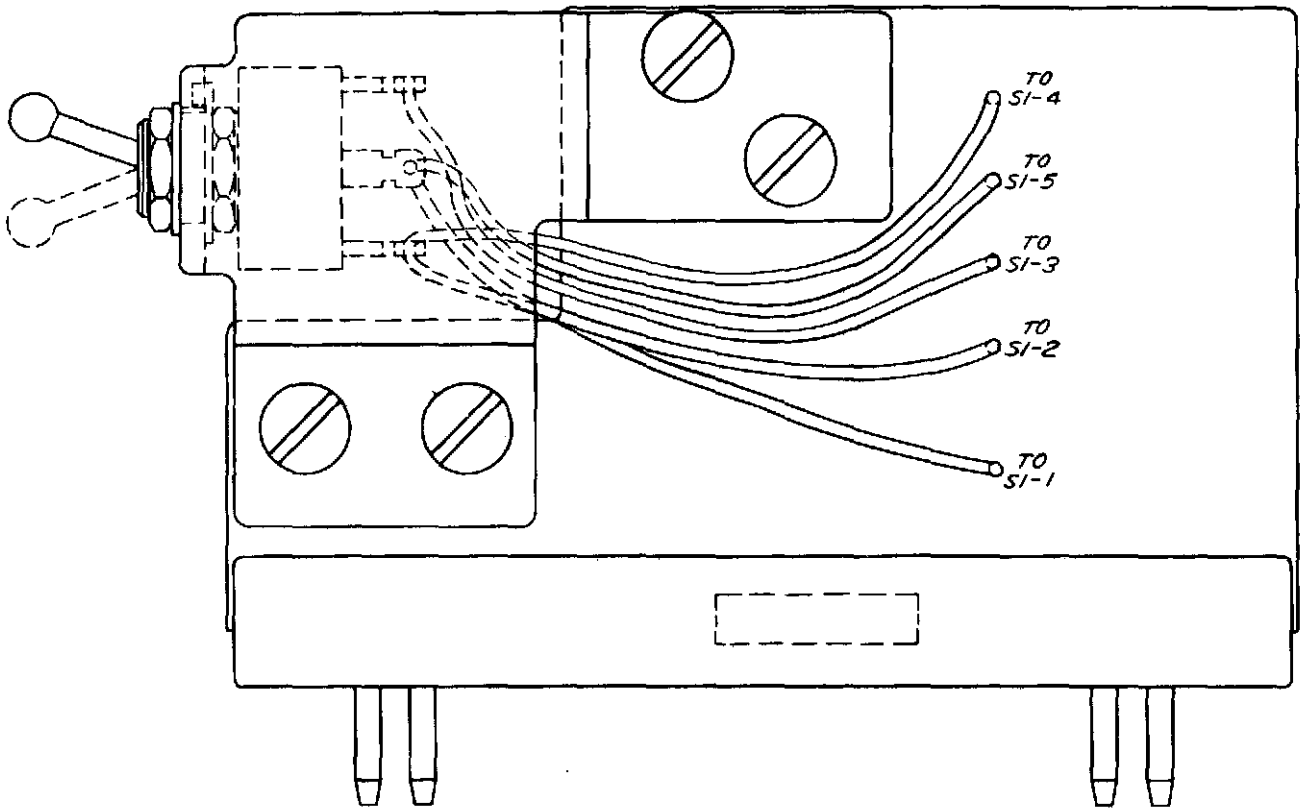


Figure 6-28. Module Type 1200 Component Layout

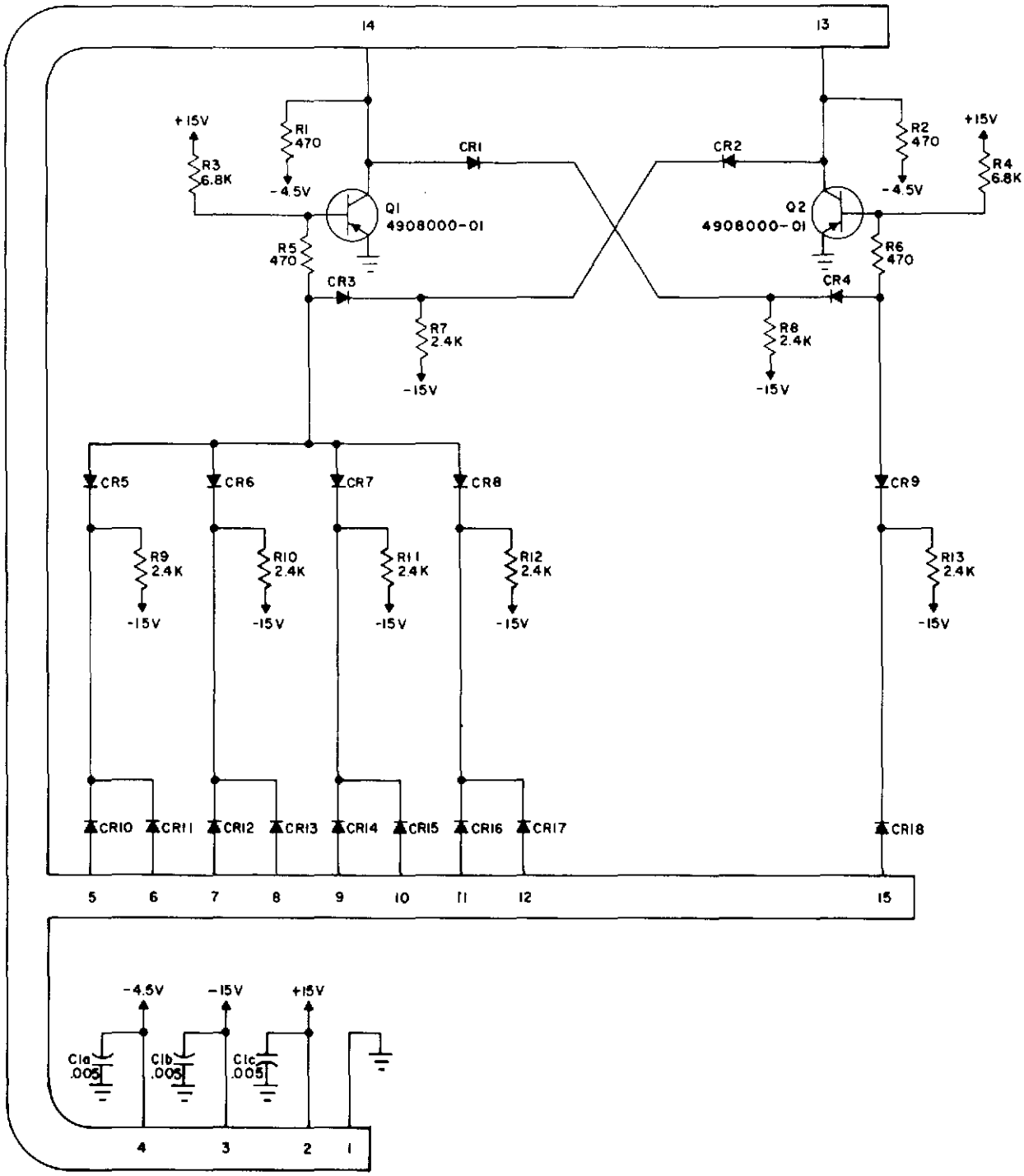


Figure 6-29. Flip-Flop, Module Type 2000, Electrical Schematic

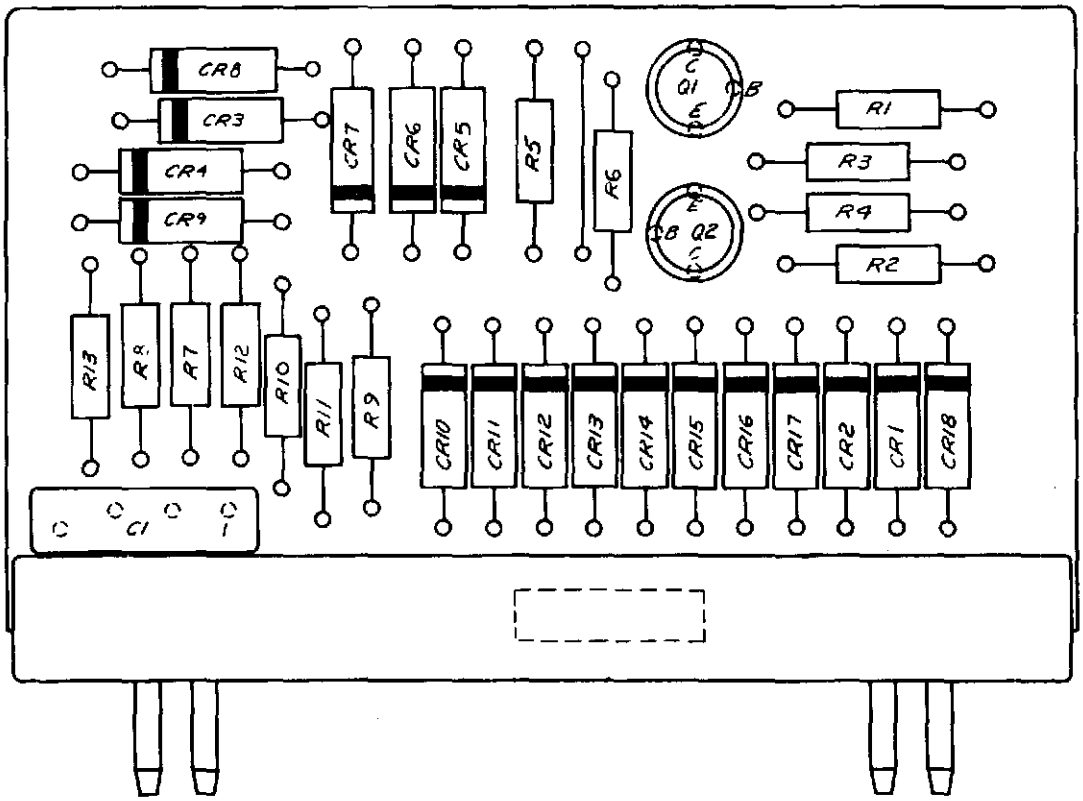


Figure 6-30. Module Type 2000 Component Layout

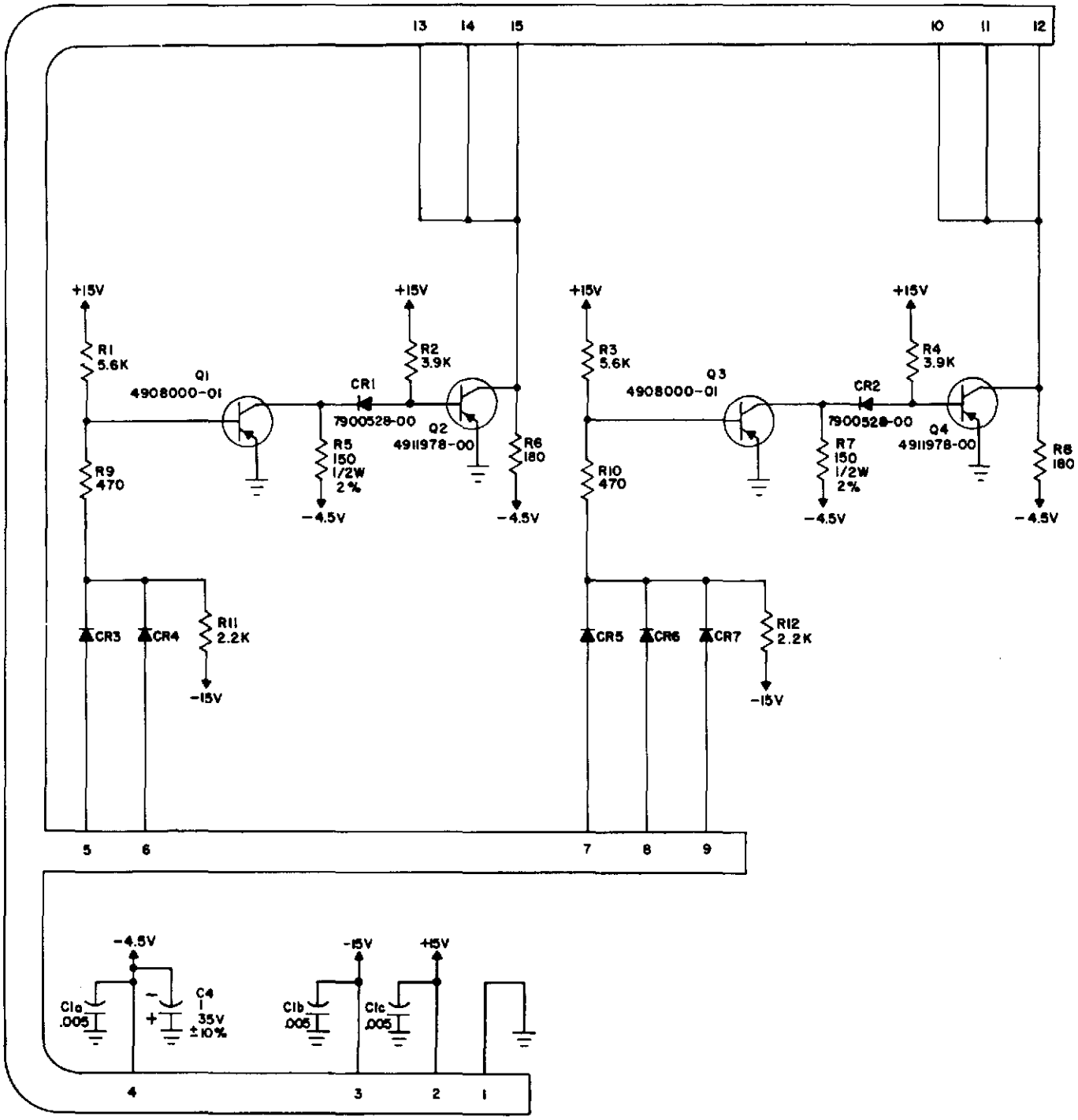


Figure 6-31. Amplifier, Module Type 2011, Electrical Schematic

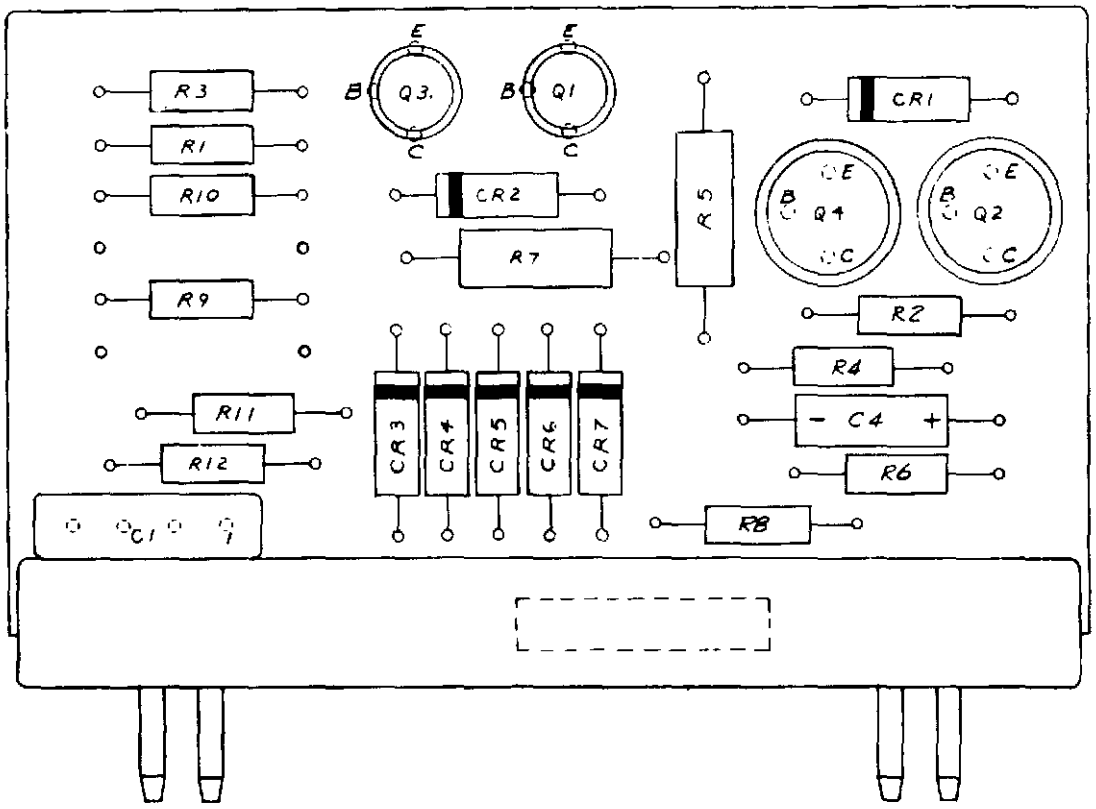


Figure 6-32. Module Type 2011 Component Layout

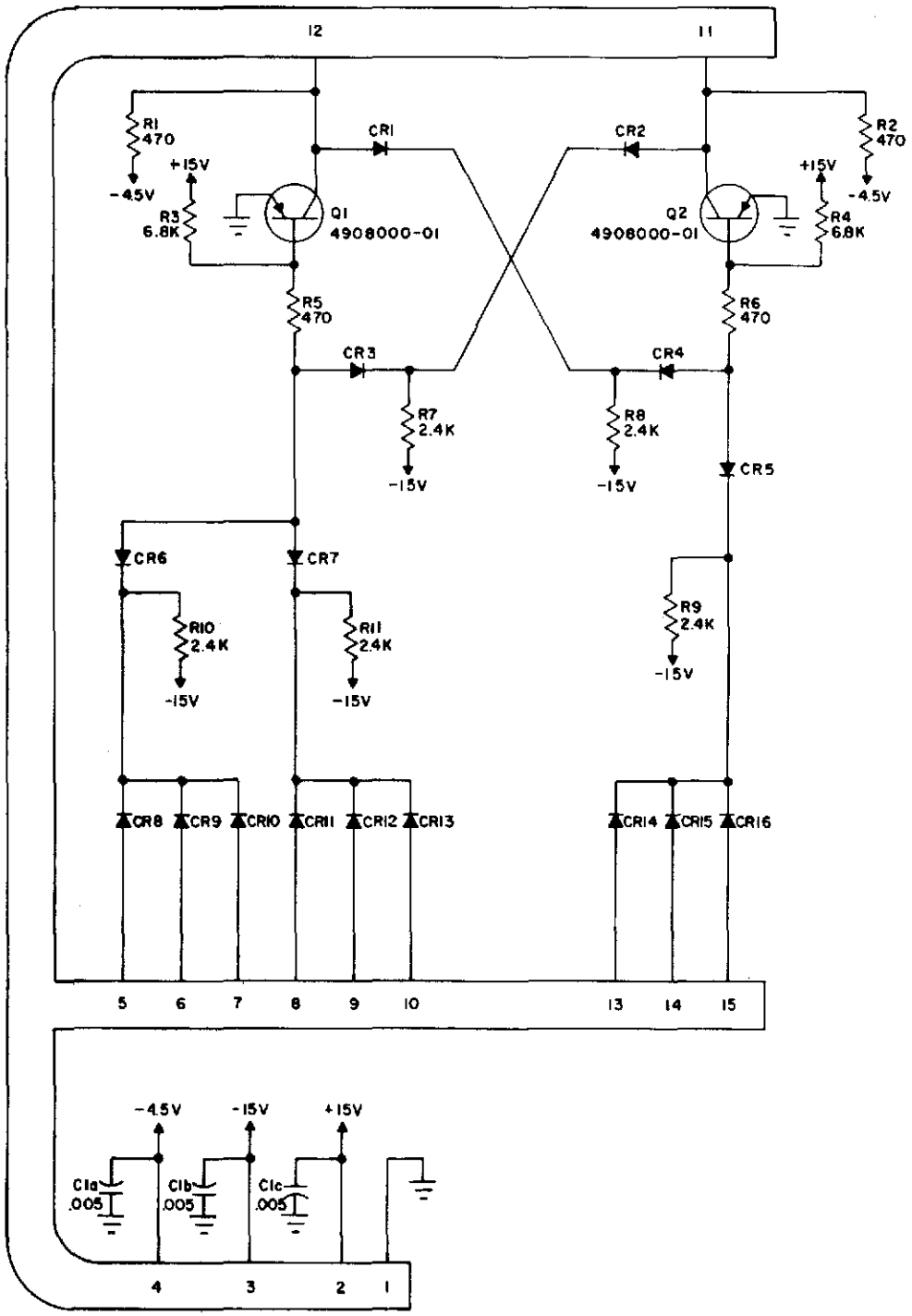


Figure 6-33. Flip-Flop, Module Type 2020, Electrical Schematic

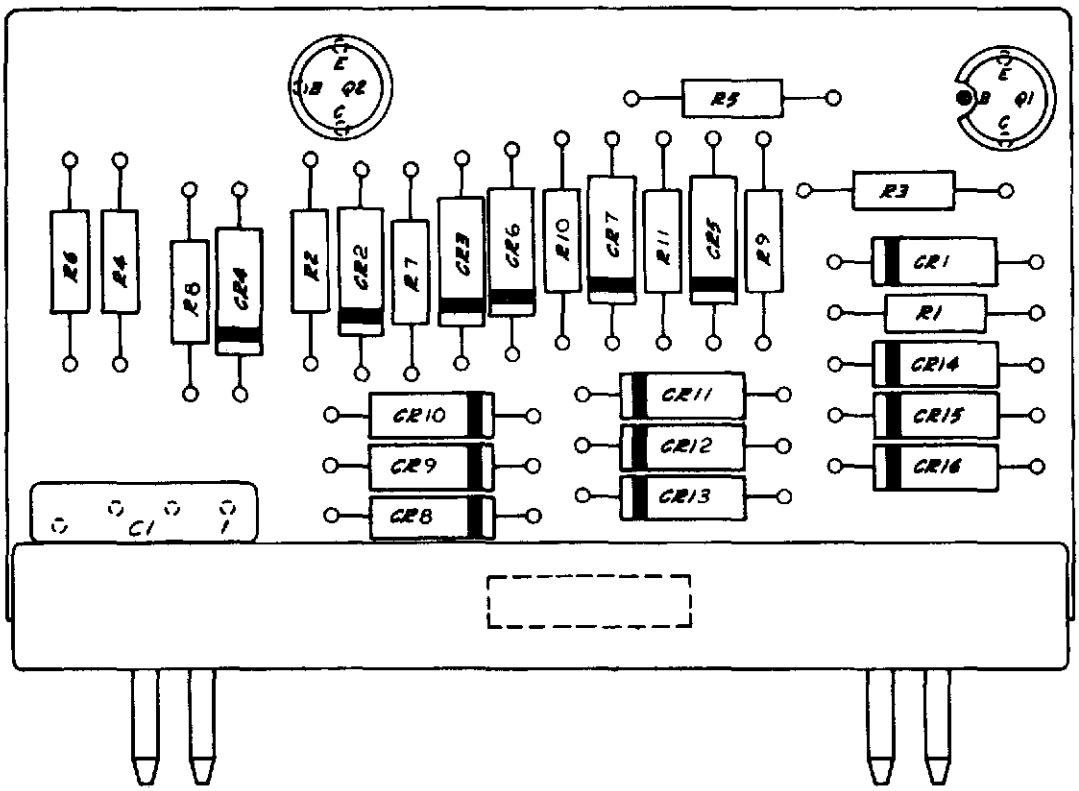


Figure 6-34. Module Type 2020 Component Layout

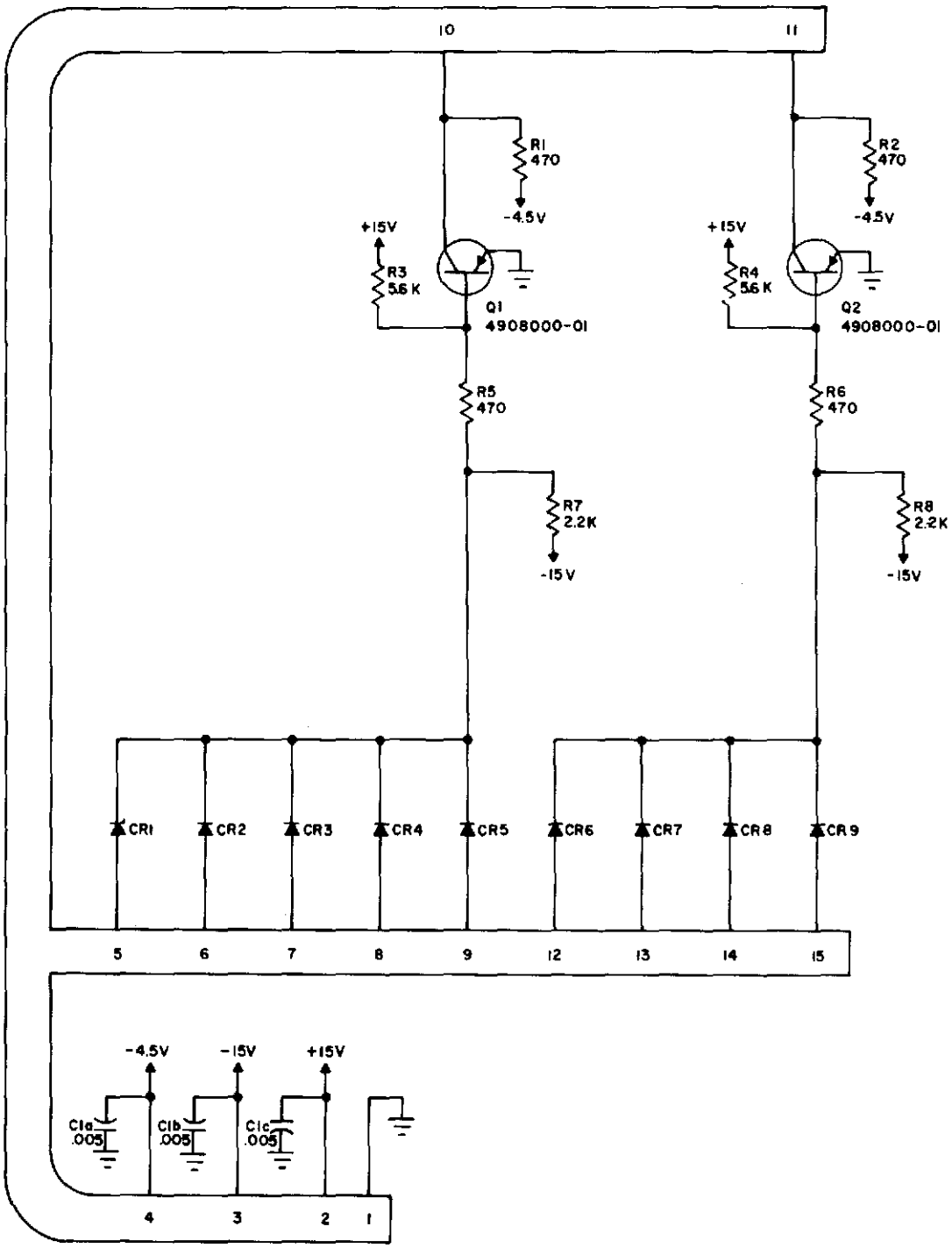


Figure 6-35. Inverter, Module Type 2030, Electrical Schematic

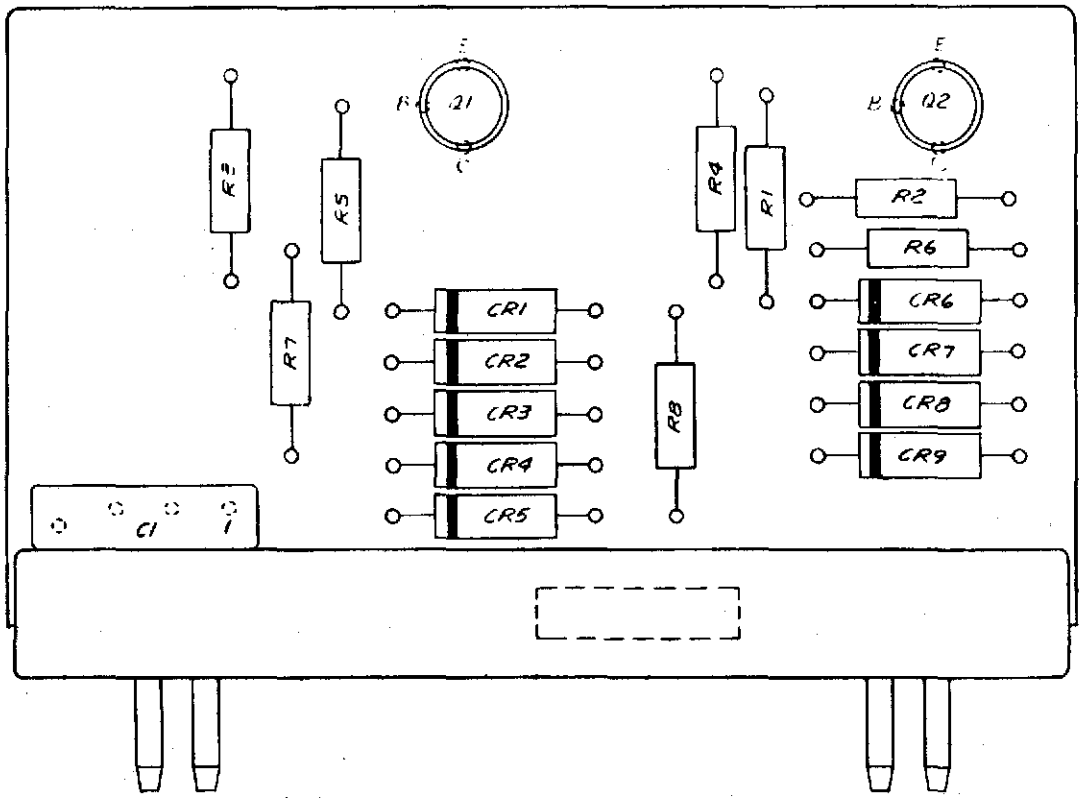


Figure 6-36. Module Type 2030 Component Layout

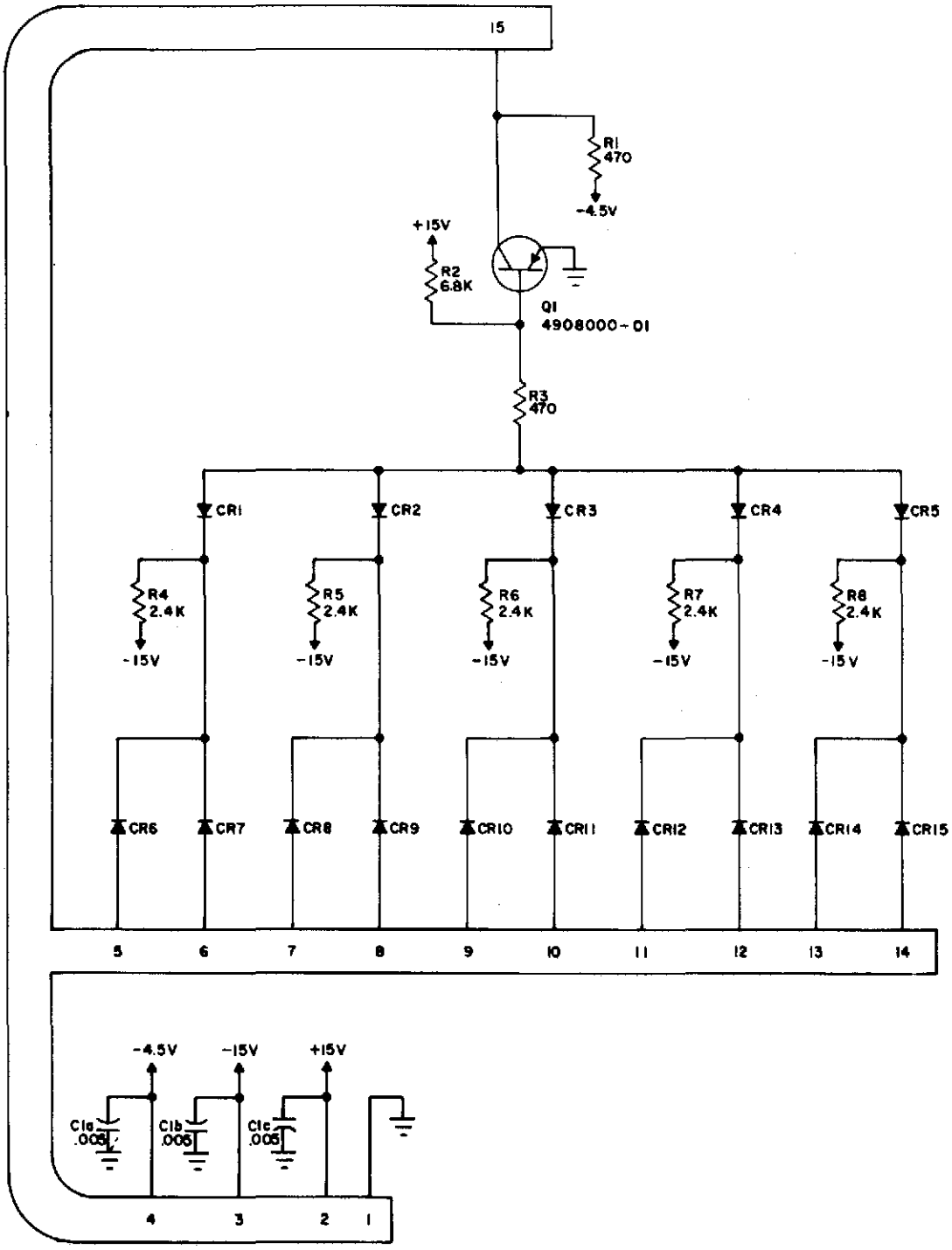


Figure 6-37. Inverter, Module Type 2040, Electrical Schematic

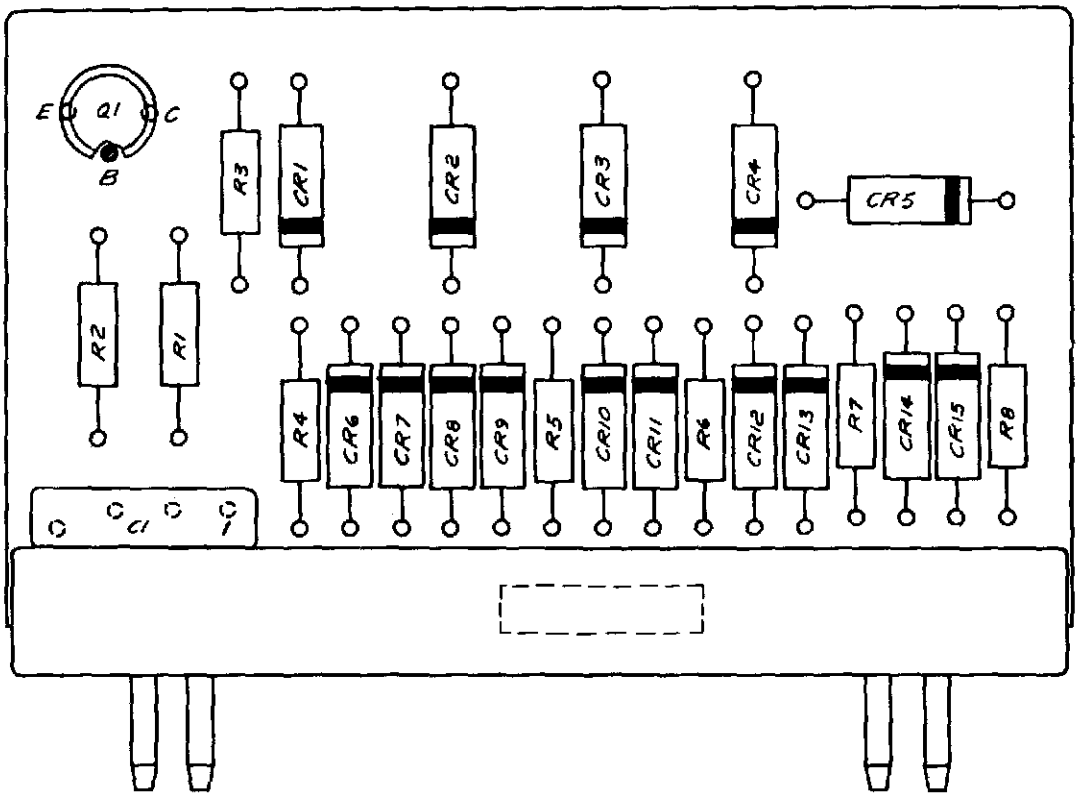


Figure 6-38. Module Type 2040 Component Layout

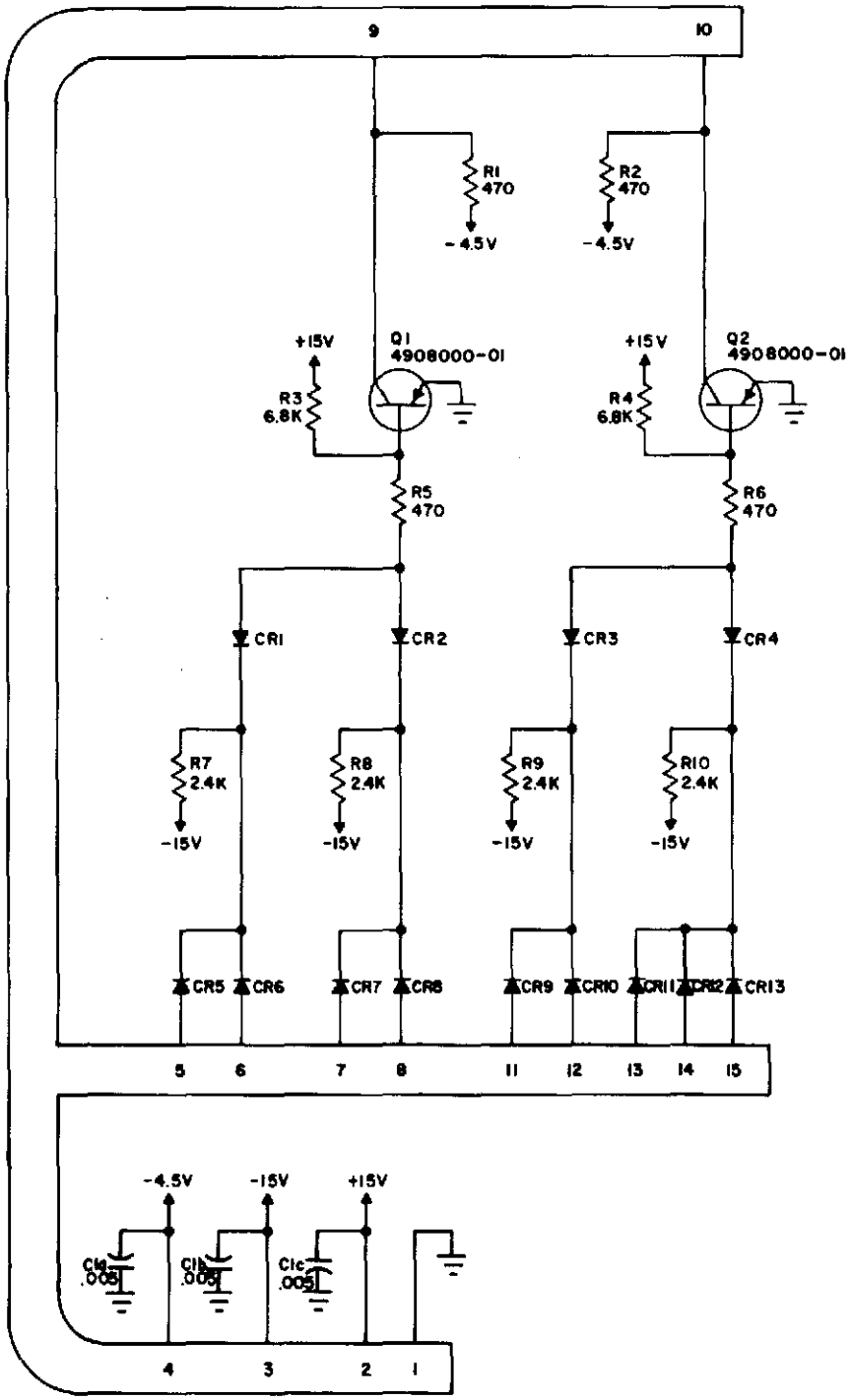


Figure 6-39. Inverter, Module Type 2050, Electrical Schematic

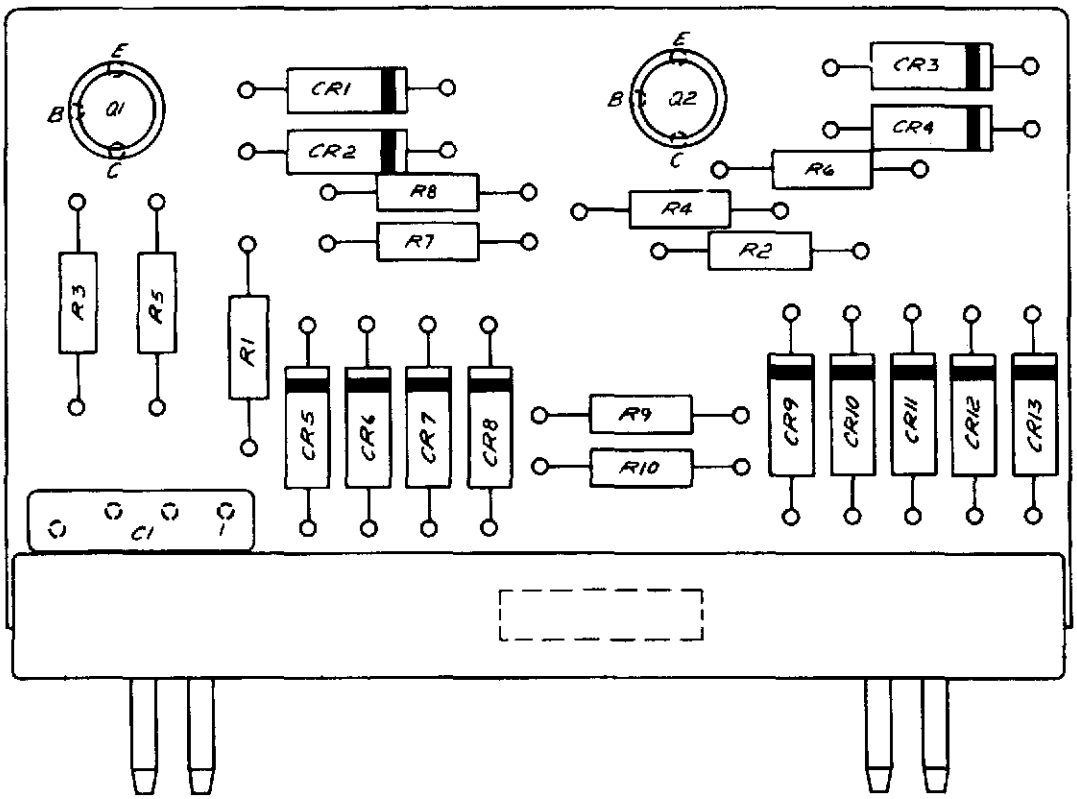


Figure 6-40. Module Type 2050 Component Layout

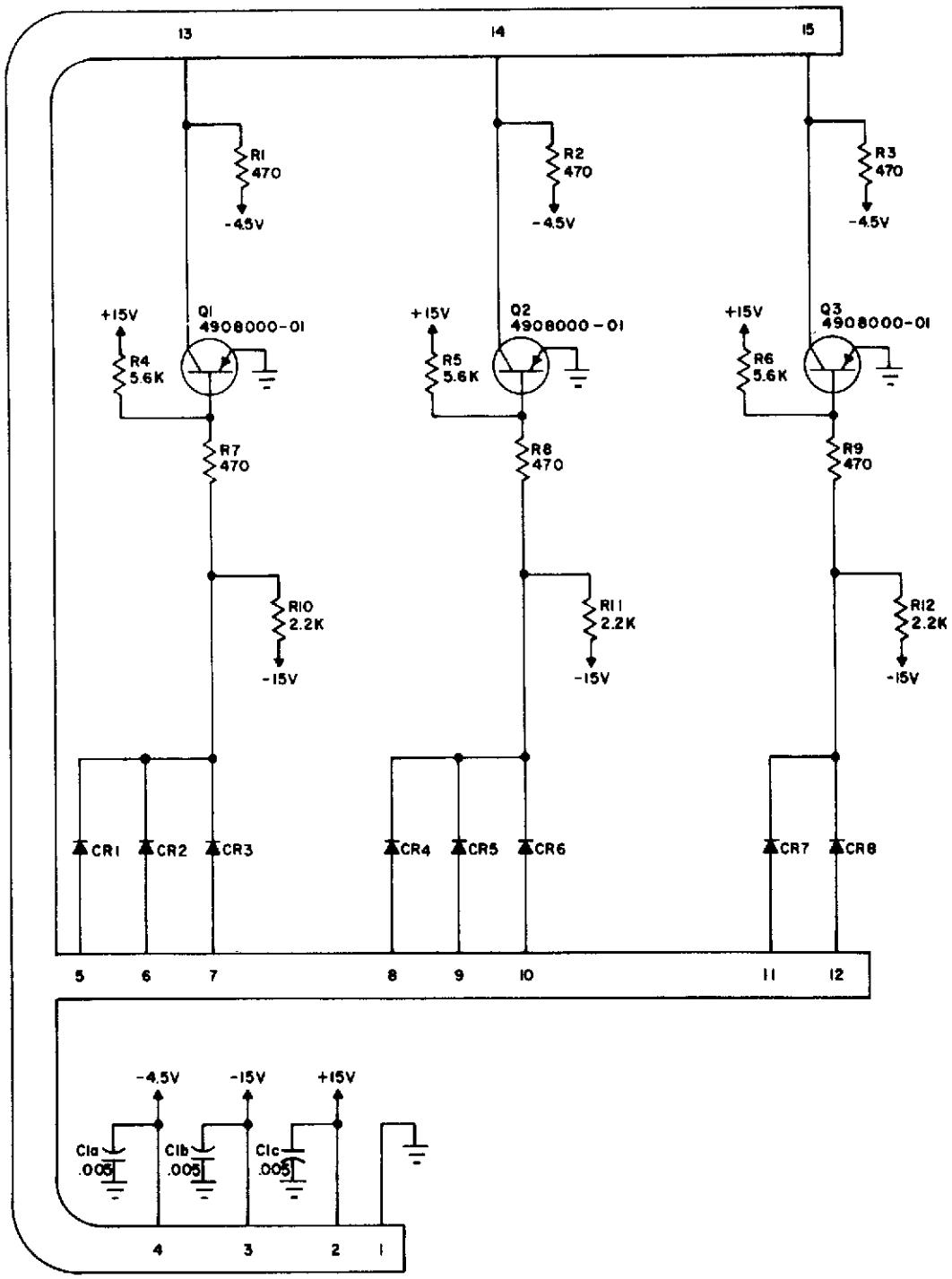


Figure 6-41. Inverter, Module Type 2060, Electrical Schematic

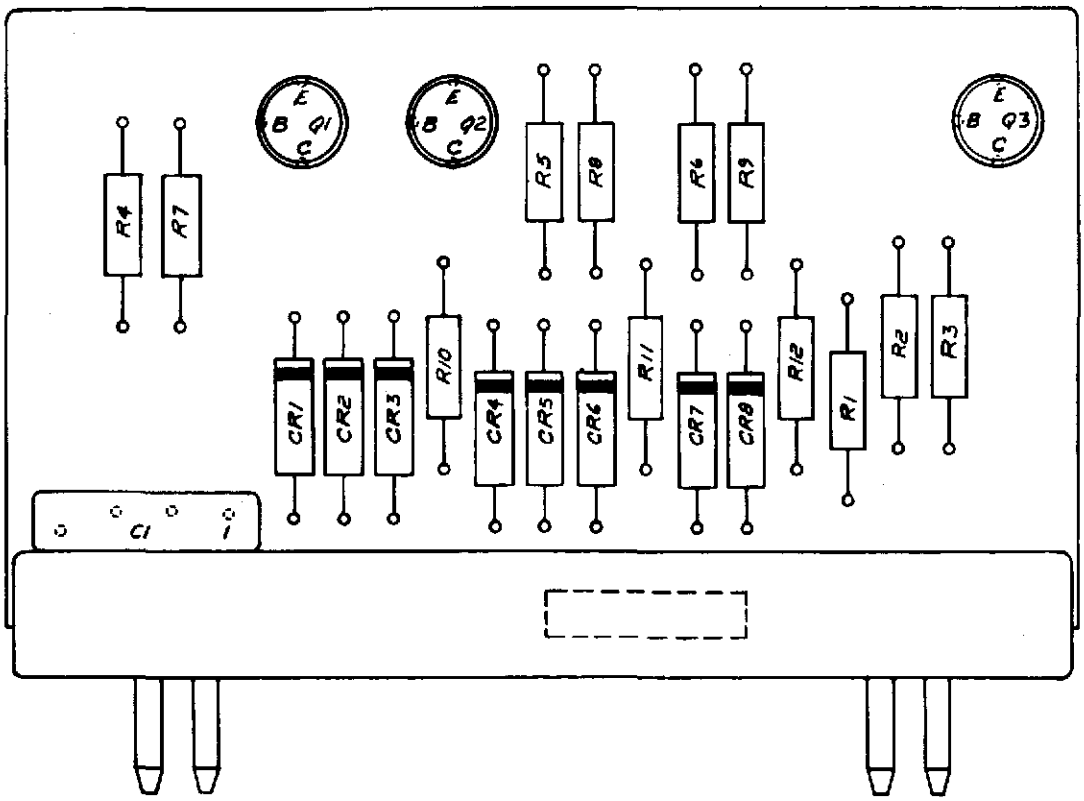


Figure 6-42. Module Type 2060 Component Layout

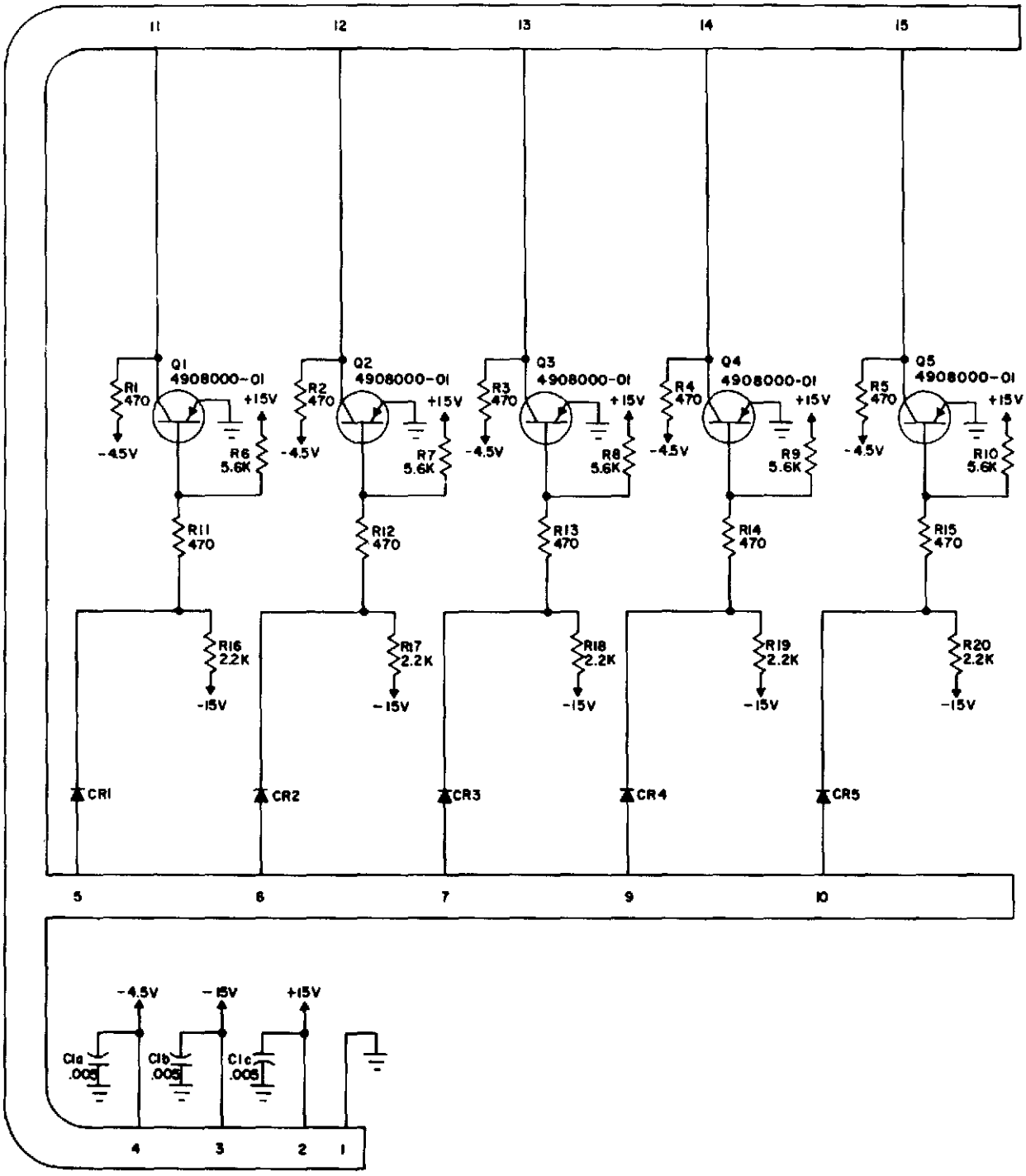


Figure 6-43. Inverter, Module Type 2070, Electrical Schematic

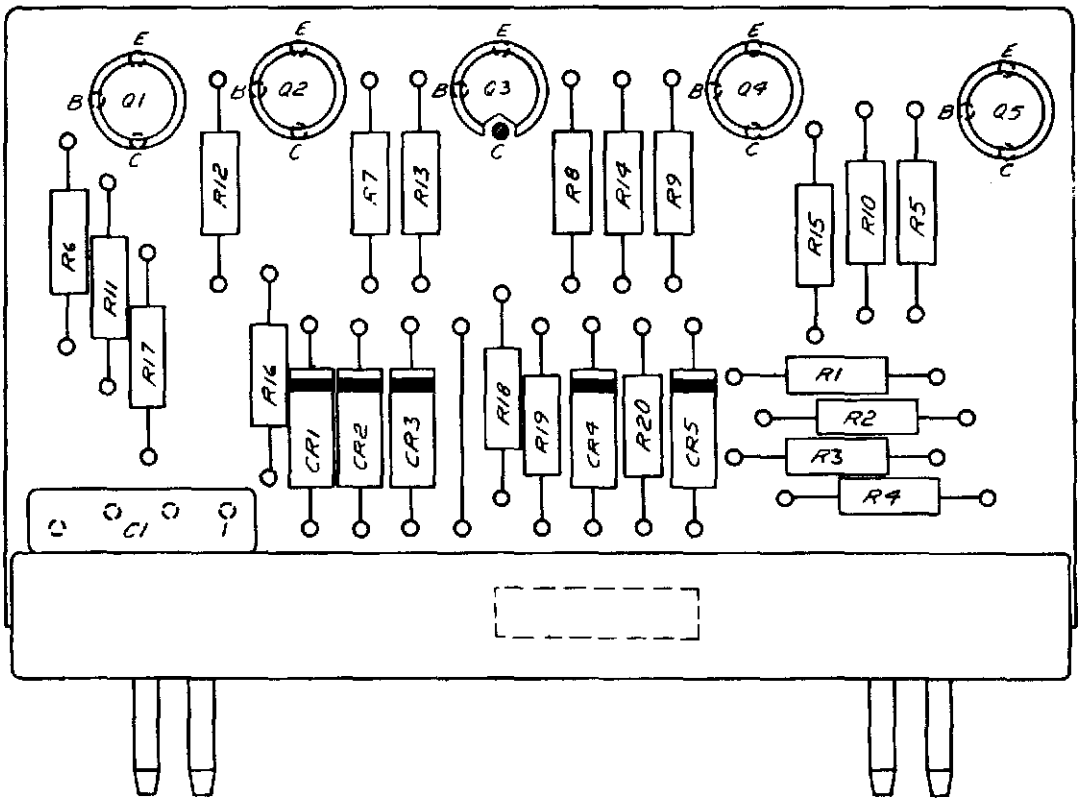


Figure 6-44. Module Type 2070 Component Layout

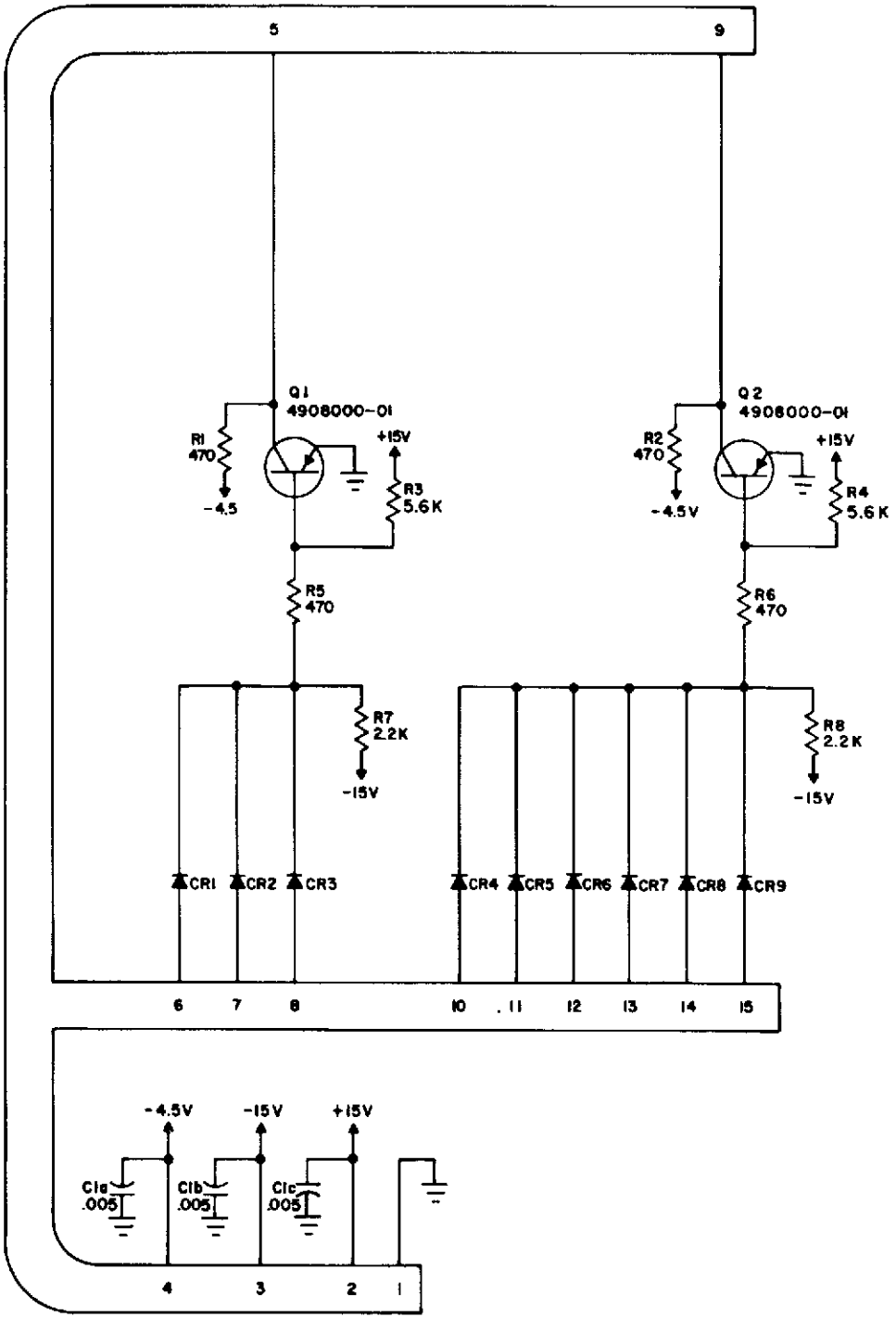


Figure 6-45. Inverter, Module Type 2080, Electrical Schematic

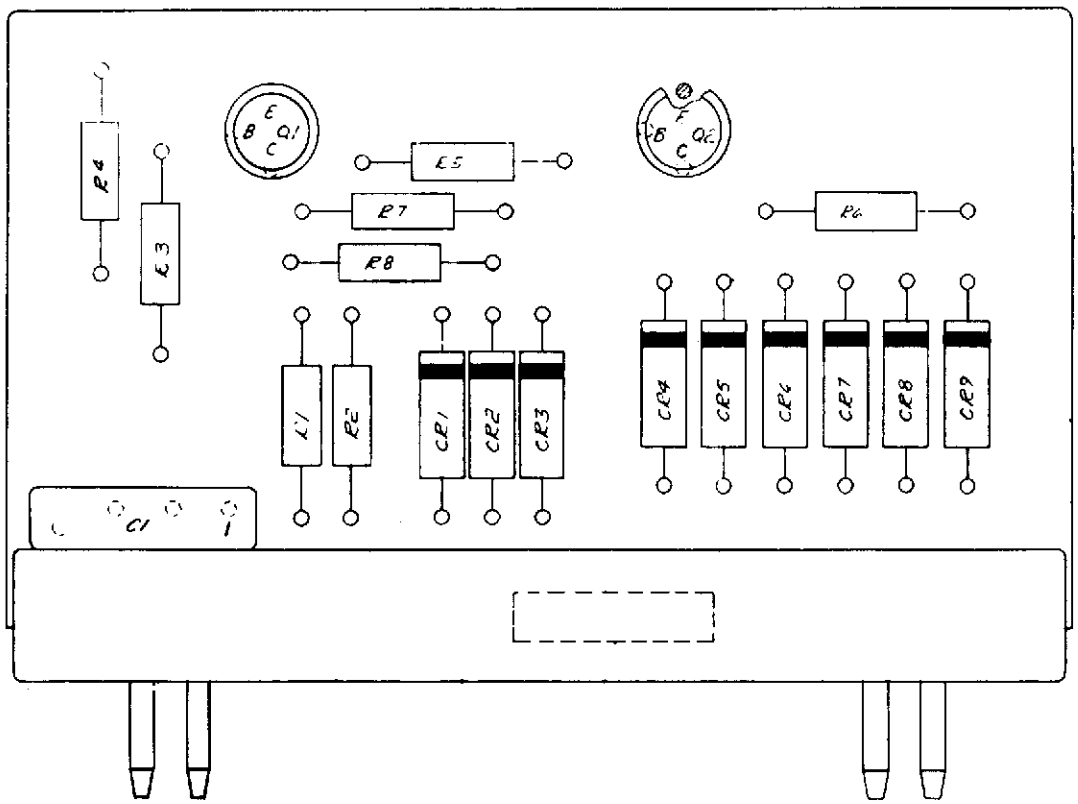


Figure 6-46. Module Type 2080 Component Layout

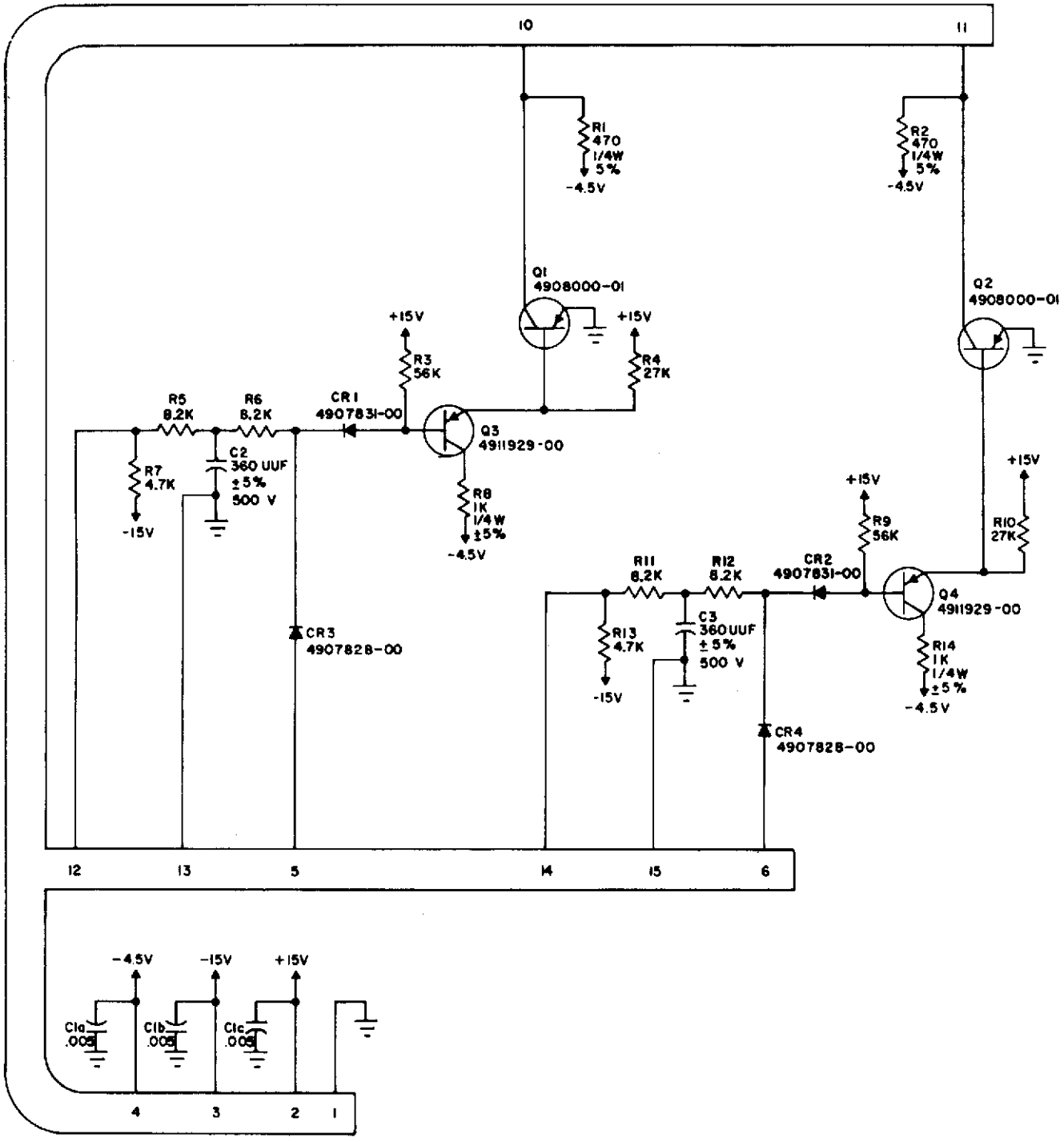


Figure 6-47. Inverter, Module Type 2090, Electrical Schematic

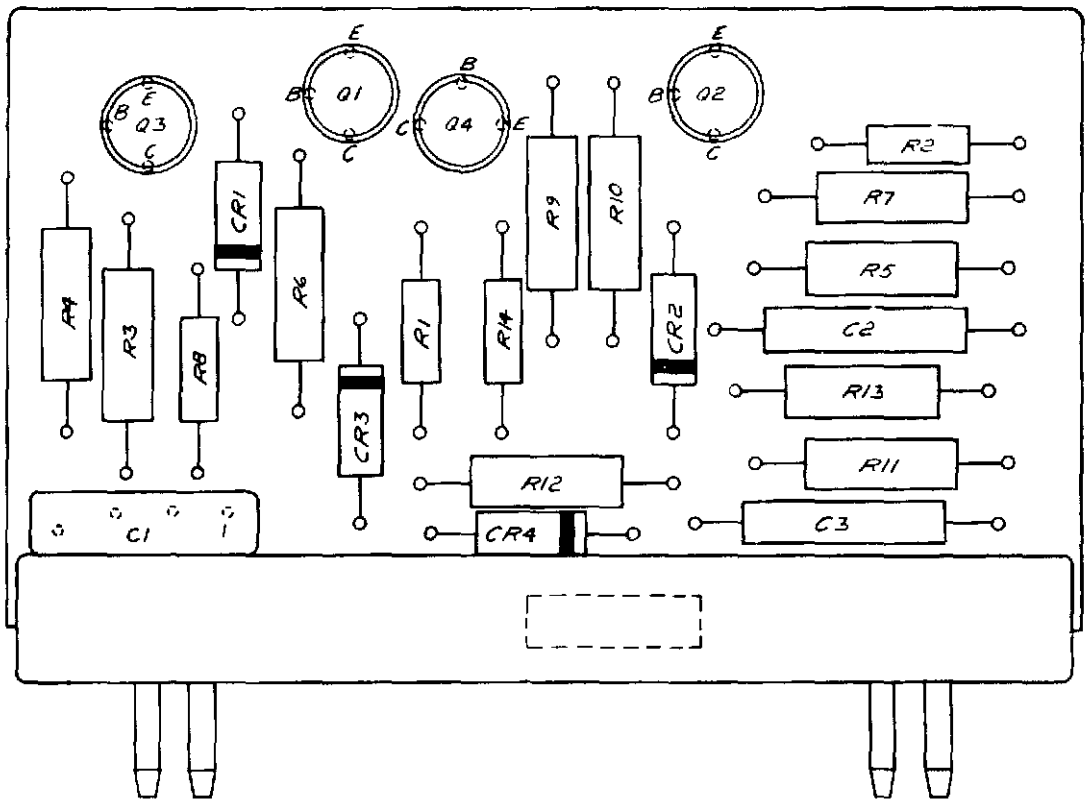


Figure 6-48. Module Type 2090 Component Layout

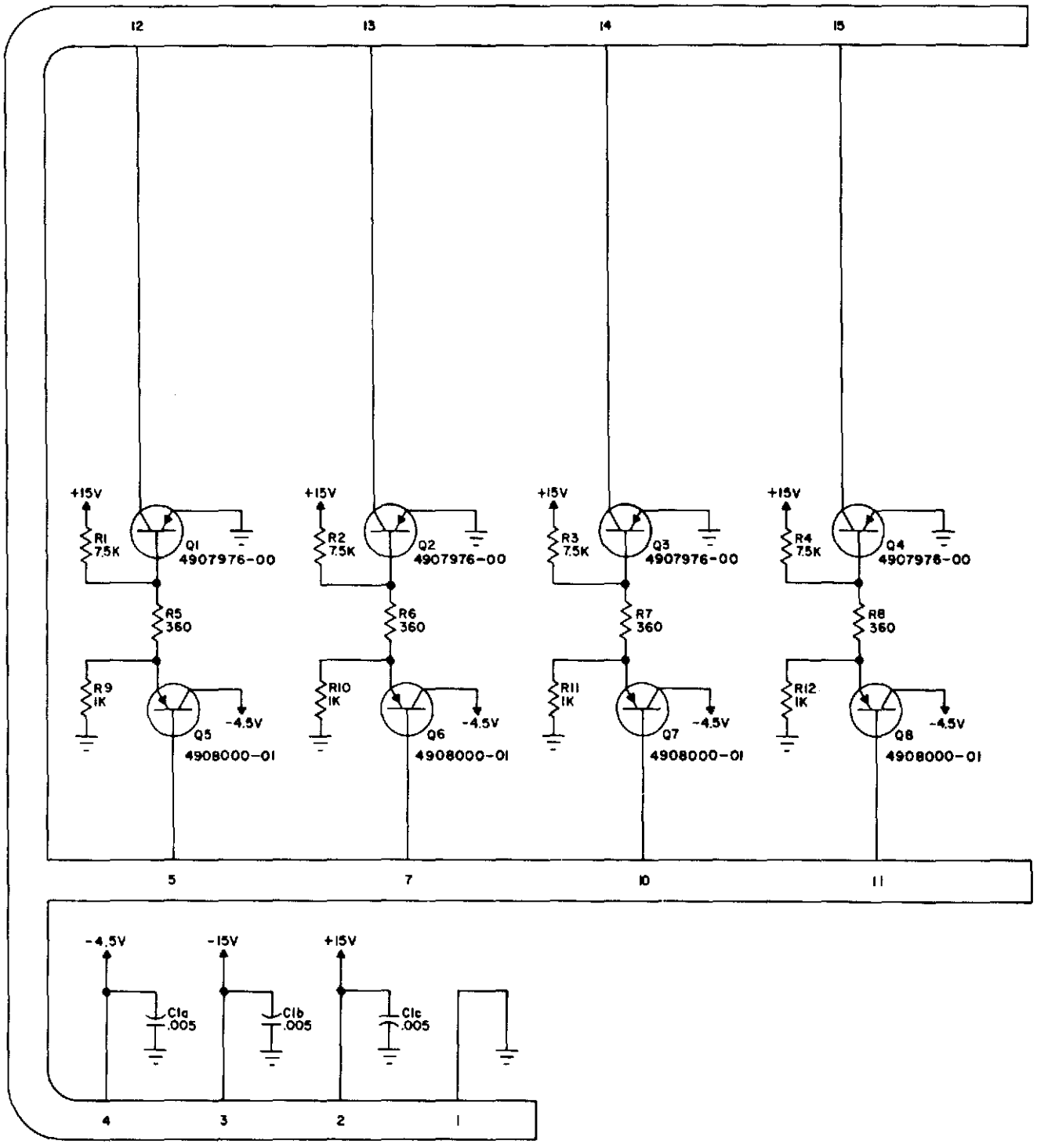


Figure 6-49. Amplifier, Module Type 2100, Electrical Schematic

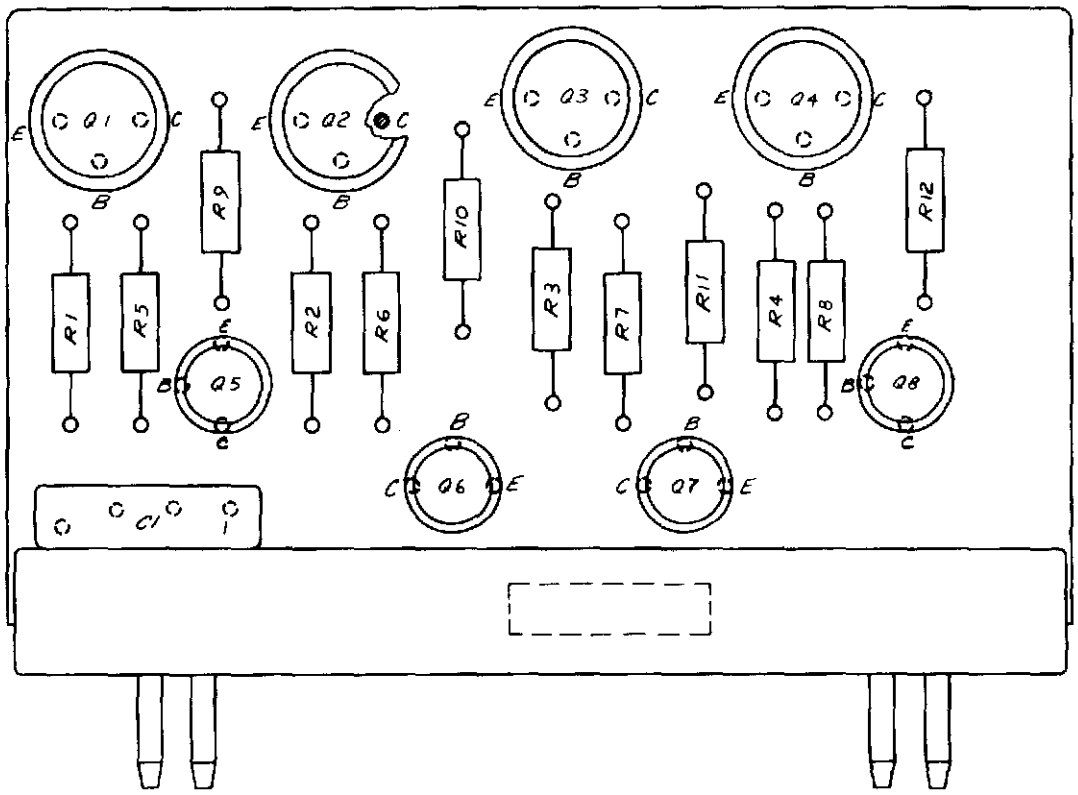


Figure 6-50. Module Type 2100 Component Layout

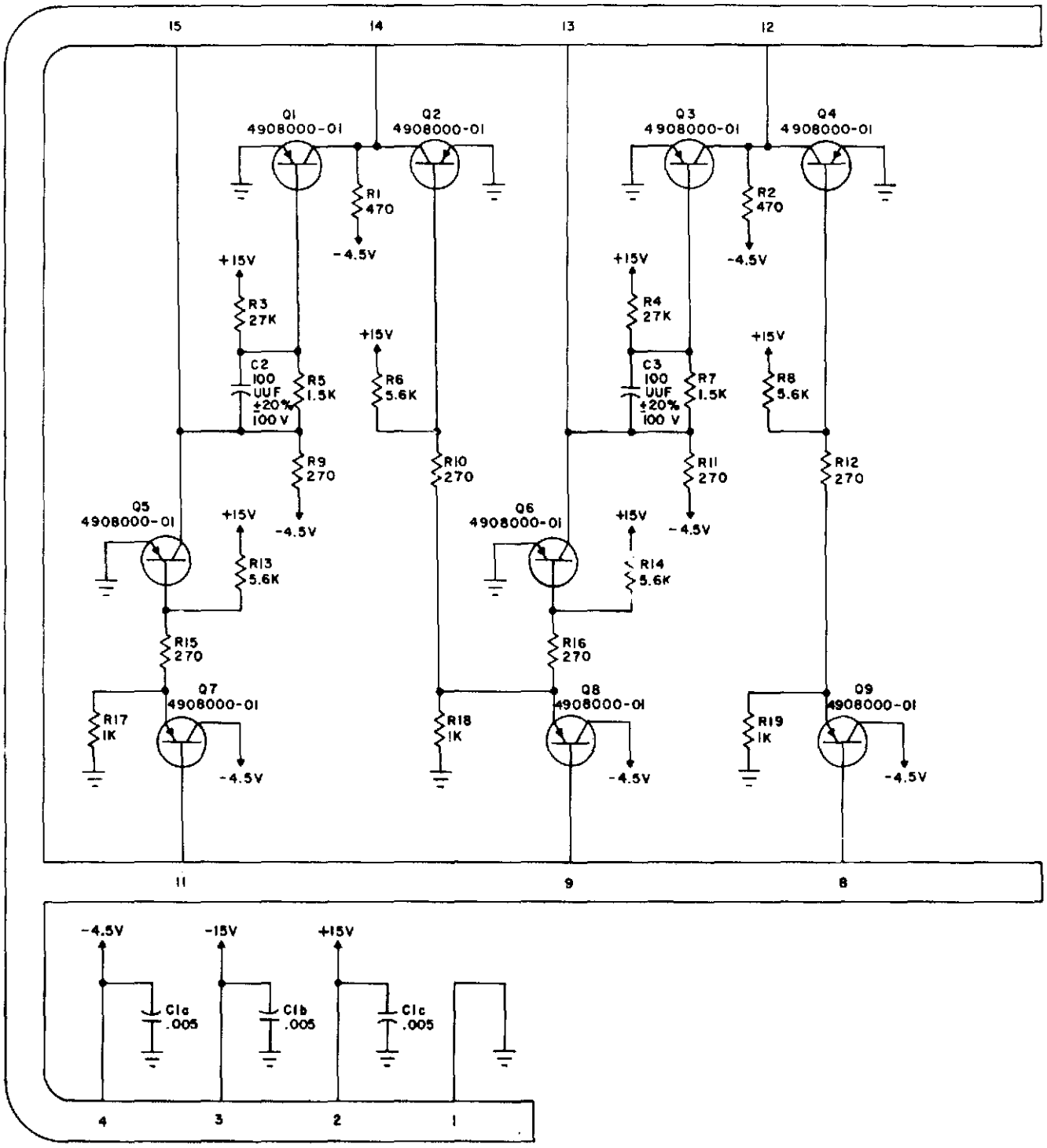


Figure 6-51. Amplifier, Module Type 2110, Electrical Schematic

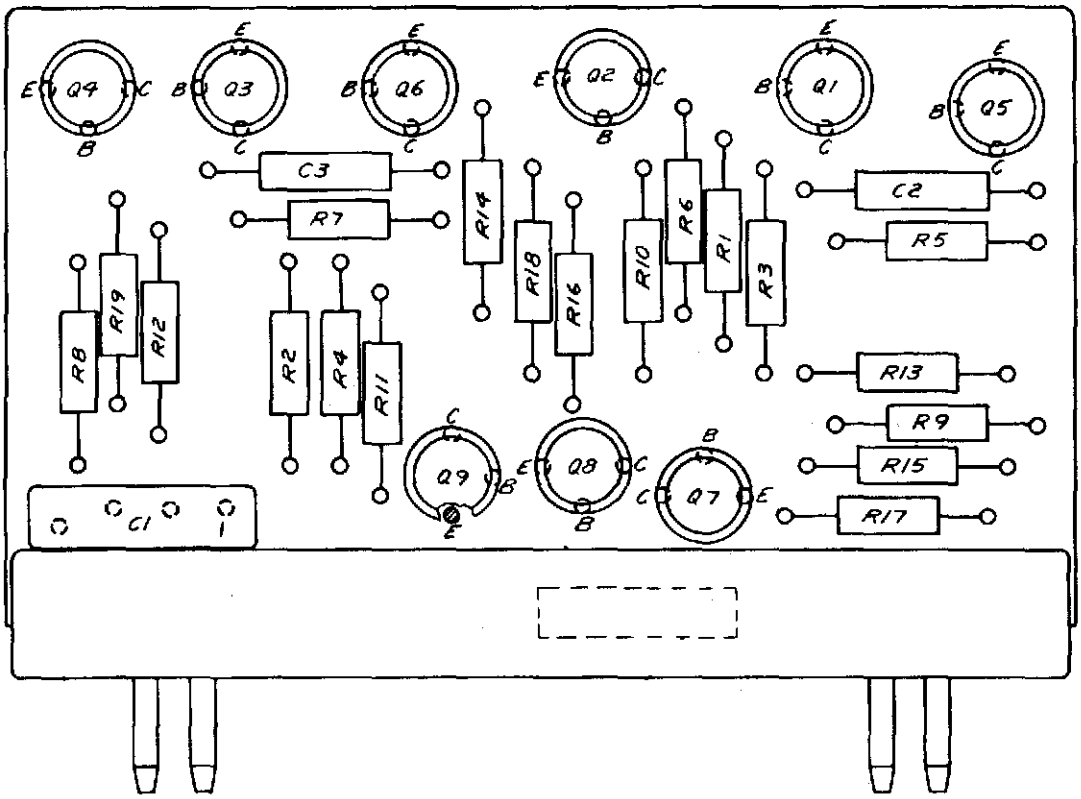


Figure 6-52. Module Type 2110 Component Layout

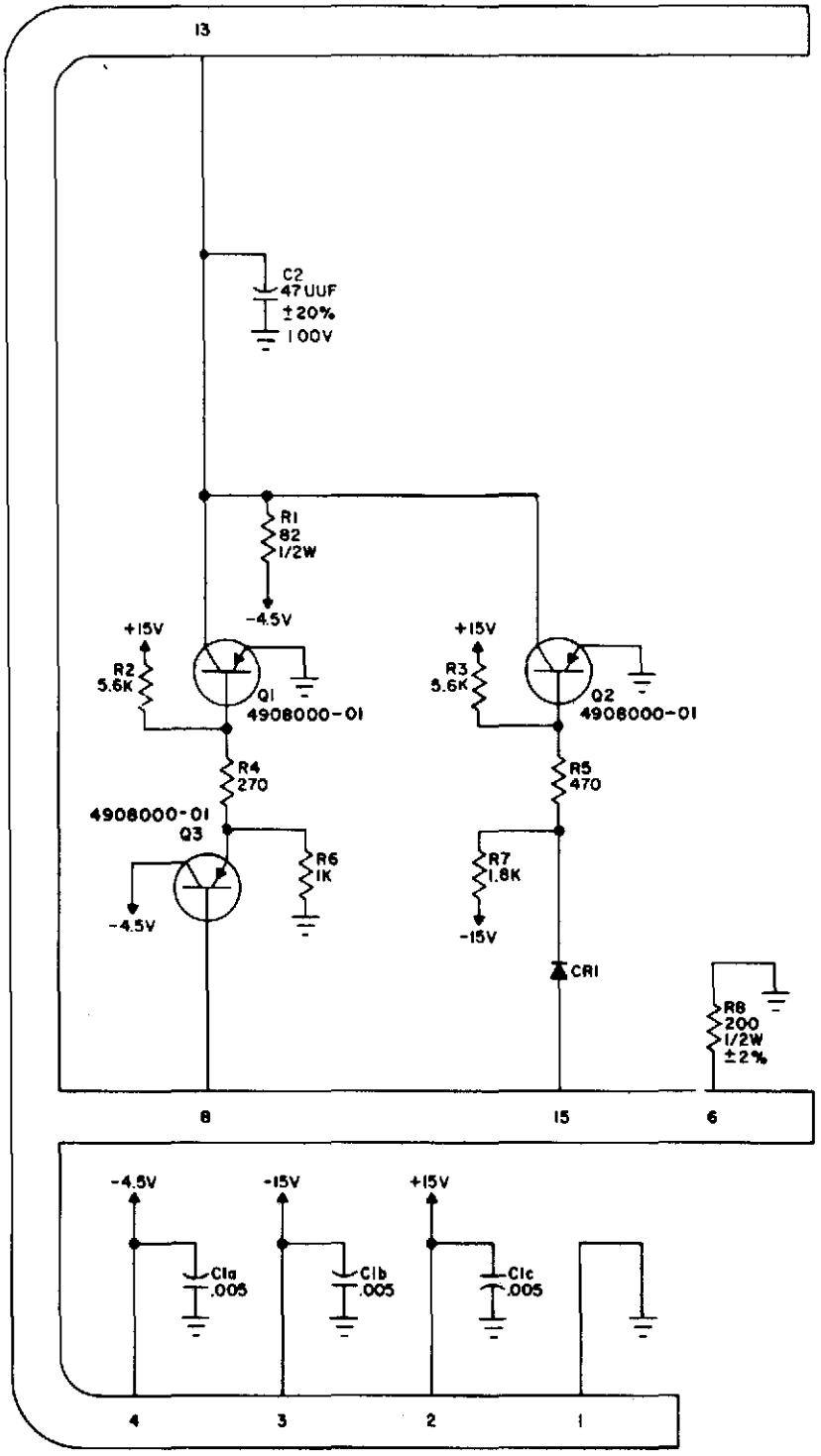


Figure 6-53. Amplifier, Module Type 2120, Electrical Schematic

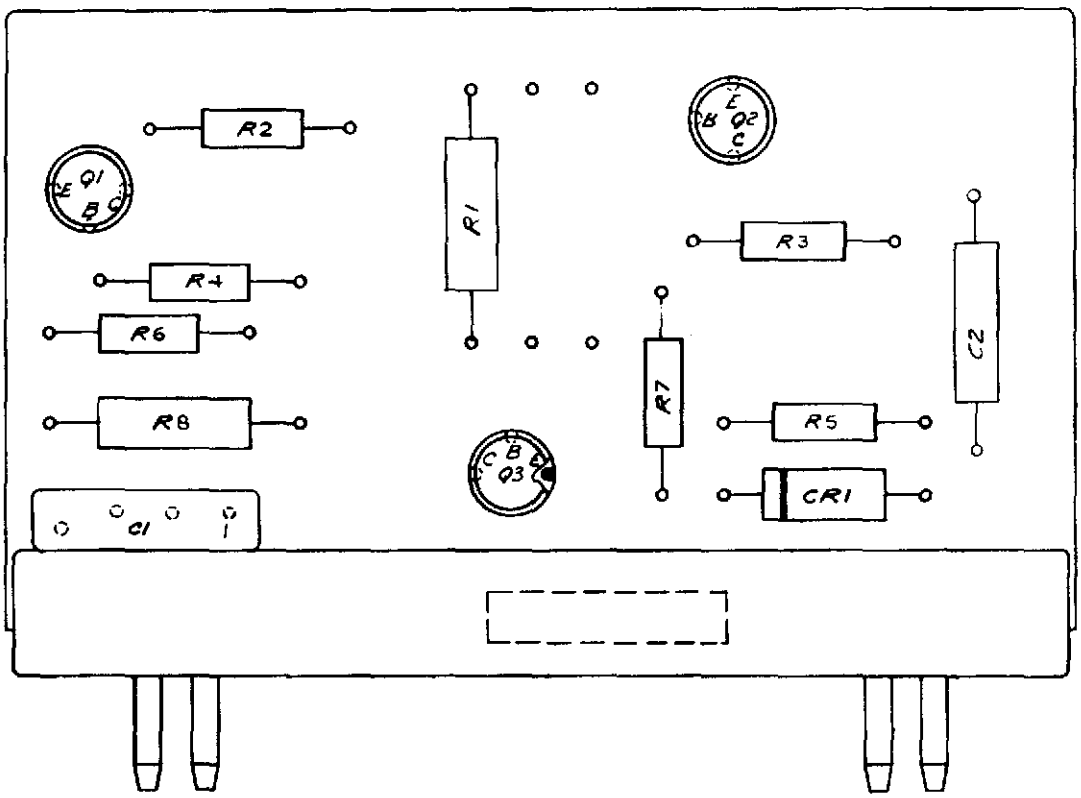


Figure 6-54. Module Type 2120 Component Layout

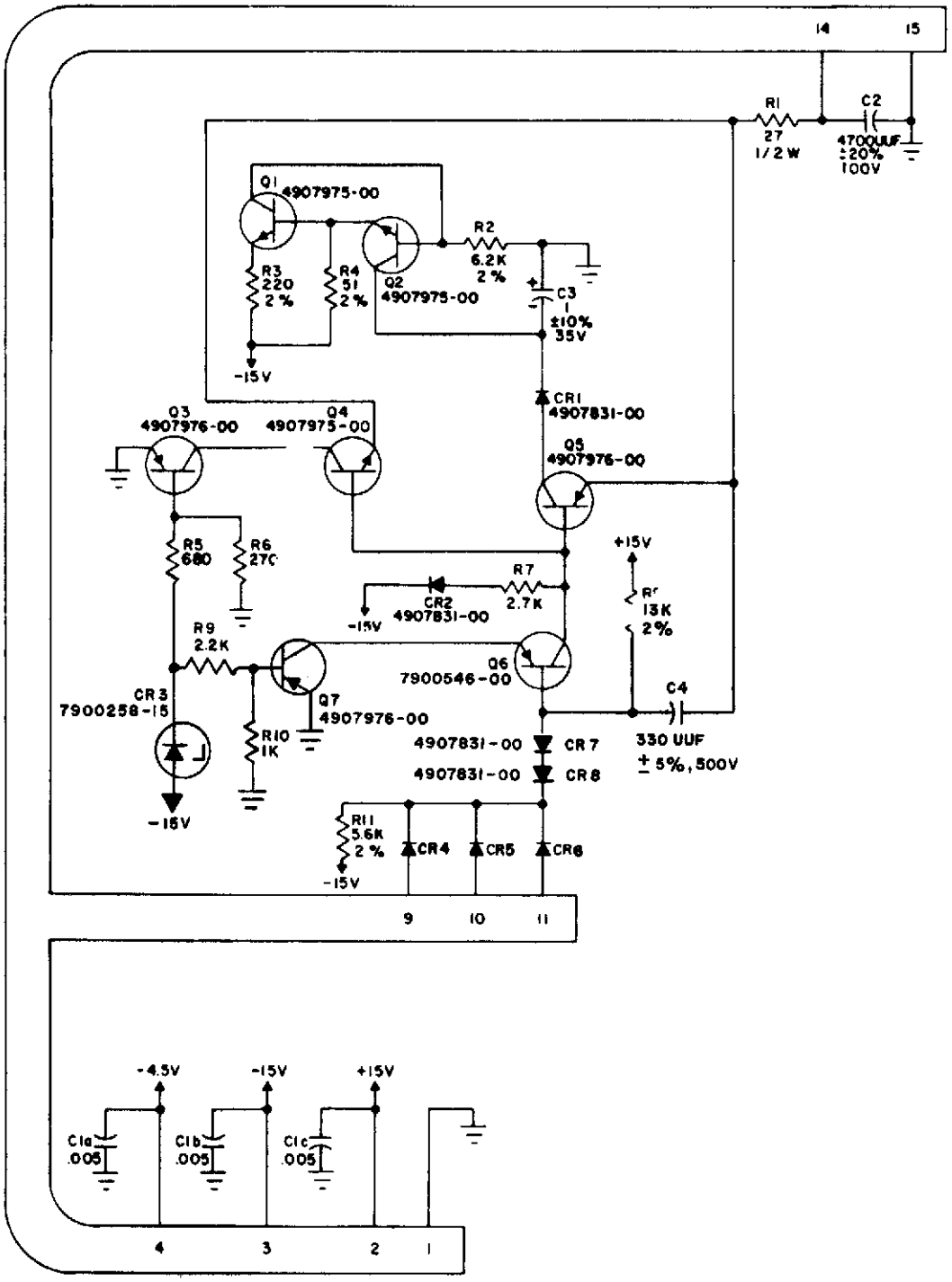


Figure 6-55. Amplifier, Module Type 2130, Electrical Schematic

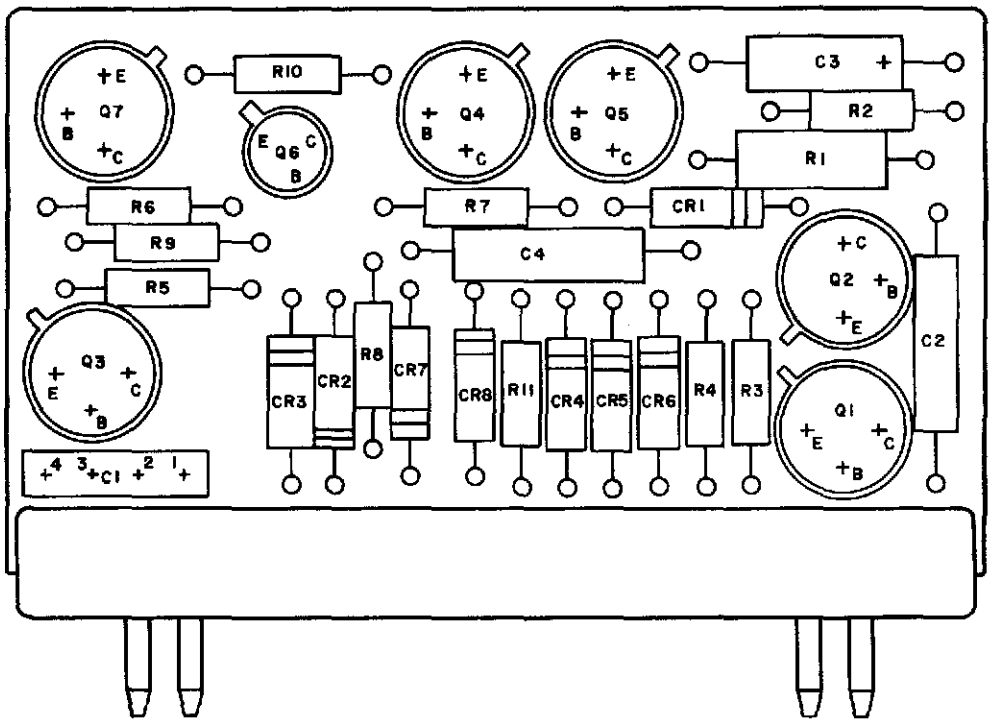


Figure 6-56. Module Type 2130 Component Layout

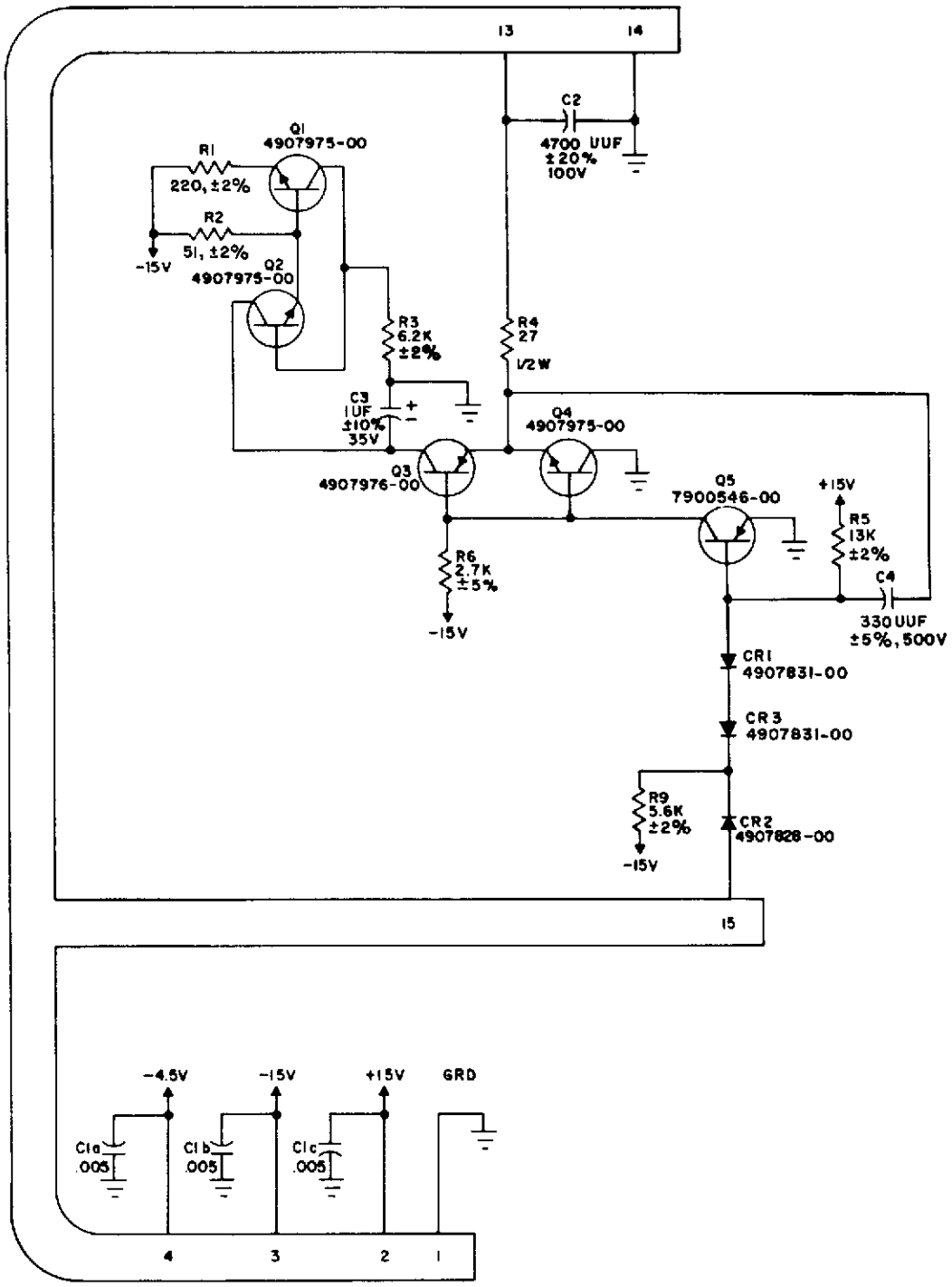


Figure 6-57. Amplifier, Module Type 2140, Electrical Schematic

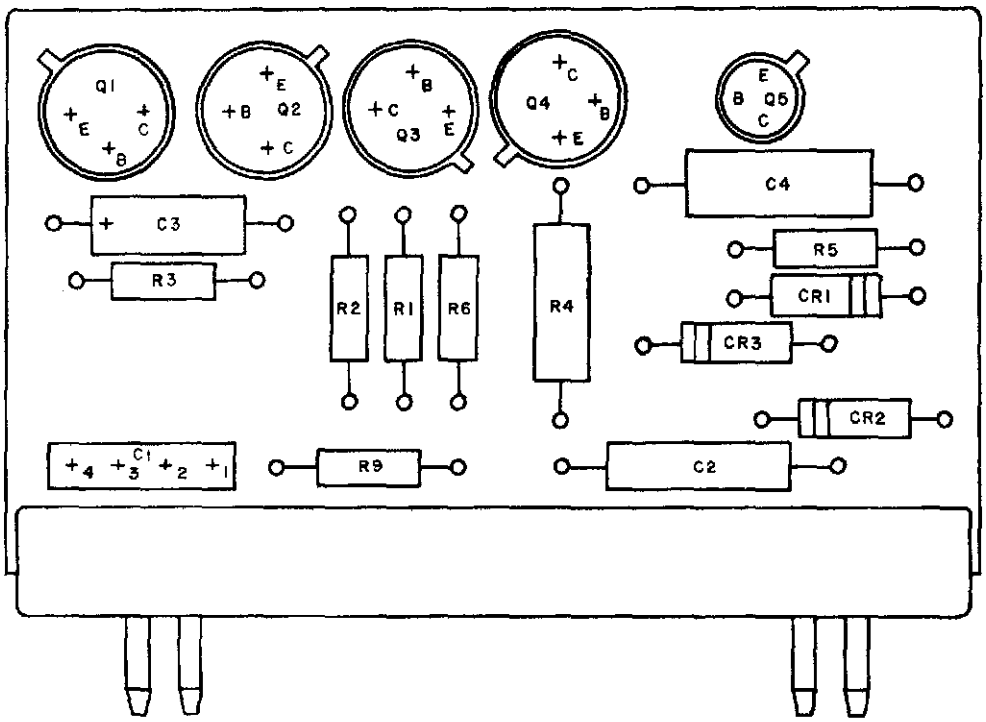


Figure 6-58. Module Type 2140 Component Layout

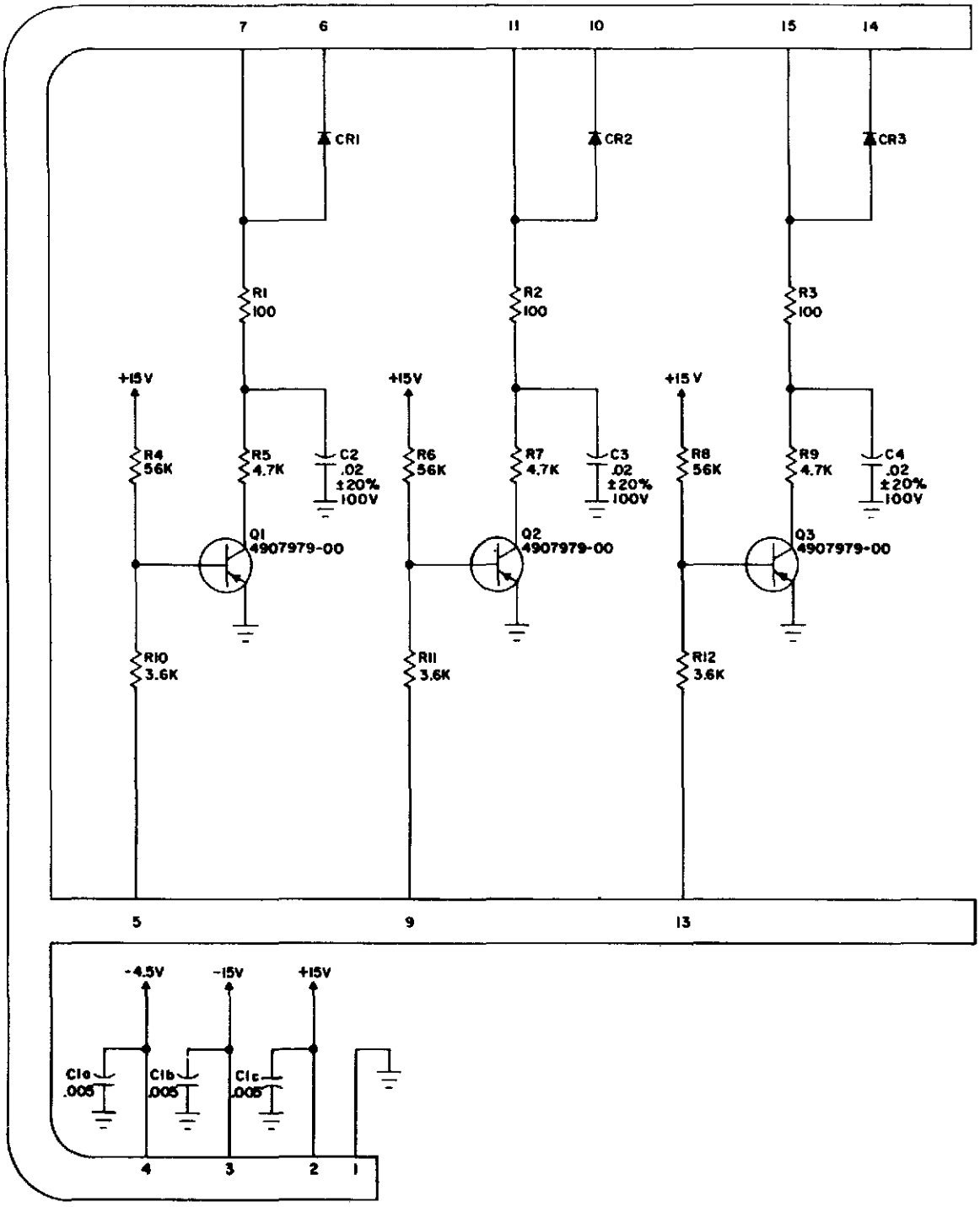


Figure 6-59. Amplifier, Module Type 2150, Electrical Schematic

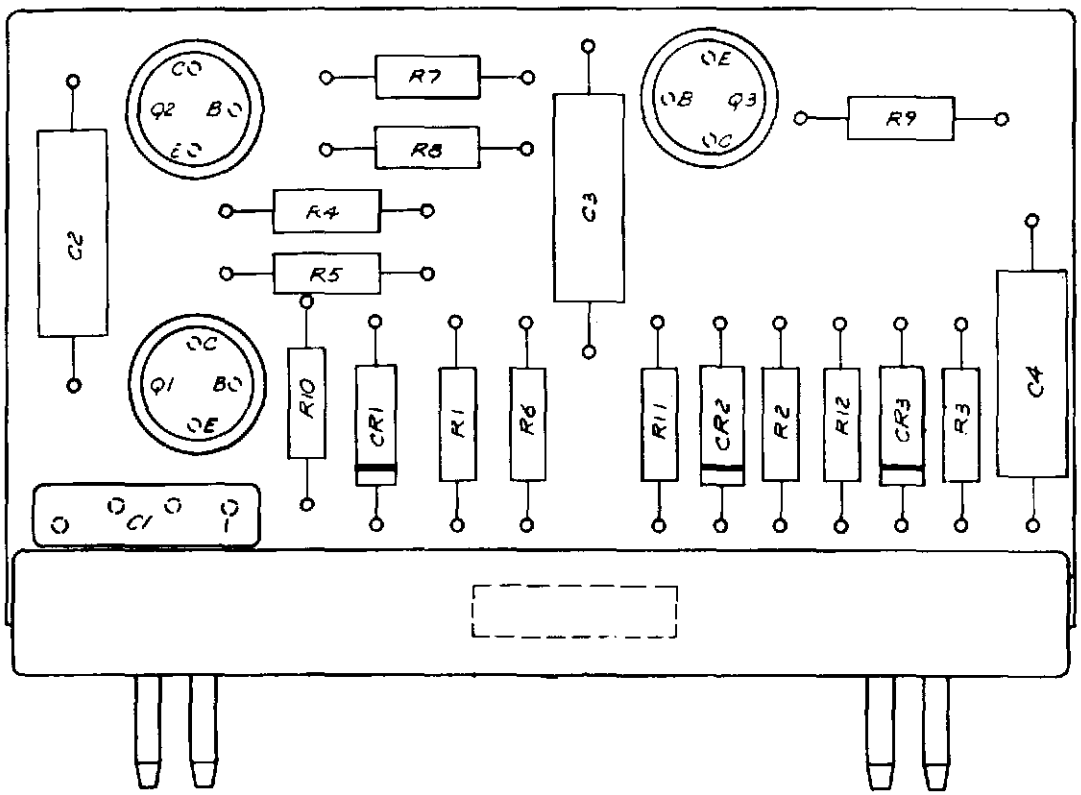


Figure 6-60. Module Type 2150 Component Layout

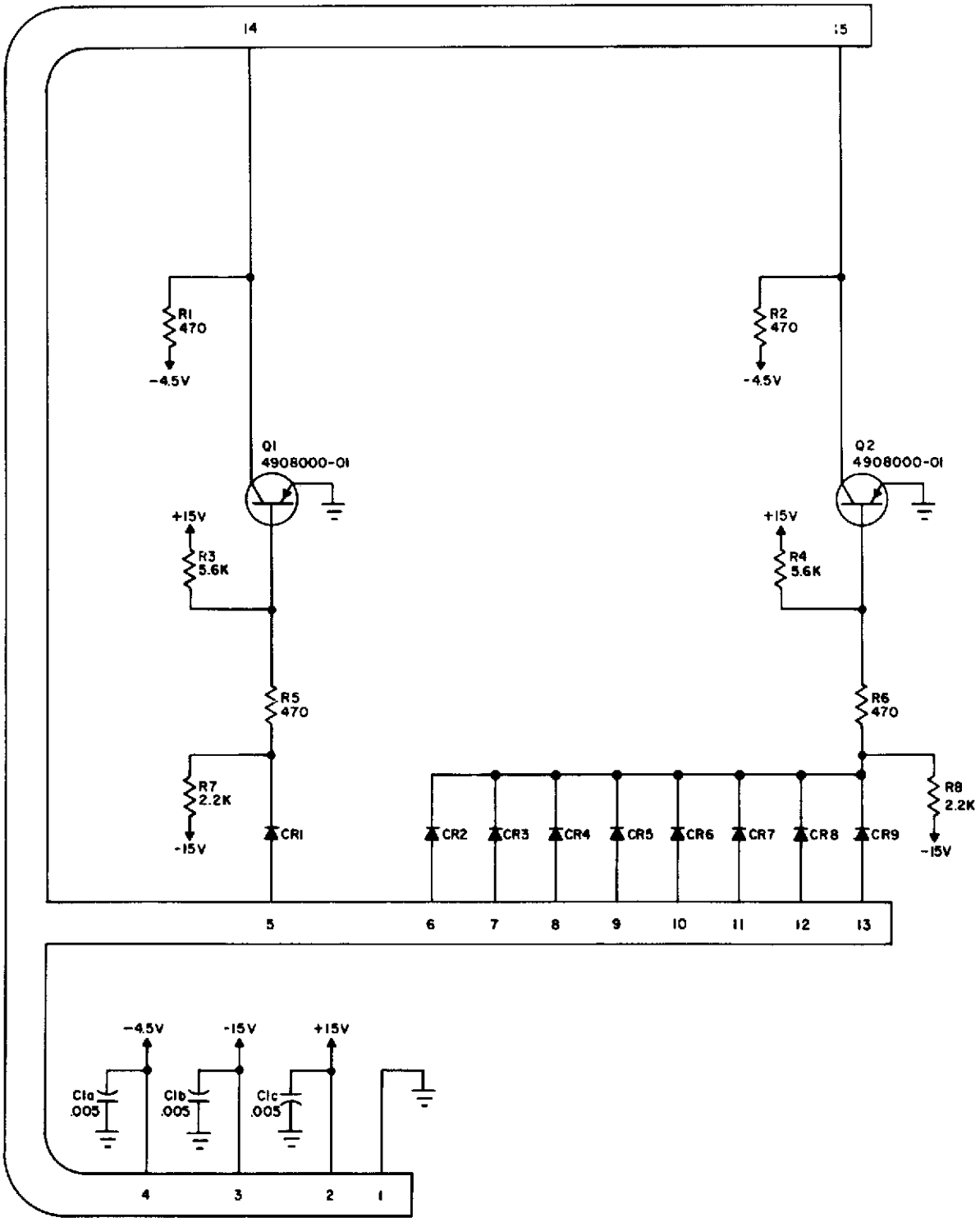


Figure 6-61. Inverter, Module Type 2160, Electrical Schematic

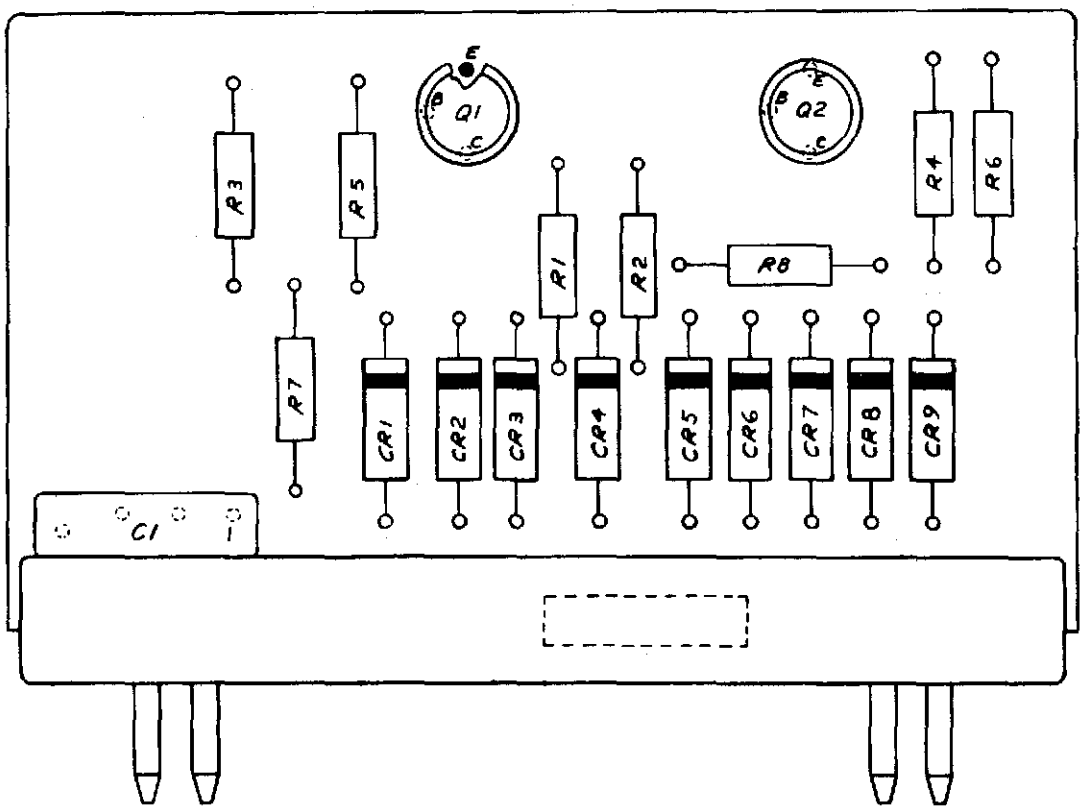


Figure 6-62. Module Type 2160 Component Layout

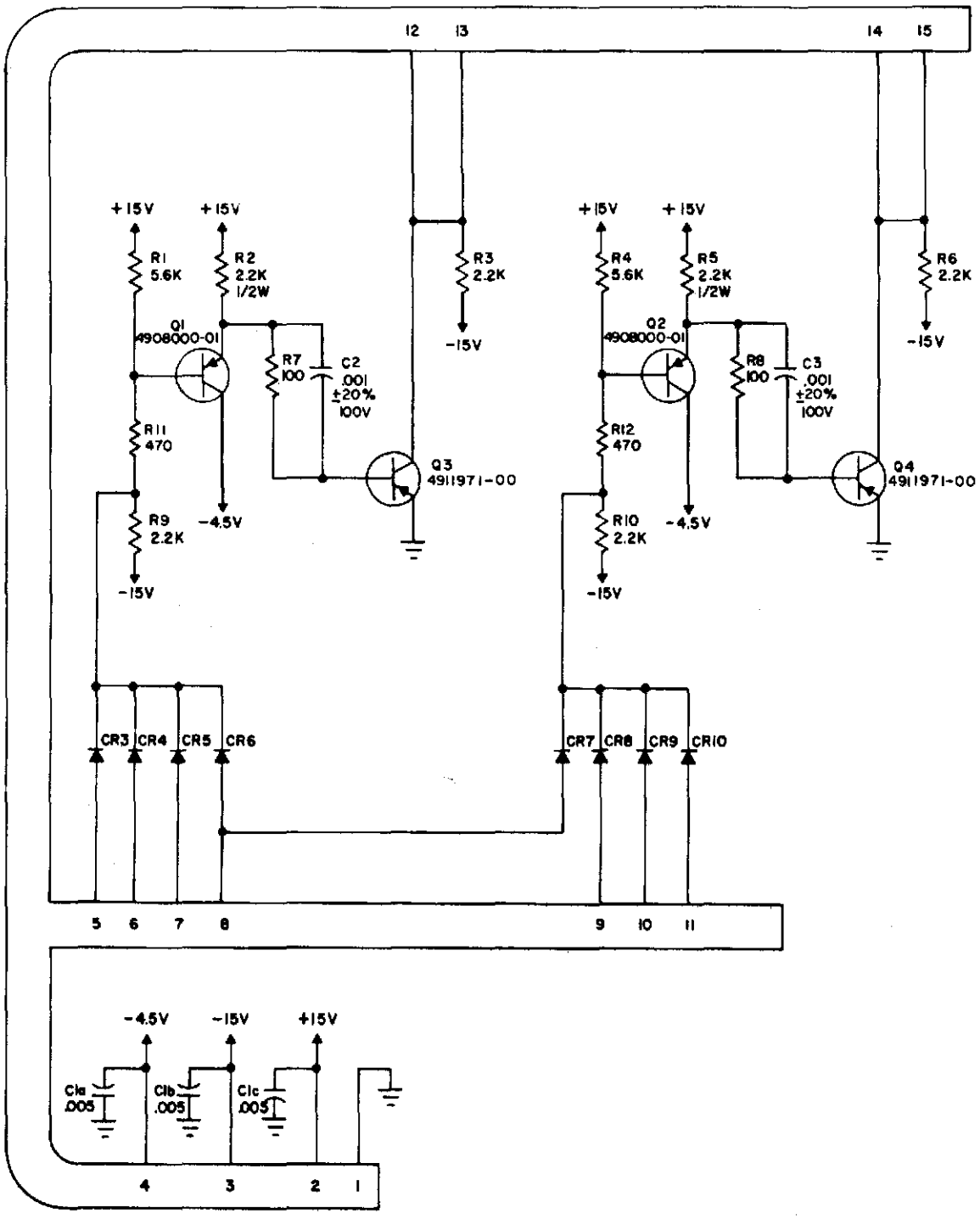


Figure 6-63. Negative Switch, Module Type 2170, Electrical Schematic

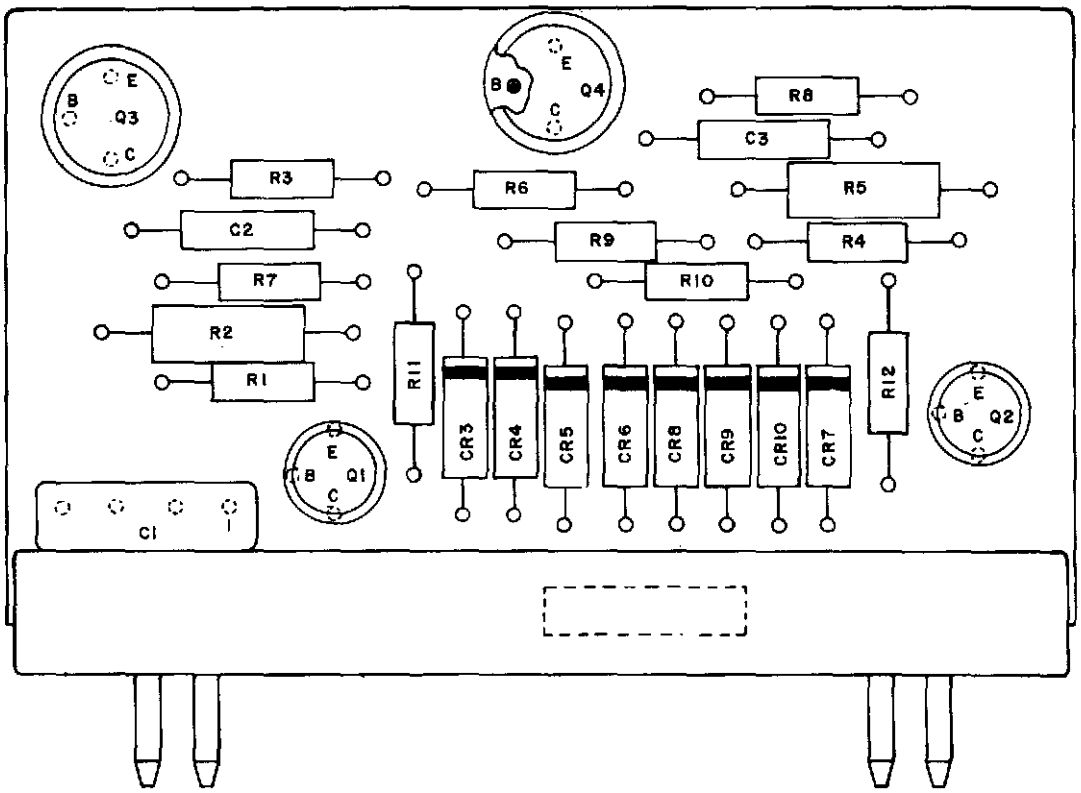


Figure 6-64. Module Type 2170 Component Layout

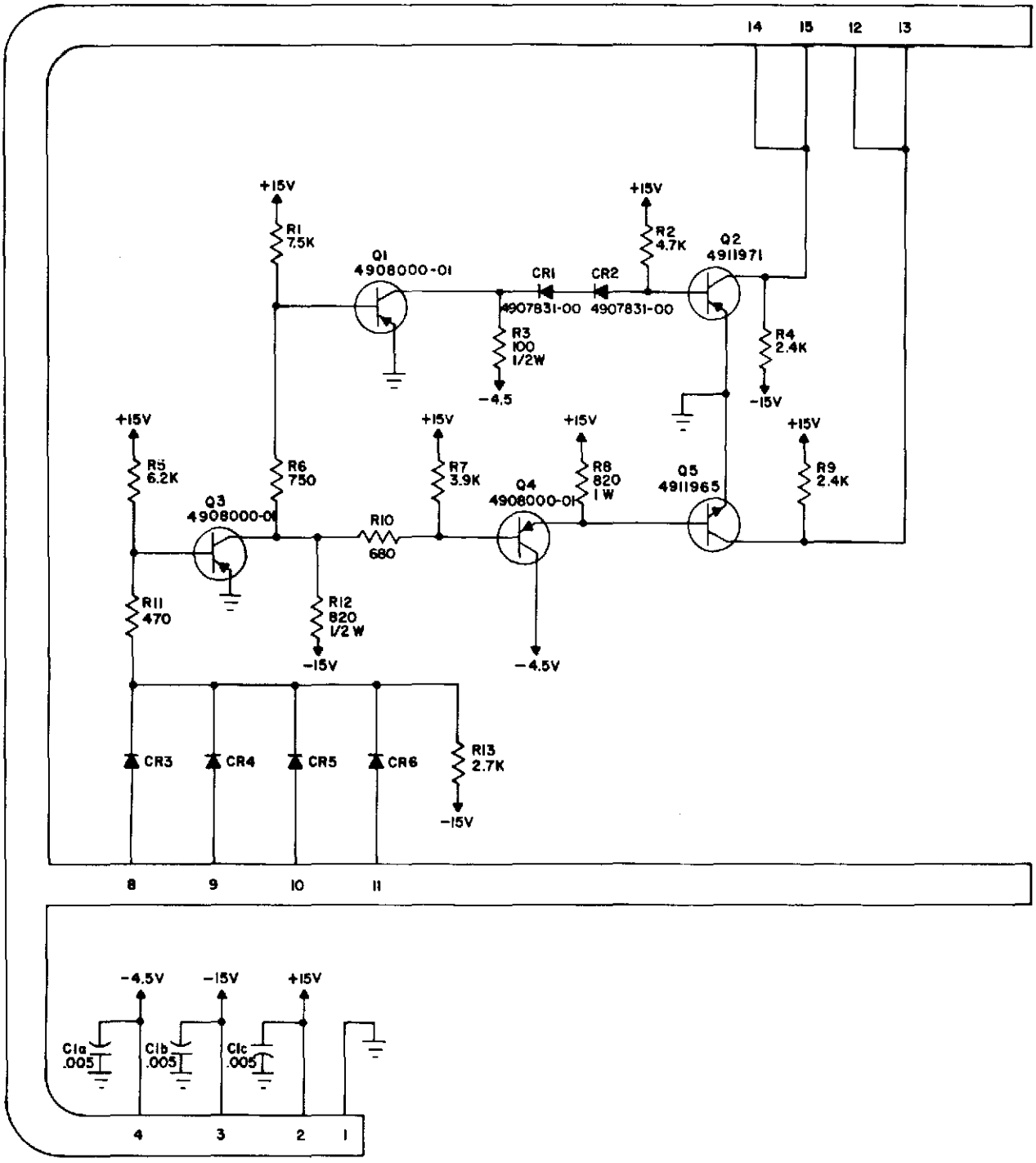


Figure 6-65. Positive and Negative Switch, Module Type 2180, Electrical Schematic

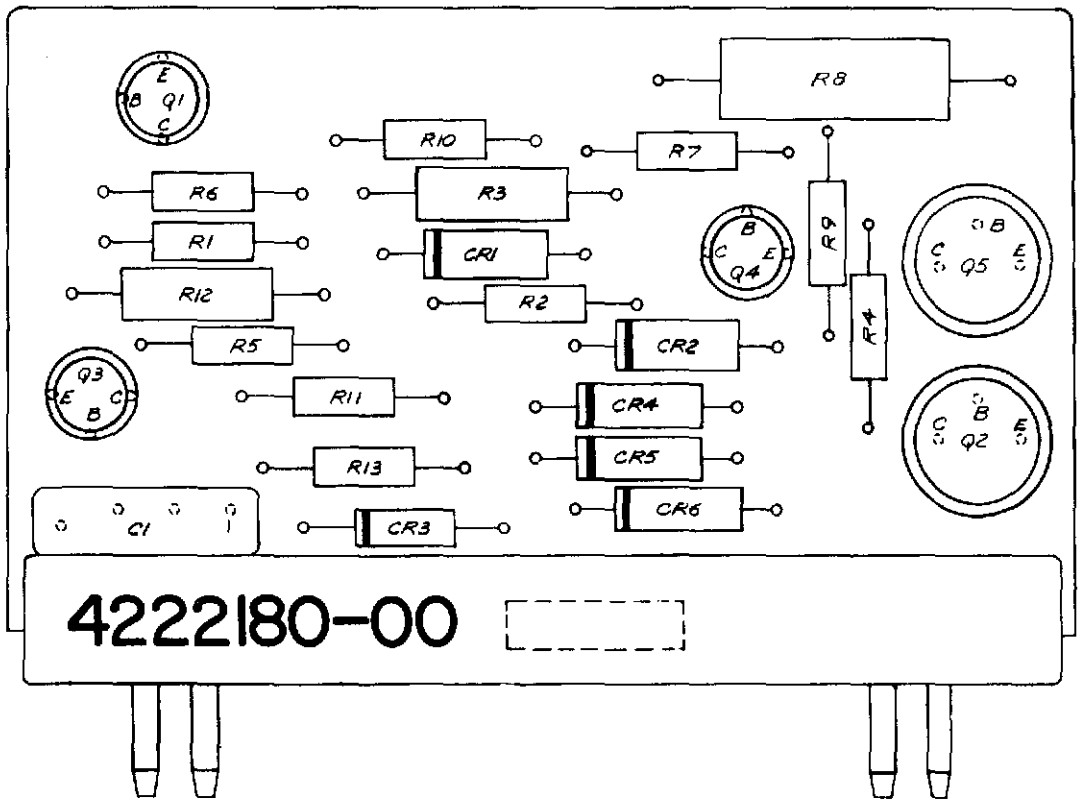


Figure 6-66. Module Type 2180 Component Layout

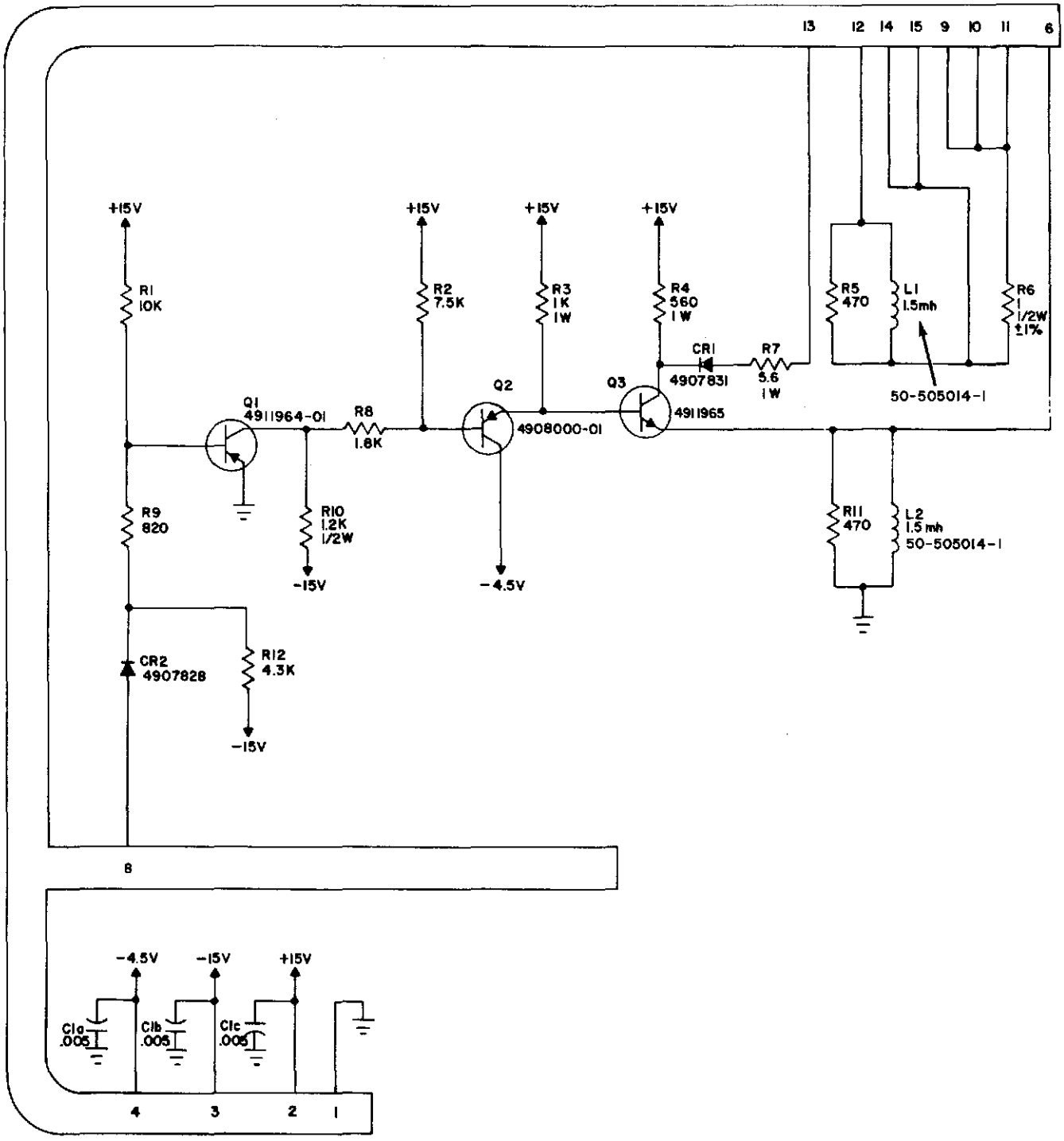


Figure 6-67. Current Diverter, Module Type 2191, Electrical Schematic

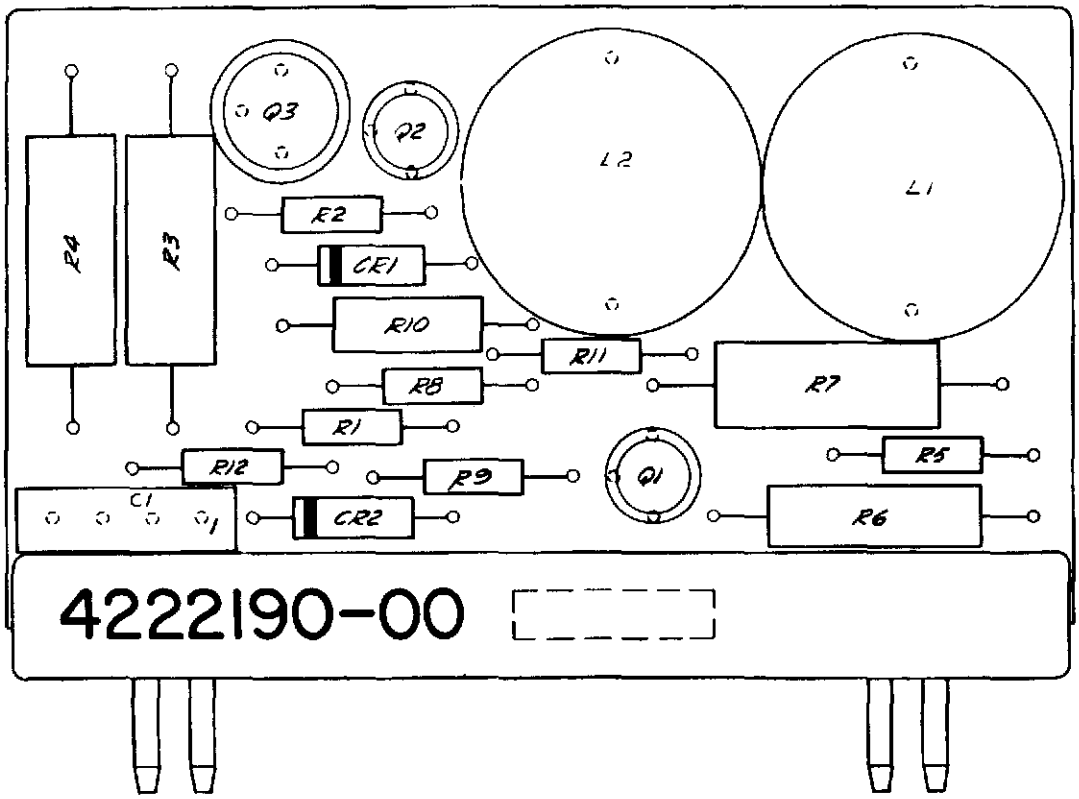


Figure 6-68. Module Type 2191 Component Layout

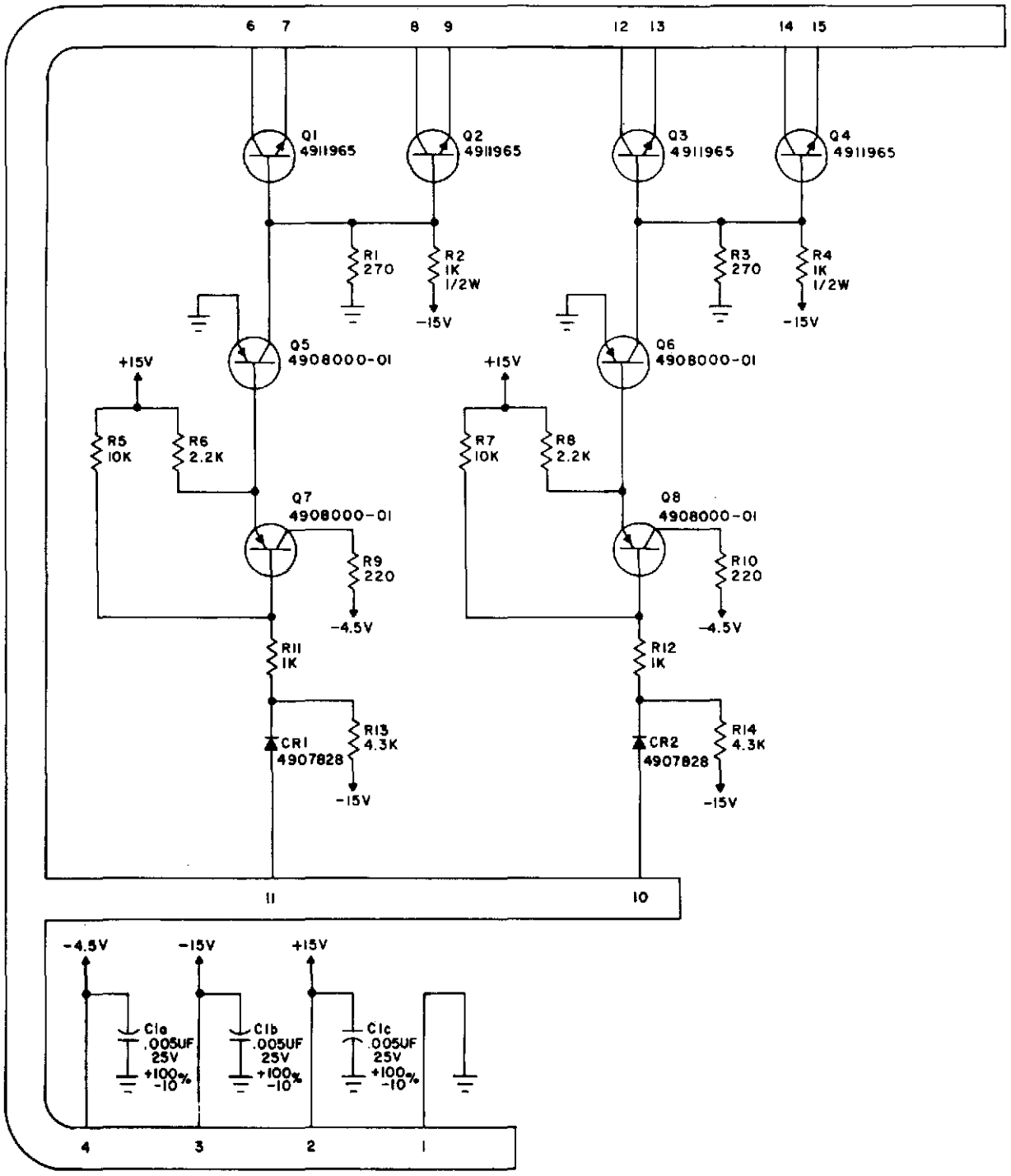


Figure 6-69. Read-Write Switch, Module Type 2200, Electrical Schematic

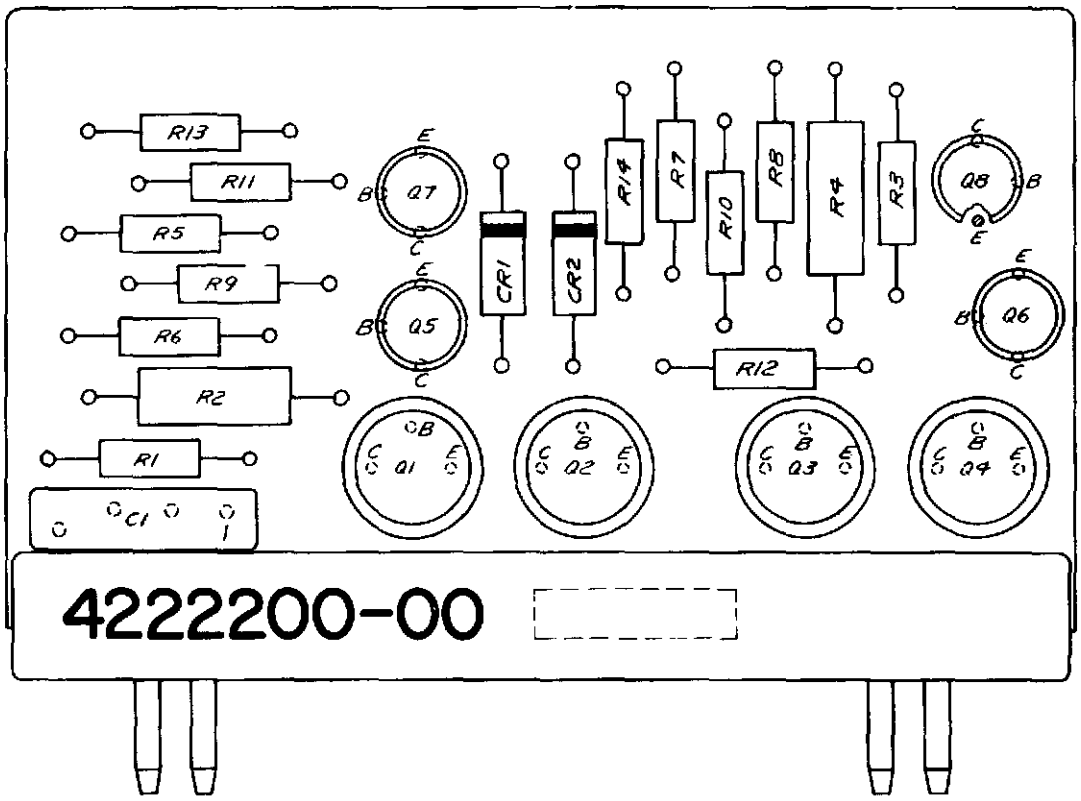


Figure 6-70. Module Type 2200 Component Layout

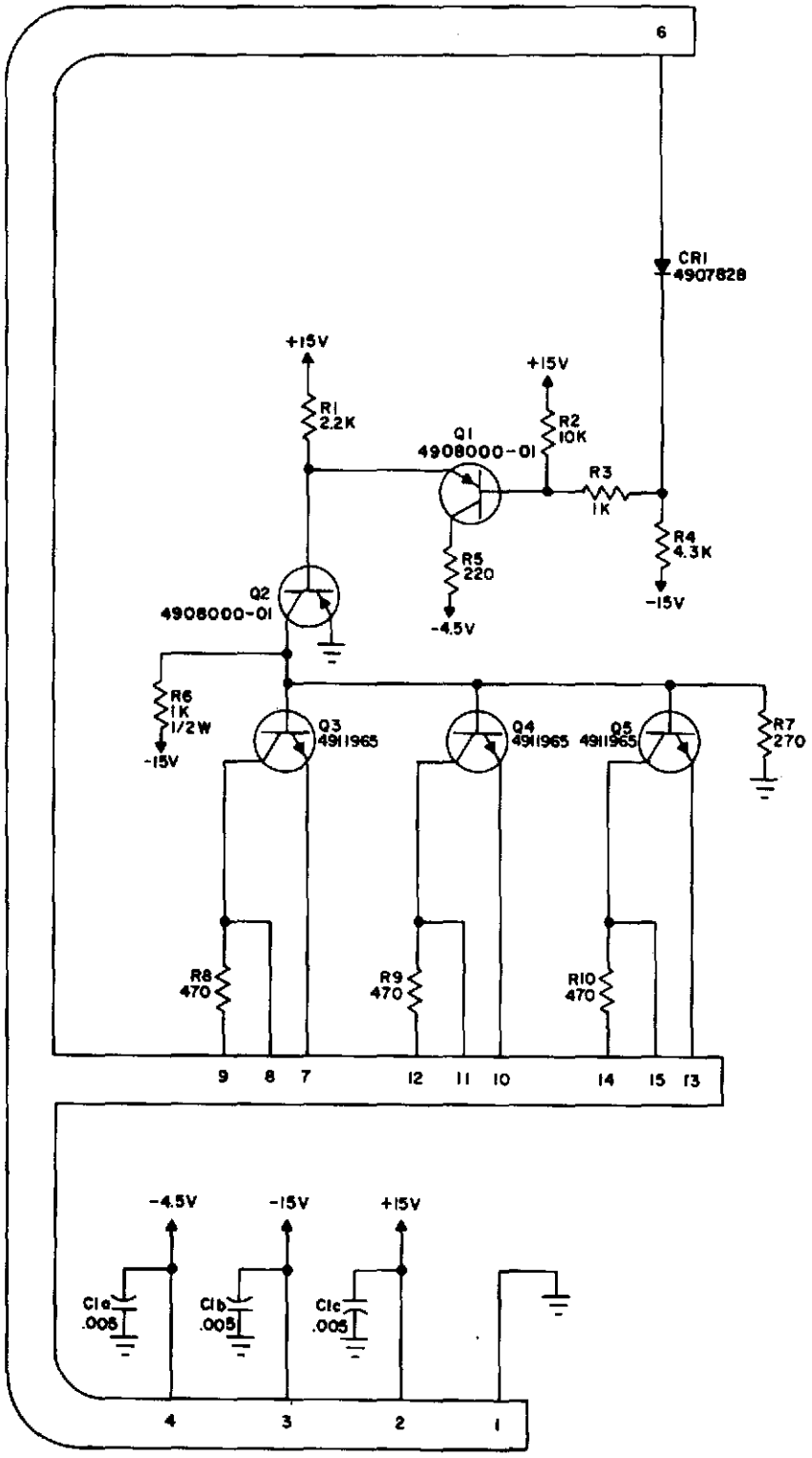


Figure 6-71. Inhibit Switch, Module Type 2210, Electrical Schematic

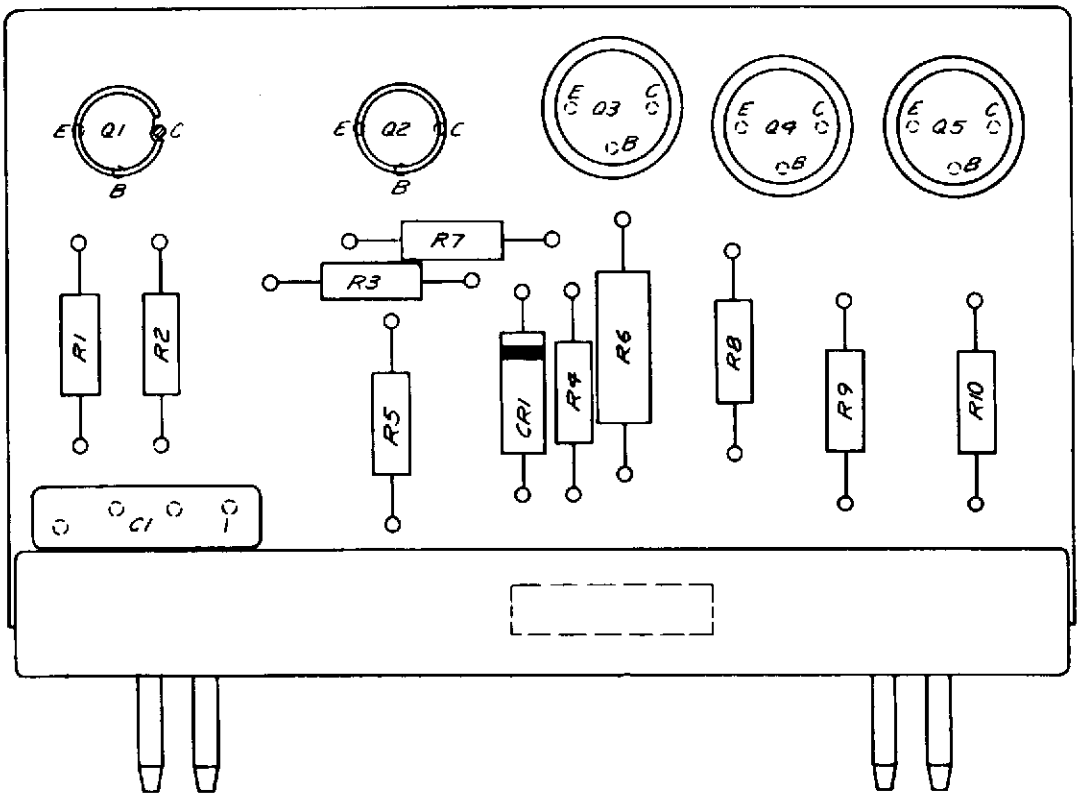


Figure 6-72. Module Type 2210 Component Layout

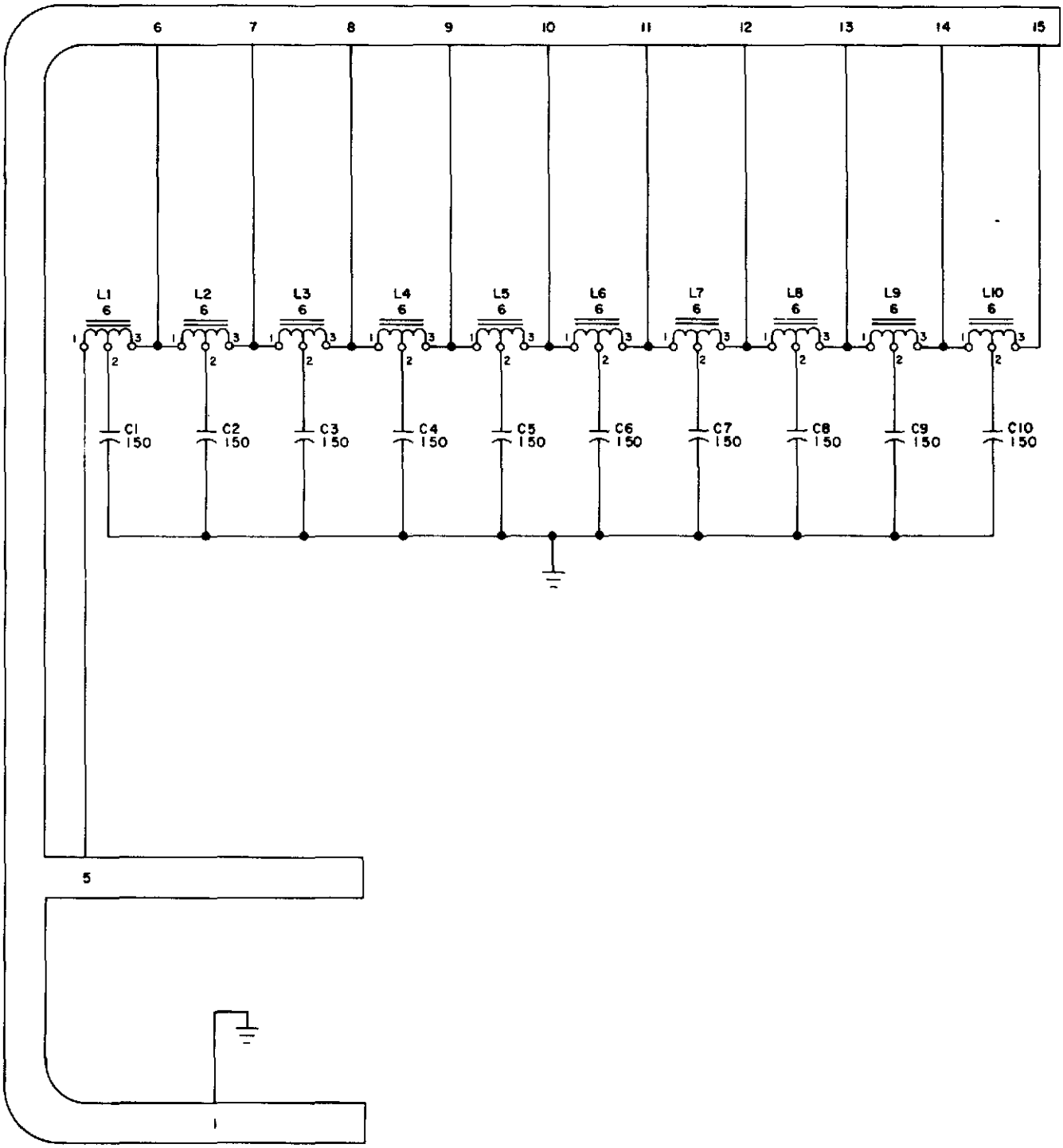


Figure 6-73. Pulse Delay Network - 3 μsec, Module Type 2350, Electrical Schematic

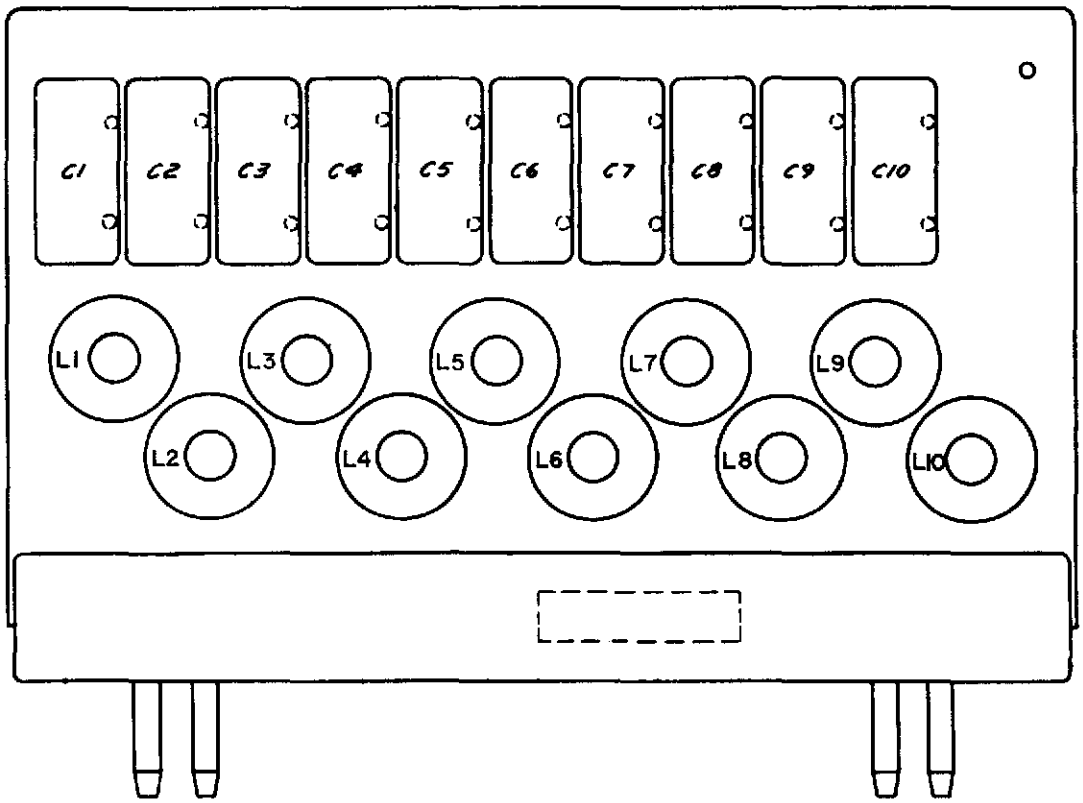


Figure 6-74. Module Type 2350 Component Layout

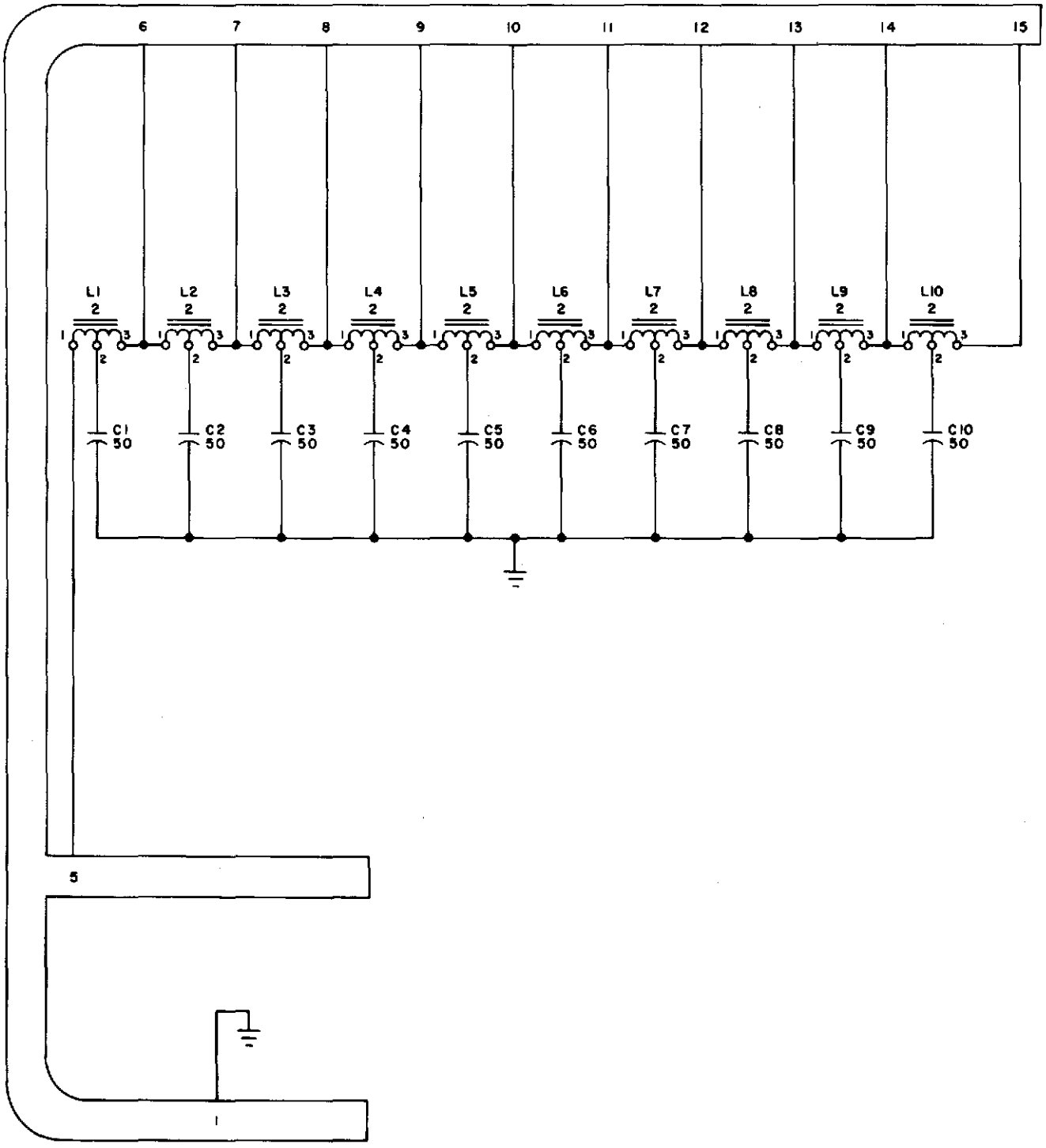


Figure 6-75. Pulse Delay Network - 1 μsec, Module Type 2360, Electrical Schematic

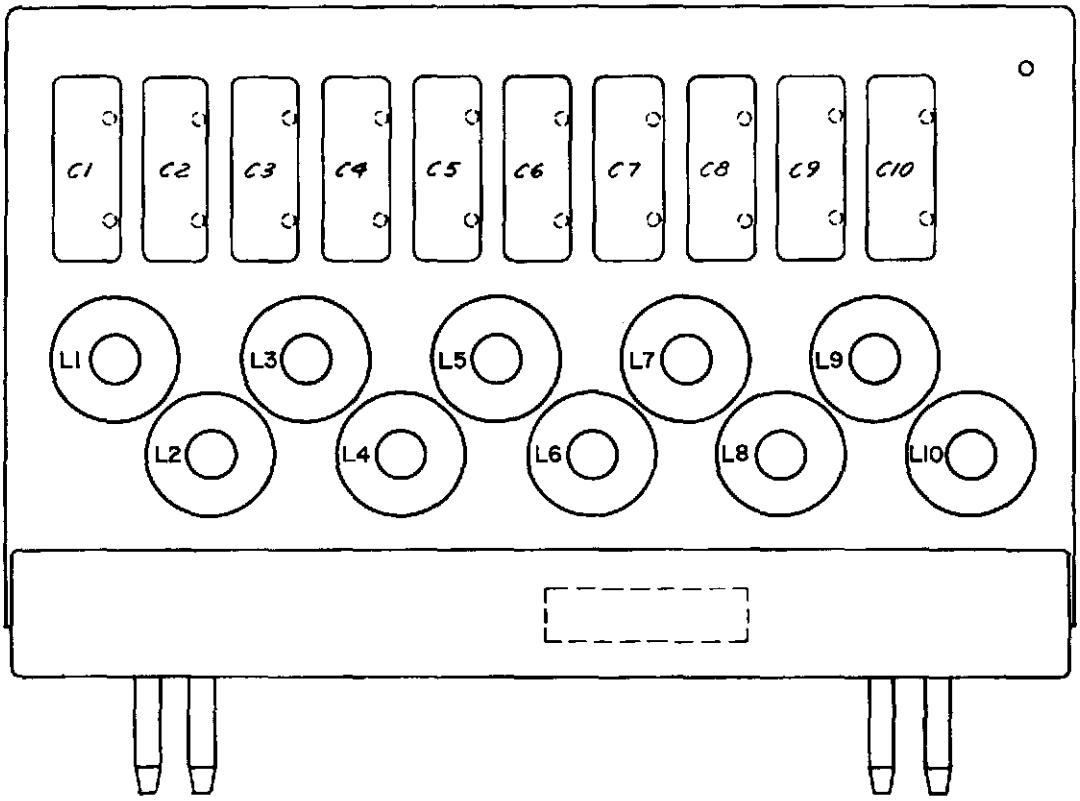


Figure 6-76. Module Type 2360 Component Layout

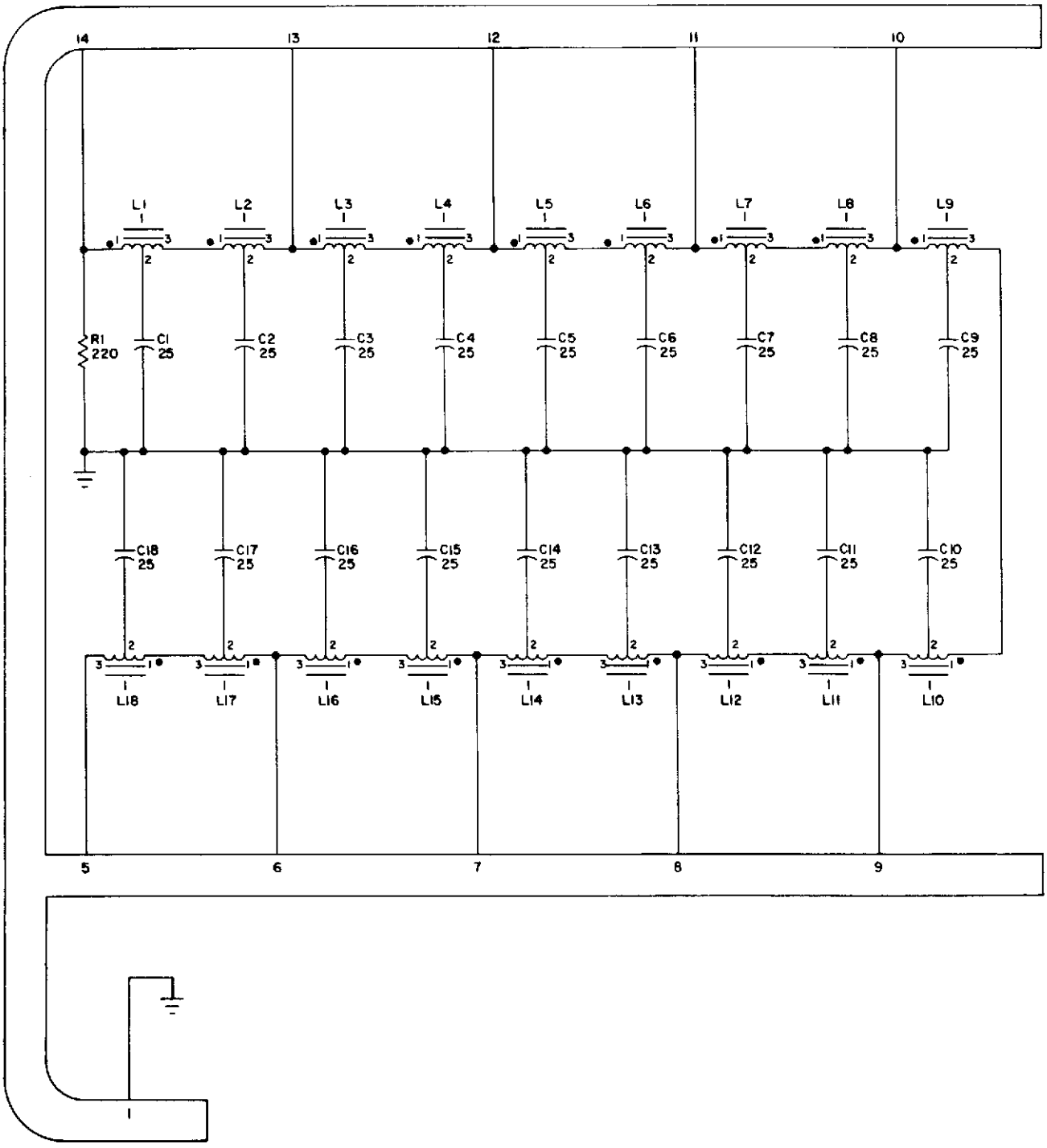


Figure 6-77. Pulse Delay Network - B, Module Type 2370, Electrical Schematic

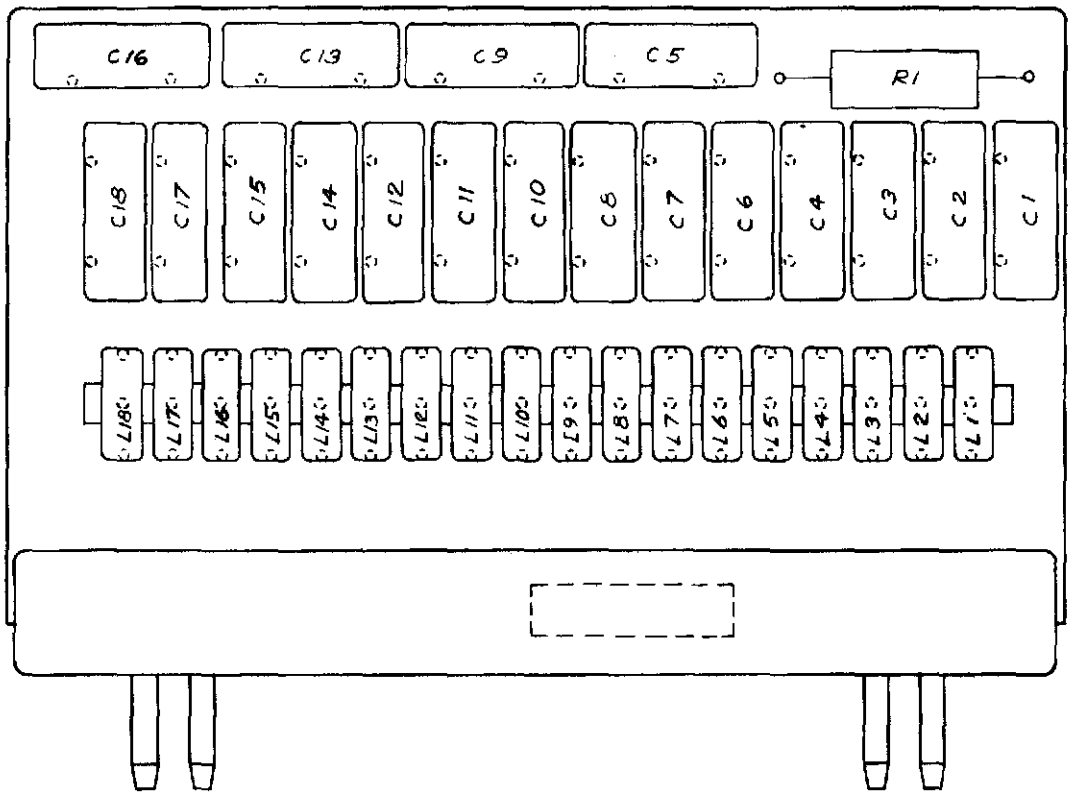


Figure 6-78. Module Type 2370 Component Layout

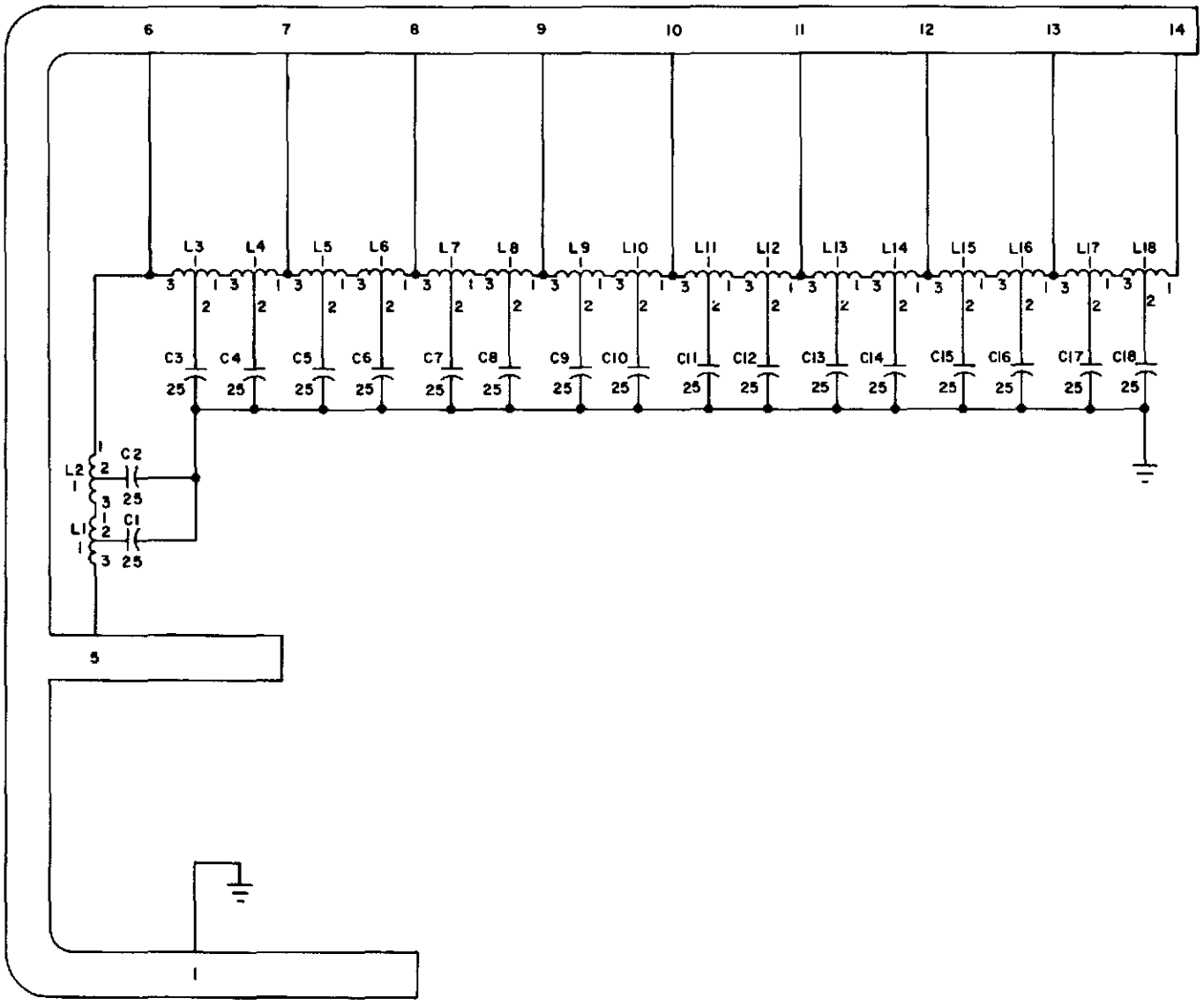


Figure 6-79. Pulse Delay Network - A, Module Type 2380, Electrical Schematic

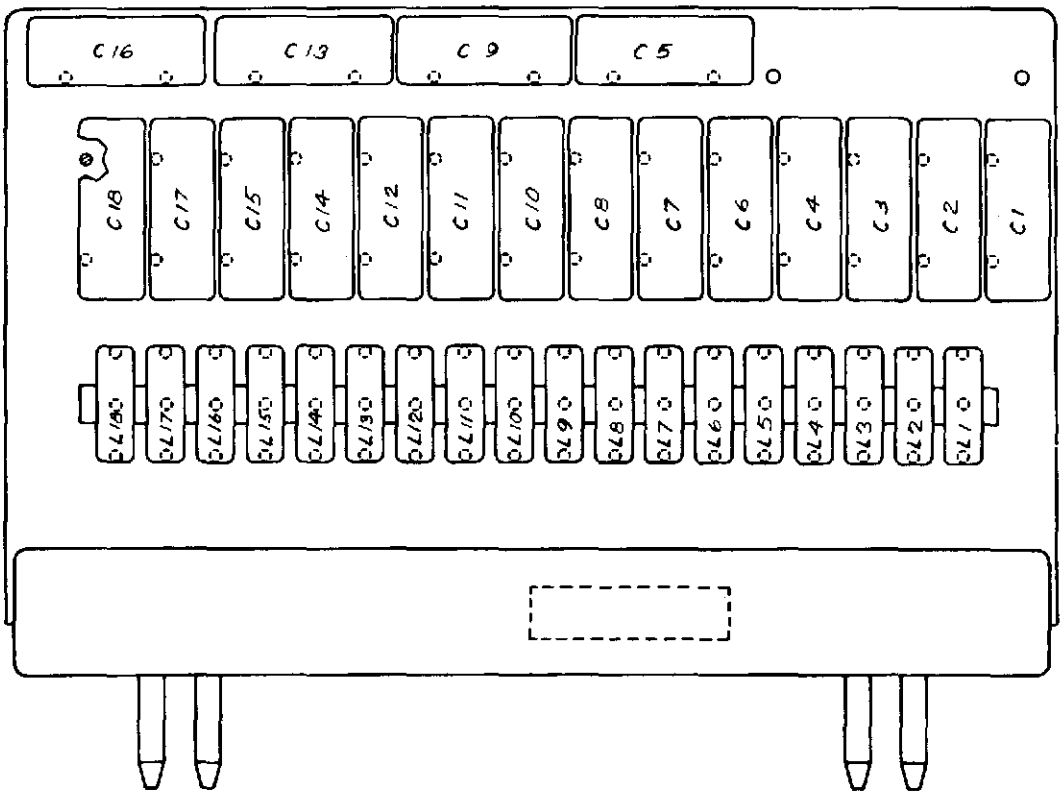


Figure 6-80. Module Type 2380 Component Layout

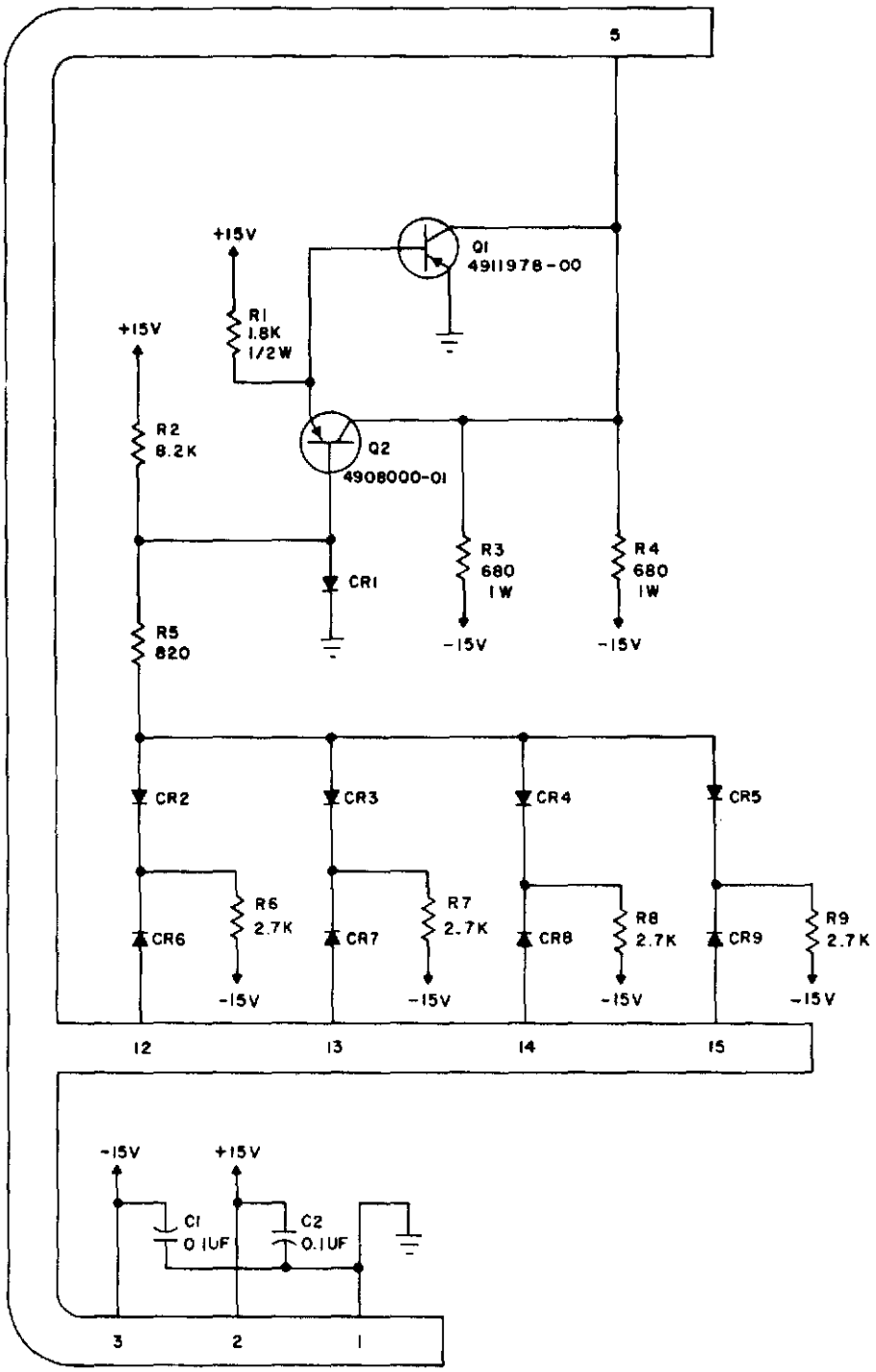


Figure 6-81. Transformer Selector - A, Module Type 2390, Electrical Schematic

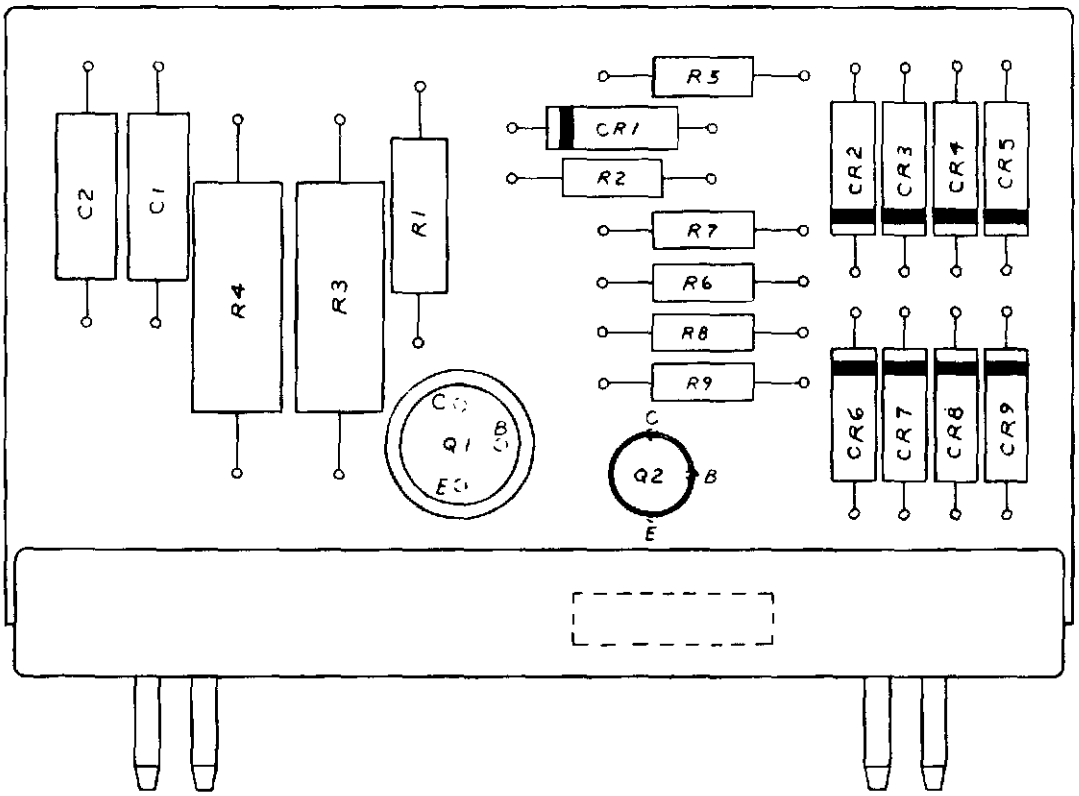


Figure 6-82. Module Type 2390 Component Layout

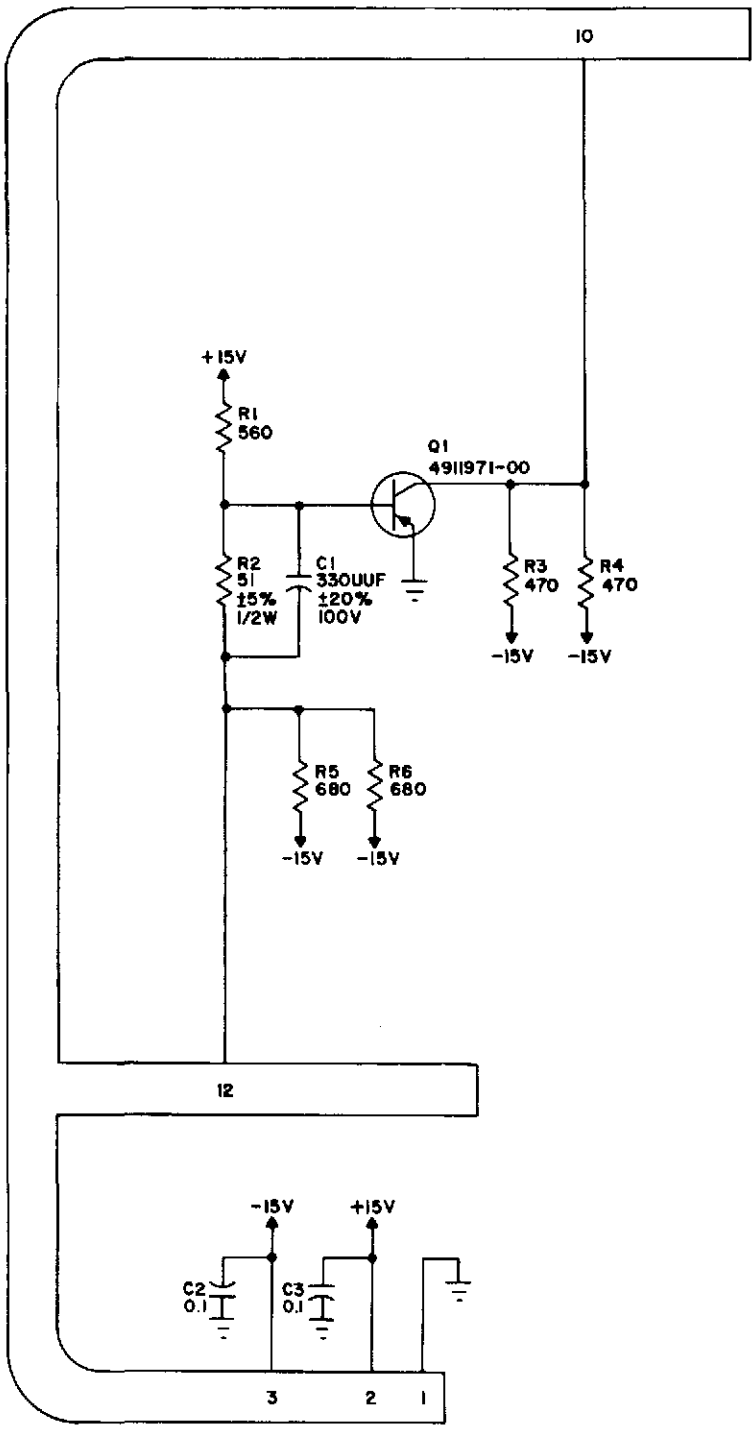


Figure 6-83. Transformer Selector - B, Module Type 2400, Electrical Schematic

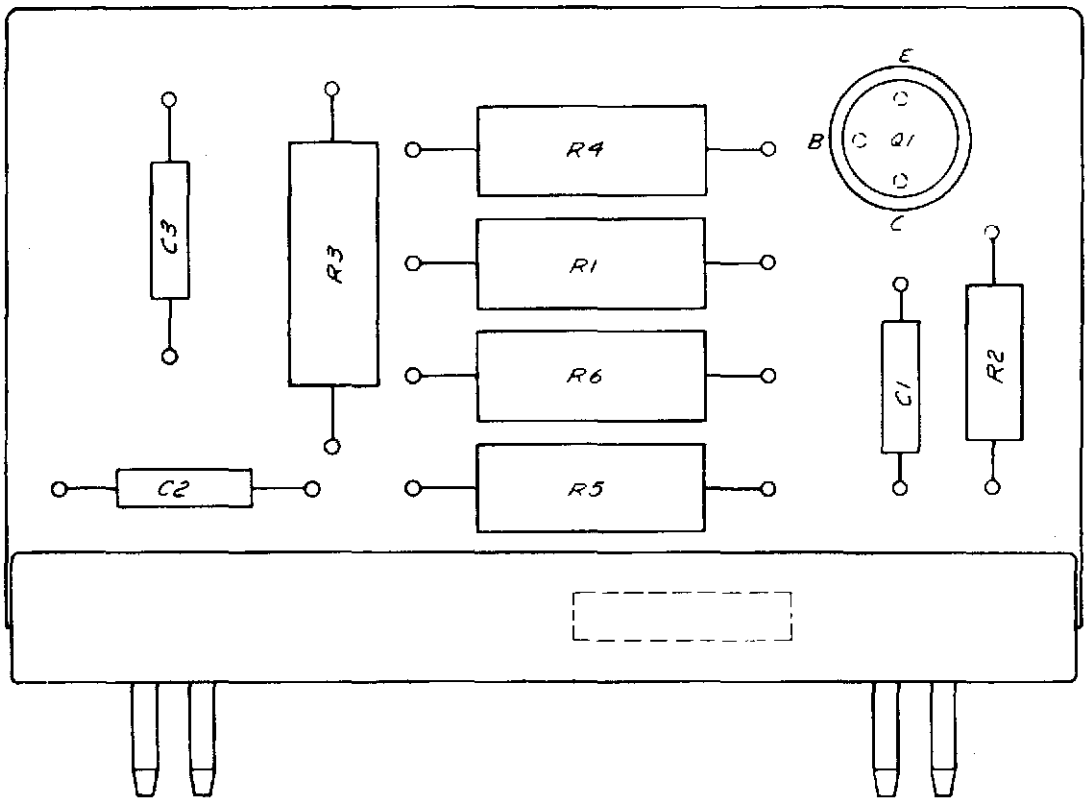


Figure 6-84. Module Type 2400 Component Layout

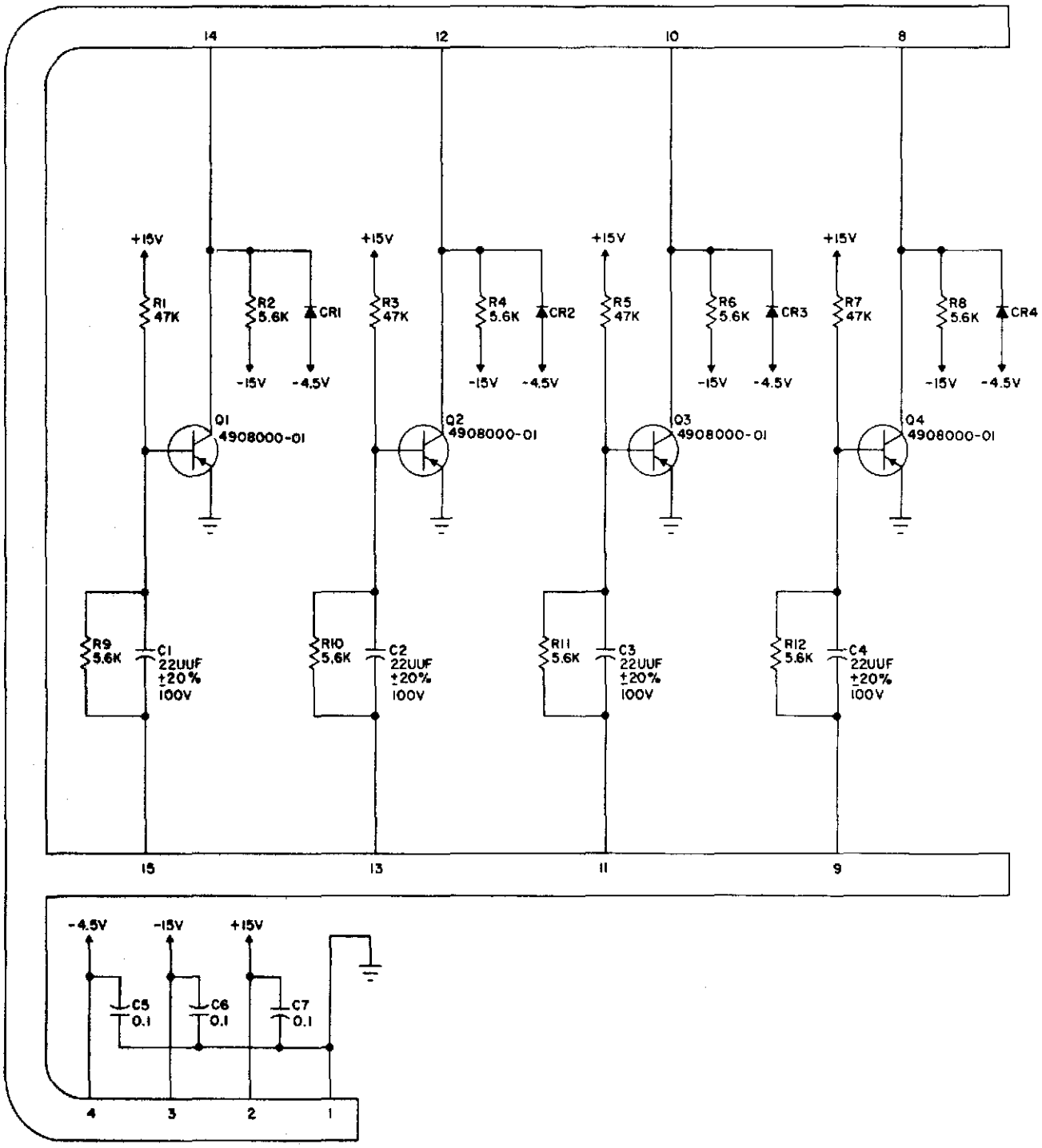


Figure 6-85. Impedance Matching, Module Type 2410, Electrical Schematic

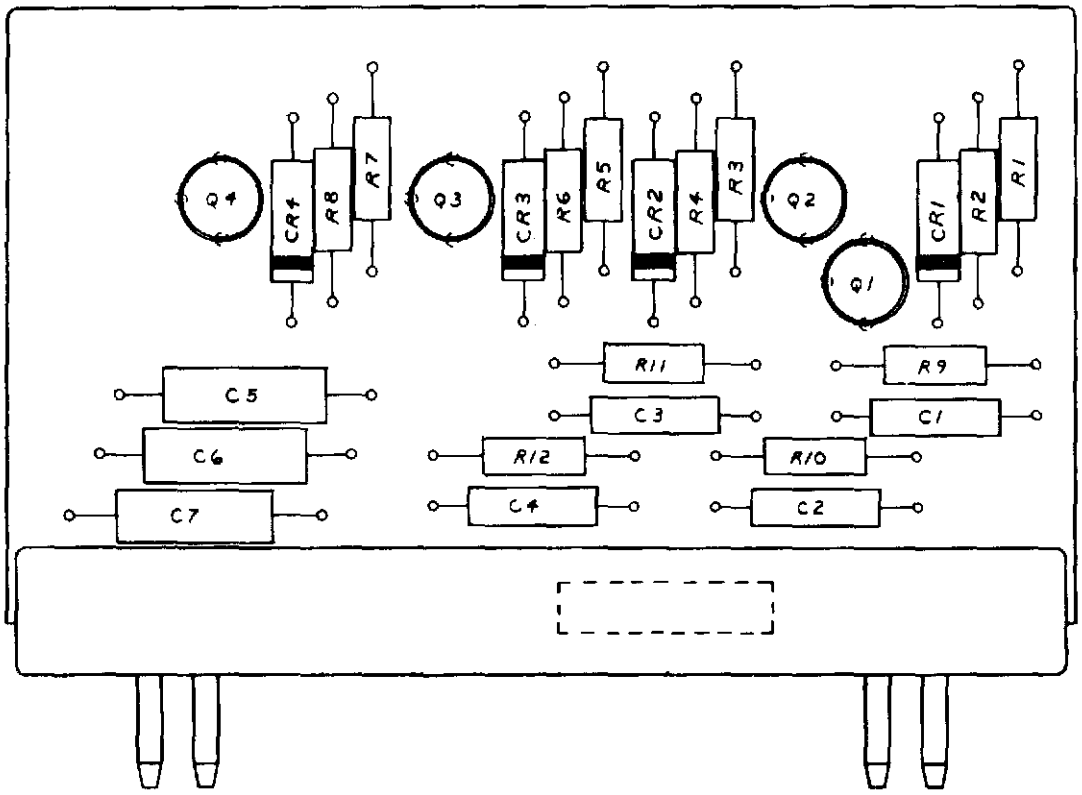


Figure 6-86. Module Type 2410 Component Layout

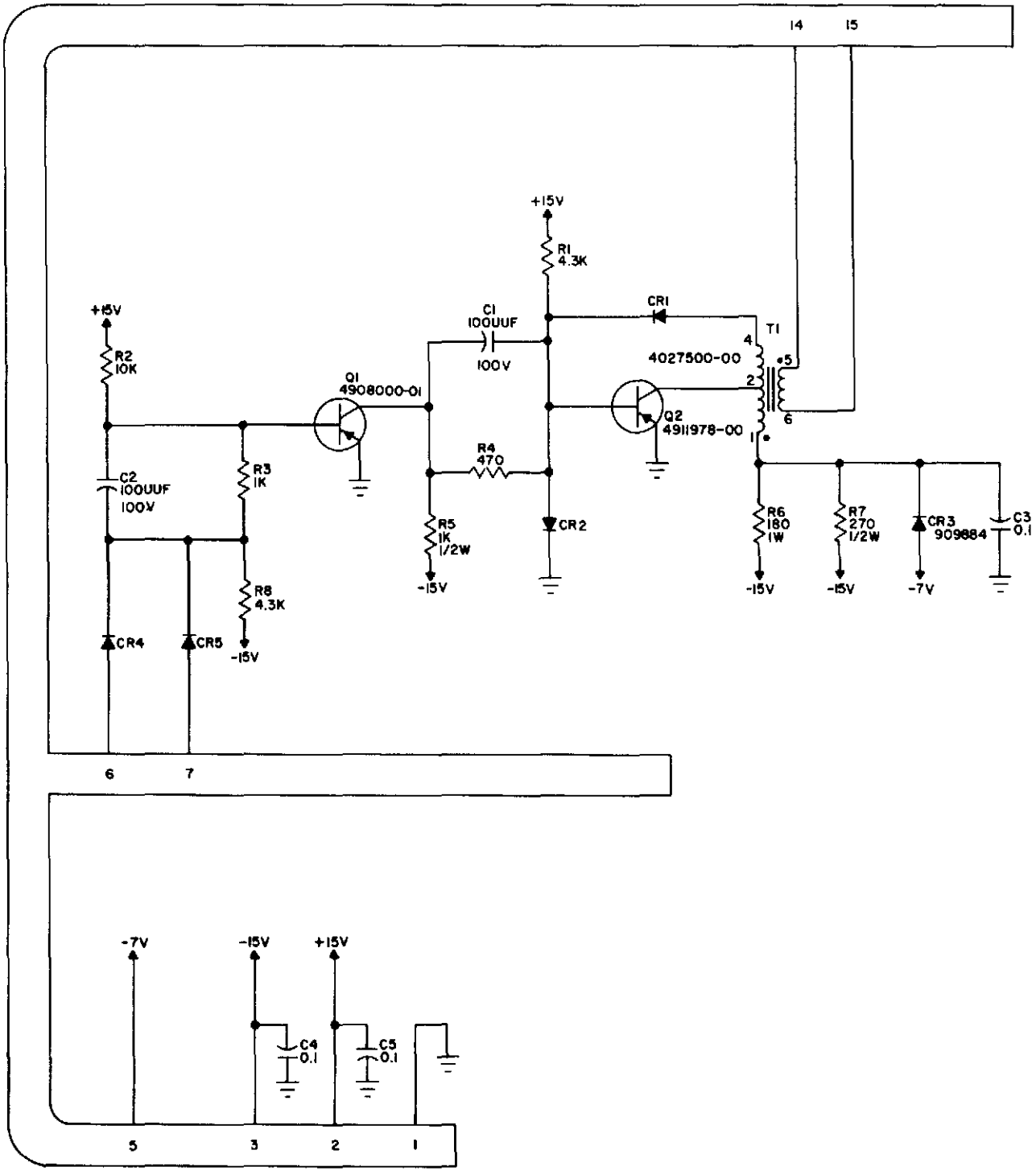


Figure 6-87. Pulse-Reset Amplifier, Module Type 2420, Electrical Schematic

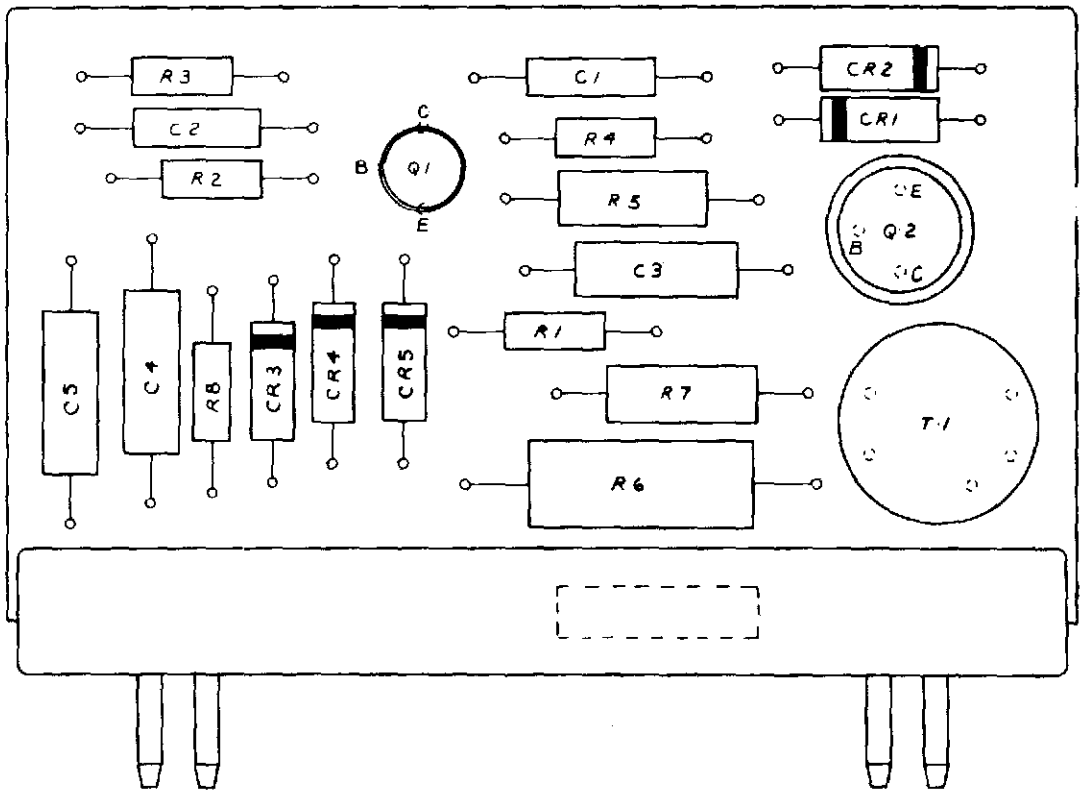


Figure 6-88. Module Type 2420 Component Layout

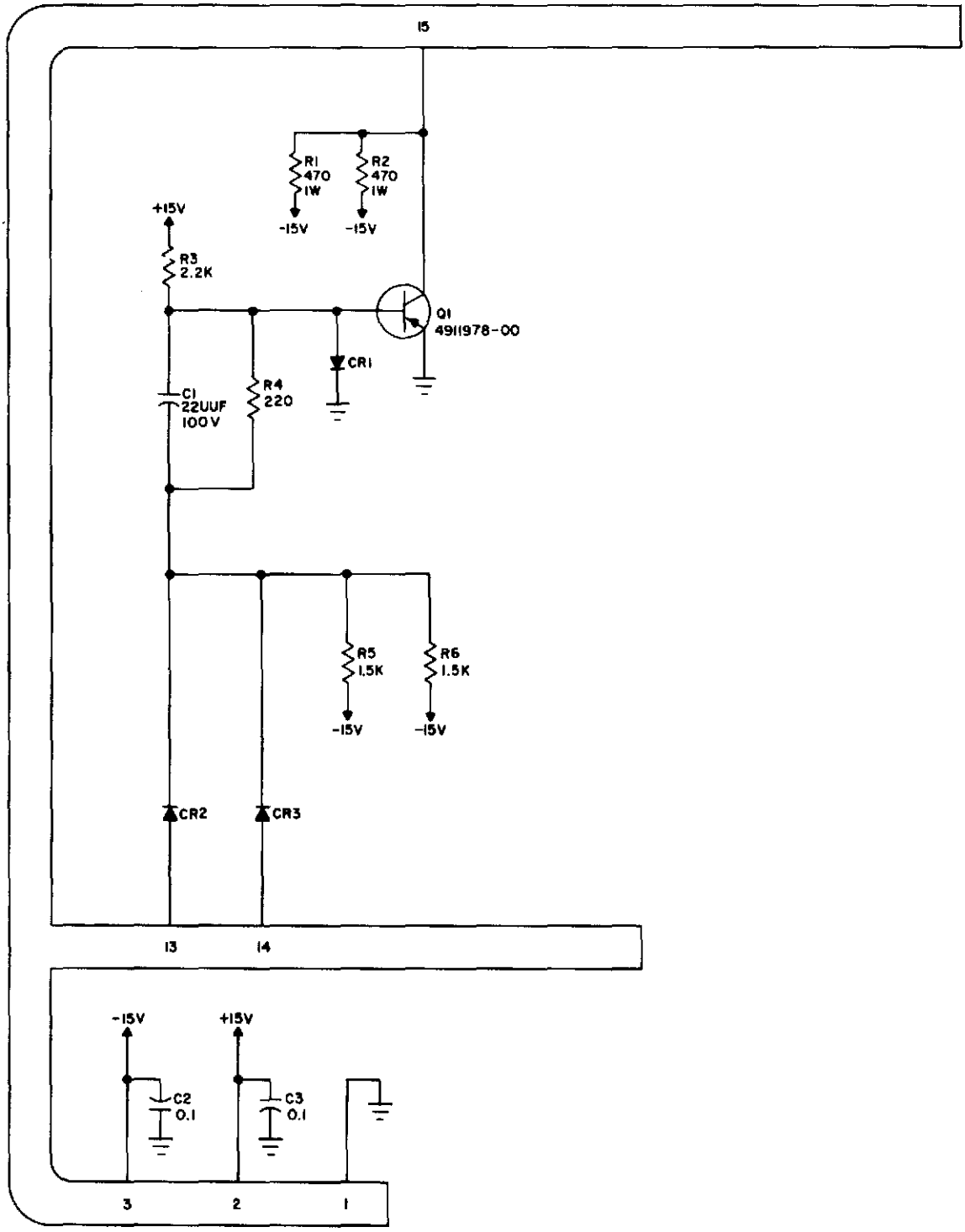


Figure 6-89. Delay Line Drawer, Module Type 2430, Electrical Schematic

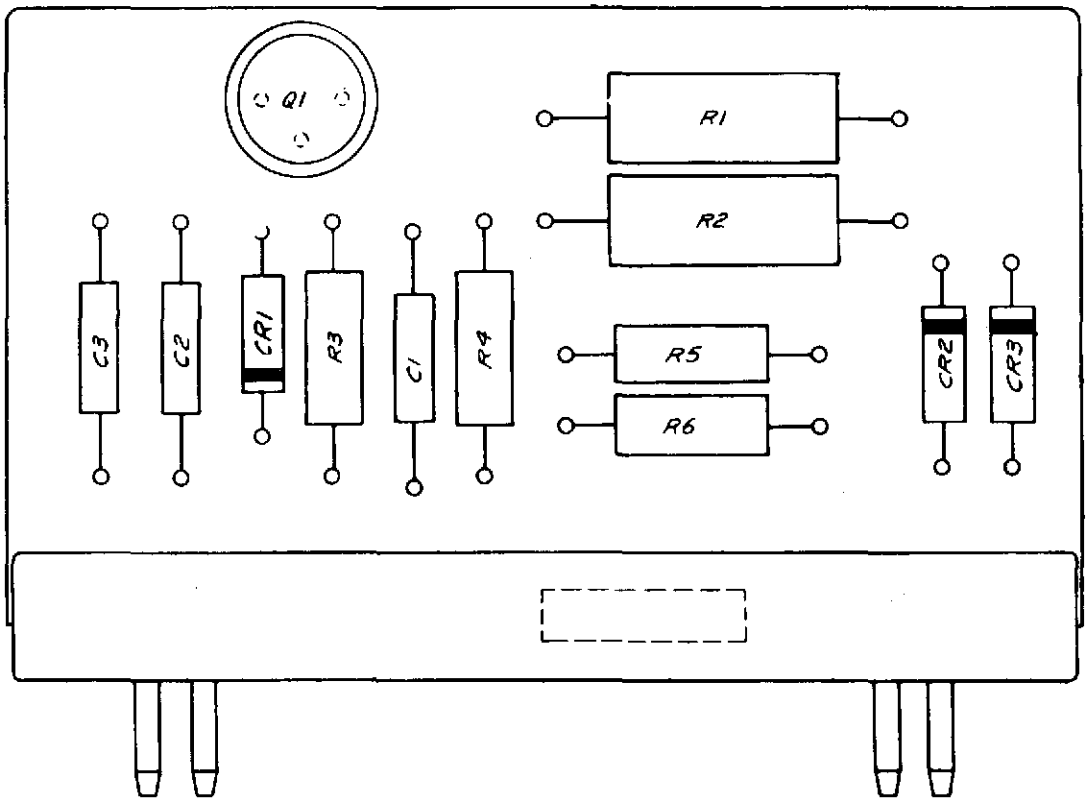


Figure 6-90. Module Type 2430 Component Layout

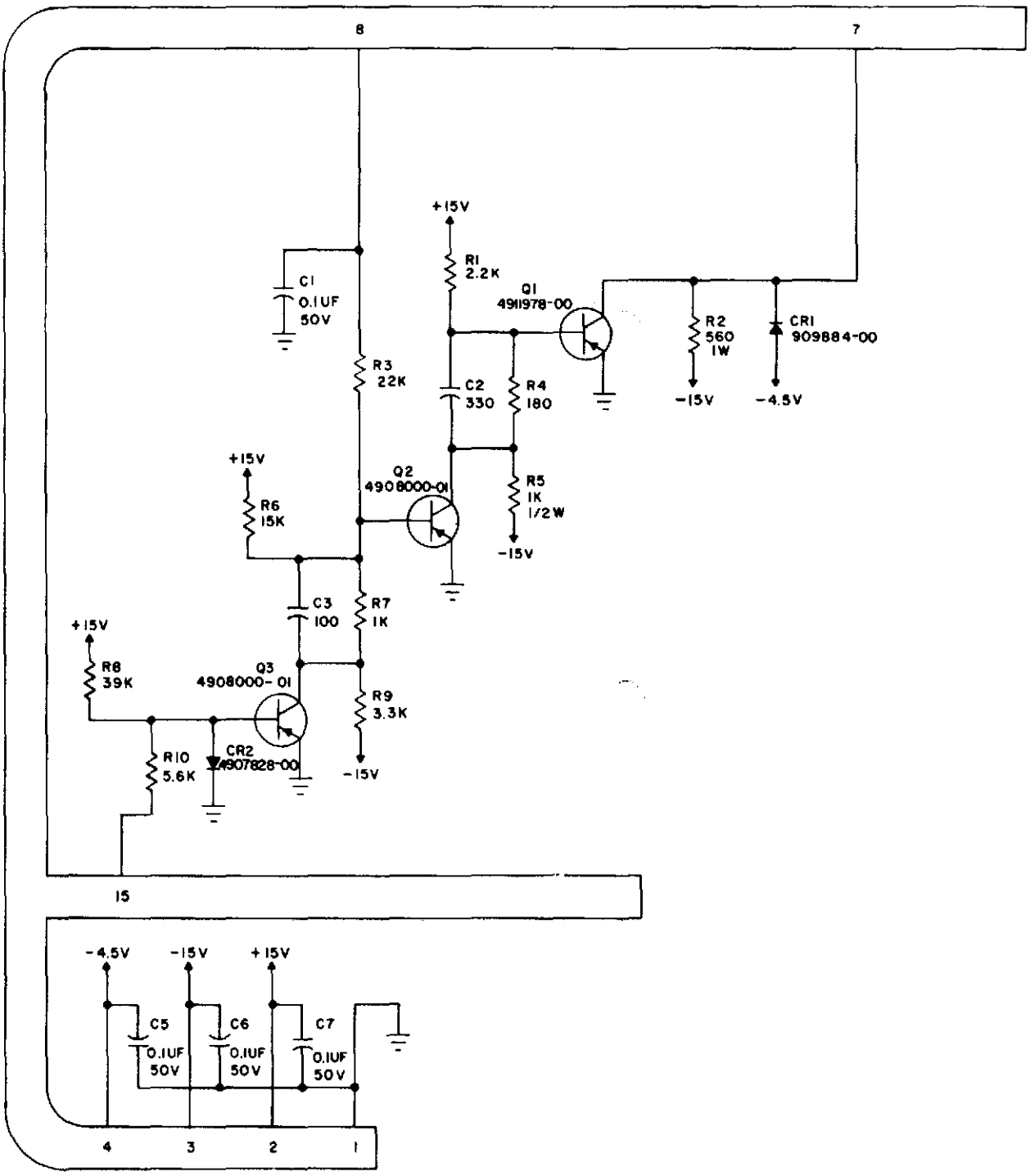


Figure 6-91. Strobe Pulse Amplifier, Module Type 2440, Electrical Schematic

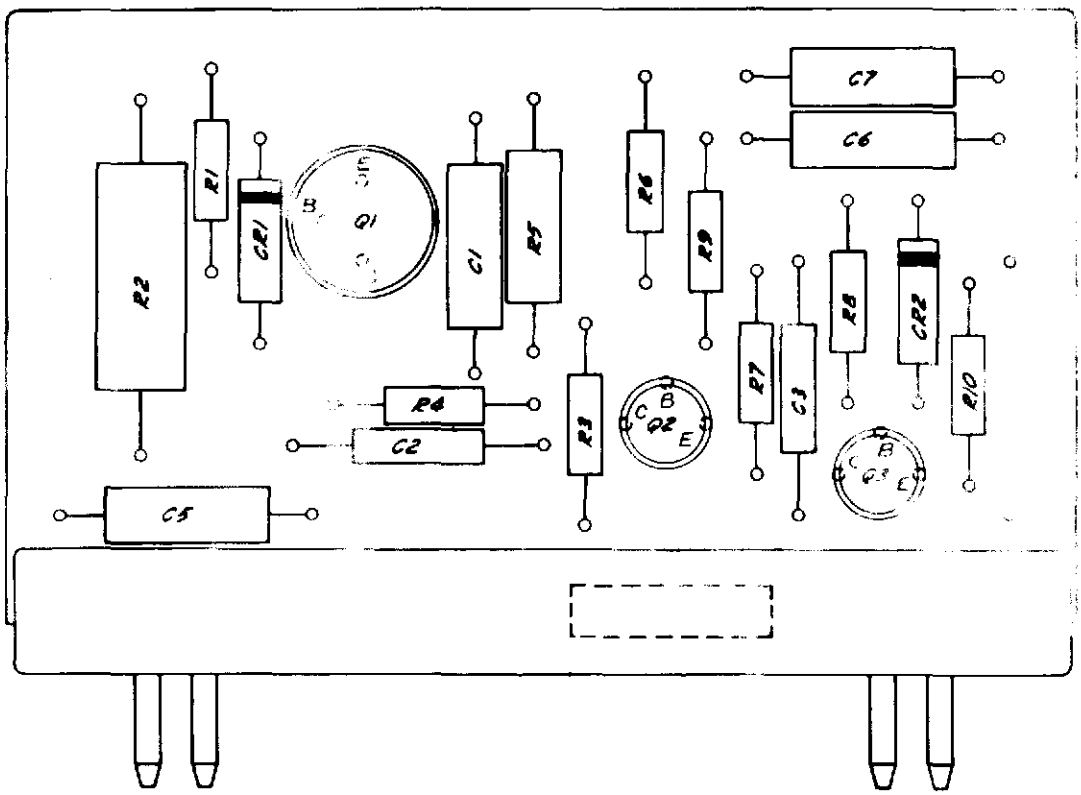


Figure 6-92. Module Type 2440 Component Layout

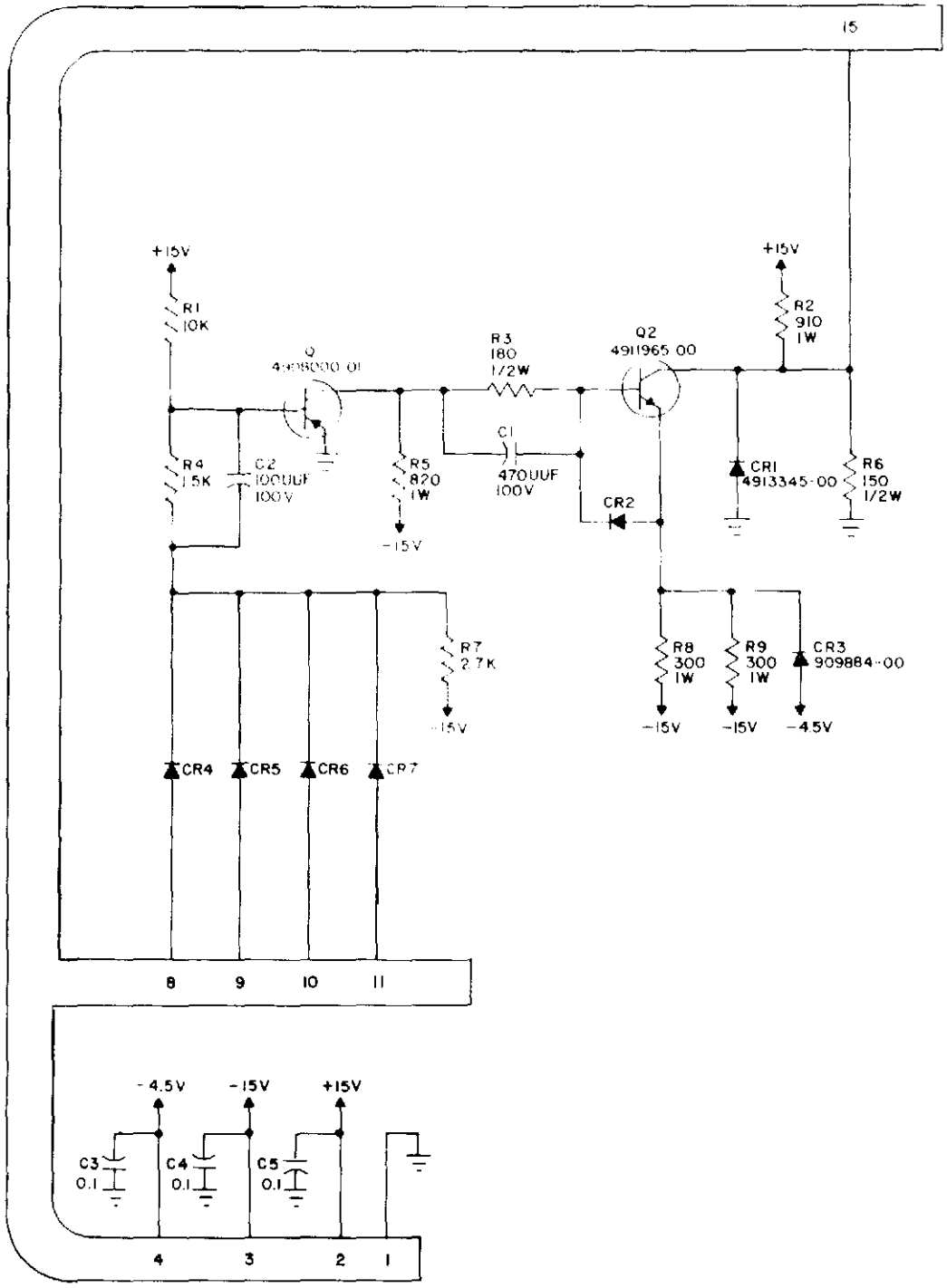


Figure 6-93. Word Current Translator, Module Type 2450, Electrical Schematic

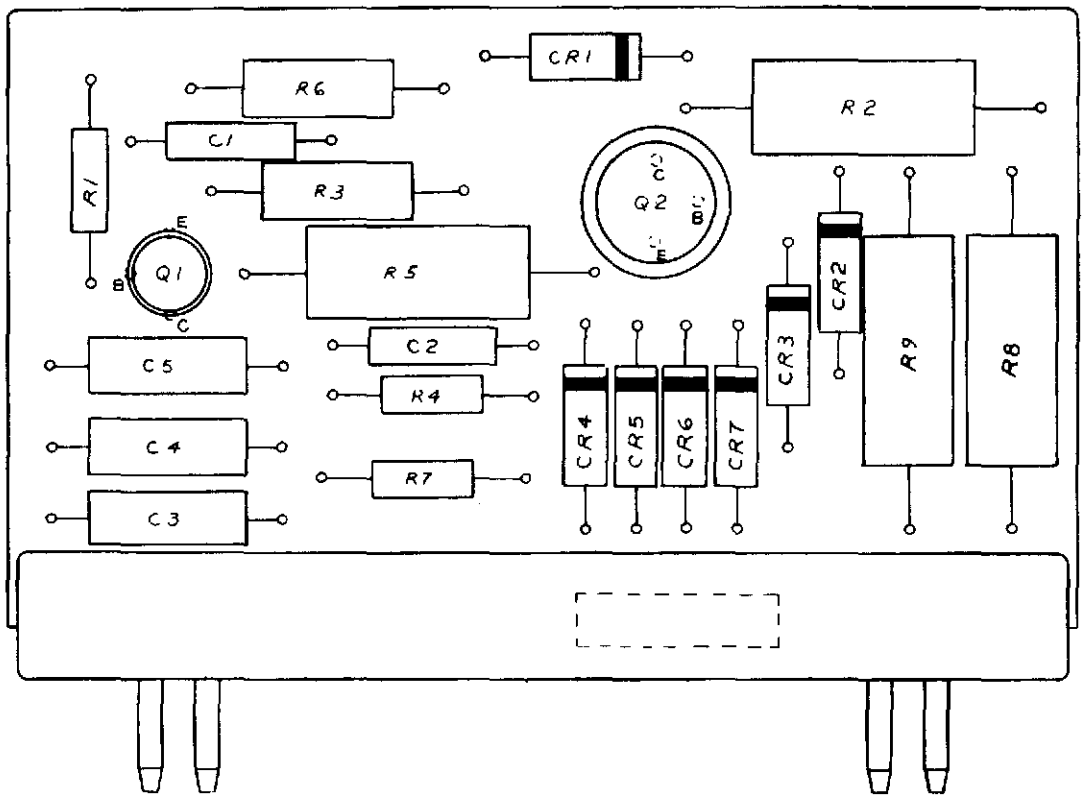


Figure 6-94. Module Type 2450 Component Layout

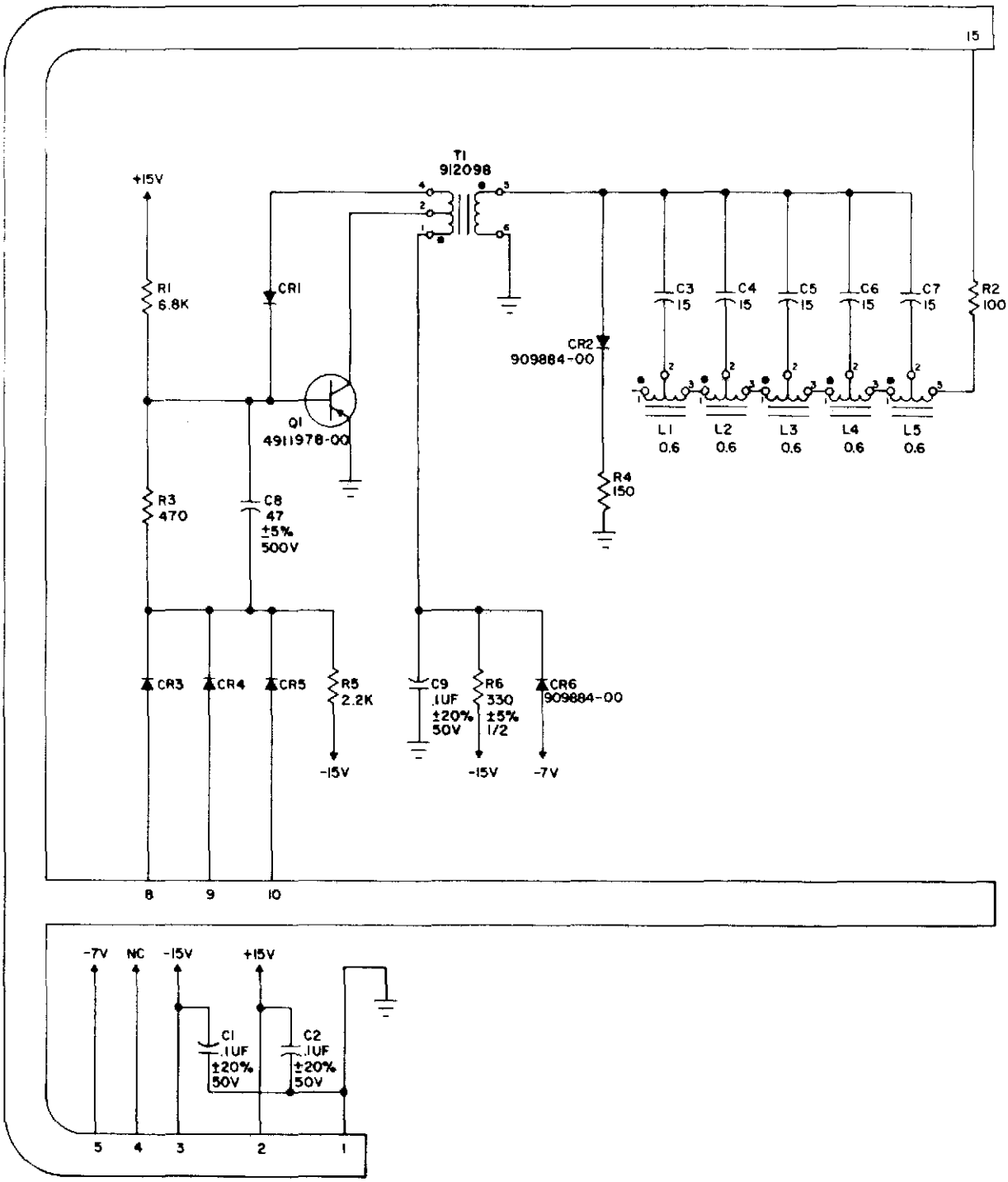


Figure 6-95. Strobe Pulse Shaper - A, Module Type 2460, Electrical Schematic

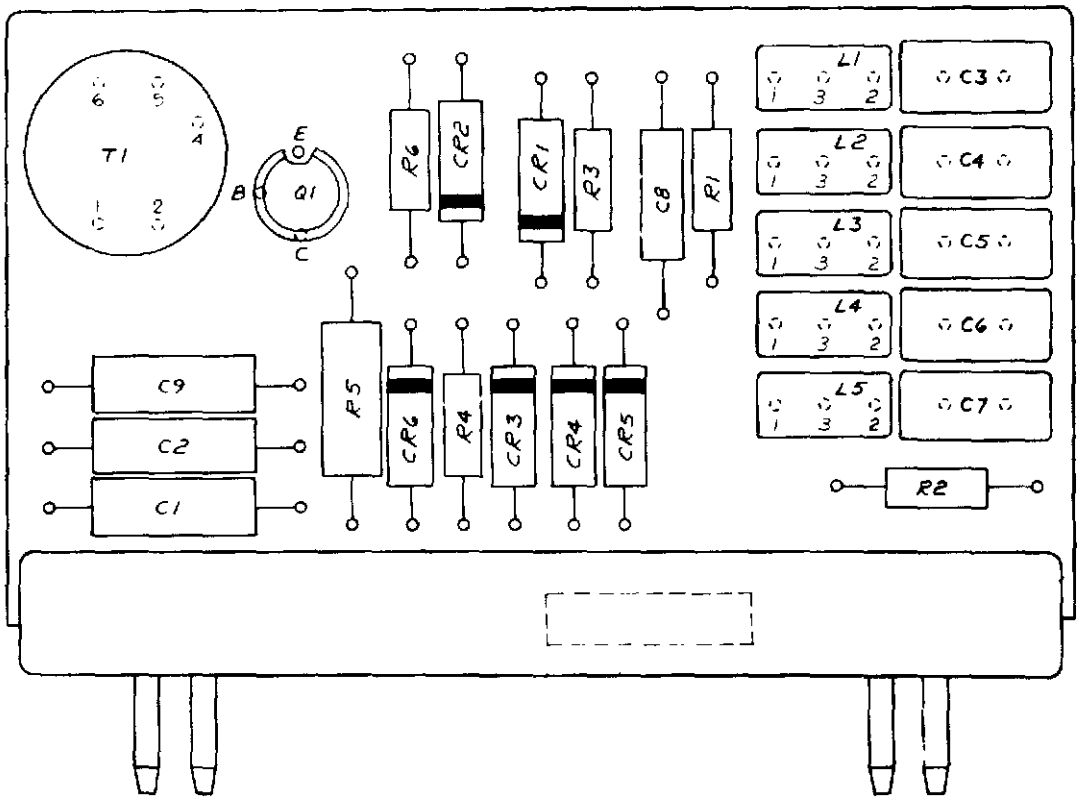


Figure 6-96. Module Type 2460 Component Layout

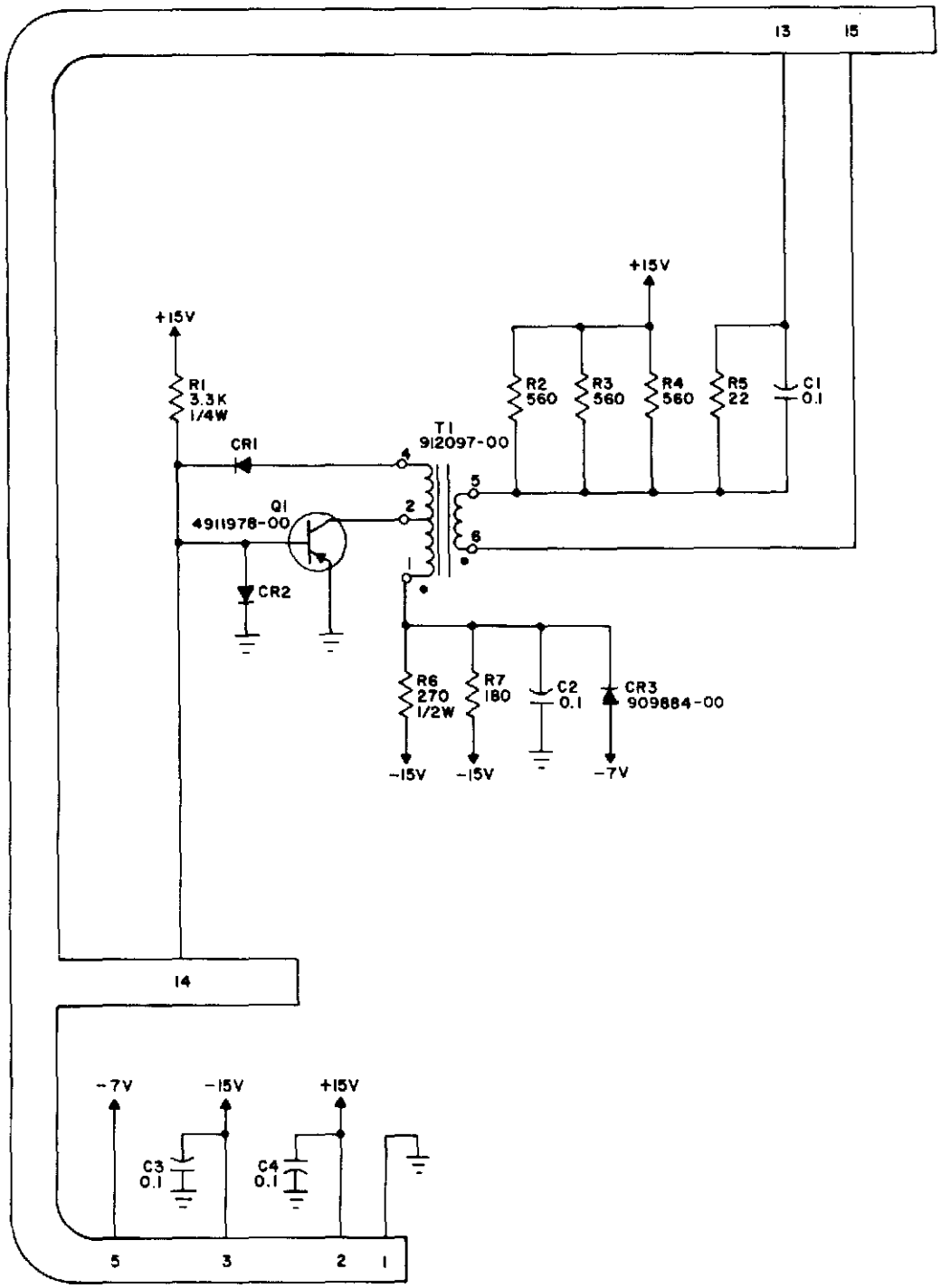


Figure 6-97. Strobe Pulse Shaper - B, Module Type 2470, Electrical Schematic

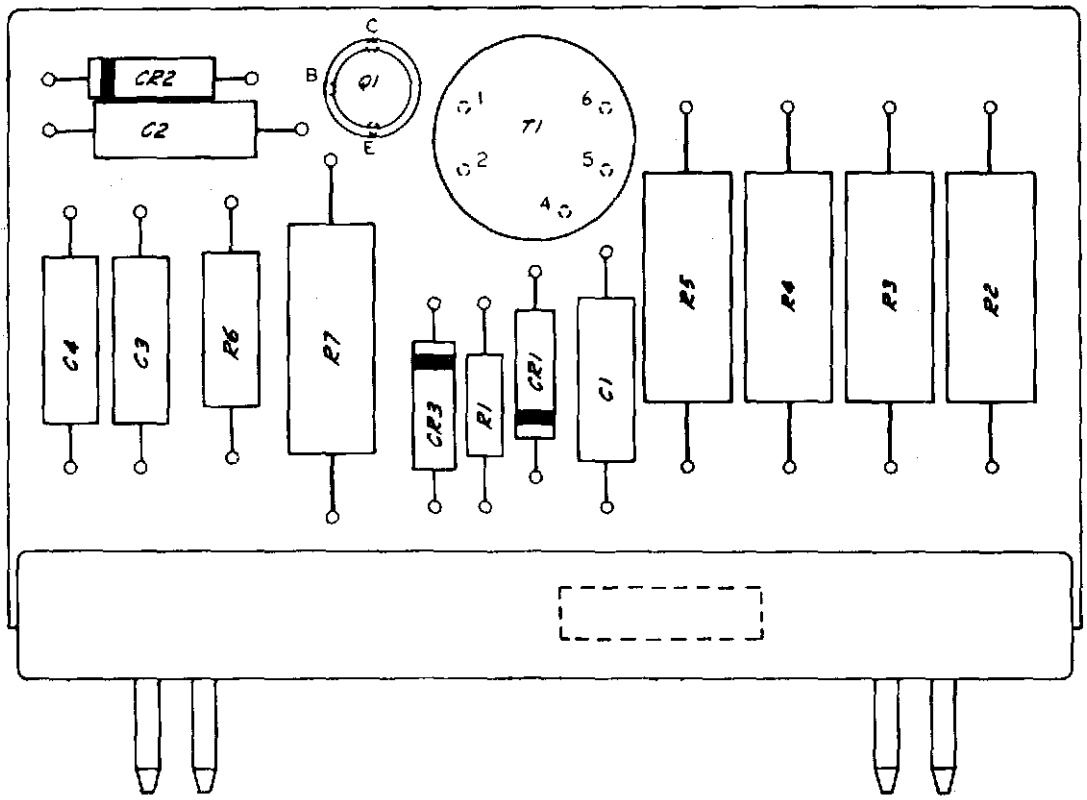


Figure 6-98. Module Type 2470 Component Layout

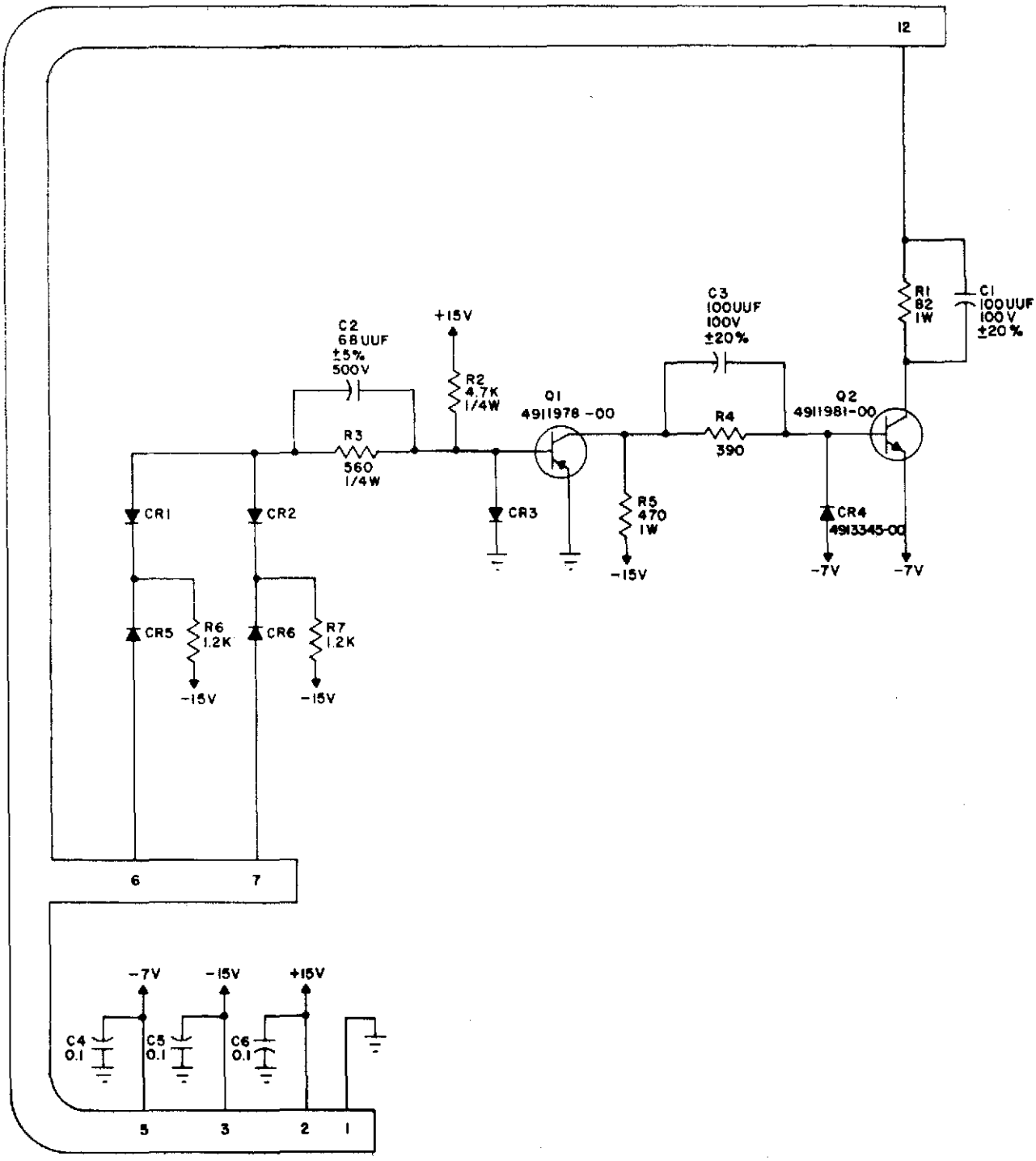


Figure 6-99. Word Current Generator - A, Module Type 2480, Electrical Schematic

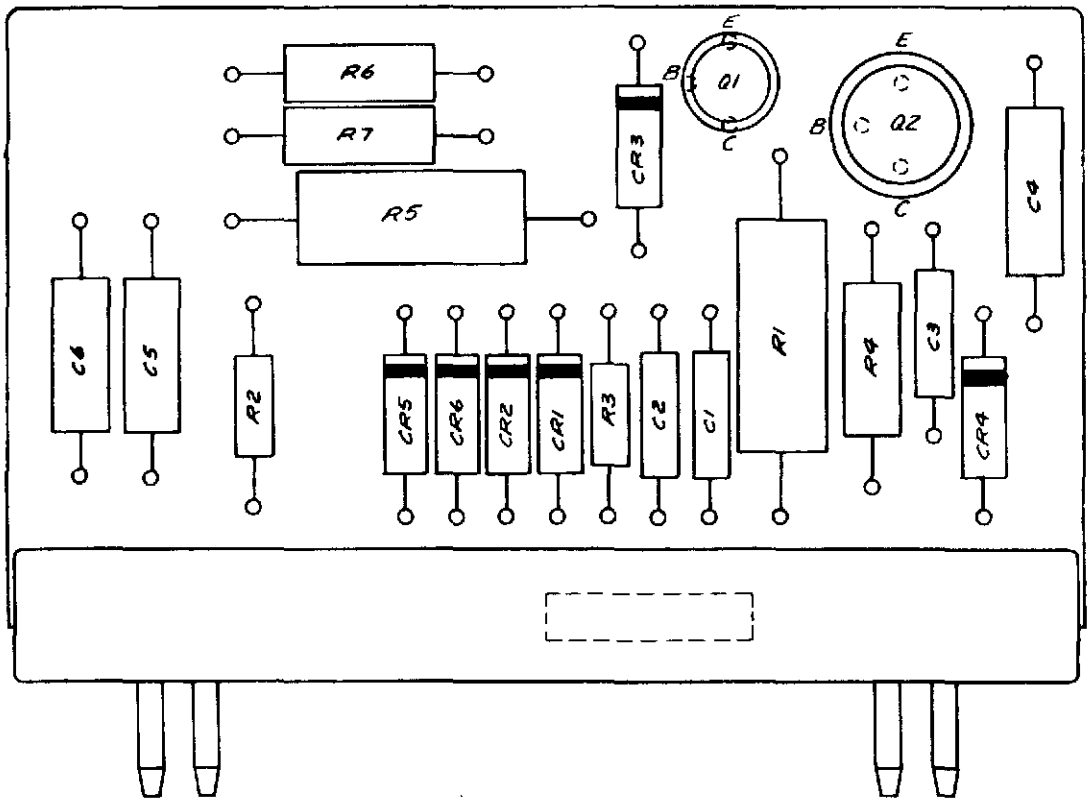


Figure 6-100. Module Type 2480 Component Layout

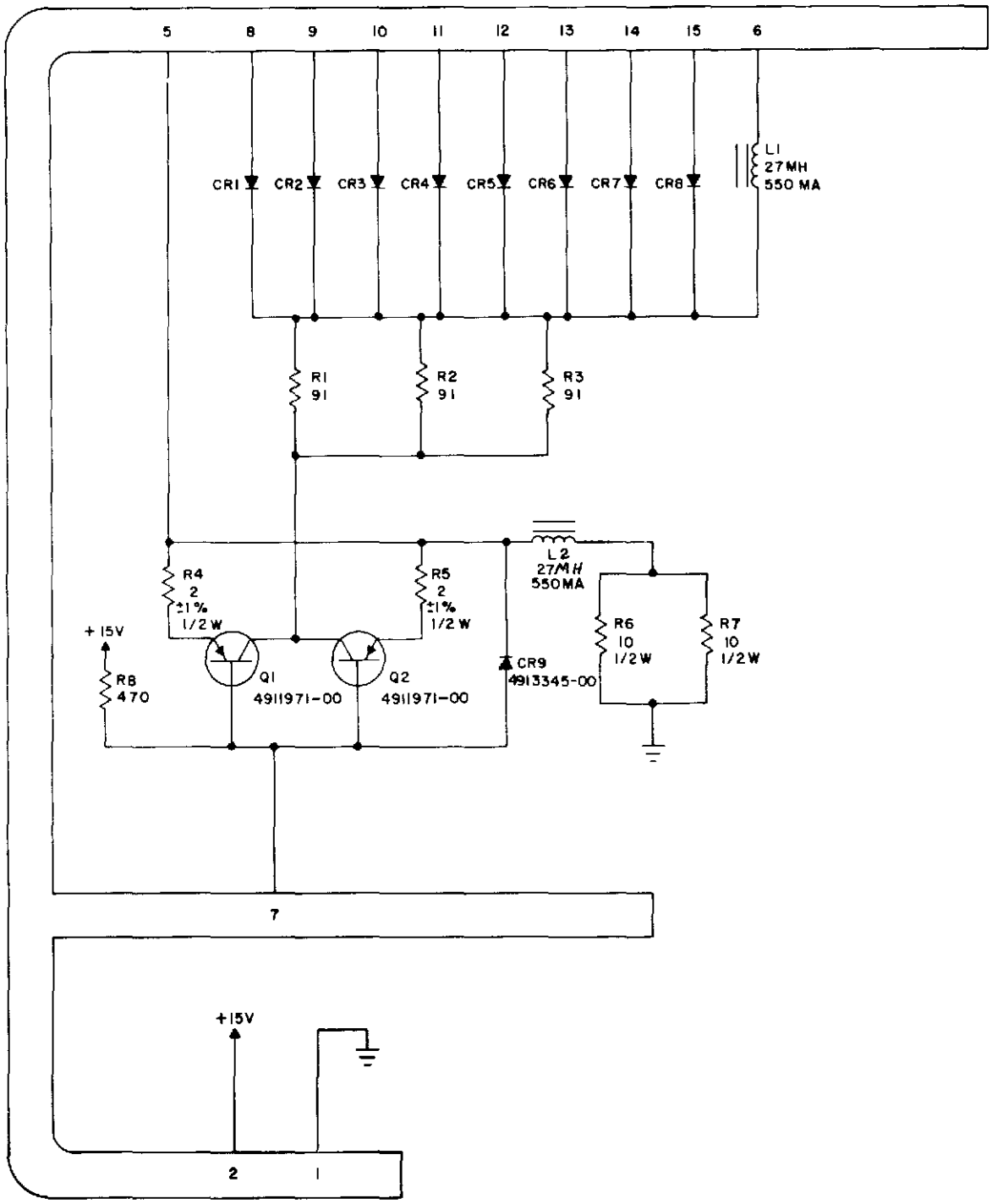


Figure 6-101. Word Current Generator - B, Module Type 2490, Electrical Schematic

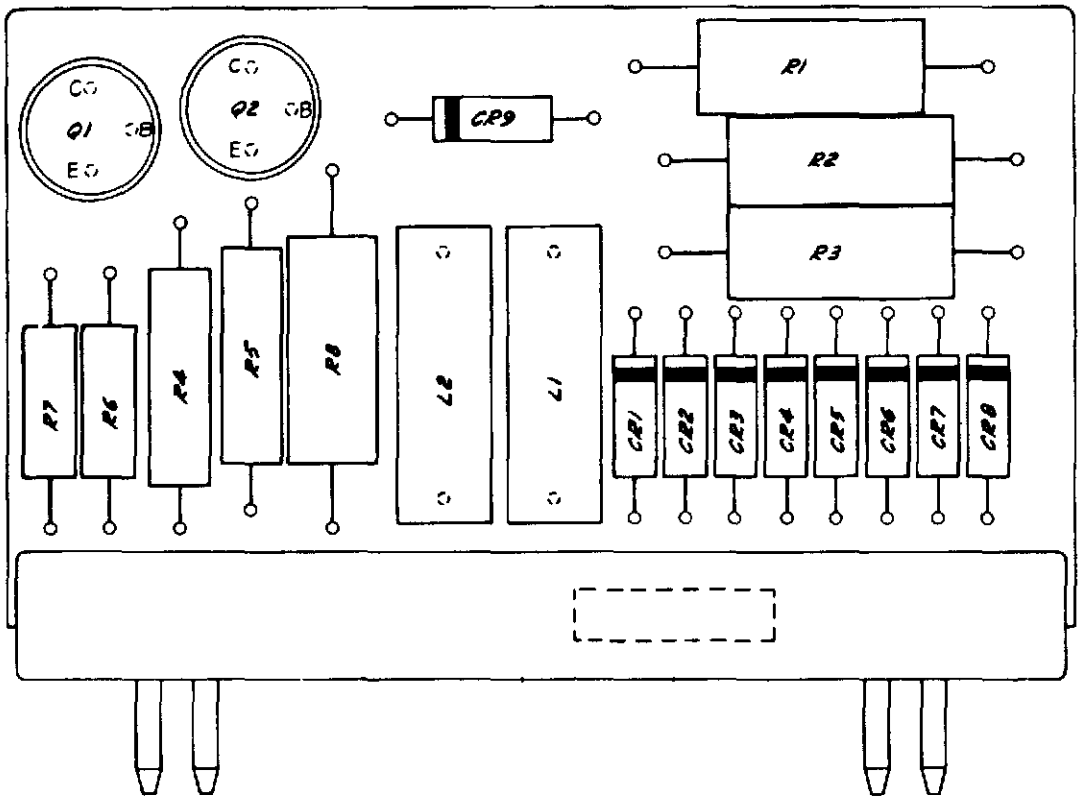


Figure 6-102. Module Type 2490 Component Layout

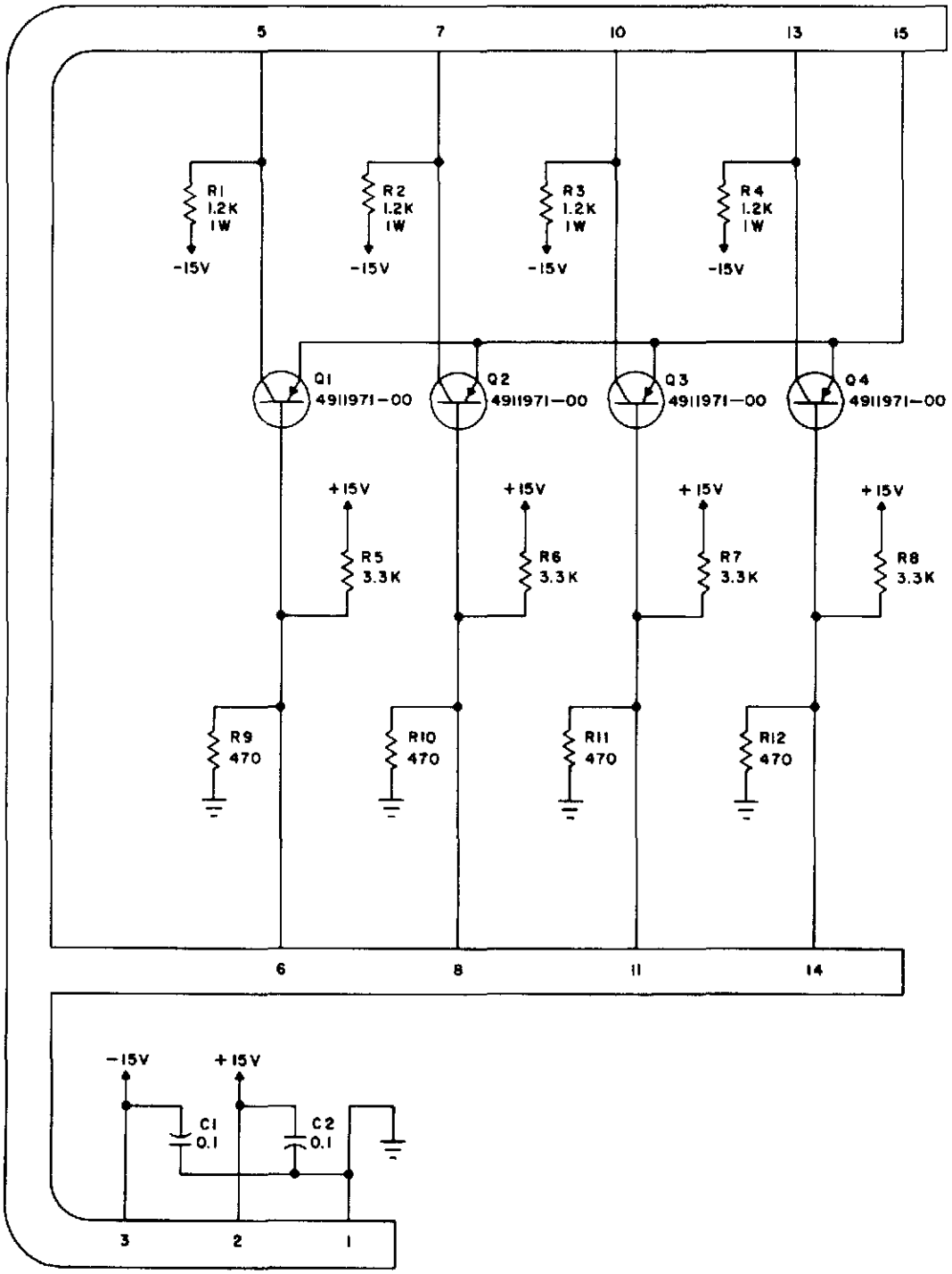


Figure 6-103. Word Current Diverter, Module Type 2500, Electrical Schematic

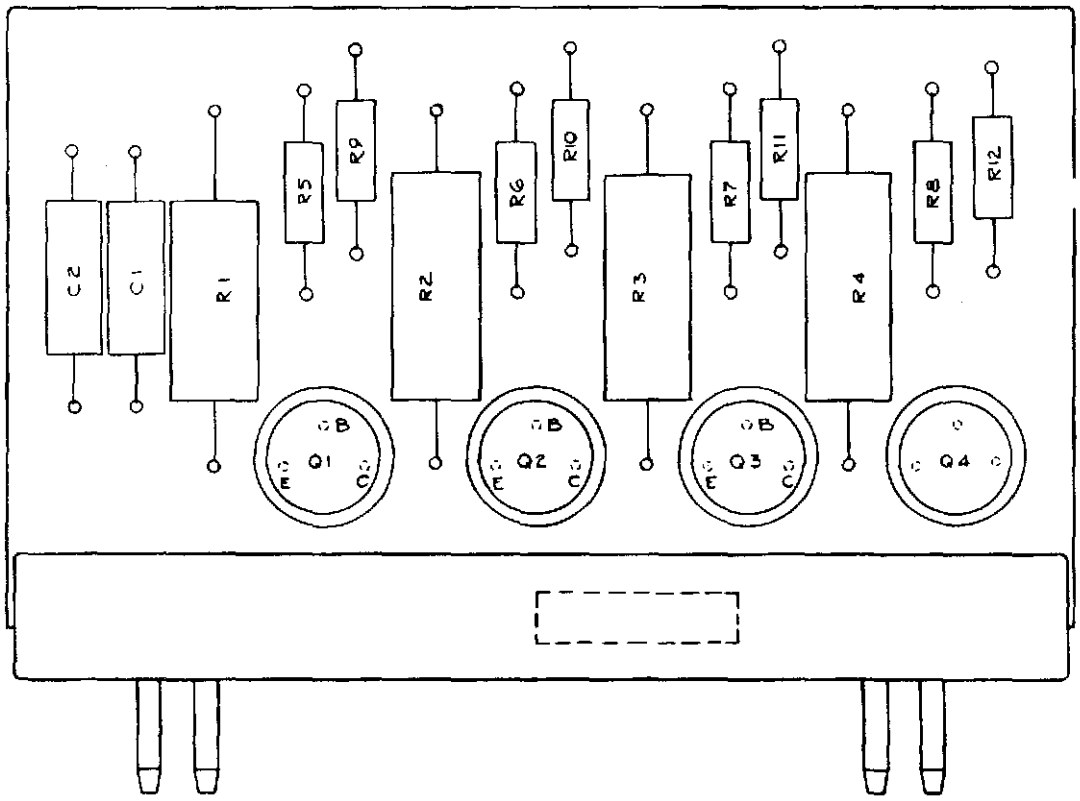


Figure 6-104. Module Type 2500 Component Layout

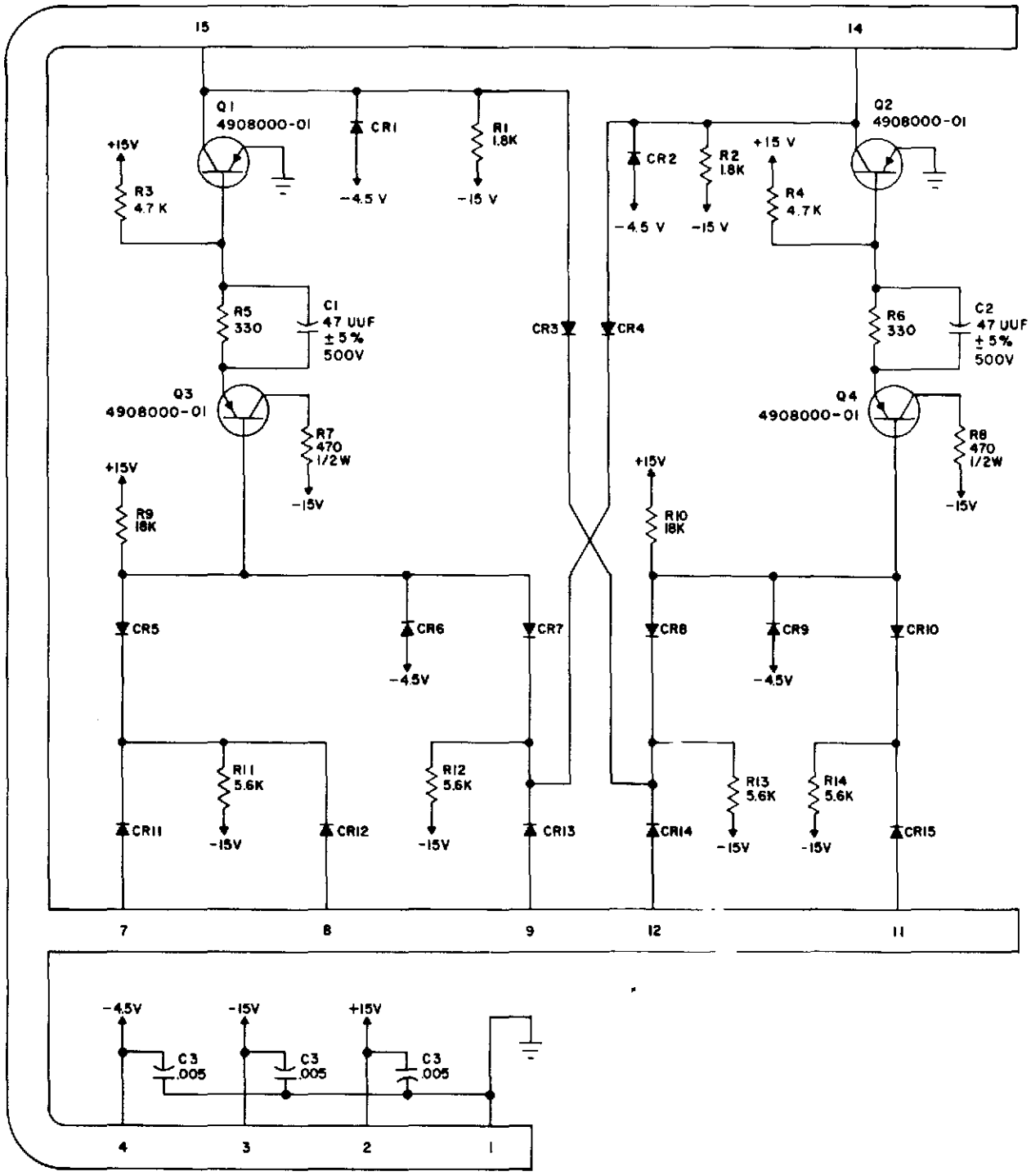


Figure 6-105. Flip-Flop, Module Type 2510, Electrical Schematic

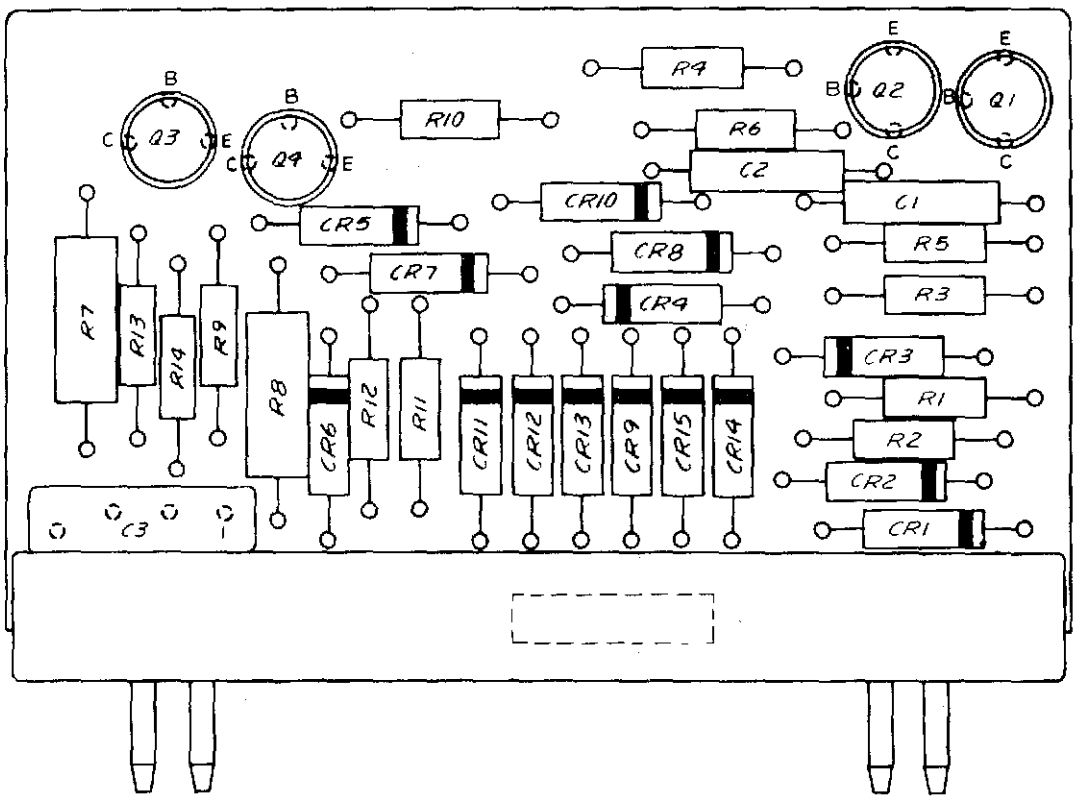


Figure 6-106. Module Type 2510 Component Layout

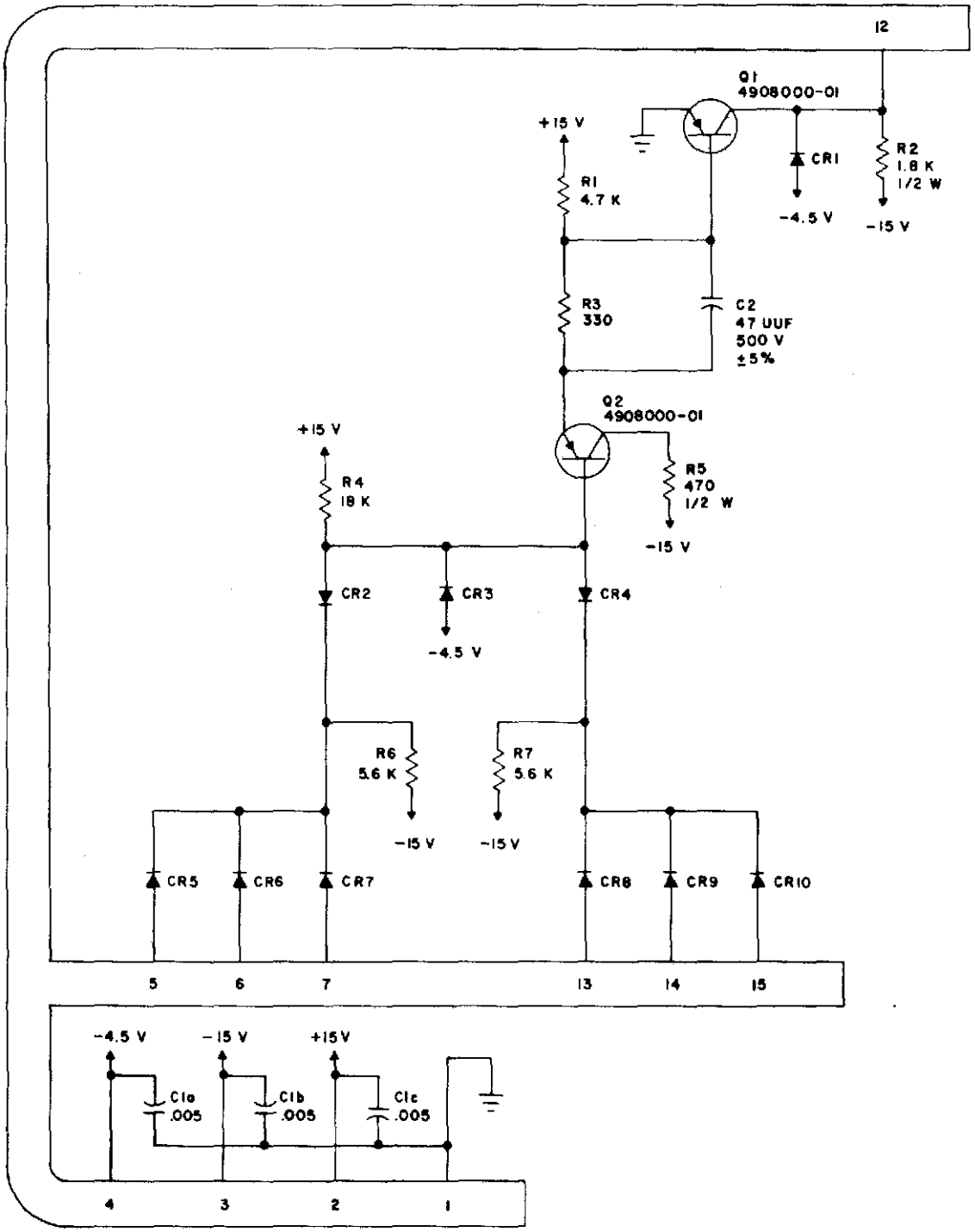


Figure 6-107. Inverter, Module Type 2520, Electrical Schematic

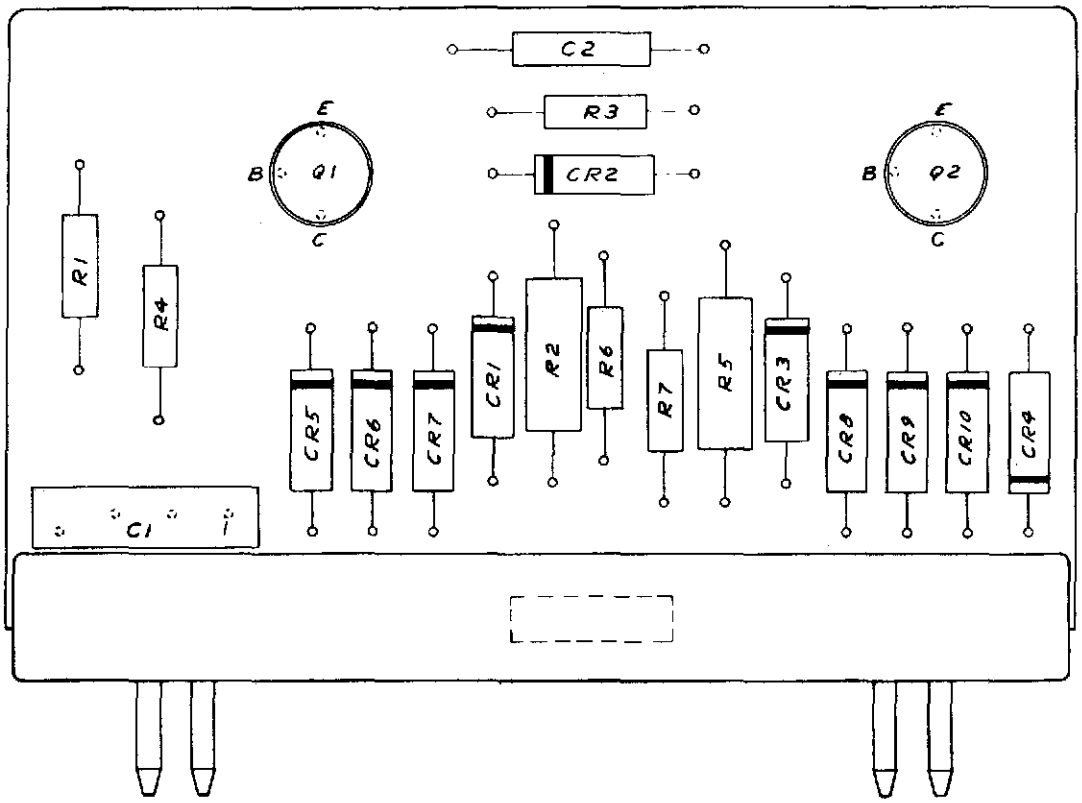


Figure 6-108. Module Type 2520 Component Layout

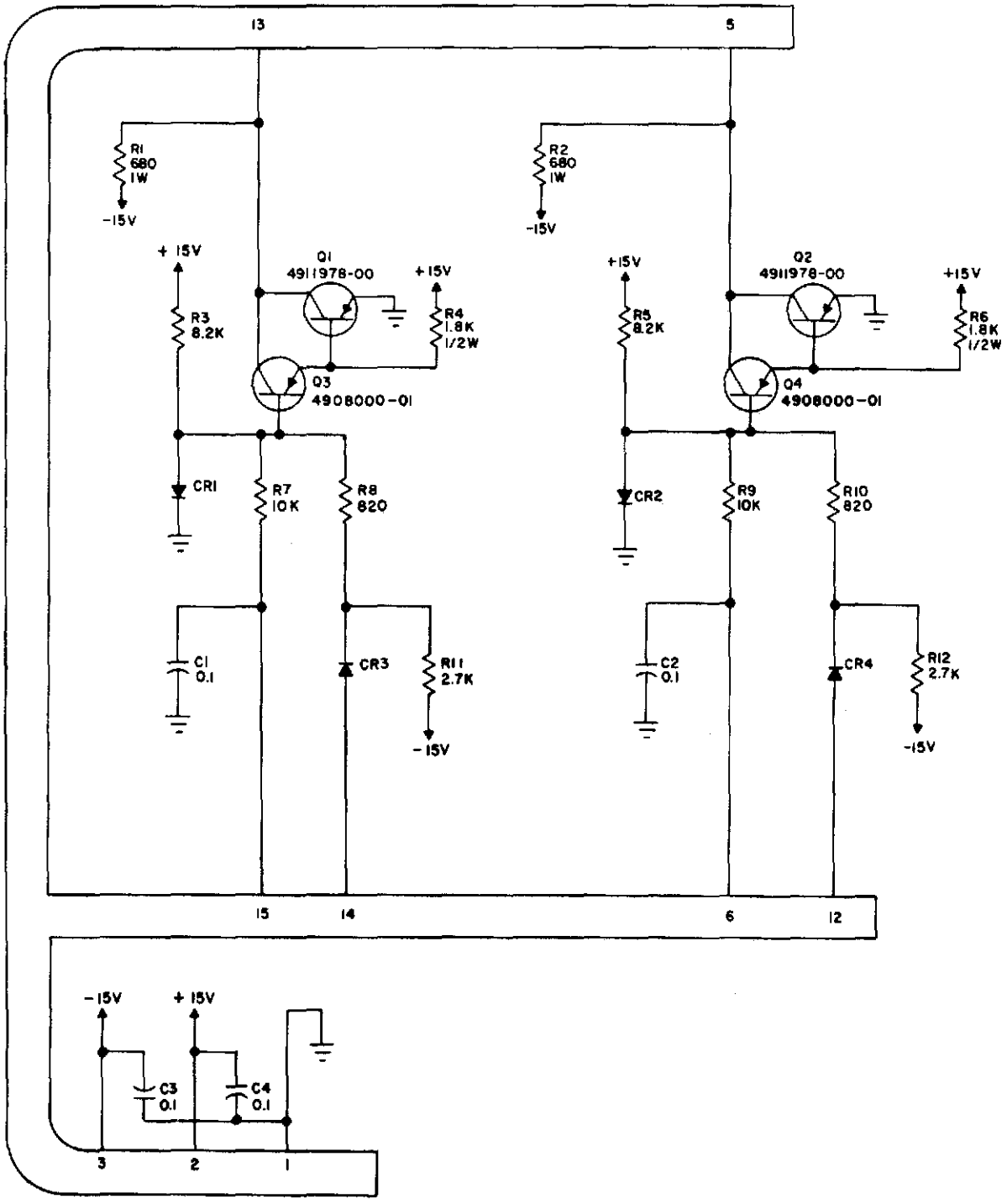


Figure 6-109. Amplifier-Digit Timing - A, Module Type 2530, Electrical Schematic

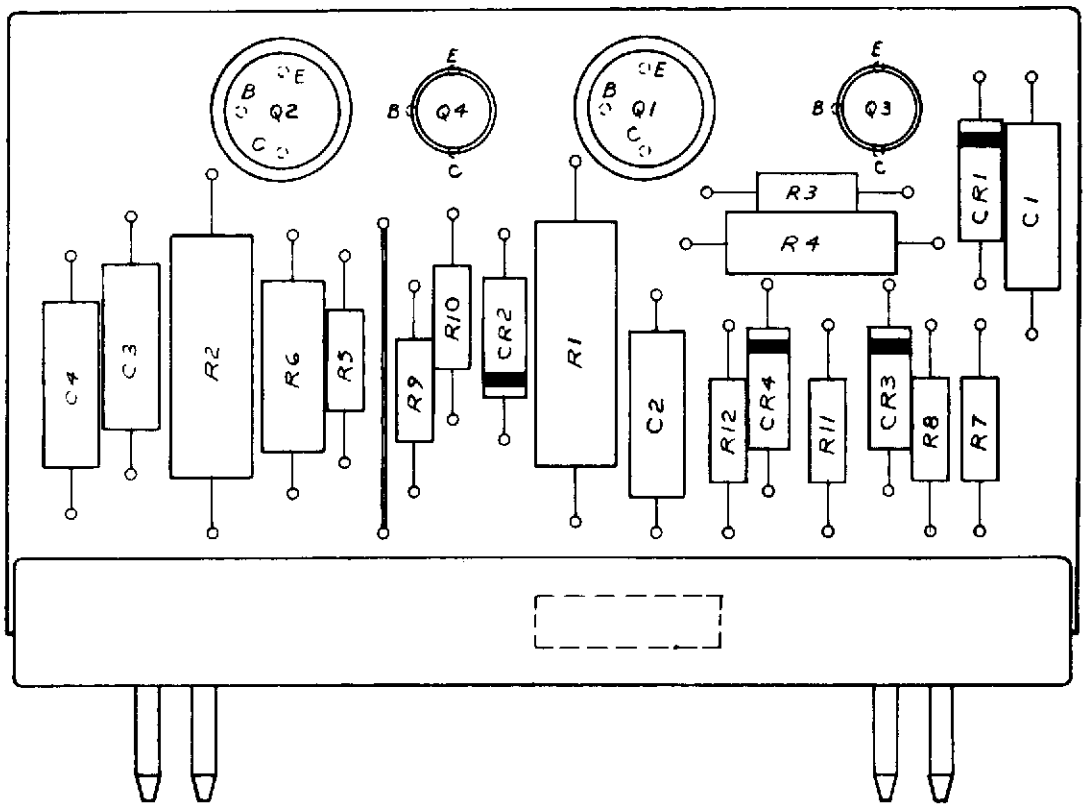


Figure 6-110. Module Type 2530 Component Layout

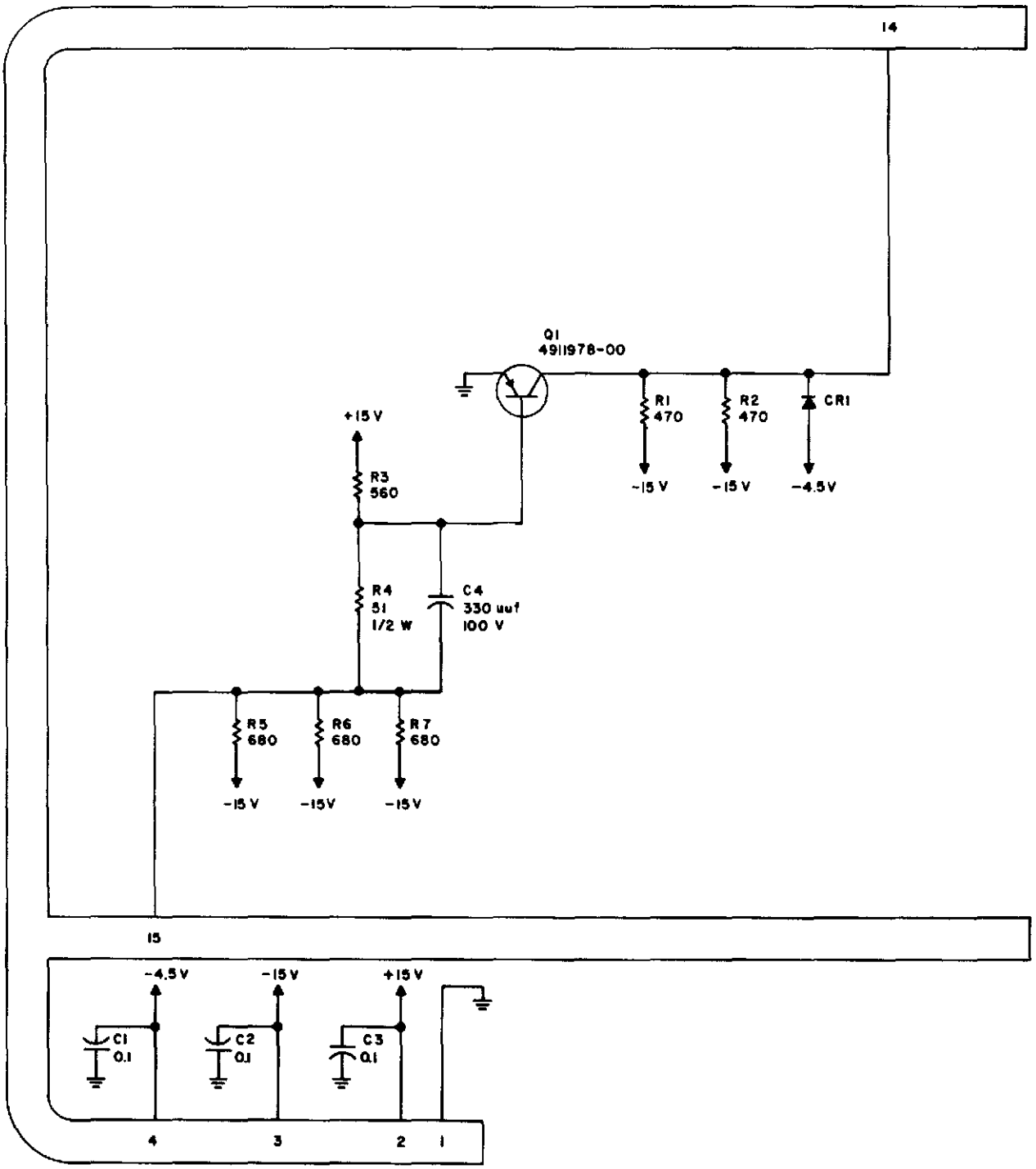


Figure 6-111. Amplifier-Digit Timing - B, Module Type 2540, Electrical Schematic

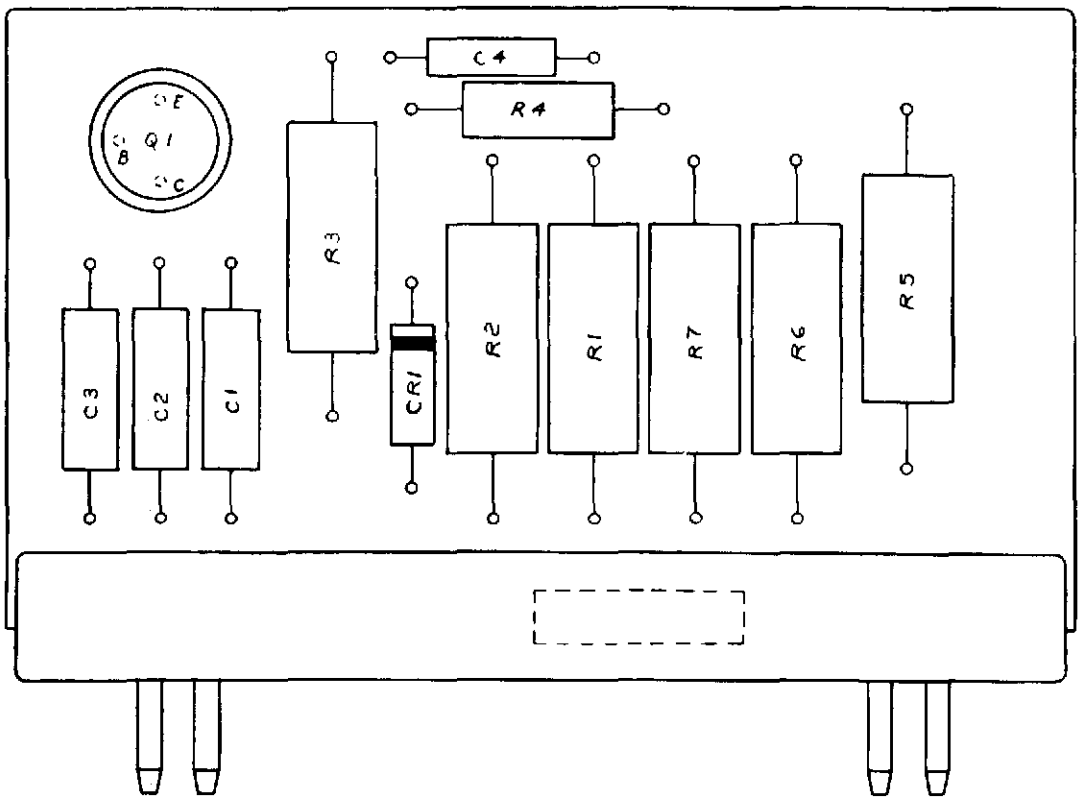


Figure 6-112. Module Type 2540 Component Layout

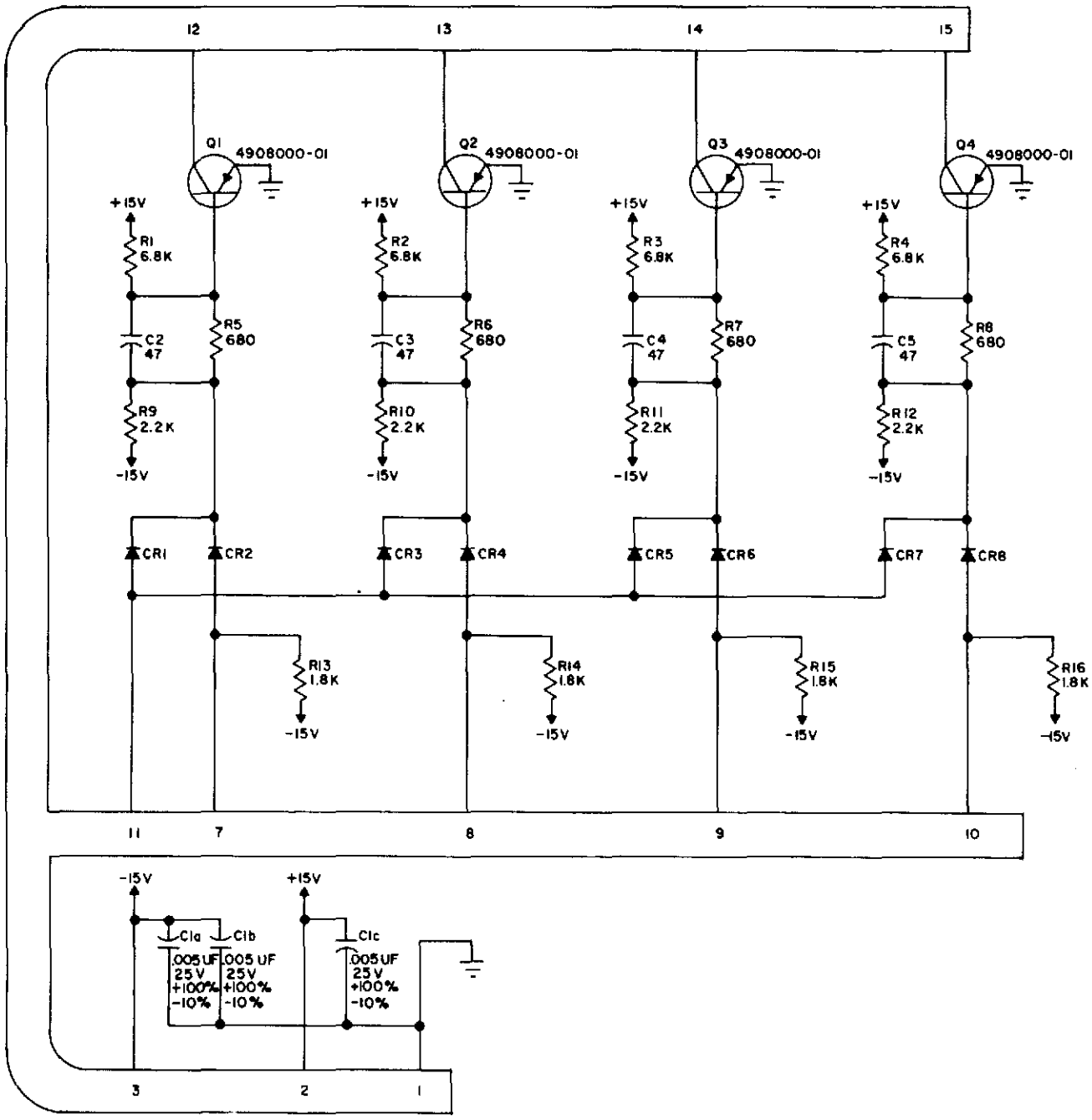


Figure 6-113. Digit Generator - A, Module Type 2550, Electrical Schematic

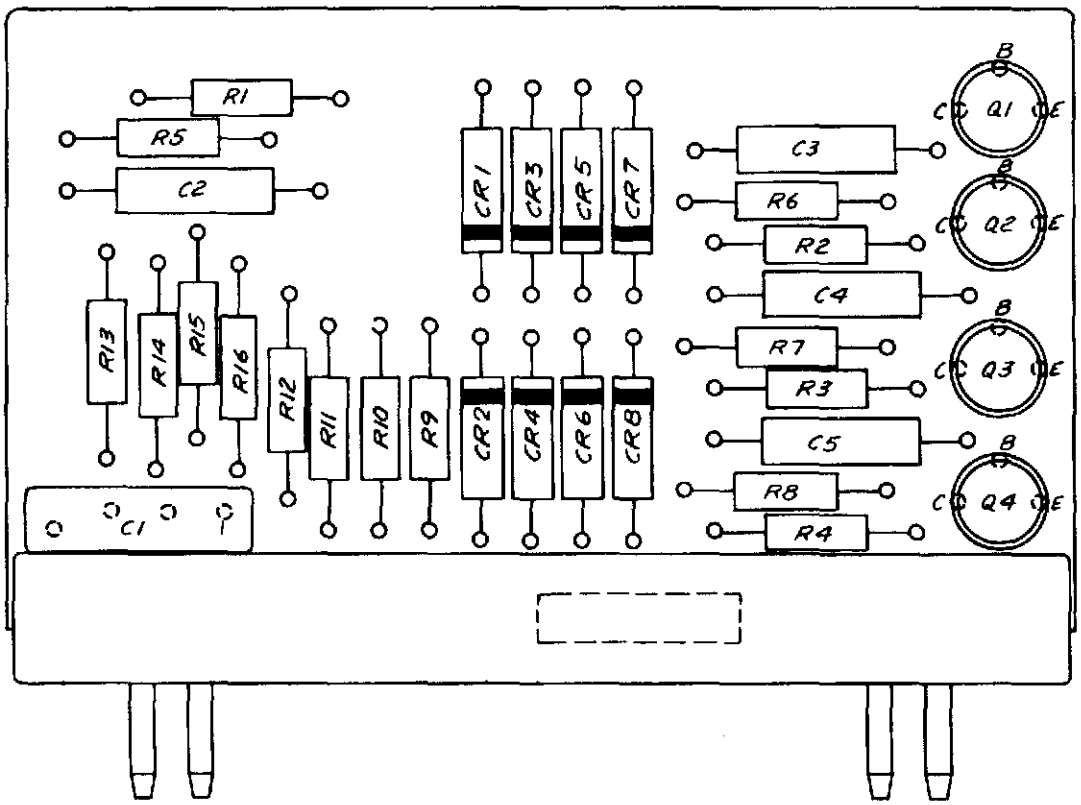


Figure 6-114. Module Type 2550 Component Layout

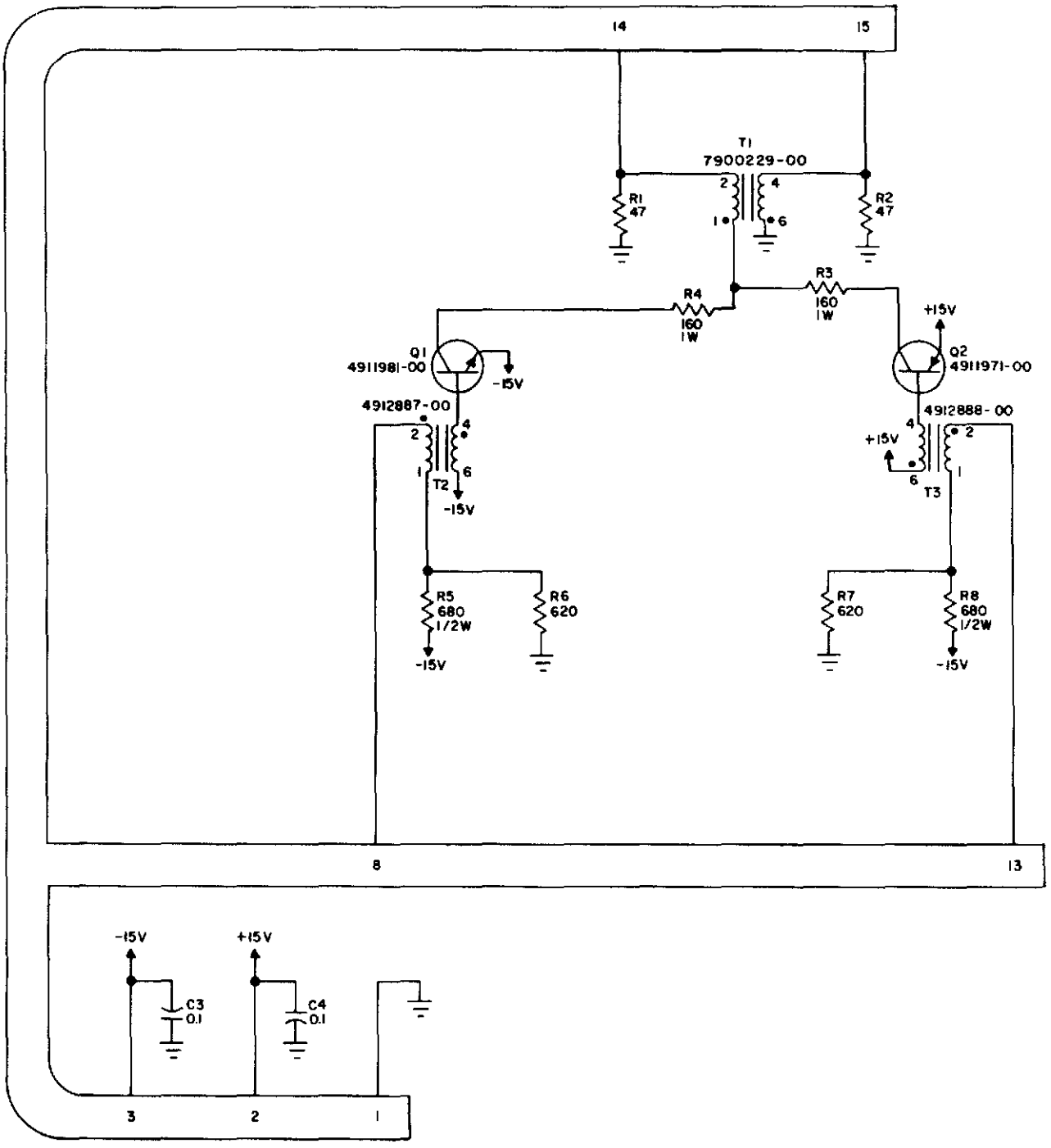


Figure 6-115. Digit Generator - B, Module Type 2560, Electrical Schematic

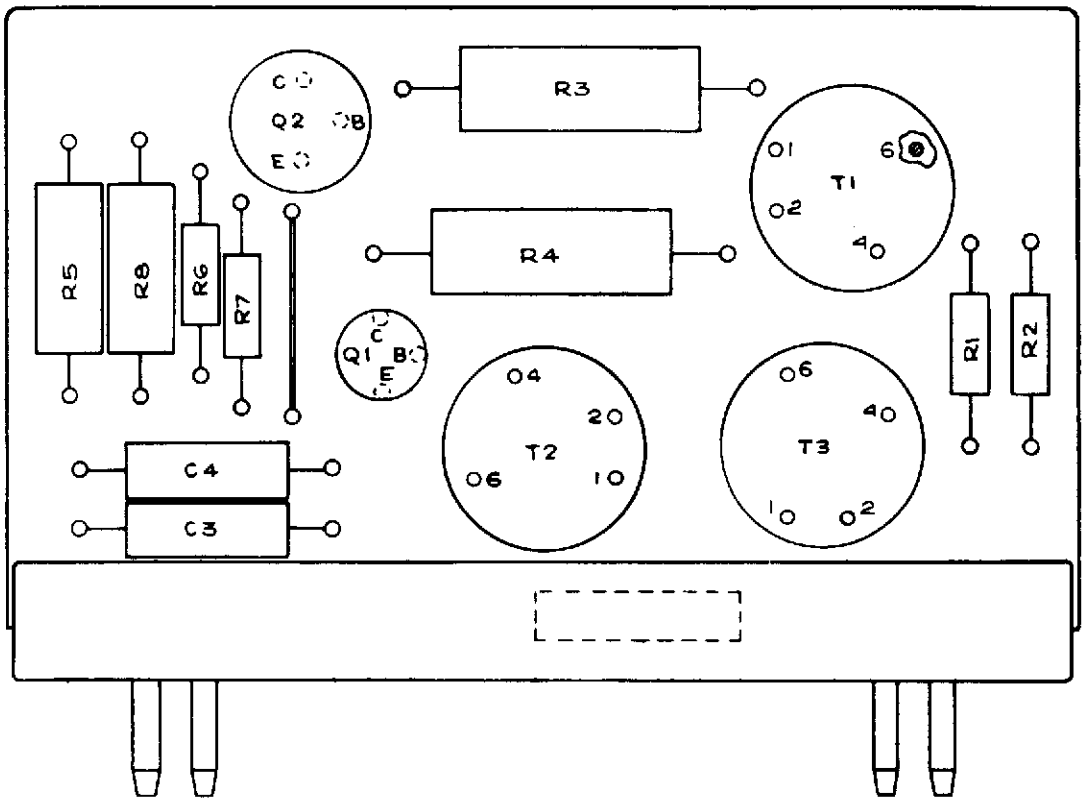


Figure 6-116. Module Type 2560 Component Layout

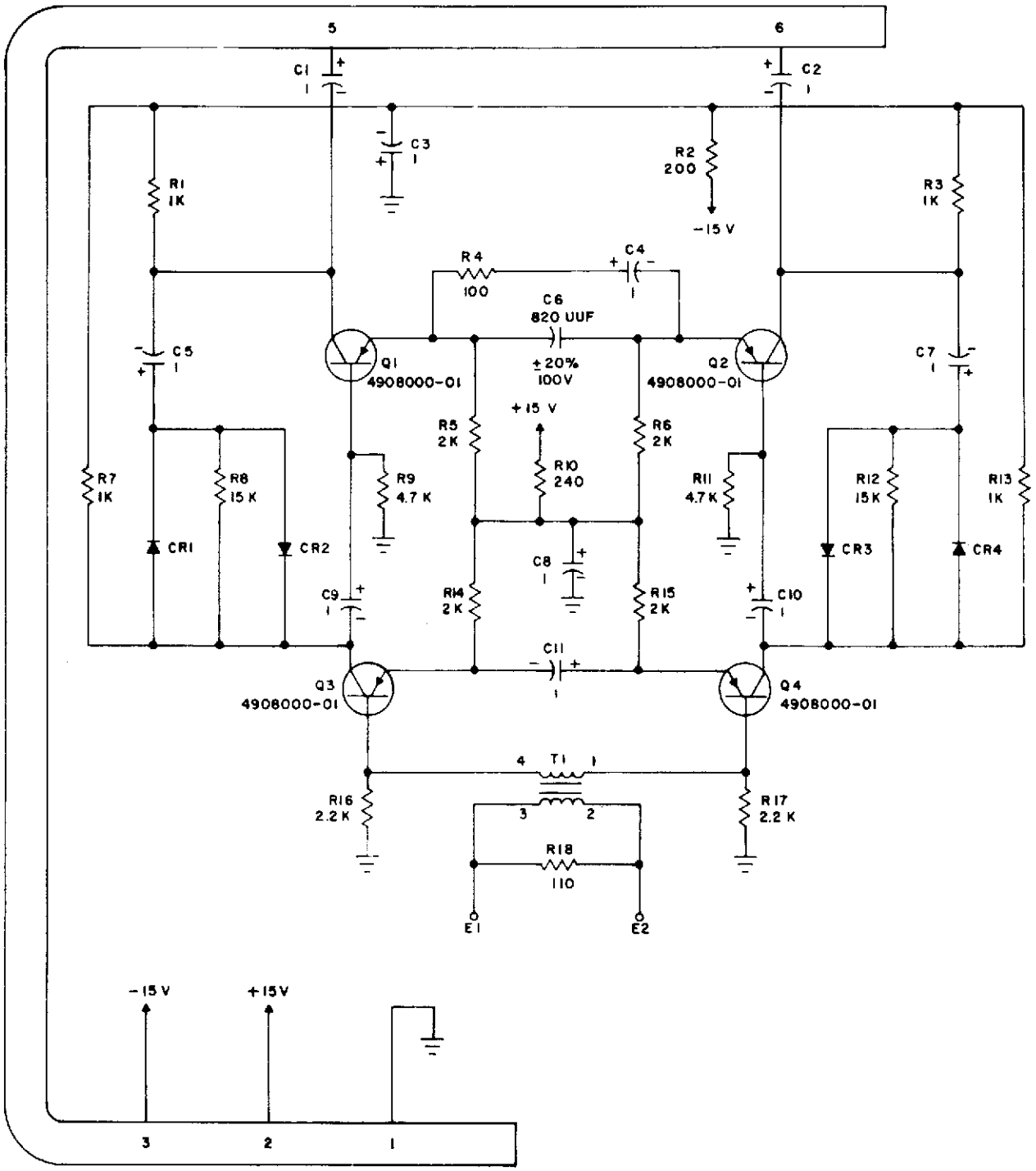


Figure 6-117. Sense Amplifier - A, Module Type 2570, Electrical Schematic

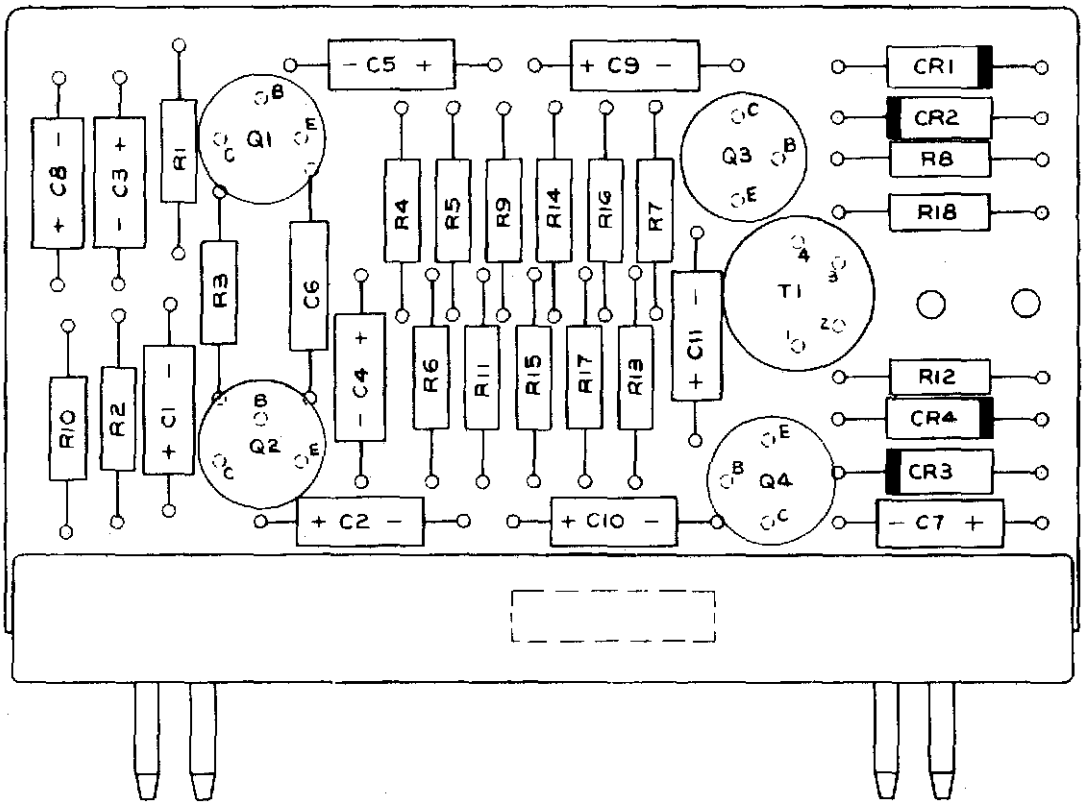


Figure 6-118. Module Type 2570 Component Layout

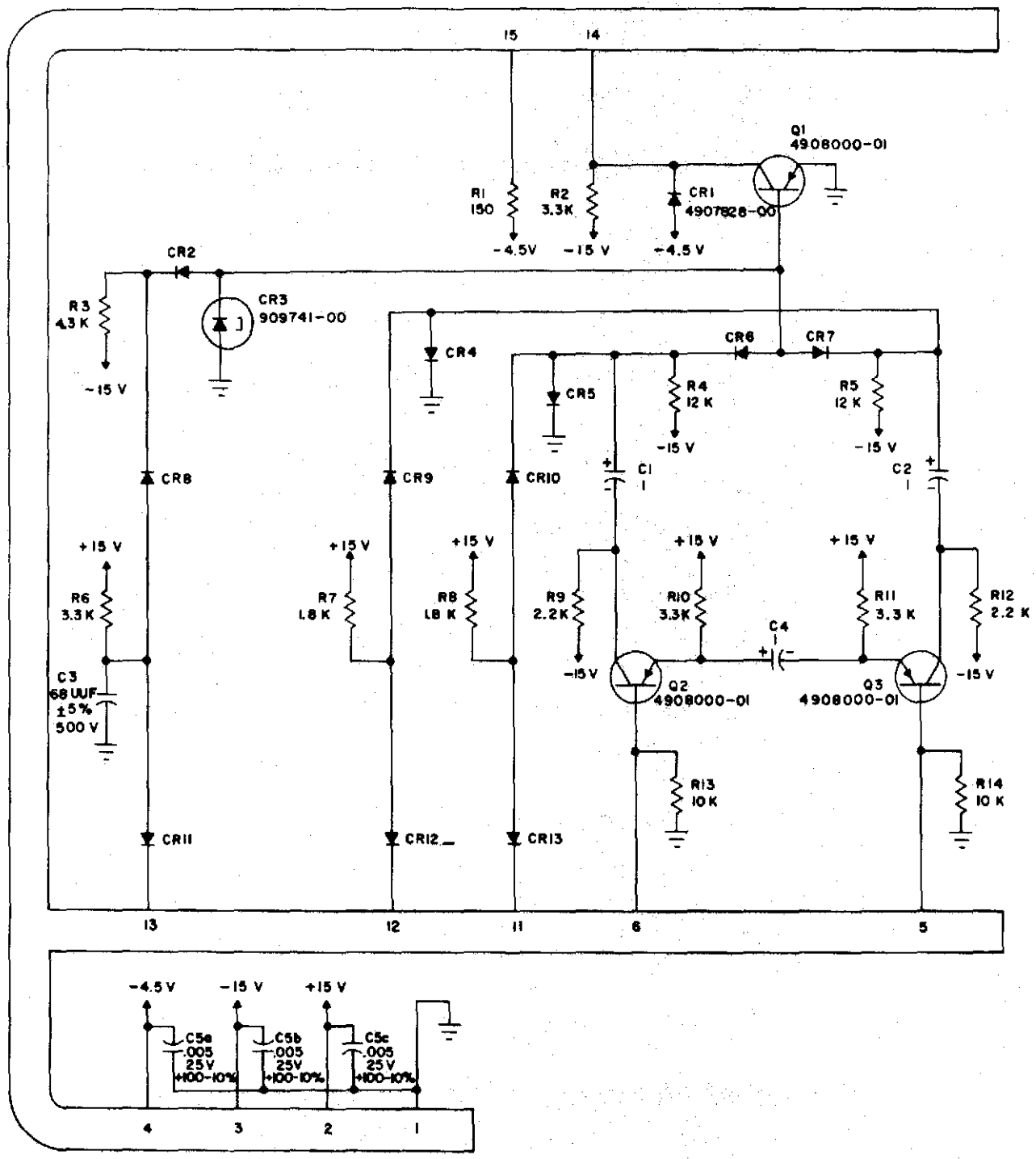


Figure 6-119. Sense Amplifier - B, Module Type 2580, Electrical Schematic

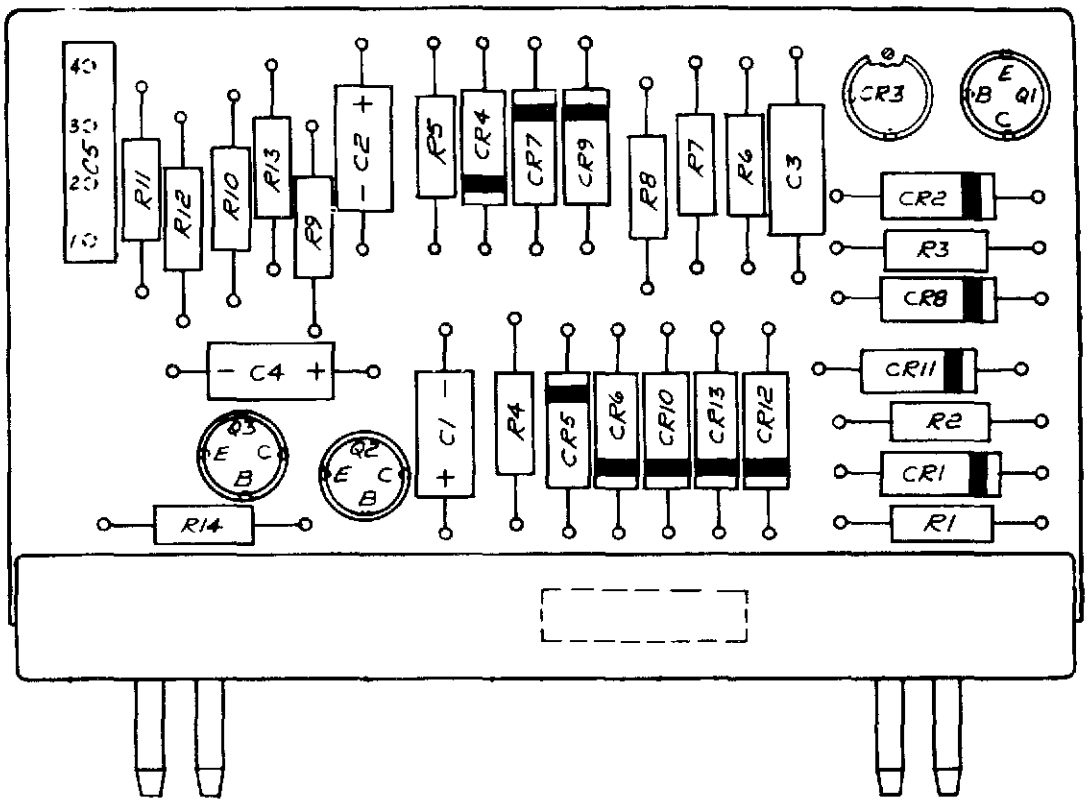


Figure 6-120. Module Type 2580 Component Layout

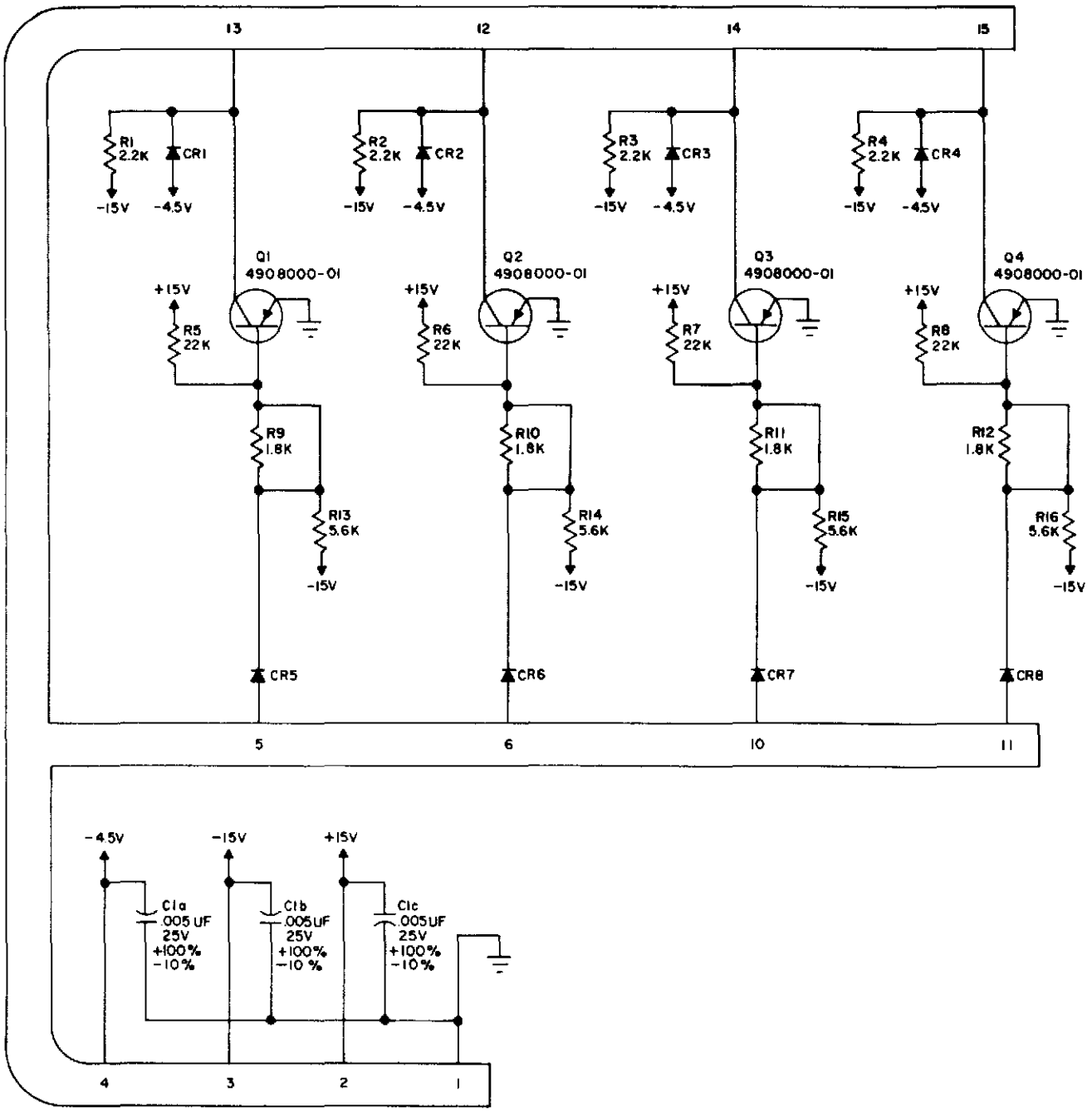


Figure 6-121. Inverter-Interface, Module Type 2590, Electrical Schematic

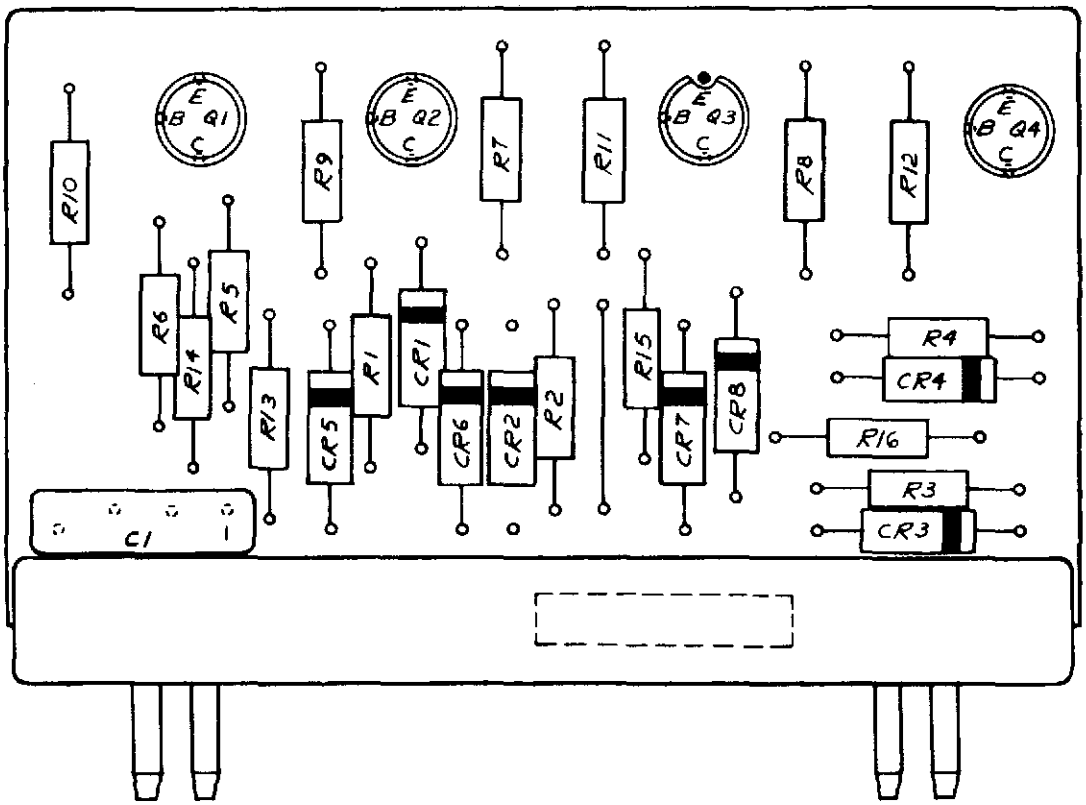


Figure 6-122. Module Type 2590 Component Layout

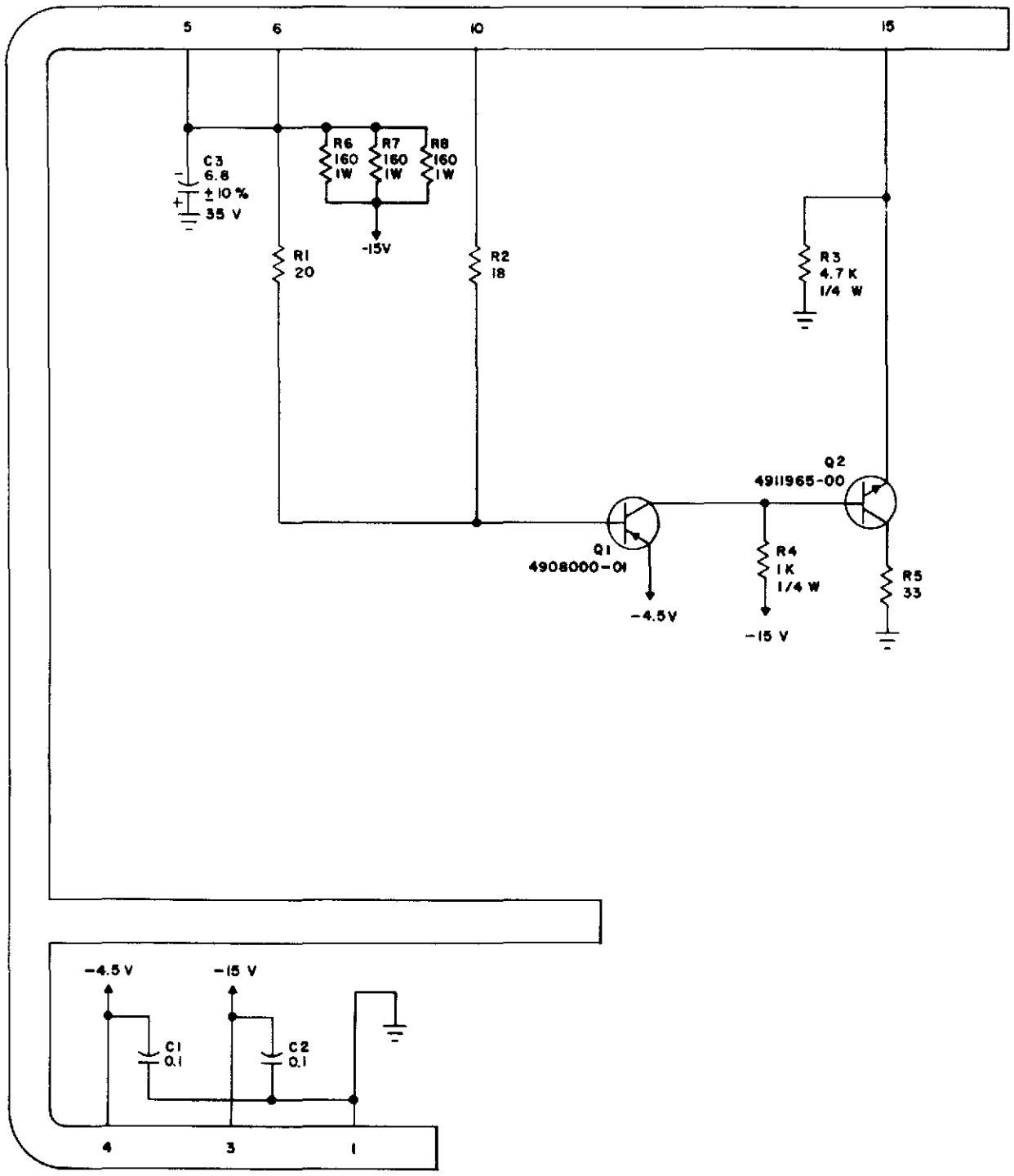


Figure 6-123. Voltage Regulator (-7V), Module Type 2600, Electrical Schematic

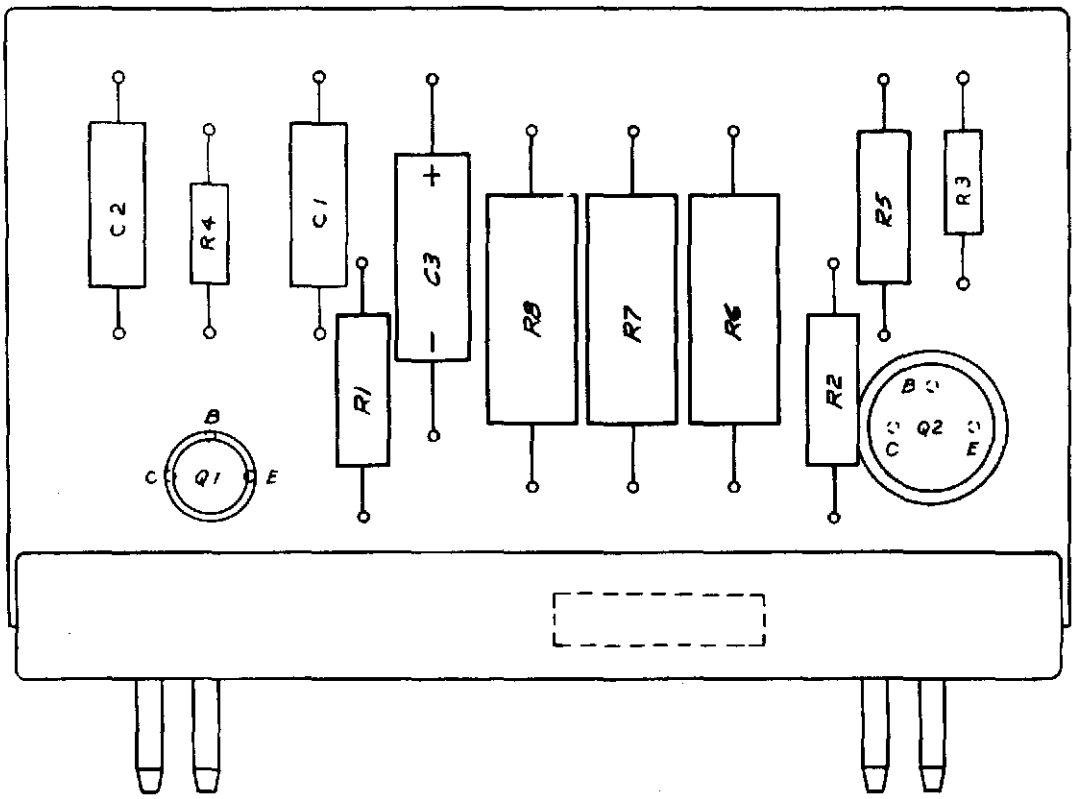


Figure 6-124. Module Type 2600 Component Layout

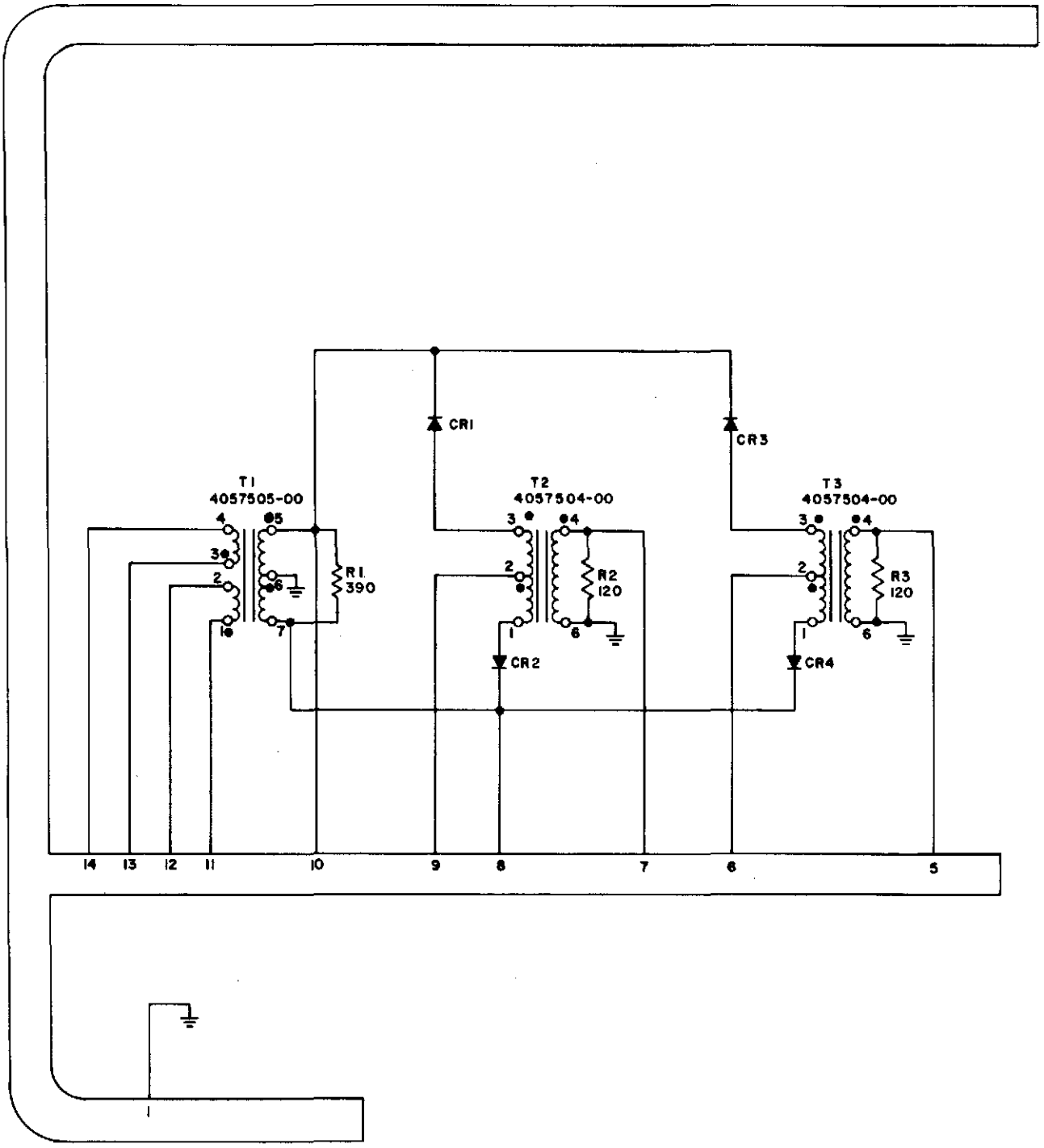


Figure 6-125. Transformer Assembly #1, Module Type 5000, Electrical Schematic

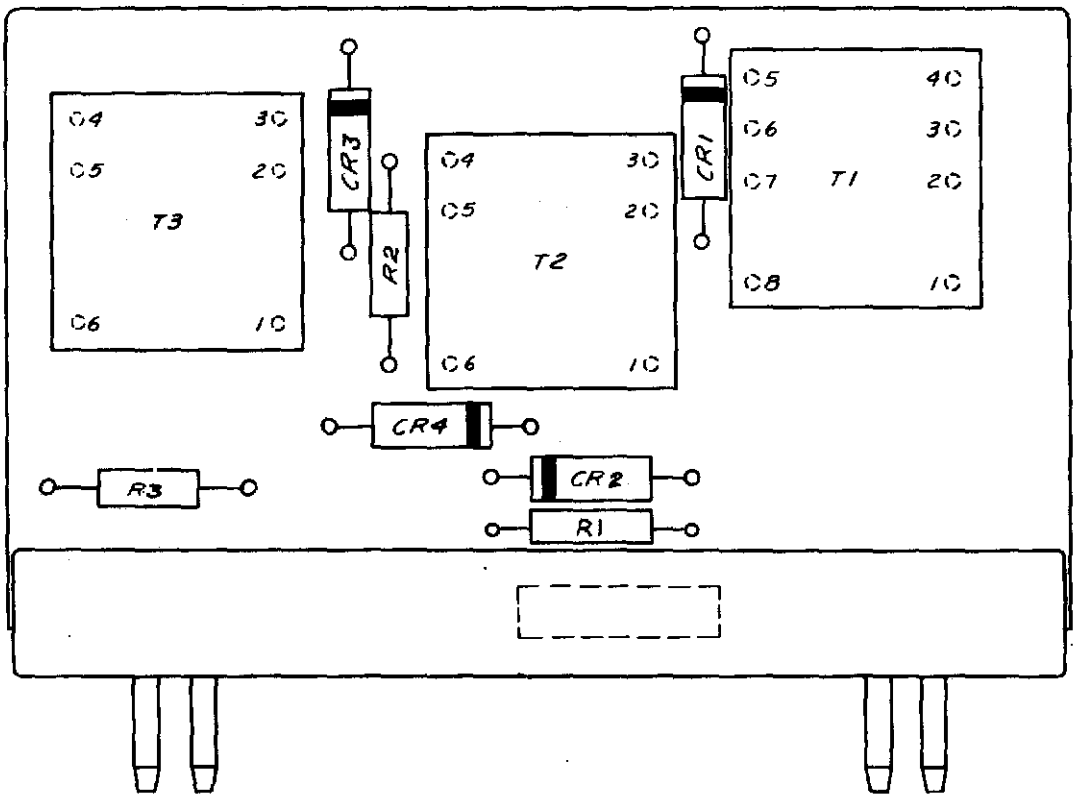


Figure 6-126. Module Type 5000 Component Layout

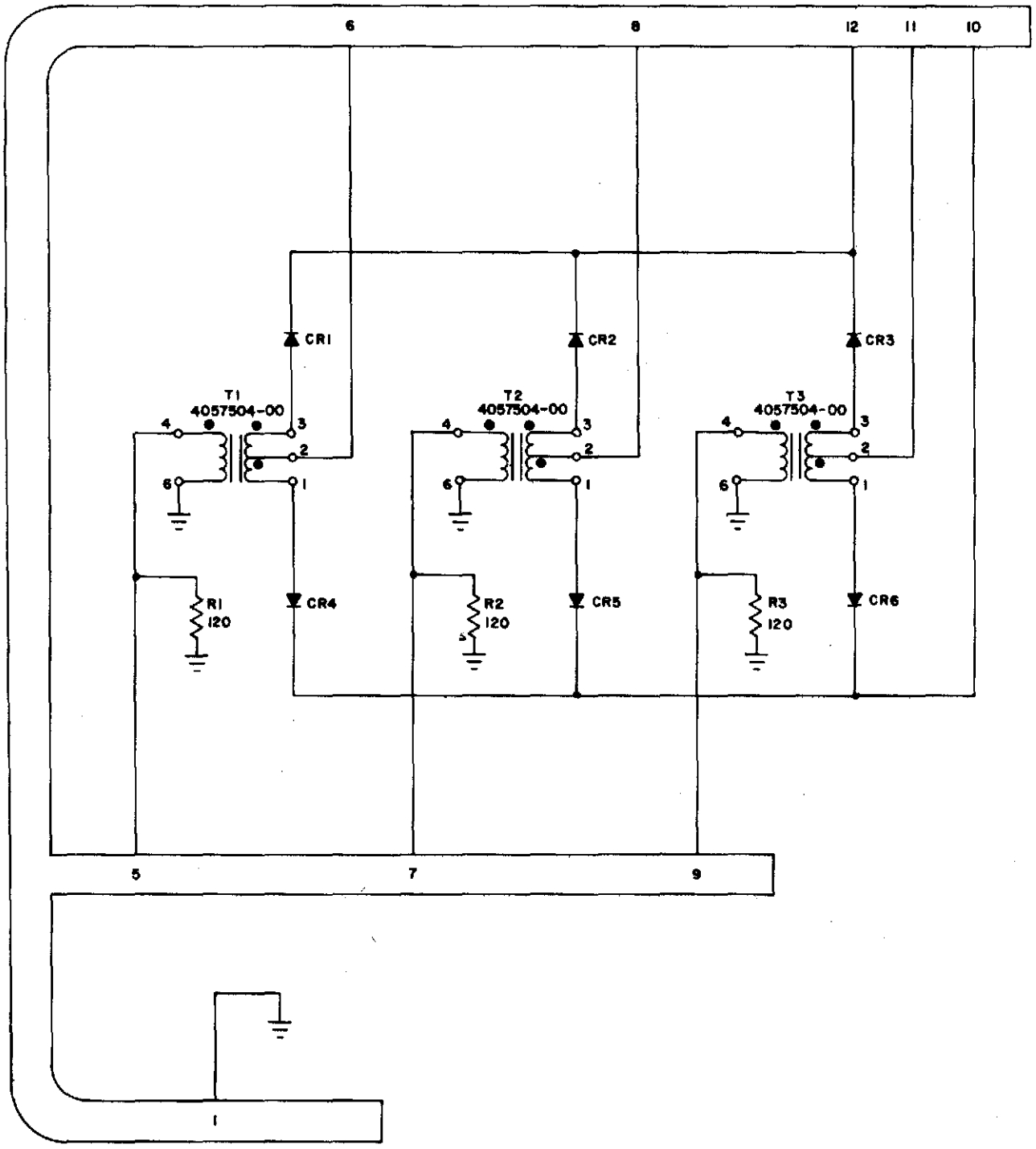


Figure 6-127. Transformer Assembly #2, Module Type 2620, Electrical Schematic

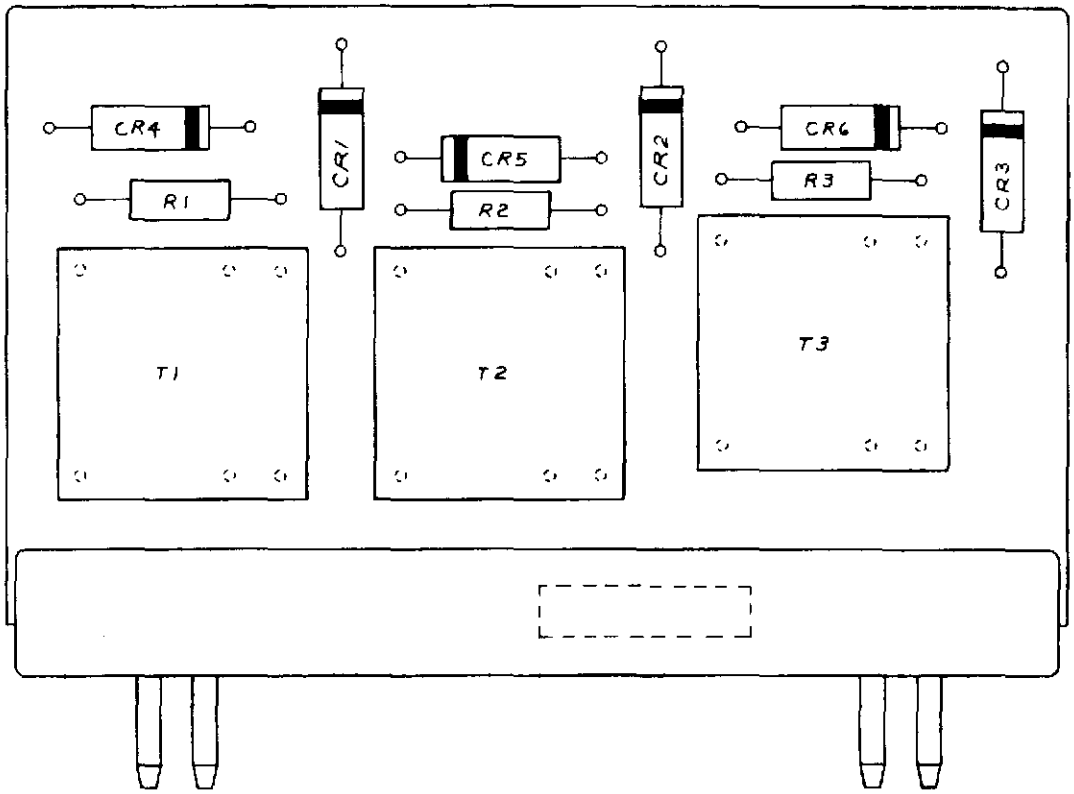


Figure 6-128. Module Type 2620 Component Layout

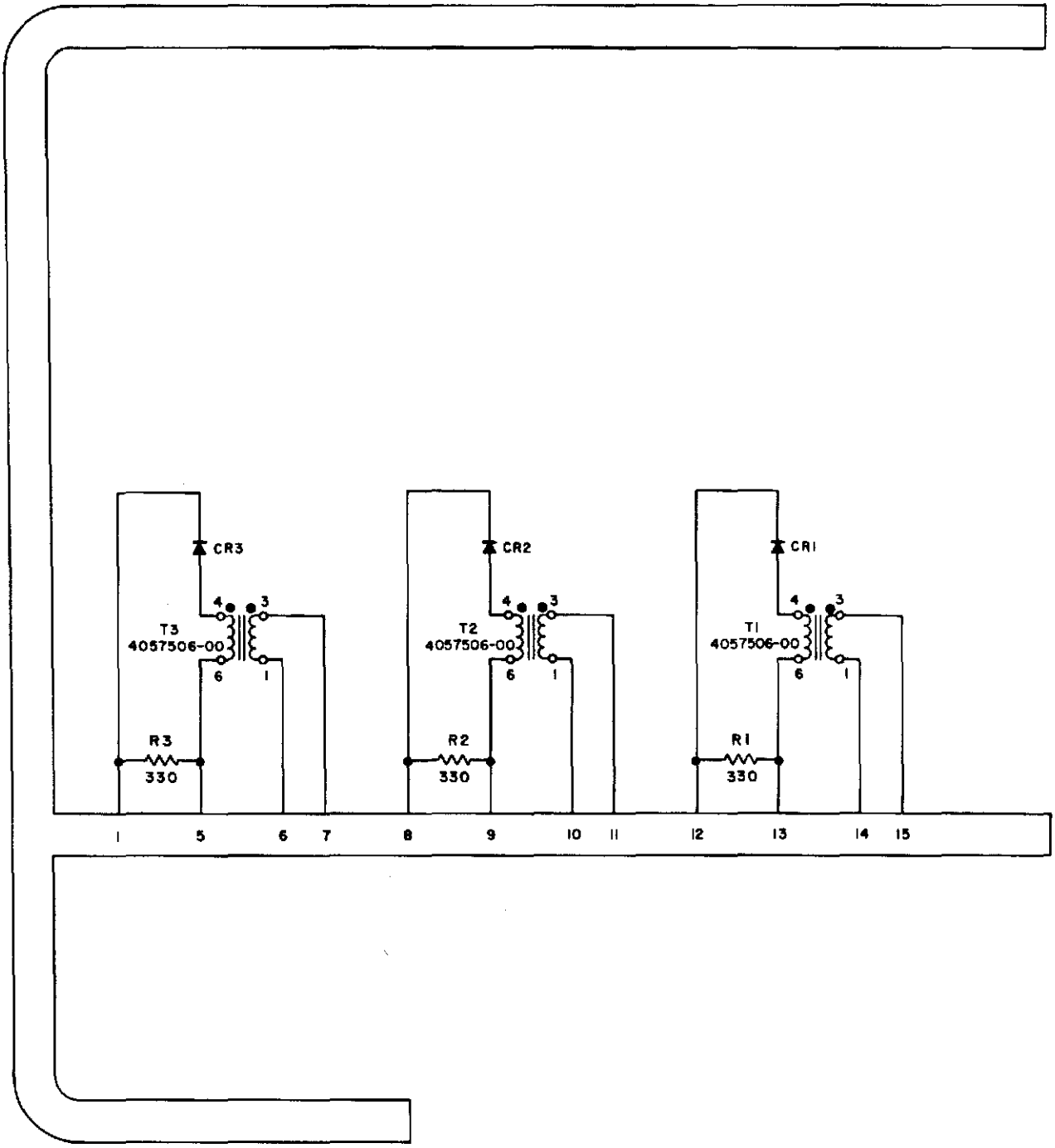


Figure 6-129. Transformer Assembly #3, Module Type 2631, Electrical Schematic

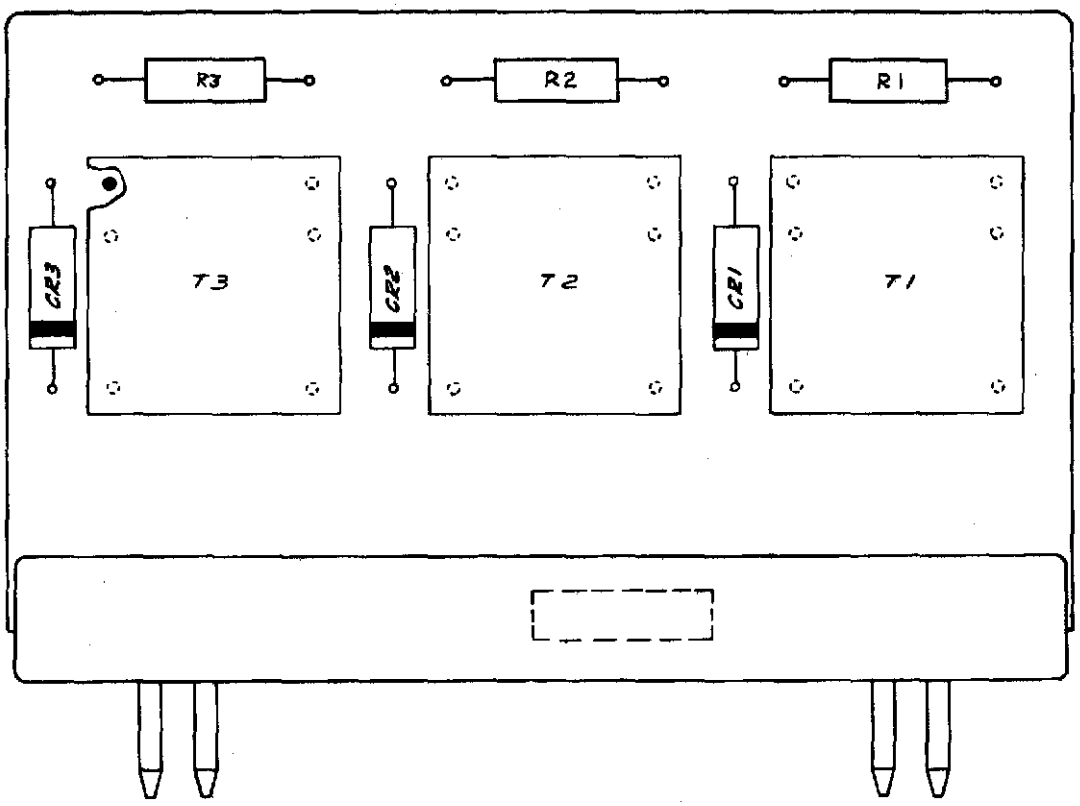


Figure 6-130. Module Type 2631 Component Layout

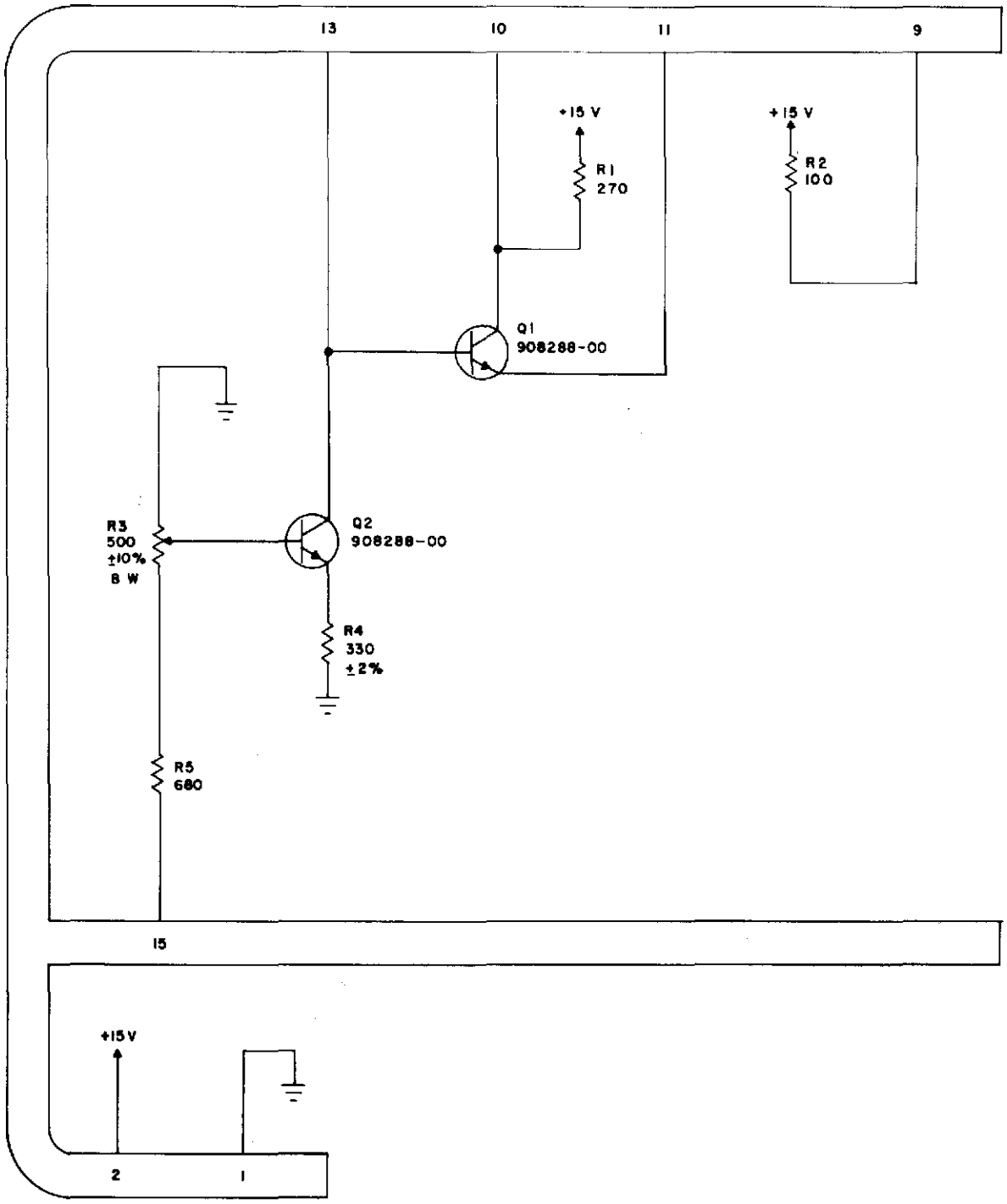


Figure 6-131. Voltage Regulator +10V, Module Type 2640, Electrical Schematic

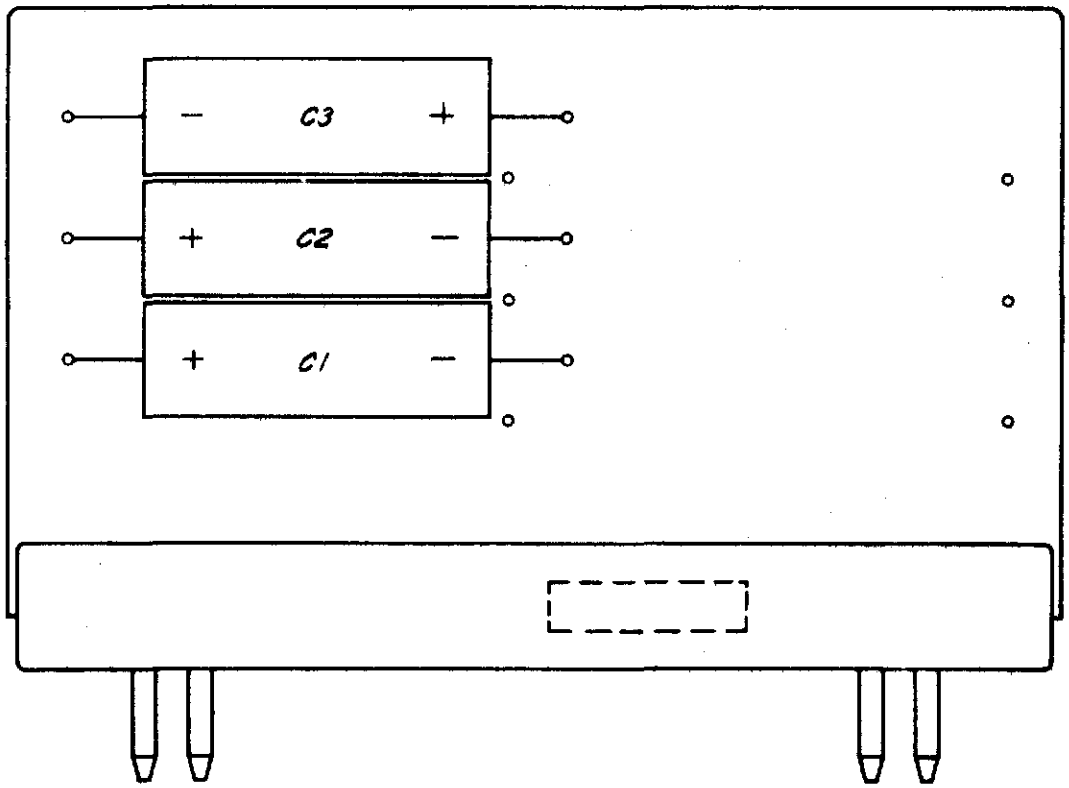


Figure 6-154. Module Type 3180 Component Layout

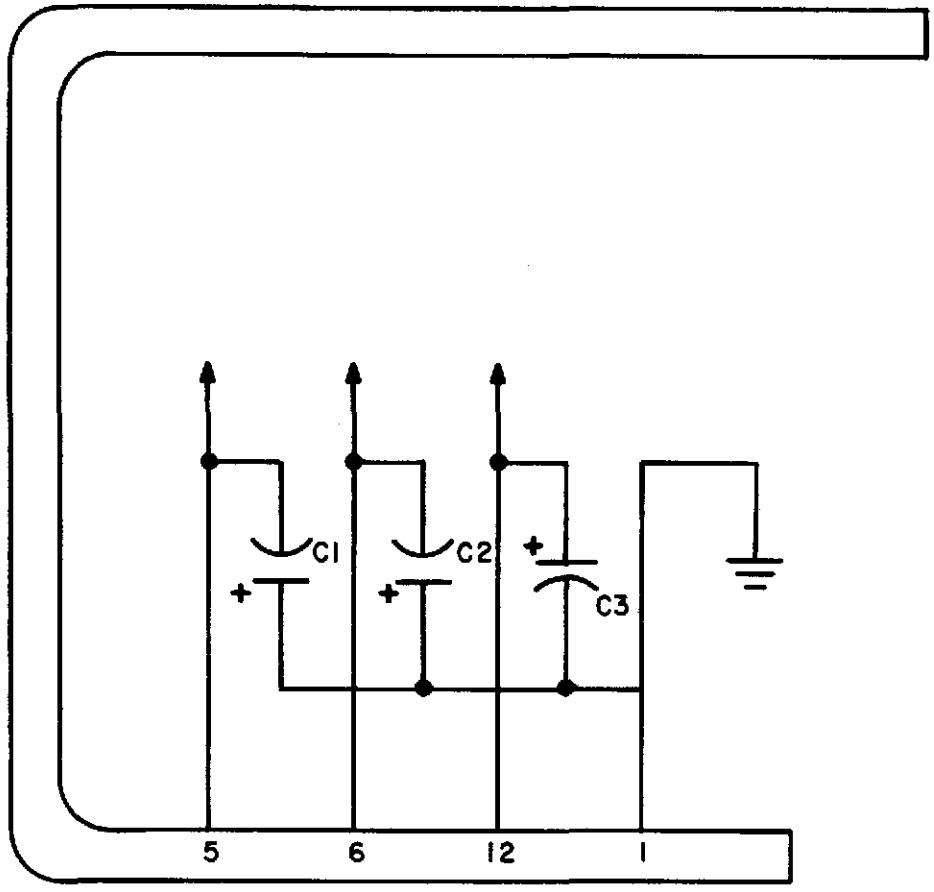


Figure 6-155. Capacitor Assembly, Module Type 5030, Electrical Schematic

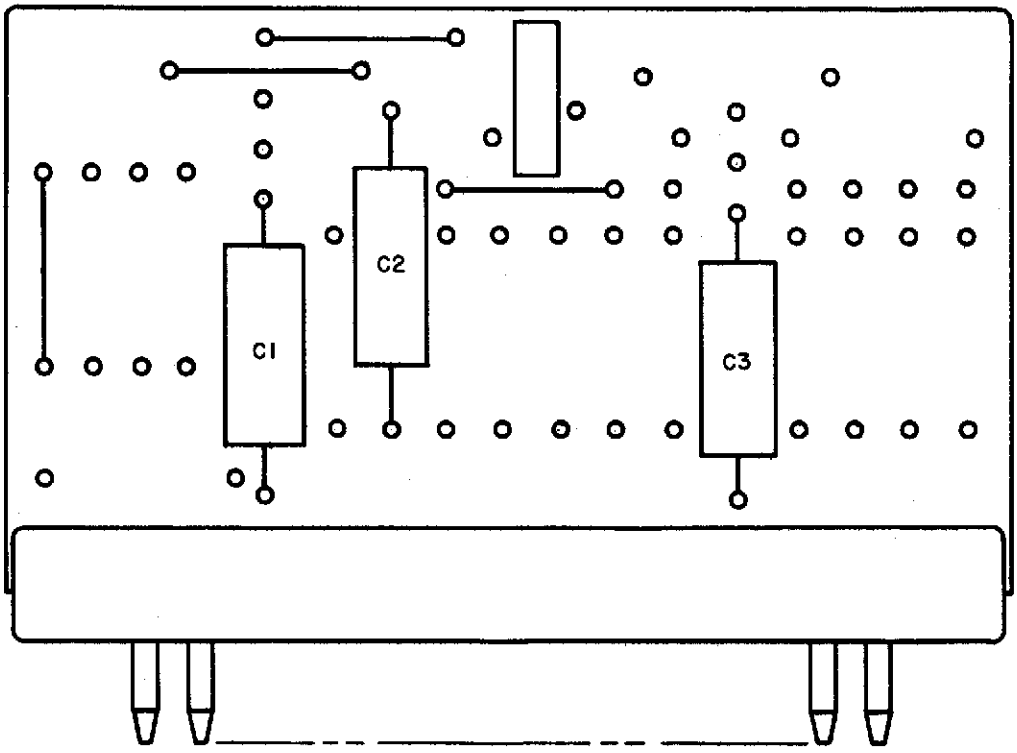


Figure 6-156. Module Type 5030 Component Layout

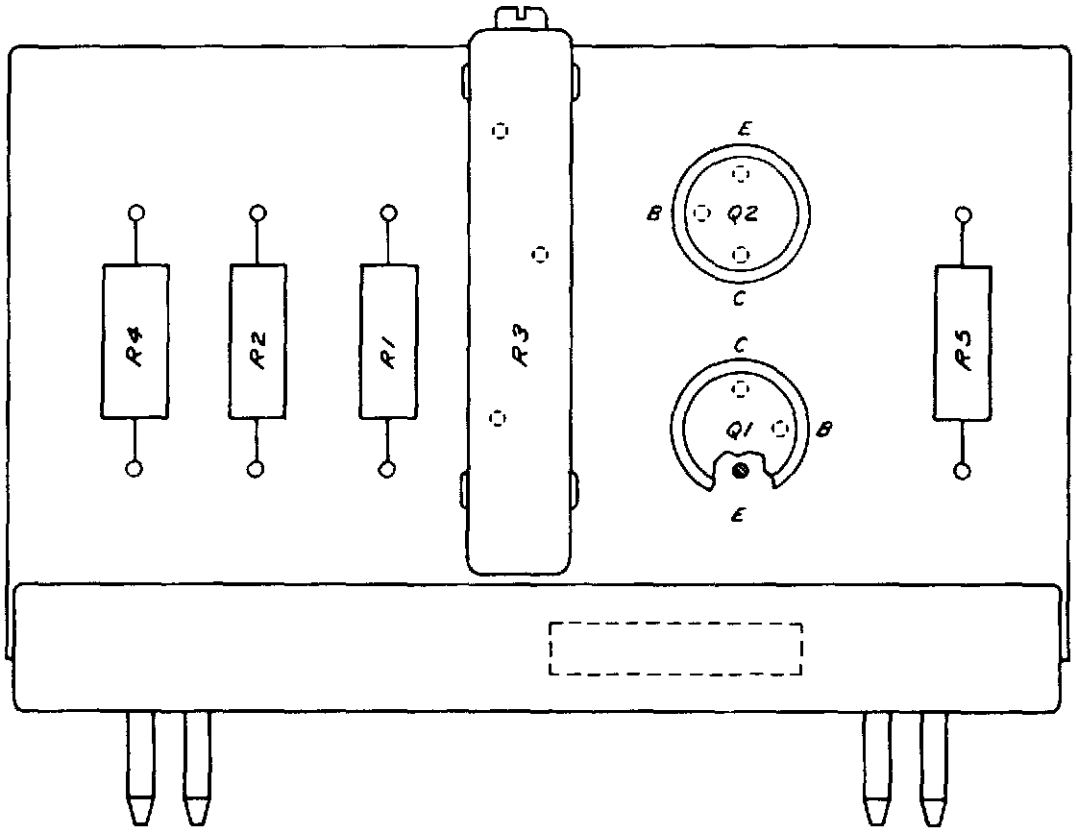


Figure 6-132. Module Type 2640 Component Layout

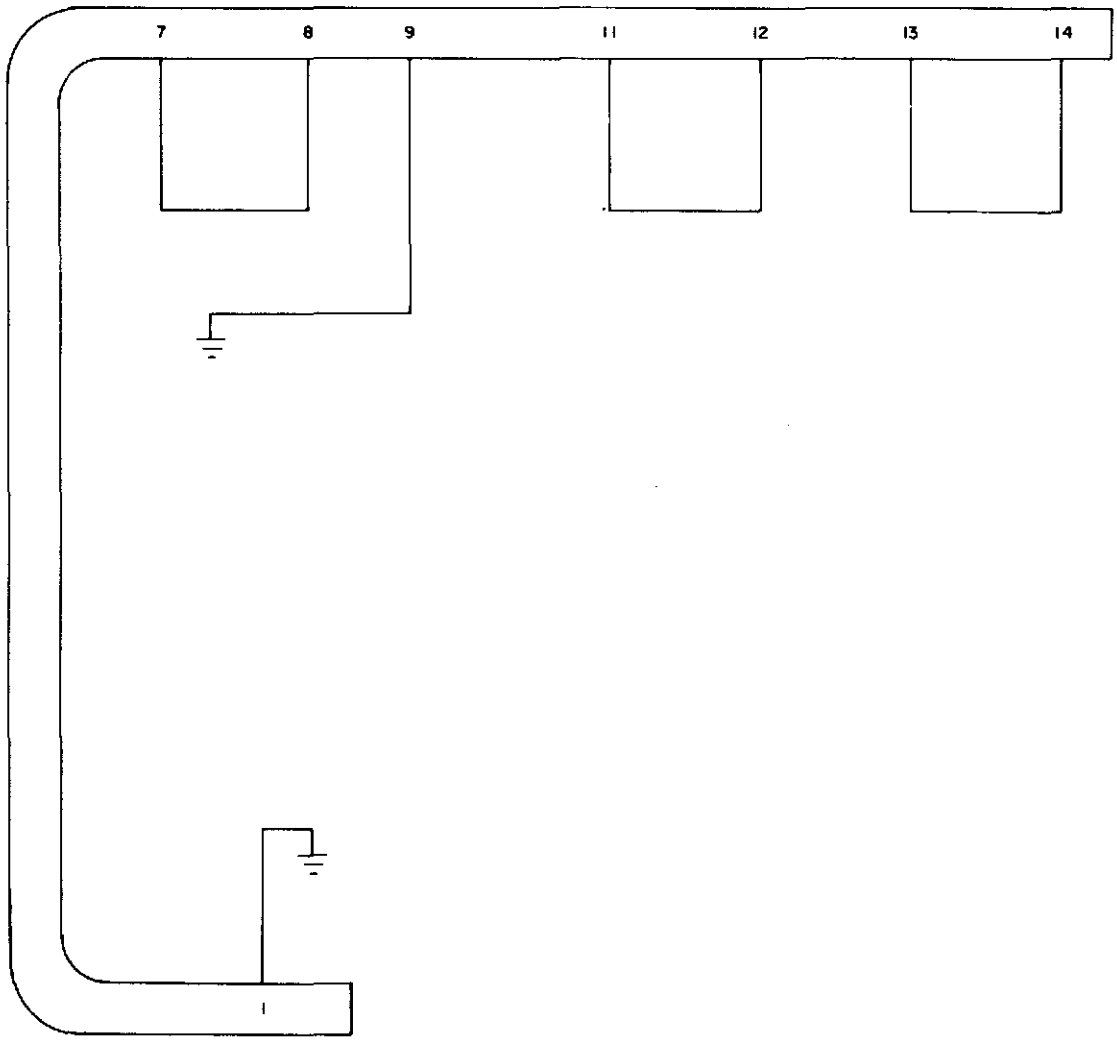


Figure 6-133. Selector Normal Channel, Module Type 2650, Electrical Schematic

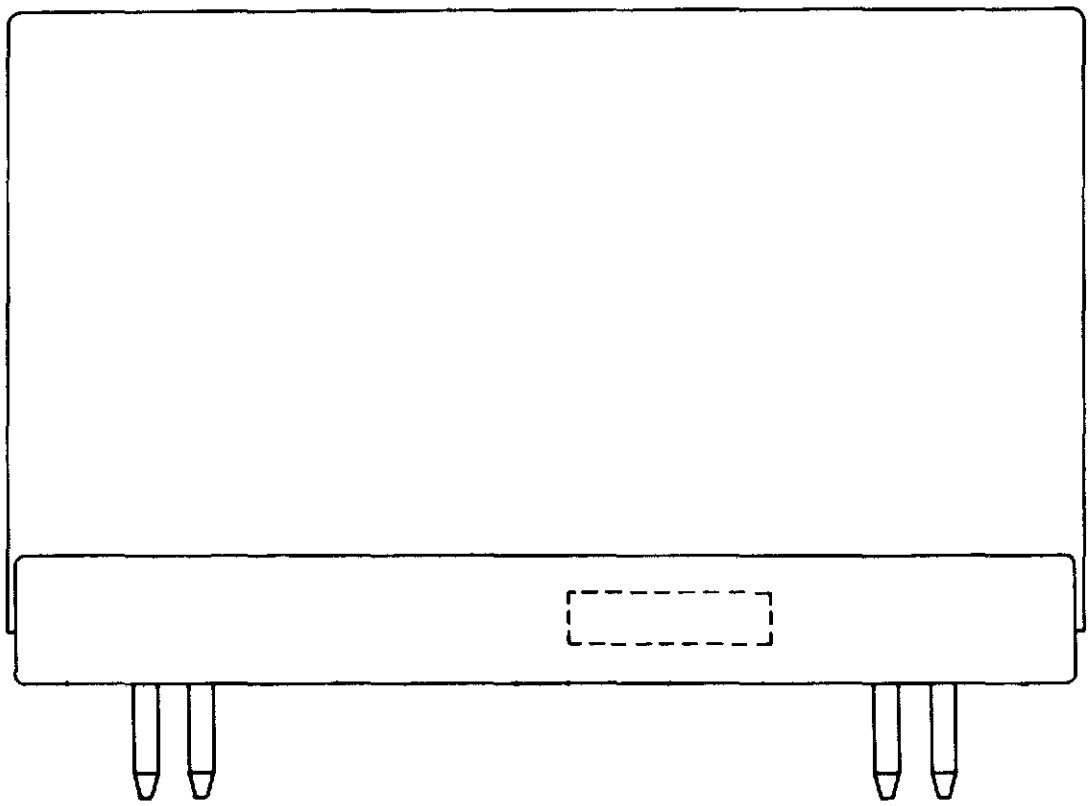


Figure 6-134. Module Type 2650 Component Layout

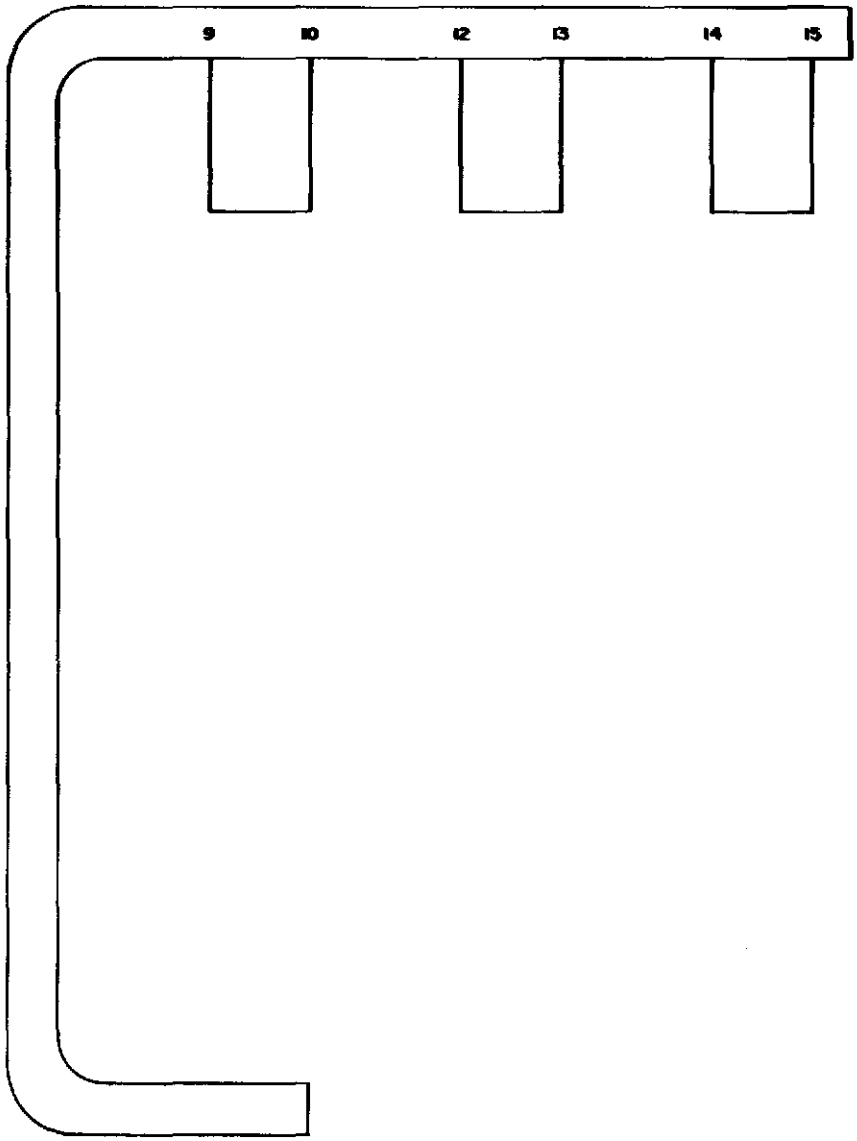


Figure 6-135. Selector Intercomputer Channel, Module Type 2660, Electrical Schematic

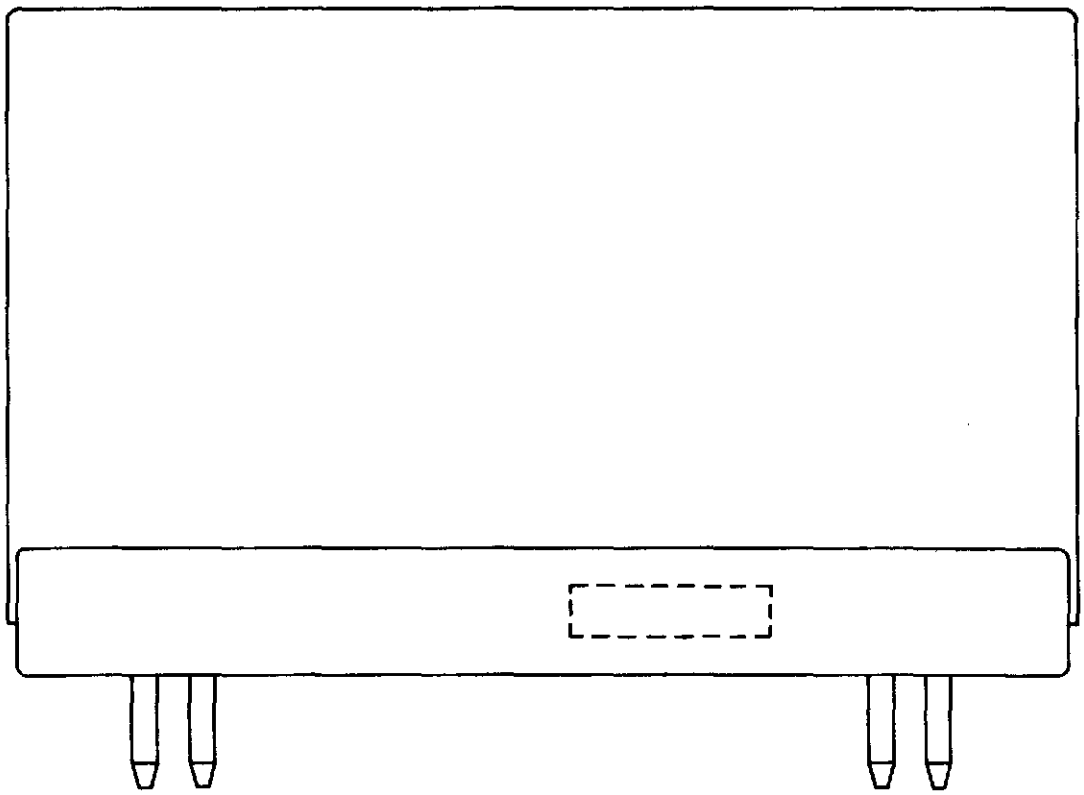


Figure 6-136. Module Type 2660 Component Layout

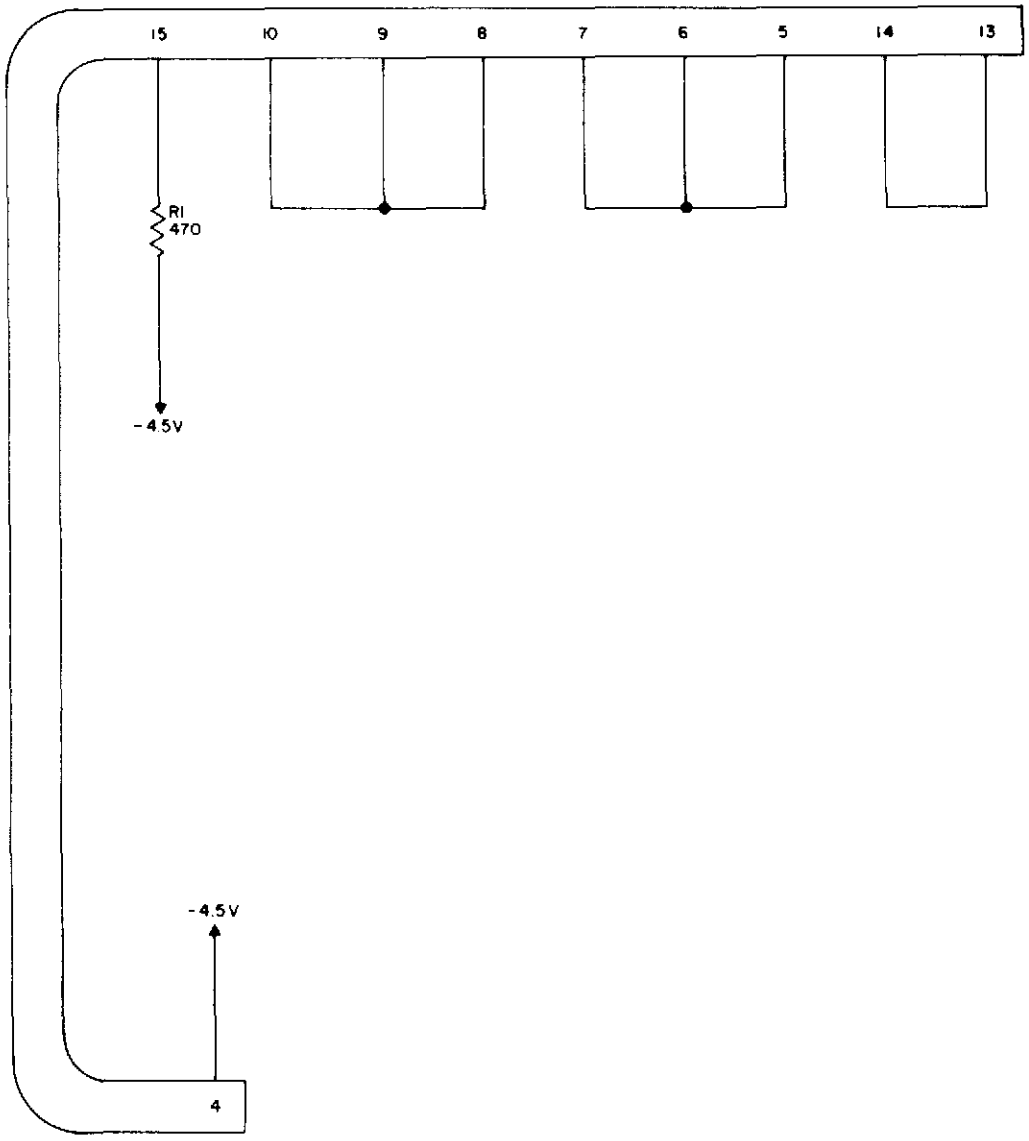


Figure 6-137. Selector Normal Speed I/O, Module Type 2720, Electrical Schematic

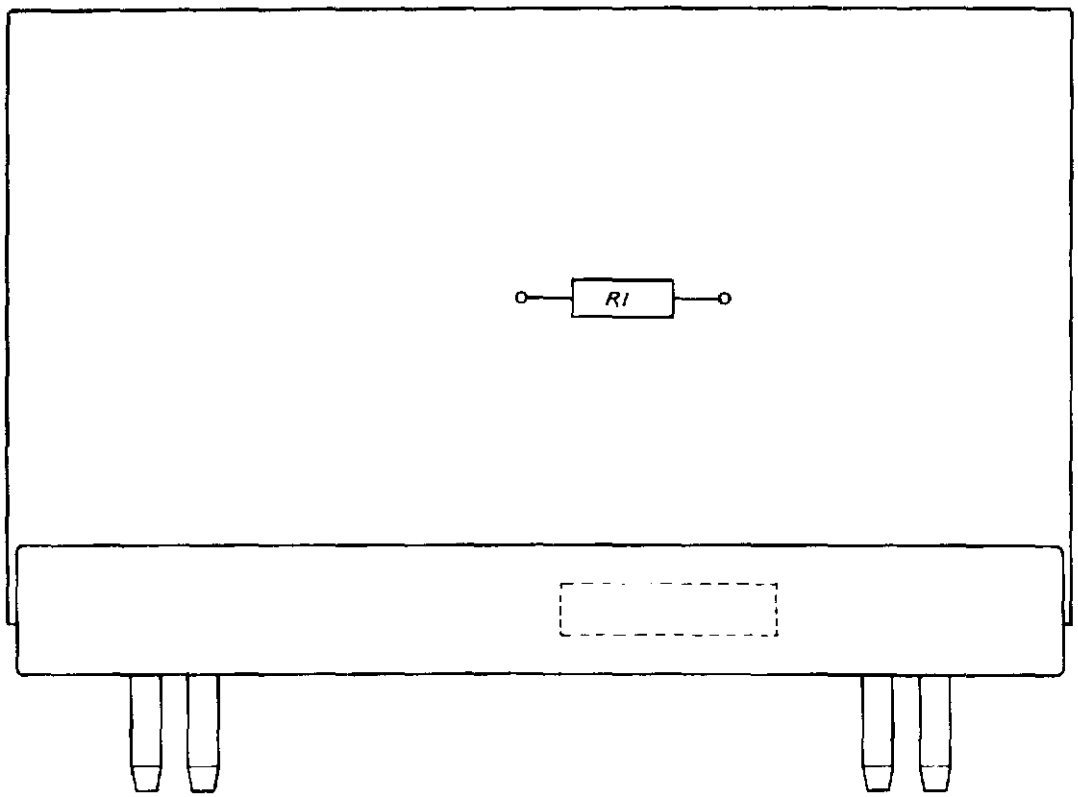


Figure 6-138. Module Type 2720 Component Layout

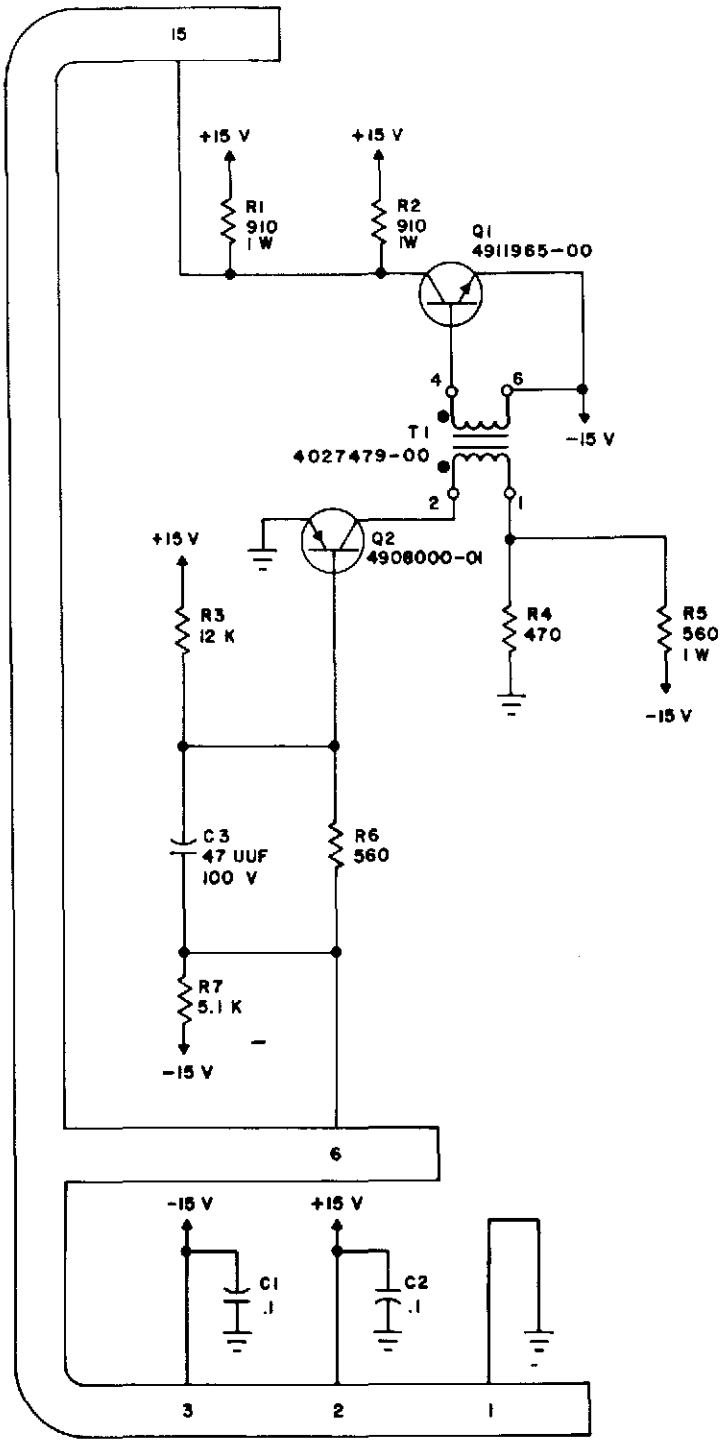


Figure 6-139. Line Capacitance Charger - A, Module Type 2740, Electrical Schematic

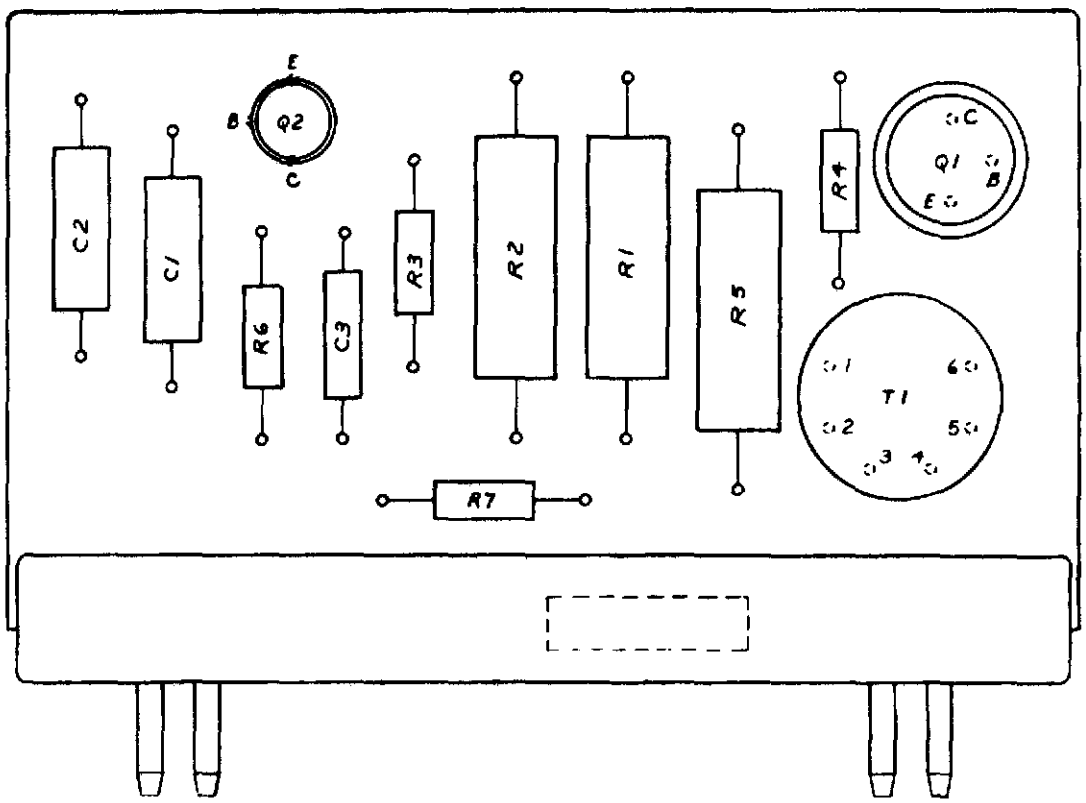


Figure 6-140. Module Type 2740 Component Layout

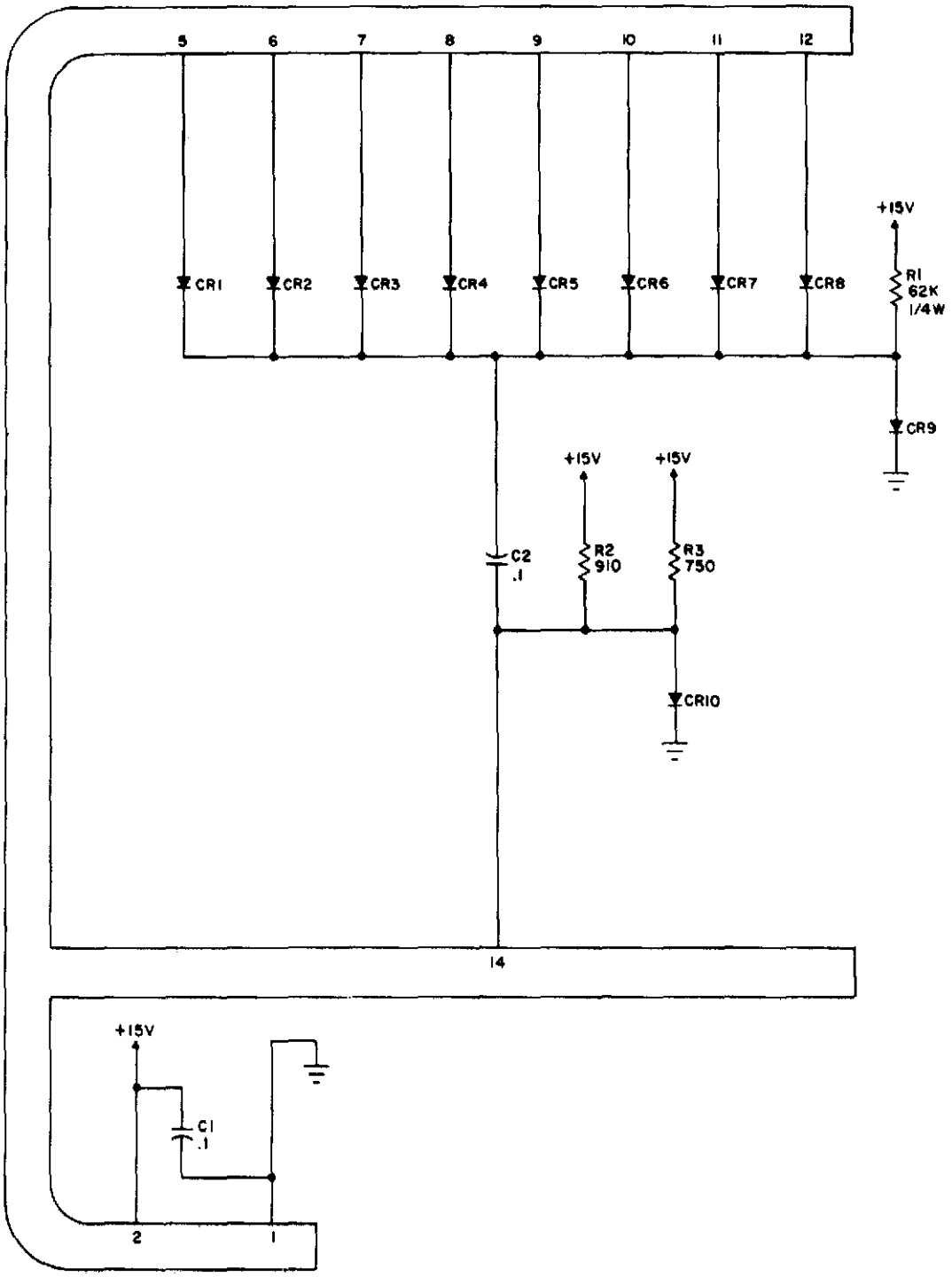


Figure 6-141. Line Capacitance Charger - B, Module Type 2750, Electrical Schematic

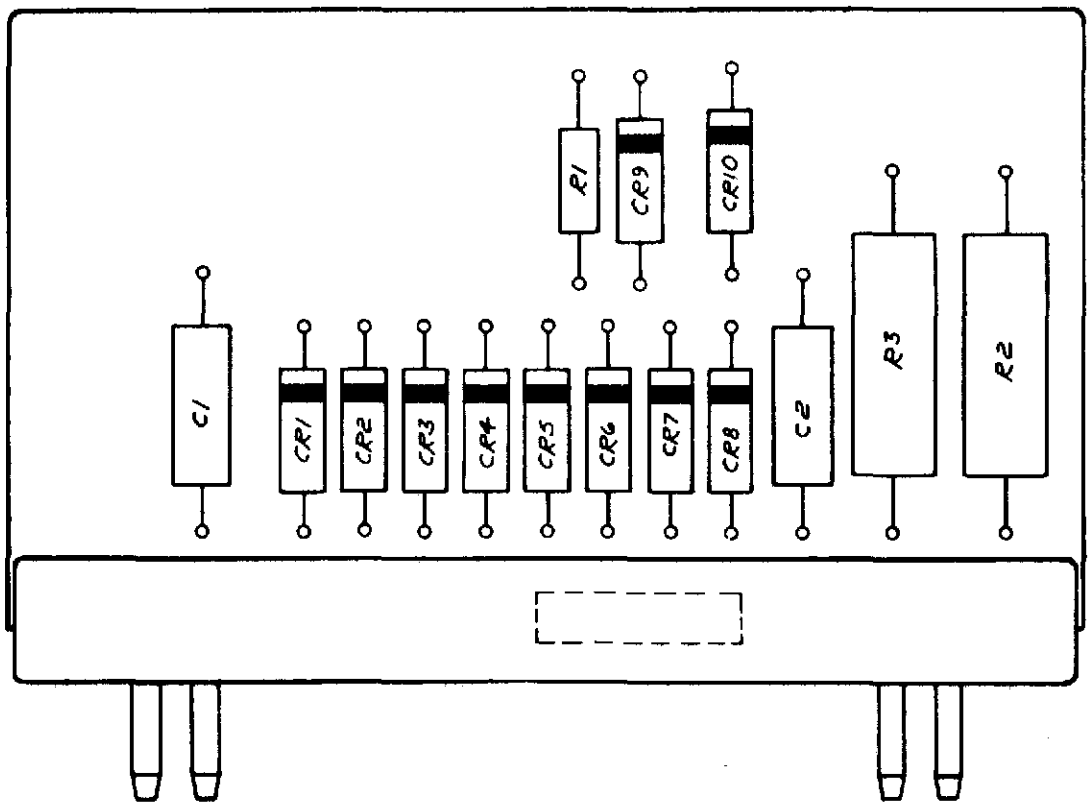


Figure 6-142. Module Type 2750 Component Layout

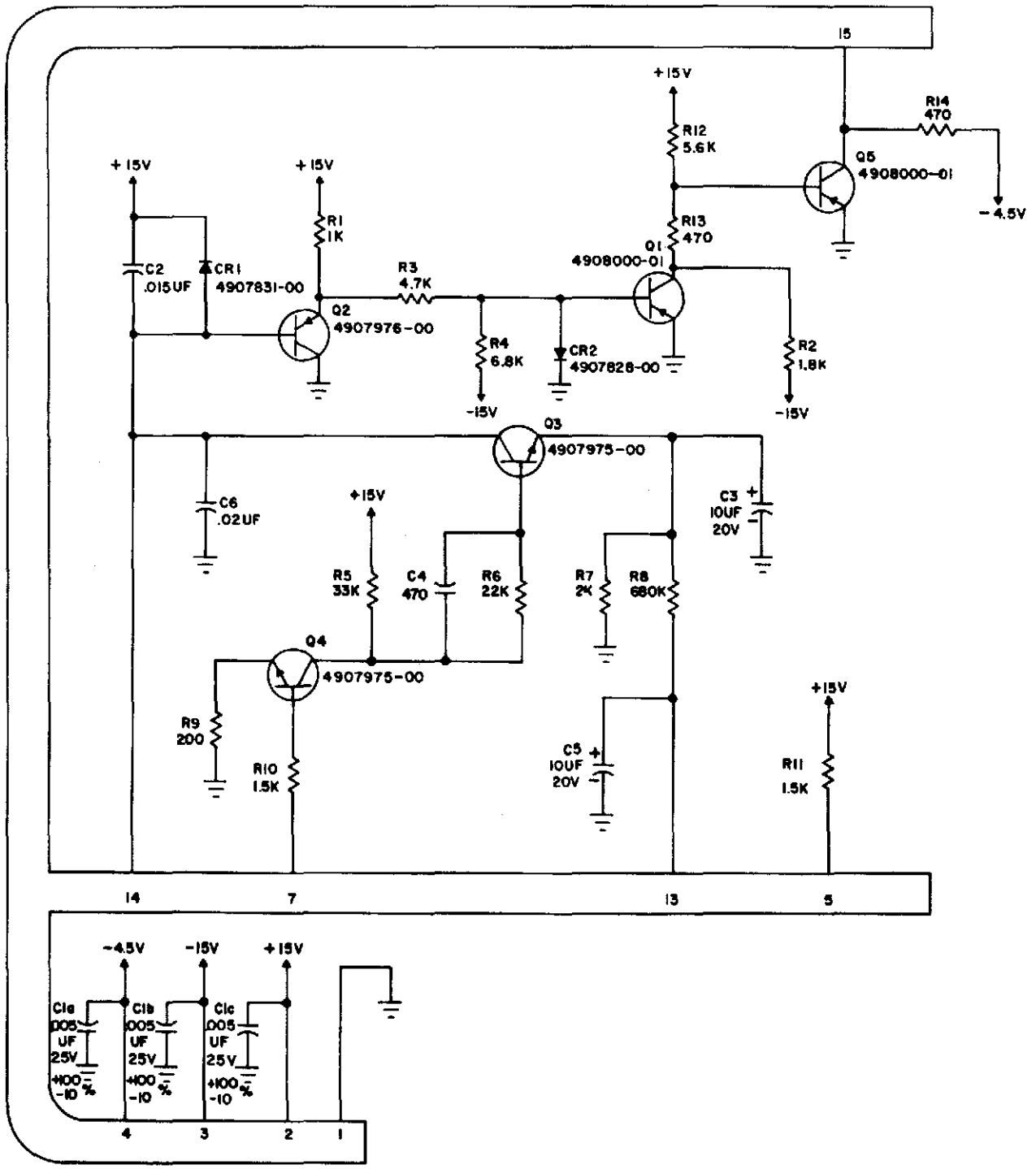


Figure 6-143. Oscillator Real Time Clock, Module Type 2760, Electrical Schematic

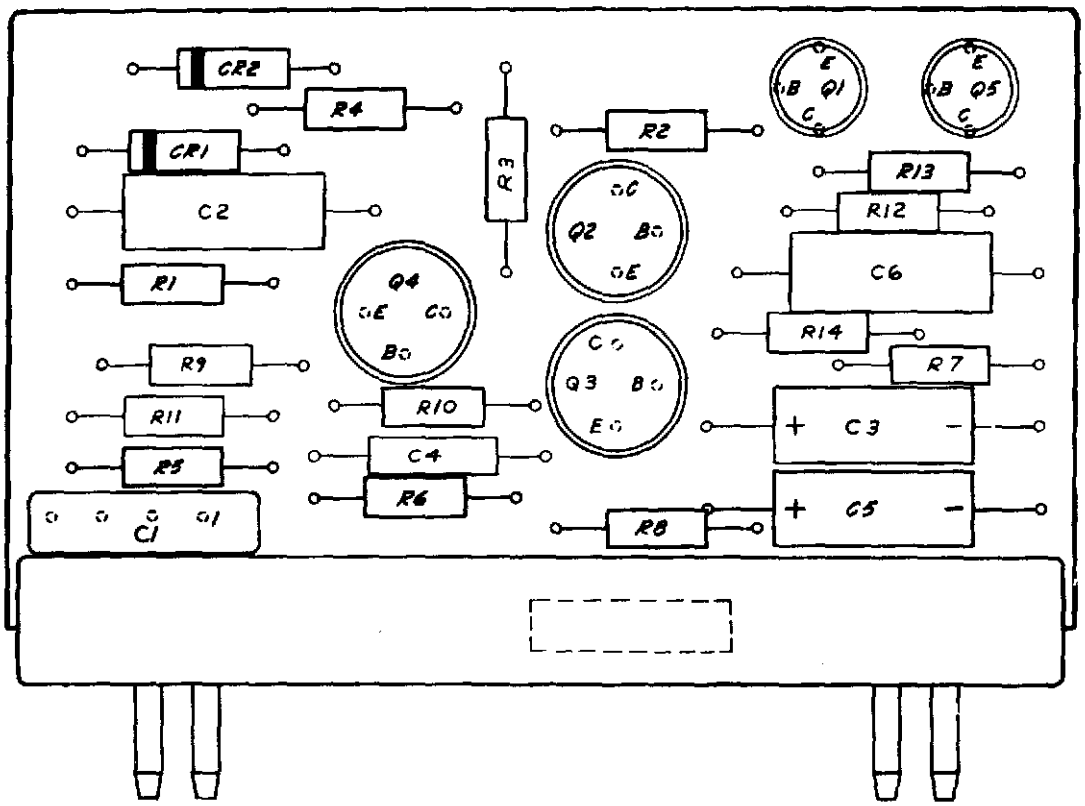


Figure 6-144. Module Type 2760 Component Layout

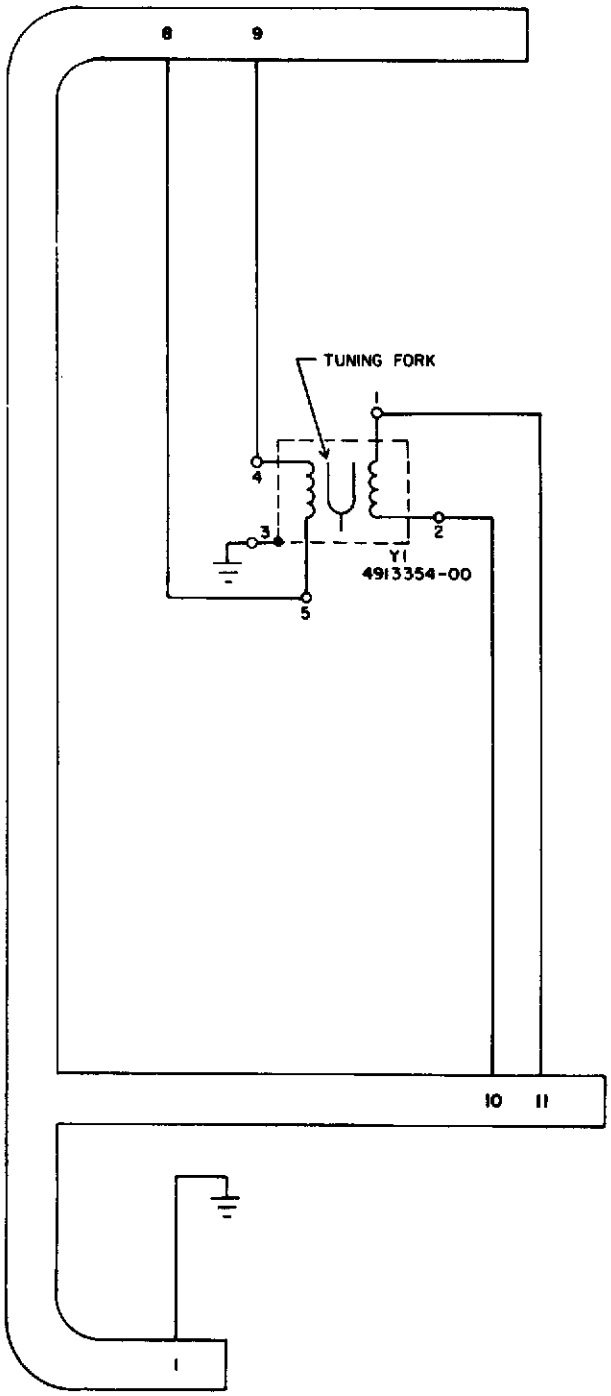


Figure 6-145. Tuning Fork Unit - 1.024kc, Module Type 2770, Electrical Schematic

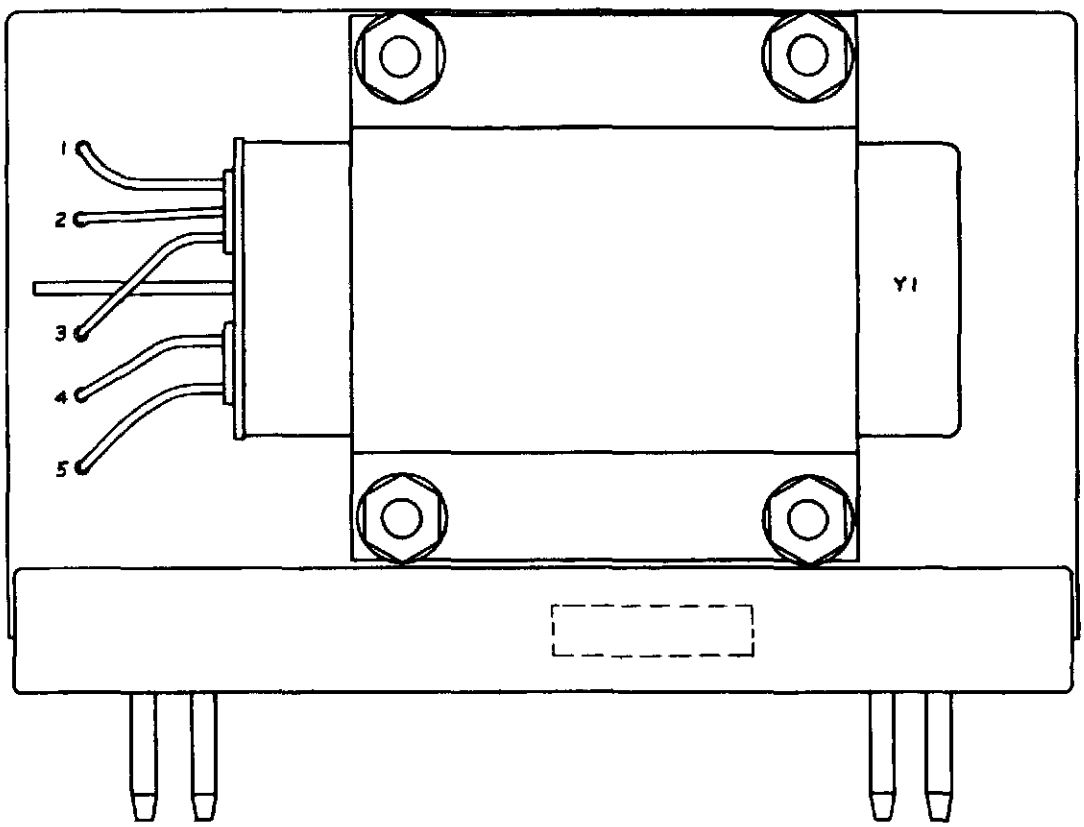


Figure 6-146. Module Type 2770 Component Layout

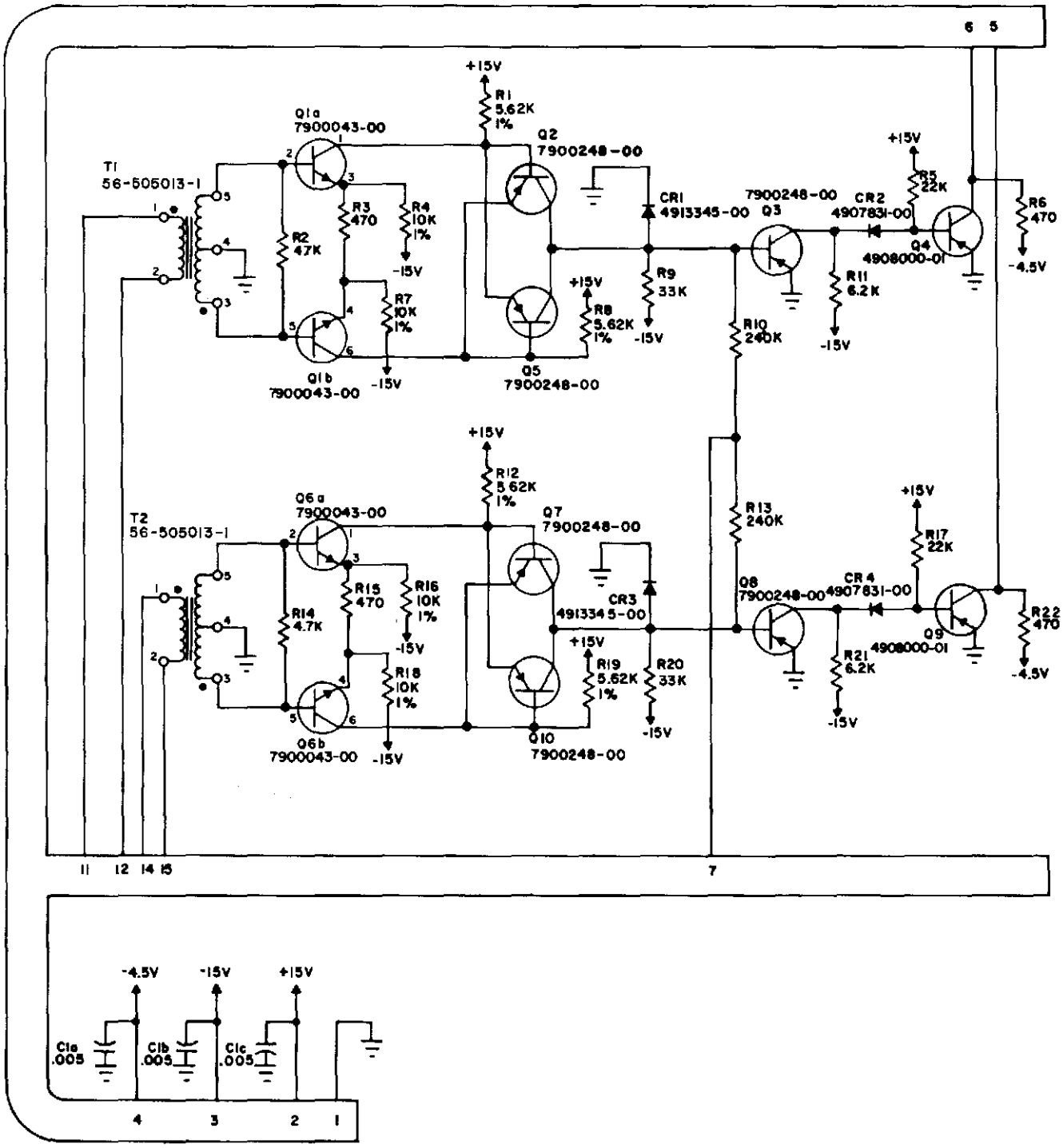


Figure 6-147. Sense Amplifier, Module Type 2851, Electrical Schematic

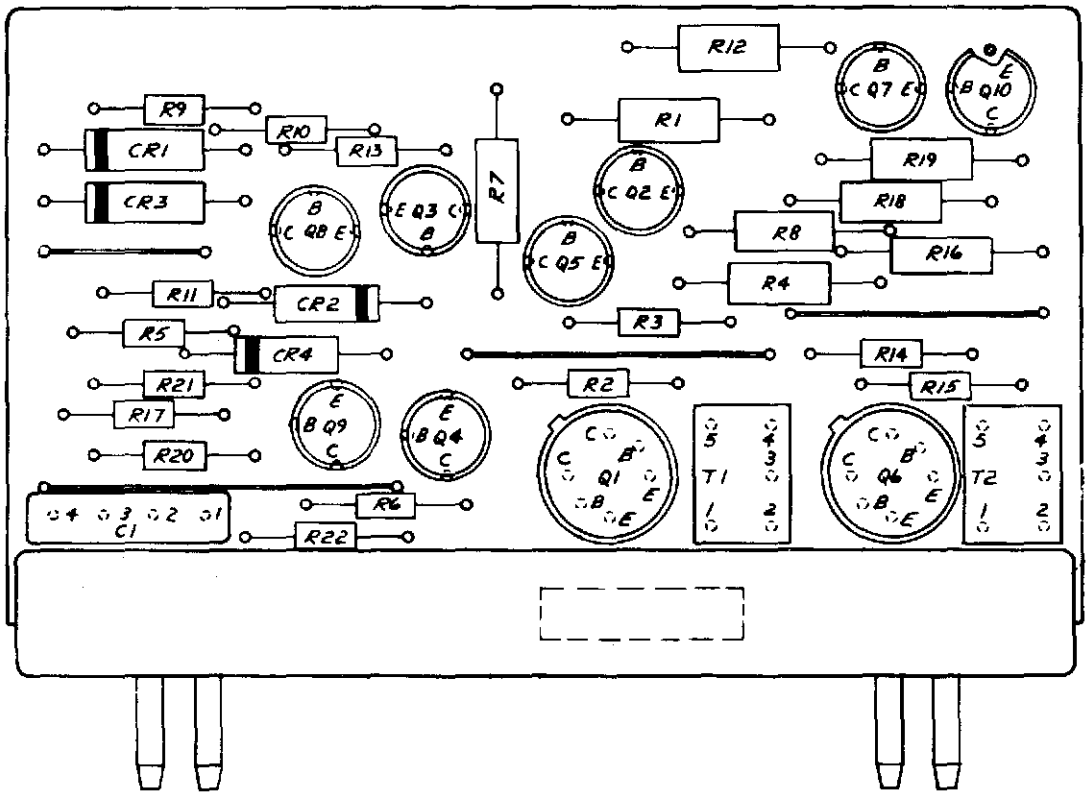


Figure 6-148. Module Type 2851 Component Layout

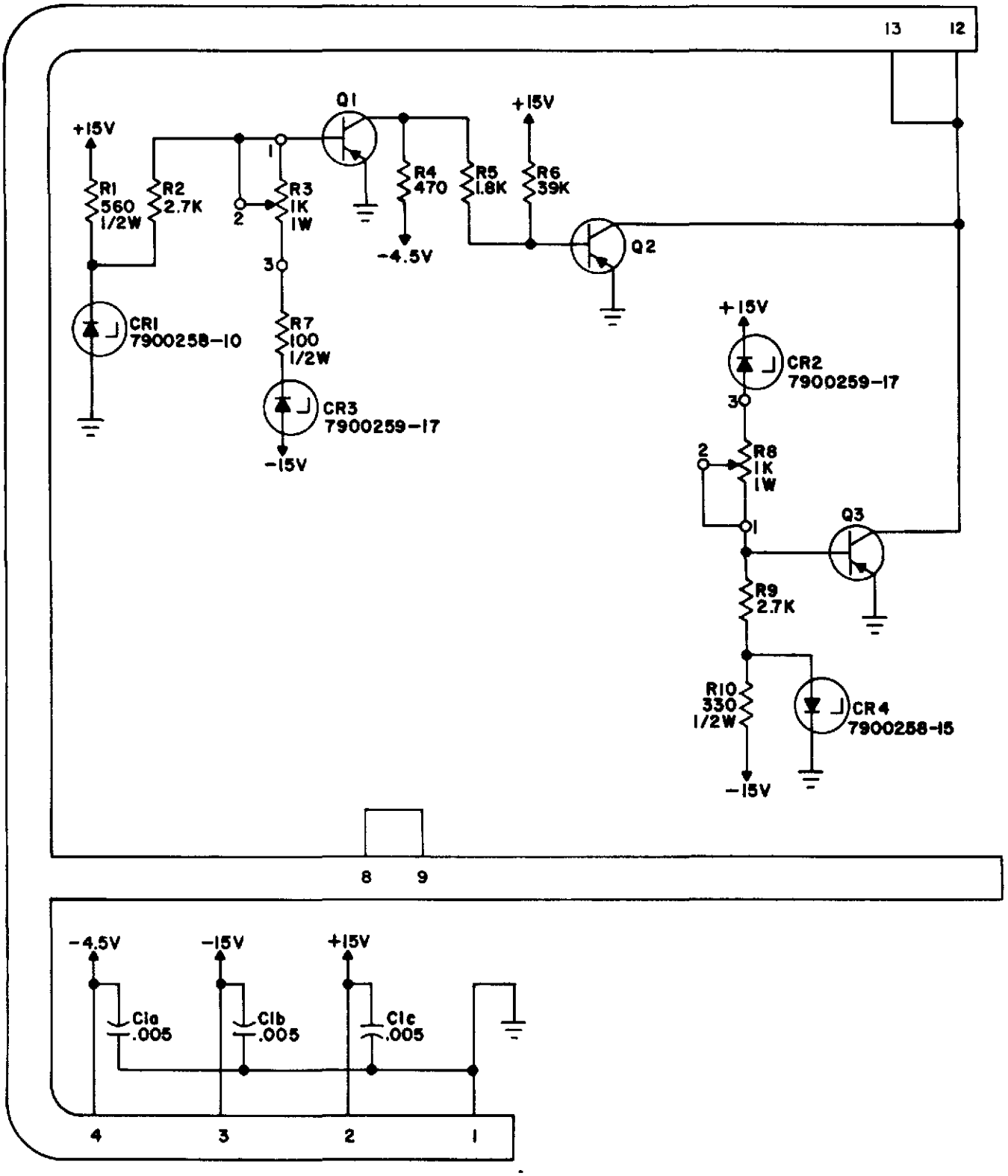


Figure 6-149. Sensor Voltage +15, -15, Module Type 2880, Electrical Schematic

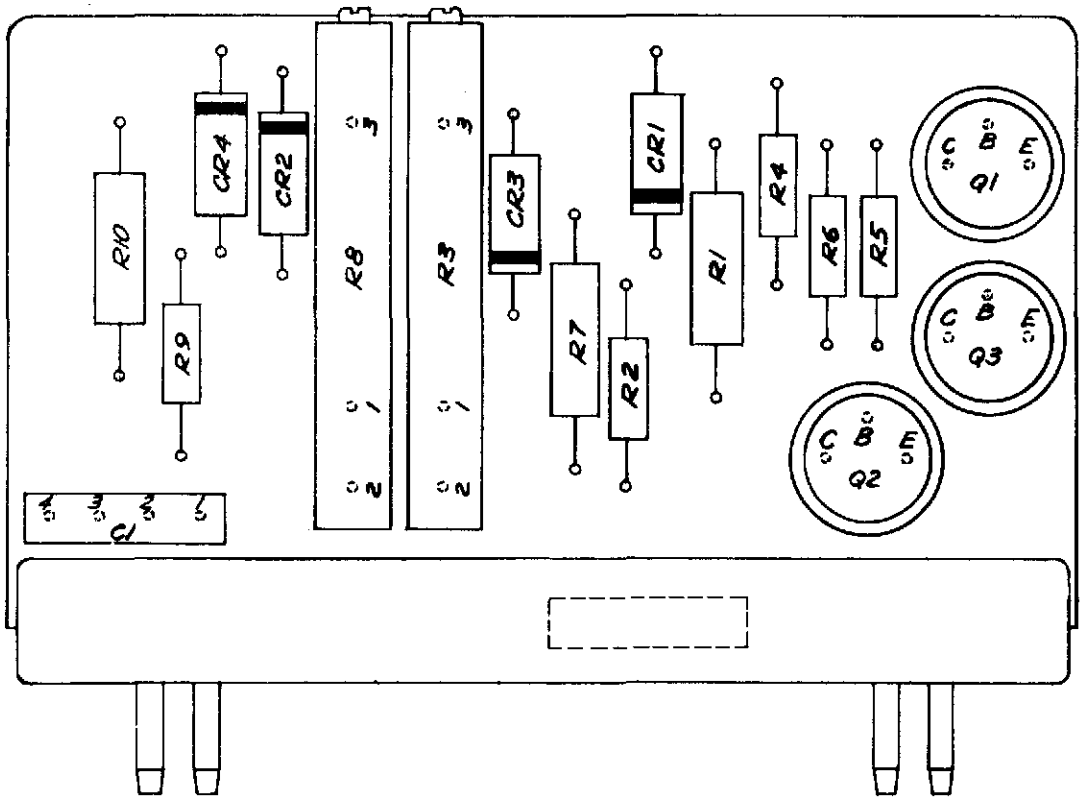


Figure 6-150. Module Type 2880 Component Layout

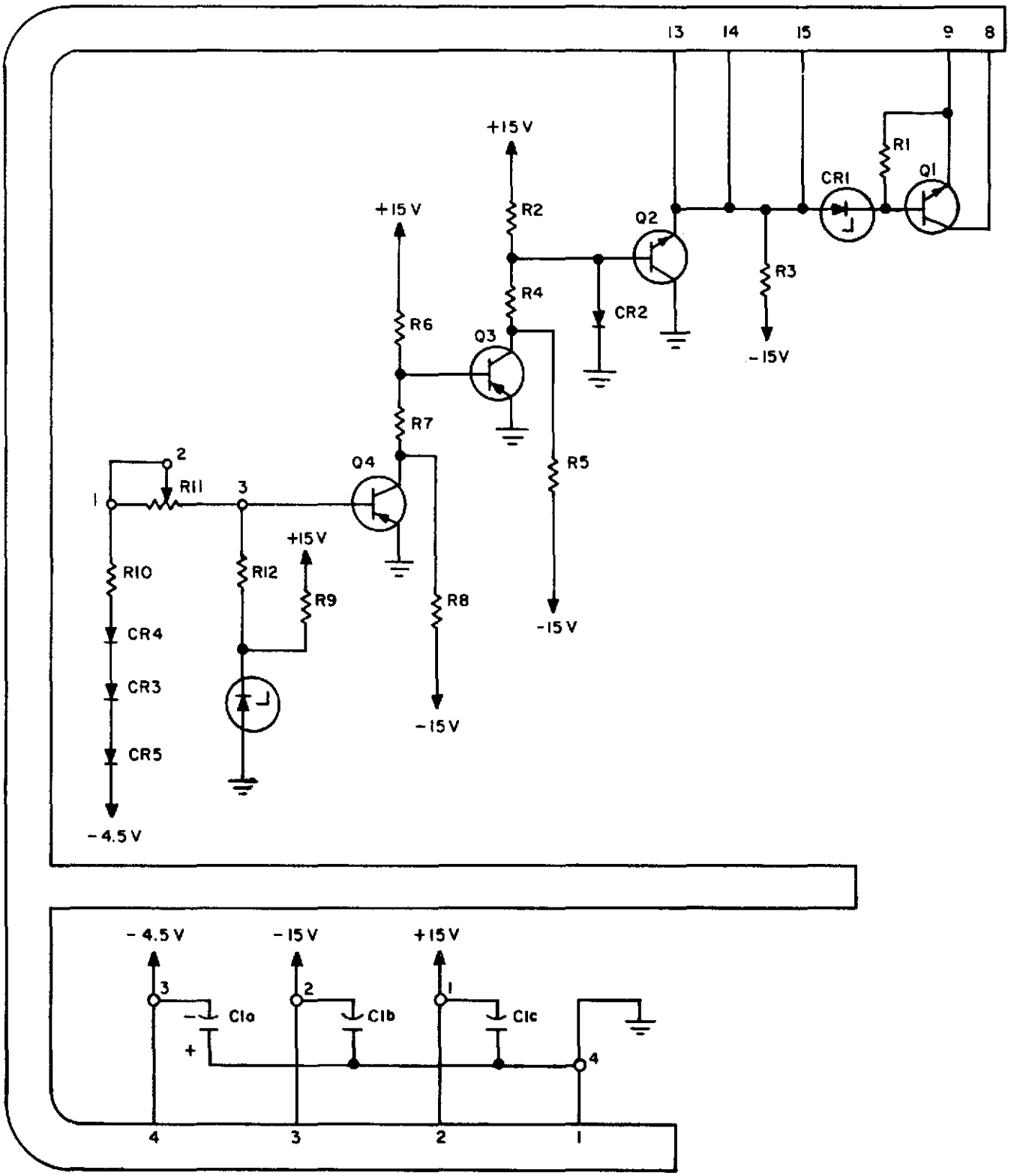


Figure 6-151. Sensor Voltage, -4.5 and Switch, Module Type 2890, Electrical Schematic

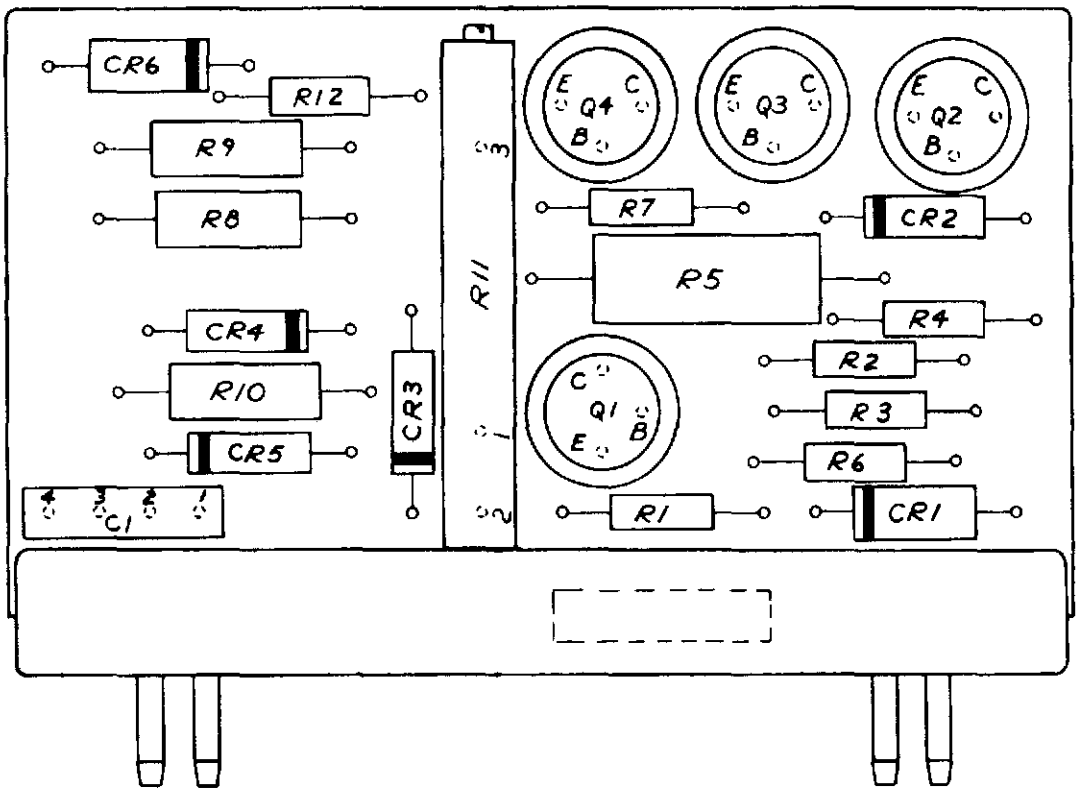


Figure 6-152. Module Type 2890 Component Layout

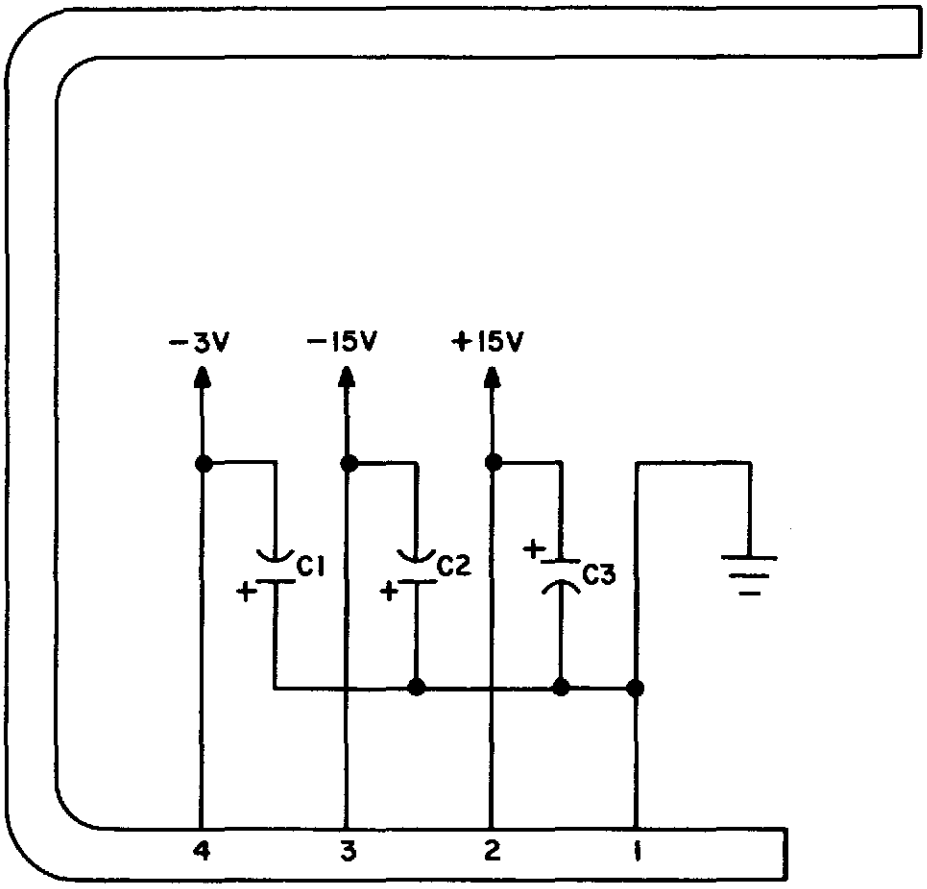


Figure 6-153. Capacitor Assembly, Module Type 3180, Electrical Schematic