TYPE 1840 MODIFIED MAGNETIC TAPE SUBSYSTEM

VOLUME I

SPERRY UNIVAC
DEFENSE SYSTEMS

TECHNICAL MANUAL

for

TYPE 1840 MODIFIED
MAGNETIC TAPE SUBSYSTEMS

VOLUME I
SECTIONS 1-6

JANUARY 1974

PX 7985-1-2

SPERRY UNIVAC
DEFENSE SYSTEMS

LIST OF EFFECTIVE PAGES

PAGE NUMBER	CHANGE IN EFFECT	PAGE NUMBER	CHANGE IN EFFECT
Volume I			
Title	Original	Figures	
ii to xv	Original	006 to 019	Original
1-0 to 1-10	Original	072 to 037	Original
2-1 to 2-28		040 to 063	Original
3-1 to 3-28	Original	066 to 074	Original
4-1 to 4-310	Original	078 to 113	Original
5-1 to 5-58	Original	115 to 126	Original
6-1 to 6-54	Original	130 to 175	Original
		175A	Original
		176	Original
Volume II		176A	Original
Title	Original	177	Original
iii to vi	Original	177A	Original
7-1 to 7-2	Original	178	Original
Dwg. No.		178A	Original
7059925-00	Original	179	Original
7059941(2)	Original	179A	Original
7059907	Original	180	Original
		180A	Original
		181	Original
		181A	Original
		182	Original
		183	Original

TABLE OF CONTENTS

SECTION 1 - GENERAL INFORMATION

SECTION 2 - INSTALLATION

SECTION 3 - OPERATION

TABLE OF CONTENTS (CONT)

SECTION 3 - OPERATION (CONT)

SECTION 4 - PRINCIPLES OF OPERATION

TABLE OF CONTENTS (CONT)

SECTION 4 - PRINCIPLES OF OPERATION (CONT)

TABLE OF CONTENTS (CONT)

SECTION 4 - PRINCIPLES OF OPERATION (CONT)

TABLE OF CONTENTS (CONT)

SECTION 4 - PRINCIPLES OF OPERATION (CONT)

TABLE OF CONTENTS (CONT)

SECTION 4 - PRINCIPLES OF OPERATION (CONT)

SECTION 5 - MAINTENANCE

SECTION 6 - PARTS LIST

TABLE OF CONTENTS (CONT)

SECTION 6 - PARTS LIST (CONT)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (CONT)

LIST OF ILLUSTRATIONS (CONT)

LIST OF ILLUSTRATIONS (CONT)

LIST OF TABLES

LIST OF TABLES (CONT)

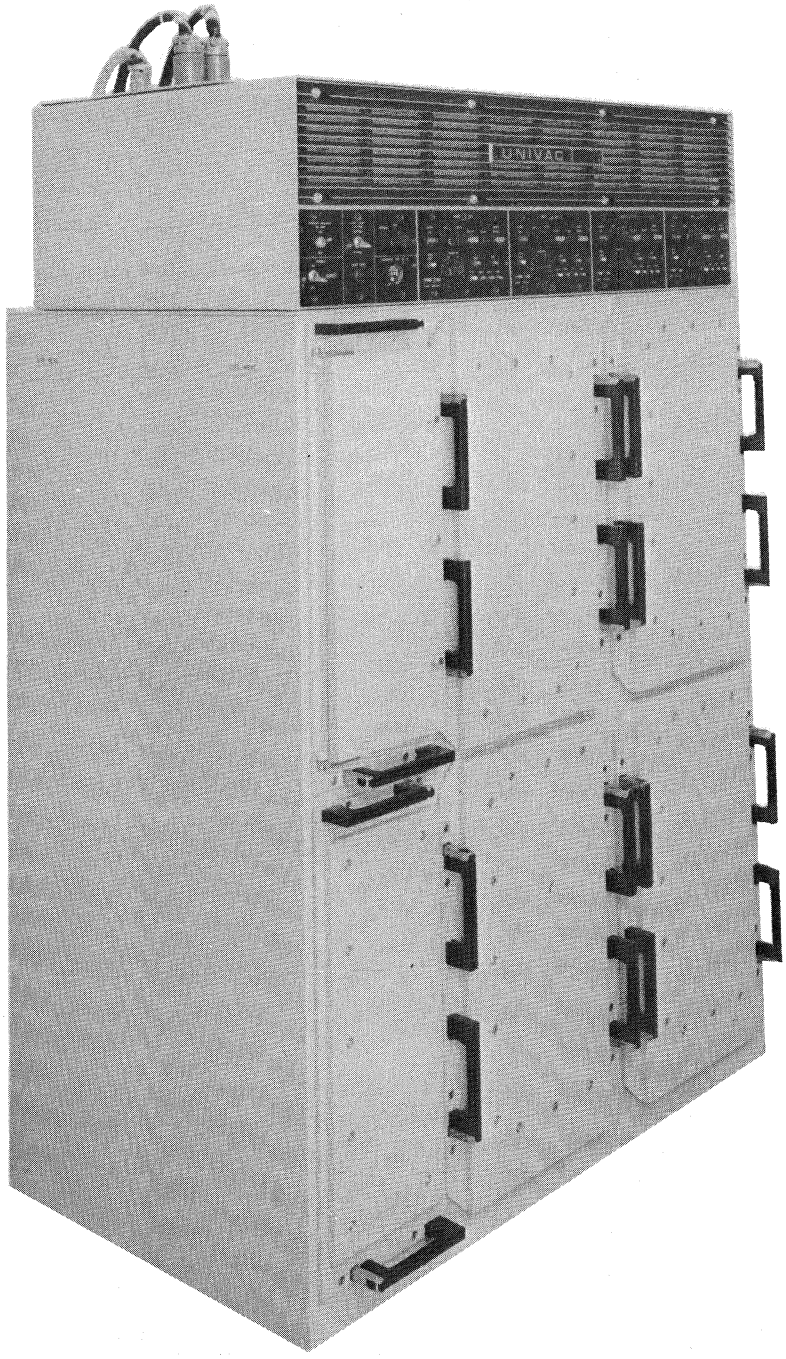


Figure 1-1. 1840 Modified Magnetic Tape Subsystem

SECTION 1

GENERAL INFORMATION

1-1. SCOPE.

This manual provides information and instructions for installing, operating, troubleshooting, and maintaining the UNIVAC® Type 1840 (Mod) Magnetic Tape Subsystem (MTS). The MTS, shown in figure 1-1, is a magnetic tape unit designed with the flexibility to allow simple alignment with a wide variety of data processing systems. Its ruggedized construction and operational flexibility make it the ideal tape unit for new systems installation as well as for upgrading or replacing elements of existing systems. Built to meet MIL-E-16400, the subsystem satisfies the functional requirements of industry standard 7-track or 9-track recording formats.

System compatibility is accomplished by the internal microprogrammed controller (MPC). This controller's read only memory (ROM) is normally programmed to implement:

1) Seven or nine-track operation

2) 16, 18, 24, 30, 32, and 36 bit computer word length

3) UNIVAC 1240 (RD-270)/UNIVAC 1540 (RD-294) operating modes

4) Duplex computer control

5) Off-line tape to printer, tape to card punch, card reader to tape or as specified by contract.

Important features such as diagnostic programs and the ability to operate with computers other than Univac are easily provided by adding or substituting appropriate programs to the microprogrammed controller's repertoire. Other available features include seven and nine-track operation; variable number of tape transport units; and -3 volt, -15 volt or +3.5 volt interface signal levels. These are achieved by hardware substitution and/or circuit card additions.

The tape transports "auto-load" feature simplifies tape loading. Gentle tape movement is accomplished by combining the features of vacuum column buffers and high precision tape servos. Quick starts and stops are eliminated and high current transients are eradicated. The result is longer tape life, less head wear, and lower power requirements.

1-2. DESCRIPTION.

a. PHYSICAL DESCRIPTION. - The ruggedized light-weight MTS fits most military applications and environments.

Lightweight (a four tape handler configuration weighs 980 pounds) and small in size, it is especially attractive for mobile and heli-hut applications. Enclosed within a shock-proof, environmentally designed cabinet, it is capable of operating from normally available ship or aircraft power. This eliminates the need for regulated power.

The cabinet accommodates up to four tape transports. Slide mounts allow the control unit, power supply, and tape transport modules to be pulled forward from the cabinet without disrupting operation, thus making tape loading easy and providing ready access to components for routine servicing and corrective maintenance. Functional modularity allows easy packaging within unique customer cabinetry.

The power switch and controls for operating the MTS with 1, 2, 3, or 4 tape transports are located on the top, front system control panel, normally referred to as the control panel. Input, output and power cable connectors are mounted on the recessed rear portion of the cabinet top.

b. FUNCTIONAL DESCRIPTION.

(1) CONTROL UNIT. - The control unit contains the functions required for controlling the subsystem and accommodating the varied requirements of the external data processing system. Its heart is the microprogrammed controller (MPC) which serves as a data switch and control center for all transfers within the tape subsystem. High transfer rates are obtained by function overlapped operations over a two bus system. Compatibility with specific magnetic tape equipment types or industry standards is achieved by changing the instructions contained within the controller's read only memory. These instructions define, interpret, and control the functional operation of the required system configuration.

In conjunction with the arithmetic logic, a scratch pad memory, service request circuits and associated control logic, the MPC performs the following functions:

1) Converts computer words to tape frames as specified by computer programmed modulus, and vice versa.

2) Longitudinal parity formation and checking.

3) External function (computer commands) interpretation.

4) Initiation of start/stop delays.

5) Status word formation.

6) Search comparison.

7) Frame count check.

8) End of record detection.

9) Input and output timing error detection.

10) Lateral parity formation and checking.

11) Cyclic redundancy check.

12) Tape transport selection.

Control unit interface circuits provide the communication links between the MPC and computer and, between the MPC and any one of up to four tape transports. Additional functions performed by the interface circuits include:

1) Read/Write amplification.

2) De-Skewing.

3) Density control and timing.

4) Time delays.

5) Dual computer control.

6) Computer electrical interface matching.

7) Off-line channel interface and timing.

The front mounted maintenance control panel contains the controls, indicators, and test points required for monitoring the dynamic operation of the unit while performing routine maintenance and troubleshooting procedures.

(2) MAGNETIC TAPE TRANSPORT. - The magnetic tape transport is designed to meet the electrical and environmental requirements of MIL-E-16400; the functional requirements of standard 7-track and 9-track recording formats; and the mechanical requirements of a reliable, vacuum buffer, tape moving mechanism. Long life heads and pluggable assemblies minimize maintenance requirements. Transport utilization is not limited to the 1840(Mod). The 7-track version is functionally, electrically and mechanically compatible with transports in the UNIVAC 1240 and UNIVAC 1540 Magnetic Tape Units. Retrofit kits are available which allow modernizing the 1240 and 1540 tape units with the 1840(Mod) magnetic tape transport. No special tools are required for installation. The 1840(Mod) transport can be installed by personnel trained in routine 1240/1540 maintenance procedures.

1-3. EQUIPMENT OPTIONS.

The MTS is available with several options to alter or vary operation. Tape speed, number of tracks, interface signal voltages, number of transports, and input power are several of these options. See table 1-1 for a listing of the available options. The MTS is constructed so that it may be modified to any optional configuration except for a change in the frequency of the input power and for expanding the subsystem from two to four transports.

1-4. QUICK REFERENCE DATA.

Quick reference data for the MTS is listed in table 1-2. Quick reference data for the MTT is contained in section one of Univac technical manual PX7984.

1-5. EQUIPMENT LISTS.

a. EQUIPMENT AND PUBLICATIONS SUPPLIED. - Table 1-3 lists the equipment and publications supplied with each MTS.

b. EQUIPMENT REQUIRED BUT NOT SUPPLIED. - Table 1-4 lists the equipment required but not supplied with the MTS.

TABLE 1-1. EQUIPMENT OPTIONS

OPTION	DESCRIPTION
Input Power	3-phase, 400 Hz, 4-wire WYE connected, 208 volts ac line-to-line: 3-phase, 400 Hz, 3-wire delta connected, 115 volts ac line-to-line. 1-phase, 60 Hz, 3-wire, 115 volts ac.
Number of Tape Transports	2 or 4 tape transports
Recording Tracks	7 or 9 tracks
Input/Output Signal Voltage Levels	-15 volts, -3 volts, or +3.5 volts interface signal levels.
Recording Technique	7 track - NRZI 9 track - NRZI or phase encoded (PE) and NRZI
Off Line Options	Program 1, 2 and 3 switch positions allow off-line operation as specified by contract and associated control program.
Input Power Filtering	Line Filters or no line filters.

TABLE 1-2. QUICK REFERENCE DATA

ITEM	DATA
PHYSICAL CHARACTERISTICS	
Height	60 inches
Width 2 tape transports 4 tape transports	22.75 inches 37.0 inches
Depth	28.0 inches
Size 2 tape transports 4 tape transports	60"H x 28"D x 22.75"W 60"H x 28"D x 37"W
Volume 2 tape transports 4 tape transports	22 cu. feet (approx) 36 cu. feet (approx)
Weight 2 tape transports 4 tape transports	730 pounds 980 pounds

TABLE 1-2. QUICK REFERENCE DATA (CONT)

ITEM	DATA
PHYSICAL CHARACTERISTICS	
Input Voltage	3Ø, 400 Hz ±5%, 208 Vac ±10%; 3Ø, 400 Hz ±5%, 115 Vac ±10%, or 1Ø, 60 Hz ±5%, 115 Vac ±10%.
Input Power	
2 Transport	2000 watts max.
4 Transport	3000 watts max.
Cooling	Direct Air Flow
INTERFACE CHARACTERISTICS	
Voltage levels	-15 volts; +3.5 and -3 volt computer interfaces by option, achieved by substituting line-driver amplifier and input amplifier pc cards.
Control lines	External function request, external function acknowledge, external interrupt request, input data request, input acknowledge, output data request, output acknowledge.
Word Size	18 bits parallel basic; to 36 bits by addition of pc cards.
FUNCTIONAL CHARACTERISTICS	
Operation Under Computer Control:	
Read	Forward or reverse
Write	Forward
Tape markers	Recognize BOT and EOT reflective marker signals; read and write tape marks
Space	Forward or reverse
Space file	Forward or reverse
Search	Forward or reverse
Search file	Forward or reverse
Rewind	To load point, with or without automatic read of first record

TABLE 1-2. QUICK REFERENCE DATA (CONT)

ITEM	DATA
FUNCTIONAL CHARACTERISTICS	
Modulus Selection	7-Track - 3, 4, 5 or 6 9-Track - 2, 3, 4 or 5
Parity	Odd or even
Density select	200, 556, 800, or 1600 (PE only) bits per inch
Duplexing	Release, request, or demand control
Recording (7-Track only)	Octal or bioctal

TABLE 1-3. EQUIPMENT AND PUBLICATIONS SUPPLIED

QUANTITY	ITEM	UNIVAC DESIGNATION
1	Magnetic Tape Subsystem	7059800-XX
2	Technical Manual for Type 1840 (Modified) Magnetic Tape Subsystem	PX 7985
2	Technical Manual for Type 1840 (Modified) Magnetic Tape Transport	PX 7984

TABLE 1-4. EQUIPMENT REQUIRED BUT NOT SUPPLIED

ITEM	QTY	FUNCTION	SOURCE AND DESIGNATION
Power Cable	1	Supply Prime Power to MTS	
Signal Cable	2 or 4	Connect from one or two computer(s) to MTS for I/O signals	
Card Extender	1	Extend transport PC cards for testing and trouble-shooting	Univac No. 7074100-00 FSN 5895 437-3825
Card Extractor	1	Remove transport PC cards	Univac No. 7073472-00
Card Extender	1	Extend controller PC cards for testing and trouble-shooting	Univac No. 7099639-00
Card Extractor	1	Remove controller PC cards	Univac No. 7902607-03
Hub Alignment Tool	1	Align hubs on transports	Univac No. 7600732-00

TABLE 1-4. EQUIPMENT REQUIRED BUT NOT SUPPLIED (CONT)

ITEM	QTY	FUNCTION	SOURCE AND DESIGNATION
Set Block	1	Adjust height of capstan	Univac No. 7602199-00
Hub Height Gauge	1	Position Supply Reel Hub	Univac No. 7602200-00
Height Gauge	1	Position Take-up Reel Hub	Univac No. 7602201-00
Wire-Wrap Gun (battery powered, portable)	1	Make wiring changes and repairs	Univac No. 7902119-00 FSN 5130 919-3486
Battery	1	Power for wire-wrap gun	Univac No. 7902118-01
Charger	1	Enable charging of wire-wrap gun battery	Univac No. 7902118-02
Wire-Wrap Sleeve 30 ga	1	Wrap 30 ga wire on wire-wrap terminals	Univac No. 7902129-03 FSN 5130 987-7056
Wire-Wrap Bit 30 ga	1	Wrap 30 ga wire on 0.025 in. square terminals	Univac No. 7902131-00 FSN 5130 731-5942
Wire-Wrap Bit 30 ga	1	Wrap 30 ga wire on 0.035 to 0.050 in. square terminals	Univac No. 7902131-05 FSN 5130 731-5985
Wire-Wrap Sleeve 26 ga	1	Wrap 26 ga wire on wire-wrap terminals	Univac No. 7902129-04 FSN 5130 459-4485
Wire-Wrap Bit 26 ga	1	Wrap 26 ga wire on wire-wrap terminals	Univac No. 7902131-04 FSN 5130 134-4570
Wire-Wrap Unwrap Tool	1	Unwrap 30 ga wire	Univac No. 7902130-00 FSN 5130 854-9888
Wire-Wrap Unwrap Tool	1	Unwrap 26 ga wire	Univac No. 7902130-01 FSN 5120 104-9022
No Nik Stripper	1	Strip 30 ga wire	Univac No. 7904445-00
No Nik Stripper	1	Strip 26 ga wire	Univac No. 7904445-01
Oscilloscope (dual trace)	1	Display waveforms for check-outs and troubleshooting	Tektronix Model 453A or equivalent Univac No. 7904455-00 FSN 6625 765-9181
Probe Volt X10	2	For use with oscilloscope	Tektronix Type P6008 or equivalent Univac No. 7904453-00 FSN 6625 896-1918

TABLE 1-4. EQUIPMENT REQUIRED BUT NOT SUPPLIED (CONT)

ITEM	QTY	FUNCTION	SOURCE AND DESIGNATION
Multimeter	1	Make general voltage, current and resistance measurements	Triplett Model 630A or equivalent
Master Skew Tape, TS800	1	Check 7-track read deskew	Univac No. 7957157-01 IBM No. 432641
Magnetic Tape Markers (250)	AR	Fabricate test tapes and repair tapes	IBM No. 352407
Extraction Tool	1	Remove connector pins	Univac No. 7904604-00 MS24256R16
Soldering Iron, Miniature	1	For soldering components on repairable items	Univac No. 8865-137
Soldering Tip 3-64	1	For use with soldering iron	Univac No. 8865-322
Soldering Tip 3-32	1	For use with soldering iron	Univac No. 8865-323
Solder Removal Tool	1	Remove melted solder when repairing items	Univac No. 8869-318
Allen Wrenches (complete set)	1	Assembly and Disassembly of components	Commercial

1-6. SHIPPING DATA.

The MTS is normally shipped as a unit on such form of transportation deemed feasible unless otherwise stipulated by the customer. Uncrated weights and dimensions of the MTS are contained in table 1-2, those for the MTT are contained in PX 7984.

1-7. EQUIPMENT SIMILARITIES.

The similarities between various configurations of the Univac Type 1840 (Modified) Magnetic Tape Subsystem are listed in table 1-5.

1-8. NONSTANDARD TERMS AND ABBREVIATIONS.

Nonstandard terms and abbreviations used in this manual are listed in table 1-6.

TABLE 1-5. EQUIPMENT SIMILARITIES

UNIVAC PART NUMBER	7 Track	9 Track	115 Volt	208 Volt	2 Transport	4 Transport	MAX BIT DENSITY	
							800	1600
7059800-03	X		X			X	X	
7059800-04		X		X		X	X	
7059800-05	X		X		X		X	
7059800-06		X	X			X		X
7059800-07		X		X		X	X	
7059800-08		X		X		X		X
7059800-09	X		X			X	X	
7059800-10	X		X		X		X	
7059800-11	X			X		X	X	
7059800-12		X	X		X			X
7059800-13	X			X		X	X	
7059800-14		X		X	X			X

TABLE 1-6. NONSTANDARD TERMS AND ABBREVIATIONS

ABBREVIATION	TERM
BOT	Beginning of Tape
CNTL	Control
COMP	Computer
DPLX	Duplex
DSKW	Deskewed
EF	External Function
EFA	External Function Acknowledge
EFR	External Function Request

TABLE 1-6. NONSTANDARD TERMS AND ABBREVIATIONS (CONT)

ABBREVIATION	TERM
EI	External Interrupt
EIR	External Interrupt Request
EOT	End of Tape
FCTN, FUNC or FUNCT	Function
FR	Function Register
IA	Input Acknowledge
IDR	Input Data Request
INH	Inhibit
INT	Interrupt
IRG	Interrecord Gap
LONG PAR	Longitudinal Parity
MCLR	Master Clear
MTS	Magnetic Tape Subsystem
MTT	Magnetic Tape Transport
MSEC	Millisecond
OD	Output Data
ODA	Output Data Acknowledge
ODR	Output Data Request
PAR	Parity
RC	Read Control
REG	Register
REV	Reverse
RWC	Read Write Control
RWD	Rewind
SSC	Start Stop Control
SWC	Start Write Control

SECTION 2

INSTALLATION

2-1. UNPACKING AND HANDLING.

The MTS, including the Magnetic Tape Transports, is crated and shipped as an assembled unit. The method of crating and shipping is governed by customer requirements. Follow normal unpacking procedures to remove the unit from its protective covering preferrably at or near the installation site to prevent possible damage during subsequent moving. After unpacking, inspect the unit for possible interior and exterior damage. During this inspection, do not extend more than one slide mounted assembly unless the MTS has been securely bolted to the deck. If damage is discovered, notify supervisory personnel.

Check to ensure that all items listed in table 1-3 have been received.

2-2. SITE SELECTION.

Place the MTS in an area which provides adequate ventilation and cooling air, adequate space for connecting cables, and ample space to extend units for maintenance procedures. See figure 2-1 for outline and dimensional data. To prevent possible data loss or signal attentuation, keep cable lengths to a minimum; but long enough to prevent strain on the connectors or sharp bends in the cable.

2-3. POWER REQUIREMENTS AND DISTRIBUTION.

The MTS is wired at the factory to operate on input power as listed in table 1-2. The system can be converted from one 400 Hz input voltage to the other by wiring changes in the field. The system cannot, however, be converted to operate from one input frequency to another.

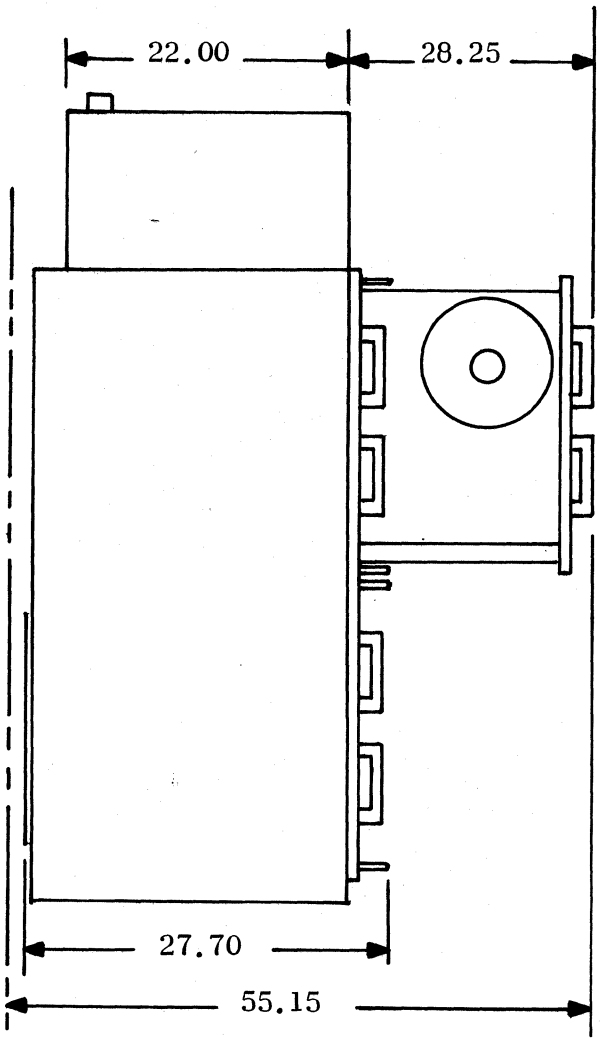
Power is applied to the MTS through J1 located on the recessed top panel and distributed as shown in figure 2-2. Input plug pin arrangements are shown in figure 2-3.

2-4. CABLE ASSEMBLIES.

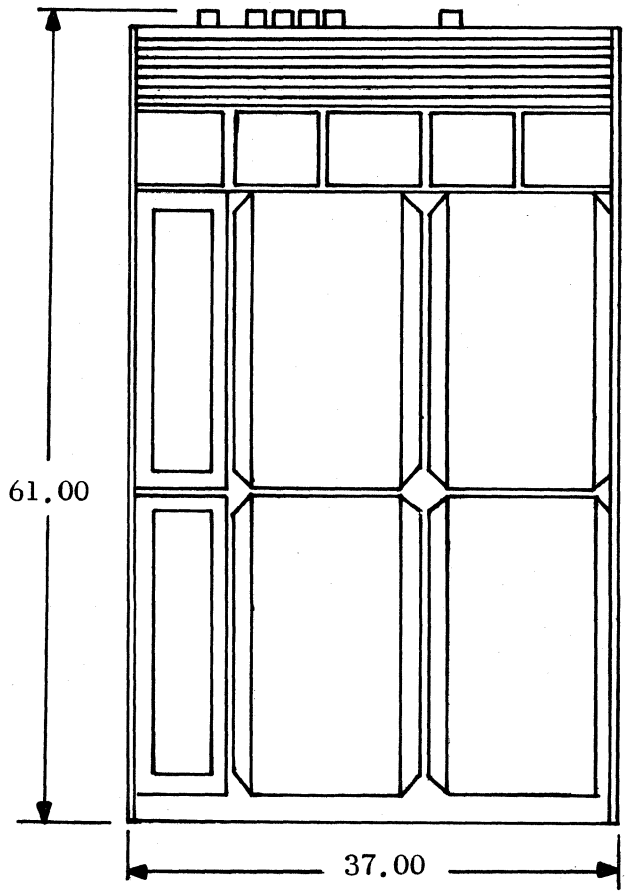
Five cable assemblies are required for operation of the MTS in the duplex mode. For operation of the MTS in the simplex mode, one input and one output cable may be eliminated. Table 2-1 contains the pin assignment for the input power cable which connects to J1. Tables 2-2 through 2-4 contain pin assignments for power cables. Input signal cable connector pin assignments are listed in tables 2-5 and 2-6. The remaining tables 2-7 through 2-10 in Section 2 contain the connector pin assignments for the MTS internal cables and jacks. Figure 2-4 identifies these cables and their destinations.

2-5. NAMEPLATE LOCATIONS.

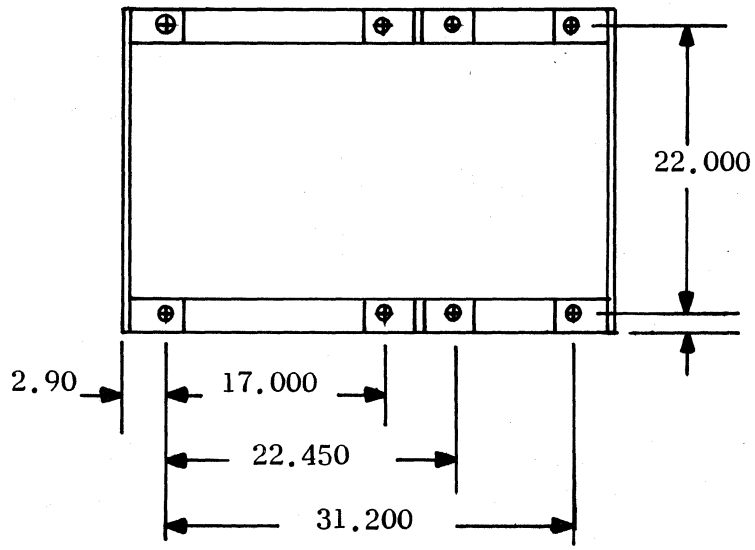
Figure 2-5 shows the locations of the various nameplates used in the MTS. One or two of the nameplates shown on the control unit portion of the figure may not be present in a given configuration due to options not being used.



LEFT SIDE VIEW



FRONT VIEW



BOTTOM VIEW

Figure 2-1. Outline Dimensional Data

NOTE 1: E5 IS CHASSIS BOLT NEAR TB1 (A1).

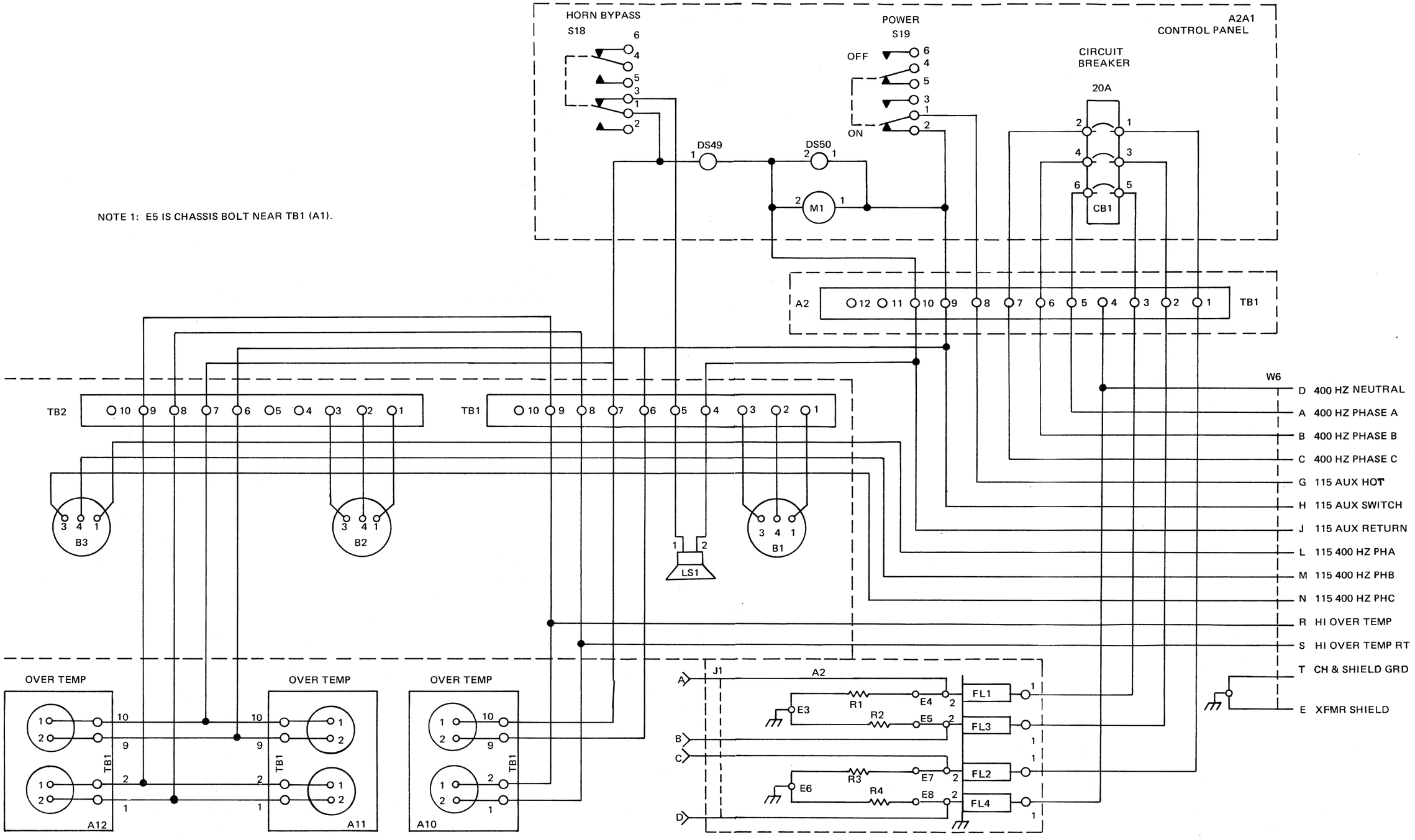
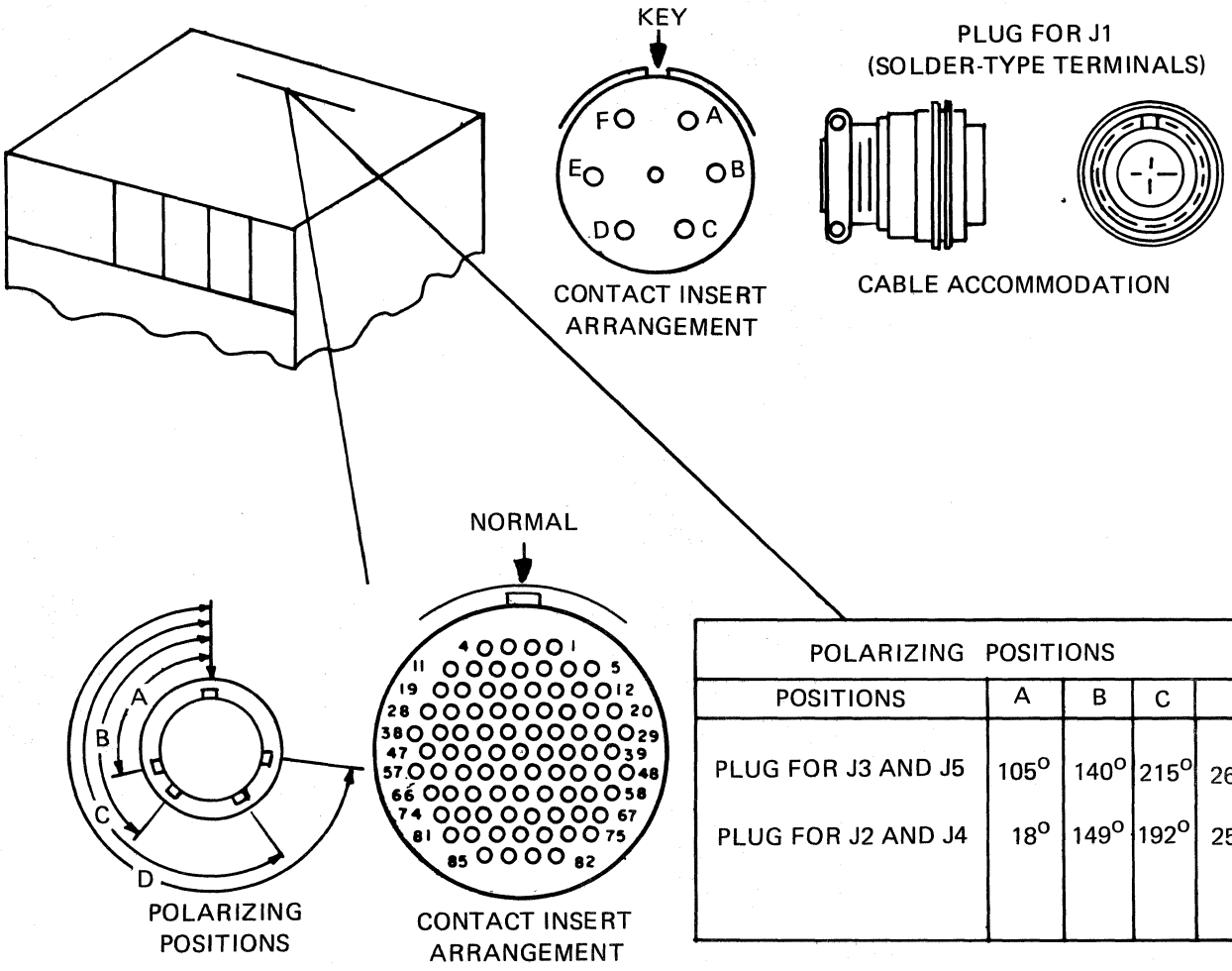
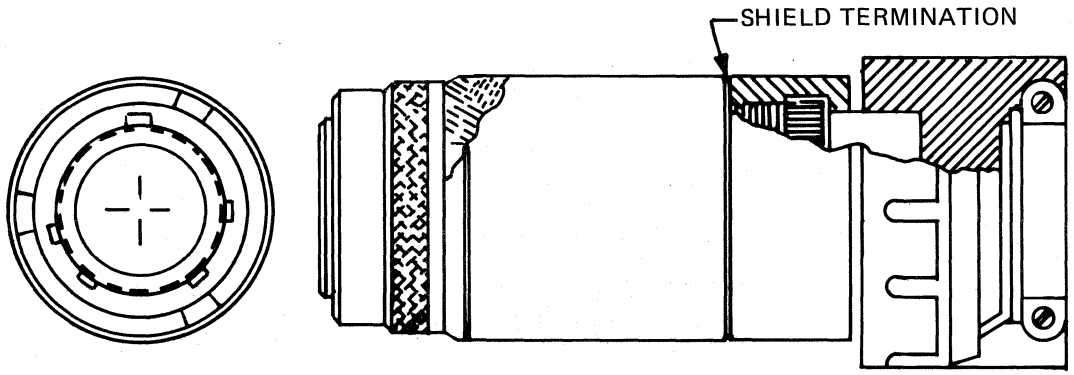


Figure 2-2. 1840 Modified Cabinet Power Wiring Schematic Diagram



POLARIZING POSITIONS				
POSITIONS	A	B	C	D
PLUG FOR J3 AND J5	105°	140°	215°	265°
PLUG FOR J2 AND J4	18°	149°	192°	259°



PLUG FOR J2 THROUGH J5

APPLICATION NOTES:

1. CONTACTS SHALL BE CRIMPED WITH THE DANIELS MH-780 HAND CRIMPING TOOL (DANIELS MANUFACTURING COMPANY, PONTIAC, MICHIGAN) OR ITS EQUIVALENT.
2. CONTACT INSERTION TOOL PER MS90459; CONTACT REMOVAL TOOL: PER MS90458.
3. FOR INFORMATION CONCERNING SPARE CONTACTS, REFER TO ASSOCIATED CONNECTOR LISTED IN PARTS LIST.

Figure 2-3. Plug Pin Assignment

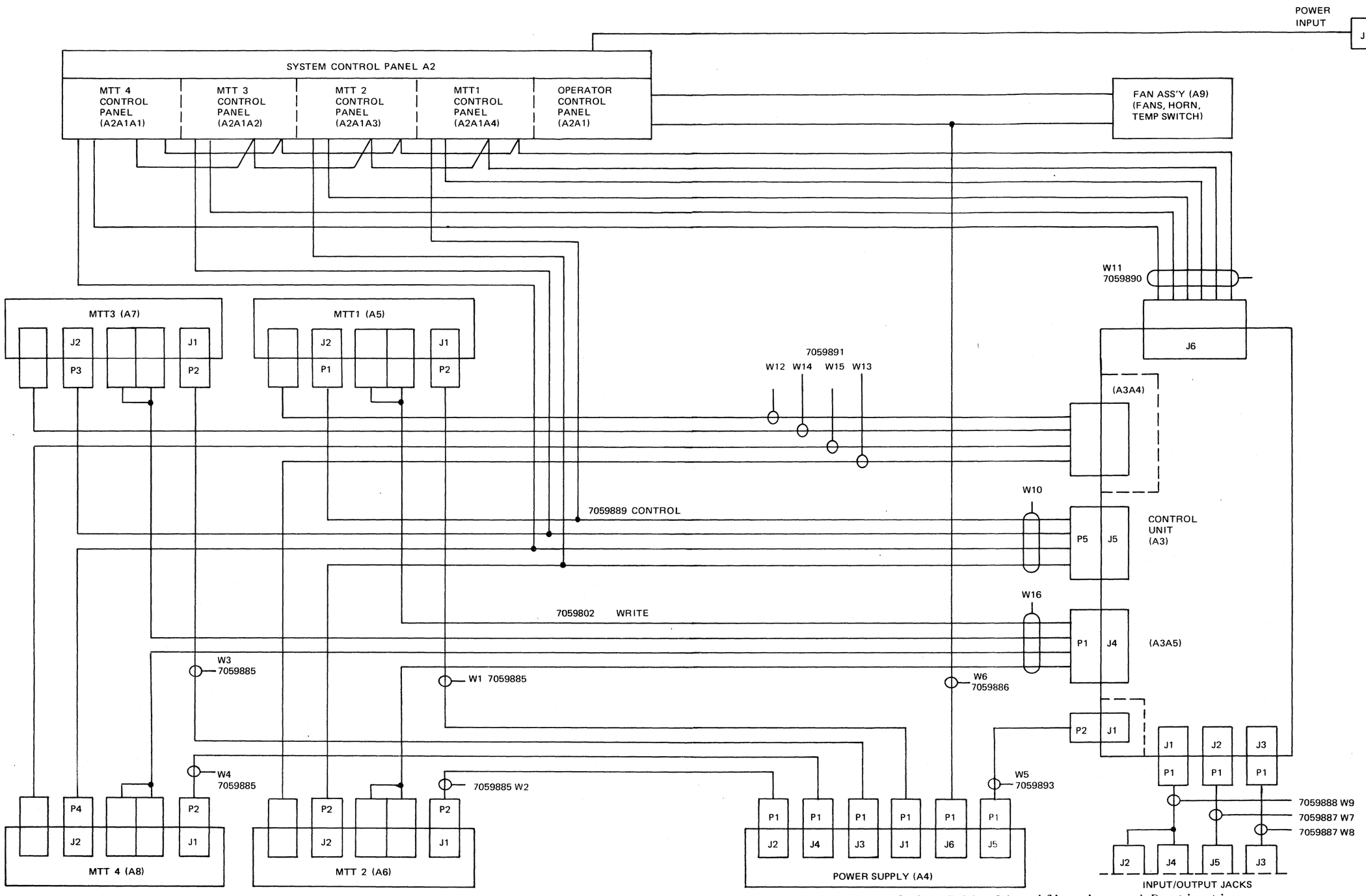
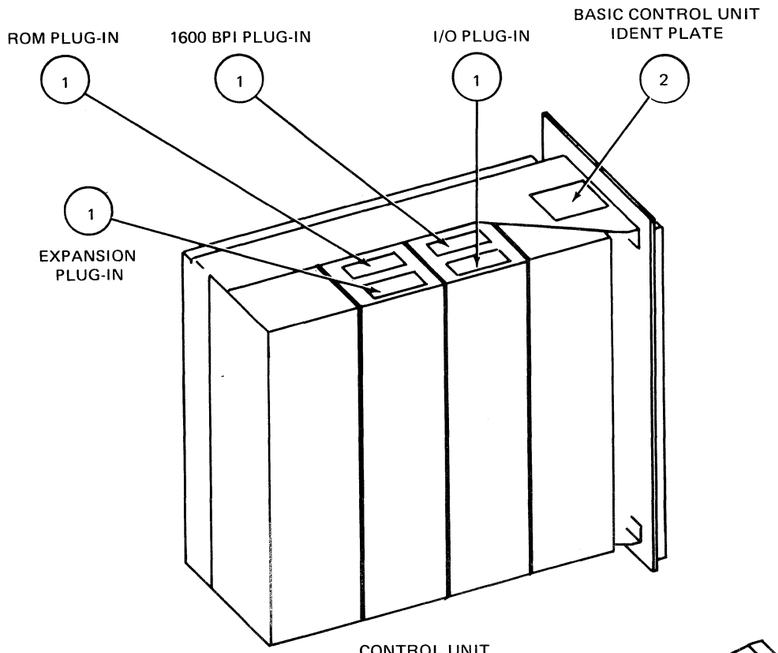
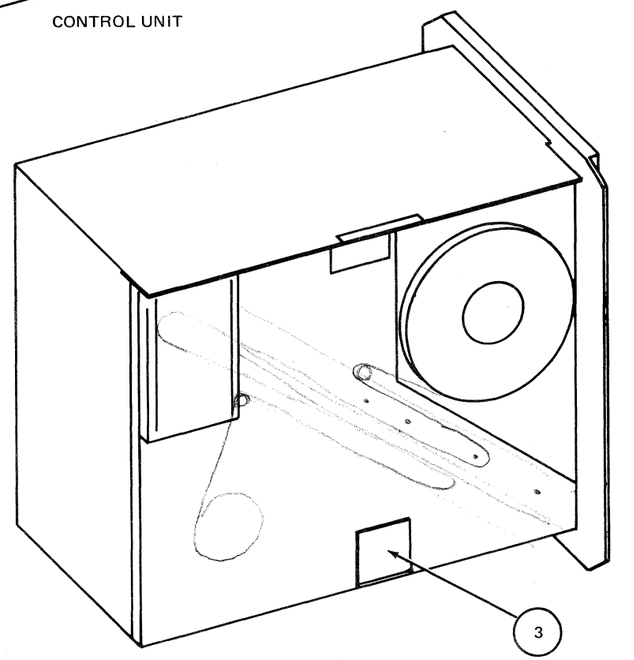


Figure 2-4. Cable Identification and Destination

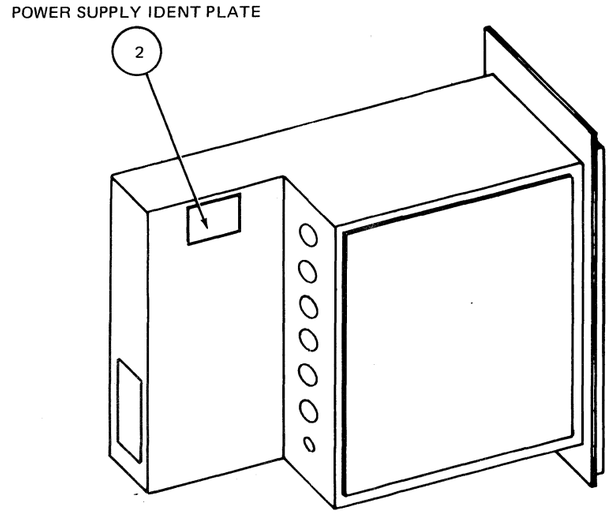


CONTROL UNIT

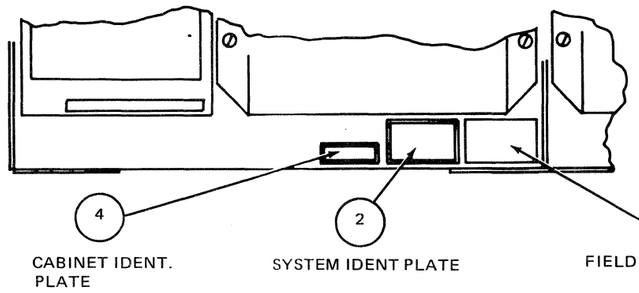


GROUP IDENT PLATE

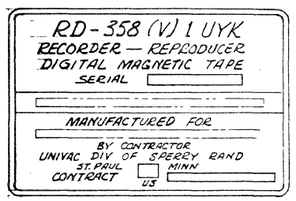
MAG TAPE TRANSPORT



POWER SUPPLY

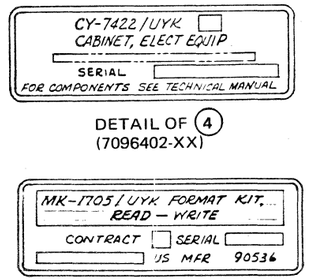


CABINET



TYPICAL DETAIL OF (2)
(7059974-XX)

DETAIL OF (3)
(V# 7903946-XX)



DETAIL OF (4)
(7096402-XX)

DETAIL OF (1)
(7120119-XX)

Figure 2-5. Nameplate Locations

TABLE 2-1. INPUT POWER CABLE CONNECTOR PIN ASSIGNMENTS

PIN	DESTINATION
A	Phase A
B	Phase B
C	Phase C
D	Neutral (When Used)

TABLE 2-2. POWER CABLE W1, W2, W3, and W4, POWER SUPPLY TO TAPE TRANSPORT (J1)

ORIGIN	DESTINATION	REMARKS
P01- A	P02- A	208 400Hz Ph A
P01- B	P02- B	208 400Hz Ph B
P01- C	P02- C	208 400Hz Ph C
P01- D	P02- D	208 400Hz Neut
P01- E	P02- E	75Vdc Pos
P01- H	P02- H	75Vdc Neg Ret
P01- F	P02- F	75Vdc Pos
P01- J	P02- J	75Vdc Neg Ret
P01- G	P02- G	75Vdc Pos
P01- K	P02- K	75Vdc Neg Ret
P01- L	P02- L	4KHz Ph A
P01- M	P02- M	4KHz Ph B
P01- N	P02- N	4KHz Return
P01- R	P02- R	Relay Line 1
P01- S	P02- S	Relay Line 2
P01- T	P02- T	Shield Grd

TABLE 2-3. POWER CABLE W5, POWER SUPPLY TO CU.

ORIGIN	DESTINATION	REMARKS
A04 P01- A	A03 P02- 1	115 400 Hz 1 Ph
A04 P01- B	A03 P02- 2	115 400Hz Ret
A04 P01- E	A03 P02- A1	75Vdc Pos
A04 P01- J	A03 P02- A2	75Vdc Ret
A04 P01- T	A03 P02- 3+2	Note 1 Chas Grd
A04 P01- U	A03 P02- 4	Out of Tol High
A04 P01- V	A03 P02- 5	Out of Tol Ret
A04 P01- W	A03 P02- 3+2	Tol Shld

TABLE 2-4. POWER CABLE S5, POWER SUPPLY TO SYSTEM CONTROL PANEL (A2) AND FAN ASS'Y (A9)

ORIGIN	DESTINATION	REMARKS
A04 P01- A	A02 TB 1-A05+2	400Hz Ph A
A04 P01- P	A02 TB 1-A05+2	400Hz Ph A
A04 P01- B	A02 TB 1-A06+2	400Hz Ph B
A04 P01- W	A02 TB 1-A06+2	400Hz Ph B
A04 P01- C	A02 TB 1-A07+2	400Hz Ph C
A04 P01- X	A02 TB 1-A07+2	400Hz Ph C
A04 P01- D	A02 TB 1-A04+2	400Hz Neutral
A04 P01- E	E- 5+2	XFMR Shield
A04 P01- G	A02 TB 1-A08	115 Aux Hot
A04 P01- H	A02 TB 1-A09+2	115 Aux Switch
A04 P01- J	A02 TB 1-A10	115 Aux Return
A04 P01- L	A09 TB 1-B01+2	115 400Hz Ph A
A04 P01- M	A09 TB 1-B02+2	115 400Hz Ph B
A04 P01- N	A09 TB 1-B03+2	115 400Hz Ph C
A04 P01- R	A09 TB 1-B09	HI Overtemp
A04 P01- S	A09 TB 1-B08	HI Overtemp Ret
A04 P01- T	E 5+2	CH & Shield Grd

TABLE 2-5. INPUT CABLE, W7 AND W8, BETWEEN CONTROL UNIT AND COMPUTER JACKS, PIN ASSIGNMENT

ORIGIN	DESTINATION	SIGNAL
P01-A01	J01- 48	Chassis Grd
P01-B01	J01- 74	Shield Grd
P01-D01	J01- 13	Data Bit 00
P01-C01	J01- 21	Data Bit 00 Ret
P01-D02	J01- 14	Data Bit 01
P01-C02	J01- 22	Data Bit 01 Ret
P01-D03	J01- 15	Data Bit 02
P01-C03	J01- 23	Data Bit 02 Ret
P01-D04	J01- 16	Data Bit 03
P01-C04	J01- 24	Data Bit 03 Ret
P01-D05	J01- 17	Data Bit 04
P01-C05	J01- 25	Data Bit 04 Ret
P01-D06	J01- 18	Data Bit 05
P01-C06	J01- 26	Data Bit 05 Ret
P01-D07	J01- 29	Data Bit 06
P01-C07	J01- 39	Data Bit 06 Ret
P01-D08	J01- 30	Data Bit 07
P01-C08	J01- 40	Data Bit 07 Ret
P01-D09	J01- 31	Data Bit 08
P01-C09	J01- 41	Data Bit 08 Ret
P01-D10	J01- 32	Data Bit 09
P01-C10	J01- 42	Data Bit 09 Ret
P01-D11	J01- 33	Data Bit 10
P01-C11	J01- 43	Data Bit 10 Ret
P01-D12	J01- 34	Data Bit 11
P01-C12	J01- 44	Data Bit 11 Ret
P01-G01	Jol- 35	Data Bit 12
P01-H01	J01- 45	Data Bit 12 Ret
P01-G02	J01- 36	Date Bit 13
P01-H02	J01- 46	Data Bit 13 Ret
P01-G03	J01- 37	Data Bit 14
P01-H03	J01- 47	Data Bit 14 Ret
P01-G04	J01- 49	Data Bit 15
P01-H04	J01- 58	Data Bit 15 Ret
P01-G05	J01- 50	Data Bit 16
P01-H05	J01- 59	Data Bit 16 Ret
P01-G06	J01- 51	Data Bit 17
P01-H06	J01- 60	Data Bit 17 Ret
P01-G07	J01- 52	Data Bit 18
P01-H07	J01- 61	Data Bit 18 Ret
P01-G08	J01- 53	Data Bit 19
P01-H08	J01- 62	Data Bit 19 Ret

TABLE 2-5. INPUT CABLE, W7 AND W8, BETWEEN CONTROL UNIT AND COMPUTER JACKS, PIN ASSIGNMENT (CONT)

ORIGIN	DESTINATION	SIGNAL
P01-G09	J01- 54	Data Bit 20
P01-H09	J01- 63	Data Bit 20 Ret
P01-G10	J01- 55	Data Bit 21
P01-H10	J01- 64	Data Bit 21 Ret
P01-G11	J01- 56	Data Bit 22
P01-H11	J01- 65	Data Bit 22 Ret
P01-G12	J01- 57	Data Bit 23
P01-H12	J01- 66	Data Bit 23 Ret
P01-J01	J01- 67	Data Bit 24
P01-K01	J01- 75	Data Bit 24 Ret
P01-J02	J01- 68	Data Bit 25
P01-K02	J01- 76	Data Bit 25 Ret
P01-J03	J01- 69	Data Bit 26
P01-K03	J01- 77	Data Bit 26 Ret
P01-J04	J01- 70	Data Bit 27
P01-K04	J01- 78	Data Bit 27 Ret
P01-J05	J01- 71	Data Bit 28
P01-K05	J01- 79	Data Bit 28 Ret
P01-J06	J01- 72	Data Bit 29
P01-K06	J01- 80	Data Bit 29 Ret
P01-J07	J01- 73	Data Bit 30
P01-K07	J01- 81	Data Bit 30 Ret
P01-J08	J01- 55	Data Bit 31
P01-K08	J01- 12	Data Bit 31 Ret
P01-J09	J01- 10	Data Bit 32
P01-K09	J01- 11	Data Bit 32 Ret
P01-J10	J01- 82	Data Bit 33
P01-K10	J01- 83	Data Bit 33 Ret
P01-J11	J01- 19	Data Bit 34
P01-K11	J01- 27	Data Bit 34 Ret
P01-J12	J01- 84	Data Bit 35
P01-K12	J01- 85	Data Bit 35 Ret
P01-B07	J01- 3	Ext Funct Ack
P01-A07	J01- 8	Ext Funct Ret
P01-B06	J01- 2	Out Data Req
P01-A06	J01- 7	Out Data Req Rt
P01-B05	J01- 1	Out Ack
P01-A05	J01- 6	Out Ack Ret
P01-B08	J01- 4	Ext Funct Req
P01-A08	J01- 9	Ext Funct Ret

TABLE 2-6. SIGNAL CABLE W9, COMPUTER INPUT (J2 AND J4)

ORIGIN	DESTINATION	REMARKS
P01-A01	J01- 48+2	Chassis Grd
J01- 48+2	J02- 48	Chassis Grd
P01-B01	J01- 74+2	Shield Grd
J01- 74+2	J02- 74	Shield Grd
P01-D01	J01- 13+2	Data Bit 00
P01-C01	J01- 21+2	Data Bit 00 Ret
J01- 13+2	J02- 13	Data Bit 00
J01- 21+2	J02- 21	Data Bit 00 Ret
P01-D02	J01- 14+2	Data Bit 01
P01-C02	J01- 22+2	Data Bit 01 Ret
J01- 14+2	J02- 14	Data Bit 01
J01- 22+2	J02- 22	Data Bit 01 Ret
P01-D03	J01- 15+2	Data Bit 02
P01-C03	J01- 23+2	Data Bit 02 Ret
J01- 15+2	J02- 15	Data Bit 02
J01- 23+2	J02- 23	Data Bit 02 Ret
P01-D04	J01- 16+2	Data Bit 03
P01-C04	J01- 24+2	Data Bit 03 Ret
J01- 16+2	J02- 16	Data Bit 03
J01- 24+2	J02- 24	Data Bit 03 Ret
P01-D05	J01- 17+2	Data Bit 04
P01-C05	J01- 25+2	Data Bit 04 Ret
J01- 17+2	J02- 17	Data Bit 04
J01- 25+2	J02- 25	Data Bit 04 Ret
P01-D06	J01- 18+2	Data Bit 05
P01-C06	J01- 26+2	Data Bit 05 Ret
J01- 18+2	J02- 18	Data Bit 05
J01- 26+2	J02- 26	Data Bit 05 Ret
P01-D07	J01- 29+2	Data Bit 06
P01-C07	J01- 39+2	Data Bit 06 Ret
J01- 29+2	J02- 29	Data Bit 06
J01- 39+2	J02- 39	Data Bit 06 Ret
P01-D08	J01- 30+2	Data Bit 07
P01-C08	J01- 40+2	Data Bit 07 Ret
J01- 30+2	J02- 30	Data Bit 07
J01- 40+2	J02- 40	Data Bit 07 Ret
P01-D09	J01- 31+2	Data Bit 08
P01-C09	J01- 41+2	Data Bit 08 Ret
J01- 31+2	J02- 31	Data Bit 08
J01- 41+2	J02- 41	Data Bit 08 Ret
P01-D10	J01- 32+2	Data Bit 09
P01-C10	J01- 42+2	Data Bit 09 Ret
J01- 32+2	J02- 32	Data Bit 09
J01- 42+2	J02- 42	Data Bit 09 Ret
P01-D11	J01- 33+2	Data Bit 10
P01-C11	J01- 43+2	Data Bit 10 Ret
J01- 33+2	J02- 33	Data Bit 10
J01- 43+2	J02- 43	Data Bit 10 Ret

TABLE 2-6. SIGNAL CABLE W9, COMPUTER INPUT (J2 AND J4) (CONT)

ORIGIN	DESTINATION	REMARKS
P01-D12	J01- 34+2	Data Bit 11
P01-C12	J01- 44+2	Data Bit 11 Ret
J01- 34+2	J02- 34	Data Bit 11
J01- 44+2	J02- 44	Data Bit 11 Ret
P01-G01	J01- 35+2	Data Bit 12
P01-H01	J01- 45+2	Data Bit 12 Ret
J01- 35+2	J02- 35	Data Bit 12
J01- 45+2	J02- 45	Data Bit 12 Ret
P01-G02	J01- 36	Data Bit 13
P01-H02	J01- 46	Data Bit 13 Ret
P01-B02	J02- 36	Data Bit 13
P01-A02	J02- 46	Data Bit 13 Ret
P01-G03	J01- 37+2	Data Bit 14
P01-H03	J01- 47+2	Data Bit 14 Ret
J01- 37+2	J02- 37	Data Bit 14
J01- 47+2	J02- 47	Data Bit 14 Ret
P01-G04	J01- 49+2	Data Bit 15
P01-H04	J01- 58+2	Data Bit 15 Ret
J01- 49+2	J02- 49	Data Bit 15
J01- 58+2	J02- 58	Data Bit 15 Ret
P01-G05	J01- 50+2	Data Bit 16
P01-H05	J01- 59+2	Data Bit 16 Ret
J01- 50+2	J02- 50	Data Bit 16
J01- 59+2	J02- 59	Data Bit 16 Ret
P01-G06	J01- 51+2	Data Bit 17
P01-H06	J01- 60+2	Data Bit 17 Ret
J02- 51	J01- 51+2	Data Bit 17
J02- 60	J01- 60+2	Data Bit 17 Ret
J01- 52+2	P01-G07	Data Bit 18
J01- 61+2	P01-H07	Data Bit 18 Ret
J02- 52	J01- 52+2	Data Bit 18
J02- 61	J01- 61+2	Data Bit 18 Ret
P01-G08	J01- 53+2	Data Bit 19
P01-H08	J01- 62+2	Data Bit 19 Ret
J01- 53+2	J02- 53	Data Bit 19
J01- 62+2	J02- 62	Data Bit 19 Ret
P01-G09	J01- 54+2	Data Bit 20
P01-H09	J01- 63+2	Data Bit 20 Ret
J01- 54+2	J02- 54	Data Bit 20
J01- 63+2	J02- 63	Data Bit 20 Ret
P01-G10	J01- 55+2	Data Bit 21
P01-H10	J01- 64+2	Data Bit 21 Ret
J01- 55+2	J02- 55	Data Bit 21
J01- 64+2	J02- 64	Data Bit 21 Ret
P01-G11	J01- 56+2	Data Bit 22
P01-H11	J01- 65+2	Data Bit 22 Ret
J01- 56+2	H02- 56	Data Bit 22
J01- 65+2	J02- 65	Data Bit 22 Ret
P01-G12	J01- 57+2	Data Bit 23

TABLE 2-6. SIGNAL CABLE W9, COMPUTER INPUT (J2 AND J4) (CONT)

ORIGIN	DESTINATION	REMARKS
P01-H12	J01- 66+2	Data Bit 23 Ret
J01- 57+2	J02- 57	Data Bit 23
J01- 66+2	J02- 66	Data Bit 23 Ret
P01-J01	J01- 67+2	Data Bit 24
P01-K01	J01- 75+2	Data Bit 24 Ret
J01- 67+2	J02- 67	Data Bit 24
J01- 75+2	J02- 75	Data Bit 24 Ret
P01-J02	J01- 68+2	Data Bit 25
P01-K02	J01- 76+2	Data Bit 25 Ret
J01- 68+2	J02- 68	Data Bit 25
J01- 76+2	J02- 76	Data Bit 25 Ret
P01-J03	J01- 69+2	Data Bit 26
P01-K03	J01- 77+2	Data Bit 26 Ret
J01- 69+2	J02- 69	Data Bit 26
J01- 77+2	J02- 77	Data Bit 26 Ret
P01-J04	J01- 70+2	Data Bit 27
P01-K04	J01- 78+2	Data Bit 27 Ret
J01- 70+2	J02- 70	Data Bit 27
J01- 78+2	J02- 78	Data Bit 27 Ret
P01-J05	J01- 71+2	Data Bit 28
P01-K05	J01- 79+2	Data Bit 28 Ret
J01- 71+2	J02- 71	Data Bit 28
J01- 79+2	J02- 79	Data Bit 28 Ret
P01-J06	J01- 72+2	Data Bit 29
P01-K06	J01- 80+2	Data Bit 29 Ret
J01- 72+2	J02- 72	Data Bit 29
J01- 80+2	J02- 80	Data Bit 29 Ret
P01-J07	J01- 73+2	Data Bit 30
P01-K07	J01- 81+2	Data Bit 30 Ret
J01- 73+2	J02- 73	Data Bit 30
J01- 81+2	J02- 81	Data Bit 30 Ret
P01-J08	J01- 5+2	Data Bit 31
P01-K08	J01- 12+2	Data Bit 31 Ret
J01- 5+2	J02- 5	Data Bit 31
J01- 12+2	J02- 12	Data Bit 31 Ret
P01-J09	J01- 10+2	Data Bit 32
P01-K09	J01- 11+2	Data Bit 32 Ret
J01- 10+2	J02- 10	Data Bit 32
J01- 11+2	J02- 11	Data Bit 32 Ret
P01-J10	J01- 82+2	Data Bit 33
P01-K10	J01- 83+2	Data Bit 33 Ret
J01- 82+2	J02- 82	Data Bit 33
J01- 83+2	J02- 83	Data Bit 33 Ret
P01-J11	J01- 19+2	Data Bit 34
P01-K11	J01- 27+2	Data Bit 34 Ret
J01- 19+2	J02- 19	Data Bit 34
J01- 27+2	J02- 27	Data Bit 34 Ret
P01-J12	J01- 84+2	Data Bit 35

TABLE 2-6. SIGNAL CABLE W9, COMPUTER INPUT (J2 AND J4) (CONT)

ORIGIN	DESTINATION	REMARKS
P01-K12	J01- 85+2	Data Bit 35 Ret
J01- 84+2	J02- 84	Data Bit 35
J01- 85+2	J02- 85	Data Bit 35 Ret
P01-B11	J02- 3	Ext Int Req
P01-A11	J02- 8	Ext Int Req Ret
P01-B10	J02- 2	In Ack
P01-A10	J02- 7	In Ack Ret
P01-B09	J02- 1	In Data Req
P01-A09	J02- 6	In Data Req Ret
P01-B07	J01- 3	Ext Int Req
P01-A07	J01- 8	Ext Int Req Ret
P01-B06	J01- 2	In Ack
P01-A06	J01- 7	In Ack Ret
P01-B05	J01- 1	In Data Req
P01-A05	J01- 6	In Data Req Ret

TABLE 2-7. CONTROL CABLE W10

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P01- /D	A01 S 16- 1	Stop Load SW
P01- /F	A01 S 16- 2	Stop Load SW RT
P01- /H	A01 DS 44- 1	Load SW
P01- /K	A01 DS 44- 3	Load SW Ret
P01- /J	A01 DS 44- 4	Load Ind
P01- /M	A01 A 4-E23+2	Load Ind Ret
P01- /N	A01 DS 48- 1	Unload SW
P01- /R	A01 DS 48- 3	Unload Ret
P01- /P	A01 DS 48- 4	Unload Ind
P01- /S	A01 A 4-E21+3	Unload Ind Ret
P01- /X	A01 S13B- 1	Auto Enable
P01- /Z	A01 S13B- 10	Auto Enable Ret
P01- /Y	A01 DS 40- 2+2	Plus 5Vdc TT
P01- DD	A01 GND-	Shield Grd
P02- /D	A01 S 12- 1	Stop Load SW
P02- /F	A01 S 12- 2	Stop Load SW RT
P02- /H	A01 DS 32- 1	Load SW
P02- /K	A01 DS 32- 3	Load SW Ret
P02- /J	A01 DS 32- 4	Load Ind
P02- /M	A01 A 3-E23+2	Load Ind Ret
P02- /N	A01 DS 36- 1	Unload SW
P02- /R	A01 DS 36- 3	Unload SW Ret
P02- /P	A01 DS 36- 4	Unload Ind
P02- /S	A01 A 3-E21+3	Unload Ind Ret
P02- /X	A01 S 9B- 1	Auto Enable
P02- /Z	A01 S 9B- 10	Auto Enable Ret
P02- /Y	A01 DS 28- 2+2	Plus 5Vdc TT
P02- DD	A01 GRD-	Shield Grd

TABLE 2-7. CONTROL CABLE W10 (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P03- /D	A01 S 8- 1	Stop Load SW
P03- /F	A01 S 8- 2	Stop Load SW RT
P03- /H	A01 DS 20- 1	Load SW
P03- /K	A01 DS 20- 3	Load SW Ret
P03- /J	A01 DS 20- 4	Load Ind
P03- /M	A01 A 2-E23+2	Load Ind Ret
P03- /N	A01 DS 24- 1	Unload SW
P03- /R	A01 DS 24- 3	Unload SW Ret
P03- /P	A01 DS 24- 4	Unload Ind
P03- /S	A01 A 2-E21+3	Unload Ind Ret
P03- /X	A01 S 58- 1	Auto Enable
P03- /Z	A01 S 58- 10	Auto Enable Ret
P03- /Y	A01 DS 16- 2+2	Plus 5 Vdc TT
P03- DD	A01 GRD-	Shield Grd
P04- /D	A01 S 4- 1	Stop Load SW
P04- /F	A01 S 4- 2	Stop Load SW RT
P04- /H	A01 DS 8- 1	Load SW
P04- /K	A01 DS 8- 3	Load SW Ret
P04- /J	A01 DS 8- 4	Load Ind
P04- /M	A01 A 1-E23+2	Load Ind Ret
P04- /N	A01 DS 12- 1	Unload SW
P04- /R	A01 DS 12- 3	Unload SW Ret
P04- /P	A01 DS 12- 4	Unload Ind
P04- /S	A01 A 1-E21+3	Unload Ind Ret
P04- /X	A01 S 1B- 1	Auto Enable
P04- /Z	A01 S 1B- 10	Auto Enable Ret
P04- /Y	A01 DS 4- 2+2	Plus 5Vdc TT
P04- DD	A01 GRD-	Shield Grd
P05-A01	P01- A	Reverse
P05-B01	P01- C	Reverse Ret
P05-C01	P01- B	Forward
P05-D01	P01- D	Forward Ret
P05-E01	P01- E	Fast
P05-F01	P01- H	Fast Ret
P05-G01	P01- F	BOT
P05-H01	P01- J	BOT Ret
P05-J01	P01- K	EOT
P05-K01	P01- M	EOT Ret
P05-A02	P01- L	Ready
P05-B02	P01- N	Ready Ret
P05-C02	P01- P	Low Tape
P05-D02	P01- S	Low Tape Ret
P05-E02	P01- R	Write Enable
P05-F02	P01- T	Write Enable RT
P05-G02	P01- U	Capstan Zero
P05-H02	P01- W	Capstan Zero RT

TABLE 2-7. CONTROL CABLE W10 (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P05-J02	P01- V	Write
P05-K02	P01- X	Write RT
P05-K03	P01- DD	Chassis Grd
P05-A04	P02- A	Reverse
P05-B04	P02- C	Reverse Ret
P05-C04	P02- B	Forward
P05-D04	P02- D	Forward Ret
P05-E04	P02- E	Fast
P05-F04	P02- H	Fast Ret
P05-G04	P02- F	BOT
P05-H04	P02- J	BOT Ret
P05-J04	P02- K	EOT
P05-K04	P02- M	EOT Ret
P05-A05	P02- L	Ready
P05-B05	P02- N	Ready Ret
P05-C05	P02- P	Low Tape
P05-D05	P02- S	Low Tape Ret
P05-E05	P02- R	Write Enable
P05-F05	P02- T	Write Enable RT
P05-G05	P02- U	Capstan Zero
P05-H05	P02- W	Capstan Zero RT
P05-J05	P02- V	Write
P05-K05	P02- X	Write Ret
P05-K06	P02- DD	Chassis Grd
P05-A07	P03- A	Reverse
P05-B07	P03- C	Reverse Ret
P05-C07	P03- B	Forward
P05-D07	P03- D	Forward Ret
P05-E07	P03- E	Fast
P05-F07	P03- H	Fast Ret
P05-G07	P03- F	BOT
P05-H07	P03- J	BOT Ret
P05-J07	P03- K	EOT
P05-K07	P03- M	EOT Ret
P05-A08	P03- L	Ready
P05-B08	P03- N	Ready Ret
P05-C08	P03- P	Low Tape
P05-D08	P03- S	Low Tape
P05-E08	P03- R	Write Enable
P05-F08	P03- T	Write Enable RT
P05-G08	P03- U	Capstan Zero
P05-H08	P03- W	Capstan Zero RT
P05-J08	P03- V	Write
P05-K08	P03- X	Write Ret
P05-K09	P03- DD	Chassis Grd
P05-K10	P04- A	Reverse

TABLE 2-7. CONTROL CABLE W10 (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P05-B10	P04- C	Reverse Ret
P05-C10	P04- B	Forward
P05-D10	P04- D	Forward Ret
P05-E10	P04- E	Fast
P05-F10	P04- H	Fast Ret
P05-G10	P04- F	BOT
P05-H10	P04- J	BOT Ret
P05-J10	P04- K	EOT
P05-K10	P04- M	EOT Ret
P05-A11	P04- L	Ready
P05-B11	P04- N	Ready Ret
P05-C11	P04- P	Low Tape
P05-D11	P04- S	Low Tape Ret
P05-E11	P04- R	Write Enable
P05-F11	P04- T	Write Enable RT
P05-G11	P04- U	Capstan Zero
P05-H11	P04- W	Capstan Zero RT
P05-J11	P04- V	Write
P05-K11	P04- X	Write Ret
P05-K12	P04- DD	Chassis Grd

TABLE 2-8. CONTROL CABLE W11, CU TO SYSTEM CONTROL PANEL

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P01-A01	A01 A 4-E29+2	Forward TTl
P01-B01	A01 A 4-E19+3	Forward Ret
P01-C01	A01 A 4-E07+2	Reverse
P01-D01	A01 A 4-E18+3	Reverse Ret
P01-E01	A01 A 4-E08+2	Rewind
P01-F01	A01 A 4-E19+3	Rewind Ret
P01-G01	A01 A 4-E28+2	Stop Switch
P01-H01	A01 A 4-E15+3	Stop Switch Ret
P01-J01	A01 A 4-E27+2	BOT SW
P01-K01	A01 A 4-E17+3	BOT SW Ret
P01-A02	A01 A 4-E26+2	EOT SW
P01-B02	A01 A 4-E16+3	EOT SW Ret
P01-C02	A01 A 4-E13+2	Manual
P01-D02	A01 A 4-E04+2	Ready
P01-E02	A01 A 4-E25+2	Select
P01-F02	A01 A 4-E15+3	Select Ret
P01-G02	A01 A 4-E06+2	BOT Ind
P01-H02	A01 A 4-E05+2	EOT Ind
P01-J02	A01 A 4-E24+2	Write Enable
P01-K02	A01 A 4-E14+3	Write Enable RT

TABLE 2-8. CONTROL CABLE W11, CU TO SYSTEM CONTROL PANEL (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P01-A03	A01 A 3-E29+2	Forward TT2
P01-B03	A01 A 3-E19+3	Forward Ret
P01-C03	A01 A 3-E07+2	Reverse
P01-D03	A01 A 3-E18+3	Reverse Ret
P01-E03	A01 A 3-E08+2	Rewind
P01-F03	A01 A 3-E19+3	Rewind Ret
P01-G03	A01 A 3-E28+2	Stop
P01-H03	A01 A 3-E15+3	Stop Ret
P01-J03	A01 A 3-E27+2	BOT SW
P01-K03	A01 A 3-E17+3	BOT SW Ret
P01-A04	A01 A 3-E26+2	EOT SW
P01-B04	A01 A 3-E16+3	EOT SW Ret
P01-C04	A01 A 3-E13+2	Manual
P01-D04	A01 A 3-E04+2	Ready
P01-E04	A01 A 3-E25+2	Select
P01-F04	A01 A 3-E15+3	Select Ret
P01-G04	A01 A 3-E06+2	BOT Ind
P01-H04	A01 A 3-E05+2	EOT Ind
P01-J04	A01 A 3-E24+2	Write Enable
P01-K04	A01 A 3-E14+3	Write Enable RT
P01-A05	A01 A 2-E29+2	Forward TT3
P01-B05	A01 A 2-E19+3	Forward Ret
P01-C05	A01 A 2-E07+2	Reverse
P01-D05	A01 A 2-E18+3	Reverse Ret
P01-E05	A01 A 2-E08+2	Rewind
P01-F05	A01 A 2-E19+3	Rewind Ret
P01-G05	A01 A 2-E28+2	Stop
P01-H05	A01 A 2-E15+3	Stop Ret
P01-J05	A01 A 2-E27+2	BOT SW
P01-K05	A01 A 2-E17+3	BOT SW Ret
P01-A06	A01 A 2-E26+2	EOT SW
P01-B06	A01 A 2-E16+3	EOT SW Ret
P01-C06	A01 A 2-E13+2	Manual
P01-D06	A01 A 2-E04+2	Ready
P01-E06	A01 A 2-E25+2	Select
P01-F06	A01 A 2-E15+3	Select Ret
P01-G06	A01 A 2-E06+2	BOT Ind
P01-H06	A01 A 2-E05+2	EOT Ind
P01-J06	A01 A 2-E24+2	Write Enable
P01-K06	A01 A 2-E14+3	Write Enable RT
P01-A07	A01 A 1-E29+2	Forward TT4
P01-B07	A01 A 1-E19+3	Forward Ret
P01-C07	A01 A 1-E07+2	Reverse
P01-D07	A01 A 1-E18+3	Reverse Ret
P01-E07	A01 A 1-E07+2	Rewind

TABLE 2-8. CONTROL CABLE W11, CU TO SYSTEM CONTROL PANEL (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P01-F07	A01 A 1-E19+3	Rewind Ret
P01-G07	A01 A 1-E28+2	Stop
P01-H07	A01 A 1-E15+3	Stop Ret
P01-J07	A01 A 1-E27+3	BOT SW
P01-K07	A01 A 1-E17+3	BOT SW Ret
P01-A08	A01 A 1-E26+2	EOT SW
P01-B08	A01 A 1-E16+3	EOT SW Ret
P01-C08	A01 A 1-E13+2	Manual
P01-D08	A01 A 1-E04+2	Ready
P01-E08	A01 A 1-E25+2	Select
P01-F08	A01 A 1-E15+3	Select Ret
P01-G08	A01 A 1-E06+2	BOT Ind
P01-H08	A01 A 1-E05+2	EOT Ind
P01-J08	A01 A 1-E24+2	Write Enable
P01-K08	A01 A 1-E14+3	Write Enable RT
P01-A09	A01 S 14- 1+2	Address 1
P01-B09	A01 S 14- 2+2	Address 2
P01-C09	A01 S 14- 3+2	Address 3
P01-D09	A01 S 14- 4+2	Address 4
P01-E09	A01 S 14- 5+2	Address 5
P01-F09	A01 S 14- 6+2	Address 6
P01-G09	A01 S 14- 7+2	Address 7
P01-H09	A01 S 14- 8+2	Address 8
P01-J09	A01 S 14- 9+2	Address 9
P01-K09	A01 S 14- 10+2	Address 10
P01-A10	A01 S 14- 11+2	Address 11
P01-B10	A01 S 14- 12+2	Address 12
P01-C10	A01 S 14- 13+2	Address 13
P01-D10	A01 S 14- 14+2	Address 14
P01-E10	A01 S 14- 15+2	Address 15
P01-F10	A01 S 14- 16+2	Address 16
P01-G10	A01 S 14-COM	Add Wiper TT1
P01-H10	A01 S 10-COM	Add Wiper TT2
P01-J10	A01 S 6-COM	Add Wiper TT3
P01-K10	A01 S 2-COM	Add Wiper TT4
P01-A11	A01 DS 42- 2+3	Plus 5 Vdc
P01-B11	A01 DS 39- 5+3	Plus 24 Vdc
P01-C11	A01 DS 39- 2+3	Plus 24 Vdc Ret
P01-D11	A01 S 17- 1	Mode SW Normal
P01-E11	A01 S 17- 2	Mode SW 1240
P01-F11	A01 S 17- 3	Off Line 1
P01-G11	A01 S 17- 4	Off Line 2
P01-H11	A01 S 17- 5	Off Line 3
P01-J11	A01 S 17- 10	Mode SW Wiper
P01-K11	A01 S 17- 10	Mode SW Wiper
P01-A12	E 05- +3	Shield Grd

TABLE 2-9. DATA CABLE W12, W13, W14, W15 TAPE TRANSPORT TO CU (READ)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
E 2-	P 2- A	
E 3-	P 1- C	
E 1-	P 1-	No Term at P1
E 5-	P 1- D	
E 6-	P 1- F	
E 4-	P 1-	No Term at P1
E 8-	P 1- H	
E 9-	P 1- K	
E 7-	P 1-	No Term at P1
E 11-	P 1- L	
E 12-	P 1- N	
E 10-	P 1-	No Term at P1
E 14-	P 1- P	
E 14-	P 1- S	
E 13-	P 1-	No Term at P1
E 17-	P 1- T	
E 18-	P 1- V	
E 16-	P 1-	No Term at P1
E 20	P 1- W	
E 21-	P 1- Y	
E 19-	P 1-	No Term at P1
E 23-	P 1- Z	
E 24-	P 1- /B	
E 22-	P 1-	No Term at P1
E 26-	P 1- /C	
E 27-	P 1- /E	
E 25-	P 1-	No Term at P1
E 29-	P 2- A	
E 30-	P 2- B	
E 28-	P 2- C	TW Pair Shield
E 32-	P 2- D	
E 33-	P 2- E	
E 31-	P 2- F	TW Pair Shield
E 35-	P 2- G	
E 36-	P 2- H	
E 34-	P 2- J	TW Pair Shield
E 38-	P 2- K	
E 39-	P 2- L	
E 37-	P 2- M	TW Pair Shield
E 41-	P 2- N	
E 42-	P 2- P	
E 40-	P 2- R	TW Pair Shield
E 44-	P 2- S	
E 45	P 2- T	

TABLE 2-9. DATA CABLE W12, W13, W14, W15 TAPE TRANSPORT TO CU (READ) (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
E 43-	P 2- U	TW Pair Shield
E 47-	P 2- V	
E 48-	P 2- W	
E 46-	P 2- X	TW Pair Shield
E 50-	P 2- Y	
E 51-	P 2- Z	
E 49-	P 2- /A	TW Pair Shield
E 53-	P 2- /B	
E 54-	P 2- /C	
E 52-	P 2- /D	TW Pair Shield
E 55-	P 2- /K	+6V
E 56-	P 2- /M	Analog Ground
E 57-	P 2- /Q	-6V
E 58-	P 1-	No Term at P1
E 59-	P 2- /R	Outer Shield

TABLE 2-10. DATA CABLE W16, CU TO TAPE TRANSPORTS 1-4 (WRITE)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P01-A01	A05 -	Shield Note 1
P01-A02	A05 P03- A	Erase Pos
P01-A03	A05 P03- E	Erase Neg
P01-B01	A05 P02- C	Track 00 0
P01-B02	A05 P02- B	CT
P01-B03	A05 P02- A	1
P01-C01	A05 P02- F	Track 01 0
P01-C02	A05 P02- E	CT
P01-C03	A05 P02- D	1
P01-D01	A05 P02- K	Track 02 0
P01-D02	A05 P02- J	CT
P01-D03	A05 P02- H	1
P01-E01	A05 P01- N	Track 03 0
P01-E02	A05 P02- M	CT
P01-E03	A05 P02- L	1
P01-F01	A05 P01- S	Track 04 0
P01-F02	A05 P02- R	CT
P01-F03	A05 P02- P	1
P01-G01	A05 P02- V	Track 05 0
P01-G02	A05 P02- U	CT
P01-G03	A05 P02- T	1
P01-H01	A05 P02- Y	Track 06 0
P01-H02	A05 P02- X	CT
P01-H03	A05 P01- W	1
P01-J01	A05 P02- /B	Track 07 0
P01-J02	A05 P02- /A	CT

TABLE 2-10. DATA CABLE W16, CU TO TAPE TRANSPORTS 1-4 (WRITE) (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P01-J03	A05 P02- Z	Track 07 1
P01-K01	A05 P02- /E	Track 08 0
P01-K02	A05 P02- /D	CT
P01-K03	A05 P02- /C	1
P01-A04	A06 -	Shield Note 2
P01-A05	A06 P05- A	Erase Pos
P01-A06	A06 P05- E	Erase Neg
P01-B04	A06 P04- C	Track 00 0
P01-B05	A06 P04- B	CT
P01-B06	A06 P04- A	1
P01-C04	A06 P04- F	Track 01 0
P01-C05	A06 P04- E	CT
P01-C06	A06 P04- D	1
P01-D04	A06 P04- K	Track 02 0
P01-D05	A06 P04- J	CT
P01-D06	A06 P04- H	1
P01-E04	A06 P04- N	Track 03 0
P01-E05	A06 P04- M	CT
P01-E06	A06 P04- L	1
P01-F04	A06 P04- S	Track 04 0
P01-F05	A06 P04- R	CT
P01-F06	A06 P04- P	1
P01-G04	A06 P04- V	Track 05 0
P01-G05	A06 P04- U	CT
P01-G06	A06 P04- T	1
P01-H04	A06 P04- Y	Track 06 0
P01-H05	A06 P04- X	CT
P01-H06	A06 P04- W	1
P01-J04	A06 P04- /B	Track 07 0
P01-J05	A06 P04- /A	CT
P01-J06	A06 P04- Z	1
P01-K04	A06 P04- /E	Track 08 0
P01-K05	A06 P04- /D	CT
P01-K06	A06 P04- /C	1
P01-A07	A07 -	Shield Note 3
P01-A08	A07 P07- A	Erase Pos
P01-A09	A07 P07- E	Erase Neg
P01-B07	A07 P06- C	Track 00 0
P01-B08	A07 P06- B	CT
P01-B09	A07 P06- A	1
P01-C07	A07 P06- F	Track 01 0
P01-C08	A07 P06- E	CT
P01-C09	A07 P06- D	1
P01-D07	A07 P06- K	Track 02 0
P01-D08	A07 P06- J	CT
P01-D09	A07 P06- H	1

TABLE 2-10. DATA CABLE W16, CU TO TAPE TRANSPORTS 1-4 (WRITE) (CONT)

ORIGIN TERMINAL	DESTINATION TERMINAL	REMARKS
P01-E07	A07 P06- N	Track 03 0
P01-E08	A07 P06- M	CT
P01-E09	A07 P06- L	1
P01-F07	A07 P06- S	Track 04 0
P01-F08	A07 P06- R	CT
P01-F09	A07 P06- P	1
P01-G07	A07 P06- V	Track 05 0
P01-G08	A07 P06- U	CT
P01-G09	A07 P06- T	1
P01-H07	A07 P06- Y	Track 06 0
P01-H08	A07 P06- X	CT
P01-H09	A07 P06- W	1
P01-J07	A07 P06- /B	Track 07 0
P01-J08	A07 P06- /A	CT
P01-J09	A07 P06- Z	1
P01-K07	A07 P06- /E	Track 08 0
P01-K08	A07 P06- /D	CT
P01-K09	A07 P06- /C	1
P01-A10	A08 -	Shield Note 4
P01-A11	A08 P09- A	Erase Pos
P01-A12	A08 P09- E	Erase Neg
P01-B10	A08 P08- C	Track 00 0
P01-B11	A08 P08- B	CT
P01-B12	A08 P08- A	1
P01-C10	A08 P08- F	Track 01 0
P01-C11	A08 P08- E	CT
P01-C12	A08 P08- D	1
P01-D10	A08 P08- K	Track 02 0
P01-D11	A08 P08- J	CT
P01-D12	A08 P08- H	1
P01-E10	A08 P08- N	Track 03 0
P01-E11	A08 P08- M	CT
P01-E12	A08 P08- L	1
P01-F10	A08 P08- S	Track 04 0
P01-F11	A08 P08- R	CT
P01-F12	A08 P08- P	1
P01-G10	A08 P08- V	Track 05 0
P01-G11	A08 P08- U	CT
P01-G12	A08 P08- T	1
P01-H10	A08 P08- Y	Track 06 0
P01-H11	A08 P08- X	CT
P01-H12	A08 P08- W	1
P01-J10	A08 P08- /B	Track 07 0
P01-J11	A08 P08- /A	CT
P01-J12	A08 P08- Z	1
P01-K10	A08 P08- /E	Track 08 0
P01-K11	A08 P08- /D	CT

TABLE 2-10. DATA CABLE W16, CU TO TAPE TRANSPORTS 1-4 (WRITE) (CONT)

ORIGINAL TERMINAL	DESTINATION TERMINAL	REMARKS
P01-K12	A08 P08- /C	Track 08 1
-	A05 P02-	Shield
-	A06 P04-	Shield
-	A07 P06-	Shield
-	A08 P08-	Shield

SECTION 3

OPERATION

3-1. GENERAL OPERATING CHARACTERISTICS.

The MTS provides auxiliary data storage for a computer. Under computer control, the MTS will perform various functions which consist, basically, of read, write, search, space file and rewind operations. Read and write density capabilities of the MTS are: 200 and 556 frames per inch in the 1240 mode; 200,556, and 800 frames per inch in the 1540 mode; and 200, 556, 800, and 1600 frames per inch in the 9-track mode. All reading and writing by the MTS uses the NRZI technique except for 9-track, 1600 frames per inch, which uses the phase encoded (PE) technique. Tape speed for read, write and search operations is 120 inches per second. Rewind is performed at 200 inches per second except for the last 100 feet of tape where the speed is reduced to 120 inches per second with an automatic stop at the load point. An automatic read of the first record after rewind is a programmer option.

The computer directs the MTS operations by means of an external function word. When the function code specifies a write operation, the MTS receives computer-sized binary words, divides each word into characters, adds a lateral parity to each character and transmits the characters, in sequence, to the MTT, where they are recorded in frames on magnetic tape. In 7-track operation, the computer word size may be 18- to 36-bit binary words, the characters may be 6-bit (bioctal) or 3-bit (octal) and the frame size is 7 bits including parity. In 9-track operation, the computer word size may be 16- to 36-bit binary words, the characters are 8-bit bytes and the frame size is 9 bits including parity. No redundant recording may be performed in the 9-track mode. A write operation is performed with tape travel in the forward direction only.

When the function word code specifies a read operation, the MTS retrieves the recorded characters from tape, reads and deletes the lateral parity bit from each character, reassembles the data characters into their original computer-word form, and transmits the words to the computer. A read operation may be performed with tape travel in either direction.

If the computer directs that a search operation be performed, the function word code specifies a search operation and the computer supplies a search key to the MTS. This key is an identifier word which is compared with the first word of a data record to locate a particular record. When the MTS receives the search key, a character by character comparison with the first word of each record is made until a find occurs. The MTS then performs a normal read of the find record and transmits the data to the computer. If no find occurs on a reel of tape, the MTS notifies the computer that beginning-of-tape (BOT) or end-of-tape (EOT) has been reached.

In a space file operation, the MTT moves tape under direction of the CU until a tape mark is detected. Tape motion is then stopped, with the read head at the interrecord gap following the tape mark.

For maintenance and testing purposes, the MTS can be operated off-line, using the maintenance panel to simulate normal computer functions. The maintenance panel pushbutton/indicators can be used to generate all operational commands and to monitor the results of the operations.

For a detailed discussion of the MTT functions during an operation, refer to Univac technical manual PX 7984.

3-2. CONTROLS AND INDICATORS.

a. SYSTEM CONTROL PANEL. - The system control panel (figure 3-1) contains the primary power controls and indicators and tape transport manual controls and indicators (one set per transport). The controls and indicators functions are described in table 3-1.

b. MAINTENANCE PANEL. - The maintenance panel (figure 3-2) contains the controls and indicators for manual off-line operation and testing of the MTS. The controls and indicators functions are described in table 3-2.

c. DC POWER CONTROL. - The dc power to the individual units of the MTS is controlled by circuit breakers on the power supply (figure 3-3). Operating a circuit breaker to the ON position, applies dc power to the associated unit. Operating a circuit breaker to the OFF position, removes all dc power from the associated unit.

3-3. PREOPERATIONAL CHECKS.

Perform the following preoperational checks before energizing the MTS.

STEP 1. Check that power switches on system control panel (figure 3-1) and power supply circuit breakers are set to OFF.

STEP 2. Visually check MTS cables and connectors to ensure all connectors are secure.

STEP 3. Check that a write enable ring is installed on tape supply reel for each transport where writing will be performed (figure 3-4).

3-4. WRITE ENABLE RING.

If a write operation is to be performed, a write enable ring must be installed on the tape supply reel, as shown in figure 3-4. A write operation cannot be performed unless the ring is installed. Read or other nonwrite operations can be performed with the ring either on or off, but the ring should be removed for such operations to prevent accidental erasing and/or writing on the tape.

The write enable ring is an industry-standard item, and one is usually included with each tape reel purchased.

3-5. TAPE LOAD PROCEDURE.

The controls and indicators required for tape loading are contained, for convenience, in two places and either set may be used. One set is on the top of the tape transport deck and the other on the system control panel section associated with the particular transport. To load an MTT, perform the following steps.

STEP 1. Ensure that power has been removed from transport to be loaded.

STEP 2. Extend transport from cabinet.

Figure 3-1

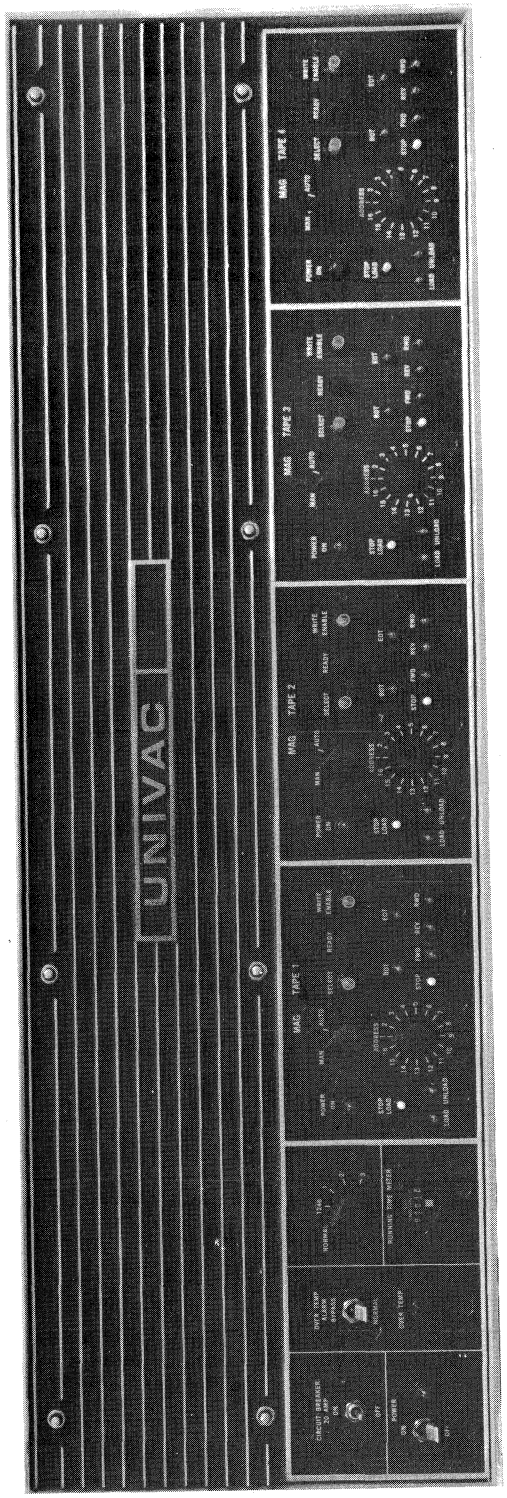


Figure 3-1. 1840 Modified System Control Panel

TABLE 3-1. SYSTEM CONTROL PANEL CONTROLS AND INDICATORS

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
CIRCUIT BREAKER 20 AMP ON/OFF	Combination Switch and Circuit Breaker: Two-Position Toggle, Manual Reset	ON: Applies primary power to MTS. OFF: Removes primary power from MTS.
POWER ON/OFF	Switch: Two-Position Toggle	ON: Applies power to MTS. OFF: Removes power from MTS.
	Indicator: Clear	Illuminates when primary power is applied to MTS power supply.
OVERTEMP ALARM		
BYPASS/NORMAL	Switch: Two-Position Toggle	BYPASS: Disables audible alarm when an overtemperature condition exists. NORMAL: Allows audible alarm to sound when an overtemperature condition exists.
OVERTEMP	Indicator: Red	Illuminates when temperature of cooling air in MTS exceeds 46±3 Degrees C. (overtemperature condition)
Program Mode	Switch: Five-Position Rotary	Select mode of operation.
NORMAL		7-Track Operation: Allows MTS to operate as a Univac 1540 MTS. 9-Track Operation: Allows MTS to operate in 9-track Phase Encoded and Non-Return-To-Zero modes by computer selection.
1240		Allows MTS to operate as a UNIVAC 1240 MTS. Not used for 9-track operation.
1		Allows MTS to operate off-line Program 1.
2		Allows MTS to operate off-line Program 2.
3		Allows MTS to operate off-line Program 3.

TABLE 3-1. SYSTEM CONTROL PANEL CONTROLS AND INDICATORS (CONT)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
RUNNING TIME METER	Meter: Time Totalizing	Cumulatively records time, in tenths of hours, that primary power is applied to MTS power supply.
POWER ON (one per transport)	Indicator: Amber	Illuminates when dc power is applied to associated tape transport.
MAN/AUTO (one per transport)	Switch: Two-Position Rotary	Selects mode of operation for associated tape transport. In MAN position, operation of associated tape transport is controlled by switches on control panel. In AUTO position, operation of the tape transport is controlled by MTS controller as selected by Program Mode switch and control panel operational switches are disabled.
SELECT (one per transport)	Indicator-Switch: Pushbutton, White	Switch: Pressing the pushbutton enables associated tape transport operation specified by Program Mode switch. Indicator: When illuminated, indicates tape transport selected.
READY (one per transport)	Indicator: Green	When illuminated, indicates associated tape transport properly loaded, in AUTO mode and ready for operation.
WRITE ENABLE (one per transport)	Indicator-Switch: Pushbutton, White	Switch: Pressing pushbutton enables associated tape transport to record if write enable ring is installed. Indicator: When illuminated, indicates associated tape transport is enabled to record.
LOAD (one per transport)	Indicator-Switch: Pushbutton, Clear	Switch: Pressing pushbutton initiates Auto Load sequence for loading tape on associated tape transport. Indicator: When illuminated, indicates Auto Load sequence is being performed. Extinguishes at the end of sequence.

TABLE 3-1. SYSTEM CONTROL PANEL CONTROLS AND INDICATORS (CONT)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
STOP LOAD (one per transport)	Switch: Pushbutton, White	Pressing pushbutton stops all operation and turns off vacuum blower on associated tape transport.
UNLOAD (one per transport)	Indicator-Switch: Pushbutton, Clear	Switch: Pressing pushbutton initiates Unload sequence which rewinds all tape to supply reel and turns off vacuum blower. Indicator: When illuminated, indicates Unload sequence is being performed. Extinguishes at end of the sequence.
ADDRESS 1-16 (one per transport)	Switch: 16-Position, Rotary	Provides for computer selection of alternate tape transport, enabling a malfunctioning transport to be taken off-line without cables having to be disconnected or interchanged. Switch setting designates associated transport as that number, i.e., position 1 designates TT1, 2 designates TT2, etc. With more than one switch in the same position, the leftmost transport designated for that position is selected. The other transport(s) is inoperative.
BOT (one per transport)	Indicator: Clear	When illuminated, indicates that associated tape transport is at beginning-of-tape (BOT) marker.
EOT (one per transport)	Indicator-Switch: Pushbutton, Clear	Switch: With forward movement of tape on associated tape transport, pressing pushbutton will simulate an end-of-tape (EOT) condition. Tape movement will stop after 10 feet and indicator will illuminate. Indicator: Illuminates when tape on associated tape transport is at or beyond EOT marker or after pushbutton is pressed.
STOP (one per transport)	Switch: Pushbutton, White	Pressing pushbutton master clears associated tape transport and stops tape movement.
FWD (one per transport)	Indicator-Switch: Pushbutton, Clear	Switch: Pressing pushbutton causes forward tape motion on associated tape transport. Tape motion continues until EOT is reached or STOP pushbutton is pressed.

TABLE 3-1. SYSTEM CONTROL PANEL CONTROLS AND INDICATORS (CONT)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
		Indicator: Illuminates while tape has forward motion.
REV (one per transport)	Indicator-Switch: Pushbutton, Clear	Switch: Pressing pushbutton causes reverse tape motion on associated tape transport. Tape motion continues until BOT is reached or STOP pushbutton is pressed. Indicator: Illuminates while tape has reverse motion.
RWD (one per transport)	Indicator-Switch: Pushbutton, Clear	Switch: Pressing pushbutton causes tape on associated tape transport to rewind at 200 ips to load point (BOT). Indicator: Illuminates while tape is rewinding.

TABLE 3-2. MAINTENANCE PANEL CONTROLS AND INDICATORS

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
COMP A/COMP B	Indicator-Switches: Pushbutton, Clear	
IN CONT		Switch: Pressing one of two pushbuttons allows associated computer control. Indicator: Illuminates when associated computer has control.
EIR		Switch: Pressing one of two pushbuttons sets external interrupt request line to associated computer. Indicator: Illuminates when external interrupt request line to associated computer is set.
EF		Switch: Pressing one of two pushbuttons simulates an external function acknowledge from associated computer. Indicator: Illuminates when an external function acknowledge, either simulated or computer generated, for associated computer is received.
DUP REQ		Switch: Pressing one of two pushbuttons simulates a duplex request control command from the associated computer. Indicator: Illuminates when a duplex request control command, either simulated or computer generated, for associated computer is received.

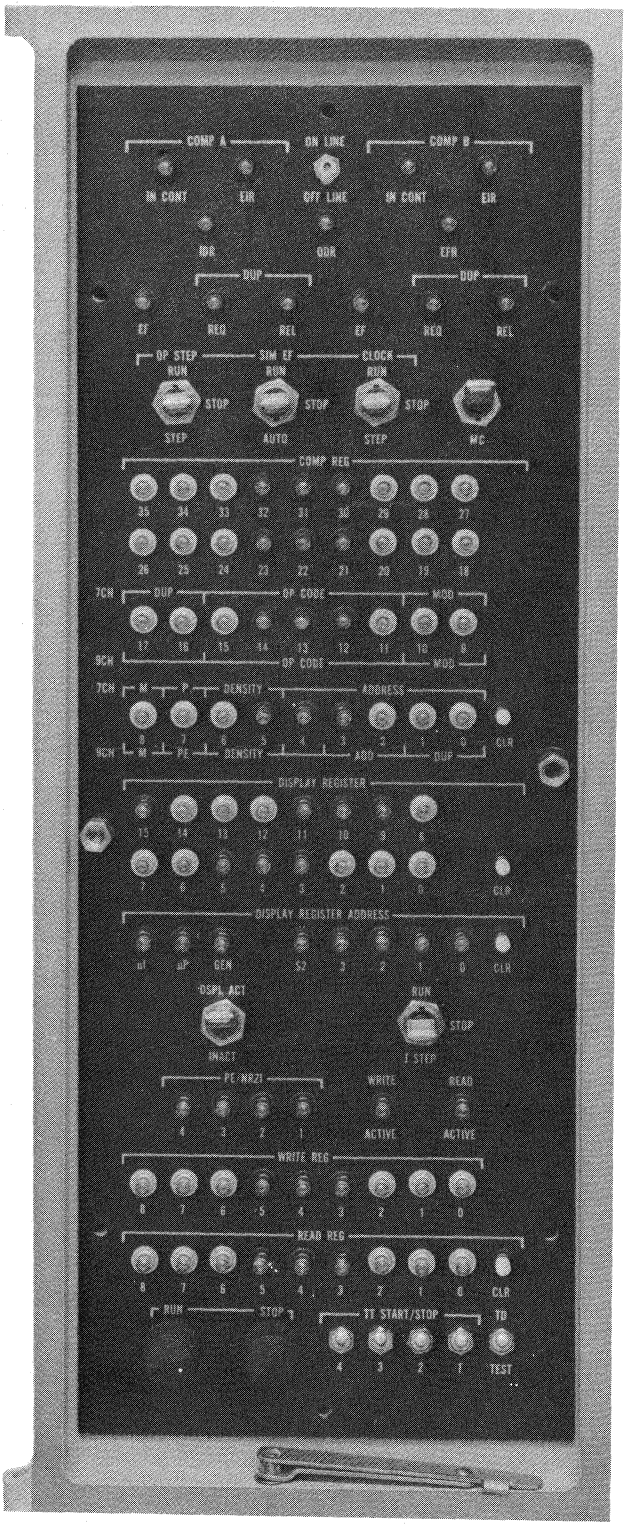


Figure 3-2. 1840 Modified Maintenance Control Panel

TABLE 3-2. MAINTENANCE PANEL CONTROLS AND INDICATORS (CONT)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
DUP REL		Switch: Pressing one of two pushbuttons simulates a duplex release control command from the associated computer. Indicator: Illuminates when a duplex release control command, either simulated or computer generated, for associated computer is received.
IDR	Indicator-Switch: Pushbutton, Clear	Switch: Pressing pushbutton sets input data request line to controlling computer when MTS is on-line. Indicator: Illuminates when input data request line to a controlling computer is set.
ODR	Indicator-Switch: Pushbutton, Clear	Switch: Pressing pushbutton sets output data request line to a controlling computer when MTS is on-line. Indicator: Illuminates when output data request line to a controlling computer is set.
EFR	Indicator: Clear	Illuminates when MTS is in idle condition.
ON LINE/OFF LINE	Switch: Two-Position Toggle	ON LINE: MTS operates under computer control. OFF LINE: Operation and control of the MTS is from maintenance panel.
OP STEP RUN/STOP/STEP	Switch: Two-Position Toggle	RUN: When MTS is on-line, allows EFs from a controlling computer to be processed. When MTS is off-line, allows an EF in the COMP REG to be processed. STOP: Disables processing of an EF. STEP: Allows one EF to be processed.
SIM EF RUN/STOP/AUTO	Switch: Three-Position Toggle	STOP: When off-line, disables processing of an EF. AUTO: Conditions MTS to process EFs at a speed determined by low speed oscillator. RUN: Conditions MTS to process EFs at normal speed.

TABLE 3-2. MAINTENANCE PANEL CONTROLS AND INDICATORS (CONT)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
CLOCK RUN/STOP/STEP	Switch: Three-Position Toggle	RUN: Selects MTS XTAL clock to free run. STOP: Disables MTS XTAL clock. STEP: Momentarily operating switch to this position allows one clock cycle.
MC	Switch: Two-Position Toggle, Spring-Loaded in MC Position	Operating switch to MC position master clears the MTS.
COMP REG 35-0	Indicator-Switches: Pushbutton, Clear	Displays contents of computer (C) register. Pressing an individual pushbutton sets corresponding flip-flop in C register.
CLR	White	Pressing CLR pushbutton clears C register.
DISPLAY REGISTER 15-0	Indicators: Clear	Displays contents of Display register. The contents of Display register are selected by DISPLAY REGISTER ADDRESS indicator-switches.
CLR	White	Pressing CLR pushbutton clears the register.
DISPLAY REGISTER ADDRESS	Indicator-Switches: Pushbutton, Clear	Switches are used to select information to be displayed in DISPLAY REGISTER.
μI		Pressing this pushbutton will cause present micro instruction to be displayed.
μP		Pressing this pushbutton will cause present microprogram address to be displayed.
GEN		Pressing this pushbutton will cause one of general registers A0-A7 to be displayed as determined by setting in DISPLAY REGISTER ADDRESS indicator-switches 3-0.
S2		Pressing this pushbutton will cause one of Source 2 registers to be displayed as determined by setting in DISPLAY REGISTER ADDRESS indicator-switches 3-0.
3, 2, 1, 0		Combination of these indicator-switches determines which general register or Source 2 register is to be displayed.
CLR		Pressing this pushbutton clears address register.

TABLE 3-2. MAINTENANCE PANEL CONTROLS AND INDICATORS (CONT)

NOMENCLATURE	SWITCH OR INDICATOR	FUNCTION
DSPL ACT/INACT	Switch: Two-Position Toggle	Operating this switch to DSPL ACT position allows contents of DISPLAY register to be displayed. Operating switch to INACT position disables displaying of Display register.
RUN/STOP/I STEP	Switch: Three-Position Toggle	Operating switch to RUN position allows MTS to perform micro instructions without restrictions. Operating switch to STOP position stops instruction execution. Operating switch to I STEP position enables MTS to perform 1 micro instruction.
PE/NRZI 4-1	Indicator-Switches: Pushbutton, Clear	Indicates recording mode of corresponding tape transport. When illuminated, mode is PE. When extinguished, mode is NRZI. Pressing a pushbutton selects corresponding tape transport for PE mode.
WRITE ACTIVE	Indicator-Switch: Pushbutton, Clear	When illuminated, indicates MTS is performing a write operation. Pressing pushbutton selects write mode of operation.
READ ACTIVE	Indicator-Switch: Pushbutton	When illuminated, indicates MTS is performing a read or post write read operation. Pressing the pushbutton selects read mode of operation.
WRITE REG 8-0	Indicator: Clear	Displays frame of information being written on tape.
READ REG 8-0 CLR	Indicators: Clear Switch: Pushbutton, White	Displays frame of information being read from tape. Pressing pushbutton clears register.
TT START/STOP 4-1	Switches: Two-Position Toggle	Operating a switch to up position allows starting and stopping of associated tape transport to be controlled by RUN and STOP potentiometers.
RUN/STOP	Rotary Switches (potentiometers)	Control speed of starting and stopping of a transport.
TD TEST	Switch: Two-Position Toggle	Operating switch to up position applies an input to logic delays for testing.

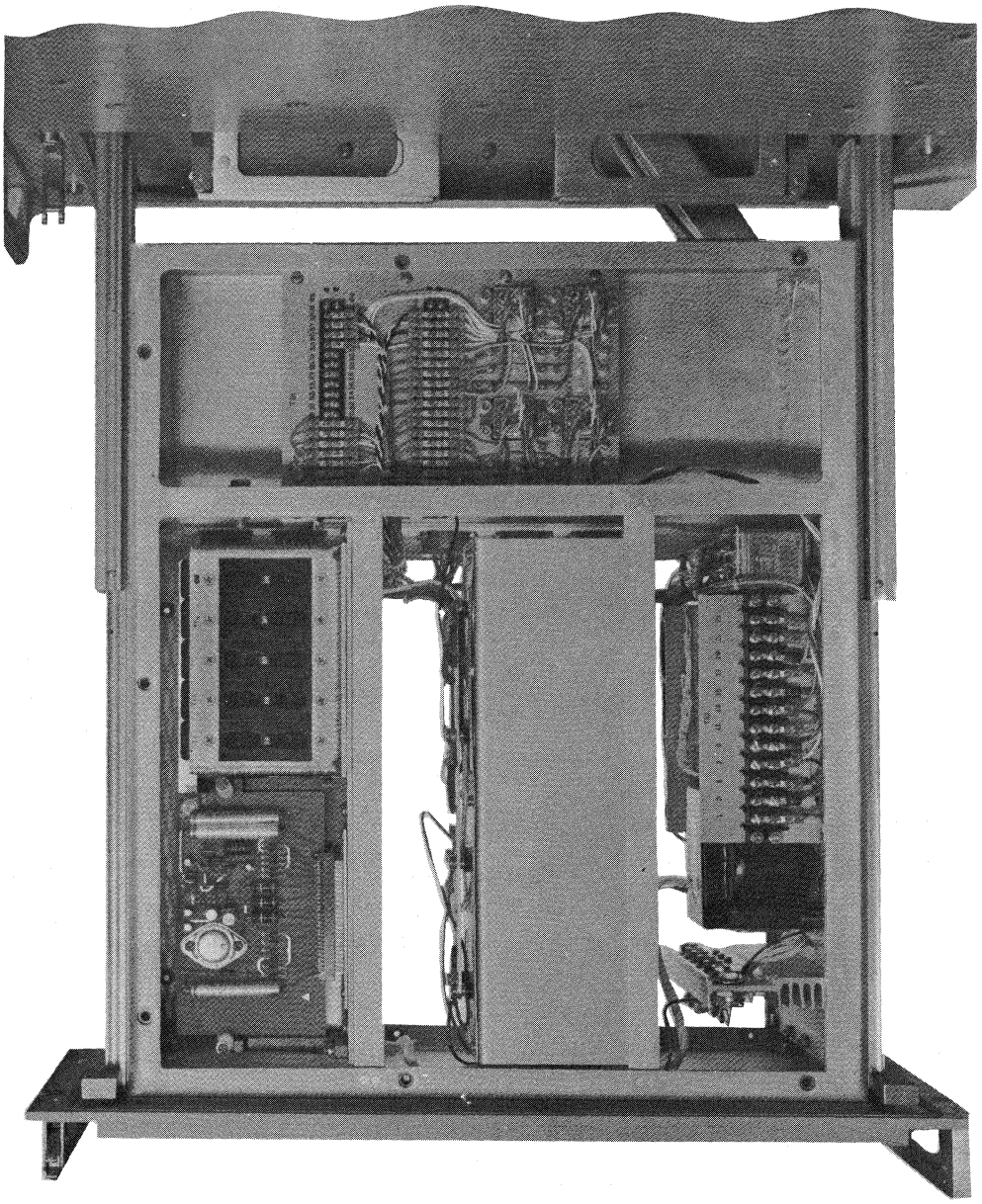


Figure 3-3. DC Power Circuit Breakers

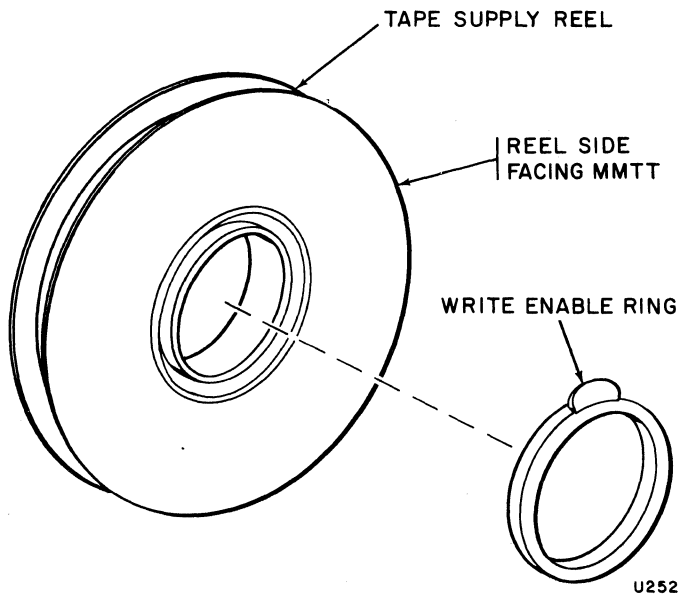


Figure 3-4. Tape Reel and Write Enable Ring

STEP 3. Release supply hub latch.

CAUTION

Avoid touching the tape at any point beyond the beginning-of-tape (BOT) marker. If the tape must be handled, grasp it along the outside edges.

STEP 4. If operation to be performed includes a write mode, ensure that a write enable ring is installed on the tape reel.

STEP 5. Install reel on reel hub so that tape is fed in a clockwise direction.

STEP 6. Lock supply hub latch.

STEP 7. If load is via system control panel, place associated MAN/AUTO switch to MAN.

STEP 8. Apply power to transport.

STEP 9. Press either associated system control panel LOAD switch or associated transport LOAD switch.

STEP 10. If associated MAN/AUTO switch is in MAN position, place it in AUTO position.

STEP 11. Close transport drawer.

The tape is now loaded and the BOT indicator and READY indicator will be lighted. The transport is now capable of operation under computer control.

3-6. TAPE UNLOAD PROCEDURE.

Unloading a tape from an MTT may be performed either via the system control panel or the associated transports UNLOAD pushbutton/indicator. To unload a tape perform the following procedure.

STEP 1. Apply power to the MTT.

STEP 2. If unloading is via system control panel, place the associated MAN/AUTO switch in the MAN position.

STEP 3. Press UNLOAD switch. Tape will rewind onto the supply reel.

STEP 4. After tape has rewound onto supply reel, remove reel from transport.

NOTE

If a malfunction occurs to prevent the unload sequence, remove power from the MTT and manually turn the supply reel counterclockwise to unload the tape.

3-7. INITIAL CONTROL SETTINGS.

The following paragraphs give the initial control settings which are to be checked before applying power to the equipment and performing a given operation.

a. COMPUTER CONTROLLED OPERATION. - Before applying power for operation under computer control, ensure the following switches are in the designated positions.

(1) MAINTENANCE PANEL CONTROLS.

1) ON LINE/OFF LINE switch to ON LINE.

2) OP STEP RUN/STOP/STEP switch to RUN.

3) SIM EF RUN/STOP/AUTO switch to RUN.

4) CLOCK RUN/STOP/STEP switch to RUN.

5) DISPL ACT/INACT switch to INACT.

6) RUN/STOP/I STEP switch to RUN.

7) TT START/STOP/1, 2, 3, 4 switches to down position.

8) TD/TEST switch to TEST position.

(2) SYSTEM CONTROL PANEL CONTROLS. - For each transport to be in operation.

1) MAN/AUTO switch to AUTO.

2) ADDRESS switch to numerical address of tape transport.

3) NORMAL/1240/1/2/3 switch to position of desired operation.

b. OFF LINE OPERATION. - The initial positions of the switches for off line operation are the same as those for computer controlled operation with the following differences.

1) ON LINE/OFF LINE switch to OFF LINE.

2) OP STEP RUN/STOP/STEP switch to STOP.

3-8. POWER-ON PROCEDURE.

To apply power to the MTS perform the following steps:

STEP 1. Ensure switches on maintenance panel and system control panel are in required positions for type of operation to be performed (see Initial Control Settings, paragraph 3-7).

STEP 2. Operate CIRCUIT BREAKER 20 AMP ON/OFF switch to ON.

STEP 3. Operate POWER ON/OFF switch to ON.

STEP 4. Operate OVER TEMP BYPASS/NORMAL switch to NORMAL.

STEP 5. On power supply drawer, release handle locks and slide out drawer to stops.

STEP 6. Operate circuit breaker switches for tape transports to be used and CU switch to ON.

STEP 7. Close and lock power supply drawer.

3-9. MICRO INSTRUCTION REPERTOIRE.

The instruction repertoire for the 1840 (Modified) Magnetic Tape Subsystem is as specified in table 3-3 and the following paragraphs. The normal use of the source (S) and destination (D) designators are as specified in tables 3-4 and 3-5, respectively.

a. TRANSFER (F=00). - This instruction transfers (S1) or (S2) to D1 or D2 as specified by M. The designator usage is as follows:

F - is 00
D - normal D1 or D2
S - normal S1 or S2
M - as specified in table 3-6.

b. JUMP (F=01). - This instruction jumps the micro program to the absolute address as specified by the 12 bit X field. (These 12 bits are loaded into the μP register.)

c. TRANSFER TO REMOTE DESTINATION (F=02). - This instruction is not used.

d. SHIFT (F=03). - This instruction shifts (S1) 1 bit position as specified by M and transfers the result to D1. The designator usage is as follows:

F - is 03
D - normal D1
S - normal S1
M - as specified in table 3-7.

TABLE 3-3. MICRO INSTRUCTION REPERTOIRE

INSTRUCTION FORMAT												DESCRIPTION
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
F = 0				D				S				M				Transfer
F = 1				X												Jump (Unconditional branch)
F = 2				D				S				M				Transfer to remote destination
F = 3				D				S				M				Shift
F = 4				D				S				M				Add Source 1
F = 5				D				S				M				Subtract
F = 6				D				S				M				Logic I
F = 7				D				S				M				Logic II
F = 10				D				K								Add constant
F = 11				D				K								Subtract constant
F = 12				D				K								Transfer constant to D1
F = 13				D				K								Transfer constant to D2
F = 14				FII				K								Branch
F = 15				FII				S				M				Micro control
F = 16				FII				K								Micro repeat
F = 17	M		R	C		P		K								Test and Set Bit

TABLE 3-4. NORMAL S-DESIGNATORS

S VALUE	SOURCE 1 (S1)	SOURCE 2 (S2)
0	Read Register	μP HOLD register
1	Read Reflective	Condition register
2	Status Register	Display register
3	Input Byte Unload Register	Console mode
4	Byte Address Register	
5	Working Storage (Buffer Memory)	
6	Format Converter	
7	CRC Register	
10	A0	
11	A1	
12	A2	
13	A3	Not assigned
14	A4	
15	A5	
16	A7	Console mode

TABLE 3-5. NORMAL D-DESIGNATORS

D VALUE	DESTINATION 1 (D1)	DESTINATION 2 (D2)
0	Write Register	μP register
1	Real Time Clock 1	Condition register
2	Real Time Clock 2	Display register
3	Output Byte Register	Cycle counter
4	Byte Address Register	
5	Working Storage (Buffer Memory)	
6	Format Converter	Not assigned
7	TT Select Register	
10	A0	CRC Register
11	A1	
12	A2	
13	A3	
14	A4	Not assigned
15	A5	
16	A6	
17	A7	

TABLE 3-6. M-DESIGNATOR FOR INSTRUCTION F=00

M				FUNCTION
3	2	1	0	
0	X	X	X	Do not update the Condition register
1	X	X	X	Update the Condition register
X	0	X	X	Transfer direct
X	1	X	X	Transfer data rotated left circularly 8 bit positions
X	X	0	0	Transfer (S1) to D1
X	X	0	1	Transfer (S2) to D1
X	X	1	0	Transfer (S1) to D2
X	X	1	1	Transfer (S2) to D2

TABLE 3-7. M-DESIGNATOR FOR INSTRUCTION F=03

M				FUNCTION
3	2	1	0	
0	X	X	X	Do not update the Condition register
1	X	X	X	Update the Condition register
X	0	X	X	Shift left 1 bit position
X	1	X	X	Shift right 1 bit position
X	X	0	0	Zero fill (right or left shift)
X	X	0	1	Sign fill (right shift) or circular (left shift)
X	X	1	0	Insert the bit shifted off in previous shift operation
X	X	1	1	Insert special (reserved for serial I/O data operations)

e. ADD SOURCE 1 (F=04). - This instruction adds (S1) to (A0) and transfers the sum to D1. The designator usage is as follows:

F - is 04
D - normal D1
S - normal S1
M - as specified in table 3-8.

TABLE 3-8. M-DESIGNATOR FOR INSTRUCTIONS F=04

M				FUNCTION
3	2	1	0	
0	X	X	X	Do not update the Condition register
1	X	X	X	Update the Condition register
X	0	0	0	(S1) + (A0) → D1, Force carry
X	0	0	1	(S1) + (A0) → D1, Carry hold
X	0	1	0	(S1) + (A0) → D1, Carry end around
X	0	1	1	(S1) + (A0) → D1, No carry
X	1	0	0	(S1) + POS ZERO → D1, Force carry
X	1	0	1	(S1) + NEG ONE → D1, Carry hold
X	1	1	0	(S1) + POS ZERO → D1, Carry end around
X	1	1	1	(S1) + NEG ONE → D1, No carry

f. SUBTRACT (F=05). - This instruction subtracts (S1) from (A0) and transfers the difference to D1. The designator usage is as follows:

F - is 05
D - normal D1
S - normal S1
M - as specified in table 3-9

TABLE 3-9. M-DESIGNATOR FOR INSTRUCTION F=05

M				FUNCTION
3	2	1	0	
0	X	X	X	Do not update the Condition register
1	X	X	X	Update the Condition register
X	0	0	0	(A0) - (S1) → D1, Force carry
X	0	0	1	(A0) - (S1) → D1, carry hold
X	0	1	0	(A0) - (S1) → D1, Carry end around
X	0	1	1	(A0) - (S1) → D1, No carry
X	1	0	0	POS ZERO - (S1) → D1, Force carry
X	1	0	1	POS ZERO - (S1) → D1, Carry hold
X	1	1	0	POS ZERO - (S1) → D1, Carry end around
X	1	1	1	POS ZERO - (S1) → D1, No carry

g. LOGIC I (F=06). - This instruction performs the logic function specified by M and transfers the result to D1. The designator usage is as follows:

F - is 06
D - normal D1
S - normal S1
M - as specified in table 3-10

TABLE 3-10. M-DESIGNATOR FOR INSTRUCTION F=06

M				FUNCTION	
3	2	1	0		
0	X	X	X	Do not update the condition register	
1	X	X	X	Update the condition register	
X	0	0	0	Logical Exclusive OR of (A0) and (S1)	$(A0) \oplus (S1)$
X	0	0	1	Logical complement of the logical AND of (A0) and (S1)	$\overline{(A0) \cdot (S1)}$
X	0	1	0	Logical AND of (A0) and the logical complement of (S1)	$(A0) \cdot \overline{(S1)}$
X	0	1	1	Logical complement of (S1)	$\overline{(S1)}$
X	1	0	0	Logical OR of (A0) and (S1)	$(A0) + (S1)$
X	1	0	1	All ones	1
X	1	1	0	(A0)	A0
X	1	1	1	Logical OR of (A0) and the logical complement of (S1)	$A0 + \overline{(S1)}$

h. LOGIC II (F=07). - This instruction performs the logic function specified by M and transfers the result to D1. The designator usage is as follows:

F - is 07
D - normal D1
S - normal S1
M - as specified in table 3-11

TABLE 3-11. M-DESIGNATOR FOR INSTRUCTION F=07

M				FUNCTION	
3	2	1	0		
0	X	X	X	Do not update the Condition register	
1	X	X	X	Update the Condition register	
X	0	0	0	Logical AND of the logical complement of (A0) and (S1)	$\overline{(A0)} \cdot (S1)$
X	0	0	1	Logical complement of (A0)	$\overline{(A0)}$
X	0	1	0	All zeros	0
X	0	1	1	Logical complement of the logical OR of (A0) and (S1)	$\overline{(A0) + (S1)}$
X	1	0	0	(S1)	(S1)
X	1	0	1	Logical OR of the logical complement of (A0) and (S1)	$\overline{(A0)} + (S1)$
X	1	1	0	Logical AND of (A0) and (S1)	$(A0) \cdot (S1)$
X	1	1	1	Logical complement of the logical Exclusive OR of (A0) and (S1)	$(A0) \oplus (S1)$

i. ADD CONSTANT (F=10). - This instruction adds the value of K in the instruction word to (A0) and transfers the sum to D1. The designator usage is as follows:

F - is 10
D - normal D1
K - an 8-bit absolute value (constant)

j. SUBTRACT CONSTANT (F=11). - This instruction subtracts the value of K in the instruction word from (A0) and transfers the difference to D1. The designator usage is as follows:

F - is 11
D - normal D1
K - an 8-bit absolute value (constant)

k. TRANSFER CONSTANT TO D1 (F=12). - This instruction transfers the value of K in the instruction word to D1. If the length of D1 is greater than eight bits, the upper bits will be zeros. The designator usage is as follows:

F - is 12
D - normal D1
K - an 8-bit absolute value (constant)

1. TRANSFER CONSTANT TO D2 (F=13). - This instruction transfers the value of K in the instruction word to D2. If the length of D2 is greater than eight bits, the upper bits will be zeros. The designator usage is as follows:

F - is 13
D - normal D2
K - an 8-bit absolute value (constant)

m. BRANCH (F=14). - This instruction transfers (μP) to μP HOLD and load bits 7-0 of μP with K leaving bits 15-8 of μP unchanged if the branch condition specified by FII is satisfied. The MPC uses the new (μP) as the address of the first instruction of a new program sequence. If the condition specified by FII is not satisfied, the MPC performs the next instruction as programmed. The designator usage shall be as follows:

F - is 14
FII - as specified in table 3-12
K - an 8-bit relative address

TABLE 3-12. FII DESIGNATOR INSTRUCTION F=14

FII				FUNCTION	BRANCH CONDITION
11	10	9	8		
0	0	0	0	BRANCH POSITIVE	Last arithmetic operation result had positive sign (COND register bit 14 set)
0	0	0	1	BRANCH ZERO	Last arithmetic operation had a result of zero (COND register bit 13 set)
0	0	1	0	BRANCH GREATER	Greater than result (COND register $[2^{11} \oplus 2^{12}] \oplus 2^{10} = 1$)
0	0	1	1	BRANCH OVERFLOW	Overflow, add or subtract (COND register $[2^{11} \cdot 2^{14}] + 2^{12} = 1$)
0	1	0	0	BRANCH CARRY	Carry (COND register bit 10 set)
0	1	0	1	BRANCH INSIDE LIMITS	Inside limits (COND register $2^9 \cdot [(2^{11} \oplus 2^{12}) \oplus 2^{10}] = 1$)
0	1	1	0	BRANCH DOUBLE ZERO	Double precision zero (COND register $2^8 + 2^{13} = 1$)
0	1	1	1	BRANCH SHIFT SAVE	Shift save (COND register bit 15 set)
1	0	0	0	BRANCH NOT ZERO	Last operation result was not zero (COND register bit 13 = 1)
1	0	0	1	BRANCH CYCLE COUNT FULL	Cycle count full
1	0	1	0	BRANCH PARITY EVEN	Parity even
1	0	1	1	BRANCH DATA NOT READY	Frame not read from tape
1	1	0	0	BRANCH ZERO FRAME	Last tape frame was all zeros (1600 BPI only)

TABLE 3-12. FII DESIGNATOR FOR INSTRUCTION F=14 (CONT)

FII				FUNCTION	BRANCH CONDITION
11	10	9	8		
1	1	0	1	BRANCH DATA READY	Frame has been read from tape
1	1	1	0	BRANCH TRUE	Last test condition was true
1	1	1	1	BRANCH FALSE	Last test condition was false

n. MICRO CONTROL (F=15). - This instruction controls various counters and discrete flip-flops in the MPC and the user and transfers K to the source bus. The designator usage is as follows:

F - is 15
FII = 0 or 4, increment
FII = 1, 2, 3, 5-17 unassigned
K - bit 0 set, Cycle counter; bits 1-7 unassigned

o. MICRO REPEAT (F=16). - This instruction repeats the next instruction or series of instructions as specified by FII and K to accomplish the function specified in table 3-13. The MPC transfers (μP) to μP HOLD before the repeat sequence (μP HOLD stores the address of the first repeated instruction; the contents of μP HOLD are transferred to μP for each repeat cycle). The designator usage is as follows:

F - is 16
FII - as specified in table 3-13
K - as specified in table 3-13

TABLE 3-13. FII AND K DESIGNATORS FOR INSTRUCTION F=16

FII				FUNCTION	K
11	10	9	8		
0	0	0	0	Multiply single: Multiply (S1) by COND and store the product in D1 (most significant half, MSH) and COND (least significant half, LSH). The MPC performs the multiplication when the instruction following the F16, FII=0 instruction is an F4 (Add) instruction with M=03, S1 specifies the source of the multiplicand, and D1 specifies one of registers A0-A3. The A register specified by D1 must be cleared before executing the F16, FII=0 instruction.	The value of K is to be equal to the number of bits of the multiplier. For K=16, the multiply single instruction shall require 3.4 μs (17 CLOCK cycles)

TABLE 3-13. FII AND K DESIGNATORS FOR INSTRUCTION F=16 (CONT)

FII				FUNCTION	K
11	10	9	8		
0	0	0	1	Divide single: Divide the double length dividend, the MSH in one of registers A0-A3, the LSH in COND by (S1) and store the quotient in COND with the remainder in D1. The MPC performs the division when the instruction following the F16, FII=1 instruction is an F5 (Subtract) instruction with M=00, S1 specifies the source of the divisor and D1 specifies one of registers A0-A3. The A register specified by D1 shall be required to be cleared before executing the F16, FII 1 instruction. The quotient must be in 2's complement fractional arithmetic. The quotient shall be an integer if the dividend is shifted left 1 bit before the F16, FII=1 instruction.	The value of K is to be equal to the number of bits of the divisor. For K=16, the divide single instruction shall require 3.4 μsec (17 Clock cycles)
0	0	1	0	Unassigned	
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1	Unassigned	
1	0	0	0	Repeat normal: Perform the following K+1 instructions are programmed n + 1 times, where n is equal to the contents of the cycle count register.	The number of instructions is 1 plus the value in 3-0 of K.
1	0	0	1	Unassigned	
1	0	1	0	Repeat normal, suppress last cycle: Perform the following K+1 instructions as programmed n times, where n is equal to the contents of the cycle count register.	The number of instructions is 1 plus the value in bits 3-0 of K.
1	0	1	1	Unassigned	
1	1	0	0	Repeat, activate multiple accumulators: Perform the following K+1 instructions as programmed n + 1 times, where n is equal to the contents of the cycle count register. The operation of instructions that reference A0 for an operand (F=4 through 11) is modified as follows: the least significant 2 bits of the D1 designator specify one of registers A0-A3 as the operand source; the destination function of D1 remains normal.	The number of instructions is 1 plus the value in bits 3-0 of K.

TABLE 3-13. FII AND K DESIGNATORS FOR INSTRUCTION F=16 (CONT)

FII				FUNCTION	K
11	10	9	8		
1	1	0	1	Unassigned	
1	1	1	0	Repeat, activate multiple accumulators, suppress last cycle: same as FII=14 except that the cycle count shall be n instead of n + 1.	The number of instructions is 1 plus the value in bits 3-0 of K
1	1	1	1	Unassigned	

p. TEST AND SET BIT (F=17). - This instruction provides the capability to:

1) Manipulate, i.e.

a) Set and/or clear discrete flip-flops.

b) Activate control signals.

2) Test the state of flip-flops or logic circuitry.

The designator usage shall be as follows:

F - is 17
M, R, C, P, as specified in table 3-14
K - as specified in table 3-15 for Hardware bits. Program bits are specified in the Microprogram.

When the cascade bit is set, the results of a series of Test Bit instructions will be combined. If the test condition(s) are satisfied, Branch True will be enabled.

TABLE 3-14. CONTROL BITS FOR INSTRUCTION F=17

M	R	C	P	FUNCTION
0	X	X	X	Test
1	X	X	X	Manipulate
X	0	X	X	Clear, or test for zero
X	1	X	X	Set, or test for one
X	X	0	X	Do not cascade test
X	X	1	X	Cascade test
X	X	X	0	K designates hardware bit
X	X	X	1	K designates program bit

TABLE 3-15. HARDWARE BITS FOR INSTRUCTION F=17

K	M	R	FUNCTION
0	0	X	Test Clock 1 Counted to Zero
0	1	X	Set or Clear Lateral Parity Check Enable
1	0	X	Test EOT
1	1	X	Set or Clear Improper Condition
2	X	X	Test, Set or Clear XIRG
3	0	X	Test Clock 2 Counted to Zero
3	1	X	Set or Clear Input Timing Error
4	X	X	Test, Set or Clear ODR
5	0	X	Test Data Ready
5	1	0	Clear Data Ready
5	1	1	Set Off Line EF
6	0	X	Test Lateral Parity Error
6	1	0	Clear Lateral Parity Error
6	1	1	Set Direction
7	X	X	Format Converter Control
10	0	X	Test Buffer Full or Buffer Empty
10	1	X	Set or Clear Longitudinal Parity Error
11	X	X	Test, Set or Clear Improper Frame Count
12	0	X	Test Capstan Zero
12	1	X	Start or Stop Transport
13	0	X	Test Power Out of Tolerance
13	1	X	Set or Clear Tape Mark
14	X	X	Test, Set or Clear OBR Loaded
15	0	X	Test IDR
15	1	0	Clear IDR
15	1	1	Clear Parity Error
16	X	X	Test and Control Direction
17	0	X	Test EF Computer B
17	1	0	Clear EF Computer B
17	1	1	Not Used
20	0	X	Test CRC
20	1	X	Set or Clear EXT INT A
21	0	X	Test CRC Error
21	1	X	Set or Clear EXT INT B

TABLE 3-15. HARDWARE BITS FOR INSTRUCTION F=17 (CONT)

K	M	R	FUNCTION
22	0	X	Test if Display Mode
22	1	X	Set or Clear Output Timing Error
23	0	X	Test for Off Line
23	1	X	Set or Clear ODR
24	0	X	Test for Write Strobe
24	1	0	Clear Write Strobe
24	1	1	Not Used
25	X	X	Test, Set or Clear A In Control
26	X	X	Test, Set or Clear B In Control
27	0	X	Test EF Computer A
27	1	0	Clear EF Computer A
27	1	1	Not Used
30	0	X	Test Transport Ready
30	1	X	Set or Clear MPC Busy
31	X	X	Test, Set or Clear Input Byte Register Loaded
32	X	X	Test or Set Write on Read
33	0	X	Test for Load Point
33	1	X	Change Bias
34	X	X	Test, Set or Clear Request Control from Computer A
35	X	X	Test, Set or Clear Release Control from Computer A
36	X	X	Test, Set or Clear Request Control from Computer B
37	X	X	Test, Set or Clear Release Control from Computer B
40	0	X	Test for Phase Encoding
40	1	X	Set or Clear OBR to IBR
41	0	X	Test for Odd or Even Parity
41	1	X	Change Parity Odd or Even
42	0	X	Test for Off Line 0
42	1	X	Set or Clear Modified Stop
43	0	X	Test for Off Line 1
43	1	X	Set or Clear Write Gap
44	0	X	Test Selected Write Enable
44	1	0	Clear WS Indices
44	1	1	Not Used
45	X	X	Test, Set or Clear 200 BPI

TABLE 3-15. HARDWARE BITS FOR INSTRUCTION F=17 (CONT)

K	M	R	FUNCTION
46	0	X	Test 1540 or Normal Mode
46	1	X	Set or Clear 556 BPI
47	0	X	Test 1240 Mode
47	1	X	Set or Clear 300 BPI
50	0	X	Test Data Active
50	1	X	Set or Clear 8 Bits Flag
51	0	X	Test ID Burst
51	1	X	Set or Clear Slow Mon Clock (RTC 2 Nano or Milli)
52	0	X	Test for Tape Mark
52	1	X	Set or Clear Not In Control Status
53	0	X	Test Phase Encoding In
53	1	X	Set or Clear Single Dead Track
54	X	X	Test, Set or Clear External Interrupt A
55	X	X	Test, Set or Clear External Interrupt B
56	0	X	Test Off Line 2
56	1	X	Set or Clear Enable Erase Head
57	X	X	Test, Set or Clear Rewind
60	0	X	Test Selected and Rewinding
60	1	X	Set or Clear Write ID Burst
61	X	X	Test, Set or Clear Postamble
64	0	X	Test Character is Zero
64	1	0	Clear Character is Zero
64	1	1	Not Used
67	1	X	Set or Clear Phase Encoding

3-10. MPC INTERRUPTS.

There are four conditions which will cause the present MPC operation to be terminated and an interrupt sequence to be started. These conditions and their associated interrupt entrance addresses are given in table 3-16.

TABLE 3-16. MPC INTERRUPTS

ENTRANCE ADDRESS	FUNCTION
10	Power out of tolerance
12	Running and not ready
14	Demand Duplex
16	PE Tape Mark detected

SECTION 4

PRINCIPLES OF OPERATION

4-1. GENERAL.

This section explains the operating principles of the MTS. The information includes block diagram analysis, functional analysis, a description of the computer/MTS interface, and function word and status word characteristics. The block and functional diagrams and accompanying theory present a simplified analysis of the MTS as an operating subsystem and make it easier to understand the detailed diagrams in section 7.

Specific information on the principles of operation of the transport is published in the Univac technical manual PX 7984.

The terms "input" and "output", as used in this section, mean input to the computer and output from the computer. Requests are always submitted by the MTS to the computer; acknowledges are always sent by the computer to the MTS.

4-2. SIMPLIFIED BLOCK DIAGRAM ANALYSIS. (Figure 4-1).

The MTS provides auxiliary data storage for a computer, performing operations under computer control. These operations consist, basically, of read, write, search, space file, and rewind. Some operations are supplemented by parity and density selection. Densities available for computer selection are 200 and 556 frames per inch when operating in the 1240 mode. When operating as a 1540, the MTS may write in either of three densities: 200, 556, or 800. When the MTS is configured for 9-track operation, the densities available are 200, 556, and 800 for NRZI recording/reading or 1600 for PE recording/reading. All operations except rewind are performed at a tape speed of 120 inches per second; tape speed during rewind is 200 inches per second.

Interaction between the computer in control and the MTS is conducted in three major steps or sequences: transmission of an external function word, transmission of data, and transmission of the status word. These functions are described in the following subparagraphs.

a. TRANSMISSION OF EXTERNAL FUNCTION WORD. - The computer directs MTS operations by means of an 18-bit external function word for 7-track configurations or a 16-bit word for a 9-track configuration. This word is sent to the MTS at the start of each operation and also when there is a change in operation. The word defines the type of operation to be performed and provides instructions for performing it. The controller then interprets the word and prepares the MTS for the specified operation and advises the computer that the MTS is ready for the transmission of data. (Refer to paragraph 4-4 for a detailed discussion of the external function word format.)

b. DATA TRANSMISSION. - Data is transmitted after completion of the function word transmission and translation. Flow of data may be either information transmitted from the computer, through the controller, to the selected transport for recording on tape, or it may be information previously recorded on tape and now retrieved and transmitted through the controller to the computer for processing.

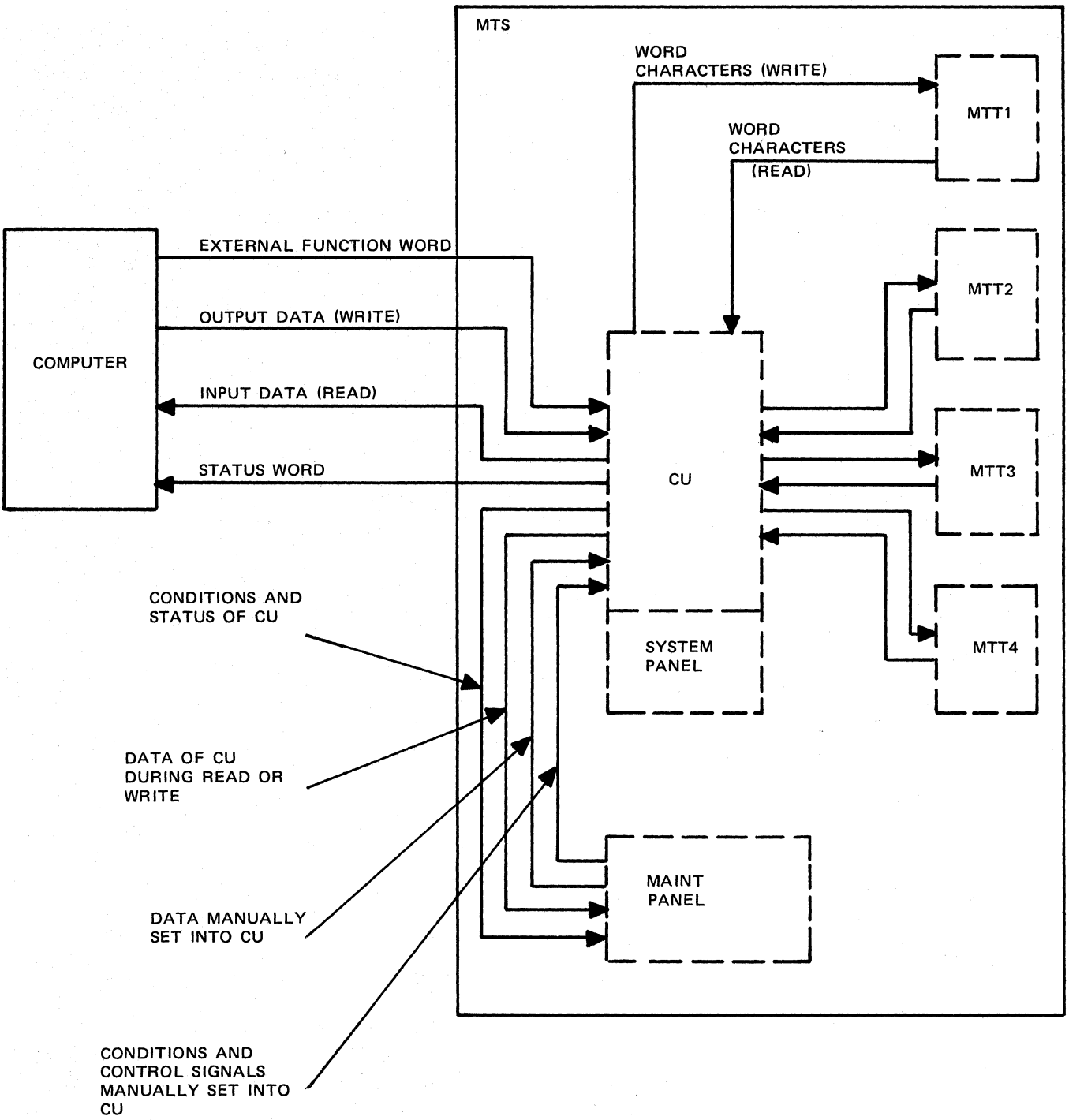


Figure 4-1. MTS and Computer, Simplified Diagram

Data words sent by the computer to the MTS during a write operation are 16- to 36-bit transmissions, depending upon computer capability. The controller receives each word and divides it into 6-bit (7-track) or 8-bit (9-track) characters, adds a lateral parity bit to each character and transmits the characters to the transport, where they are written as frames on tape.

During a read operation, the controller retrieves the characters recorded on tape, checks and then deletes the parity bit from each character, reassembles the character into the modulus specified computer word form and transmits each reassembled word to the computer.

c. STATUS WORD TRANSMISSION. - After a data record has been processed or on request from the computer (1540 or 9-track modes), the MTS sends the computer a 15-bit or 16-bit (9-track mode only) status word. This status word informs the computer of the MTS status at the time the computer requests status or after completion of an operation. When status is sent after completion of an operation, the word advises the computer whether or not an operation was completed successfully, of any errors detected, and the type of error. In the 9-track mode of operation, the status word indicates the method of recording used, either NRZI or PE. For a detailed analysis of the status word formats, refer to paragraph 4-5.

4-3. MTS/COMPUTER INTERFACE.

Communications between the MTS and the computer are accomplished over two main channels, an input channel and an output channel. There is one cable for each channel. Conductors within each cable are grouped as shown in figure 4-2. The functions performed over each channel are explained in table 4-1.

4-4. EXTERNAL FUNCTION WORD FORMATS.

The MTS is capable of operation using any of three different external function word formats. One format is for operation in the 1240 mode; one for the 1540 mode; and the third for 9-track operation. The MTS communicates with the computer using requests and acknowledges. The computer issues commands to the MTS by means of the external function signal and an instruction (function) word. The MTS inspects the instruction word and performs the specified operation(s).

a. 1240 Mode. - In the 1240 mode of operation, there are four types of external function words: master clear; address word; instruction word; and transmit extra. The address word (figure 4-3) specifies the transport and the instruction word (figure 4-4) operation(s) to be performed by the transport.

Five basic operations can be initiated by the instruction word: read, search, write, backspace, and rewind. The basic operations are supplemented by format and density selections. All external function commands except master clear are ignored by the MTS during the performance of an operation (MTS busy).

The MTS is capable of communicating with only one transport at a particular moment. Starting from the idle state, the general sequence of events is:

1) Computer sends an address word via the external function command

2) MTS selects the addressed transport

3) Computer sends an instruction word via the external function command

TABLE 4-1. MTS/COMPUTER INTERACTION

CHANNEL	SIGNAL NAME	ORIGIN	MEANING
Output	External Function Request (EFR)	MTS	The MTS is ready to perform an operation and requests an external function word from the controlling computer
	External Function Acknowledge (EFA)	Computer	The controlling computer has placed an external function word on the output data lines to the MTS and now is acknowledging the request by this signal. (The function word commands the MTS to set up for and perform a specific task or type of operation.)
	Output Data Request (ODR)	MTS	The MTS has set up its circuits for and is ready to perform the operation specified by the function word. It is now requesting an output data word from the computer. (This signal is used for selective read or search codes and write operations.)
	Output Data Acknowledge (ODA)	Computer	The computer has placed data on the output data lines in response to the ODR and now is acknowledging the data request by this signal. (The data may be either a selective read or search code or data to be written on tape.)
Input	Input Data Request (IDR)	MTS	The MTS has placed a computer word on the input data lines and is now requesting the computer to accept the data.
	Input Acknowledge (IA)	Computer	The computer has accepted the data from the MTS and acknowledges the request by this signal. The lines are cleared and the MTS may now send another IDR. This signal is also used to acknowledge an external interrupt or status interrupt.
	External Interrupt (EI) or Status Interrupt	MTS	The MTS has detected a condition which ends an operation (i.e., end-of-record, parity error, etc.) and now sends this signal to indicate that a status word has been placed on the input data lines.

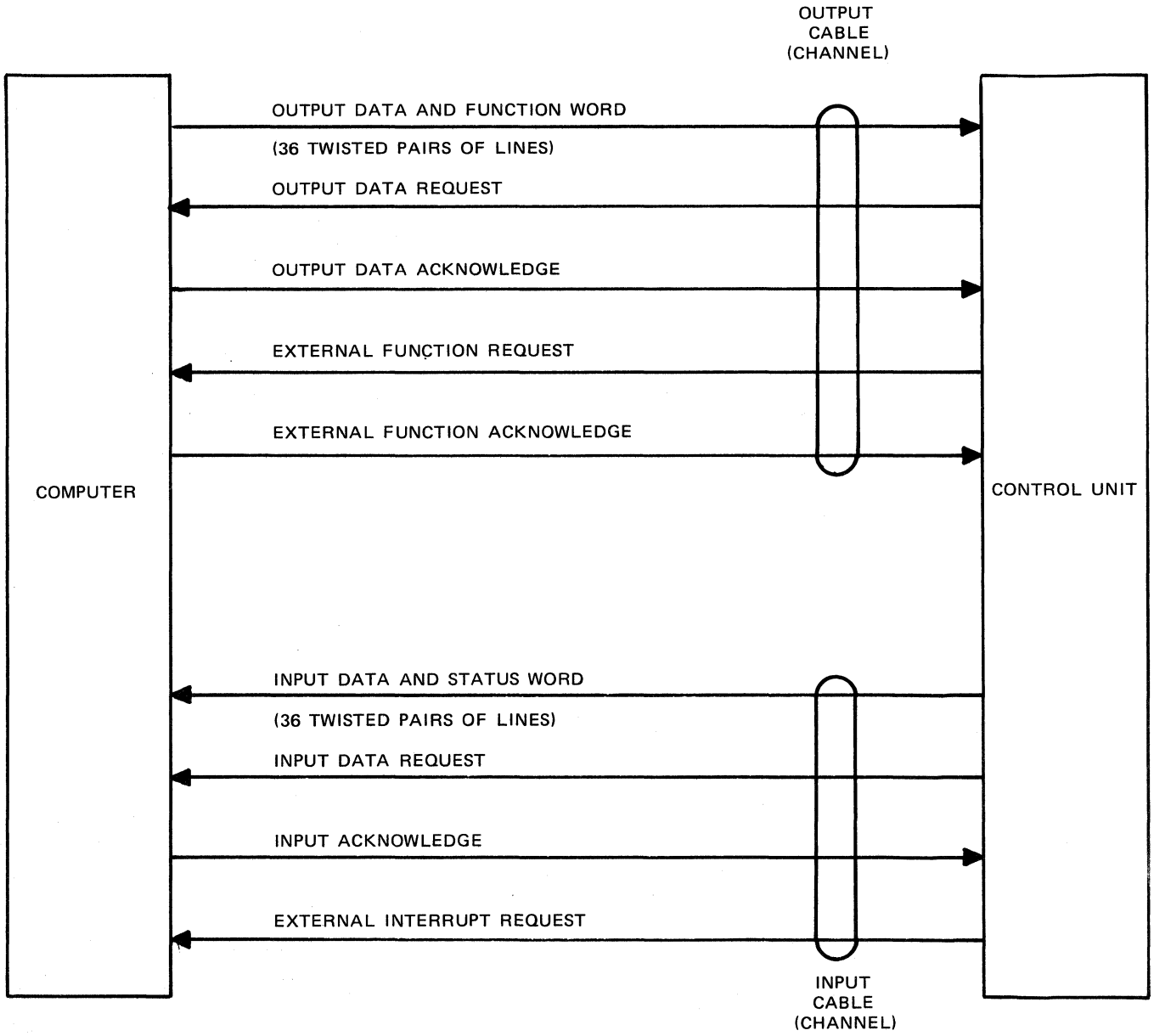
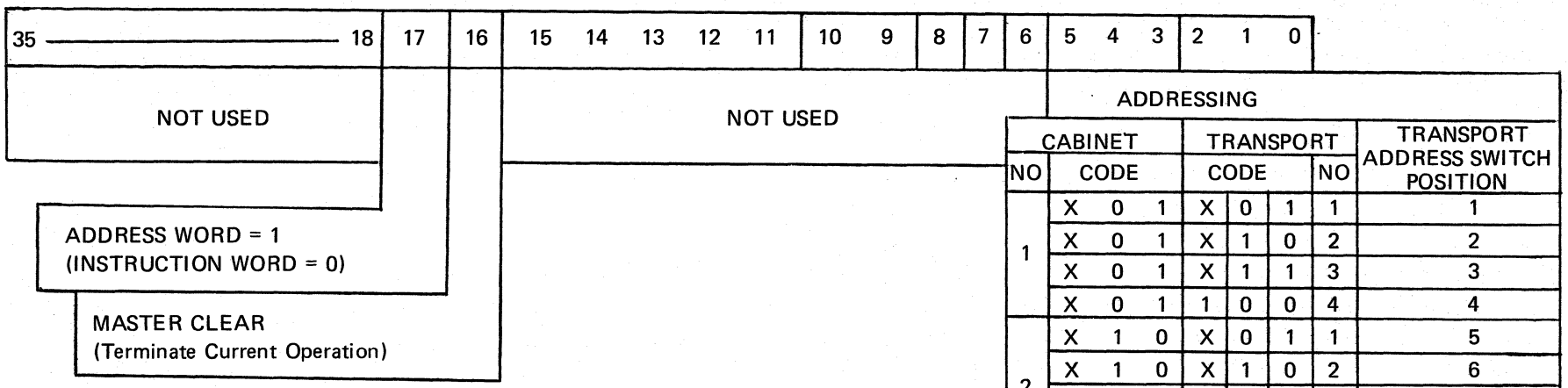


Figure 4-2. MTS/Computer Interface

ADDRESS WORD FROM COMPUTER



CABINET NO	CABINET CODE			TRANSPORT CODE			TRANSPORT NO	TRANSPORT ADDRESS SWITCH POSITION
1	X	0	1	X	0	1	1	1
	X	0	1	X	1	0	2	2
	X	0	1	X	1	1	3	3
	X	0	1	1	0	0	4	4
2	X	1	0	X	0	1	1	5
	X	1	0	X	1	0	2	6
	X	1	0	X	1	1	3	7
	X	1	0	1	0	0	4	8
3	X	1	1	X	0	1	1	9
	X	1	1	X	1	0	2	10
	X	1	1	X	1	1	3	11
	X	1	1	1	0	0	4	12
4	X	0	0	X	0	1	1	13
	X	0	0	X	1	0	2	14
	X	0	0	X	1	1	3	15
	X	0	0	1	0	0	4	16

X = Bit not interpreted

Figure 4-3. 1240 Mode Address Word

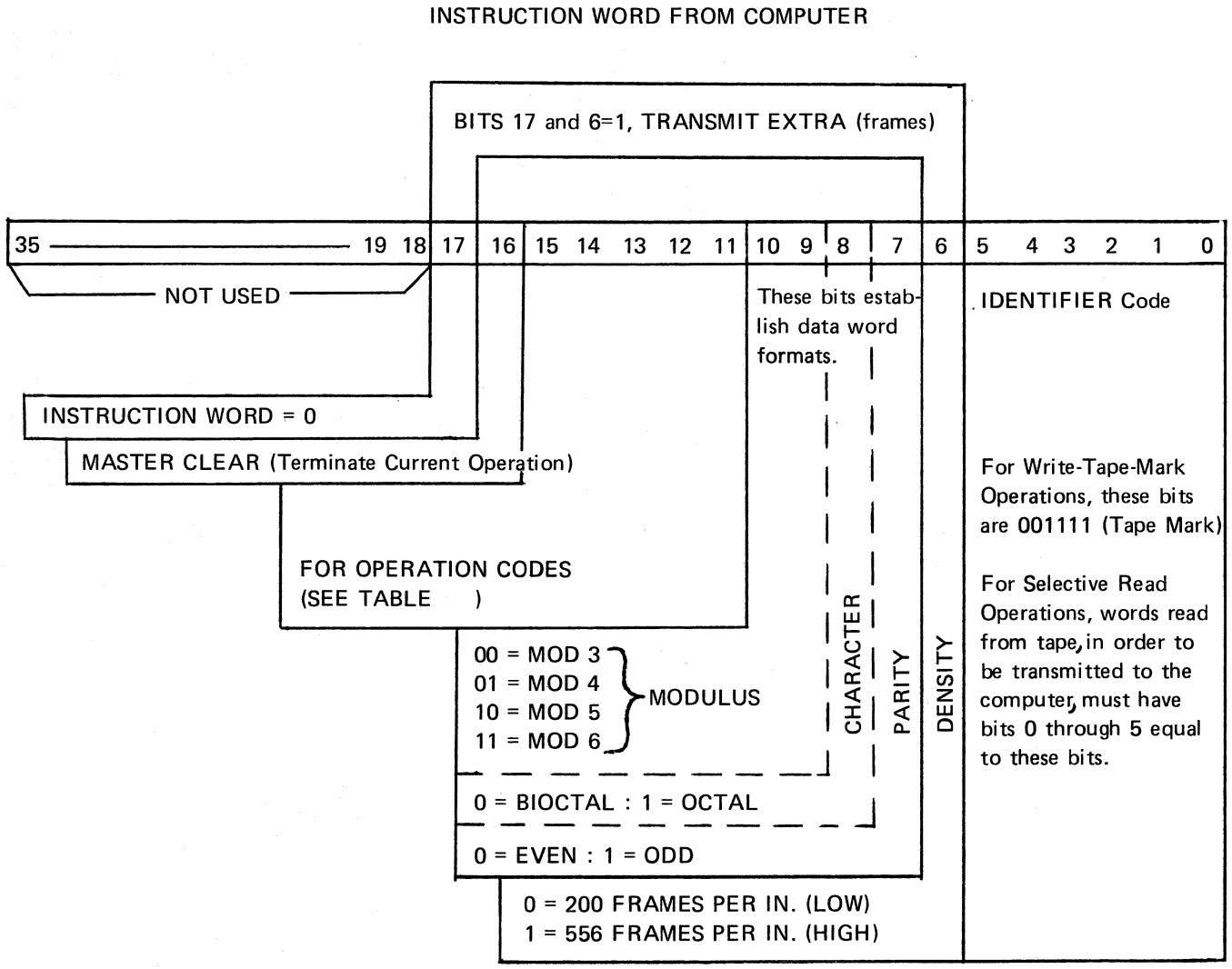


Figure 4-4. 1240 Instruction Word

4) MTS under microprogram control interprets the instruction word and becomes busy

5) Microprogram controller initiates the instruction word specified operation(s).

6) At completion of the specified operation(s), MTS sends a status word via an external interrupt and issues a stop command to the transport.

b. 1540 Mode. - In the 1540 mode of operation, the operations stated in the external function word (figure 4-5) are of six basic types: duplex selection, read, search, write, space file and rewind. The basic operations are supplemented by transport selection, bias selection, format designators, and density.

The computer is capable of communicating with only one transport at a particular moment. Starting from a master cleared state, the general sequence of events is as follows:

1) Computer sends an external function command word via the external function acknowledge signal.

2) The MTS under microprogram control interprets the external function command and selects the addressed transport.

3) Microprogram controller initiates the specified operation(s).

4) At completion of the specified operation(s), MTS sends a status word via the external interrupt and issues a stop command to the selected transport.

5) Computer interprets the status word and acknowledges the interrupt thereby placing the MTS in the idle state.

c. 9-TRACK MODE. - In the 9-track mode of operation, the operations stated in the external function word (figure 4-6) are of eight basic types: duplex selection, read, search, space file, space block, write, erase, and rewind. The basic operations are supplemented by transport selection, format designators, density, and recording method.

The computer is capable of communicating with only one transport at a particular moment. Starting from a master clear state, the general sequence of events is as follows:

1) Computer sends an external function command word via the external function acknowledge signal.

2) The MTS under microprogram control interprets the external function command and selects the addressed transport.

3) Microprogram controller initiates the specified operation(s).

4) At completion of the specified operation(s), MTS sends a status word via the external interrupt and issues a stop command to the selected transport.

5) Computer interprets the status word and acknowledges the interrupt thereby placing the MTS in the idle state.

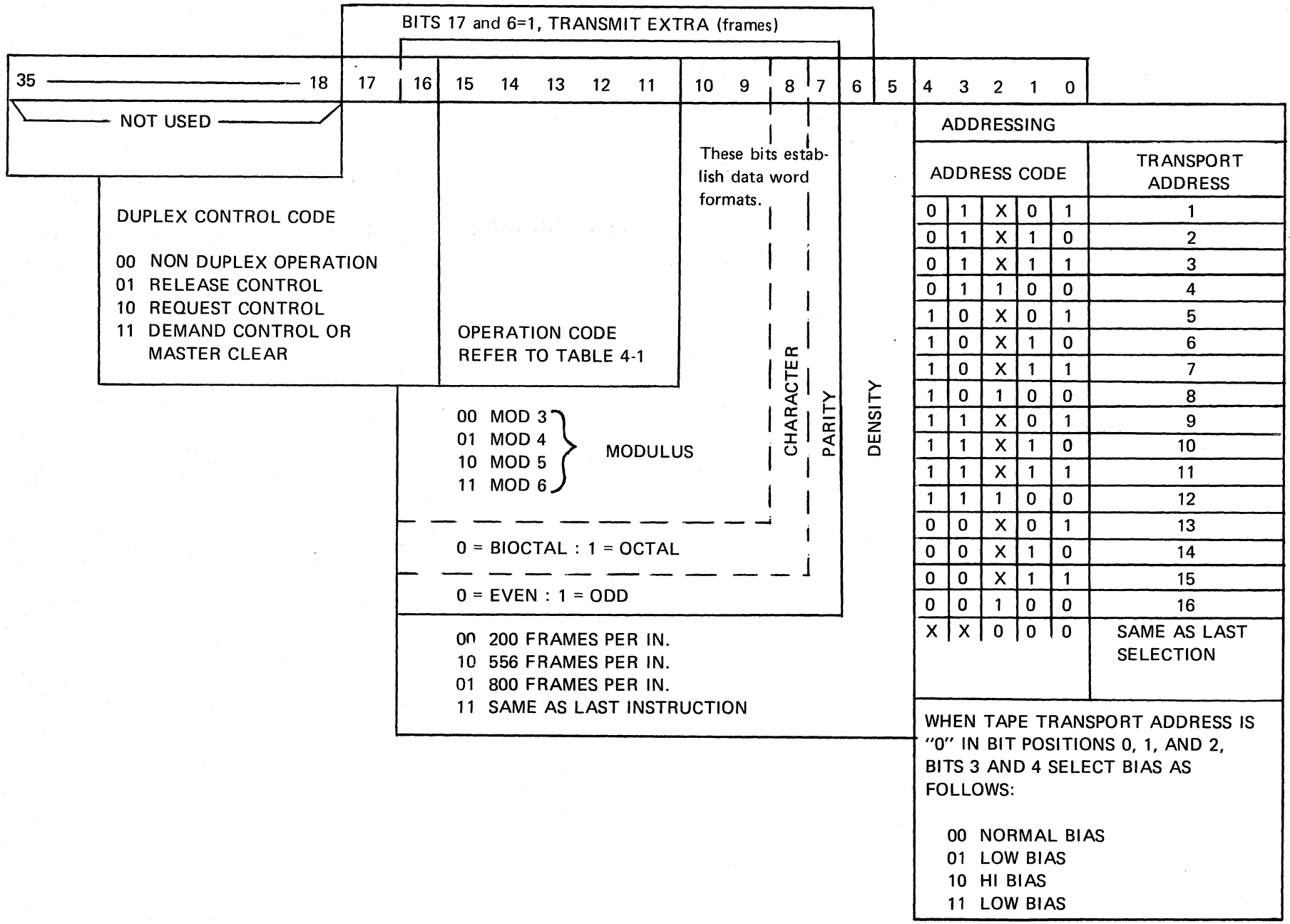


Figure 4-5. External Function Word Format - 1540 Mode

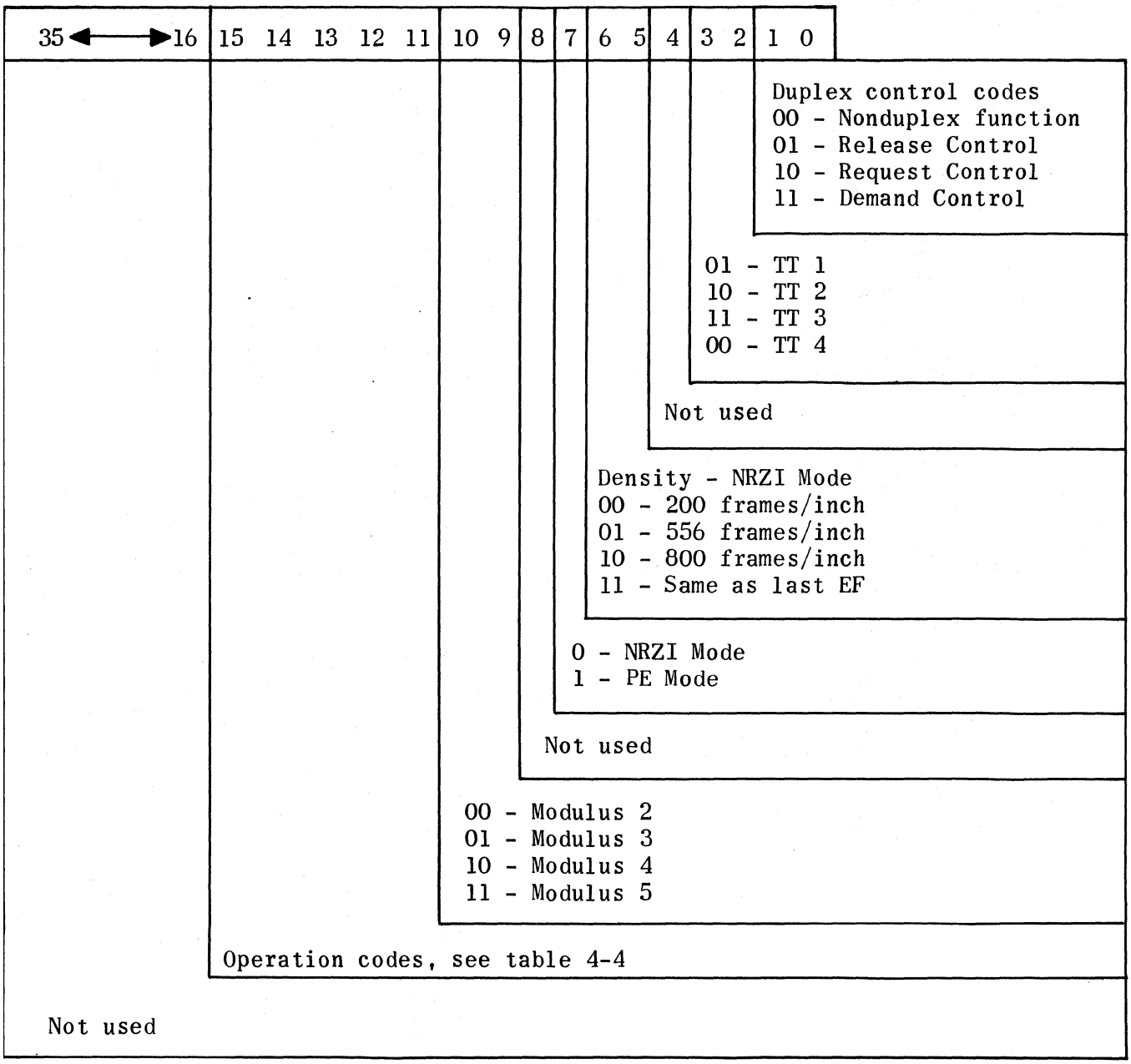


Figure 4-6. External Function Word, 9-Track Mode

d. FUNCTION WORD DESIGNATOR, 1240 MODE. - The function word designator is used only in the 1240 mode of operation. When the function word designator, bit 17, is a "1", the function word is defined as an address word. When the designator is a "0", the function word is defined as an instruction word. Figure 4-3 shows the address word format and figure 4-4 the instruction word format.

e. MASTER CLEAR, 1240 MODE. - In the 1240 mode of operation, a master clear of the MTS is performed when bit 16 in the external function word is a "1". (See figures 4-3 and 4-4.)

The master clear differs from the other 1240 operations in three respects:

1) It may be performed at any time.

2) Master clear has priority over all other operations in the function word.

3) It does not result in a status interrupt.

Master clear stops all tape motion (except a rewinding tape) and sets the MTS to the idle state. The MTS will accept another external function any time after the master clear. Since master clear is not considered a normal operation, its use should be restricted to times when the MTS is believed to be in an illogical state, or when the state of the MTS cannot be determined.

f. OPERATION CODES. - The operation codes for all three modes of operation are determined by bits 15-11 of the external function word. Table 4-2 gives the operation codes for the 1240 mode of operation; table 4-3 for the 1540 mode; and table 4-4 for the 9-track mode. While some codes perform the same type of operation in all modes, other codes produce different operations depending on the mode. The following subparagraphs give the description of the codes and differences were applicable.

(1) READ FORWARD (00000). - The transport moves tape forward at normal speed and transfers 7-bit/9-bit frames from the tape to the controller. One bit in each frame is the lateral parity bit. The other bits are data. The controller, under microprogram, control checks lateral parity for each frame and, at the same time, the data from the other channels is assembled into 18, 24, 30 or 36-bit computer words for 7-track operation or 16, 24, 32 or 36-bit computer words for 9-track operation. After assembling a computer word, the controller places the data on the input data lines to the computer. The IDR line is then set to request computer acceptance of the data. The computer responds with an input acknowledge to signify its acceptance of the data word. Data being read from tape, which cannot be immediately assembled into a computer word, is stored in the working storage memory for future assembly when the computer input lines are free. This assembly and transfer of data words continues until the IRG is reached, regardless of any error detected during parity checking.

When the controller senses the end of record, it sends a status-interrupt to the computer. The status word indicates any errors encountered during the reading of the record.

(2) READ SELECTIVE (00001). - The transport moves tape forward at normal speed reading the words from one record whose bits 5 through 0 (7-track) or 7 through 0 (9-track) of the first frame are the same as the selective read code. The read portion of the selective read operation is the same as for a normal read. After initiation of the read selective operation, the MTS sends an ODR to the

TABLE 4-2. OPERATION CODES, 1240 MODE

EF Bits 15	14	13	12	11	OPERATION
0	0	0	0	0	Read Forward
0	0	0	0	1	Read Selective
0	0	0	1	0	Read, Ignore Error Halt
0	0	0	1	1	Space File
0	0	1	0	0	Search, Type I
0	0	1	0	1	Search, Type II
0	0	1	1	0	Search File, Type I
0	0	1	1	1	Search File, Type II
0	1	0	0	0	Write
0	1	0	0	1	Write XIRG
0	1	0	1	0	Write Ignore Error Halt
0	1	0	1	1	Write XIRG, Ignore Error Halt
0	1	1	0	0	Write Tape Mark
0	1	1	0	1	Write Tape Mark, XIRG
0	1	1	1	1	Write Tape Mark, XIRG
1	0	0	0	0	Backspace
1	0	0	0	1	Backspace
1	0	0	1	0	Backspace - Read
1	0	0	1	1	Backspace - File
1	0	1	0	0	Backsearch Type I
1	0	1	0	1	Backsearch Type II
1	0	1	1	0	Backsearch File Type I
1	0	1	1	1	Backsearch File Type II
1	1	0	0	0	Rewind
1	1	0	0	1	Rewind, Clear Write Enable
1	1	0	1	0	Rewind
1	1	0	1	1	Rewind, Clear Write Enable
1	1	1	0	0	Rewind Read
1	1	1	0	1	Rewind - Read, Clear Write Enable
1	1	1	1	0	Rewind Read
1	1	1	1	1	Rewind - Read, Clear Write Enable

TABLE 4-3. OPERATION CODES, 1540 MODE

EF Bits 15	14	13	12	11	OPERATION
0	0	0	0	0	Read Forward
0	0	0	0	1	Read Selective
0	0	0	1	0	Read, Modified Stop
0	0	0	1	1	Space File
0	0	1	0	0	Search, Type I
0	0	1	0	1	Search, Type II
0	0	1	1	0	Search, File, Type I
0	0	1	1	1	Search, File, Type II

TABLE 4-3. OPERATION CODES, 1540 MODE (CONT)

EF Bits					OPERATION
15	14	13	12	11	
0	1	0	0	0	Write
0	1	0	0	1	Write XIRG
0	1	0	1	0	Write, Ignore Error Halt
0	1	0	1	1	Write XIRG, Ignore Error Halt
0	1	1	0	0	Write Modified Stop
0	1	1	0	1	Write Edit
0	1	1	1	0	Write Tape Mark
0	1	1	1	1	Write Tape Mark, XIRG
1	0	0	0	0	Backread
1	0	0	0	1	Backread Selective
1	0	0	1	0	Backread, Modified Stop
1	0	0	1	1	Backspace File
1	0	1	0	0	Backsearch Type I
1	0	1	0	1	Backsearch Type II
1	0	1	1	0	Backsearch File Type I
1	0	1	1	1	Backsearch File Type II
1	1	0	0	0	Rewind
1	1	0	0	1	Rewind Clear-Write Enable
1	1	0	1	0	Rewind
1	1	0	1	1	Rewind, Clear Write Enable
1	1	1	0	0	Rewind Read
1	1	1	0	1	Rewind Read, Clear Write Enable
1	1	1	1	0	Rewind Read
1	1	1	1	1	Request Transport Status

TABLE 4-4. OPERATION CODES, 9-TRACK MODE

EF Bits					OPERATION
15	14	13	12	11	
0	0	0	0	0	Read Forward
0	0	0	0	1	Read Selective
0	0	0	1	0	Space Block
0	0	0	1	1	Space File
0	0	1	0	0	Search, Type I
0	0	1	0	1	Search, Type II
0	0	1	1	0	Search File, Type I
0	0	1	1	1	Search File, Type II
0	1	0	0	0	Write
0	1	0	0	1	Write XIBG
0	1	0	1	0	Write, Ignore Error Halt
0	1	0	1	1	Write XIBG, Ignore Error Halt
0	1	1	0	0	Write Modified Stop
0	1	1	0	1	Erase
0	1	1	1	0	Write Tape Mark
0	1	1	1	1	Write Tape Mark, XIBG

TABLE 4-4. OPERATION CODES, 9-TRACK MODE (CONT)

EF Bits					OPERATION
15	14	13	12	11	
1	0	0	0	0	Backread
1	0	0	0	1	Backread Selective
1	0	0	1	0	Backspace Block
1	0	0	1	1	Backspace File
1	0	1	0	0	Backsearch Type I
1	0	1	0	1	Backsearch Type II
1	0	1	1	0	Backsearch File Type I
1	0	1	1	1	Backsearch File Type II
1	1	0	0	0	Rewind
1	1	0	0	1	Rewind, Clear Write Enable
1	1	0	1	0	Rewind, Interrupt at Load Point
1	1	0	1	1	Rewind
1	1	1	0	0	Rewind Read
1	1	1	0	1	Reread
1	1	1	1	0	Rewind Read
1	1	1	1	1	Request Transport Status

computer requesting the selective read identifier code. If the computer does not transmit the code word before the first word from tape is assembled, the operation is terminated and the MTS sends a status external interrupt word with an output timing error indication.

(3) READ, IGNORE ERROR HALT (00010), 1240 MODE. - The transport moves tape forward at normal speed and reads data from tape as for a normal read except parity errors will be ignored and the entire record will be sent. After transmitting the entire record, the MTS will send a status external interrupt word with a parity error indication if an error was detected.

(4) READ, MODIFIED STOP (00010), 1540 MODE. - The operation of the read modified stop is the same as for a normal read except for the stopping of the transport.

The read modified stop, used in a forward direction, delays the stopping of the transport for an additional 0.3 inch of tape travel. The modified stop gives the computer time to initiate a new forward function without a stop signal actually being applied to the transport. If a new forward function is not received immediately, the tape stops after moving an additional 0.3 inch into the IRG.

(5) SPACE BLOCK (00010), 9-TRACK MODE. - The transport moves forward at normal speed and stops in the next IRG. No data is transferred during this operation.

(6) SPACE FILE (00011). - The transport moves forward at normal speed and stops in the IRG past the first tape mark detected (see figure 4-7). The transport stops and the MTS generates a status external interrupt to the computer with a tape mark indication.

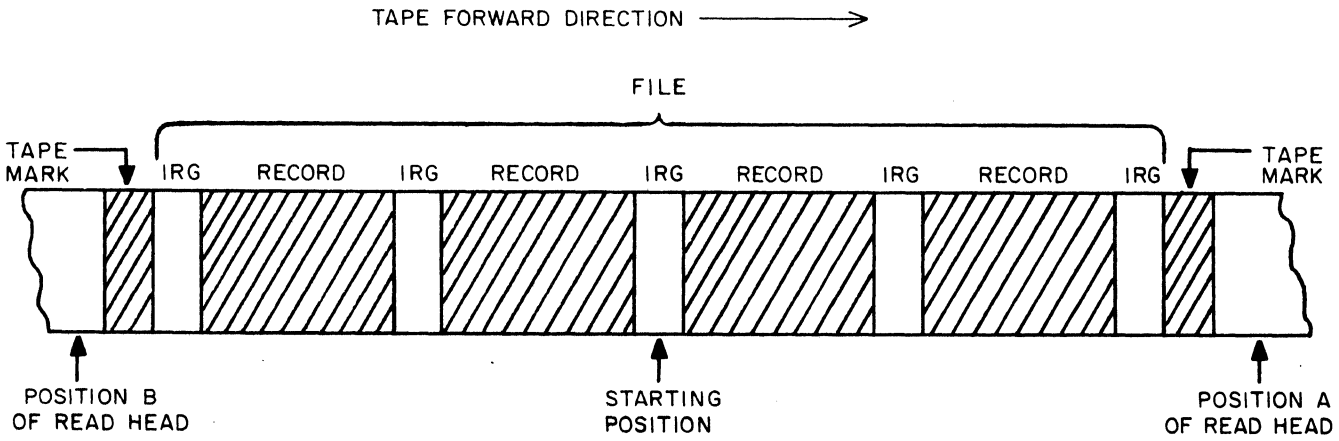


Figure 4-7. Search/Space File

(7) SEARCH, TYPE I (00100). - In a search type I operation, the transport moves forward at normal speed searching for a record whose first word read is equal to or greater than the search key word. When a search comparison is satisfied, the MTS performs a normal read operation on the record. At the initiation of a search operation, the computer must transfer an output data word to the MTS which is the search key word. If the computer does not transfer the search key word before the first word from tape is assembled, the operation will terminate and the MTS will generate a status external interrupt word with an output timing error indication. If a parity error occurs before a search comparison is made, the MTS will terminate the search operation and generate a status external interrupt word with a parity error indication.

(8) SEARCH, TYPE II (00101). - The search type II operation is identical to the search type I except that the first word of the record must be identical to the search key word to have a search comparison.

(9) SEARCH FILE, TYPE I (00110). - The search file type I operation performs the same function as the search type I operation except that the search operation is limited to a file. A file is defined as one or more records separated from the succeeding file by a tape mark. The difference between search type I and search file type I is that the search file type I operation terminates if a tape mark is detected before a type I comparison is made. When the MTS detects a tape mark, a status external interrupt is generated with a tape mark indication.

(10) SEARCH FILE, TYPE II (00111). - The search file type II operation performs the same function as the search type II operation except that the search operation is limited to a file and terminates if a tape mark is detected before

a find. Detection of a tape mark causes the MTS to generate a status external interrupt with a tape mark indication.

(11) WRITE (01000). - The write function is supplemented by format, density, modulus, and recording method (9-track only). The selected transport moves tape forward at normal speed to write one record of data. The MTS accepts output data words from the computer, disassembles them into data frame characters according to the modulus selection and character configuration, generates frame parity (9-track is odd parity only) and transfers each data frame character to the transport for recording in a frame on tape. A lateral parity check is made of each frame written on tape. If a parity error is detected, the MTS stops the write operation and generates a status external interrupt to the computer with a parity error indication. If an output timing error occurs during the write operation, the MTS stops the write operation and generates a status external interrupt to the computer with an output timing error indication. When the working storage buffer is empty and the computer does not respond to an ODR within sufficient time for another word to be written, the MTS initiates the end-of-write sequence. In 7-track operation, the end-of-write consists of writing three frames of zeros followed by the longitudinal parity character and then dropping the ODR and stopping the transport. In 9-track 200 bpi NRZI operation, the end-of-write consists of writing three frames of zeros followed by the longitudinal parity character. In 9-track 556 or 800 bpi NRZI operation, the end-of-write consists of three frames of zeros, the cyclic redundancy check, three frames of zeros, and then the longitudinal parity character. In 9-track 1600 bpi PE operation, the postamble is written following the data. After each of the 9-track type operations, the ODR is dropped and the tape transport stopped. After the write operation is completed, the MTS sends a status external interrupt to the computer with all status.

(12) WRITE XIRG (01001). - The write XIRG operation is the same as the normal write operation except that the interrecord gap is 3-1/2 $\pm$1/2 inches instead of the normal 3/4 inch gap. This gap precedes the record specified by the external function word.

(13) WRITE IGNORE ERROR HALT (01010). - The write ignore error halt operation is the same as a normal write operation except that lateral parity errors are ignored and the transport does not stop until all data is recorded. After the record is completed, the status word sent to the computer will contain the indication that at least one lateral parity error occurred.

(14) WRITE XIRG IGNORE ERROR HALT (01011). - The write XIRG ignore error halt operation is the same as for a normal write except that the interrecord gap preceding the record is extended to 3-1/2 $\pm$1/2 inches and lateral parity errors are ignored until status is sent to the computer.

(15) WRITE TAPE MARK (01100), 1240 MODE. - The tape mark is a special mark written in a fixed format in a tape frame. It functions as a one frame record and is used to separate files. A file can be one or more records. The tape mark consists of 1's in tracks 1, 2, 3 and 4 and 0's in tracks 5, 6 and 7. The instruction word containing the write tape mark operation code must specify even parity, bioctal character and have the 001111 in bit positions 5 through 0. After the tape mark is written, three frames of all 0's (end-of-record) and the longitudinal parity frame are written on tape. After all of the above frames have been written to indicate end of file, the MTS generates a status external interrupt to the computer and stops tape motion.

(16) WRITE MODIFIED STOP (01100). - The operation code 01100 is used for the write modified stop operation in the 1540 and 9-track modes. There is no write modified stop operation in the 1240 mode.

(a) 1540 MODE. - The write modified stop operation is the same as for a normal 1540 mode write except for the stopping of the transport. The stop signal to the transport is delayed for an additional 0.3 inch of tape movement.

(b) 9-TRACK MODE. - The write modified stop operation is the same as for a normal 9-track mode write except for the stopping of the transport. The stop signal to the transport is delayed for an additional 0.15 inch of tape movement.

(17) WRITE TAPE MARK, XIRG (01101), 1240 MODE. - The write tape mark XIRG operation is the same as for a normal 1240 mode write tape mark operation except that the interrecord gap before the tape mark is extended to 3-1/2 $\pm$1/2 inches.

(18) WRITE EDIT (01101), 1540 MODE. - The write edit operation is the same as a normal 1540 mode write operation except that the erase head is not energized. Certain programming restrictions are placed on the operation since the writing is imposed over the previous record. These restrictions are:

1) The record to be recorded must be exactly the same length as the record to be written over if another record follows it.

2) Reverse motion of the tape, except rewind if first record on tape is to be written over, should not immediately precede a write edit as tape creep may cause the spacing to be incorrect and leave part of the old record in the IRG

3) Care must be exercised with any records that were written using XIRG because part of the old record may be left in the succeeding IRG.

(19) ERASE (01101), 9-TRACK MODE. - The erase operation code enables the erase head on the selected transport and causes the transport to move forward erasing tape for 3 inches. The transport then stops.

(20) WRITE TAPE MARK (01110), 1540 MODE or 9-TRACK MODE. - The writing of a tape mark in either the 1540 or 9-track mode uses the operation code 01110. The type of tape mark written is dependent on the mode of operation and, for 9-track the recording density.

(a) 1540 MODE. - The tape mark functions as a one frame record to separate files. In the 1540 mode of operation, the tape mark consists of 1's in tracks 1, 2, 3 and 4 and 0's in tracks 5, 6 and 7. Initiating a write tape mark operation will cause the selected transport to write the tape mark followed by three frames of all 0's (end-of-record) and then the longitudinal parity character. After writing these frames, the MTS sends a stop signal to the transport.

(b) 9-TRACK MODE. - In the 9-track mode of operation, the write tape mark operation code will cause one of three types of tape marks to be written. The type of tape mark is dependent on the recording density.

1. 200 FPI. - When 200 fpi density is specified, the tape mark recorded on tape consists of one frame with 1's in tracks 2, 3 and 8 and 0's in the remaining tracks. Then three frames are recorded with 0's in all tracks. The longitudinal parity character is recorded in the next frame and a stop is sent to the transport.

2. 556 or 800 FPI. - When either 556 or 800 fpi density is specified, the tape mark recorded on tape consists of one frame with 1's in tracks 2, 3 and 8 and 0's in the remaining tracks. This is followed by recording six frames of 0's in all tracks, the cyclic redundancy check, three frames of 0's in all tracks, and then the longitudinal parity character. The MTS then sends a stop to the transport.

3. 1600 FPI. - When 1600 fpi density is specified, the tape mark recorded on tape consists of 83 frames of 0's in tracks 1, 2, 4, 5, 7 and 8 and tracks 3, 6 and 9 dc erased. After the tape mark is written, the MTS sends a stop to the transport.

(21) WRITE TAPE MARK XIRG (01111), 1540 MODE or 9-TRACK MODE. - The write tape mark XIRG operation code initiates the same operations as for a write tape mark in the 1540 and 9-track modes except that the interrecord gap is longer. The extended interrecord gap is 3-1/2 $\pm$1/2 inches.

(22) BACKSPACE (1000X), 1240 MODE. - The 1240 mode backspace operation code, may be either 10000 or 10001, causes the addressed transport to move one record in the reverse direction. The tape then stops in the IRG properly positioned for reading or writing. Parity is checked while backspacing and, if an error is detected, the status external interrupt word will contain a parity error indication. The backspace function is supplemented by formal and density.

(23) BACKREAD (10000), 1540 MODE or 9-TRACK MODE. - A backread operation may be performed only in the 1540 or 9-track mode. The backread operation in either of these two modes is the same as for a read forward except the MTS moves tape in the reverse direction. Since the data is read from tape in the reverse order, the MTS reverses the assembly order to produce normal words and transfers the words to the computer in reverse order, i.e., last word first and first word last. The MTS stops the tape in the IRG preceding the record read so that the record may be re-read or rewritten.

(24) BACKREAD SELECTIVE(10001), 1540 MODE or 9-TRACK MODE. - A backread selective operation may be performed only in the 1540 or 9-track mode. The operation is the same as a read selective operation except with reverse tape direction and word assembly as for a backread operation.

(25) BACKSPACE-READ (10010), 1240 MODE. - The backspace-read operation causes the addressed transport to move one record in the reverse direction, to stop in the IRG at the beginning of the record, and then to perform a normal read forward transferring the record to the computer. Parity is checked while backspacing. If either a longitudinal or lateral parity error is detected, the record will not be read. Instead, tape motion will be stopped in the IRG preceding the record and a status external interrupt will be sent to the computer with the error indication. The backspace-read operation is supplemented by format and density.

(26) BACKREAD, MODIFIED STOP (10010), 1540 MODE. - The backread modified stop operation is the same as for a backread except that the tape stops 0.072 inch less than normal into the IRG. This allows the recovery of data from tapes having abnormally short IRGs. Subsequent rewriting may destory information in the record following the one being written over.

(27) BACKSPACE BLOCK (10010), 9-TRACK MODE. - The backspace block (record) operation code causes the selected transport to move one record in the reverse direction. The tape then stops in the IRG preceding the record. Parity is checked

while backspacing and, if an error is detected, the status external interrupt word will contain a parity error indication. The backspace function is supplemented by format and density.

(28) BACKSPACE FILE (10011). - The transport moves in reverse at normal speed and stops in the IRG beyond the first tape mark detected. The transport stops and the MTS generates a status external interrupt to the computer with a tape mark indication.

(29) BACKSEARCH TYPE I (10100). - The backsearch type I operation is basically the same as a search type I operation except the tape is moved in the reverse direction. The MTS mode of operation determines the word on which the comparison is made and the continued operation of the MTS.

(a) 1240 MODE. - In the 1240 mode of operation, the comparison is made on the last word read in the record. Since the tape motion is reverse, the search-key word must be reversed characterwise for a positive comparison. When the MTS determines a comparison of the search-key and the last word read, the transport is stopped, the direction is changed to forward, and a normal read and transfer is made of the record.

(b) 1540 MODE or 9-TRACK MODE. - In either the 1540 or 9-track mode of operation, the comparison is made on the first word read in the record. Since the tape motion is reverse, the word read from tape is assembled in reverse order characterwise for comparison with the search-key word. When the MTS determines a comparison of the search-key and the first word read, a backread operation is performed to read the entire record.

(30) BACKSEARCH TYPE II (10101). - The backsearch type II operation is basically the same as a search type II except tape is moved in the reverse direction MTS operation for determining a find and continued operation is the same as for a backsearch type I.

(31) BACKSEARCH FILE TYPE I (10110). - The backsearch file type I operation is the same as a backsearch type I operation except the search is limited to a file. Detecting a tape mark before making a comparison will cause the MTS to stop transport movement and send a status external interrupt to the computer with a tape mark indication.

(32) BACKSEARCH FILE TYPE II (10111). The backsearch file type II operation is the same as a backsearch type II operation except the search is limited to a file. Detecting a tape mark before making a comparison will cause the MTS to stop transport movement and send a status external interrupt to the computer with a tape mark indication.

(33) REWIND (110X0), 1240 MODE or 1540 MODE. - The operation codes 11000 and 11010 will cause the addressed transport to rewind to BOT at rewind speed of 200 ips when operating in either the 1240 or 1540 mode. After initiating the rewind, the MTS will send a status external interrupt to the computer.

(34) REWIND (11000 or 11011), 9-TRACK MODE. - The operation codes 11000 or 11011 will cause the addressed transport to rewind to BOT at rewind speed of 200 ips when operating in the 9-track mode. After initiating the rewind, the MTS will send a status external interrupt to the computer.

(35) REWIND, CLEAR WRITE ENABLE (110X1), 1240 MODE or 1540 MODE. - The operation codes 11001 and 11011 are used in either the 1240 or 1540 mode of operation to initiate a rewind and clear the write enable. To perform writing on tape after either of the two codes is used, the write enable must be manually set.

(36) REWIND, CLEAR WRITE ENABLE (11001), 9-TRACK MODE. - The operation code 11001 is used in the 9-track mode of operation to initiate a rewind and clear the write enable. To perform writing on tape after this code is used, the write enable must be manually set.

(37) REWIND, INTERRUPT AT LOAD POINT (11010), 9-TRACK MODE. - The rewind interrupt at load point operation is used only in the 9-track mode. This operation code will initiate a rewind operation to the selected transport and send a status external interrupt word when the tape reaches BOT. This allows the computer to perform other operations not concerned with the rewinding transport but be informed when that transport is ready for other operations.

(38) REWIND READ (111X0). - The rewind read operation code causes the selected transport to perform a rewind and, after reaching BOT, read the first record on tape. A status external interrupt is not sent to the computer until after completion of the read portion of the operation. The rewind read is supplemented by format and density.

(39) REWIND READ, CLEAR WRITE ENABLE. - The rewind read, clear write enable operation is used only in the 1240 and 1540 modes.

(a) 1240 MODE (111X1). - To perform a rewind read, clear write enable while in the 1240 mode, either operation code 11101 or 11111 may be used. Either code will cause the selected transport to rewind, the write enable for that transport will be disabled and the first record on tape will be read. After reading the record, a status external interrupt will be sent to the computer.

(b) 1540 MODE (11101). - The rewind read, clear write enable operation in the 1540 mode is the same as for the 1240 mode except only operation code 11101 will initiate the operation.

(40) REREAD (11101), 9-TRACK MODE. - The reread 9-track operation code will cause the MTS to backspace the tape on the addressed transport one record and then read the record in the forward direction. If the recording mode and density selection are NRZI and 556 or 800 frames per inch, the MTS will perform error correction for a single track error.

(41) REQUEST TRANSPORT STATUS (11111), 1540 MODE or 9-TRACK MODE. - On receiving a request transport status in either the 1540 or 9-track mode, the MTS will send a status external interrupt to the computer with the status of the selected transport.

g. MODULUS SELECT. - The modulus for reading and writing are determined by bit positions 10 and 9 of the external function word for all three modes of operation. These bit positions determine moduli 3 through 6 for 7-track operation and 2 through 5 for 9-track operation. The computer may specify any of the moduli for reading or writing tape. However, when reading a tape written by another system, the computer word size of the other system must be the same as, or less than, the system for which the MTS is reading. Table 4-5 gives the modulus code and word size for both 7 and 9-track operation.

TABLE 4-5. MODULUS CODE

EF BITS		7-TRACK		9-TRACK	
10	9	MODULUS	WORD LENGTH	MODULUS	WORD LENGTH
0	0	3	18-BIT	2	16-BIT
0	1	4	24-BIT	3	27-BIT
1	0	5	30-BIT	4	32-BIT
1	1	6	36-BIT	5	40-BIT*

NOTE: Word lengths are maximum. Computer word size to be equal to or less than modulus selected when writing tapes. Tapes must be read in same modulus as when written.

*Maximum word length of MTS is 36 bits.

(1) 7-TRACK OPERATION. - The following subparagraphs define the moduli for 7-track operation. The bit arrangement on the tape for bioctal recording is shown in figure 4-8 and octal reading in figure 4-9.

(a) MODULUS 3. - Modulus 3 is obtained by reducing 18 bits of a computer word to three (bioctal characters) frames of data. In reading modulus 3 bioctal, a word is sent to the computer for every three characters assembled. The characters are assembled in the lower 18 bits (17-0) of the data word. The upper bits (if any) of the data word contain 0's. When reading octal, six tape frames are read to complete the computer word.

When recording modulus 3 bioctal, the 18 bits of a computer word are recorded in three 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of tape frames is doubled.

(b) MODULUS 4. - Modulus 4 is obtained by reducing 24 bits of a computer word to four (bioctal characters) frames of data. In reading modulus 4 bioctal, a word is sent to the computer for every four characters assembled. The characters are assembled in the lower 24 bits (23-0) of the data word. The upper bits (if any) of the data word contain 0's. When reading octal, eight tape frames are read to complete the computer word.

When recording modulus 4 bioctal, the 24 bits of a computer word are recorded in four 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of tape frames is doubled.

(c) MODULUS 5. - Modulus 5 is obtained by reducing 30 bits of a computer word to five (bioctal characters) frames of data. In reading modulus 5 bioctal, a word is sent to the computer for every five characters assembled. The characters are assembled in the lower 30 bits (29-0) of the data word. The upper bits (if any) of the data word contain 0's. When reading octal, ten frames are read to complete the computer word.

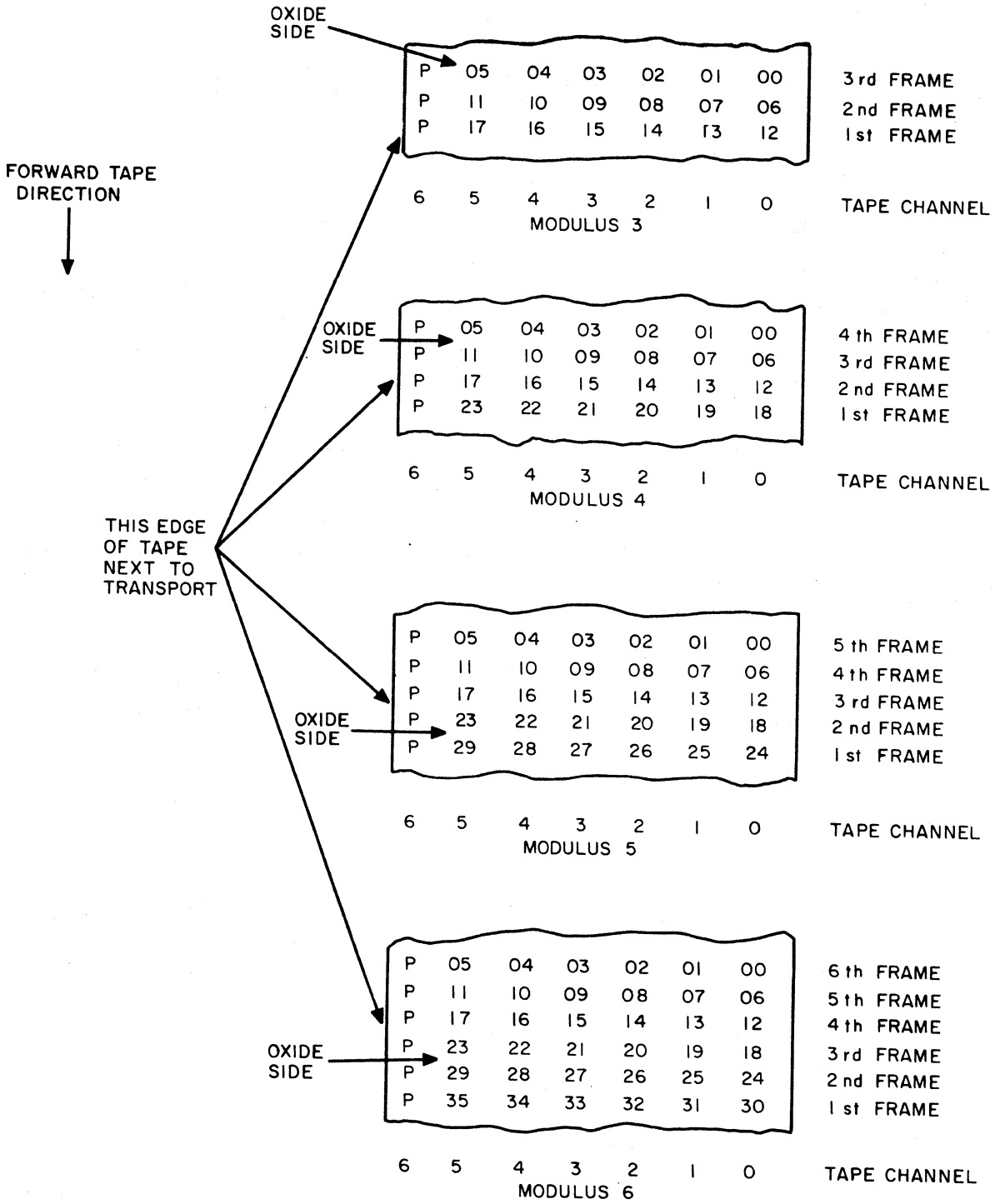


Figure 4-8. Bioctal Tape Formats, 7-Track By Modulus

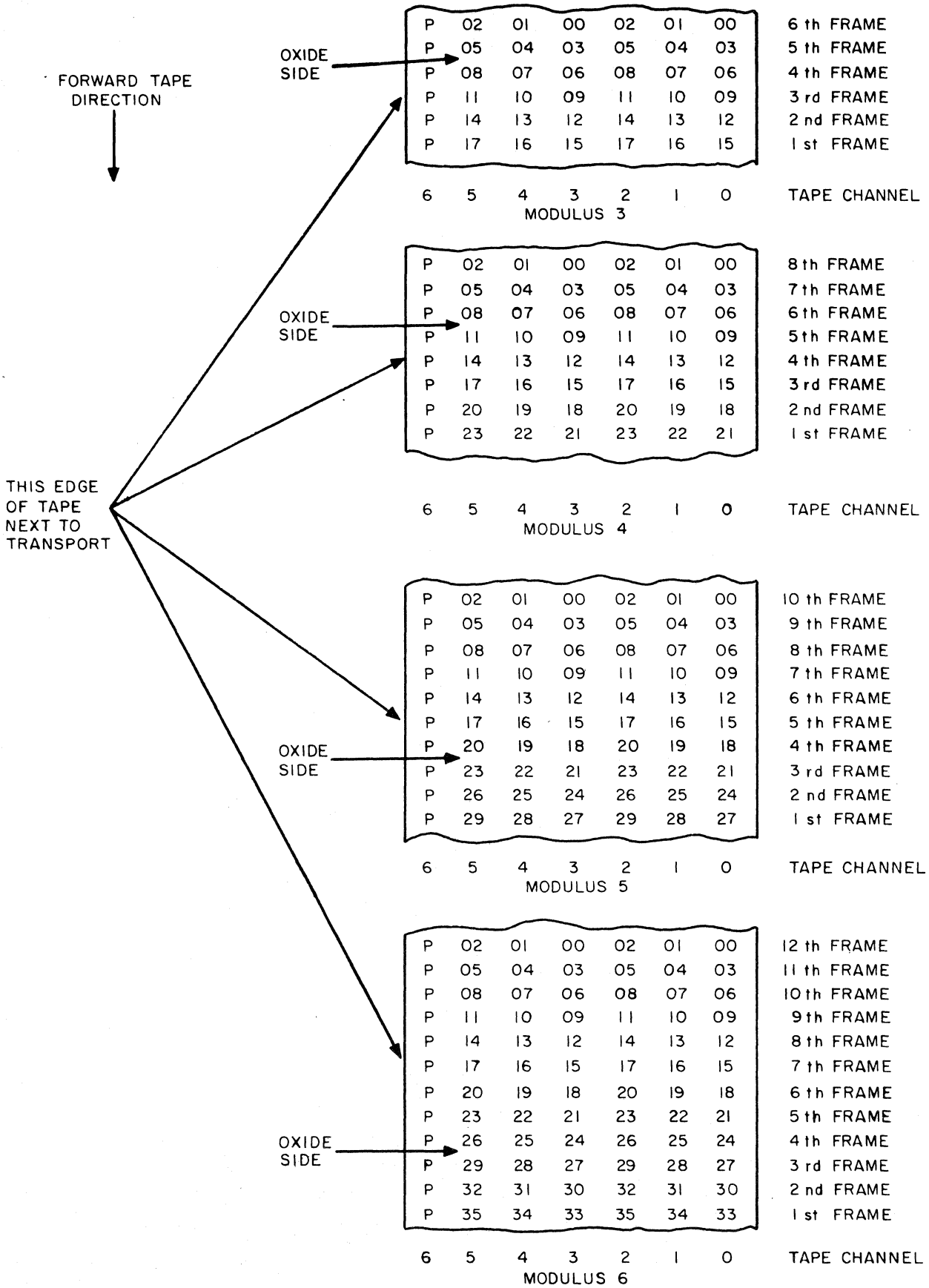


Figure 4-9. Octal Tape Formats, 7-Track By Modulus

When recording modulus 5 bioctal, the 30 bits of a computer word are recorded in five 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of tape frames is doubled.

(d) MODULUS 6. - Modulus 6 is obtained by reducing 36 bits of a computer word to six (bioctal characters) frames of data. In reading modulus 6 bioctal, a word is sent to the computer for every six characters assembled. The characters are assembled in the 36 bits (35-0) of the data word. When reading octal, twelve frames are read to complete the computer word.

When recording modulus 6 bioctal, the 36 bits of a computer word are recorded in six 7-bit frames with each frame consisting of a 6-bit character plus parity. For octal recording, the number of frames is doubled.

(2) 9-TRACK OPERATION. - The following subparagraphs define the moduli for 9-track operation. The bit arrangements on the tape for nonredundant recording is shown in figure 4-10. No redundant recording is performed in 9-track operation.

(a) MODULUS 2. - Modulus 2 is obtained by reducing 16 bits of a computer word to two 8-bit frames of data. In reading modulus 2, a word is sent to the computer for every two frames of data assembled. The two frames are assembled in the lower 16 bits (15-0) of the data word. The upper bits (if any) of the data word contain 0's.

When recording modulus 2, the 16 bits of a computer word are recorded in two 9-bit frames with each frame consisting of an 8-bit character plus parity.

(b) MODULUS 3. - Modulus 3 is obtained by reducing 24 bits of a computer word to three 8-bit frames of data. In reading modulus 3, a word is sent to the computer for every three frames of data assembled. The three frames are assembled in the lower 24 bits (23-0) of the data word. The upper bits (if any) of the data word contain 0's.

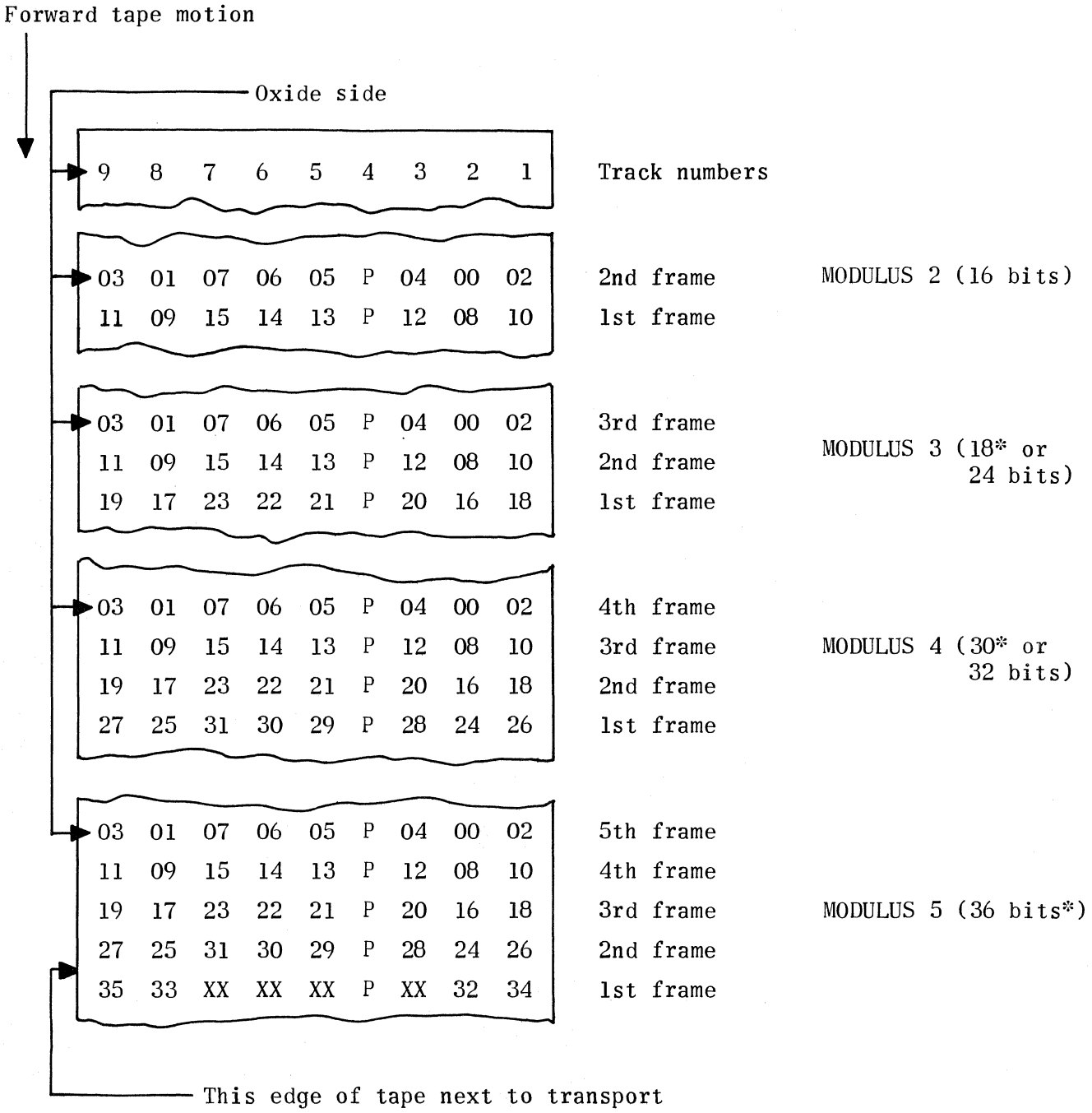
When recording modulus 3, the 24 bits of a computer word are recorded in three 9-bit frames with each frame consisting of an 8-bit character plus parity.

(c) MODULUS 4. - Modulus 4 is obtained by reducing 32 bits of a computer word to four 8-bit frames of data. In reading modulus 4, a word is sent to the computer for every four frames of data assembled. The four frames are assembled in the lower 32 bits (31-0) of the data word. The upper bits (if any) of the data word contain 0's.

When recording modulus 4, the 32 bits of a computer word are recorded in four 9-bit frames with each frame consisting of an 8-bit character plus parity.

(d) MODULUS 5. - Modulus 5 is obtained by reducing 40 bits of a computer word to five 8-bit frames of data. The maximum word length for the MTS is 36 bits. Therefore, a 36-bit computer word will be recorded on tape with the upper four bits recorded as 0's. In reading modulus 5, a 36-bit word is sent to the computer for every five frames of data assembled.

When recording modulus 5, the 36 bits of a computer word are recorded in five 9-bit frames with each frame consisting of an 8-bit character plus parity.



*MTS writes zeros in bit positions not provided by the computer interface (i.e., bits 23 - 18 will be zeros in Modulus 3 with 18-bit interface; bits 31 and 30 will be zeros in Modulus 4 with a 30-bit interface).

Figure 4-10. Recording, 9-Track By Modulus

h. OCTAL/BIOCTAL, 1240 MODE or 1540 MODE. - Two types of character recording can be designated in either the 1240 or 1540 mode of operation, octal, and bioctal. Bit 8 of the EF word being a 1 causes each octal number in the computer word to be recorded twice in the same frame for added reliability. For instance, if the computer word contained octal 01234 56701, it would appear on tape as shown in figure 4-11. Note that when recording octally, a 0 is recorded as 0 111 000. When recording octally, the parity designator is ignored and odd parity is always generated. When read, the two halves of each frame are combined in an OR type function so that if a 1 bit has been dropped on one half of the tape, it may be recovered from the other half.

A 0 in bit 8 causes two octal numbers (six bits) of the computer word to be recorded in each frame. The parity designated may be either odd or even.

i. 9-TRACK RECORDING. - Character recording in the 9-track mode is performed only in the nonredundant mode. Figure 4-12 shows a sample of 9-track recording using a 32-bit computer word.

j. LATERAL PARITY, 1240 MODE or 1540 MODE. - When reading or recording in either the 1240 or 1540 mode of operation, bit 7 of the EF words designates the parity of the characters. Bit 7 being a 1 designates odd parity and a 0 designates even parity. When reading or recording in the octal format, the MTS automatically selects odd parity and the parity bit of the EF word is ignored.

When recording in the bioctal format, either odd or even parity may be specified. However, when recording in bioctal format with even parity, exercise care to ensure that no more than two sequential zero frames are recorded. Exceeding two zero frames causes the MTS to generate frame count errors or an end-of-record indication. If zero data frames are liable to be recorded, odd parity should be used to ensure against a false end-of-record or frame count errors.

k. NRZI/PE, 9-TRACK MODE. - When reading or recording in 9-track, bit 7 of the EF word specifies either the NRZI or PE mode. Bit 7 as a 1 specifies PE recording/reading and as a 0 specifies NRZI. The MTS will interpret this bit only when the tape is at BOT and the EF word specifies a write operation. For subsequent operations, the mode selection is stored for each transport. The method in which data was recorded will determine the mode when a read operation is specified.

l. DENSITY SELECTION. - The density at which data is read or recorded is specified by bit 6 (1240 mode) or bits 6 and 5 of the EF word, with one exception, in the 9-track mode. This exception is defined in the paragraph 4-41(3).

(1) 1240 MODE. - In the 1240 mode of operation, the MTS is capable of recording and reading in either of two densities as specified by bit 6 of the EF instruction word. When bit 6 is a 1 a density of 556 fpi is used and when a 0 a density of 200 fpi. The density of 556 fpi is referred to as high density and 200 fpi is referred to as low density.

(2) 1540 MODE. - In the 1540 mode of operation, the MTS is capable of recording/reading data in any of three densities as specified by bits 6 and 5 of the EF word. These densities are as follows:

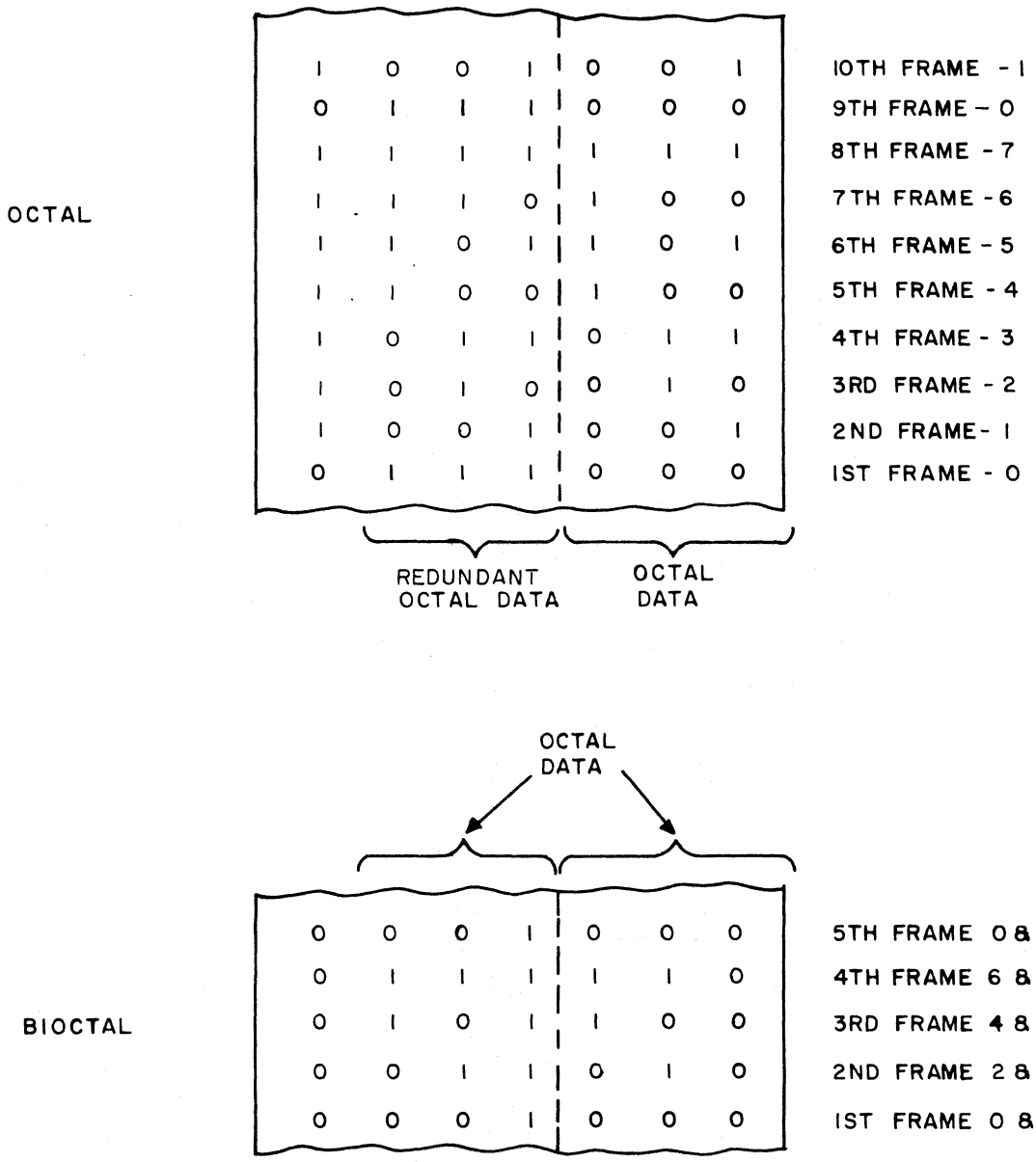


Figure 4-11. Octal and Bioctal Recording Examples

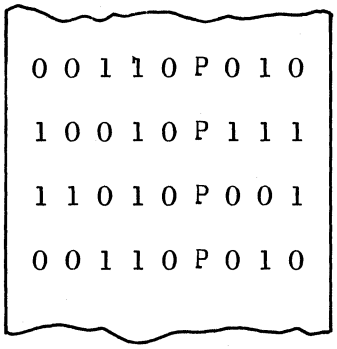


Figure 4-12. 9-Track Recording Example

BITS 6	5	DENSITY
0	0	200 fpi
1	0	556 fpi
0	1	800 fpi
1	1	same as last instruction

(3) 9-TRACK MODE. - In the 9-track mode of operation, the MTS is capable of recording/reading data in any of four densities. When bit 7 is a 0, the recording will be NRZI and bits 6 and 5 will determine the density in the same codes as for the 1540 mode. When bit 7 is a 1, bits 6 and 5 are ignored and the recording density will be 1600 fpi PE.

m. TRANSPORT SELECTION. - There are three methods of addressing transports in the MTS. How an individual transport is selected is dependent on the mode of operation being used. The following paragraphs describe each method of selection.

(1) 1240 MODE. - In the 1240 mode of operation, individual transport selection is initiated by an EF word with bit 17 a 1 the transport code in the lower six bits, and all other bits a 0. This is defined as an address word. Figure 4-3 shows the address word format. Also given in figure 4-3, is the conversion between 1240 addressing terminology and the addressing of a transport in the MTS. The setting of an individual transport ADDRESS switch will designate the associated transport as having that program address. This allows using present 1240 programs with

transport addresses higher than four. As an example, if the operational computer specifies transport 14 and the MAG TAPE 1 ADDRESS switch is set to 14, the associated transport will be selected to perform the desired operation.

(2) 1540 MODE. - In the 1540 mode of operation, individual transport selection is controlled by bits 4 through 0 of an EF word. The first EF word must specify the transport by which the operation is to be performed. When consecutive operations are to be performed by the same transport, the first EF word specifies the transport and succeeding EF words may contain either the transport address or have 0's in bits 2 through 0. These lower three bits containing 0's specify that the last transport selected is to perform the operation specified by the EF word. Figure 4-5 gives the conversion between 1540 type addressing and the settings of the transport ADDRESS switches. As an example, if the computer operational program specifies transport 8 and the MAG TAPE 1 ADDRESS switch is set to 8, the associated transport will be selected to perform the desired operation. If the next operation to be performed by the MTS is to be done by the same transport, the EF word may contain 0's in the lower three bits instead of the actual transport address.

(3) 9-TRACK MODE. - In the 9-track mode of operation, bits 3 and 2 of the EF word are used to select a transport for operation. Each time an EF word is transmitted to the MTS a transport must be specified. Which transport actually performs the operation specified, is dependent on the settings of the individual ADDRESS switches and the code sent. The codes for transport selection are given in figure 4-6. Any transport whose associated ADDRESS switch is set to a number higher than 4 cannot be selected by the computer program.

n. DUPLEX CONTROL. - The MTS is capable of operation under control of two computers (duplexed) in only the 1540 or 9-track modes. The description of the control selection is given in the following paragraphs. Table 4-6 gives the duplex control codes for both modes of operation. Except for different bits of each mode being used, the operation under duplex control is the same.

(1) NON-DUPLEX OPERATION. - The non-duplex control code is the only one that permits a tape operation to be initiated and is used after a computer has gained control. When a computer initiating the non-duplex operation has previously established control, the MTS accepts the EF word and performs the specified operation. If the computer initiating the non-duplex operation is not in duplex control, the MTS will generate status external interrupt to the non-controlling computer with a not-in-control indication.

(2) RELEASE CONTROL. - When the controlling computer sends an EF word with the release duplex control code, the MTS will remove the controlling computer from control after the current operation is completed. If the computer not in control sends a release duplex control code, the MTS will not respond to the request.

(3) REQUEST CONTROL. - When neither computer is in duplex control, the MTS, on receiving a request duplex control code in an EF word, will place the requesting computer in control. The MTS then issues a status external interrupt with an in-control indication. This notifies the computer that it has established control. If the computer initiating the request duplex control is already in control, the MTS issues a status external interrupt to that computer notifying it that it is in control. The MTS then continues operation with that computer. If one computer requests control and the other computer is in control, the MTS stores the request for

TABLE 4-6. DUPLEX CONTROL CODES

1540 MODE EF BITS		9-TRACK MODE EF BITS		FUNCTION
17	16	1	0	
0	0	0	0	Non-duplex
0	1	0	1	Release Duplex Control
1	0	1	0	Request Duplex Control
1	1	1	1	Demand Duplex Control

control until the other computer releases control. After control is released, the MTS places the first computer in control and notifies it by way of a status external interrupt with an in-control indication.

(4) DEMAND CONTROL. - When one computer has control and the other computer requires the MTS immediately, the second computer may gain control by sending an EF word with the demand duplex control code. Sending this code will master clear the MTS, thus stopping all operation. The second computer is placed in control and the first computer is sent a status external interrupt with a not-in-control (lost control) indication. No interrupt is sent to the computer now placed in control. If neither computer is in control when a demand is received, the MTS places the demanding computer in control. No interrupt is issued to either computer. Issurance of a demand control code by a computer in control is, in effect an EF master clear.

o. TRANSMIT EXTRA. - The transmit extra is a special EF code used only in the 1240 and 1540 modes of operation. The transmit extra function can only be performed after using a forward read. When reading a tape in a modulus other than the one in which it was recorded, the number of frames read may not form an integral number of computer words. When this occurs, the extra frames of data remain stored in the MTS. A status external interrupt is generated to the computer with the incorrect frame count indication but with no longitudinal parity error indication. The computer may then send an EF word with bits 17 and 6 set to 1's which requests the extra frames of data. The MTS responds by sending a computer word of the length specified by the modulus in which the tape was read. The lower six bits of the word will contain a code which indicates, by a 1 bit-position coded, the frames containing no data. Figure 4-13 gives the format for transmit extra data words.

4-5. STATUS/EXTERNAL INTERRUPT WORD FORMATS.

There are three status external interrupt word formats used by the MTS. The format used at any given time is dependent on the mode of operation. Figure 4-14 shows the 1240 mode format; figure 4-15 the 1540 mode format; and figure 4-16 the 9-track mode format. In the following paragraphs differences in bit position usage will be indicated, where they exist. When operation is in the 1240 mode, two bits are always set, the bit indicated in the following paragraphs and the bit 15-bit positions displayed, as shown in figure 4-14.

A status word is sent to the computer following the completion of most functions specified by an operation code. It is placed on the data lines of the computer input cable. The bit structure of the status word enables the computer to determine whether or not the previous operation has been successfully completed.

Modulus Number	No. of Extra Characters	35 - 30	29 - 24	23 - 18	17 - 12	11 - 6	5 - 0
6	1	ZZZZZZ	------	------	------	------	011111
6	2	YYYYYY	ZZZZZZ	------	------	------	001111
6	3	XXXXXX	YYYYYY	ZZZZZZ	------	------	000111
6	4	WWWWWW	XXXXXX	YYYYYY	ZZZZZZ	------	000011
6	5	VVVVVV	WWWWWWW	XXXXXX	YYYYYY	ZZZZZZ	000001
5	1		ZZZZZZ	------	------	------	001111
5	2		YYYYYY	ZZZZZZ	------	------	000111
5	3		XXXXXX	YYYYYY	ZZZZZZ	------	000011
5	4		WWWWWW	XXXXXX	YYYYYY	ZZZZZZ	000001
4	1			ZZZZZZ	------	------	000111
4	2			YYYYYY	ZZZZZZ	------	000011
4	3			XXXXXX	YYYYYY	ZZZZZZ	000001
3	1				ZZZZZZ	------	000011
3	2				YYYYYY	ZZZZZZ	000001

Extra characters; Z indicates bit positions used for last character read, Y indicates bit position used for next to last character read, etc. Dashes indicate bits not to be interpreted.

Corresponds to bit positions 35 - 30, always "0".

Corresponds to bit positions 29 - 24
"1" denotes no data

Corresponds to bit positions 23 - 18
"1" denotes no data

Corresponds to bit positions 17 - 12
"1" denotes no data

Corresponds to bit positions 11 -6
"1" denotes no data

"0" denotes that original transmission was a complete word. "1" denotes no data in positions 5-0.

Figure 4-13. Transmit Extra Data Word Formats

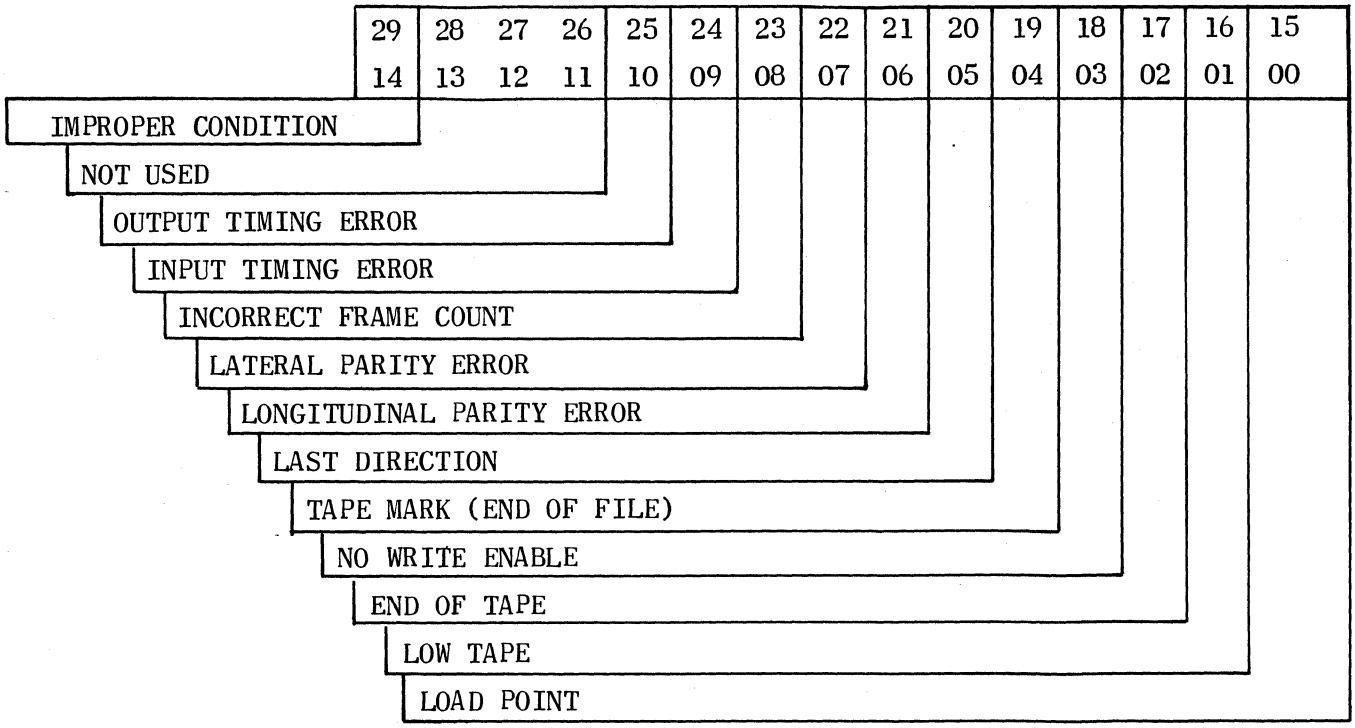


Figure 4-14. 1240 Status Word Format

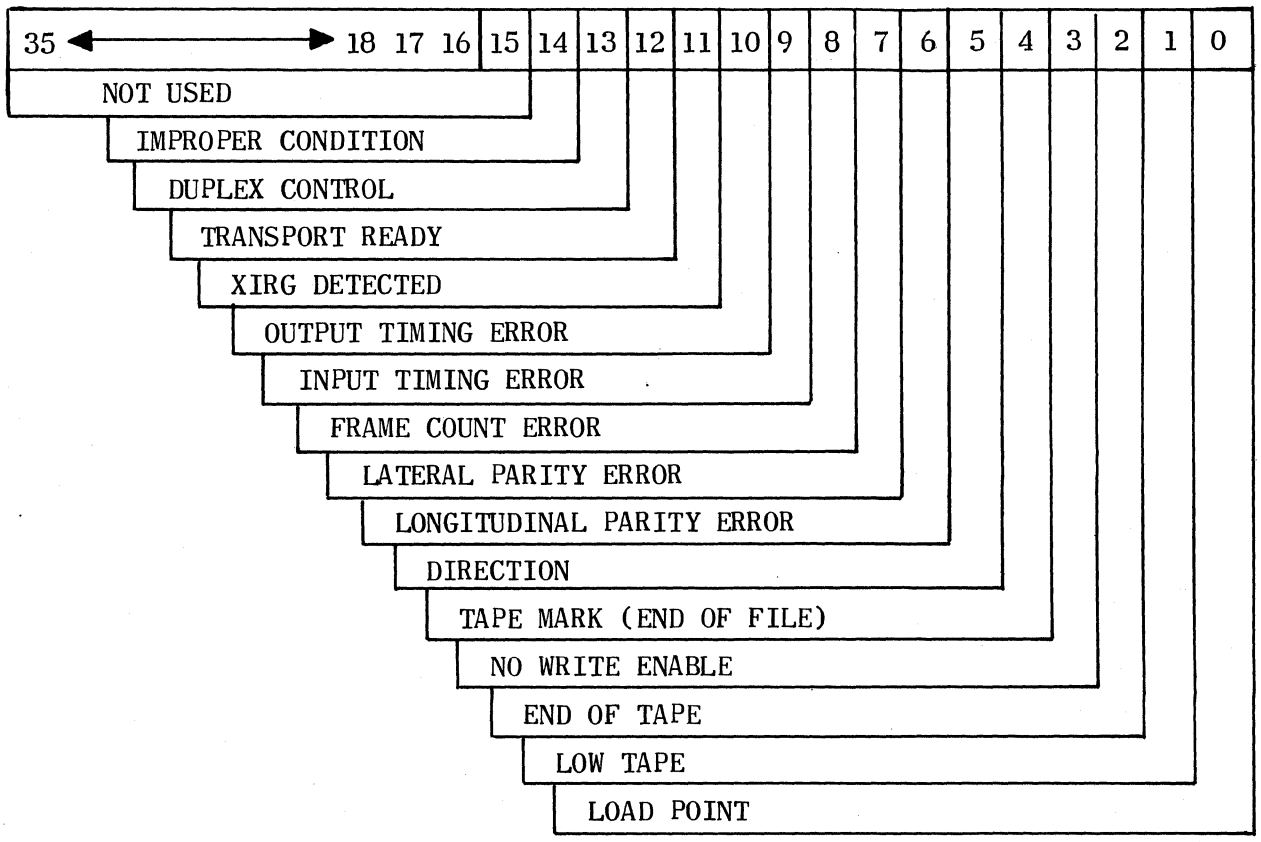


Figure 4-15. 1540 Status Word Format

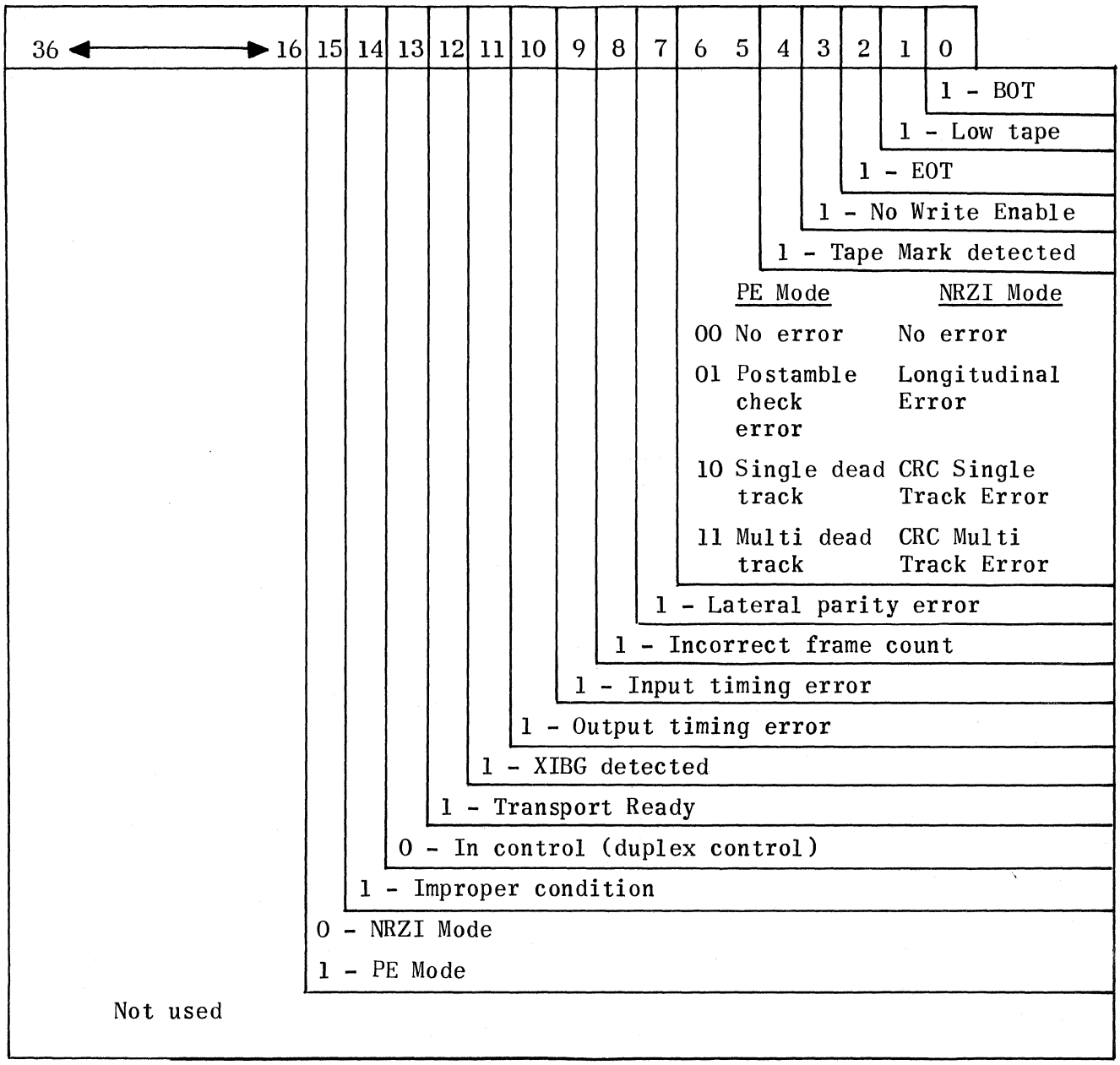


Figure 4-16. 9-Track Status Word Format

a. BOT/LOAD POINT (Bit 0 = 1). - Whenever an operation is terminated with the tape positioned at the load point (BOT) marker, bit 0 in the status word will be a 1. This bit will also be a 1 when an operation requesting reverse motion of tape is attempted with the tape at BOT.

b. LOW TAPE (Bit 1 = 1). - Whenever an operation is terminated with less than 100 feet of tape remaining on the supply reel, bit 1 of the status word will be a 1.

c. END OF TAPE (EOT) (Bit 2 = 1). - Whenever an operation is terminated with the record/read head positioned at or beyond the EOT marker, bit 2 of the status word will be a 1.

d. NO WRITE ENABLE (Bit 3 = 1). - Whenever a write (all modes) or erase (9-track mode only) operation is attempted and either the Write Enable Ring is not installed or the WRITE ENABLE indicator is extinguished, bit 3 of the status word will be a 1.

e. TAPE MARK (Bit 4 = 1). - Whenever a tape mark is detected during a read, write tape mark, space file, or search file operation, bit 4 of the status word will be a 1.

f. LAST DIRECTION (Bit 5), 1240 MODE or 1540 MODE. - In the 1240 and 1540 modes of operation, bit 5 of the status word is used to indicate the last direction of tape movement. Bit 5 is a 0 when the last tape movement was forward and a 1 when the direction was reverse.

g. LONGITUDINAL PARITY ERROR (Bit 6 = 1), 1240 MODE or 1540 MODE. - When recording, longitudinal parity is generated by the MTS for each tape channel and is recorded after the three frames of zeros past the last data frame. When performing read-type operations, the longitudinal parity of a record is checked by the MTS and, if an error is indicated, bit 6 of the status word will be a 1.

NOTE

Some errors which may occur during a read or write operation are recoverable errors. Normally two same-direction reads of the record in error will obtain the correct data during a read operation. An error during a write operation may be caused by a bad spot on tape. If the first write retry does not result in a good record, successive tries with a Write XIRG should be used to space past a possible bad spot on tape.

h. 9-TRACK ERRORS (Bits 5 and 6). - In the 9-track mode of operation, the four possible combinations of bits 6 and 5 of the status word are used to signify either no error or a specific error. The type of error is determined by the method used in recording the data. When bits 6 and 5 are both 0's, no error was detected. The following paragraphs define the other combinations of bits 6 and 5 by recording method.

(1) NRZI MODE. - When reading 9-track NRZI recorded data three types of errors may be detected: longitudinal error; CRC single track error; or CRC multi-track error.

(a) LONGITUDINAL ERROR. - Whenever the MTS detects a longitudinal error during an NRZI read operation, the status word sent to the computer will have bit 6 a 0 and bit 5 a 1. This indicates that the longitudinal parity of at least one track did not agree when the longitudinal parity check was performed.

(b) CRC SINGLE TRACK ERROR. - Whenever the MTS detects a CRC single track error during an NRZI read operation, the status word to the computer will have bit 6 a 1 and bit 5 a 0. This indicates that an error was detected in one track when the cyclic redundancy check was performed.

(c) CRC MULTI TRACK ERROR. - Whenever the MTS detects a CRC multi-track error during a NRZI read operation, the status word to the computer will have bit 6 a 1 and bit 5 a 1. This indicates that an error was detected in two or more tracks when the cyclic redundancy check was performed.

(2) PE MODE. - When reading 9-track PE recorded data three types of errors may be detected: postamble check error; single dead track error, or multi dead track error.

(a) POSTAMBLE CHECK ERROR. - Whenever the MTS detects a postamble check error during a PE read operation, the status word to the computer will have bit 6 a 0 and bit 5 a 1. This indicates that the phase of the postamble check region does not agree with the phase of the preamble check region.

(b) SINGLE DEAD TRACK. - Whenever the MTS detects an error or errors in one track during a PE read operation, the status word to the computer will have bit 6 a 1 and bit 5 a 0. This indicates that the track with errors is considered a dead track and a reread operation should be performed for error correction by the MTS.

(c) MULTI DEAD TRACK. - Whenever the MTS detects errors in more than one track during a PE read operation, the status word to the computer will have bit 6 a 1 and bit 5 a 1. This indicates that the tracks with errors are considered dead tracks. No error correction may be performed for multi dead track errors.

i. LATERAL PARITY ERROR (Bit 7 = 1). - Bit 7 of the status word to the computer will be a 1 when the MTS detects that the parity of a frame read does not agree with the specified parity. A lateral parity error indication will also inform the computer that it did not receive the complete record in which the error occurred unless the operation included the ignore-error-halt command. When the error is detected without ignore-error-halt, the read operation is stopped and the tape is spaced to the IRG following the record.

j. INCORRECT FRAME COUNT (Bit 8 = 1). - Bit 8 of the status word to the computer will be a 1 when the last frames of data read did not form a complete computer word as specified by the modulus. This indication may result from one or more of the following conditions.

1) One or more frames were not properly read or recorded.

2) Bad spots on tape causing frames to be lost.

3) The record was read in the wrong modulus (i.e., reading a record in modulus 3 which was recorded in modulus 4).

If the cause was lost frames, a longitudinal parity error will usually be indicated also.

k. INPUT TIMING ERROR (Bit 9 = 1). - Bit 9 of the status word to the computer will be a 1 if the computer fails to accept data from the MTS at the rate determined by the recorded density and modulus. When an input timing error occurs, the MTS stops input data transfers to the computer, moves tape to the end of the record and then interrupts the computer with status.

l. OUTPUT TIMING ERROR (Bit 10 = 1). - Bit 10 of the status word to the computer will be a 1 if one of the following has occurred.

1) The first data word from the computer failed to arrive in time to be written in the specified modulus and density during a write operation.

2) A word after the first which failed to arrive in time to be written in its proper place as specified by modulus and density but arrives before the MTS generates a status external interrupt to the computer. When the data does not arrive in time, the MTS assumes an end of record condition.

3) A selective read code or search key from the computer failed to arrive in time to be compared to the first data read from tape during a selective read, search or backsearch operation.

m. XIRG DETECTED (Bit 11 = 1) - 1540 MODE or 9-TRACK MODE. - Bit 11 of the status word is not used in the 1240 mode of operation. In the 1540 and 9-track modes of operation, bit 11 of the status word will be a 1 when the MTS moves tape two inches without detecting the start of a record except when starting from BOT.

n. TRANSPORT READY (Bit 12 = 1) - 1540 MODE or 9-TRACK MODE. - Bit 12 of the status word is not used in the 1240 mode of operation. In the 1540 and 9-track modes of operation, bit 12 of the status word will be a 1 when all of the following transport conditions exist.

1) Power is on.

2) Vacuum is on.

3) Tape reel is installed and tape is properly loaded and threaded.

o. DUPLEX CONTROL (Bit 13) - 1540 MODE or 9-TRACK MODE. - Bit 13 of the status word is not used in the 1240 mode of operation as this mode has no duplex capability. In the 1540 and 9-track modes of operation, bit 13 of the status word is used to indicate whether or not a computer has control of the MTS. Bit 13 of the status word being a 0, indicates to the receiving computer that it has control. When bit 13 is a 1, the receiving computer is notified that it does not have control.

p. IMPROPER CONDITION (Bit 14 = 1). - Bit 14 of the status word to the computer is a 1 when one or more of the following conditions exists.

1) The selected transport is not in an automatic condition. The MAN/AUTO switch is in the MAN position or the transport is not ready.

2) The power is out of tolerance.

3) A command requiring forward tape movement is sent to the MTS with the selected transport tape at EOT.

4) A command requiring reverse tape movement, other than any of the rewind commands, is sent to the MTS with the selected transport tape at BOT.

5) A command requiring a write or erase operation is sent to the MTS and the selected transport has no write enable.

The MTS will clear the improper condition when the computer sends an external function word and the improper condition has ceased to exist.

q. NRZI/PE MODE (Bit 15) - 9-TRACK MODE. - Bit 15 of the status word is only used in the 9-track mode of operation and indicates the last recording mode. If the last recording mode was NRZI, bit 15 will be a 0. If the last recording mode was PE, bit 15 will be a 1.

4-6. FUNCTIONAL BLOCK DIAGRAM DESCRIPTION.

The following paragraphs describe the major logic sections that comprise the controller portion of the MTS and the main function or functions each logic section performs. The descriptions are referenced to the functional block diagram in figure 4-17.

a. MTS/COMPUTER INTERFACE. - The MTS/computer interface is composed of data and control lines as listed below. The MTS communicates with a computer via input and output connectors located at the top, rear of the cabinet. One pair of connectors is for computer A and the other for computer B. An identical set of communication lines is terminated at each pair of connectors. The lines are:

1) 36 computer input data lines for transmitting data and status words to a computer.

2) 36 computer output data lines for receiving data and external function words from a computer.

3) Four computer input control lines for transmitting external function, external interrupt, input data and output data request signals to a computer.

4) Three computer output control lines for receiving external function, input data and output data acknowledge signals from a computer.

All data and control signals between the MTS controller and computer are transmitted through line drivers and receivers via twisted-pair lines. The computer input data lines, except for computer B data bit 13, originate and the output data lines terminate at the cards located in the controller card rack positions 1A-6A. The MTS/computer control lines and computer B input data bit 13 originate or terminate at the card located in card rack position 7A. Each of the cards used in the MTS/computer interface are a combination of line drivers and receivers. Six bits of the MTS/computer data interface are contained on each data interface card. The lower six bits (5-0) are on the card at location 1A and the upper six bits (35-30) are on the card at location 6A.

b. CONTROLLER/TRANSPORT INTERFACE. - The controller/transport interface is composed of the following data and control lines.

1) Nine write data lines (including parity) to each transport (only seven lines are used for 7-track operation).

2) One erase line to each transport (used in 9-track operation only).

3) Four control signals to each transport (Write, Forward, Reverse and Fast).

4) Nine read data lines (including parity) to each transport (only seven lines are used for 7-track operation).

5) Six control/status lines from each transport (Write Ring, EOT, BOT, Ready, Capstan 0 and Low Tape).

All data and control signals transmitted between the controller and a transport are via twisted-pair lines. The control signals to a transport originate at the card located in A8 (TT1), A9 (TT2), A10 (TT3), or A11 (TT4). The write ring, EOT, and BOT signals from the transports terminate in the same associated card. The ready, capstan 0, and low tape status signals from each transport all terminate in the card located at B7. The read data signals from the transports terminate at the card located in A31 (TT1), A32 (TT4), A33 (TT2), or A34 (TT3). The write data signals to the transports originate at the cards located in locations A13 through A17. The erase and track 0 signals originate at A13 and the track 7 and track 8 signals originate at A17.

c. DUPLEX CONTROL. - The duplex control logic provides the MTS with the ability to operate with two computers in the duplex mode (duplexing not used in 1240 mode of operation). In duplex operation, two computers may be connected to the MTS but only one computer at a time can have control over the MTS. The duplex control logic allows a computer's control request (request control, release control or demand control) to be processed by the MPC portion of the MTS. The processing by the MPC determines whether or not a request by a computer will be acted on at the time. Selection of a computer and/or responding to a request is based on three conditions: the computer's responses to the controller generated external function request, the MTS status when it receives the responses, and the type of response from each computer. The duplex control logic is contained on the card at location B6.

d. I/O CONTROL. - The I/O control (request/acknowledge control) logic is composed of circuits that generate and transmit request signals to the computer and circuits that receive and initially process acknowledge signals from the computer. The request signals are generated as a result of MPC control signals. The MPC performs the final processing of acknowledge signals to determine the next sequence of events. The circuits include the following:

1) External function request - When the MPC portion of the MTS determines that no operation is requested, the Busy control is cleared. This notifies the computer, via an external function request, of the MTS ability to accept and process an external function word.

2) External function acknowledge - The external function acknowledge circuit consists of two flip-flops. The first flip-flop stores the acknowledge from the computer and its set output is gated into the acknowledge flip-flop. The output of the acknowledge flip-flop notifies the MPC that an external function acknowledge was received and is to be acted on.

3) Output data request - Flip-flop set by the MPC to notify the computer that the MTS is ready to receive and process data.

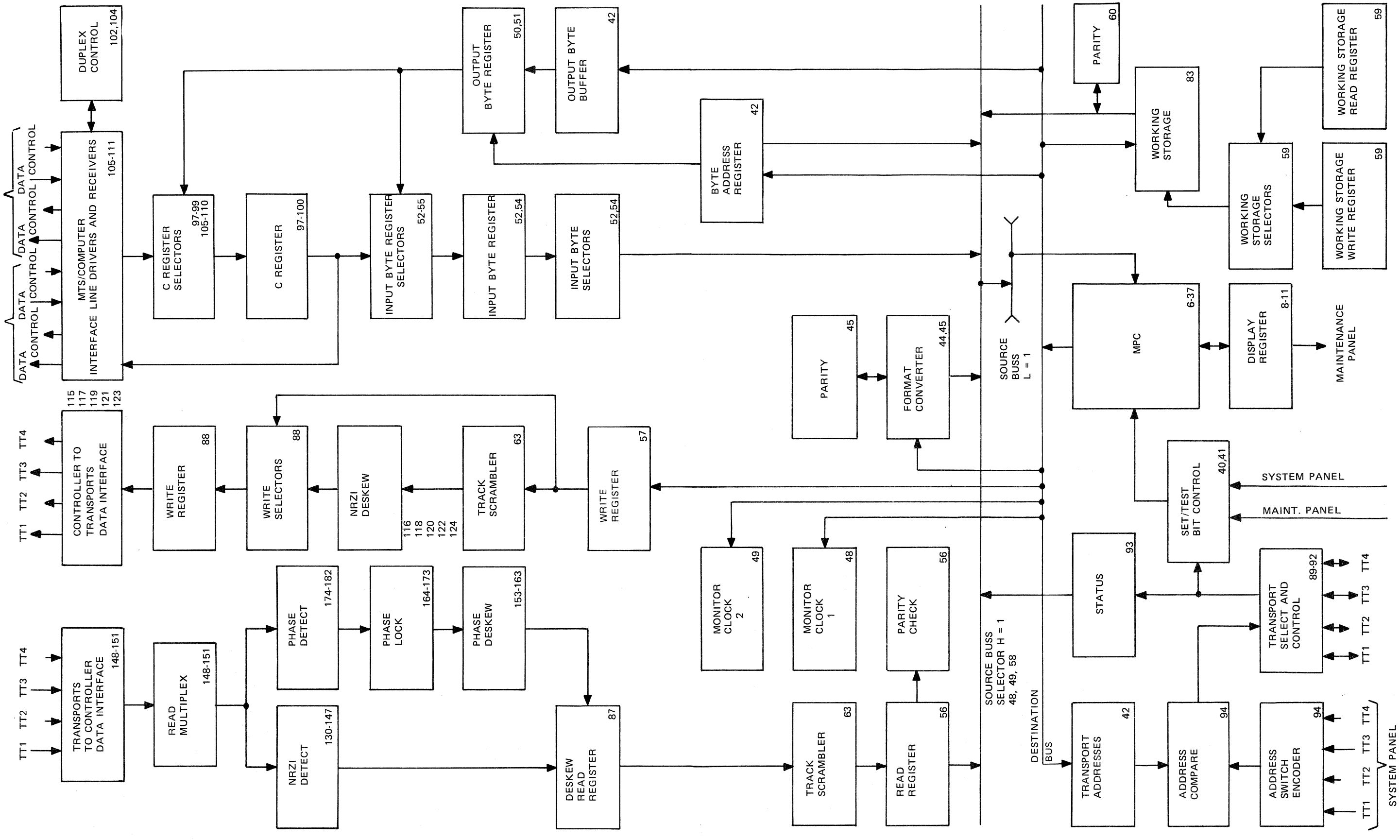


Figure 4-17. MTS Functional Block Diagram

4) Output acknowledge - Two flip-flops, operating as a step chain, to accept the output data acknowledge from the computer, transfer the incoming data into the C register and clear the output data request flip-flop.

5) Input data request - Flip-flop set after the output byte register is loaded to notify the computer that the MTS has data ready for transmission.

6) Input acknowledge - Three flip-flops, operating as a stepping chain, to accept input acknowledge signals from the computer, clear the input data request (or external interrupt request) to the computer, and inform the MPC that the acknowledge was received.

7) External interrupt request - Flip-flop set by the MPC to notify the computer that the MTS has a status word ready for transmission.

The output data request, output acknowledge and external function acknowledge circuits are on the card at location B5. The input data request and external interrupt request circuits are on the card at location A12. The external function request (idle/busy store circuit) is on the card at location B11. The input acknowledge circuits are on the card at location B6.

e. I/O SELECTORS. - The I/O selector circuits are quad multiplexers used to gate data from either the controlling computer or the output byte register into the C register. The particular data to be gated is governed by the type of operation being performed by the MTS. The I/O selectors are located on the following cards:

BITS	CARD LOCATION
0, 1, 6 and 7	B1
16, 17, 18 and 19	B2
24, 25, 30 and 31	B3
2, 3, 4 and 5	A1
8, 9, 10 and 11	A2
12, 13, 14 and 15	A3
20, 21, 22 and 23	A4
26, 27, 28 and 29	A5
32, 33, 34 and 35	A6

f. C REGISTER. - The C (I/O) register is a temporary storage register for all information received from and transmitted to the computer. Data and control words received from the computer enter the register via the MTS controller line receivers and I/O selectors. From the C register all words (control or data) from the computer are transferred into the input byte register via the input byte register selectors for processing by the MPC. Data and status words being transferred to the computer enter the C register via the I/O selectors from the output byte register and are transmitted via the line drivers. The C register is contained on cards at locations B1 through B4.

g. INPUT BYTE REGISTER SELECTORS. - The input byte register selectors consist of quad multiplexer circuits used, under MPC program control, to transfer either the C register or output byte register contents into the input byte register. The selectors are on cards at location B16 and B17 of the MTS controller logic section.

h. INPUT BYTE REGISTER. - The input byte register is used as a temporary storage for data and control words. During search operations, the search identifier is stored in the input byte register. Under MPC program control, a word stored in the input byte register is disassembled either for writing on tape or for interpretation. When the word stored is an external function word, the MPC interprets each byte of the word for the operation to be performed, the transport and the format. During search operations, the first (or last) word of each record is compared, byte by byte, with the contents of the input byte register.

The input byte register is on cards at locations B16 and B17. The even numbered data bits are on the card at B16 and the odd numbered bits are on the card at B17.

i. INPUT BYTE SELECTORS. - The input byte selectors consist of multiplexers which, under MPC program control, transfer a selected 6-bit (7-track) or 8-bit (9-track) byte from the input byte register to a destination determined by a program instruction. The particular byte being transferred is selected by the contents of the byte address register.

The input byte selectors are on cards at locations B16 and B17 with the even bits on B16 and the odd bits on B17.

j. SOURCE BUS SELECTOR. - The source bus selector consists of multiplexers which, under MPC program control, selects the information to be placed on the source bus to the MPC. The source of the information placed on the source bus is determined by the contents of the S field of the program instruction. When the S field contains any number 0 through 7, the source bus selector will place information on the source bus. The source bus selector is on the cards at locations B27 and B28.

k. OUTPUT BYTE BUFFER. - The output byte buffer is an 8-bit temporary storage for transferring the information placed on the destination bus to the output byte register. The byte position of the output byte register, into which the output byte contents is transferred, is controlled by the contents of the byte address register. The output byte buffer is on the card at location B13.

l. OUTPUT BYTE REGISTER. - The output byte register assembles the data from the output byte buffer into words. The number of bytes necessary to form a complete word is specified by the modulus of the current operation. When transferring a byte from the output byte buffer to the output byte register, the contents of the byte address register is decoded and specifies which position in the word the current byte is to be placed. All transfer from the output byte buffer to the output byte register is in 8-bit bytes. In 7-track operation, only six bits of the 8-bit byte have data and the upper two bits have no significance. When a transfer is made from the output byte register to either the I/O selectors or the C register during 7-track operation, each byte is essentially shifted the proper number of places to pack the word. For example, using modulus 3 (three bytes make a word), the lower order byte is not shifted, the next order byte is shifted two places, and the last (third) byte is shifted four places. This process eliminates the six insignificant bits (of the 24 bits in the output byte register) and transfers the 18 bits of data. The output byte register is on the card at location B9.

m. FORMAT CONVERTER. - The format converter is used only in 7-track operation for octal (redundant) reading and recording. An MPC instruction is used to select the format converter as a destination and a following instruction selects it as a

source. When writing data on tape, the format converter takes a 6-bit byte and converts it into two 6-bit bytes. One of the converted bytes will contain the lower three bits of the original byte recorded in both the lower and upper three data positions. The other converted byte will contain the upper three bits of the original byte similarly recorded. When reading data from tape, the format converter takes two 6-bits of frame data and converts them back into one 6-bit byte of a computer word. The format converter is on the card at location B21.

n. BYTE ADDRESS REGISTER. - The byte address register is a 4-bit register used to select the position either of the input byte register, from which a byte is to be sampled, or of the output byte register to which a byte is to be transferred. The byte address register is set to a particular quantity via an MPC instruction and its contents may be read via another instruction. The byte address register is on the card at location B13.

o. MONITOR CLOCKS. - There are two monitor clocks in the MTS controller logic. Each clock has 12 stages and must be preset to a count before counting will start. When a clock has counted to capacity, a flag is generated for sampling by the MTC program. The clocks are used to time critical functions in the MTS operation. Monitor clock 1 is capable of counting only at a nanosecond rate while monitor clock 2 may be controlled to count at either a nanosecond or a millisecond rate. Monitor clock 1 is on the card at location B27 and monitor clock 2 is on the card at location B28.

p. WORKING STORAGE. - The working storage is used as a sequential access read/write memory with a capacity of 256 words, eight bits per word. The controls on the memory by its read and write address registers are such that the first word written in will be the first word read out. The memory uses a roll-over read/write; that is, when one of the address registers has caused address 255 to be referenced the register is set to 0 for the next reference. The memory is used to store data frames from tape when the output byte register is full, and to store data to be written on tape as disassembled from the input byte register. The working storage memory is on the card at location B19.

q. WORKING STORAGE CONTROL. - The working storage control consists of the read address register, the write address register, address selectors and read from memory parity generation. At the beginning of an MTS operation where reading from or writing on tape is performed, the two address registers are both set to address 0. Each time data is written into the memory, the write address register is incremented. Each time data is read from memory, the read address register is incremented. The address selectors multiplex the contents of the address registers to select the address for a read or write. As data is read from the memory, the parity generation circuits supply the appropriate parity for the data. The working storage control is on the card at location B18.

r. TRANSPORT SELECT. - The transport select circuits consist of the ADDRESS switches on the system control panel, select timing chain and multiplex-decode logic. When selecting a transport, each transport ADDRESS switch is checked via the multiplex-decode logic. A switch set to the address position of the computer requested transport will cause the associated transport to be selected. The selected transport's control circuits will then cause the transport to perform the operation requested by the external function word. The transport select circuits are on the card at location A12. The control circuits are on the card at locations A8, A9, A10, and A11.

s. WRITE REGISTER. - The write register receives data in frame length (7 or 9 bits) including parity under control of the MPC program via the destination bus. This register acts as a temporary storage for the data. From the write register the data is gated to either the track scrambler (NRZI recording) or the write selectors (PE recording). The write register is on the card at location B14.

t. READ REGISTER. - The read register receives data that was read from tape and, if recorded in 9-track length, unscrambled. This register acts as a temporary storage for the data until taken by the MPC. While the data is being stored in the read register, the parity of the data is checked. The read register and parity check circuits are on the card at location B14.

u. TRACK SCRAMBLER. - One section of the track scrambler is used to convert the computer data into the proper configuration for recording on tape in the 9-track NRZI recording mode. Another section of the track scrambler is used to convert 9-track recorded data back into the form used by the computer. See figure 4-10 for examples of how computer words, by bit position, are recorded on tape in 9-track recording. When 7-track reading or writing is performed, the data passes through the track scrambler with no reformatting. The track scrambler is on the card at location B26.

v. TRANSPORT DESKEW CIRCUITS. - Due to variations inherent in write head manufacturing, the information to be recorded on tape would be skewed (not aligned across the tape). The same variations in read head manufacturing must also be corrected. To correct these variations during NRZI recording and reading, compensation delays are used in the MTS. There is, in the MTS, one delay for each track in each transport for writing NRZI, one delay for each track in each transport for reading forward NRZI, and one delay for each track in each transport for reading backward NRZI. The write delays are on cards at locations A13 through A17. The read forward and read backward delays are on cards at locations A22 through A30. When reading PE recorded data, each track is timed by MTS controller logic. Therefore, no electrical delays are used.

w. MICRO PROGRAM CONTROL. - All operations in the MTS are controlled and/or monitored by a program stored in a read only memory. The sequence of instructions obtained from the read only memory by the MPC determined what, when, and how events will be done in the MTS. The MPC is a computer with arithmetic and control capabilities. All computation, such as longitudinal parity and operation decode, is performed in the MPC. The MPC obtains information or data via the source bus and sends data via the destination bus. The source and destination of information and data is specified by the program instruction. Figure 4-18 is the functional block diagram of the MPC section of the MTS.

4-7. FUNCTIONAL SECTION DESCRIPTION.

The following paragraphs give a functional description of each logical section of the MTS.

a. DUPLEX CONTROL LOGIC. - The duplex control logic (figure 7-102) performs three basic functions in 1540 and 9-track modes of operation: request control, release control, and demand control. In the 1240 mode, the MTS does not have duplex capability, but the duplex control circuits are used to interrupt the MPC for a master clear external function code.

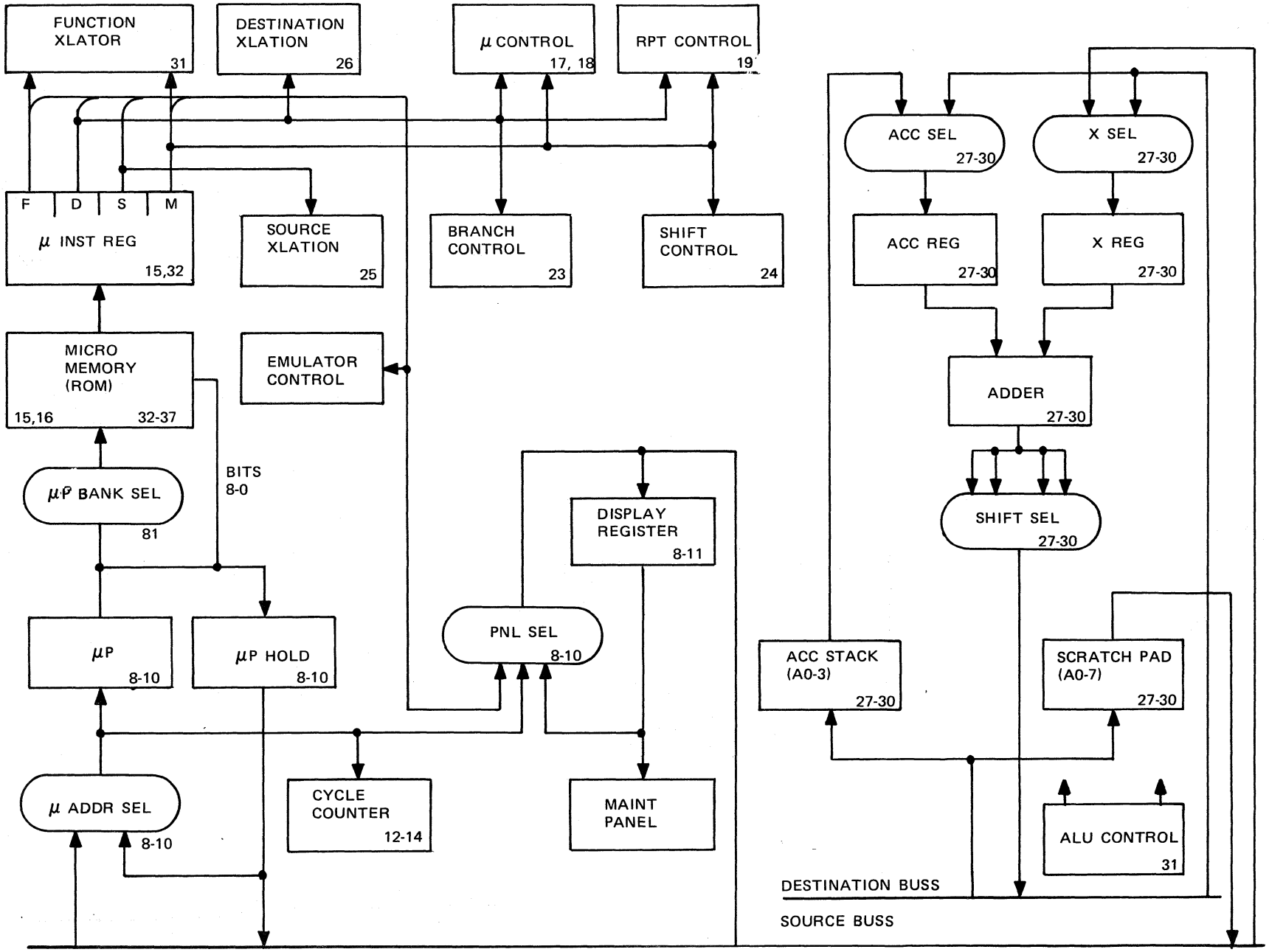


Figure 4-18. MPC Functional Block Diagram

An external function acknowledge from a computer causes either bits 17 and 16 (1540 mode) or bits 1 and 0 (9-track mode) of the external function word to be loaded into the duplex control logic for the responding computer. Having detected an external function acknowledge, the ROM program determines which computer sent the acknowledge and what the duplex request is: release control or request control. If both duplex bits are set, an interrupt is generated to the MPC to signify a demand control. After establishing the type of control request, the ROM program clears the duplex control flip-flops. In the 1240 mode of operation, bit 16 of the external function word is loaded into the duplex control circuits where it is ANDed with a 1240 mode signal to interrupt the MPC. The ROM program then causes the controller circuits to be cleared to await the next external function command from the computer.

(1) REQUEST CONTROL. - With the external function word bit 17 (1540 mode) or bit 1 (9-track mode) set and bit 16 (1540 mode) or bit 0 (9-track mode) clear, the bits are gated into the duplex control logic and the request control flip-flop for the associated computer is set. The release control flip-flop remains in the clear state. The ROM program, on finding an external function acknowledge from a computer, checks the outputs of the duplex control flip-flops. Assuming neither computer has control, the ROM program, on finding a request control flip-flop set, grants control to the requesting computer and clears the request control flip-flop. If the other computer has control when the request for control is made, the request is stored until the controlling computer releases control.

(2) RELEASE CONTROL. - With the external function word bit 16 (1540 mode) or bit 0 (9-track mode) set and bit 17 (1540 mode) or bit 1 (9-track mode) clear, the bits are gated into the duplex control logic and the release control flip-flop for the associated computer is set. The ROM program, on finding an external function acknowledge from a computer, checks the outputs of the duplex control flip-flops. Assuming the computer in control sent the release control, the ROM program, on finding the release control flip-flop set, clears the release control flip-flop and the in-control flag for the associated computer. If the other computer has a request control stored when the controlling computer releases control, the program grants control to the other computer and sends a status external interrupt with an in-control indication.

(3) DEMAND CONTROL. - With the external function word bits 17 and 16 (1540 mode) or bits 1 and 0 (9-track mode) both set, the bits are gated into the duplex control logic and both the release control and request control flip-flops are set. Outputs from both flip-flops are ANDed to generate a demand control signal. This signal causes the ROM program operation to be interrupted by forcing the address register to a predetermined address. The subroutine performed removes control from the controlling computer and gives control to the demanding computer. A status interrupt is sent to the computer which lost control with a not-in-control indication. The present operation is terminated and the MTS prepared for the next external function command from the computer now in control.

b. INPUT/OUTPUT CONTROL. - The requests from the MTS to a computer are initiated by instructions in the ROM program. Acknowledges from the computer to the MTS are interpreted by instructions also in the ROM program. Decisions made by the ROM program control the operations and timing of events in the input/output control logic. The following paragraphs define the input/output control signal generation or interpretation.

(1) EXTERNAL FUNCTION REQUEST/ACKNOWLEDGE. - The external function request signal to a (both, if duplex operation) computer(s) is sent when the busy store circuit (figure 7-79) is storing a 0 indicating not busy or idle. This store circuit will have a 0 stored when the ROM program has determined that neither computer has sent an external function acknowledge, or after processing a control request from the computer not in control. The store circuit will have a 1 stored during the processing of a control request and during the performance of an operation as specified by an external function command word from a controlling computer.

An external function acknowledge from a computer enters the MTS via the control interface logic (figure 7-111) and is clocked into the external function control logic (figure 7-84). There are two identical sets of control logic: one for computer A and the other for computer B. The setting of the control flip-flop for the associated computer also causes the duplex control bits to be gated into the duplex logic. With the control flip-flop set, a flag is generated. The ROM program interprets the flag and determines which duplex function is requested: request control or release control. When control is requested and granted, the next external function acknowledge from the controlling computer gates the external function word into the C register for interpretation by the ROM program. A signal generated by an instruction in the ROM program clears the external function control flip-flop after it has been detected by the program.

(2) INPUT DATA REQUEST/ACKNOWLEDGE. - The initiation of an input data request to a computer is under control of the ROM program. When the ROM program determines that the number of bytes required have been assembled in the output byte register, the output byte register loaded signal is generated by a program instruction. This signal is clocked through control logic (figure 7-95) and sets the input data request flip-flop. The output of the flip-flop is gated through the interface control logic (figure 7-111) to the computer in control of the MTS.

When the controlling computer accepts the data, it responds with an input data acknowledge. This acknowledge is received by the interface control logic and clocked through logic (figure 7-102) to clear the input data request flip-flop. When the ROM program finds the input data request flip-flop in the clear state, it then can start loading the output byte register again if another transmission is to be made.

(3) OUTPUT DATA REQUEST/ACKNOWLEDGE. - The initiation of an output data request to a computer is under control of the ROM program. When the ROM program determines that a data transfer from the computer is required, a signal is generated to set the output data request flip-flop (figure 7-84). The output of the flip-flop is gated through the interface control logic (figure 7-111) to the computer in control of the MTS. The input data request is sent to obtain one of the following: data to be written on tape, the selective read code, or the search key.

When the controlling computer sends the requested data, it responds with an output data acknowledge. This acknowledge is received by the interface control logic and clocked through logic (figure 7-84) to clear the output data request flip-flop. When the ROM program finds the output data request flip-flop in the clear state, it transfers the data from the C register to the input byte register for processing.

(4) EXTERNAL INTERRUPT REQUEST. - An external interrupt request flip-flop (figure 7-95) is set under ROM program control. The external interrupt request is used to send status information to a computer. When the ROM program initiates an

external interrupt, a signal is generated to interrupt the appropriate computer (computer A or computer B). After accepting the status information, the interrupted computer responds with an input data acknowledge to clear the external interrupt flip-flop.

c. CLOCK LOGIC. - There are two basic clocks in the MTS. The following paragraphs describe the purposes of each clock.

(1) MASTER CLOCK. - Figure 7-7 is the functional schematic of the master clock and distribution. Figure 4-19 is the timing diagram for the master clock with delay line connections of E11 to E3, E12 to E7, and E13 to pin 6. The master clock has a 200-nanosecond repetition rate. The voltage transitions of the phase early (ØE) clock pulses occur 30 nanoseconds prior to the transitions of the phase normal (ØN) clock pulses. Of the 200 nanoseconds, each clock phase will be a low for 70 nanoseconds and a high for 130 nanoseconds. The master clock is used to time the operations of the MPC portion of the MTS.

(2) FOUR-PHASE CLOCK. - Figure 7-86 is the functional schematic of the four-phase clock and distribution. Figure 4-20 is the timing diagram for the clock. The outputs of a crystal controlled oscillator (figure 7-74) are used to sequentially generate the phase outputs of the four-phase clock. The phase outputs of the clock are used to time transport operation and computer/MTS communication.

d. DENSITY SELECTION. - The density at which the MTS will operate is determined by the ROM program. Figure 4-21 is a flow chart of density selection by the 7-track ROM program. The density bit(s) of the external function word are examined by the program and the appropriate store circuit (figure 7-82) is set. The output of each density store circuit is ANDed with outputs of the write counter (figure 7-86) and the read counter (figure 7-87) to generate strobe pulses. The strobe pulses are, therefore, timed by the density selected.

e. TRANSPORT SELECTION. - The ROM program examines the combination of transport select bits in the external function word to determine which transport position setting to select. This operation is necessary since the external function word transport addressing codes are not sequential and the switch position selections are. When the transport position setting has been determined, one of the multiplexers on figure 7-94 is enabled for the given position and a program instruction causes the first flip-flop in the select timing chain to be set. Sequentially, each flip-flop in the chain is set and the preceding flip-flop cleared. As a flip-flop (after the first flip-flop) is set, a signal is sent through the associated transport's ADDRESS switch to the multiplexers (figure 7-94). When an ADDRESS switch has the required setting, the associated transport will be selected and the sequencing of the flip-flops stopped. If none of the ADDRESS switches have the required setting, the sequencing will stop after the last flip-flop is cleared and no transport will be selected.

f. C REGISTER. - The C (I/O) register (figures 7-97 through 7-100) is a 36-bit temporary storage register for all data communicated between the MTS and a computer. Data is entered into the register by one of the following:

1) External function acknowledge from either computer when the MTS is in the idle state.

2) External function acknowledge or output data acknowledge from the computer having control of the MTS.

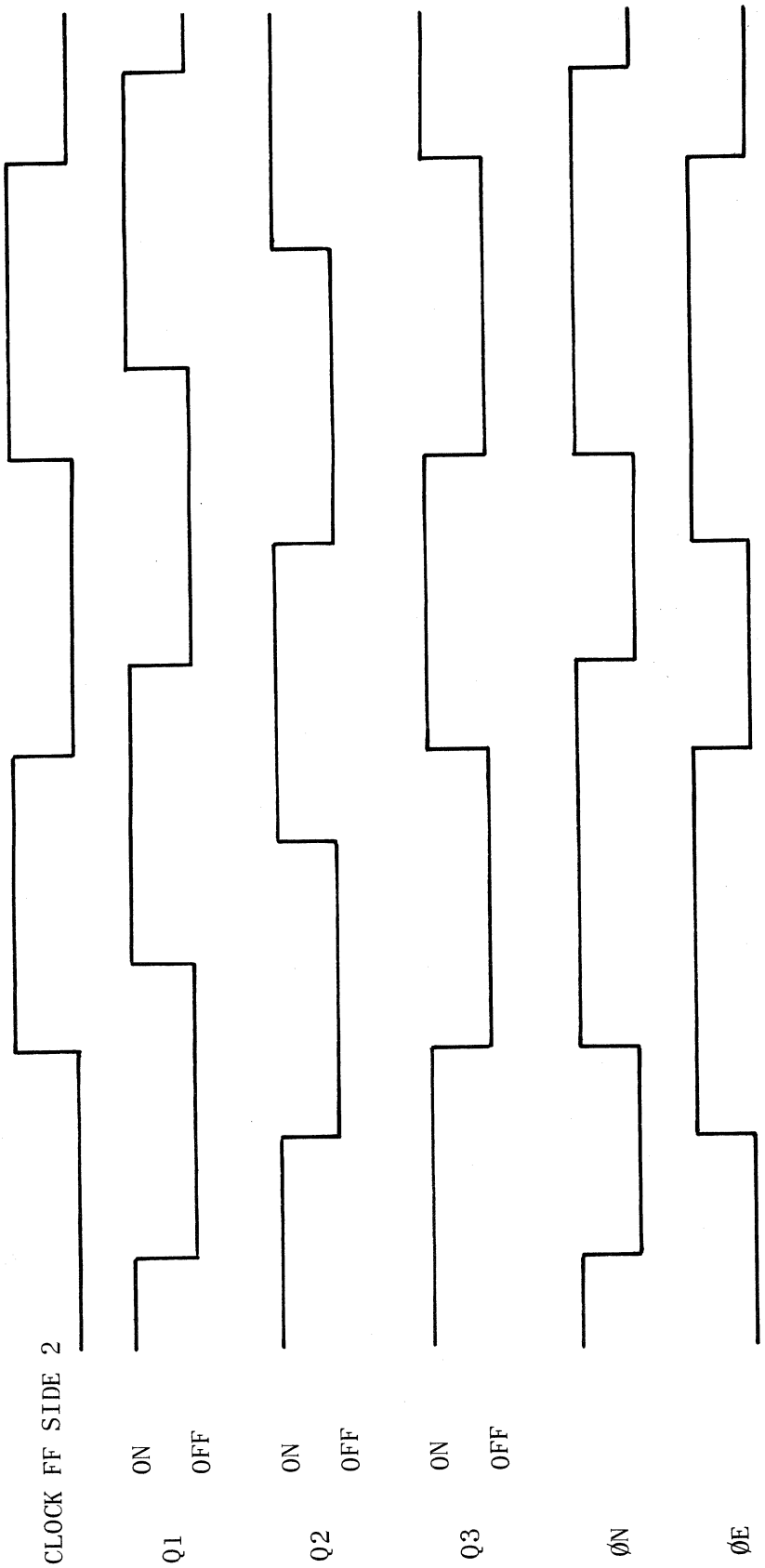


Figure 4-19. Master Clock Timing Diagram

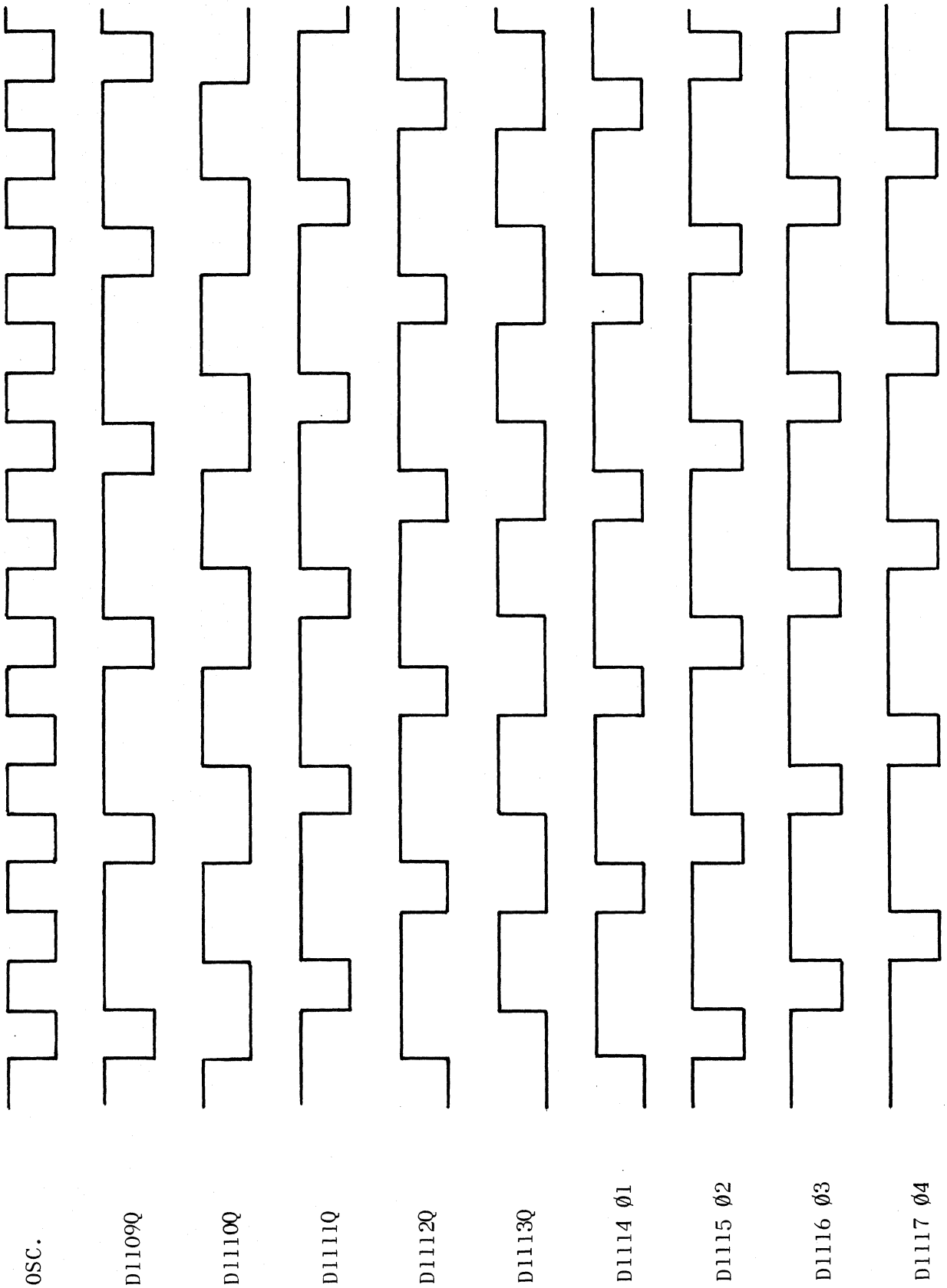


Figure 4-20. Four-Phase Clock Timing Diagram

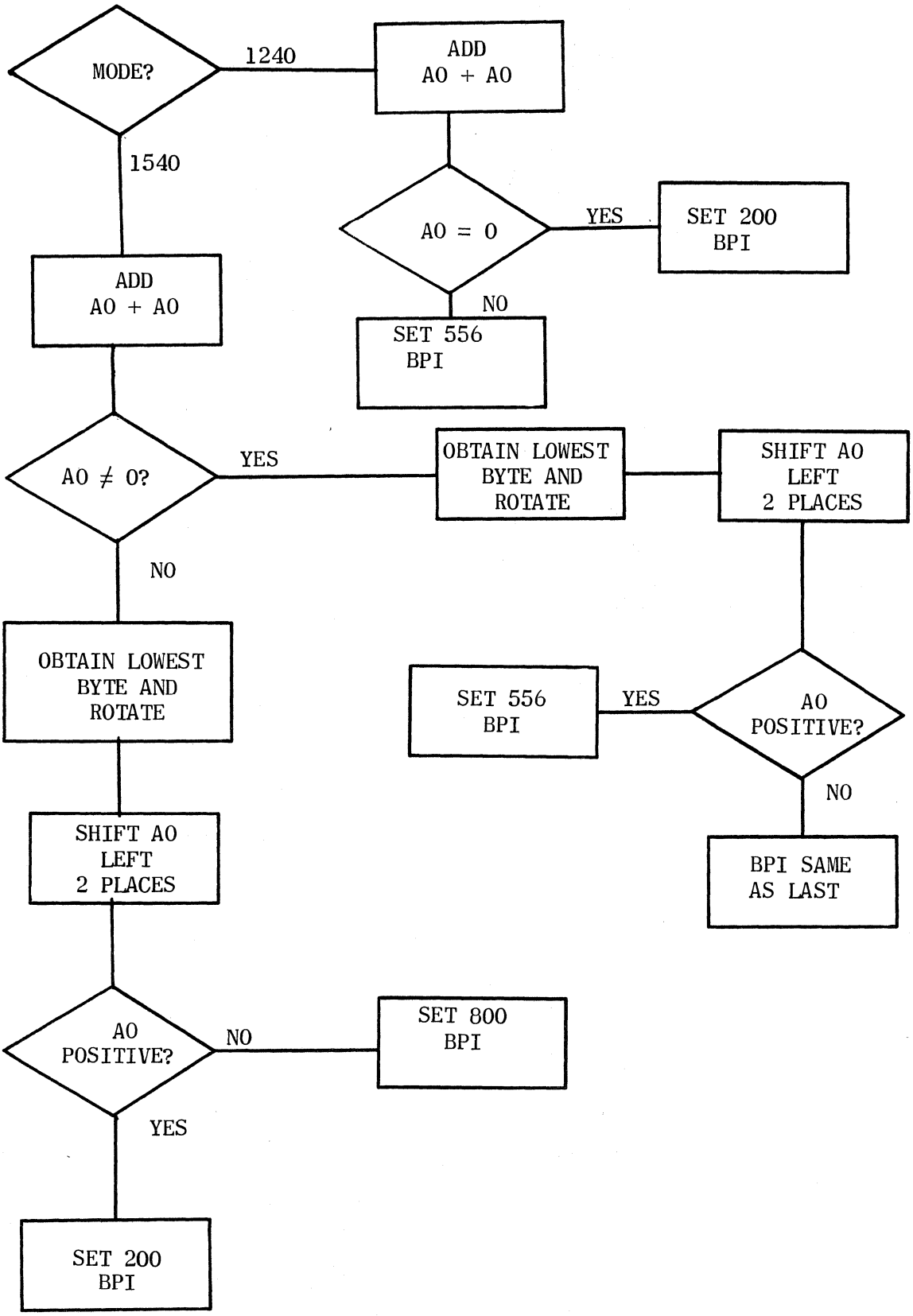


Figure 4-21. 7-Track Density Selection

3) The ROM program sets the output byte register loaded flag after a word is formed in the output byte register.

Data from the C register is transmitted either to the data line drivers for communication to a computer or to the input byte register. The entering of the data into the input byte register is under ROM program control.

g. INPUT BYTE REGISTER. - The input byte register (figures 7-53 and 7-55) is a 36-bit temporary storage register for computer length words. Data is transferred into the register from either the C register or the output byte register via the input byte register selectors (figures 7-53 and 7-55). The source of data to be transferred into the input byte register and the time when the register is loaded are both under control of the ROM program. The outputs of the register go to the input byte network.

h. INPUT BYTE NETWORK. - The input byte network (figures 7-52 and 7-54) consists of multiplexers used to select a given byte in the input byte register. The contents of the byte address register (figure 7-42) determines which byte is selected. When the bytes are being selected in 7-track operation, the outputs of the lower three 9312 multiplexers on each figure are gated through the associated 9322 quad multiplexer. When in 9-track operation, the upper four 9312 multiplexers outputs are used. The outputs of the quad multiplexers are selected by the ROM program for transfer via the source bus.

i. OUTPUT BYTE REGISTER. - The output byte register (figures 7-50 and 7-51) serves as the assembly register for the MTS. The ROM program transfers data in byte form as read from tape or from the working storage to the output byte register buffer (figure 7-42). The contents of the byte address register (figure 7-42) is decoded and the resultant enable gates a data byte into the output byte register. All data bytes gated into the register are considered to be 8-bit bytes. In 9-track operation, the assembled data is gated directly through multiplexers (figures 7-50 and 7-51) to either the C register selectors or the input byte register selectors (ROM program specifies which one). In 7-track operation, the gating enable on the multiplexers is changed and the data in each pair of store 4 circuits is treated as 6 bits instead of 8 bits (the upper two bits of each pair are ignored). As the assembled data is gated through the multiplexers, it is packed into computer word form. The pair with data bits 5 through 0 requires no shifting, the pair with bits 11 through 6 are shifted right two places, the pair with bits 17 through 12 are shifted right four places, bits 23 through 18 shifted right 6 places, 29 through 24 shifted right 8 places and bits 35 through 30 shifted right 10 places.

j. MONITOR CLOCKS 1 AND 2. - There are two monitor clocks used in the MTS: monitor clock 1 (RTC1 - figure 7-48) and monitor clock 2 (RTC2- figure 7-49). RTC1 counts at the rate of the phase N clock pulse. RTC2 counts at either the rate of the phase N clock pulse or at a one millisecond rate. The counting rate of the RTC2 is determined by ROM program selection. RTC1 is used to determine when data transfers have been completed or, if data is received after 2-1/2 frame times after the last transfer, to indicate a timing error has occurred. RTC2 is used to determine the length of IRG gaps and to time certain program delays. Both clocks are preset by program instructions and generate a "counter full" signal when the associated clock has counted to full capacity.

k. BYTE ADDRESS REGISTER. - The byte address register (figure 7-42) is a 4-bit register used to control the selection of bytes either from the input byte register

or to the output byte register. The register is loaded, read, or modified by program instructions. By monitoring the contents of the register, the program determines when the last required byte has been loaded or read.

l. FORMAT CONVERTER. - The format converter (figures 7-44 and 45) is used by the ROM program during 7-track redundant (octal) operations. During write operations, each octal character is duplicated by the format converter to generate a 6-bit data byte. During read operations, each data frame read from tape is sent to the format converter to form one-half of a 6-bit data byte. Two consecutive frames transferred to the format converter during read operations would form a 6-bit data byte. The redundancy toggle signal controls the position into which each one-half data byte is placed. The resultant three bits formed by the first frame to the format converter are stored in the format converter until the second frame is converted. A ROM program instruction then transfers the resultant 6-bit byte from the format converter to a location specified by the instruction.

m. WORKING STORAGE CONTROL. - The working storage control (figure 7-59) consists of two address counter/registers and multiplexers. One address counter/register is for selection of working storage addresses during a working storage write and the other selects addresses during a working storage read. The associated counter is incremented when a working storage reference is made. The multiplexers allow the selection of either of the counter/registers. Also associated with the working storage control are two 5-bit comparators. The comparators are used to generate a low signal when the read and write address counters contain the same amount indicating the same address. This signal is used by the ROM program to determine if data is contained in the working storage. When the signal is a high, data is contained in the working storage. When the signal is a low, either the working storage is filled with data or all data has been read from the working storage. The ROM program makes the determination of whether the working storage is full or empty. Control circuits are used to make the counters "roll over counters". When a counter has reached a count of octal 357, the counter is reset to address zero.

n. FLAG TEST CIRCUITS. - The flag test circuits (figure 7-41) are used by the ROM program to make operational decisions. The decision by the ROM program may be made on the state (high or low) of either one or a series of flags. When a series of flags are tested, the first test instruction must be without cascade and the remaining instructions with cascade. As long as there is a "test was true" indication after each test in a cascade series, the result of the next test will be clocked into the detection circuits. When one test in a series is not true, none of the succeeding tests in the series will be clocked into the detection circuits. After a test or a cascaded series of tests has been completed, the ROM program may at any time make a program branch decision on the resultant signal. The ROM program may examine the state of any flag, whether a program flag or hardware flag in the MTS, by use of the flag test circuits.

When a flag is to be manipulated (changed from one state to the other), the flag test circuits are disabled and the clear or set group 1 or 2 and write program flag circuits are enabled.

o. PARITY GENERATION. - There are two parity generating circuits in the MTS: Write data parity 7-track redundant recording and Write data parity 7-track non-redundant and 9-track recording.

(1) 7-TRACK REDUNDANT RECORDING. - When doing 7-track redundant (octal) recording, the parity of the data frame is generated by the format converter circuits (figure 7-45). The parity generating circuits control bit 6 of the word from the format converter such that the parity of a frame is always odd.

(2) 7-TRACK NONREDUNDANT AND 9-TRACK RECORDING. - When doing 7-track nonredundant (bioctal) or 9-track recording, the parity of a frame is generated as it is read from the working storage. The parity generating circuits are on figure 7-60. The parity circuits consist of a parity generator and controls. When the operation is a read, the AND circuits fed by the output of the parity generator are disabled. The inputs to the parity generator are from the working storage bits and the parity flag. In 7-track operation, the parity bit is generated and inserted in the working storage bit 6 position. In 9-track operation, the parity bit is generated and inserted in the working storage bit 8 position.

p. NRZI DESKEW. - Due to variations inherent in read/write head manufacturing, information frames to be recorded on tape would be skewed (figure 4-22). To prevent this skewing, delays are built into the write circuits to realign the data bits when written on tape. There is one write delay per track per transport. The delays are shown as follows: track 0 figure 7-116; tracks 1 and 2 figure 7-118; tracks 3 and 4 figure 7-120; tracks 5 and 6 figure 7-122; and tracks 7 and 8 figure 7-124. The deskewing adjustment for each data bit is set to compensate for each transport track variation so that a frame of data will appear on tape with as little skew as possible. The read amplifiers also utilize time delays in much the same manner, to present the data bits detected on tape to the read register (figure 7-87) at, as nearly as possible, the same instant. There are two read delays per track per transport. One delay is for read forward and the other for read reverse. The delays are shown as follows: track 0 figure 7-131; track 1 figure 7-133; track 2 figure 7-135; track 3 figure 7-137; track 4 figure 7-139; track 5 figure 7-141; track 6 figure 7-143; track 7 figure 7-145; and track 8 figure 7-147.

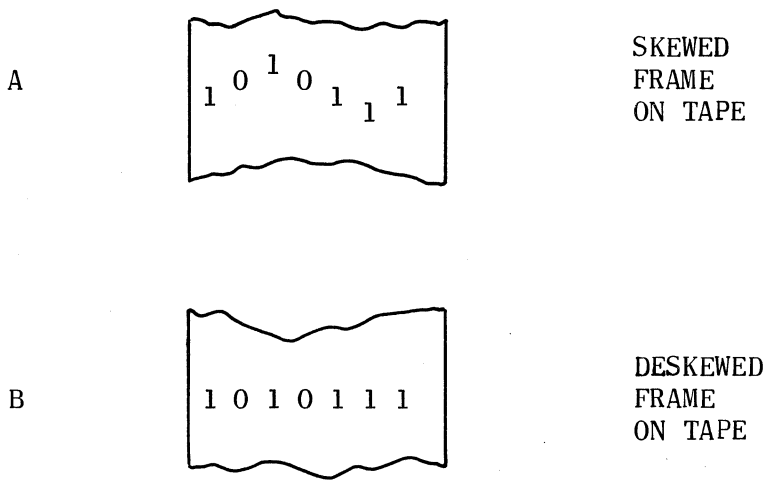


Figure 4-22. Skew

q. PHASE-ENCODED DESKEW. - When reading phase-encoded data, the MTS uses data bins and data bin selectors (figures 7-153 through 7-157) to deskew data frames. There are four data bins and one selector for each read head track. After data has been placed in a data bin, the selector is clocked to select the next sequential data bin. When all bits of a frame from tape have been interred into their associated data bin, the frame is gated to the read register. The data bin of each bit from which the frame is gated is controlled by bin selector G6111 (figure 7-162). Each time a frame is gated to the read register by a PE strobe signal, the bin selector is clocked to select the next sequential data bin selection.

r. START CONTROL. - The ROM program, by examining the external function word instruction code, determines the direction of operation for a tape transport. A manipulate instruction, via the instruction decode circuits (figure 7-78), generates a signal either from D8115G to clear the direction store circuit (E7110D, figure 7-82) or from D8116G to set the direction store circuit. The direction store circuit in the clear state (storing a zero) indicates the forward direction and in the set state (storing a one) indicates the reverse direction. If the operation is a rewind, the rewind store circuit (E7116B, figure 7-82) will be set via the instruction decode circuits (figure 7-80) signal from D8316H. After the direction has been determined and the store circuit(s) placed in the required state, the ROM program, at the beginning of the instruction sequence for the required operation, will set the run store circuit (D8119D, figure 7-78) via the instruction decode circuits. The output of the run store circuit, with a phase 3 pulse and the stop flip-flop in the clear state, will start the start pulse timing chain (figure 7-113). The start pulse generated by the timing chain is ANDed with the set output of the selected transport's select flip-flop (figures 7-89 through 7-92) to clock in the direction instruction into the appropriate flip-flop(s) and generate a start tape motion command to the selected transport.

s. STOP CONTROL. - For all operations, except rewind, the ROM program determines the end-of-current operation and initiates the stopping of a tape transport. A manipulate instruction is executed to clear the run store circuit (D8119B, figure 7-78). The output signal from D8115C which clears the run store circuit (clearing causes the circuit to store a zero) also sets the stop enable store circuit (E7116C, figure 7-82). The high from E7116C completes AND circuit D7104 (figure 7-96) and enables the stop multiplexer (D1136, figure 7-112) to start either the FWD STOP or REV STOP delay (figure 7-96). At the end of the delay, the positive going signal from D7120 clocks a zero (clears) into the stop flip-flop (D3116, figure 7-113). The high output from the stop flip-flop clear side causes the selected transport direction flip-flop to be cleared. Clearing the direction flip-flop removes the direction signal to the transport, thereby causing the transport to stop. When the operation is a rewind, the transport reaching BOT causes the associated RWD flip-flop (figure 7-89 through 7-92) to be cleared, removing the reverse drive signal to the transport.

4-8. SEQUENCE FLOW DIAGRAMS. (FIGURES 4-23 THROUGH 4-89)

a. READ CONTROL. - The control of a read operation in the 1840 (Modified) is performed by the ROM program. There are three basic read functions performed by the program: Read Initiation; Read Data Store; and Buffer to OBR. The following paragraphs describe each basic read function.

(1) READ INITIATION. - Figure 4-27 is a flow chart of the read initiation. The executive portion of the ROM program decodes and interprets an instruction word

from the controlling computer. When it is determined that the operation code in the instruction word specifies a read operation, a jump is performed to the read subroutine. The read initiation portion of the read subroutine then checks for a selective read operation. If a selective read is to be performed, a code word is requested from the controlling computer. Prior to starting the selected transport, the following occurs:

1) The BAR is preset for word assembly, value determined by modulus.

2) The lateral parity check is enabled.

3) The redundant flag is initialized for redundant reading.

4) Arithmetic register A5 is cleared for use in longitudinal parity checking.

After the preceding has occurred, the selected transport is started and the RTC2 set to count for two inches of tape. The RTC2 is used in this instance to check for either a normal IRG or an XIRG. A data ready being detected before the RTC2 has completed its count indicates a normal IRG. If the RTC2 completes its count before data is ready, an XIRG is indicated. After the data ready has been detected, the ODR flag is checked to see if one of two conditions exists: 1) Selective read and identifier code has been received; or 2) Normal read and no code required. Either condition is identified by the flag not set. If, at this time, the flag is set, an output timing error is generated and the transport spaces to the next IRG. Assuming the flag is not set, the program then starts to read data to the buffer.

(2) READ DATA STORE. - Figure 4-28 is a flow chart of the read data store sequence during a read operation. As data is read from tape, it is checked, converted (if redundant data) and stored in the working storage buffer. Data is read, checked and stored in the buffer until one word, as specified by the modulus, has been stored. When the BAR contents equals zero, the output byte register (OBR) flag is checked to see if the buffer to OBR sequence is to be started. If not, the data being read from tape continues to be stored in the buffer. Each time the BAR contents equals zero, the OBR flag is checked. Each frame read from tape is stored in sequential addresses and read from the buffer in the same sequential order.

At the start of the read data store sequence, the frame of data is transferred to the A0 register. The data ready flag is cleared to allow its resetting when the next frame is read from tape. The contents of the A5 register is logically added to the contents of A0 to compute the longitudinal parity. The condition of the lateral parity error flag is then tested for a frame parity error and a test made of whether an error is to be ignored or not to be ignored. If an error occurred and it is not to be ignored, the transport then spaces to the next IRG and a status error is sent to the controlling computer. With no error occurring, the redundant flag is tested and, if set, the data is transferred to the format converter for conversion before being stored in the buffer. After storing a frame of data in the buffer, a check is made to see if the buffer is full. The buffer full indication signifies that the working storage write register contents now equals that of the working storage read register during a read data from tape operation. The buffer will become full if the controlling computer does not accept word transfers at a fast enough rate. The buffer full flag being set will cause the transport to be spaced to the next IRG and a status error will be sent to the computer. After a frame has been stored in the buffer and the buffer full test indicates not full, the contents of the BAR are checked for being zero (modulus specified word stored

in buffer). When the BAR contents are not zero, the BAR is decremented. The next data frame is read from tape and the sequence of events repeated. The contents of the BAR equal zero will cause a branch in the sequence of events to check the OBR loaded flag (set condition indicates word in OBR not taken by computer). With the flag set, the BAR is set to the modulus minus one value for reading the next frame of data and continuing until another word has been read. When the OBR loaded flag is not set (indicates no word to be transmitted in OBR), the MTS enters the buffer to OBR sequence.

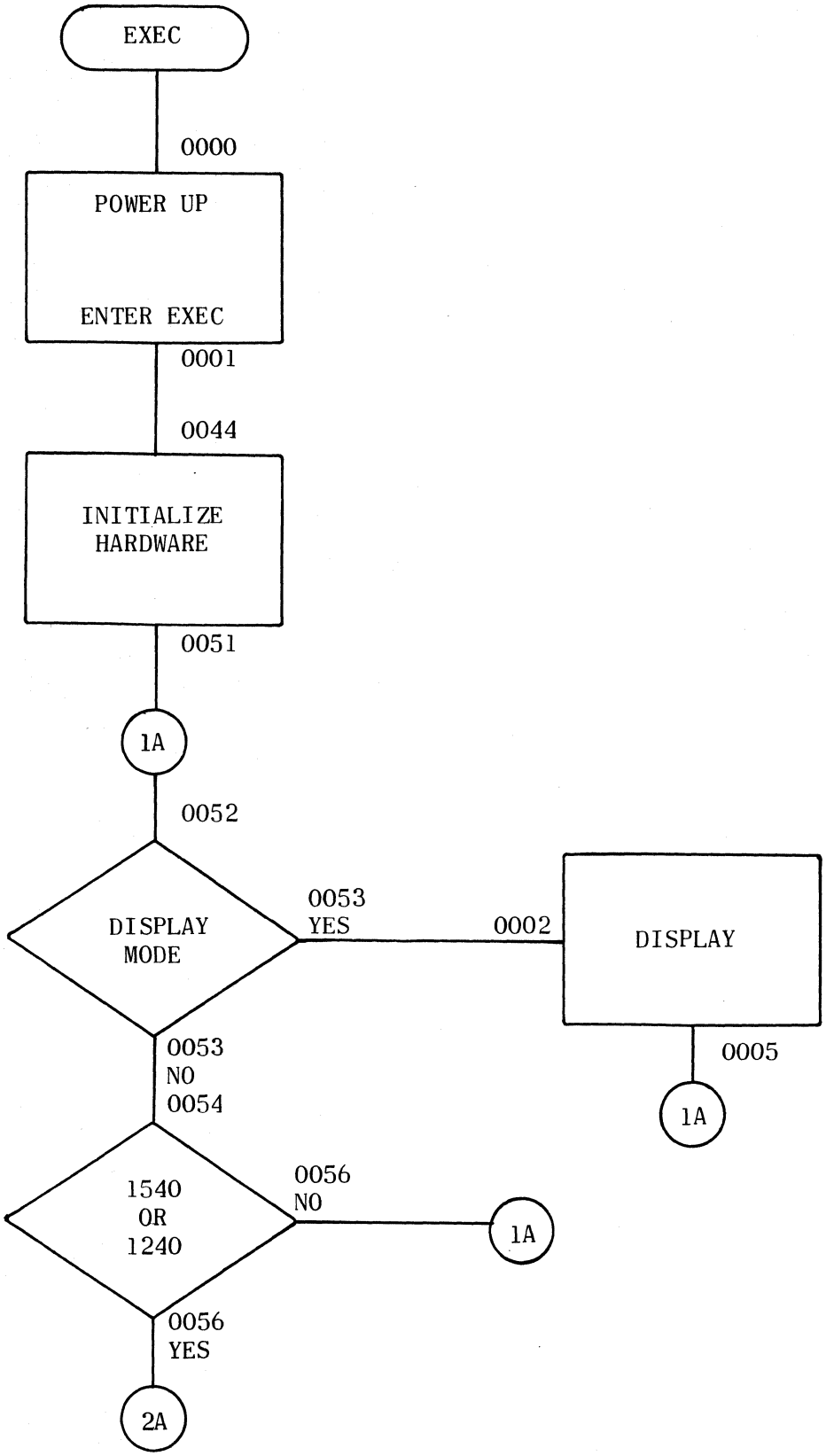


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 1 of 19)

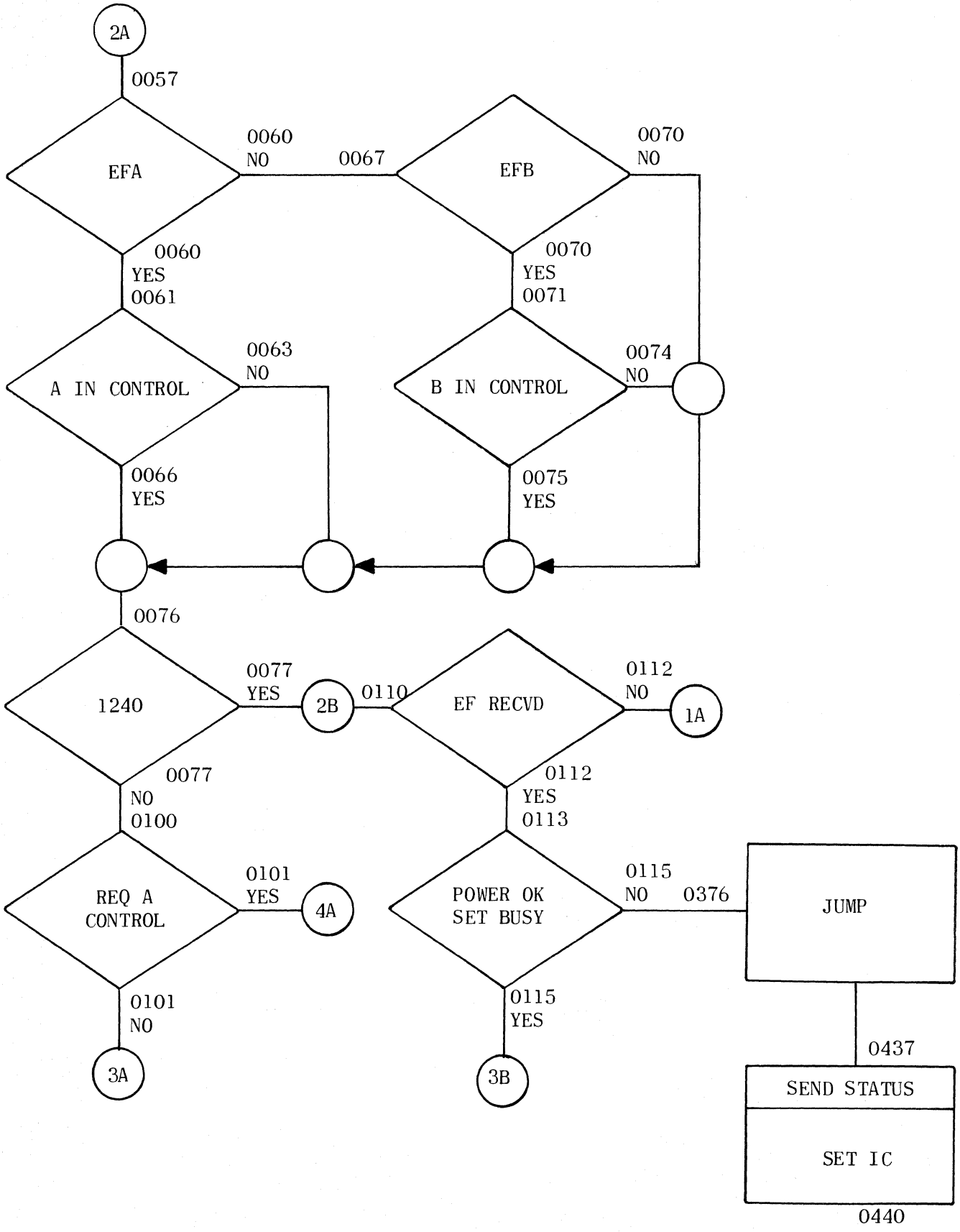


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 2 of 19)

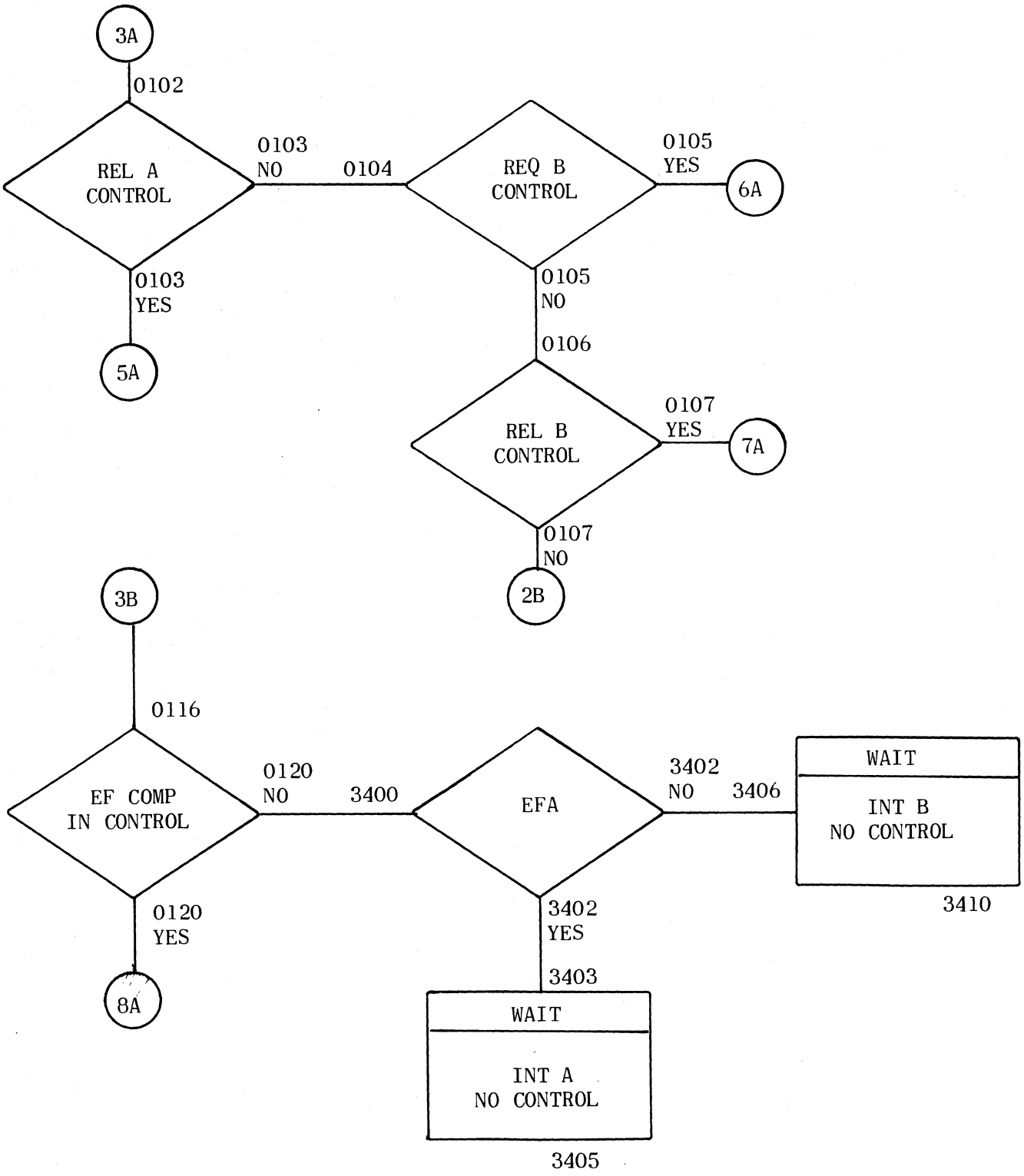


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 3 of 19)

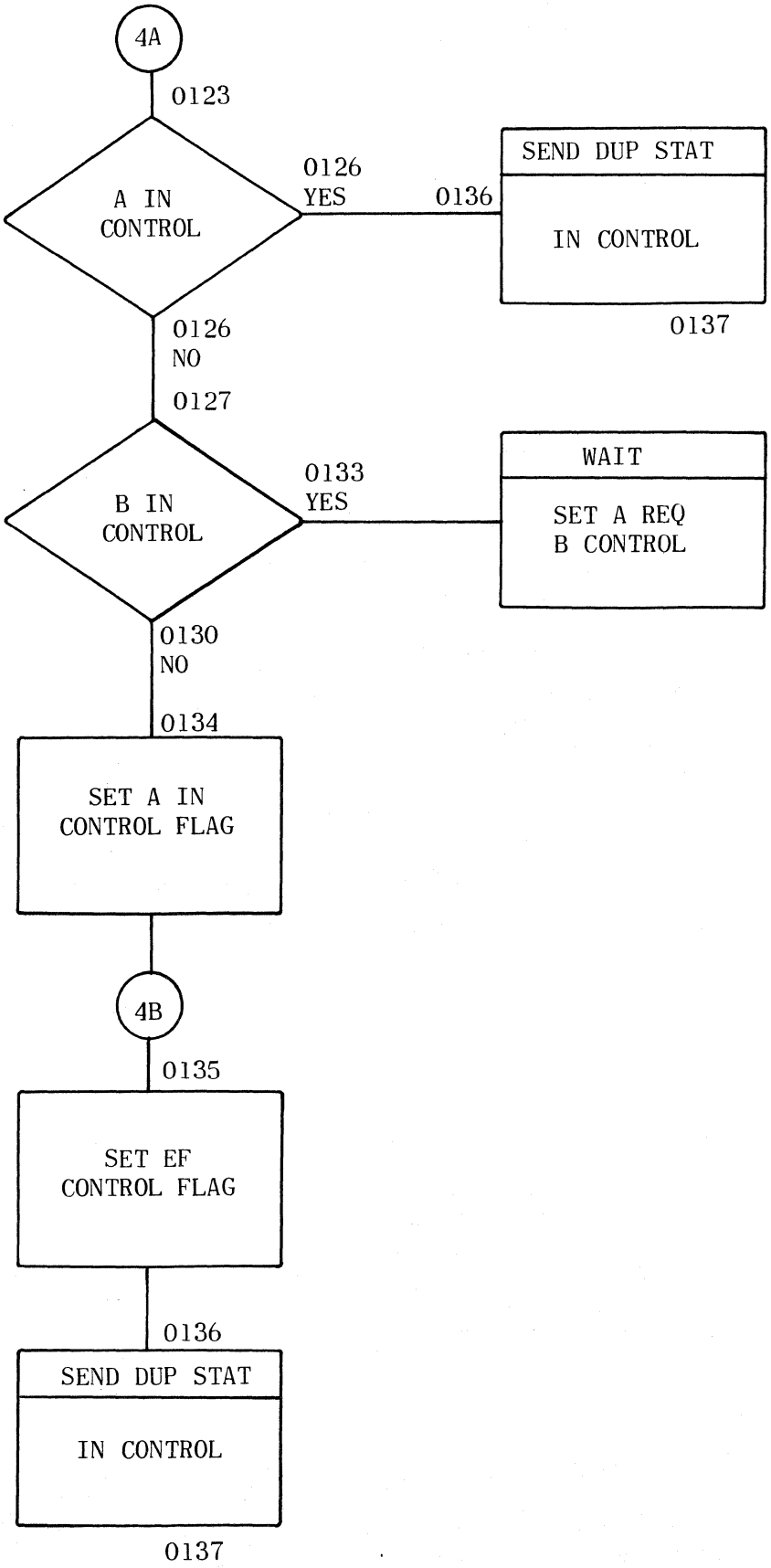


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 4 of 19)

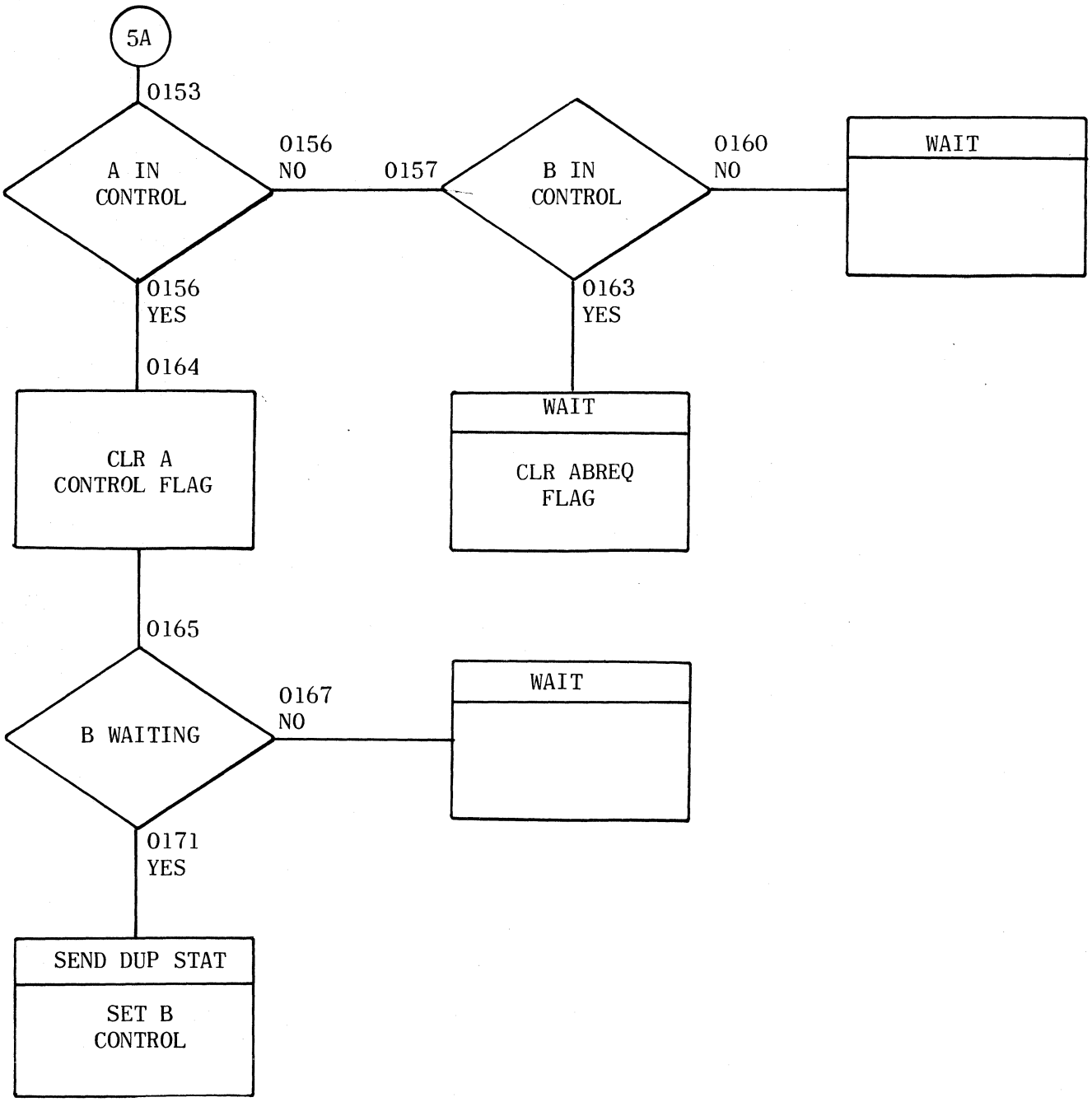


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 5 of 19)

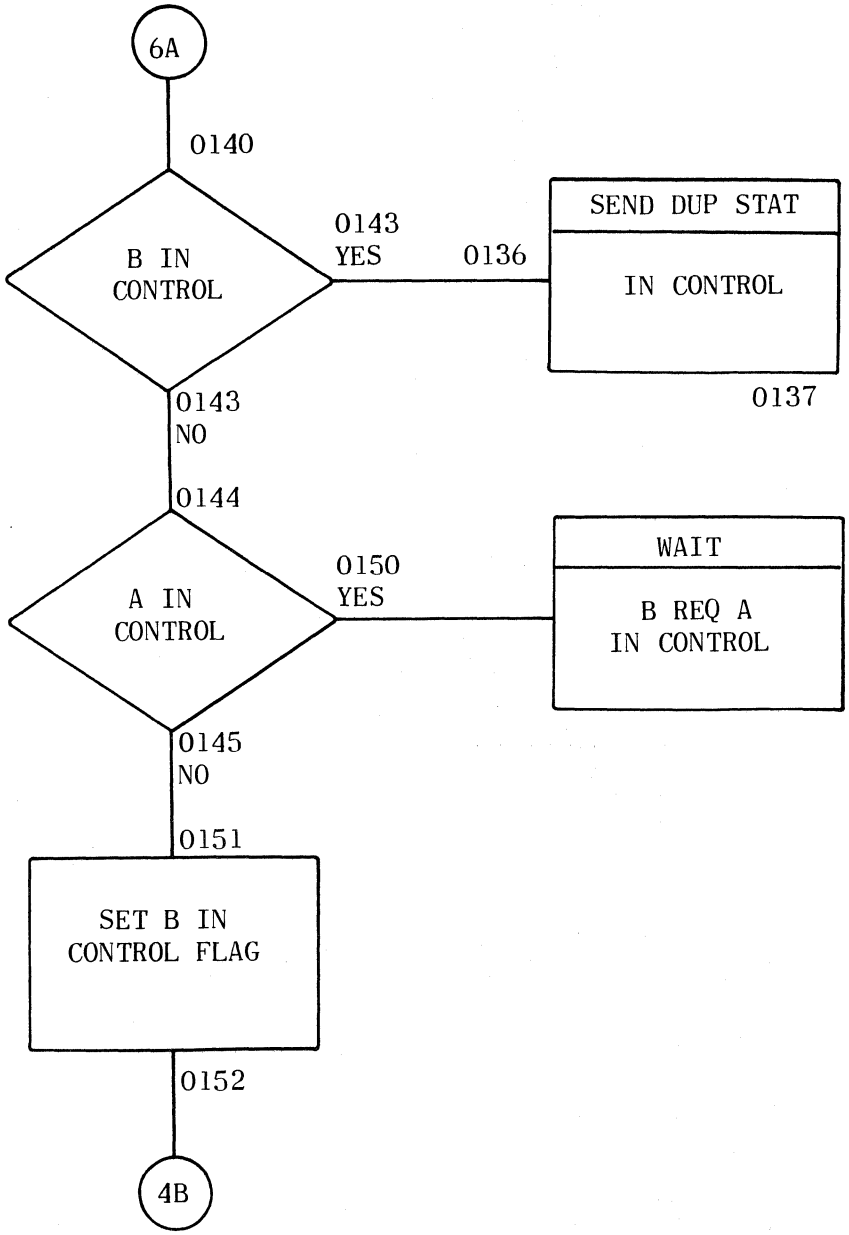


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 6 of 19)

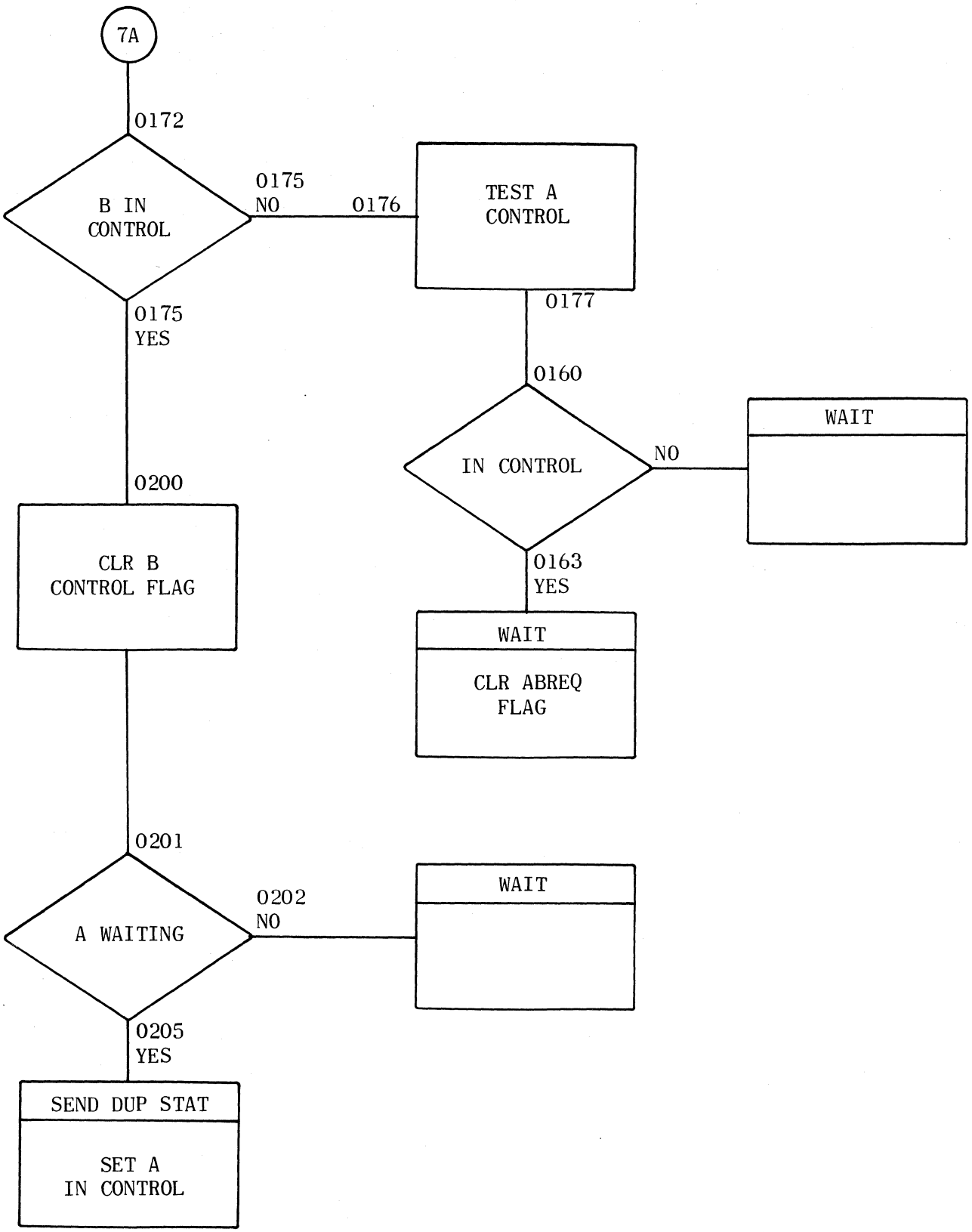


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 7 of 19)

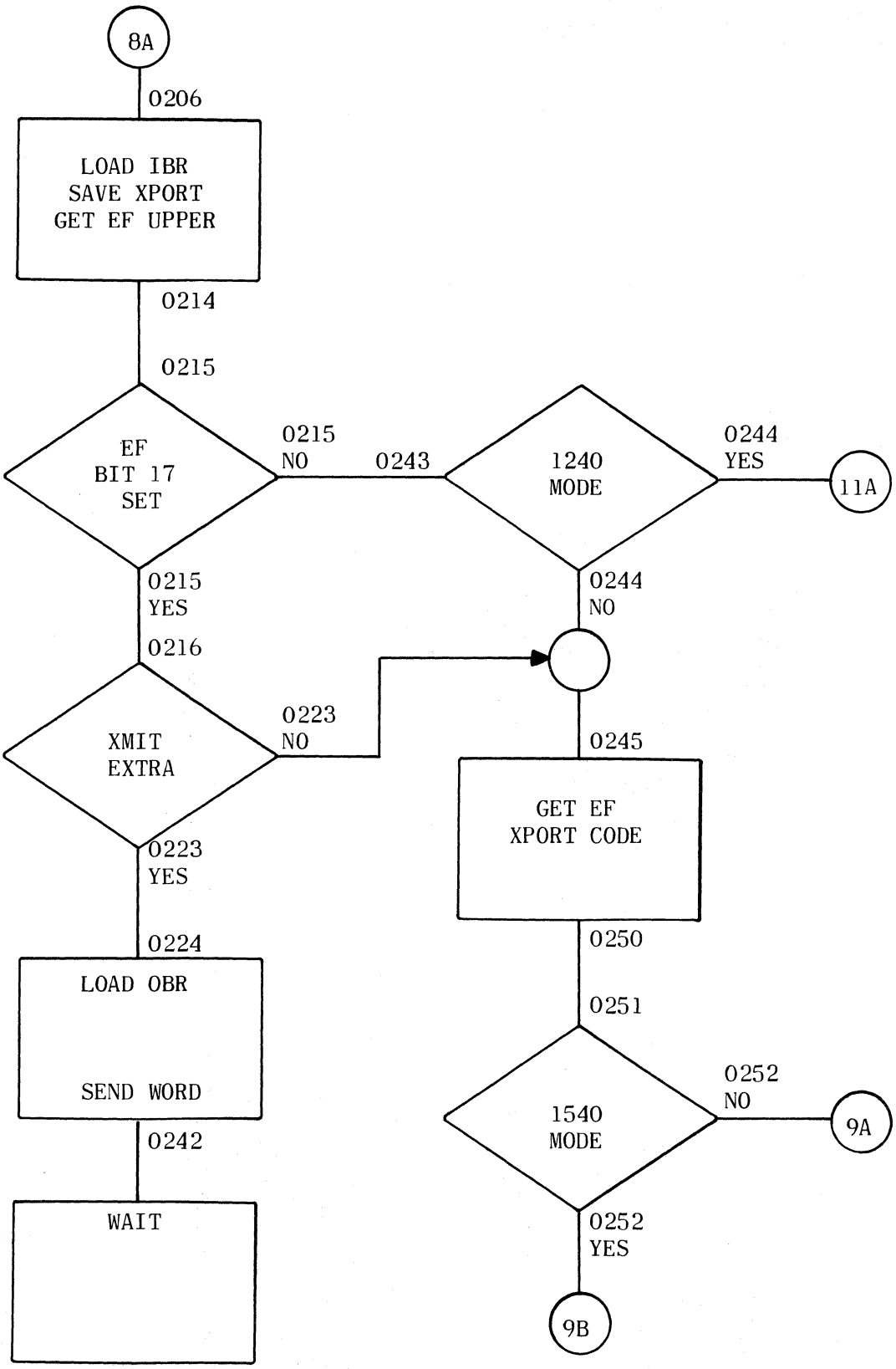


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 8 of 19)

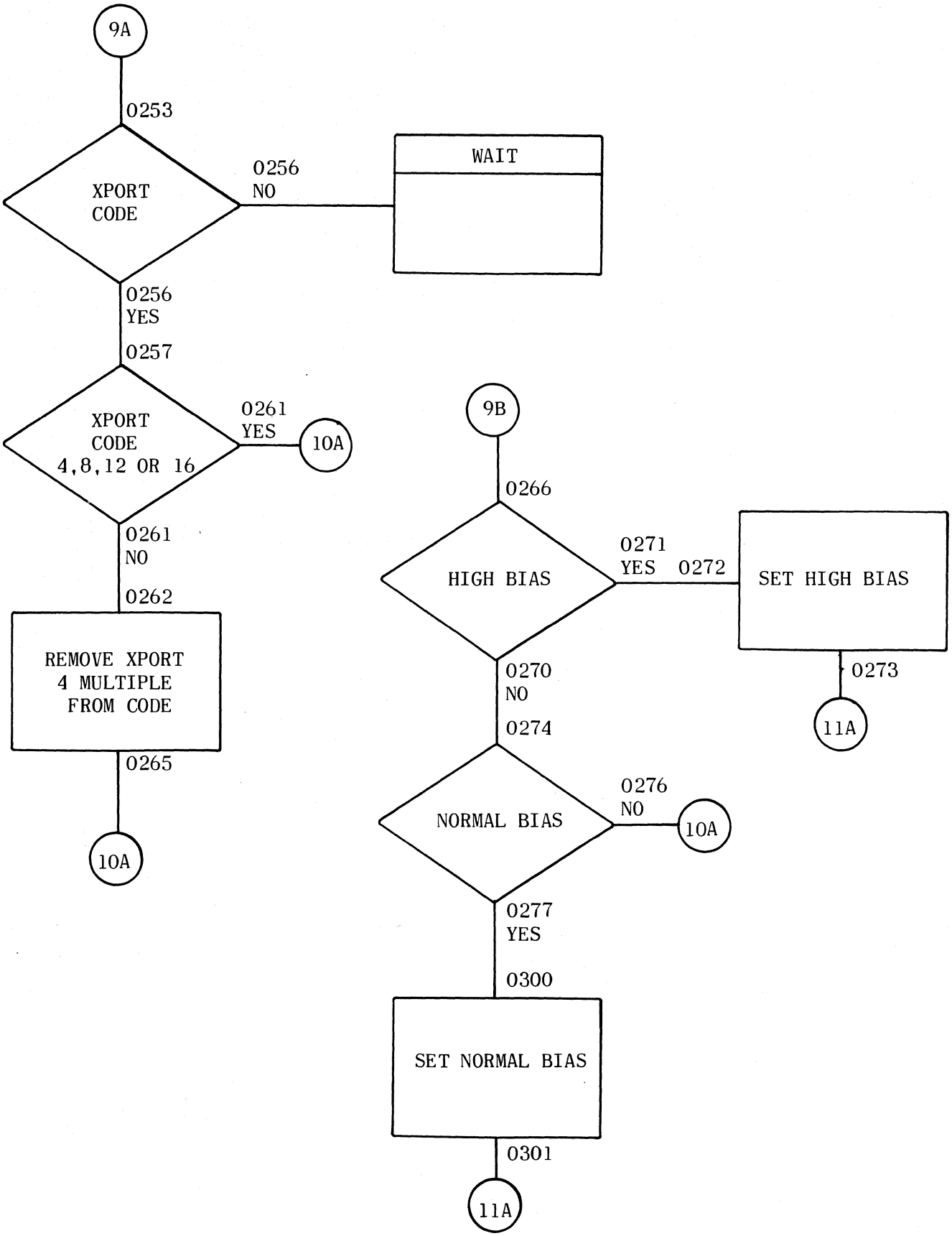


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 9 of 19)

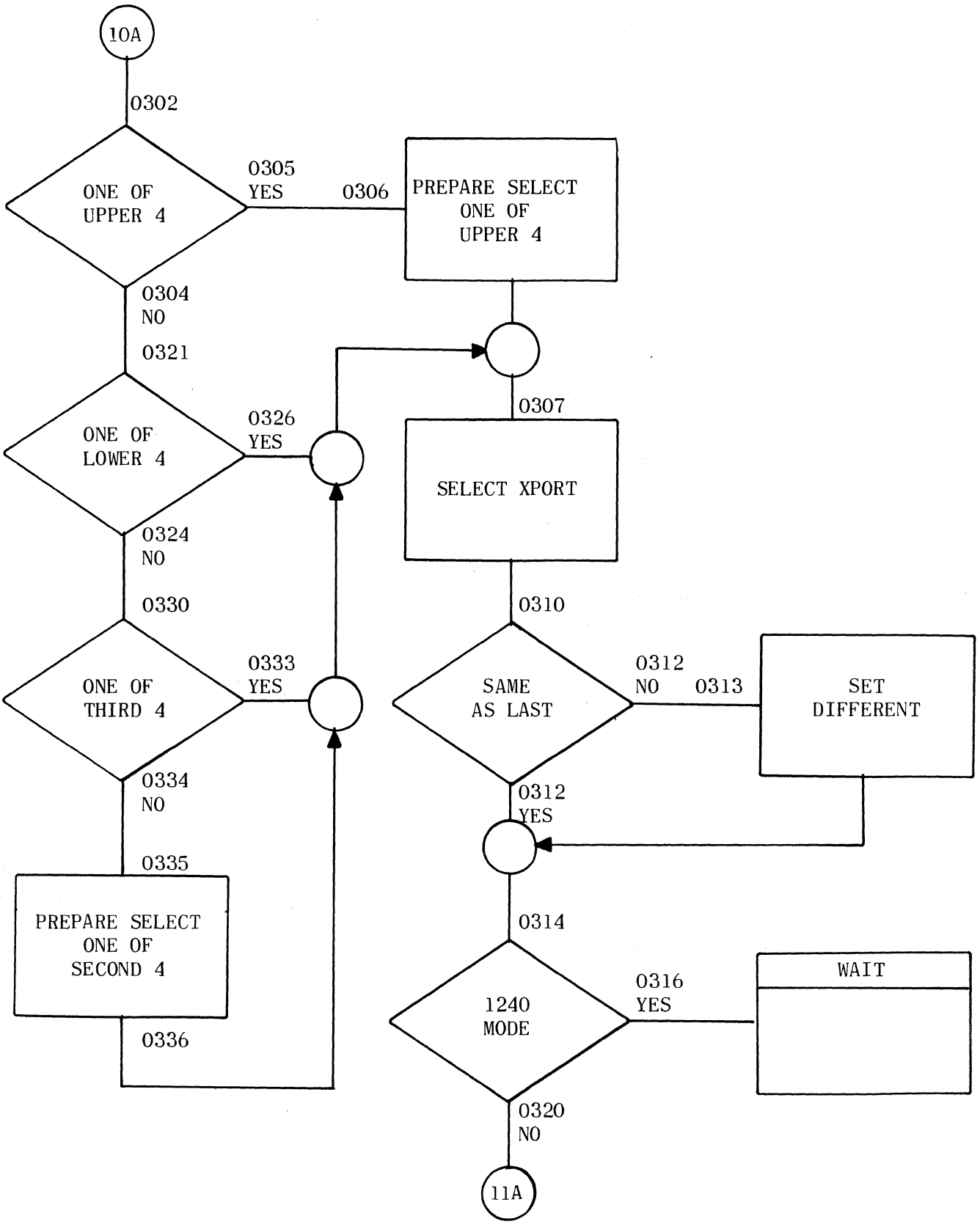


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 10 of 19)

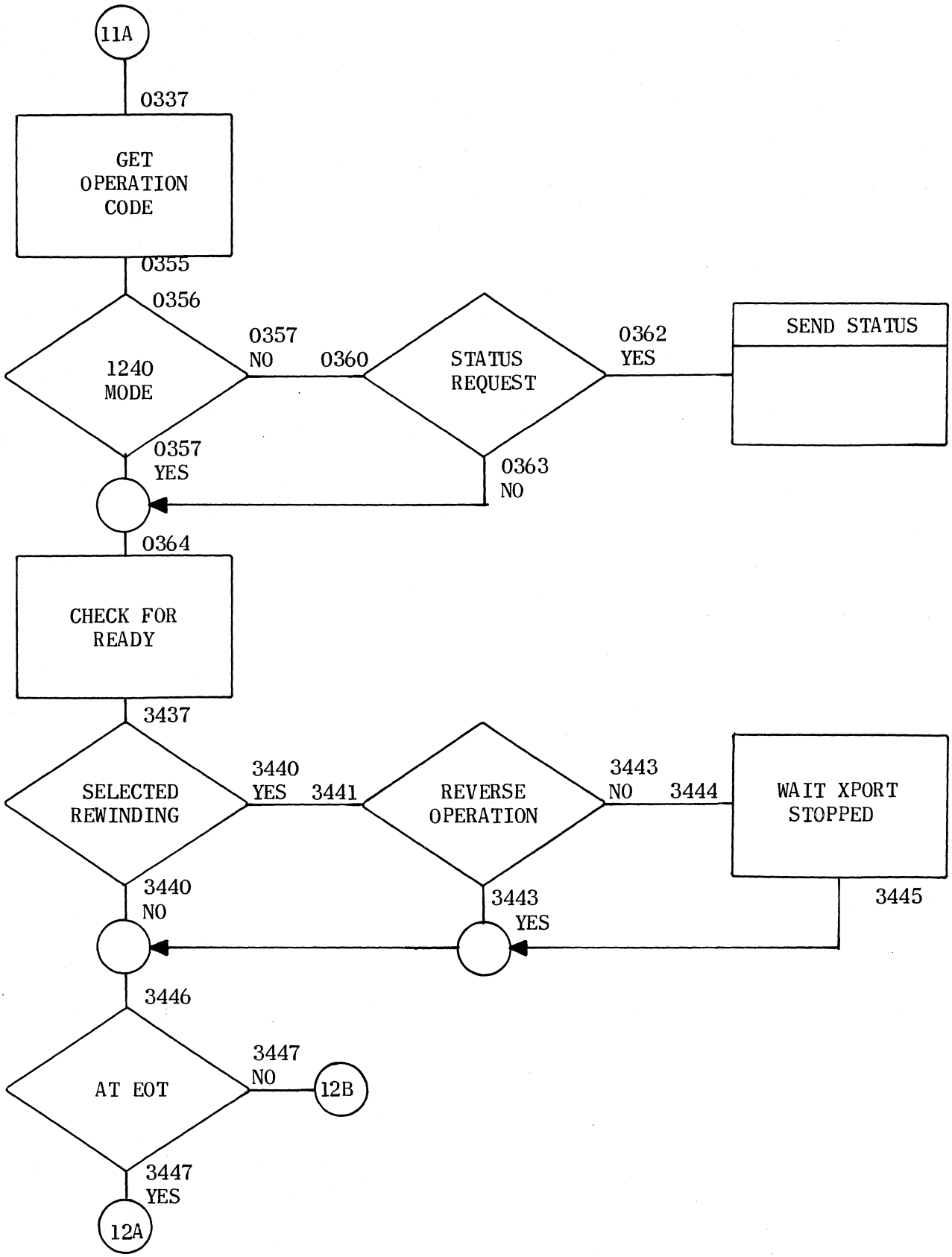


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 11 of 19)

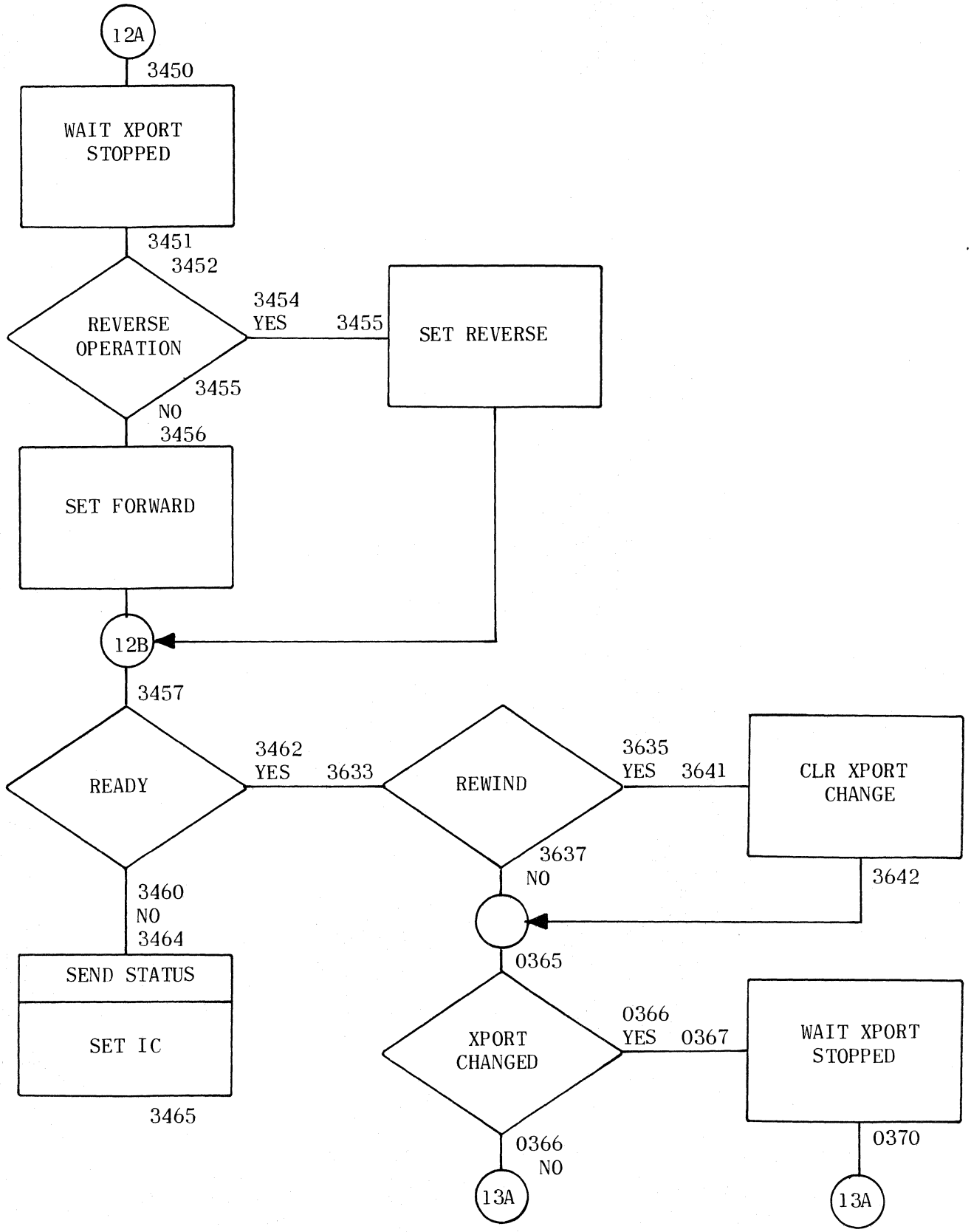


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 12 of 19)

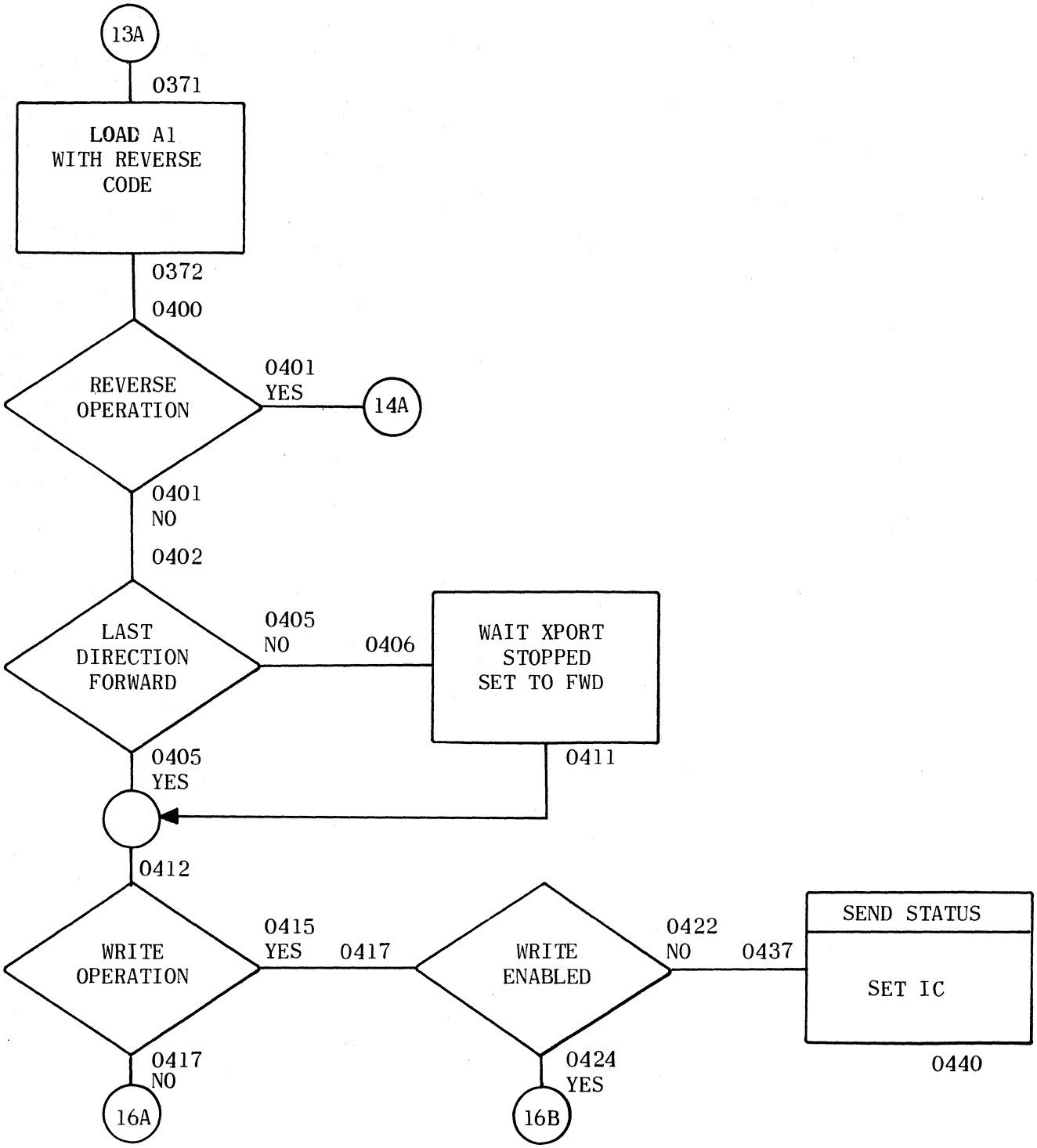


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 13 of 19)

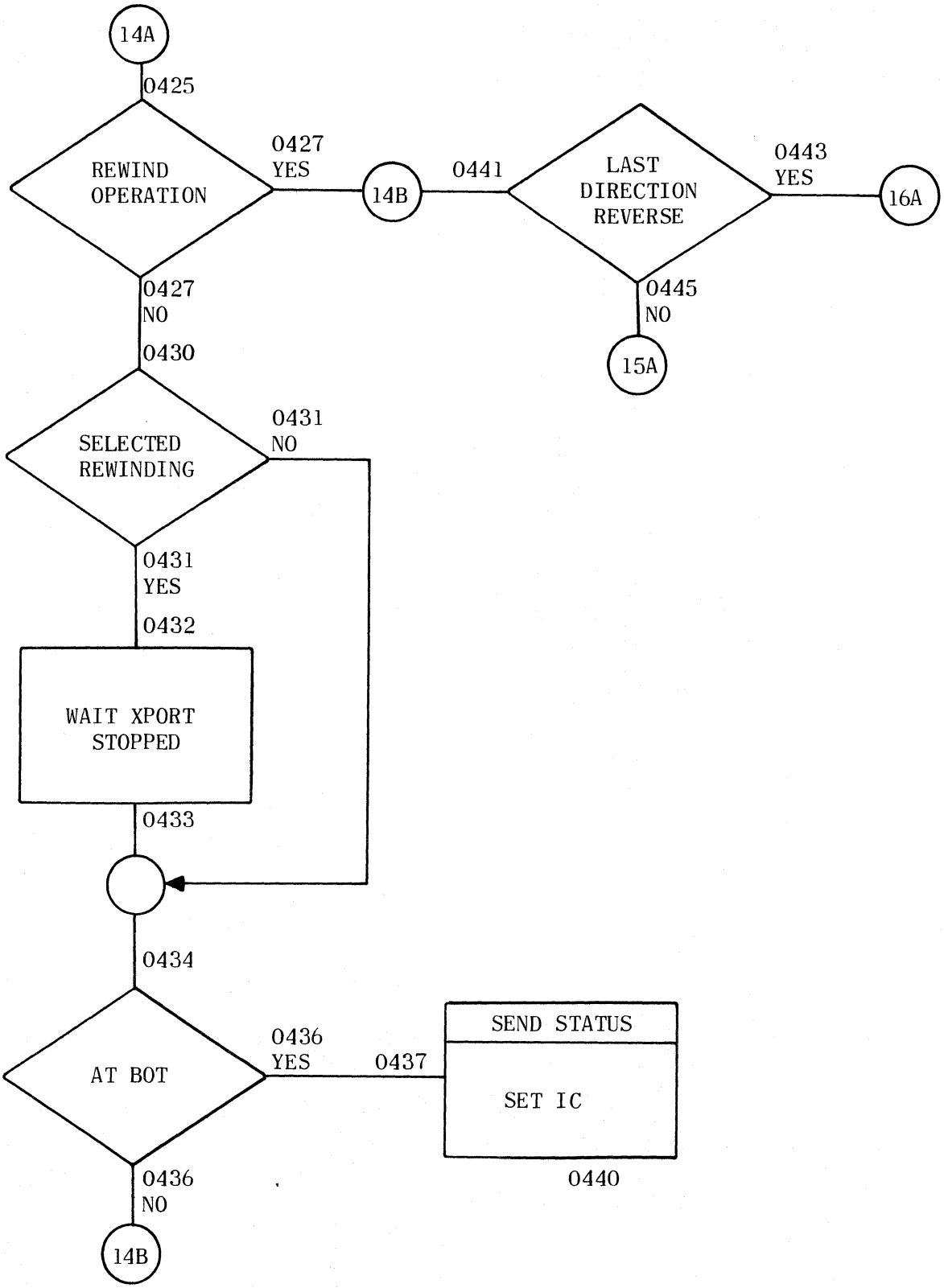


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 14 of 19)

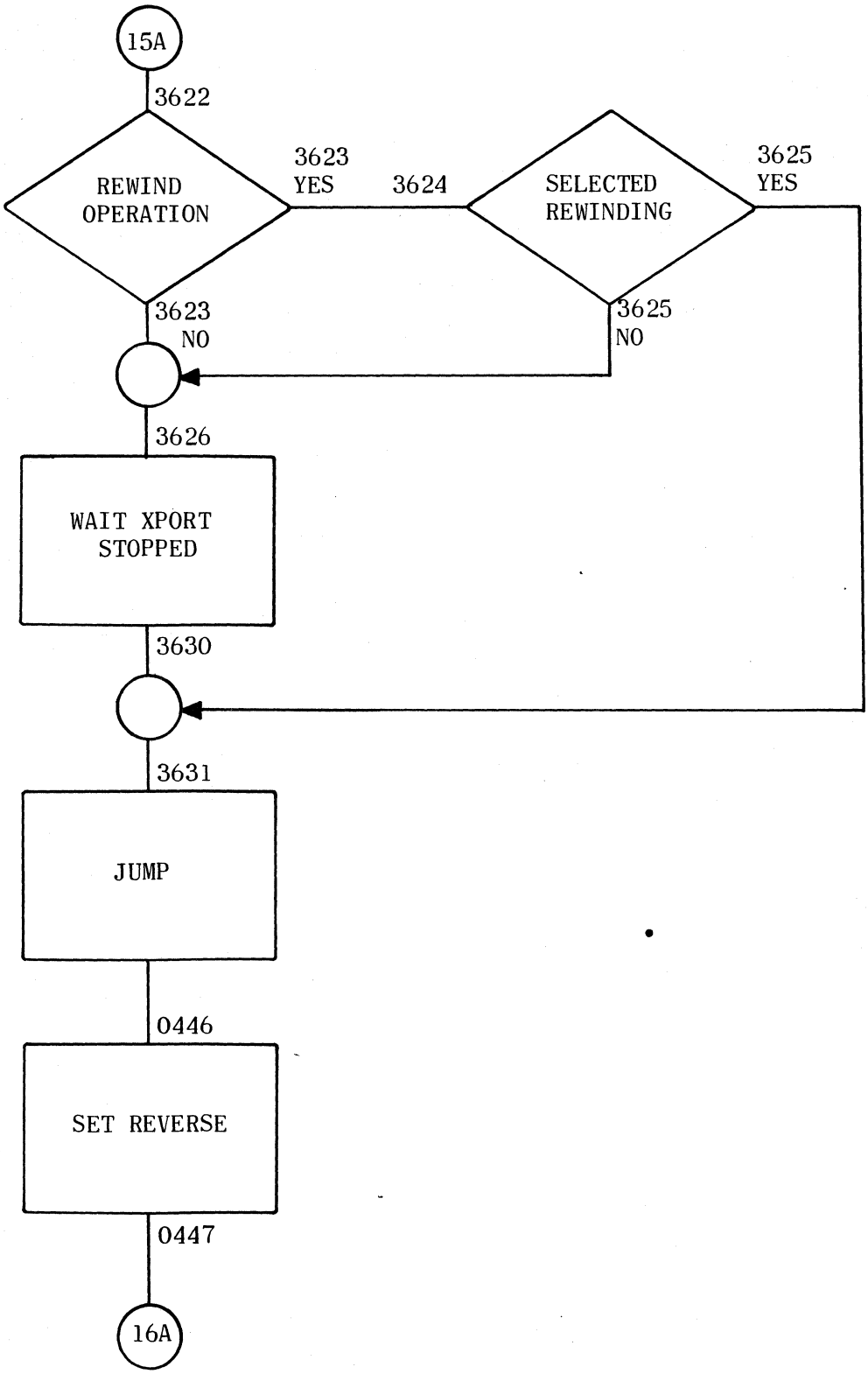


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 15 of 19)

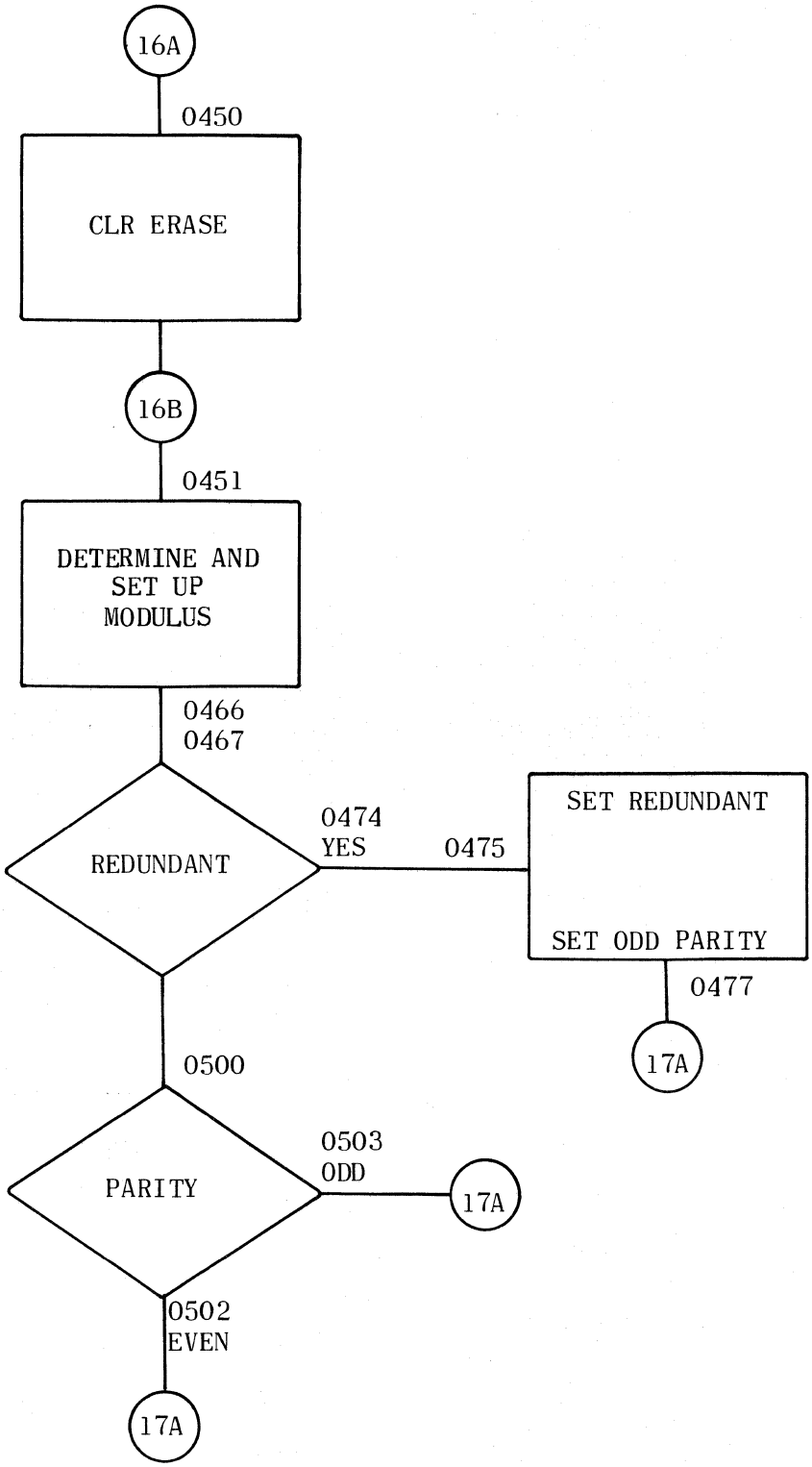


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 16 of 19)

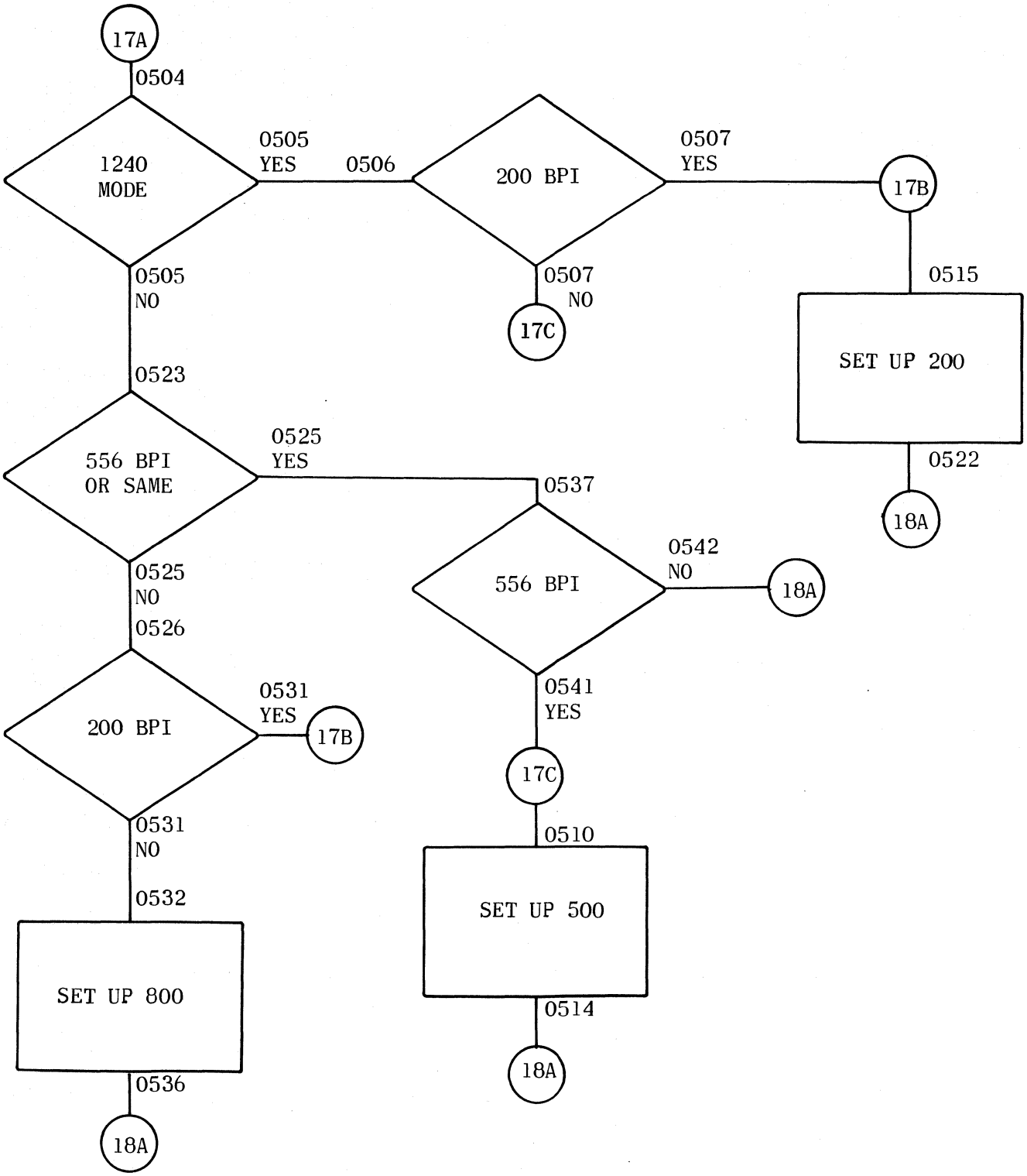


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 17 of 19)

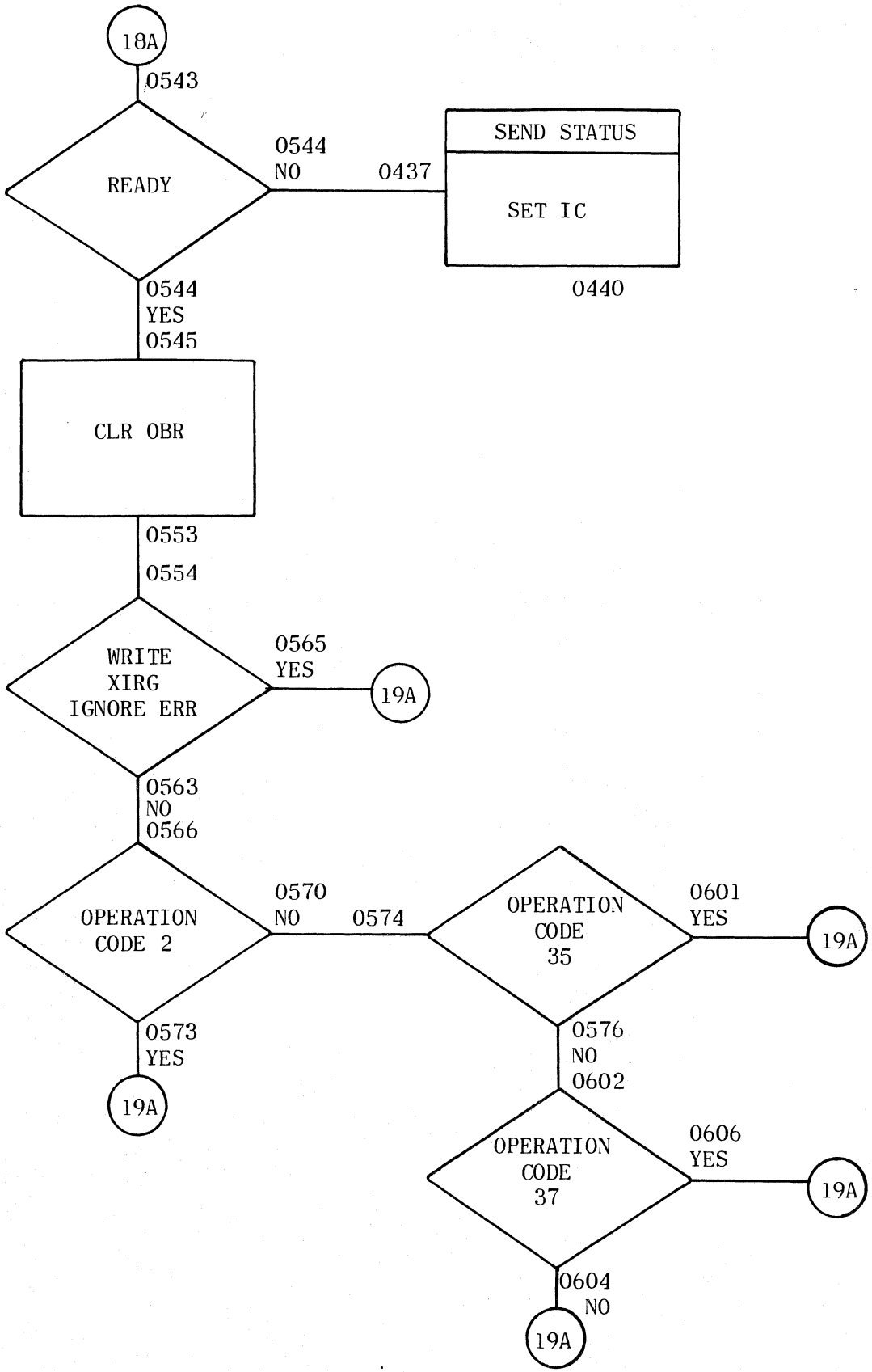


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 18 of 19)

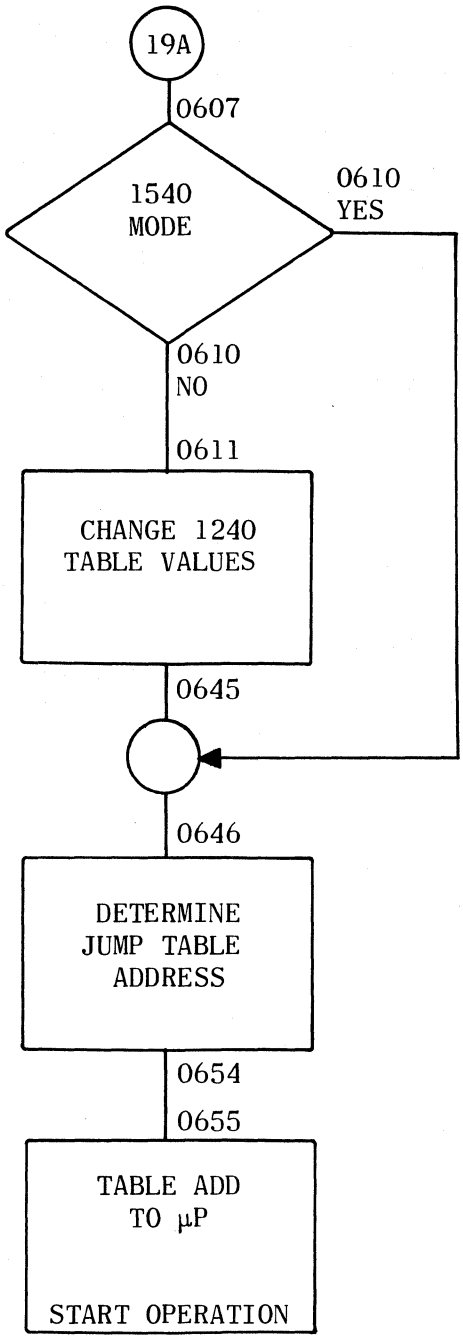


Figure 4-23. Seven Track Executive Sequence Flow Diagram (Sheet 19 of 19)

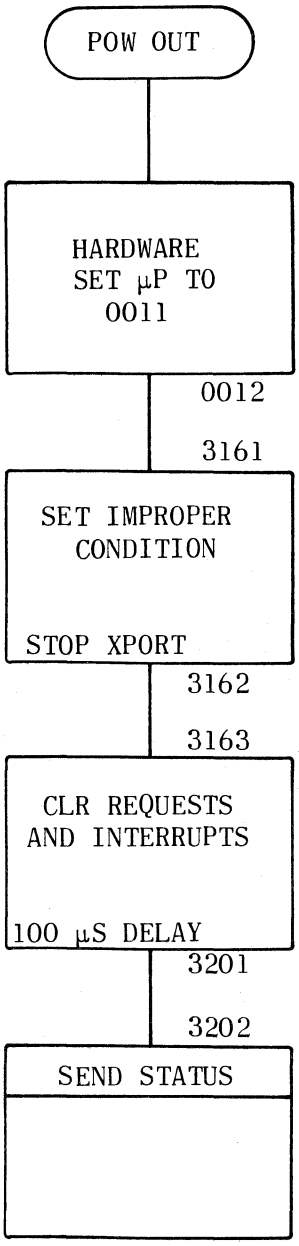


Figure 4-24. Power Out of Tolerance Sequence Flow Diagram

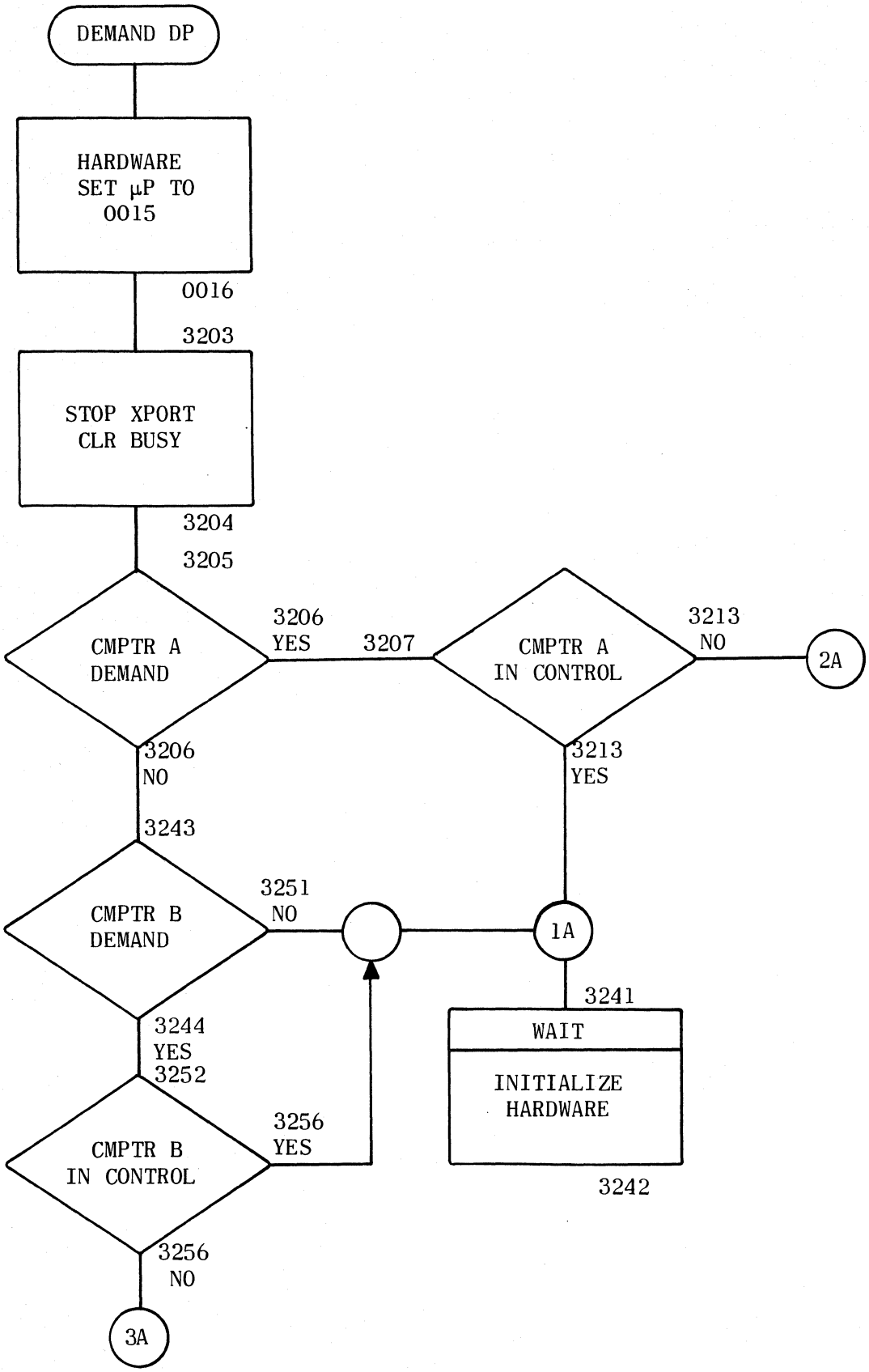


Figure 4-25. Demand Duplex Sequence Flow Diagram (Sheet 1 of 3)

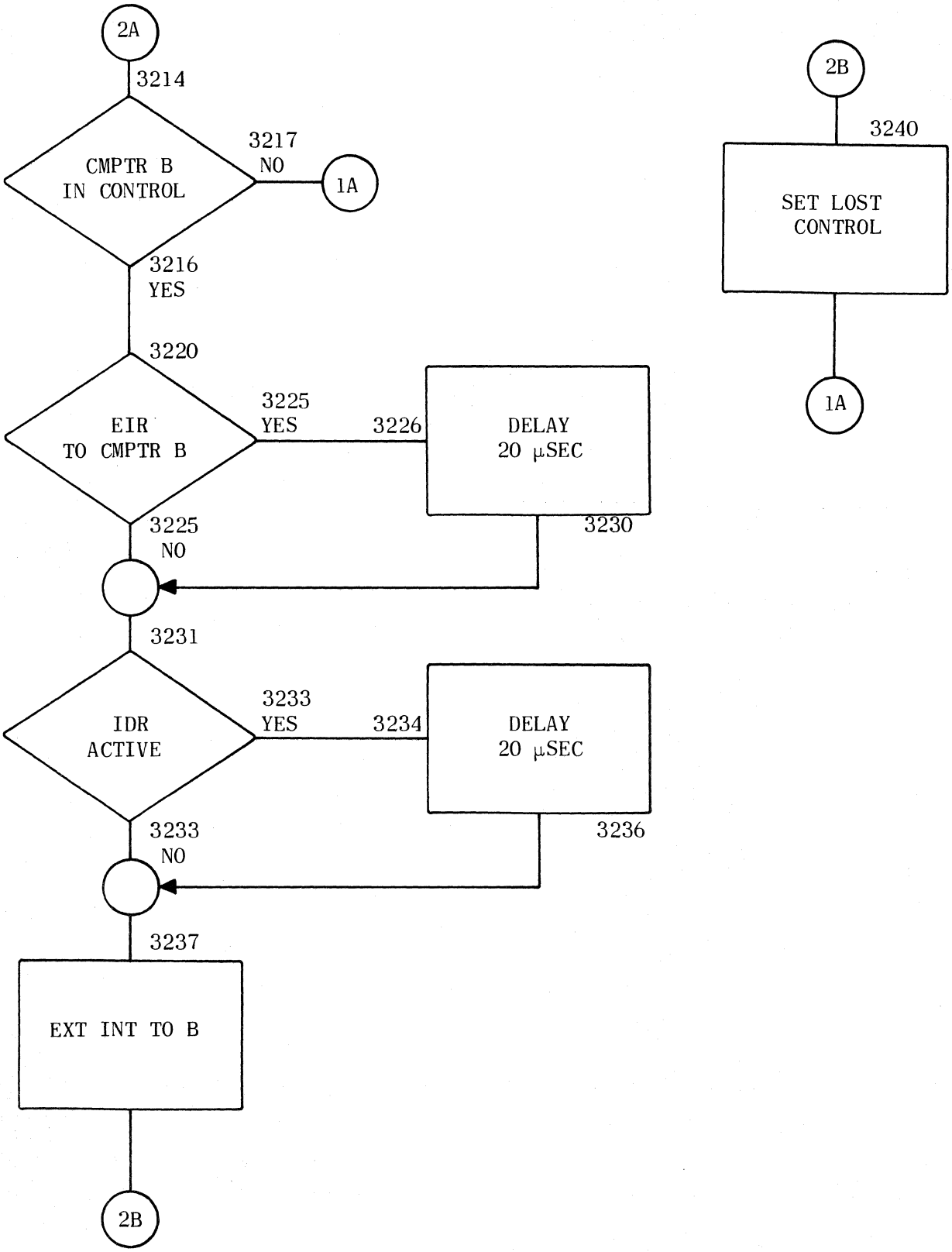


Figure 4-25. Demand Duplex Sequence Flow Diagram (Sheet 2 of 3)

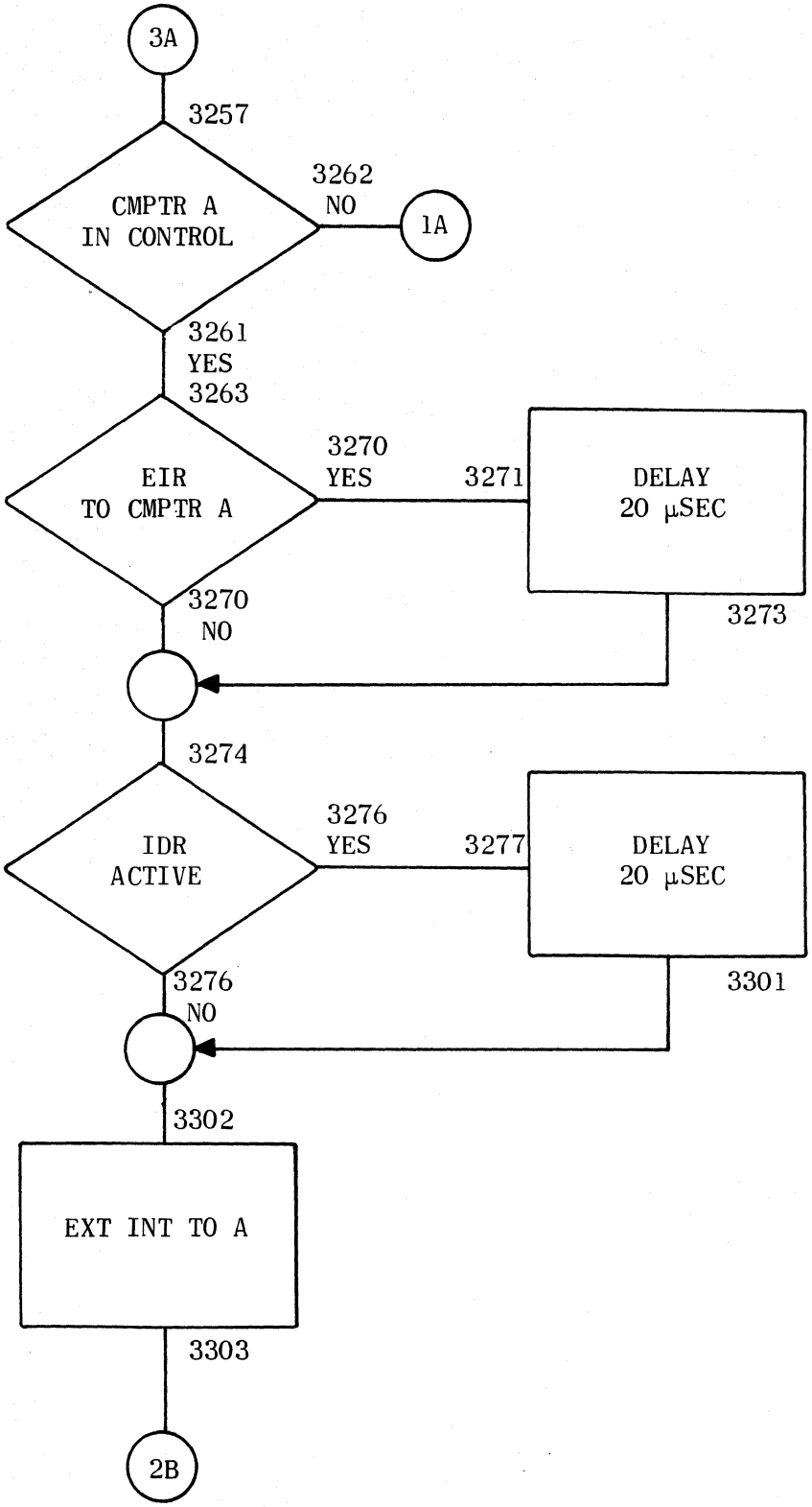


Figure 4-25. Demand Duplex Sequence Flow Diagram (Sheet 3 of 3)

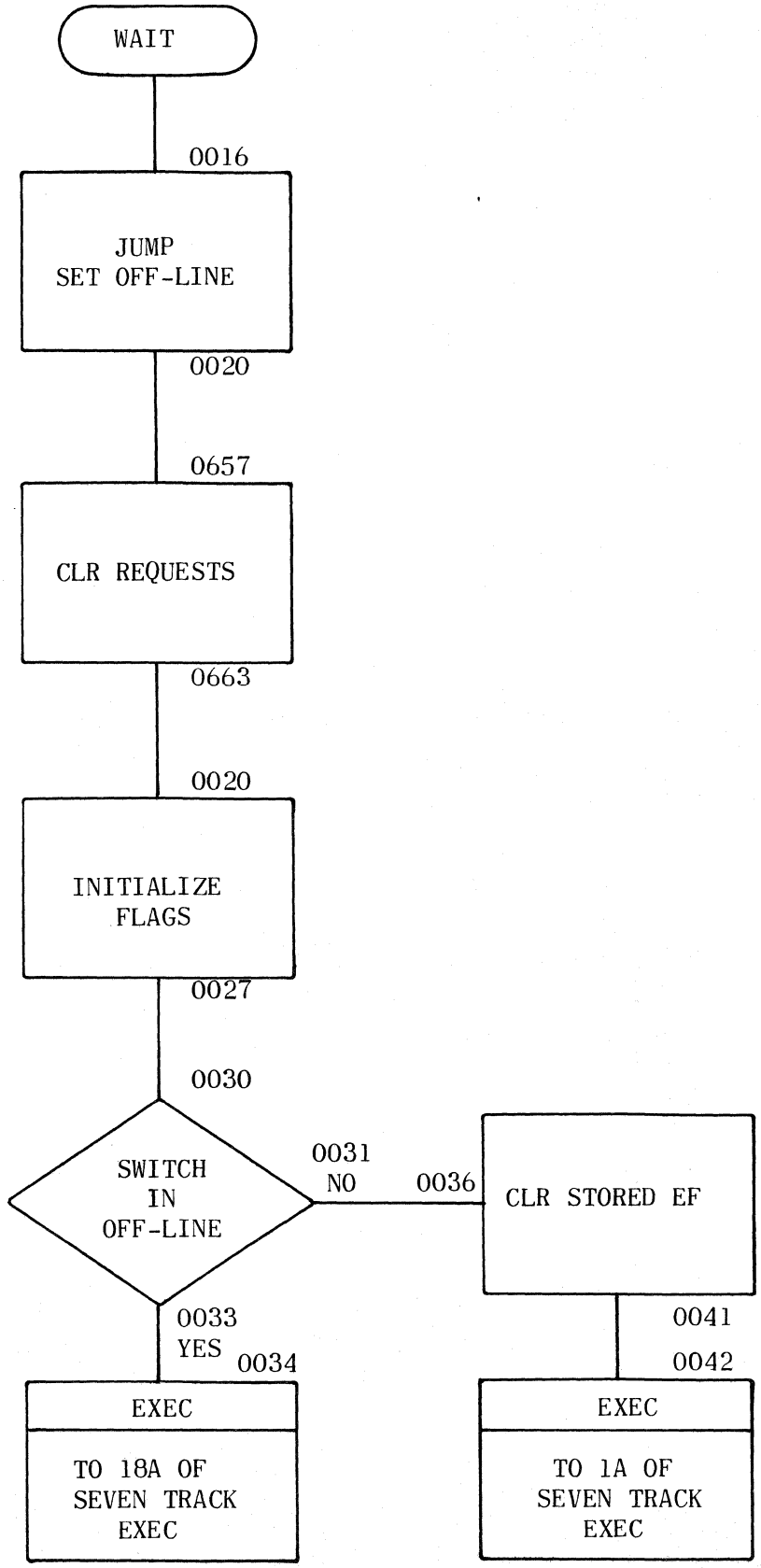


Figure 4-26. Wait Sequence Flow Diagram

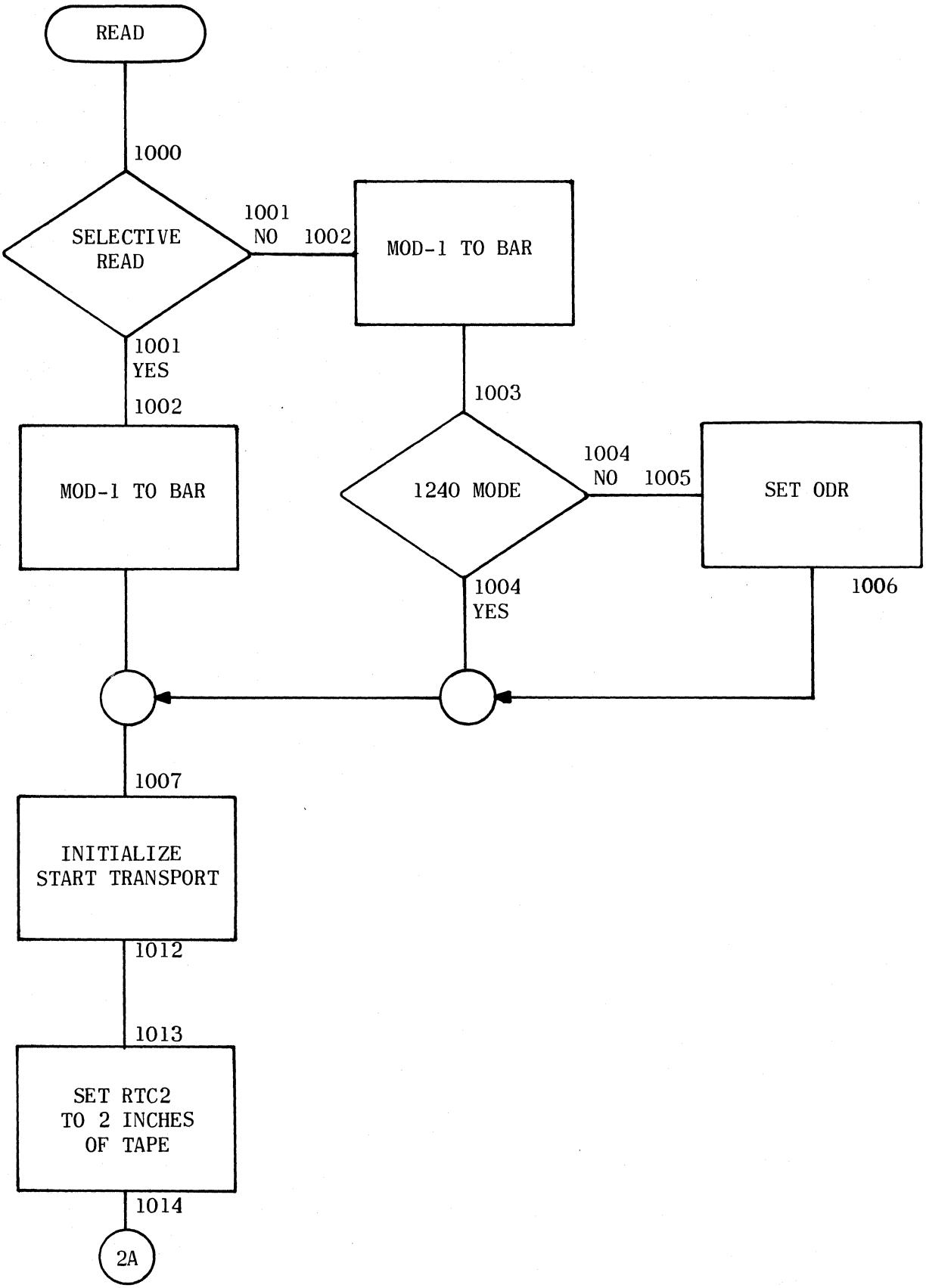


Figure 4-27. Read Initiation Sequence Flow Diagram (Sheet 1 of 2)

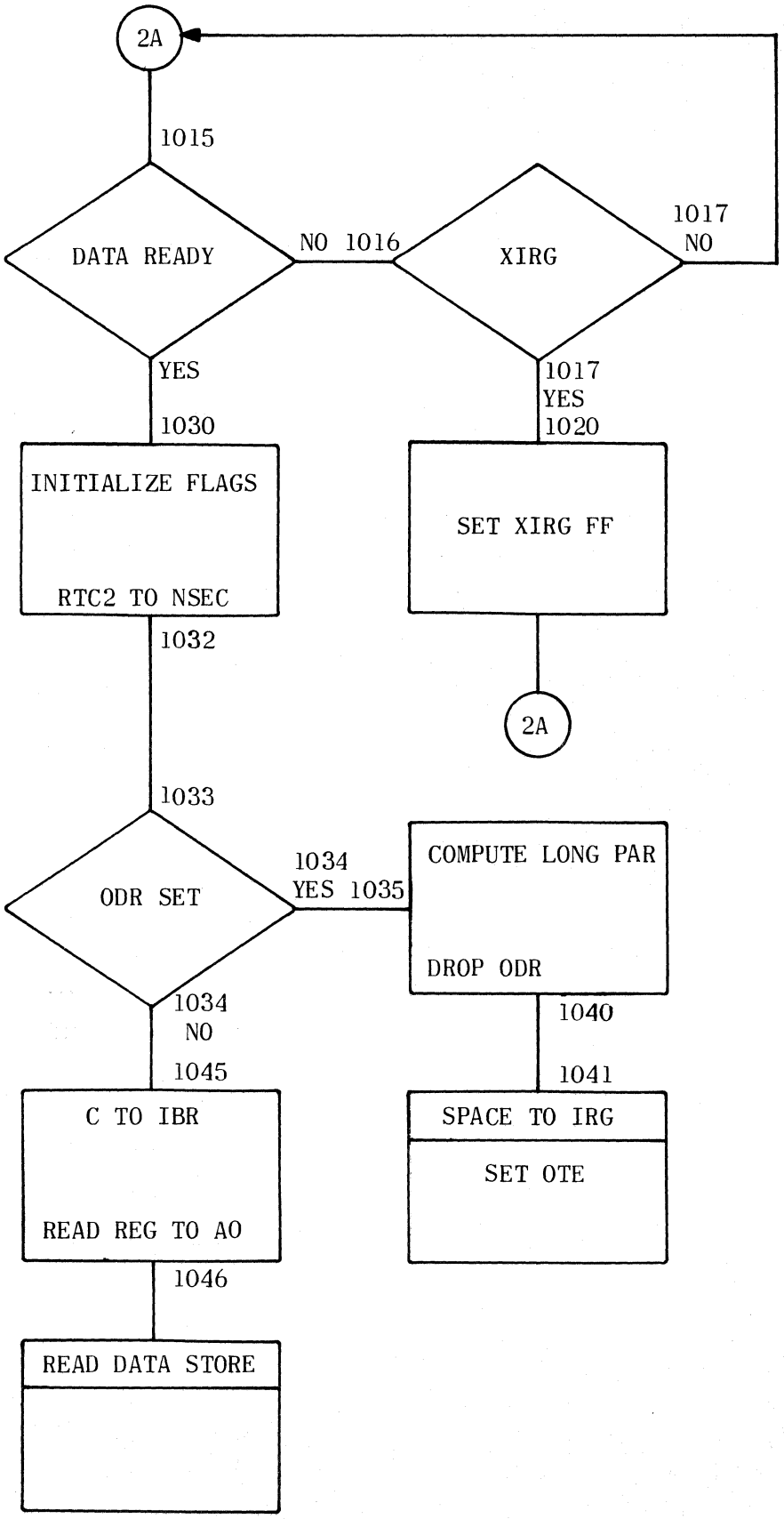


Figure 4-27. Read Initiation Sequence Flow Diagram (Sheet 2 of 2)

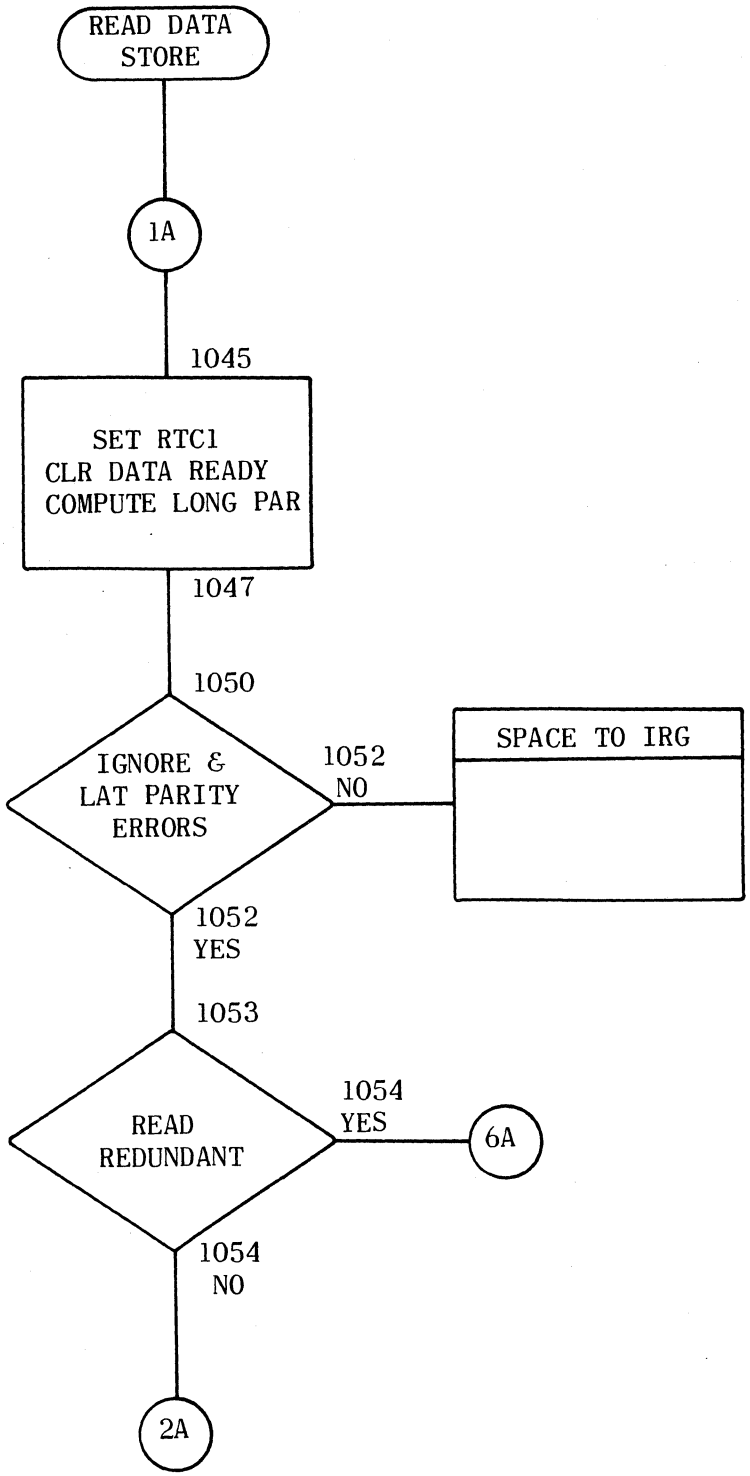


Figure 4-28. Read Data Store Sequence Flow Diagram (Sheet 1 of 6)

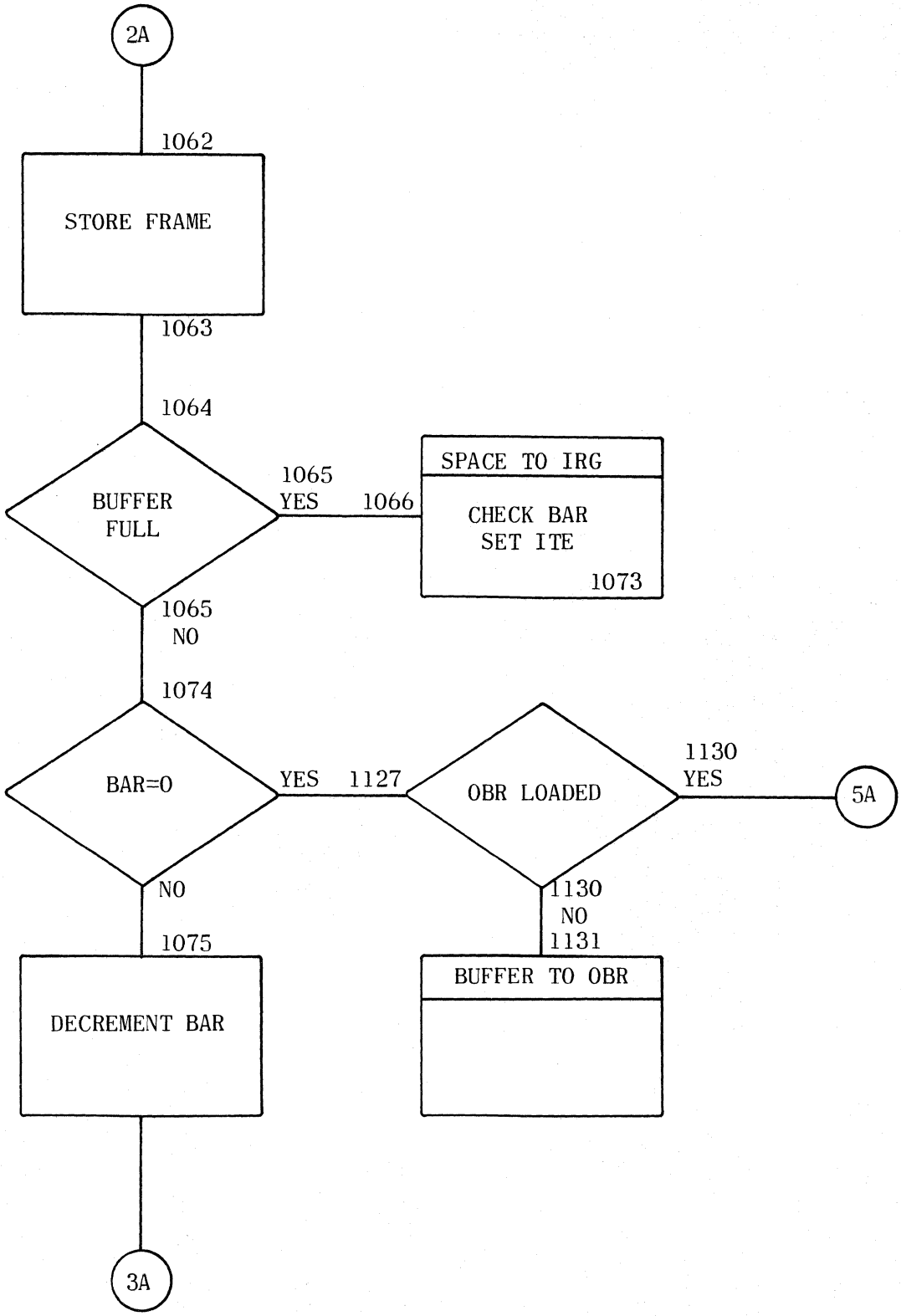


Figure 4-28. Read Data Store Sequence Flow Diagram (Sheet 2 of 6)

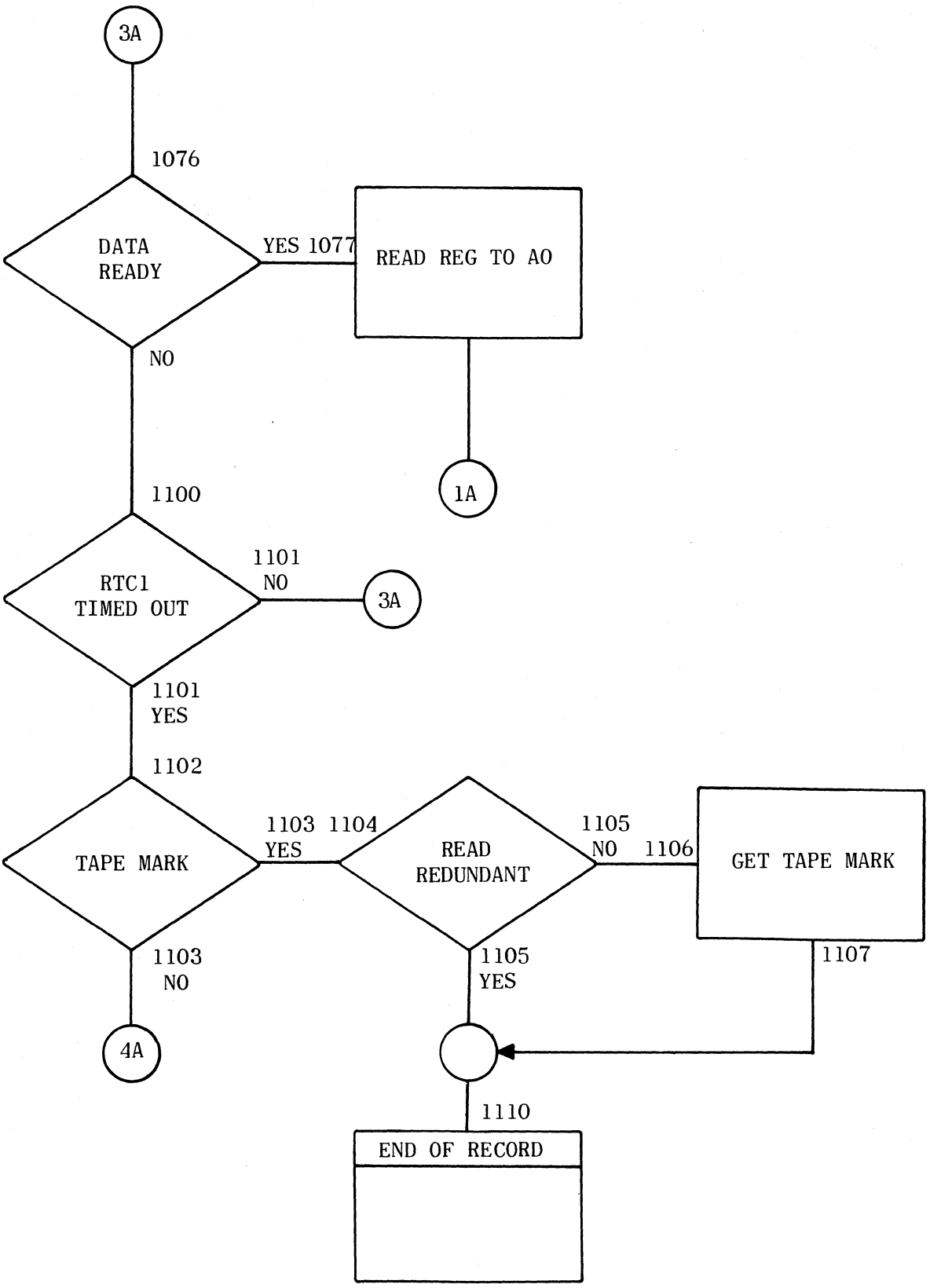


Figure 4-28. Read Data Store Sequence Flow Diagram (Sheet 3 of 6)

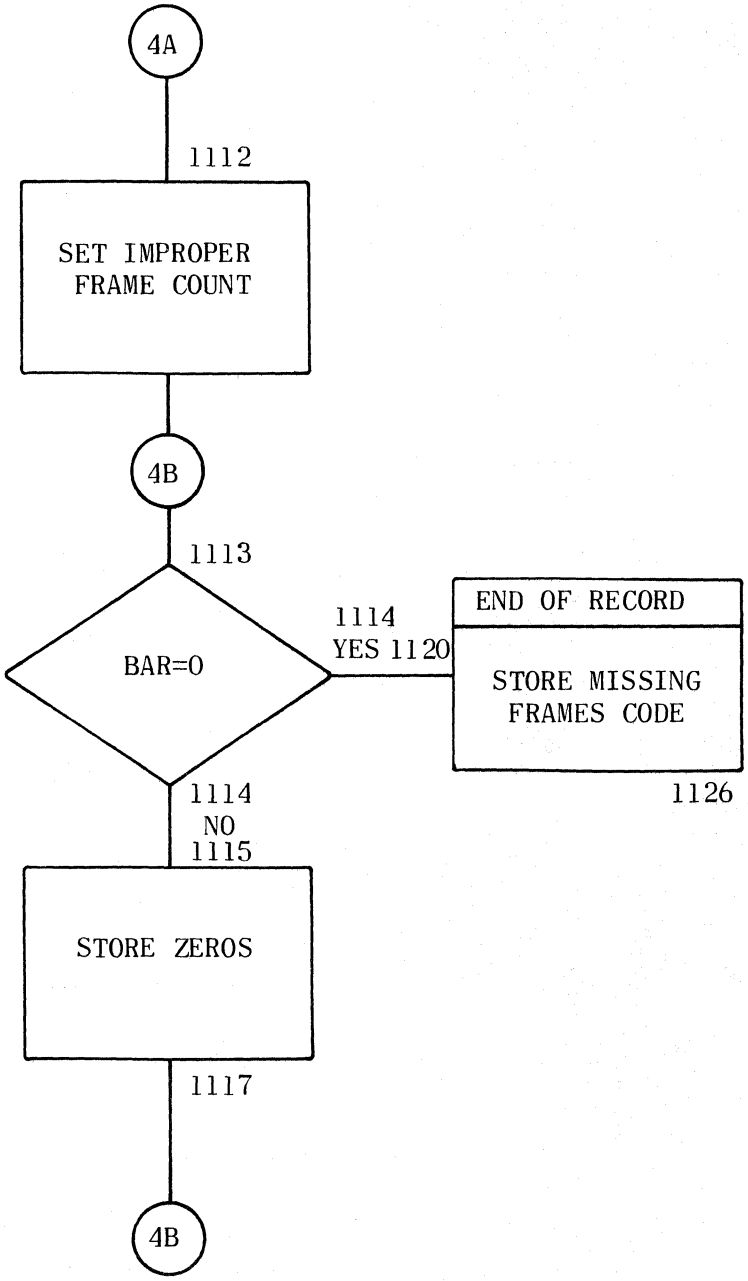


Figure 4-28. Read Data Store Sequence Flow Diagram (Sheet 4 of 6)

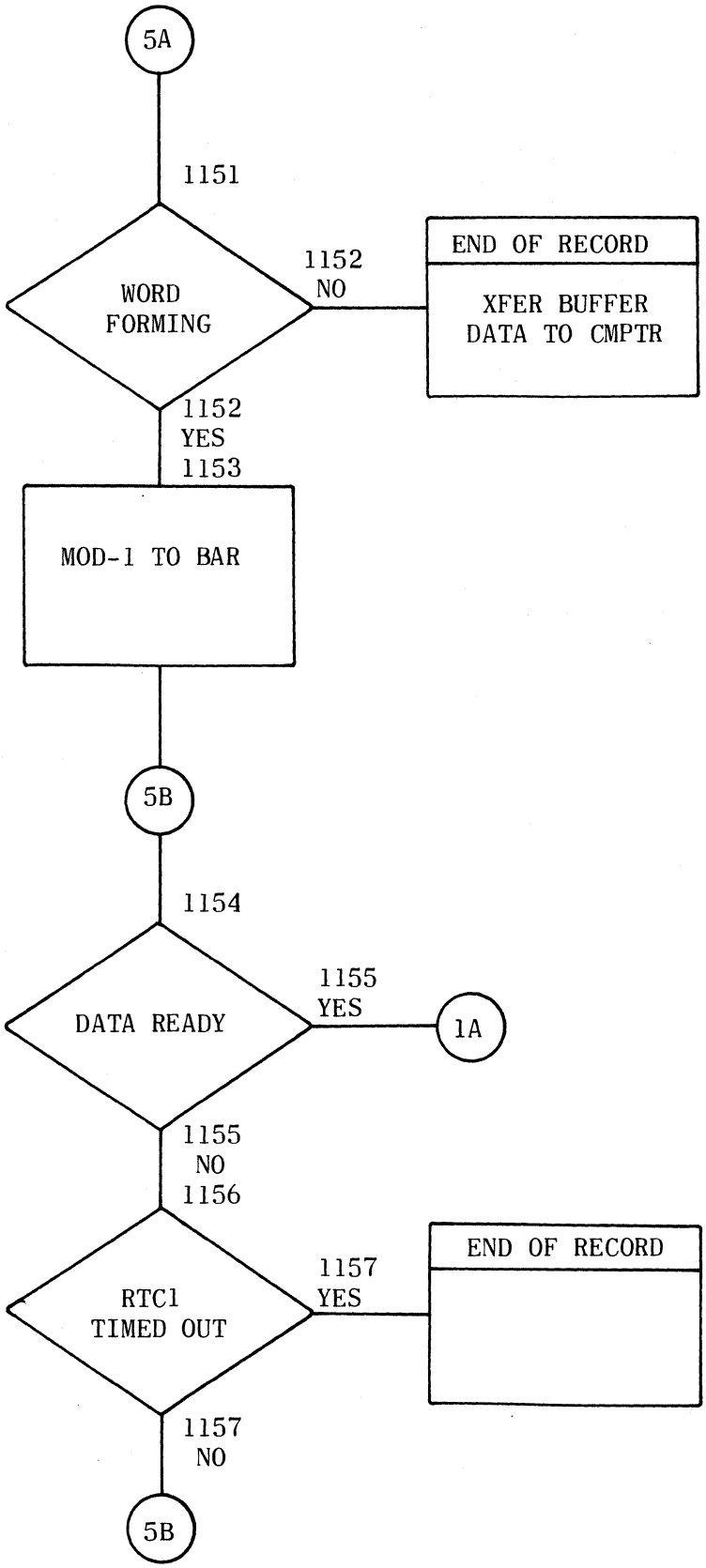


Figure 4-28. Read Data Store Sequence Flow Diagram (Sheet 5 of 6)

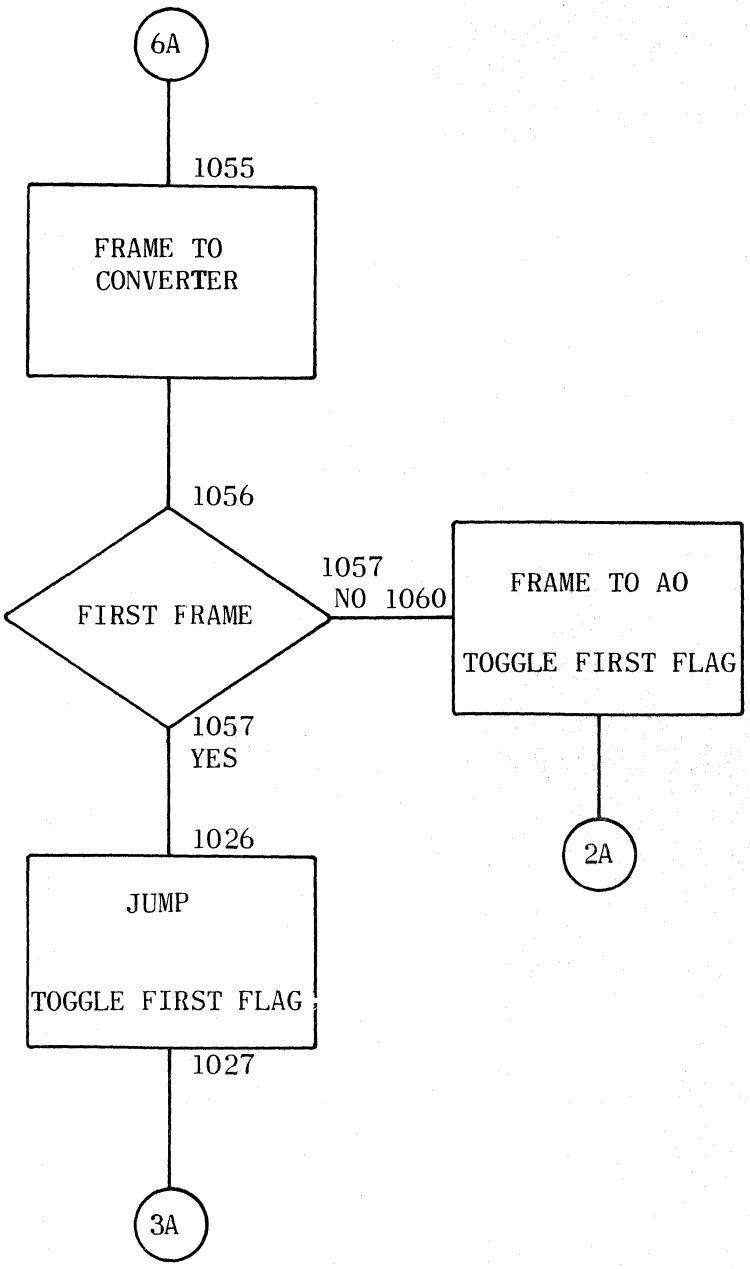


Figure 4-28. Read Data Store Sequence Flow Diagram (Sheet 6 of 6)

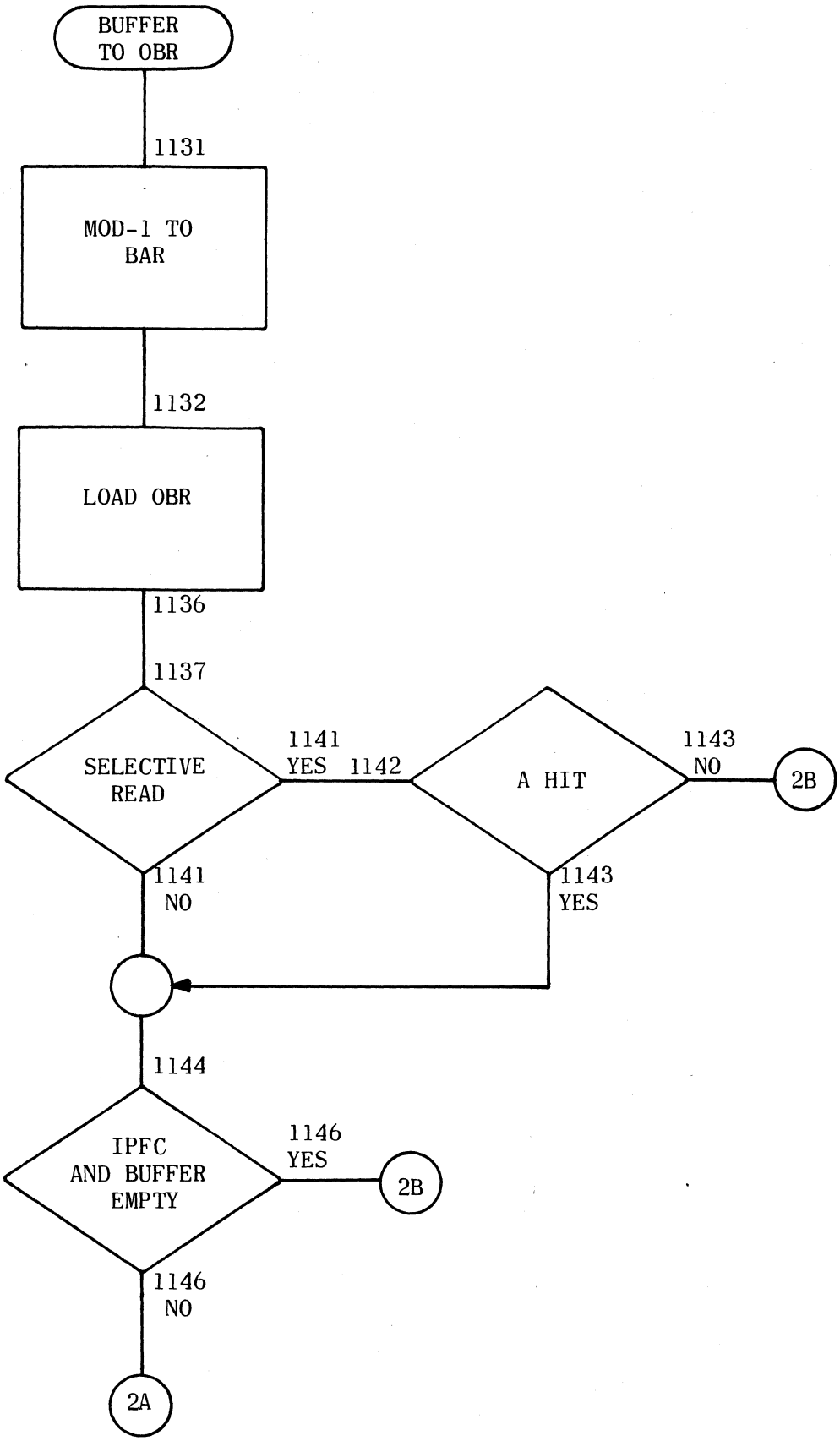


Figure 4-29. Buffer to OBR Sequence Flow Diagram (Sheet 1 of 2)

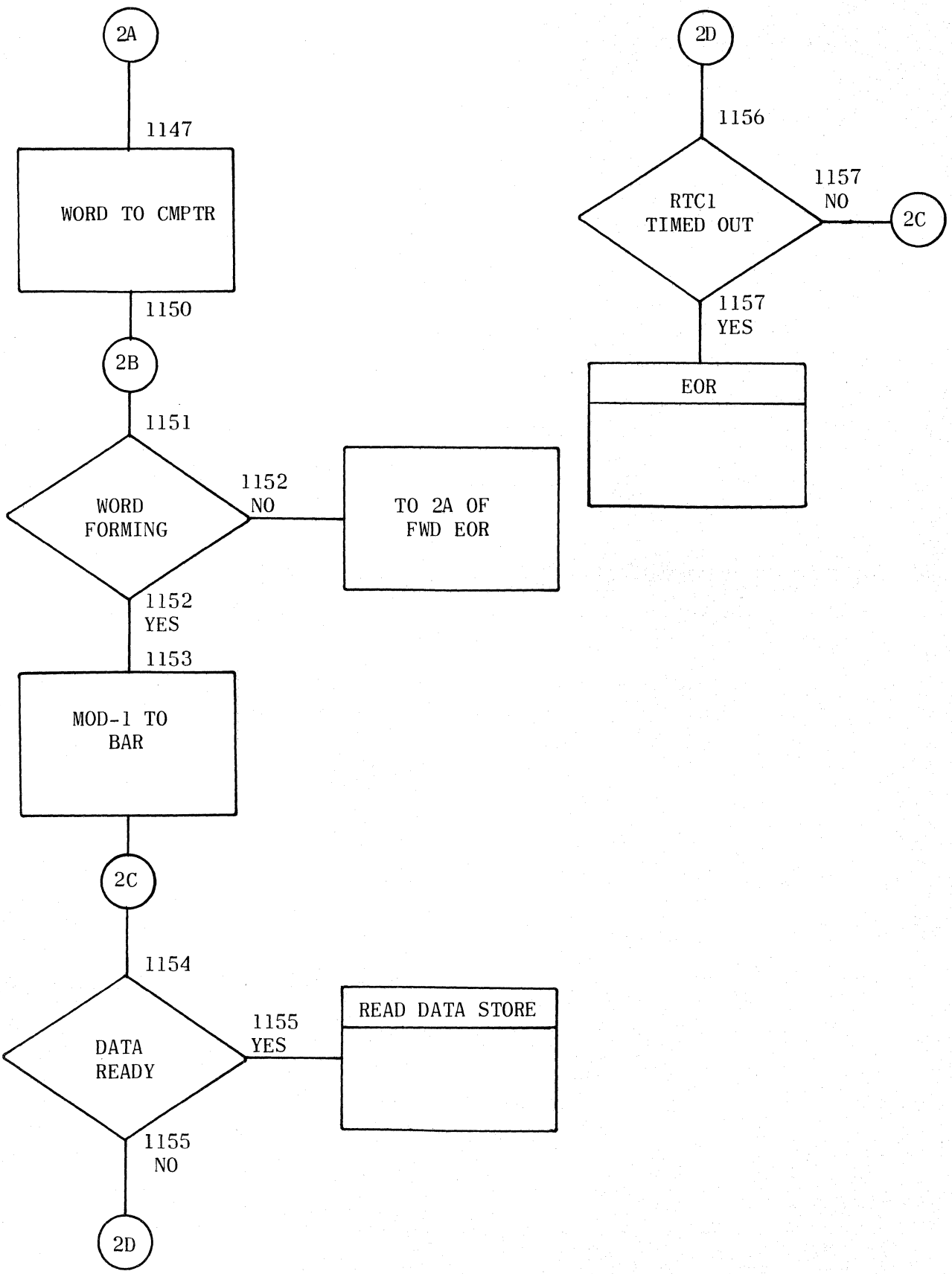


Figure 4-29. Buffer to OBR Sequence Flow Diagram (Sheet 2 of 2)

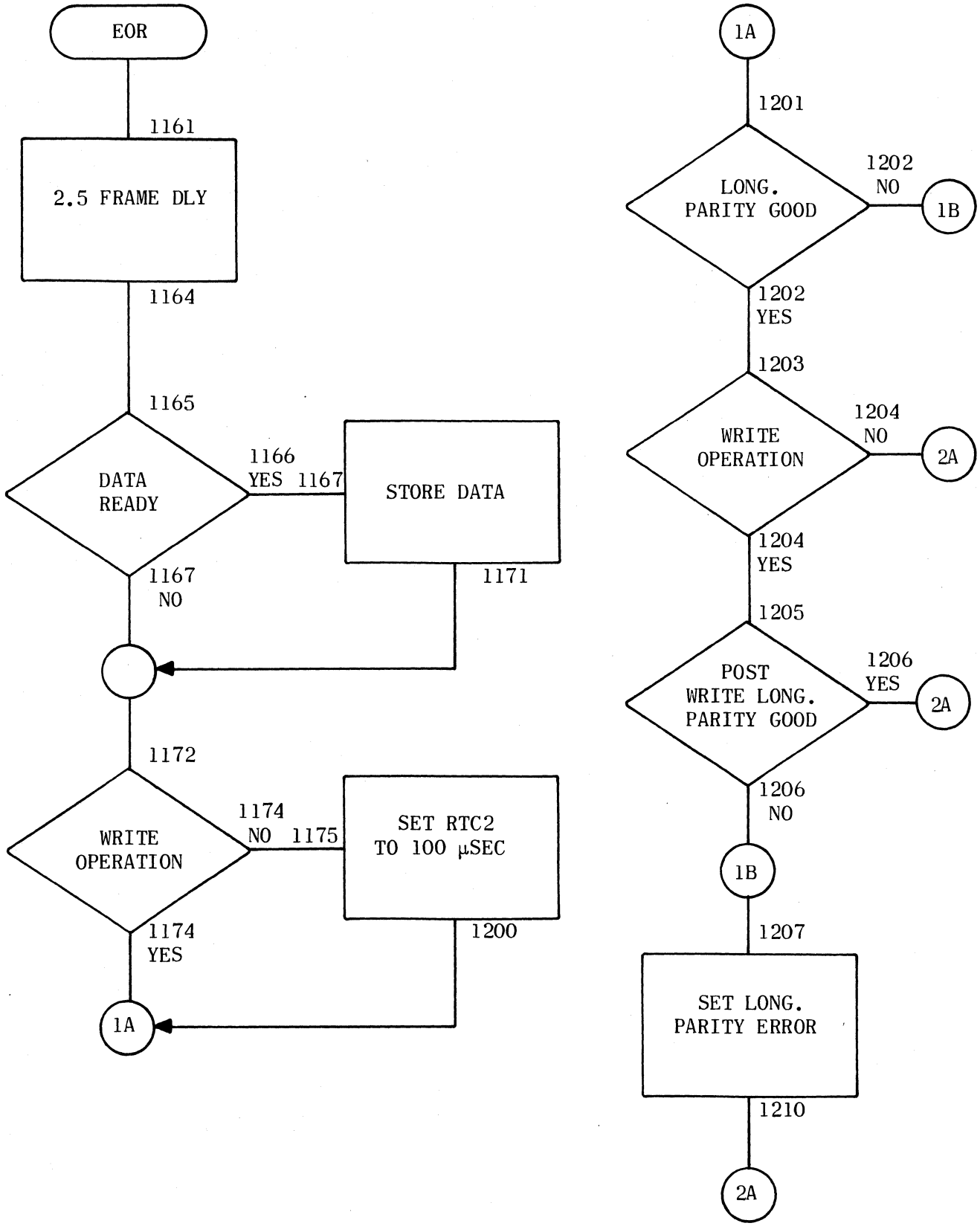


Figure 4-30. Forward End of Record Sequence Flow Diagram (Sheet 1 of 4)

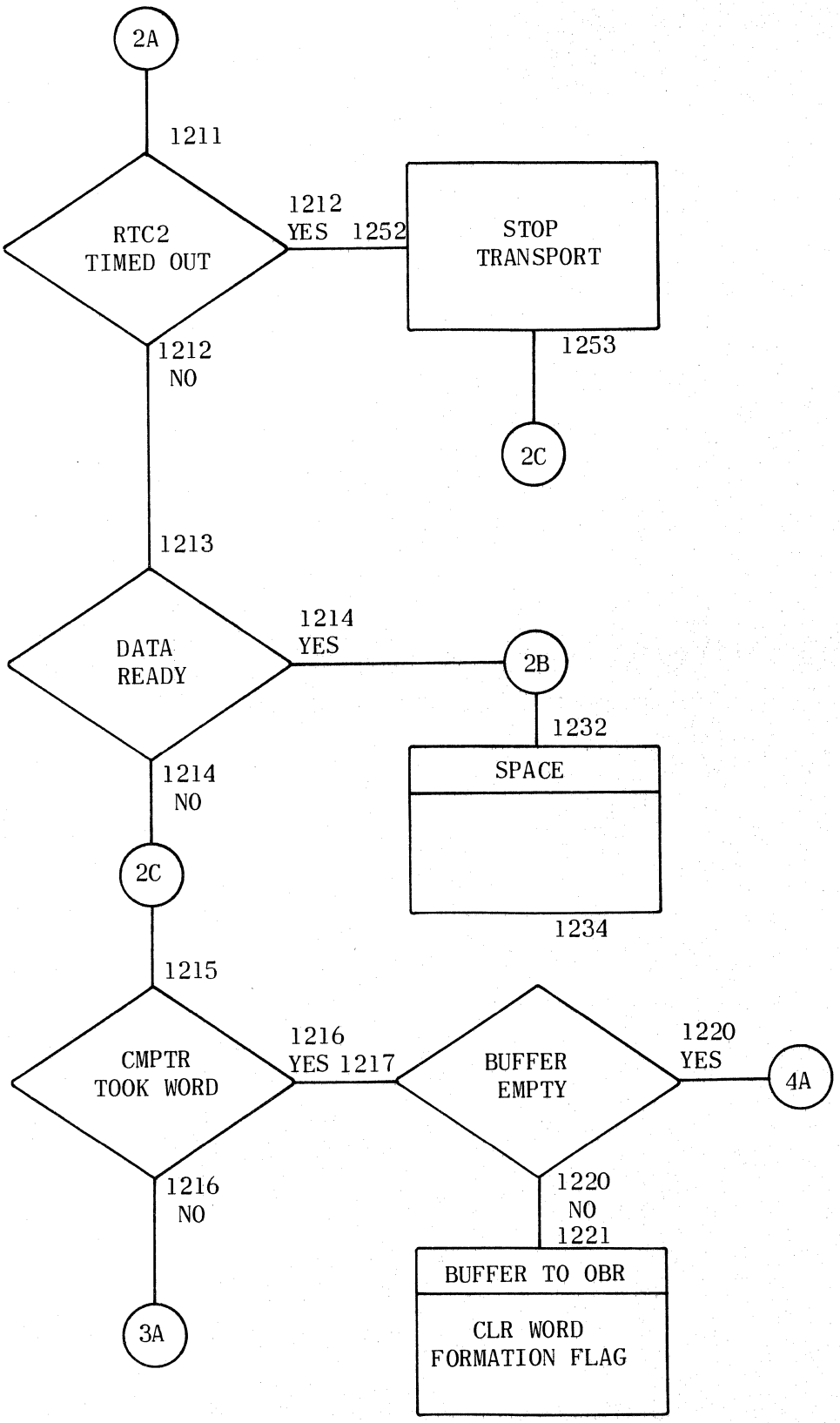


Figure 4-30. Forward End of Record Sequence Flow Diagram (Sheet 2 of 4)

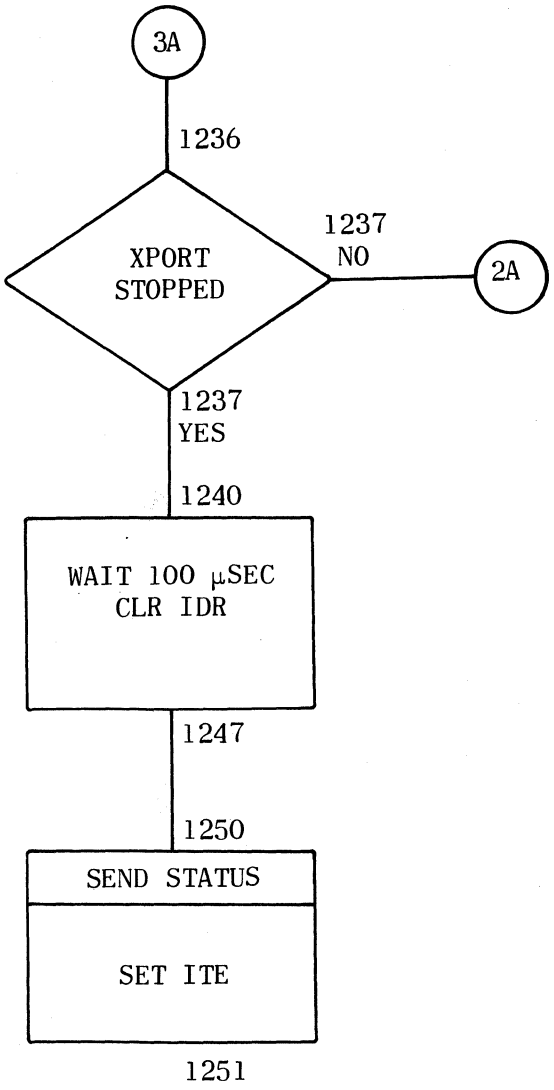


Figure 4-30. Forward End of Record Sequence Flow Diagram (Sheet 3 of 4)

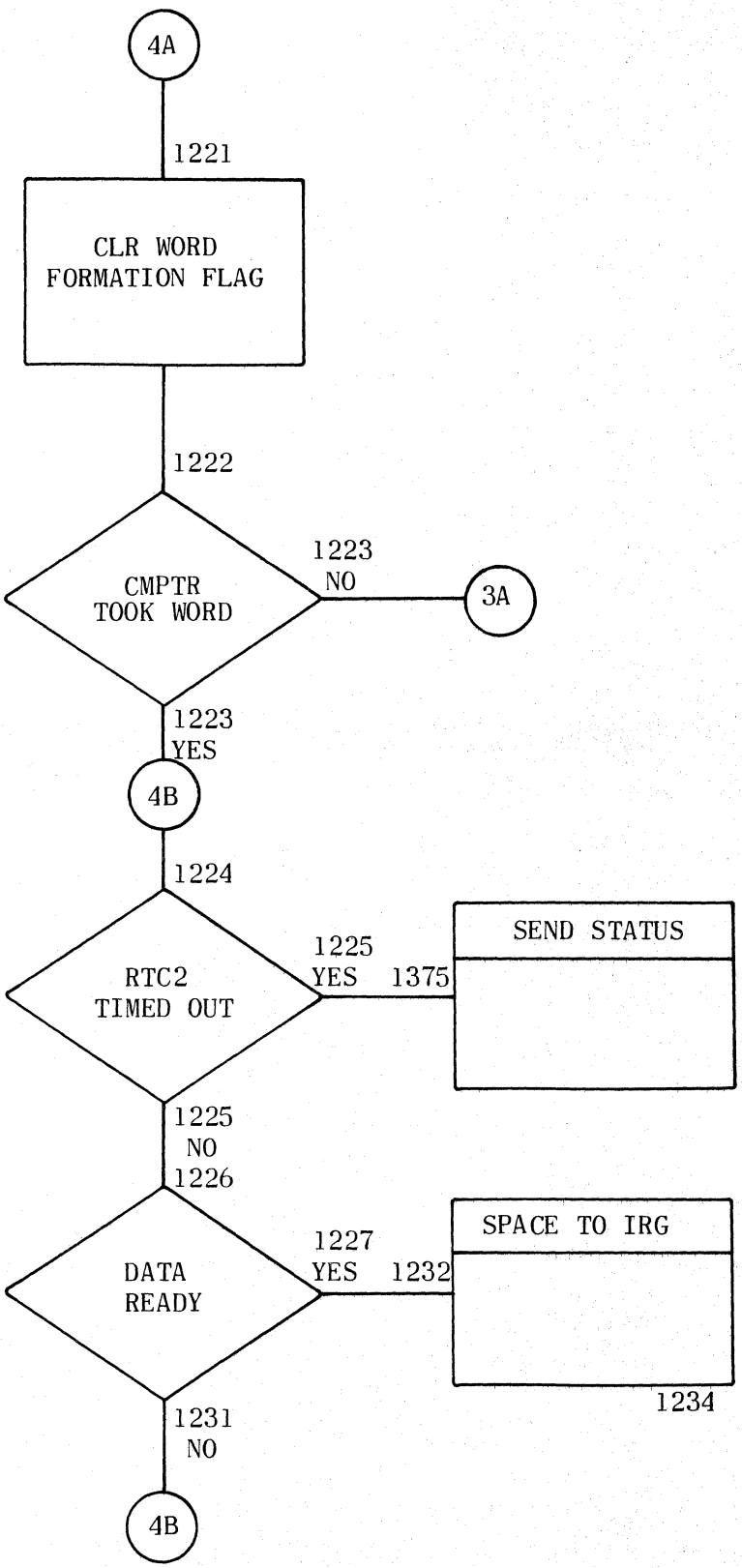


Figure 4-30. Forward End of Record Sequence Flow Diagram (Sheet 4 of 4)

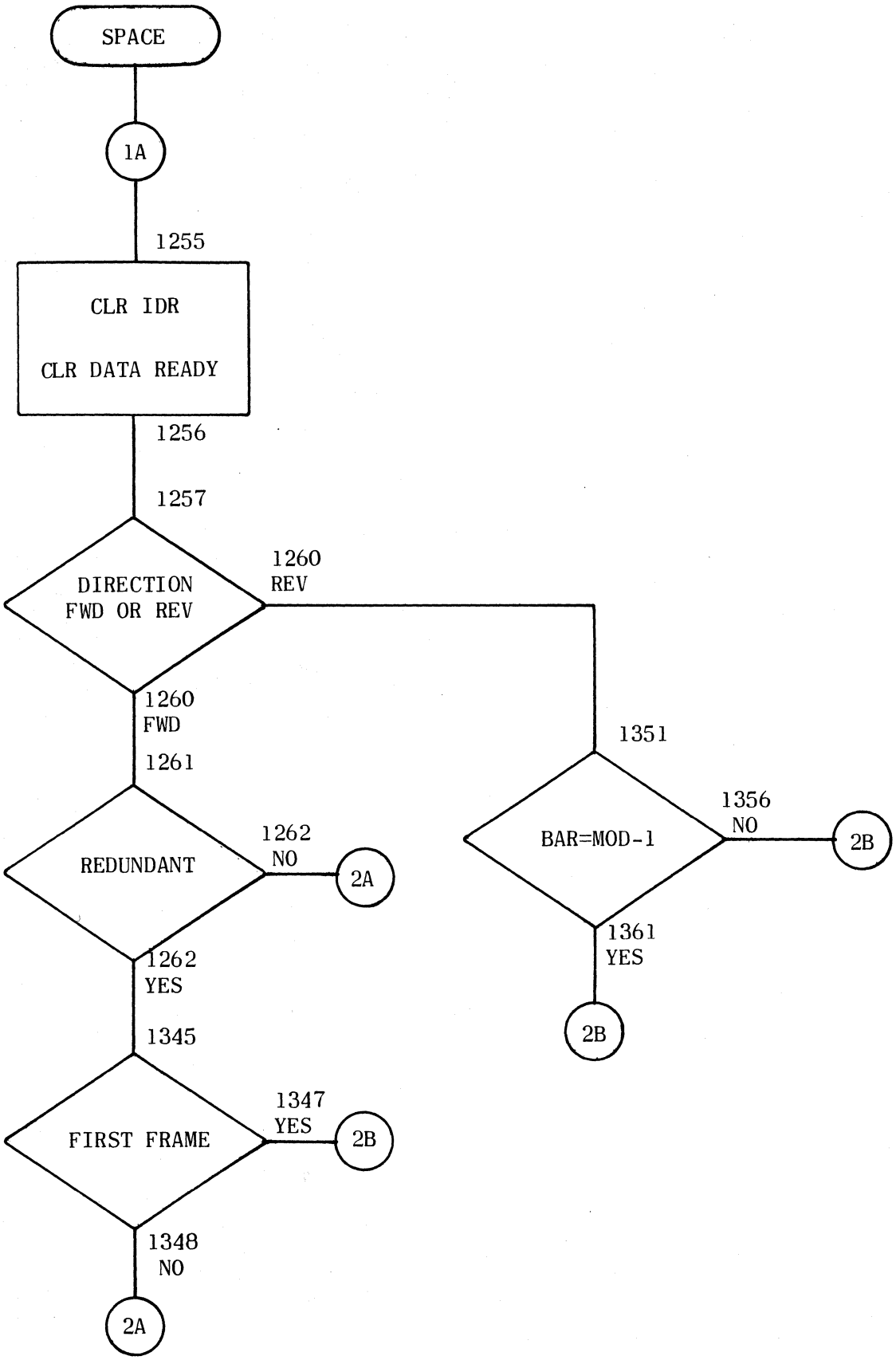


Figure 4-31. Space to IRG Sequence Flow Diagram (Sheet 1 of 5)

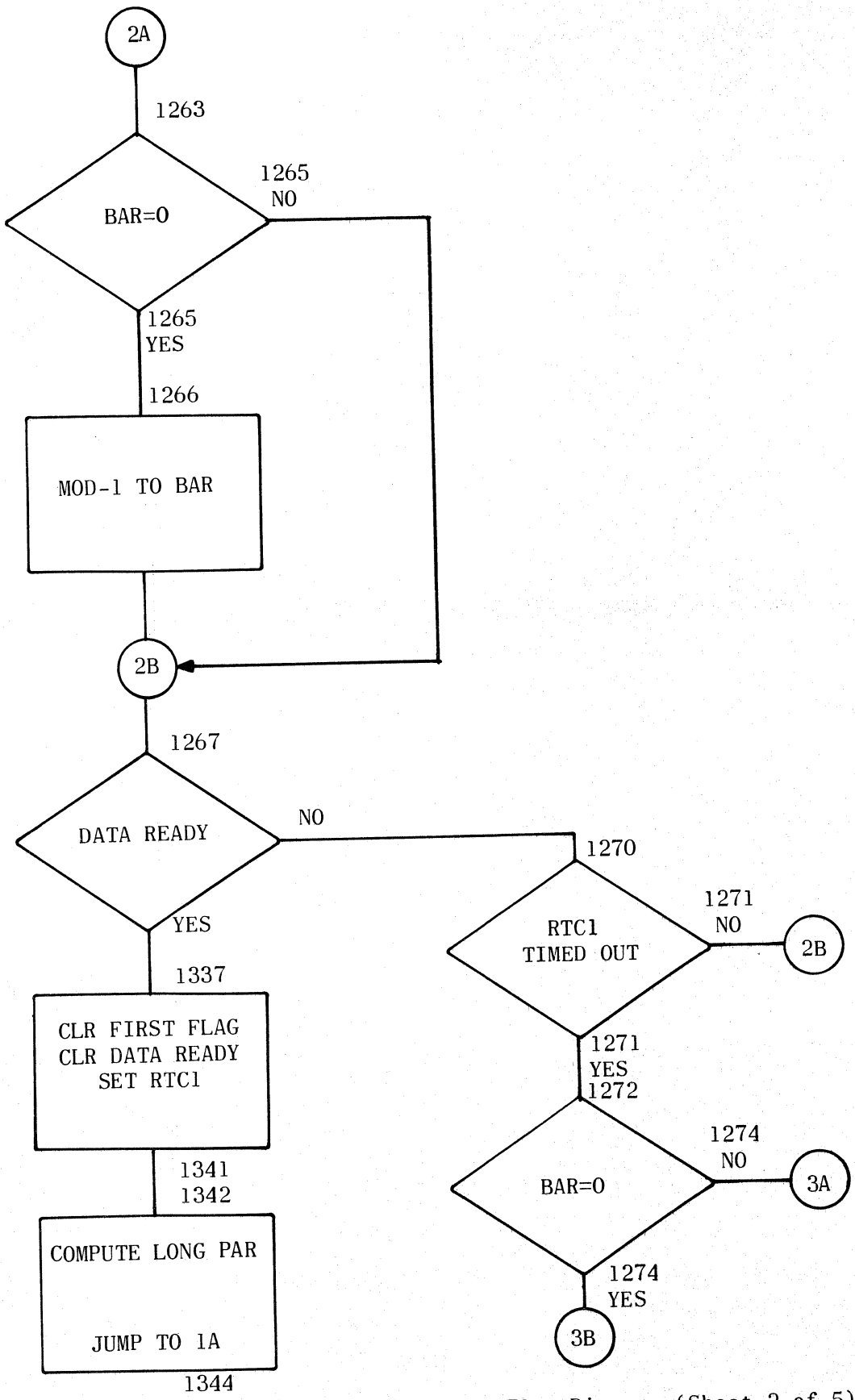


Figure 4-31. Space to IRG Sequence Flow Diagram (Sheet 2 of 5)

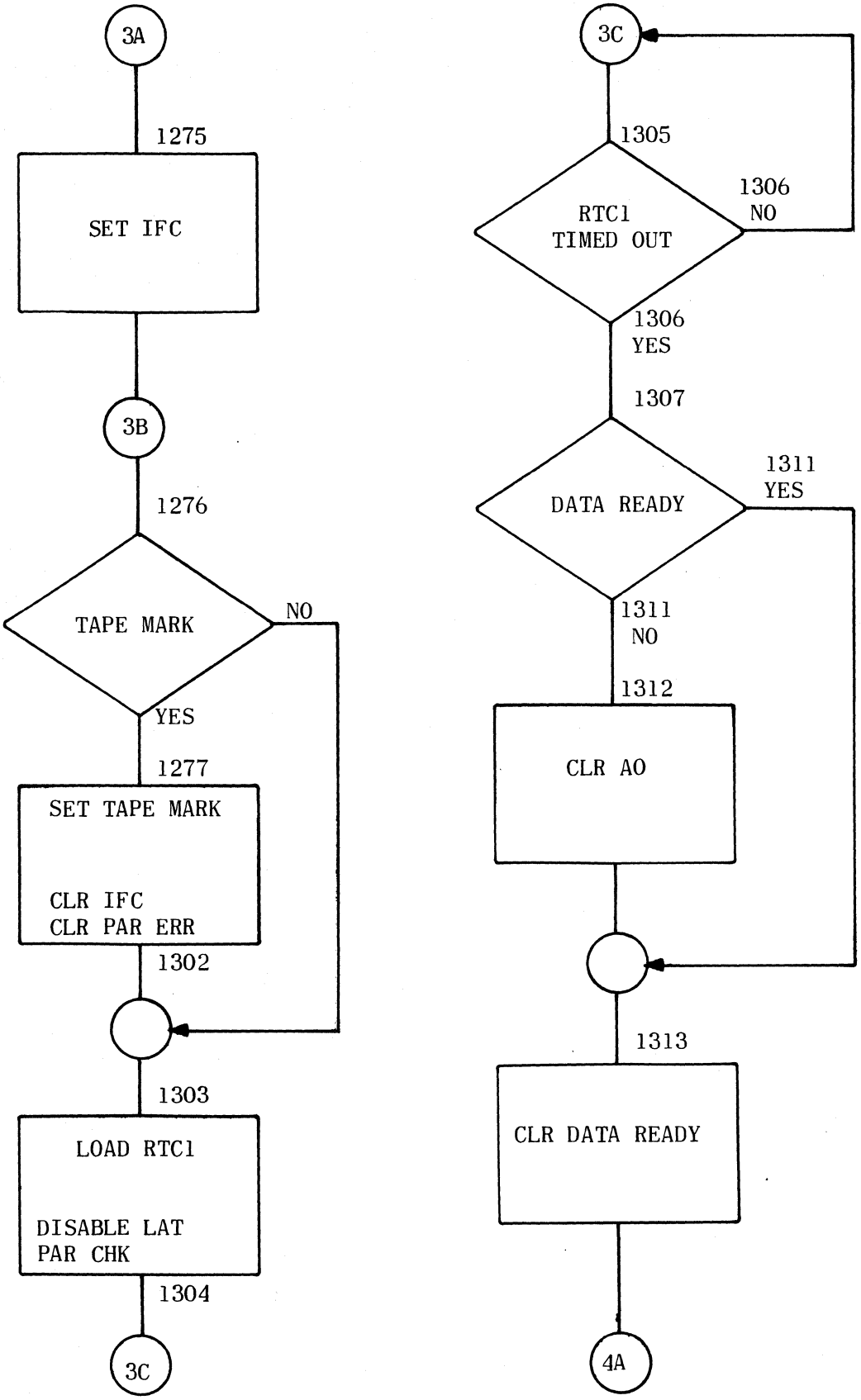


Figure 4-31. Space to IRG Sequence Flow Diagram (Sheet 3 of 5)

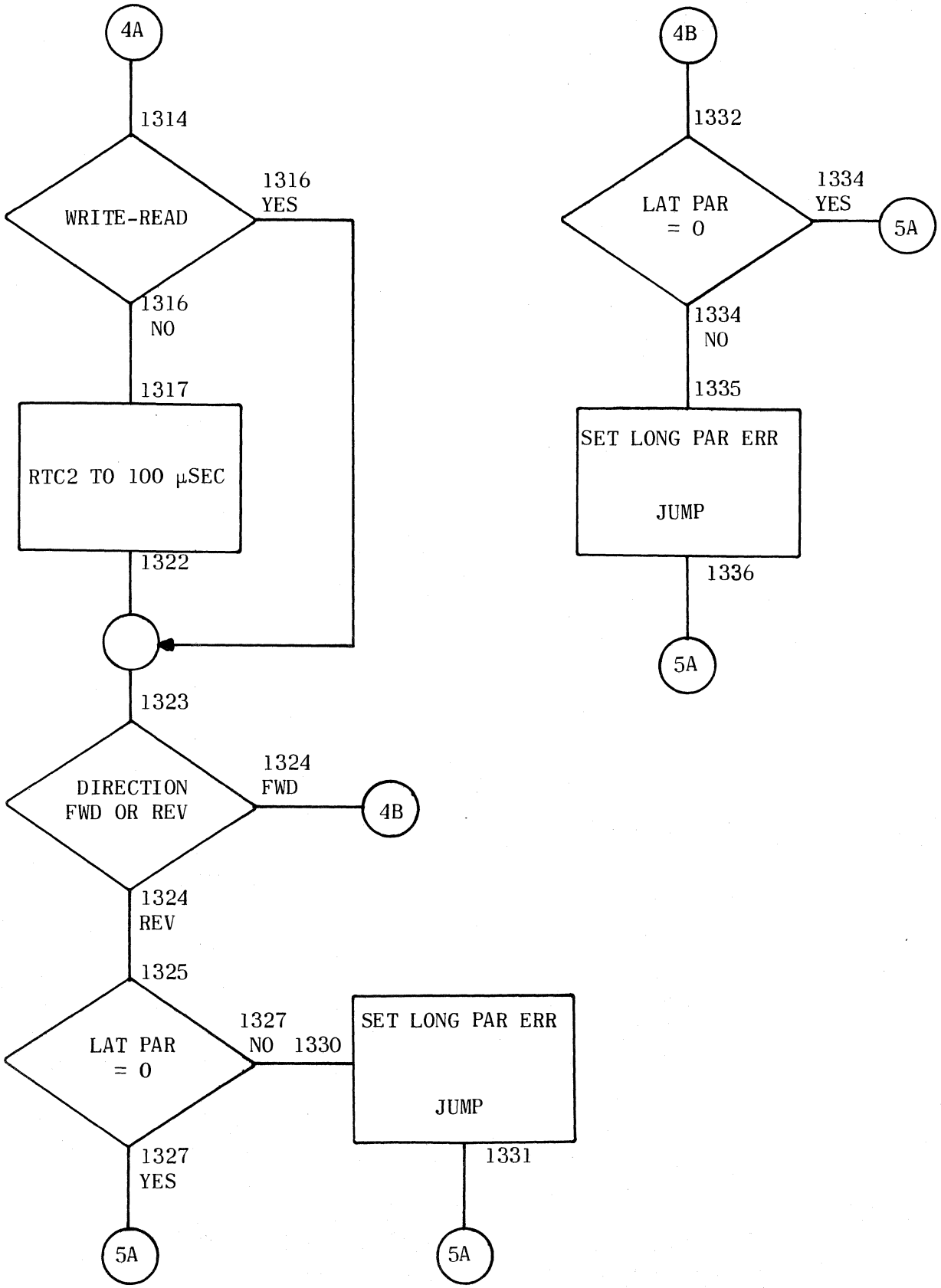


Figure 4-31. Space to IRG Sequence Flow Diagram (Sheet 4 of 5)

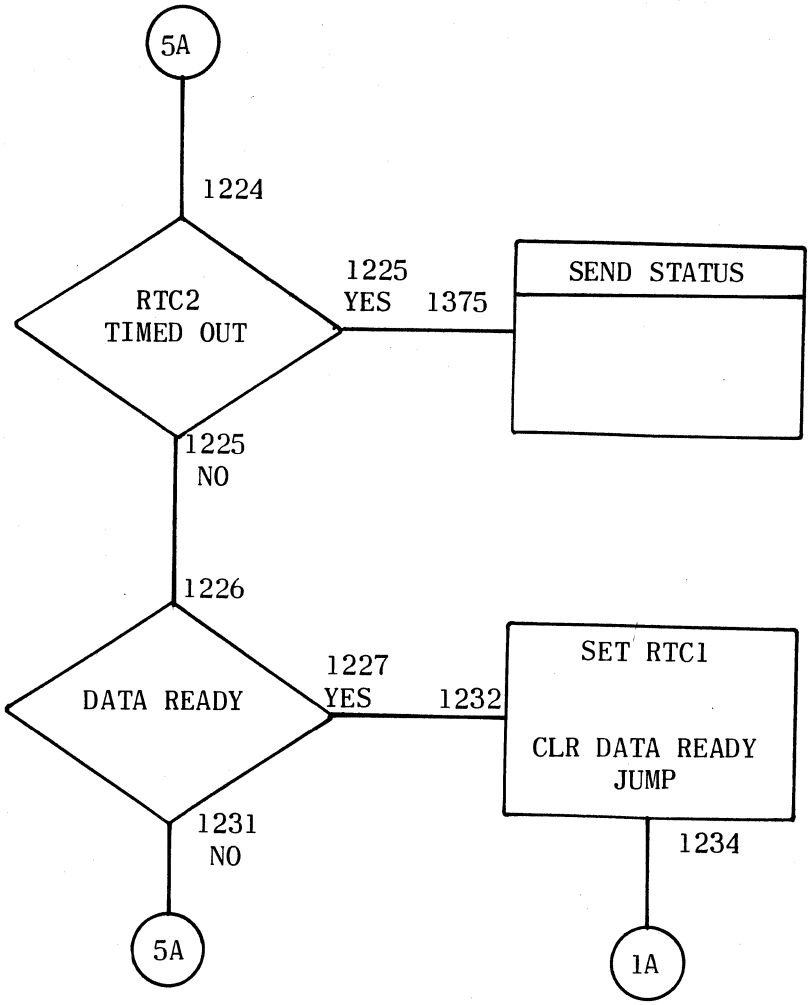


Figure 4-31. Space to IRG Sequence Flow Diagram (Sheet 5 of 5)

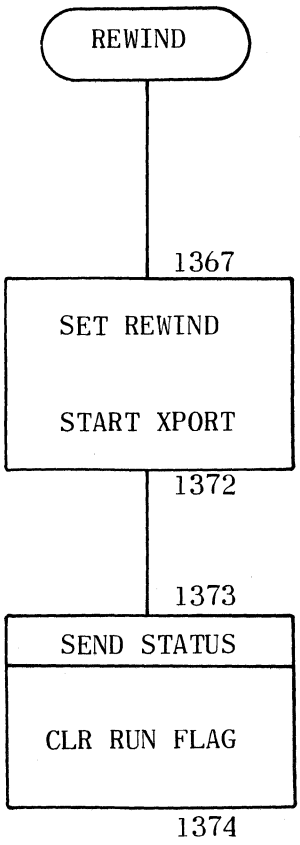


Figure 4-32. Rewind Sequence Flow Diagram

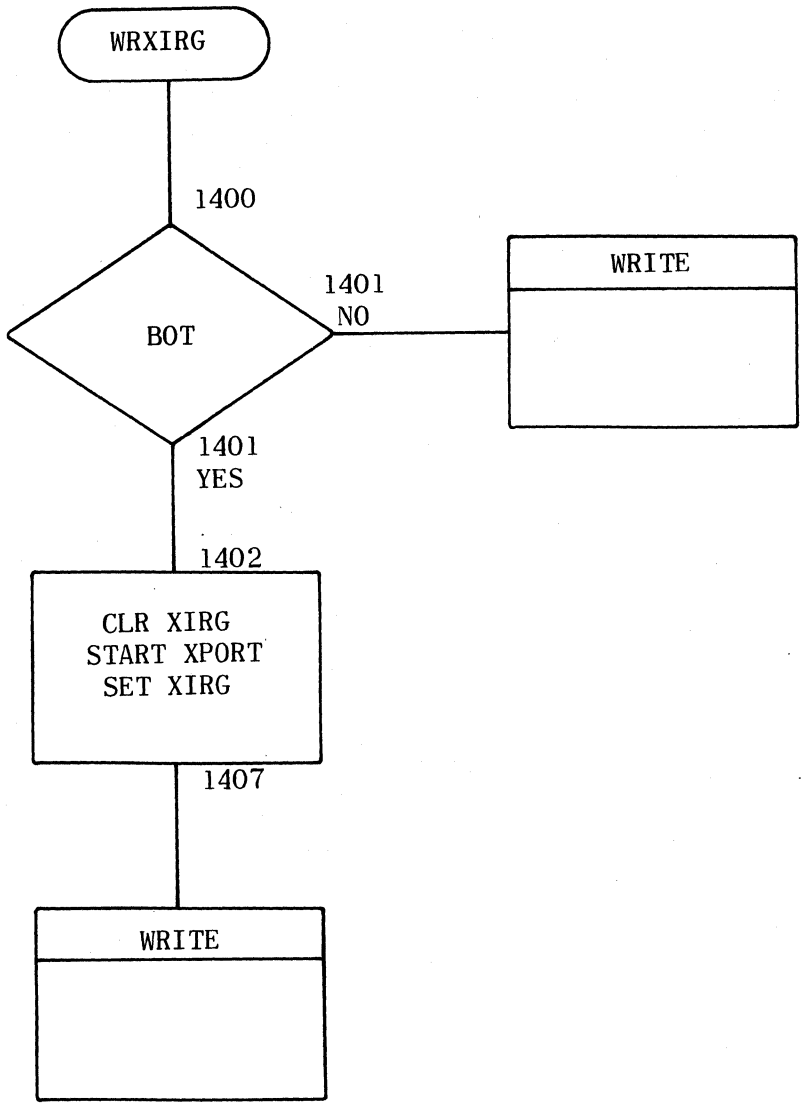


Figure 4-33. Write XIRG Sequence Flow Diagram

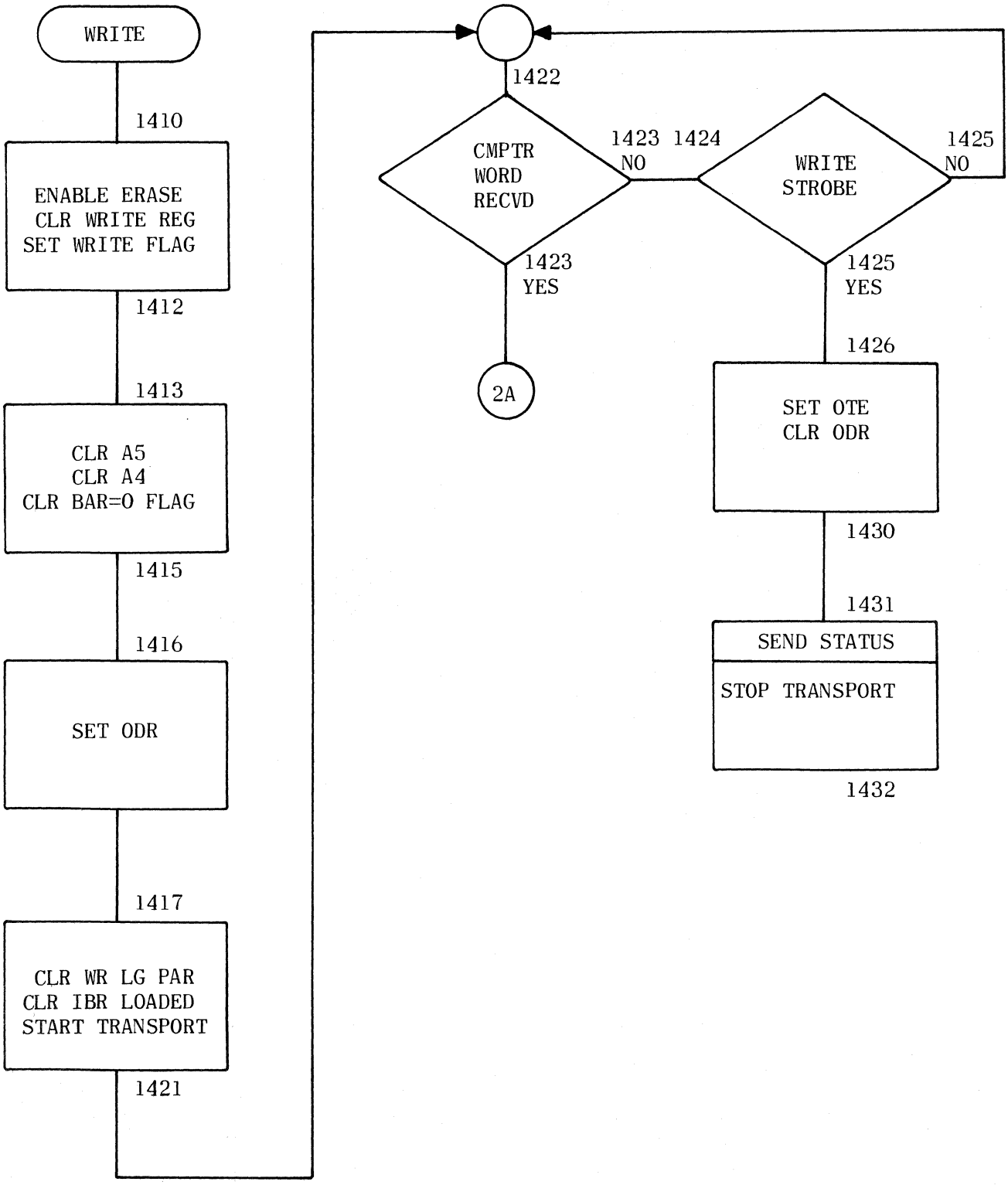


Figure 4-34. Write Sequence Flow Diagram (Sheet 1 of 8)

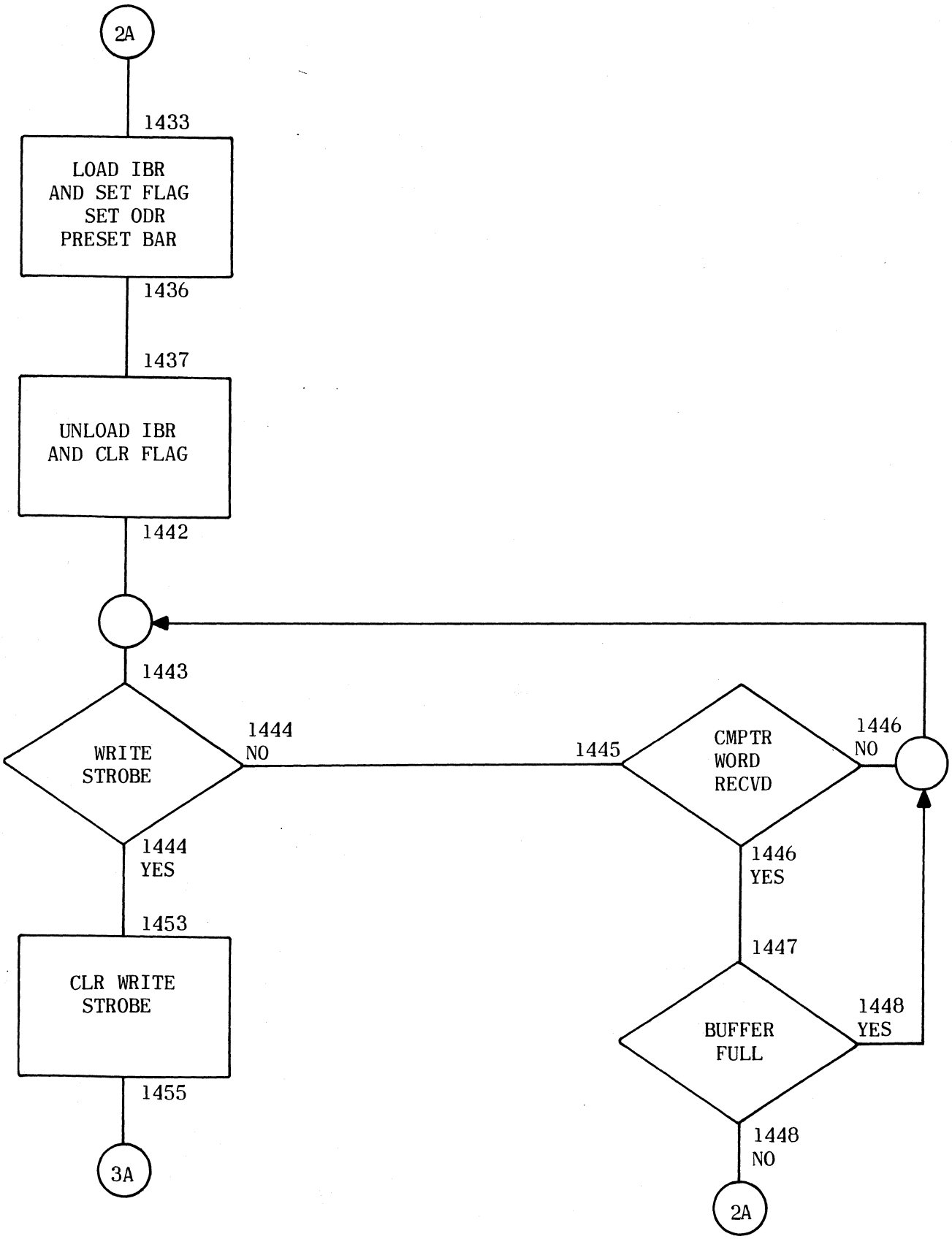


Figure 4-34. Write Sequence Flow Diagram (Sheet 2 of 8)

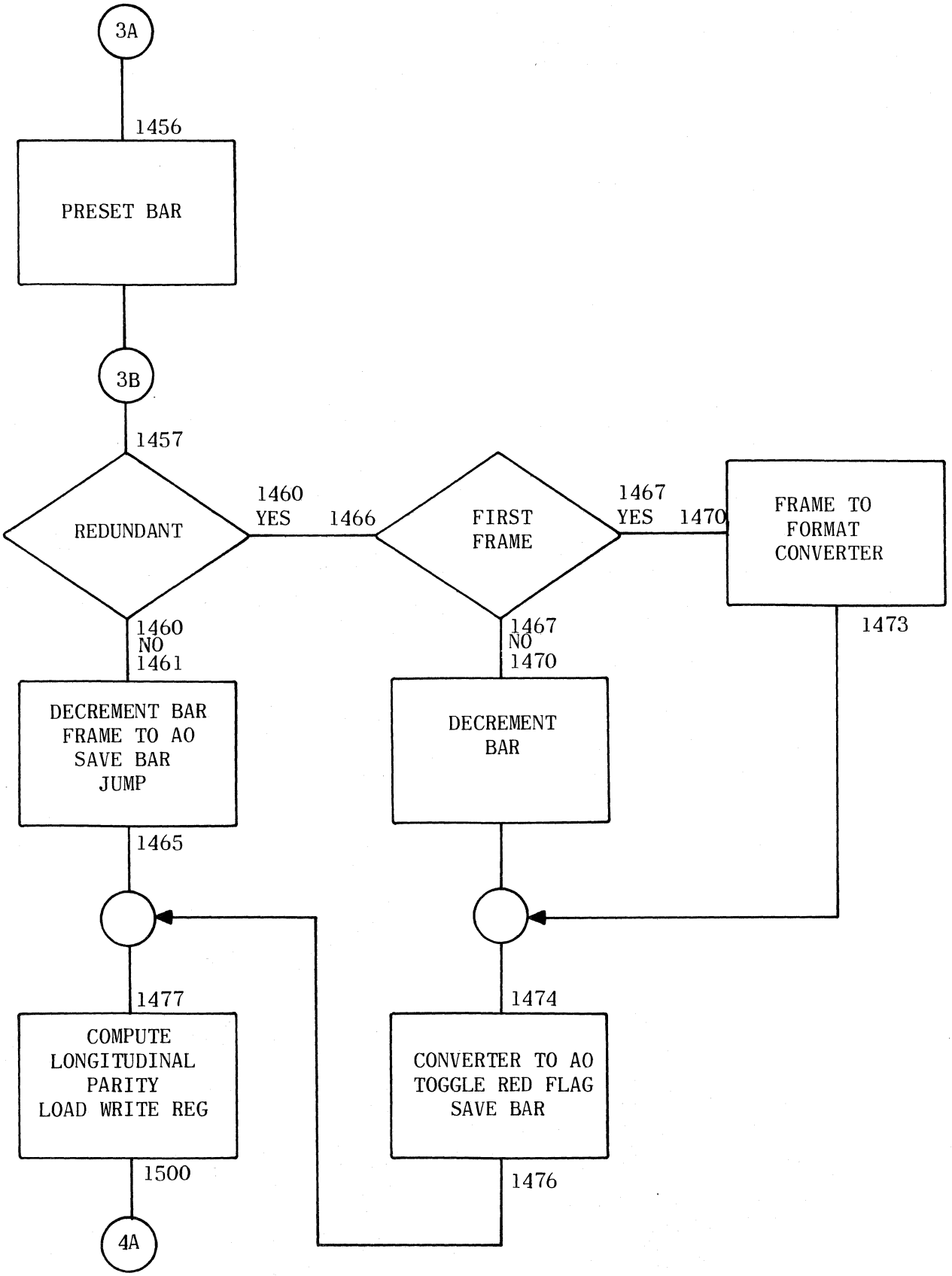


Figure 4-34. Write Sequence Flow Diagram (Sheet 3 of 8)

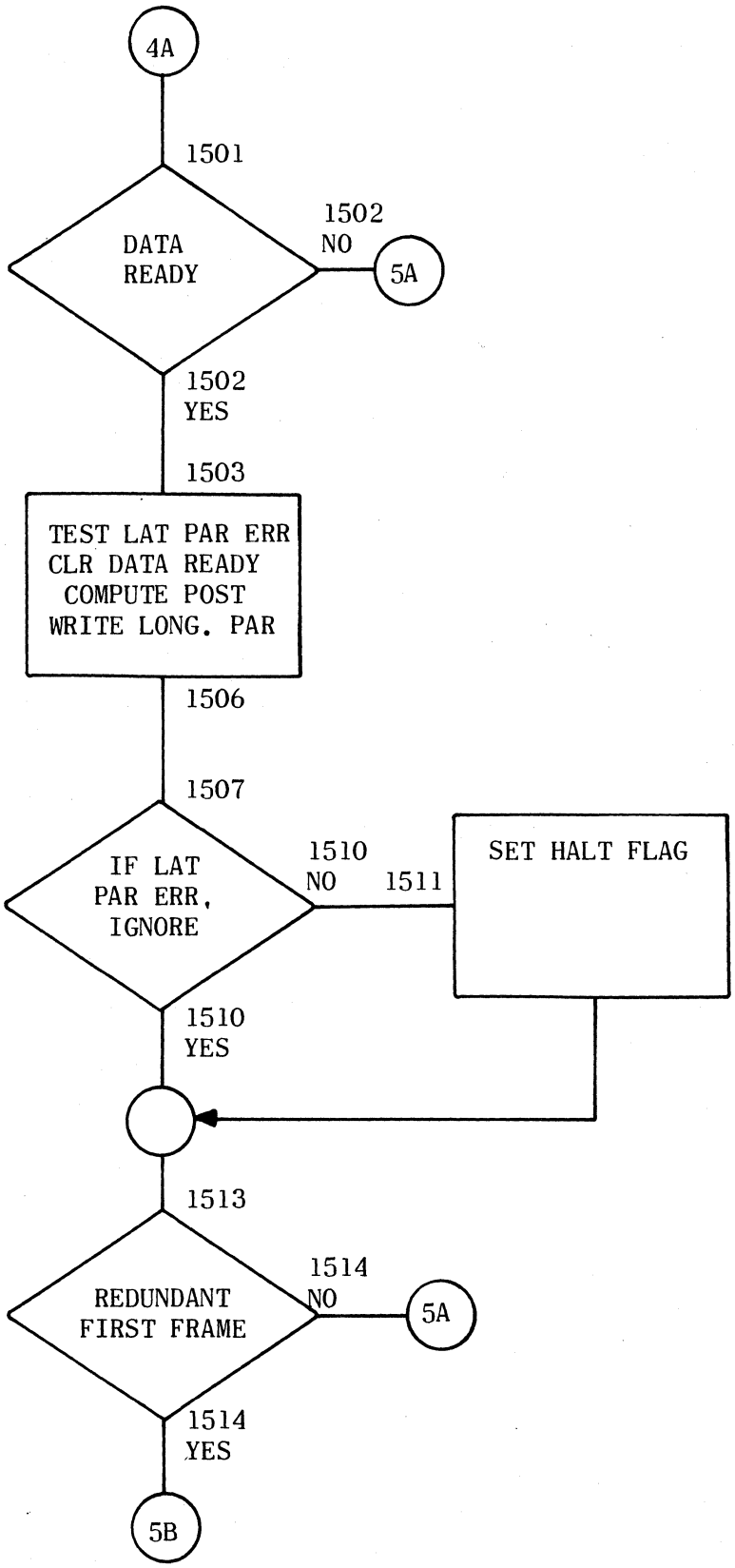


Figure 4-34. Write Sequence Flow Diagram (Sheet 4 of 8)

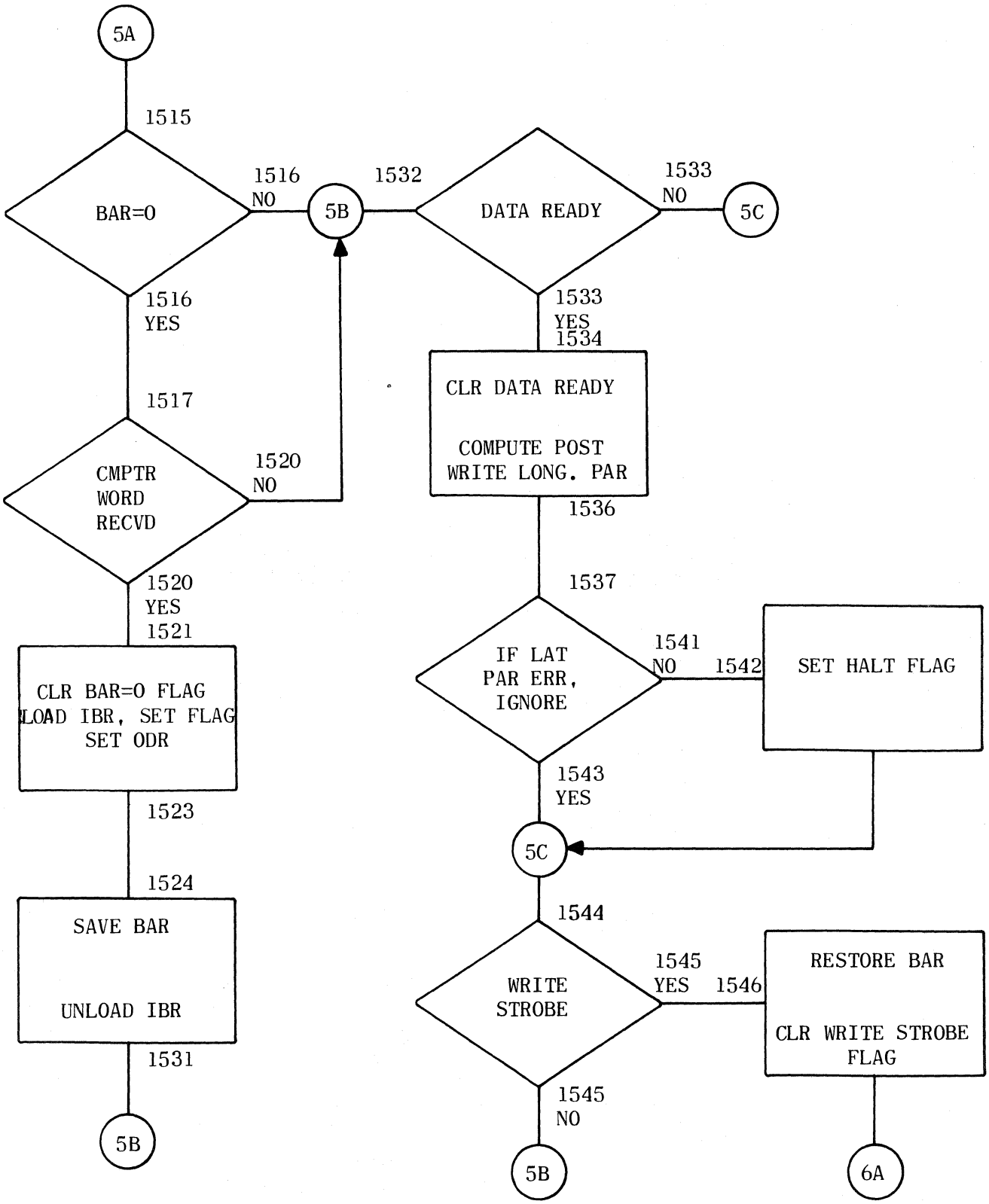


Figure 4-34. Write Sequence Flow Diagram (Sheet 5 of 8)

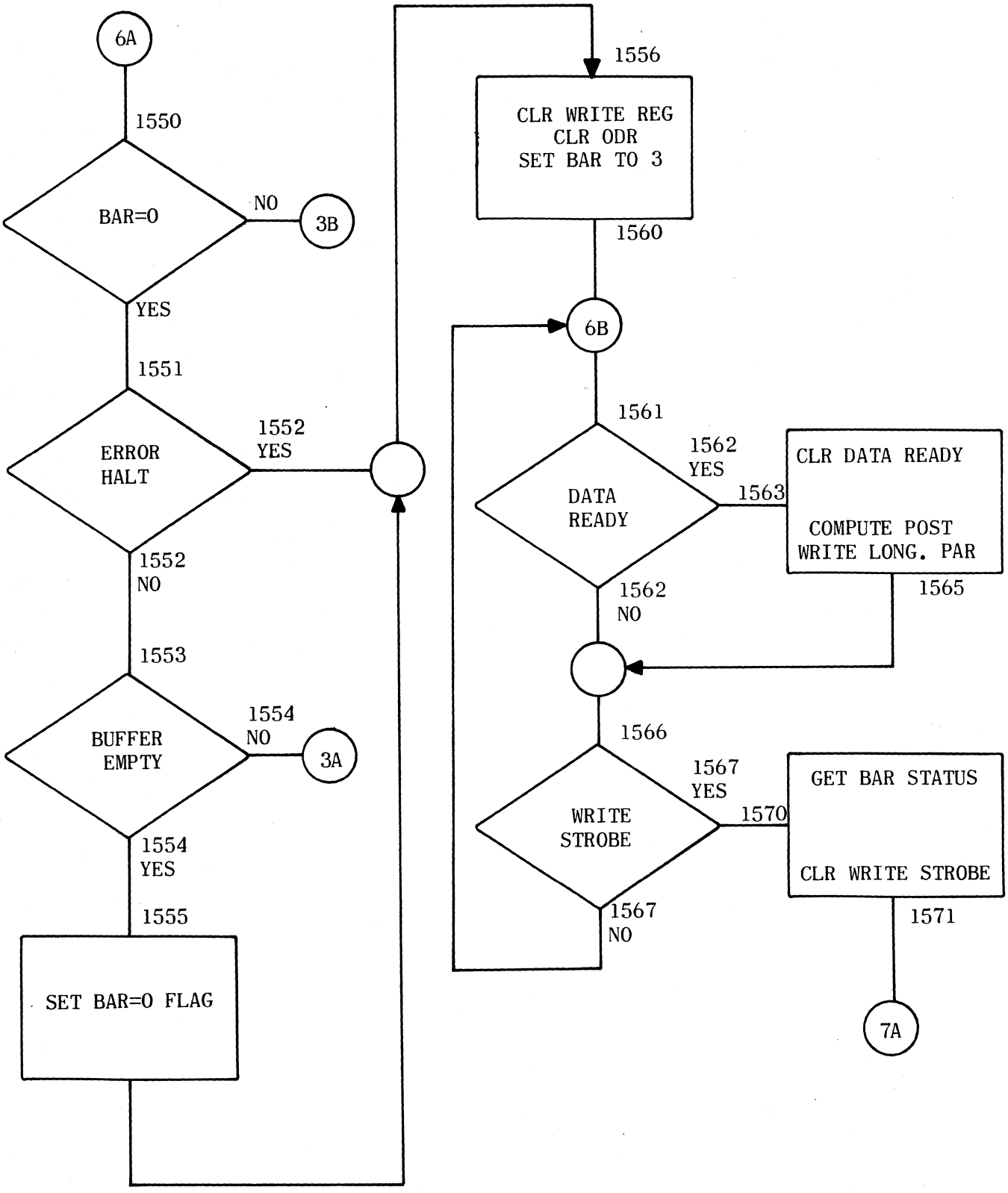


Figure 4-34. Write Sequence Flow Diagram (Sheet 6 of 8)

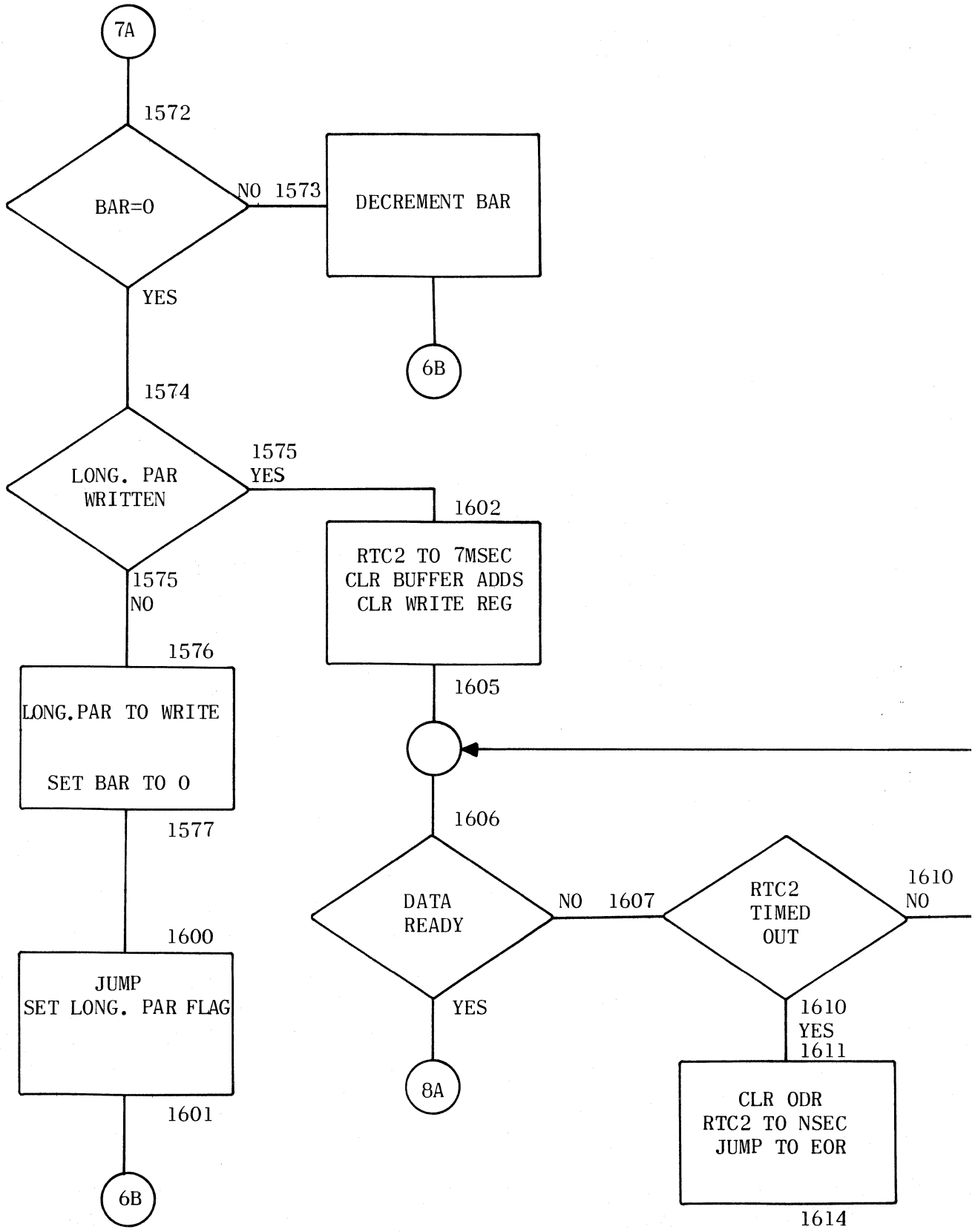


Figure 4-34. Write Sequence Flow Diagram (Sheet 7 of 8)

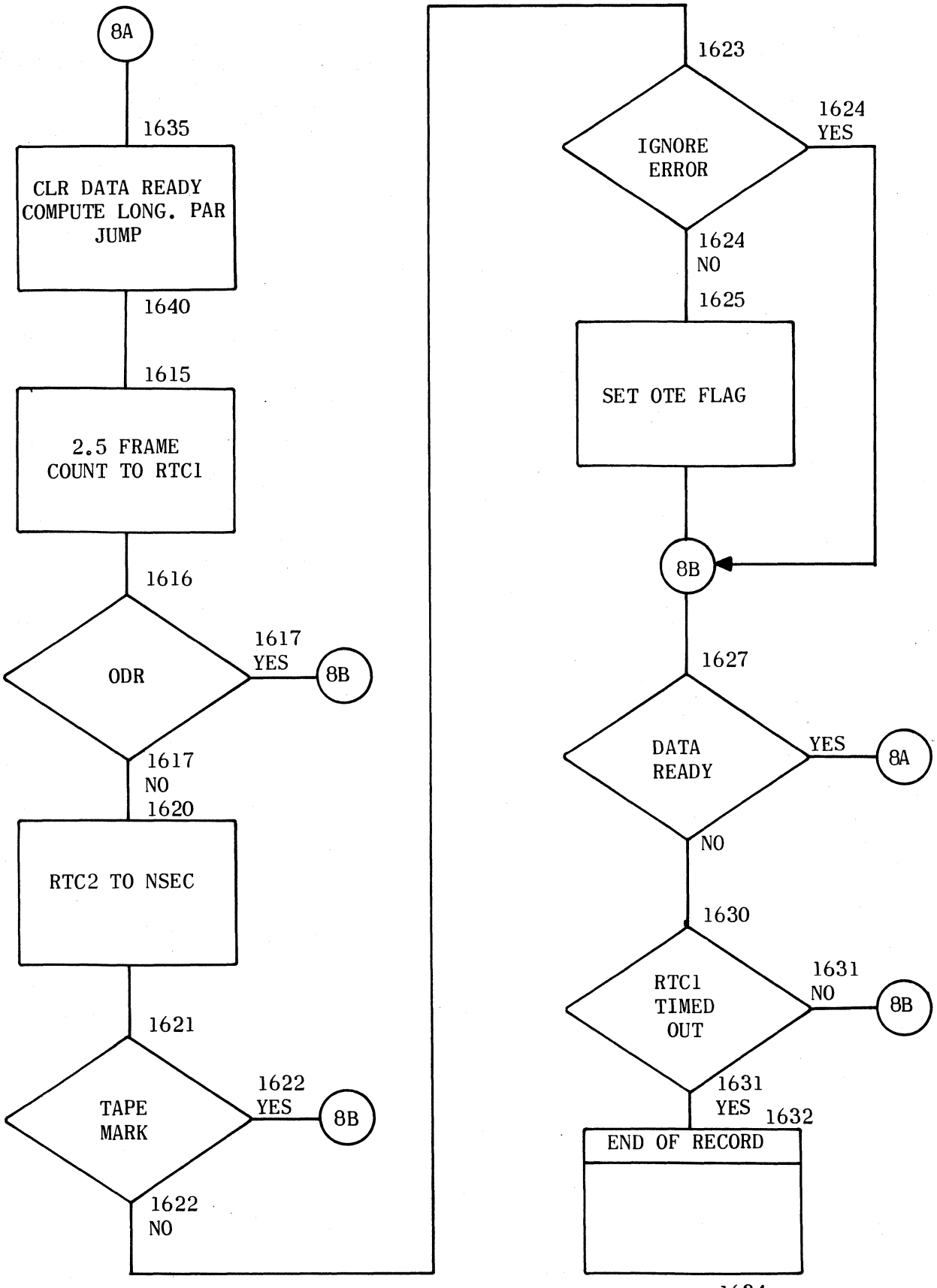


Figure 4-34. Write Sequence Flow Diagram (Sheet 8 of 8)

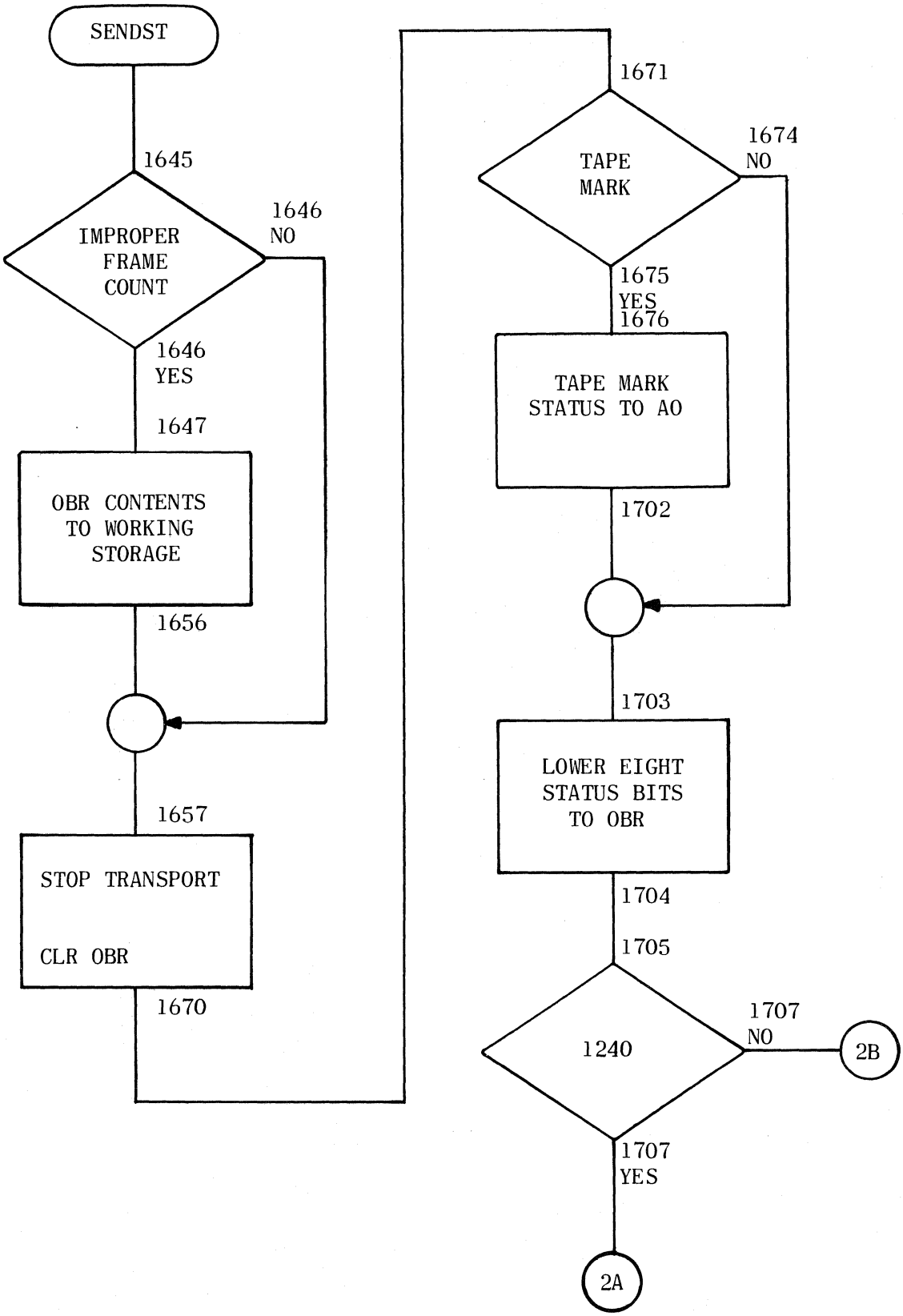


Figure 4-35. Send Status Sequence Flow Diagram (Sheet 1 of 2)

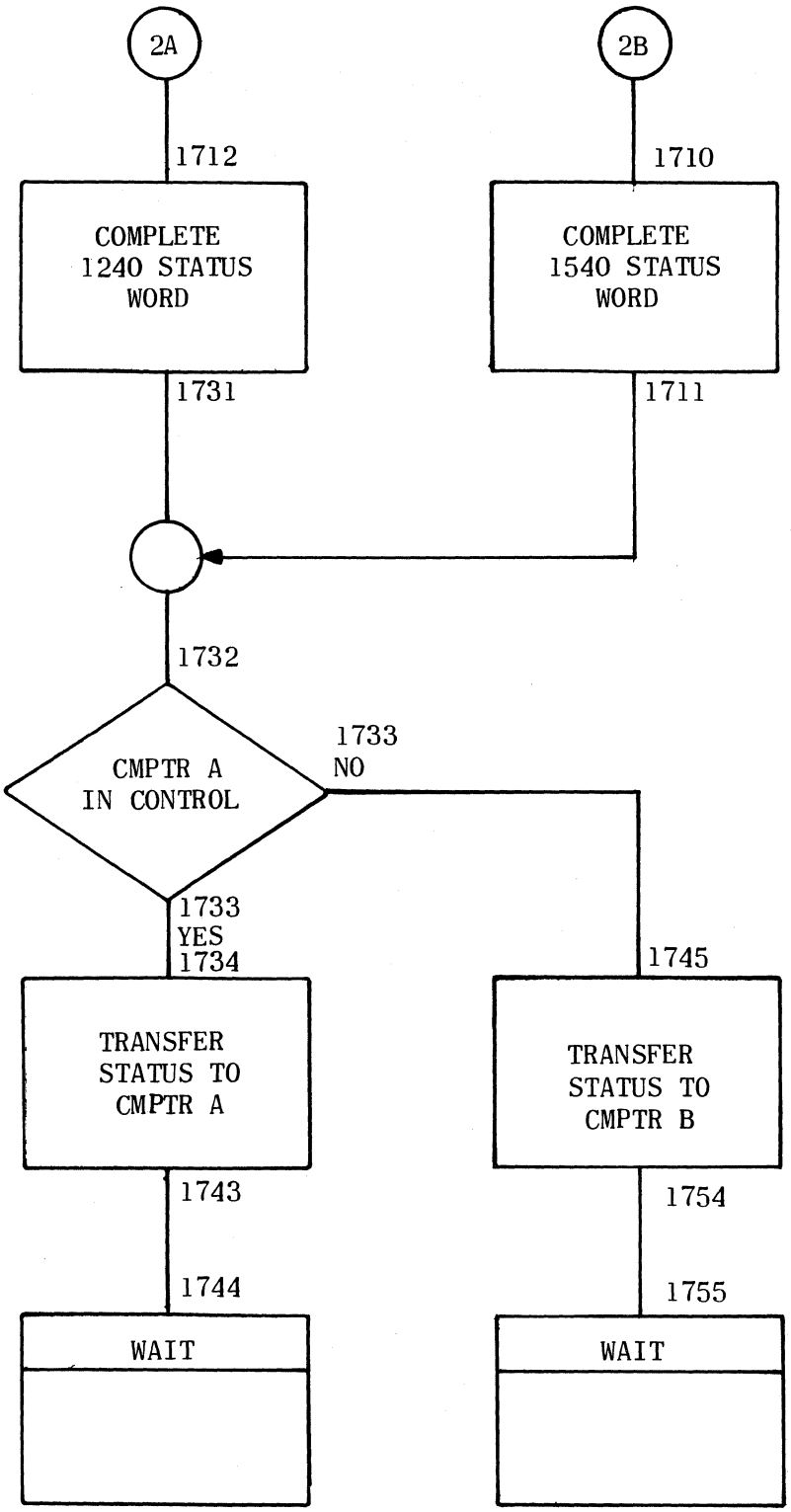


Figure 4-35. Send Status Sequence Flow Diagram (Sheet 2 of 2)

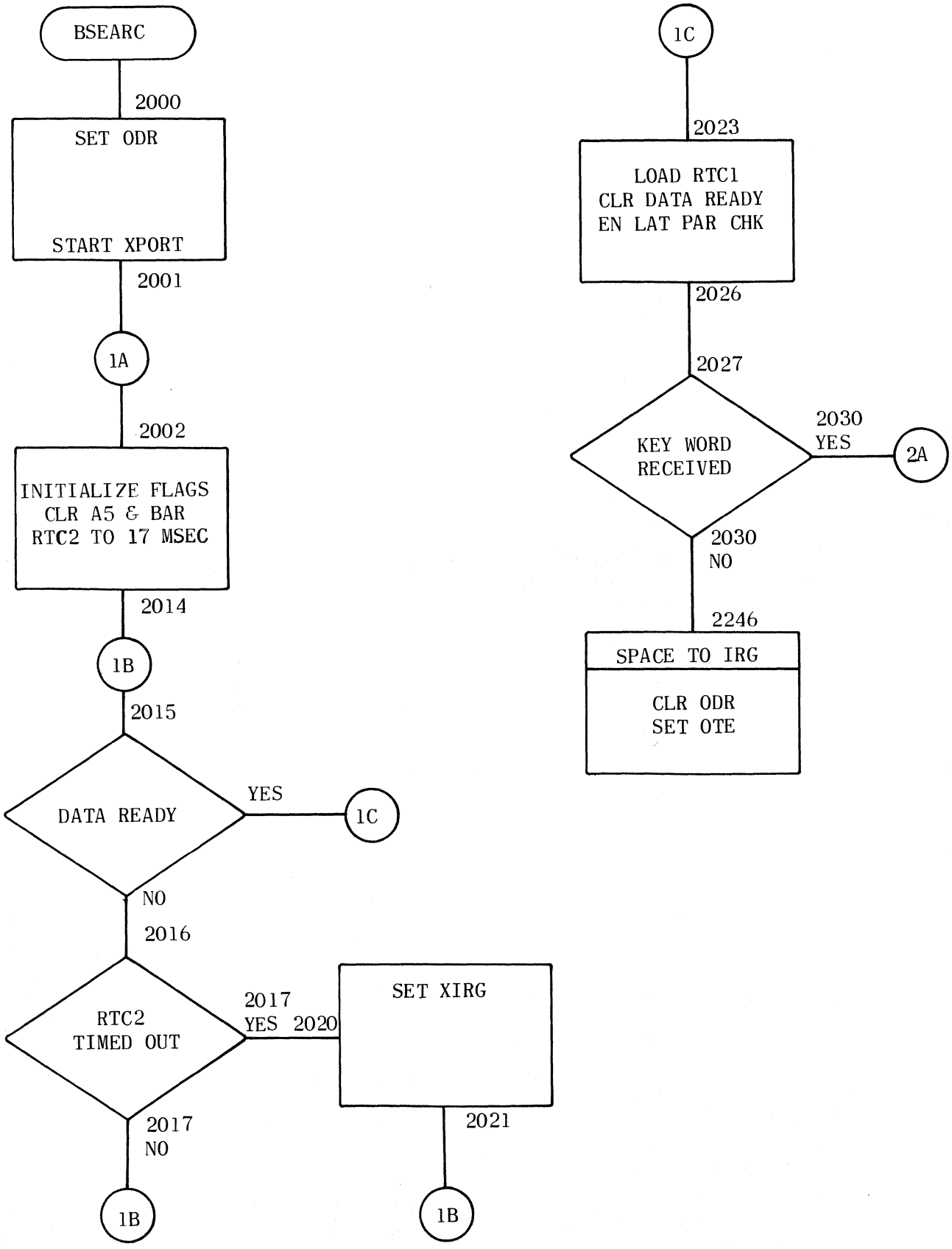


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 1 of 14)

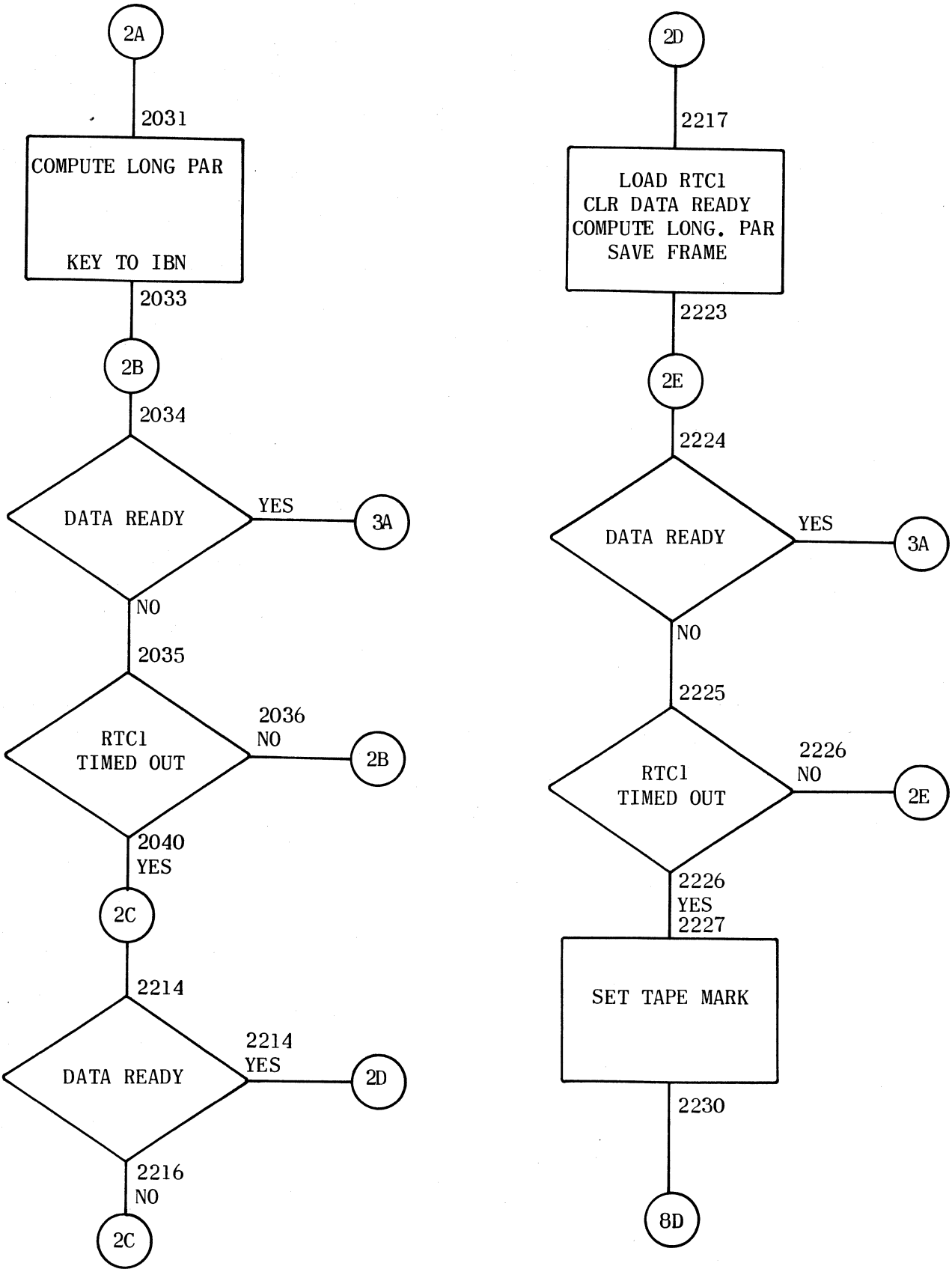


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 2 of 14)

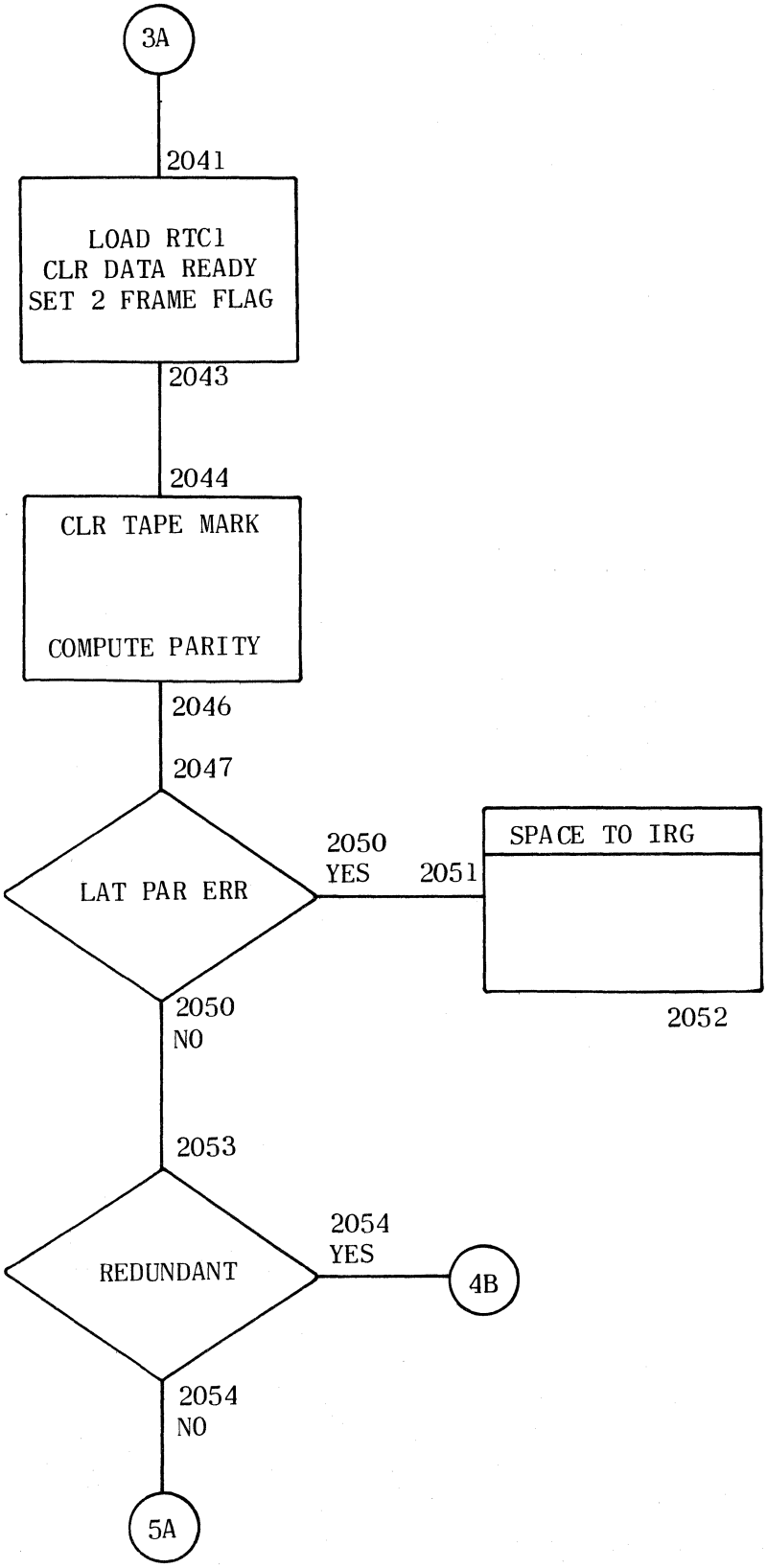


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 3 of 14)

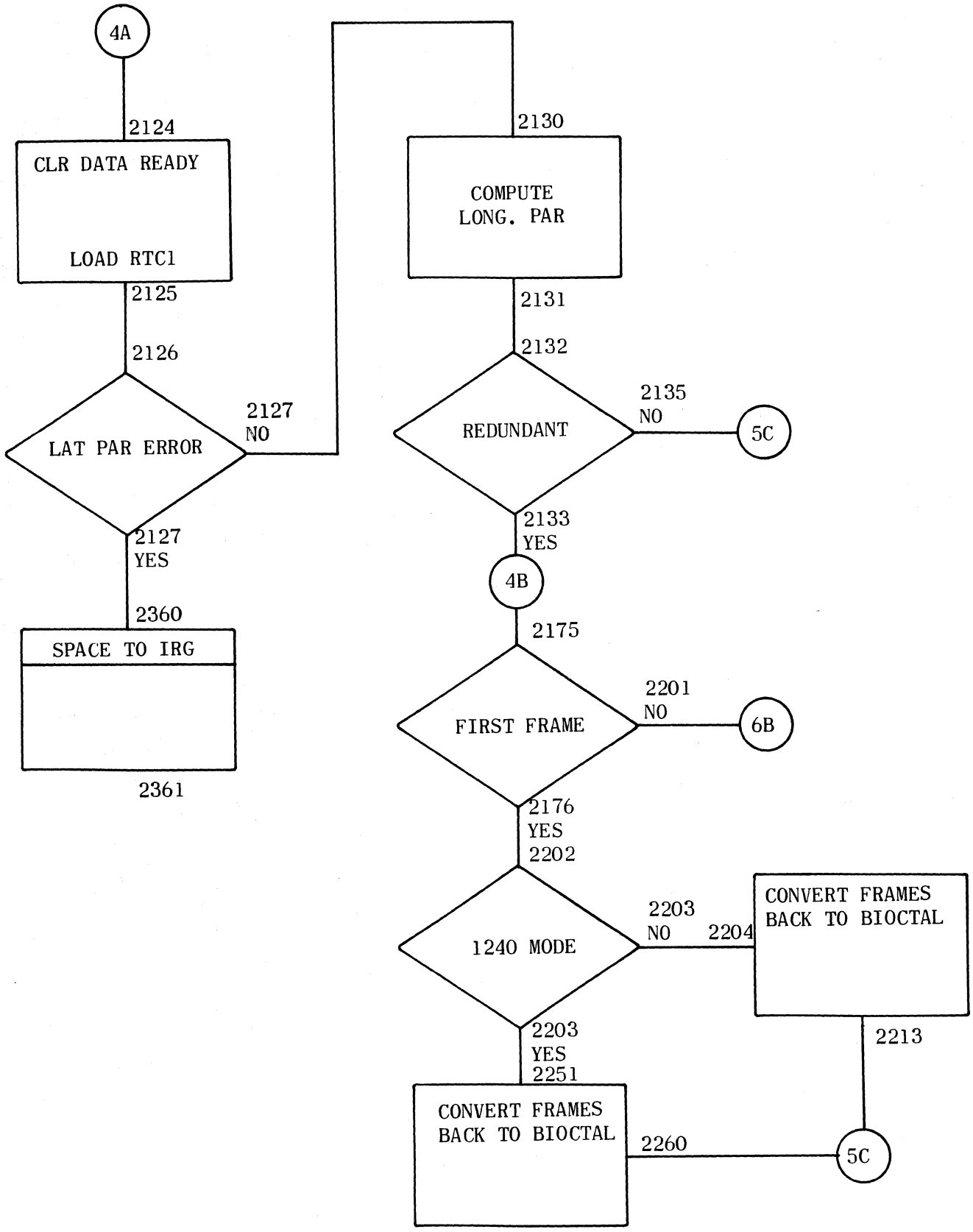


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 4 of 14)

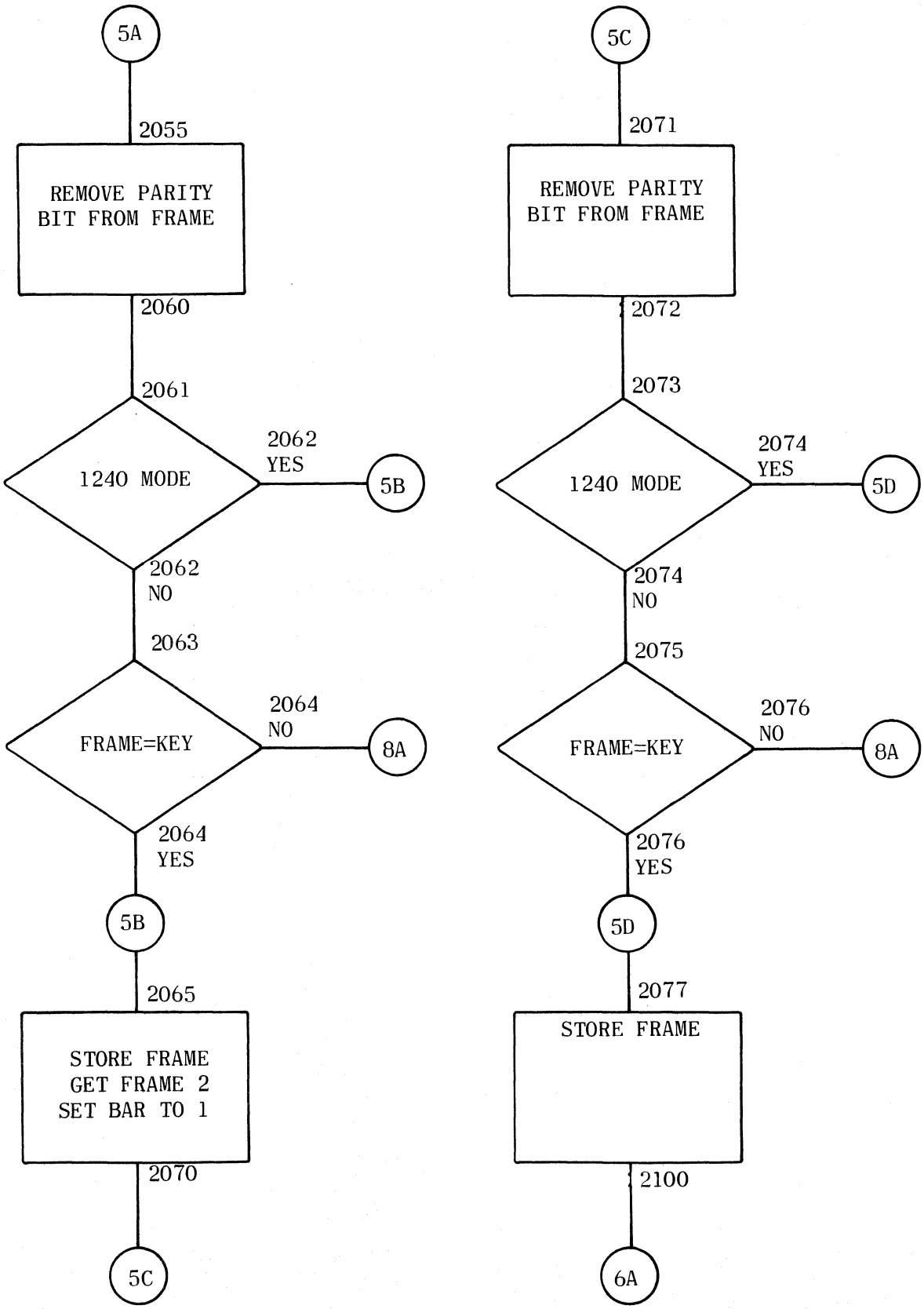


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 5 of 14)

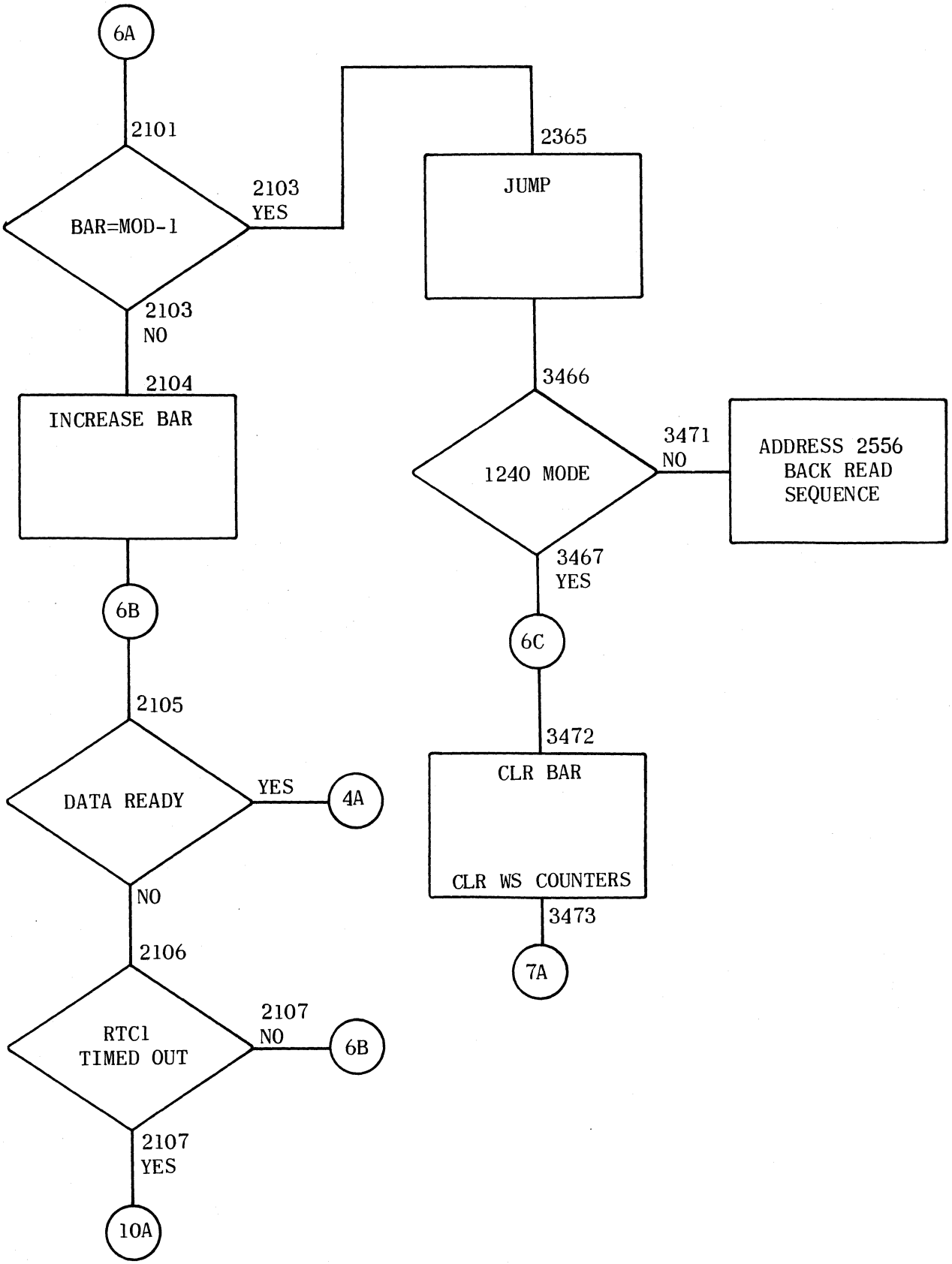


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 6 of 14)

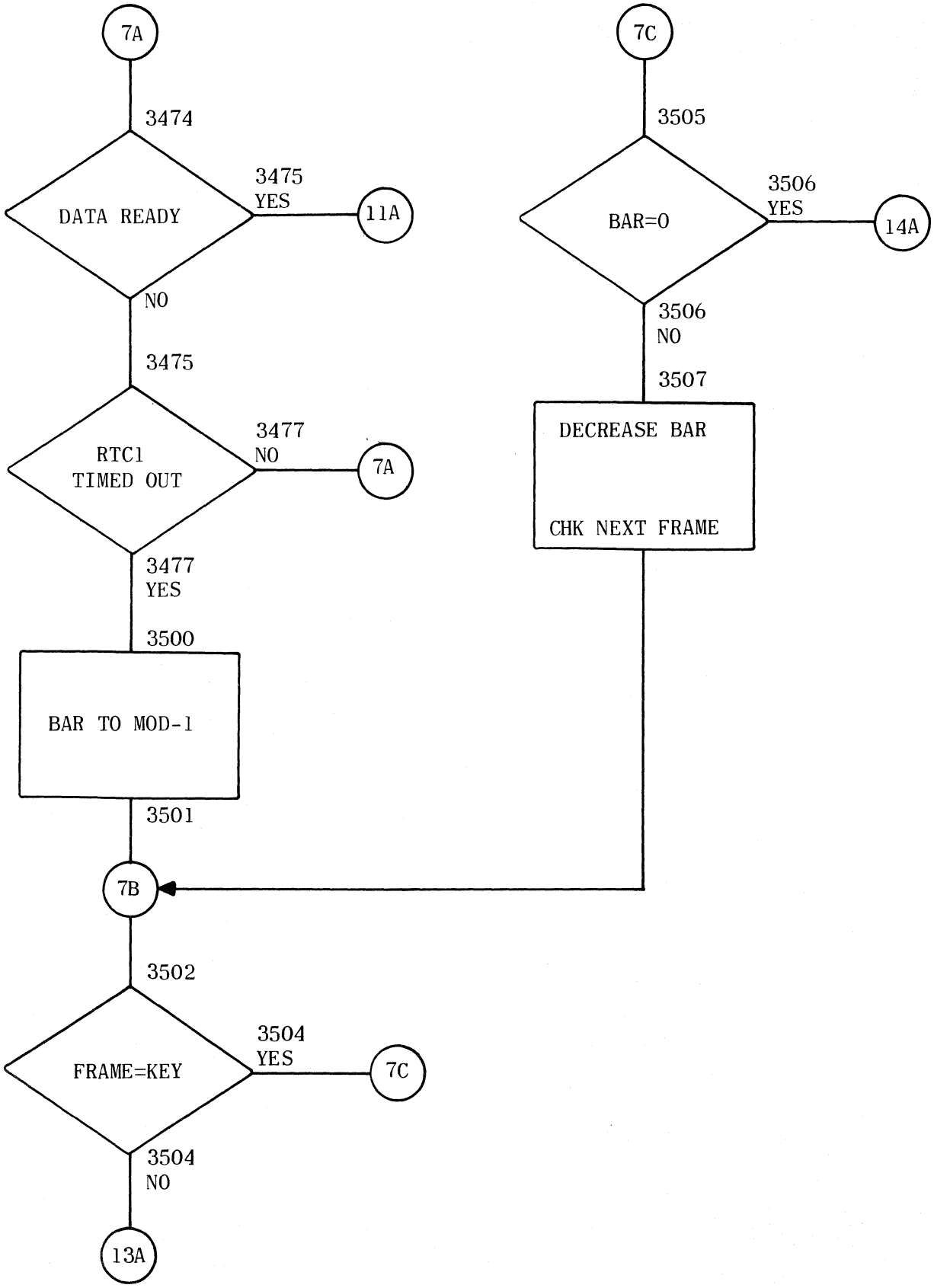


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 7 of 14)

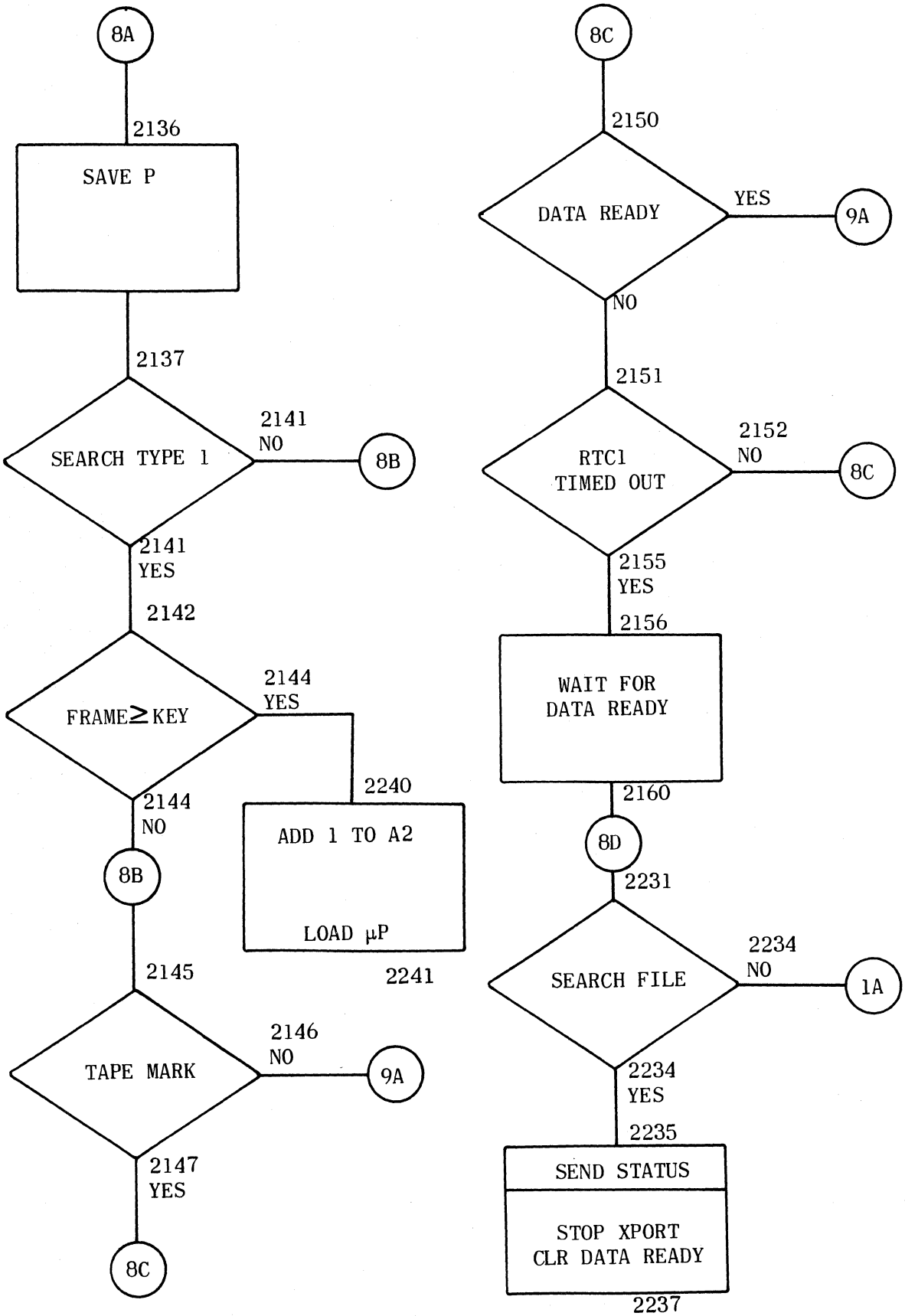


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 8 of 14)

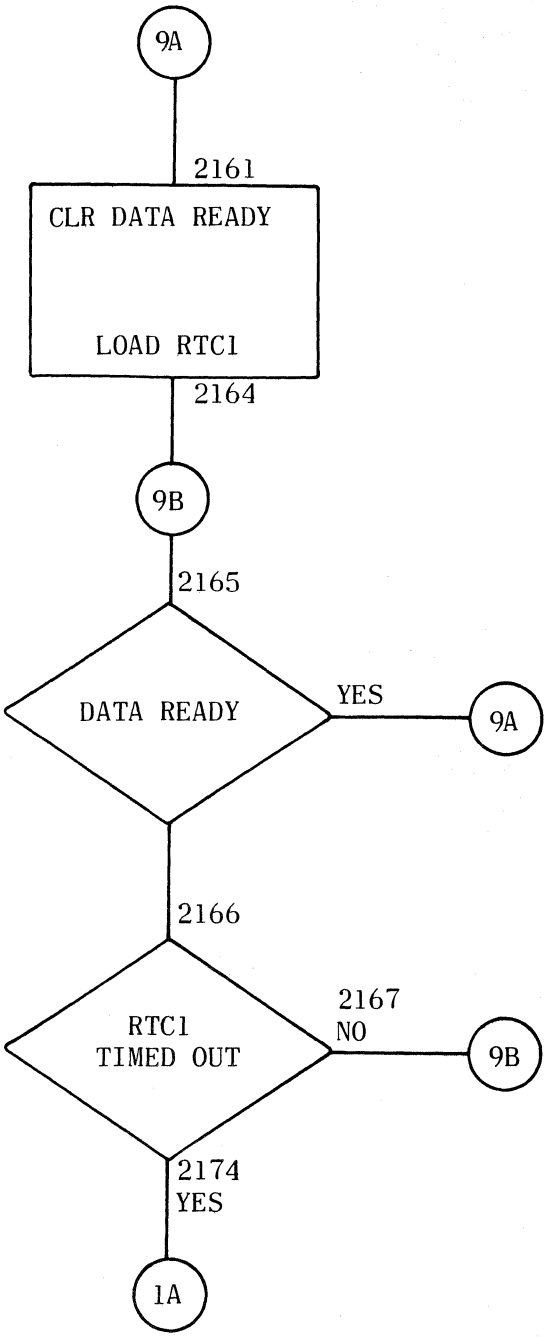


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 9 of 14)

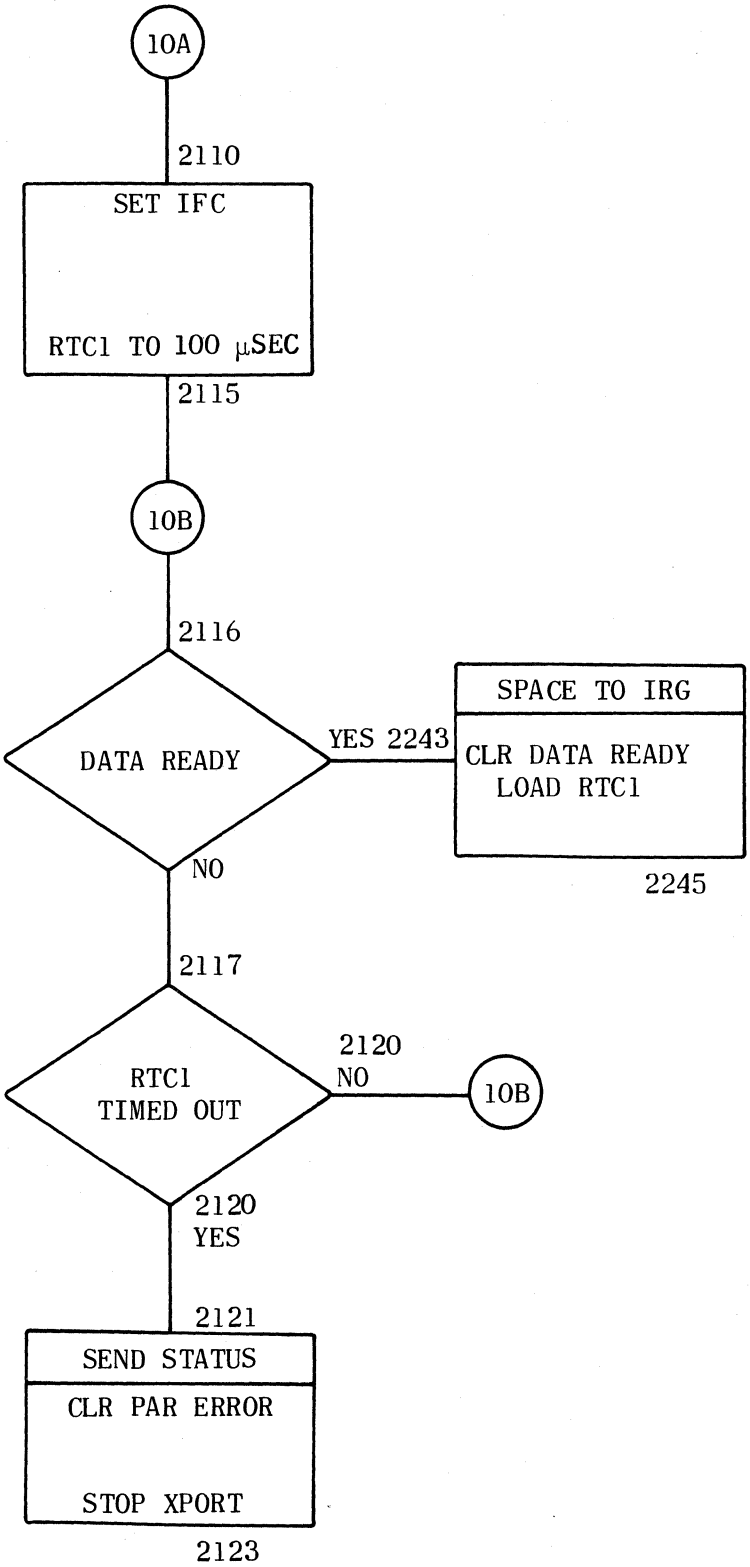


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 10 of 14)

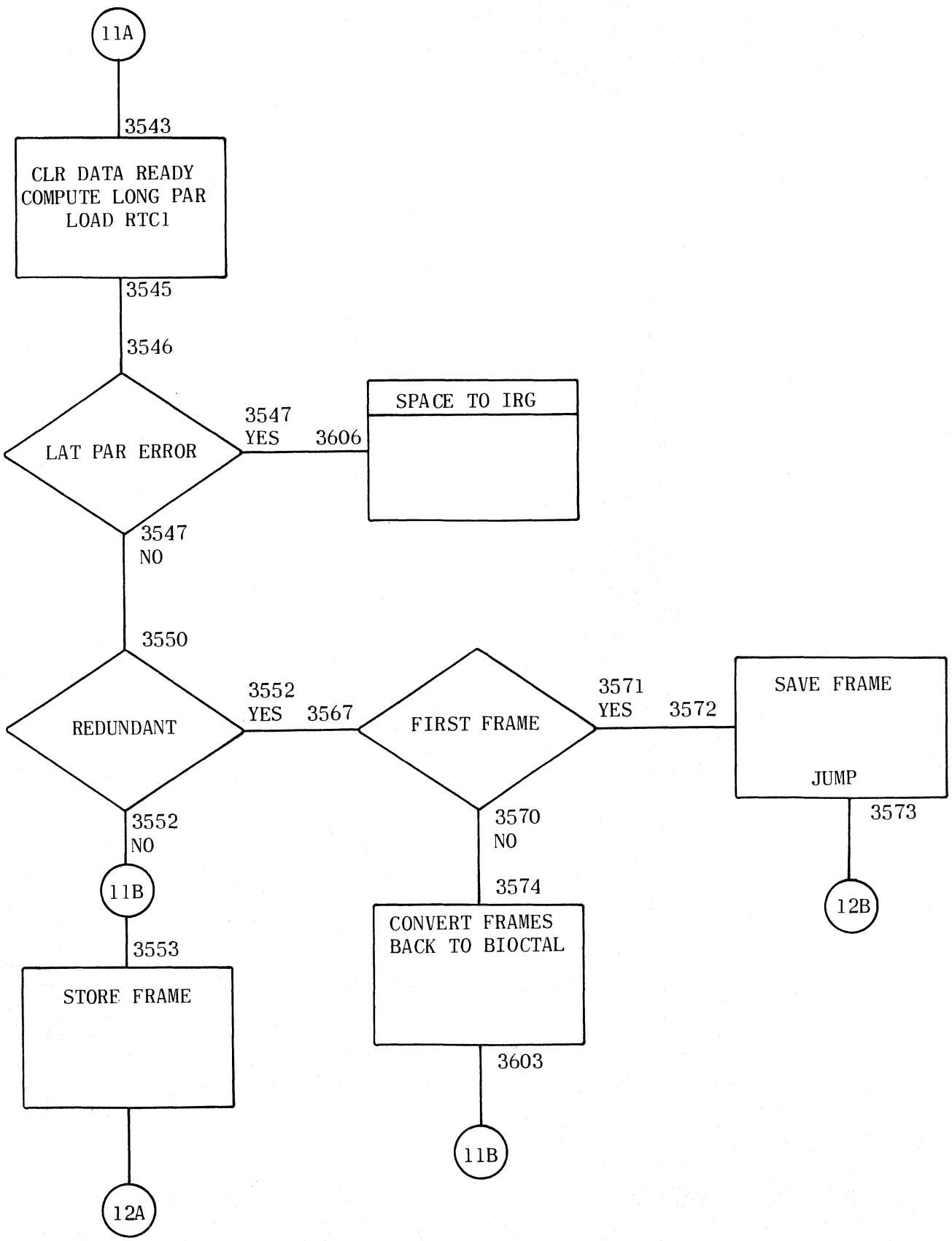


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 11 of 14)

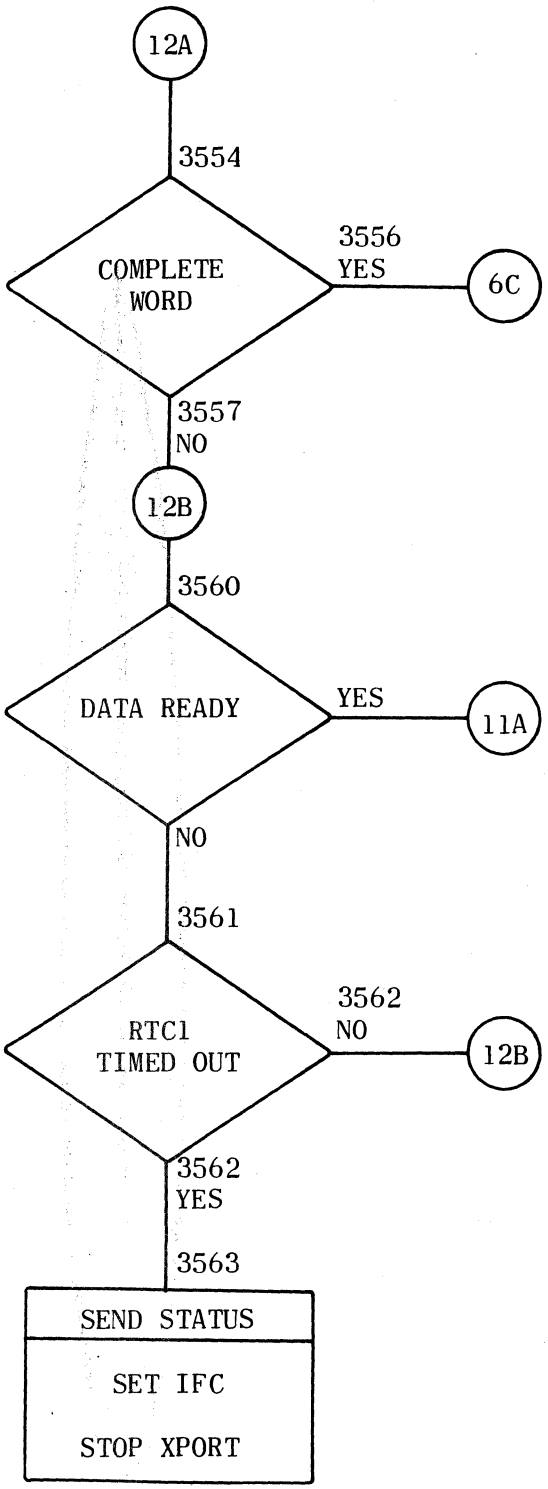


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 12 of 14)

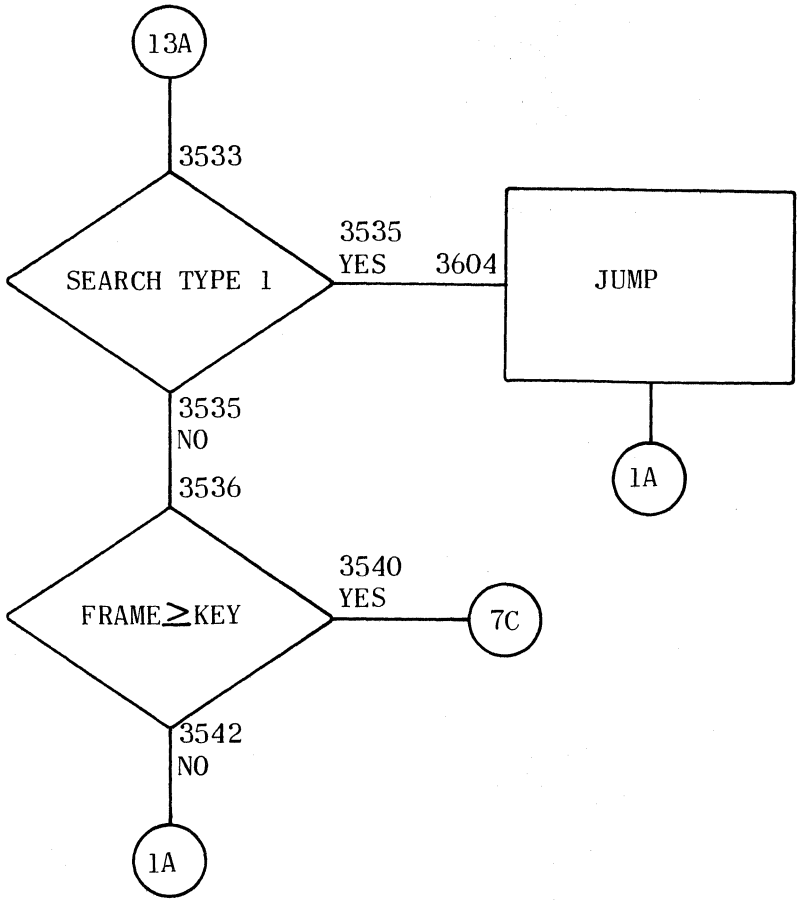


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 13 of 14)

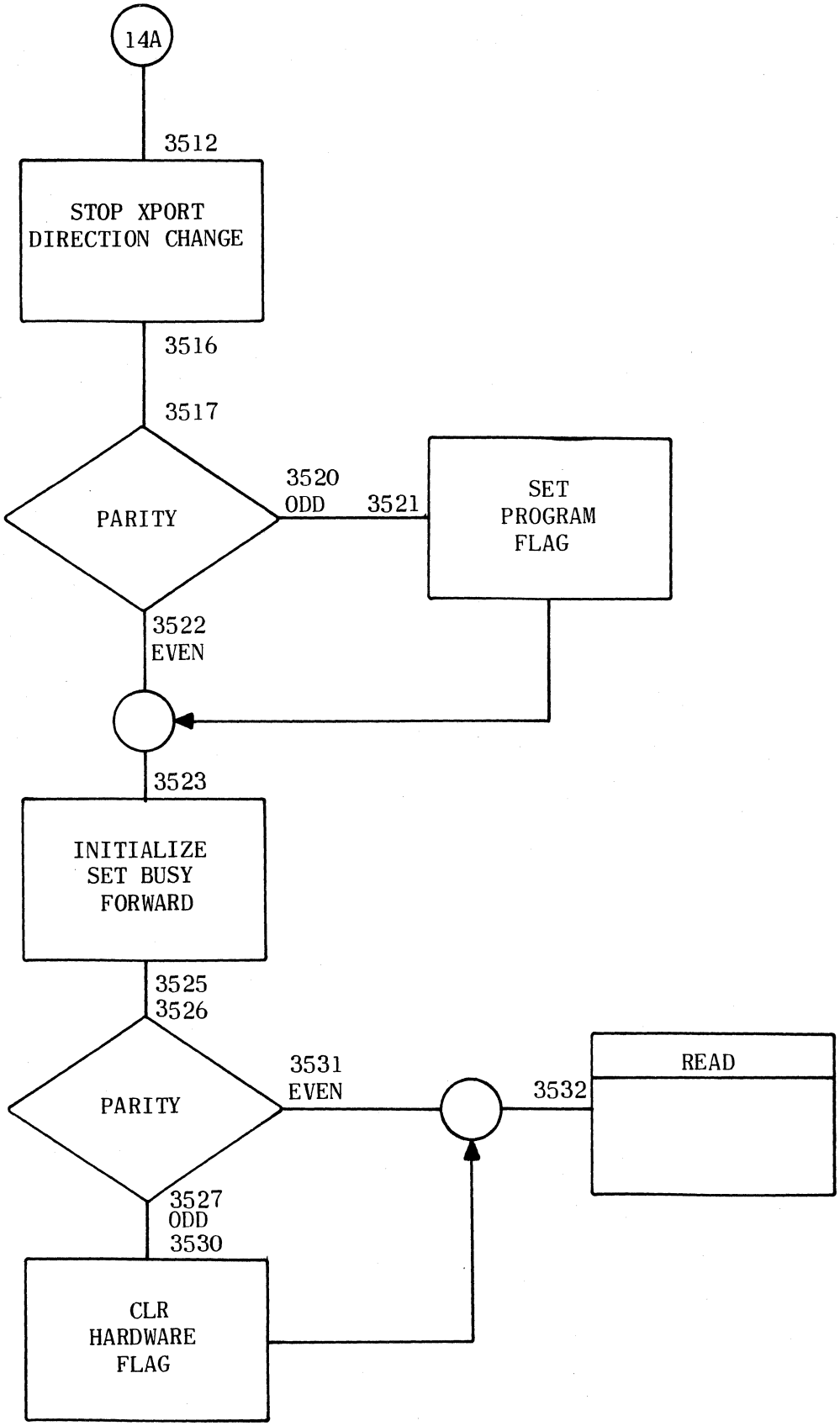


Figure 4-36. Backsearch Sequence Flow Diagram (Sheet 14 of 14)

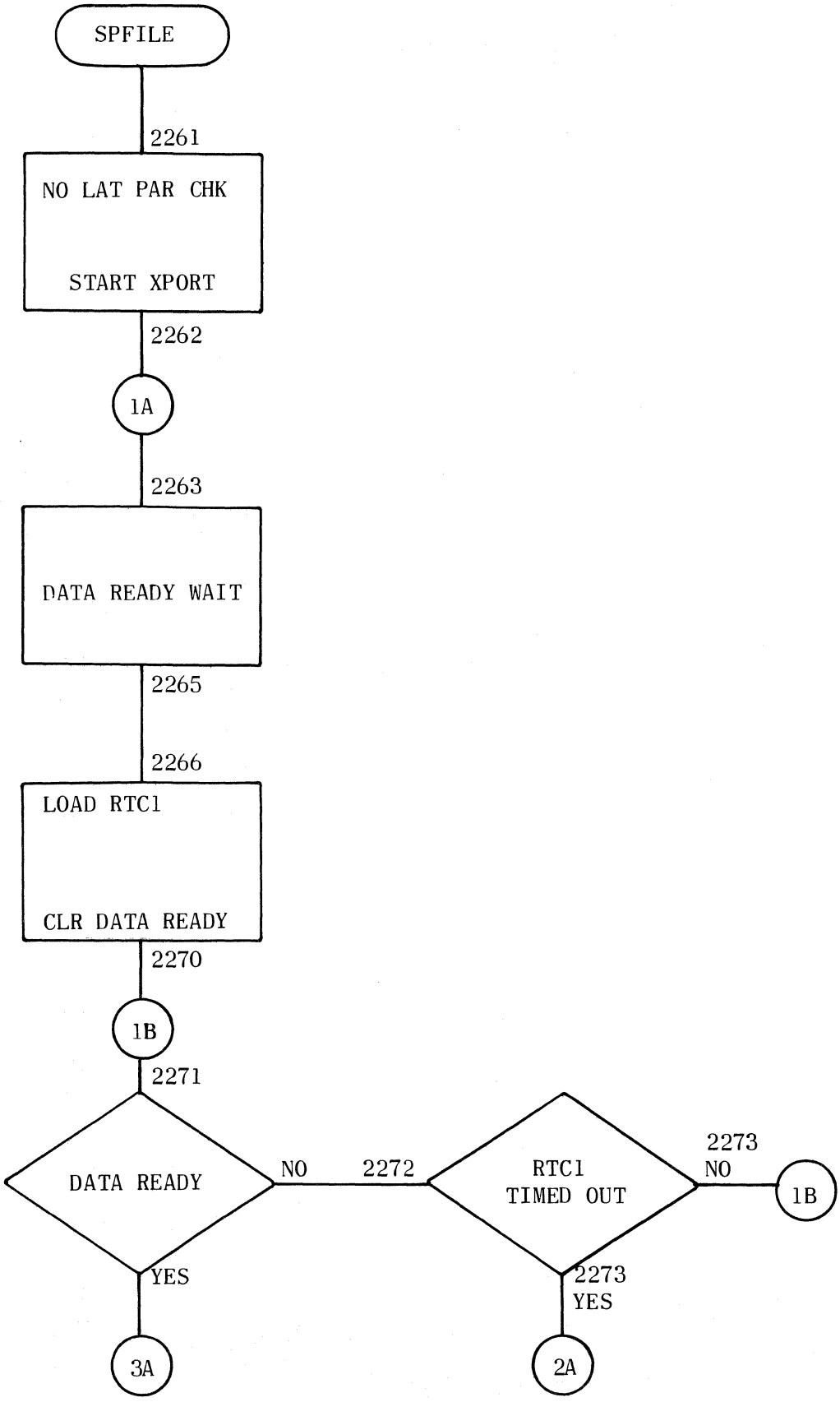


Figure 4-37. Space File Sequence Flow Diagram (Sheet 1 of 3)

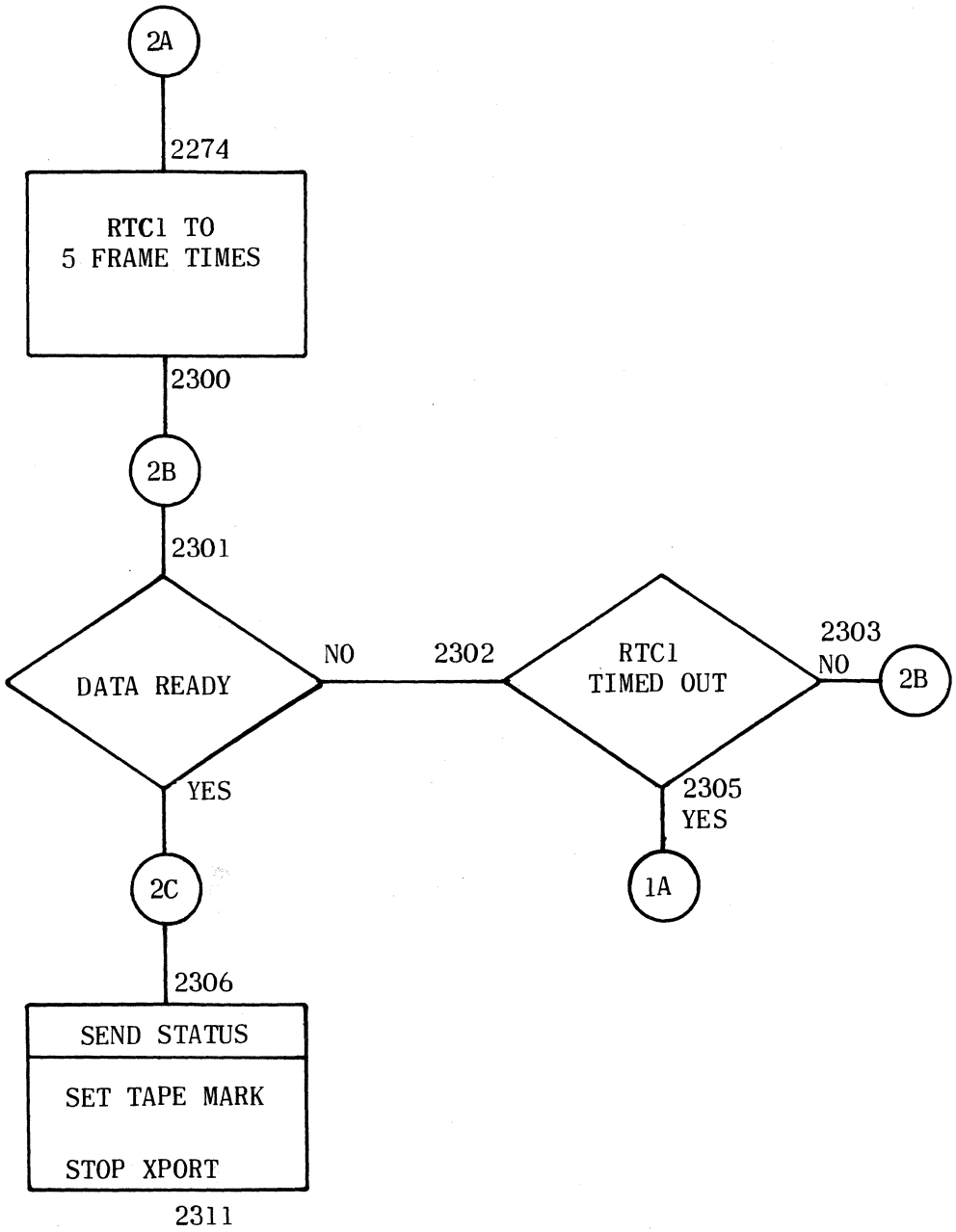


Figure 4-37. Space File Sequence Flow Diagram (Sheet 2 of 3)

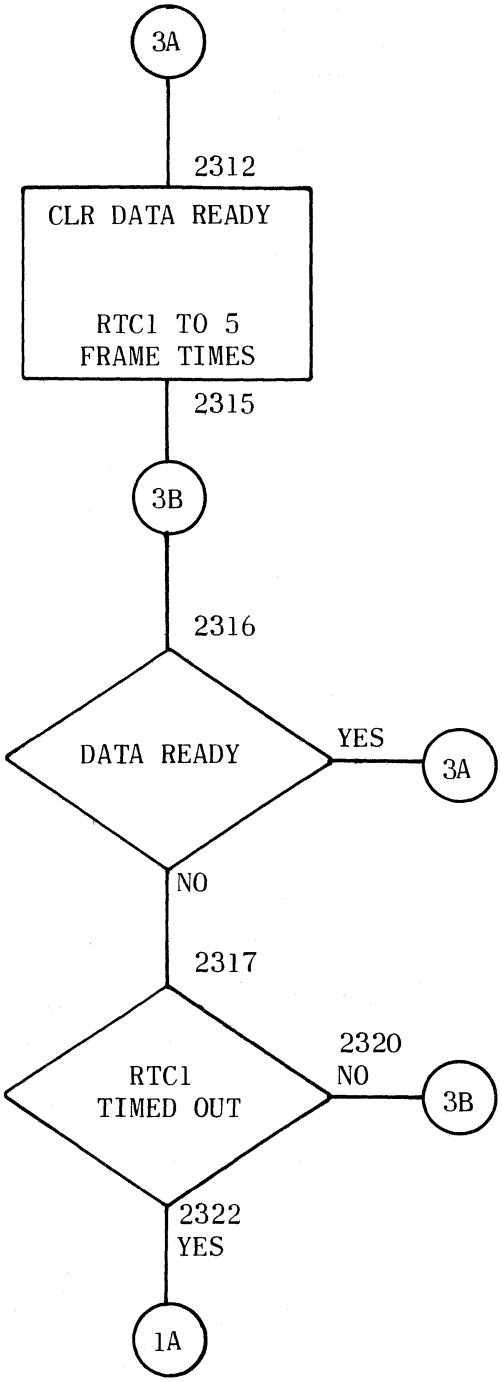


Figure 4-37. Space File Sequence Flow Diagram (Sheet 3 of 3)

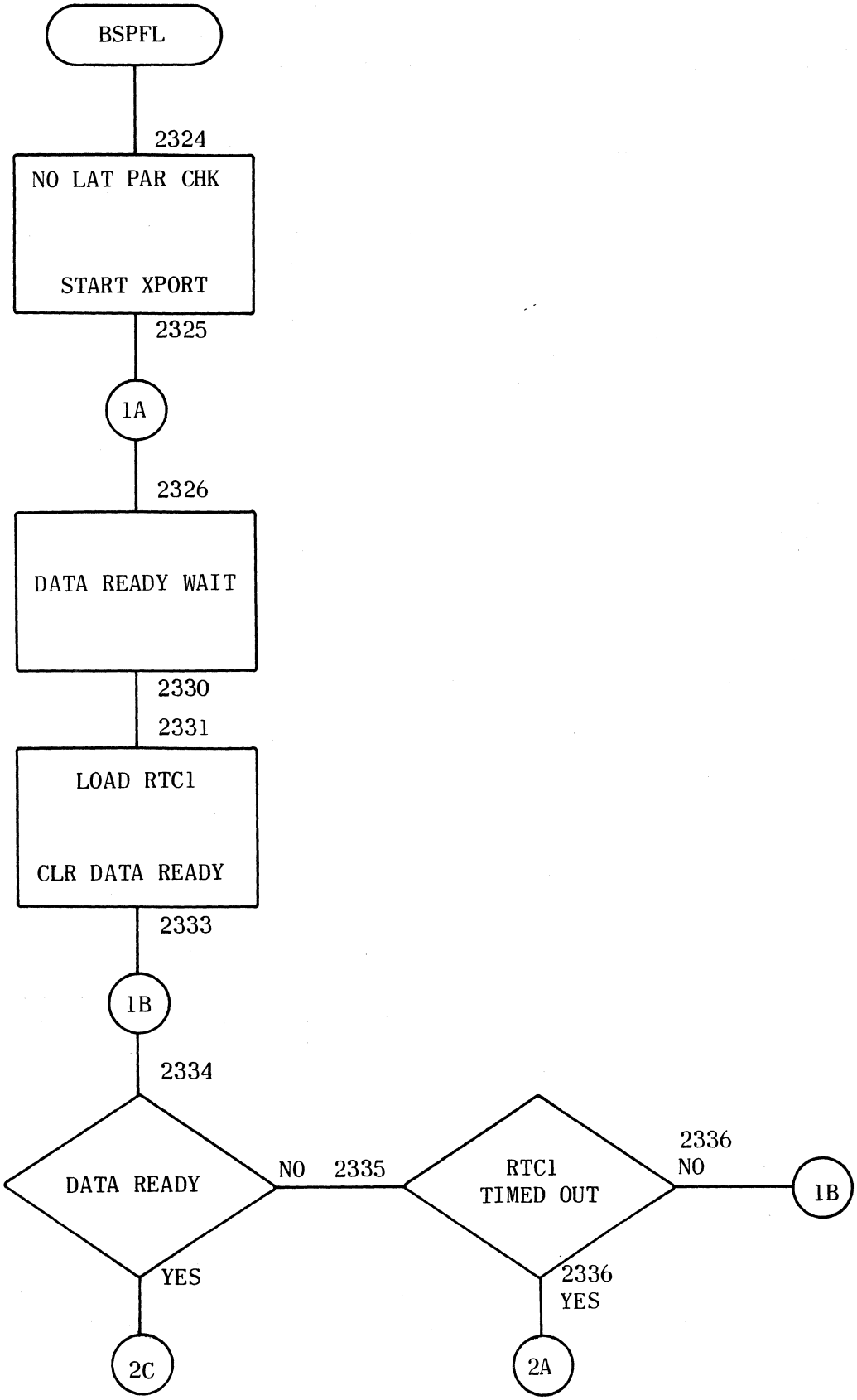


Figure 4-38. Backspace File Sequence Flow Diagram (Sheet 1 of 2)

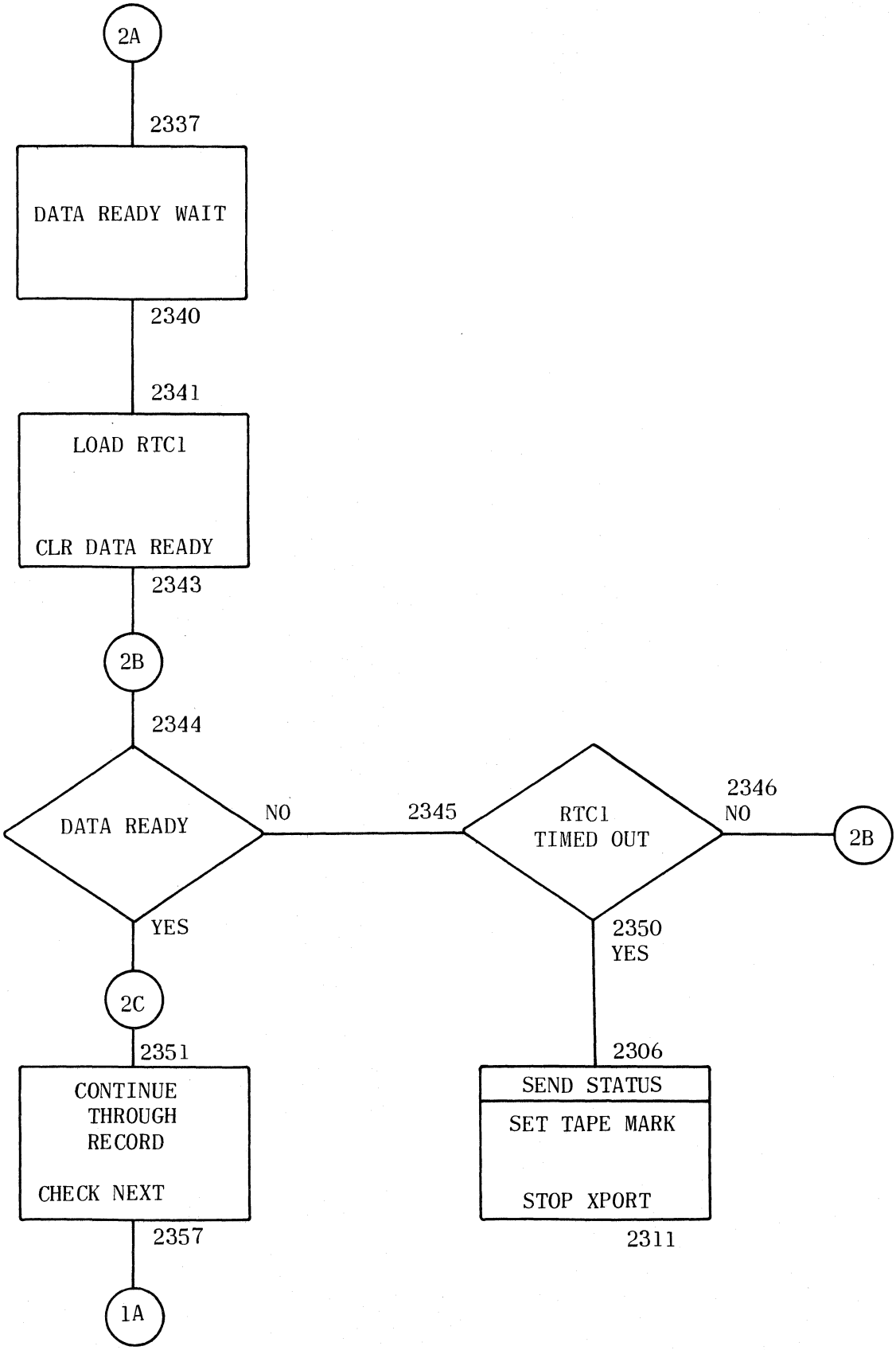


Figure 4-38. Backspace File Sequence Flow Diagram (Sheet 2 of 2)

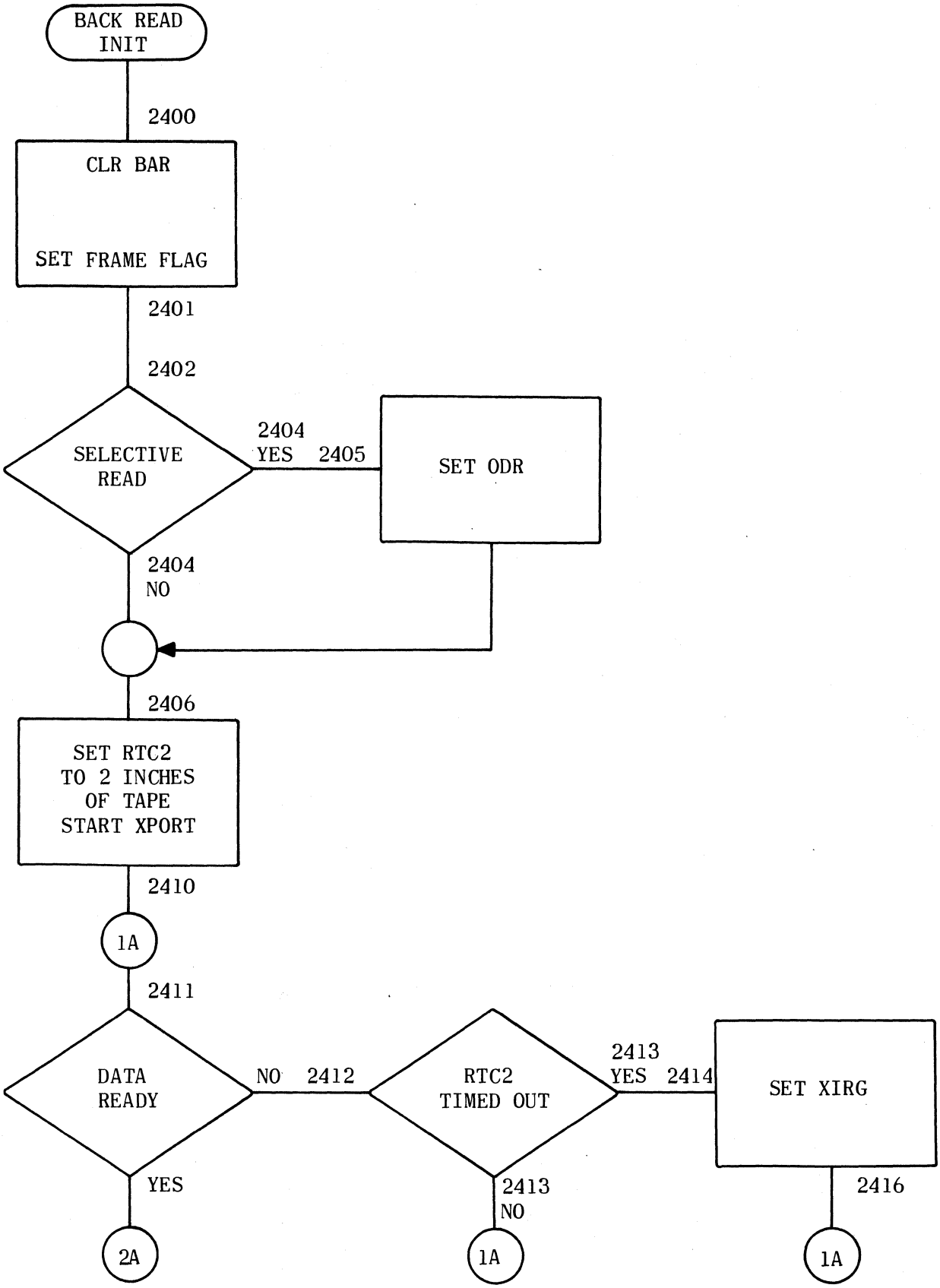


Figure 4-39. Back Read Initiation Sequence Flow Diagram (Sheet 1 of 2)

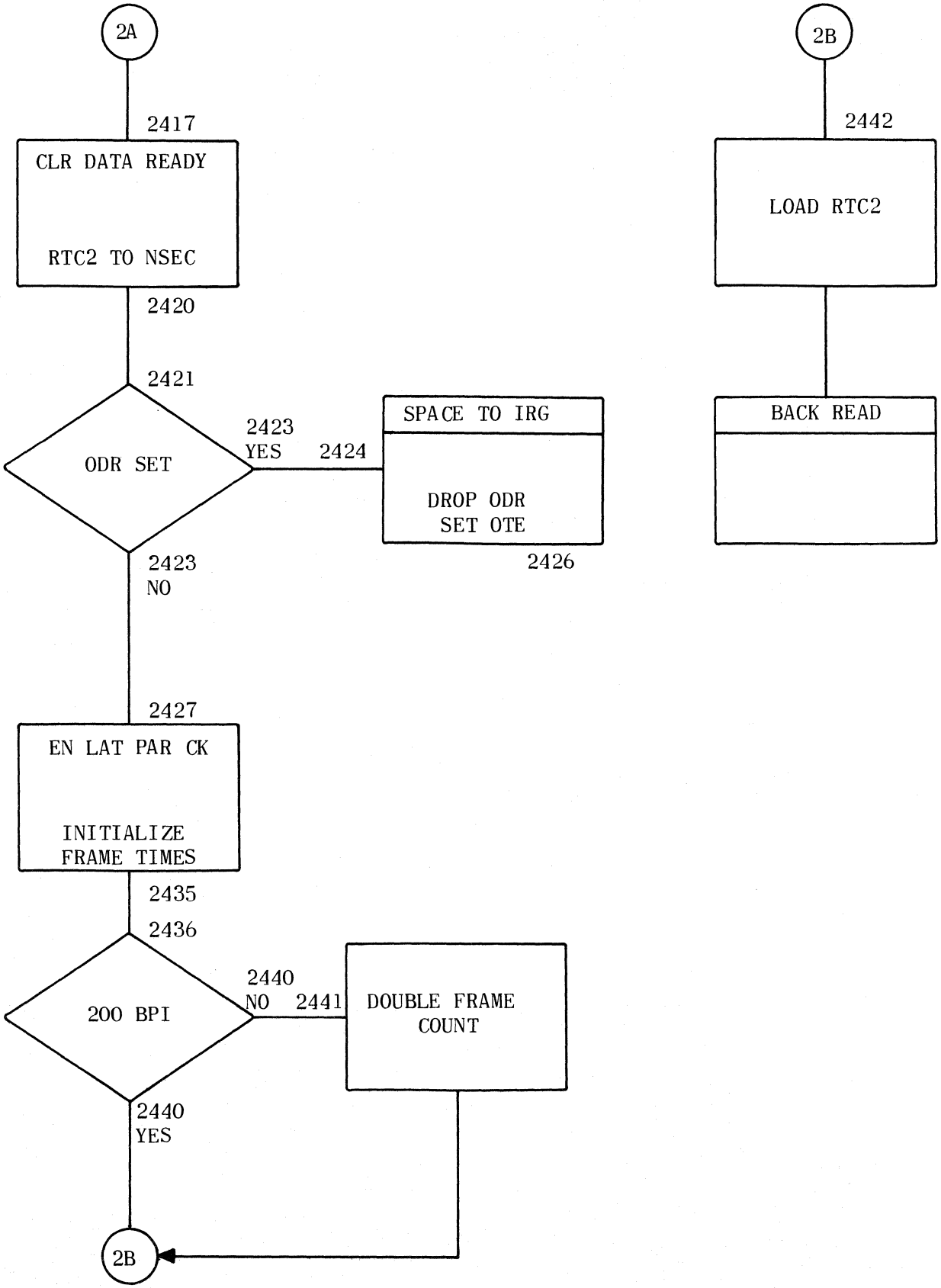


Figure 4-39. Back Read Initiation Sequence Flow Diagram (Sheet 2 of 2)

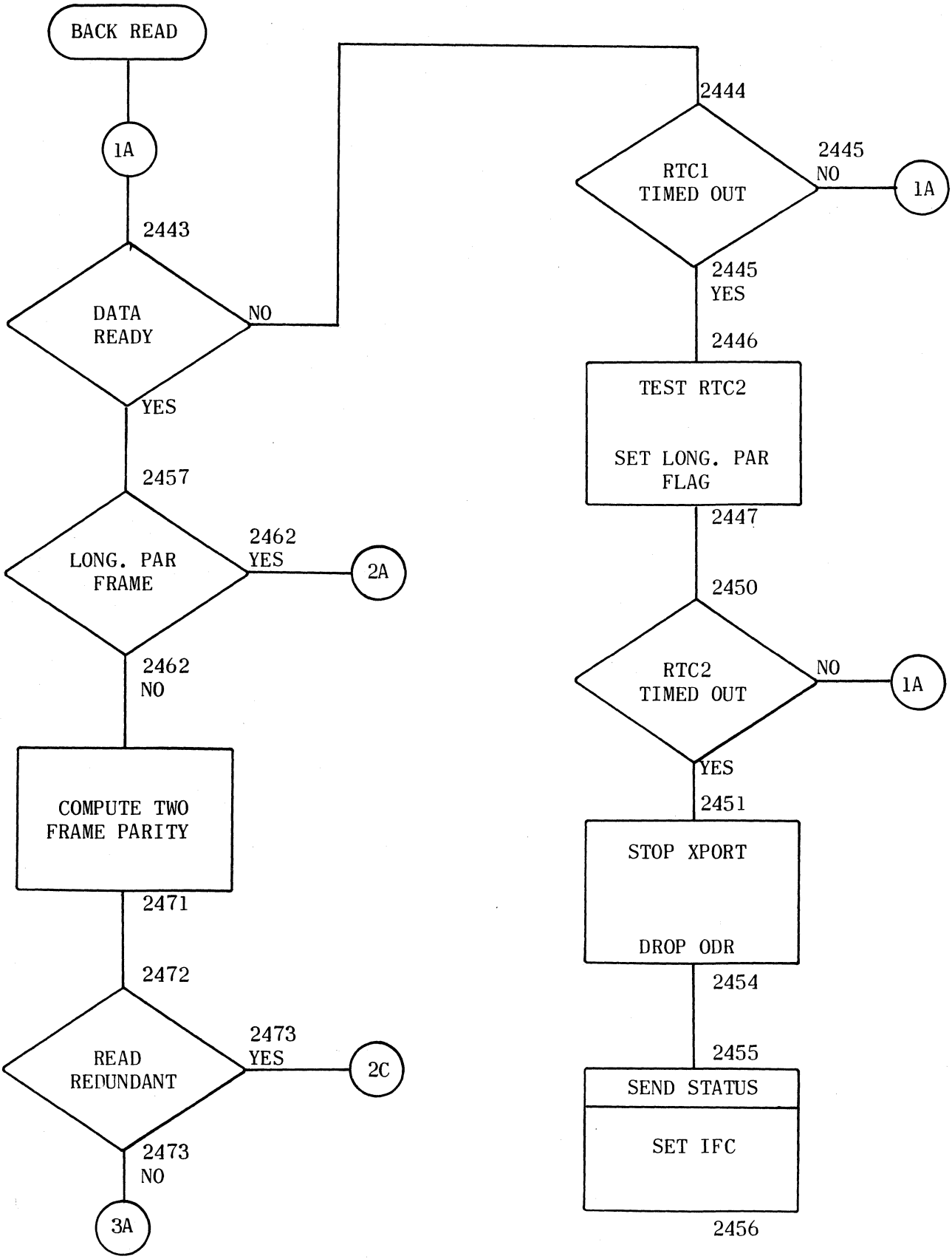


Figure 4-40. Back Read Sequence Flow Diagram (Sheet 1 of 6)

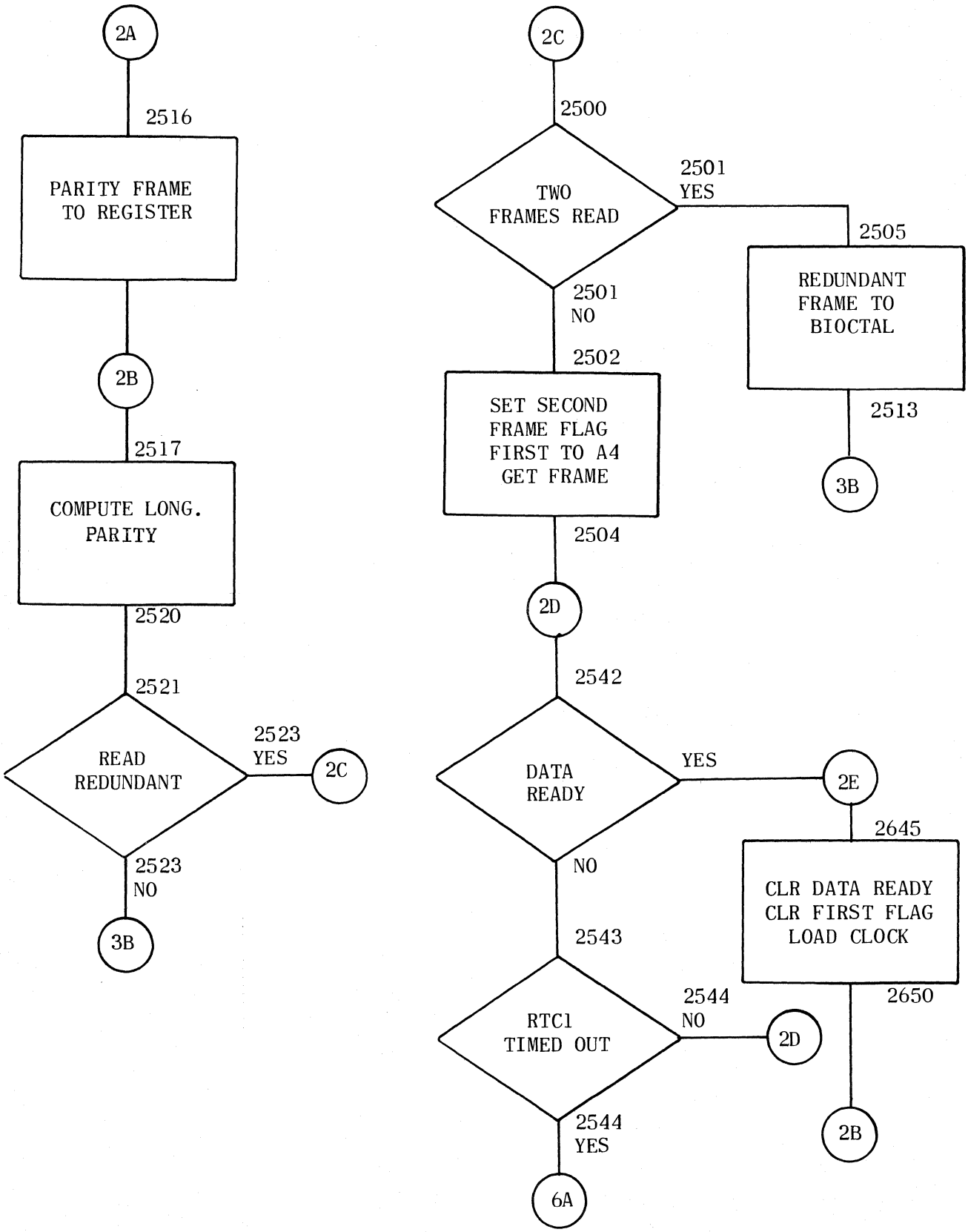


Figure 4-40. Back Read Sequence Flow Diagram (Sheet 2 of 6)

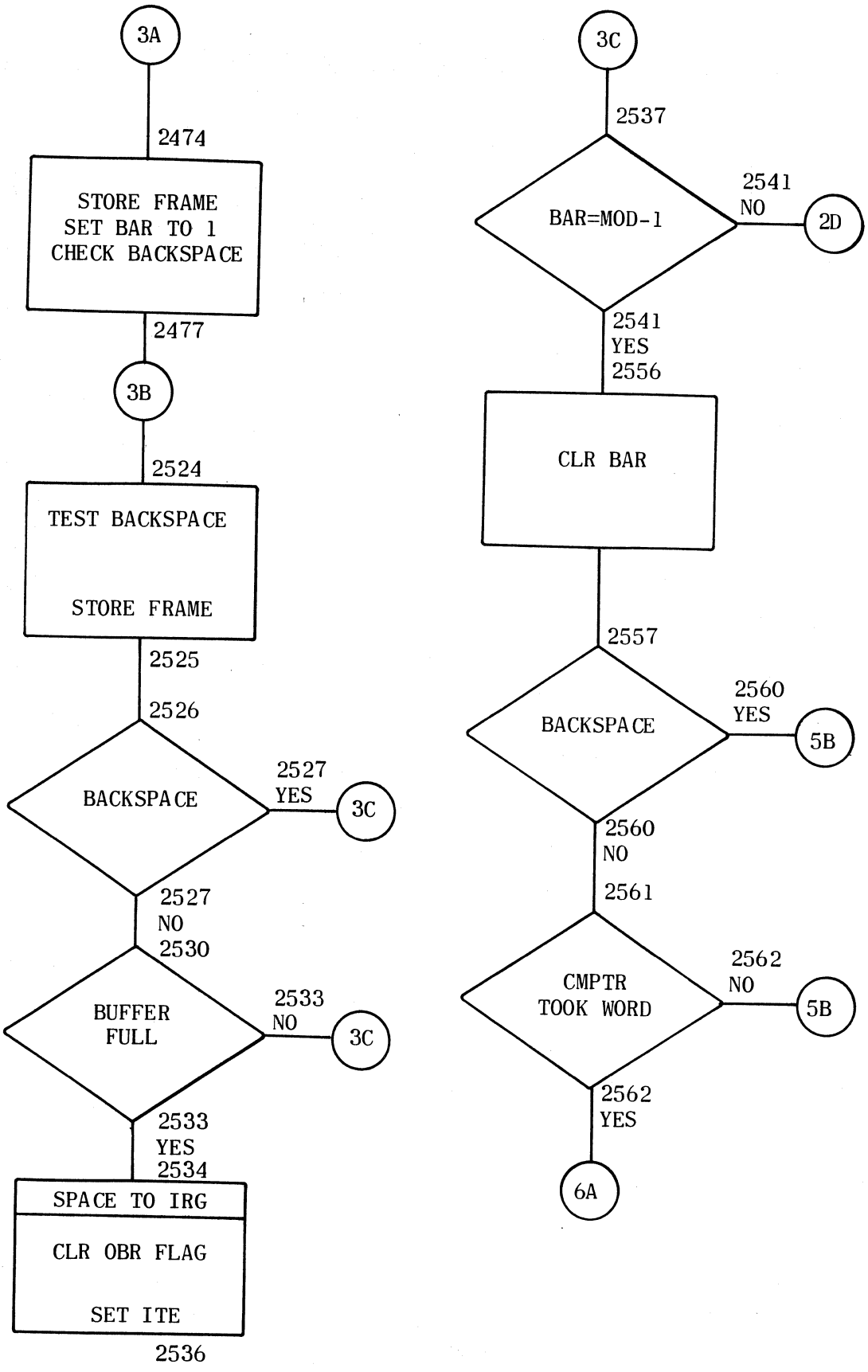


Figure 4-40. Back Read Sequence Flow Diagram (Sheet 3 of 6)

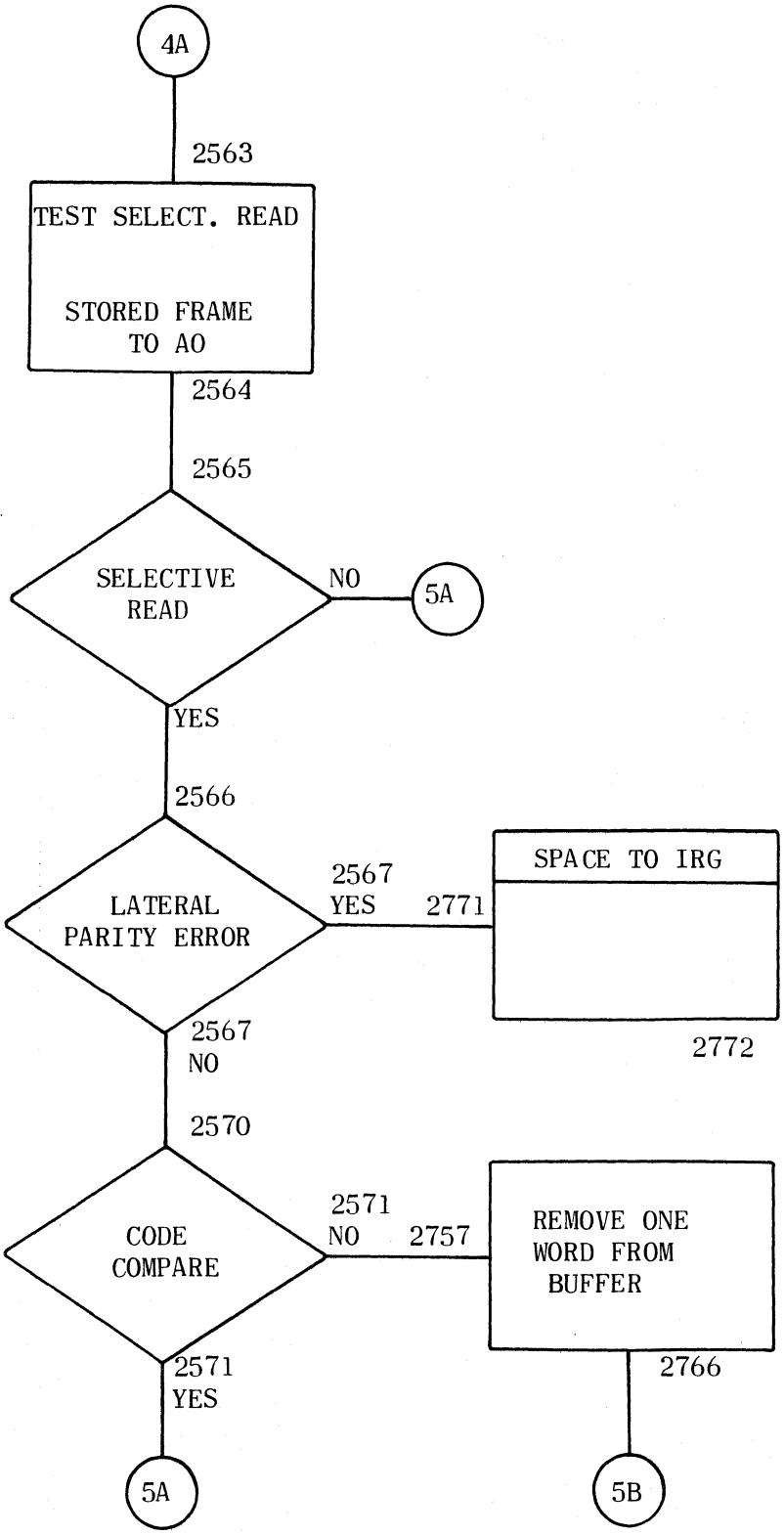


Figure 4-40. Back Read Sequence Flow Diagram (Sheet 4 of 6)

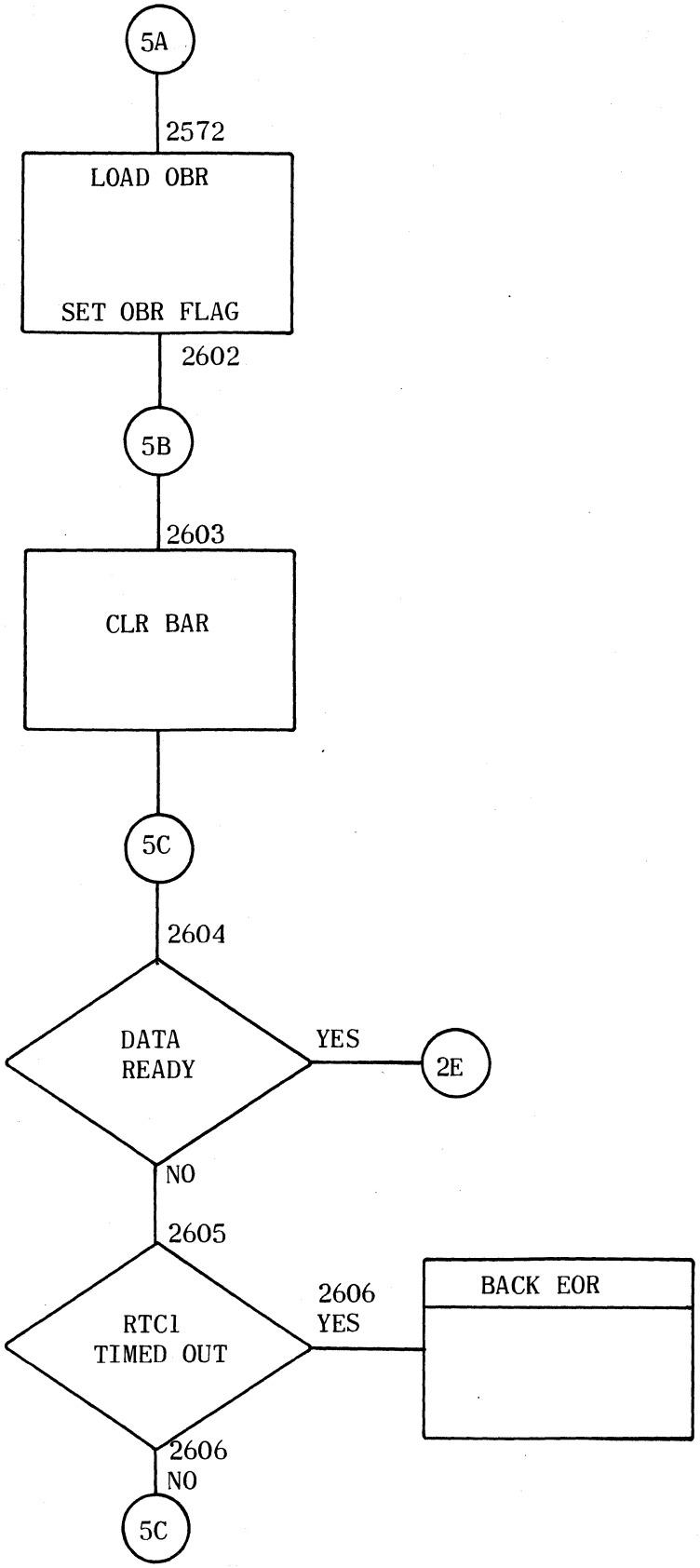


Figure 4-40. Back Read Sequence Flow Diagram (Sheet 5 of 6)

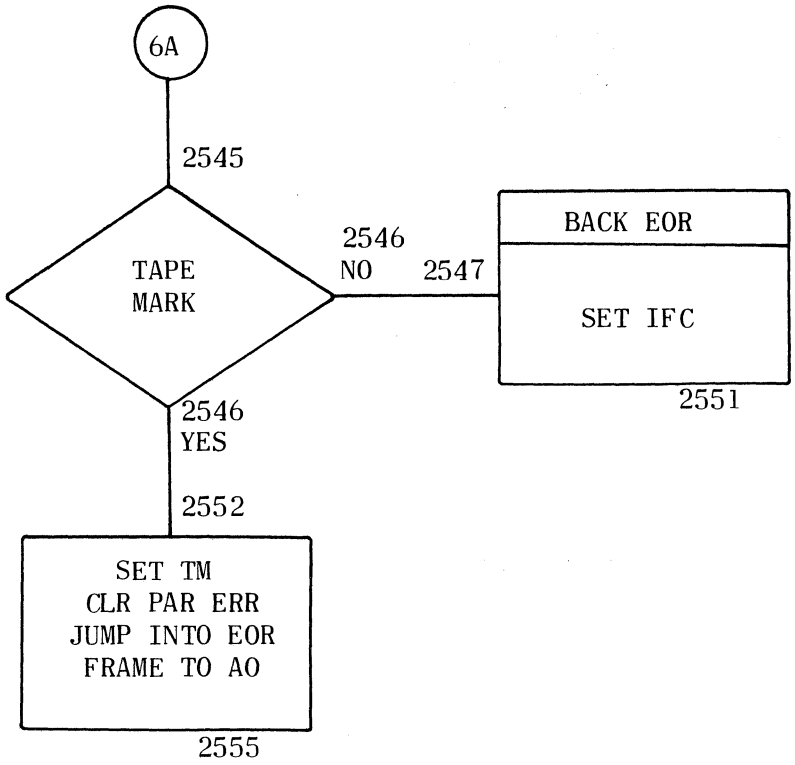


Figure 4-40. Back Read Sequence Flow Diagram (Sheet 6 of 6)

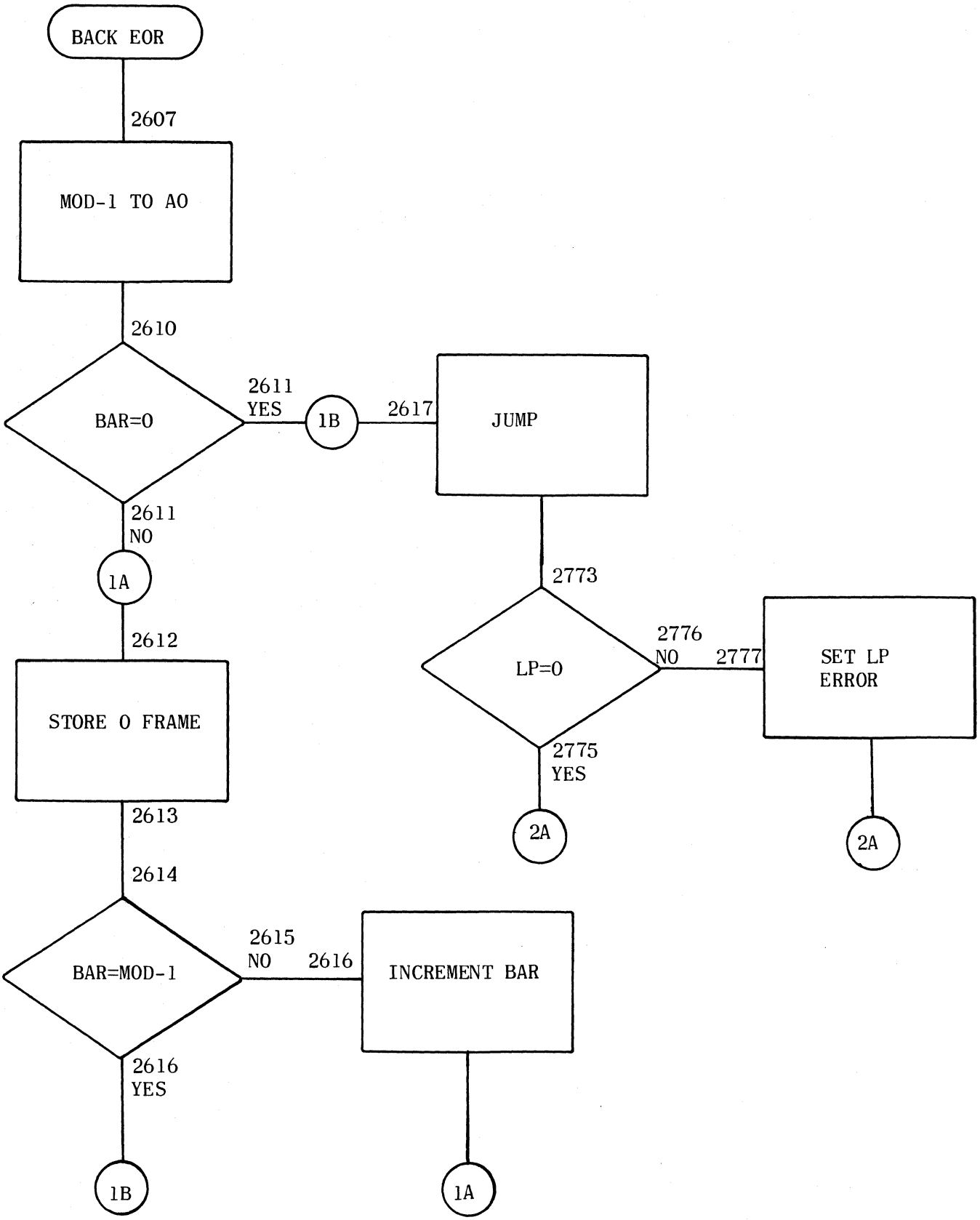


Figure 4-41. Back End of Record Sequence Flow Diagram (Sheet 1 of 6)

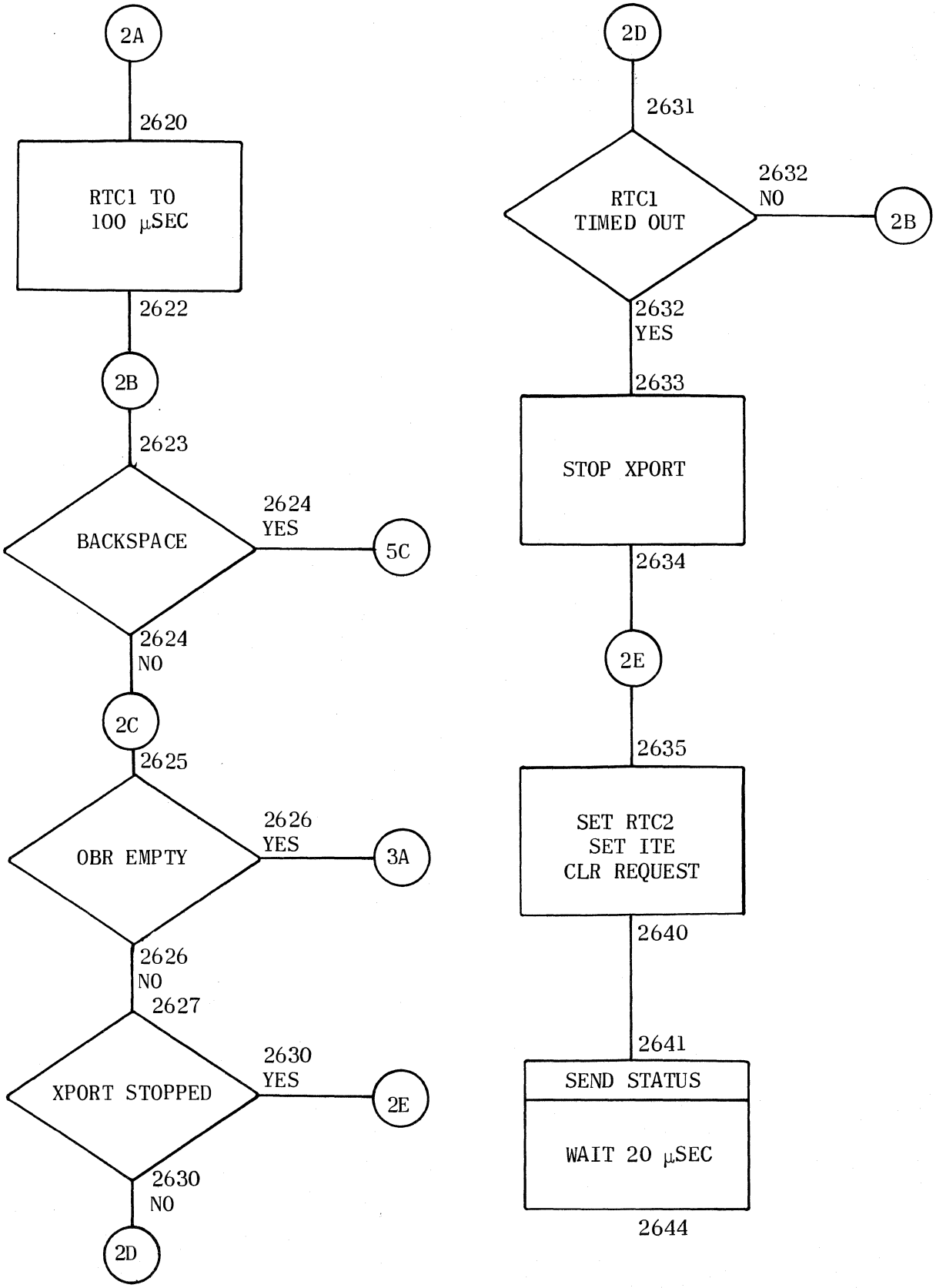


Figure 4-41. Back End of Record Sequence Flow Diagram (Sheet 2 of 6)

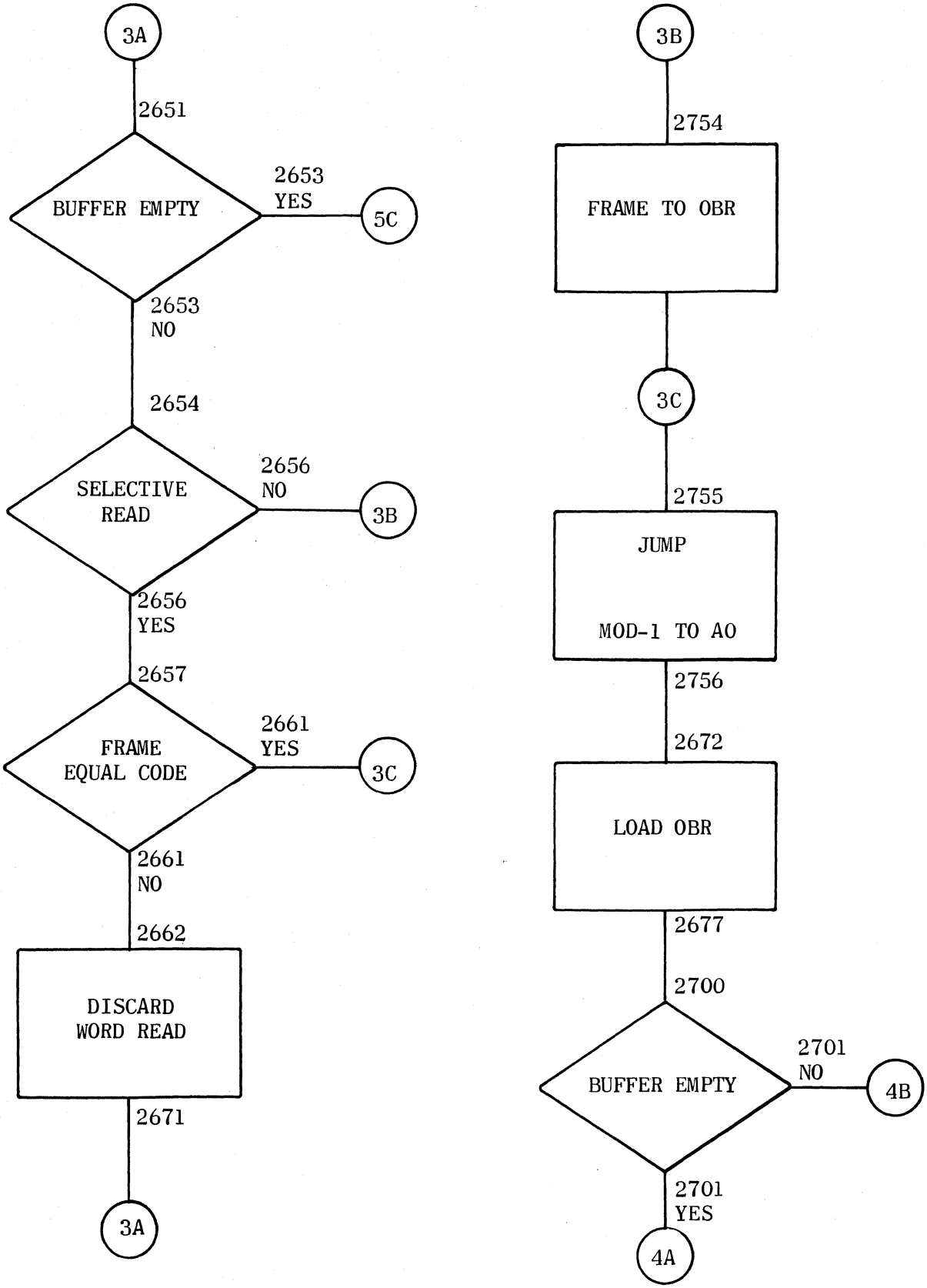


Figure 4-41. Back End of Record Sequence Flow Diagram (Sheet 3 of 6)

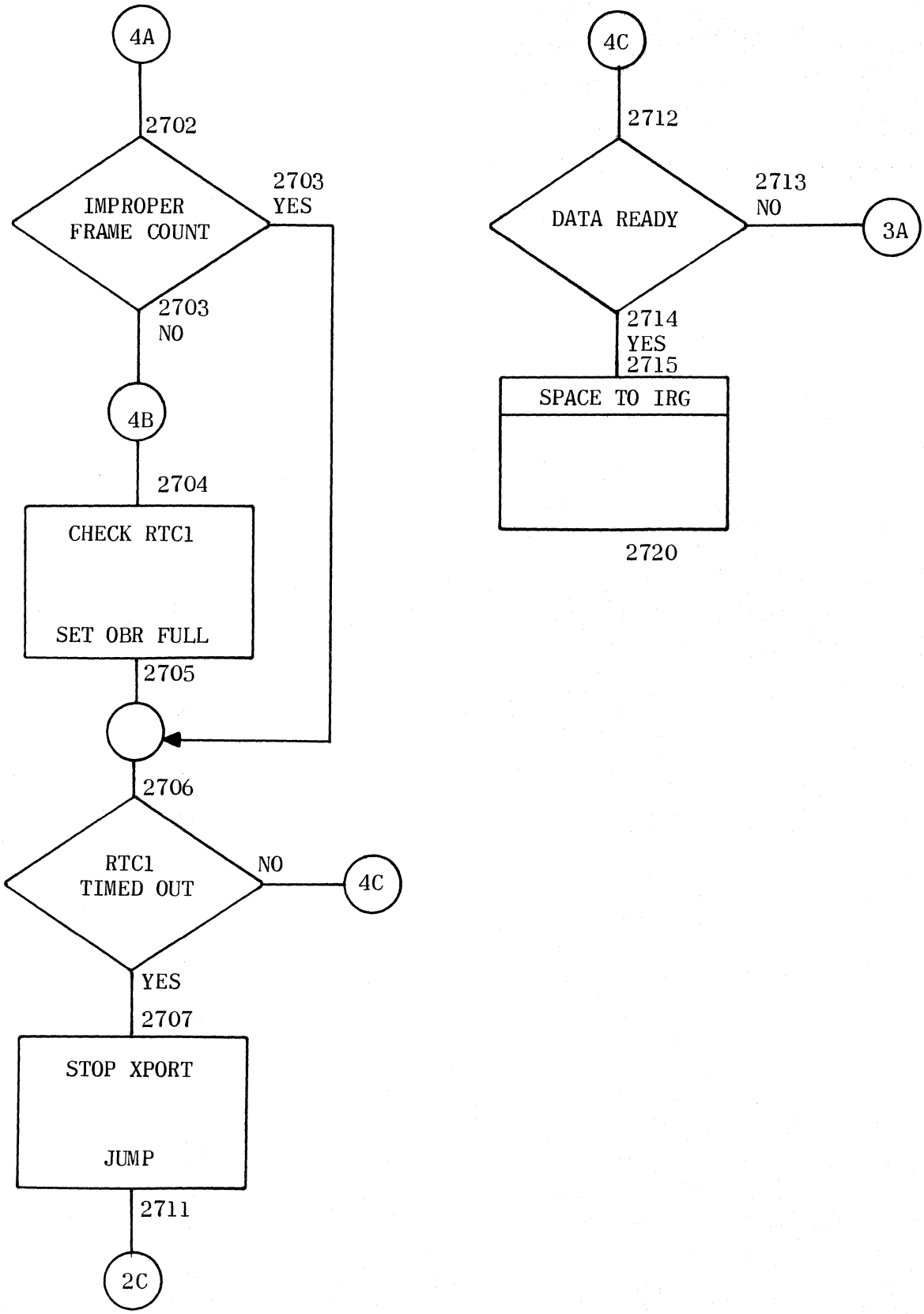


Figure 4-41. Back End of Record Sequence Flow Diagram (Sheet 4 of 6)

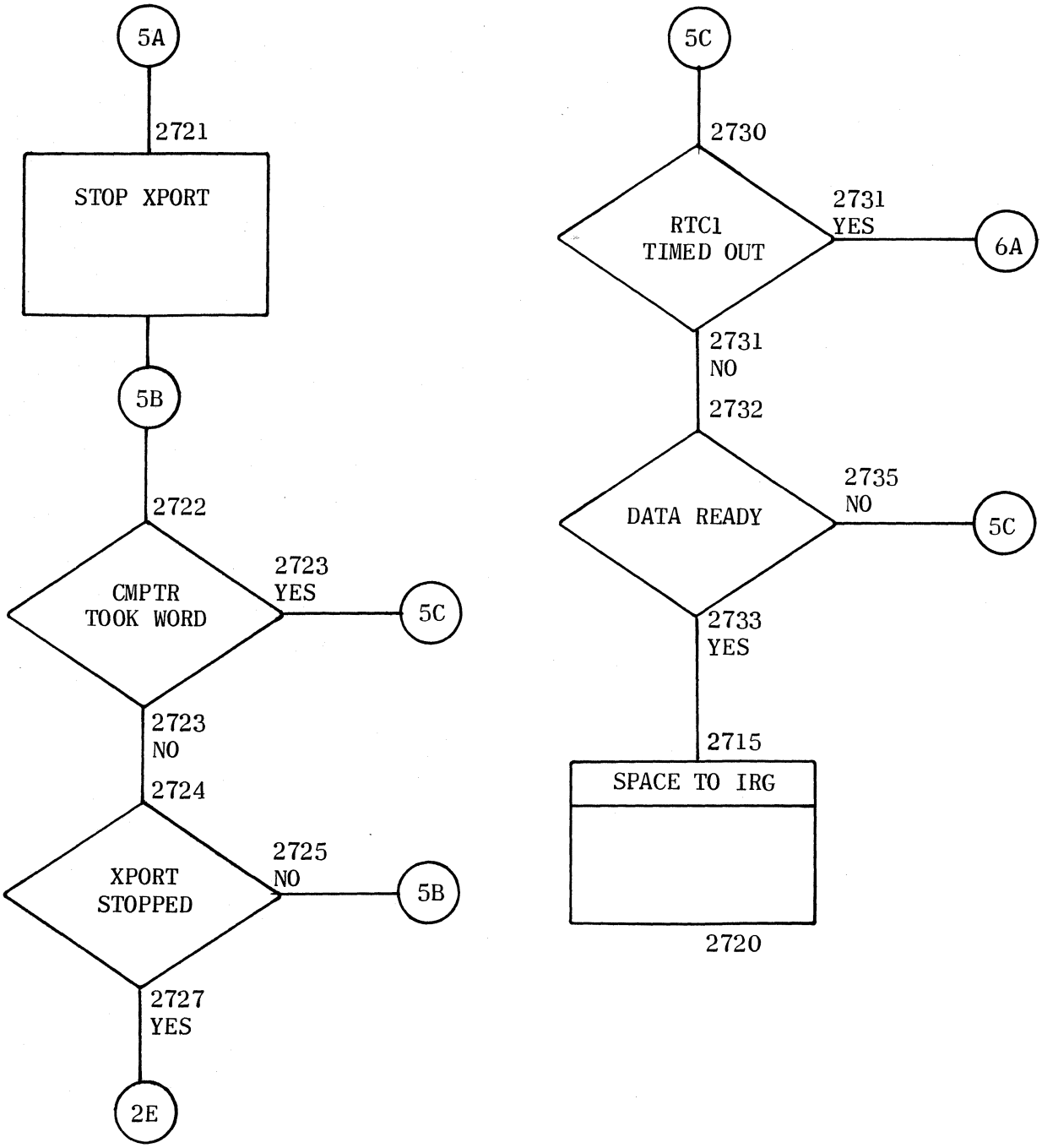


Figure 4-41. Back End of Record Sequence Flow Diagram (Sheet 5 of 6)

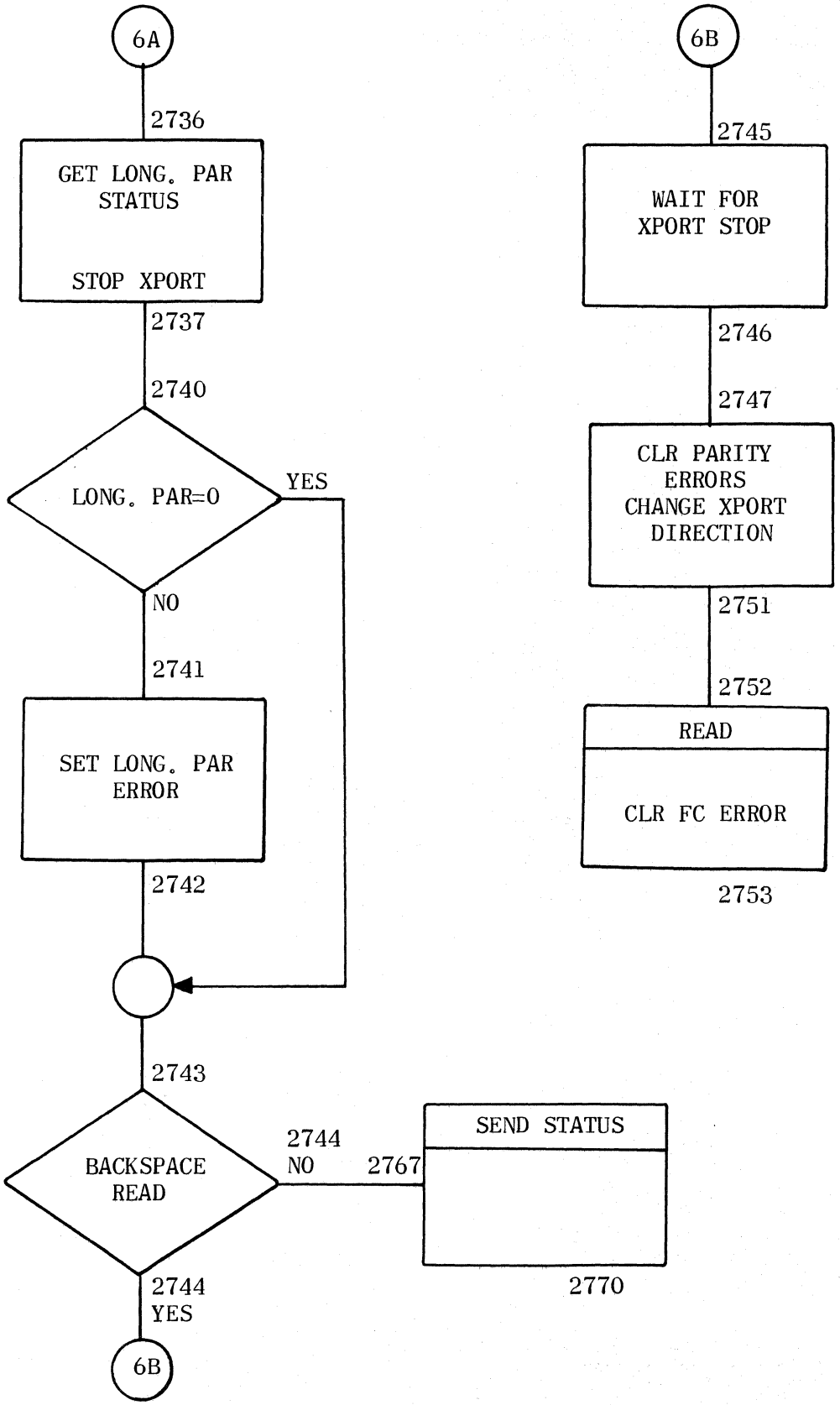


Figure 4-41. Back End of Record Sequence Flow Diagram (Sheet 6 of 6)

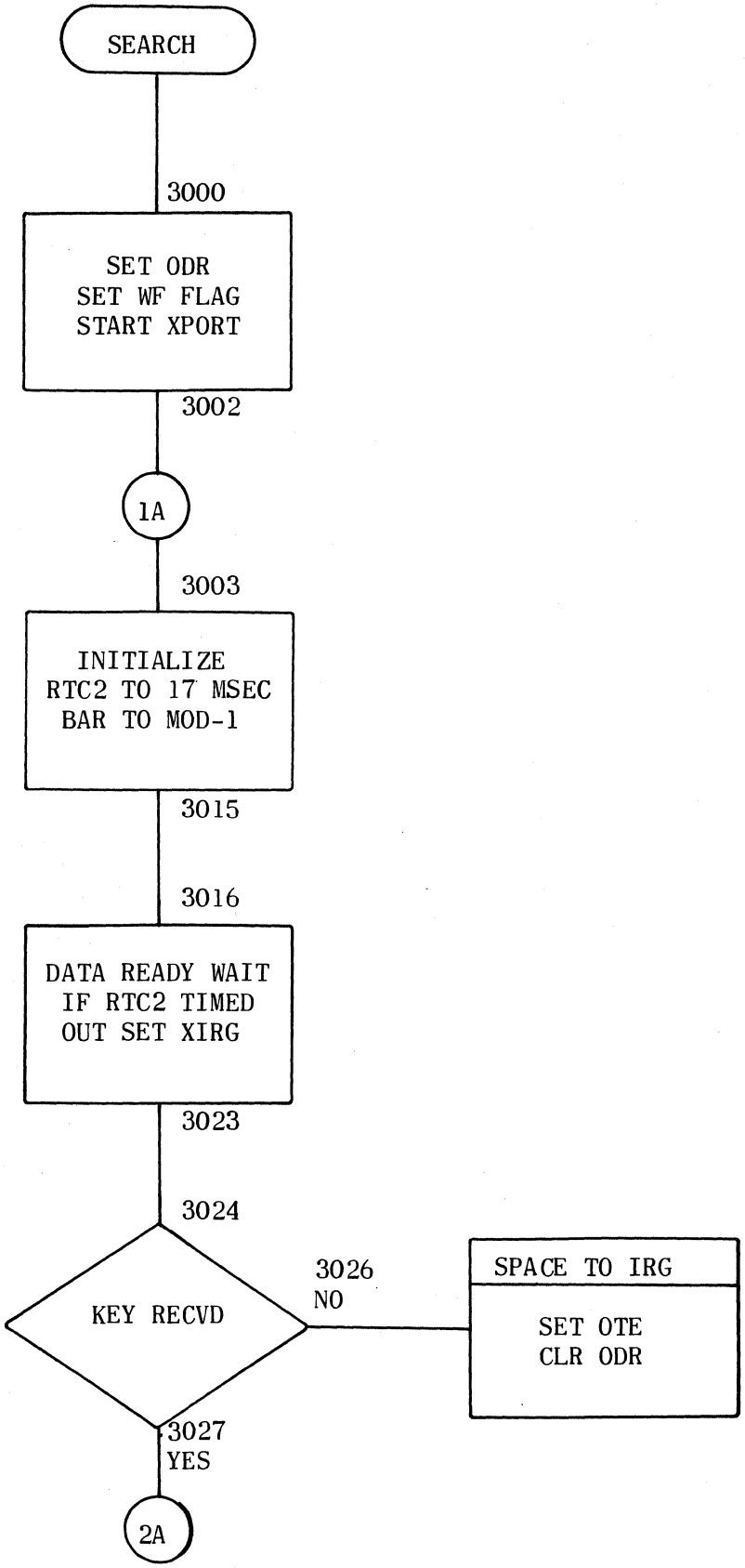


Figure 4-42. Search Sequence Flow Diagram (Sheet 1 of 6)

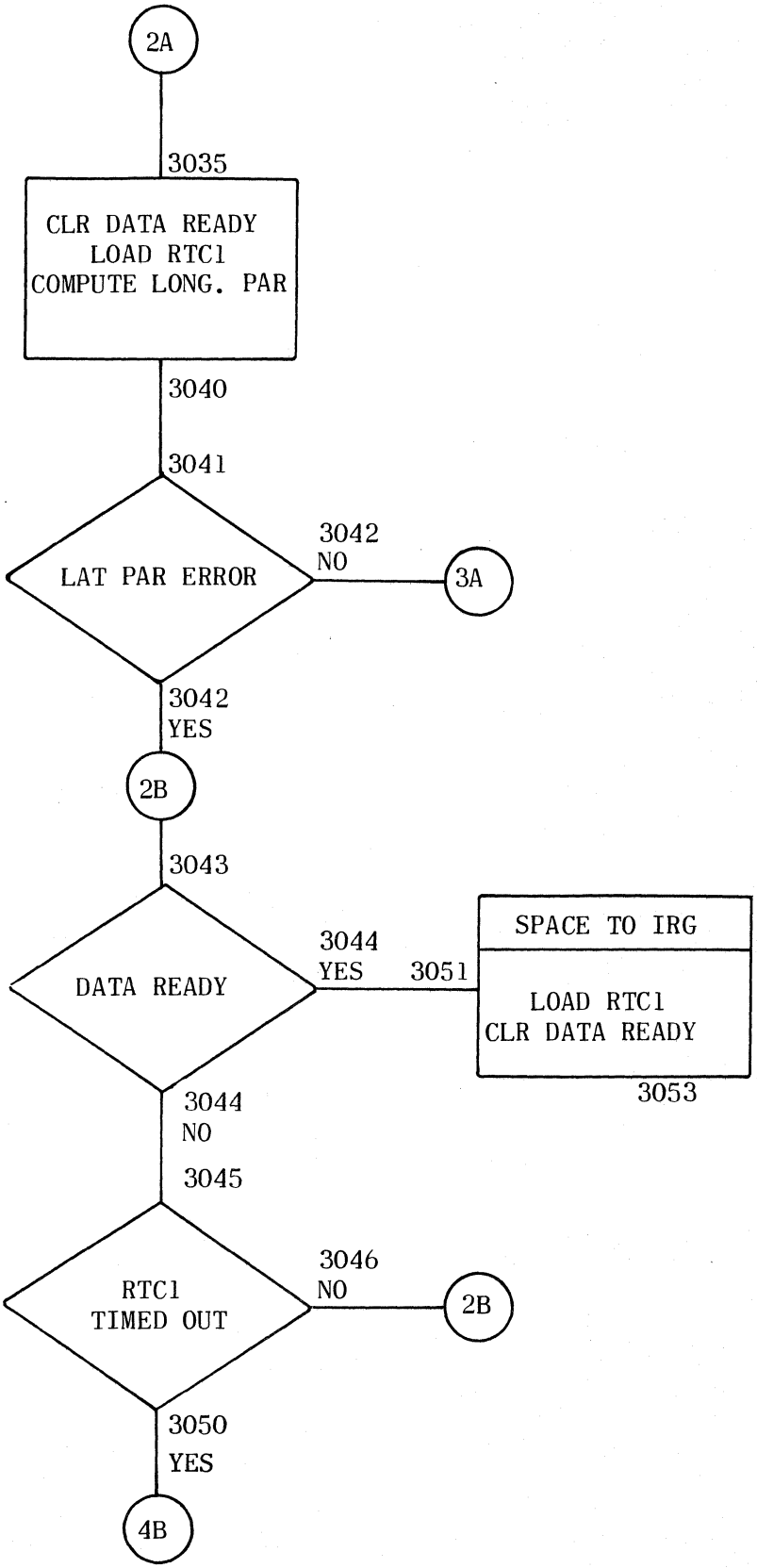


Figure 4-42. Search Sequence Flow Diagram (Sheet 2 of 6)

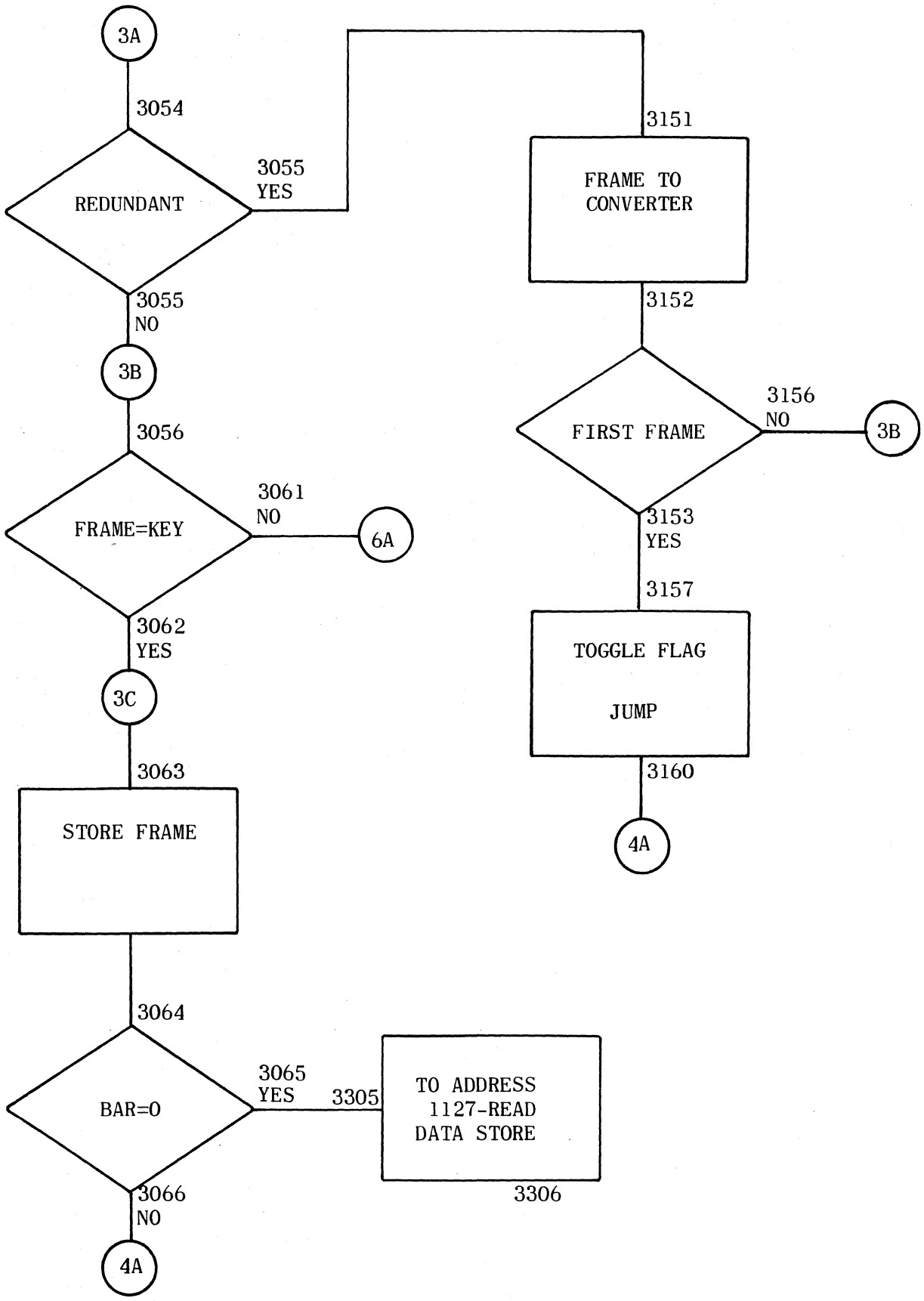


Figure 4-42. Search Sequence Flow Diagram (Sheet 3 of 6)

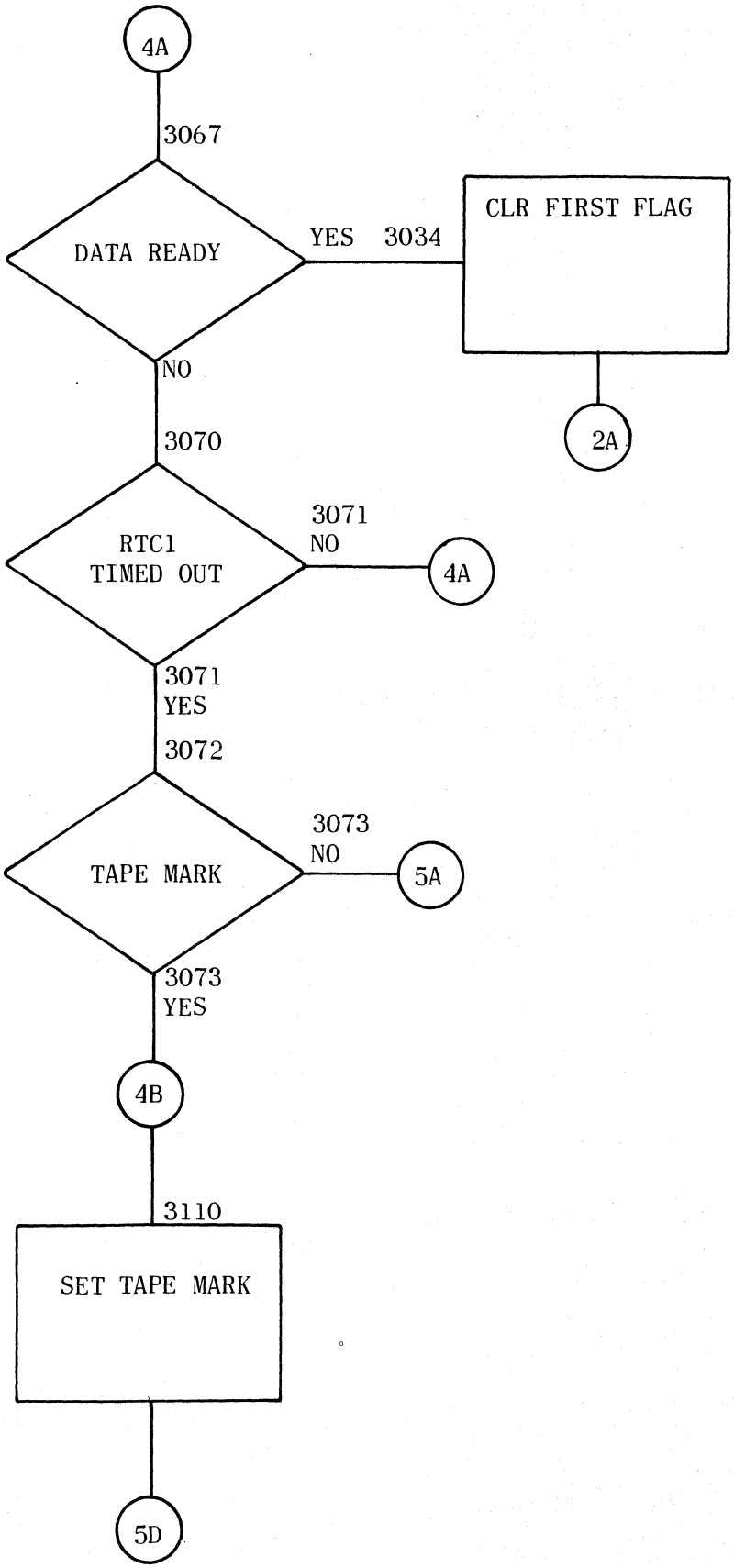


Figure 4-42. Search Sequence Flow Diagram (Sheet 4 of 6)

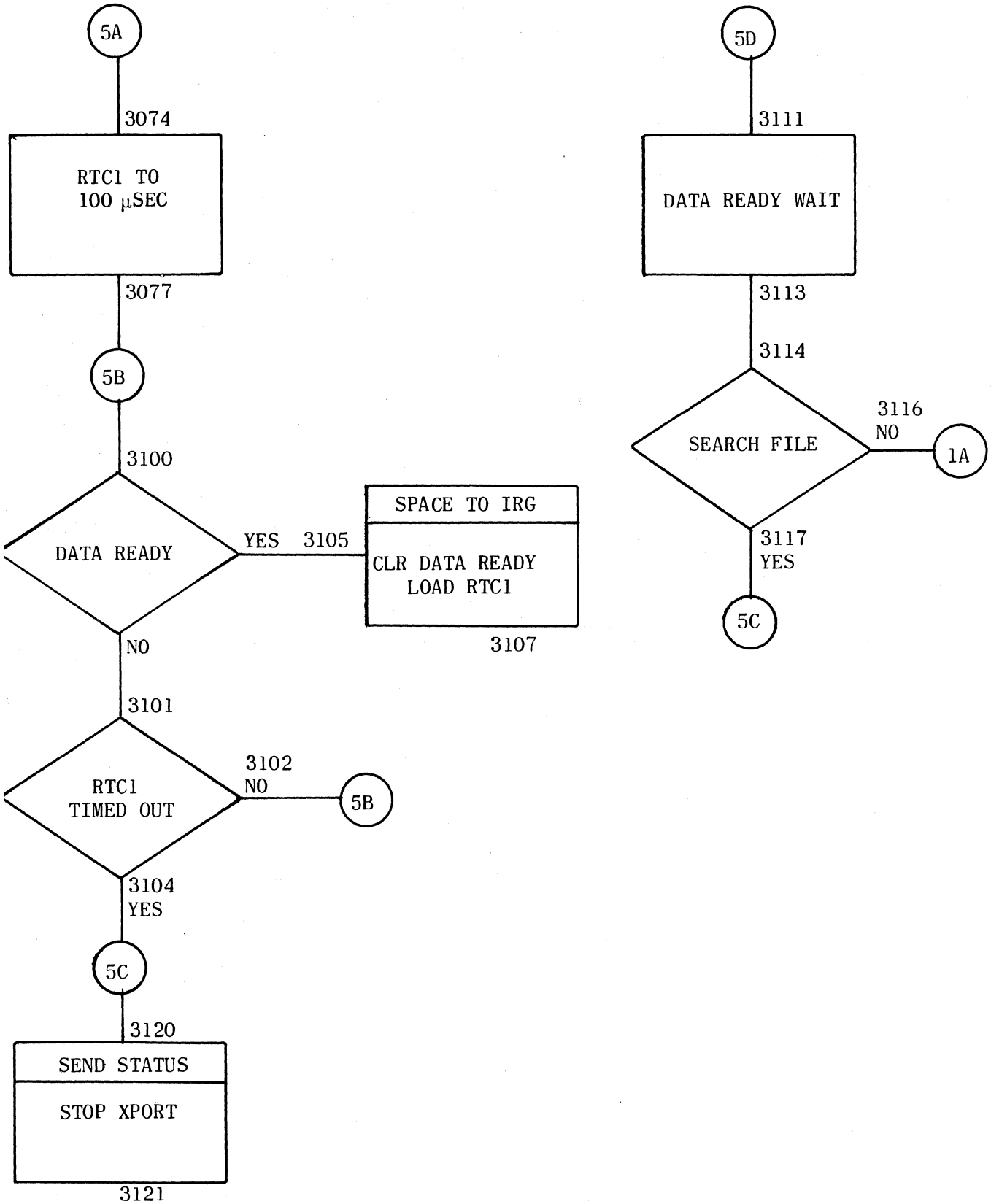


Figure 4-42. Search Sequence Flow Diagram (Sheet 5 of 6)

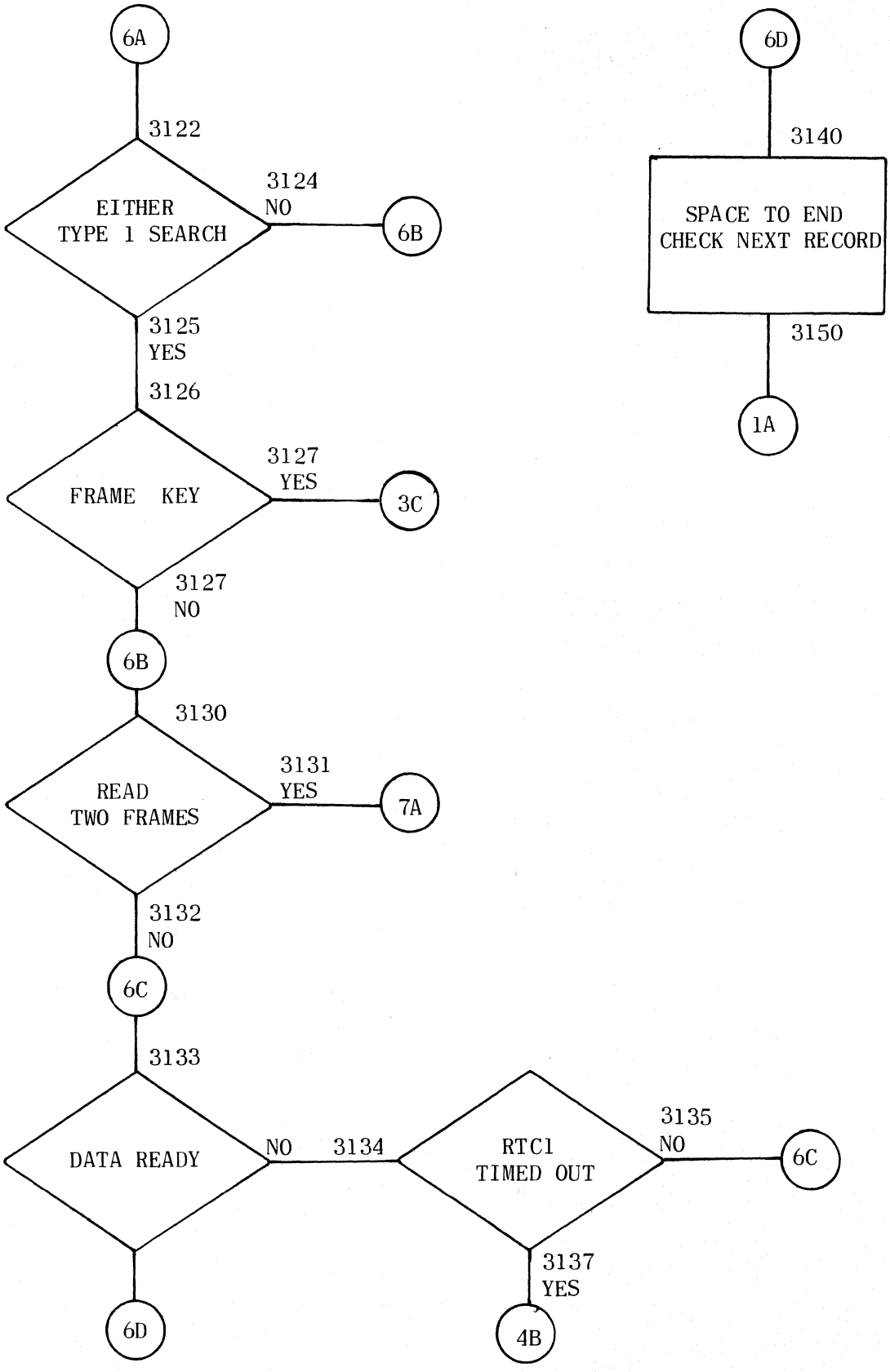


Figure 4-42. Search Sequence Flow Diagram (Sheet 6 of 6)

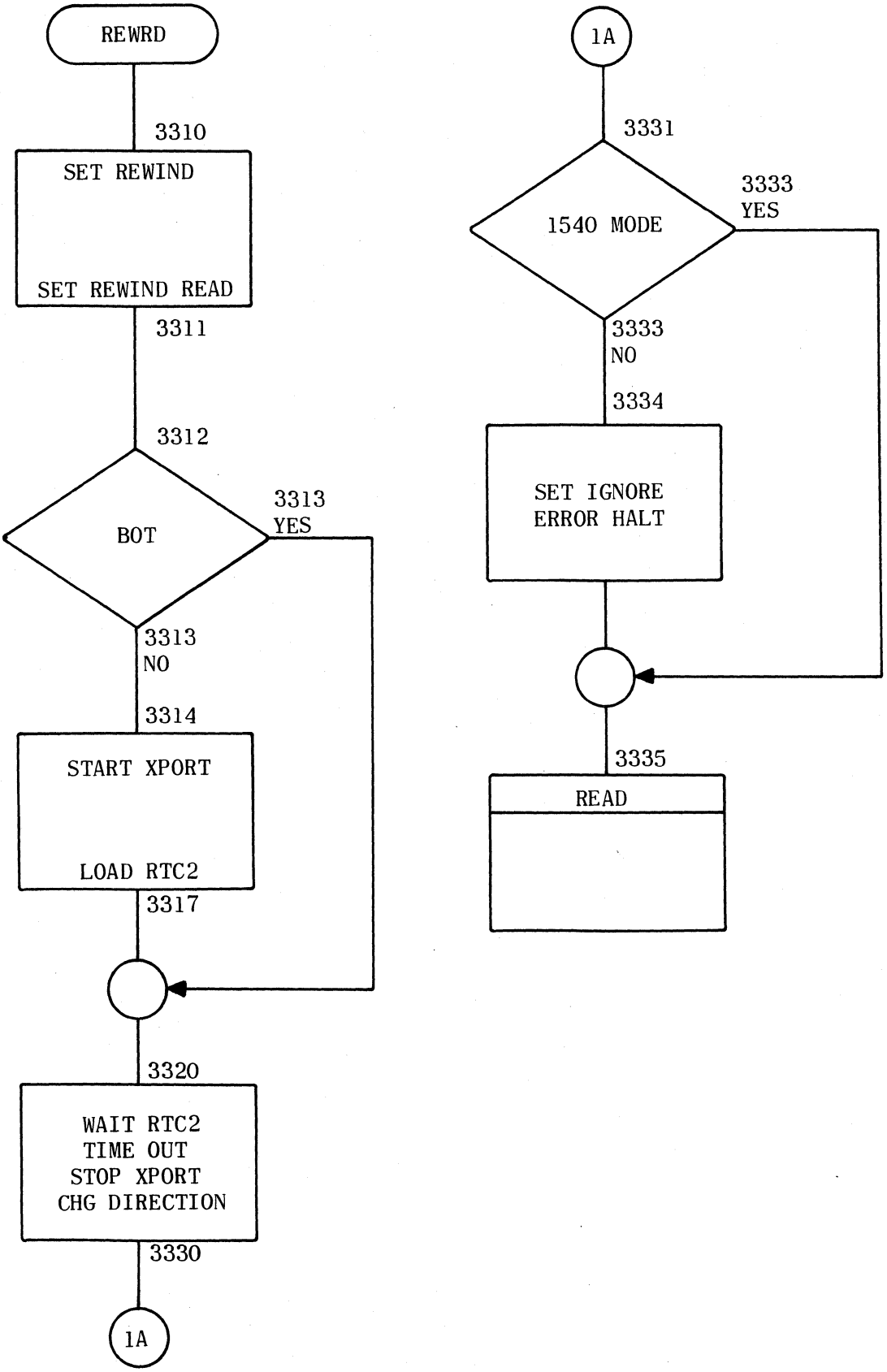


Figure 4-43. Rewind Read Sequence Flow Diagram

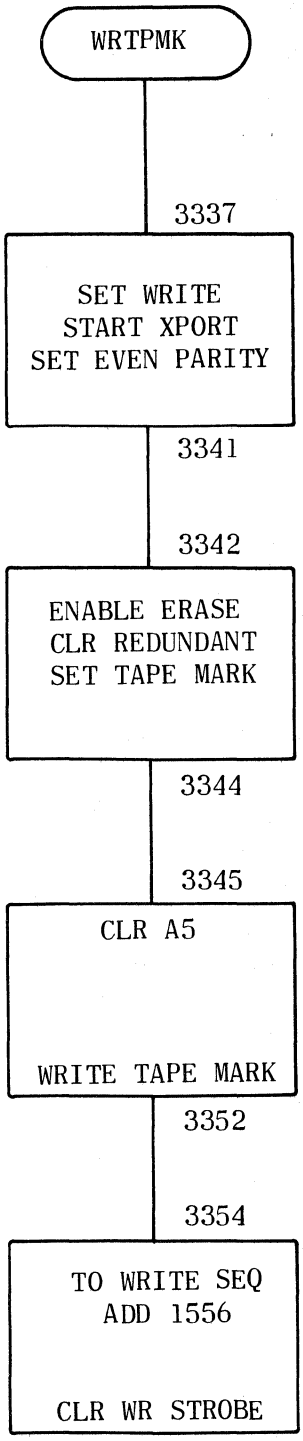


Figure 4-44. Write Tape Mark Sequence Flow Diagram

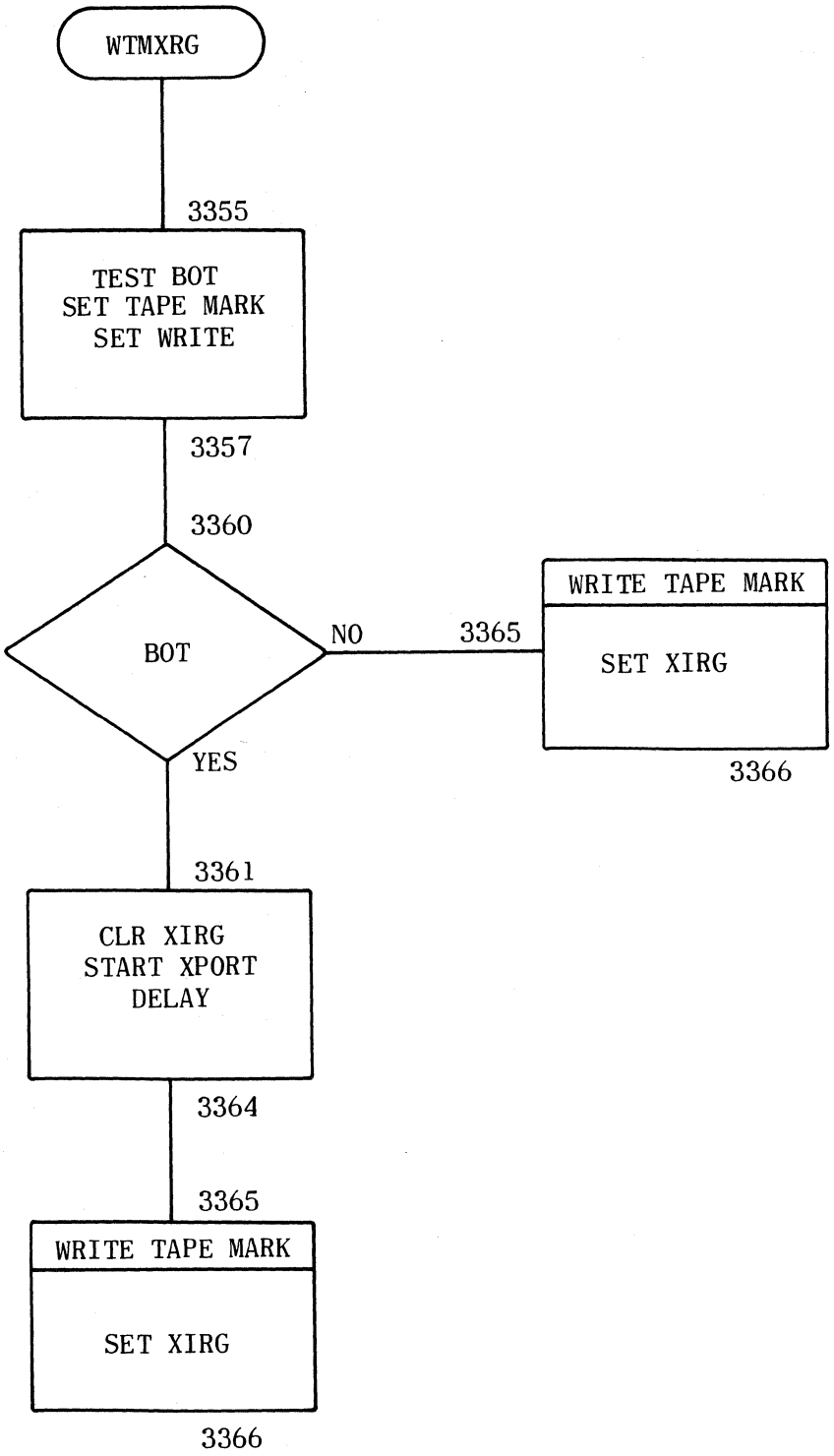


Figure 4-45. Write Tape Mark XIRG Sequence Flow Diagram

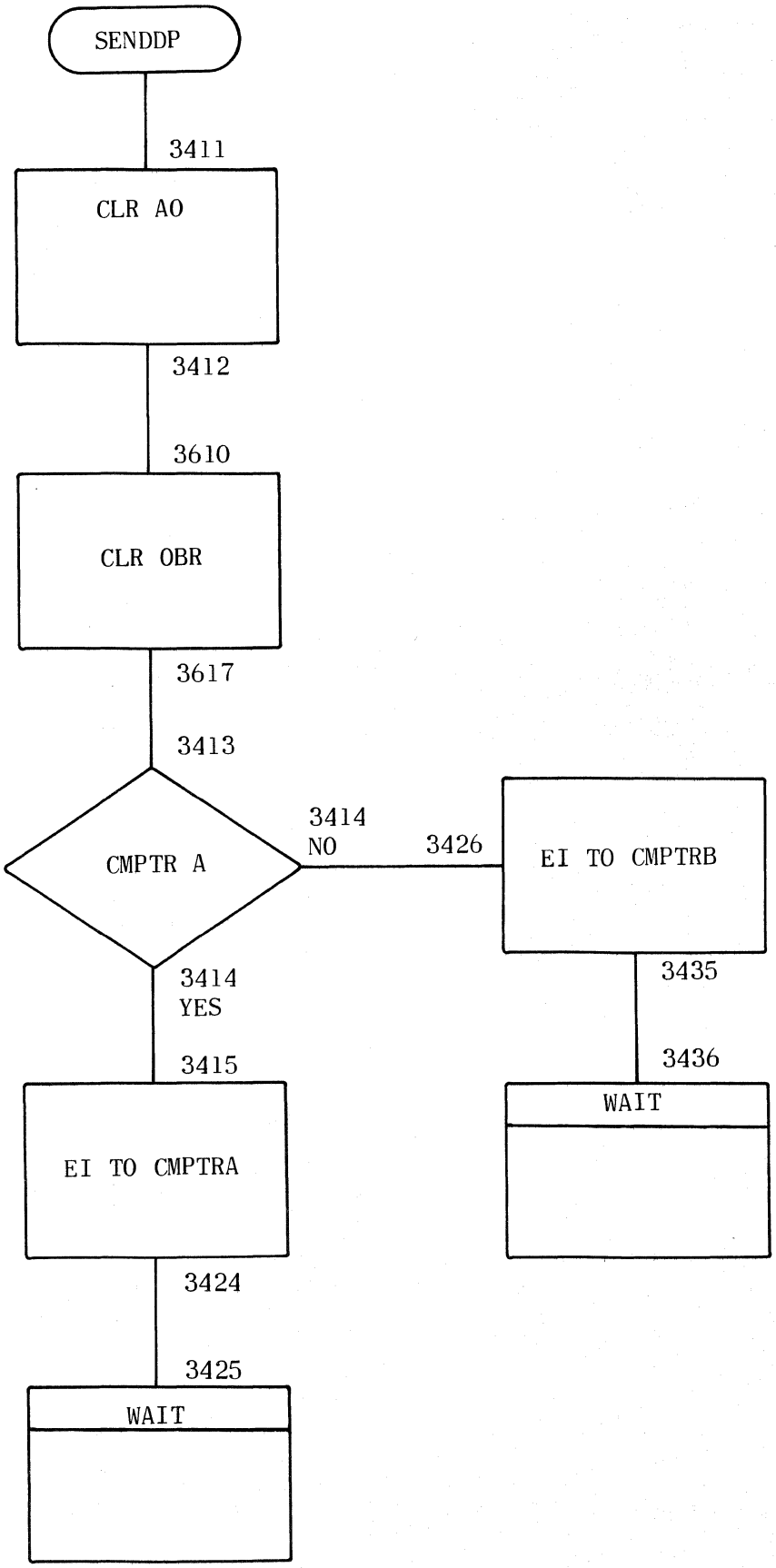


Figure 4-46. Send Duplex Control Sequence Flow Diagram

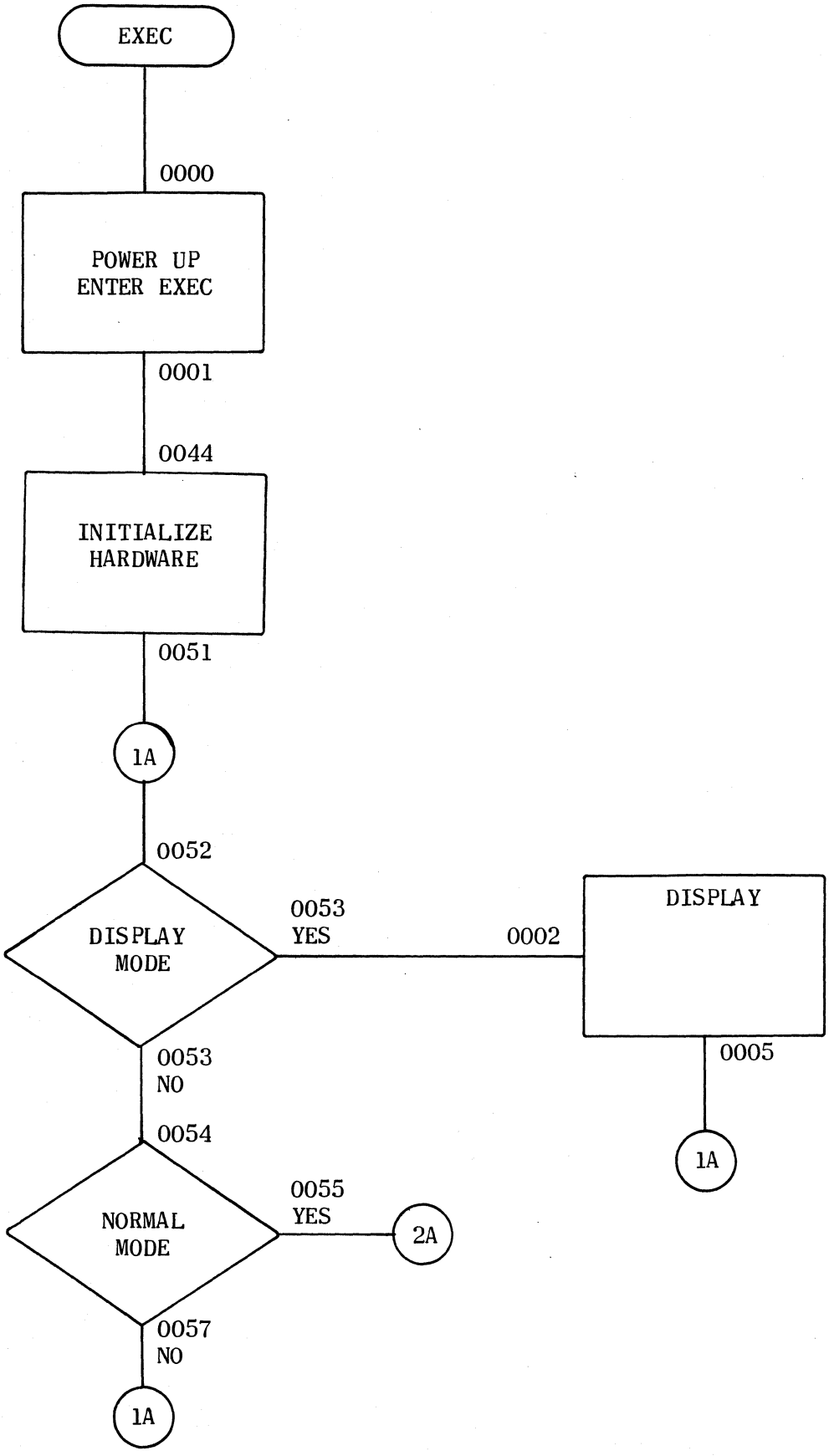


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 1 of 22)

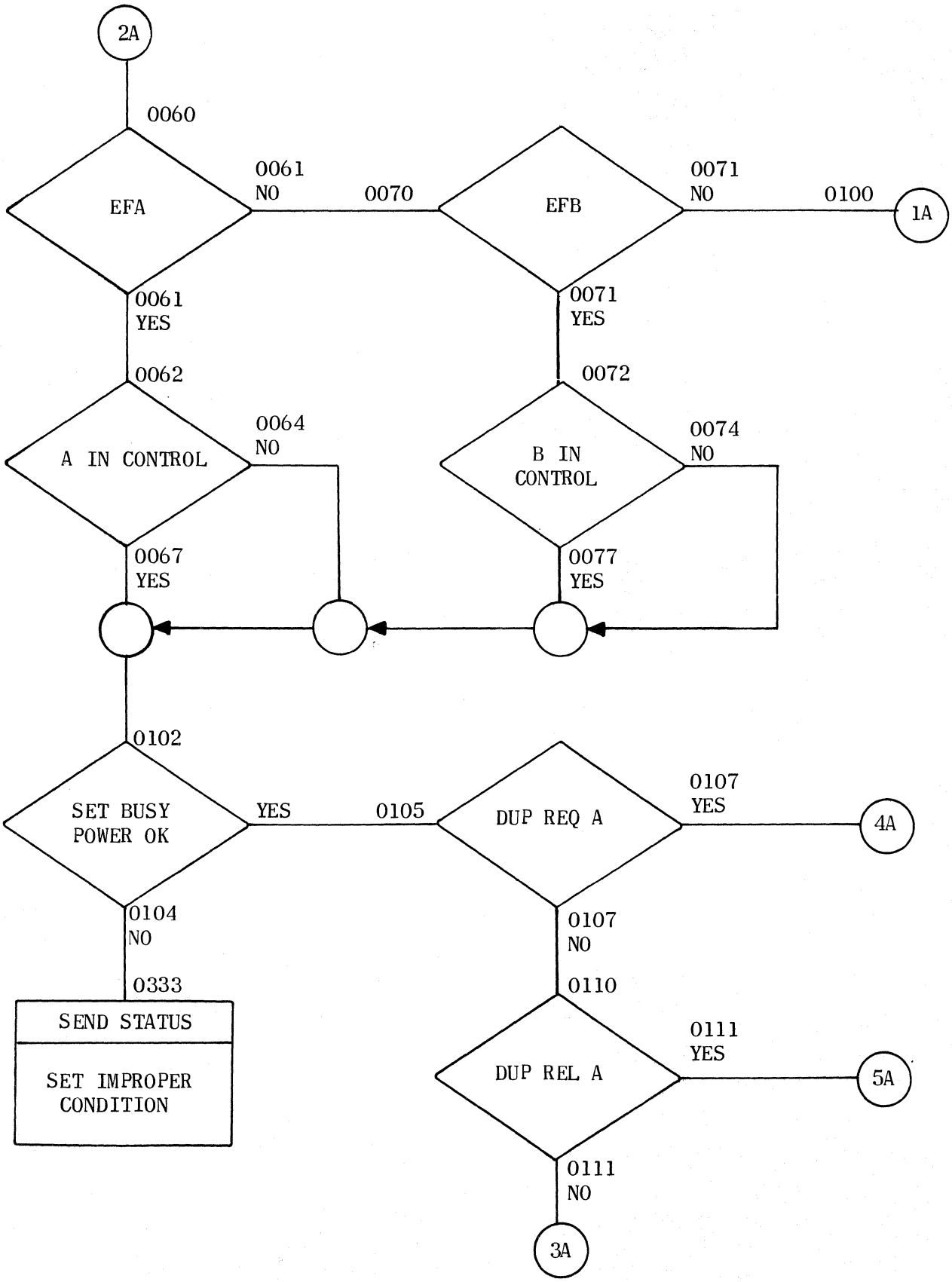


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 2 of 22)

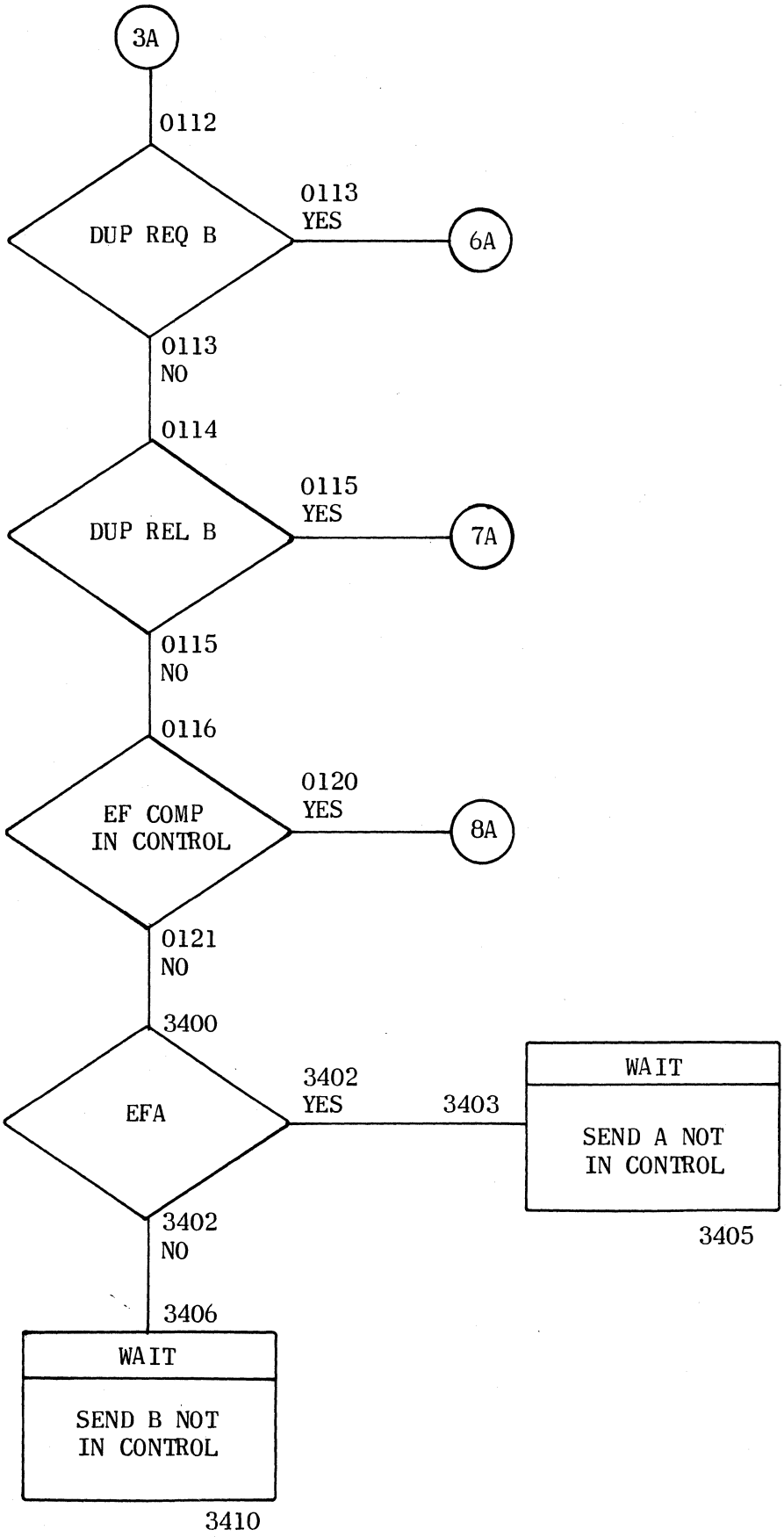


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 3 of 22)

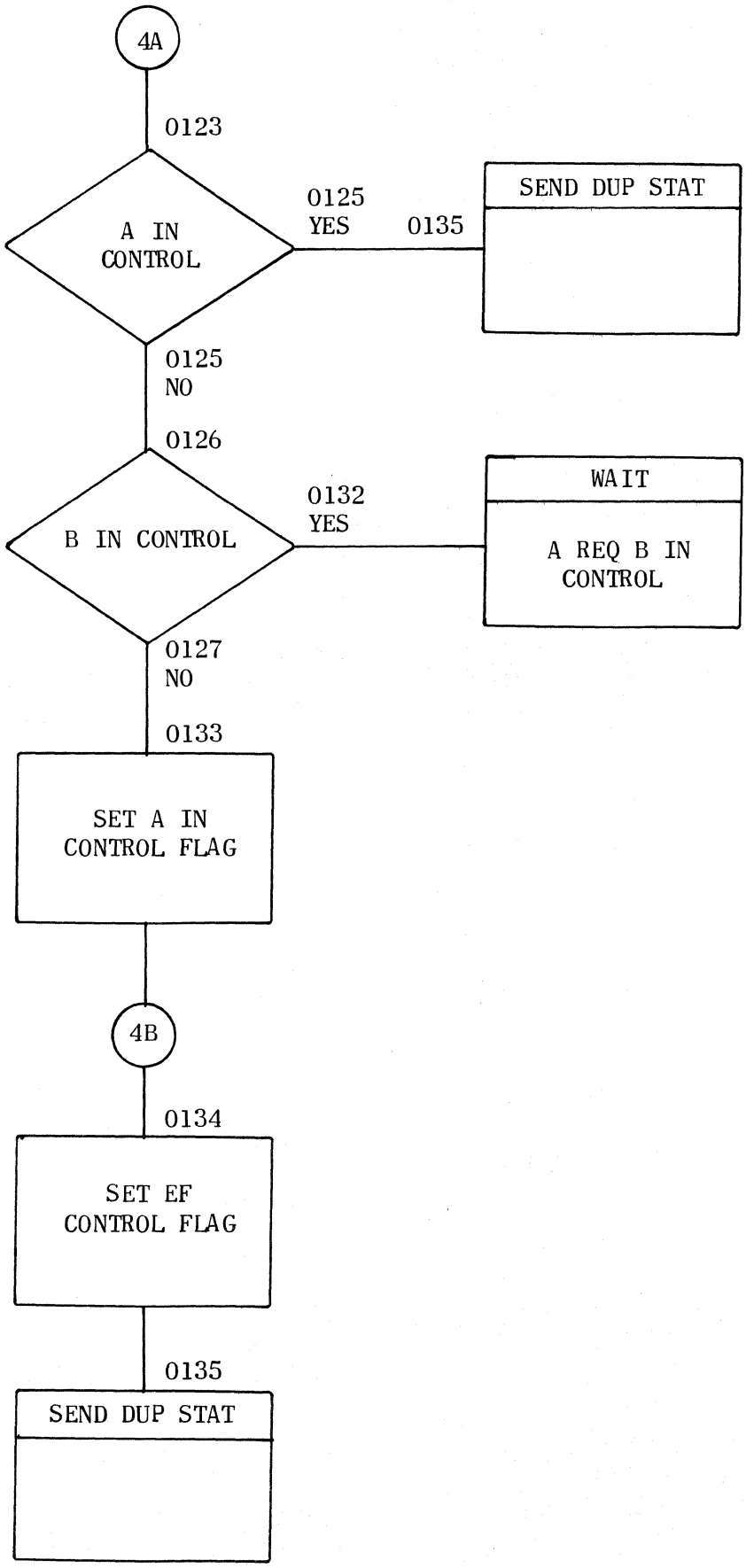


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 4 of 22)

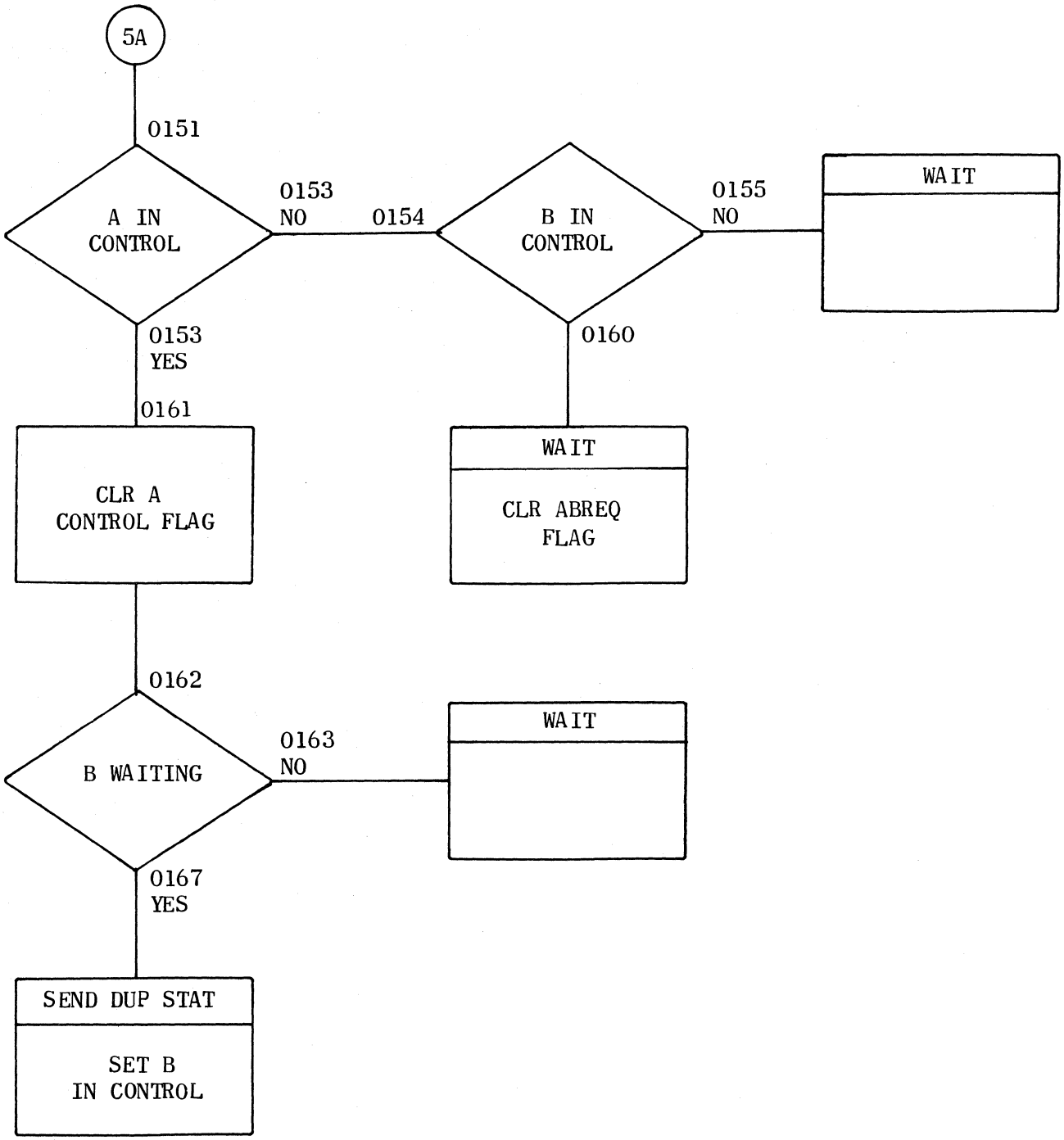


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 5 of 22)

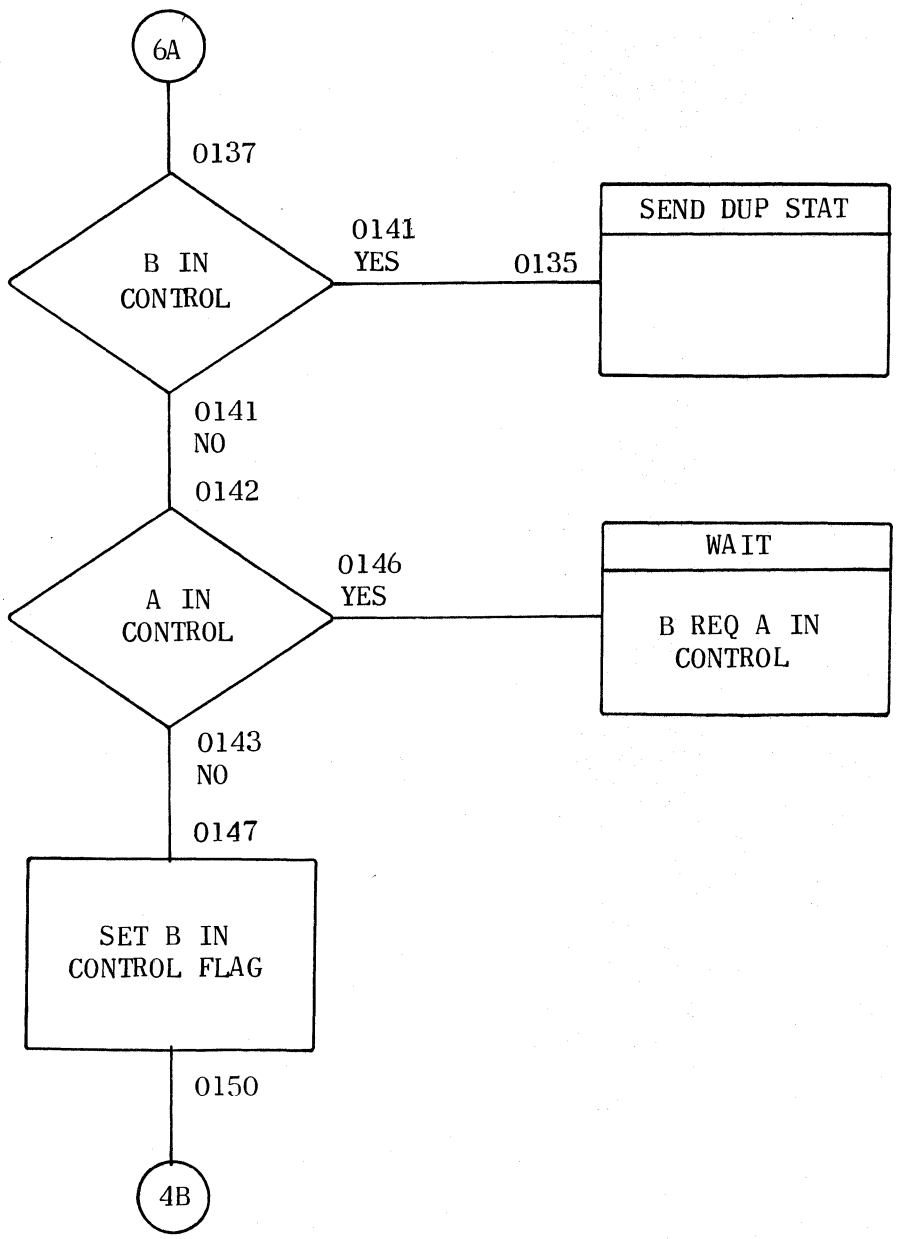


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 6 of 22)

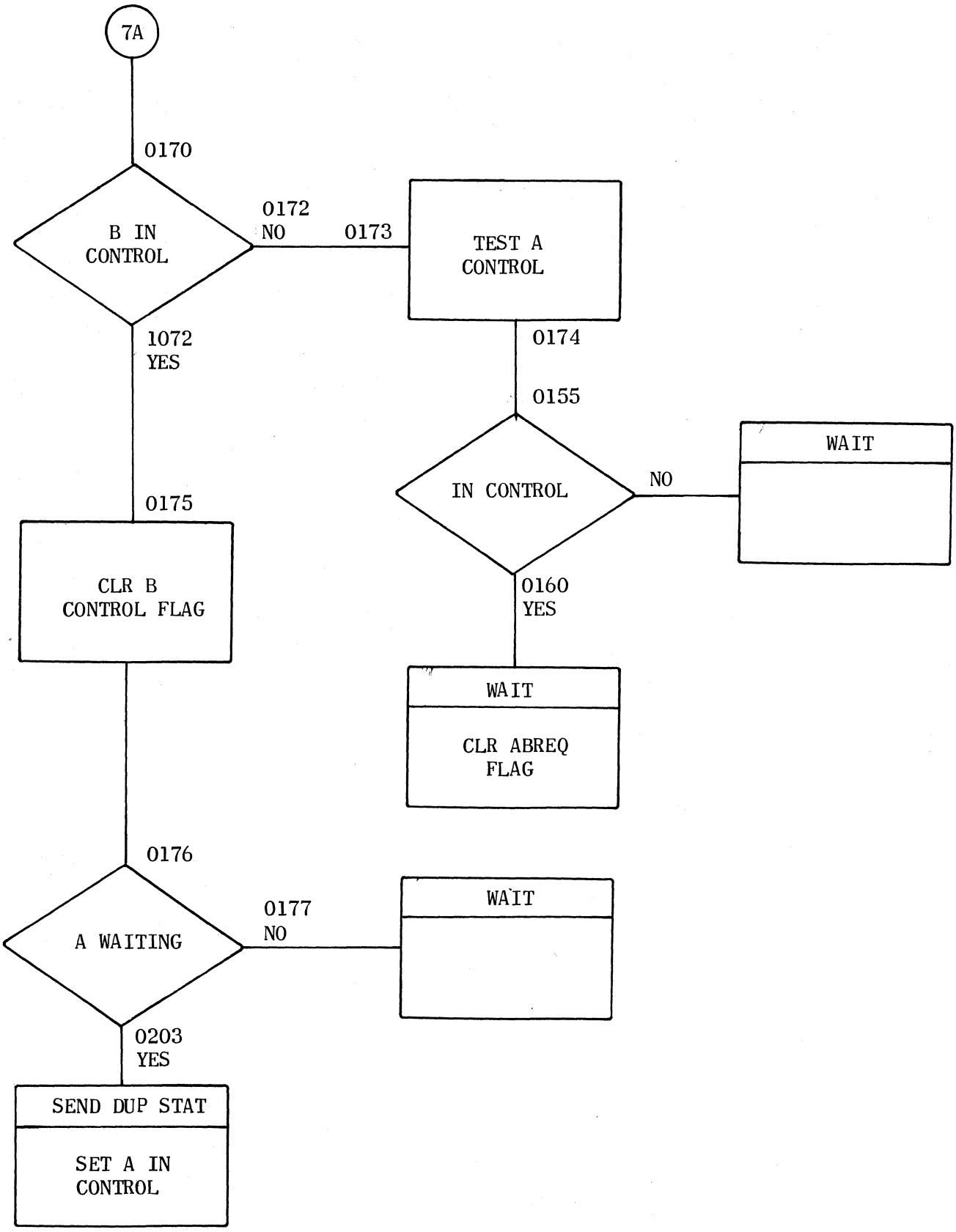


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 7 of 22)

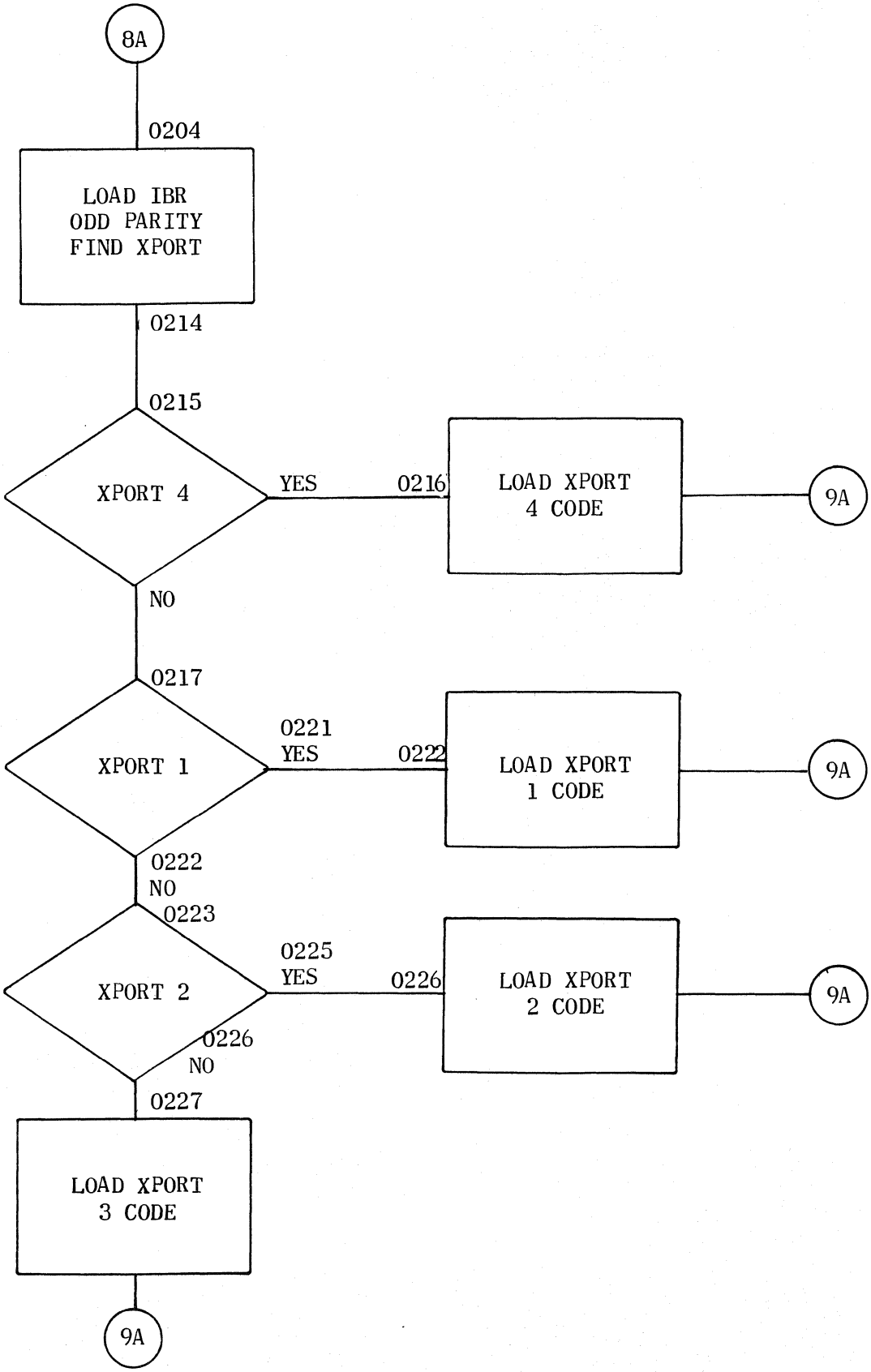


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 8 of 22)

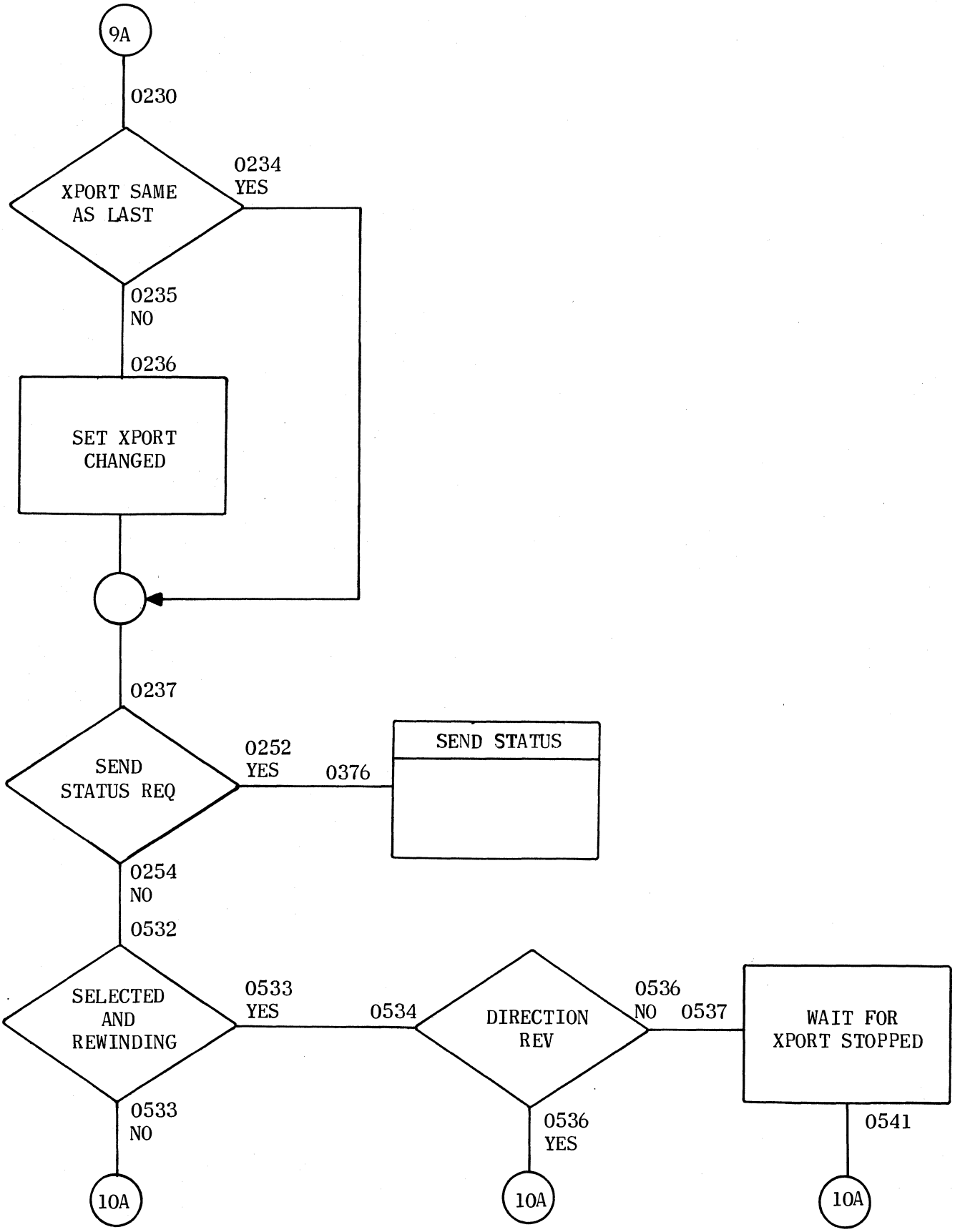


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 9 of 22)

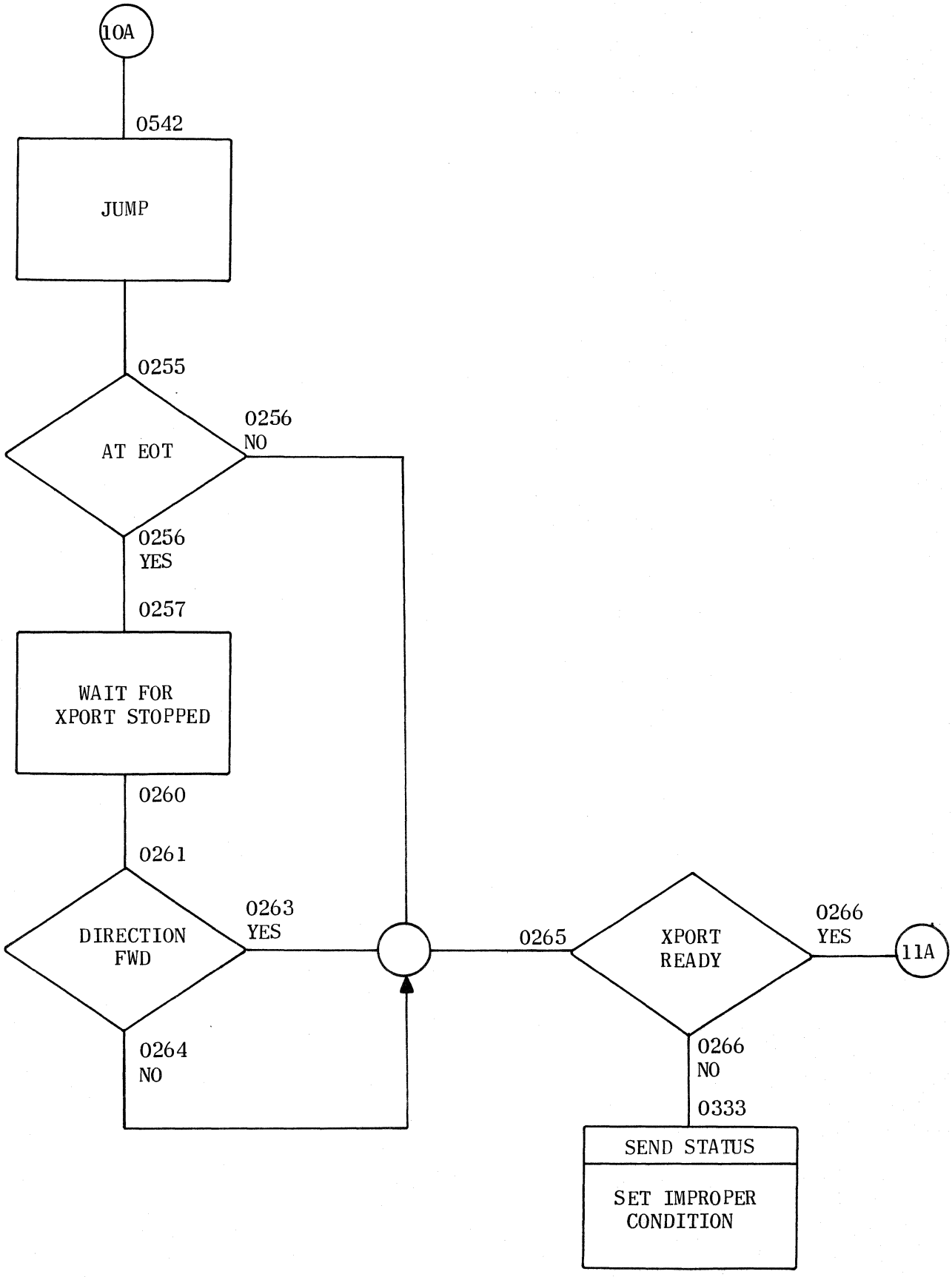


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 10 of 22)

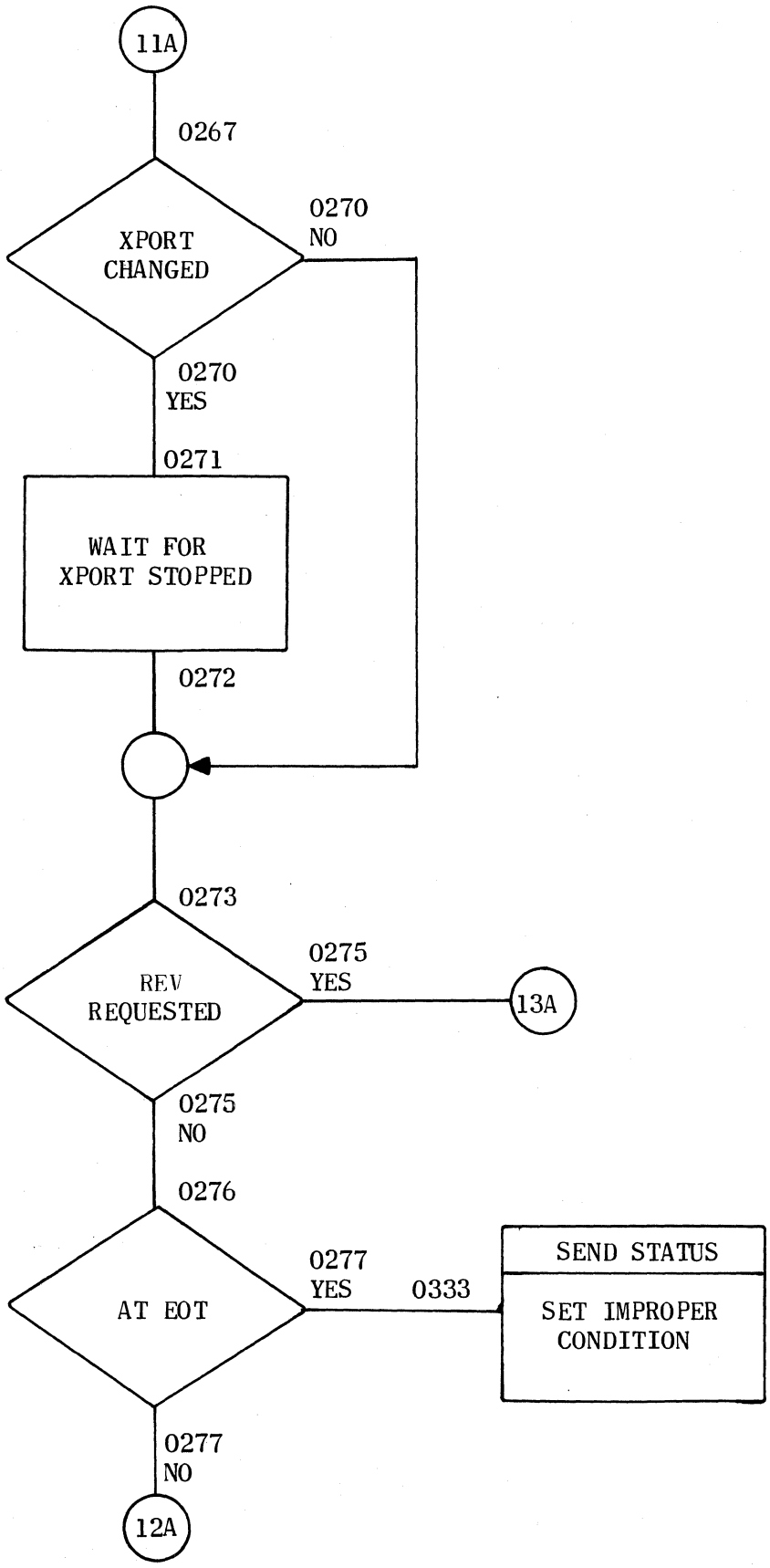


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 11 of 22)

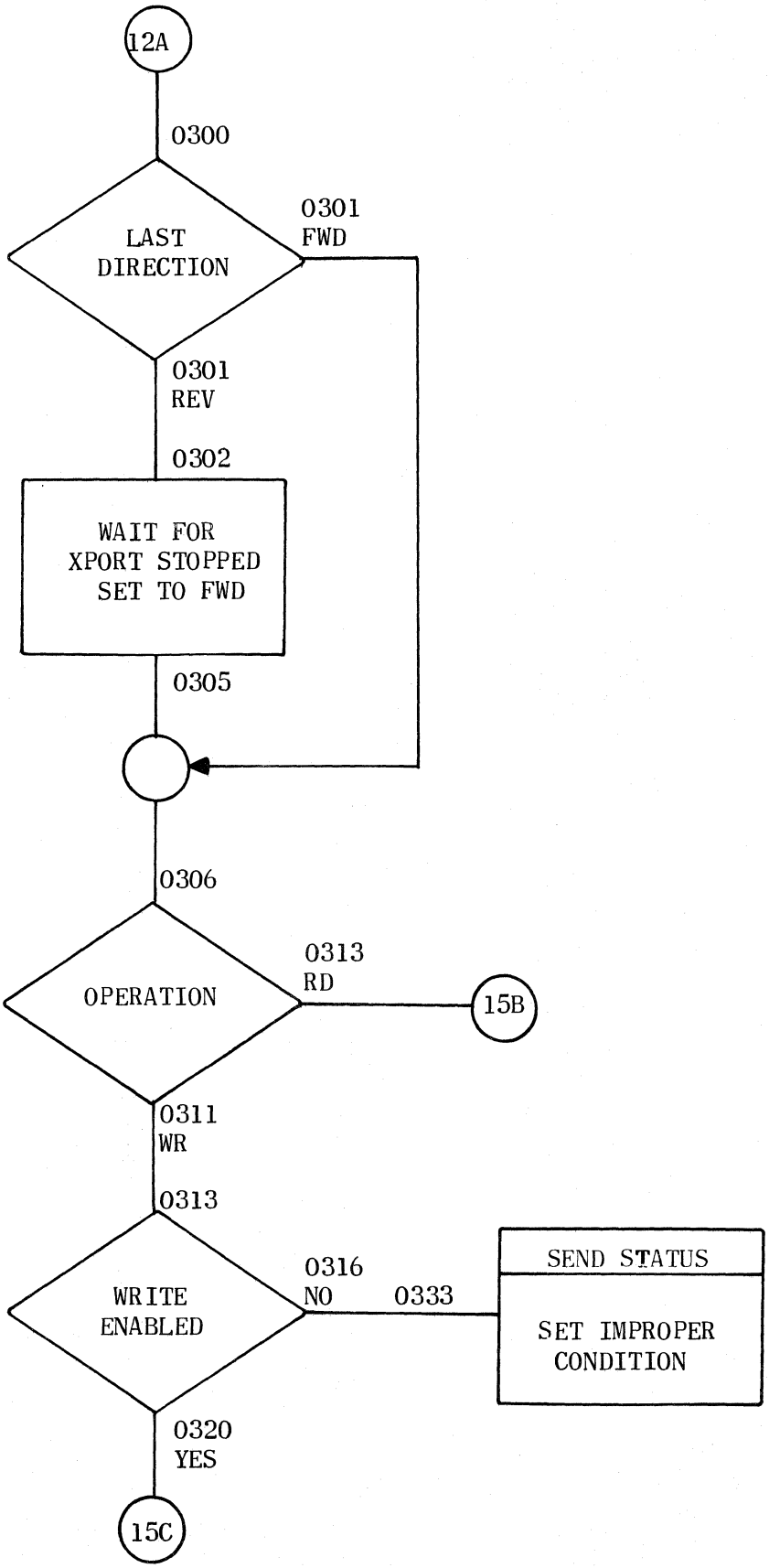


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 12 of 22)

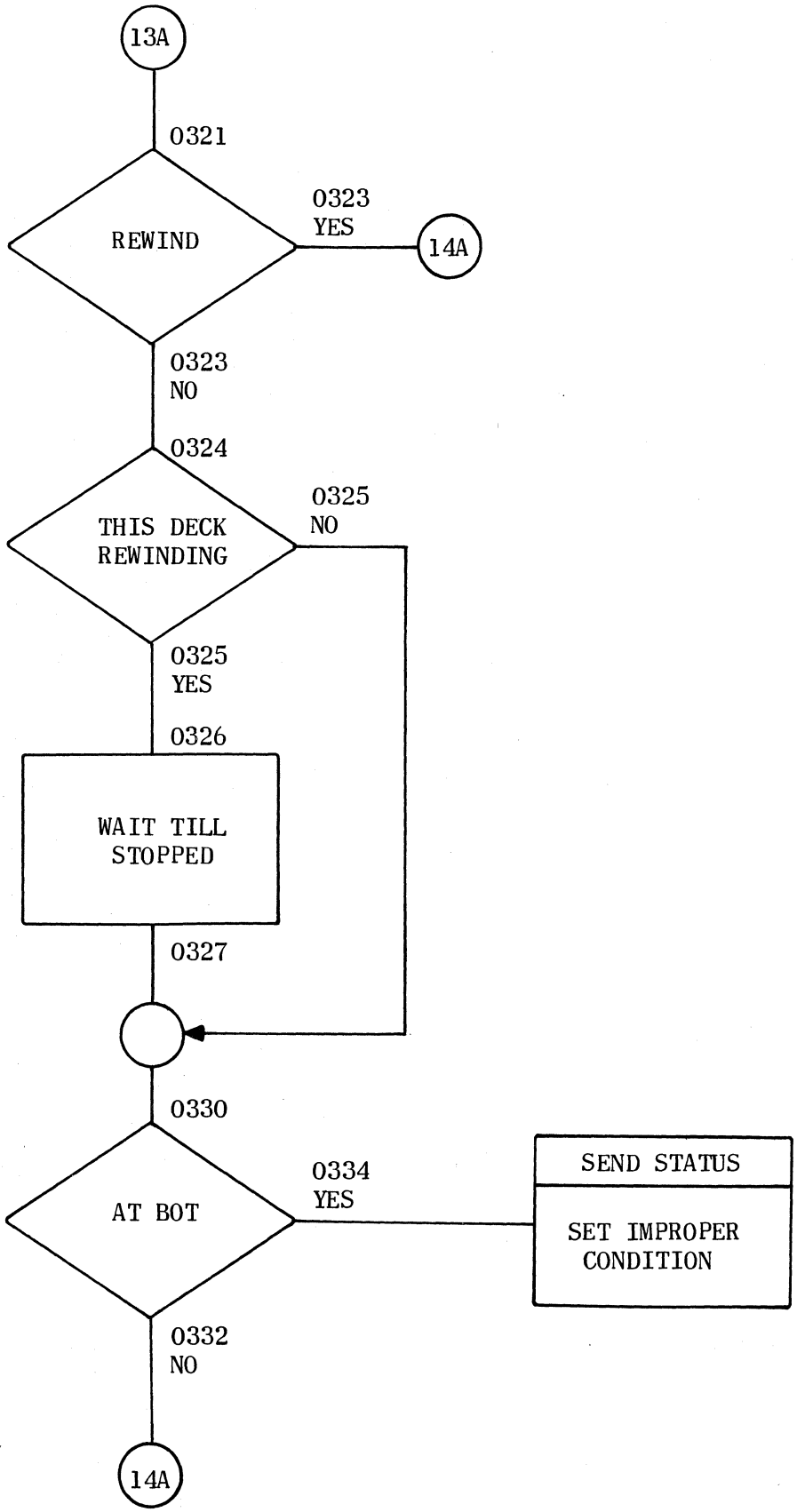


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 13 of 22)

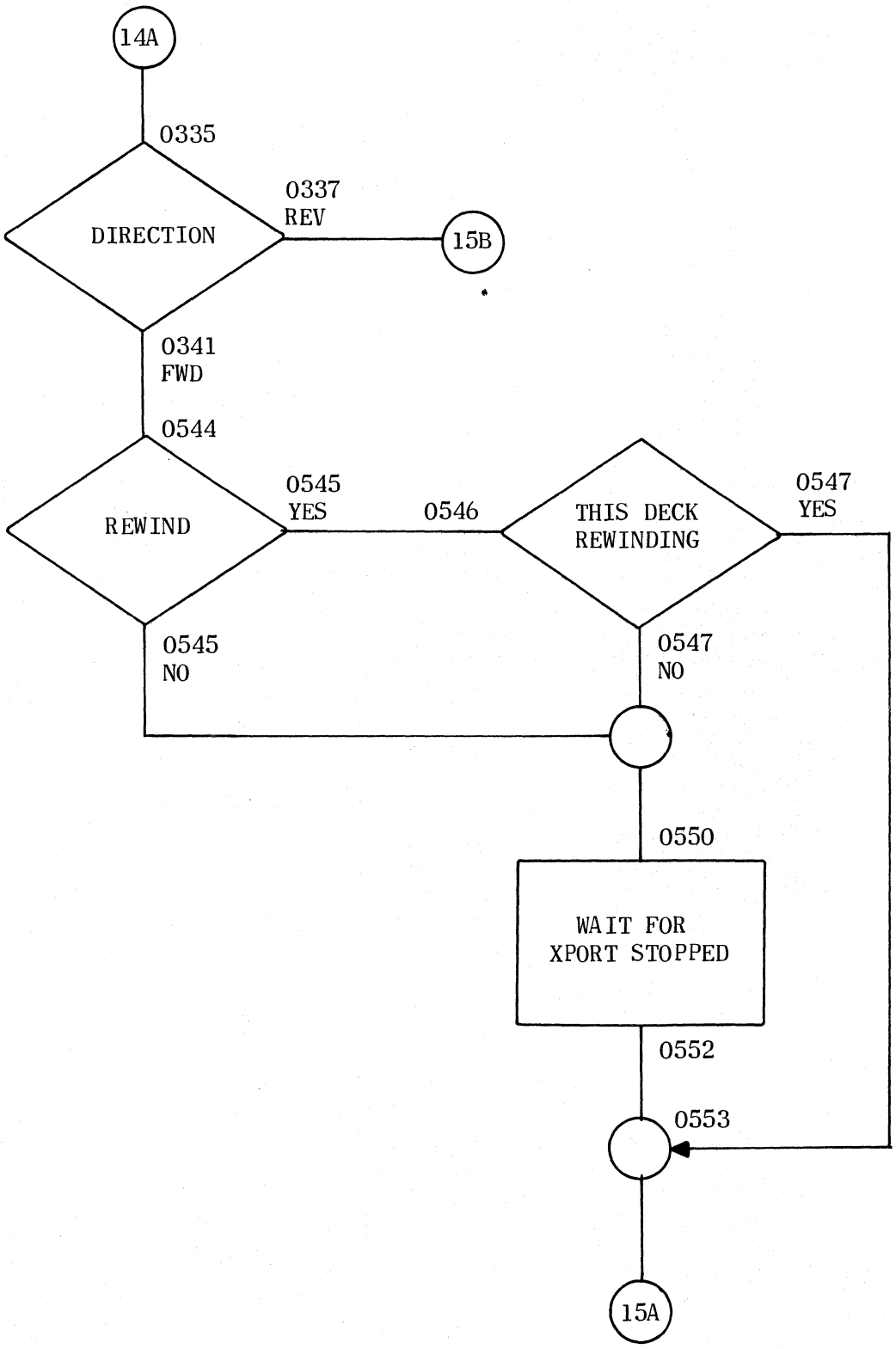


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 14 of 22)

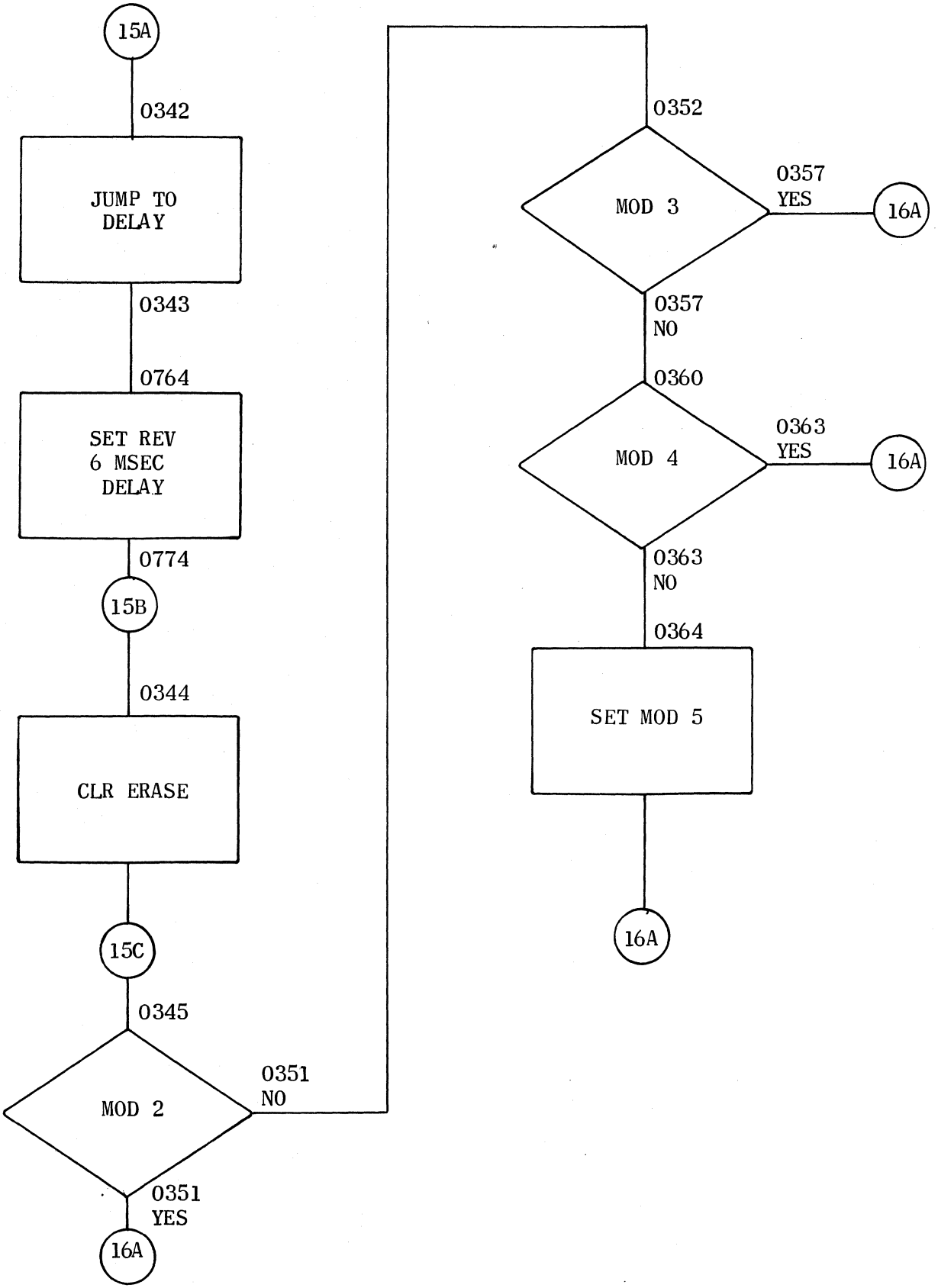


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 15 of 22)

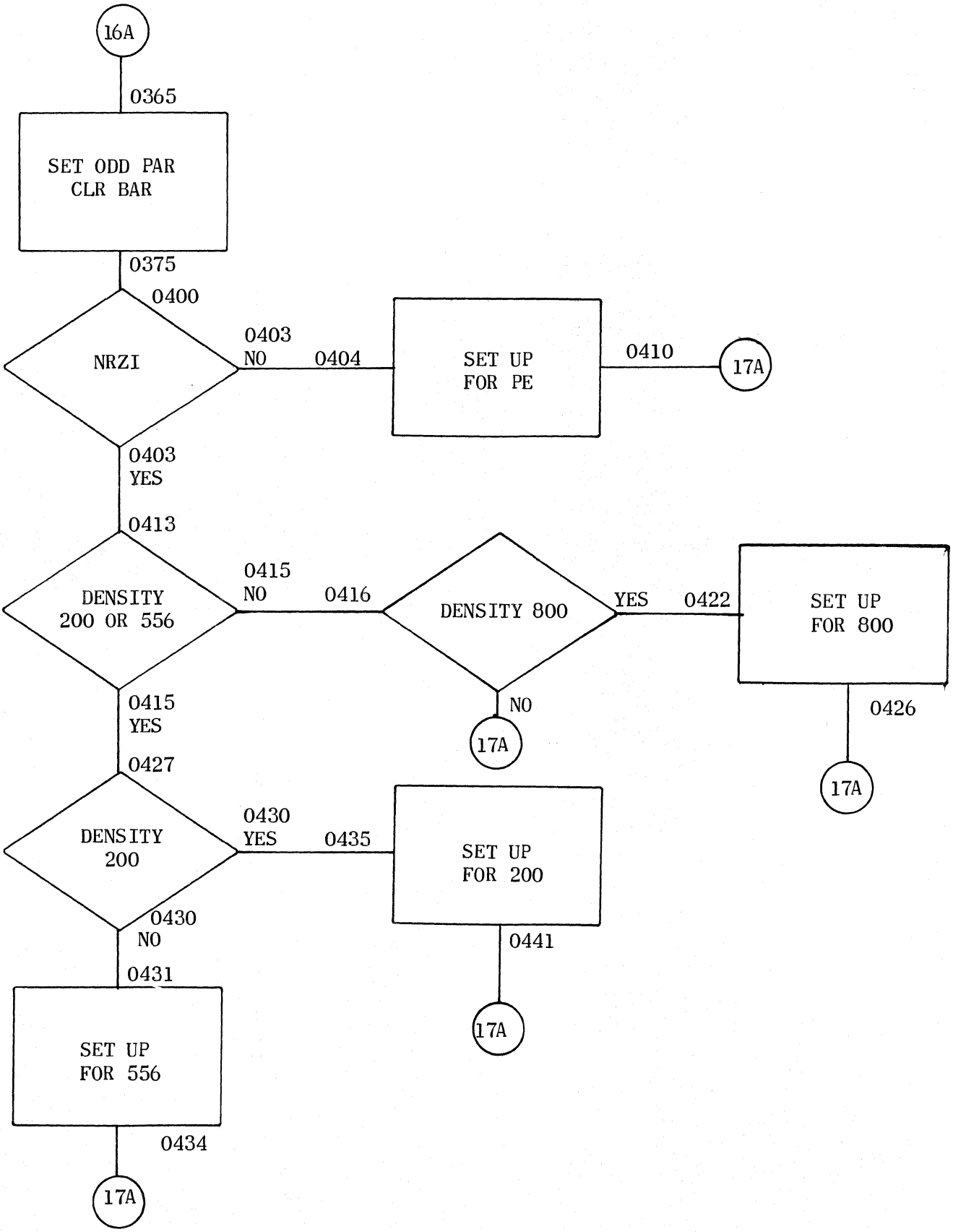


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 16 of 22)

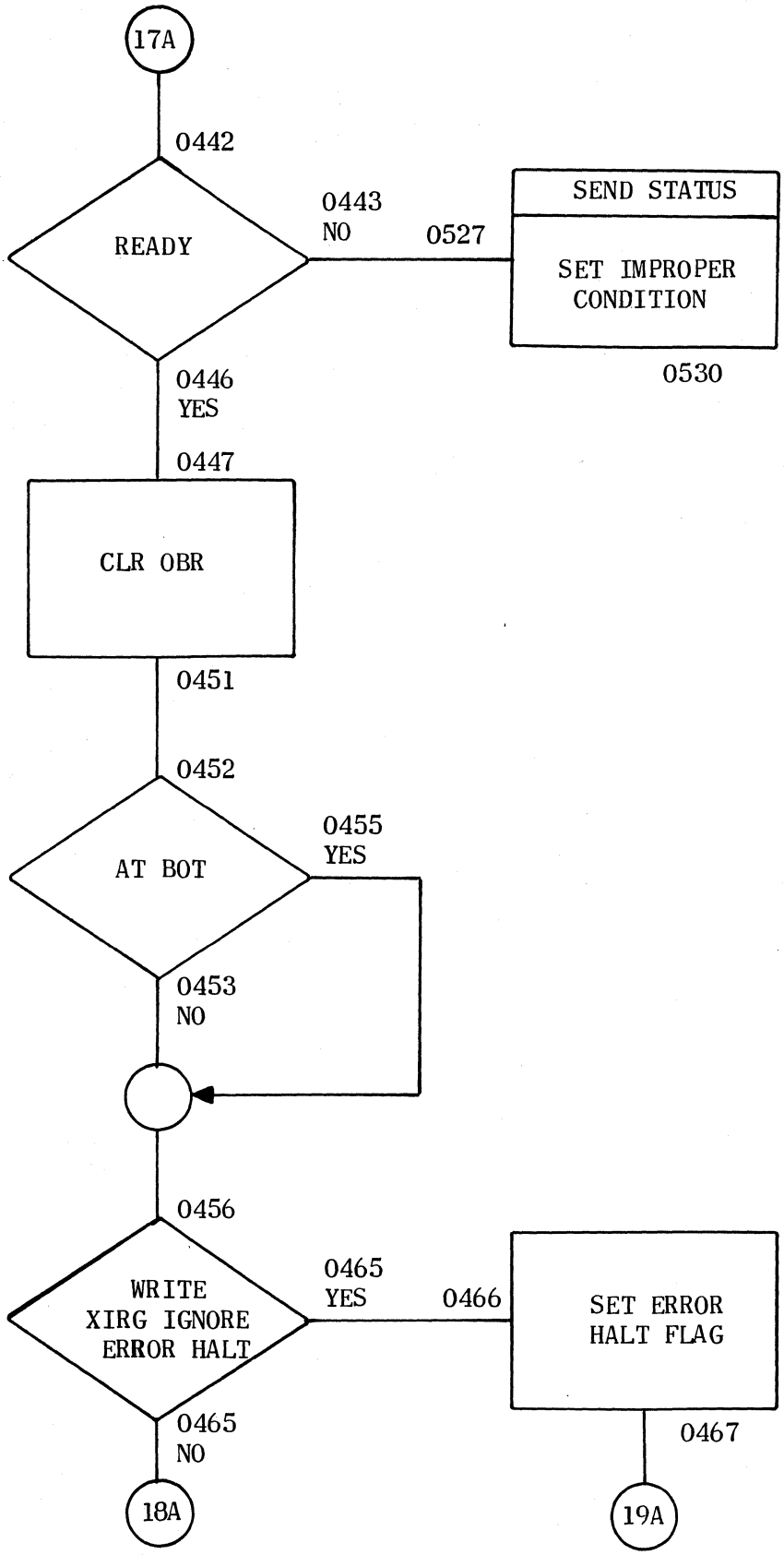


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 17 of 22)

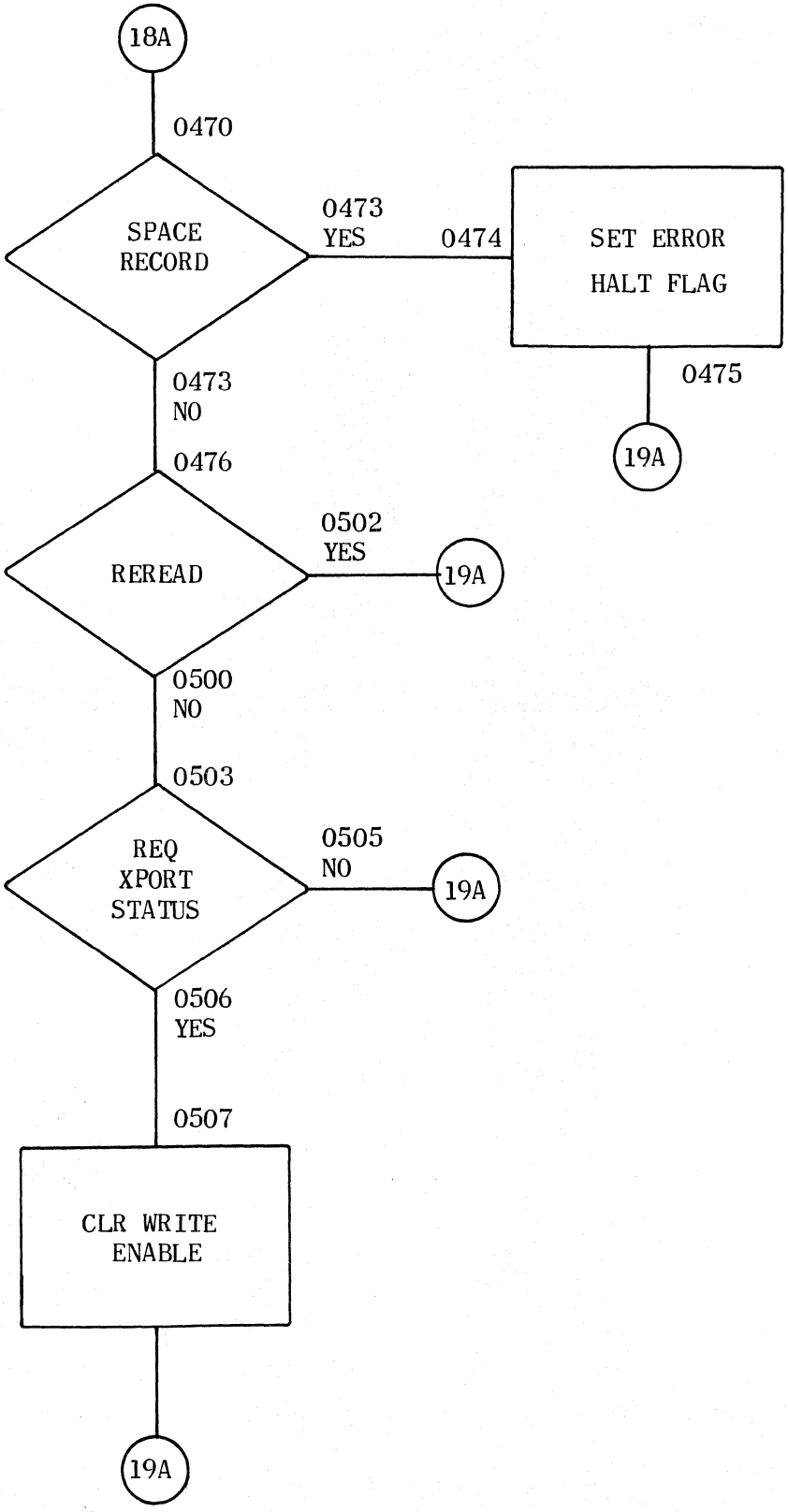


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 18 of 22)

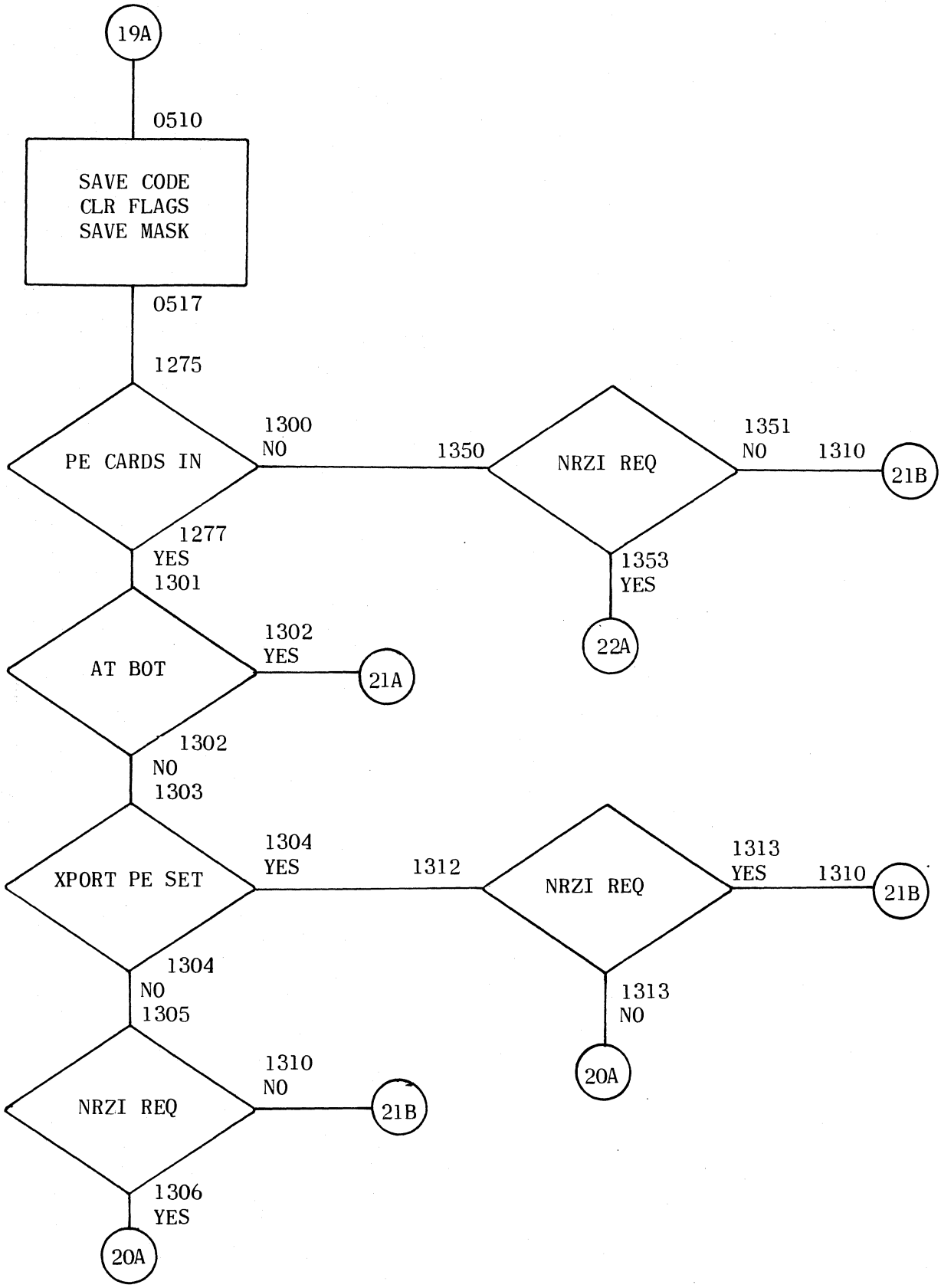


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 19 of 22)

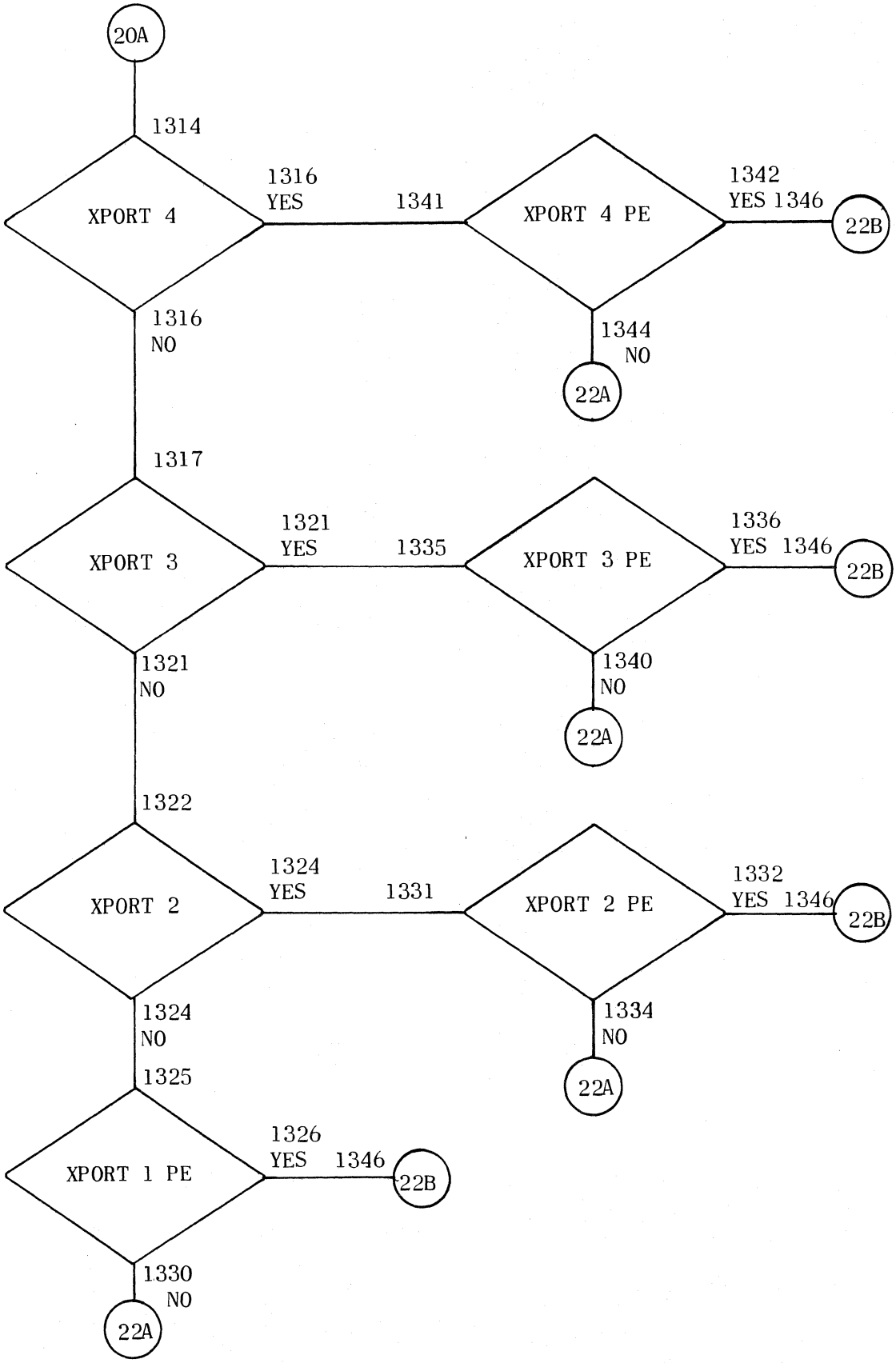


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 20 of 22)

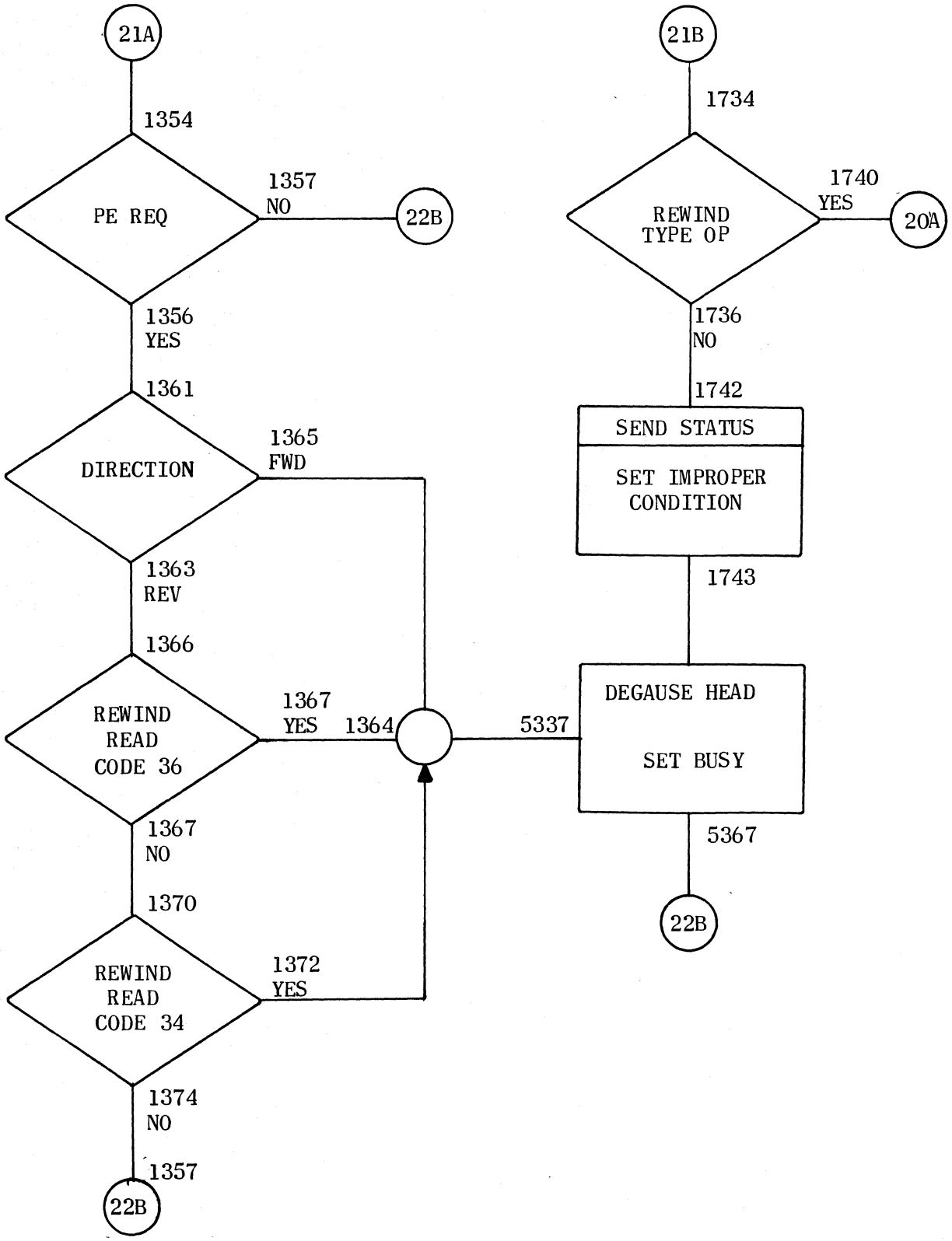


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 21 of 22)

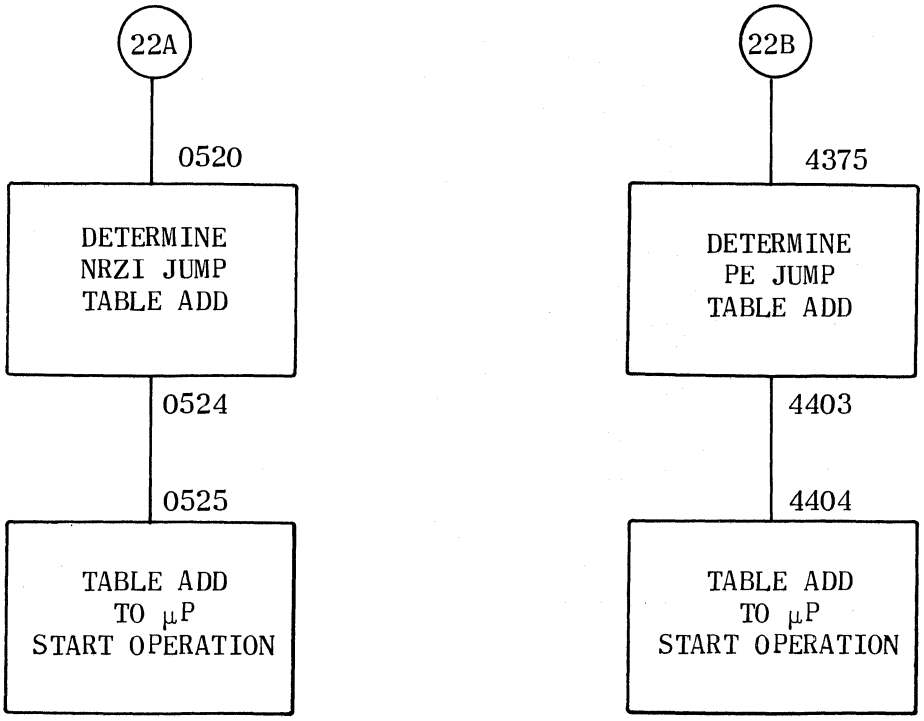


Figure 4-47. Nine Track Executive Sequence Flow Diagram (Sheet 22 of 22)

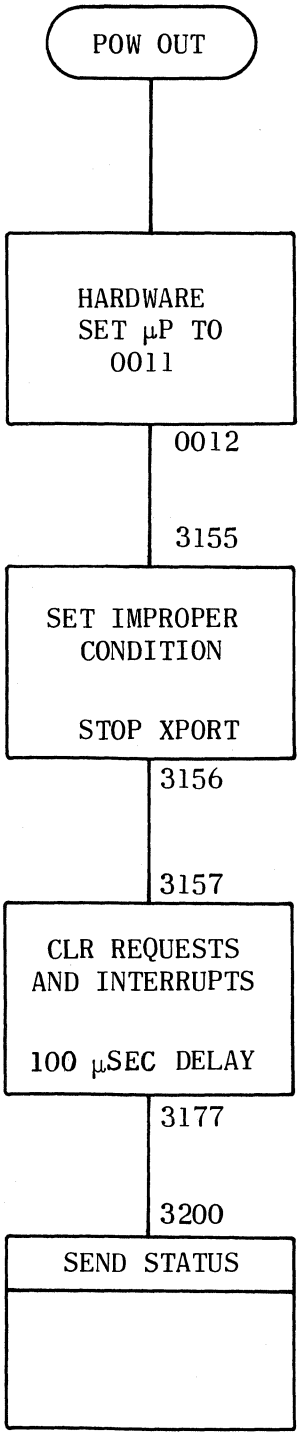


Figure 4-48. Power Out of Tolerance Interrupt Sequence Flow Diagram

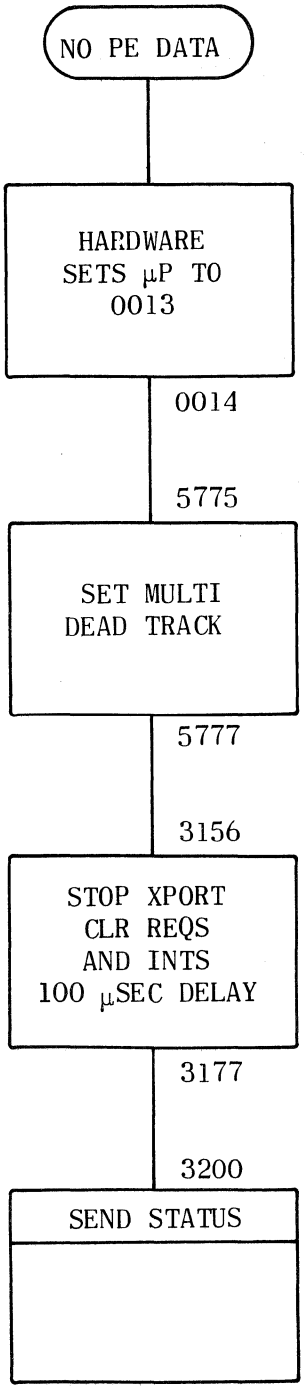


Figure 4-49. No PE Data Interrupt Sequence Flow Diagram

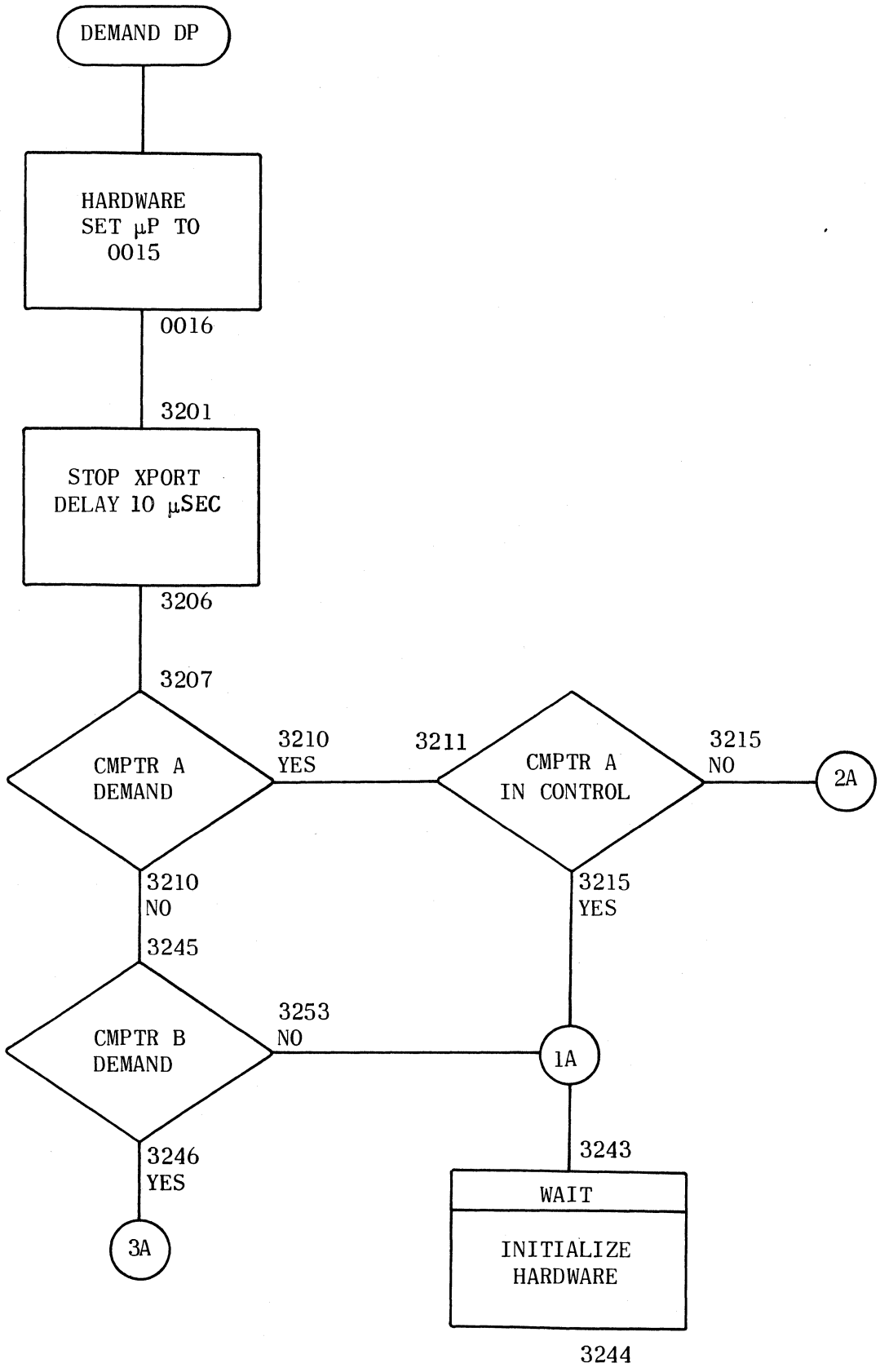


Figure 4-50. Demand Duplex Sequence Flow Diagram (Sheet 1 of 3)

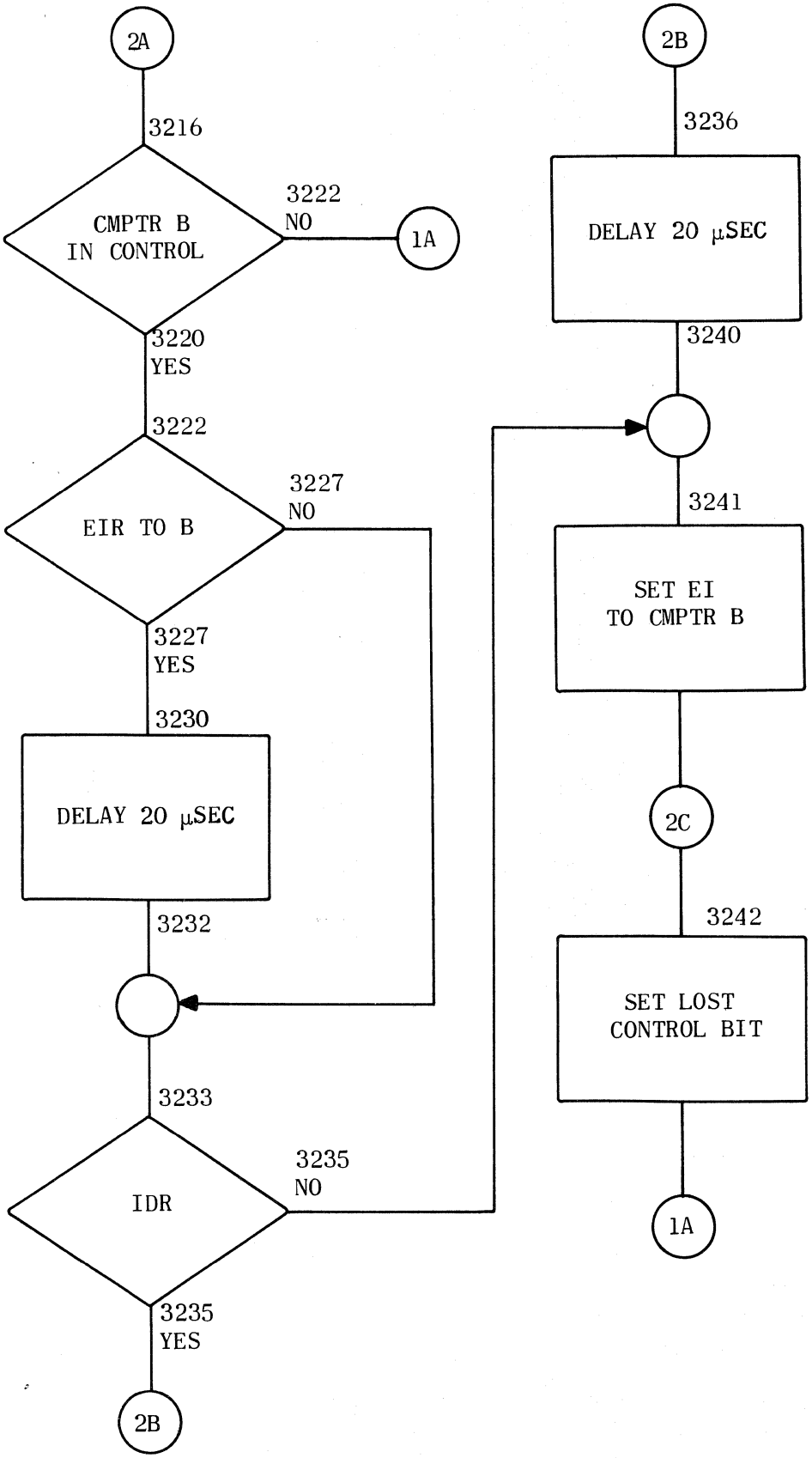


Figure 4-50. Demand Duplex Sequence Flow Diagram (Sheet 2 of 3)

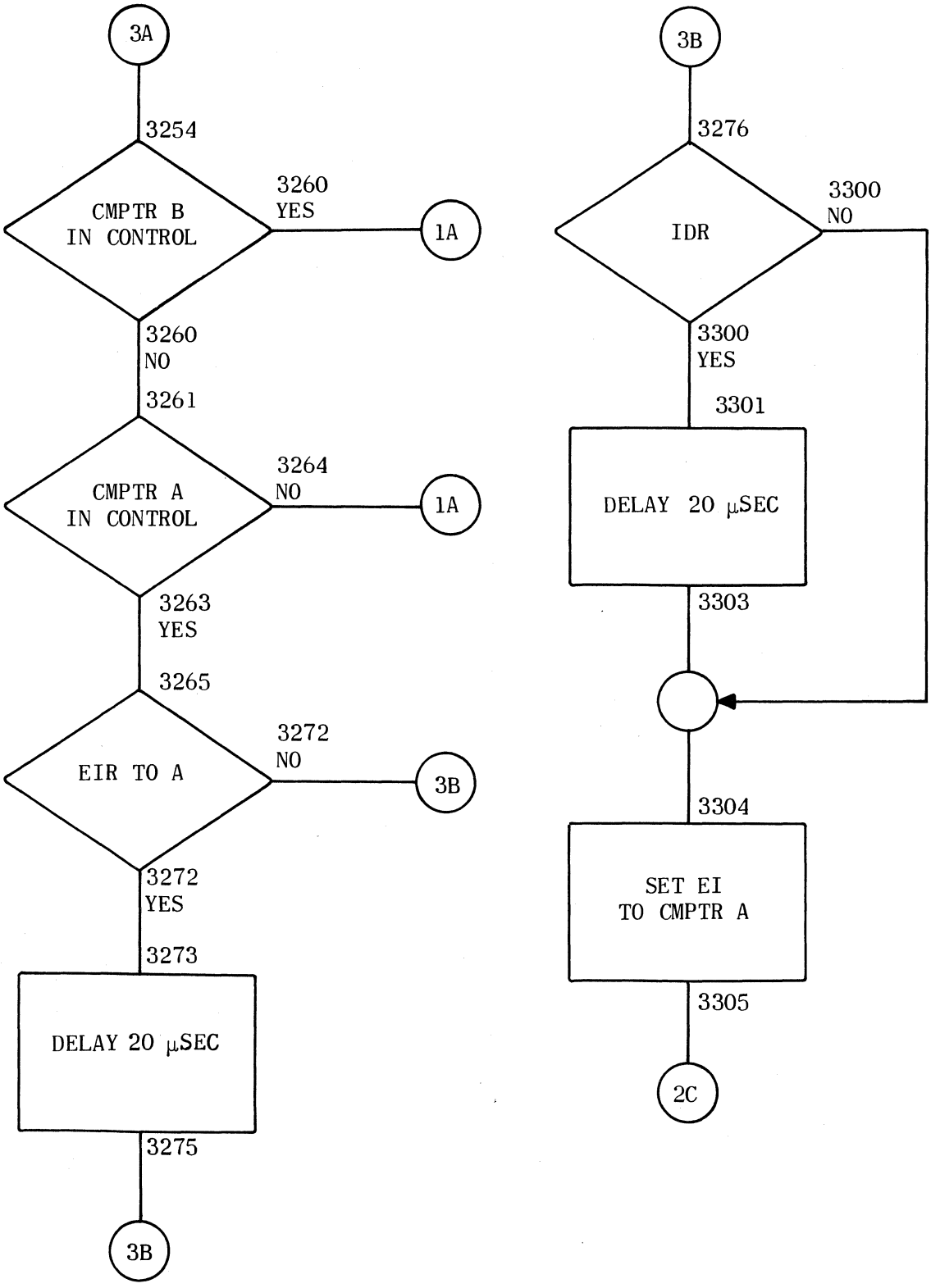


Figure 4-50. Demand Duplex Sequence Flow Diagram (Sheet 3 of 3)

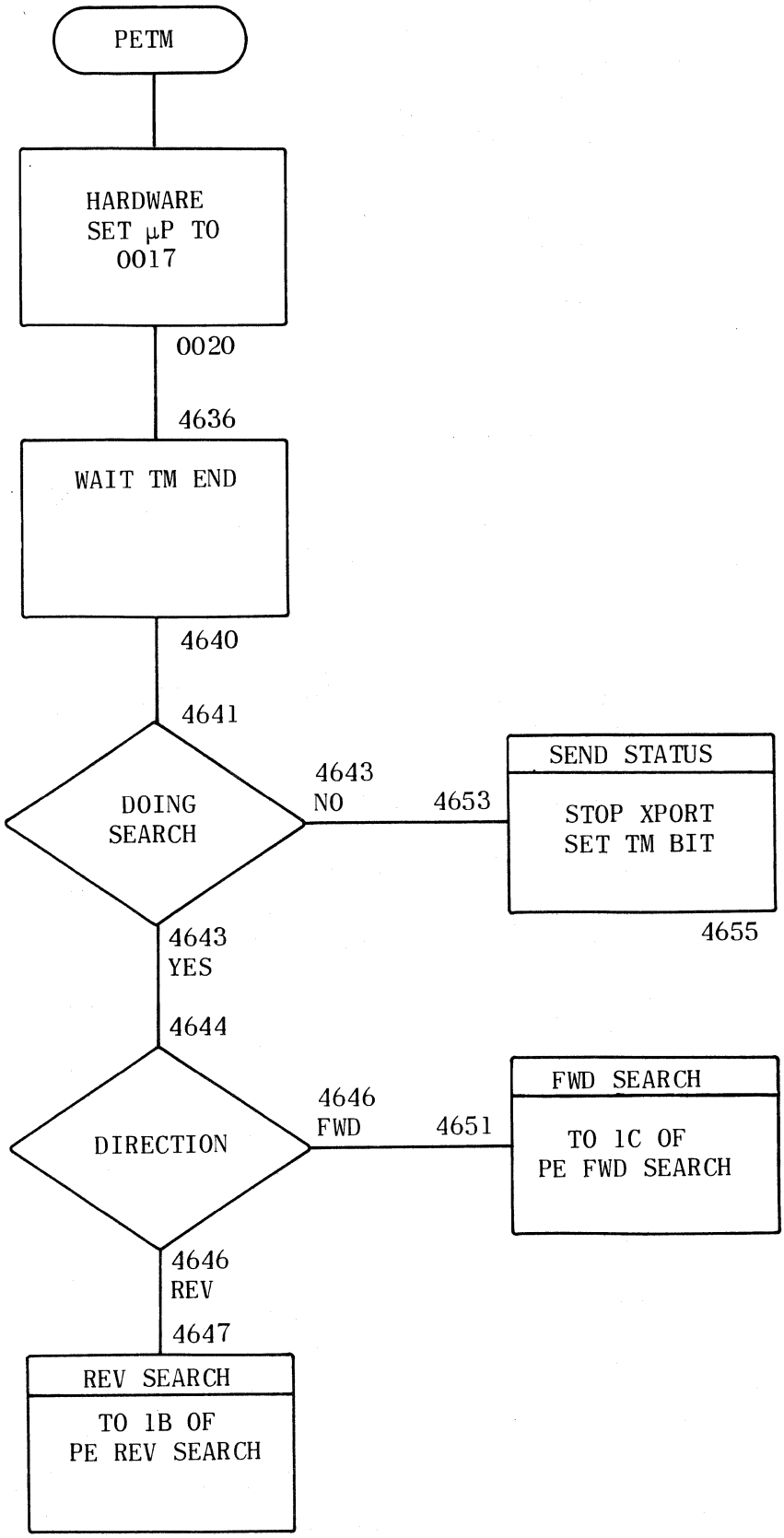


Figure 4-51. PE Tape Mark Interrupt Sequence Flow Diagram

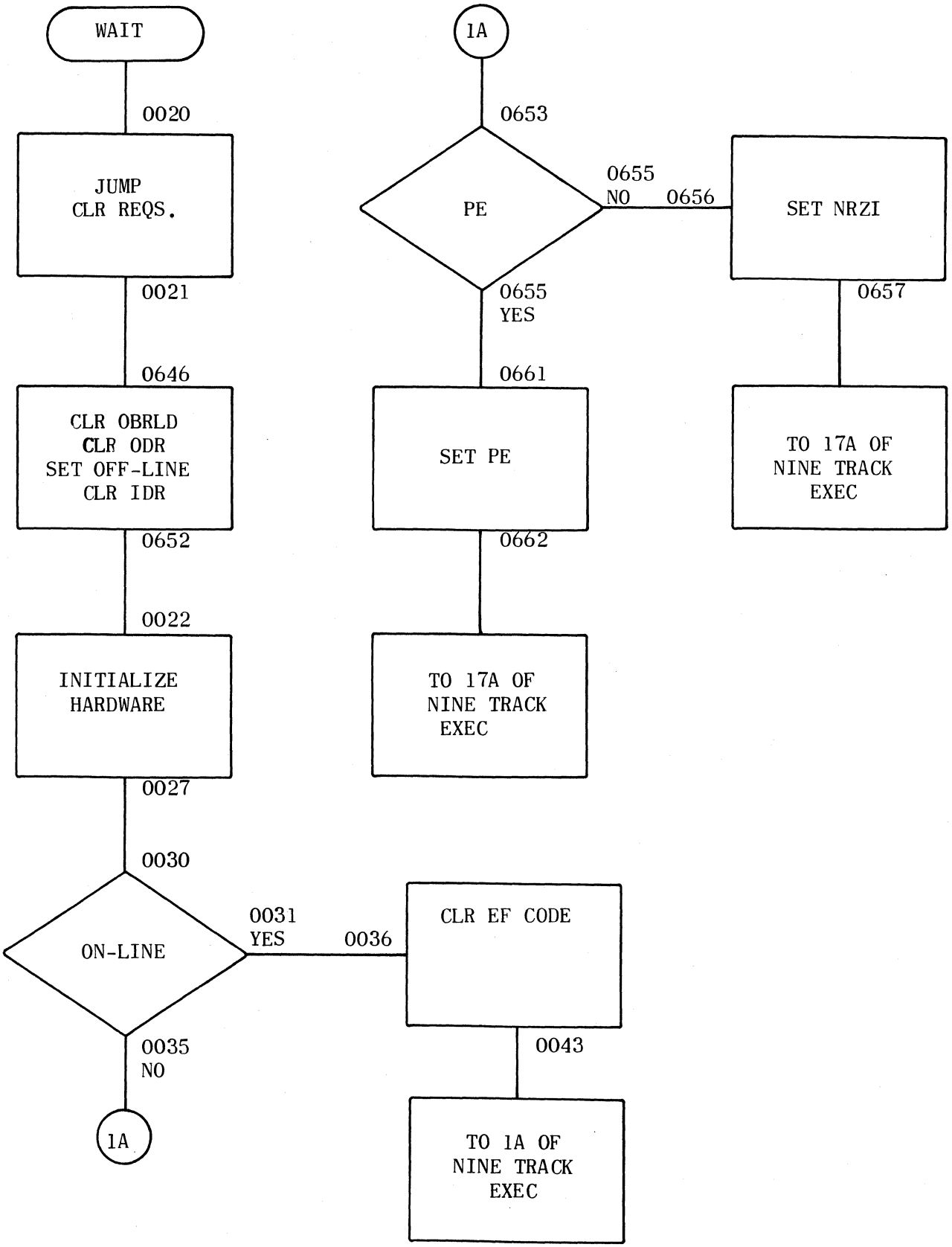


Figure 4-52. Wait Sequence Flow Diagram

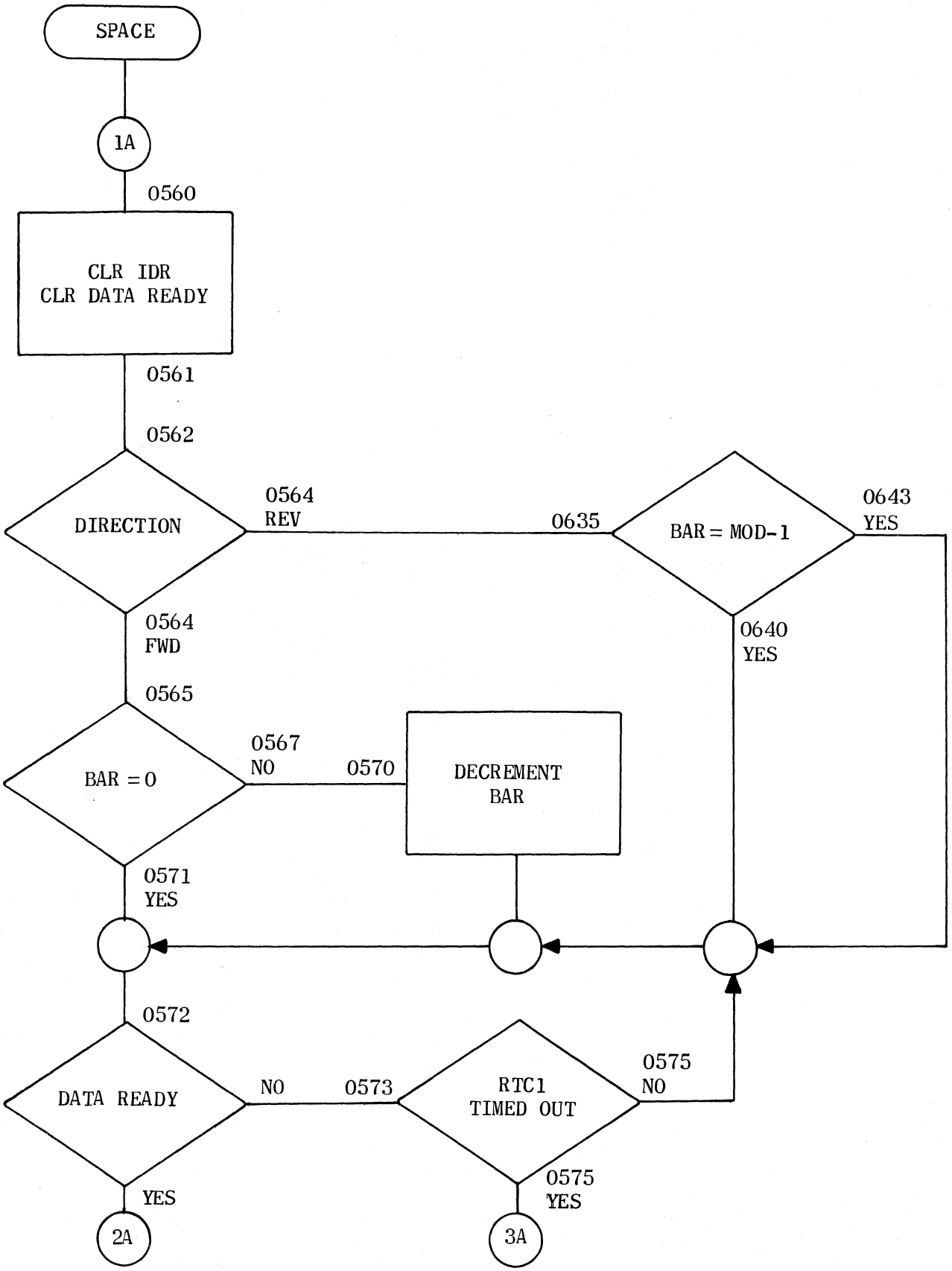


Figure 4-53. Space to IRG Sequence Flow Diagram (Sheet 1 of 3)

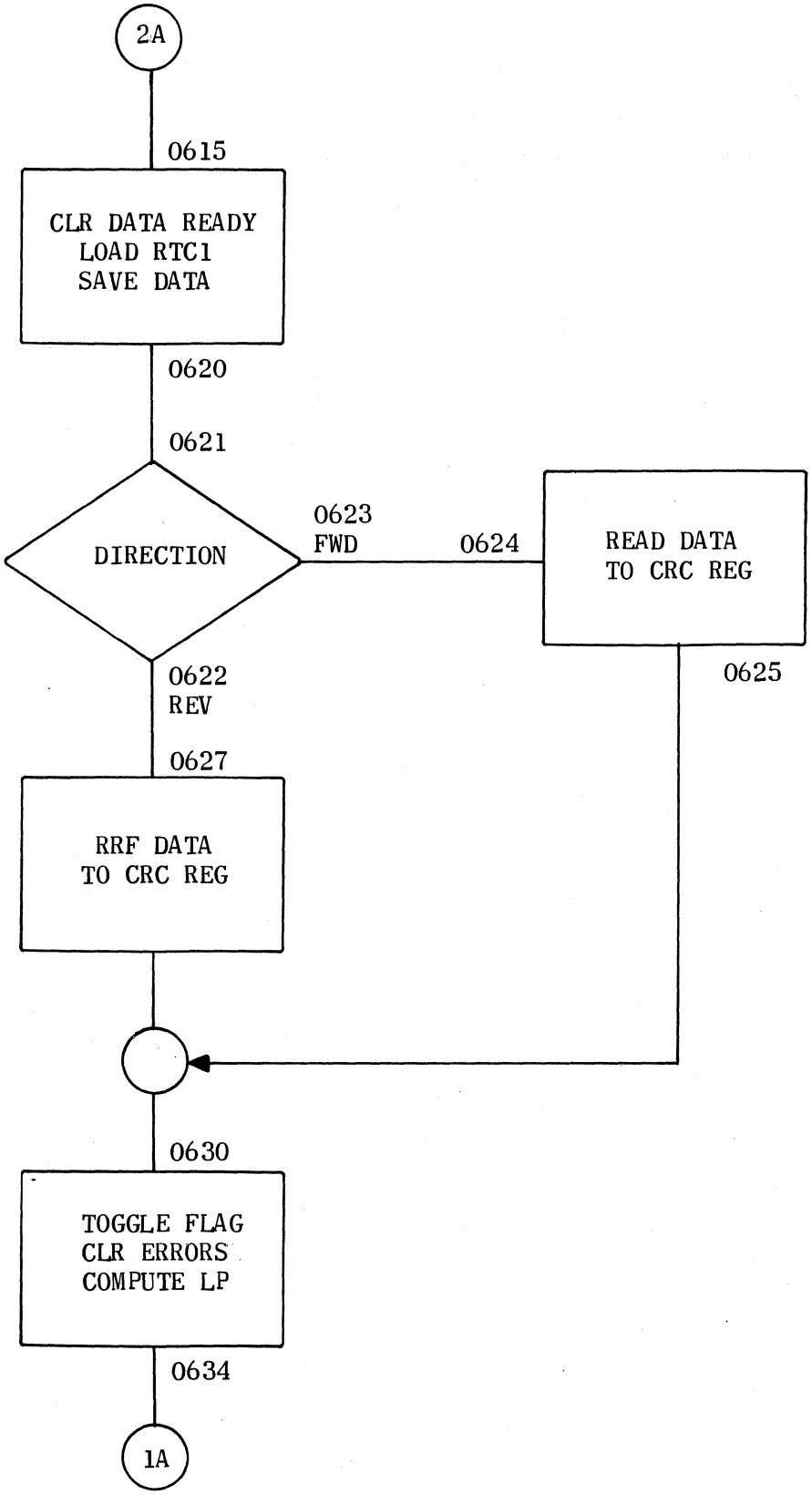


Figure 4-53. Space to IRG Sequence Flow Diagram (Sheet 2 of 3)

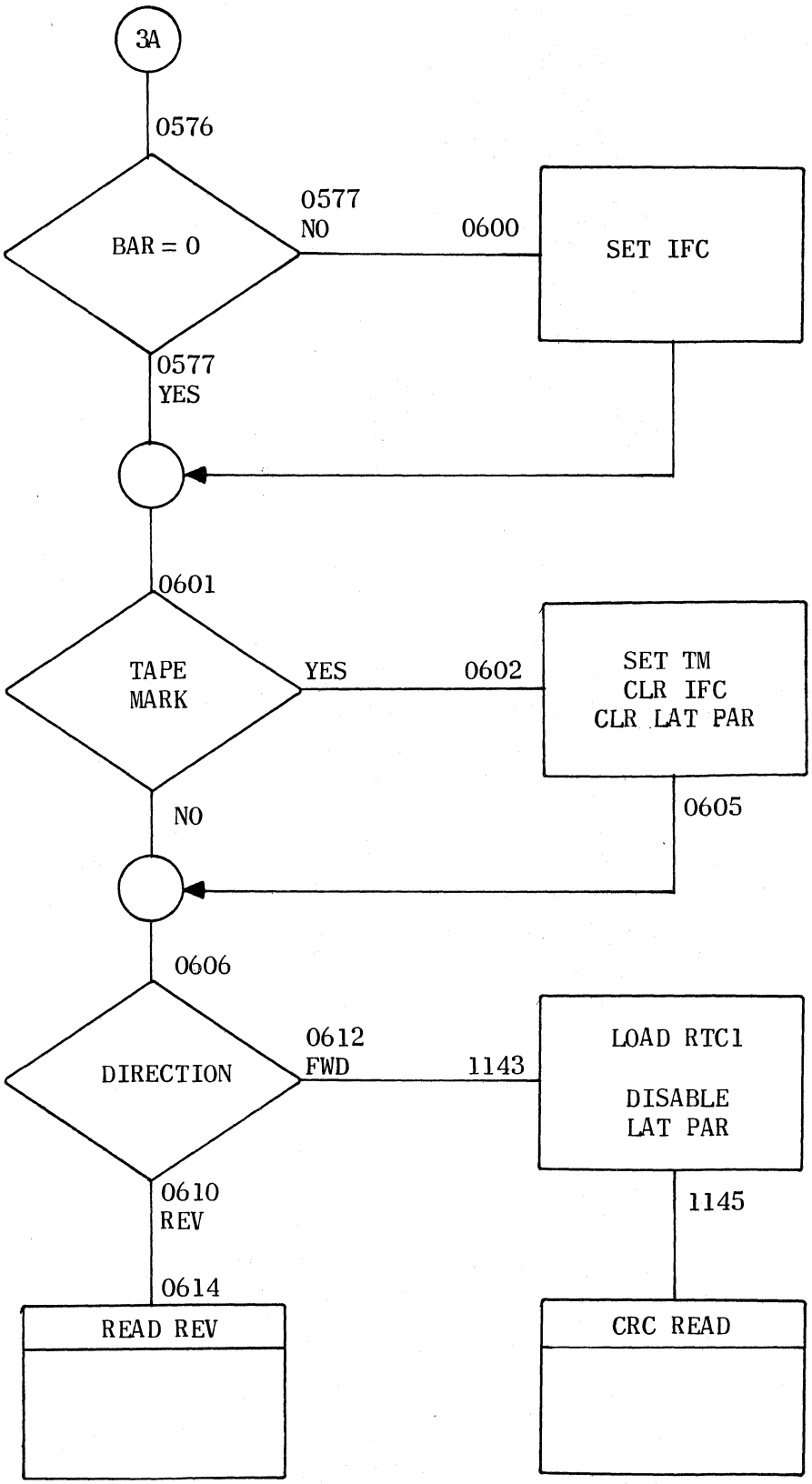


Figure 4-53. Space to IRG Sequence Flow Diagram (Sheet 3 of 3)

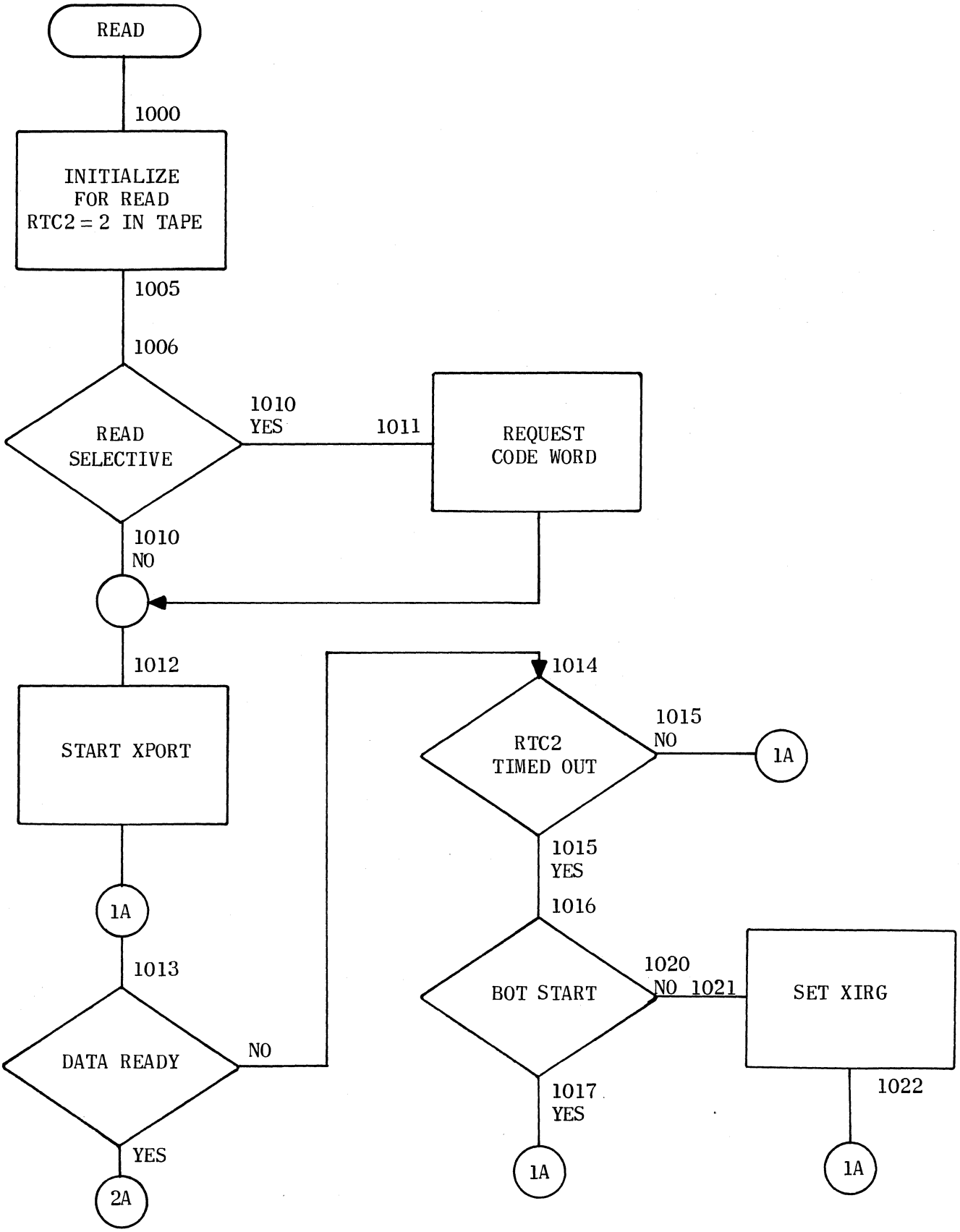


Figure 4-54. Read Sequence Flow Diagram (Sheet 1 of 7)

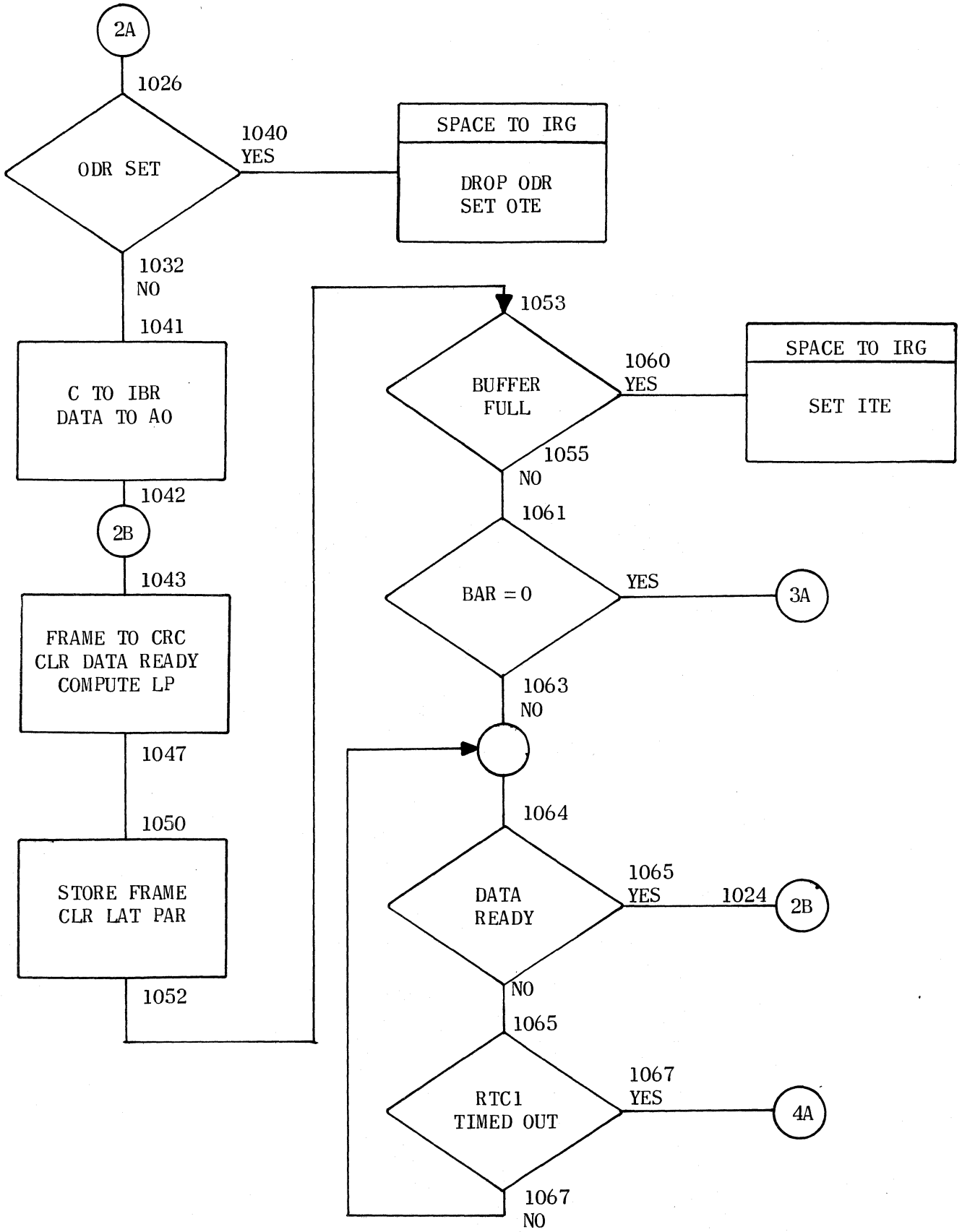


Figure 4-54. Read Sequence Flow Diagram (Sheet 2 of 7)

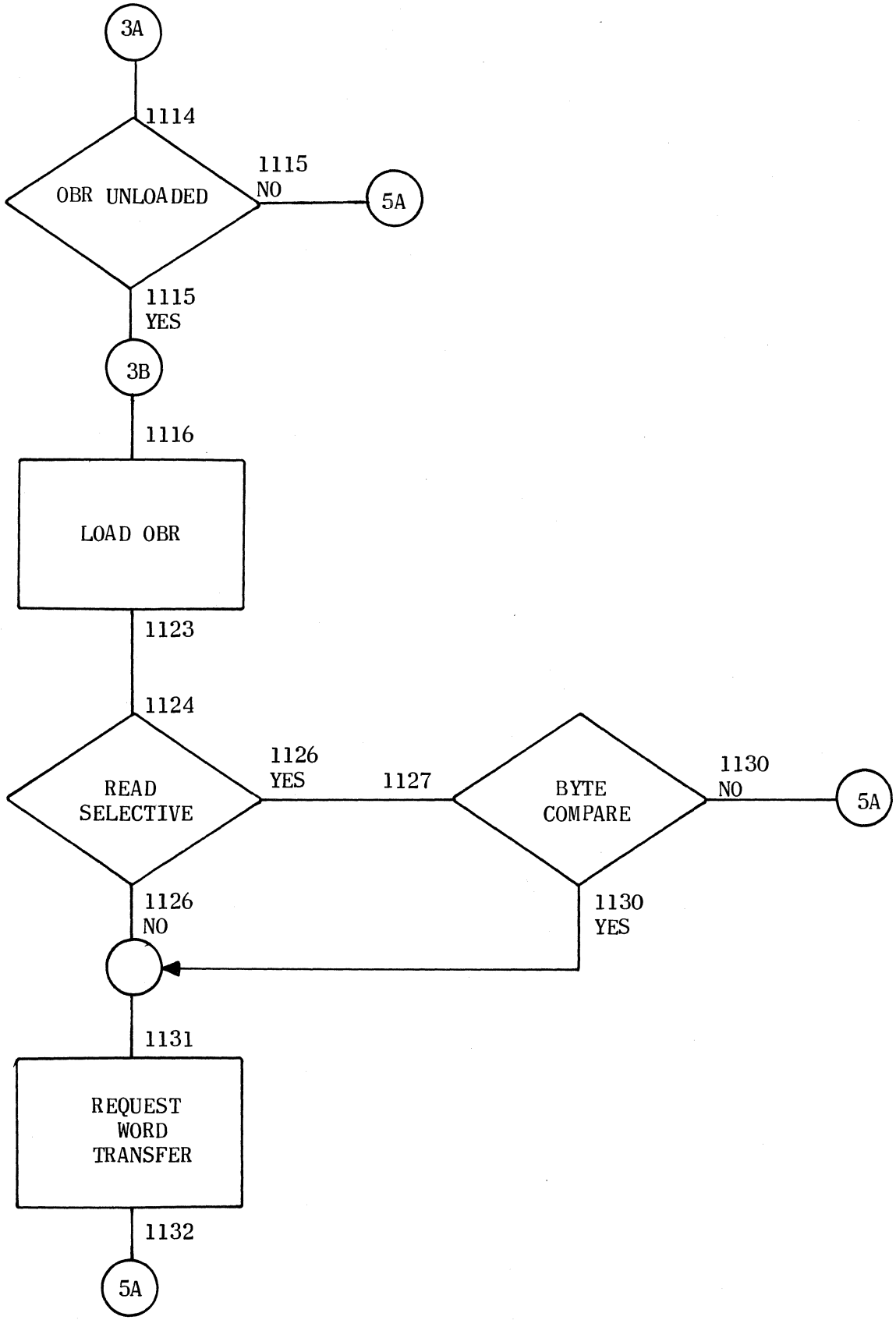


Figure 4-54. Read Sequence Flow Diagram (Sheet 3 of 7)

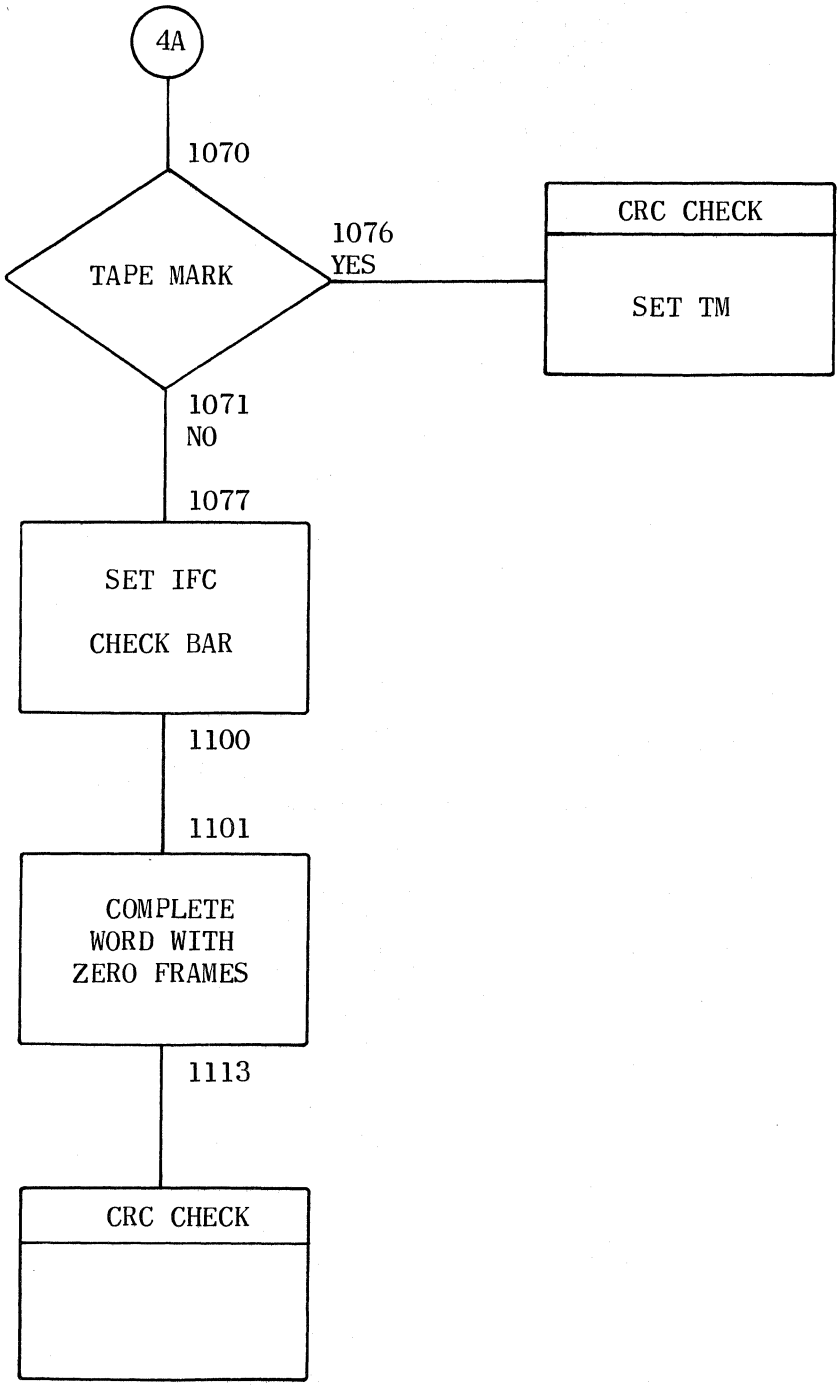


Figure 4-54. Read Sequence Flow Diagram (Sheet 4 of 7)

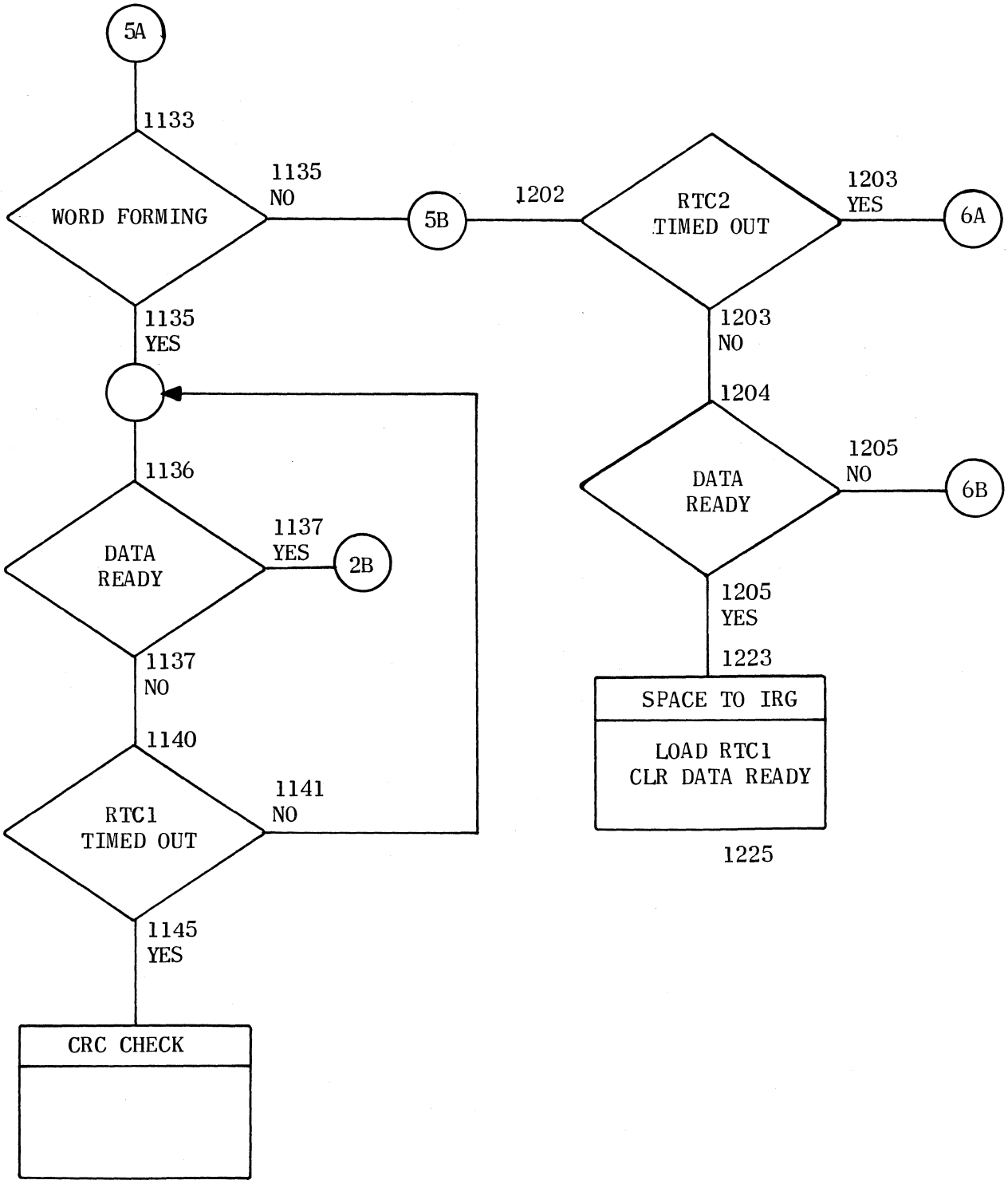


Figure 4-54. Read Sequence Flow Diagram (Sheet 5 of 7)

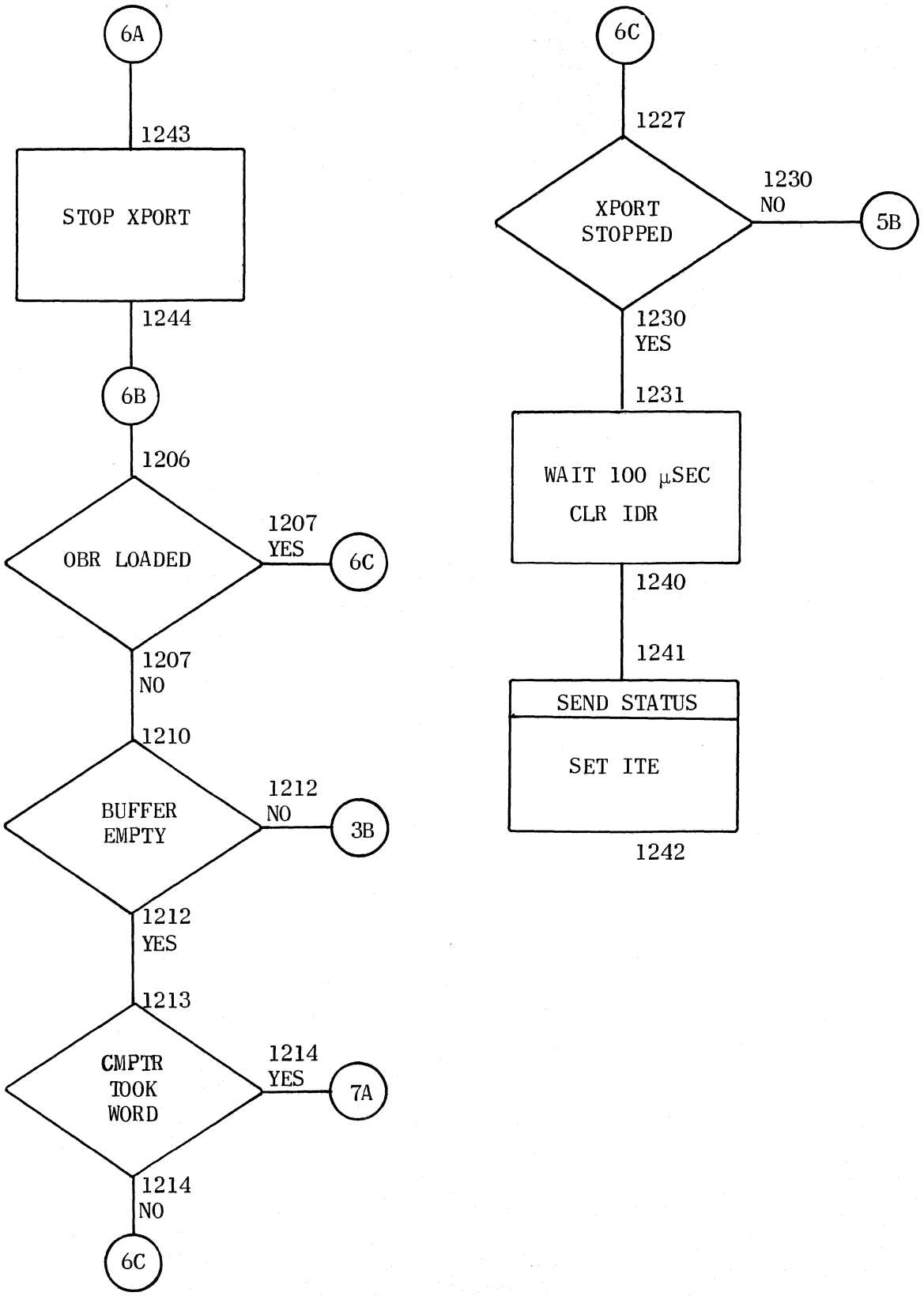


Figure 4-54. Read Sequence Flow Diagram (Sheet 6 of 7)

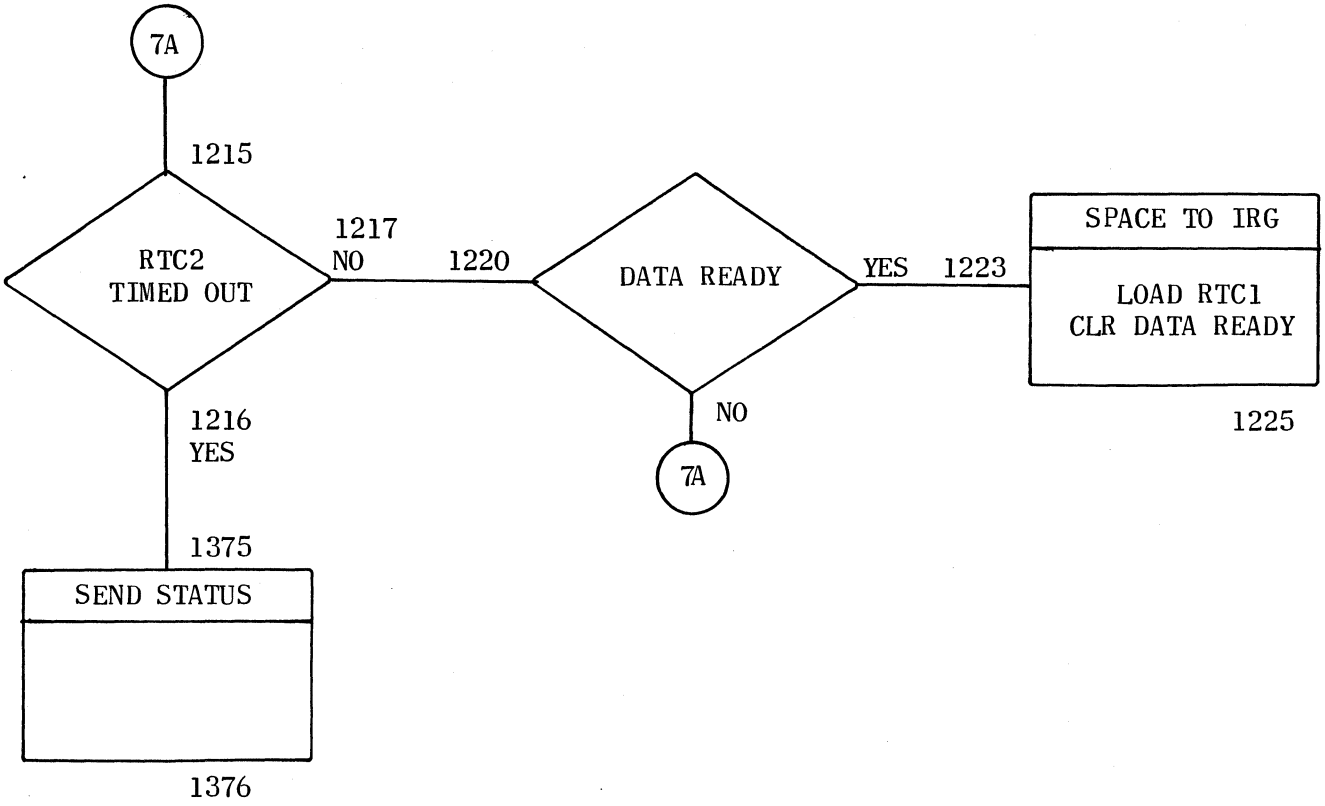


Figure 4-54. Read Sequence Flow Diagram (Sheet 7 of 7)

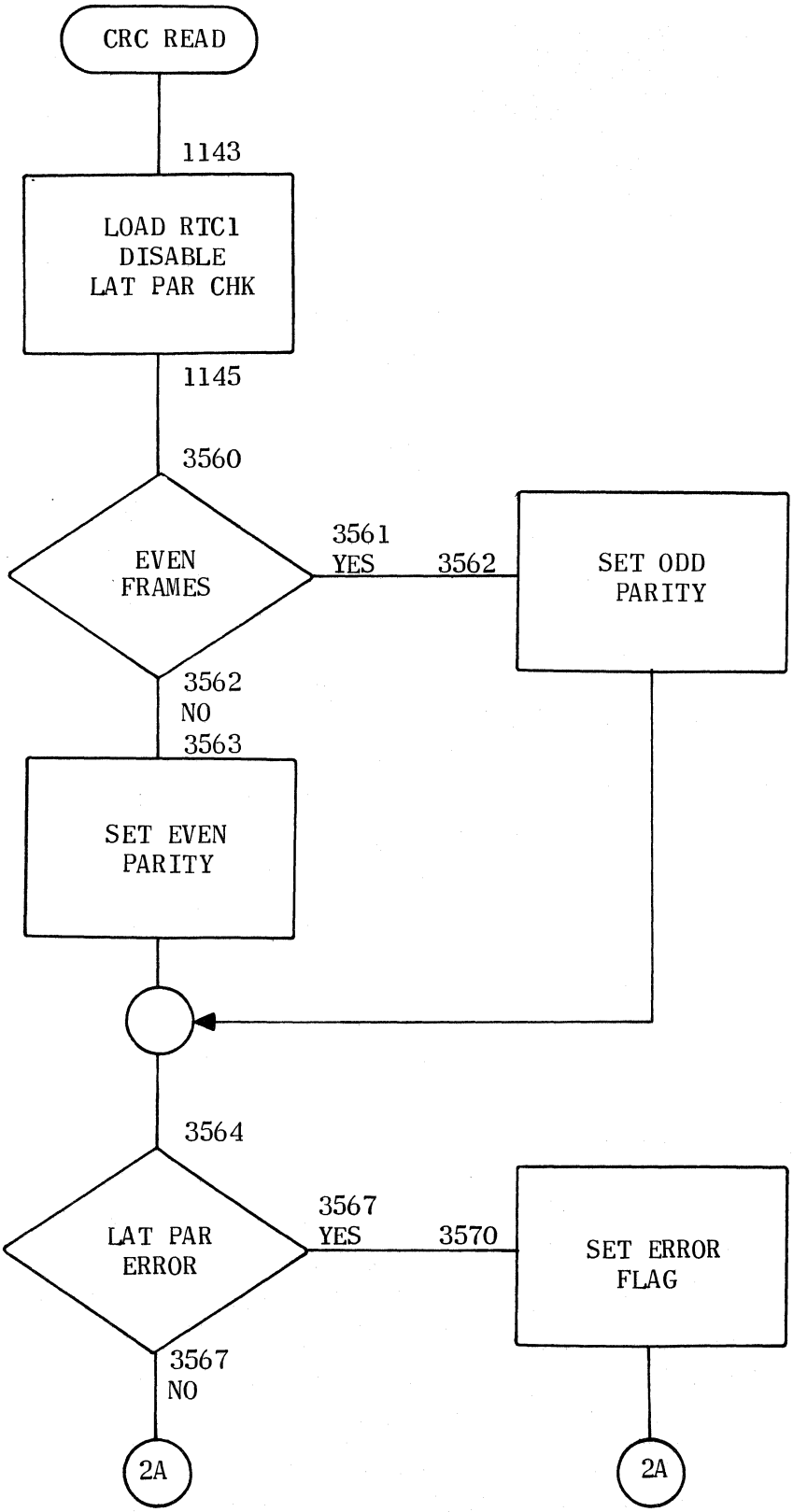


Figure 4-55. CRC Read Sequence Flow Diagram (Sheet 1 of 5)

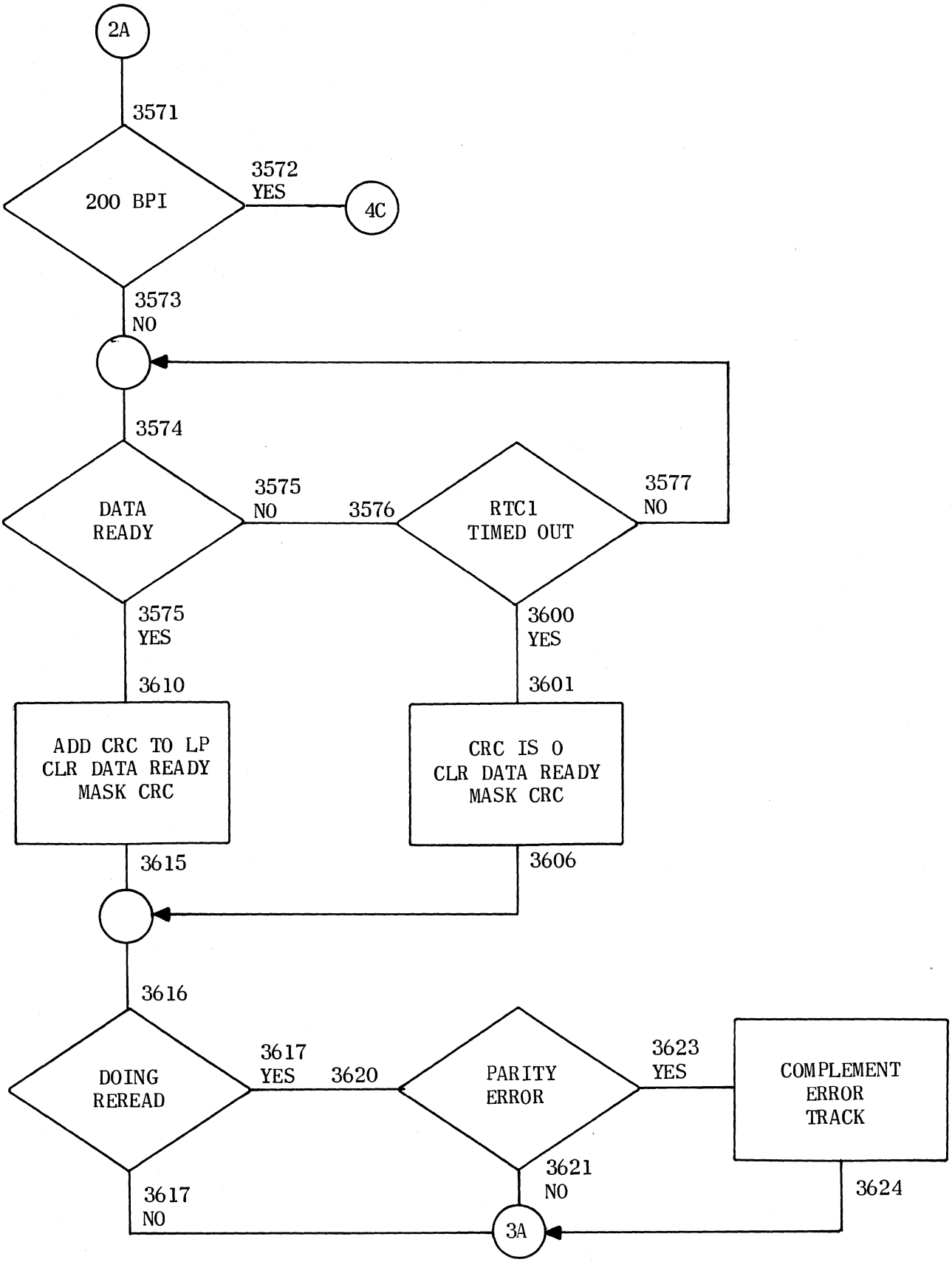


Figure 4-55. CRC Read Sequence Flow Diagram (Sheet 2 of 5)

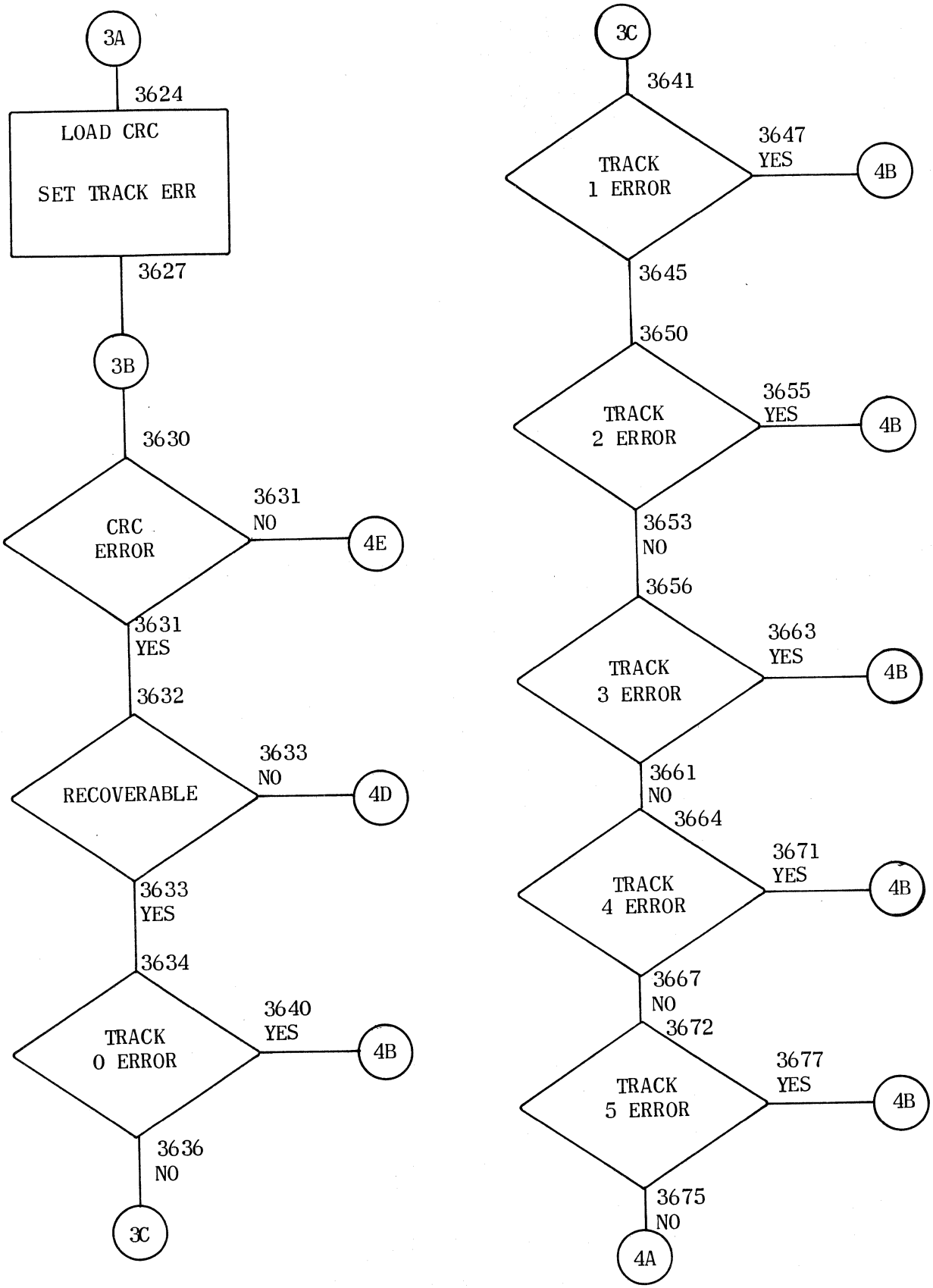


Figure 4-55. CRC Read Sequence Flow Diagram (Sheet 3 of 5)

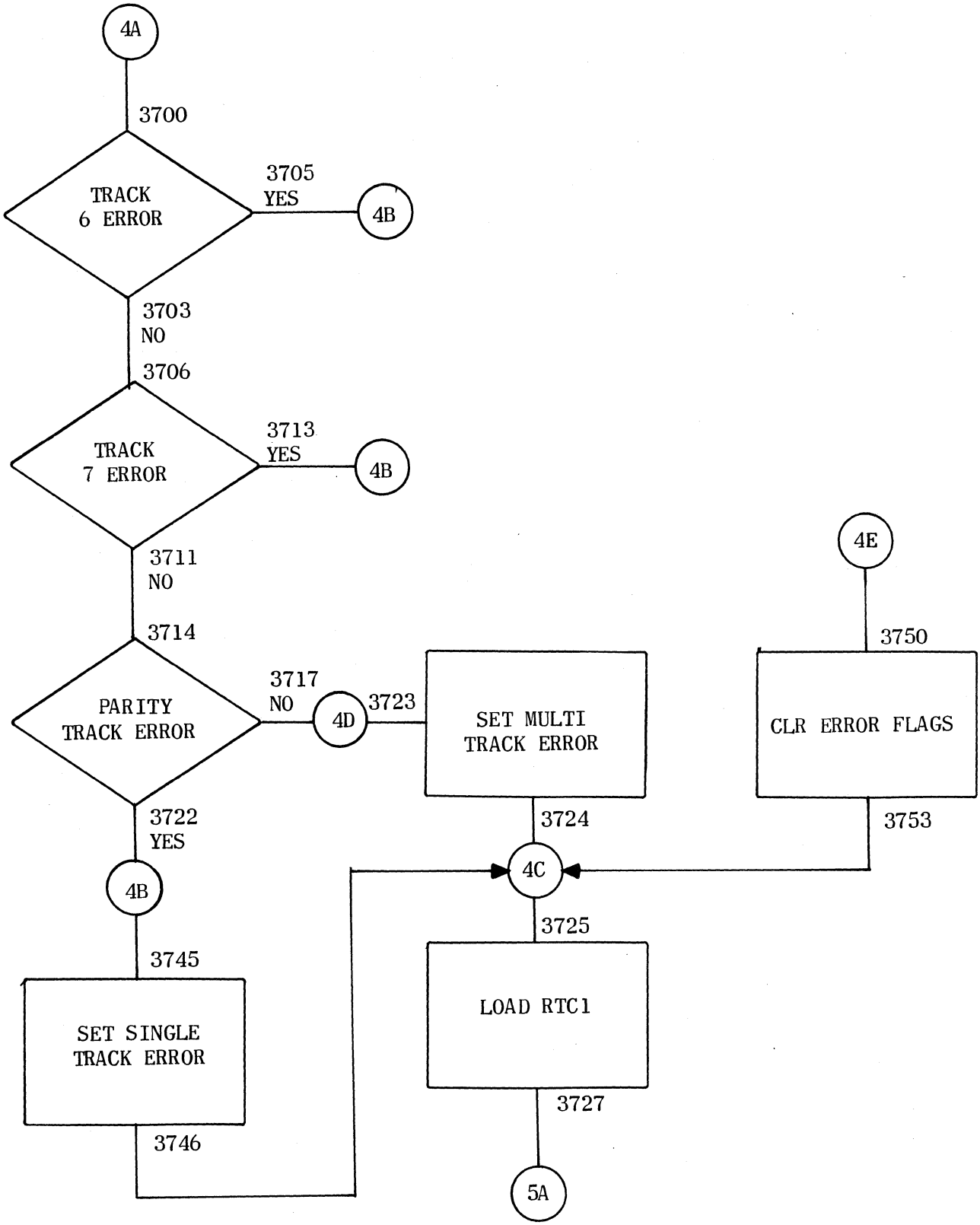


Figure 4-55. CRC Read Sequence Flow Diagram (Sheet 4 of 5)

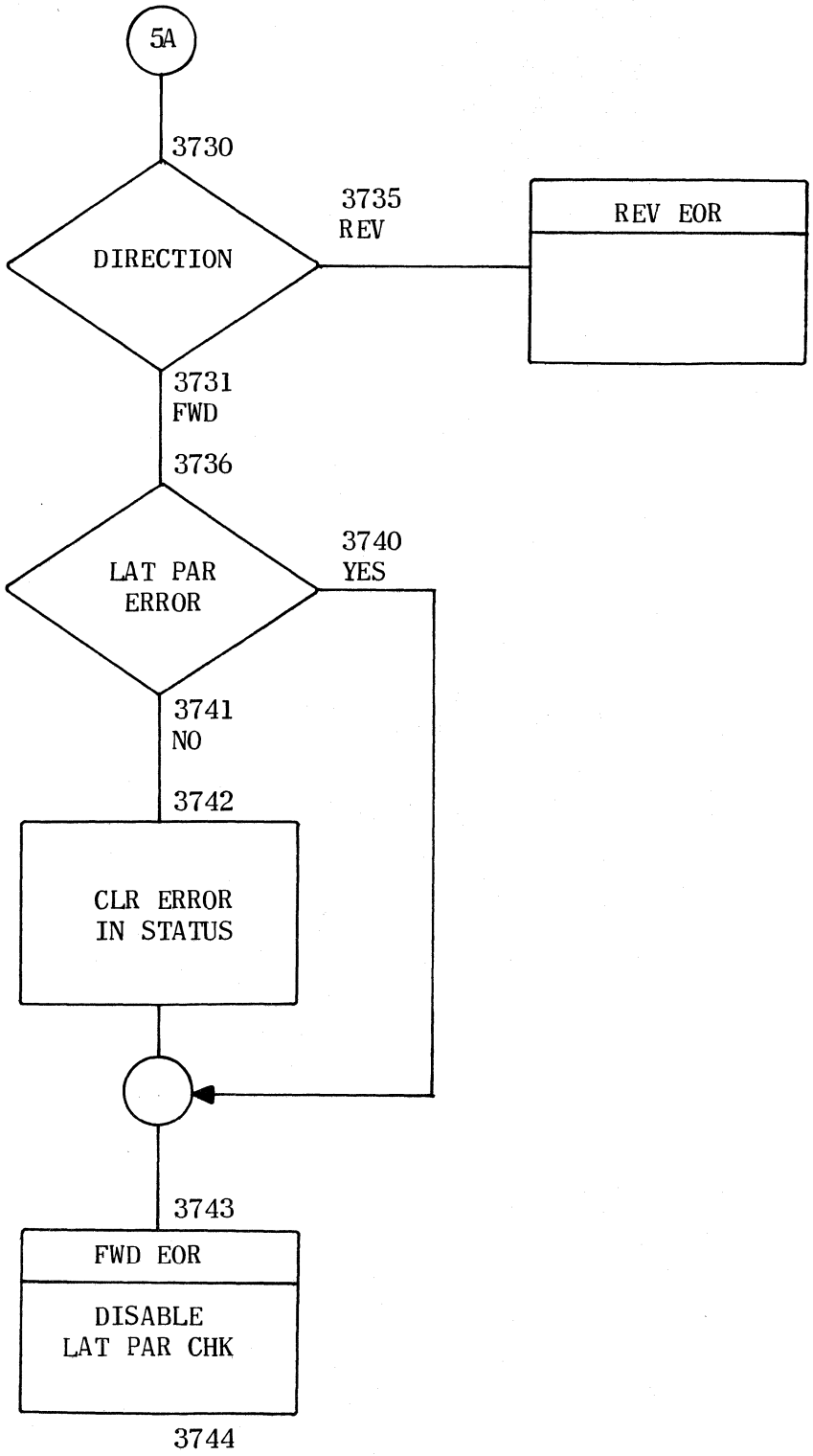


Figure 4-55. CRC Read Sequence Flow Diagram (Sheet 5 of 5)

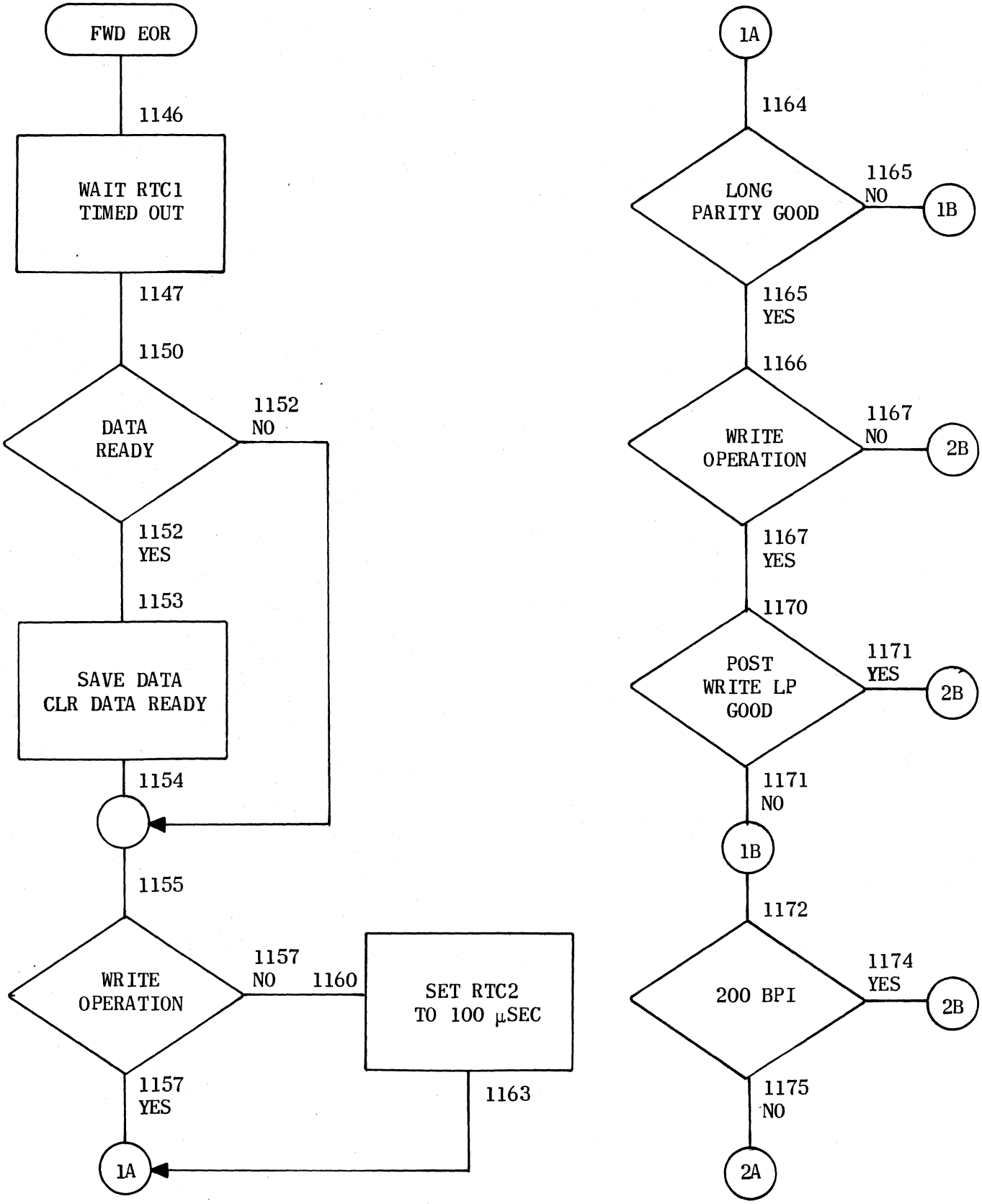


Figure 4-56. Forward End of Record Sequence Flow Diagram (Sheet 1 of 3)

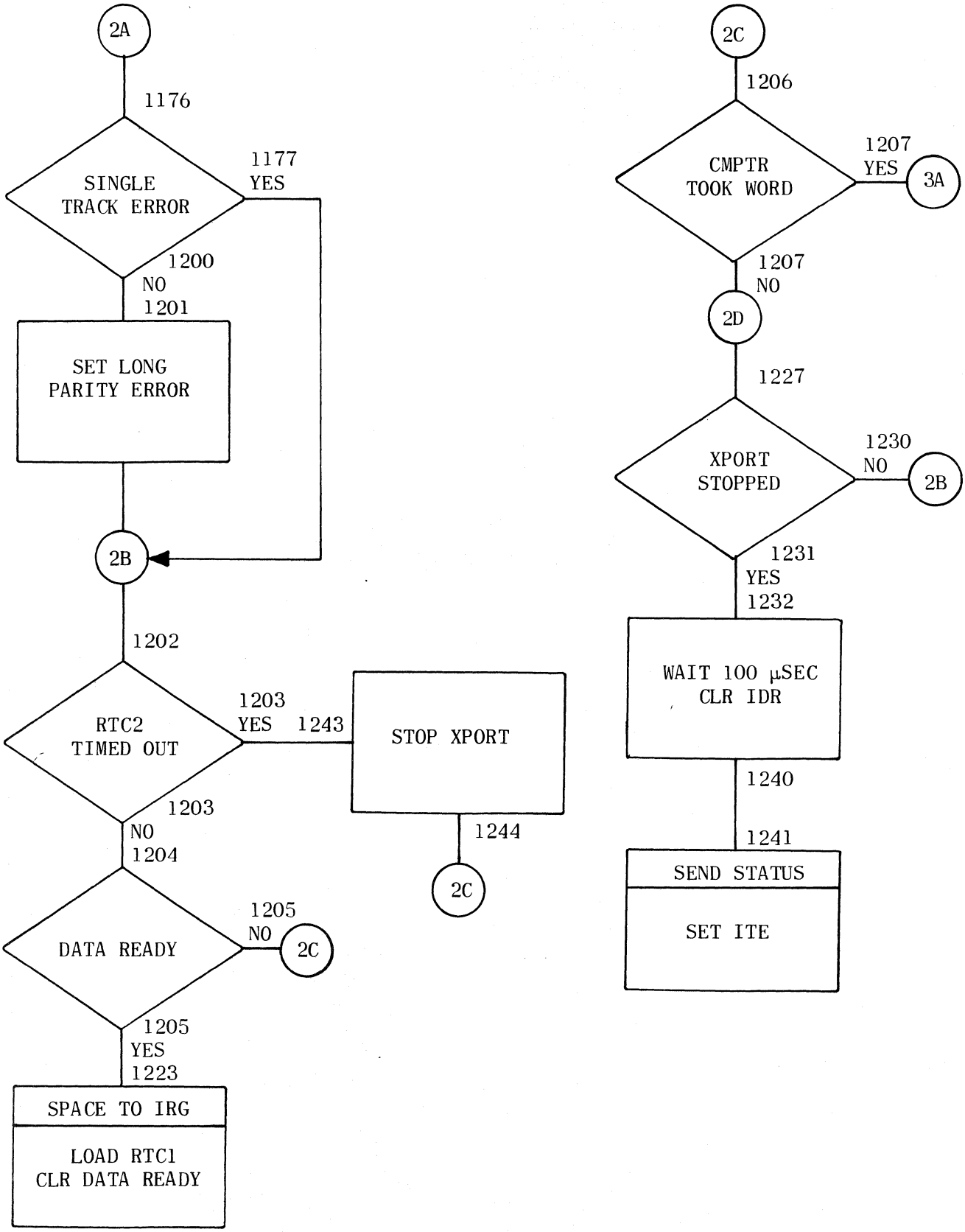


Figure 4-56. Forward End of Record Sequence Flow Diagram (Sheet 2 of 3)

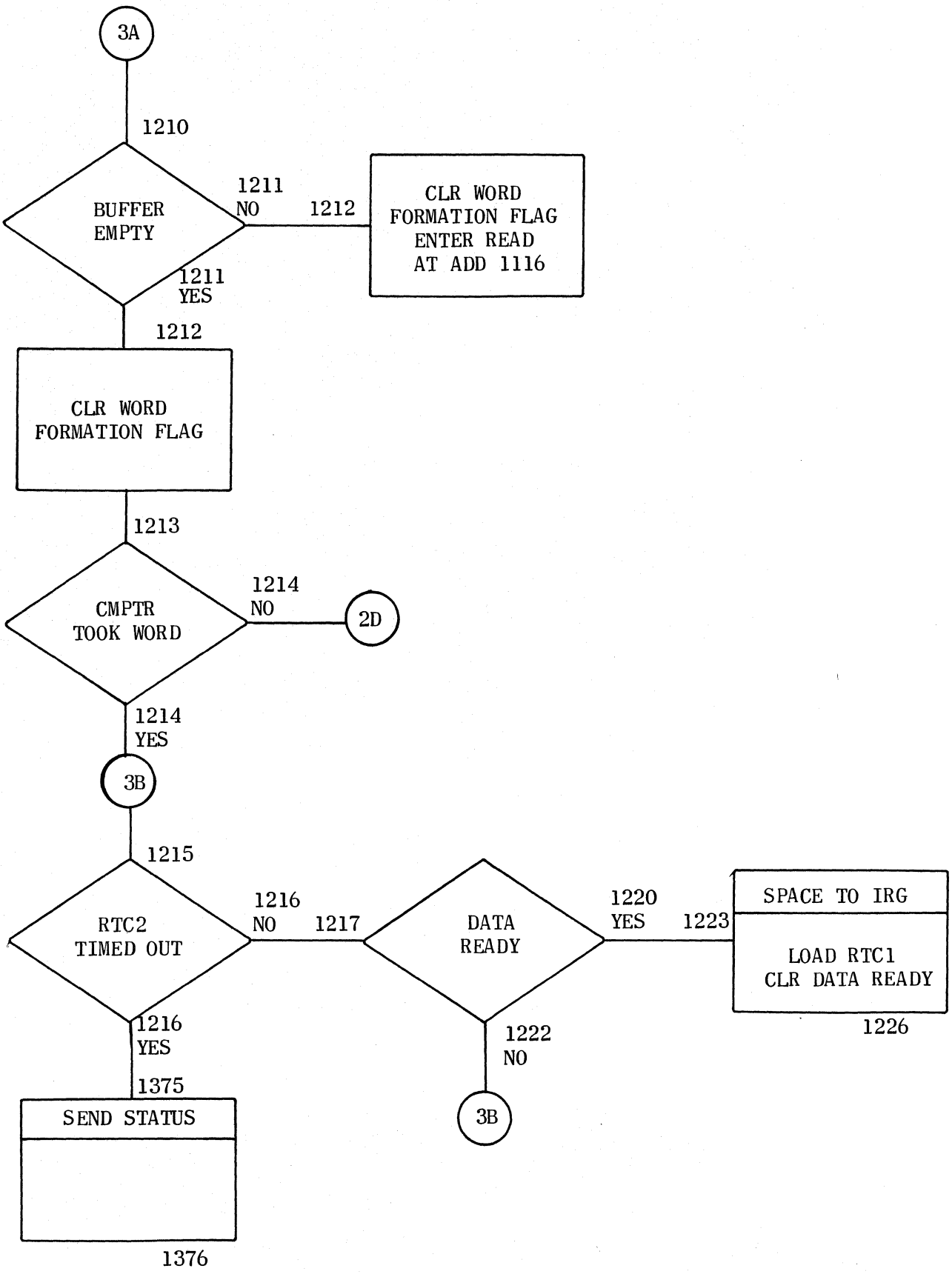


Figure 4-56. Forward End of Record Sequence Flow Diagram (Sheet 3 of 3)

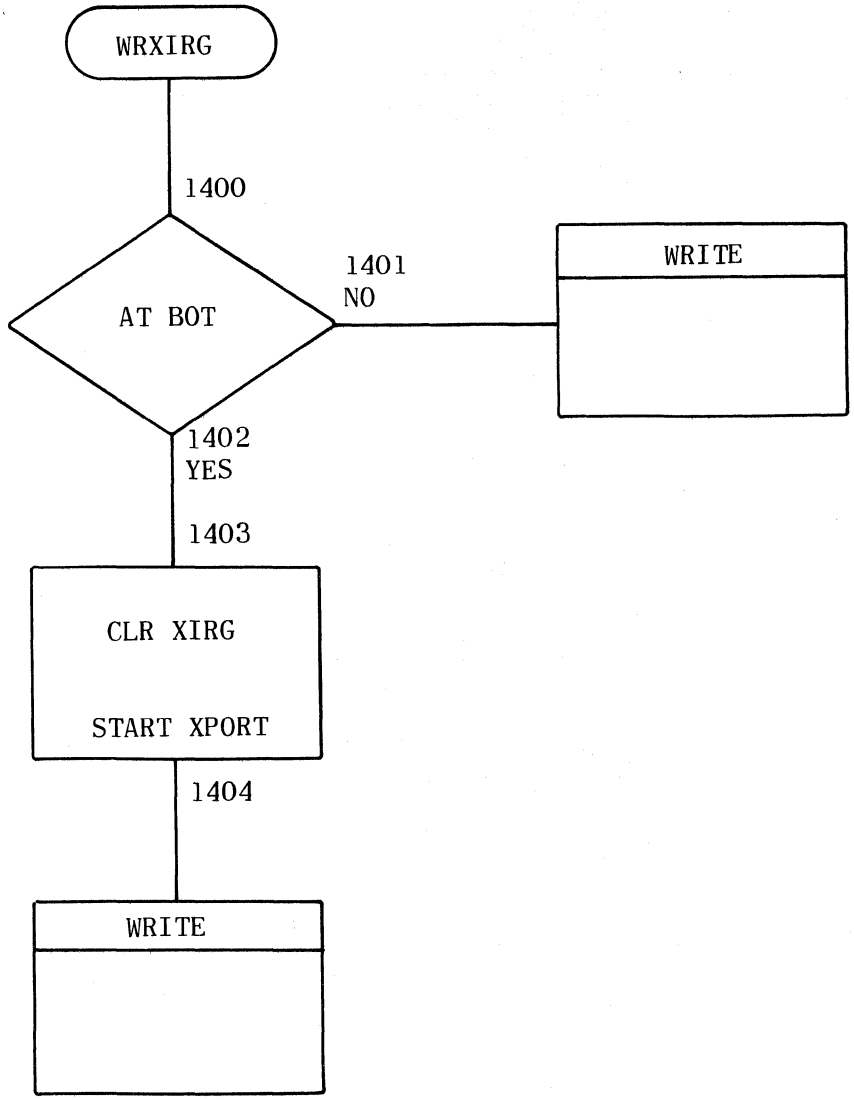


Figure 4-57. Write XIRG Sequence Flow Diagram

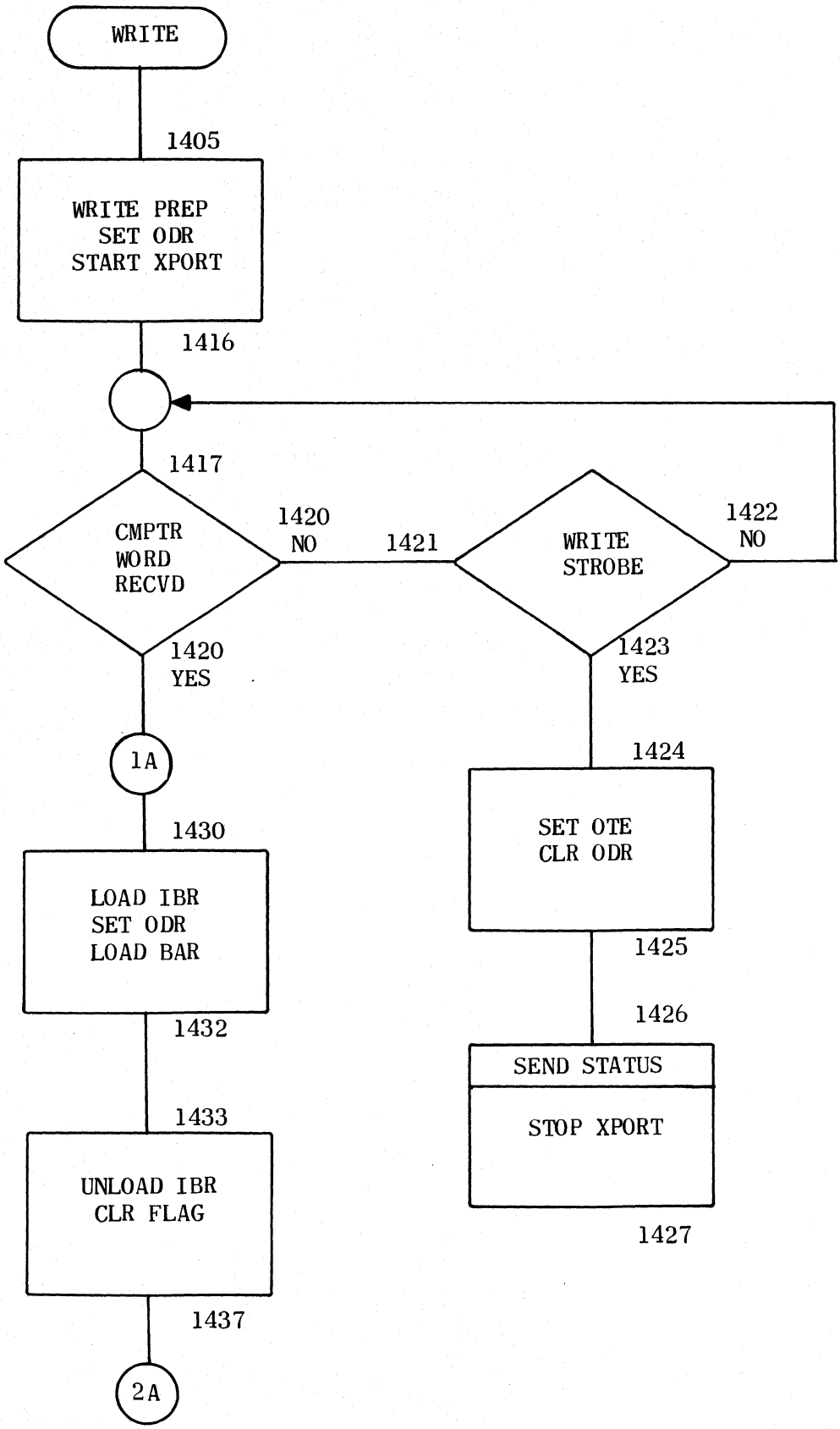


Figure 4-58. Write Sequence Flow Diagram (Sheet 1 of 9)

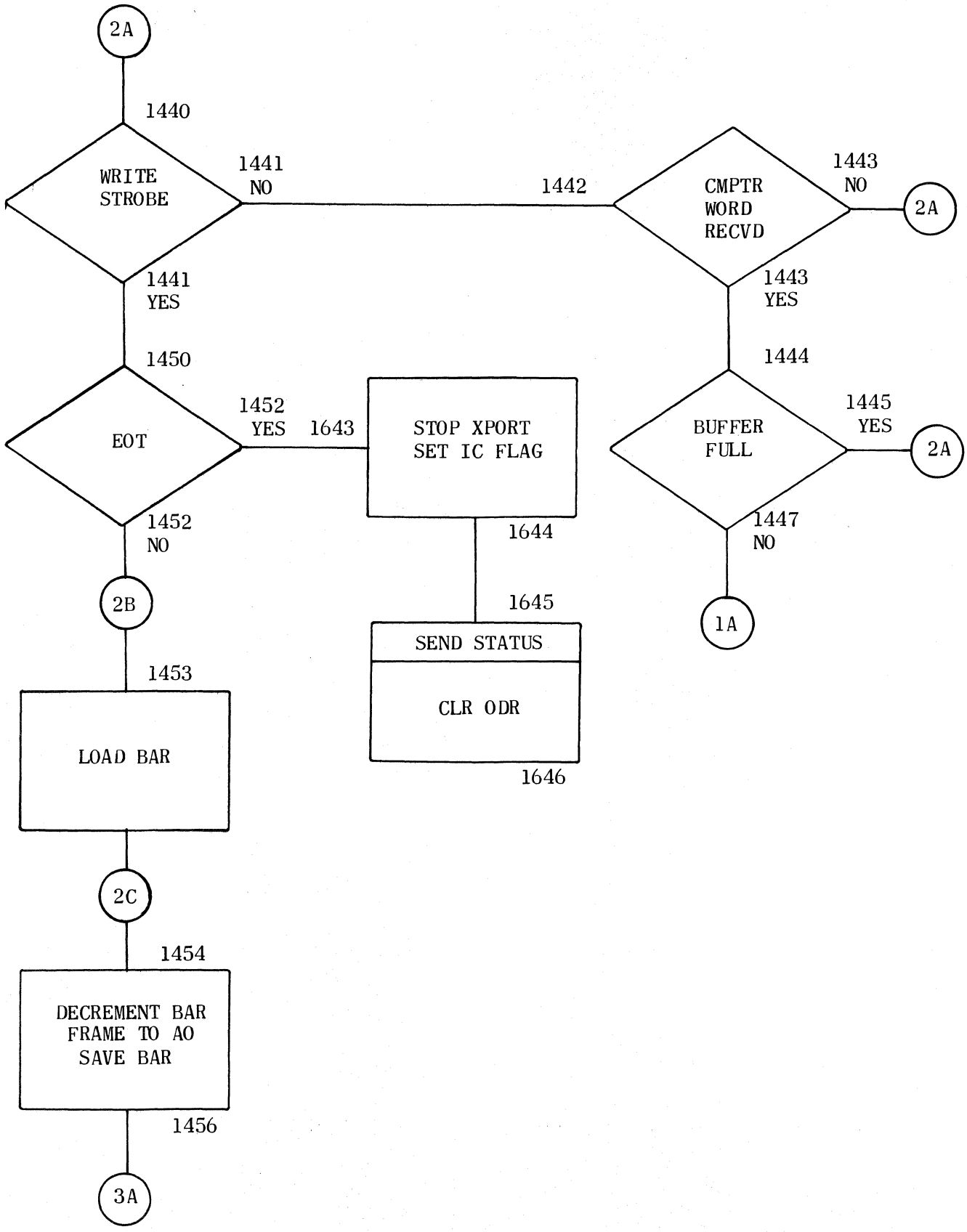


Figure 4-58. Write Sequence Flow Diagram (Sheet 2 of 9)

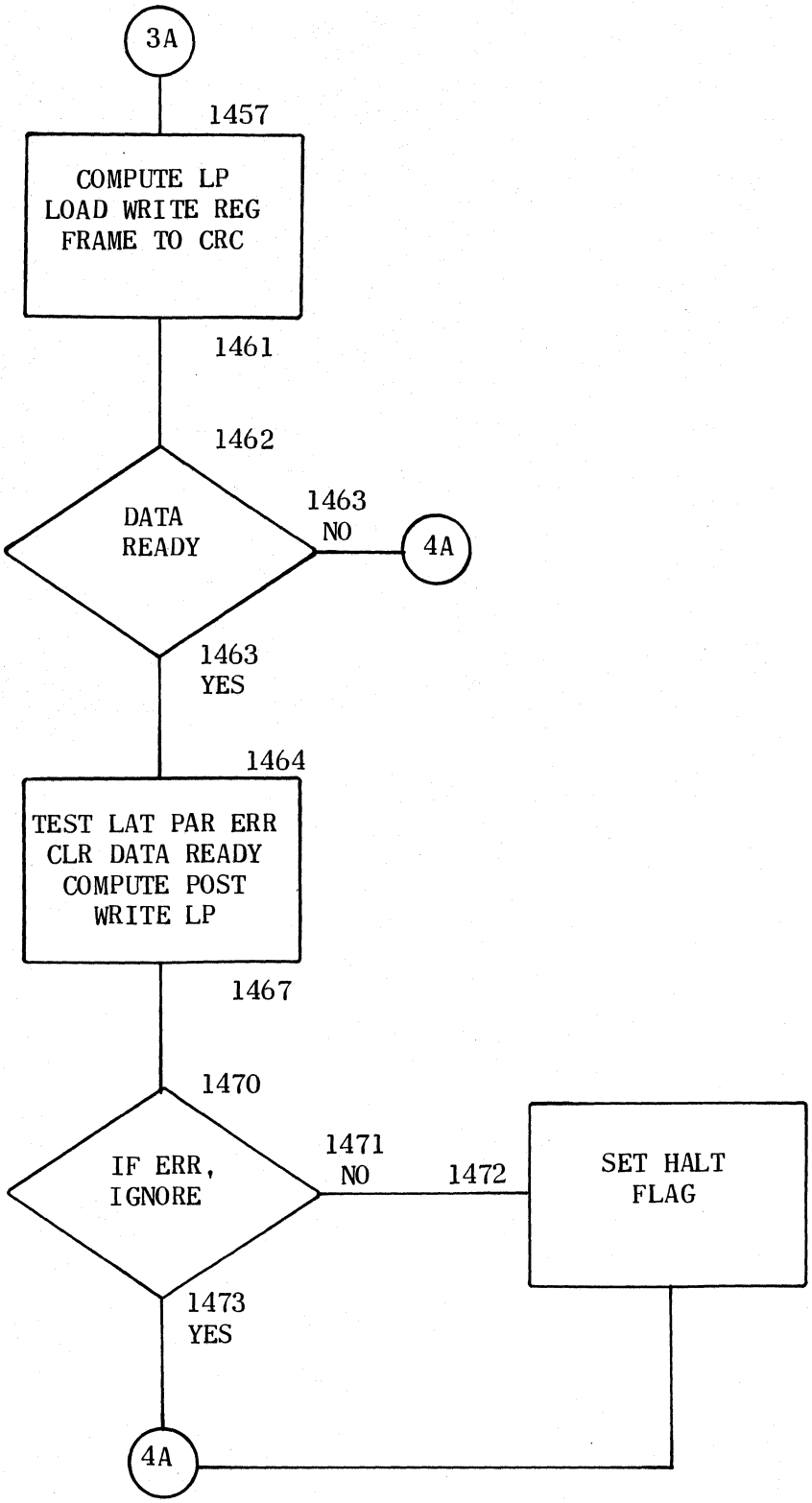


Figure 4-58. Write Sequence Flow Diagram (Sheet 3 of 9)

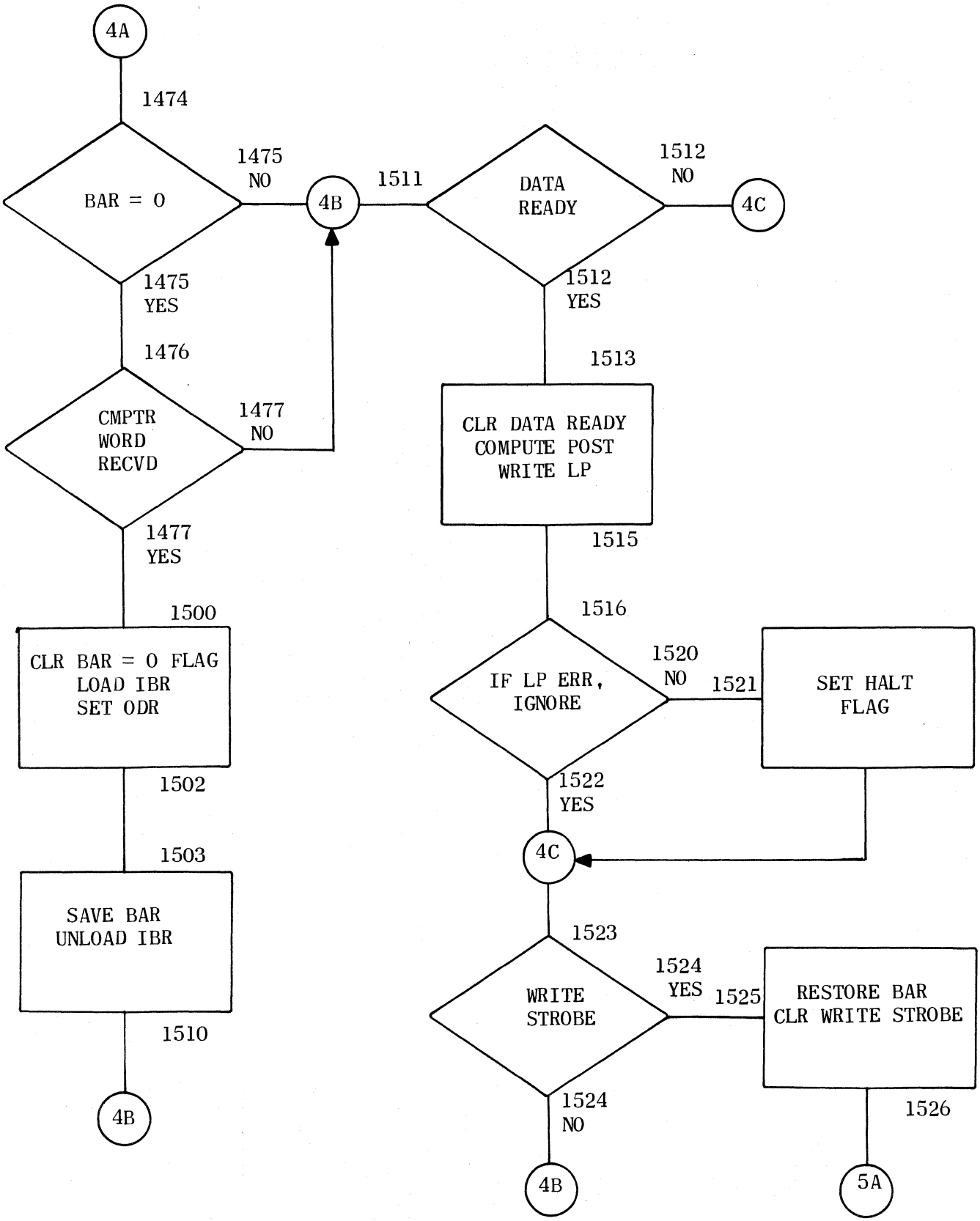


Figure 4-58. Write Sequence Flow Diagram (Sheet 4 of 9)

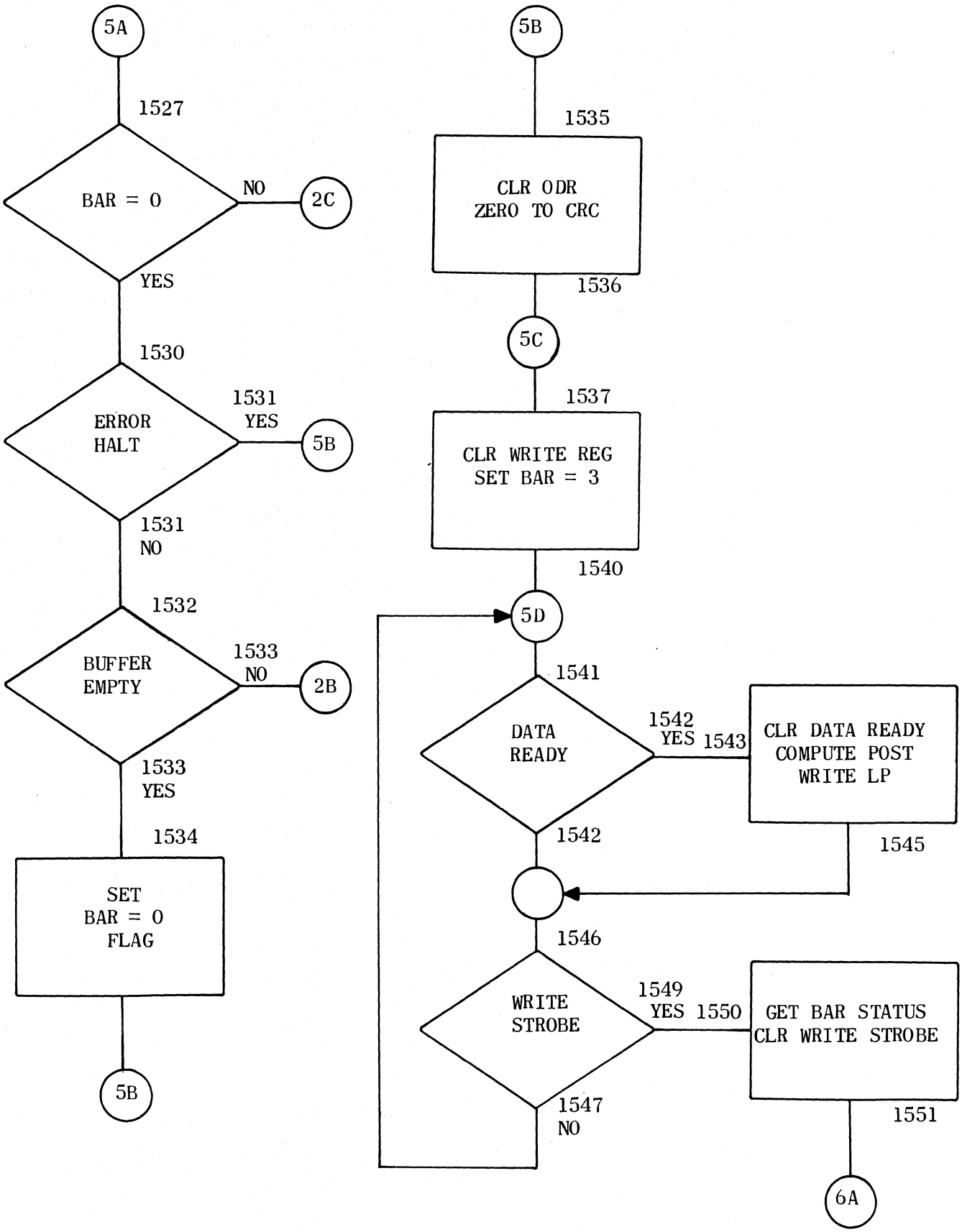


Figure 4-58. Write Sequence Flow Diagram (Sheet 5 of 9)

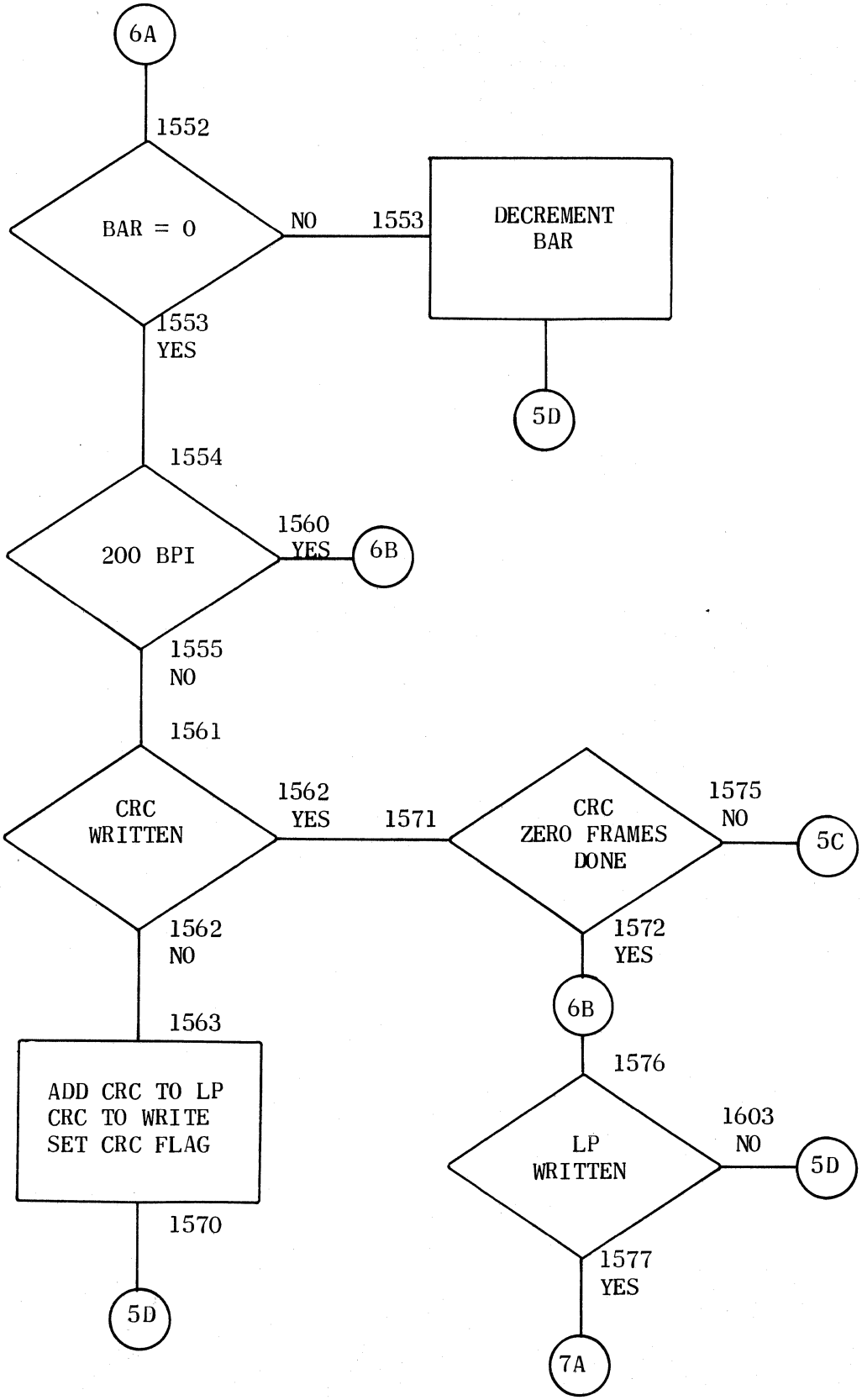


Figure 4-58. Write Sequence Flow Diagram (Sheet 6 of 9)

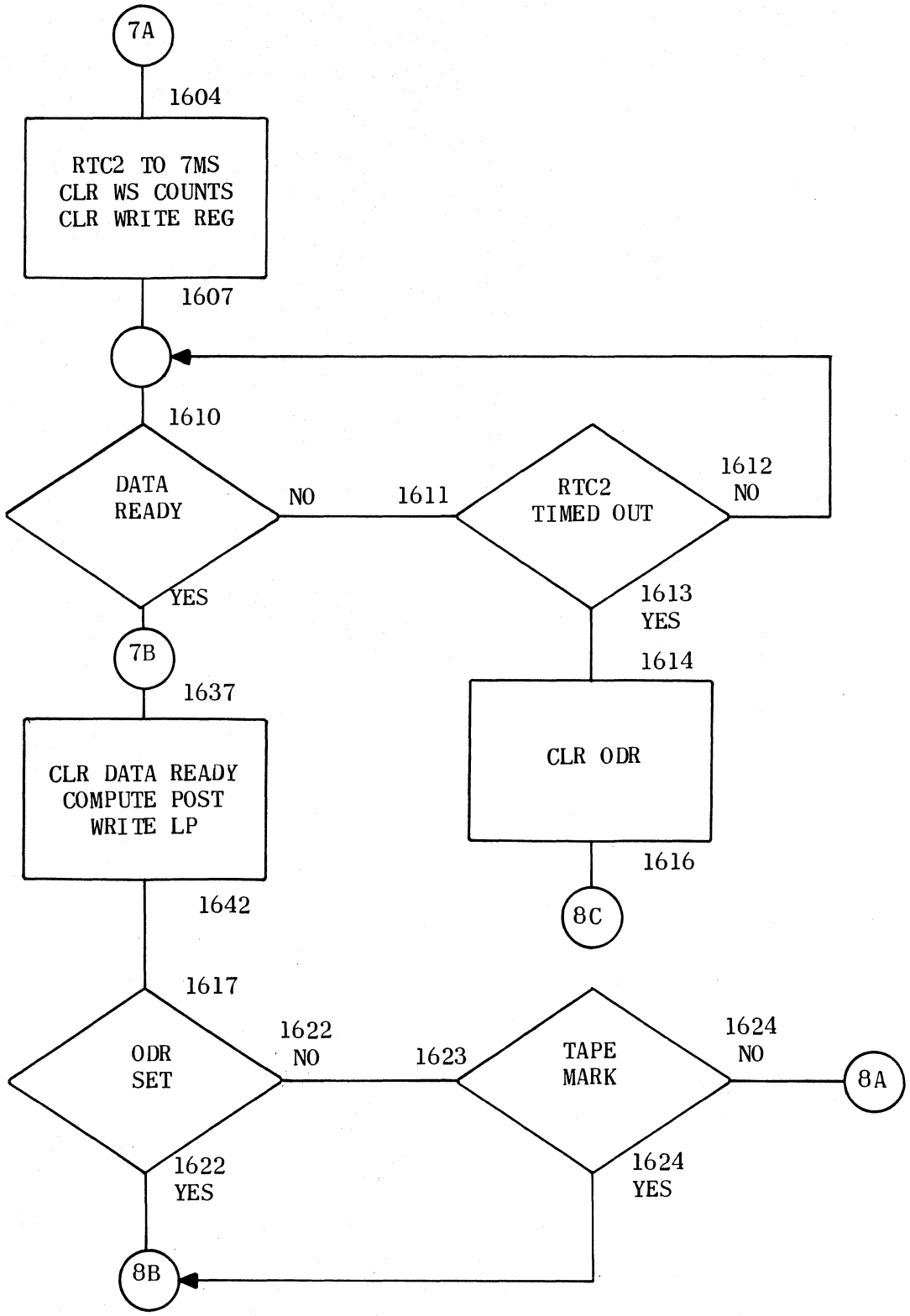


Figure 4-58. Write Sequence Flow Diagram (Sheet 7 of 9)

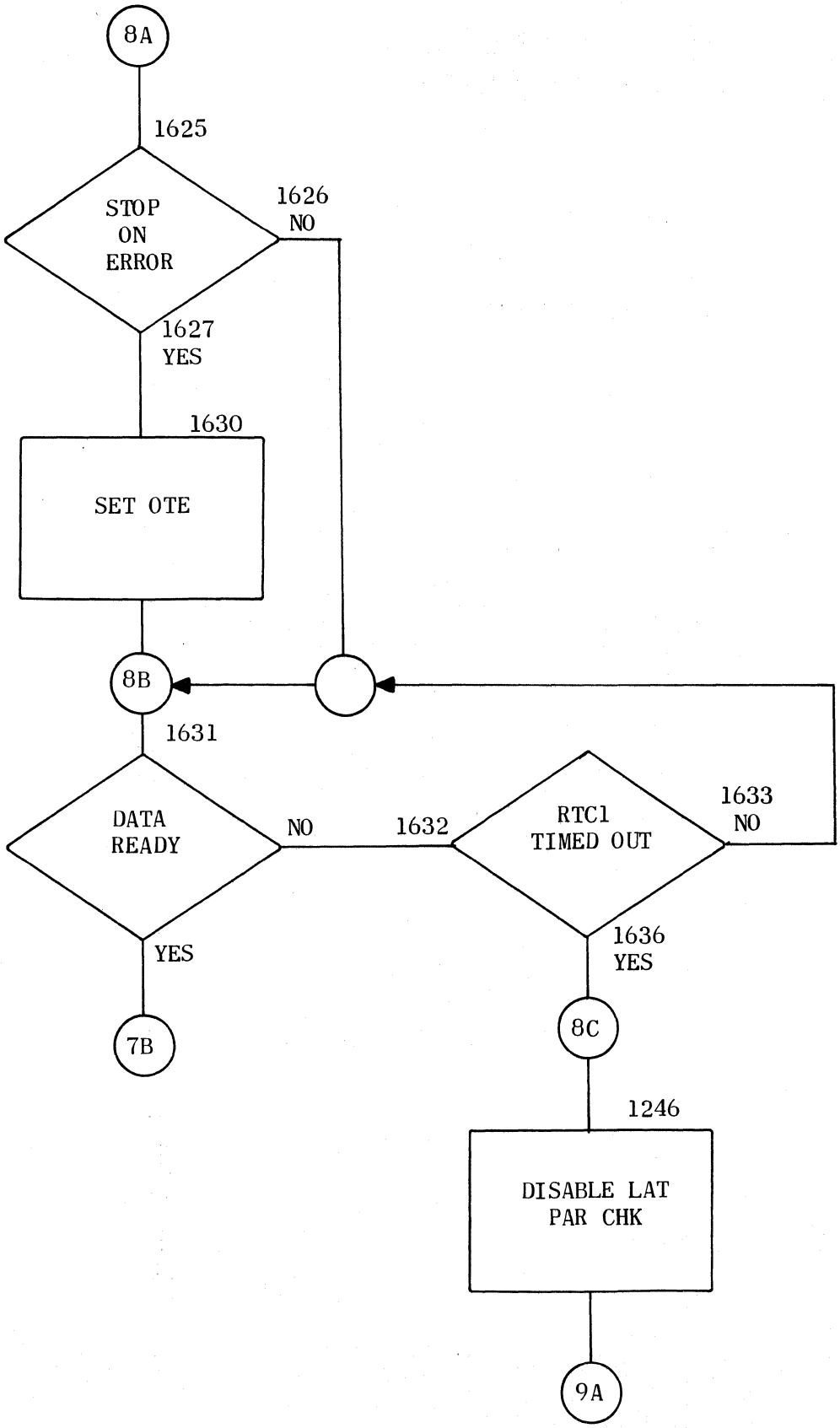


Figure 4-58. Write Sequence Flow Diagram (Sheet 8 of 9)

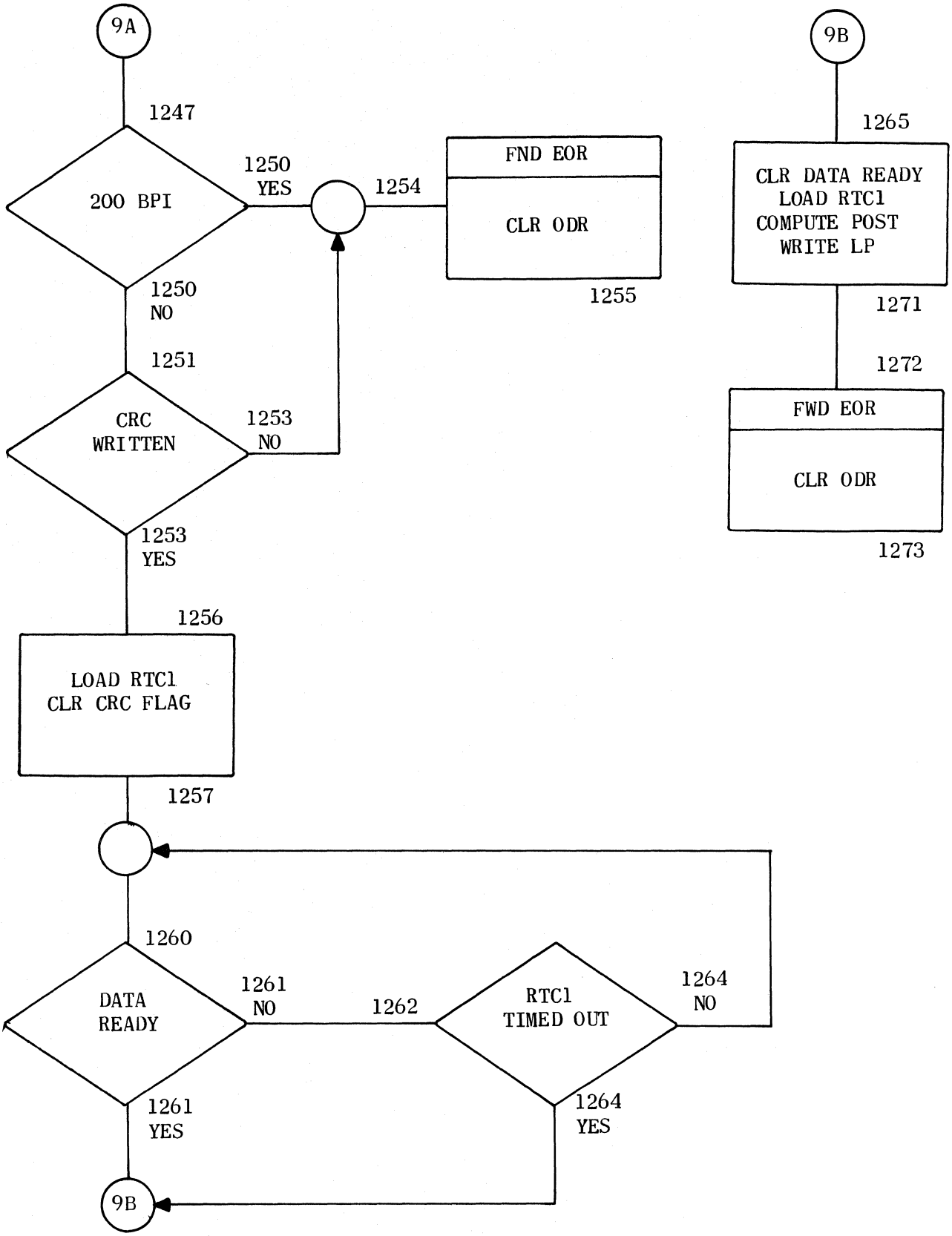


Figure 4-58. Write Sequence Flow Diagram (Sheet 9 of 9)

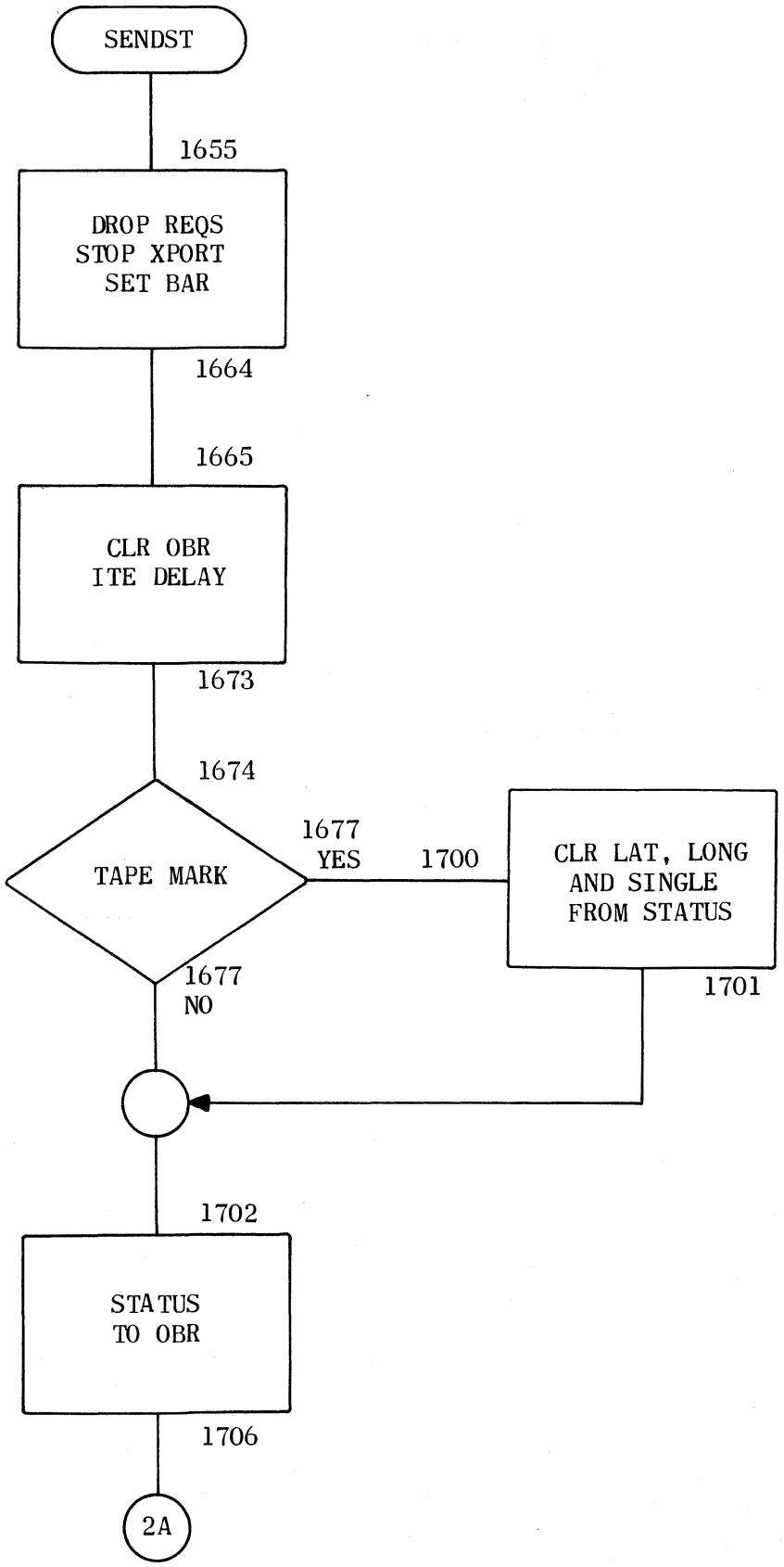


Figure 4-59. Send Status Sequence Flow Diagram (Sheet 1 of 2)

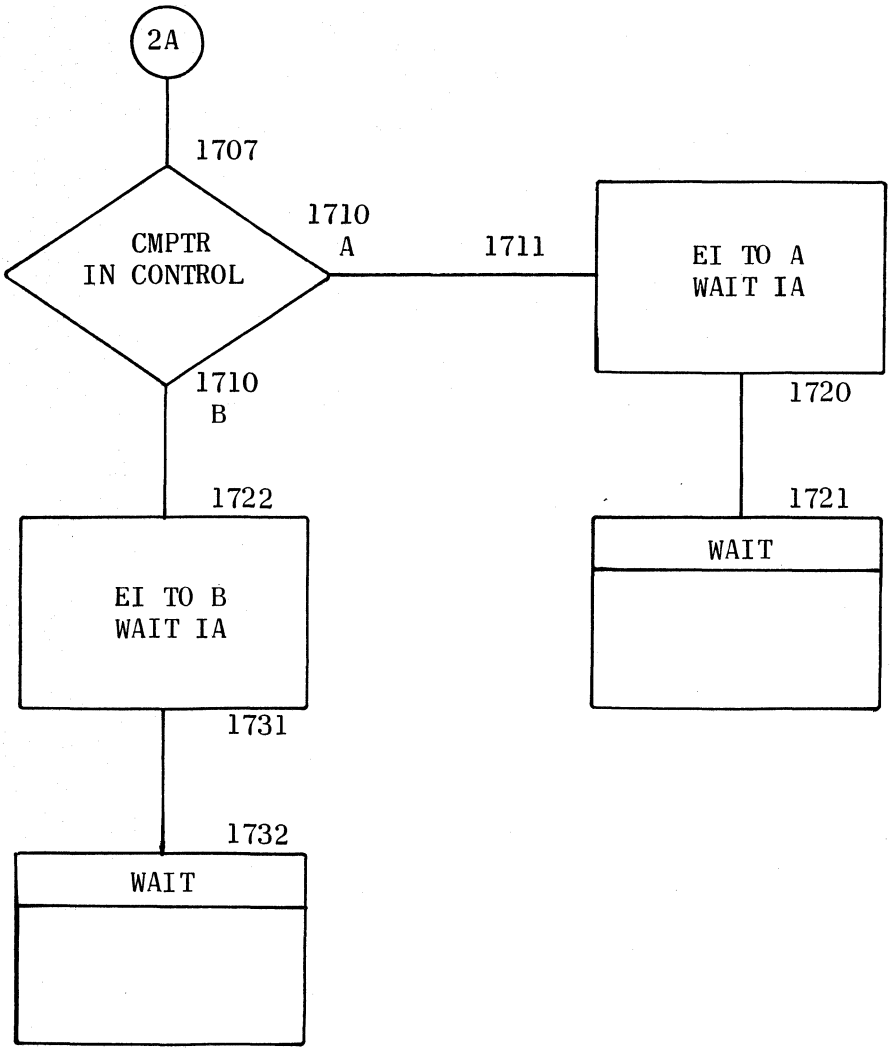


Figure 4-59. Send Status Sequence Flow Diagram (Sheet 2 of 2)

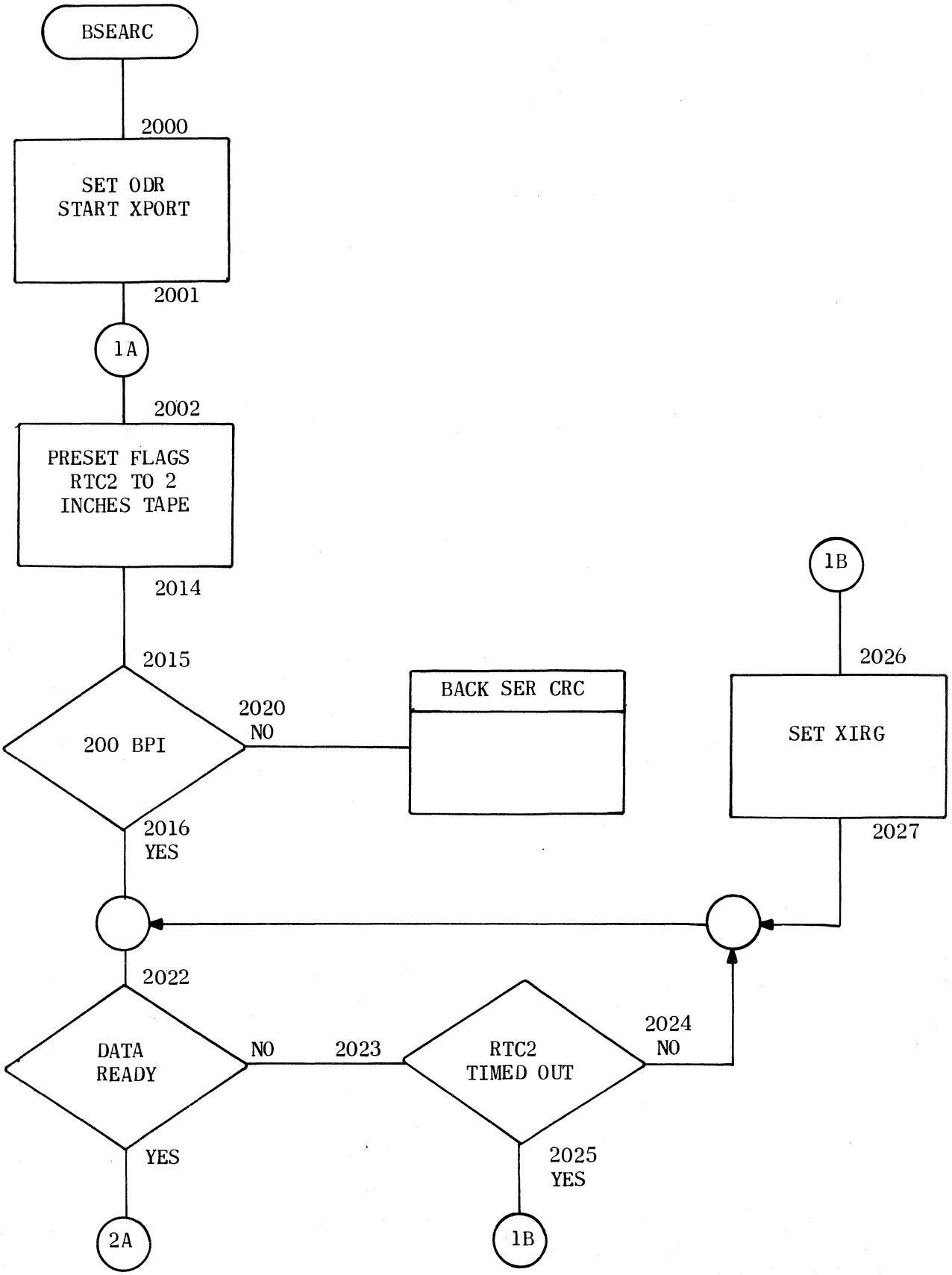


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 1 of 8)

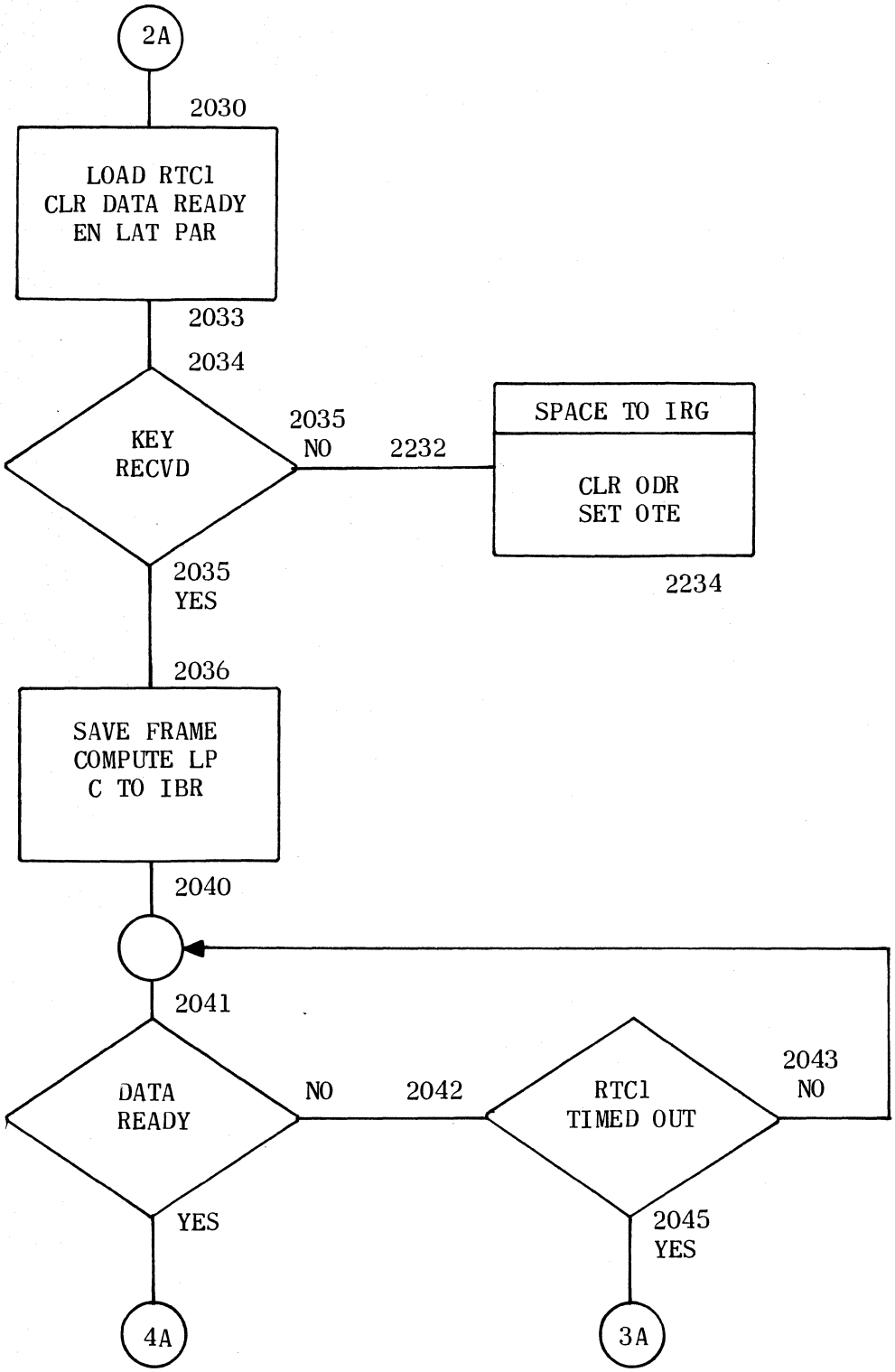


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 2 of 8)

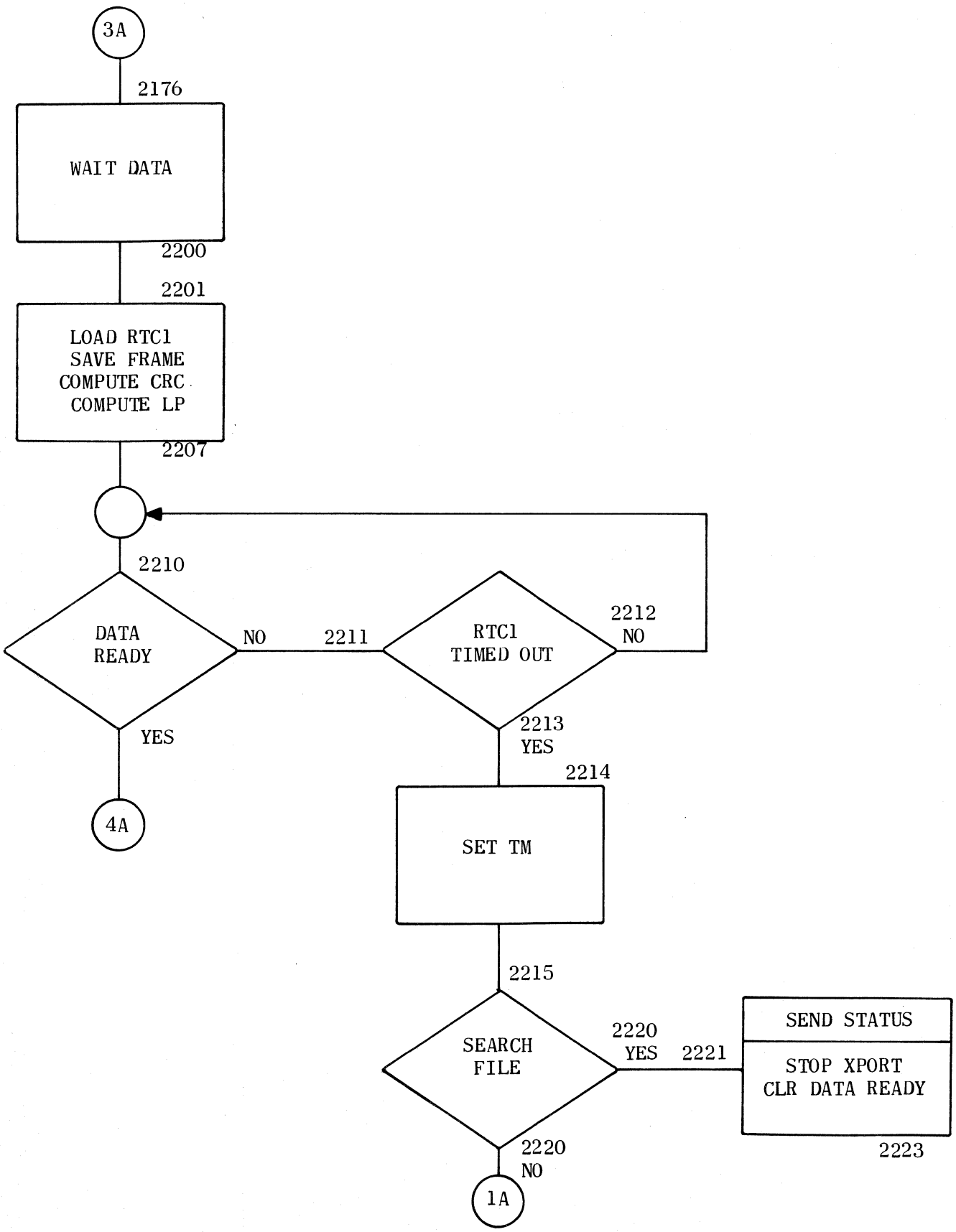


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 3 of 8)

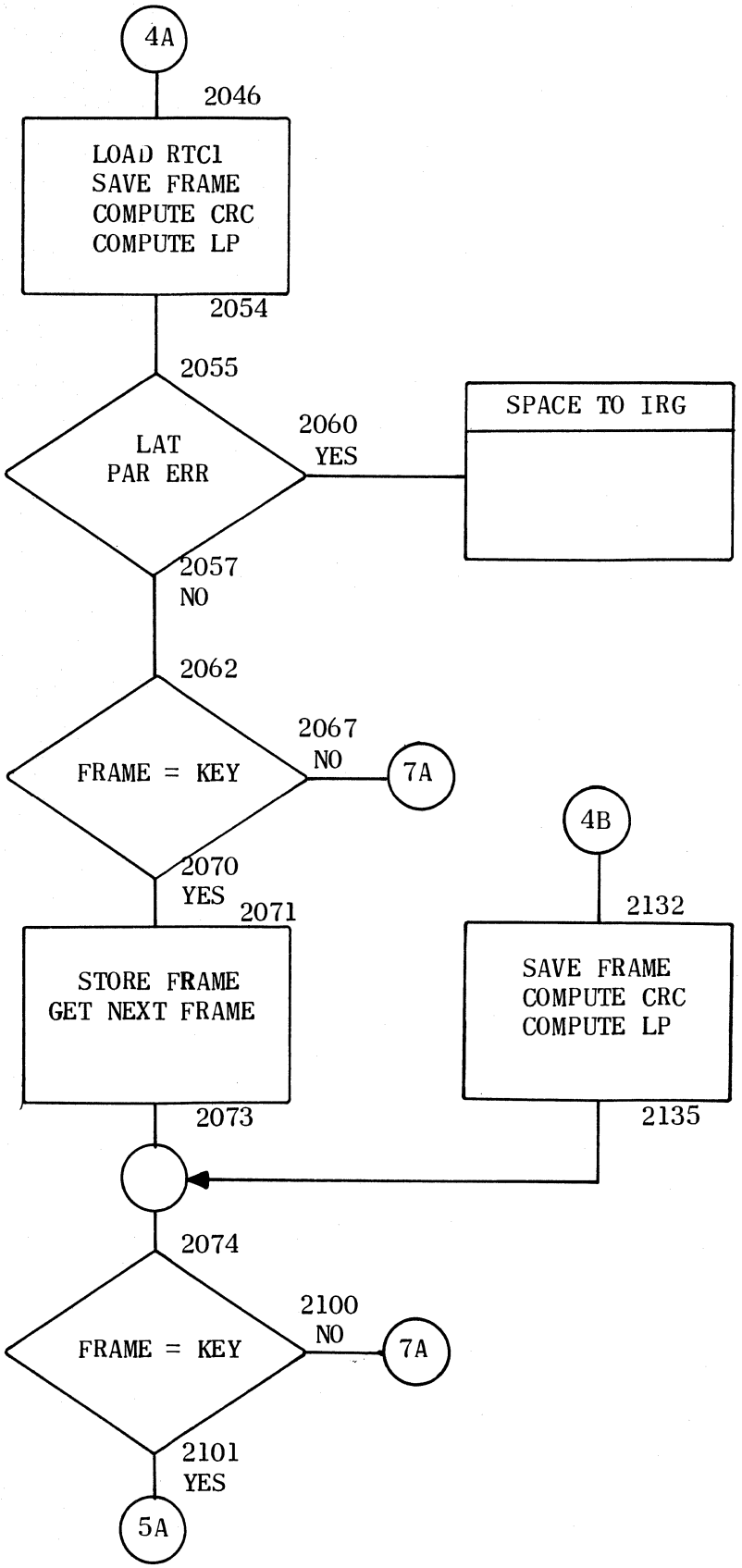


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 4 of 8)

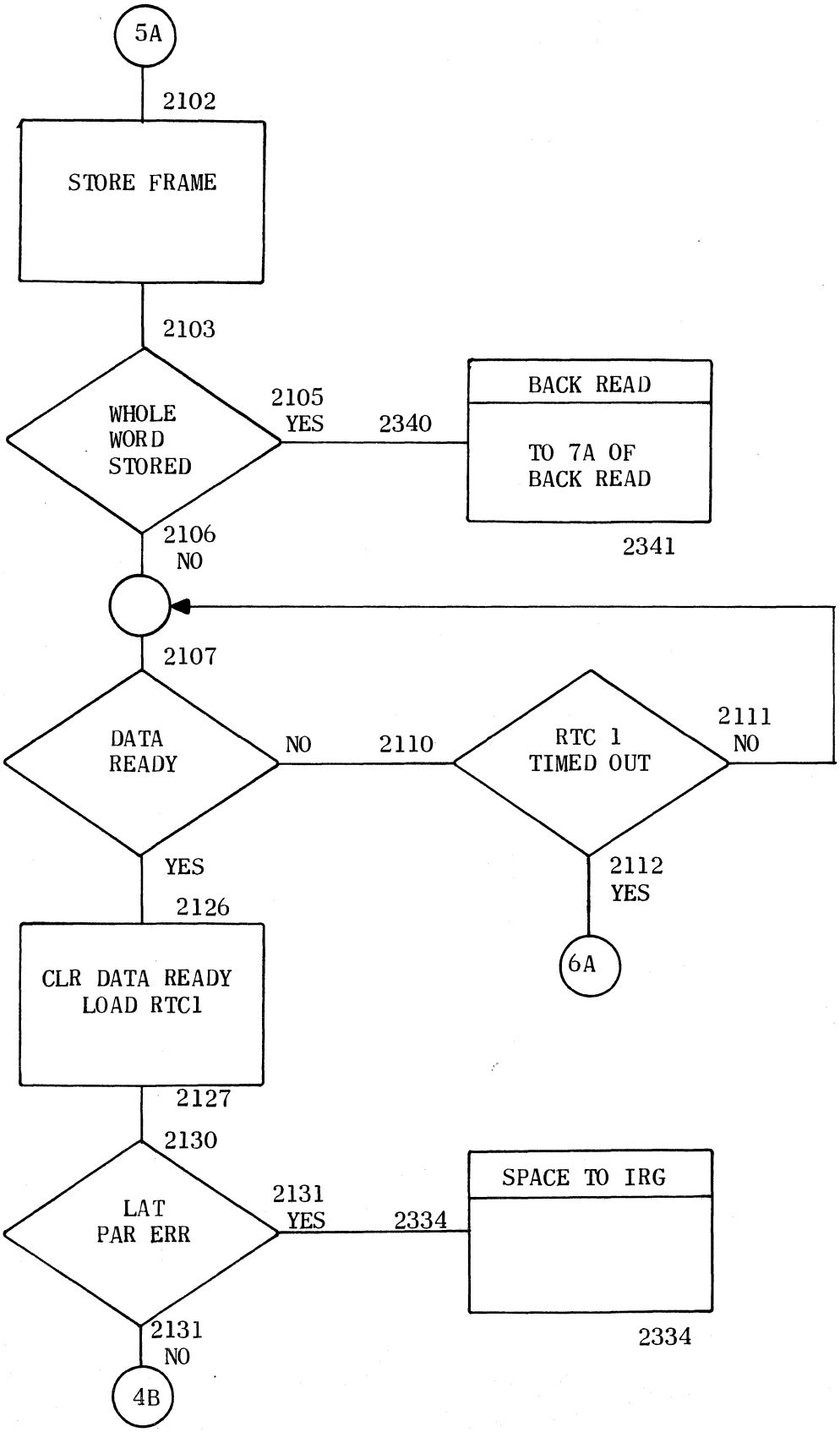


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 5 of 8)

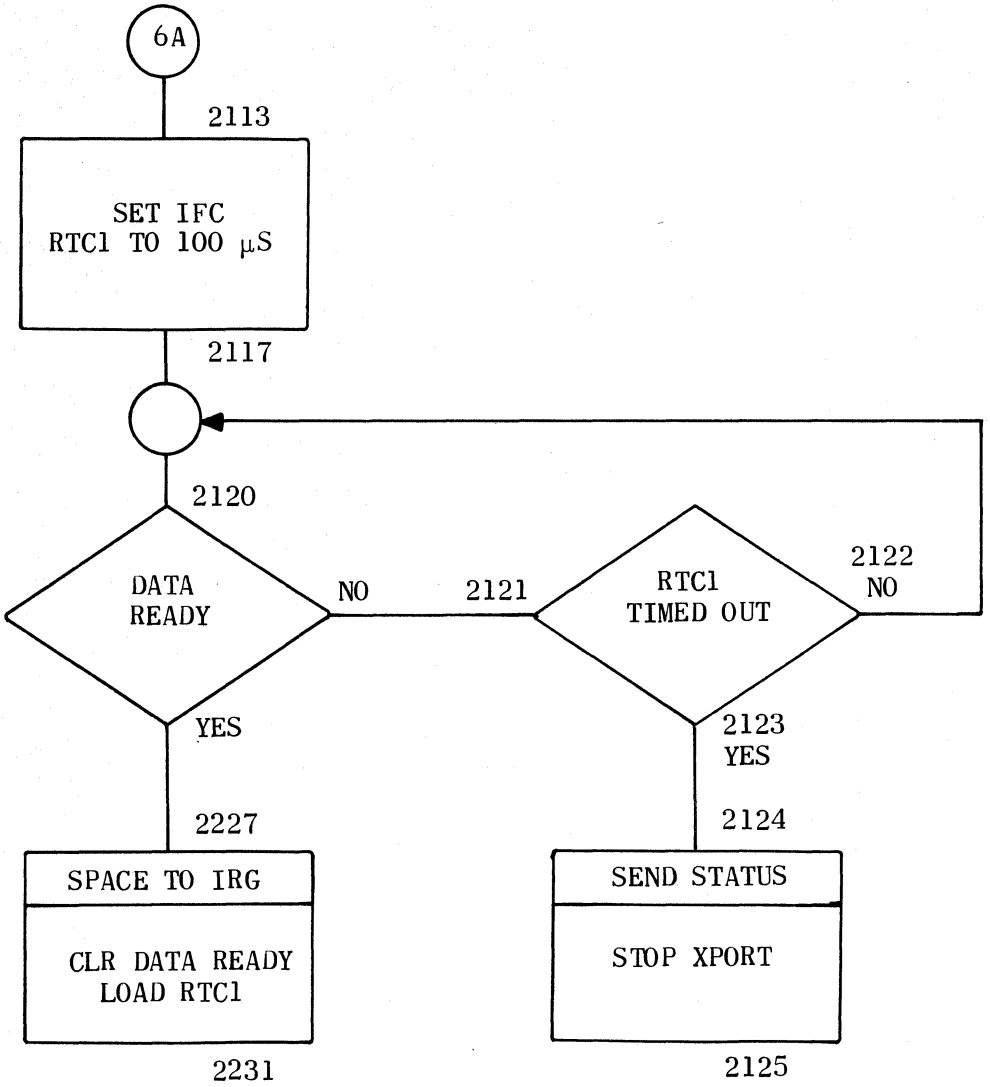


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 6 of 8)

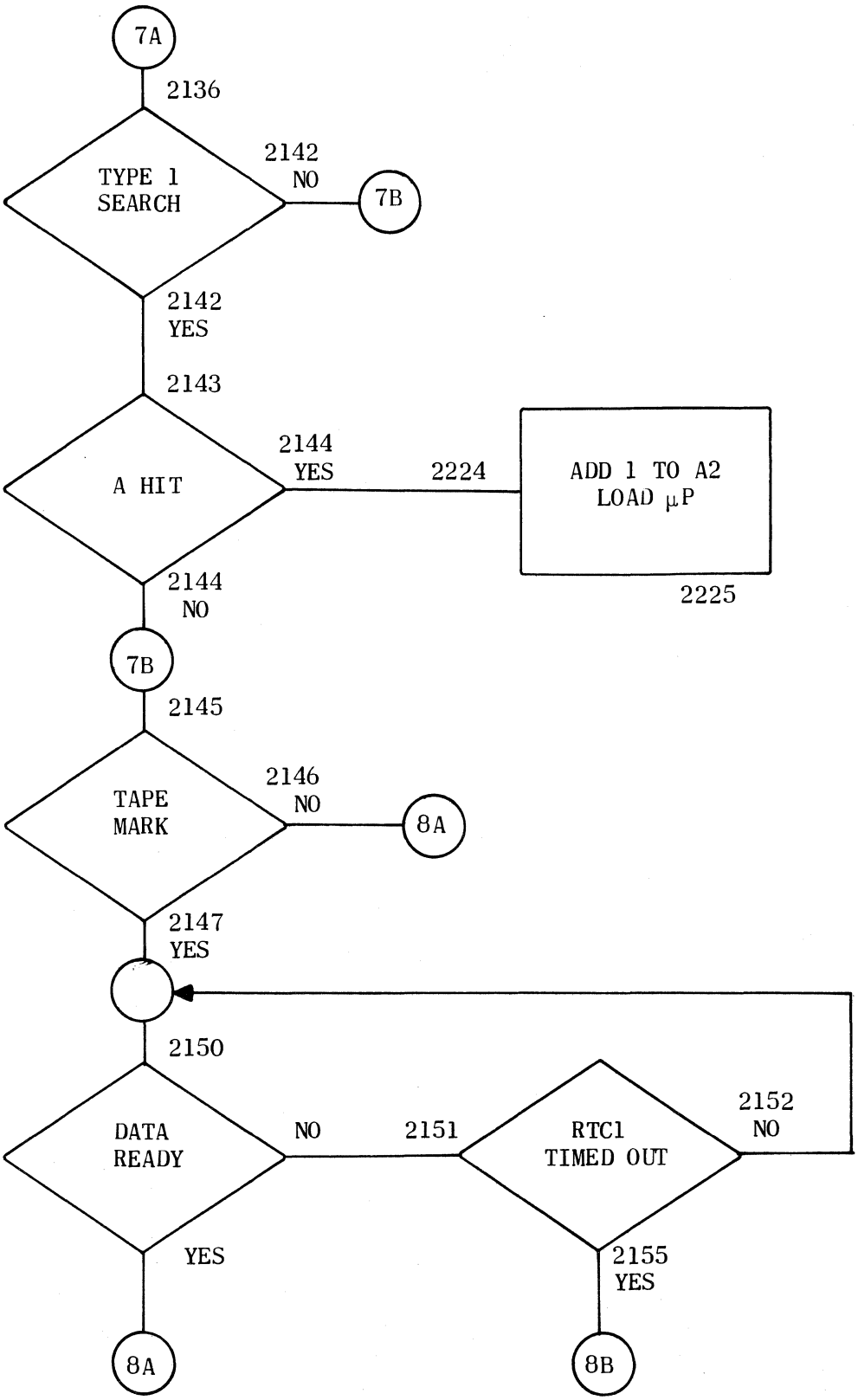


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 7 of 8)

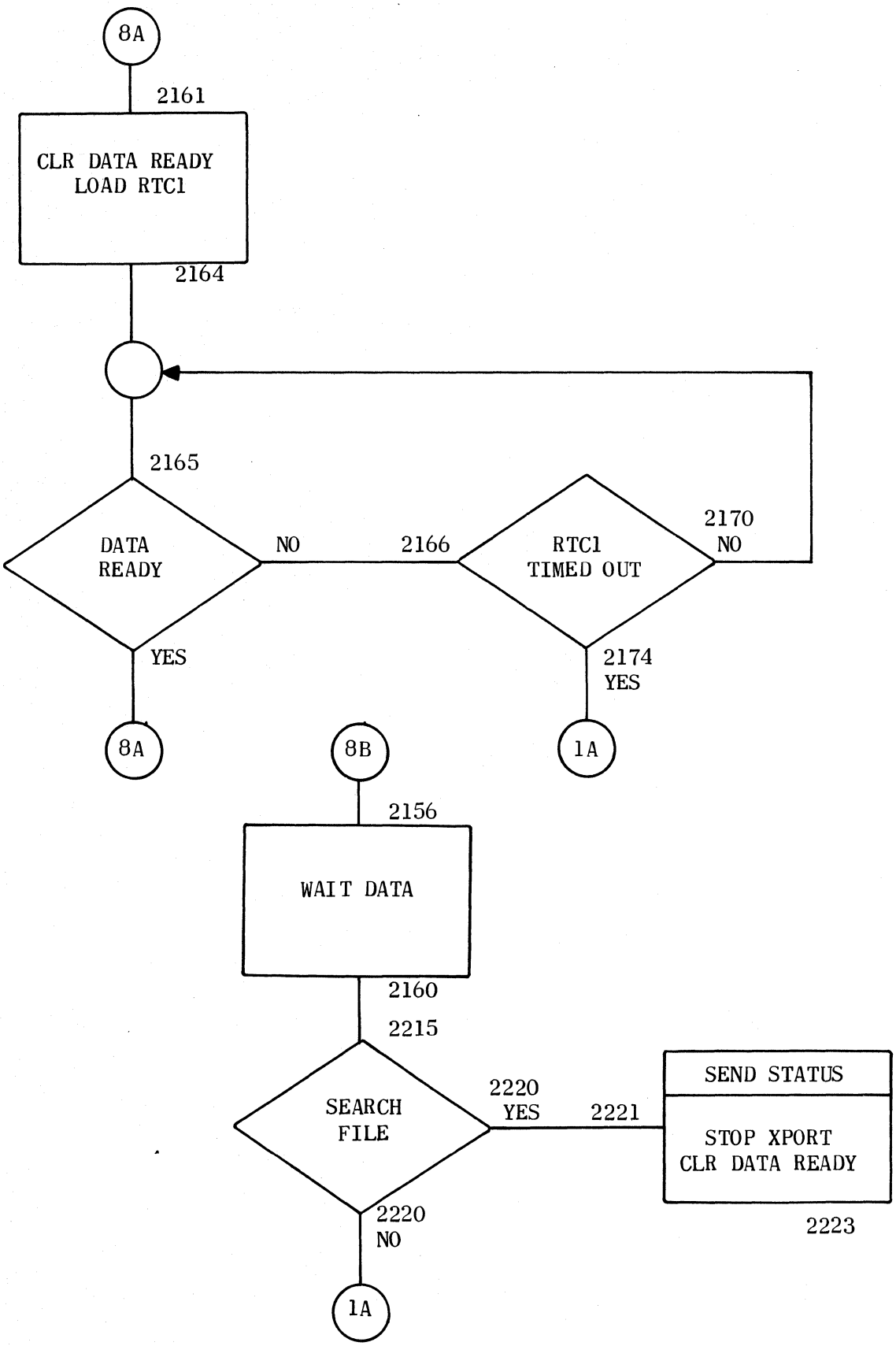


Figure 4-60. Back Search Sequence Flow Diagram (Sheet 8 of 8)

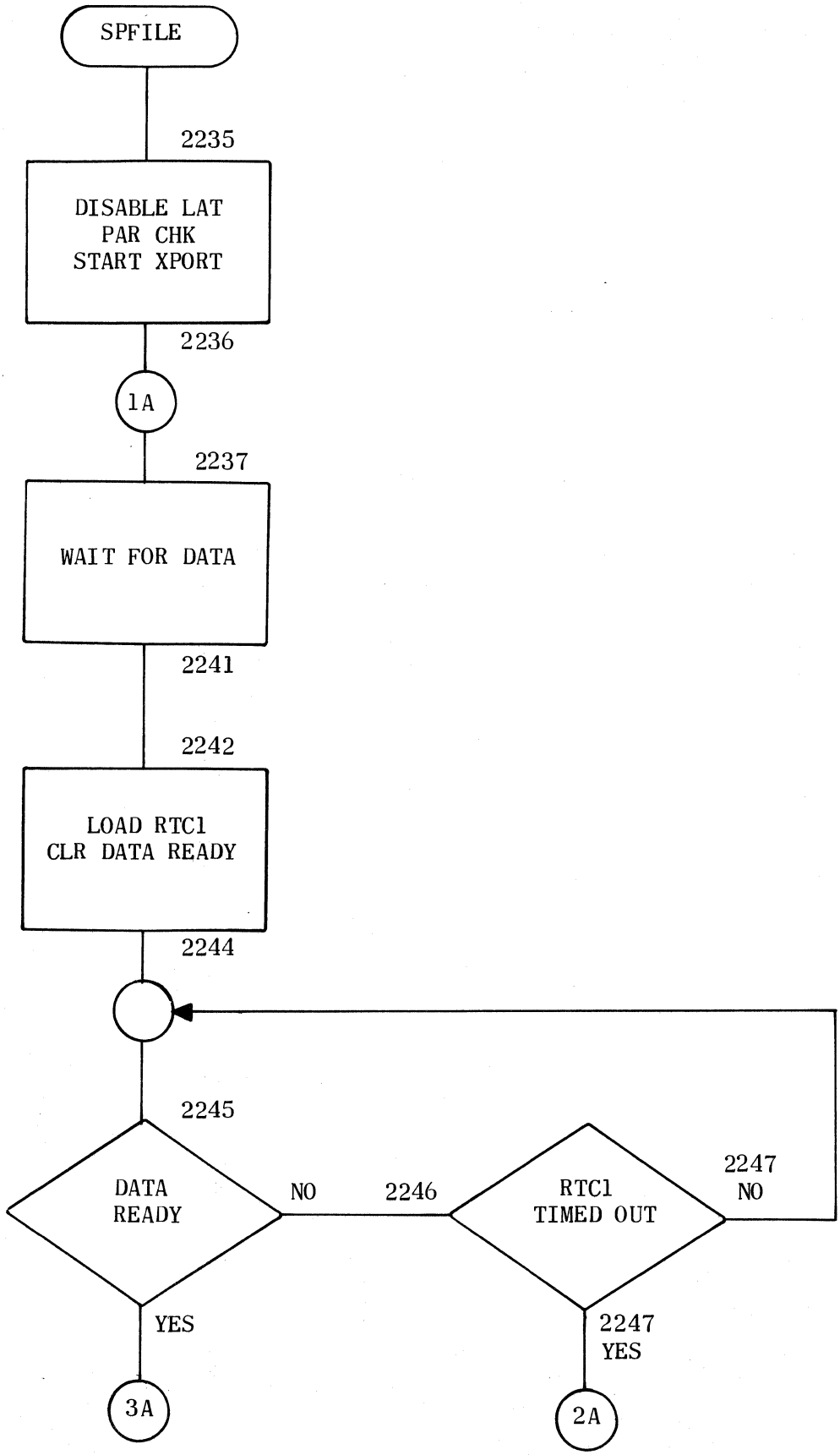


Figure 4-61. Space File Sequence Flow Diagram (Sheet 1 of 3)

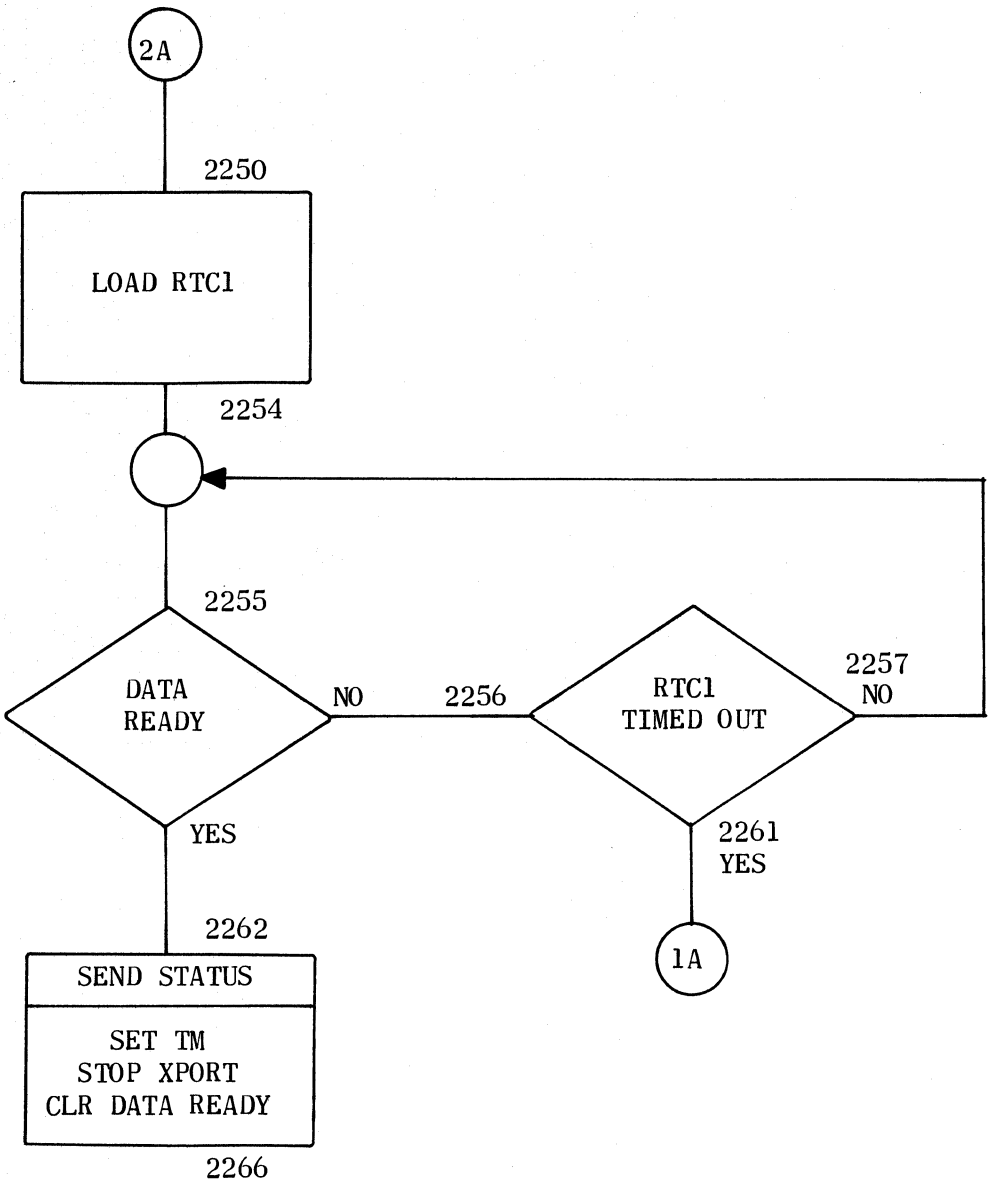


Figure 4-61. Space File Sequence Flow Diagram (Sheet 2 of 3)

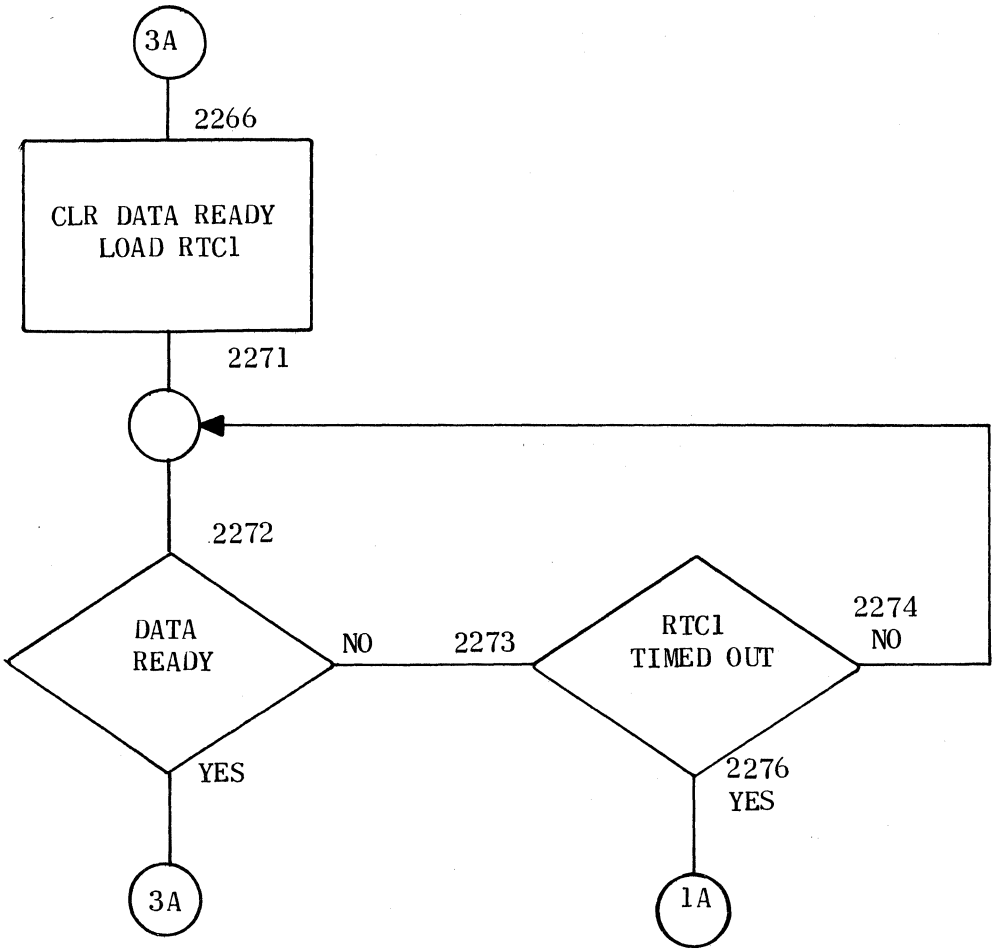


Figure 4-61. Space File Sequence Flow Diagram (Sheet 3 of 3)

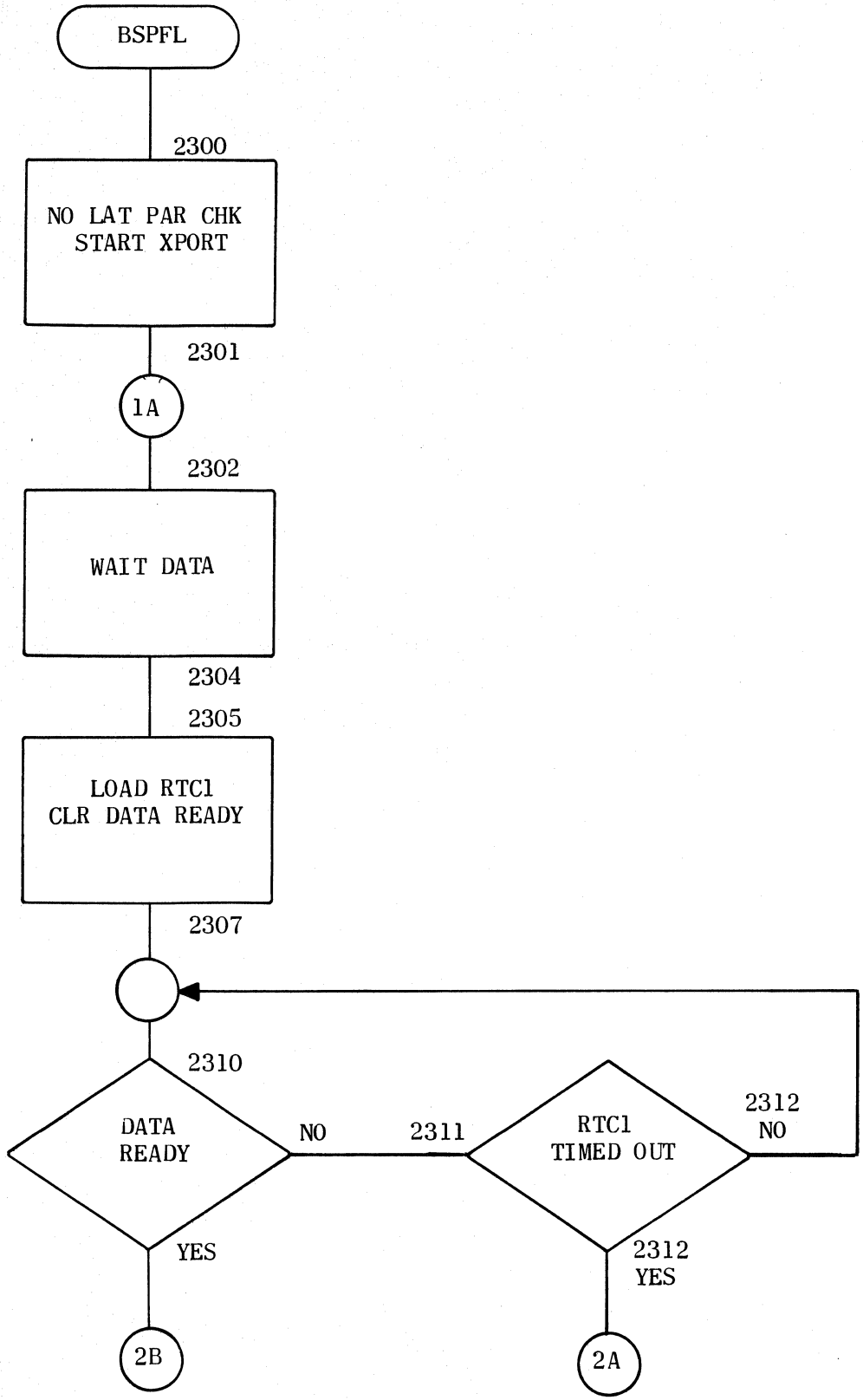


Figure 4-62. Backspace File Sequence Flow Diagram (Sheet 1 of 3)

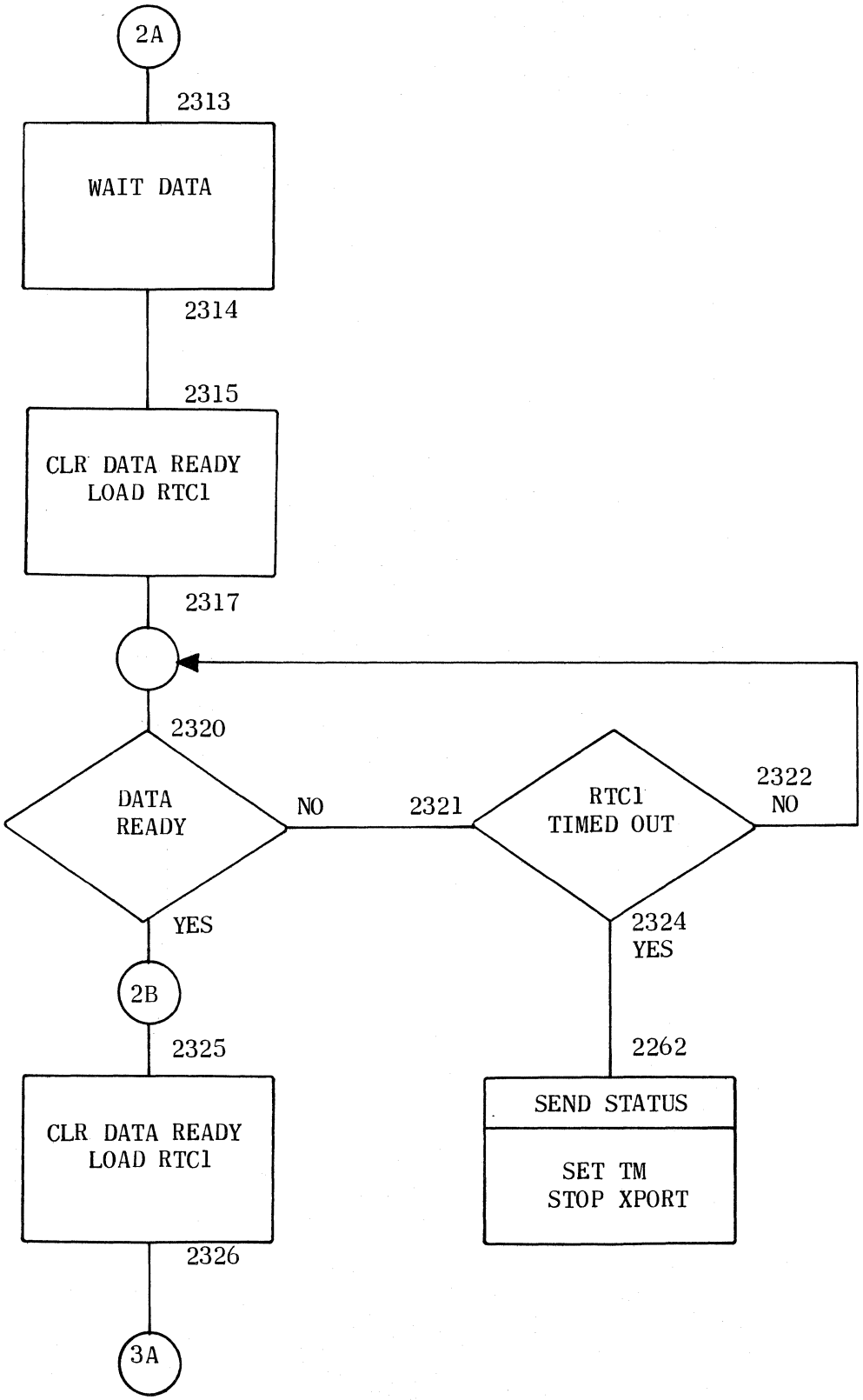


Figure 4-62. Backspace File Sequence Flow Diagram (Sheet 2 of 3)

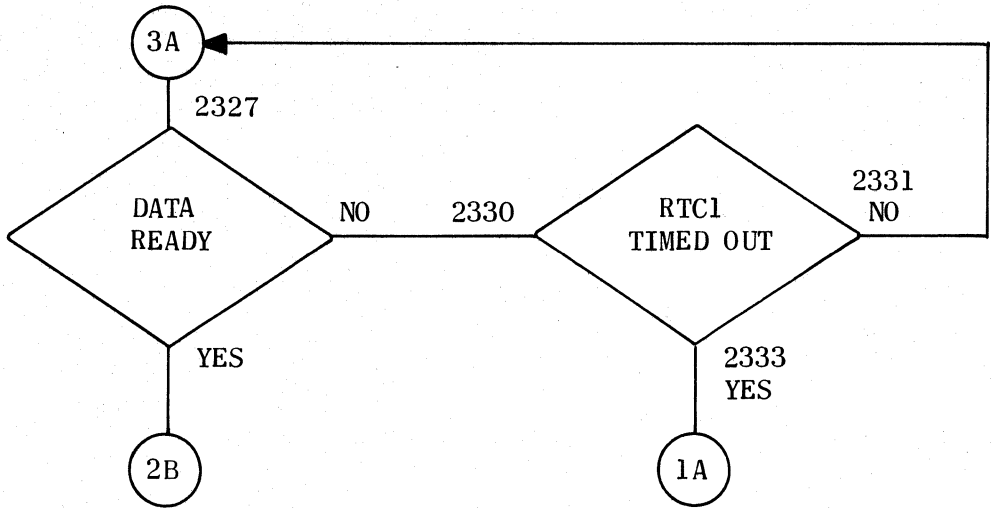


Figure 4-62. Backspace File Sequence Flow Diagram (Sheet 3 of 3)

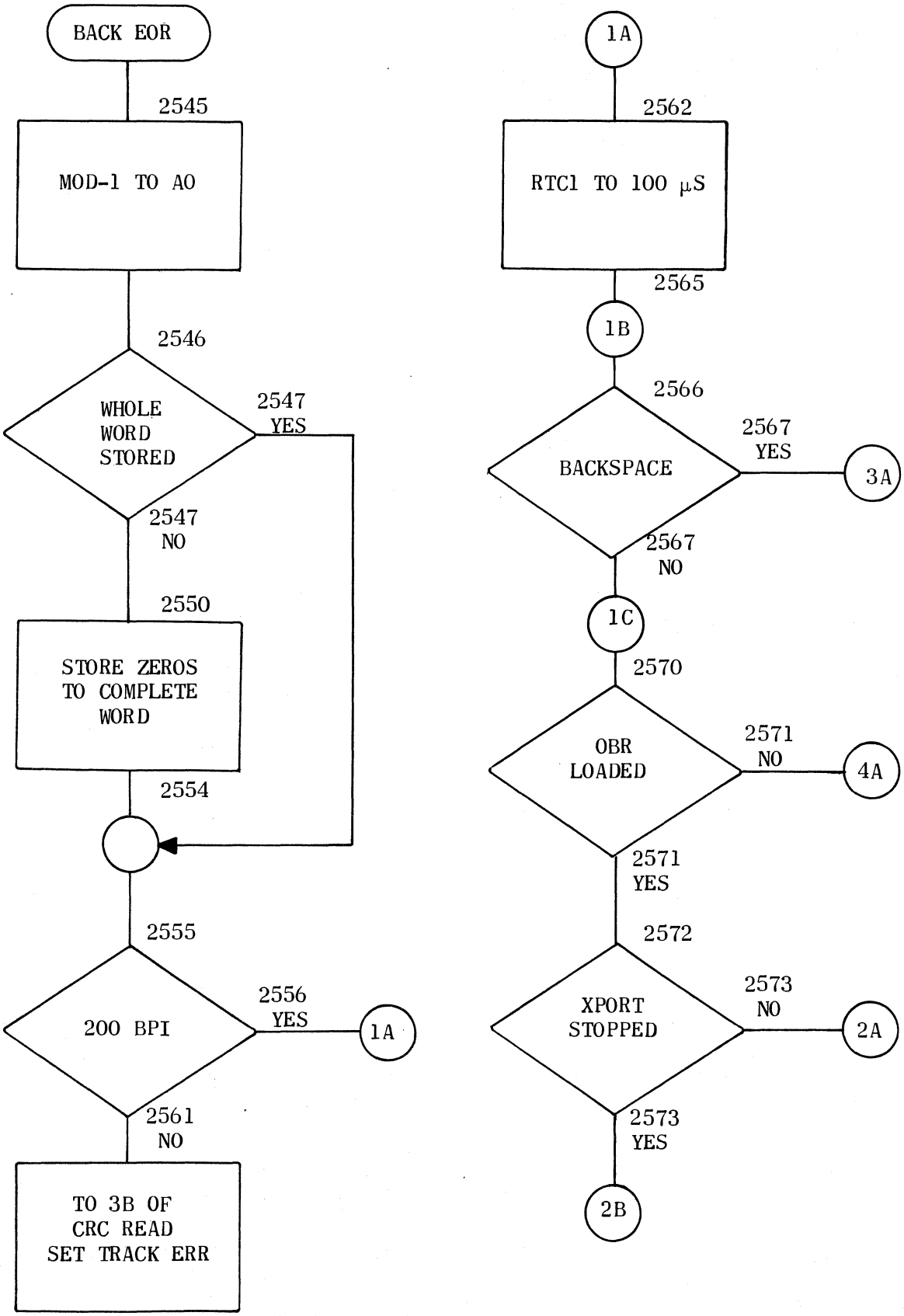


Figure 4-63. Back End of Record Sequence Flow Diagram (Sheet 1 of 6)

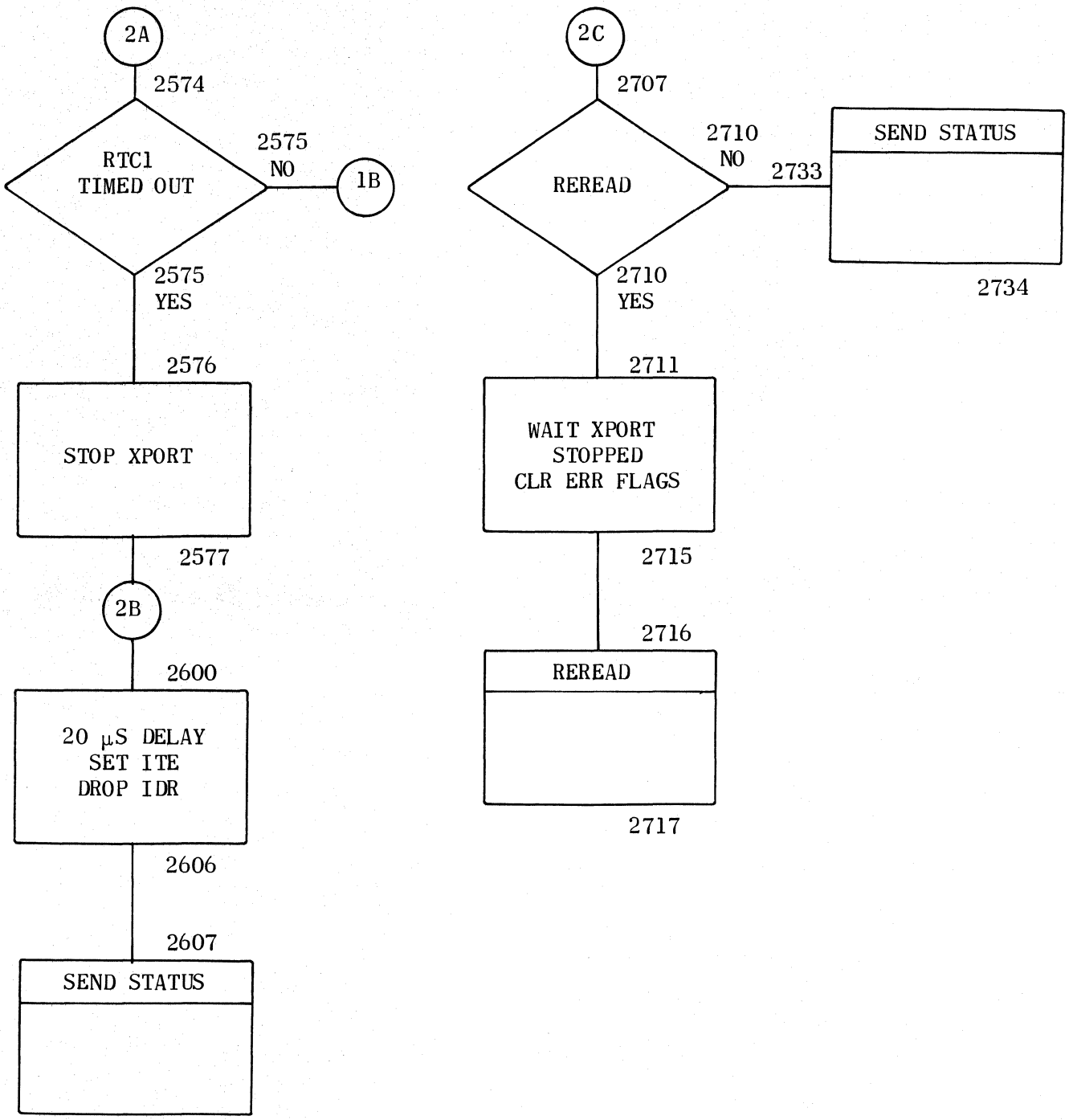


Figure 4-63. Back End of Record Sequence Flow Diagram (Sheet 2 of 6)

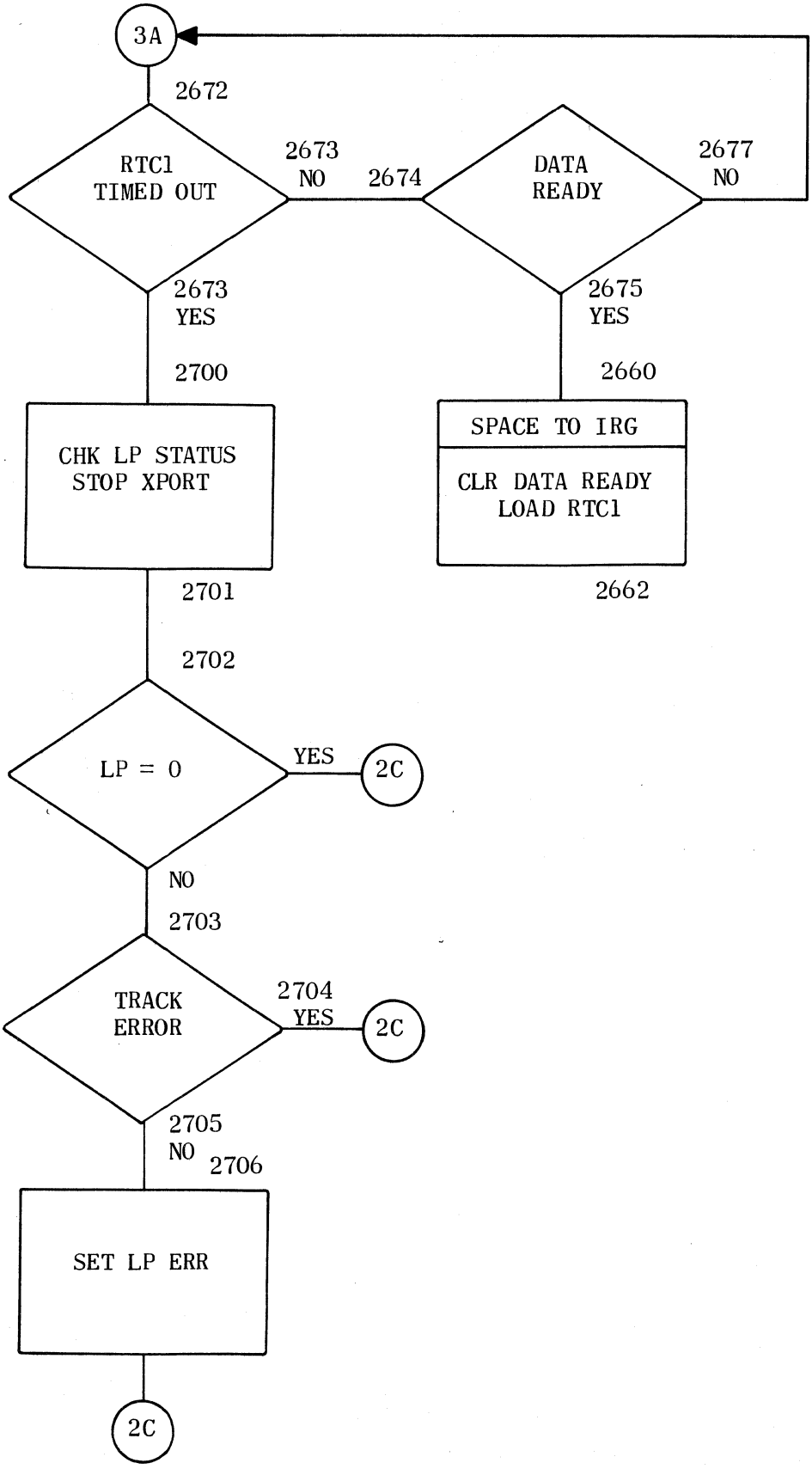


Figure 4-63. Back End of Record Sequence Flow Diagram (Sheet 3 of 6)

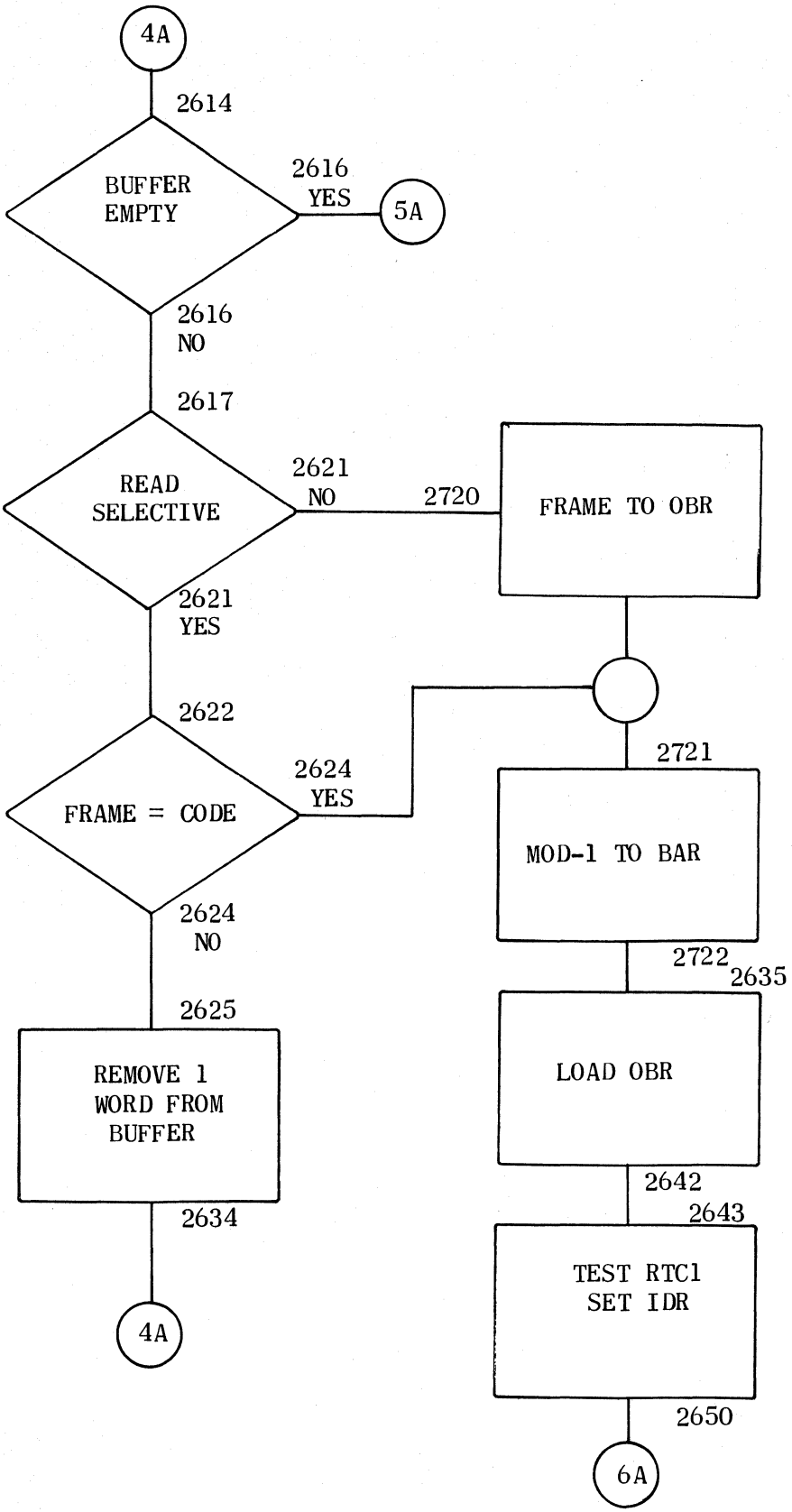


Figure 4-63. Back End of Record Sequence Flow Diagram (Sheet 4 of 6)

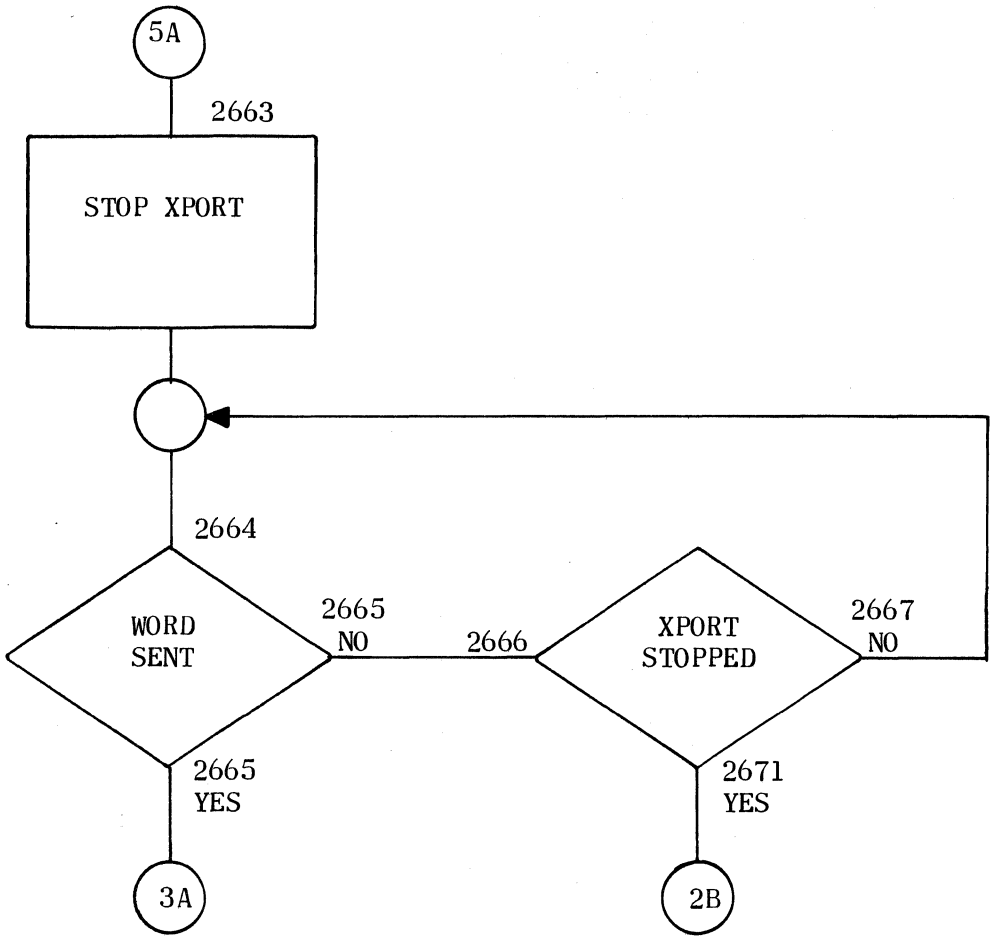


Figure 4-63. Back End of Record Sequence Flow Diagram (Sheet 5 of 6)

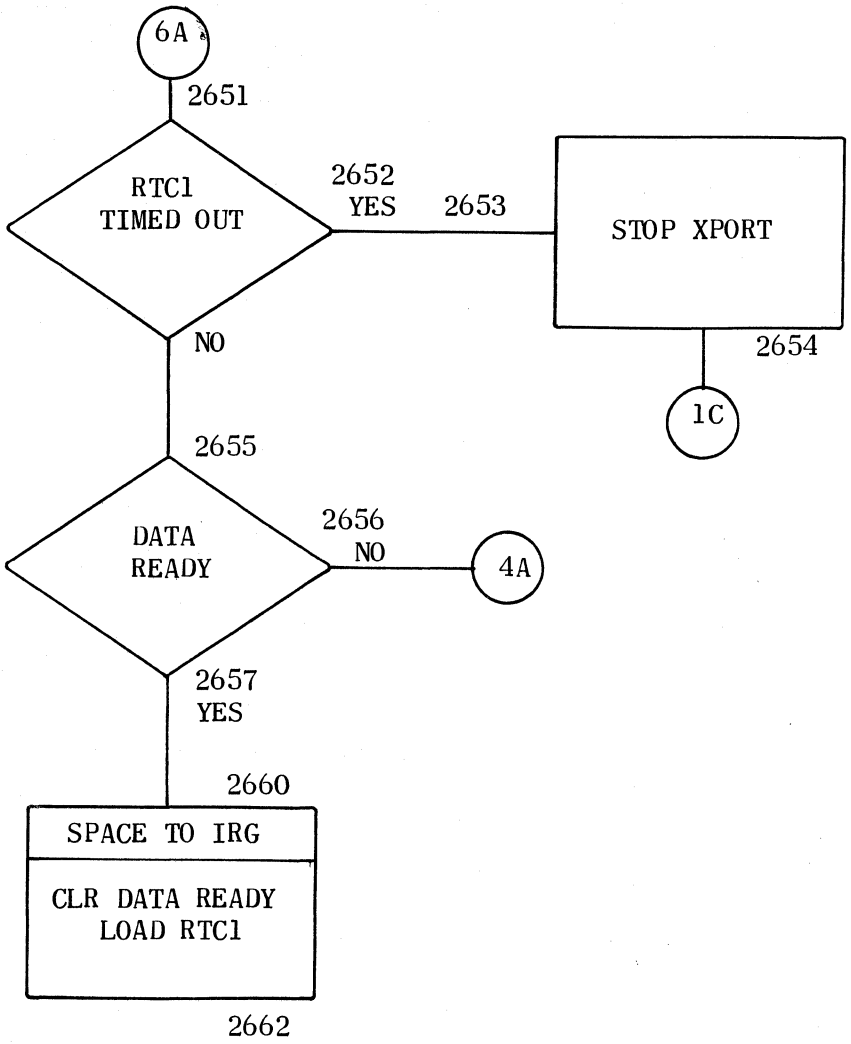


Figure 4-63. Back End of Record Sequence Flow Diagram (Sheet 6 of 6)

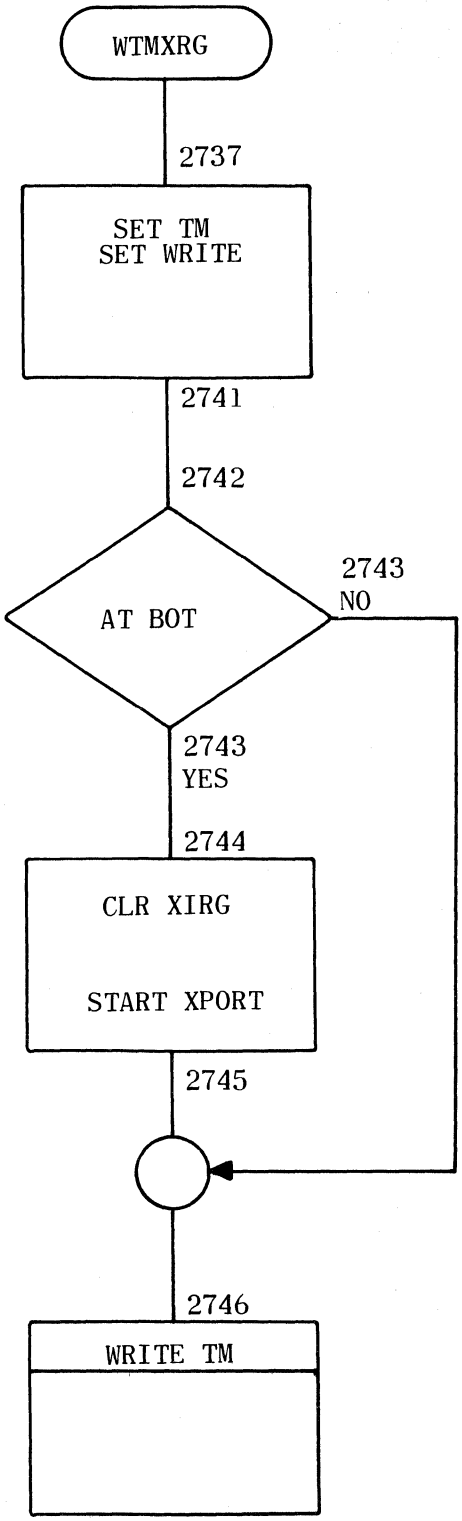


Figure 4-64. Write Tape Mark XIRG Sequence Flow Diagram

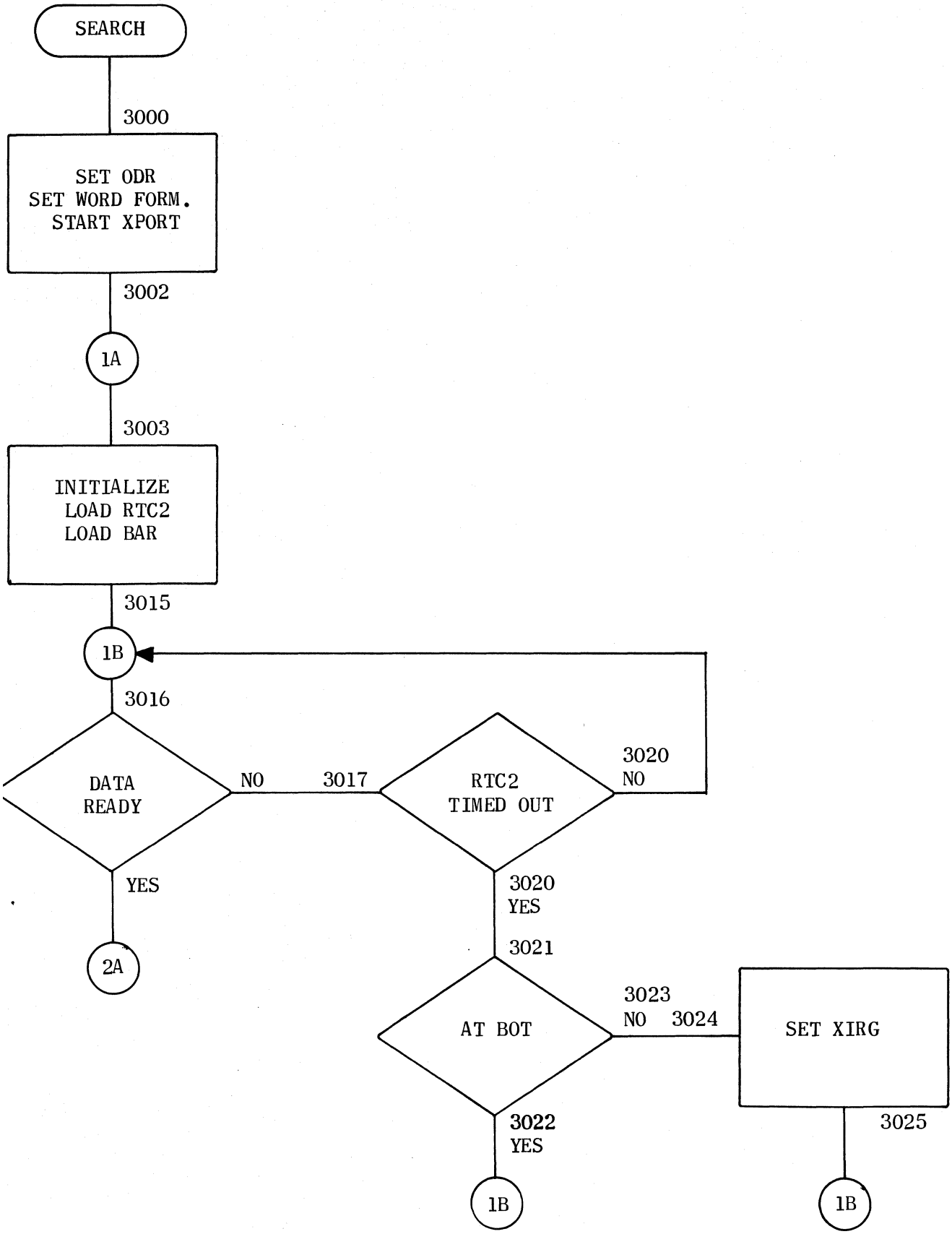


Figure 4-65. Search Sequence Flow Diagram (Sheet 1 of 6)

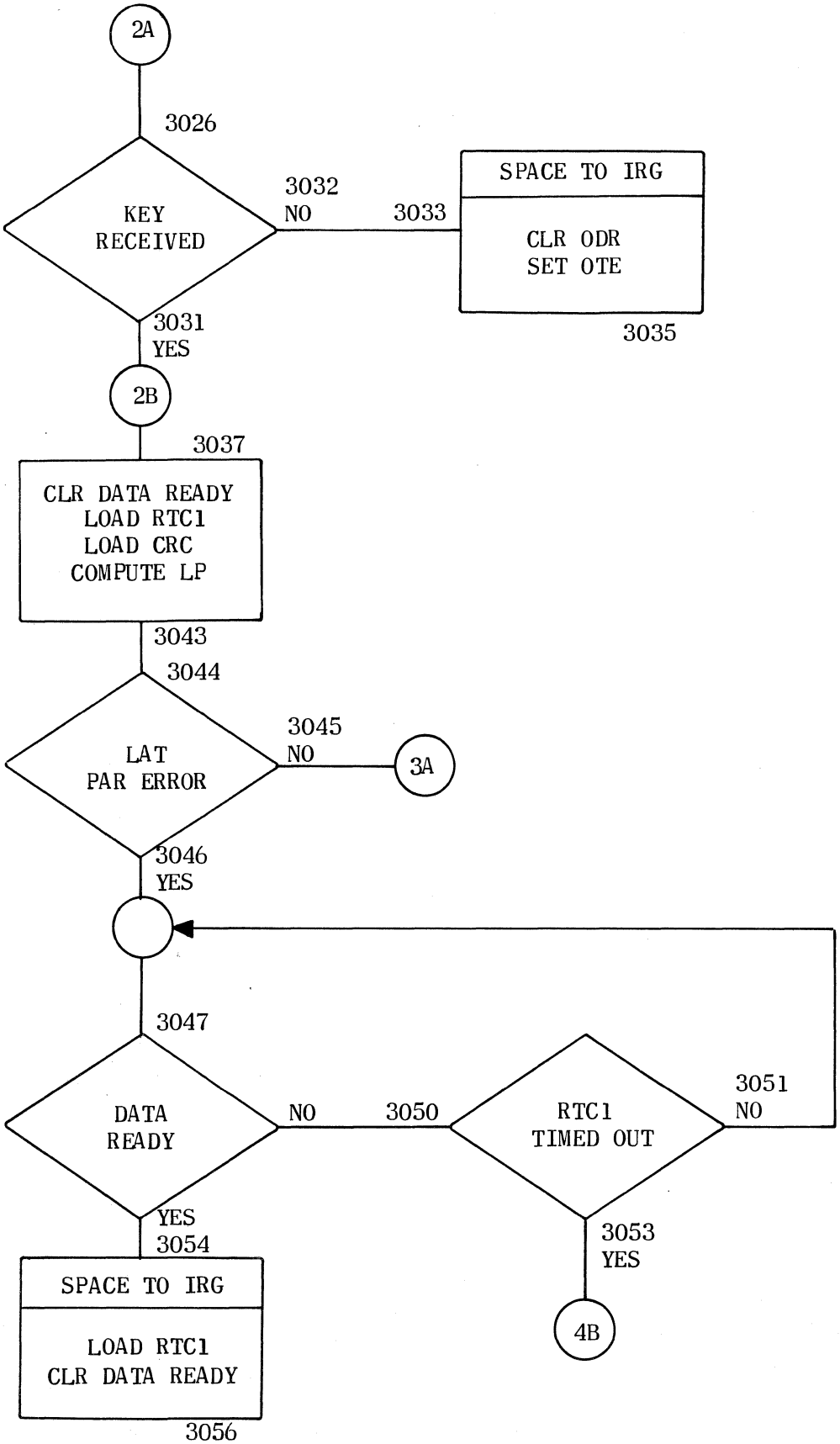


Figure 4-65. Search Sequence Flow Diagram (Sheet 2 of 6)

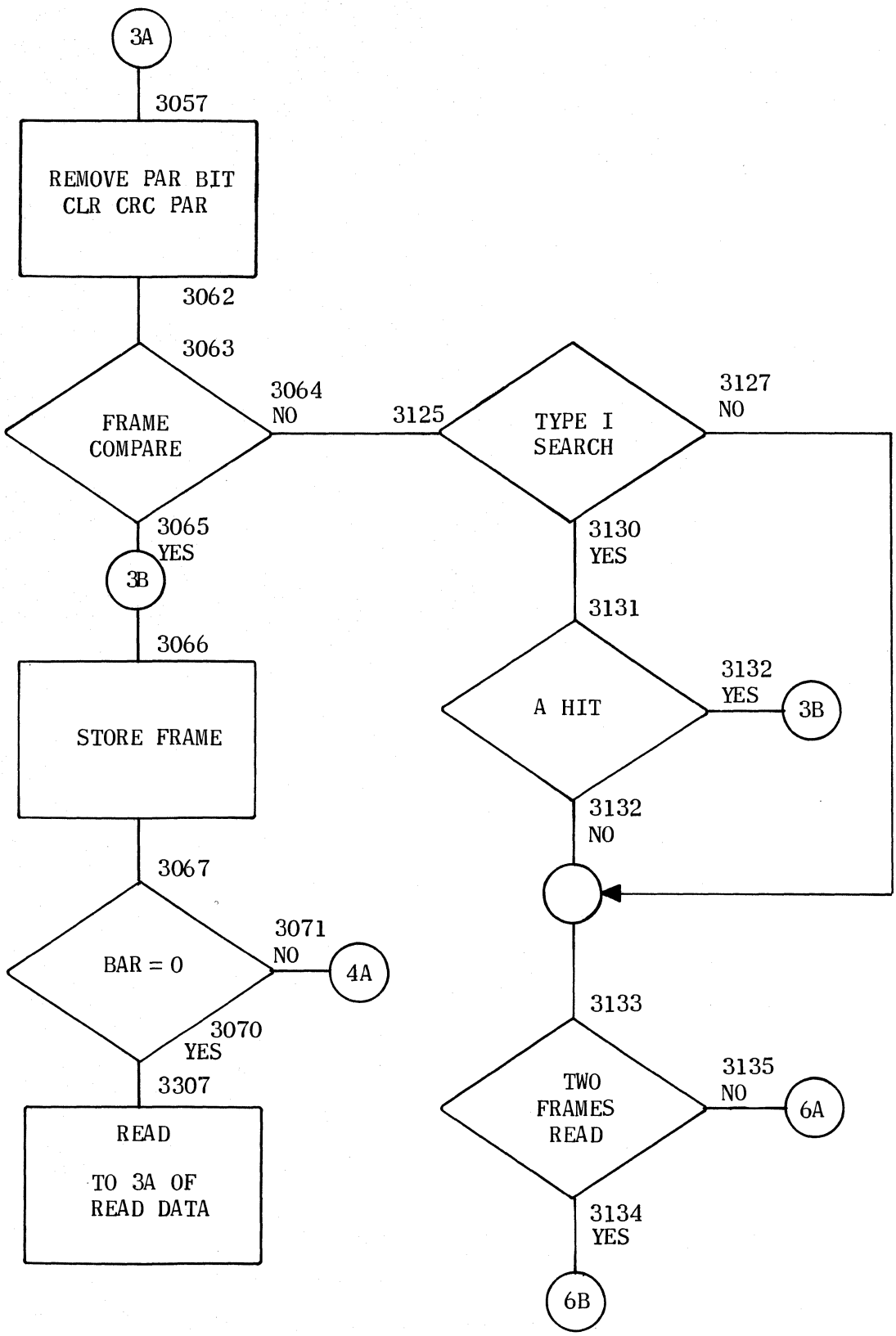


Figure 4-65. Search Sequence Flow Diagram (Sheet 3 of 6)

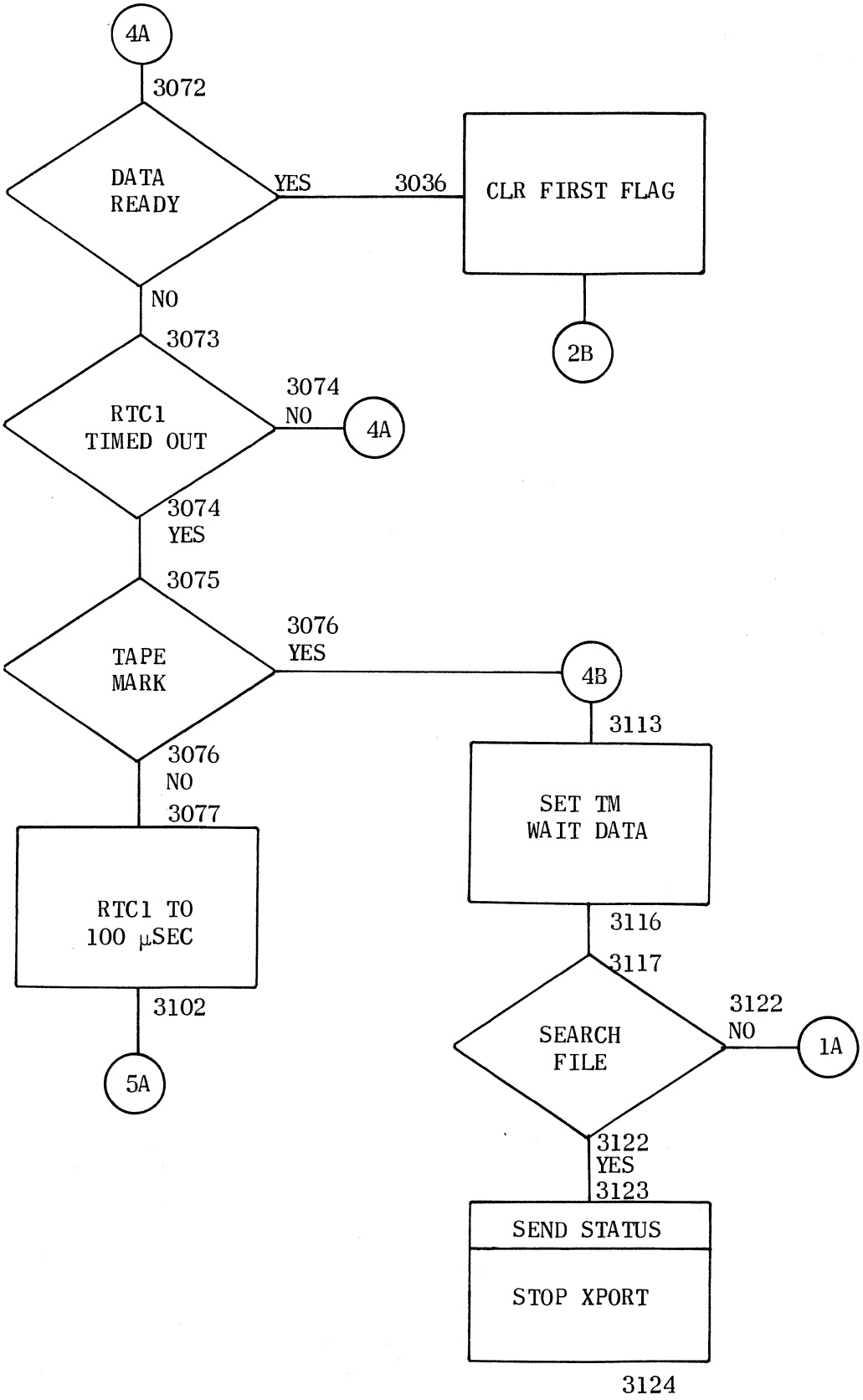


Figure 4-65. Search Sequence Flow Diagram (Sheet 4 of 6)

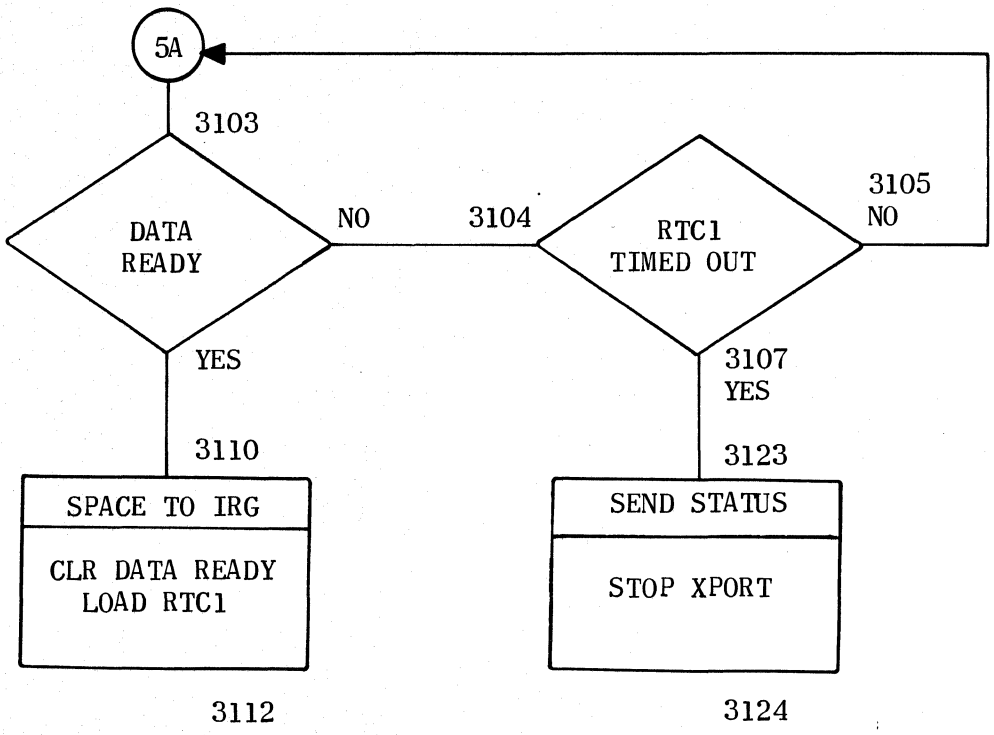


Figure 4-65. Search Sequence Flow Diagram (Sheet 5 of 6)

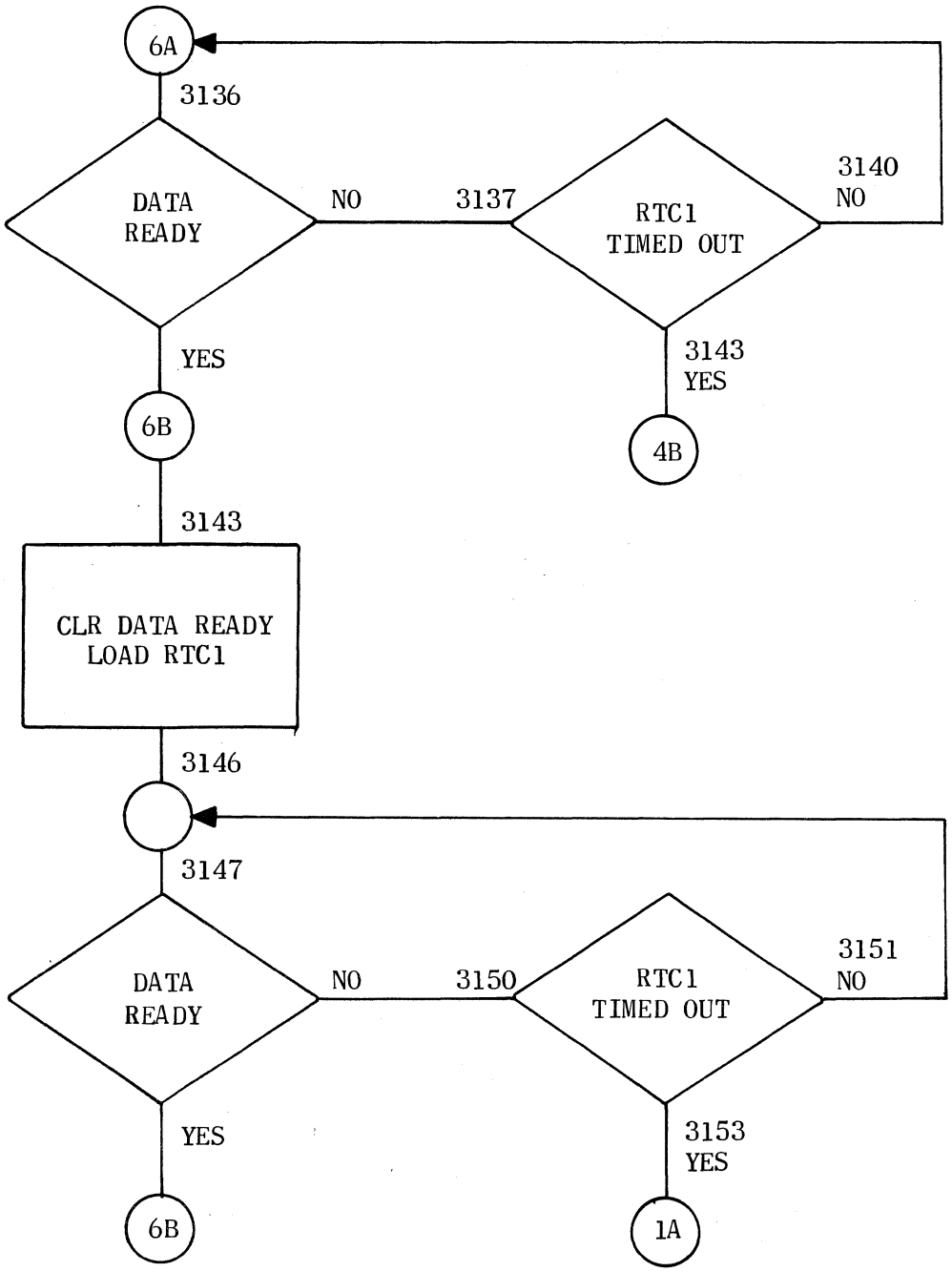


Figure 4-65. Search Sequence Flow Diagram (Sheet 6 of 6)

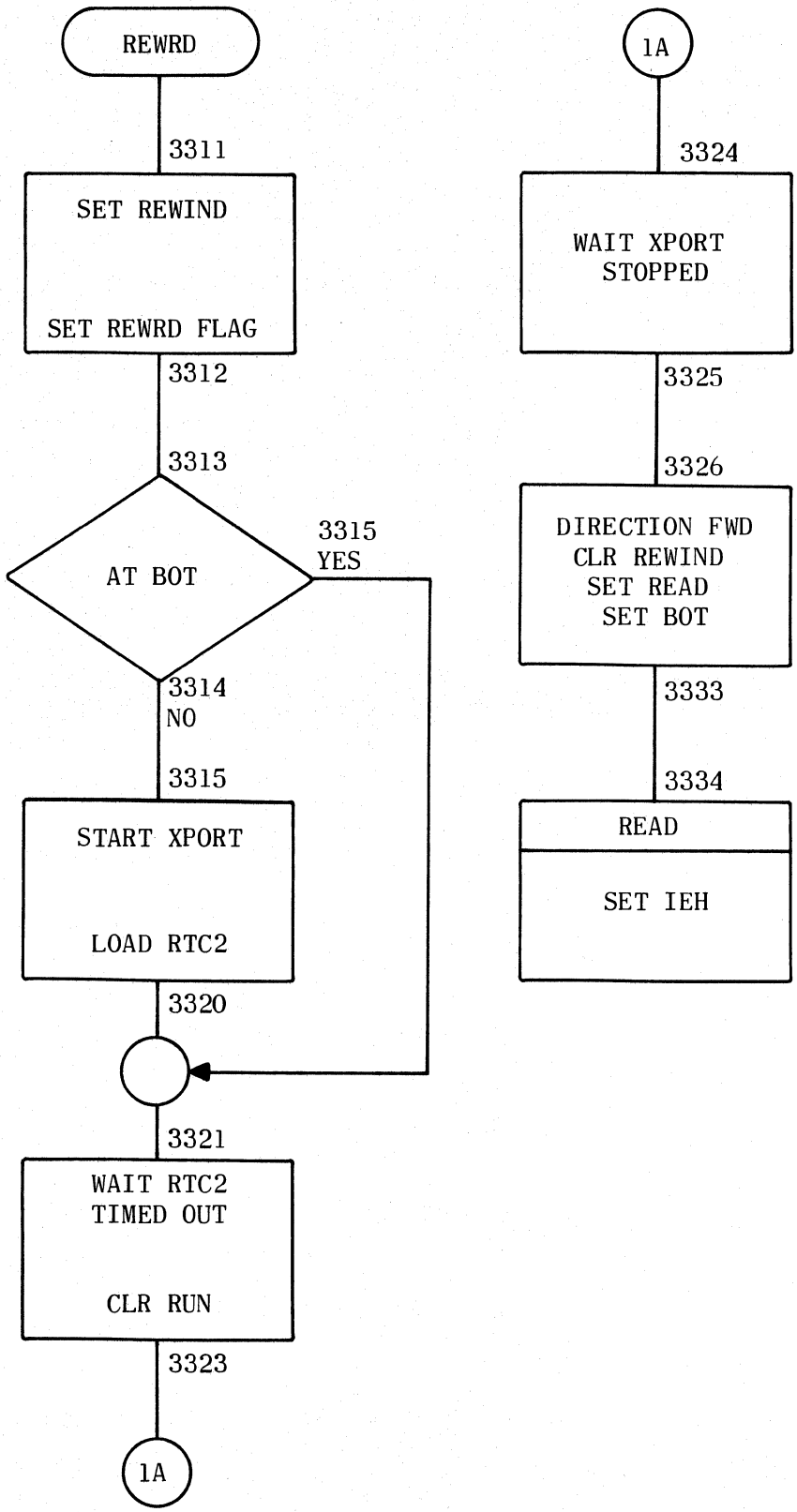


Figure 4-66. Rewind Read Sequence Flow Diagram

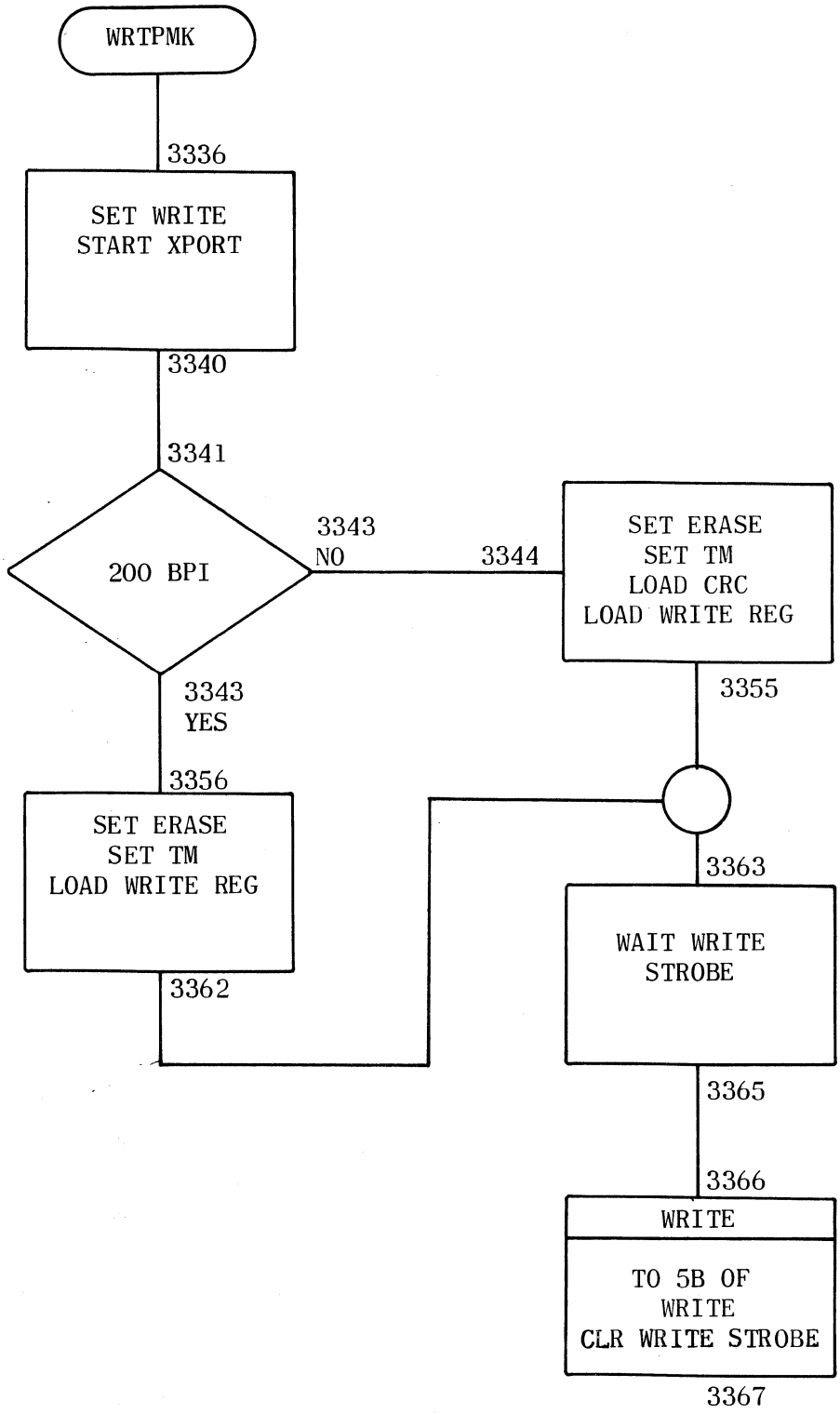


Figure 4-67. Write Tape Mark Sequence Flow Diagram

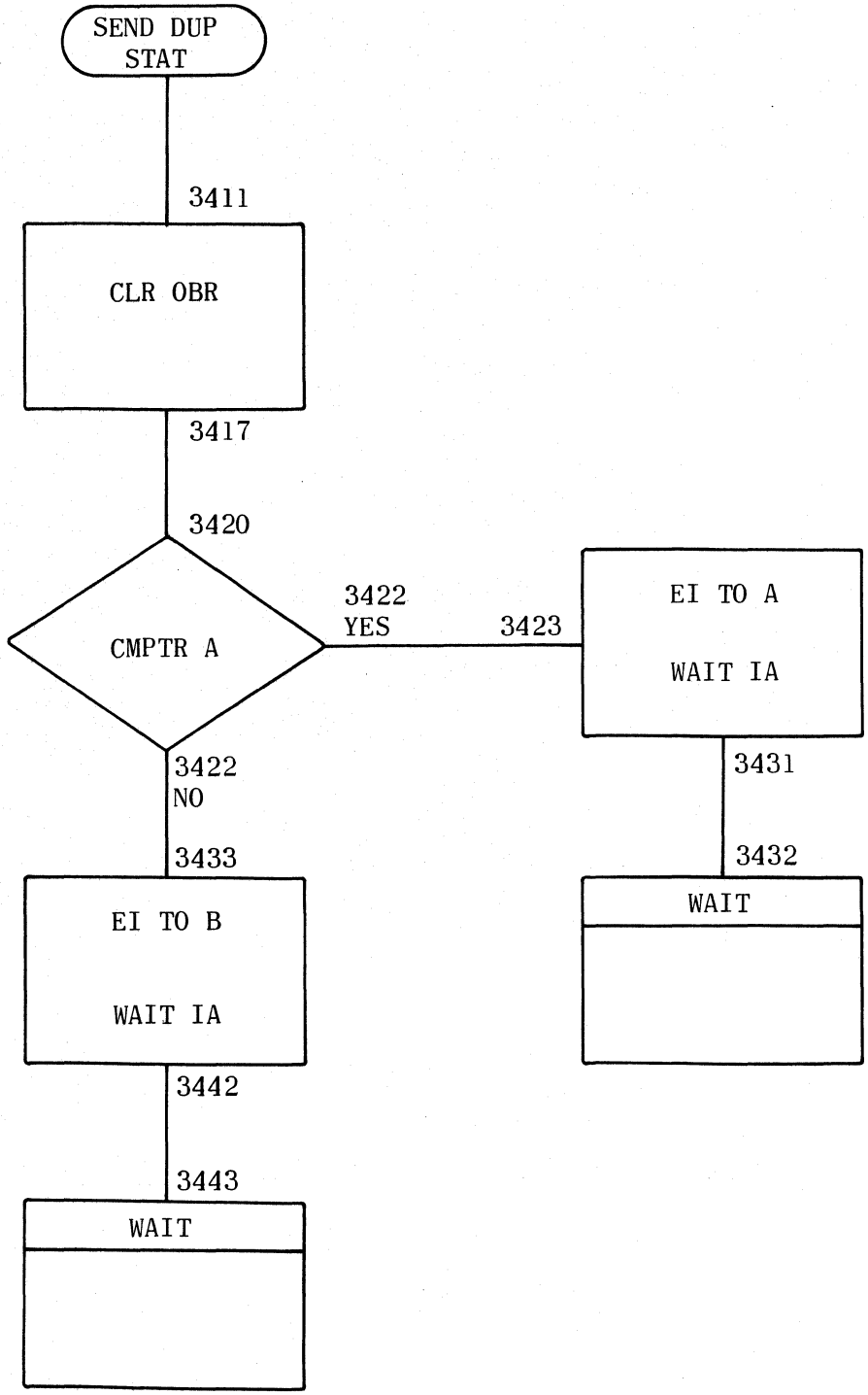


Figure 4-68. Send Duplex Status Sequence Flow Diagram

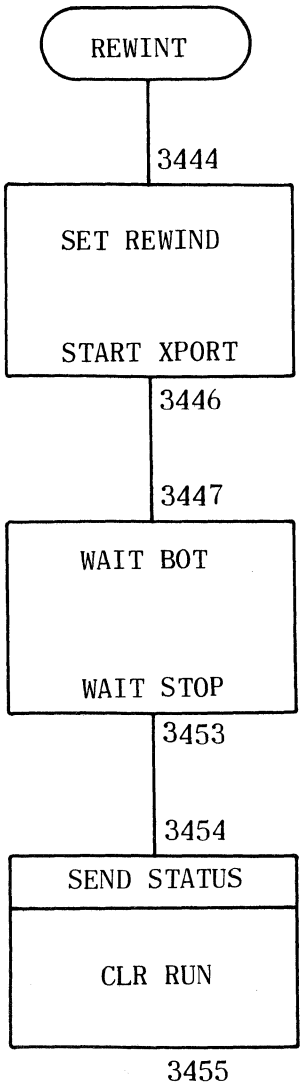


Figure 4-69. Rewind Interrupt at BOT Sequence Flow Diagram

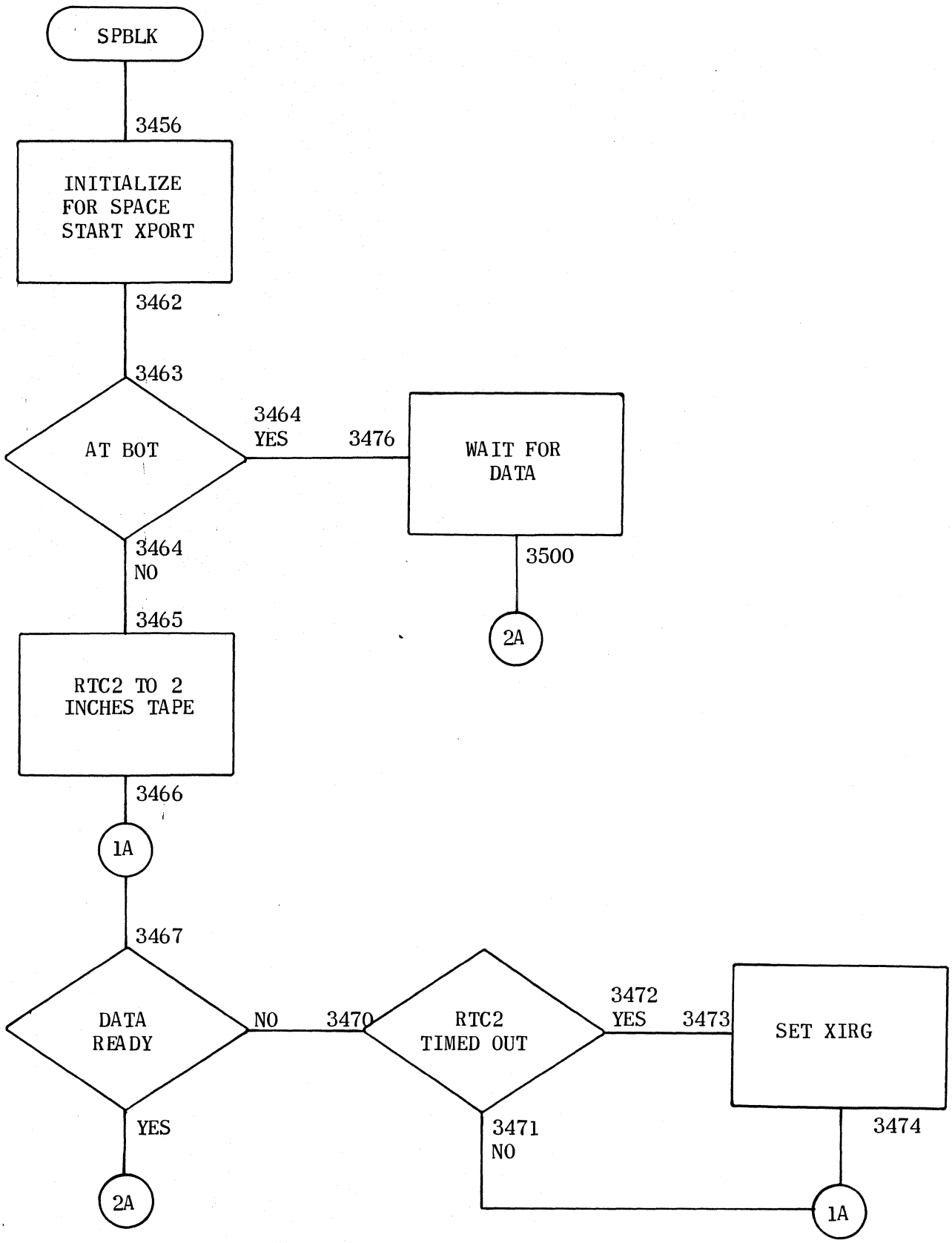


Figure 4-70. Space Block Sequence Flow Diagram (Sheet 1 of 3)

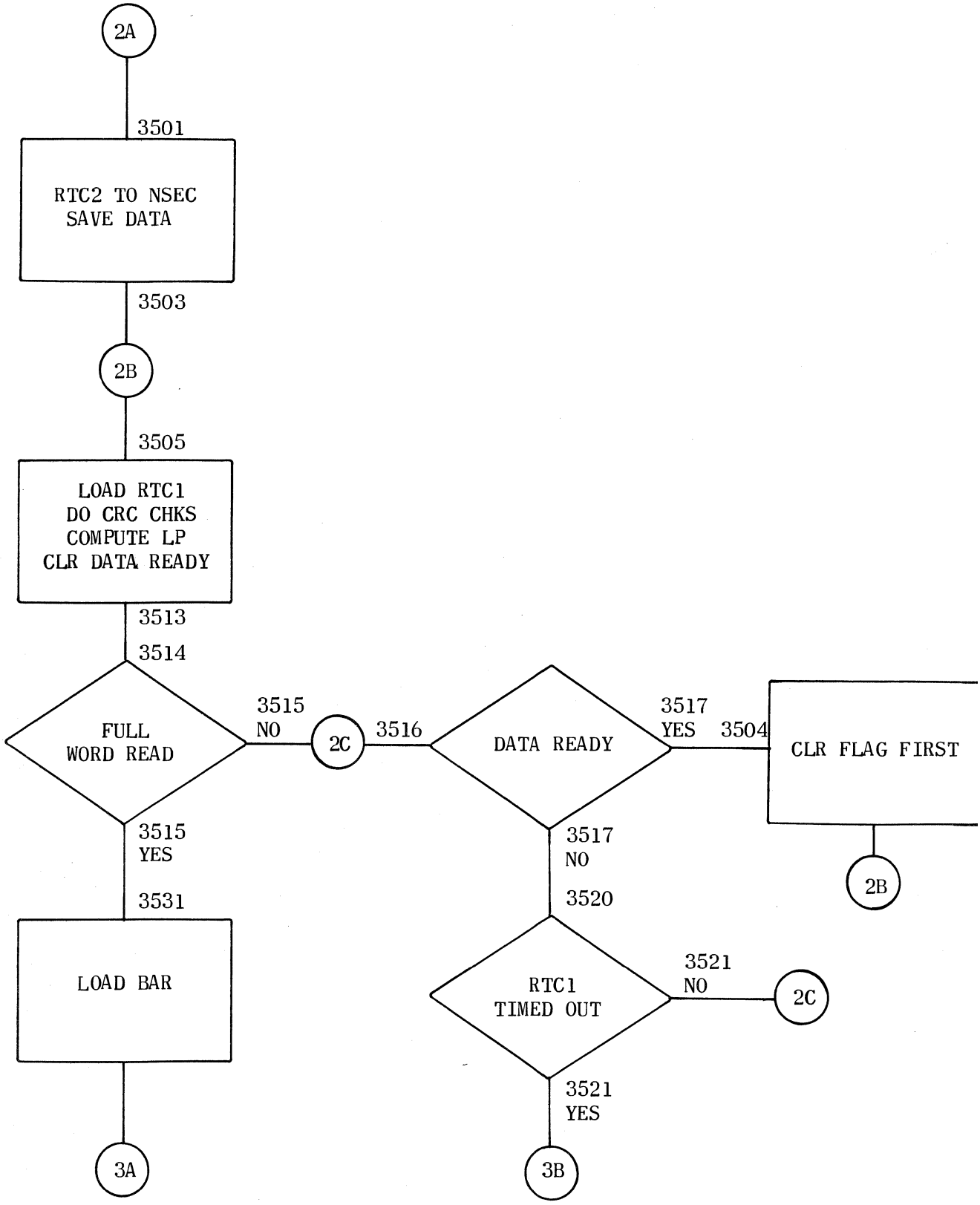


Figure 4-70. Space Block Sequence Flow Diagram (Sheet 2 of 3)

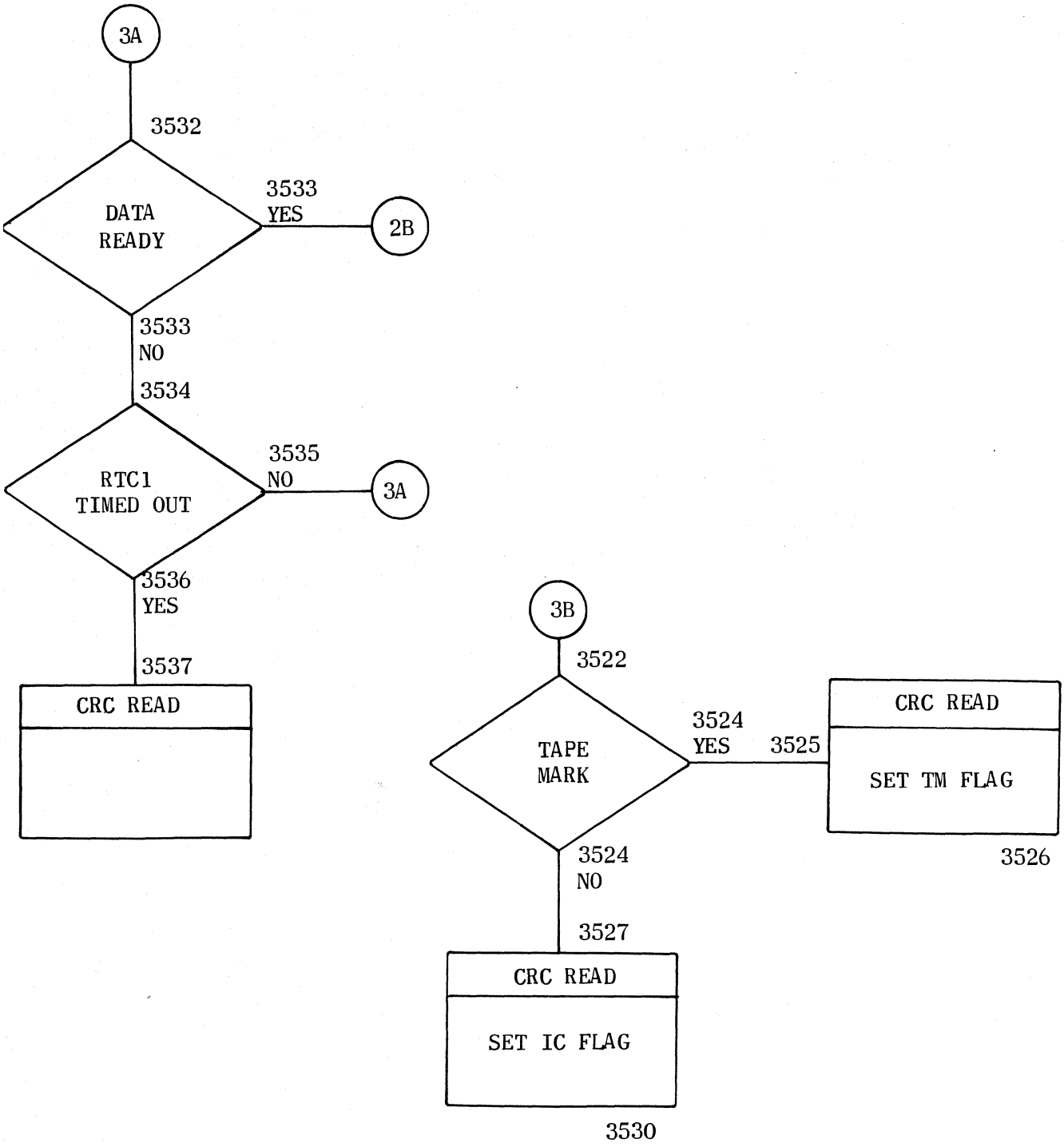


Figure 4-70. Space Block Sequence Flow Diagram (Sheet 3 of 3)

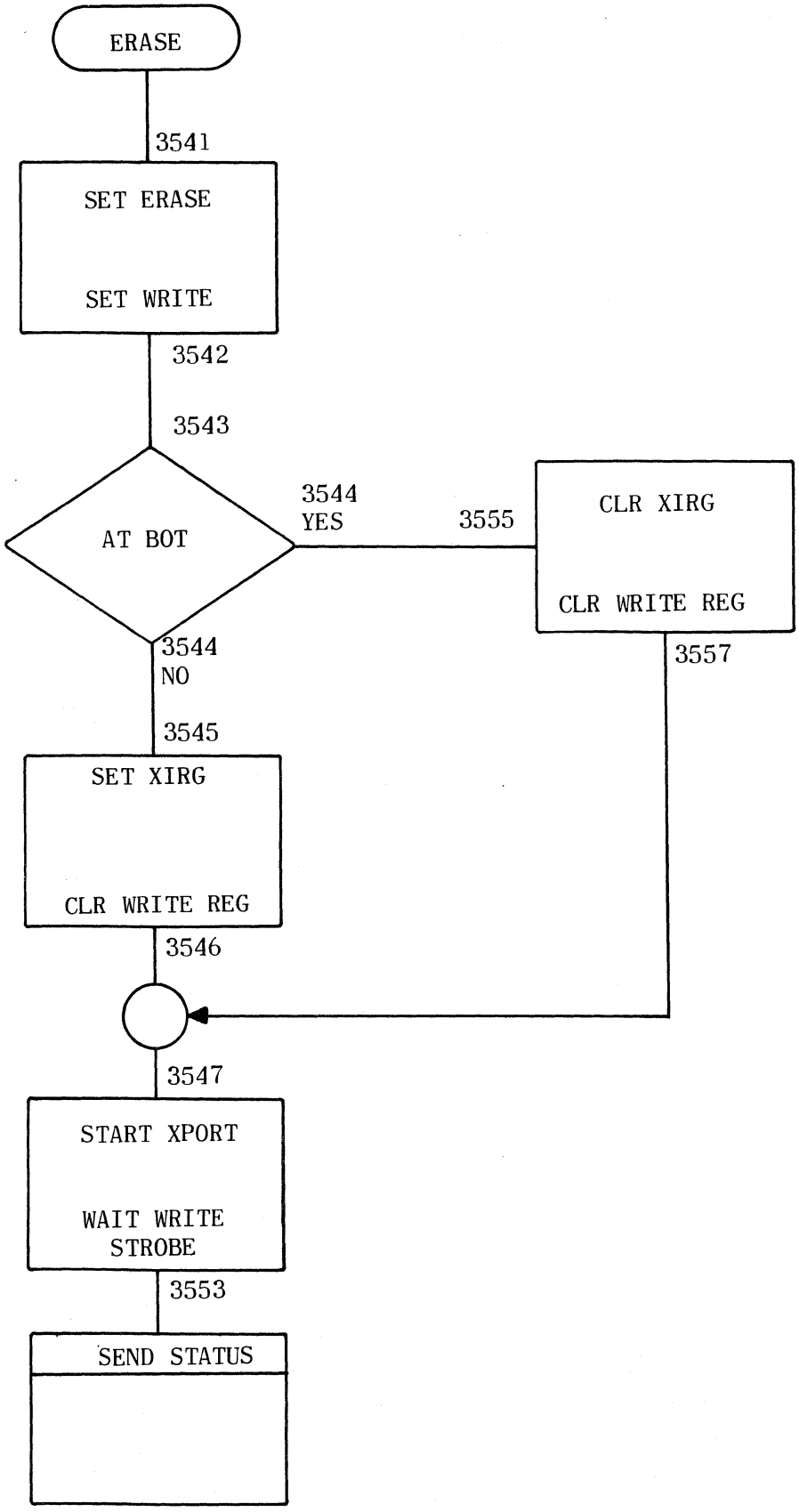


Figure 4-71. Erase Sequence Flow Diagram

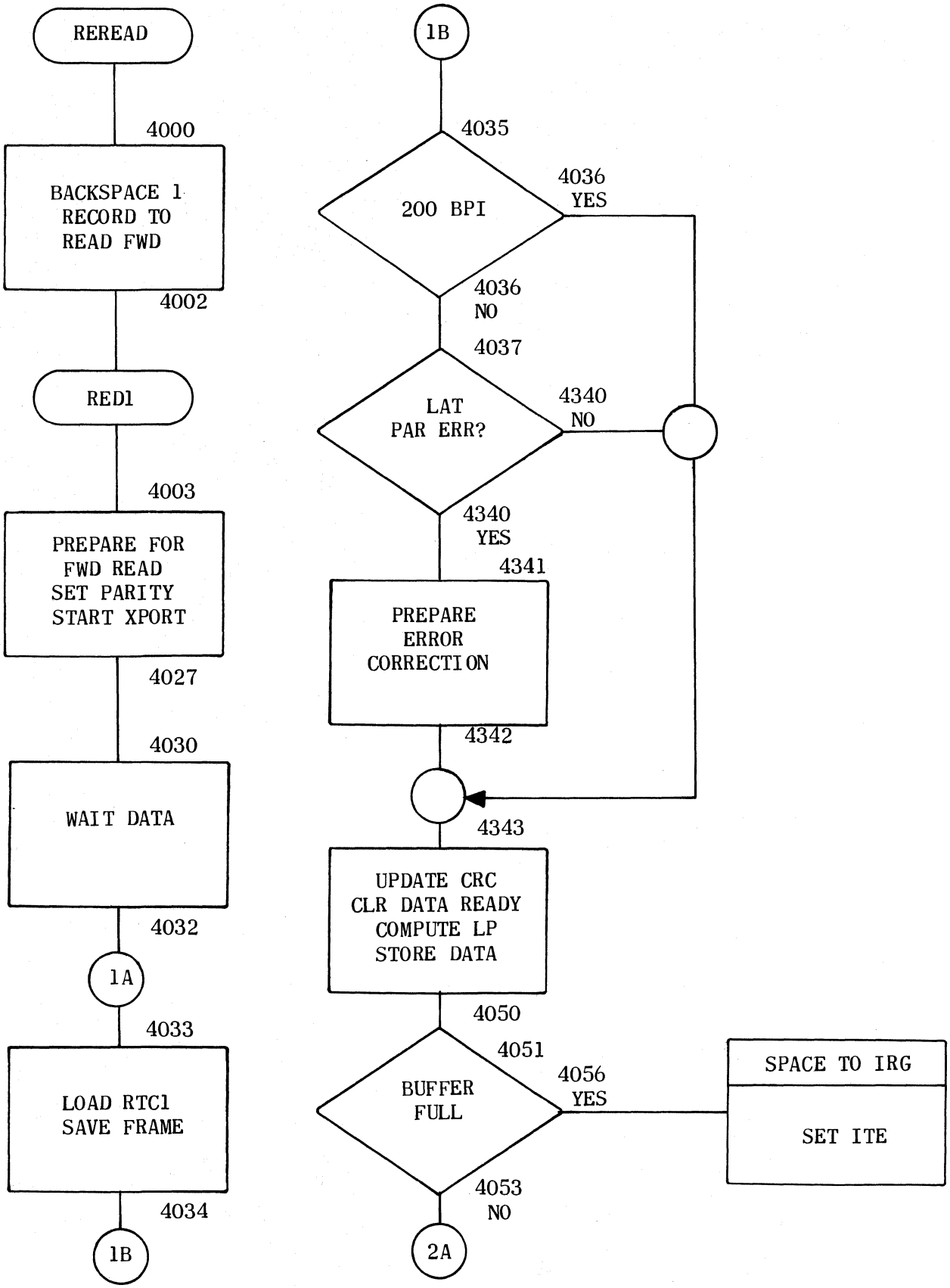


Figure 4-72. Reread Sequence Flow Diagram (Sheet 1 of 3)

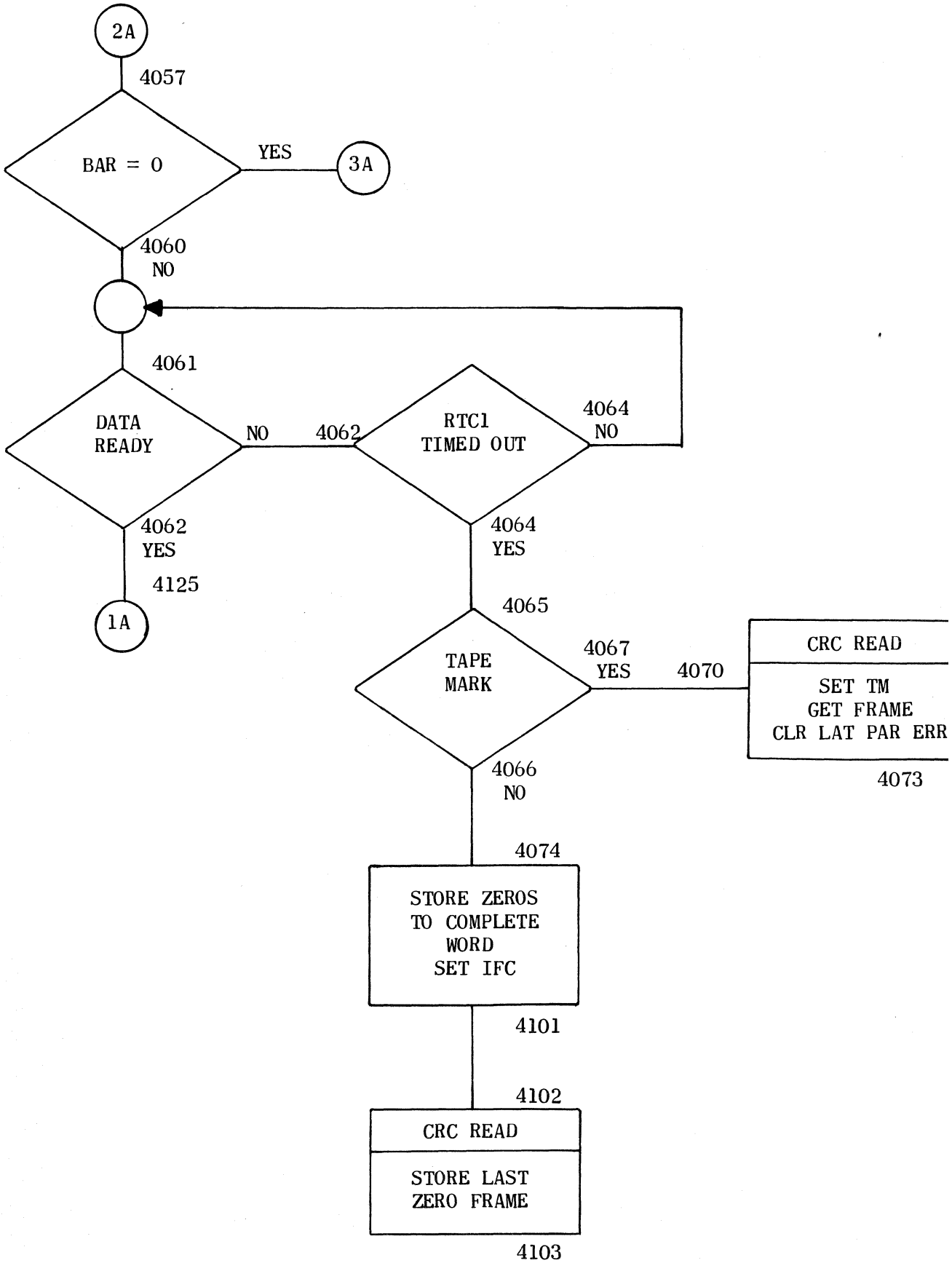


Figure 4-72. Reread Sequence Flow Diagram (Sheet 2 of 3)

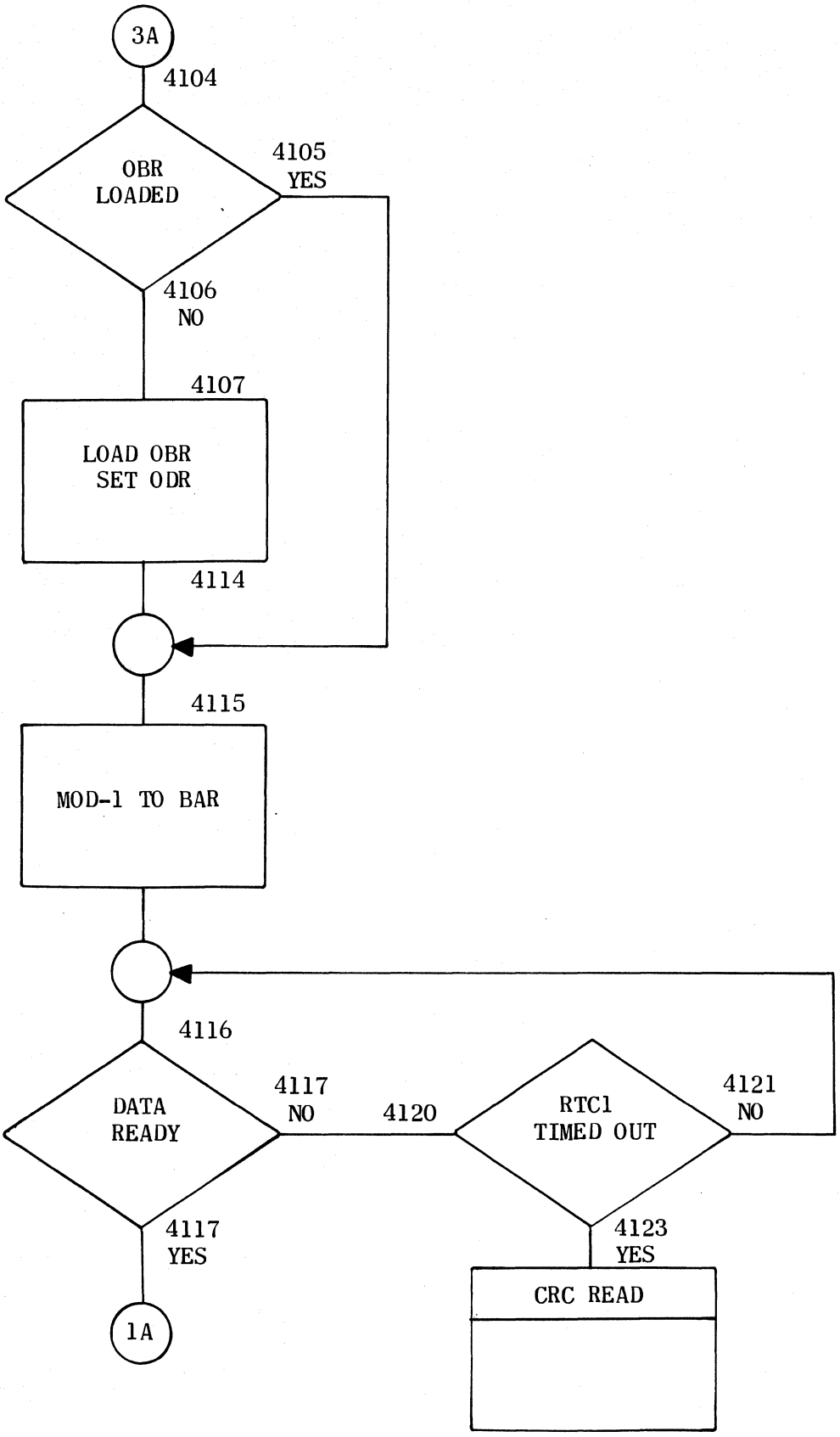


Figure 4-72. Reread Sequence Flow Diagram (Sheet 3 of 3)

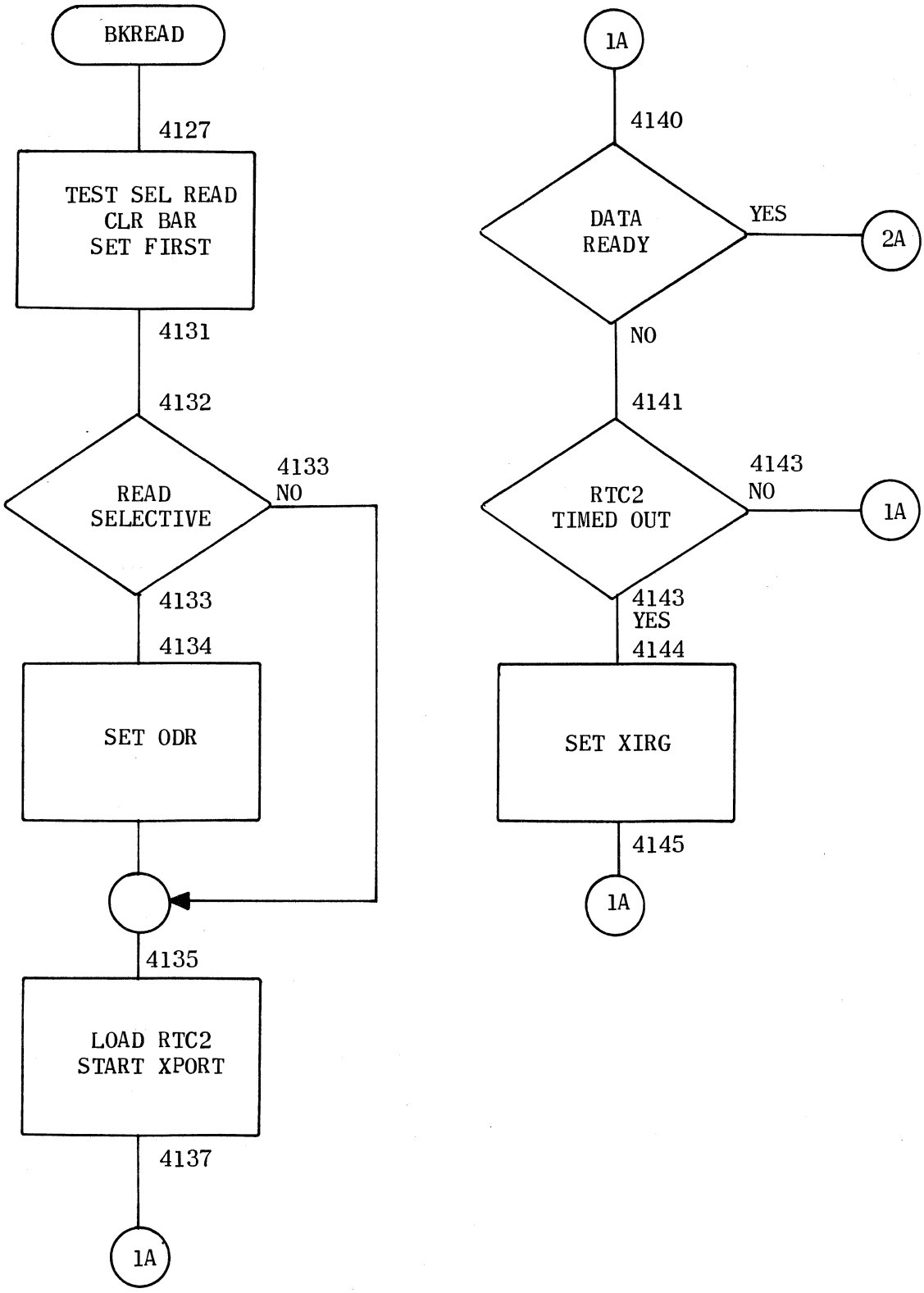


Figure 4-73. Back Read Sequence Flow Diagram (Sheet 1 of 7)

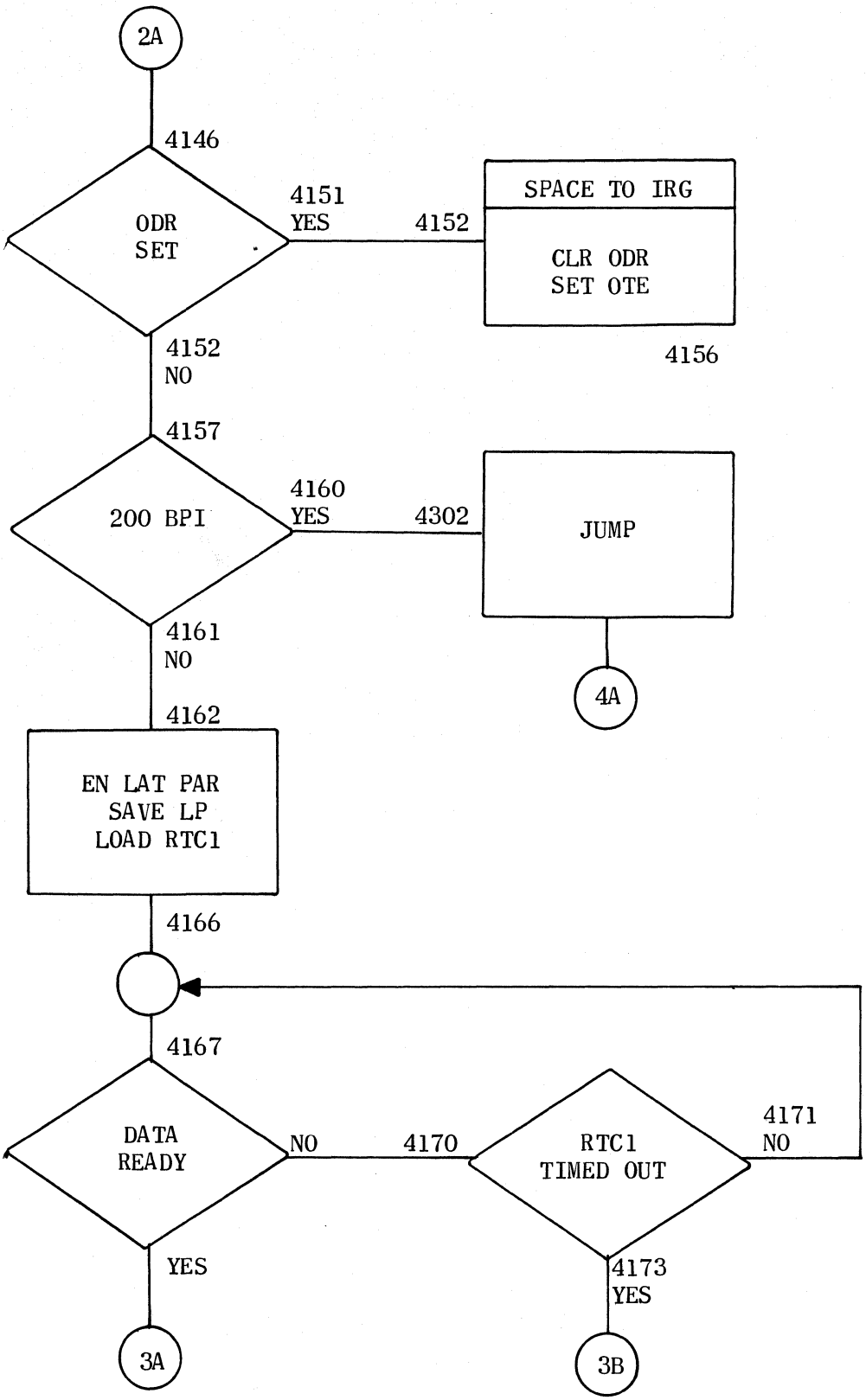


Figure 4-73. Back Read Sequence Flow Diagram (Sheet 2 of 7)

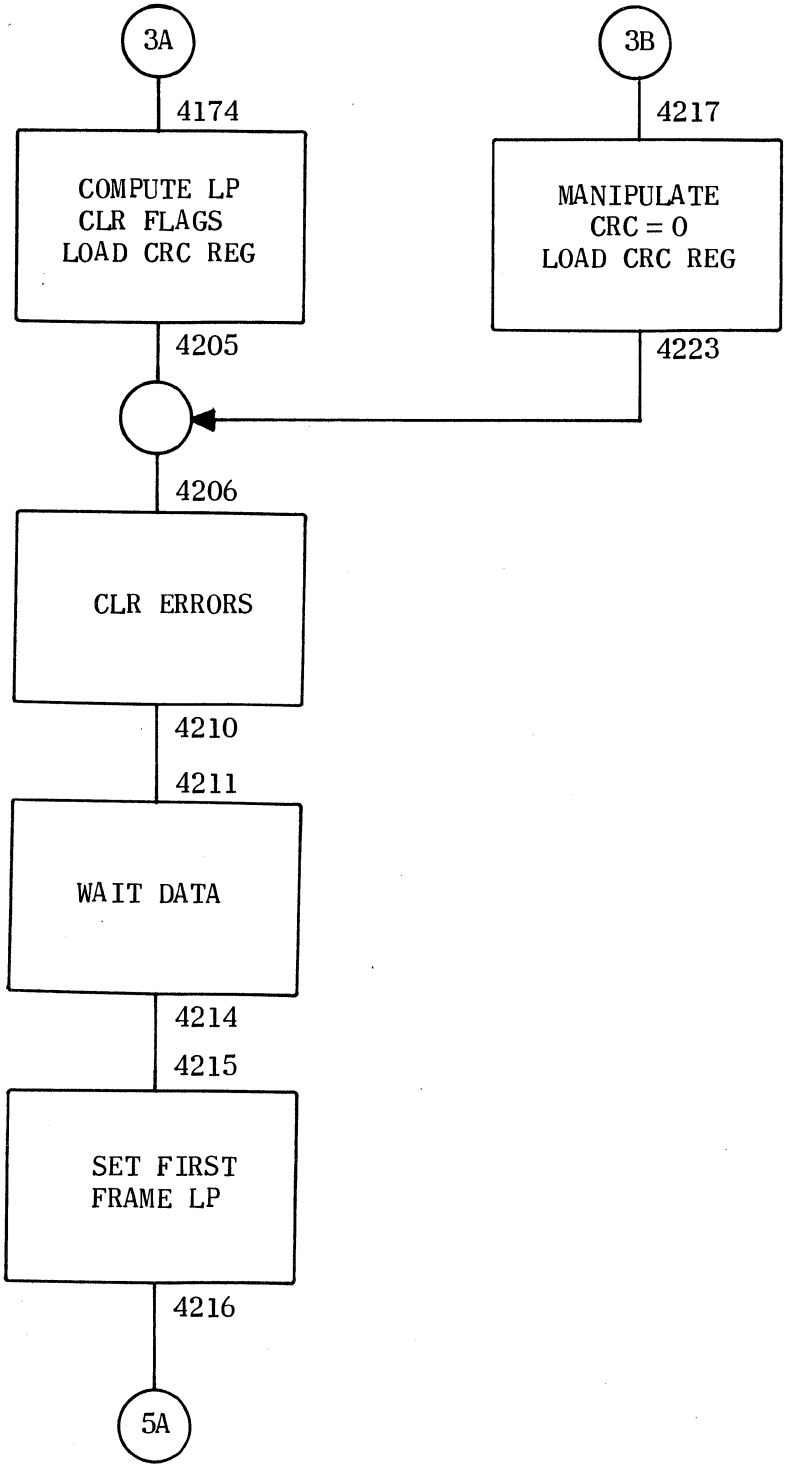


Figure 4-73. Back Read Sequence Flow Diagram (Sheet 3 of 7)

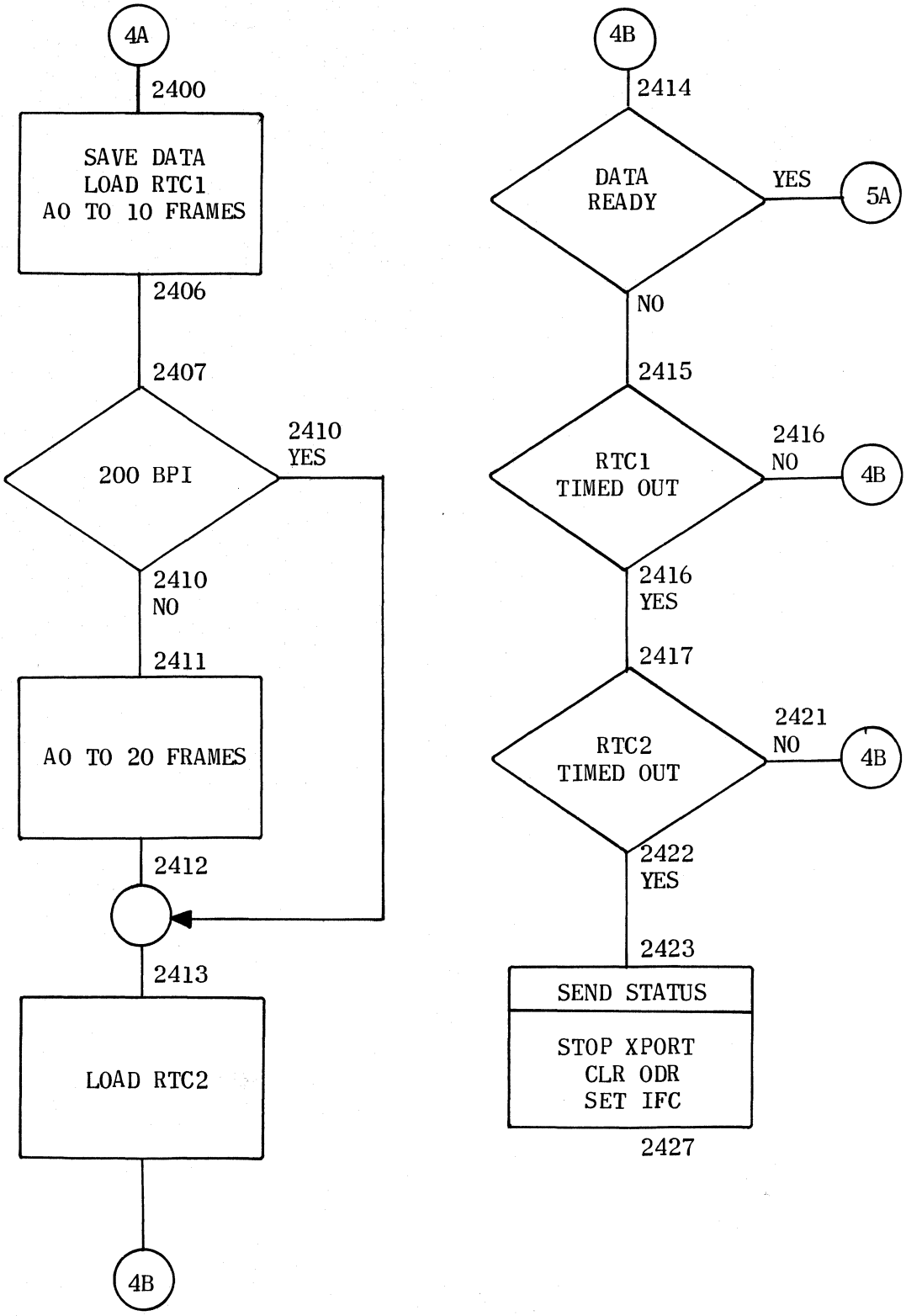


Figure 4-73. Back Read Sequence Flow Diagram (Sheet 4 of 7)

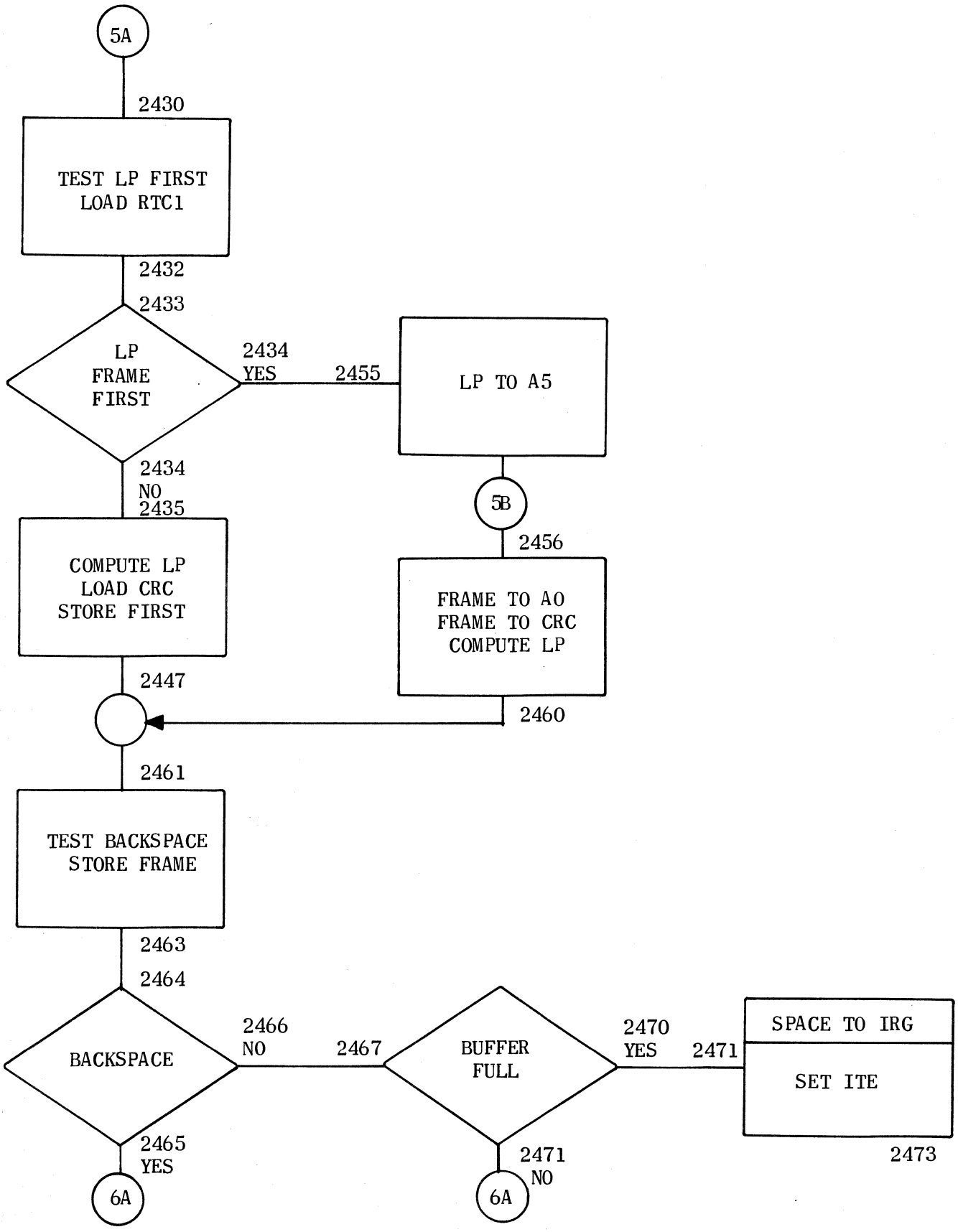


Figure 4-73. Back Read Sequence Flow Diagram (Sheet 5 of 7)

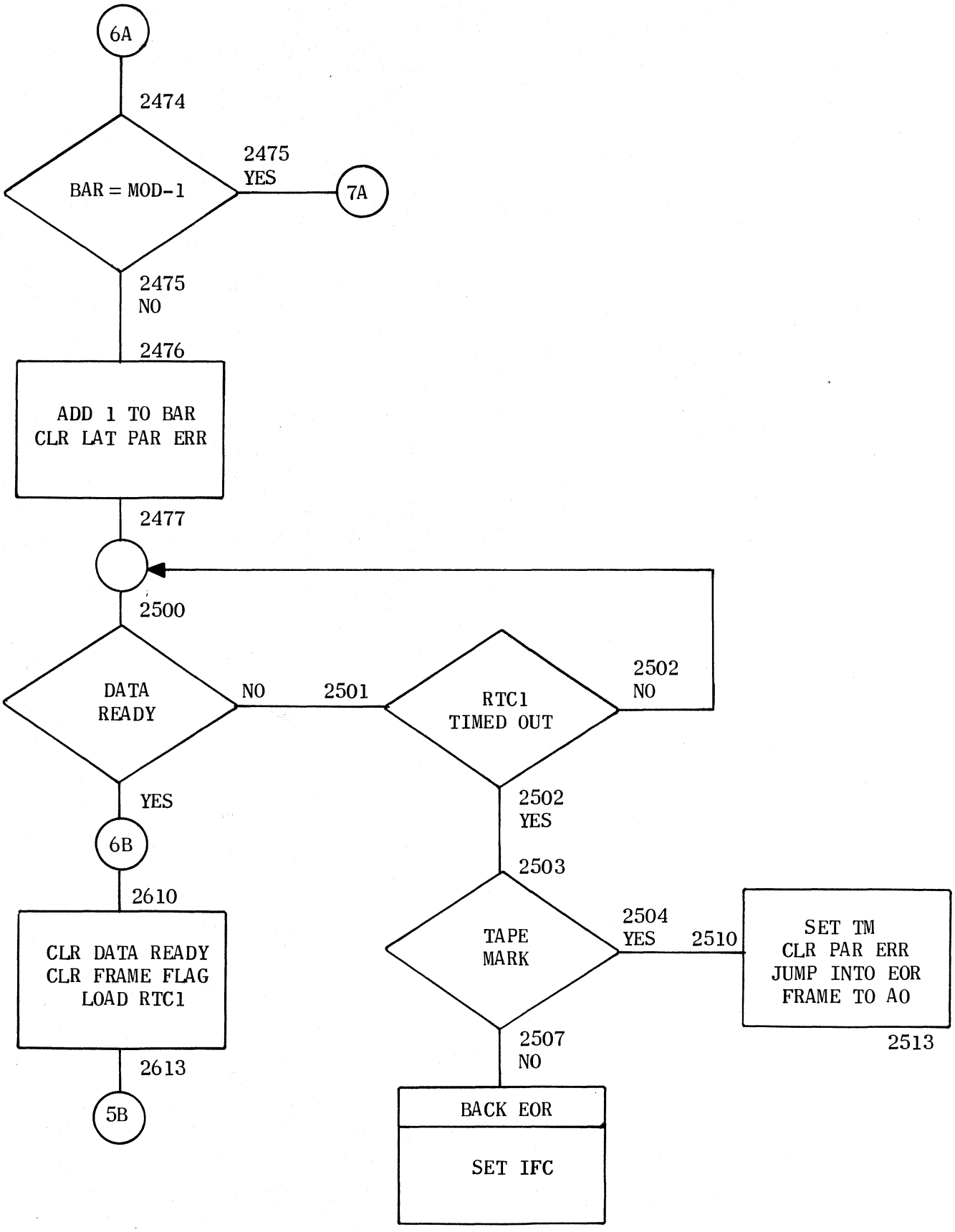


Figure 4-73. Back Read Sequence Flow Diagram (Sheet 6 of 7)

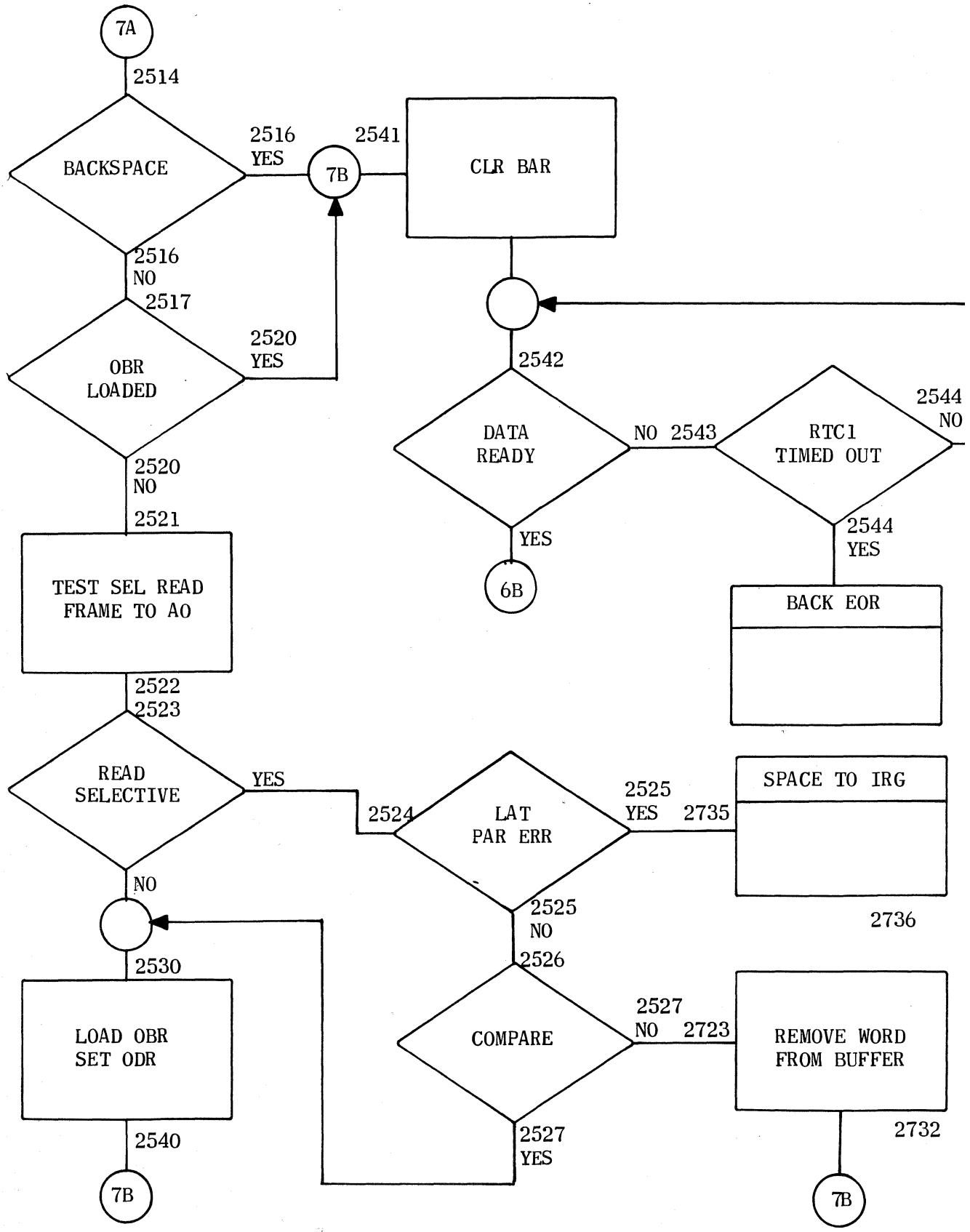


Figure 4-73. Back Read Sequence Flow Diagram (Sheet 7 of 7)

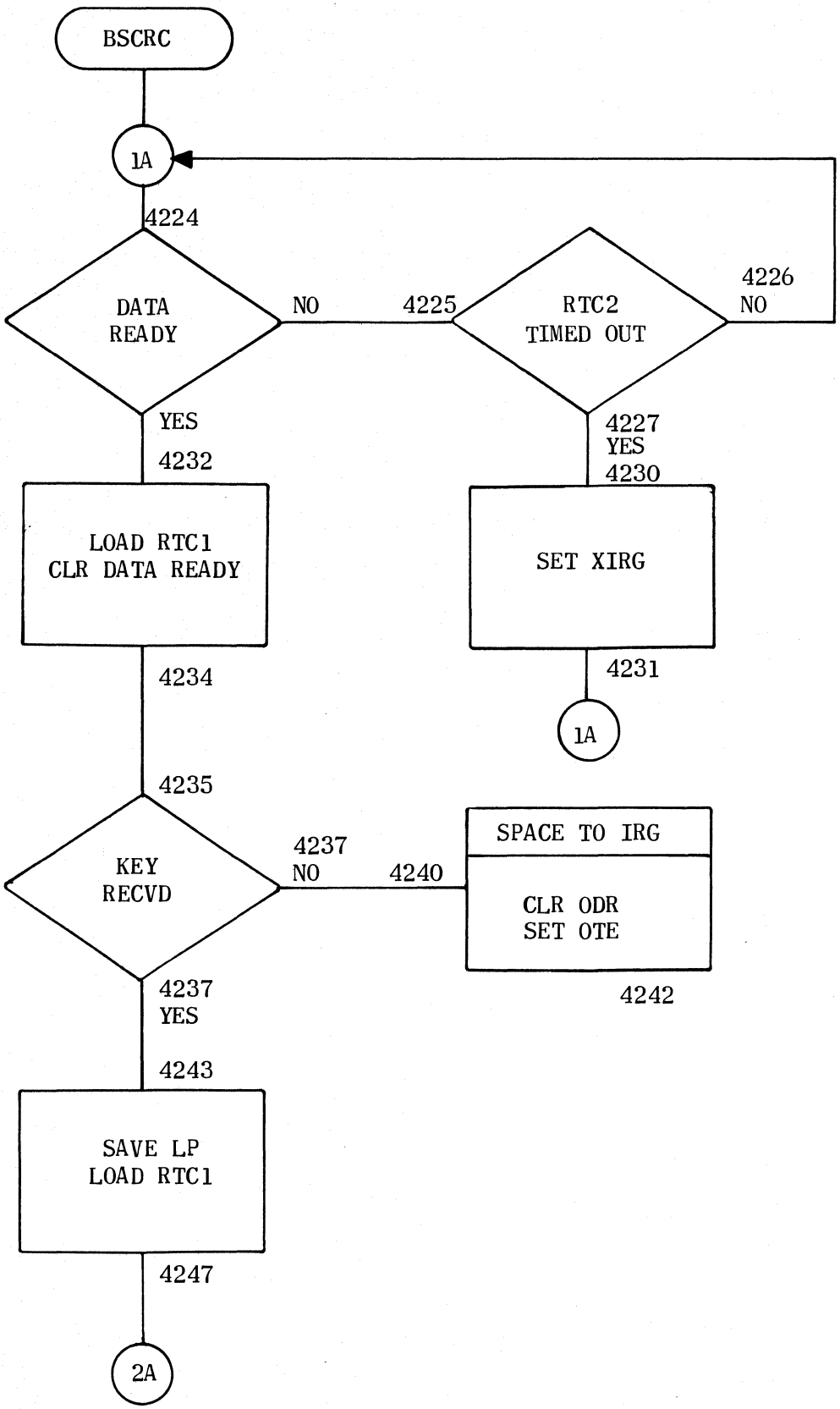


Figure 4-74. CRC Back Search Sequence Flow Diagram (Sheet 1 of 2)

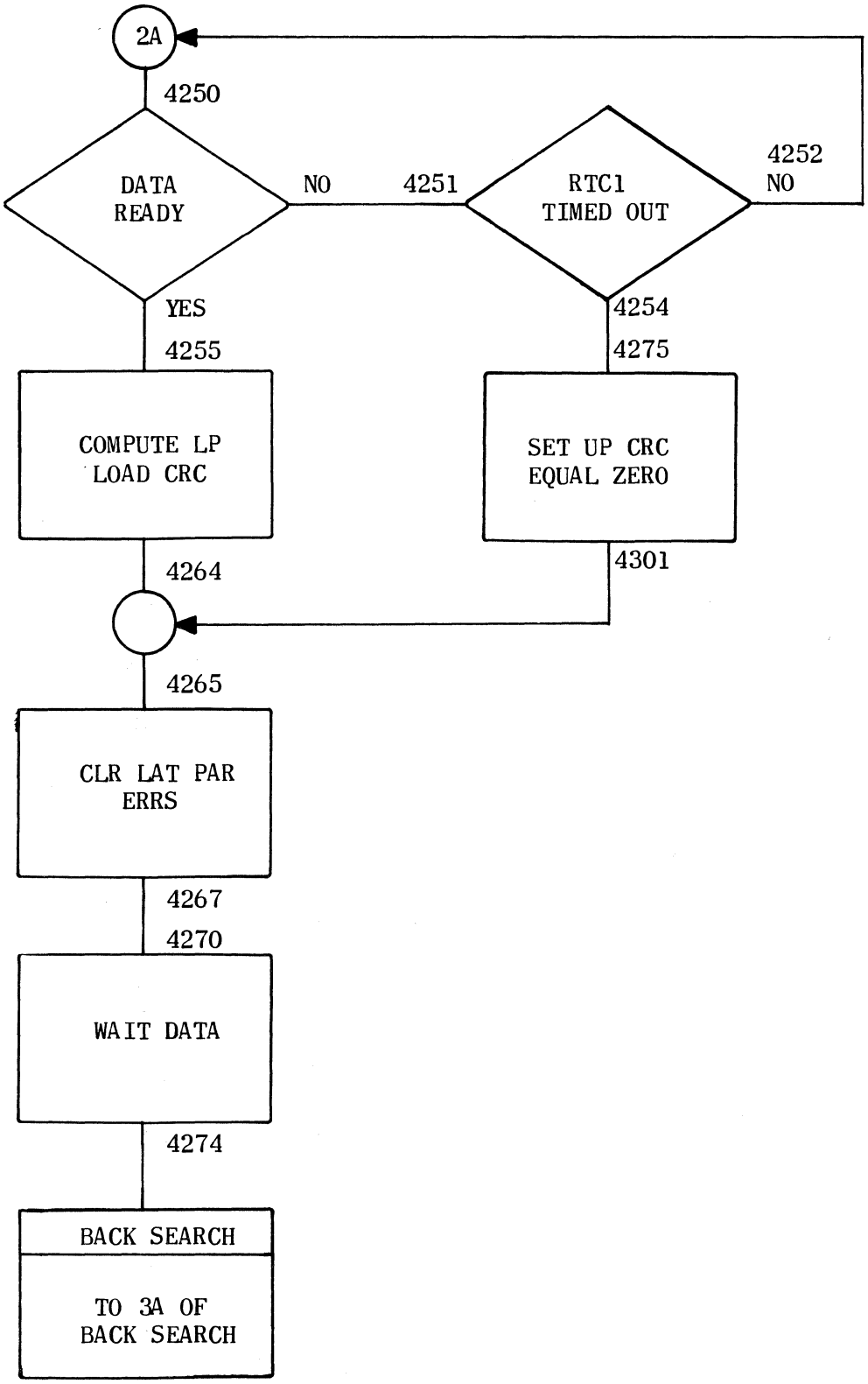


Figure 4-74. CRC Back Search Sequence Flow Diagram (Sheet 2 of 2)

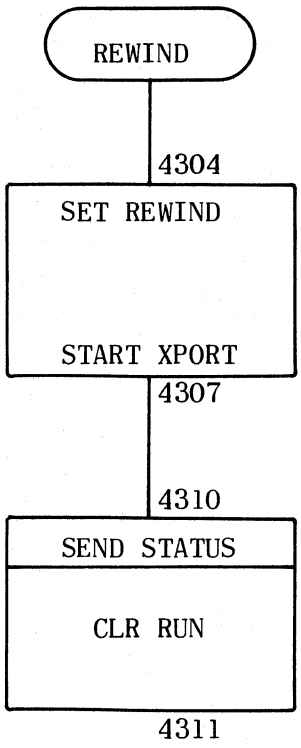


Figure 4-75. Rewind Sequence Flow Diagram

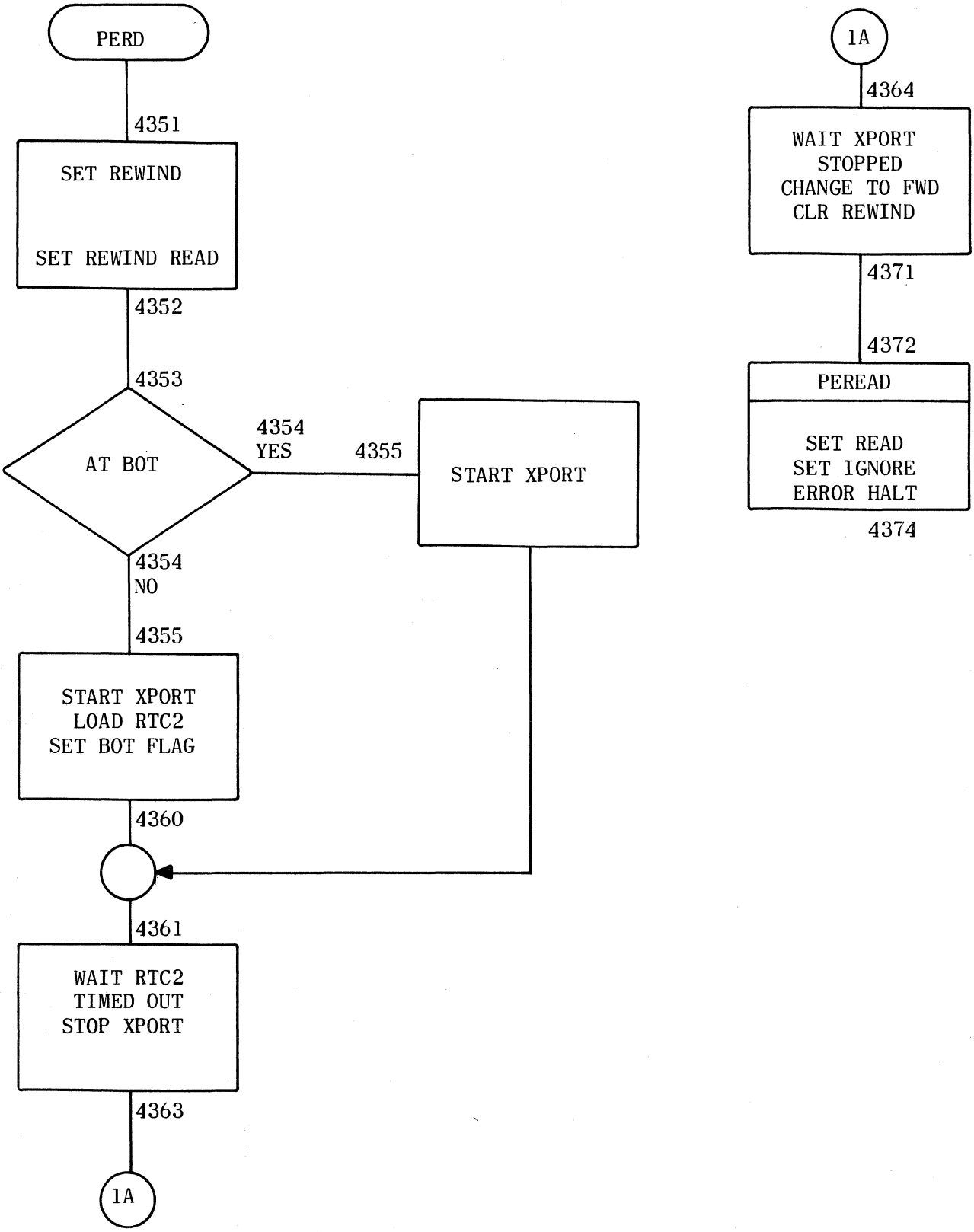


Figure 4-76. PE Rewind Read Sequence Flow Diagram

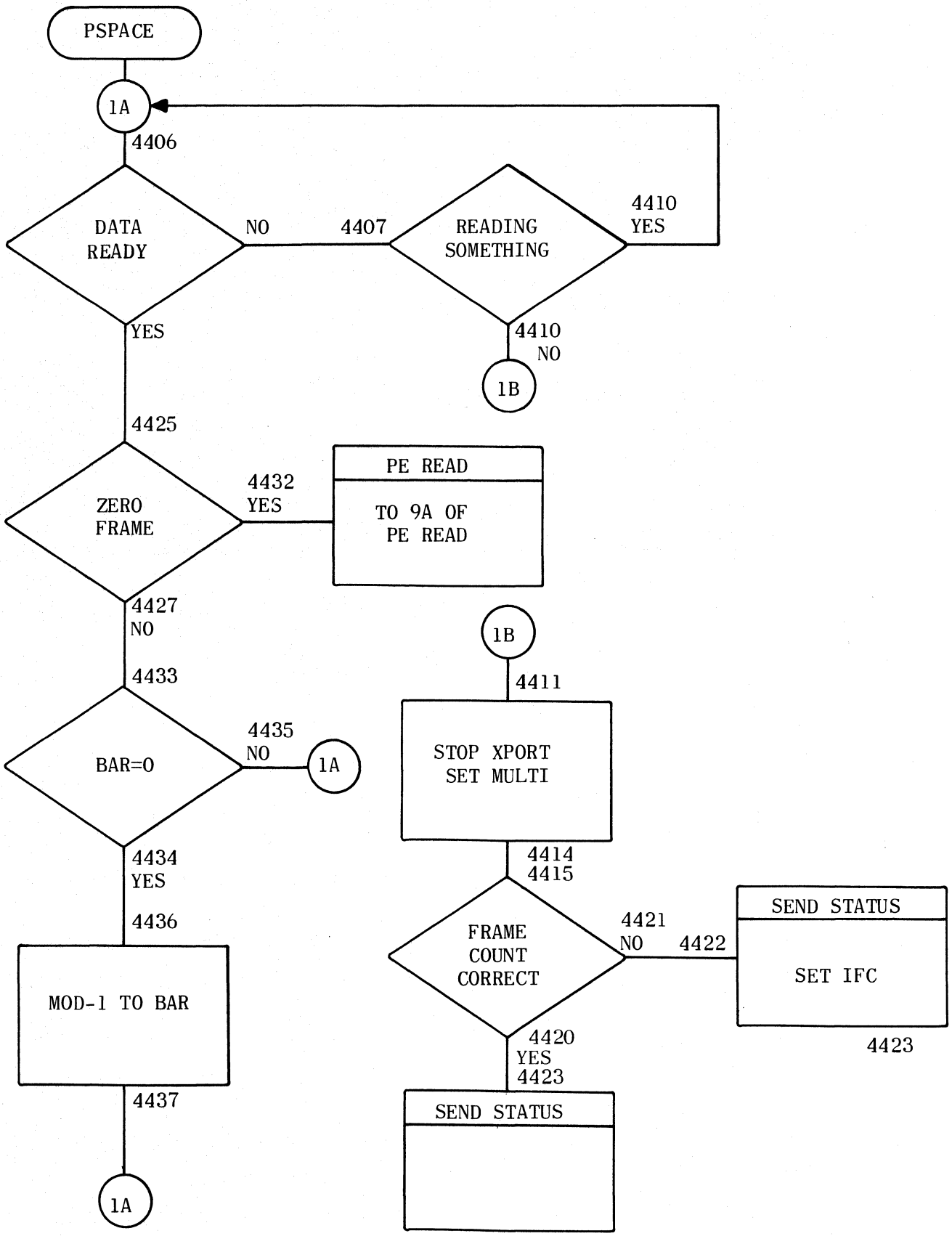


Figure 4-77. PE Space to IRG Sequence Flow Diagram

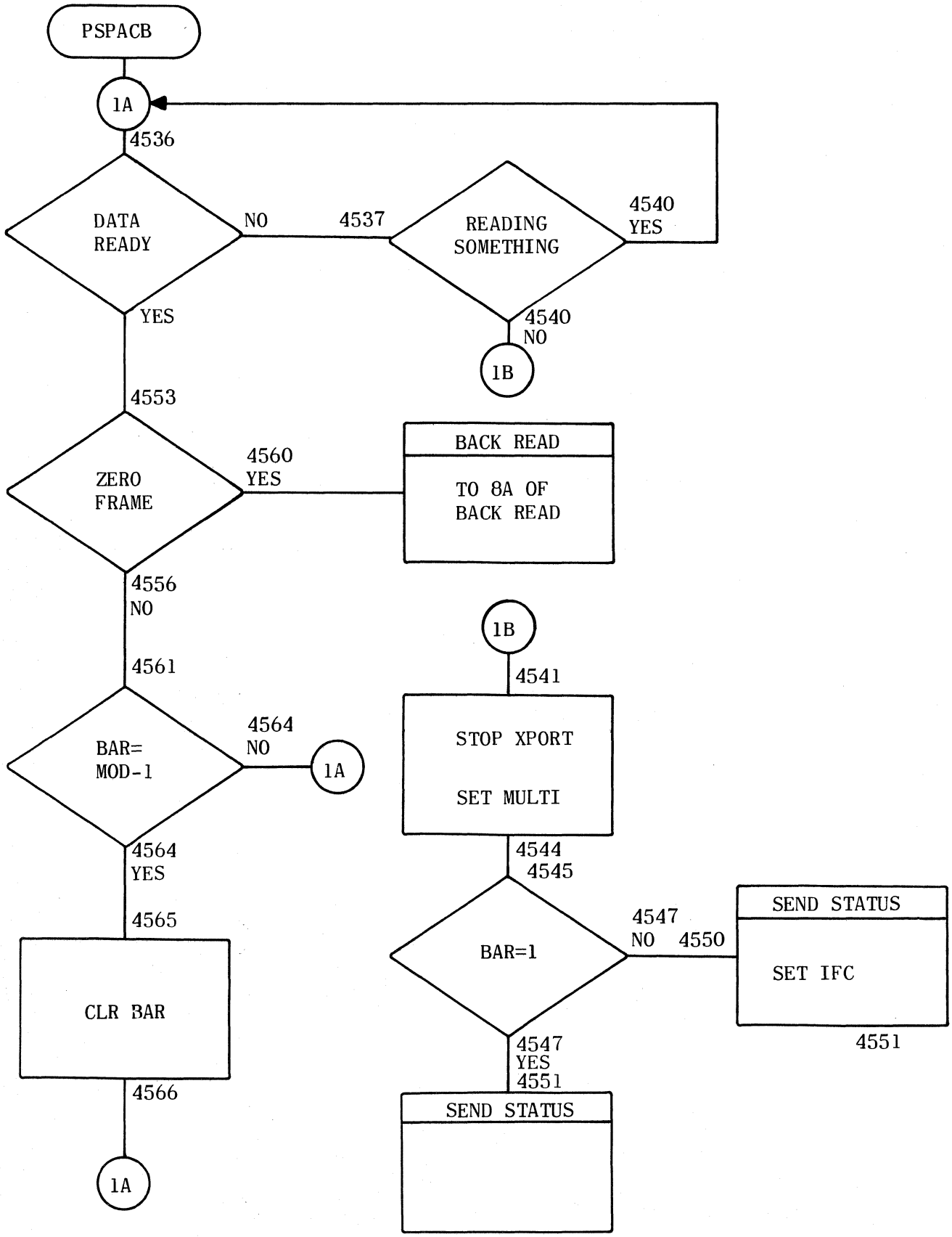


Figure 4-78. PE Backspace Sequence Flow Diagram

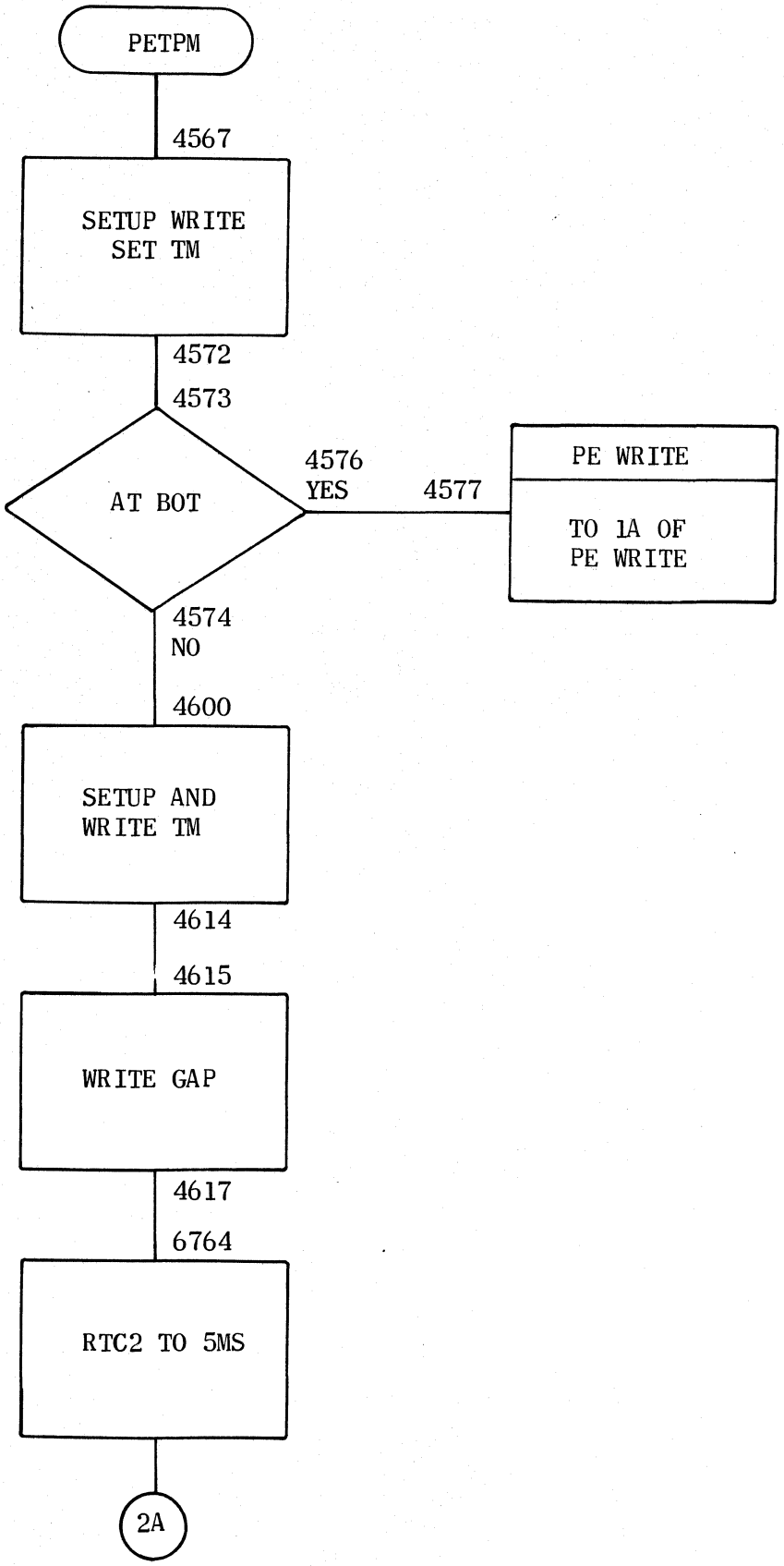


Figure 4-79. PE Write Tape Mark Sequence Flow Diagram (Sheet 1 of 2)

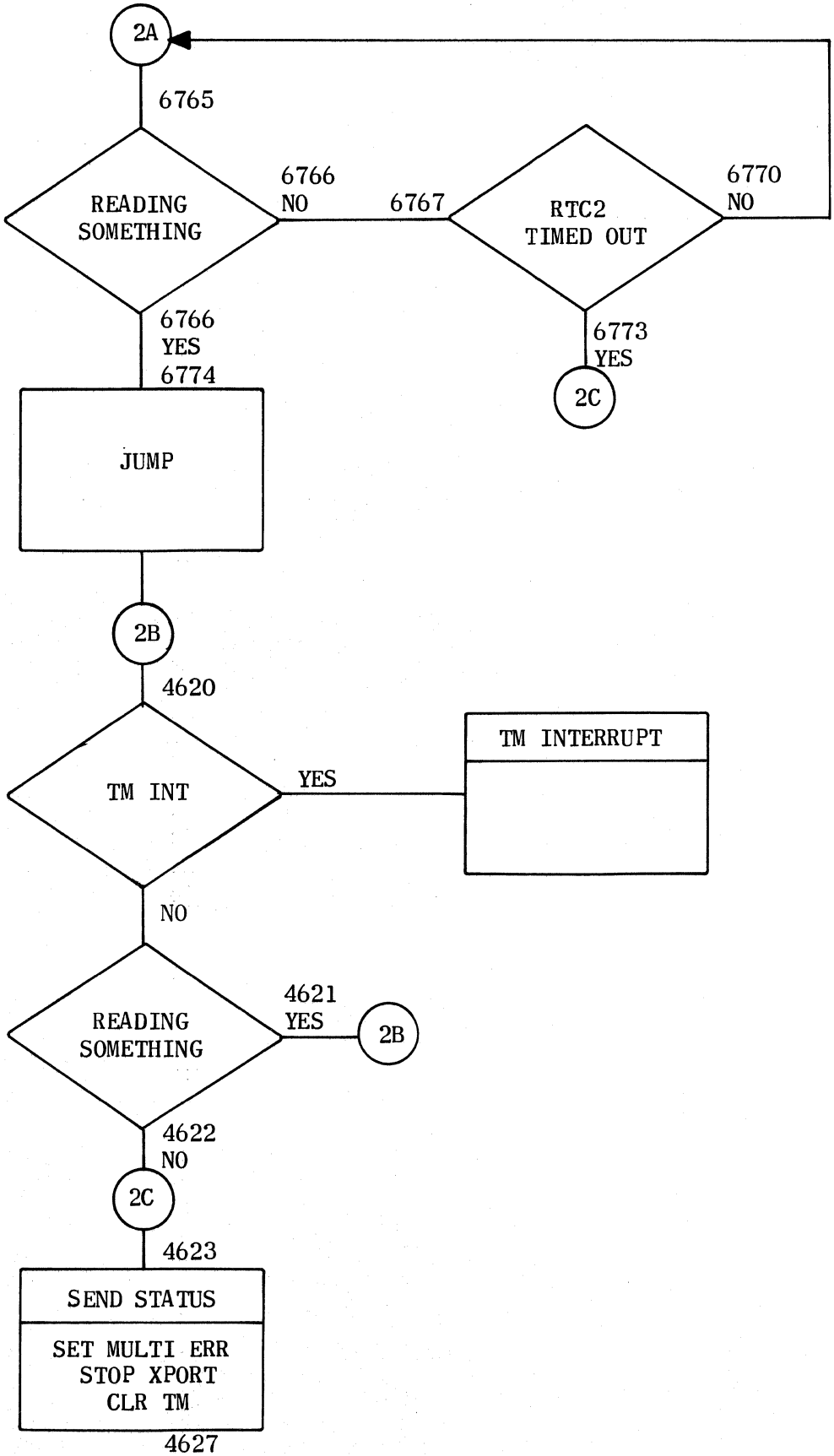


Figure 4-79. PE Write Tape Mark Sequence Flow Diagram (Sheet 2 of 2)

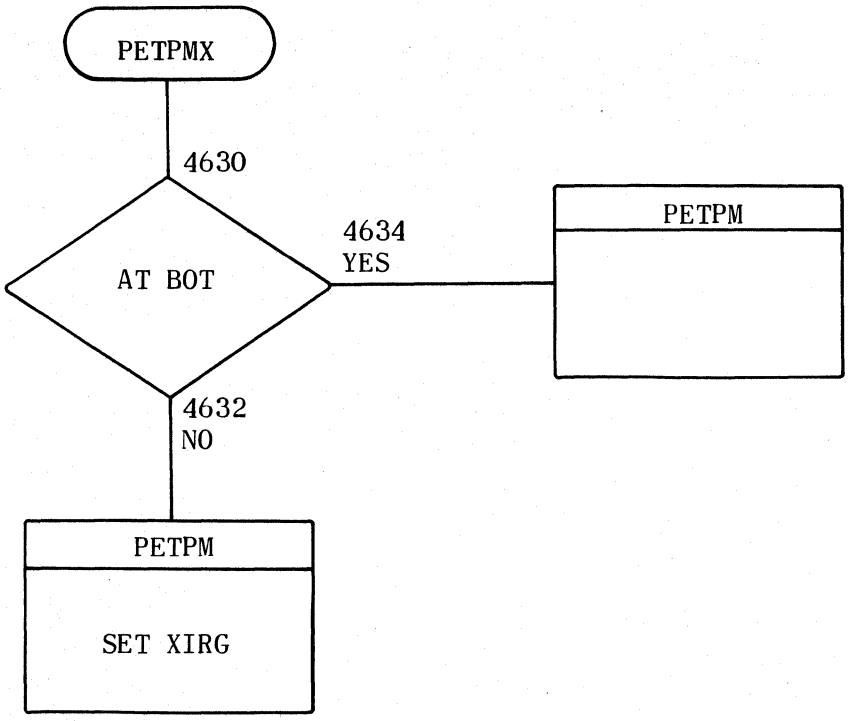


Figure 4-80. PE Write Tape Mark XIRG Sequence Flow Diagram

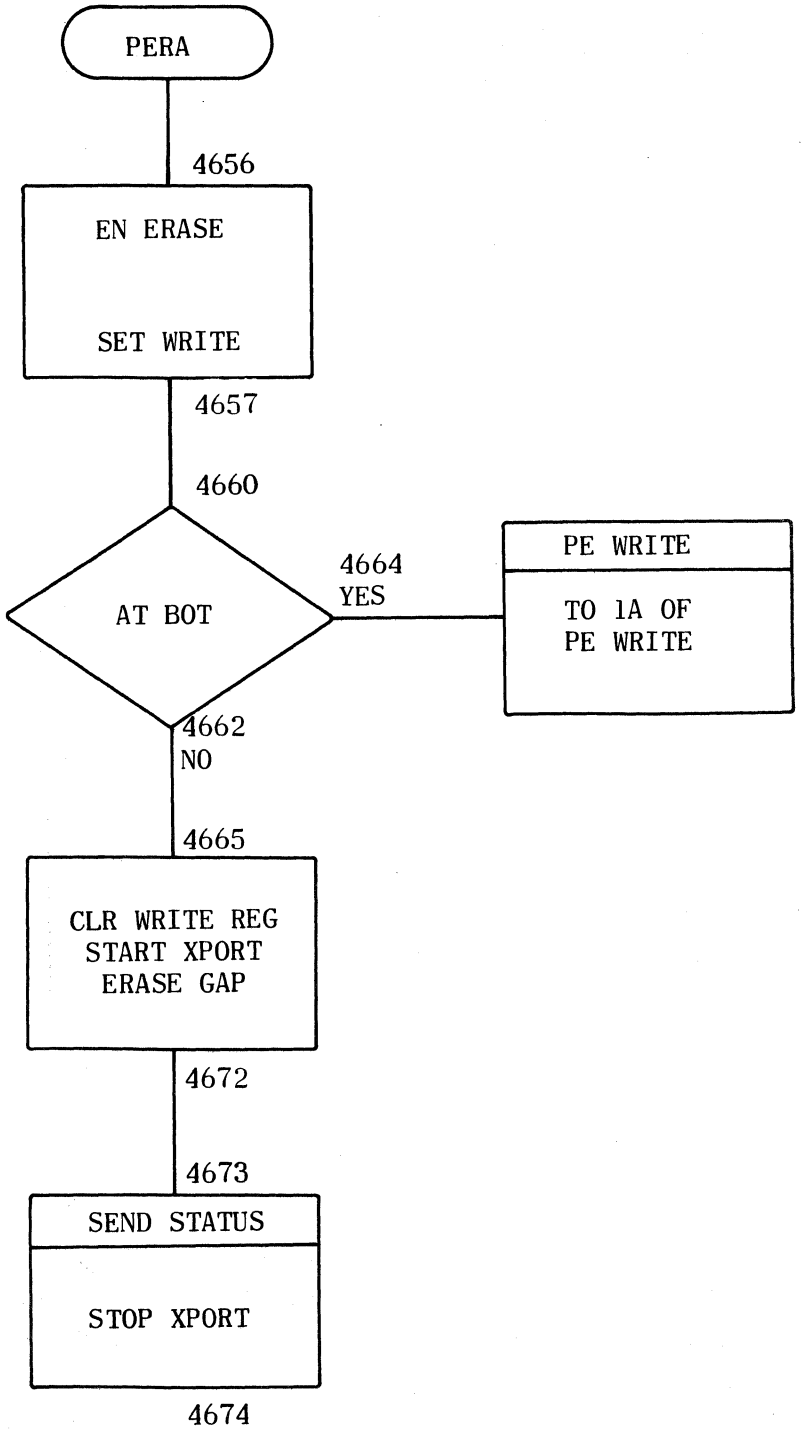


Figure 4-81. PE Erase Sequence Flow Diagram

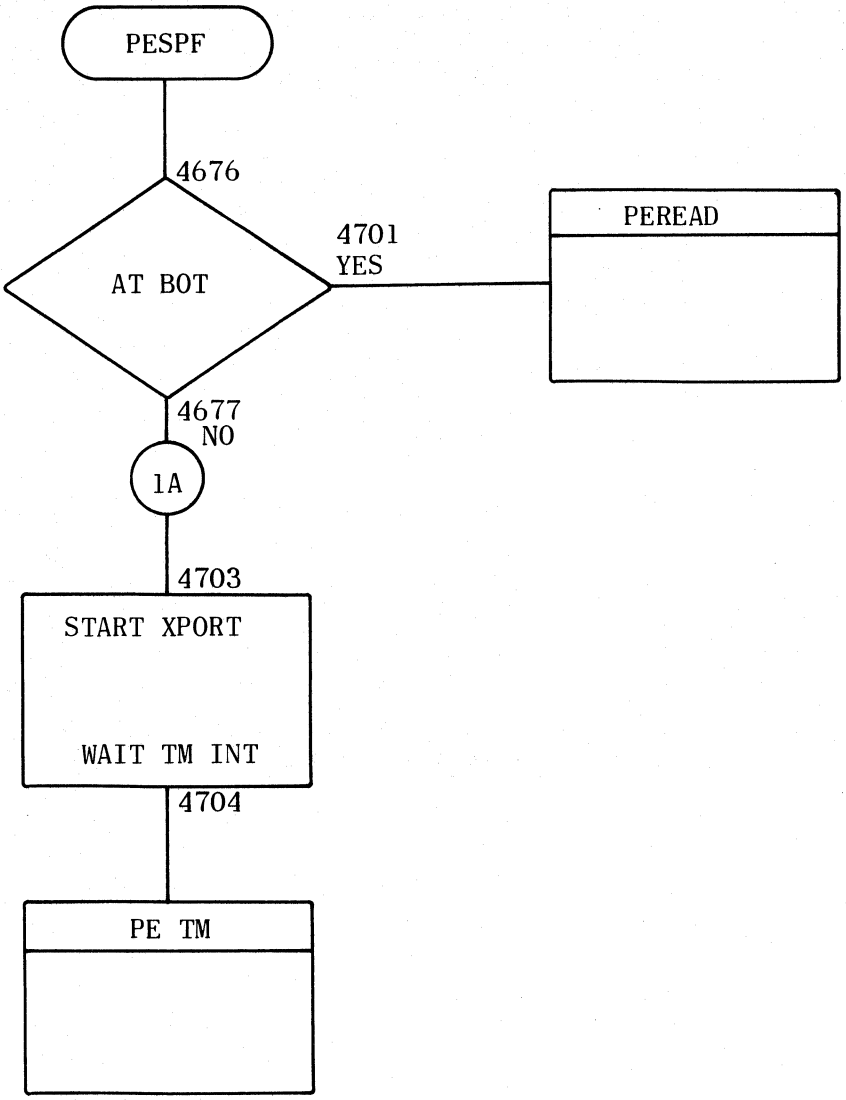


Figure 4-82. PE Space File Sequence Flow Diagram

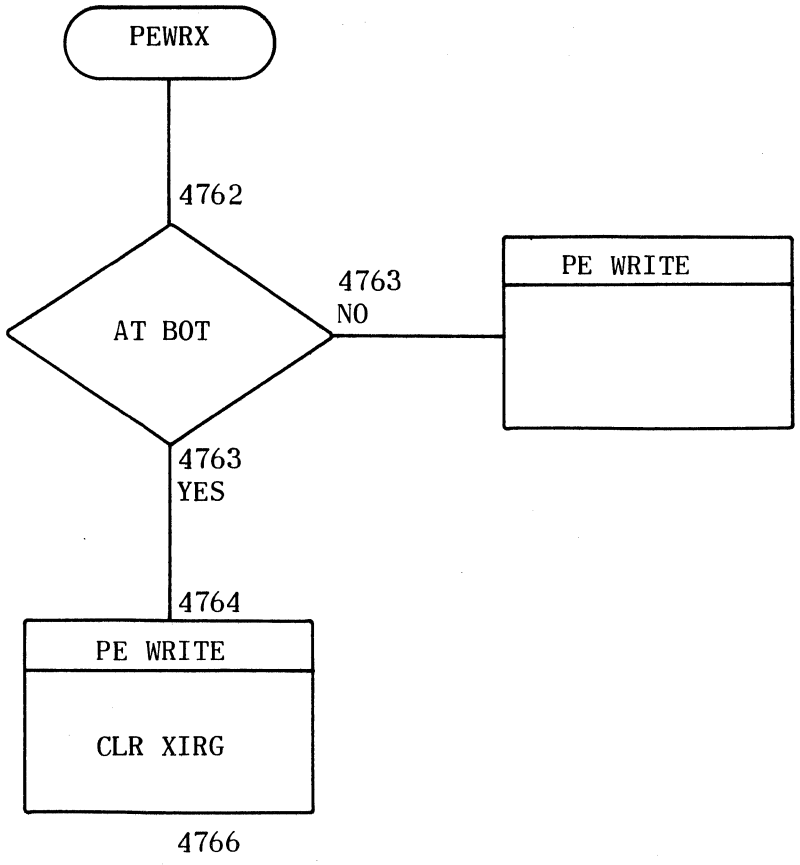


Figure 4-83. PE Write XIRG Sequence Flow Diagram

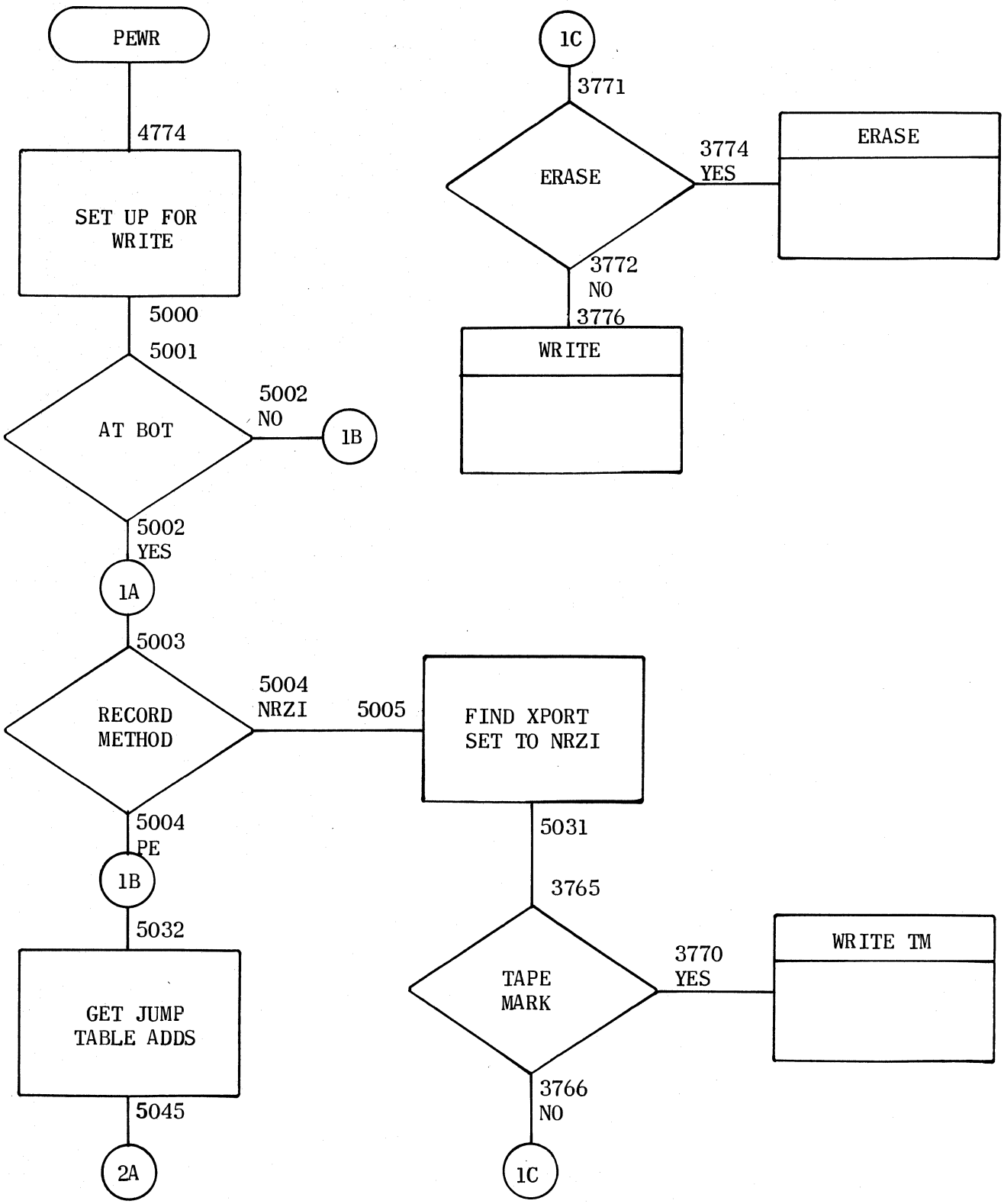


Figure 4-84. PE Write Sequence Flow Diagram (Sheet 1 of 6)

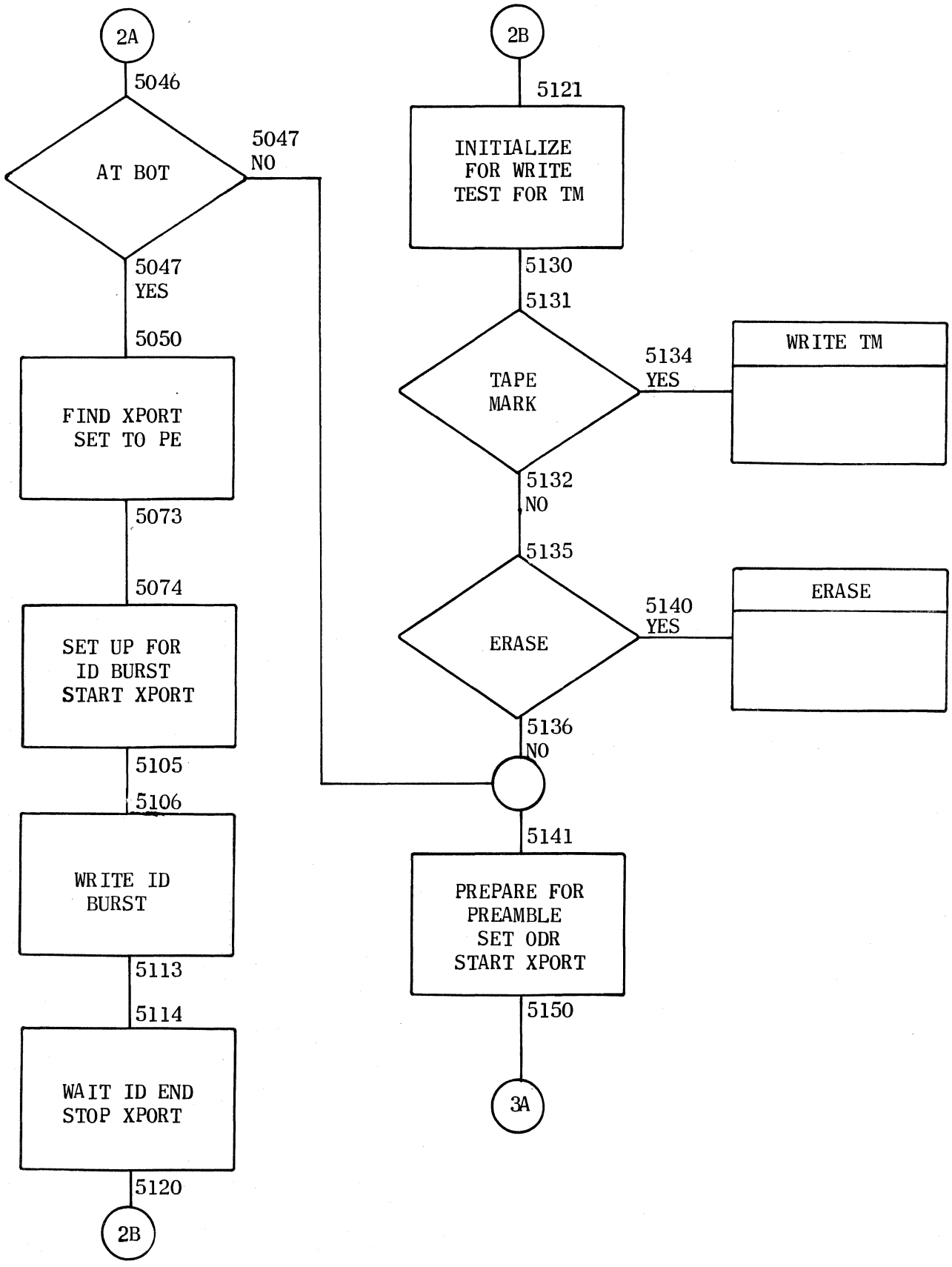


Figure 4-84. PE Write Sequence Flow Diagram (Sheet 2 of 6)

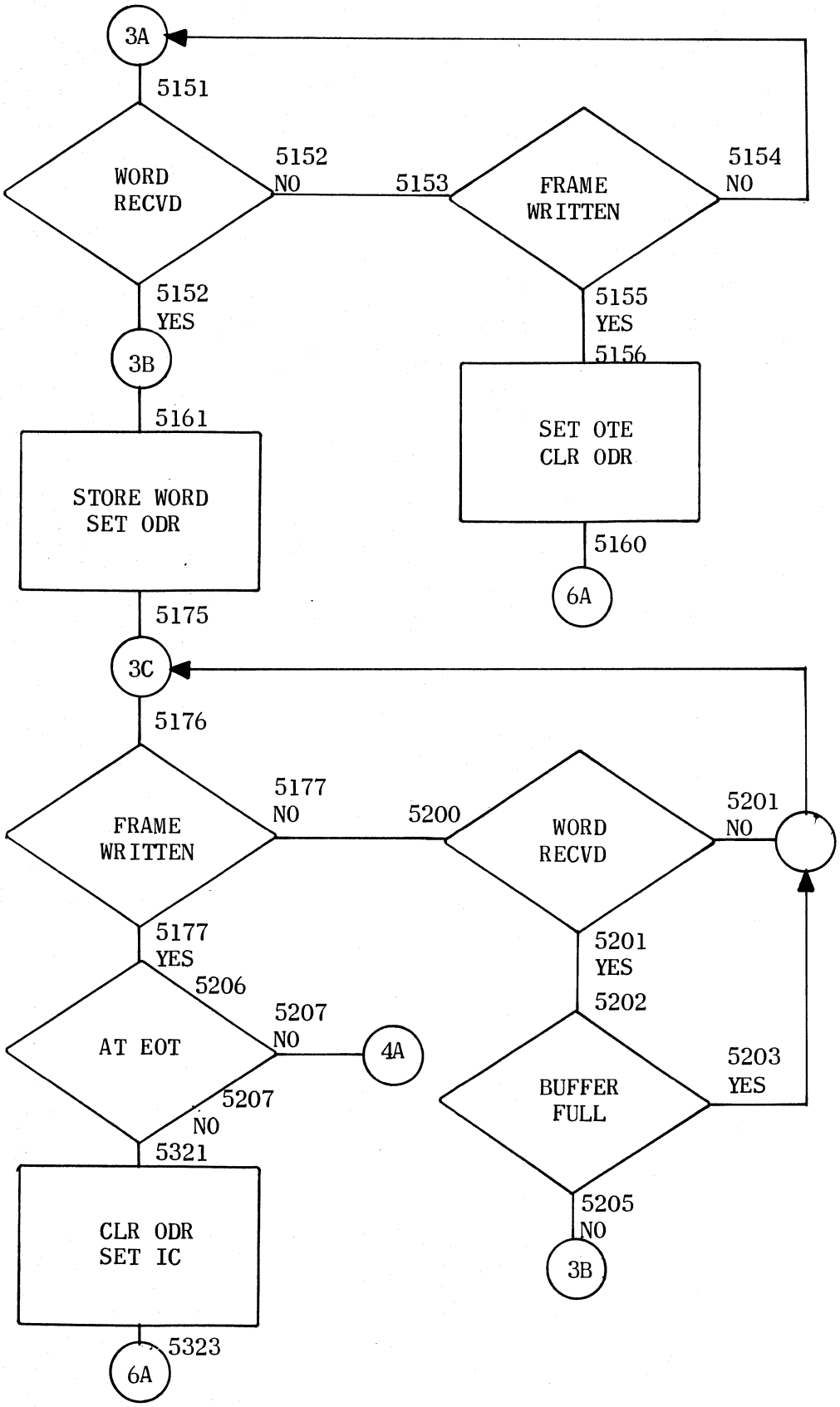


Figure 4-84. PE Write Sequence Flow Diagram (Sheet 3 of 6)

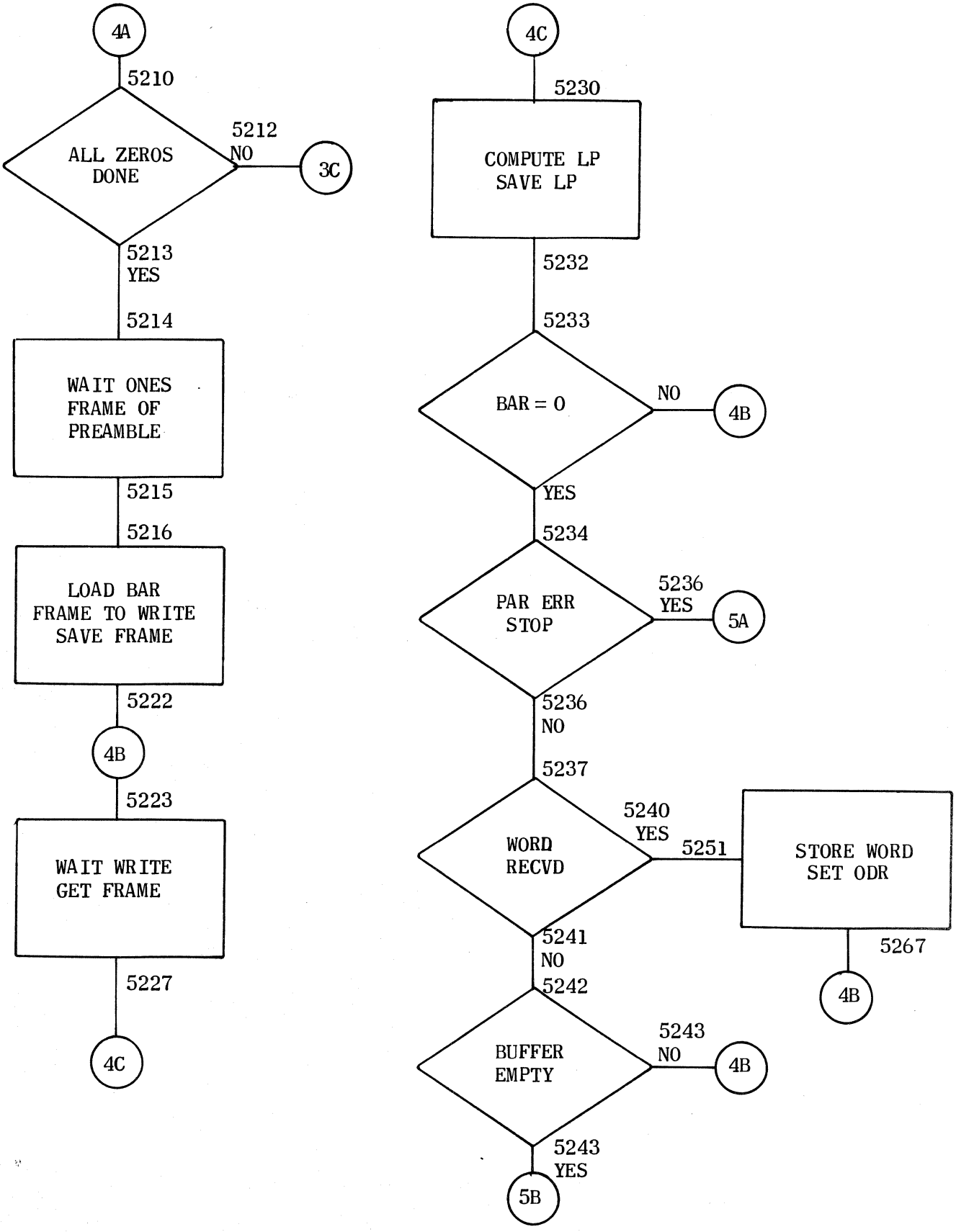


Figure 4-84. PE Write Sequence Flow Diagram (Sheet 4 of 6)

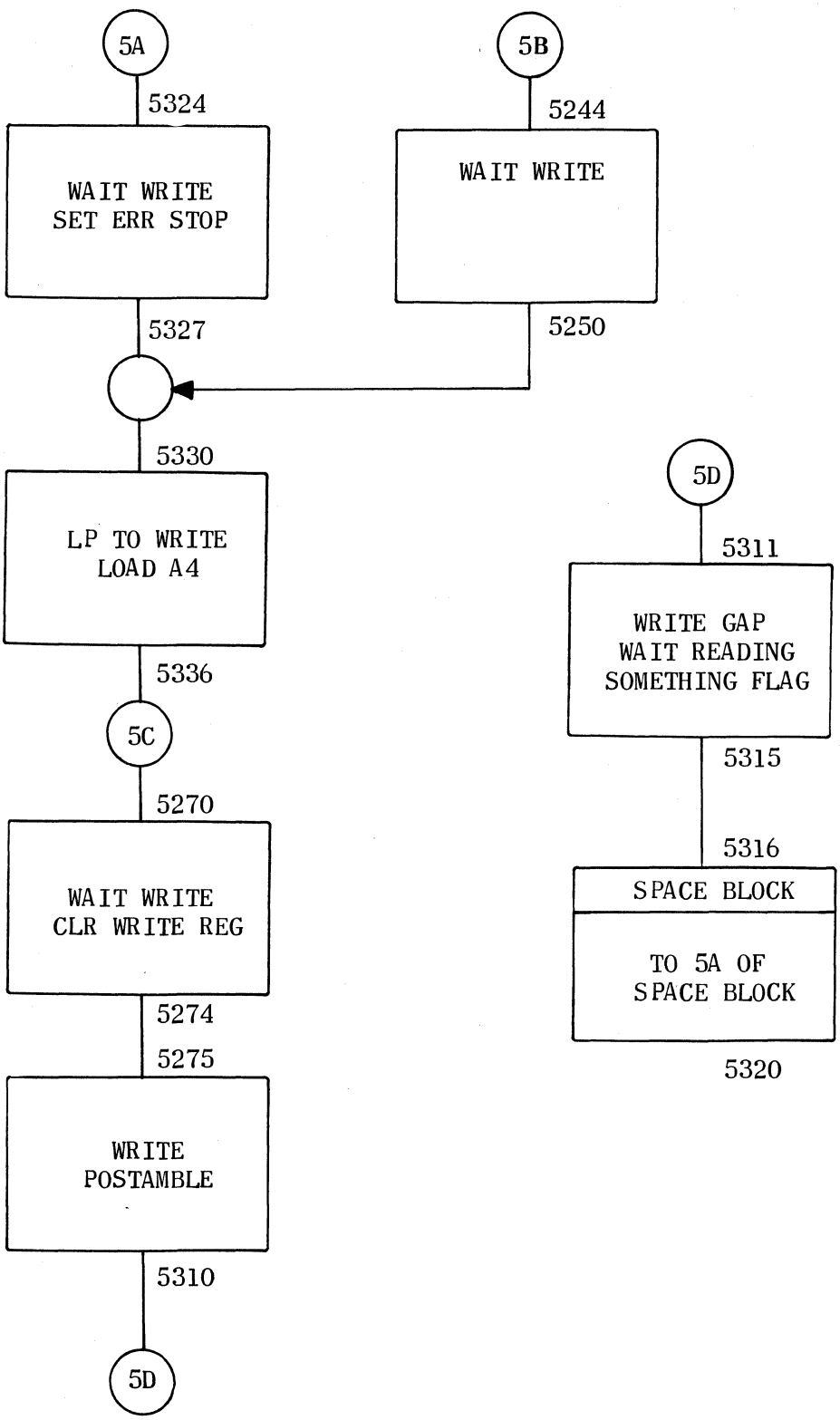


Figure 4-84. PE Write Sequence Flow Diagram (Sheet 5 of 6)

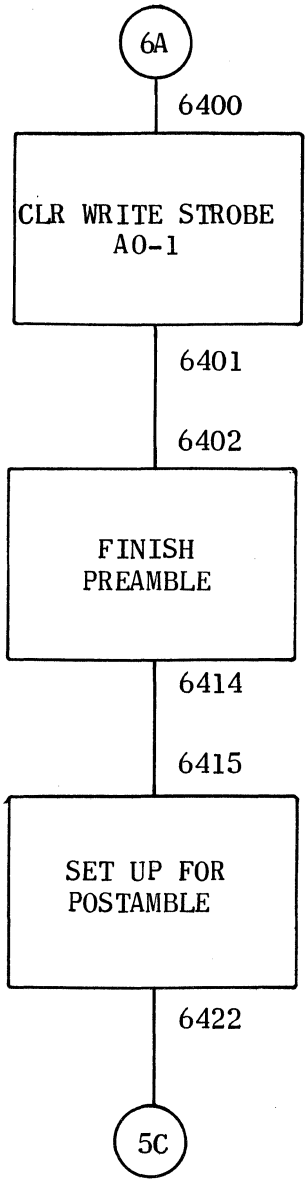


Figure 4-84. PE Write Sequence Flow Diagram (Sheet 6 of 6)

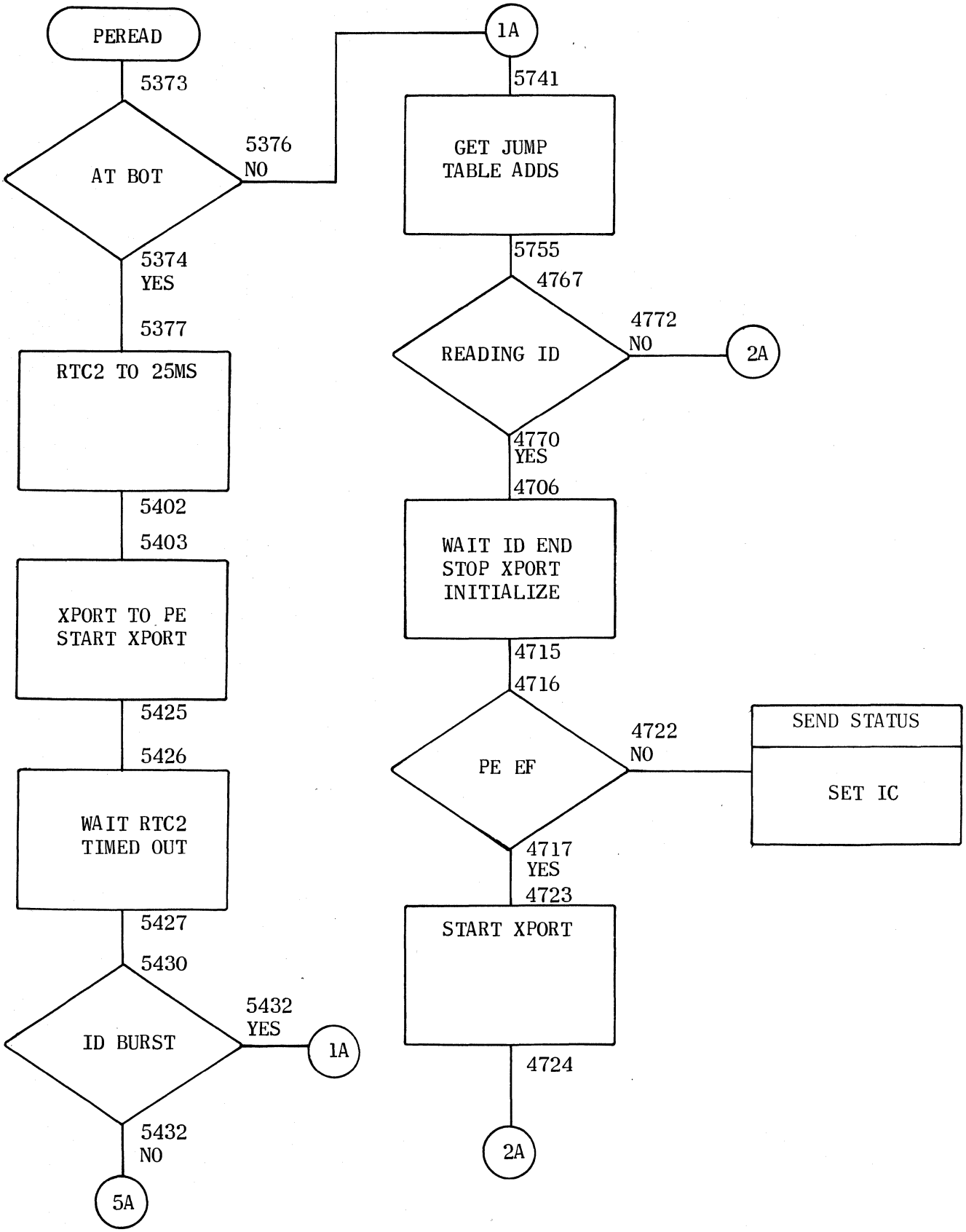


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 1 of 11)

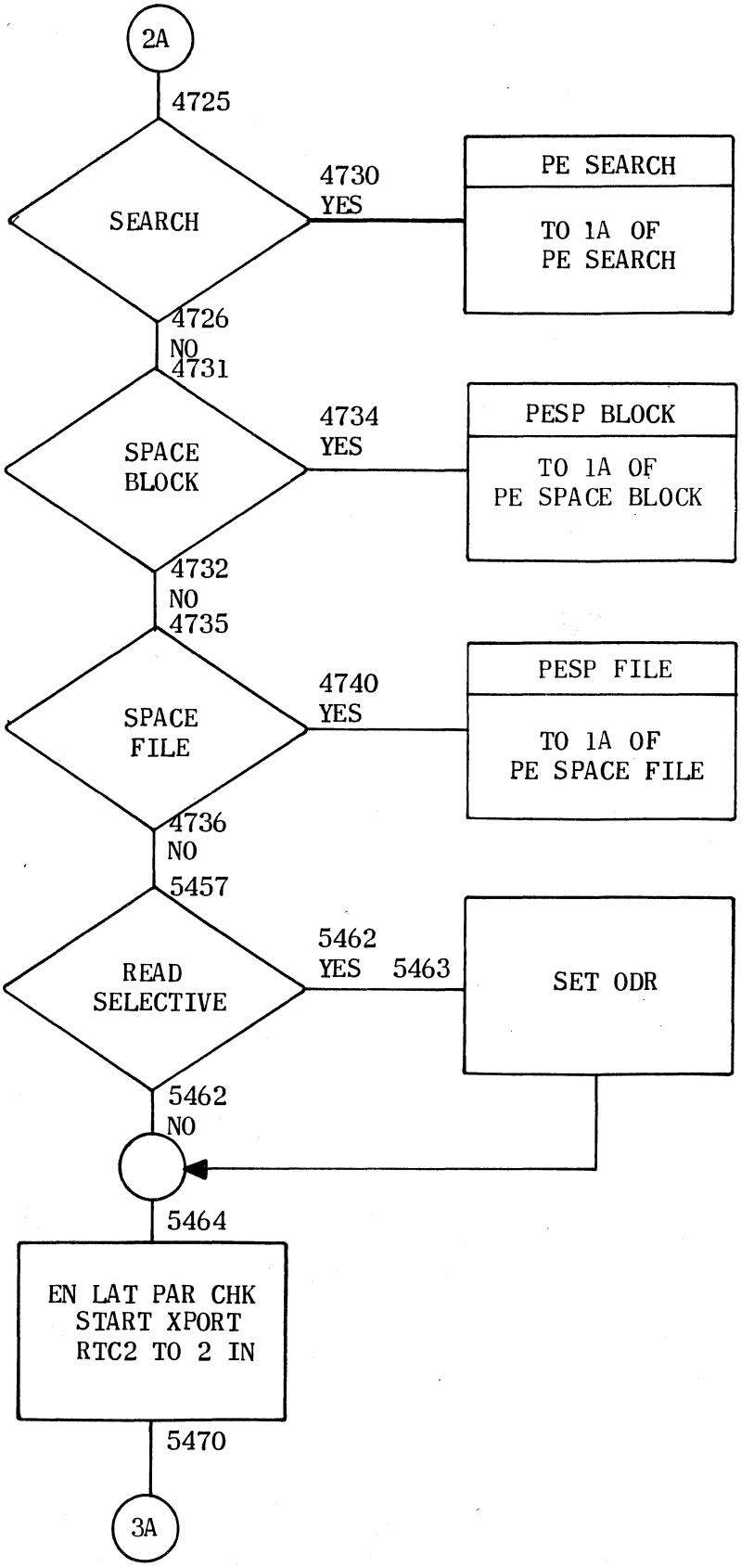


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 2 of 11)

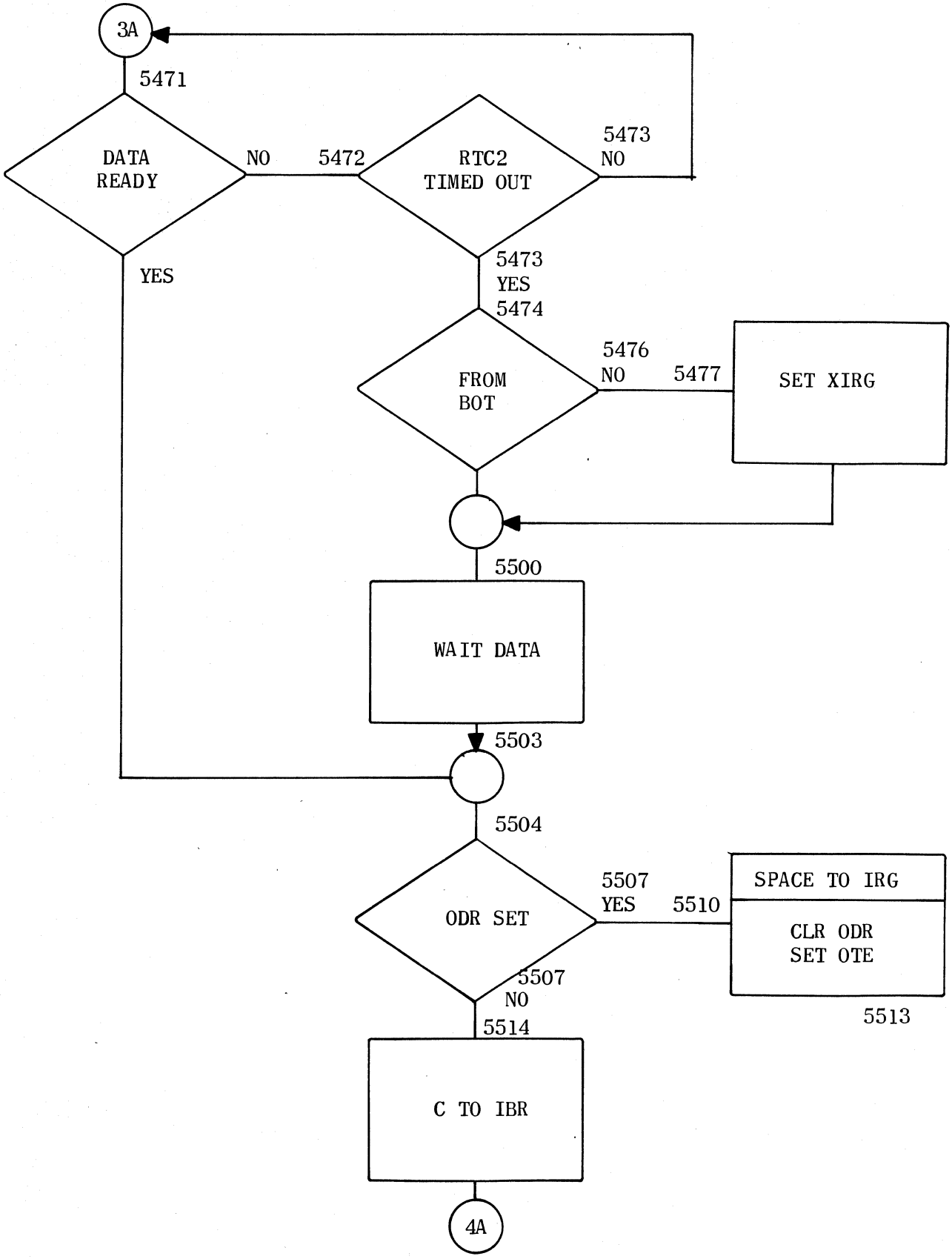


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 3 of 11)

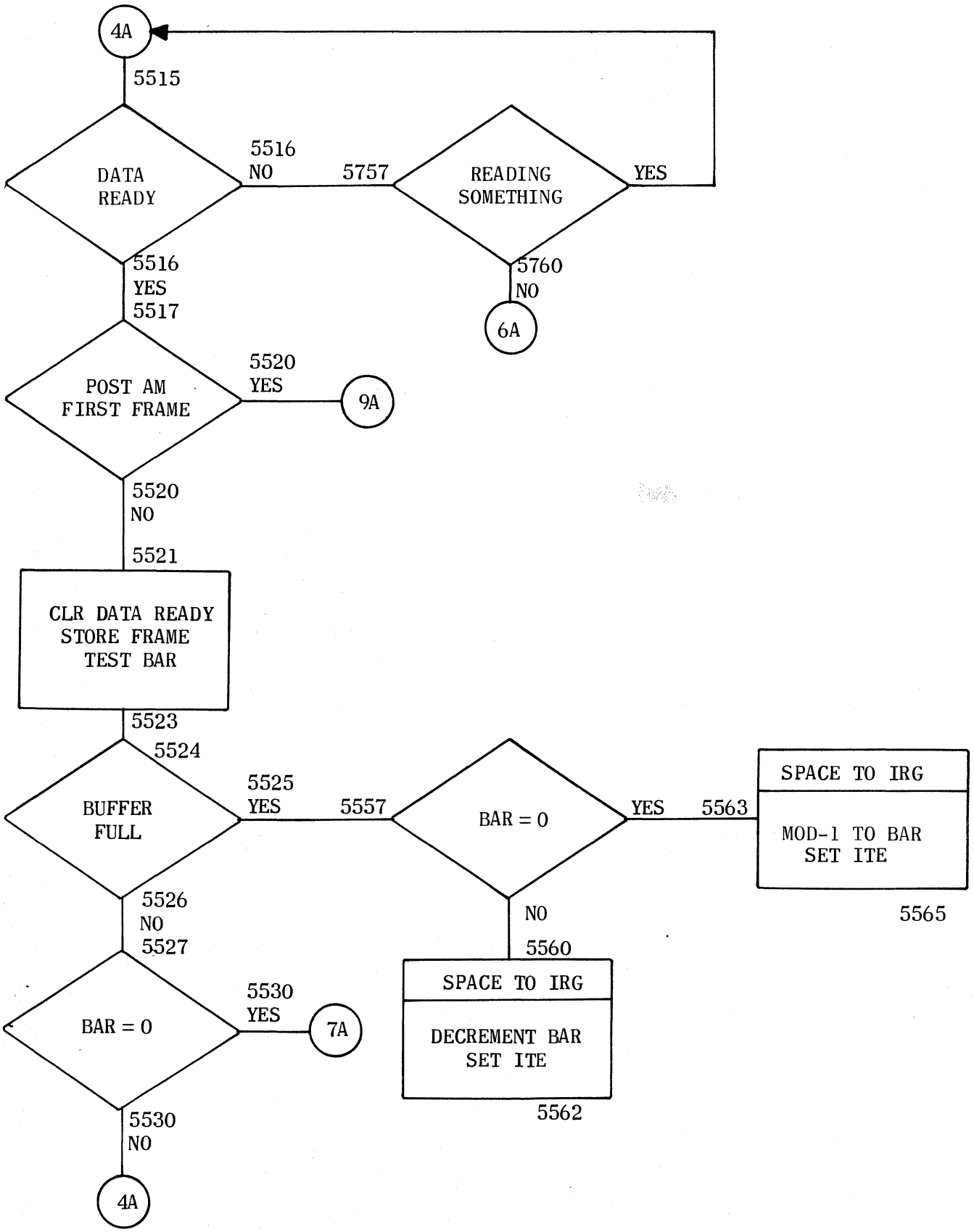


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 4 of 11)

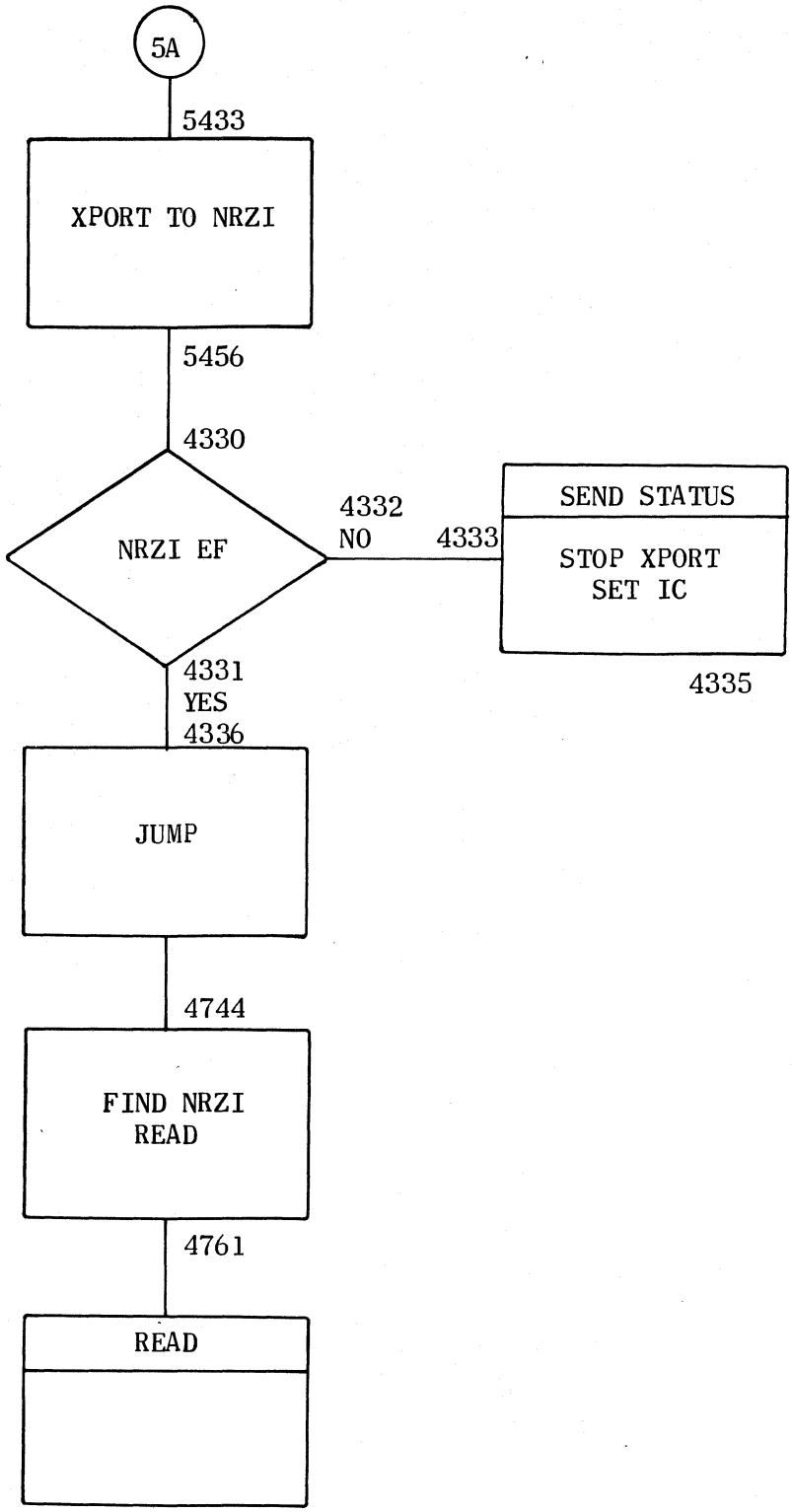


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 5 of 11)

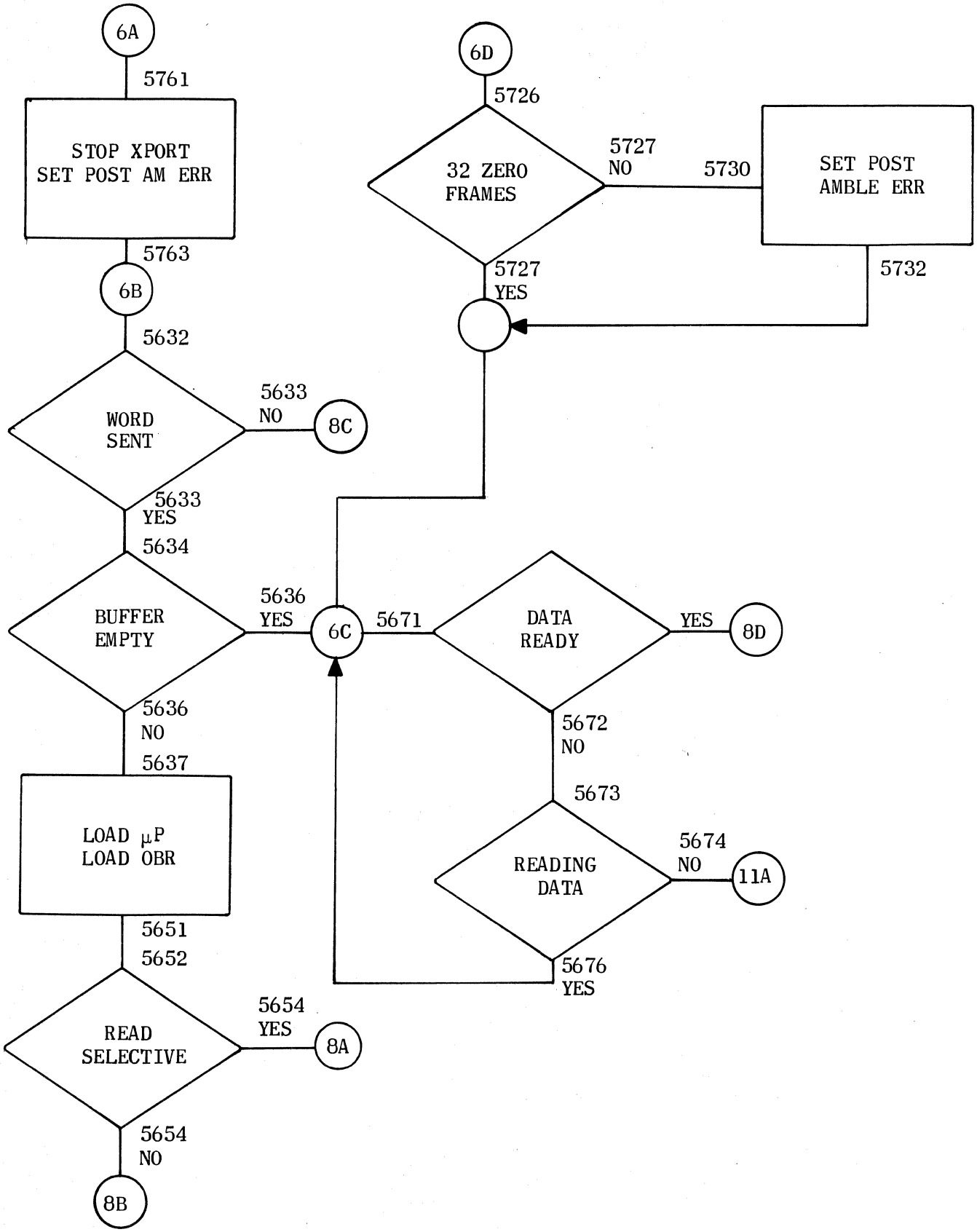


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 6 of 11)

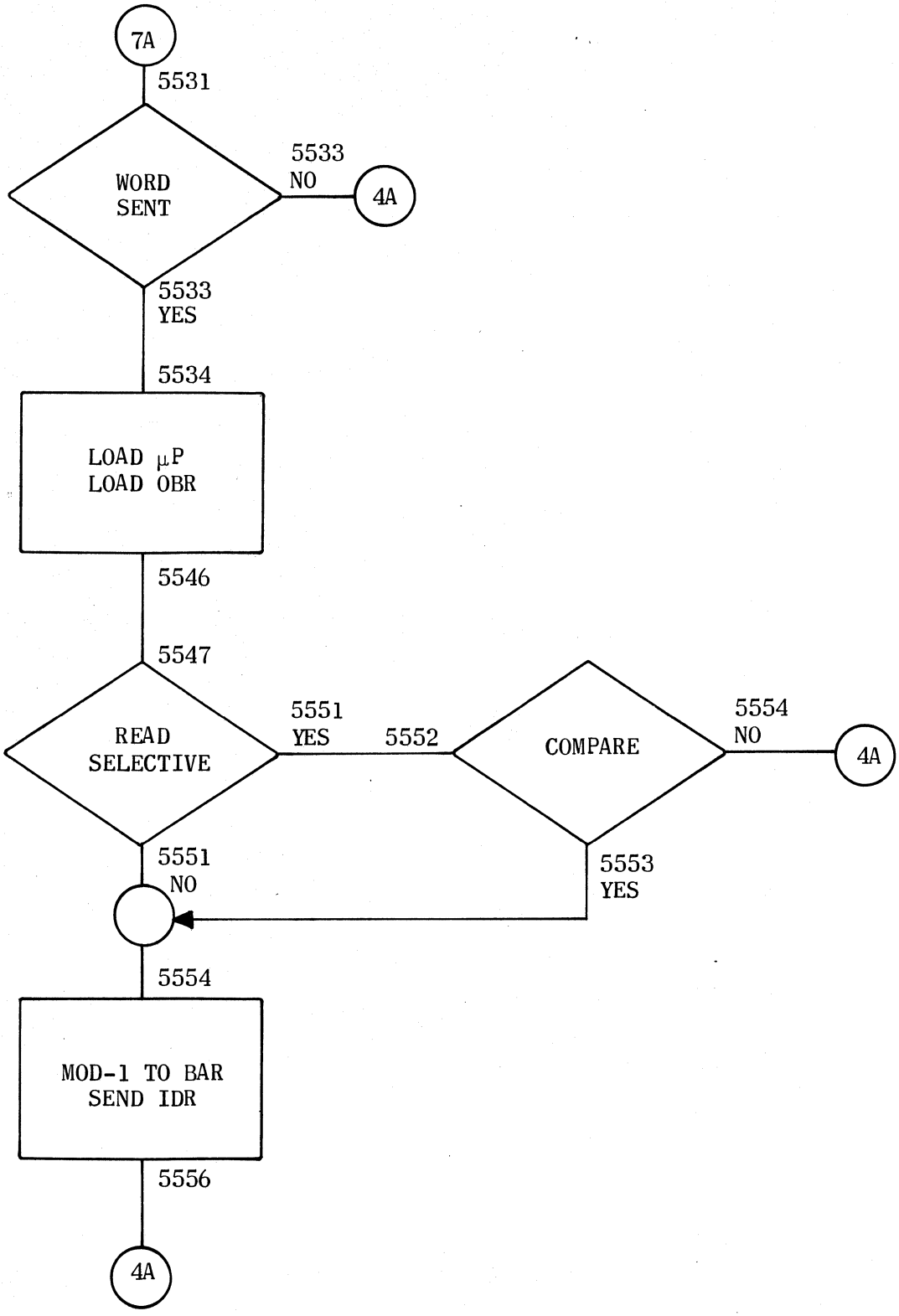


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 7 of 11)

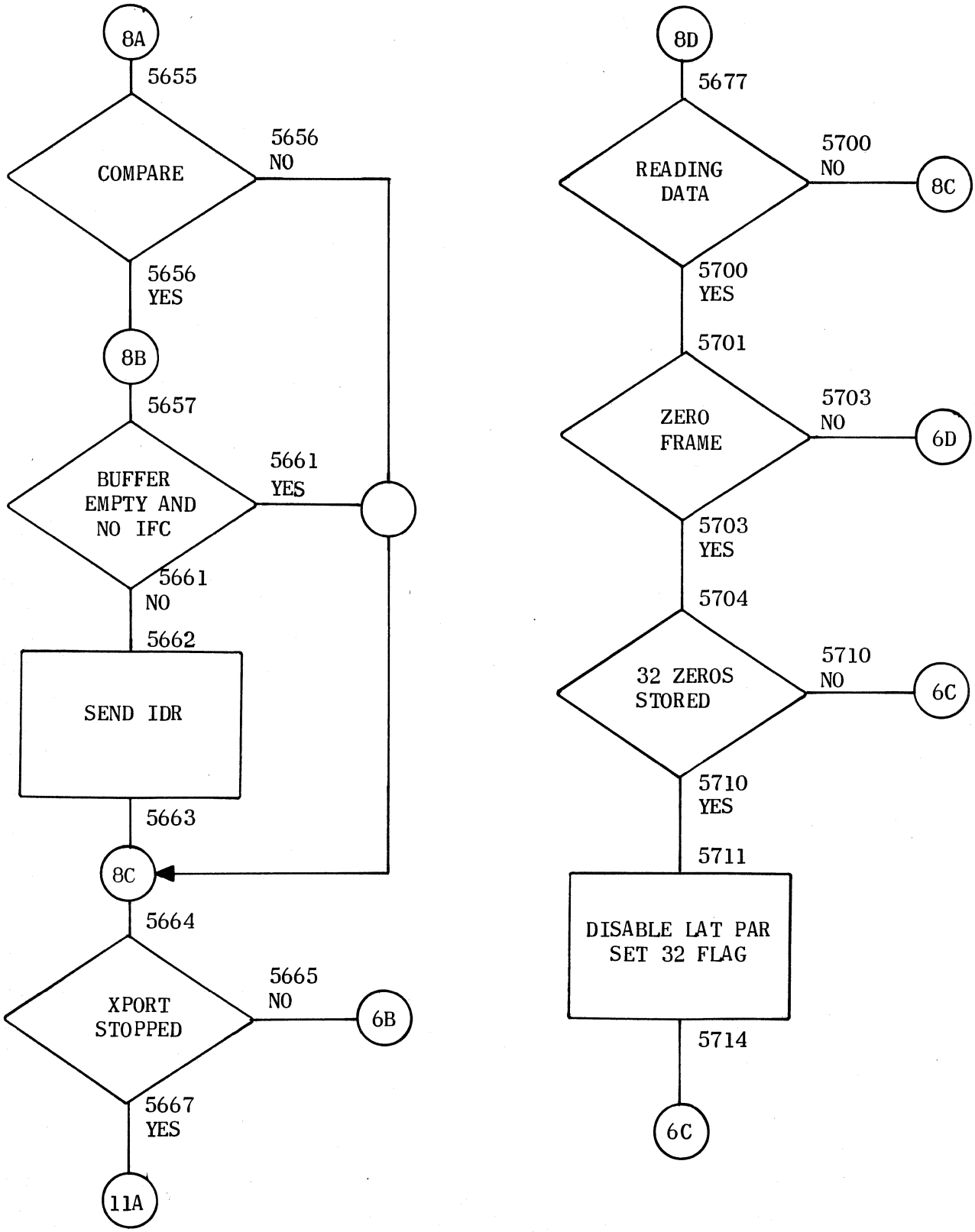


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 8 of 11)

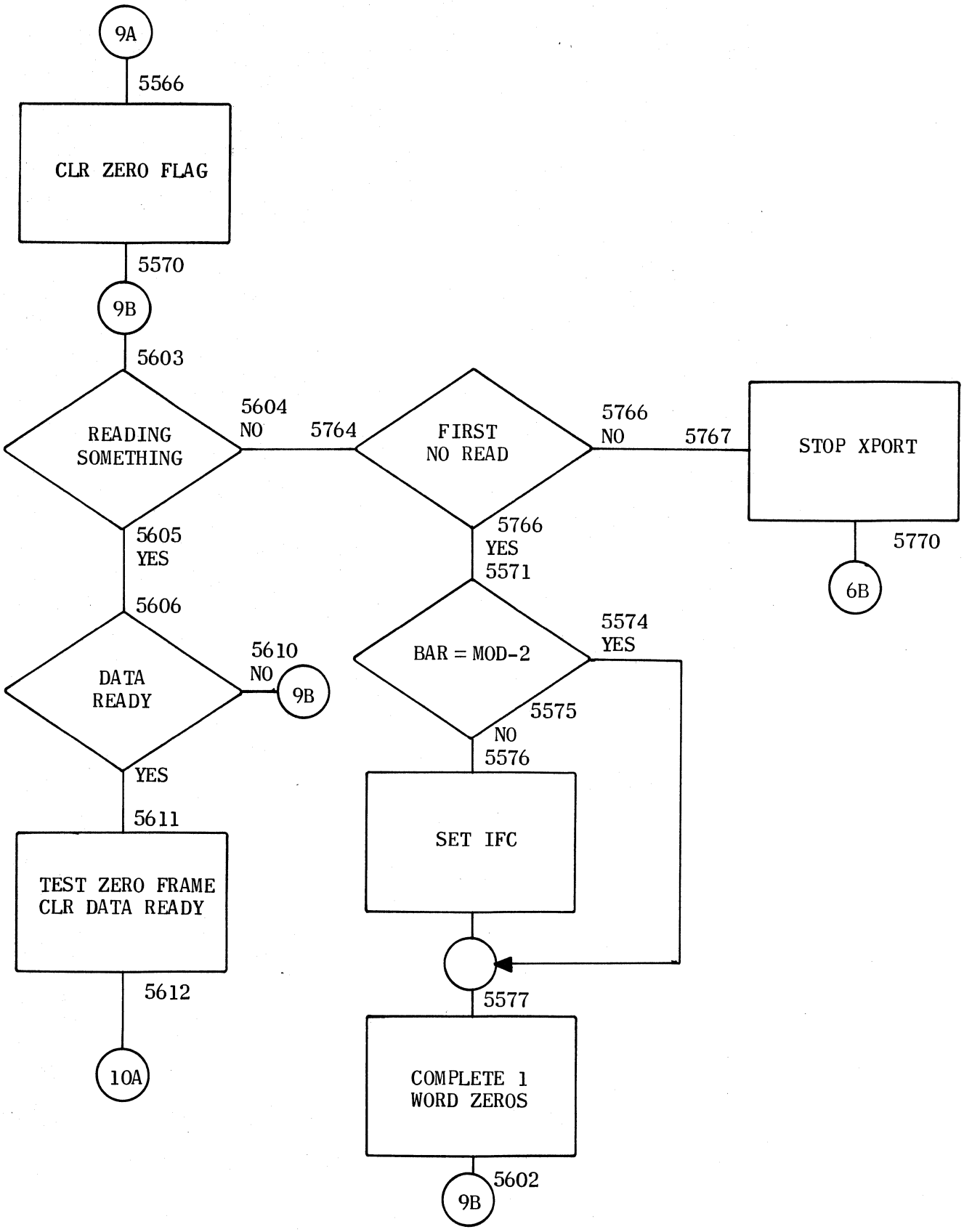


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 9 of 11)

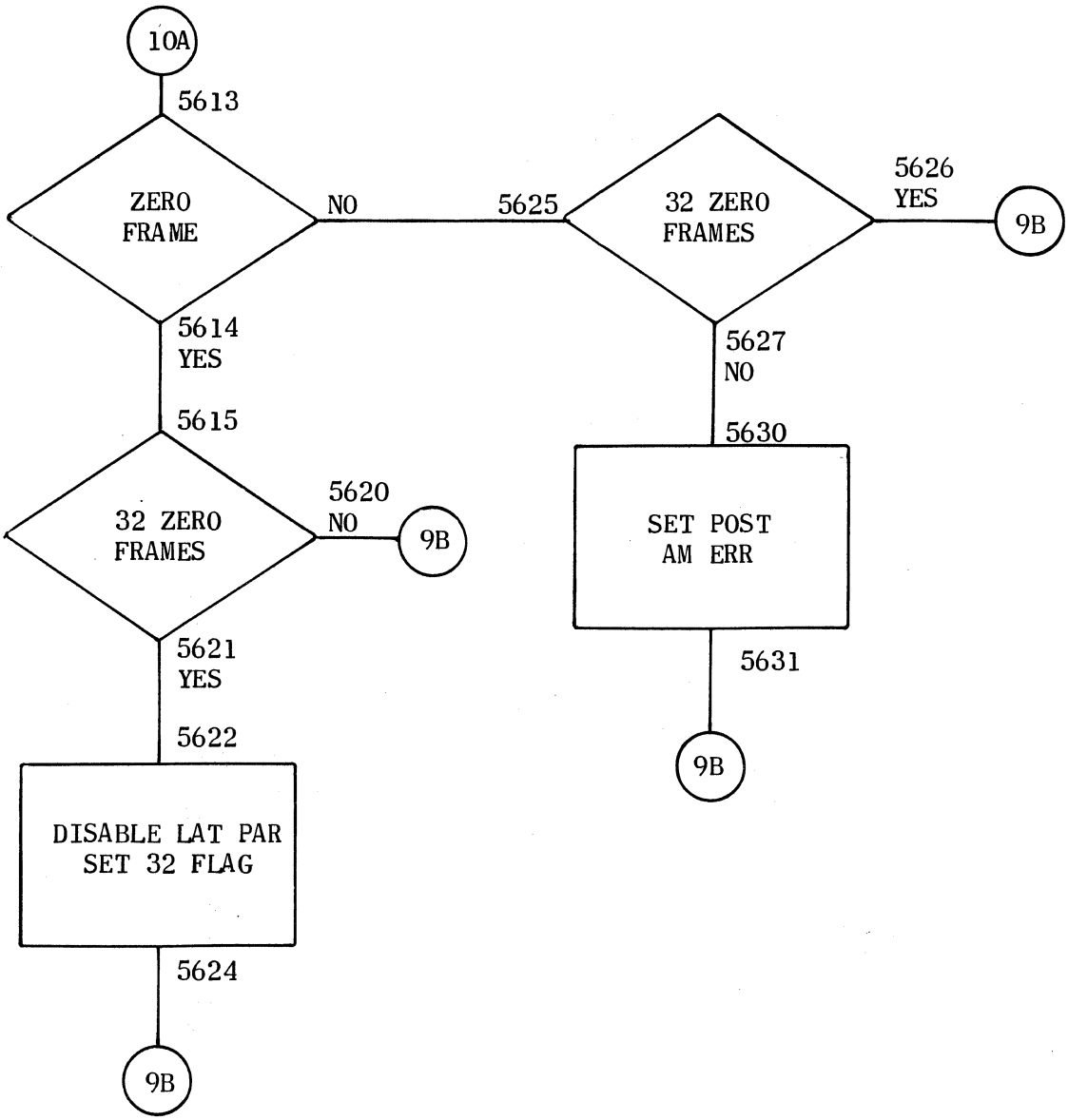


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 10 of 11)

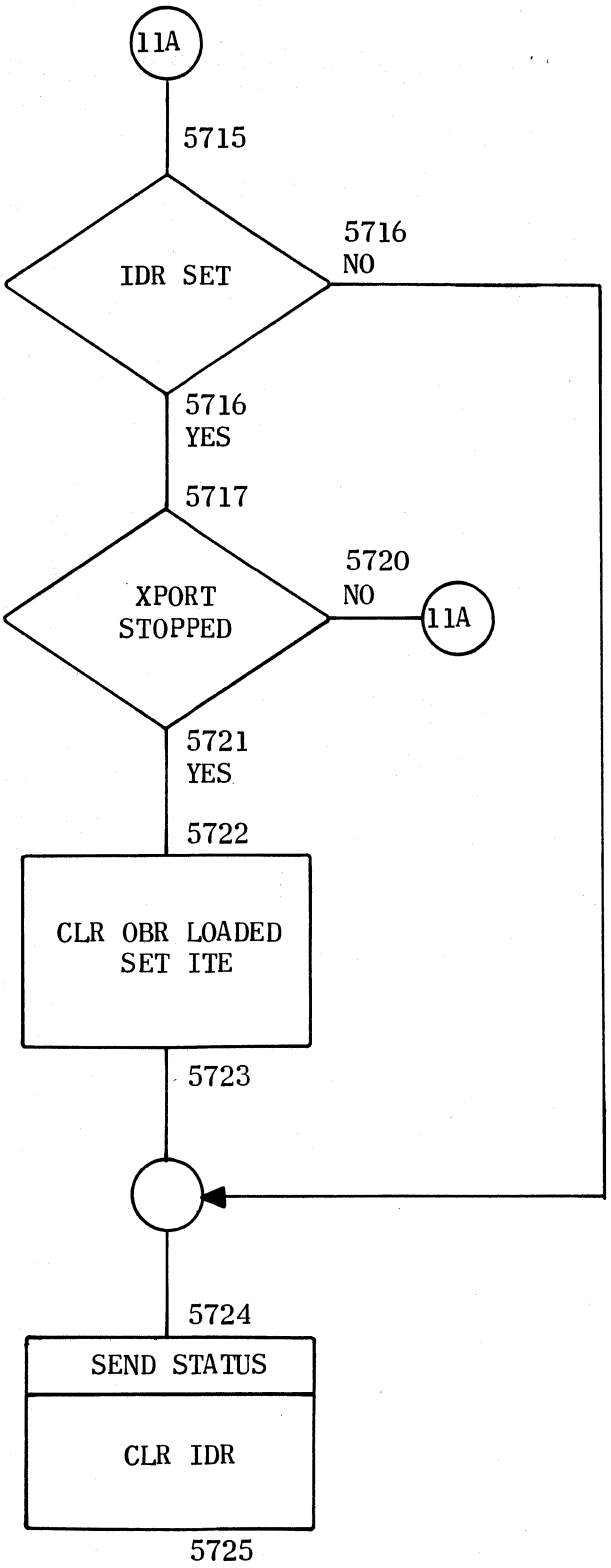


Figure 4-85. PE Read Sequence Flow Diagram (Sheet 11 of 11)

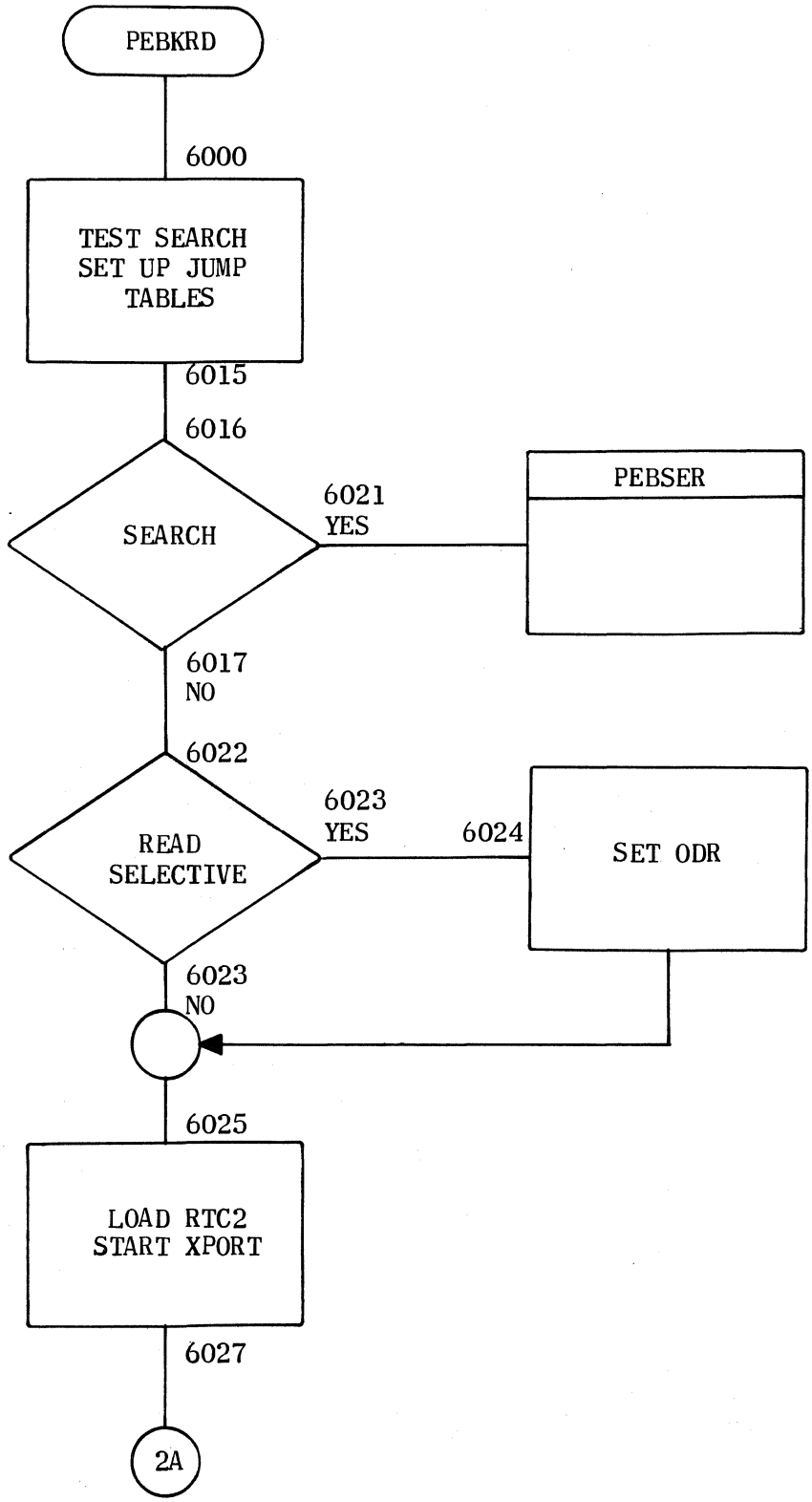


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 1 of 9)

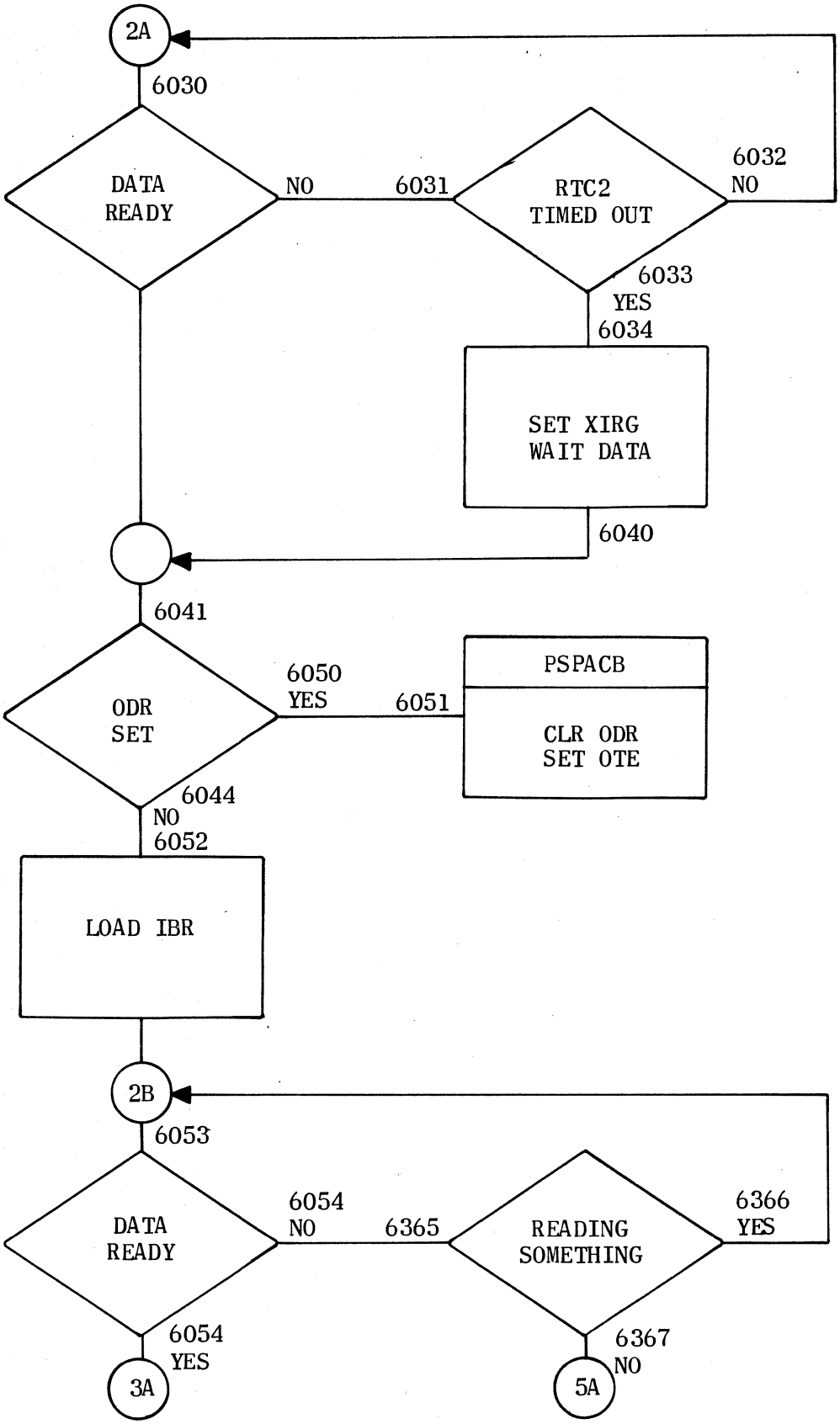


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 2 of 9)

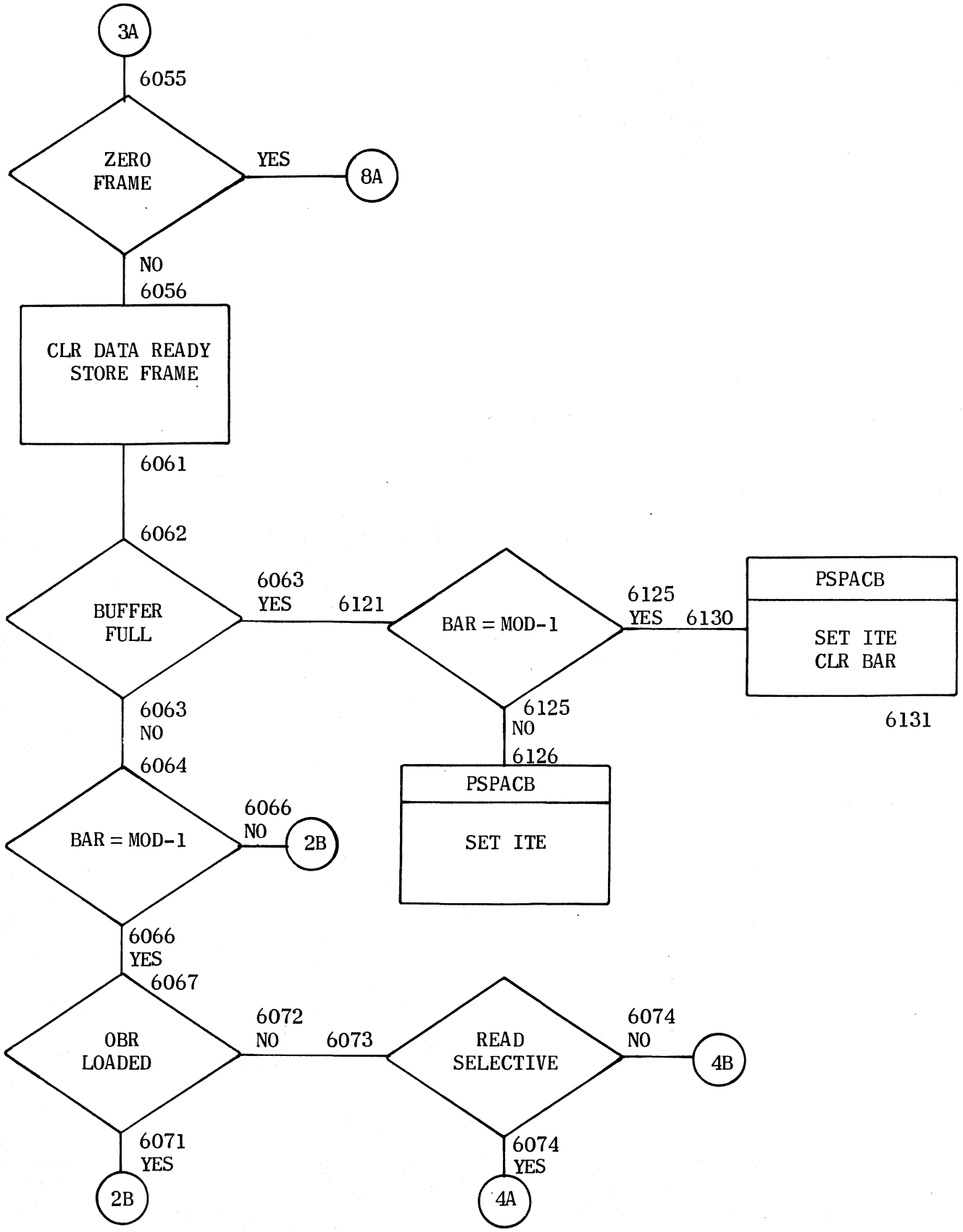


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 3 of 9)

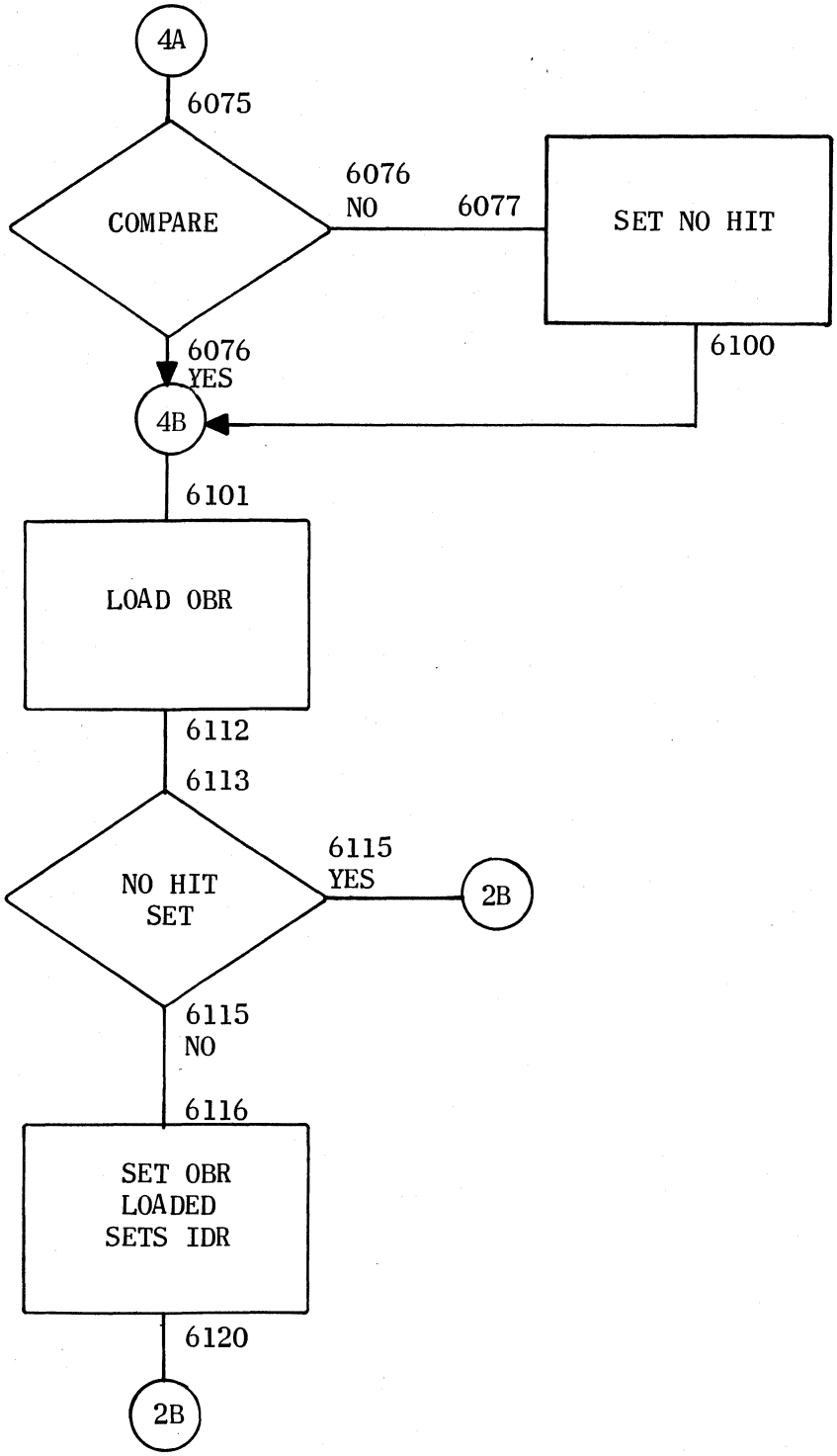


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 4 of 9)

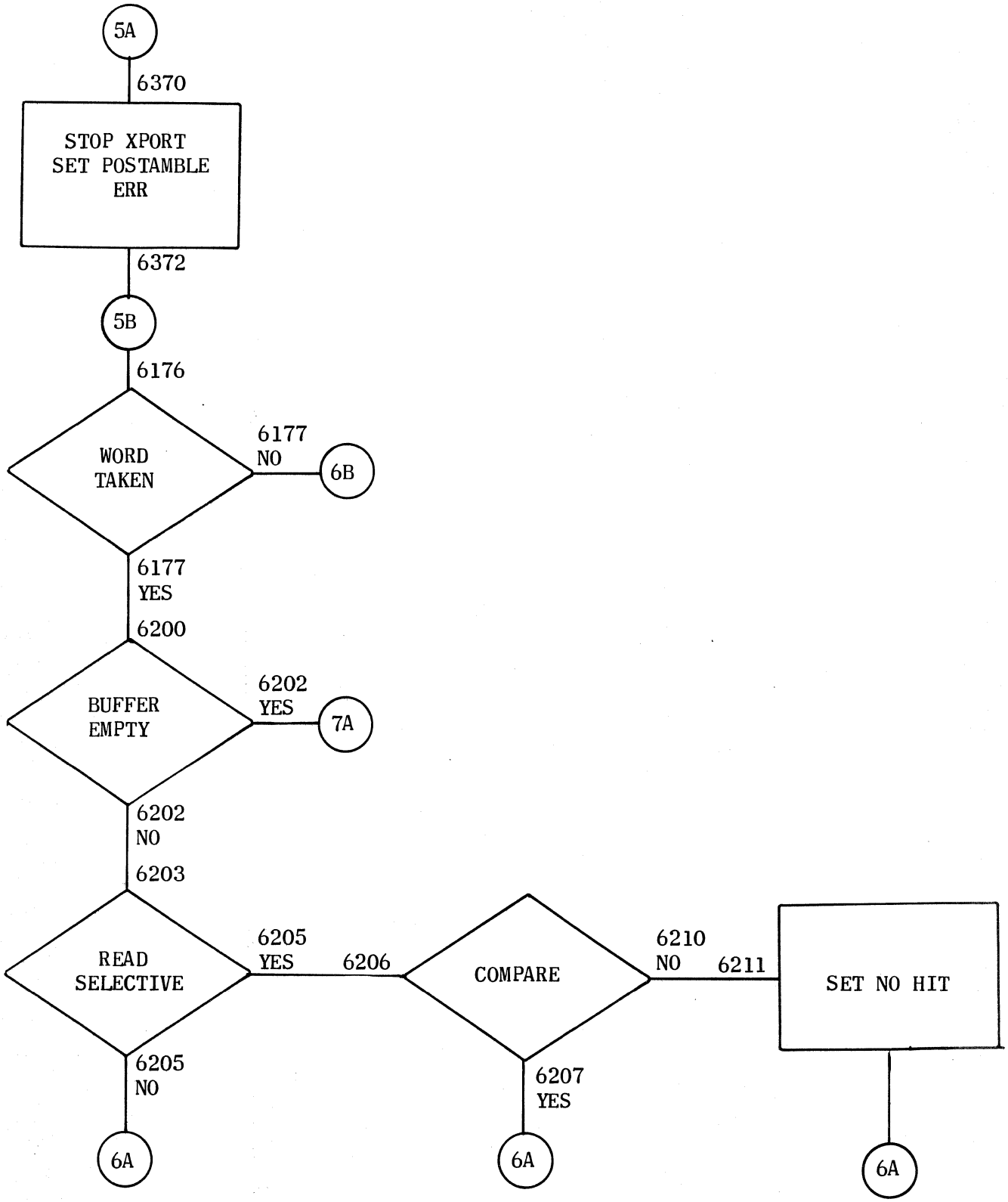


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 5 of 9)

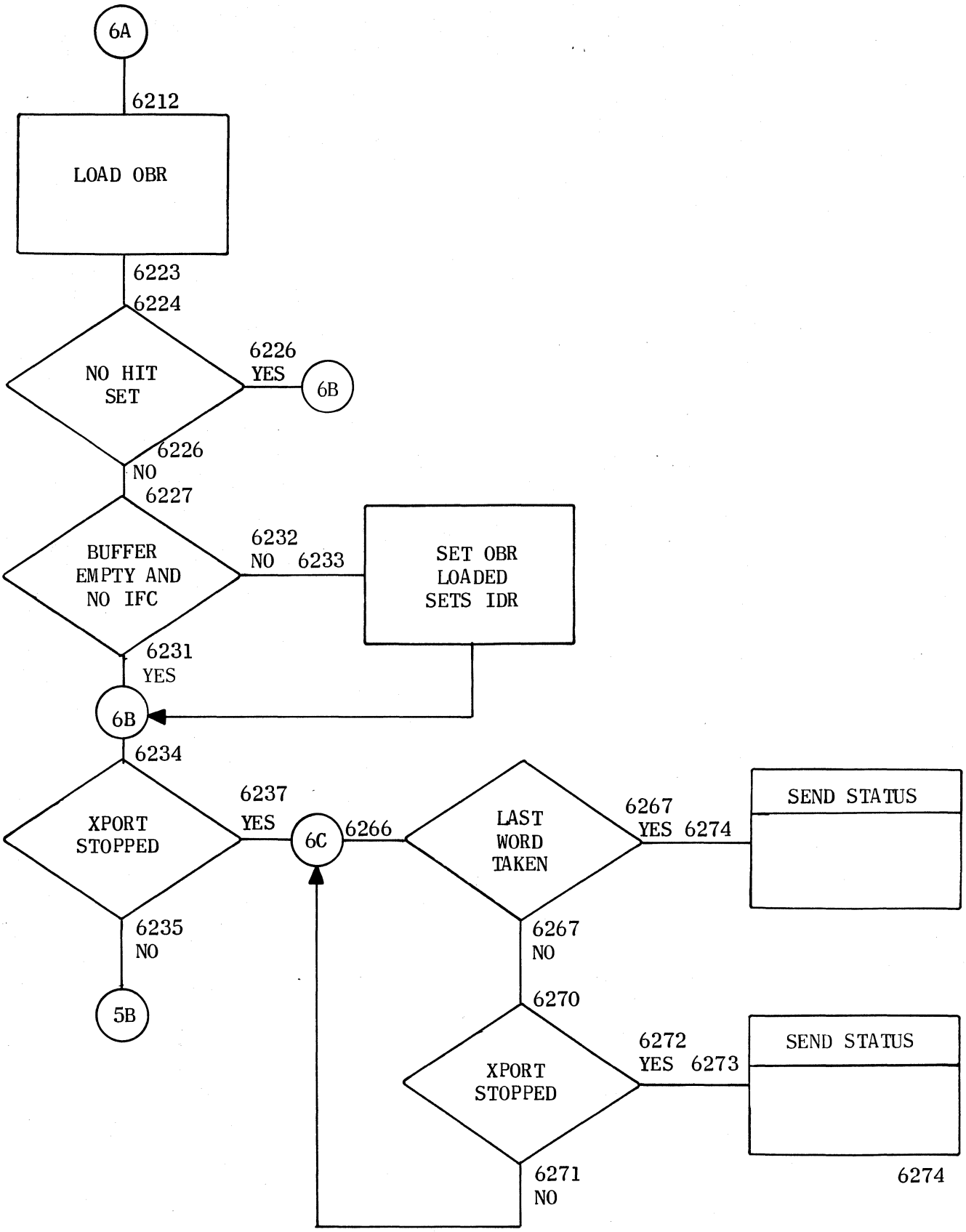


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 6 of 9)

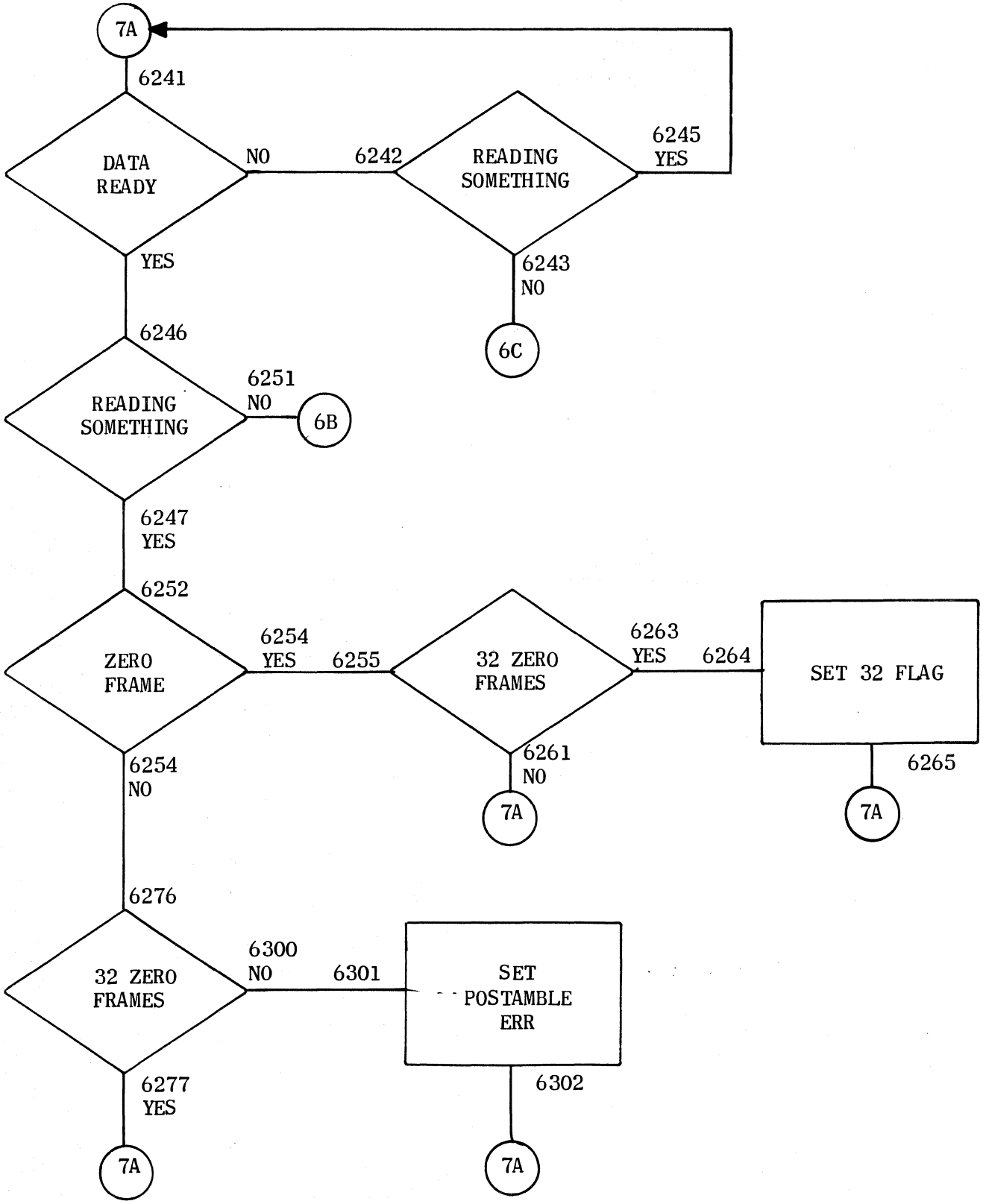


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 7 of 9)

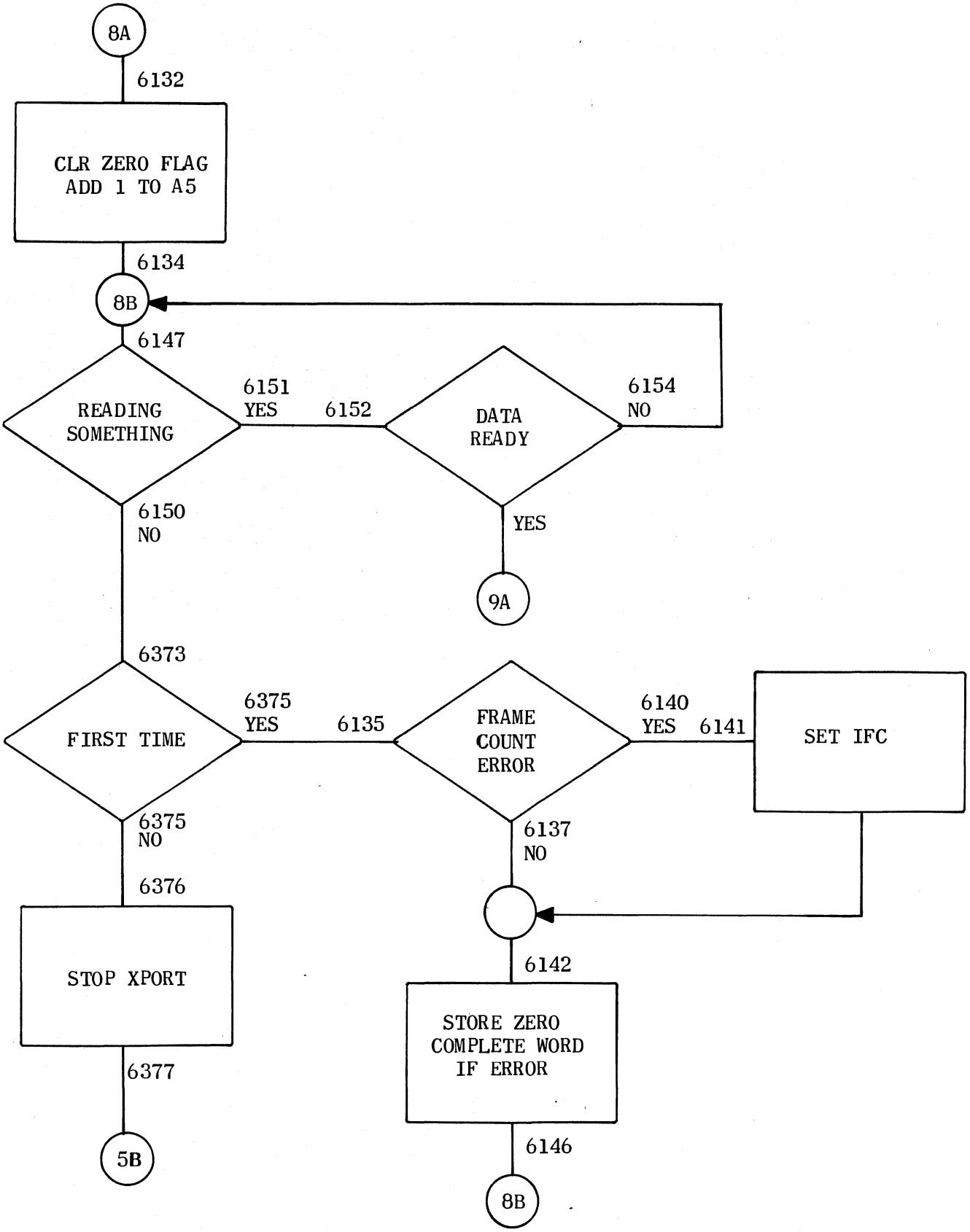


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 8 of 9)

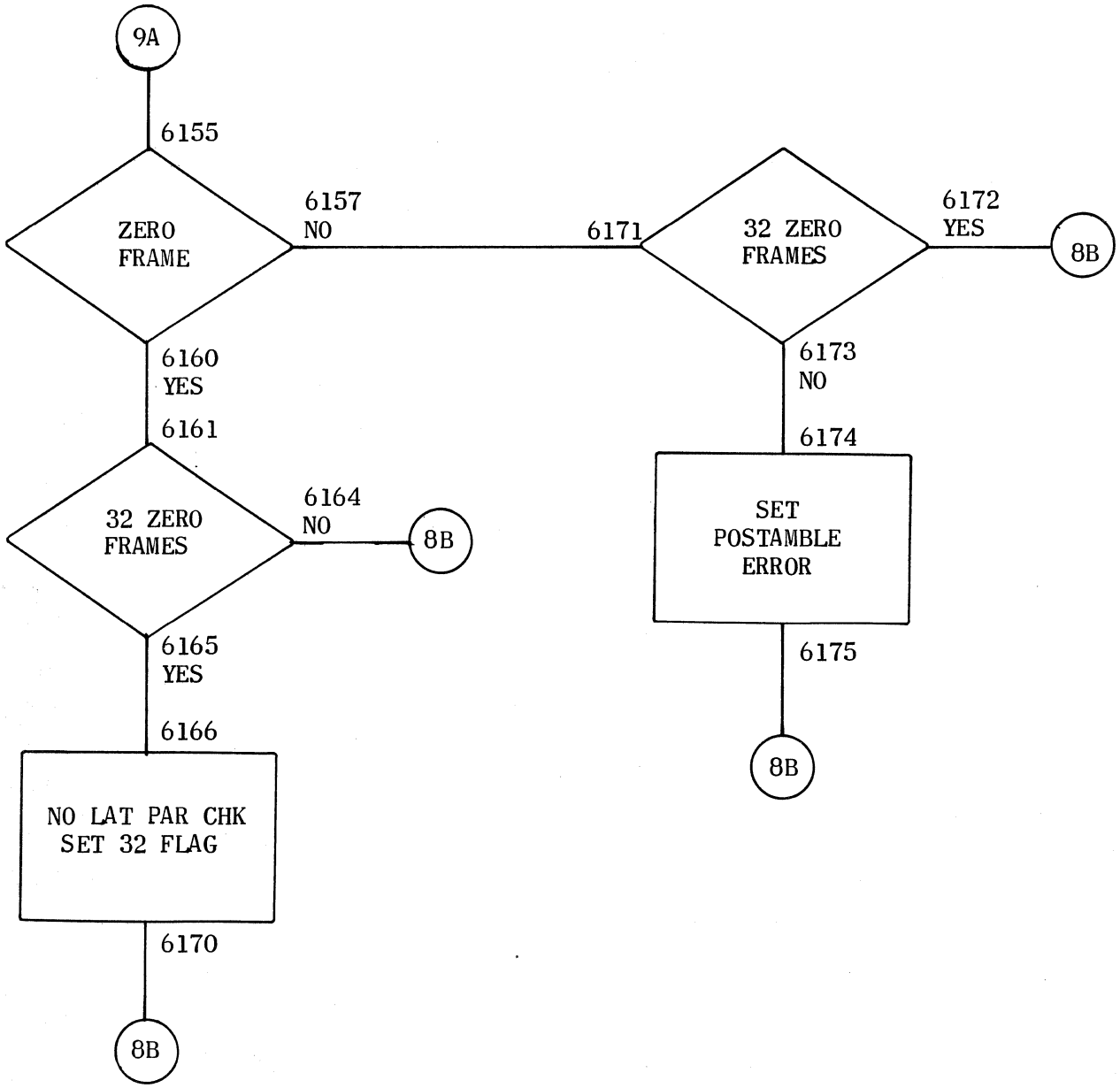


Figure 4-86. PE Back Read Sequence Flow Diagram (Sheet 9 of 9)

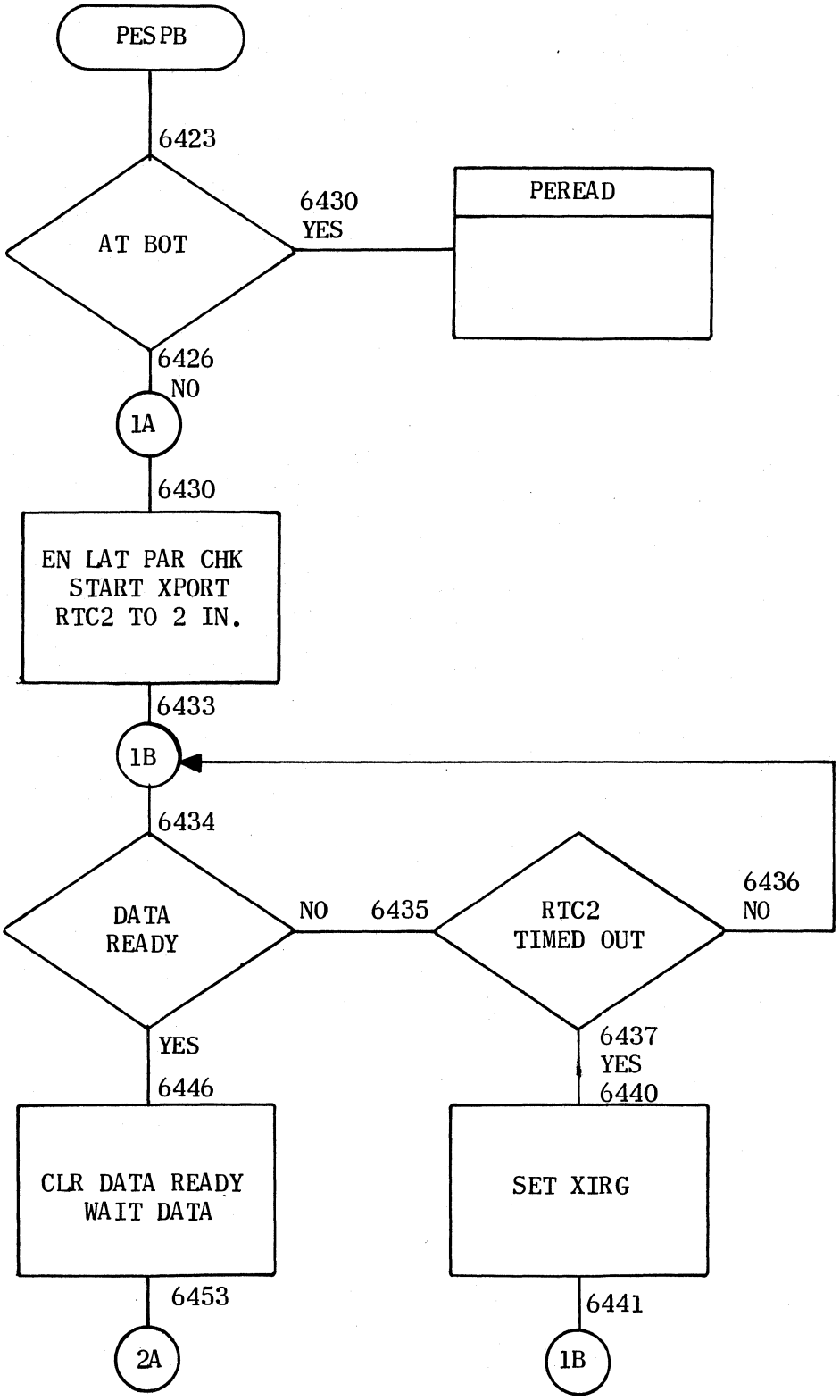


Figure 4-87. PE Space/Backspace Block Sequence Flow Diagram (Sheet 1 of 7)

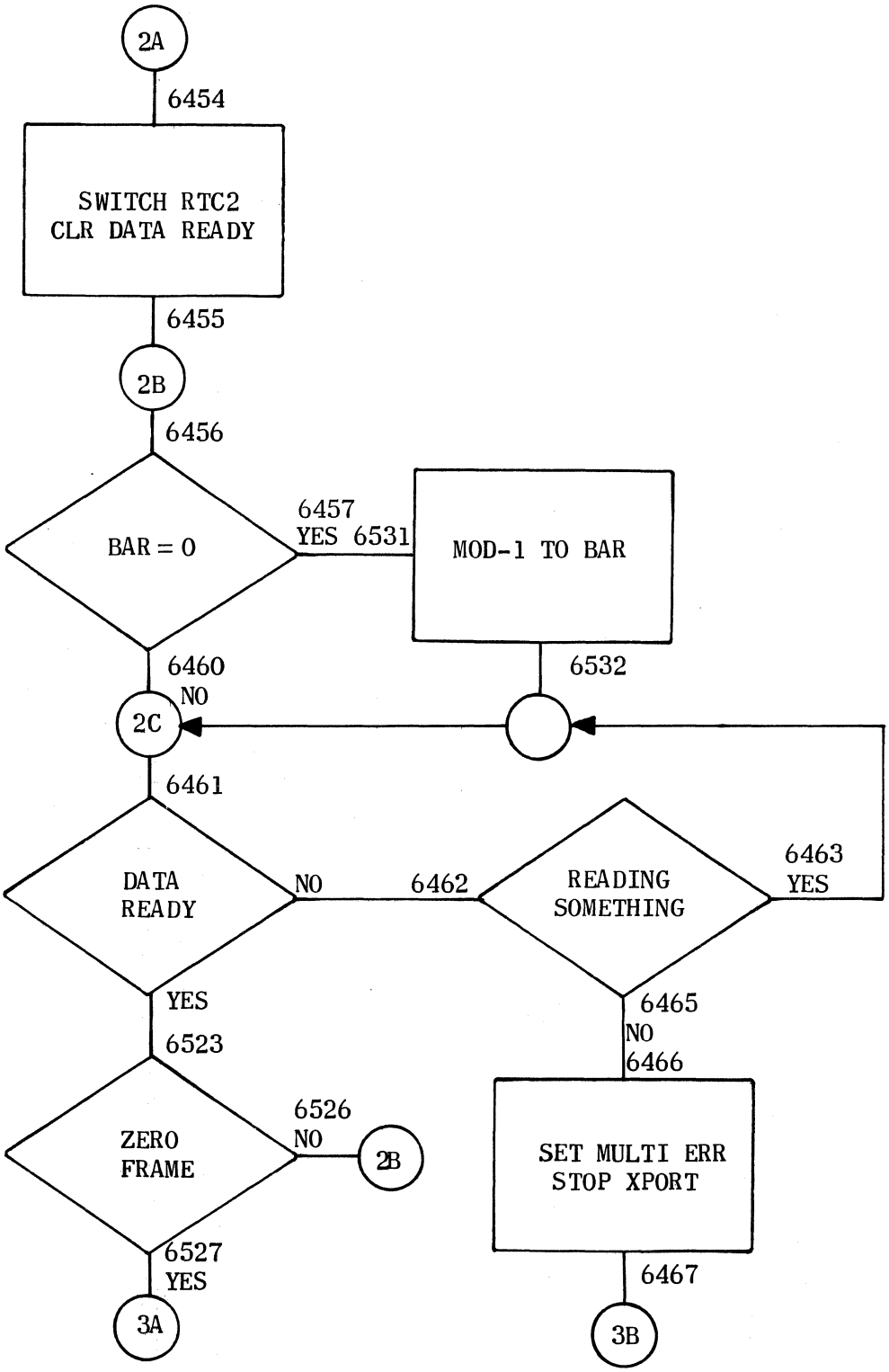


Figure 4-87. PE Space/Backspace Block Sequence Flow Diagram (Sheet 2 of 7)

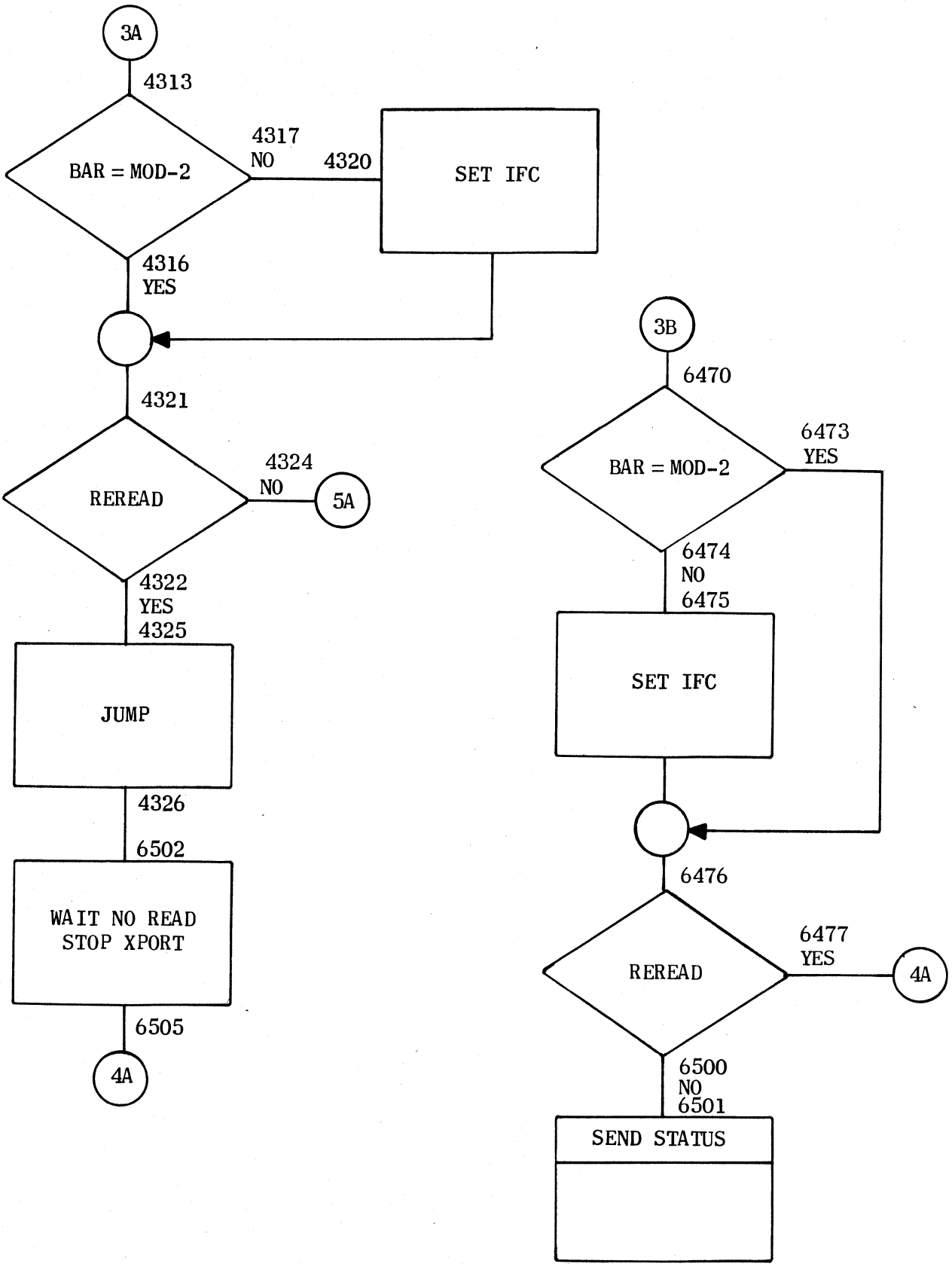


Figure 4-87. PE Space/Backspace Block Sequence Flow Diagram (Sheet 3 of 7)

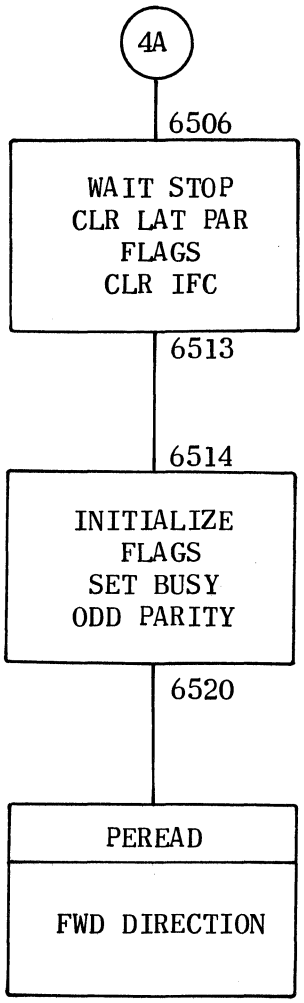


Figure 4-87. PE Space/Backspace Block Sequence Flow Diagram (Sheet 4 of 7)

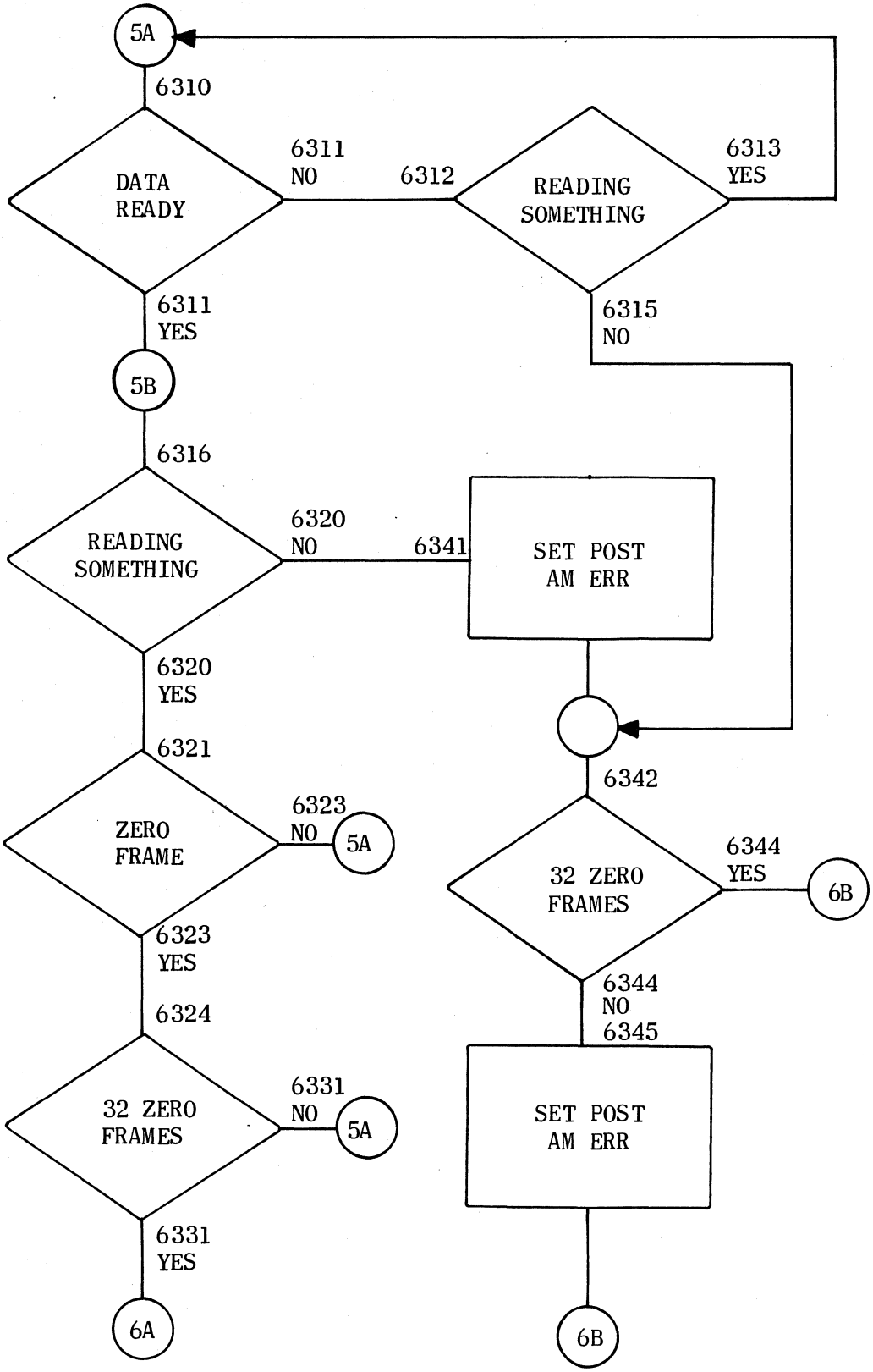


Figure 4-87. PE Space/Backspace Block Sequence Flow Diagram (Sheet 5 of 7)

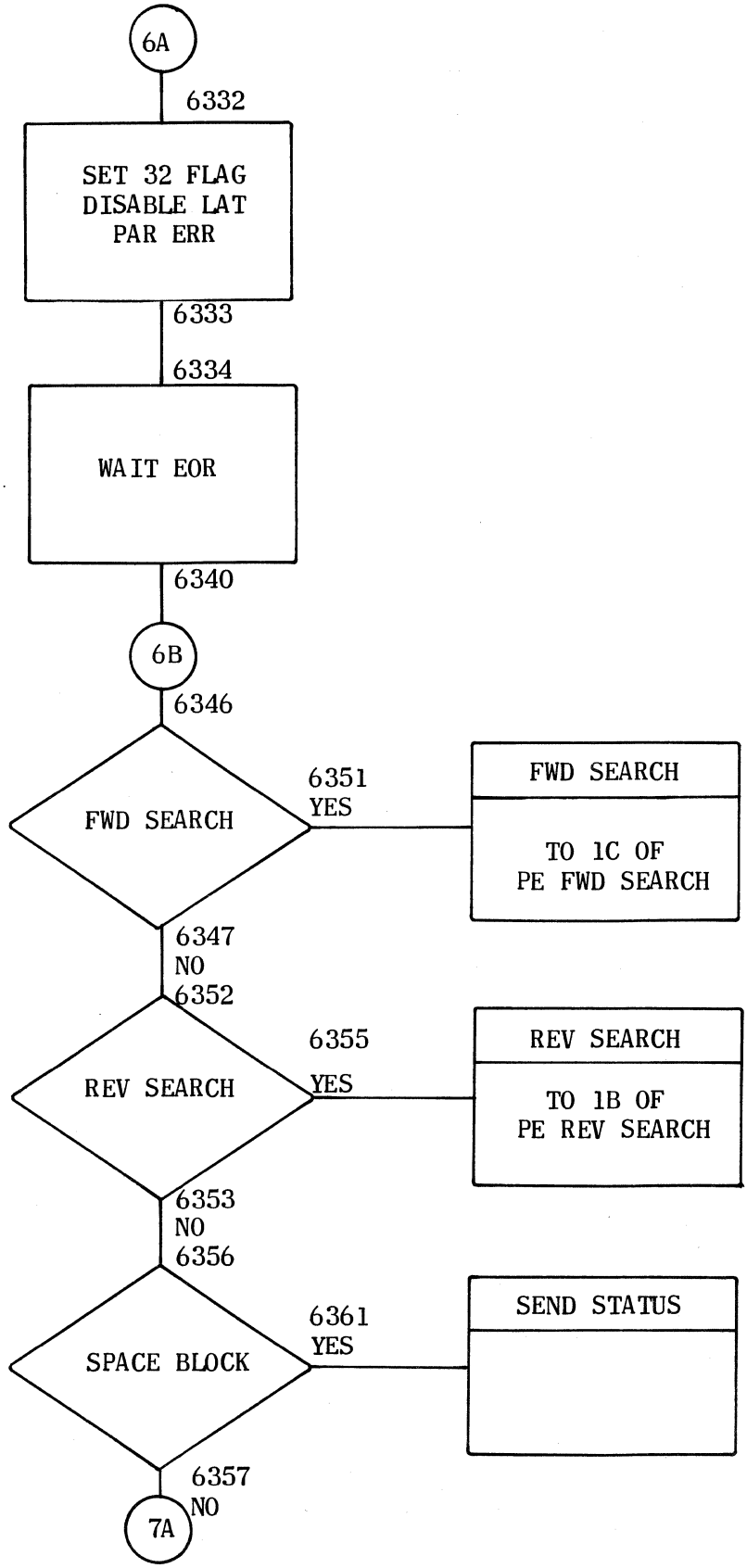


Figure 4-87. PE Space/Backspace Block Sequence Flow Diagram (Sheet 6 of 7)

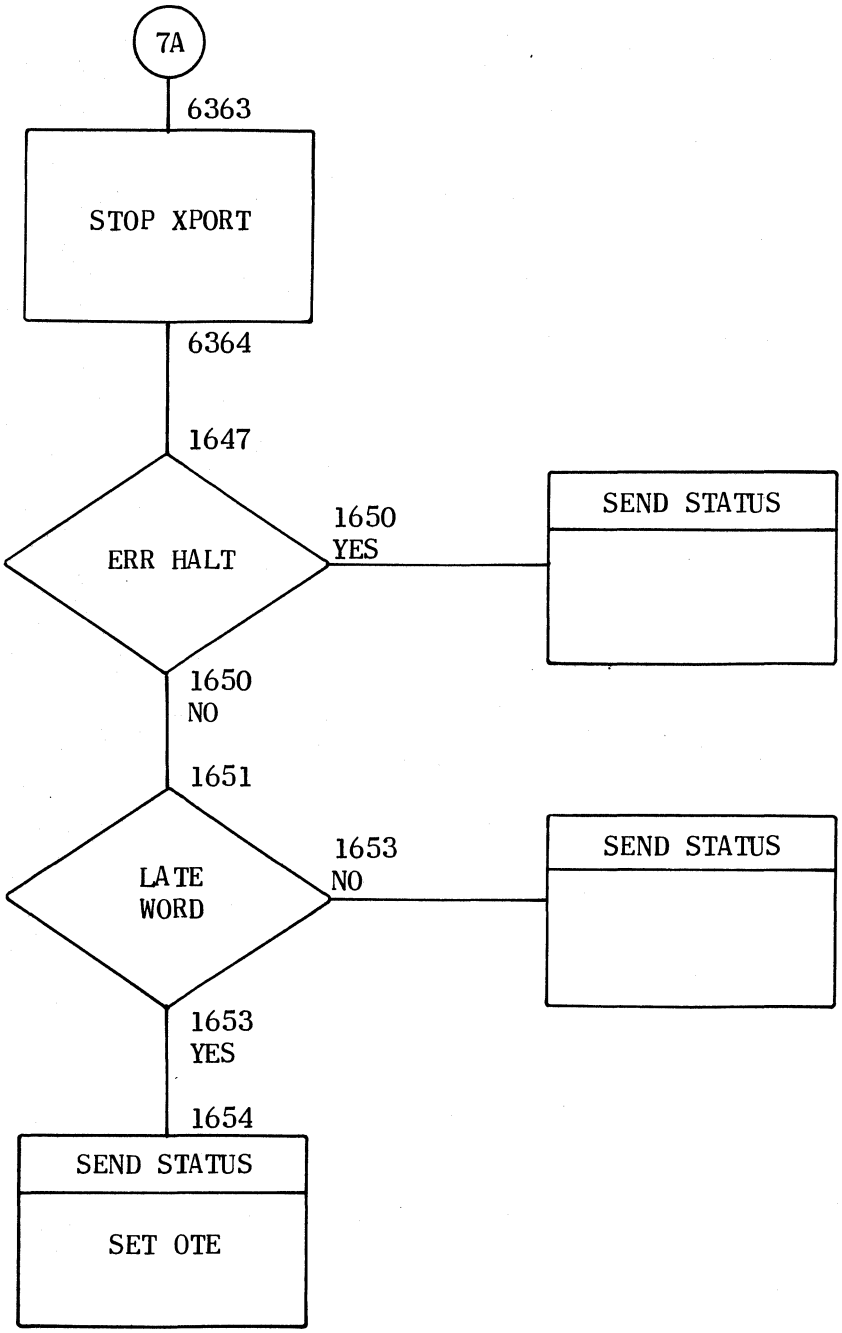


Figure 4-87. PE Space/Backspace Block Sequence Flow Diagram (Sheet 7 of 7)

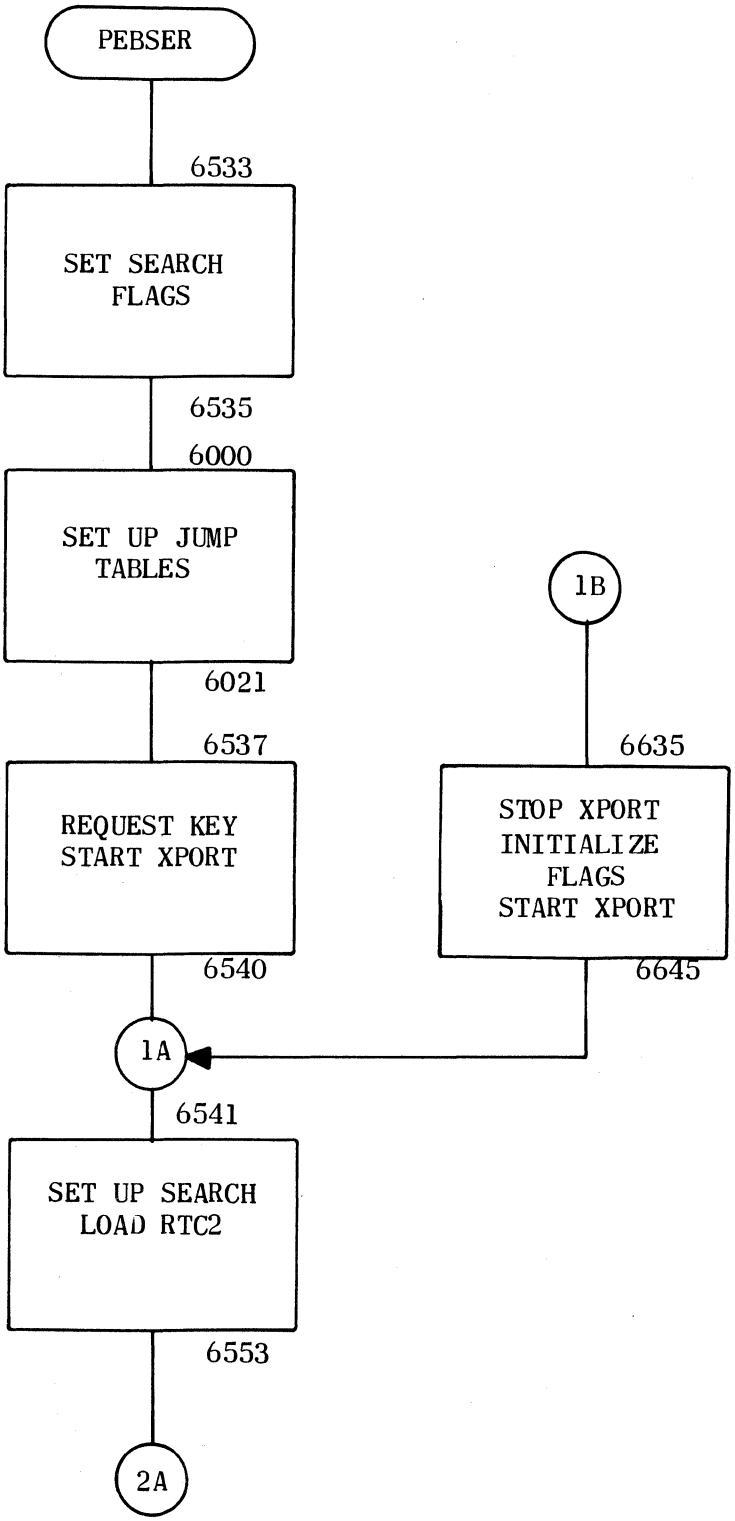


Figure 4-88. PE Back Search Sequence Flow Diagram (Sheet 1 of 3)

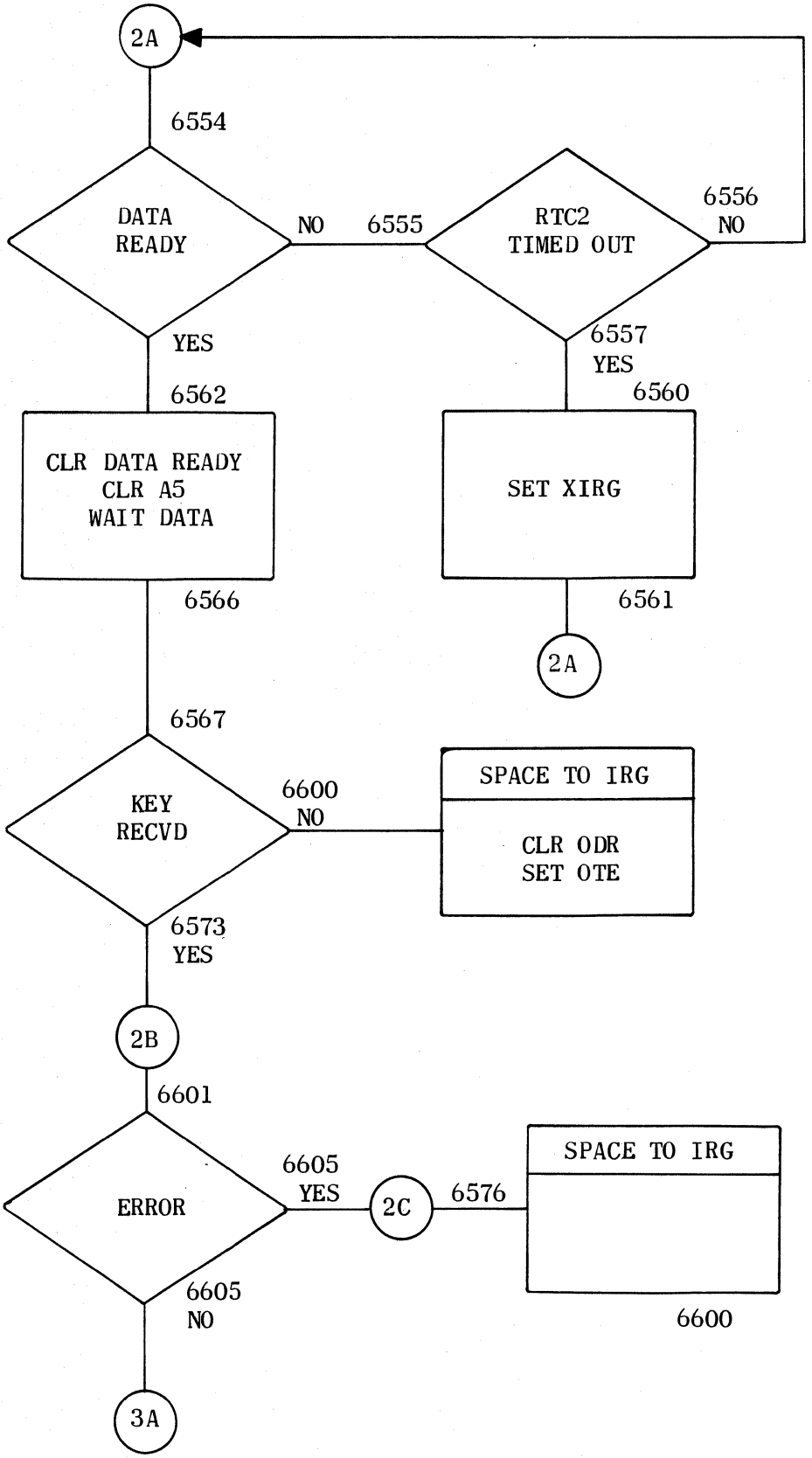


Figure 4-88. PE Back Search Sequence Flow Diagram (Sheet 2 of 3)

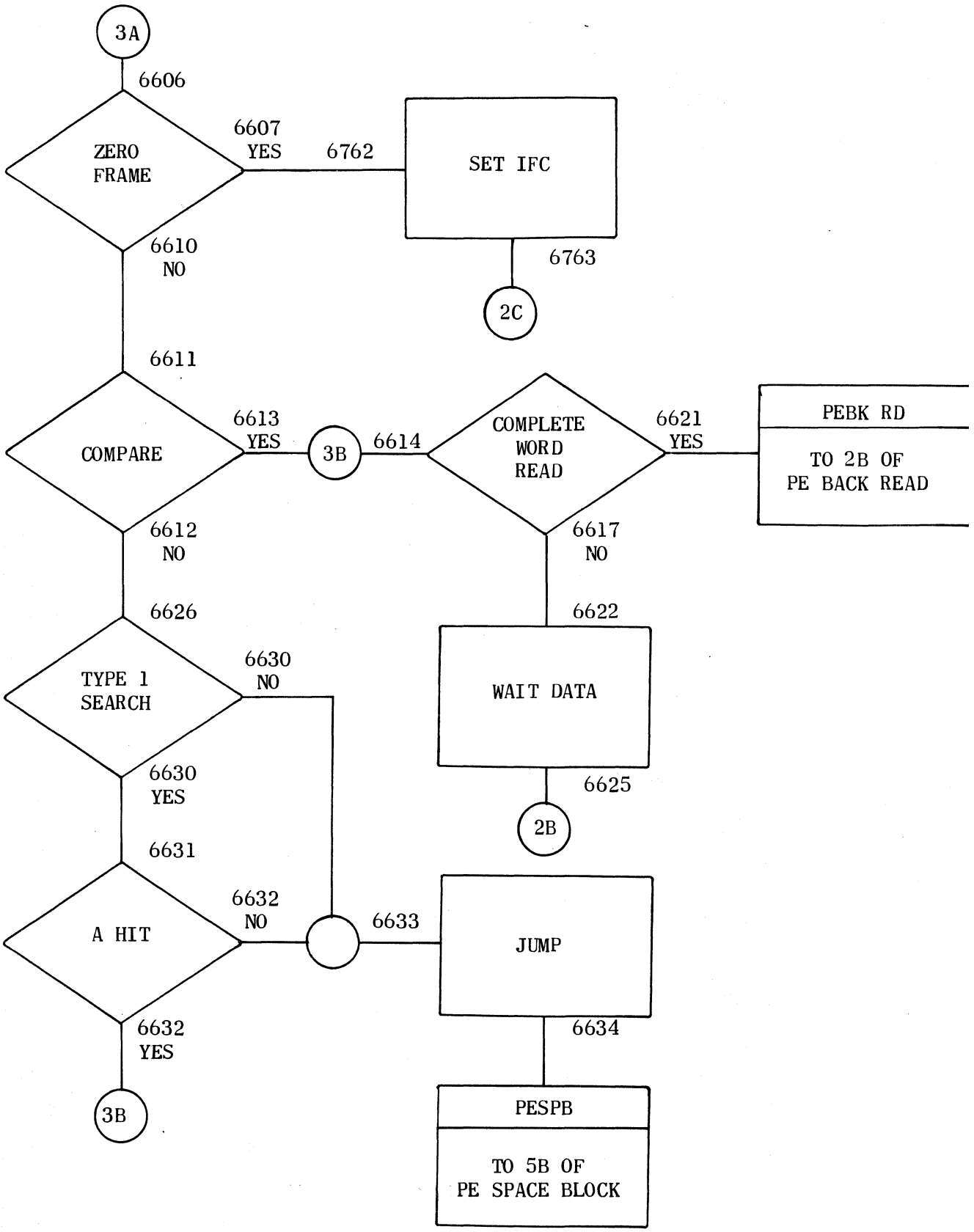


Figure 4-88. PE Back Search Sequence Flow Diagram (Sheet 3 of 3)

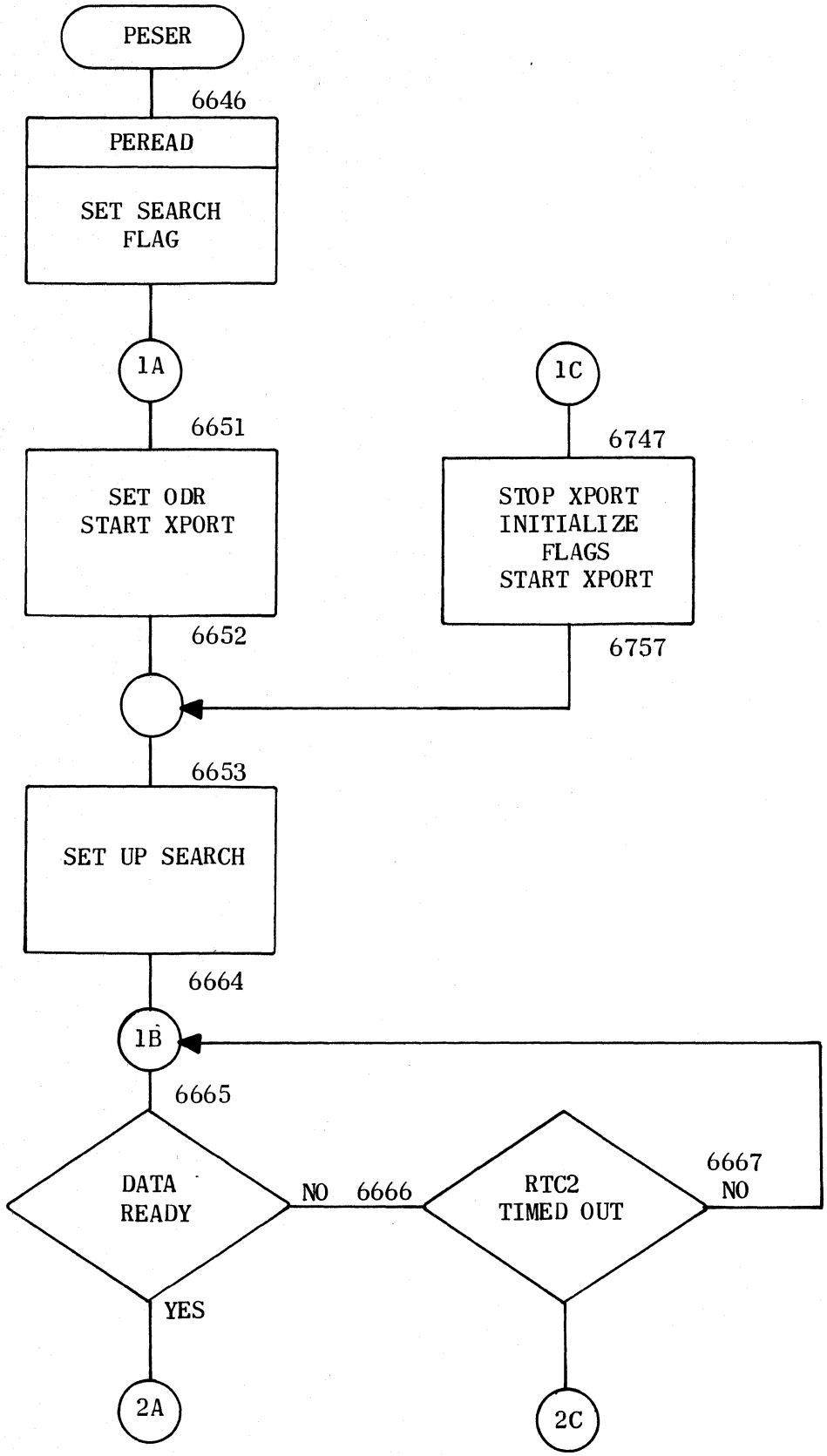


Figure 4-89. PE Search Sequence Flow Diagram (Sheet 1 of 3)

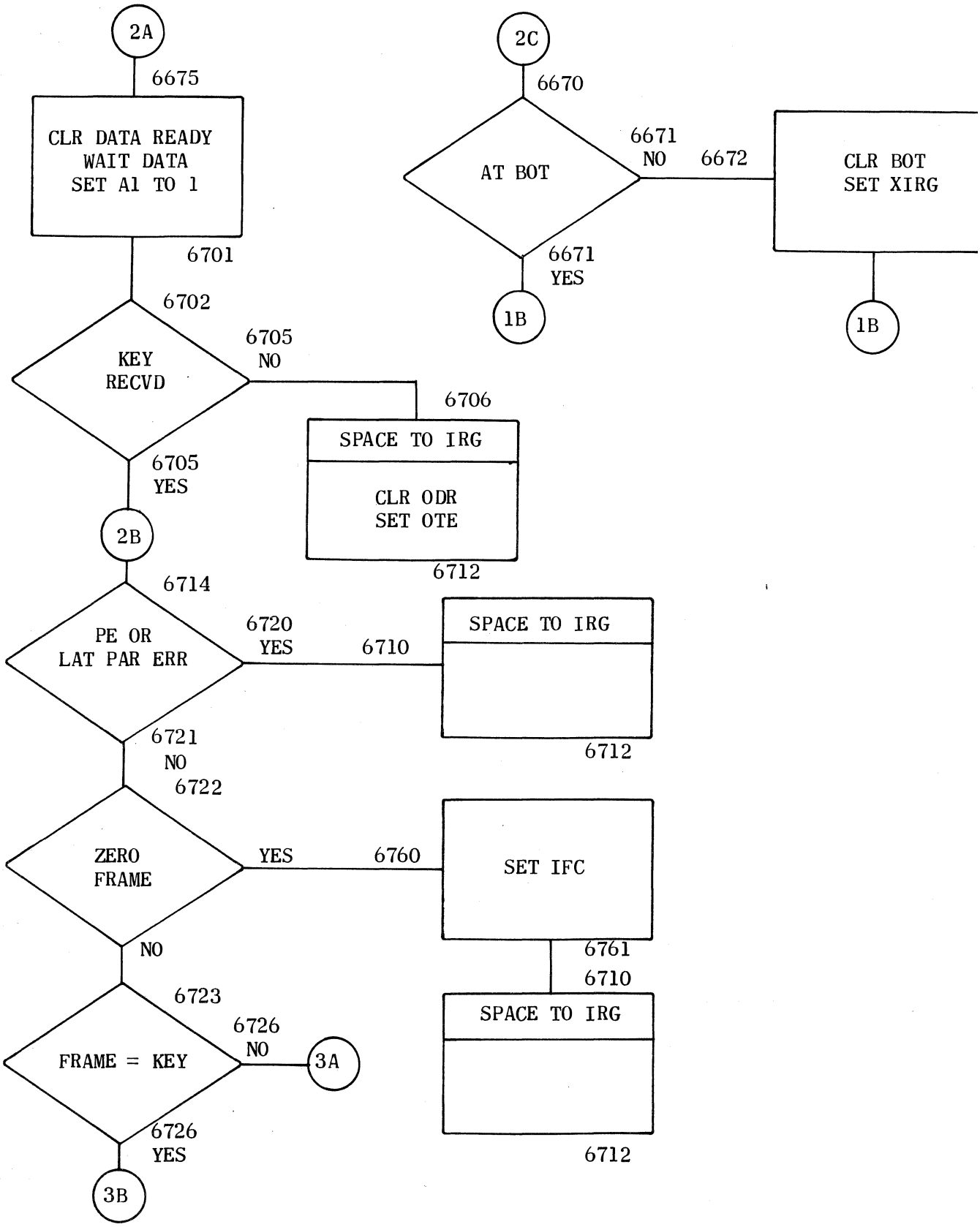


Figure 4-89. PE Search Sequence Flow Diagram (Sheet 2 of 3)

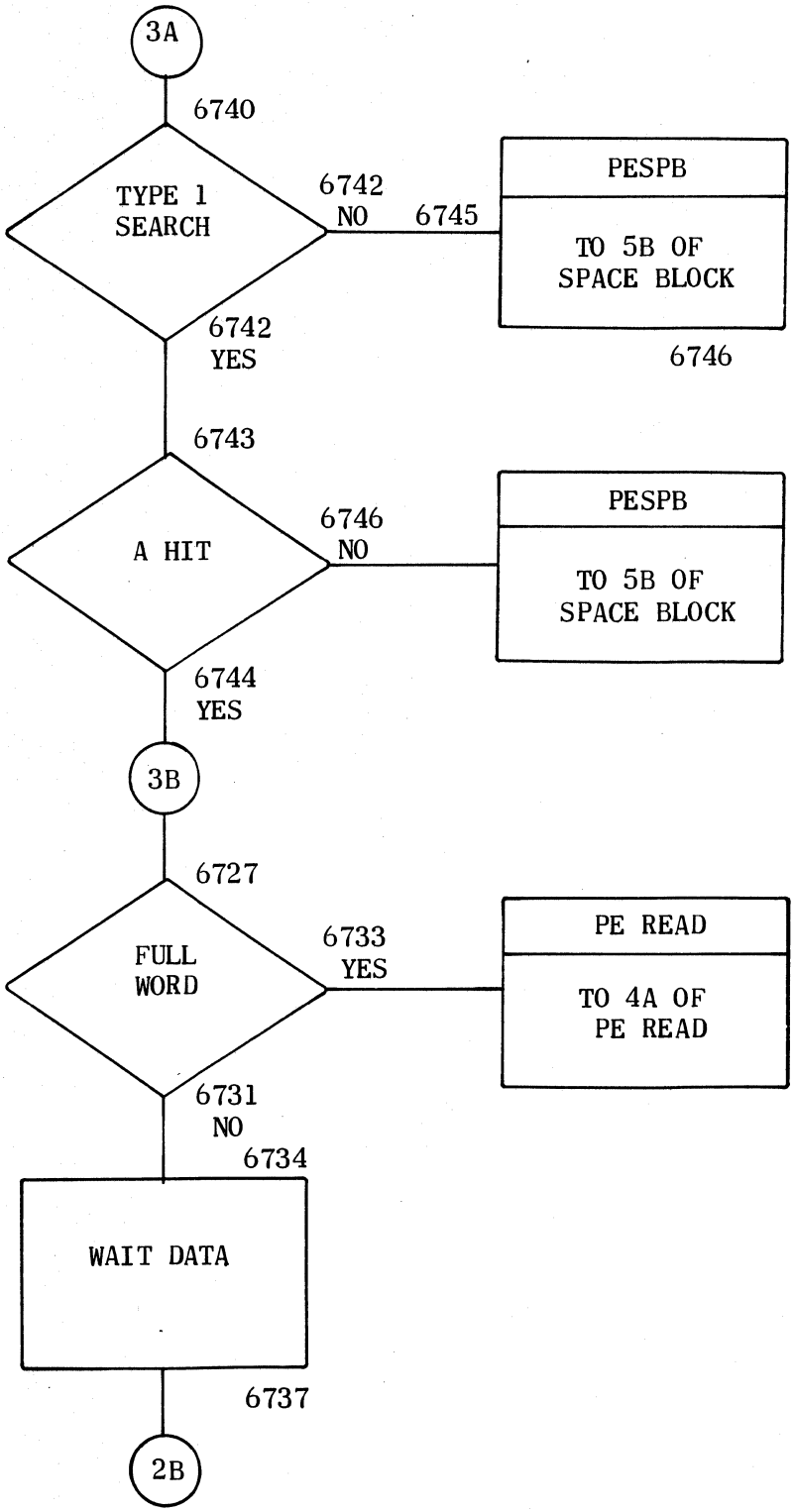


Figure 4-89. PE Search Sequence Flow Diagram (Sheet 3 of 3)

SECTION 5

MAINTENANCE

5-1. TEST EQUIPMENT AND SPECIAL TOOLS.

Test equipment and special tools required for adjustments and repair of the MTS are listed in table 5-1. Tools and equipment listed support the maintenance concept which enables field replacement of all switches, indicators, fan motors, connectors, and printed circuit logic cards. Although the manual provides instructions for this depth of repair, the actual maintenance concept in use should be determined by local directive based on skill level, parts availability, and available maintenance time.

5-2. PREVENTIVE MAINTENANCE.

Preventive maintenance is performed to reduce unscheduled maintenance and extend the operational life of the equipment. Preventive maintenance procedures are performed at regularly scheduled intervals depending on the operating schedule of the system. Where continuous operation is required, this operation must be interrupted for required maintenance to avoid unscheduled maintenance due to failures.

Preventive maintenance procedures are divided into weekly, monthly, and semiannually. The following paragraphs list the procedures to be performed and the frequency of performance.

For preventive maintenance for the Magnetic Tape Transport and the power supply, refer to Univac PX 7984, Section 5.

a. WEEKLY. - Remove and clean the air filter located behind the grill at the top front of the cabinet. Use a mild detergent and water to remove the collected dust. Air dry the filter before replacing.

Perform weekly maintenance on the tape transports as specified in PX 7984.

b. MONTHLY. - Perform the following steps and observe the stated results on the maintenance control panel. In the event the stated result does not occur, refer to the corrective maintenance procedures to isolate the malfunction.

(1) TAPE TRANSPORT CHECKS.

STEP 1. Apply power to MTS.

STEP 2. Starting with MTT #1, place a tape on supply reel and press LOAD indicator-switch on control panel. Observe that LOAD indicator is lighted and tape threads and loads into buffer columns. After tape is loaded, LOAD indicator is extinguished and BOT and READY indicators are lighted.

STEP 3. Press FWD indicator-switch and observe that FWD indicator is lighted and tape moves forward.

STEP 4. Press STOP switch and observe that tape movement stops and FWD indicator is extinguished.

TABLE 5-1. TEST EQUIPMENT AND SPECIAL TOOLS

ITEM	FUNCTION	REQUIREMENTS
Oscilloscope with Dual-trace Capability (Tektronix Model 453A or equivalent)	Display waveforms during checkout and trouble-shooting	Bandwidth of 60 MHz Sweep rate of 100 nsec/div.
Multimeter (Triplett Model 630A or equivalent)	General voltage, current, and resistance measurements	DC Range 0-300 volts AC Range 0-200 volts DC Current 0-12 amps Resistance 0-100 megohms
Card Extender	Extend transport printed circuit cards	Univac No. 7074100-00
Card Extractor	Remove transport printed circuit cards	Univac No. 7073472-00
Card Extender	Extend controller printed circuit cards	Univac No. 7099639-00
Card Extractor	Remove controller printed circuit cards	Univac No. 7902607-03
Hub Alignment Tool	Align hubs on transports	Univac No. 7600732-00
Set Block	Adjust height of capstan	Univac No. 7602199-00
Hub Height Gauge	Position Supply Reel Hub	Univac No. 7602200-00
Height Gauge	Position Take Up Reel Hub	Univac No. 7602201-00
Wire Wrap Gun (Battery powered, portable)	Make wiring changes and repairs	Univac No. 7902119-00
Battery	Power wire wrap gun	Univac No. 7902118-01
Charger	Enable charging wire wrap gun battery	Univac No. 7902118-02
Wire Wrap Sleeve 30 ga	Wrap 30 ga wire on wire wrap terminals	Univac No. 7902129-03
Wire Wrap Bit 30 ga	Wrap 30 ga wire on 0.025 in. square terminals	Univac No. 7902131-00
Wire Wrap Sleeve 26 ga	Wrap 26 ga wire on wire wrap terminals	Univac No. 7902129-04
Wire Wrap Bit 26 ga	Wrap 26 ga wire on wire wrap terminals	Univac No. 7902131-04
Wire Wrap Unwrap Tool	Unwrap 30 ga wire	Univac No. 7902130-00

TABLE 5-1. TEST EQUIPMENT AND SPECIAL TOOLS (CONT)

ITEM	FUNCTION	REQUIREMENTS
No Nik Stripper	Strip 30 ga wire	Univac No. 7904445-00
No Nik Stripper	Strip 26 ga wire	Univac No. 7904445-01
Master Skew Tape, TS800	Check 7-track read deskew	Univac No. 7957157-01
Extraction Tool	Remove connector pins	Univac No. 7904604-00

STEP 5. Press STOP LOAD switch and observe that vacuum blowers stop.

STEP 6. Press LOAD indicator-switch and observe that LOAD indicator is lighted, vacuum blowers operate, and, when proper vacuum and pressure are established, LOAD indicator is extinguished.

STEP 7. Press RWD indicator-switch and observe that RWD indicator is lighted and tape is rewound. When tape movement stops, RWD indicator is extinguished and BOT indicator is lighted.

STEP 8. Press FWD indicator-switch and allow tape to move forward for approximately 10 seconds. Press STOP switch. Press UNLOAD indicator-switch and observe that UNLOAD indicator is lighted and tape rewinds. When all tape is rewound on supply reel, the vacuum blowers stop and UNLOAD indicator is extinguished.

STEP 9. Press LOAD indicator-switch to again load tape. When LOAD indicator is extinguished and BOT indicator is lighted, press FWD indicator-switch to allow tape to move forward for approximately 5 seconds. Press STOP switch.

STEP 10. Place MAN/AUTO switch in AUTO position. Press following switches and observe that there is no effect on tape position:

FWD
REV
RWD
LOAD
UNLOAD
STOP LOAD

Place MAN/AUTO switch in MAN position.

STEP 11. Press RWD switch and observe that tape rewinds to BOT, BOT indicator is lighted and RWD indicator is extinguished.

STEP 12. Place MAN/AUTO switch in AUTO position.

STEP 13. Repeat steps 2 through 12 for each remaining MTT.

(2) MAINTENANCE PANEL CHECKS.

STEP 1. Apply power to MTS.

STEP 2. On maintenance panel, press to set the COMP A EIR, COMP B EIR, and COMP REG 0 through 35 indicator-switches and observe that each indicator remains lighted. Press MC switch and observe that indicator-switches listed above are extinguished and EFR indicator is lighted.

STEP 3. Place OP STEP RUN/STOP/STEP switch in RUN position. Place CLOCK RUN/STOP/STEP switch in RUN position. Press to set following indicator-switches in order given:

COMP A IN CONT
COMP B DUP REQ
COMP A DUP REL
COMP A EF

Observe that:

a) COMP A IN CONT clears
b) COMP B EIR sets
c) COMP B IN CONT sets
d) COMP B DUP REQ clears

STEP 4. Master clear MTS and observe that COMP B EIR is cleared and COMP B IN CONT remains set. Press to set following indicator-switches in order given:

COMP A DUP REQ
COMP B DUP REL
COMP B EF

Observe that:

a) COMP B IN CONT clears
b) COMP A EIR sets
c) COMP A IN CONT sets
d) COMP A DUP REQ clears

STEP 5. Master clear MTS. Press to set IDR and ODR indicator-switches to light indicators. Master clear MTS and observe that IDR and ODR indicators are extinguished.

STEP 6. Press to set COMP REG 0 through 35 indicator-switches to light indicators. Press COMP REG CLEAR switch and observe that all COMP REG indicators are extinguished.

STEP 7. Master clear MTS. Place OP STEP RUN/STOP/STEP switch in STOP position and SIM EF RUN/STOP/AUTO switch in RUN position. Set COMP REG bits corresponding to appropriate MTS configuration and MTT as specified in figure 5-1 for a write ignore error halt external function. Press to set COMP A EF. Place OP STEP RUN/STOP/STEP switch to RUN position and observe that tape on MTT under test does not move.

STEP 8. On control panel, press to set WRITE ENABLE indicator-switch for MTT under test. Master clear MTS. Place OP STEP RUN/STOP/STEP switch in STOP position.

STEP 9. Press to set COMP REG indicator-switches corresponding to appropriate MTS configuration and MTT as specified in figure 5-1 for a write ignore error halt external function. Press to set COMP A EF and place OP STEP RUN/STOP/STEP switch in RUN position. Observe that tape on selected MTT moves forward and associated SELECT indicator-switch on control panel is lighted.

STEP 10. Clear COMP REG. Sequentially set bits 0 through 35 of COMP REG. Observe that WRITE ACTIVE, READ ACTIVE, WRITE REG, and READ REG indicators are lighted. Place SIM EF RUN/STOP/AUTO switch in STOP position and observe that tape motion stops. Master clear MTS.

STEP 11. Place OP STEP RUN/STOP/STEP switch in STOP position. Place SIM EF RUN/STOP/AUTO switch in RUN position. Press to set COMP REG indicator-switches corresponding to appropriate MTS configuration and MTT as specified in figure 5-1 for a backread external function. Set COMP A EF indicator-switch.

STEP 12. Place OP STEP RUN/STOP/STEP switch in RUN position and observe that COMP REG 0 through 35 indicators are lighted and then are sequentially extinguished as tape on selected MTT moves in reverse. The READ ACTIVE and READ REG indicator-switches are lighted. Tape movement should stop automatically.

STEP 13. Repeat steps 7 through 12 for each MTT in MTS.

STEP 14. Master clear MTS and place OP STEP RUN/STOP/STEP switch in STOP position. Press to set COMP REG indicator-switches corresponding to appropriate configuration and MTT as specified in figure 5-1 for a write ignore error halt external function. Place the OP STEP RUN/STOP/STEP in RUN position and observe that tape on specified MTT moves forward.

STEP 15. On control panel associated with specified MTT, press EOT indicator-switch and observe that, after a short period of time, tape movement stops and EOT indicator-switch is lighted. Place OP STEP RUN/STOP/STEP switch in STOP position.

STEP 16. Master clear MTS and set COMP REG indicator-switches corresponding to appropriate configuration and MTT as specified in figure 5-1 for a backread external function. Press to set COMP A EF indicator-switch. Place OP STEP RUN/STOP/STEP switch in RUN position and observe that tape moves in reverse. Press EOT indicator-switch and observe that, after a short period of time, tape movement stops and EOT indicator is extinguished.

STEP 17. Repeat steps 14, 15, and 16 for each MTT in MTS.

STEP 18. Master clear MTS. Press to set DISPLAY REGISTER ADDRESS μP indicator-switch. Toggle RUN/STOP/I STEP switch repeatedly to I STEP position and observe that DISPLAY REGISTER indicators are lighted with a different display each time switch is toggled.

STEP 19. Master clear MTS. Press to set DISPLAY REGISTER ADDRESS μI indicator-switch. Toggle RUN/STOP/I STEP switch repeatedly to I STEP position and observe that DISPLAY REGISTER indicators are lighted with a different display each time switch is toggled.

BITS															
35 ——— 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
												0	1	0	0	1 TT 1	7-TRACK CONFIGURATION
												0	1	0	1	0 TT 2	
												0	1	0	1	1 TT 3	
												0	1	1	0	0 TT 4	
												0	0	1	0	0 TT 1	9-TRACK CONFIGURATION
												0	1	0	0	0 TT 2	
												0	1	1	0	0 TT 3	
												0	0	0	0	0 TT 4	
										0	0						
									1	7-TRACK CONFIGURATION							
									0	9-TRACK CONFIGURATION							
	0	1	0	0	0	1	1	0	WRITE								
	0	1	0	1	0	1	1	0	WRITE IGNORE ERROR HALT								
	0	1	0	1	1	1	1	0	WRITE XIBG, IGNORE ERROR HALT								
	1	0	0	0	0	1	1	0	BACKREAD								
	1	1	0	0	0	1	1	0	REWIND								
X ——— X	NOT USED																

Figure 5-1. COMP REG Bit Settings

STEP 20. Place DSPL ACT/INACT in ACT position and RUN/STOP/I STEP switch in RUN position. Press to set DISPLAY REGISTER ADDRESS GEN indicator-switch. For each of eight general registers, A0 through A7, press to set DISPLAY REGISTER ADDRESS bits 0 through 3 for selected register (A0 = 10_8, A1 = 11_8, A2 = 12_8, A3 = 13_8, etc.). Perform this step and step 21 for each register before going to next register.

STEP 21. Press to set each DISPLAY REGISTER indicator-switch and observe that each indicator-switch is lighted. Press DIPSLAY REGISTER CLR switch and observe that DISPLAY REGISTER is cleared.

STEP 22. Press to set bit in DISPLAY REGISTER corresponding to general register being displayed (Bit 0 = A0, Bit 1 = A1, etc.). Clear DISPLAY REGISTER ADDRESS and repeat steps 20, 21 and 22 for each of eight general registers.

STEP 23. Clear DISPLAY REGISTER ADDRESS. Start with general register A0 and press to set appropriate bits in DISPLAY REGISTER ADDRESS for general register being displayed (A0 = 10_8, A1 = 11_8, etc.). Observe that bit in DISPLAY REGISTER corresponding to general register (A0 = 10_8, A1 = 11_8, etc.) being displayed is set. Clear DISPLAY REGISTER. Repeat this step for each general register.

STEP 24. Clear DISPLAY REGISTER ADDRESS. Press to set DISPLAY REGISTER ADDRESS bits S2 and 0 and all bits in DISPLAY REGISTER. Clear DISPLAY REGISTER ADDRESS and observe display in DISPLAY REGISTER has been altered. Press to set DISPLAY REGISTER ADDRESS bits S2 and 0 and observe that all bits in DISPLAY REGISTER are lighted. Place DSPL ACT/INACT in INACT position.

STEP 25. Master clear MTS and place CLOCK RUN/STOP/STEP switch in RUN position. Press to set PE/NRZI 1 through 4, WRITE ACTIVE, and READ ACTIVE indicator-switches and observe that all remain lighted. Press each WRITE REG indicator-switch and observe that all remain extinguished. Press to set each READ REG indicator-switch and observe that all remain lighted. Press READ REG CLR switch and observe that all READ REG indicator-switches are extinguished.

STEP 26. Place the main POWER ON/OFF switch on control panel to OFF position and then to ON position. Reload tape on each MTT in MTS. Place MAN/AUTO switch for each MTT in MAN position.

STEP 27. Press FWD indicator-switch for MTT-1 and observe that indicator remains lighted and tape on MTT-1 moves forward. On maintenance panel, rotate RUN and STOP controls in both directions and observe that there is no effect on tape movement.

STEP 28. Place TT START/STOP 1 switch in up position. Rotate RUN control in both directions and observe that tape speed changes as RUN control is rotated. Rotate STOP control and observe that tape speed changes as the STOP control is rotated. Place TT START/STOP 1 switch in down position and press STOP control for MTT-1 on control panel. Repeat steps 27 and 28 for each MTT, using TT START/STOP 2 switch for MTT2, etc.

STEP 29. Master clear MTS and place TD TEST switch in up position. Observe that READ ACTIVE and WRITE ACTIVE indicator-switches are lighted. Place TD TEST switch in down position.

STEP 30. Master clear MTS and place OP STEP RUN/STOP/STEP switch in the STOP position. Place MAN/AUTO switch for each MTT in AUTO position. Remove printed circuit assembly in card position A22 in control unit. Press to set COMP REG indicator-switches corresponding to appropriate MTS configuration and MTT 1 as specified in figure 5-1 for a write external function. Press to set COMP A EF and place OP STEP RUN/STOP/STEP switch in the RUN position. Observe that COMP A EIR and COMP REG 7 indicators are lighted. Place the OP STEP RUN/STOP/STEP switch in the STOP position and reinstall printed circuit assembly in A22 position.

STEP 31. Master clear MTS and press to set COMP REG bits corresponding to appropriate MTS configuration and MTT 1 as specified in figure 5-1 for a write ignore error halt.

STEP 32. Press to set COMP A EF indicator-switch and external function. Place OP STEP RUN/STOP/STEP switch in the RUN position. Clear COMP REG and set COMP REG bits 0 through 35. Observe that WRITE ACTIVE, READ ACTIVE WRITE REG, AND READ REG indicators are lighted.

STEP 33. Remove printed circuit assembly from position A22 of the control unit and observe that the COMP REG bits 0 through 35 remain lighted and MTS continues to operate. Reinstall printed circuit assembly in A22 position.

STEP 34. Place SIM EF switch in STOP position and observe that tape motion stops.

STEP 35. Master clear MTS. Place OP STEP RUN/STOP/STEP switch in STOP position. Place SIM EF switch in RUN position.

STEP 36. Set COMP REG bits corresponding to appropriate MTS configuration and MTT-1 as specified in figure 5-1 for a write XIRG, ignore error halt external function. Repeat steps 32 through 35.

STEP 37. Set COMP REG bits corresponding to appropriate MTS configuration and MTT-1 as specified in table 5-1 for a rewind external function. Press to set COMP A EF indicator-switch and place OP STEP RUN/STOP/STEP switch in RUN position. Observe that tape rewinds on MTT-1.

c. SEMI-ANNUALLY. - Remove all subassemblies from the cabinet and vacuum the entire interior and exterior of the cabinet and of each subassembly. Check all cable assemblies for shorts, opens, and breaks. Replace all units and perform all monthly preventive maintenance and programmed fault isolation tests. Repair as necessary by referring to corrective maintenance procedures in this section and in PX 7984, Section 5.

5-3. CORRECTIVE MAINTENANCE.

Corrective maintenance for the MTS consists of removal and replacement procedures, wire-wrap procedures and troubleshooting.

a. REMOVAL AND REPLACEMENT. - The following paragraphs describe removal and replacement procedures for the controller, transports, air filter, system control panel switches and indicators, and the electrical cabinet blowers.

(1) CONTROLLER. - To remove and replace the controller drawer perform the following steps:

STEP 1. Remove power from electrical cabinet.

STEP 2. Extend controller drawer from electrical cabinet until stops engage.

STEP 3. Remove protective cover from wire-wrap side of drawer.

STEP 4. Disconnect ground wires at both terminals E8 and E9.

STEP 5. Remove all cable clamps on paddle board cables.

STEP 6. Remove paddle boards from wire-wrap side of drawer.

STEP 7. Disconnect white signal ground wire W20 (A3 W2-1).

STEP 8. Disconnect lavender chassis ground wire W21 (A3 E7).

STEP 9. Remove signal/power cables clamp on card rack side of drawer.

STEP 10. Disconnect cables from J1 through J7 on card rack side of drawer.

STEP 11. Remove two bolts holding grasshopper bracket to drawer.

STEP 12. Release top and bottom slide stops and pull chassis from cabinet.

To replace the chassis in the cabinet perform the above steps in reverse order.

(2) TRANSPORT. - To remove and replace a transport perform the following steps:

STEP 1. Fully extend transport to be removed.

STEP 2. Remove power from electrical cabinet.

STEP 3. Turn seven captive screws on rear cover one-quarter turn counterclockwise and remove cover.

STEP 4. Remove screws securing grasshopper cables cable clamps to bracket.

STEP 5. Disconnect cables at J1, J2 and J3.

STEP 6. Disconnect ground wire at E1.

STEP 7. Open head access cover and remove protective cover over read/write head

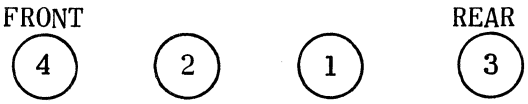
STEP 8. Using a rocking motion gently remove plug connected to write head.

STEP 9. Remove wires connected to erase head.

STEP 10. Ensure all cabling associated with grasshopper is clear of transport chassis.

STEP 11. Remove retaining screw securing retractable grasshopper arm to chassis and carefully retract arm and associated cables into cabinet.

STEP 12. Remove four retaining screws from the top slide in the following number order:



WARNING

At least two persons should now remove the chassis from the cabinet.

STEP 13. Release bottom slide quick disconnect lock by turning counterclockwise until flat surfaces are horizontal.

STEP 14. Draw transport forward, supporting both ends to retain a near horizontal removal plane.

To replace a transport in the cabinet perform the above steps in reverse order with an additional person used to guide the transport onto bottom slide in initial step.

(3) POWER SUPPLY. - To remove and replace the 75-volt power supply perform the following steps:

STEP 1. Remove power from electrical cabinet.

STEP 2. Extend power supply drawer from cabinet to locked position.

STEP 3. Disconnect cables from J1 through J6.

STEP 4. Disconnect ground wire from E1.

STEP 5. Remove two screws holding grasshopper bracket to chassis.

WARNING

Two persons are required to perform the remaining effort.

STEP 6. Release top and bottom slide stops and pull chassis from cabinet.

To replace a power supply in the cabinet, perform the preceding steps in reverse order.

(4) CONTROLLER DC-TO-DC CONVERTER. - To remove and replace the controller dc-to-dc converter perform the following steps:

STEP 1. Remove power from the electrical cabinet.

STEP 2. Fully extend the drawer to slide stops.

STEP 3. Disconnect cable from J8.

STEP 4. While supporting the converter assembly, remove two screws on assembly bottom bracket and two screws on assembly top bracket.

STEP 5. Remove converter assembly.

To replace the converter assembly, perform the preceding steps in reverse order.

(5) SYSTEM CONTROL PANEL REPLACEABLE INDICATORS. - The POWER, OVER TEMP, and top four indicators of each magnetic tape control section of the system control panel are replaceable indicators. To replace a defective indicator with a new one perform the following steps:

STEP 1. Remove lens by unscrewing counterclockwise.

CAUTION

Three different voltage rating lamps are used. Be sure to replace a defective lamp only with one of the same type.

STEP 2. Remove defective lamp and insert new one.

STEP 3. Reinstall lens.

(6) SYSTEM CONTROL PANEL SWITCHES AND LEDS. - To replace a defective system control panel switch or LED perform the following steps:

WARNING

Lethal voltages are present on the back side of the system control panel. Power must be removed from electrical cabinet.

STEP 1. Operate CIRCUIT BREAKER 20 AMP switch to OFF.

STEP 2. Disconnect input power connector from cabinet.

STEP 3. Remove all screws on system control panel except two holding running time meter.

STEP 4. If a switch to be changed has a knob, remove knob.

STEP 5. Remove and tag wires connected to switch or indicator.

STEP 6. Remove lock nut.

To install the new switch or indicator perform the above steps in reverse order.

(7) MAINTENANCE PANEL SWITCHES AND INDICATORS. - To replace a defective maintenance panel switch or indicator perform the following steps:

STEP 1. Remove power from electrical cabinet.

STEP 2. Open door on control unit drawer.

STEP 3. Remove five screws and three extension studs holding panel to drawer.

STEP 4. Remove and tag wires connected to switch or indicator.

STEP 5. Remove locking nut holding switch or indicator.

To install the new switch or indicator perform the above steps in reverse order.

(8) BLOWER REPLACEMENT. - To replace a defective blower in the top hat assembly perform the following steps:

STEP 1. Remove top hat cover plate.

STEP 2. Determine which blower is defective.

STEP 3. Remove power from electrical cabinet.

STEP 4. Slide insulating rubber boot from terminal block on fan.

STEP 5. Remove and tag wires connected to fan.

STEP 6. Remove three fan holding screws and retaining blocks.

STEP 7. Lift fan from fan assembly.

To install a new fan perform the above steps in reverse order.

(9) HORN REPLACEMENT. - To replace the horn in the electrical cabinet perform the following steps:

STEP 1. Remove power from electrical cabinet.

STEP 2. Remove top hat cover plate.

STEP 3. Remove and tag wires connected to horn.

STEP 4. Remove three screws holding horn to fan assembly.

STEP 5. Remove horn from fan assembly.

To install a new horn perform the above steps in reverse order.

(10) TRANSPORT PRINTED CIRCUIT CARDS. - To replace a printed circuit card in a transport card rack, perform the following steps:

STEP 1. Remove power from the transport.

STEP 2. Extend transport from cabinet until stops engage.

STEP 3. Turn seven captive screws on rear cover counterclockwise and remove cover.

STEP 4. Remove eight screws holding card rack assembly cover and remove cover.

STEP 5. Attach card extractor (Univac No. 7073472-00) to card and remove card.

STEP 6. Carefully slide a new card of the same type, as was removed, into card slot and ensure secure seating.

STEP 7. Perform steps 1 through 4 above in reverse order.

(11) CONTROLLER PRINTED CIRCUIT CARDS. - To replace a printed circuit card in the controller card rack, perform the following steps:

STEP 1. Remove power from controller drawer.

STEP 2. Extend controller drawer until stops engage.

STEP 3. Attach card extractor (Univac No. 7902607-03) to card and remove card.

STEP 4. Carefully slide a new card of same type, as was removed, into card slot and ensure secure seating.

STEP 5. Perform steps 1 and 2 above in reverse order.

b. ADJUSTMENTS. - The following paragraphs describe the various adjustment procedures for MTS operation.

(1) TIME DELAY ADJUSTMENTS. - Several time delay circuits are used to develop proper delay pulses for transport operation. These delays are adjustable and should be checked if cards are replaced. To adjust these delays, use an oscilloscope and observe the wave forms at the test points listed in table 5-2. If necessary, adjust the associated potentiometer to produce the required delay. Figure 5-2 identifies the location of the adjustments.

(2) DESKEWING ADJUSTMENTS. - The control unit contains three deskewing adjustments for each MTT in the system. These are read forward deskew, read reverse deskew, and write deskew. The read deskew adjustments are contained on the 7091815 cards in card locations J22A through J28A for the seven-track systems and J22A through J30A for the nine-track systems. The write deskew adjustments are contained on the 7091805 cards in card locations J13A through J16A for the seven-track systems. J17A is added for tracks 7 and 8 in the nine-track systems.

TABLE 5-2. TIME DELAYS

DELAY	TEST POINT	CONTROL	ADJUST FOR
Reverse Stop	J52A-TP5	J52A-R22	3 msec
Read	J52A-TP9	J52A-R20	3 msec
Read BOT	J52A-TP10	J52A-R18	20 msec
Write	J52A-TP11	J52A-R19	4 msec
Write XIRG	J52A-TP3	J52A-R17	25 msec
Write BOT	J52A-TP7	J52A-R16	50 msec
ODR/IDR	J52A-TP2	J52A-R23	fast = 3 μsec slow = 7 μsec
MTT1 EOT	J04B-TP11	J04A-R21	500 msec
MTT2 EOT	J04B-TP10	J04A-R20	500 msec
MTT3 EOT	J04B-TP5	J04A-R19	500 msec
MTT4 EOT	J04B-TP6	J04A-R18	500 msec

(a) READ FORWARD DESKEW. - After the mechanical deskew adjustments have beer made, adjust the read forward deskew by performing the following steps:

STEP 1. Load master deskew tape on transport for which deskewing is to be adjusted.

STEP 2. Ensure ON LINE/OFF LINE switch is in OFF LINE position. Apply power to MTS per paragraph 3-8.

STEP 3. Press to set COMP A IN CONT indicator-switch. Master clear MTS.

STEP 4. On maintenance control panel, for 7-track, set bits 7, 5 and proper combination of bits in COMP REG for address of associated transport. For 9-track, set bits 6 and associated transport address bits.

STEP 5. Press to set COMP A EF indicator-switch.

STEP 6. Operate the OP STEP RUN/STOP/STEP switch to the STEP position. MTS is now reading all "1"s from tape.

STEP 7. Use an oscilloscope with negative sync, adjust associated control (see figure 5-3a) on the 7091815 card in card location J25A (J26A for 9-track units) to obtain a 3.0 microsecond pulse at TP12. This is center track.

STEP 8. Use dual trace and connect sweep A to TP6 on center track card. Connect positive sync to this TP6.

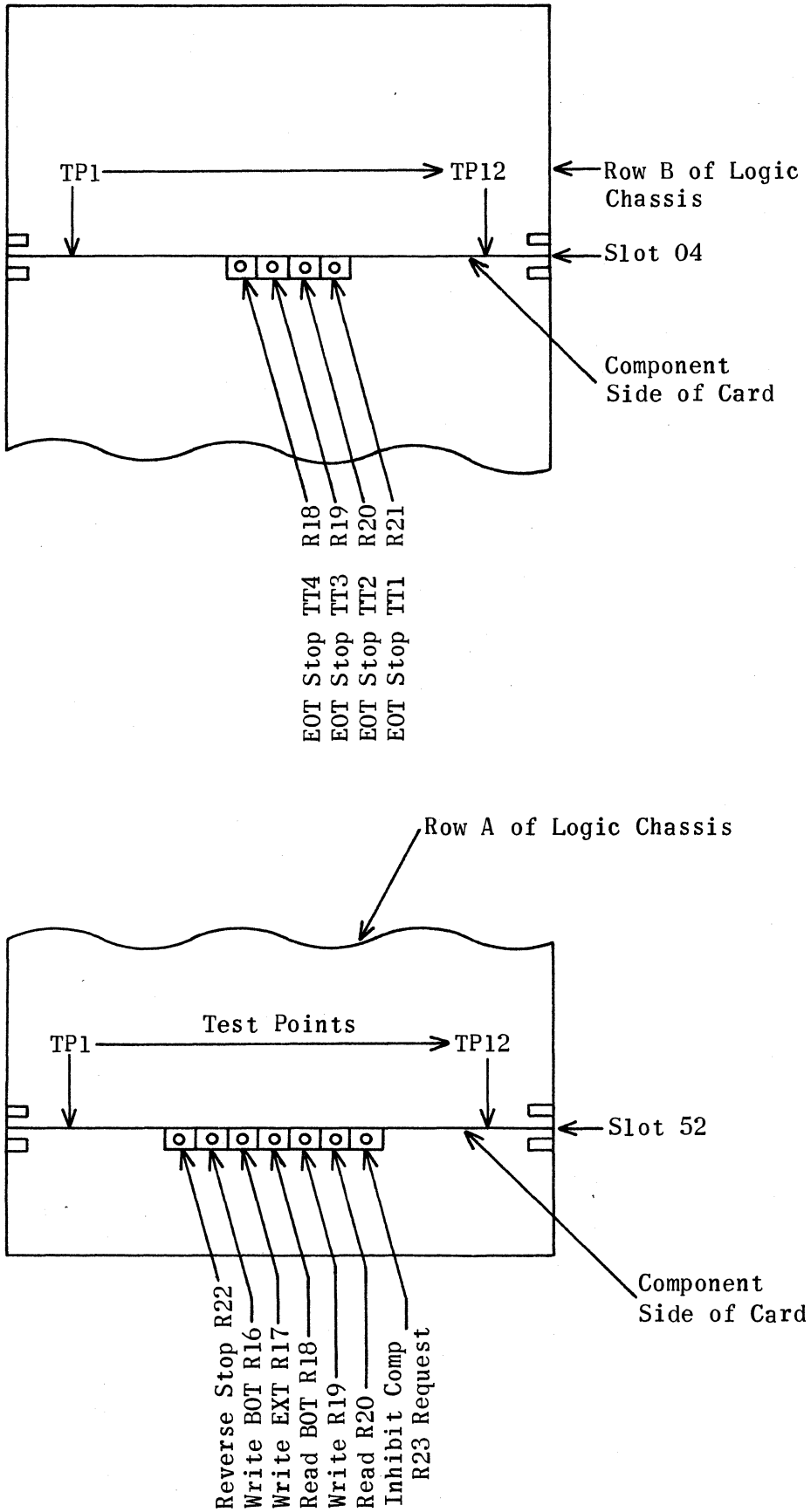
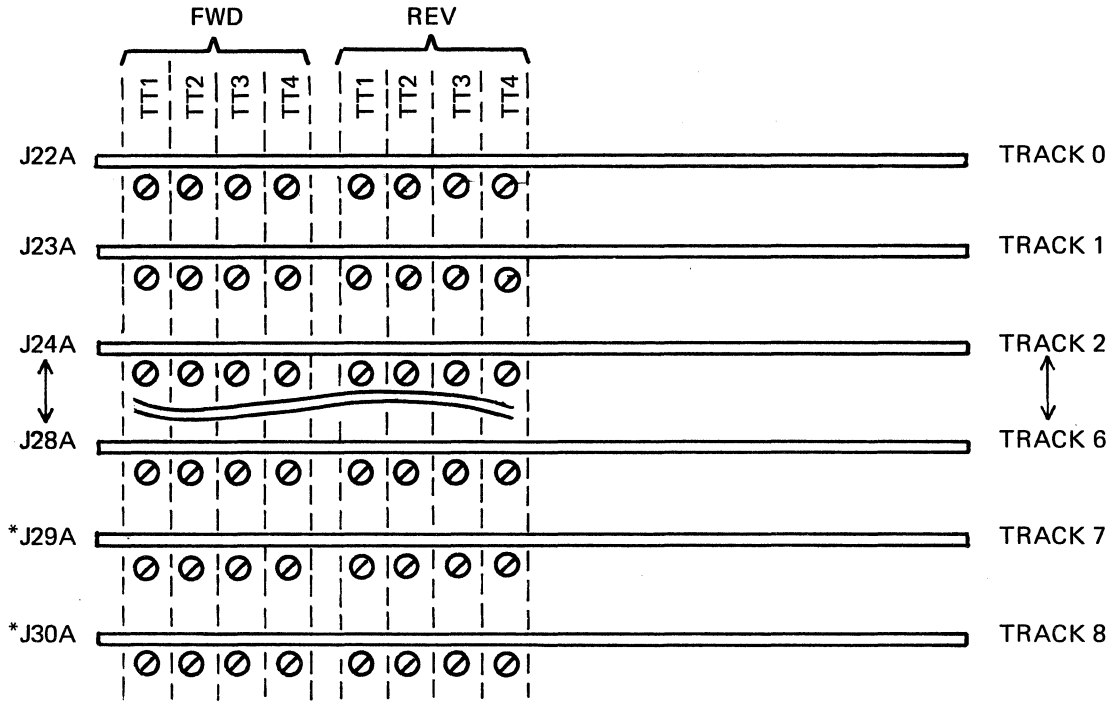
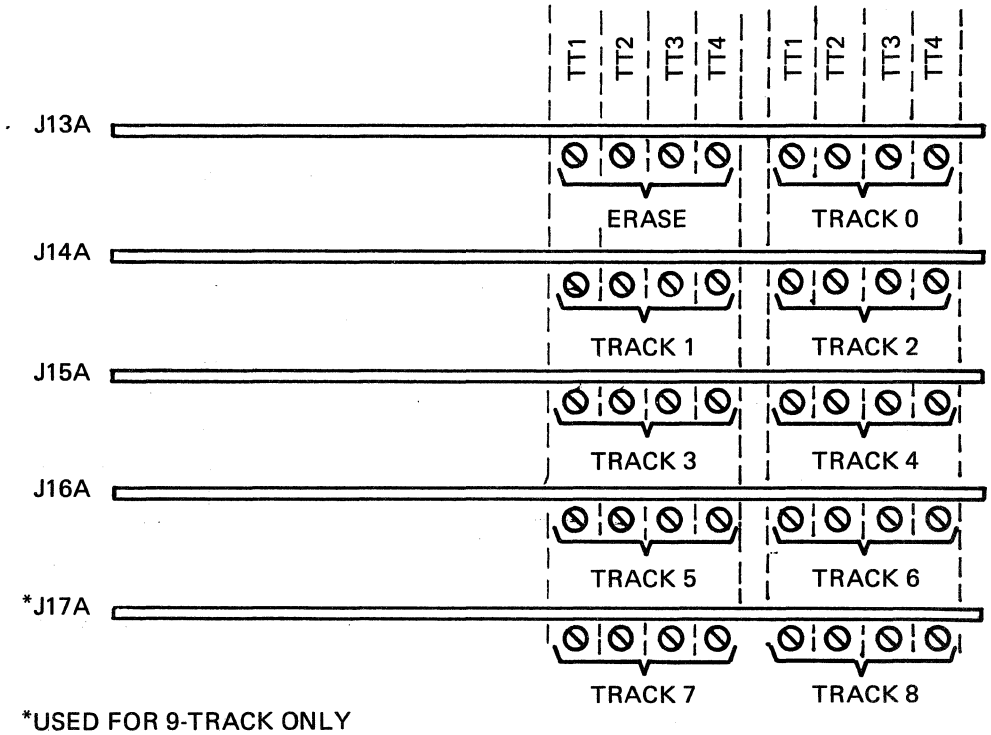


Figure 5-2. Delay Adjustment Identification



* USED FOR 9-TRACK ONLY
J25A CENTER TRACK, 7-TRACK UNIT
J26A CENTER TRACK, 9-TRACK UNIT

a. Read Deskew Adjustments



*USED FOR 9-TRACK ONLY

b. Write Deskew Adjustments

Figure 5-3. Deskew Adjustment Identification

STEP 9. Connect sweep B to TP6 on each 7091815 card, as shown in figure 5-3a, and adjust control associated with transport in use to produce a pulse pattern corresponding to sweep A.

STEP 10. If read reverse deskew adjustments are to follow, run tape to EOT. Otherwise, unload and remove master deskew tape.

(b) READ REVERSE DESKEW. - If the run forward deskew adjustments have been made, the tape is loaded and at EOT. If not, load the master deskew tape and run to EOT. Perform the following steps.

STEP 1. Ensure that ON LINE/OFF LINE switch is in OFF LINE position. Master clear MTS.

STEP 2. Set COMP A IN CONT.

STEP 3. Set bits 15, 7, 5 and proper bits for transport address in COMP REG for 7-track. For 9-track, set bits 15, 6, and associated transport address bits.

STEP 4. Set COMP A EF.

STEP 5. Place OP STEP RUN/STOP/STEP switch in STEP position. Transport is now reading all "1"s in a read reverse mode.

STEP 6. Use an oscilloscope with negative sync and adjust associated control (see figure 5-3a) on 7091815 card for center track to obtain a 3.0 microsecond pulse at TP12.

STEP 7. Use dual trace and connect sweep A and sync to TP6, sync positive, of center track card. Connect sweep B to each 7091815 card TP6 and adjust associated read reverse control to obtain a pulse pattern corresponding to sweep A.

STEP 8. Allow tape to run to BOT. Unload master skew tape.

(c) WRITE DESKEW. - To adjust the write deskew circuits, load a scratch tape and run to BOT. Perform the following steps.

STEP 1. Ensure that ON LINE/OFF LINE switch is in OFF LINE position.

STEP 2. Master clear MTS and press to set COMP A IN CONT indicator-switch.

STEP 3. On maintenance control panel, for 7-track, set bits 14, 12, 7, 5 and the proper combination of bits in COMP REG for address of associated transport. For 9-track, set bits 14, 12, 6, and associated transport address bits.

STEP 4. Press to set EF indicator-switch. Place DISPL ACT/INACT to INACT position.

STEP 5. Place RUN/STOP I STEP switch in RUN position.

STEP 6. Press to set bits 0 through 17 in COMP REG. Place OP STEP RUN/STOP/ STEP switch in RUN position. MTS is now writing "1"s on tape on selected transport.

STEP 7. Use a dual trace oscilloscope and observe waveform at center track, J15A-TP6 for 7-track and J15A-TP1 for 9-track. If necessary, adjust associated potentiometer to produce a pulse of 4.0 microseconds. Figure 5-3b shows potentiometer identification.

STEP 8. Use dual trace A and observe and sync positive at J25A-TP6 (J26A for 9-track) for center track. Use trace B and compare outputs at TP6 on 7091815 cards in J22A through J28A (J30A for 9-track) to trace A. If necessary, adjust associated write deskew potentiometer to produce a corresponding trace.

STEP 9. After all tracks have been adjusted, stop MTS and rewind and remove scratch tape. Repeat above steps 1 through 9 for each transport.

c. WIRE-WRAP PROCEDURE. - Most of the electrical connections in the MTS are mechanical, solderless connections formed by wrapping a component lead or wire around a terminal post. Each terminal post has a square cross section. The wrapped connection forms a helical coil around the terminal post, with points of contact at each of the four terminal post corners. Four points of contact are made for each turn of the connecting wire that encircles the post.

Before a broken wire can be replaced, the terminal post lead must be removed. An unwrap tool is used for removing the leads. If it is impractical to remove the wire, trim both ends of the wire lead and leave it in place. A replacement wire lead is routed exactly as the original lead except that it is placed on top of the other leads.

Wire-wrap connections are formed with a wire-wrap gun. This machine has a stationary sleeve and various sized bits for different gauge wires. The stationary sleeve has a slotted end that holds the bit in place and prevents the wire from rotating during the wrapping operation. The sleeve is held in the wire-wrap machine by a chuck. Each bit has a longitudinal groove that accommodates the end of the wire to be wrapped. A hole in the end of the bit allows it to be slipped over the terminal post on which the wire-wrap connection is to be made.

When the wire-wrap gun is used, the end of the wire lead is inserted between the longitudinal groove in the bit and the stationary sleeve. The wire is bent so tha the wire lead is perpendicular to the longitudinal axis on the bit before the wire wrap gun and wire are positioned over the terminal where the wire-wrap connection is to be made. Positioning the wire-wrap gun over the terminal and pressing the trigger wraps the wire. Figure 5-4 shows unacceptable and acceptable wire-wrappin

The wire-wrap gun supplies the necessary power from a detachable rechargeable battery which forms the handle. Recharging the battery is accomplished by twistin the handle 90° counterclockwise and inserting it in a conventional 117 Vac 60 Hz single phase electrical outlet for twelve hours.

NOTE

Do not wire-wrap with a gun that does not have fully charged batteries.

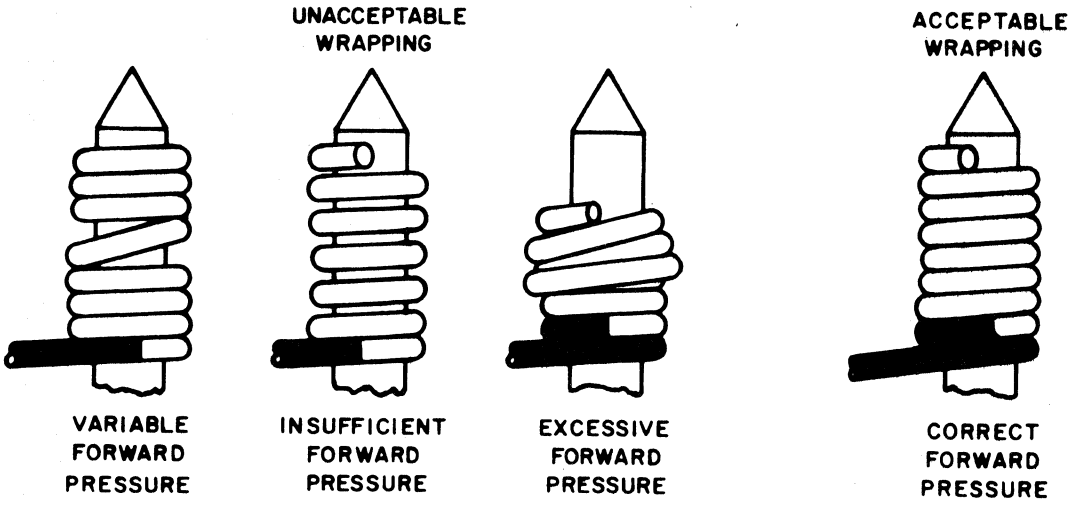
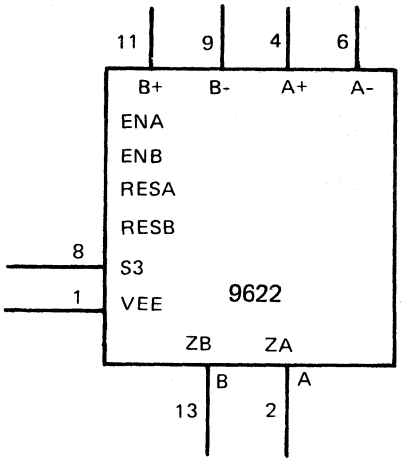


Figure 5-4. Wire-Wrap Examples

5-4. INTEGRATED CIRCUIT DESCRIPTIONS (Figures 5-5 through 5-40).

The MTS uses unique integrated circuits in its logic configuration. The logic diagrams, truth tables and pin assignments are provided as an aid in malfunction isolation and not as replacement data. Because the maintenance philosophy is for card replacement rather than circuit component replacement, no procedures are provided to repair circuit cards. The data presented on the IC's is informational only. Component replacement may be performed for emergency operation following normal shop procedures.



GROUND PIN – 14
VOLTAGE PIN – 07

PIN NAMES

A+, A-, B+, B-	Inputs
EN A, EN B	Enables
VEE, S3	-10 Volts Supply
RES A, RES B	Terminating Resistors
ZA, ZB	Outputs

DESCRIPTION

This integrated circuit contains two line receivers which are designed to discriminate worst case logic swing of 2 volts from a ±10 volts common mode noise signal or groun shift. Each output is enabled by a high enable (ENA or ENB). The logic configuratic is shown below.

LOGIC CONFIGURATION

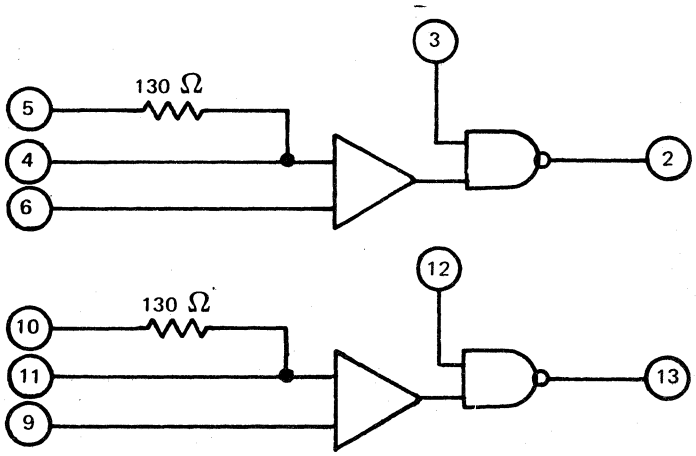
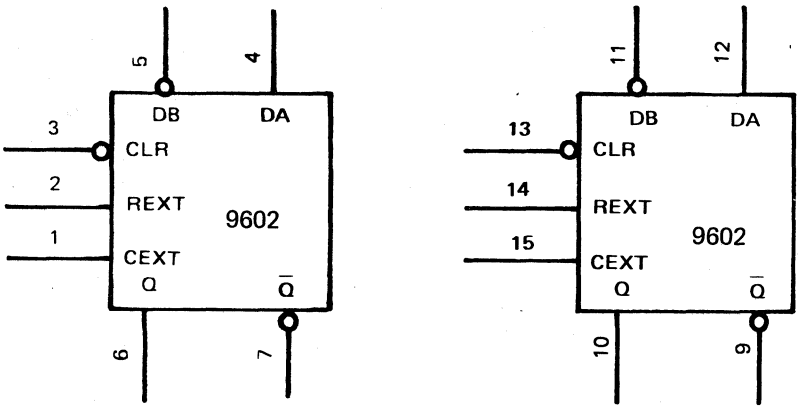


Figure 5-5. Dual Line Receiver (7903776)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

DA	Trigger Input (Active High)	CEXT, REXT	External Timing
DB	Trigger Input (Active Low)	Q	Output
CLR	Master Reset (Active Low)	$\overline{Q}$	Complementary Output

DESCRIPTION

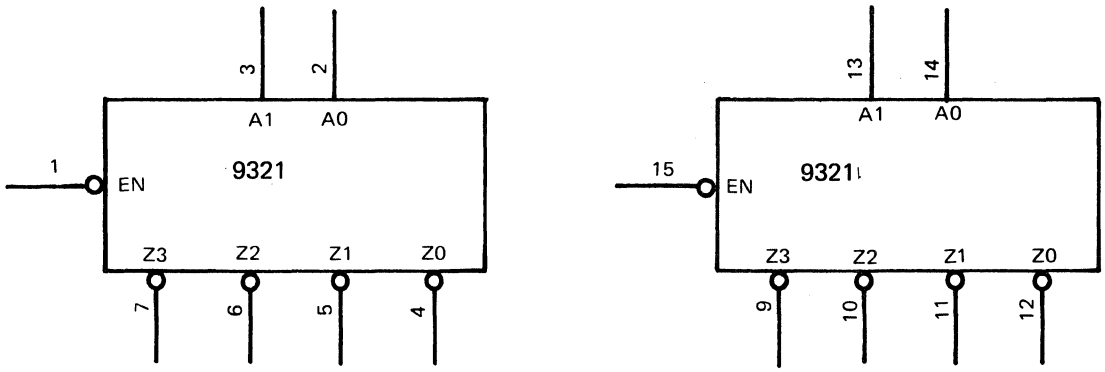
The one-shot multivibrator provides an output pulse whose duration and accuracy depends on external timing components connected to CEXT and REXT. The multivibrator has two trigger inputs, one active high (DA), and one active low (DB). This allows leading edge or trailing edge triggering. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the multivibrator and result in a continuous true output. A LOW level at the CLR input terminates the output pulse.

TRIGGERING TRUTH TABLE

DA	DB	CLR	Operation
L → H	H	H	Trigger
L	H → L	H	Trigger
X	X	L	Reset

H = High voltage level
L = Low voltage level
X = Irrelevant
H → L = High to low voltage level transition
L → H = Low to high voltage level transition

Figure 5-6. Dual One-Shot Multivibrator (7903777)



GROUND PIN – 08

VOLTAGE PIN – 16

PIN NAMES

EN	Enable Inputs (Active Low)
A1, A0	Inputs
Z3, Z2, Z1, Z0	Outputs (Active Low)

DESCRIPTION

This decoder consists of two independent one-of-four decoders, each with an active low enable. The two bit input code is translated into one-of-four mutually exclusive active low outputs. The active low enable must be present to permit any output to be low.

TRUTH TABLE

INPUTS			OUTPUTS			
EN	A1	A0	Z3	Z2	Z1	Z0
H	X	X	H	H	H	H
L	L	L	H	H	H	L
L	L	H	H	H	L	H
L	H	L	H	L	H	H
L	H	H	L	H	H	H

H = High voltage level
L = Low voltage level
X = Don't care condition

LOGIC CONFIGURATION

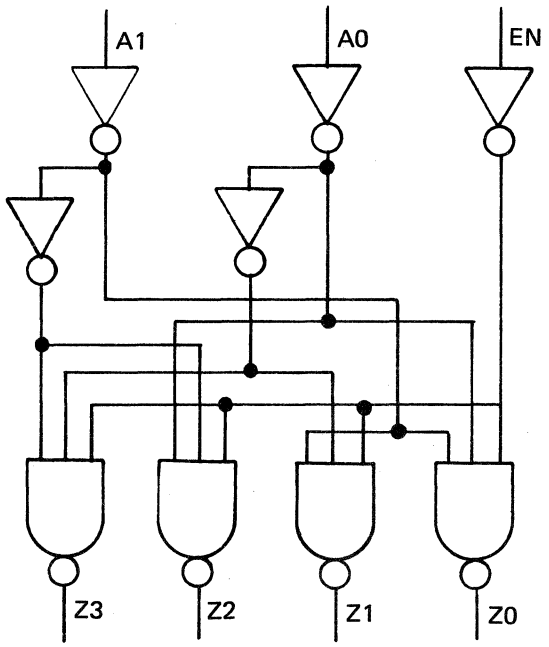
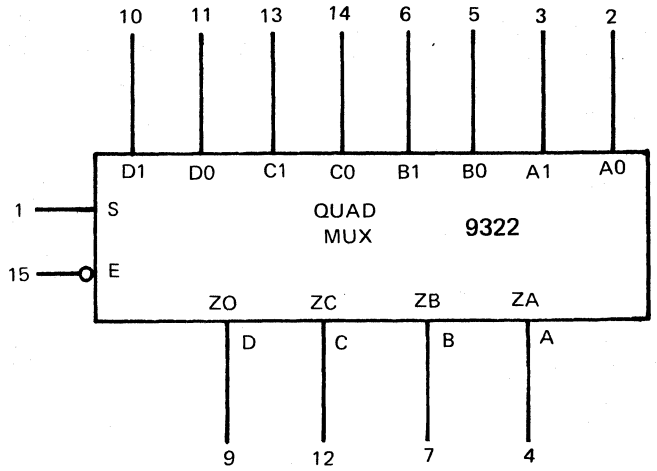


Figure 5-7. Dual One-Of-Four Decoder (7903779)



PIN NAMES

SEL	Common Select Input
EN	Enable Input (Active Low)
(A, B, C, D,)'s	Inputs
Z's	Outputs

DESCRIPTION When the enable is low, this device selects 1 of 2 bits of data from each of four sources. Selection is determined by the condition of the SEL (select) input.

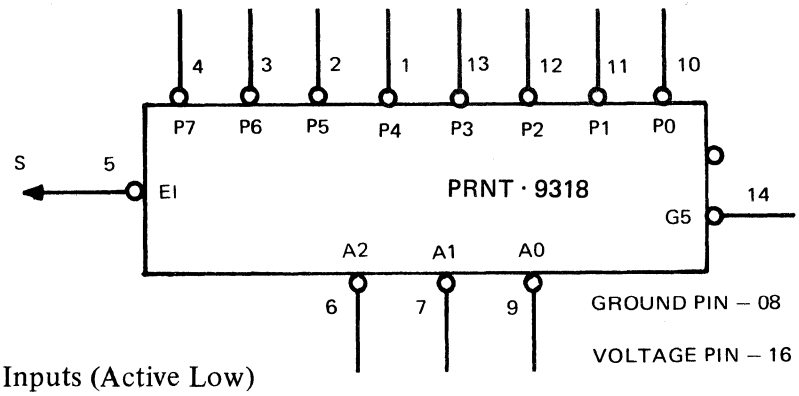
TRUTH TABLE FOR ONE BIT

EN	SEL	ZA
H	X	L
L	L	A0
L	H	A1

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure 5-8. Quad Two-Input Multiplexer (7903780)

Figure 5-9



PIN NAMES

A0 – A7	Priority Inputs (Active Low)
EN IN	Enable Input (Active Low)
EN OUT	Enable Output (Active Low)
GS	Group Select Output (Active Low)
Z0, Z1, Z2	Address Output (Active Low)

DESCRIPTION

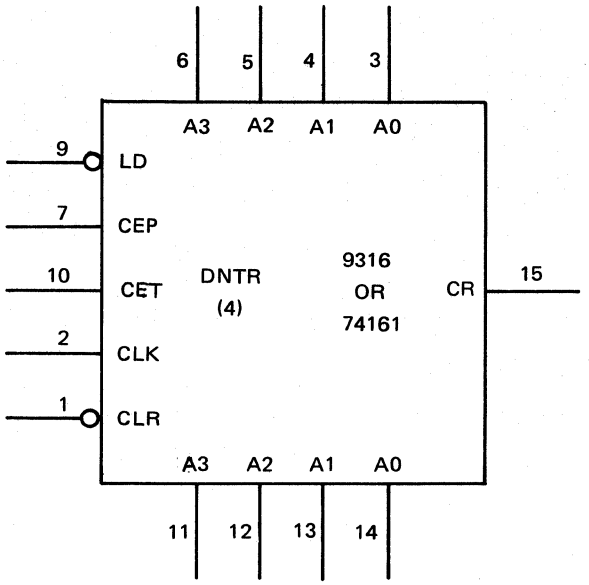
This integrated circuit accepts 8 active low inputs and produces a binary weighted output code of the highest priority input. A priority is assigned to each input such that when two or more inputs are active lows, the input with the highest priority is represented on the output. The order of priority is A7 first, A6 next, - - - -A0 last. The active low input and output enables provide the capability to expand a priority scheme to more inputs. This is accomplished by connecting the output enable of the highest priority network to the input enable of the next highest priority network.

TRUTH TABLE

EN IN	A7	A6	A5	A4	A3	A2	A1	A0	GS	Z2	Z1	Z0	EN OUT
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	X	X	X	X	X	X	X	L	L	L	L	H
L	H	L	X	X	X	X	X	X	L	L	L	H	H
L	H	H	L	X	X	X	X	X	L	L	H	L	H
L	H	H	H	L	X	X	X	X	L	L	H	H	H
L	H	H	H	H	L	X	X	X	L	H	L	L	H
L	H	H	H	H	H	L	X	X	L	H	L	H	H
L	H	H	H	H	H	H	L	X	L	H	H	L	H
L	H	H	H	H	H	H	H	L	L	H	H	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure 5-9. Eight-Input Priority Encoder (7903781)



PIN NAMES

LD	Parallel Enable Input (Active Low)
A3, A2, A1, A0	Parellal Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CLK	Clock (leading positive edge)
CLR	Master Reset (Active Low)
Q3, Q2, Q1, Q0	Parallel Outputs
CR	Terminal Count Output

DESCRIPTION

This device is a 4-bit synchronous binary up counter. The counter output changes state after the low to high transition of the clock.

Mode selection is accomplished as shown below. A restriction is placed on the manner of selection. The transition of CEP or CET from high to low or of ID from low to high may only be done when CLK is high.

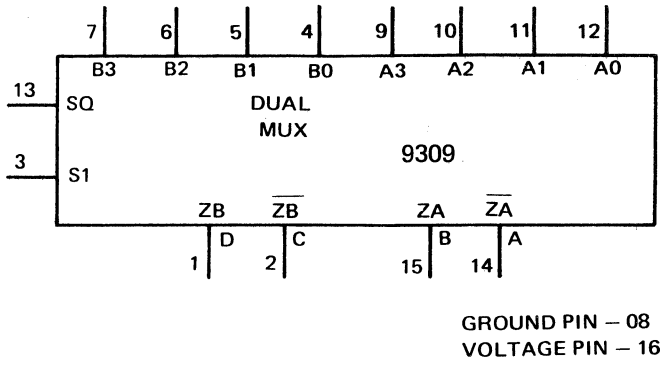
The CLR signal overrides all other signals and will force all outputs low.

MODE SELECTION

CE	LD	MODE
H	H	COUNT UP
L	H	NO CHANGE
X	L	Pre-SET BY A INPUTS

CE = CEP and CET
H = High voltage level
L = Low voltage level
X = Don't care condition

Figure 5-10. Four-Bit Binary Counter (7903782, 7094137)



PIN NAMES

SEL 0, 1	Common Select Inputs
(A, B,)'s	Data Inputs
Z's	Outputs
$\overline{Z}$'s	Complementary Outputs

DESCRIPTION

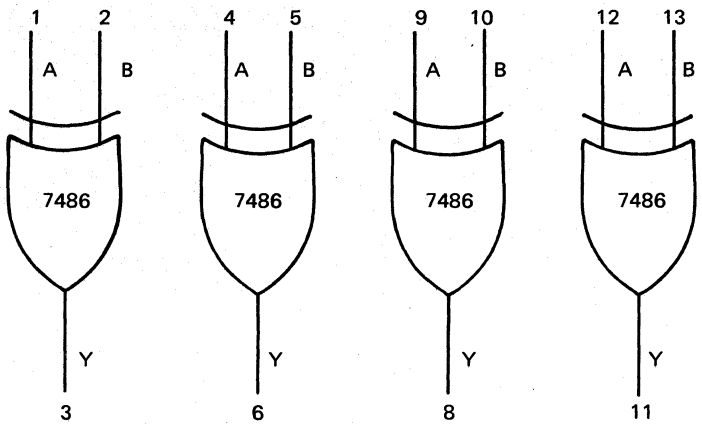
This integrated circuit selects one of four bits of data from each of two differen sources. It is normally used to select data bits from one of four registers.

TRUTH TABLE

	SEL1	SEL0	ZB	$\overline{ZB}$	ZA	$\overline{ZA}$	INPUT PINS ENABLED
(00)	L	L	B0	$\overline{B0}$	A0	$\overline{A0}$	4, 12
(01)	L	H	B1	$\overline{B1}$	A1	$\overline{A1}$	5, 11
(10)	H	L	B2	$\overline{B2}$	A2	$\overline{A2}$	6, 10
(11)	H	H	B3	$\overline{B3}$	A3	$\overline{A3}$	7, 9

H = High voltage level
L = Low voltage level

Figure 5-11. Dual Four-Input Multiplexer (7903783)



DESCRIPTION

This device contains four exclusive OR gates. When either but not both inputs are high the output will be high. When both inputs are either high or low the output will be low.

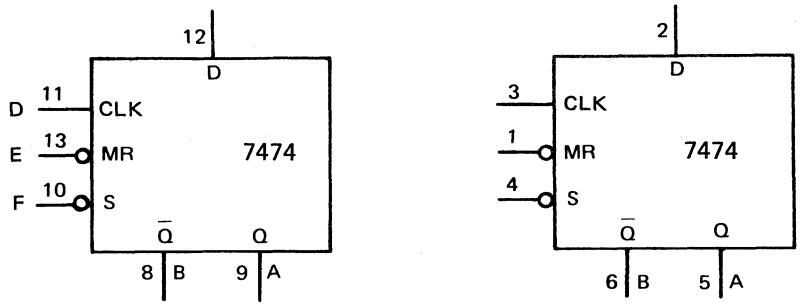
A·B = Y

A·B = Y

A·B = Y

A·B = Y

Figure 5-12. Quadruple, 2-Input Exclusive OR Gate (7903784)



GROUND PIN – 07
VOLTAGE PIN – 14

PIN NAMES

D	Input
CLK	Clock (leading positive edge)
MR	Master Reset (Active Low)
S	Set (Active Low)
Q	Output
$\overline{Q}$	Complementary Output

DESCRIPTION

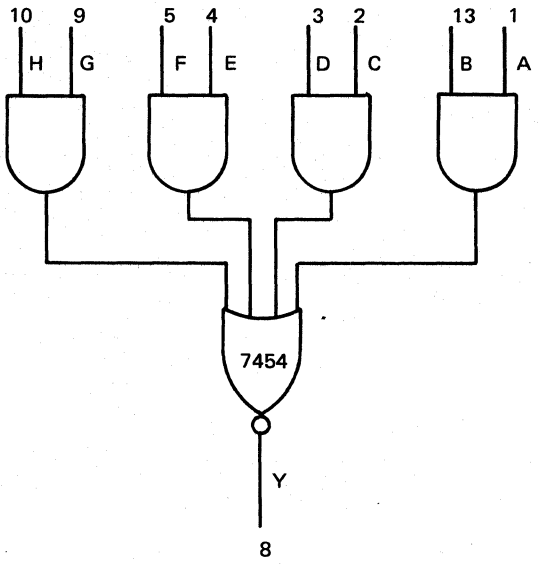
This integrated circuit contains two D type flip-flops with direct clear and set inpu and both Q and $\overline{Q}$ outputs. Information at the D input is transferred to the outputs the positive edge of the clock pulse. The truth table shows the outputs for each inpu The S and MR inputs are independent of the clock. A LOW on the S input sets Q to HIGH. A LOW on the MR input sets Q to a low. A low on both inputs sets Q to a hi and $\overline{Q}$ to a high.

TRUTH TABLE

INPUT	OUTPUTS	
D	Q	$\overline{Q}$
L	L	H
H	H	L

H = High voltage level
L = Low voltage level

Figure 5-13. Dual D Flip-Flop (7903785)

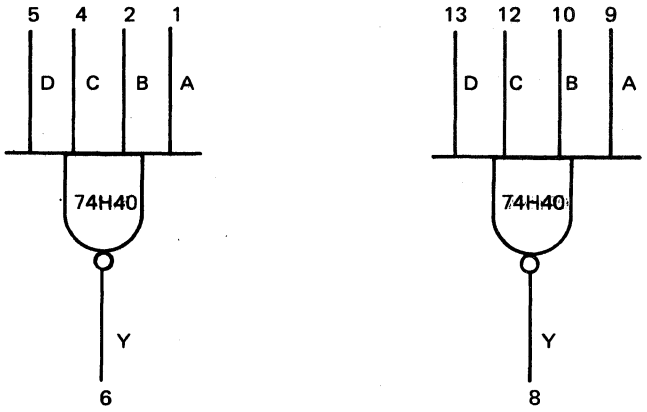


DESCRIPTION

This device contains four dual-input AND gates and an inverting OR output gate. With both inputs to any AND gate a high, a low output will be produced from the inverting OR gate. With at least one input to each AND gate a low, the OR gate output will be a high.

$Y = A \cdot B + C \cdot D + E \cdot F + G \cdot H$

Figure 5-14. Four-Wide, 2-Input, AND-OR Inverter Gate (7903786)

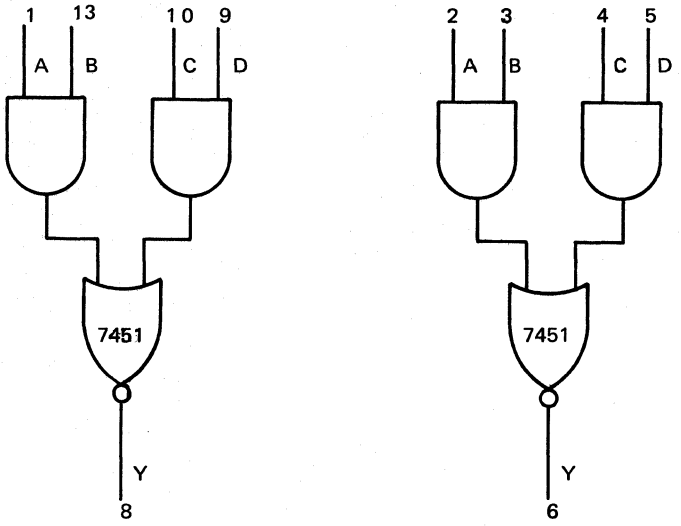


DESCRIPTION

This device contains two 4-input NAND buffer gates. The output of the gate will be low when all four inputs are high. Any input a low will cause the output to be high.

$Y = A \cdot B \cdot C \cdot D$

Figure 5-15. Dual 4-Input Positive NAND Buffer (7903787)

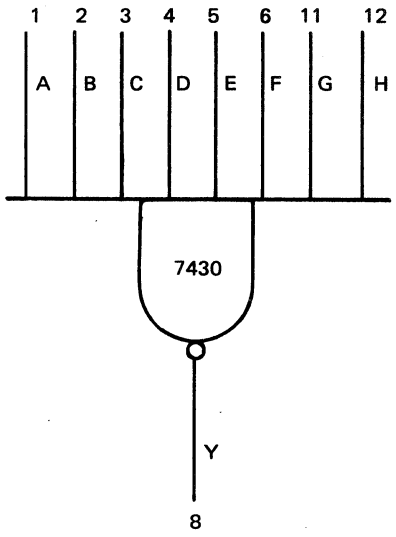


DESCRIPTION

This device contains two inverting circuits consisting of dual 2-input AND gates and an inverting OR. When both inputs to either AND are high, the output of the OR will be low. With at least one input to both ANDs a low, the output of the OR will be high.

$Y = A \cdot B + C \cdot D$

Figure 5-16. Dual 2-Wide, 2-Input AND-OR-Invert (7903788)

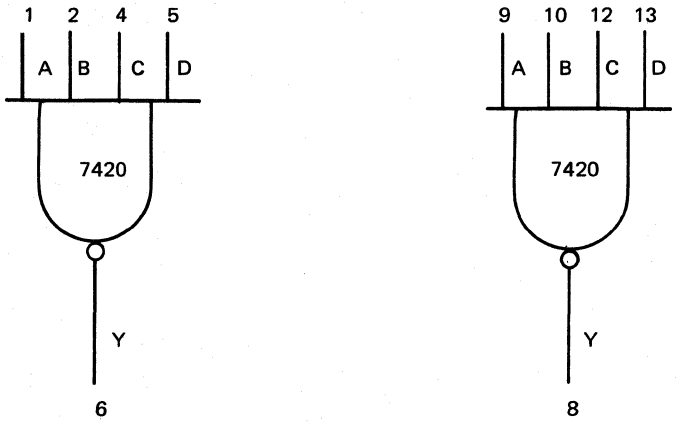


DESCRIPTION

This device contains one 8-input positive NAND Gate. The output is low when all eight inputs are high. Any input a low will cause a high output.

$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$

Figure 5-17. Single 8-Input Positive NAND Gate (7903789)

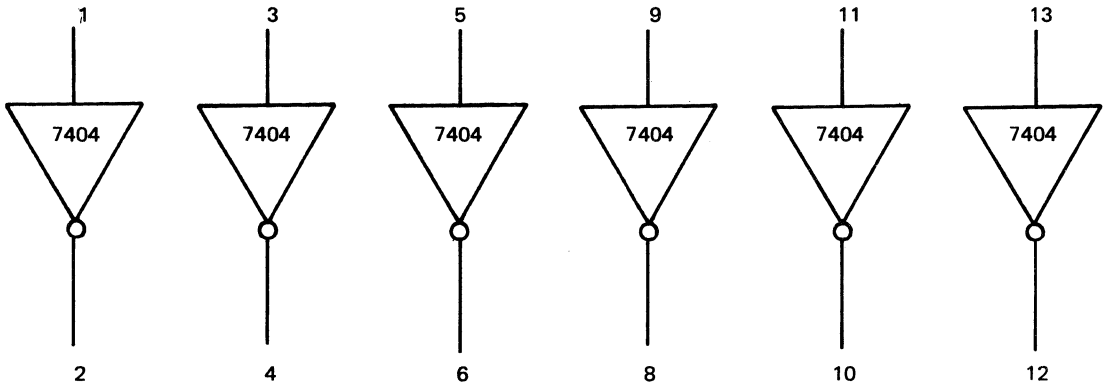


DESCRIPTION

This device contains two 4-input NAND gates. The output of each is low when all four inputs are high. Any one input to a gate will cause its output to be high.

$Y = A \cdot B \cdot C \cdot D$

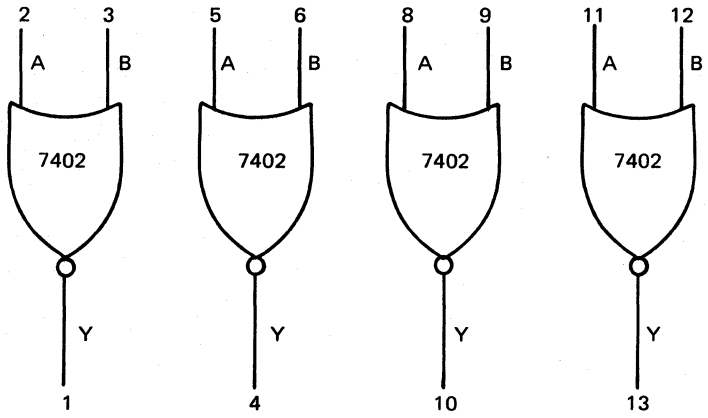
Figure 5-18. Dual 4-Input NAND Gate (7903790)



DESCRIPTION

This device contains six one-input inverter circuits. The output of each is the opposite of the input.

Figure 5-19. Hex Single-Input Inverter Gate (7903791)

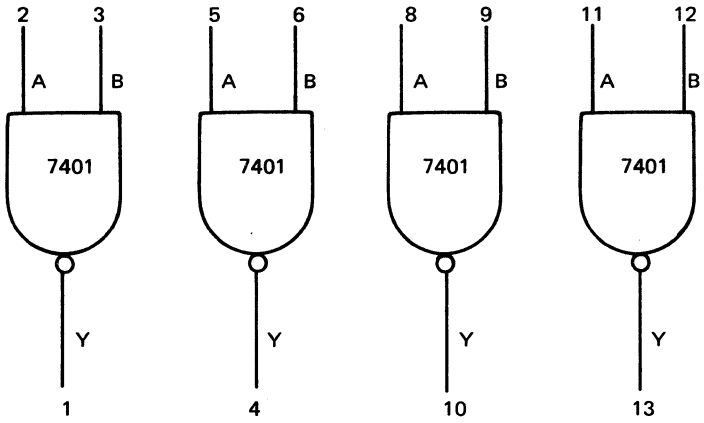


DESCRIPTION

This device contains four 2-input positive NOR gates. The output of each is low when either of its inputs is high. The output of each is high when both of its inputs are low.

$Y = A+B$

Figure 5-20. Quad 2-Input Positive NOR Gate (7903792)

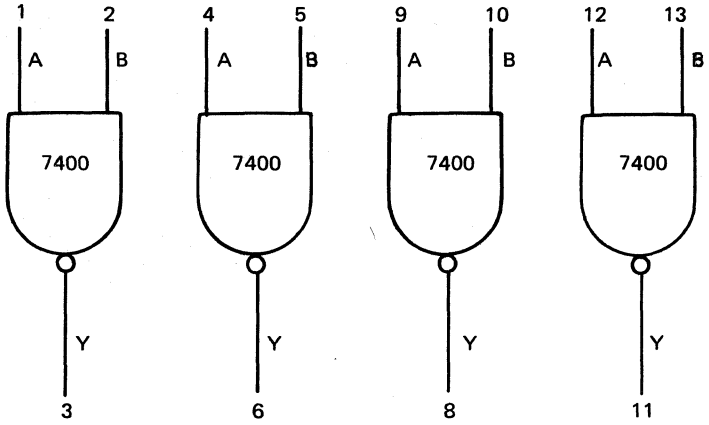


DESCRIPTION

This device contains four 2-input NAND gates with open collector outputs. The output is low when both inputs to the gate are high. The output is high when either input is low.

$Y = A \cdot B$

Figure 5-21. Quad 2-Input NAND Gate, Open Collector (7903793)

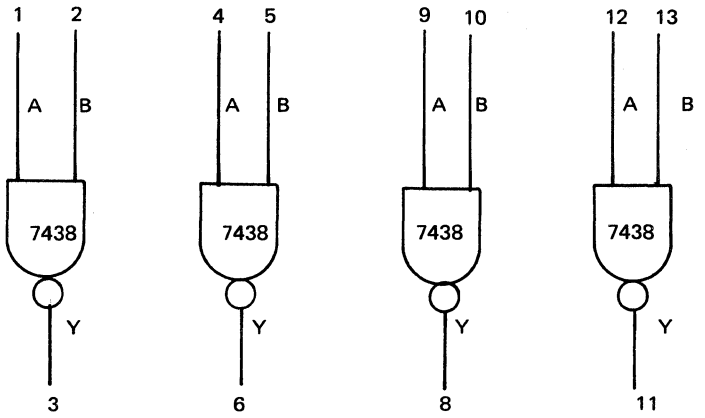


DESCRIPTION

This device contains four 2-input positive NAND gates. The output of each gate is low when both inputs are high. The output is high when either input is low.

$Y = A \cdot B$

Figure 5-22. Quad 2-Input Positive NAND Gate (7903794)

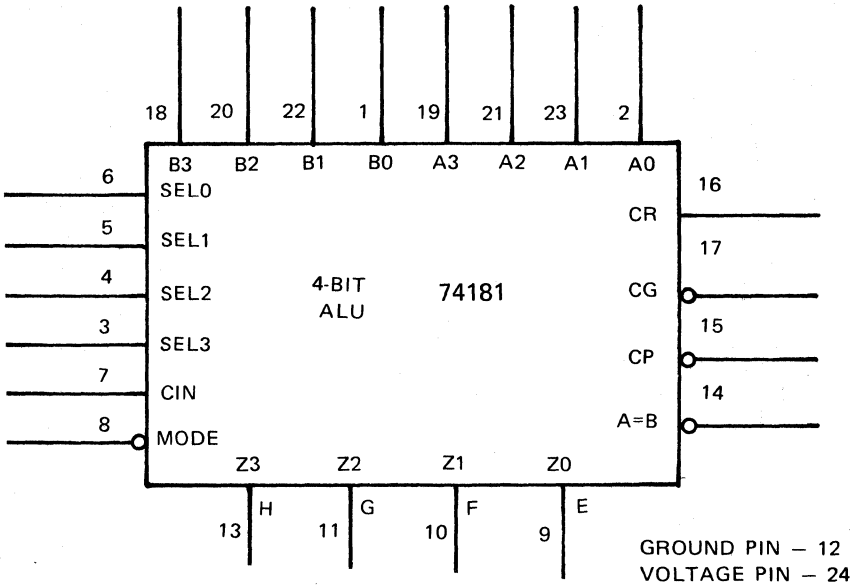


DESCRIPTION

This device contains four 2-input positive NAND buffer gates with open collector outputs. The output of each gate is low when both of its inputs are high. The output is high when either of the inputs are low.

$$\overline{Y} = A \cdot B$$

Figure 5-23. Quad 2-Input Positive NAND Buffer, Open Collector (7903798)



PIN NAMES

A3, A2, A1, A0	Word A Inputs
B3, B2, B1, B0	Word B Inputs
SEL 0 – SEL 3	Function Selection Inputs
CR IN	Carry Input
MODE	Mode Control Input (Active Low)
Z3, Z2, Z1, Z0	Function Outputs
CR	Ripple Carry Output
CR G	Carry Generate Output (Active Low)
CR P	Carry Propagate Output (Active Low)
A = B	Word A Equals Word B

DESCRIPTION

This integrated circuit is a 4-bit high-speed arithmetic logic unit capable of performing 16 different arithmetic operations and 16 different logical operations depending on the condition of the function selection inputs and the mode control inputs. The table shows the possible operations for the adder using active low inputs.

Larger (greater than 4-bit) adders can be built by cascading the less significant CR outputs to the more significant CR IN inputs. By using the CR G and CR P outputs in conjunction with the Carry Lookahead Device propagation time of the ripple carry is reduced.

A = B output goes high when outputs Z0-Z3 are high.

Figure E-20. Four-Bit Arithmetic Logic Unit (Adder) (7903799)

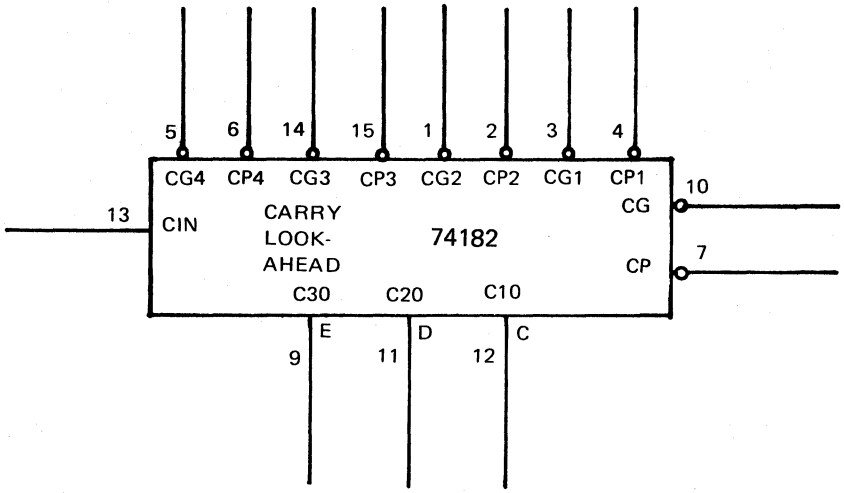
Figure 5-24. Four-Bit Arithmetic Logic Unit (Adder) (7903799) (Sheet 1 of 2)

MODE SELECTION FOR ACTIVE LOW INPUT DATA

SELECTION				MODE=H	MODE=L ARITHMETIC MODE	
S E L 3	S E L 2	S E L 1	S E L 0	LOGIC MODE	CR IN = L (No Carry)	CR IN = H (With Carry)
L	L	L	L	F=$\overline{A}$	F=A MINUS 1	F=A
L	L	L	H	F=$\overline{AB}$	F=A$\overline{B}$ MINUS 1	F=A$\overline{B}$
L	L	H	L	F=$\overline{A+B}$	F=A$\overline{B}$ MINUS 1	F=A$\overline{B}$
L	L	H	H	F=1	F=MINUS 1 (2's comp)	F=ZERO
L	H	L	L	F=$\overline{A}$+B	F=A PLUS (A+$\overline{B}$)	F=A PLUS (A+$\overline{B}$) PLUS 1
L	H	L	H	F=$\overline{B}$	F=AB PLUS (A+$\overline{B}$)	F=AB PLUS (A+$\overline{B}$) PLUS 1
L	H	H	L	F=$\overline{A \oplus B}$	F=A MINUS B MINUS 1	F=A MINUS B
L	H	H	H	F=$\overline{A}$+B	F=A+$\overline{B}$	F=(A+$\overline{B}$) PLUS 1
H	L	L	L	F=$\overline{AB}$	F=A PLUS (A+B)	F=A PLUS (A+B) PLUS 1
H	L	L	H	F=A$\oplus$B	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	F=A$\overline{B}$ PLUS (A+B)	F=A$\overline{B}$ PLUS (A+B) PLUS 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) PLUS 1
H	H	L	L	F=0	F=A PLUS A	F=A PLUS A PLUS 1
H	H	L	H	F=A$\overline{B}$	F=A$\overline{B}$ PLUS A	F=A$\overline{B}$ PLUS A PLUS 1
H	H	H	L	F=AB	F=A$\overline{B}$ PLUS A	F=A$\overline{B}$ PLUS A PLUS 1
H	H	H	H	F=A	F=A	F=A PLUS 1

L = Low voltage level
H = High voltage level

Figure 5-24. Four-Bit Arithmetic Logic Unit (Adder) (7903799) (Sheet 2 of 2)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

CR IN	Carry Input
CG0 – CG3	Carry Generate Inputs (Active Low)
CP0 – CP3	Carry Propagate Inputs (Active Low)
C0, C1, C2	Carry Outputs
CR G	Carry Generate Output (Active Low)
CR P	Carry Propagate Output (Active Low)

DESCRIPTION

This integrated circuit is a high-speed lookahead carry generator. It is used with the 4-bit arithmetic logic unit to provide high-speed lookahead over word length of more than four bits. The lookahead carry generator accepts up to four pairs of Carry Propagate and Carry Generate signals and a Carry Input signal and provides anticipated carries (C0, C1, C2) across four groups of binary adders. The Carry Propagate and Carry Generate outputs are used for further levels of lookahead.

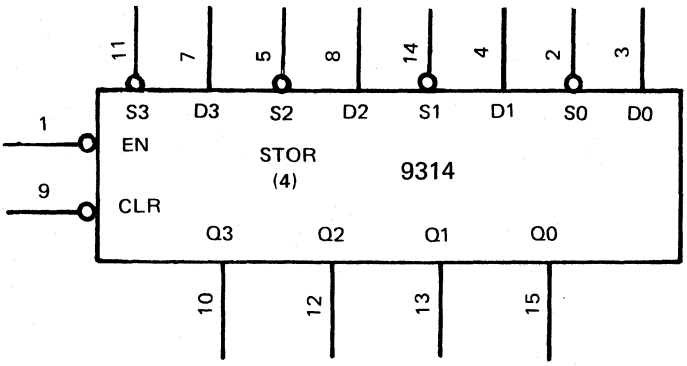
Figure 5-25. Carry Lookahead Unit (7903800) (Sheet 1 of 2)

TRUTH TABLE

INPUTS									OUTPUTS				
CRIN	CG0	CP0	CG1	CP1	CG2	CP2	CG3	CP3	C0	C1	C2	CRG	CRP
X	H	H							H				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

L = Low voltage level
H = High voltage level
X = Irrelevant

Figure 5-25. Carry Lookahead Unit (7903800) (Sheet 2 of 2)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

EN	Enable Input
D3 – D0	Parallel Data Inputs
S3 – S0	Set Inputs (Active Low)
CLR	Master Reset (Active Low)
Q3 – Q0	Parallel Outputs

DESCRIPTION

This integrated circuit is a 4-bit latch which can be used in applications where D type latches or set/reset latches are required.

When the common enable goes high, data present in the latches is stored and the state of the latches is no longer affected by the S and D inputs. The master reset when activated overrides all other input conditions forcing all latch outputs low.

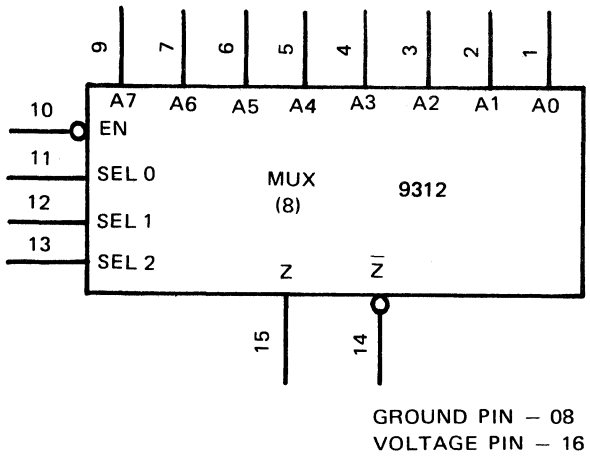
Each of the four latches can be operated either as an active low set/reset latch with reset override or, with S low, as a D type storage latch.

TRUTH TABLE

CLR	EN	D	S	QN	OPERATION
H	L	L	L	L	D MODE
H	L	H	L	H	
H	H	X	X	QN-1	
H	L	L	L	L	R/S MODE
H	L	H	L	H	
H	L	L	H	L	
H	L	H	H	QN-1	
H	H	X	X	QN-1	
L	X	X	X	L	RESET

H = High voltage level
L = Low voltage level
X = Irrelevant
QN-1 = Previous output state
QN = Present output state

Figure 5-26. Four-Bit Latch (7903801)



PIN NAMES

A7 – A0	Inputs
SEL 0, 1, 2	Select Inputs
EN	Enable Input (Active Low)
Z15	Output
Z14	Complementary Output

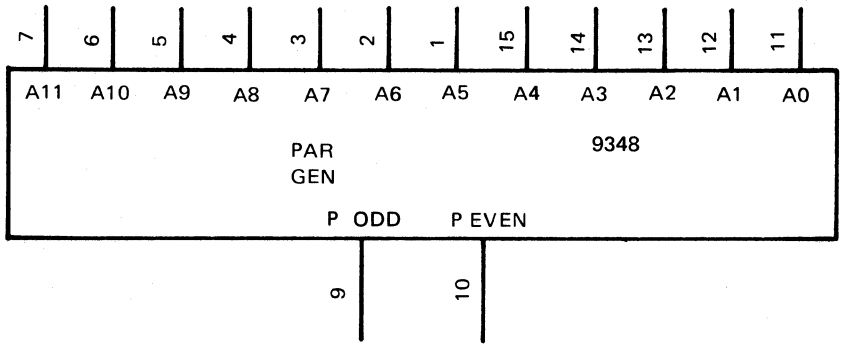
DESCRIPTION When the enable is low, this integrated circuit selects one bit of data from up to eigh sources as determined by SEL inputs.

TRUTH TABLE

	EN	SEL 2	SEL 1	SEL 0	Z15	Z14
	H	X	X	X	L	$\overline{H}$
(000)	L	L	L	L	A0	$\overline{A0}$
(001)	L	L	L	H	A1	$\overline{A1}$
(010)	L	L	H	L	A2	$\overline{A2}$
(011)	L	L	H	H	A3	$\overline{A3}$
(100)	L	H	L	L	A4	$\overline{A4}$
(101)	L	H	L	H	A5	$\overline{A5}$
(110)	L	H	H	L	A6	$\overline{A6}$
(111)	L	H	H	H	A7	$\overline{A7}$

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure 5-27. Eight-Input Multiplexer (7903803)



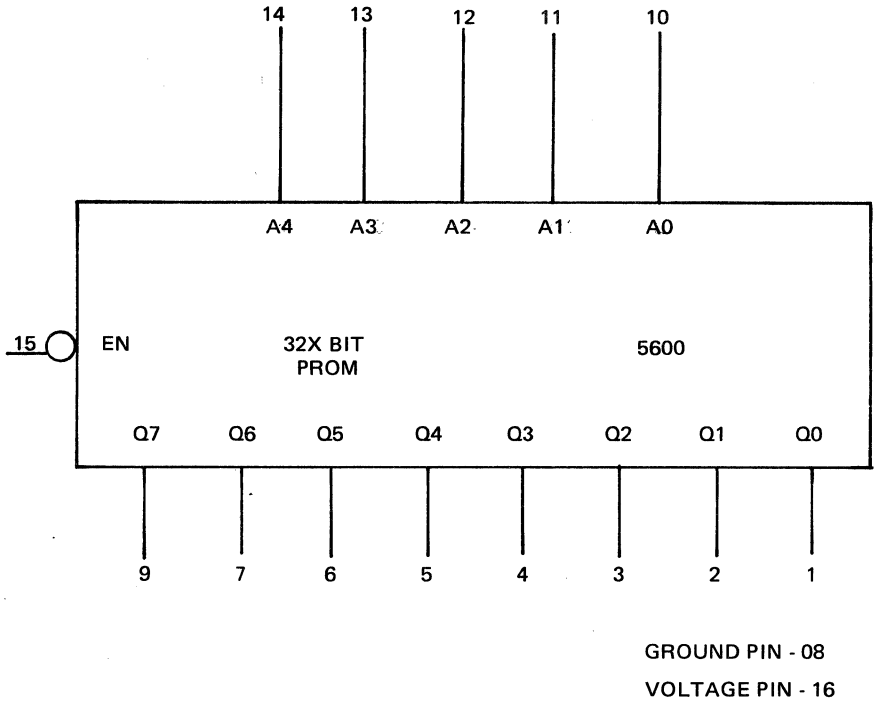
GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

A11 – A0	Parity Inputs
P ODD	Odd Parity Output
P EVEN	Even Parity Output

DESCRIPTION This device is a 12-bit parity checker/generator generating odd and even parity outputs. The even parity output will be high if an even number of inputs are high. The odd parity output will be high if an odd number of inputs are high.

Figure 5-28. 12-Bit Parity Checker/Generator (7903908)



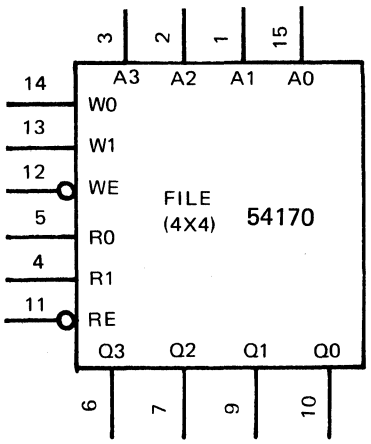
PIN NAMES

A4 - A0	Address Inputs
Q7 - Q0	Outputs
EN	Enable

DESCRIPTION

This device is a 256-bit Read Only Memory containing thirty-two 8-bit words. The five address inputs select the desired word. The eight outputs are enabled by the EN output.

Figure 5-29. 256-Bit Read Only Memory (7903993)



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

A3 – A0	Inputs
W1, W0	Write Address Inputs
WE	Write Enable (Active Low)
R1, R0	Read Address Inputs
RE	Read Enable (Active Low)
Q3 – Q0	Outputs

DESCRIPTION

This integrated circuit contains 16 flip-flops used to hold four-bit words. The write address inputs (W1, W0) select the word location to store the data inputs (A3-A0). The data is gated to the selected location when the write enable (WE) is low. The read address inputs (R1, R0) select the word location to place on the data outputs (Q3-Q0). Data is gated to the outputs when the read enable (RE) is low.

TRUTH TABLES

WRITE FUNCTION

Inputs			Word Selected
W1	WO	WE	
L	L	L	Word 0
L	H	L	Word 1
H	L	L	Word 2
H	H	L	Word 3
X	X	H	No change

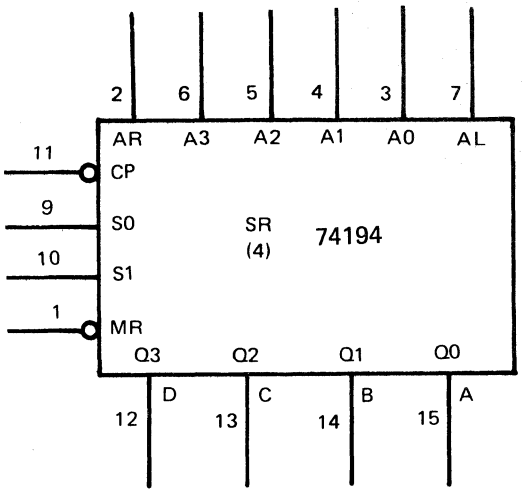
READ FUNCTION

Inputs			Outputs			
R1	RO	RE	Q3	Q2	Q1	Q0
L	L	L		Word 0		
L	H	L		Word 1		
H	L	L		Word 2		
H	H	L		Word 3		
X	X	H	H	H	H	H

H = High voltage level
L = Low voltage level
X = Irrelevant

Figure 5-30. 4X4 Register File (7904135)

Figure 5-31



GROUND PIN – 08
VOLTAGE PIN – 16

PIN NAMES

A3 – A0	Parallel Data Inputs	S0, S1	Mode Selection Inputs
AL	Shift Left Serial Input	CLR	Master Reset Input (Active Low)
AR	Shift Right Serial Input	Q3 – Q0	Parallel Data Outputs
CLK	Clock Input (Active Low)		

DESCRIPTION

This integrated circuit is a 4-bit shift register with four modes of operation; paral load, shift left, shift right, and hold. The mode of operation is determined by the mo selection inputs (S0, S1) as shown in the truth table. Data is loaded or shifted by t negative going edge of the clock pulse. For a left shift operation, data is shifted in t direction of Q3 toward Q0 with the contents of Q0 shifted off and the serial inp (AL) loaded into Q3. For a right shift operation, data is shifted in the direction of (toward Q3 with the contents of Q3 shifted off and the serial input (AR) loaded in Q0.

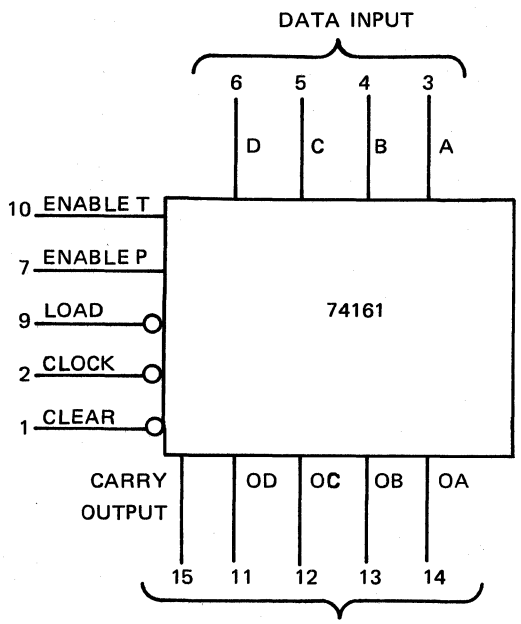
The master reset (active low) forces all outputs low.

MODE SELECTION

Inputs			Mode
CLR	S1	S0	
H	H	H	Parallel Load
H	L	H	Shift Right (in direction Q0 toward Q3)
H	H	L	Shift Left (in direction Q3 toward Q0)
H	L	L	Hold (inhibit clock)
L	X	X	Reset

L = Low voltage level
H = High voltage level
X = Irrelevant

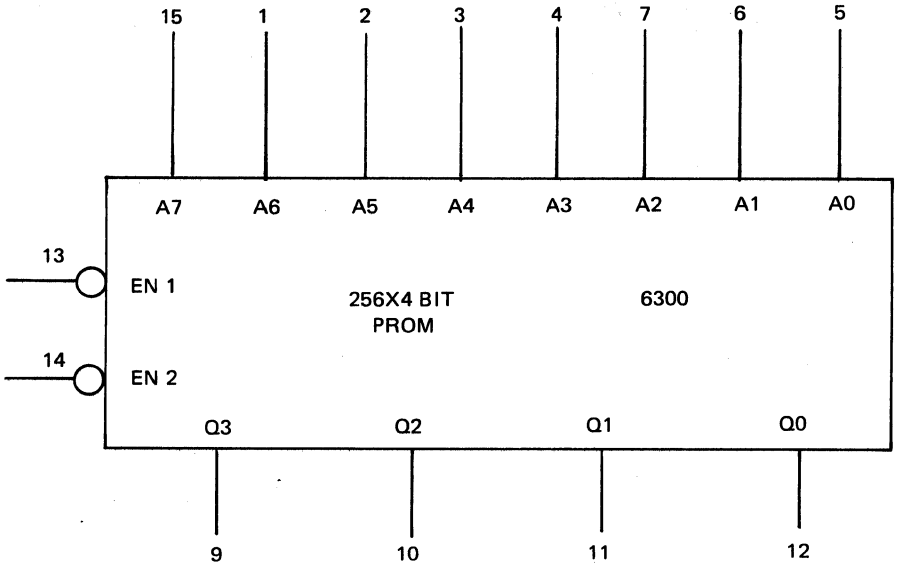
Figure 5-31. Shift Register (7904136)



ESCRIPTION

This device contains a four-bit synchronous, presettable binary counter with carry look-ahead for high speed counting. Synchronous operation is achieved by having all flip-flops clocked simultaneously. A buffered clock input triggers four master-slave flip-flops on the rising edge of the input clock. The counter may be preset to any obtainable value. A low input on the LOAD pin disables the counter and allows the value on the DATA INPUT pins to be entered into the counter by the next clock pulse regardless of the ENABLE T and P inputs. A low on the CLEAR pin clears all flip-flops. The carry look-ahead circuit provides for an n-bit synchronous counter. The two ENABLE inputs and the CARRY OUTPUT provides for expanded counters. Both the ENABLE P and T must be a high for the count function. The ENABLE T input is used to enable the CARRY OUTPUT. The CARRY OUTPUT is used to enable successive stages of the counter. High-to-low level transitions at the ENABLE P or T inputs occur only when the CLOCK input is high.

Figure 5-32. Four-bit Binary Counter (7904137)



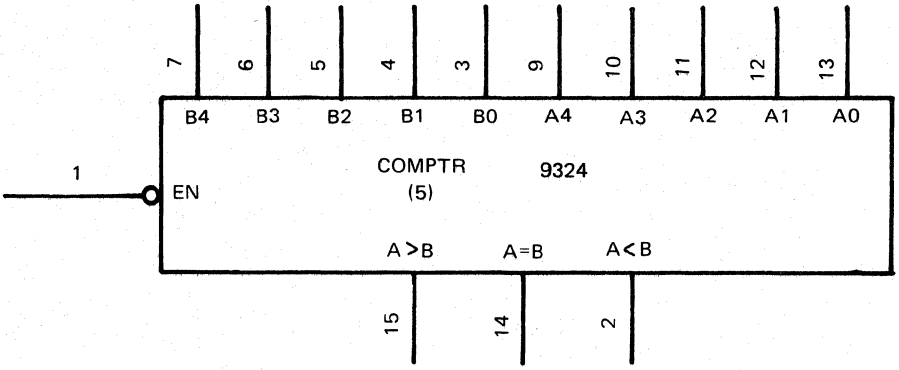
PIN NAMES

A7 - A0	Address Inputs
EN1, EN2	Enables
Q3 - Q0	Outputs

DESCRIPTION

This device is a 1024-bit Read Only Memory containing 256 4-bit words. The eight address inputs select the desired word. The four outputs are enabled by the EN1 and EN2 inputs.

Figure 5-33. 1024-Bit Read Only Memory (7904152)



GROUND PIN – 08
VOLTAGE PIN – 16

IN NAMES

,4 – A0	Word A Parallel Inputs
;4 – B0	Word B Parallel Inputs
;N	Enable Input (Active Low)
, > B	A Greater than B Output
, < B	A Less Than B Output
,=B	A Equal to B Output

)ESCRIPTION

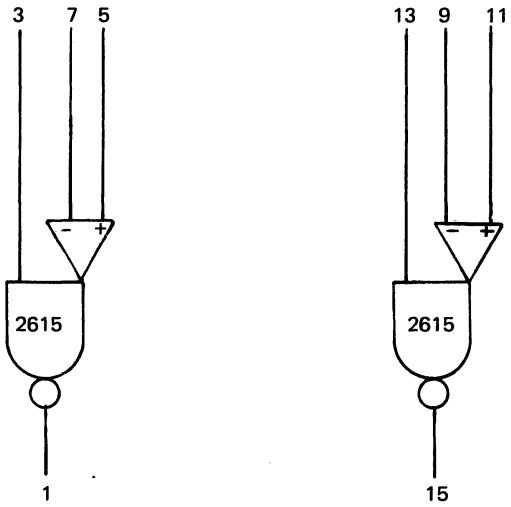
This circuit compares two 5-bit words and provides three outputs, "less than," "greater than," and "equal to." The A4 and B4 inputs are the most significant inputs and A0, B0 are the least significant. All three outputs are activated by a low enable input (EN). Connecting the A > B output from one device into an A input on another device and the A < B output into the corresponding B input permits easy expansion.

'RUTH TABLE

EN	Word A		Word B	A>B	A < B	A=B
H	X		X	L	L	L
L	Word A	>	Word B	H	L	L
L	Word A	<	Word B	L	H	L
L	Word A	=	Word B	L	L	H

H = High voltage level
L = Low voltage level
X = Irrelevant

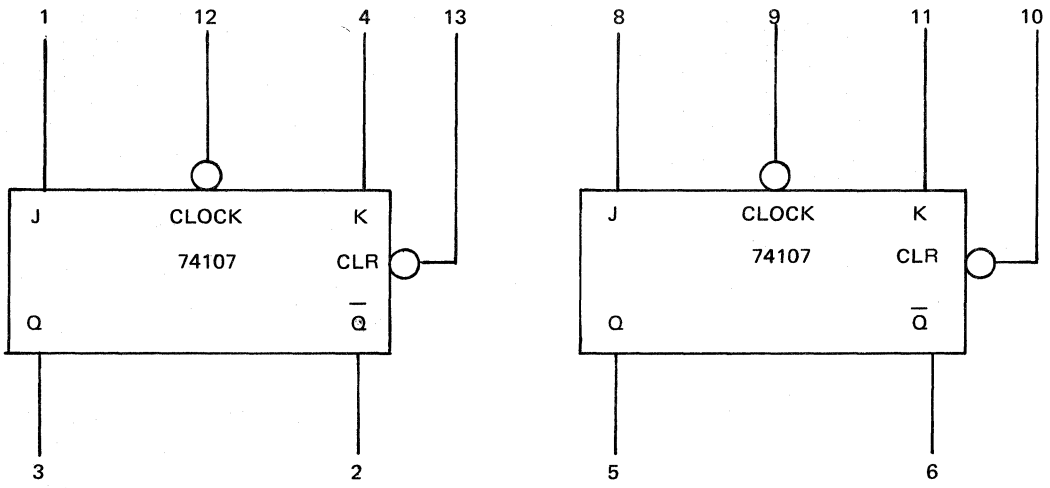
Figure 5-34. Five-Bit Comparator (7904164)



DESCRIPTION

This device contains two differential line receivers with open collectors. Differential digital data is received at the amplifier section. The data is gated by the input to the AND section. The gate function allows the use of this device in multicomputer configurations.

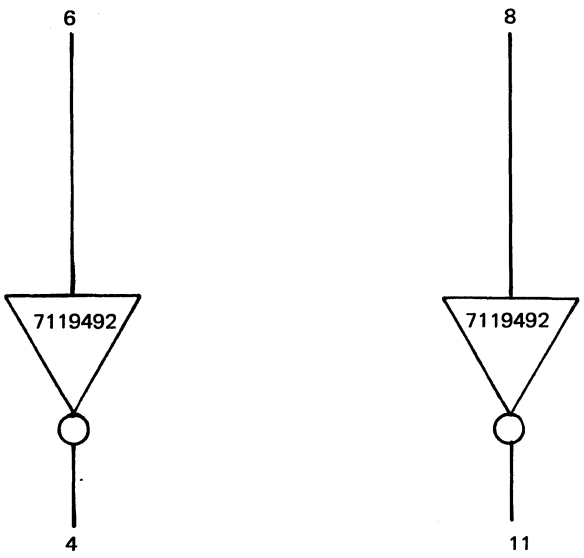
Figure 5-35. Dual Differential Line Receiver (7904174)



)ESCRIPTION

This device contains two J-K master-slave flip-flops with clear capability. When the clear input is low, the flip-flop will be cleared regardless of the other inputs. When the J and K inputs are dissimilar, the information will be clocked into the flip-flop. With both the J and K inputs a low, no change in state will occur when a clock pulse is received. With bot the J and K inputs a high, the flip-flop will be toggled when a clock pulse is received. The clock pulse going from low to high gates the J-K information into the master flip-flop. The high to low transition transfers from the master-to-slave flip-flop.

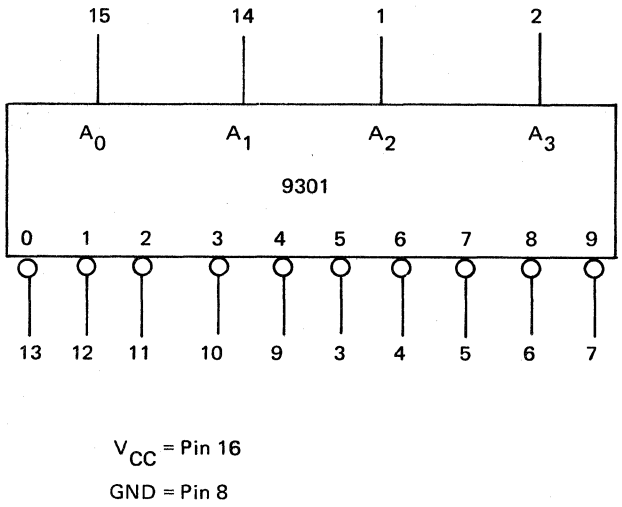
Figure 5-36. Dual J-K Master-Slave Flip-Flop With Clear (7904196)



DESCRIPTION

This device contains two -3 volt line drivers used to drive output lines. A ground signal in will cause a ground (external logic 1) signal out. A +5 volt signal in will cause a -3 volt (external logic 0) out.

Figure 5-37. Dual -3 Volt Line Driver (7904200)



PIN NAMES

A_0, A_1, A_2, A_3	Address Inputs
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW

DESCRIPTION

This device contains a BCD-to-decimal decoder of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

Figure 5-38. One-of-Ten Decoder (7904259) (Sheet 1 of 2)

LOGIC CONFIGURATION

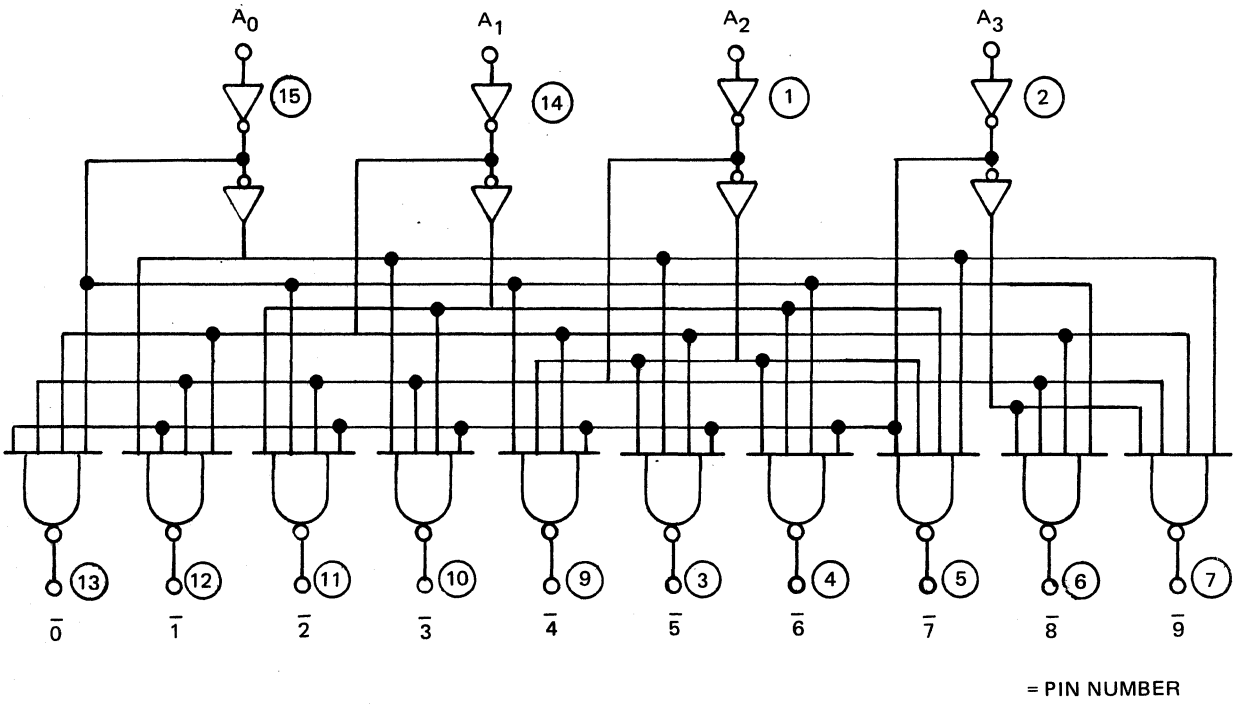
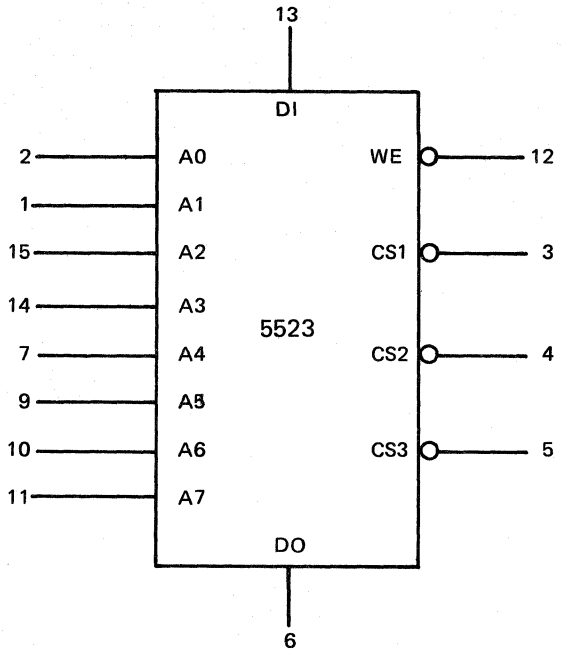


Figure 5-38. One-of-Ten Decoder (7904259) (Sheet 2 of 2)



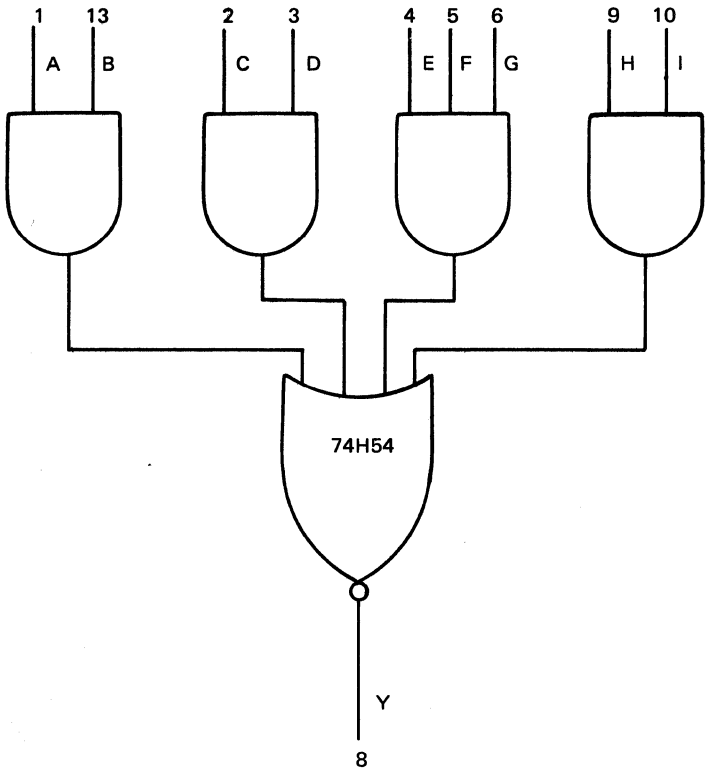
PIN NAMES

A0-A7	Address Inputs
CS1-CS3	Chip Selector Inputs
WE	Write Enable
DI	Data Input
DO	Data Output

DESCRIPTION

This device contains 256 one-bit memory locations addressable for either a read or write function. The complement of the information at the data input is written into the selected location when all chip selector inputs and the write enable are low. While the write enable input is low, the output is in a high resistance state which will neither load or drive the output line. The stored information, the complement of the input, is available at the output when the write enable is high and the three chip selector inputs are low. If any of the chip selector inputs is high, the output will be in the high resistance state.

Figure 5-39. 256-Bit Random Access Memory, 3-State Output (7904274)



DESCRIPTION

This device contains an inverting OR gate which has three two-input AND gates and one three-input AND gate as inputs. The output of the OR will be low when all inputs to any AND are high. The output of the OR gate will be high when at least one input to all ANDs are low.

Figure 5-40. Single, 2-2-2-3 AND-OR-INVERT Gate (7904418)

SECTION 6

PARTS LIST

6-1. INTRODUCTION.

THIS ILLUSTRATED PARTS BREAKDOWN (IPB) LISTS AND ILLUSTRATES THE FIELD-REPLACEMENT PARTS FOR THE DIGITAL MAGNETIC TAPE RECORDER-REPRODUCER.

THIS IPB SHOULD NOT BE USED FOR DISASSEMBLY OR ASSEMBLY PROCEDURES.

6-2. GROUP ASSEMBLY PARTS LIST.

THE GROUP ASSEMBLY PARTS LIST CONSISTS OF ILLUSTRATIONS AND LISTINGS OF ASSEMBLIES AND DETAIL PARTS. THE ACCOMPANYING ILLUSTRATION PRECEDES THE PARTS BREAKDOWN LISTING FOR EACH ASSEMBLY. EACH ASSEMBLY IS FOLLOWED BY A LISTING OF ITS COMPONENT PARTS.

A. FIGURE AND INDEX NUMBER COLUMN. - THIS COLUMN SHOWS THE FIGURE NUMBER OF THE ASSEMBLY AND ALL COMPONENT PART INDEX NUMBERS. EACH NEW ASSEMBLY SECTION AND FIGURE NUMBER IS CARRIED FORWARD AS THE FIRST ENTRY OF EACH SUCCEEDING PAGE.

B. REFERENCE DESIGNATION COLUMN. - THIS COLUMN LISTS THE REFERENCE DESIGNATOR ASSIGNED TO THE ASSEMBLY OR DETAIL PART. THESE DESIGNATORS COINCIDE WITH THE DESIGNATIONS MARKED ON THE EQUIPMENT, DRAWINGS, AND DIAGRAMS.

C. INDENTURE COLUMN. - THIS COLUMN IS CODED NUMERICALLY TO SHOW RELATIONSHIP TO THE NEXT HIGHER ASSEMBLY.

D. DESCRIPTION. - THIS COLUMN LISTS THE ITEM NAME OF A PART OR ASSEMBLY FOLLOWED BY AN IDENTIFYING DESCRIPTION. ATTACHING PARTS ARE LISTED IMMEDIATELY FOLLOWING THE ASSEMBLY OR PART WHICH THEY SECURE.

THE ABBREVIATIONS NHA, NLA, U/W AND AP APPEARING IN THE DESCRIPTION COLUMN HAVE THE FOLLOWING MEANINGS- NHA INDICATES NEXT HIGHER ASSEMBLY, NLA INDICATES NEXT LOWER ASSEMBLY, U/W INDICATES USED WITH, AND AP INDICATES ATTACHING PARTS.

E. MANUFACTURERS CODE. - THE FEDERAL SUPPLY CODE FOR MANUFACTURERS (FSCM) IS A CODING SYSTEM OF FIVE-DIGIT NUMBERS ASSIGNED TO MANUFACTURERS HAVING DESIGN CONTROL OF ITEMS OF SUPPLY PROCURED BY AGENCIES OF THE FEDERAL GOVERNMENT. THE CODES USED IN THIS SECTION ARE LISTED IN NUMERICAL SEQUENCE IN TABLE 6-1.

F. PART NUMBER COLUMN. - THE FIRST ENTRY IN THIS COLUMN IS THE UNIVAC PART NUMBER, OR UNIVAC SPECIFICATION DRAWING NUMBER, WITH THE CORRESPONDING GOVERNMENT PART NUMBER OR VENDOR PART NUMBER AS THE NEXT ENTRY.

A COML ENTRY INDICATES THAT THE PART MAY BE PURCHASED COMMERCIALLY.

G. UNITS PER ASSEMBLY. - THIS COLUMN LISTS THE QUANTITY OF PARTS PER ASSEMBLY. WHEN EQUIPMENT CONTAINS TWO OR MORE IDENTICAL ASSEMBLIES, OR IF SIMILAR ASSEMBLIES HAVE BEEN COMBINED IN ONE ILLUSTRATION, THIS COLUMN WILL INDICATE THE QUANTITY OF PARTS FOR ONE ASSEMBLY ONLY.

TWO ABBREVIATIONS ARE USED IN THIS COLUMN; REF AND AR. THE REF INDICATES THE QUANTITY USED ON AN ASSEMBLY PREVIOUSLY CONSIDERED. THE AR INDICATES A QUANTITY AS REQUIRED.

H. USED ON CODE COLUMN. - LETTER CODES IN THIS COLUMN INDICATE VARIATIONS OF PARTS AND ASSEMBLIES WHICH BECAUSE OF THEIR PHYSICAL SIMILARITY HAVE BEEN COMBINED ON ONE ILLUSTRATION. NO CODE SIGNIFIES THE PART IS USED ON ALL ASSEMBLIES.

6-3. NUMERICAL INDEX.

THE NUMERICAL INDEX PROVIDES ALL THE PART NUMBERS IN ALPHANUMERIC ORDER. THE FIGURE AND INDEX NUMBERS ARE GIVEN FOR EACH PART TO AID IN LOCATING THE PART IN THE GROUP ASSEMBLY PARTS LIST. THIS INDEX IS LOCATED AT THE END OF THE SECTION.

TABLE 6-1. LIST OF MANUFACTURERS

CODE	NAME	ADDRESS
00779	AMP INC	PO BOX 3608 HARRISBURG PA 17105
03508	GENERAL ELECTRIC CO SEMI-CONDUCTOR PRODUCTS DEPT	ELECTRONICS PARK SYRACUSE NY 13201
05236	JONATHAN MFG CO	1101 SOUTH ACACIA AVE FULLERTON CA 92631
07115	CORNING GLASS WORKS ELECTRONIC COMPONENTS DEPARTMENT	BRADFORD PA
07137	TEC INC	6700 WASHINGTON AVE SOUTH EDEN PRAIRIE MN 55343
12969	UNITROBE CORP	580 PLEASANT STREET WATERTOWN MA 02172
18324	SIGNETICS CORP	811 EAST ARGUES AVE SUNNYVALE CA 94086
21845	SOLITRON DEVICES INC TRANSISTOR DIVISION	1177 BLUE HERON BLVD RIVIERA BEACH FL 33404
22526	BERG ELECTRONICS INC	YOUK EXPRESSWAY NEW CUMBERLAND PA 17070
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA 01247
71286	REX CHAINBELT INC CAMLOC DIVISION	22 SPRING VALLEY ROAD PARAMUS NJ 07652
71468	ITT CANNON ELECTRIC	666 EAST DYER ROAD SANTA ANA CA 92702
71590	CENTRALAB ELECTRONICS DIVISION OF GLOBE-UNION INC	5757 NORTH GREEN BAY AVE MILWAUKEE WI 53201
71744	CHICAGO MINIATURE LAMP WORKS	4433 RAVENSWOOD AVE CHICAGO IL 60640
72969	ELLIOTT-LEWIS ELECTRICAL CO INC	PHILADELPHIA PA
73803	TEXAS INSTRUMENTS INC METALLURGICAL MATERIALS DIVISION	ATTLEBORO MA 02703
75382	KULKA ELECTRIC CORP	633-643 SOUTH FULTON AVE MOUNT VERNON NY 10550
80252	FARADAY INC	805 SOUTH MAUMEE STREET TECUMSEH MI 49286
81312	WINCHESTER ELECTRONICS DIVISION OF LITTON INDUSTRIES INC	MAIN STREET AND HILLSIDE AVE OAKVILLE CT 06779
81349	MILITARY SPECIFICATION PROMULGATED	UNDER AUTHORITY OF DEFENSE

TABLE 6-1. LIST OF MANUFACTURERS

CODE	NAME	ADDRESS
81349	BY MILITARY DEPARTMENTS/AGENCIES	STANDARDIZATION MANUAL 4120 3-M
82877	ROTRON INC	7-9 HASBROUCK LANE WOODSTOCK NY 12498
90536	SPERRY UNIVAC DEFENSE SYSTEMS	UNIVAC PARK PO BOX 3525 ST PAUL MN 55165
91812	JANCO CORP	3111 WINONA AVE BOX 3038 BURBANK CA 91504
91929	HONEYWELL INC MICRO SWITCH DIVISION	CHICAGO AND SPRING STREETS FREEPORT IL 61032
92702	IMC MAGNETICS CORP EASTERN DIVISION	570 MAIN STREET WESTBURY LONG ISLAND NY 11591
96906	MILITARY STANDARDS PROMULGATED BY MILITARY DEPARTMENTS UNDER	AUTHORITY OF DEFENSE STANDARDIZATION MANUAL 4120 3-M

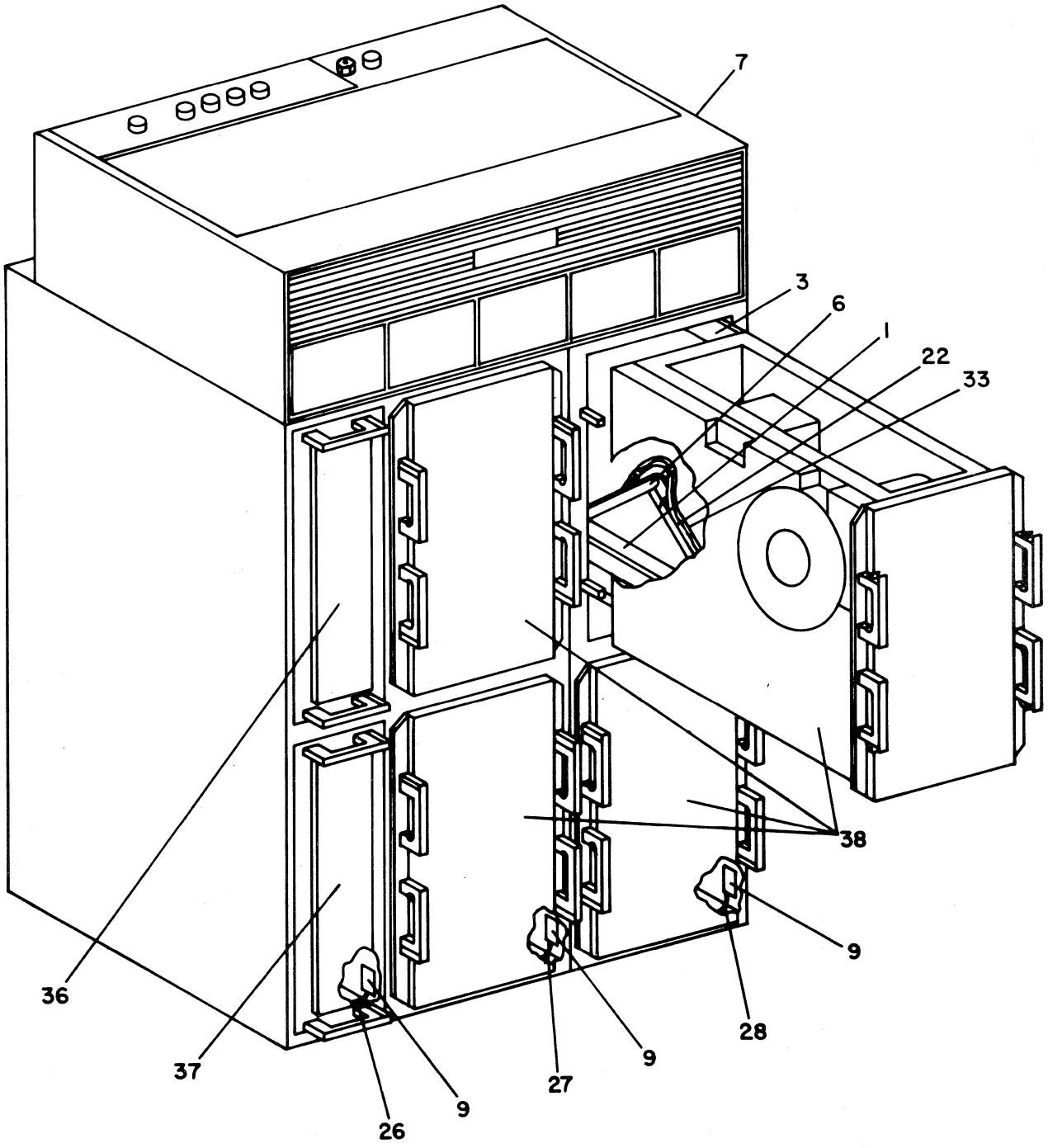


FIGURE 6-1. DIGITAL MAG TAPE RECORDER-REPRODUCER (SHEET 1 OF 2)

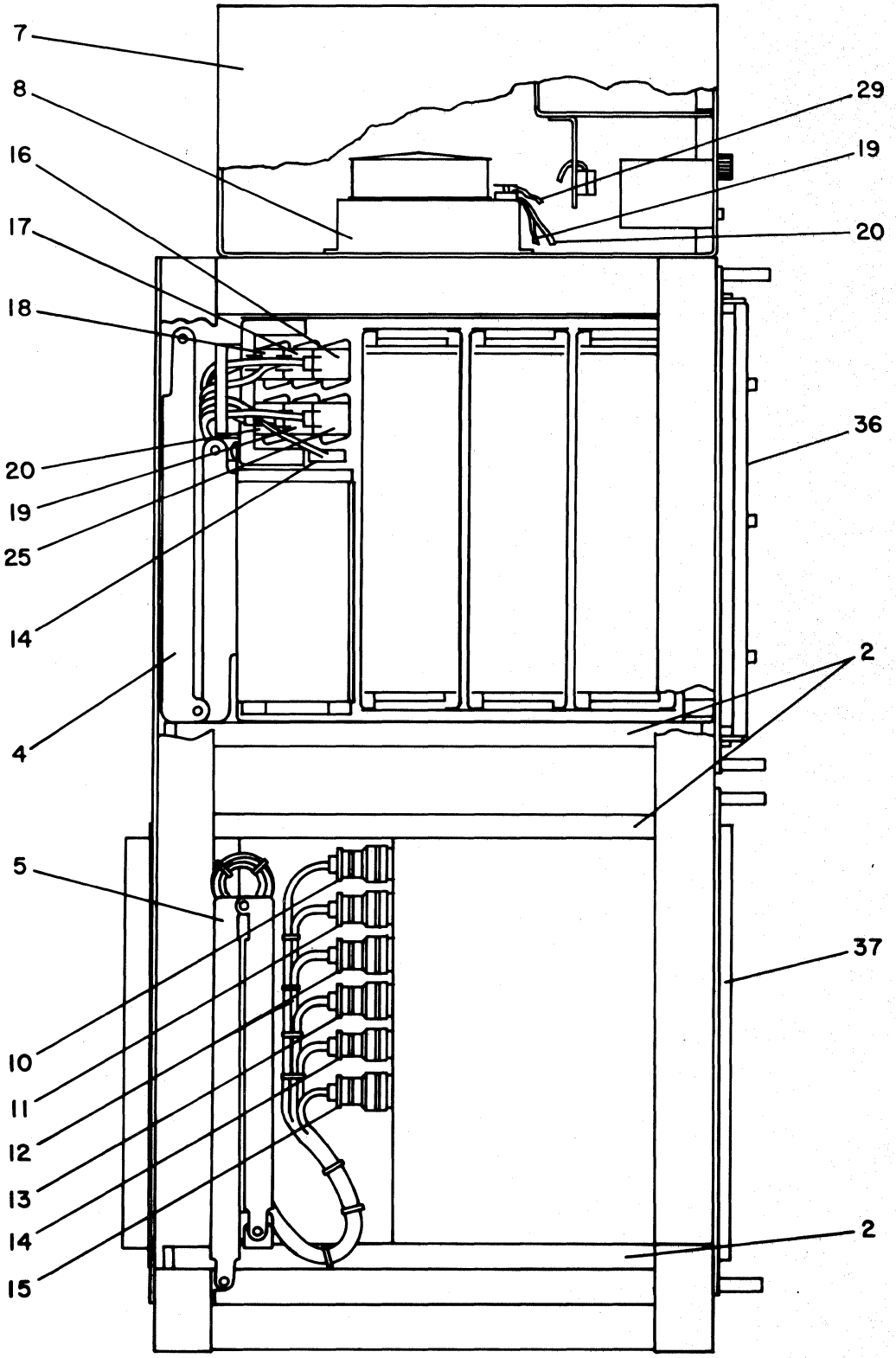


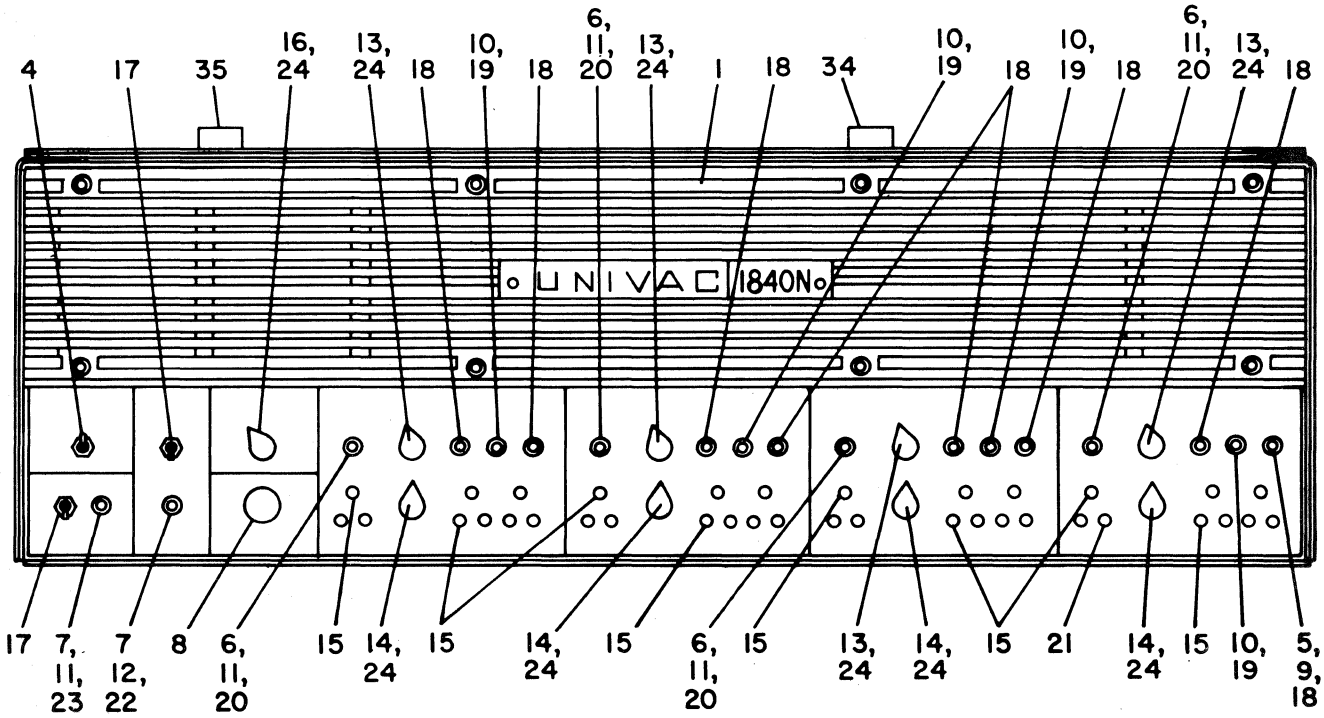
FIGURE 6-1. DIGITAL MAG TAPE RECORDER-REPRODUCER (SHEET 2 OF 2)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USE ON
6- 1		1	RECORDER-REPRODUCER, DIGITAL MAGNETIC TAPE	90536	7059800-03	1	A
			RECORDER-REPRODUCER, DIGITAL MAGNETIC TAPE	90536	7059800-04	1	B
			RECORDER-REPRODUCER, DIGITAL MAGNETIC TAPE	90536	7059800-05	1	C
			RECORDER-REPRODUCER, DIGITAL MAGNETIC TAPE	90536	7059800-06	1	D
1-1		2	SLIDE, TELESCOPIC, 26 INCH SLIDE LENGTH, QUICK DISCONNECT	05236	7904291-00 05236-300321	4	
1		2	SCREW, MACH, FLAT HD 10-32UNF-2A, 0.750 L (AP)	96906	7903133-51 MS24693-C274	8	
			SCREW, MACH, FLAT HD 1/4-28UNF-2A, 0.750 L (AP)	96906	7903133-70 MS24693-C296	16	
			WASHER, FLAT, SIZE 1/4 (AP)	96906	4912548-04 MS15795-810	16	
			NUT, SELF-LOCKING, HEX 1/4-28UNF-3B (AP)	96906	4912794-01 MS21044-C4	16	
1-2		2	SLIDE, TELESCOPIC, 24 INCH SLIDE LENGTH, QUICK DISCONNECT	05236	7903167-03 620411-R	4	
1		2	SCREW, MACH, FLAT HD 1/4-28UNF-2A, 0.750 L (AP)	96906	7903133-70 MS24693-C296	16	
			SCREW, MACH, FLAT HD 1/4-28UNF-2A, 1.000 L (AP)	96906	7903133-72 MS24693-C298	8	
1-3		2	SLIDE, TELESCOPIC, 24 INCH SLIDE LENGTH, QUICK DISCONNECT		7904590-00 TO BE ESTAB	4	
1		2	SCREW, MACH, FLAT HD 10-32UNF-2A, 0.875 L (AP)	96906	7903133-52 MS24693-C275	8	
			WASHER, FLAT, NO 10 (AP)	96906	4912548-13 MS15795-842	8	
			NUT, SELF-LOCKING, HEX 10-32UNF-3B (AP)	96906	4912794-00 MS21044-C3	8	
1	A1	2	CABINET ASSEMBLY, WIRED	90536	7059815-00	1	
1-4		3	CABLE EXTENDOR, CONTROL UNIT	90536	7059853-00	1	
1-5		3	CABLE EXTENDOR, POWER SUPPLY	90536	7059845-00	1	
1-6		3	CABLE EXTENDOR, TAPE TRANSPORT	90536	7059895-00	4	
1-7	A2	3	TOP HAT ASSEMBLY, 4 TAPE TRANSPORT (SEE FIG 6-2 FOR NLA)	90536	7059860-00	1	
1-8	A9	3	FAN ASSEMBLY (SEE FIG 6-3 FOR NLA)	90536	7059817-00	1	
1		3	SCREW, CAP, HEX HD, MACH 10-32NF-2A, 3/4 L (AP)		903654-06 COML	16	
			WASHER, FLAT, NO 10 (AP)		4912548-13	16	

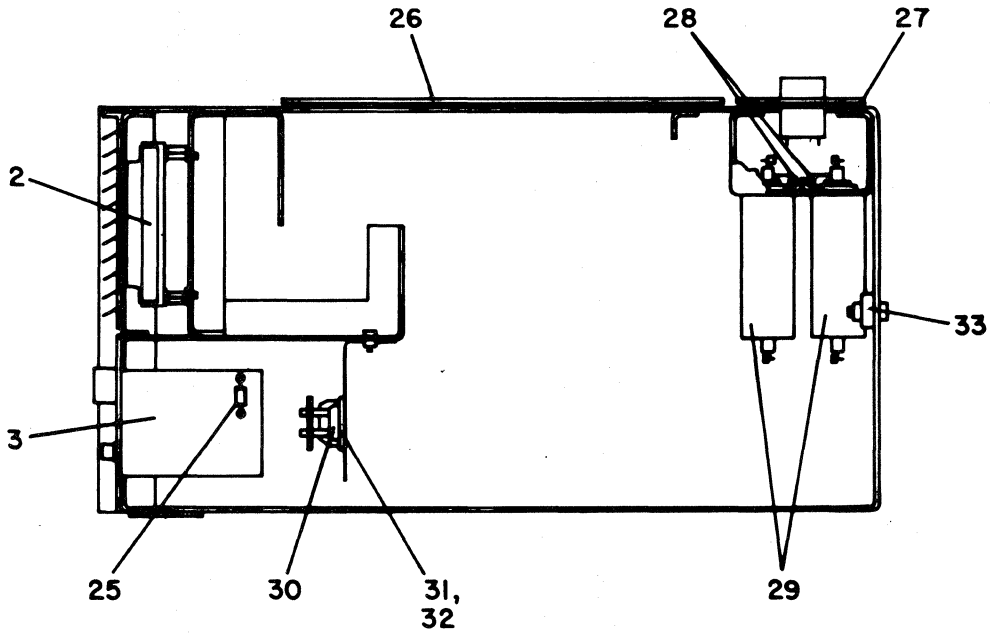
FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 1			RECORDER-REPRODUCER, DIGITAL		CONTINUED		
				96906	MS15795-842		
1-9	A10 A11 A12	3	TEMPERATURE SENSOR ASSEMBLY (SEE FIG 6-8 FOR NLA)	90536	7059802-00	3	
1		3	SCREW, MACH, PAN HD, 8-32UNC-2A 5/8 L (AP)		4912532-01	4	
				96906	MS51957-46		
			WASHER, FLAT, NO 8 (AP)		4912548-12	4	
				96906	MS15795-841		
			NUT, SELF-LOCKING, HEX 8-32UNC-3B (AP)		4912796-02	4	
				96906	MS21044-C08		
1-10	W1	3	CABLE ASSEMBLY, POWER (SEE FIG 6-9 FOR NLA)	90536	7059885-00	1	
1-11	W2	3	CABLE ASSEMBLY, POWER (SEE FIG 6-9 FOR NLA)	90536	7059885-01	1	
1-12	W3	3	CABLE ASSEMBLY, POWER (SEE FIG 6-9 FOR NLA)	90536	7059885-02	1	
1-13	W4	3	CABLE ASSEMBLY, POWER (SEE FIG 6-9 FOR NLA)	90536	7059885-03	1	
1-14	W5	3	CABLE ASSEMBLY, CONTROL UNIT POWER (SEE FIG 6-9 FOR NLA)	90536	7059893-00	1	
1-15	W6	3	CABLE ASSEMBLY, MAIN POWER (SEE FIG 6-9 FOR NLA)	90536	7059886-00	1	
1-16	W7	3	CABLE ASSEMBLY, I/O (SEE FIG 6-10 FOR NLA)	90536	7059887-00	1	
1-17	W8	3	CABLE ASSEMBLY, I/O (SEE FIG 6-10 FOR NLA)	90536	7059887-01	1	
1-18	W9	3	CABLE ASSEMBLY, I/O (SEE FIG 6-10 FOR NLA)	90536	7059888-00	1	
1-19	W10	3	CABLE ASSEMBLY (SEE FIG 6-11 FOR NLA)	90536	7059889-00	1	
1-20	W11	3	CABLE ASSEMBLY (SEE FIG 6-10 FOR NLA)	90536	7059890-00	1	
1-21	W12	3	CABLE ASSEMBLY, READ (SEE FIG 6-12 FOR NLA)	90536	7059880-00	1	
1-22	W13	3	CABLE ASSEMBLY, READ (SEE FIG 6-12 FOR NLA)	90536	7059880-01	1	
1-23	W14	3	CABLE ASSEMBLY, READ (SEE FIG 6-12 FOR NLA)	90536	7059880-02	1	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USE ON
6- 1			RECORDER-REPRODUCER, DIGITAL		CONTINUED		
1-24	W15	3	CABLE ASSEMBLY, READ (SEE FIG 6-12 FOR NLA)	90536	7059880-03	1	
1-25	W16	3	CABLE ASSEMBLY, WRITE (SEE FIG 6-13 FOR NLA)	90536	7059892-00	1	
1-26	W17	3	CABLE ASSEMBLY, TEMPERATURE SENSOR	90536	7059978-00	1	
1-27	W18	3	CABLE ASSEMBLY, TEMPERATURE SENSOR	90536	7059978-01	1	
1-28	W19	3	CABLE ASSEMBLY, TEMPERATURE SENSOR	90536	7059978-02	1	
1-29	W20	3	CABLE ASSEMBLY, SIGNAL AND CHASSIS GND	90536	7059979-00	1	
1-30	W21	3	CABLE ASSEMBLY, SIGNAL AND CHASSIS GND	90536	7059979-01	1	
1-31	W22	3	CABLE ASSEMBLY, SIGNAL AND CHASSIS GND	90536	7059979-02	1	
1-32	W23	3	CABLE ASSEMBLY, SIGNAL AND CHASSIS GND	90536	7059979-03	1	
1-33	W24	3	CABLE ASSEMBLY, SIGNAL AND CHASSIS GND	90536	7059979-04	1	
1-34	W25	3	CABLE ASSEMBLY, SIGNAL AND CHASSIS GND	90536	7059979-05	1	
1-35	W26	3	CABLE ASSEMBLY, SIGNAL AND CHASSIS GND	90536	7059979-06	1	
1-36	A3	2	CONTROL UNIT ASSEMBLY (SEE FIG 6-4 FOR NLA)	90536	7059900-00	1	
1-37	A4	2	POWER SUPPLY, 400HZ TO 75VDC (SEE PX 7984)	90536	7601768-01	1	ACI
			POWER SUPPLY, 400HZ TO 75VDC (SEE PX 7984)	90536	7601768-02	1	B
1-38	A5 THRU A8	2	TRANSPORT, MAG TAPE, 7 TRACK (SEE PX 7984)	90536	7059983-00	4	A
	A5 THRU A8		TRANSPORT, MAG TAPE, 9 TRACK (SEE PX 7984)	90536	7059983-01	4	BD
	A5 A6		TRANSPORT, MAG TAPE, 7 TRACK (SEE PX 7984)	90536	7059983-00	2	C
1		2	4 TRANSPORT 7 TRACK, PC CARD KIT	90536	7059850-00	1	AC
			4 TRANSPORT 9 TRACK, PC CARD KIT	90536	7059878-00	1	BD

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 1			RECORDER-REPRODUCER, DIGITAL		CONTINUED		
1	A20A	3	CIRCUIT CARD ASSEMBLY, AMPLIFIER WRITE ENABLE	90536	7091810-01	1	
1	A33A A34A	3	CIRCUIT CARD ASSEMBLY MULTIPLEXER, READ	90536	7091820-01	2	
1	A10A A11A	3	CIRCUIT CARD ASSEMBLY, TAPE TRANSPORT CONTROL	90536	7091850-01	2	
1	A17A	3	CIRCUIT CARD ASSEMBLY, AMPLIFIER DRIVER, WRITE	90536	7091805-01	1	BD
1	A29A A30A	3	CIRCUIT CARD ASSEMBLY, DETECTOR NRZI	90536	7091815-01	2	BD
1	A20B	3	CIRCUIT CARD ASSEMBLY	90536	7091890-01	1	BD
1		2	7 TRACK ROM, PC CARD KIT	90536	7059992-00	1	AC
			9 TRACK NRZ ROM, PC CARD KIT	90536	7059993-00	1	BD
1	A42B	3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY	90536	7092250-00	1	AC
1	A43B	3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY EXPANSION I	90536	7092240-00	1	AC
1	A42B	3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY	90536	7092250-01	1	BD
1	A43B	3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY EXPANSION I	90536	7092240-01	1	BD
1	A44B	3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY EXPANSION II	90536	7092245-00	1	BD



FRONT VIEW



RIGHT SIDE VIEW

FIGURE 6-2. 4 TAPE TOP HAT ASSEMBLY (A2)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 2	A2	3	TOP HAT ASSEMBLY, 4 TAPE TRANSPORT (SEE FIG 6-1 FOR NHA)	90536	7059860-00	REF	
2-1		4	GRILL, AIR INTAKE	90536	7059866-00	1	
2		4	SOCKET, PUSH BUTTON FASTENER (AP)	71286	7900612-00 15R1-1AC AND 15R10-1AC	8	
			STUD, PB, FASTENER (AP)	71286	7900611-00 15S11-1AC AND 15S1-1-1AC	8	
2-2		4	FILTER, AIR INTAKE, MODIFIED	90536	7059867-00	1	
2-3		4	OPERATOR PANEL ASSEMBLY	90536	7059810-00	1	
2		4	SCREW, SPECIAL FINISH (AP)	90536	7059865-00	34	
2-4	CB1	5	CIRCUIT BREAKER, MAGNETIC, 3 POLES, 20.0A, 240V, 400HZ	81349	7903070-47 M39019-5-80	1	
2-5	DS1 DS2 DS3 DS13 DS14 DS15 DS25 DS26 DS27 DS37 DS38 DS39	5	LAMP, INCANDESCENT, 28VDC 40 MILLIAMPERS	96906	7902253-00 MS18209-387	12	
2-6	DS4 DS16 DS28 DS40	5	LAMP, INCANDESENT, 5.0V, .06A TYPE 7333	71744	7904348-00 CM7333	4	
2-7	DS49 DS50	5	LAMP, GLOW NEON, FLANGED BASE NE-2D	96906	909902-00 MS25252-C7A	2	
2-8	M1	5	METER, TIME TOTALIZING, 400HZ 0 TO 9999.9 HOURS	96906	7900499-00 MS17325-1	1	
2-9	MP1 MP3 MP13 MP15 MP25 MP27 MP37 MP39	5	LENS, INDICATOR LIGHT TRANSPARENT WHITE	07137	7904335-09 221059-32	8	
2-10	MP2 MP14	5	LENS, INDICATOR LIGHT TRANSPARENT GREEN	07137	7903193-13 221710-33	4	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 2			TOP HAT ASSEMBLY, 4 TAPE		CONTINUED		
	MP26 MP38						
2-11	MP4 MP16 MP28 MP40 MP50	5	LENS, INDICATOR LIGHT TRANSPARENT AMBER	07137	7903193-11 221710-28	5	
2-12	MP49	5	LENS, INDICATOR LIGHT TRANSPARENT RED	07137	7903193-10 221710-28	1	
2-13	S1 S5 S9 S13	5	SWITCH, ROTARY, NON-SHORTING 2 DECK, 2 POSITION	96906	7900003-09 MS16109-36-2-2N	4	
2-14	S2 S6 S10 S14	5	SWITCH, ROTARY, 1 DECK, 16 POSITIONS	91812	7900362-14 3-1900-1B16C	4	
2-15	S3 S4 S7 S8 S11 S12 S15 S16	5	SWITCH, PUSH, SUBMINITURE, SPST N/O, MOMENTARY	07137	7903825-04 SBS-A9	8	
2-16	S17	5	SWITCH, ROTARY, NON-SHORTING 1 DECK, 5 POSITION	96906	7900003-03 MS16109-36-1-5N	1	
2-17	S18 S19	5	SWITCH, TOGGLE, DPDT	91929	7900925-00 23AT402-T2	2	
2-18	XDS1 XDS3 XDS13 XDS15 XDS25 XDS27 XDS37 XDS39	5	SWITCH, PUSH, INDICATOR TYPE LESS LAMP AND LENS, TSTRZ	07137	7904320-00 MT1B-8743A	8	
2-19	XDS2 XDS14 XDS26 XDS38	5	LIGHT, INDICATOR, INCANDESCENT TSTRZ, LESS LENS	07137	7904321-00 MT1B-8742A	4	
2-20	XDS4 XDS16 XDS28	5	LIGHT, INDICATOR, W/O LAMP AND LENS	07137	7904322-00 DLR-8746A	4	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6- 2			TOP HAT ASSEMBLY, 4 TAPE		CONTINUED		
	XDS40						
2-21	XDS5 XDS6 XDS8 THRU XDS12 XDS17 XDS18 XDS20 THRU XDS24 XDS29 XDS30 XDS32 THRU XDS36 XDS41 XDS42 XDS44 THRU XDS48	5	SWITCH, INDICATOR, SPST, N/O MOMENTARY, LIGHT EMITTING DIODE	07137	7903823-00 SSBLB05AL07	28	
2-22	XDS49	5	LIGHT, INDICATOR, W/O LAMP AND LENS	07137	7904322-02 DLR-8744A	1	
2-23	XDS50	5	LIGHT, INDICATOR, W/O LAMP AND LENS	07137	7904322-01 DRL-8745A	1	
2-24		5	KNOB, CONTROL, POINTER, W/O SKIRT, SIZE 7, BLACK	96906	912070-02 MS91528-1P2B	9	
2		5	DIODE ASSEMBLY	90536	7059811-00	4	
2-25		6	SEMICONDUCTOR DEVICE, DIODE, SI SWITCHING, 500MW, 75V	03508	7901009-00 DJX499	3	
2-26		4	COVER, TOP HAT	90536	7059862-00	1	
2-27		4	INPUT/OUTPUT PANEL	90536	7059864-00	1	
2		4	SCREW, MACH, PAN HD, 10-32UNC-2A 3/4 L (AP) WASHER, FLAT, NO 10 (AP)	96906 96906	4912534-02 MS51958-65 4912548-13 MS15795-842	54 54	
2-28	R1 THRU R4	4	RESISTOR, FXD, FILM, 2W, +-2PCT 100K OHM	81349	7900182-96 RL42S104G	4	
2-29	FL1 THRU FL4	4	FILTER, RF, 400VDC, 20A	56289	7900608-00 20JX31	4	
2-30	TB1	4	TERMINAL BOARD, BARRIER TYPE SECTION TYPE TERMINALS	75382	900126-12 602-12	1	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 2			TOP HAT ASSEMBLY, 4 TAPE		CONTINUED		
2-31		4	INSULATOR, TERMINAL BOARD	90536	7059806-00	1	
2-32		4	INSULATOR, TERMINAL BOARD	90536	7059806-01	1	
2		4	SCREW, MACH, PAN HD, 8-32UNC-2A		7903132-31	4	
			0.375 L (AP)	96906	MS51957-43		
			WASHER, LOCK, HEL, NO 8 (AP)		4912550-02	4	
				96906	MS35338-137		
			WASHER, FLAT, NO 8 (AP)		4912548-12	8	
				96906	MS15795-841		
			STUD, EXTENSION (AP)	90536	7059820-01	4	
2-33	W1 W2	4	BUS BAR	90536	7059808-00	2	
2-34	E2	4	CONNECTOR, RCPT, ELEC, MALE		905418-05	1	
			7 CONTACT	96906	MS3102R20-15PW		
2-35	J1	4	CONNECTOR, RCPT, ELEC, MALE		905418-04	1	
			7 CONTACT	96906	MS3102R20-15P		
2		4	SCREW, MACH, PAN HD, 4-40UNC-2A		908552-07	8	
			1/2 L (AP)	96906	MS51957-17		
			WASHER, FLAT, NO 4 (AP)		4912548-10	16	
				96906	MS15795-804		
			NUT, SELF LOCKING, HEX		4912796-00	8	
			4-40UNC-3B (AP)	96906	MS21044-C04		

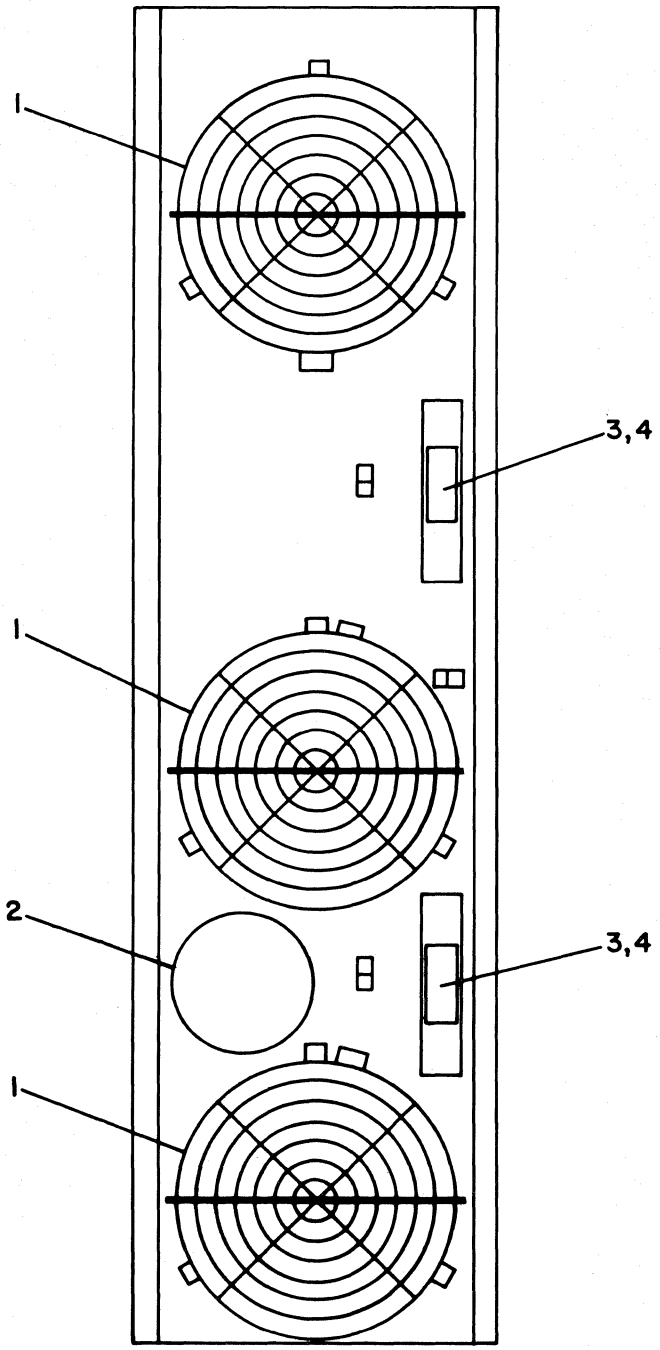
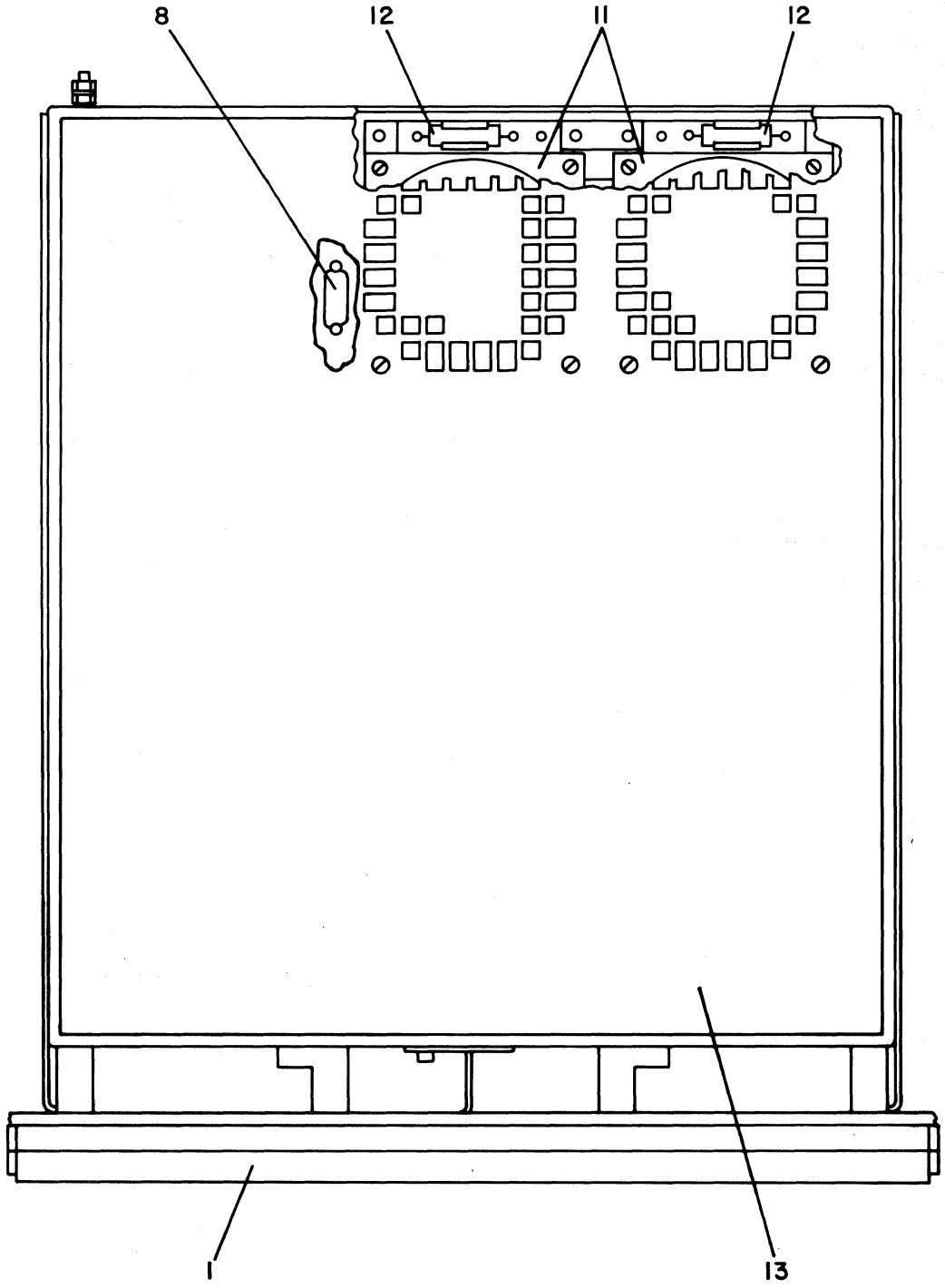


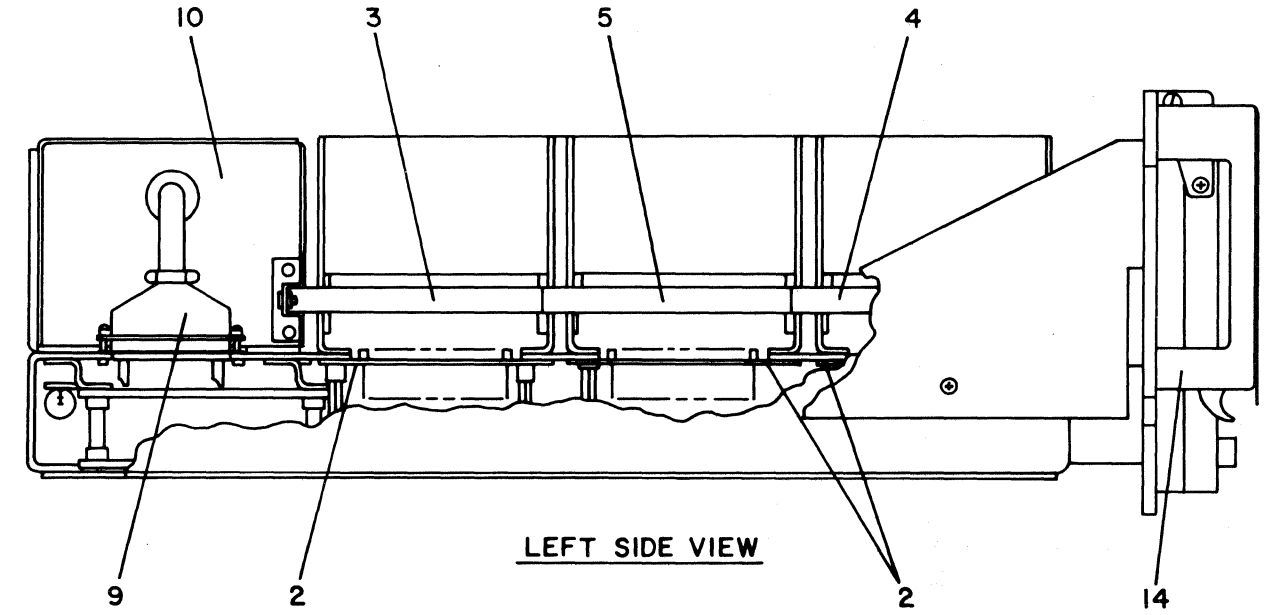
FIGURE 6-3. FAN ASSEMBLY (A9)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USE ON
6- 3	A9	3	FAN ASSEMBLY (SEE FIG 6-1 FOR NHA)	90536	7059817-00	REF	
3-1	B1 B2 B3	4	FAN, TUBEAXIAL, 400HZ, 115VAC 3 PHASE	82877	906905-06 656JS AND 14559	3	
3		4	SCREW, MACH, PAN HD, 4-40UNC-2A 5/8 L (AP)	96906	908552-09 MS51957-18	9	
			WASHER, FLAT, NO 4 (AP)	96906	4912548-10 MS15795-804	9	
			BLOCK, FAN RETAINING (AP)	90536	254828-00	9	
3-2	LS1	4	HORN, ELEC, 400HZ, 120VAC 250 MA MAX	80252	909862-01 434M1-120V400HZ	1	
3		4	SCREW, MACH, PAN HD, 6-32UNC-2A 7/16 L (AP)	96906	4912531-03 MS51957-29	3	
			WASHER, FLAT, NO 6 (AP)	96906	4912548-11 MS15795-806	3	
3-3	TB1 TB2	4	TERMINAL BOARD, BARRIER TYPE	81349	910161-04 8TB10	2	
3-4		4	COVER, TERMINAL BOARD	90536	7059819-00	2	
3		4	SCREW, MACH, PAN HD, 8-32UNC-2A 0.438 L (AP)	96906	7903132-32 MS51957-44	4	
			WASHER, LOCK, HEL, NO 8 (AP)	96906	4912550-02 MS35338-137	4	
			WASHER, FLAT, NO 8 (AP)	96906	4912548-12 MS15795-841	8	
			STUD, EXTENSION (AP)	90536	7059820-00	4	

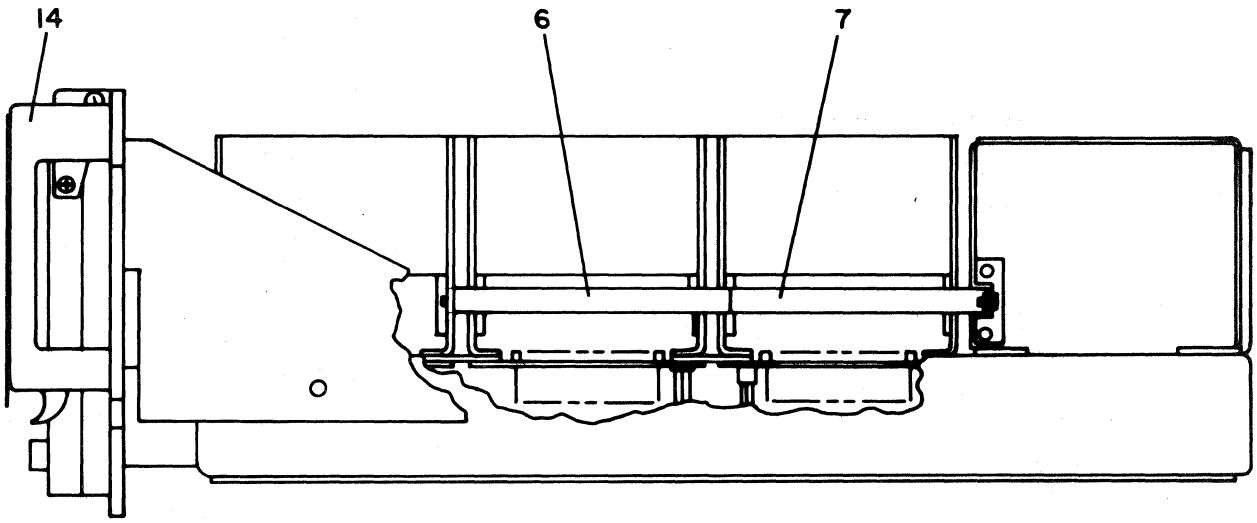


BOTTOM VIEW

FIGURE 6-4. CONTROL UNIT ASSEMBLY (A3) (1 OF 2)



LEFT SIDE VIEW



RIGHT SIDE VIEW

FIGURE 6-4. CONTROL UNIT ASSEMBLY (A3) (2 OF 2)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6- 4	A3	2	CONTROL UNIT ASSEMBLY (SEE FIG 6-1 FOR NHA)	90536	7059900-00	REF	
4		3	CIRCUIT CARD PLACEMENT CHART (SEE FIG 6-5 FOR NLA)	90536	7059907-00	1	
4-1	A3A1	3	PANEL ASSEMBLY, CONTROLLER (SEE FIG 6-6 FOR NLA)	90536	7059910-00	1	
4		3	SCREW, MACH, PAN HD, 8-32UNC-2A 3/4 L (AP)	96906	4912532-02 MS51957-47	5	
			SCREW, MACH, FLAT HD, 8-32UNC-2A 0.75 L (AP)	96906	7903133-35 MS24693-C52	4	
			WASHER, FLAT, NO 8 (AP)	96906	4912548-02 MS15795-807	AR	
			NUT, SELF LOCKING, HEX 8-32UNC-3B (AP)	96906	4912796-02 MS21044-C08	AR	
			STUD, EXTENSION (AP)	90536	7059932-00	3	
			SCREW, MACH, FLAT HD 1/4-28UNF-2A, 0.500 L (AP)	96906	7903133-68 MS24693-C294	6	
4-2	A3A2	3	CONNECTOR PLATE ASSEMBLY	90536	7059912-00	1	
4		3	SPACER (AP)	90536	7059919-00	2	
			SCREW, CAP, SOCKET HD 1/4-28UNF-3A, .500 L (AP)	96906	911607-00 MS16996-21	8	
			WASHER, FLAT, SIZE 1/4 (AP)	96906	4912548-04 MS15795-810	8	
4-3	W1	3	BUS BAR, CONNECTION TAB 5V	90536	7059963-00	1	
4-4	W1-1 W2-1	3	BUS BAR, JUMPER	90536	7059967-00	2	
4-5	W1-2	3	BUS BAR, JUMPER	90536	7118224-00	1	
4-6	W2	3	BUS BAR, JUMPER	90536	7059967-01	1	
4-7	W2-2	3	BUS BAR, CONNECTION GROUND	90536	7059966-00	1	
4		3	SCREW, MACH, PAN HD, 6-32UNC-2A 5/16 L (AP)	96906	4912531-01 MS51957-27	AR	
			WASHER, LOCK, I/T, NO 6 (AP)		4912552-01 COML	AR	
			NUT, PLAIN, HEX, MACH 6-32UNC-2B (AP)		4912544-01 COML	AR	
4-8	J7	3	CONNECTOR, PLUG, ELEC, 5 CONTACT	71468	7902651-00 DAM-7W2P	1	
4		3	CONTACT, ELEC, MALE (AP)	71468	7902559-02 D0110551	AR	
4-9	J8	3	CONNECTOR, RCPT, ELEC, FEMALE 3-37 CONTACT	71468	7902558-05 DCM-27W2S	1	
4		3	CONTACT, ELEC, FEMALE (AP)	71468	7902560-02 DM53744-7	AR	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6- 4			CONTROL UNIT ASSEMBLY		CONTINUED		
			JACKSCREW ASSY, CONN, MALE AND FEMALE (AP)	71468	7904208-01 D0110551	4	
			WASHER, FLAT, NO 4 (AP)	96906	4912548-00 MS15795-803	4	
			NUT, SELF LOCKING, HEX 4-40UNC-3B (AP)	96906	4912796-00 MS21044-C04	4	
4-10	A3A3	3	POWER SUPPLY, DC CONVERTER (SEE FIG 6-7 FOR NLA)	90536	7059925-00	1	
4		3	SCREW, MACH, PAN HD, 10-32UNF-2A 5/8 L (AP)	96906	4912534-01 MS51958-64	4	
			WASHER, FLAT, NO 10 (AP)	96906	4912548-03 MS15795-808	4	
4-11	B1 B2	3	FAN, TUBEAXIAL, 115VAC, 400HZ 1 PHASE, 123 AND 190 CFM	92702	7904171-00 BC2206F-0-1	2	
4		3	SCREW, MACH, PAN HD, SLOTTED 6-32UNC-2A, 1.75 L (AP)		4912524-13 COML	8	
			WASHER, LOCK, HEL, NO 6 (AP)	96906	4912550-01 MS35338-136	8	
			WASHER, FLAT, NO 6 (AP)	96906	4912548-01 MS15795-805	8	
			SPACER, MOUNT (AP)	90536	259327-00	8	
4-12	C1 C2	3	CAPACITOR, PAPER, DIELECTRIC 600V, 0.22UF, +-10PCT	81349	7900838-19 CH09A1NF224K	2	
4-13		3	COVER, ACCESS, CHASSIS	90536	7059902-00	1	
4-14		3	LATCH SET, RIM, CHASSIS HANDLE	71286	7901084-01 72L2-1-1AB	2	
4		3	SCREW, MACH, FLAT HD 10-32UNF-2A, 0.500 L (AP)	96906	7903133-49 MS24693-C272	4	

A4		A3		A2
41 (-3V)	1	26	1	
41 (-3V)	2	26	2	
41 (-3V)	3	26	3	
41 (-3V)	4	27	4	
41 (-3V)	5	5	5	
41 (-3V)	6	28	6	
42 (-3V)	7	10	7	
9	8	24	8	
9	9	18	9	
9 (4 TRANSPORTS)	10	13	10	
9 (4 TRANSPORTS)	11	13	11	
11	12	13	12	
1	13	15	13	
1	14	21	14	
1	15	8	15	
1	16	19	16	
1	17	19	17	
2	18	23	18	
	19	29	19	
2 (4 TRANSPORTS)	20	44 (9 TRACK)	20	
	21	16	21	
3	22	14	22	
3	23	20	23	
3	24	39	24	
3	25	22	25	
3	26	40	26	48 (1600 BPI)
3	27	17	27	
3	28	17	28	49 (1600 BPI)
3 (9 TRACK)	29	30	29	
3 (9 TRACK)	30	30	30	50 (1600 BPI)
4	31	30	31	51 (1600 BPI)
4	32	30	32	52 (1600 BPI)
4 (4 TRANSPORTS)	33	31	33	53 (1600 BPI)
4 (4 TRANSPORTS)	34	35	34	54 (1600 BPI)
7	35	37	35	54 (1600 BPI)
43 (1600 BPI)	36	32	36	55 (1600 BPI)
43 (1600 BPI)	37	32	37	55 (1600 BPI)
43 (1600 BPI)	38	32	38	55 (1600 BPI)
43 (1600 BPI)	39	33	39	55 (1600 BPI)
43 (1600 BPI)	40	34	40	55 (1600 BPI)
43 (1600 BPI)	41	36	41	55 (1600 BPI)
43 (1600 BPI)	42	45 (7 & 9 TRACK)	42	55 (1600 BPI)
43 (1600 BPI)	43	46 (7 & 9 TRACK)	43	55 (1600 BPI)
43 (1600 BPI)	44	47 (9 TRACK)	44	55 (1600 BPI)
	45	47 (1600 BPI)	45	56 (1600 BPI)
	46	47 (1600 BPI)	46	
	47	47 (1600 BPI)	47	
	48	47 (1600 BPI)	48	
	49	47 (1600 BPI)	49	
	50	38	50	
	51	6	51	
12	52	25	52	

FIGURE 6-5. CIRCUIT CARD PLACEMENT CHART

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 5		3	CIRCUIT CARD PLACEMENT CHART (SEE FIG 6-4 FOR NHA)	90536	7059907-00	REF	
5-1		3	CIRCUIT CARD ASSEMBLY, AMPLIFIER DRIVER, WRITE	90536	7091805-01	5	
5-2		3	CIRCUIT CARD ASSEMBLY, AMPLIFIER WRITE ENABLE	90536	7091810-01	2	
5-3		3	CIRCUIT CARD ASSEMBLY, DETECTOR NRZI	90536	7091815-01	9	
5-4		3	CIRCUIT CARD ASSEMBLY MULTIPLEXER, READ	90536	7091820-01	4	
5-5		3	CIRCUIT CARD ASSEMBLY, I/O CONTROL	90536	7091830-01	1	
5-6		3	CIRCUIT CARD ASSEMBLY, WRITE TIMING	90536	7091835-01	1	
5-7		3	CIRCUIT CARD ASSEMBLY, REGISTER NRZI READ	90536	7091840-01	1	
5-8		3	CIRCUIT CARD ASSEMBLY, REGISTER WRITE	90536	7091845-01	1	
5-9		3	CIRCUIT CARD ASSEMBLY, TAPE TRANSPORT CONTROL	90536	7091850-01	4	
5-10		3	CIRCUIT CARD ASSEMBLY, TAPE TRANSPORT STATUS LINES	90536	7091855-01	1	
5-11		3	CIRCUIT CARD ASSEMBLY, ADDRESS SWITCH DECODE & SELECT TIMING	90536	7091860-01	1	
5-12		3	CIRCUIT CARD ASSEMBLY START/STOP CONTROL	90536	7091865-01	1	
5-13		3	CIRCUIT CARD ASSEMBLY, GENERATOR PULSE	90536	7091870-01	3	
5-14		3	CIRCUIT CARD ASSEMBLY, PROGRAM FLAGS, BIT TEST	90536	7091875-01	1	
5-15		3	CIRCUIT CARD ASSEMBLY, BAR, OBR CONTROL	90536	7091880-01	1	
5-16		3	CIRCUIT CARD ASSEMBLY, FORMAT CONVERTER, 7 TRACK	90536	7091885-01	1	
5-17		3	CIRCUIT CARD ASSEMBLY, SOURCE BUS SEL AND MON CLOCK	90536	7091895-01	2	
5-18		3	CIRCUIT CARD ASSEMBLY, REGISTER OUTPUT BYTE	90536	7092400-01	1	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 5			CIRCUIT CARD PLACEMENT CHART		CONTINUED		
5-19		3	CIRCUIT CARD ASSEMBLY, REGISTER INPUT BYTE	90536	7092405-01	2	
5-20		3	CIRCUIT CARD ASSEMBLY, EXTENDED BIT TEST	90536	7092410-01	1	
5-21		3	CIRCUIT CARD ASSEMBLY, WRITE AND READ REGISTERS	90536	7092415-01	1	
5-22		3	CIRCUIT CARD ASSEMBLY, SOURCE BUS 8-15 AND DEST DECODE	90536	7092420-01	1	
5-23		3	CIRCUIT CARD ASSEMBLY, WS CONTROL	90536	7092425-01	1	
5-24		3	CIRCUIT CARD ASSEMBLY, OFF LINE TEST	90536	7092450-01	1	
5-25		3	CIRCUIT CARD ASSEMBLY OSCILLATOR, 6.144 MHZ	90536	7092455-01	1	
5-26		3	CIRCUIT CARD ASSEMBLY, I/O REGISTER NO 1	90536	7092435-01	3	
5-27		3	CIRCUIT CARD ASSEMBLY, I/O REGISTER NO 2	90536	7092440-01	1	
5-28		3	CIRCUIT CARD ASSEMBLY, DUPLEX CONTROL	90536	7092445-01	1	
5-29		3	CIRCUIT CARD ASSEMBLY, MEMORY RAM, 256 X 8	90536	7091500-01	1	
5-30		3	CIRCUIT CARD ASSEMBLY ARITHMETIC LOGIC UNIT	90536	7092175-01	4	
5-31		3	CIRCUIT CARD ASSEMBLY ARITHMETIC LOGIC CONTROL UNIT	90536	7092180-00	1	
5-32		3	CIRCUIT CARD ASSEMBLY, MICRO REGISTER	90536	7092185-01	3	
5-33		3	CIRCUIT CARD ASSEMBLY, MICRO CONTROL	90536	7092190-00	1	
5-34		3	CIRCUIT CARD ASSEMBLY, BRANCH CONTROL	90536	7092195-01	1	
5-35		3	CIRCUIT CARD ASSEMBLY, CLOCK	90536	7092030-01	1	
5-36		3	CIRCUIT CARD ASSEMBLY, REPEAT CLOCK CONTROL	90536	7092200-01	1	
5-37		3	CIRCUIT CARD ASSEMBLY, SOURCE AND DEST TRANS	90536	7092205-01	1	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 5			CIRCUIT CARD PLACEMENT CHART		CONTINUED		
5-38		3	CIRCUIT CARD ASSEMBLY MAINTENANCE CONTROL	90536	7092430-01	1	
5-39		3	CIRCUIT CARD ASSEMBLY INTERRUPT CONTROL	90536	7092000-01	1	
5-40		3	CIRCUIT CARD ASSEMBLY, TRACK SCRAMBLER	90536	7092165-01	1	
5-41		3	CIRCUIT CARD ASSEMBLY, DATA INTERFACE, -3 VOLT	90536	7091775-01	6	
5-42		3	CIRCUIT CARD ASSEMBLY, CONTROL INTERFACE, -3 VOLT	90536	7091785-01	1	
5-43		3	CIRCUIT CARD ASSEMBLY, DETECTOR PHASE ENCODER	90536	7092460-01	9	
5-44		3	CIRCUIT CARD ASSEMBLY, CRC REGISTER	90536	7091890-01	1	
5-45		3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY EXPANSION III	90536	7092250-00/01	1	
5-46		3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY EXPANSION I	90536	7092240-00/01	1	
5-47		3	CIRCUIT CARD ASSEMBLY, MICRO MEMORY EXPANSION II	90536	7092245-00	6	
5-48		3	CIRCUIT CARD ASSEMBLY, CONTROL WRITE CURRENT STEP	90536	7092255-01	1	
5-49		3	CIRCUIT CARD ASSEMBLY, GENERATOR PULSE	90536	7091870-01	1	
5-50		3	CIRCUIT CARD ASSEMBLY, CHARACTOR TIMING	90536	7092495-01	1	
5-51		3	CIRCUIT CARD ASSEMBLY, CHARACTOR DESKEN AND BIN OF	90536	7092485-01	1	
5-52		3	CIRCUIT CARD ASSEMBLY, DATA TOGGLES	90536	7092480-01	1	
5-53		3	CIRCUIT CARD ASSEMBLY, DEAD TRACK AND DATA ENABLE REGISTER	90536	7092490-01	1	
5-54		3	CIRCUIT CARD ASSEMBLY, DATA BINS	90536	7092475-01	2	
5-55		3	CIRCUIT CARD ASSEMBLY, DECODER PHASE DATA	90536	7092465-01	9	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 5			CIRCUIT CARD PLACEMENT CHART		CONTINUED		
5-56		3	CIRCUIT CARD ASSEMBLY, BLOCK DETECTOR AND SYNC CONTROL	90536	7092470-01	1	

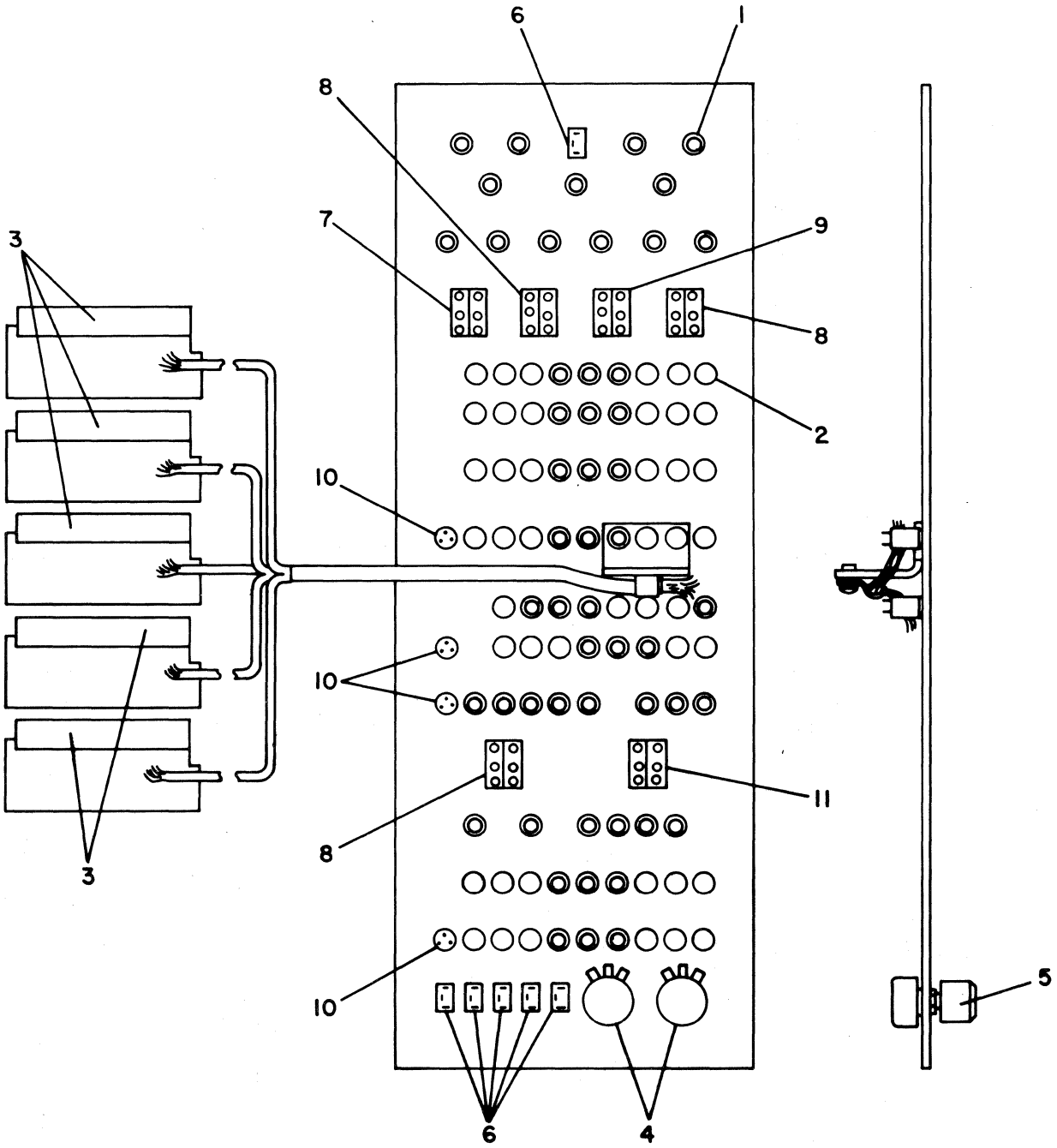


FIGURE 6-6. CONTROLLER PANEL ASSEMBLY (A1)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 6	A1	3	PANEL ASSEMBLY, CONTROLLER (SEE FIG 6-4 FOR NHA)	90536	7059910-00	REF	
6-1	DS01 THRU DS13 DS17 DS18 DS19 DS26 DS27 DS28 DS35 DS36 DS37 DS44 DS45 DS46 DS51 DS52 DS53 DS57 DS61 DS62 DS63 DS66 THRU DS79 DS83 DS84 DS85 DS92 DS93 DS94	4	SWITCH, INDICATOR, SPST, N/O MOMENTARY, LIGHT EMITTING DIODE	07137	7903823-00 SSBLB05AL07	52	
6-2	DS14 DS15 DS16 DS20 THRU DS25 DS29 THRU DS34 DS38 THRU DS43 DS47 THRU DS50 DS54 DS55 DS56 DS58 DS59 DS60	4	SWITCH, INDICATOR, SPST, N/O MOMENTARY, LIGHT EMITTING DIODE	07137	7903823-03 SSBLB05CL07	45	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6- 6			PANEL ASSEMBLY, CONTROLLER		CONTINUED		
	DS64 DS65 DS80 DS81 DS82 DS86 THRU DS91 DS95 DS96 DS97						
6-3	P1 THRU P5	4	CONNECTOR PLUG, ELEC, 60 CONTACT	90536	7096411-00	5	
6-4	R01 R02	4	RESISTOR, VARIABLE, COMP, 1W 1.0MEG OHM, +-10PCT	81349	7903140-24 RV2NAYSD105A	2	
6-5		4	KNOB, CONTROL, ROUND, W/O SKIRT SIZE 7	96906	912052-02 MS91528-1N2B	2	
6-6	S01 S13 THRU S17	4	SWITCH, TOGGLE, SUBMINIATURE 1 POLE, 2-3 POSITION	96906	7903797-02 MS75028-23	6	
6-7	S02	4	SWITCH, TOGGLE, DPDT	91929	7900925-01 23AT403T2	1	
6-8	S03 S05 S09	4	SWITCH, TOGGLE, 2 POLE 3 POSITION	91929	7900635-01 13AT418T2	3	
6-9	S04	4	SWITCH, TOGGLE, 2 POLE 3 POSITION	91929	7900635-00 13AT417T2	1	
6-10	S06 S07 S08 S12	4	SWITCH, PUSH, SUBMINITURE SPST, N/O, MOMENTARY	07137	7903825-04 SBS-A9	4	
6-11	S10	4	SWITCH, TOGGLE, DPDT	91929	7900925-00 23AT402T2	1	

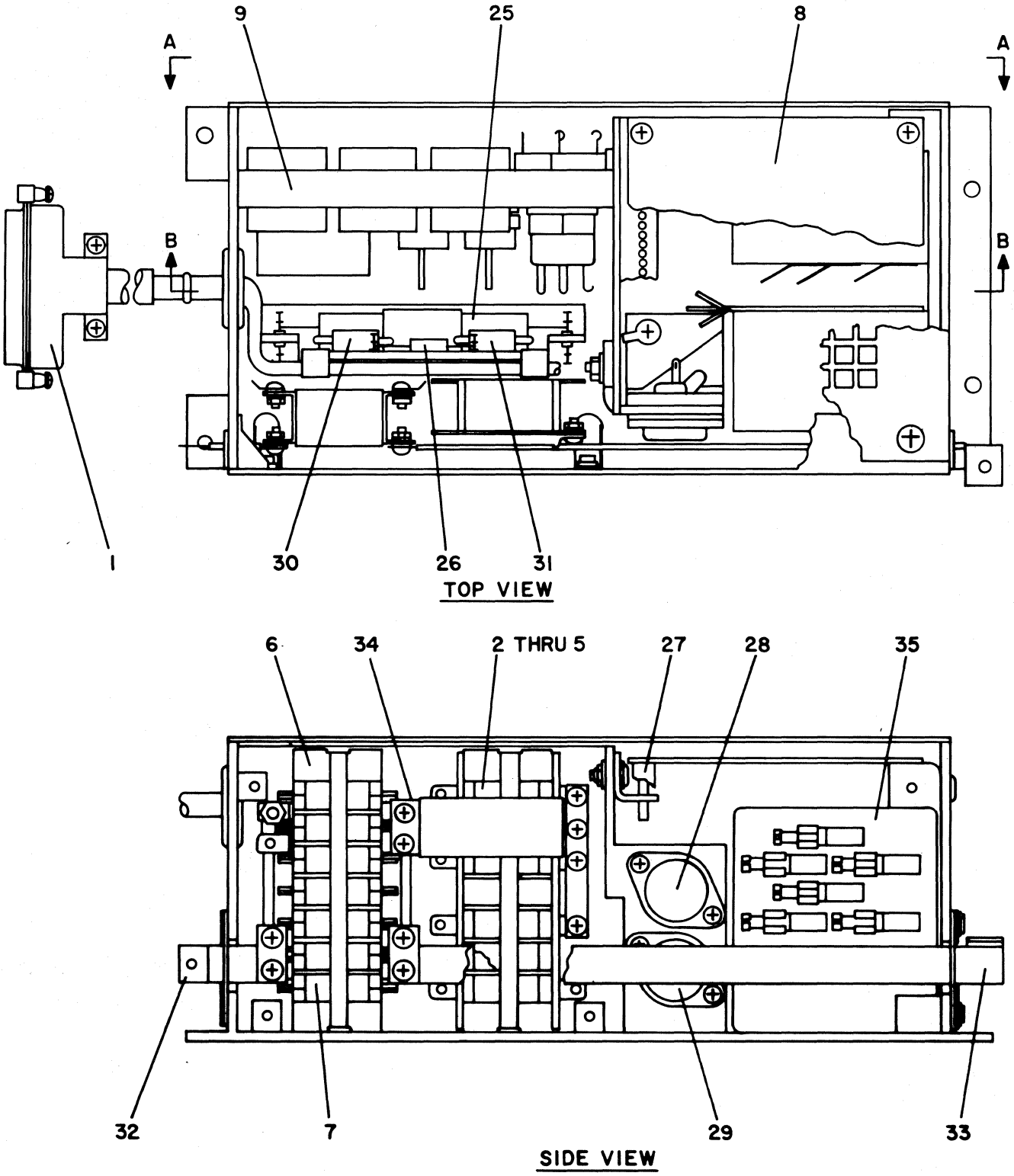
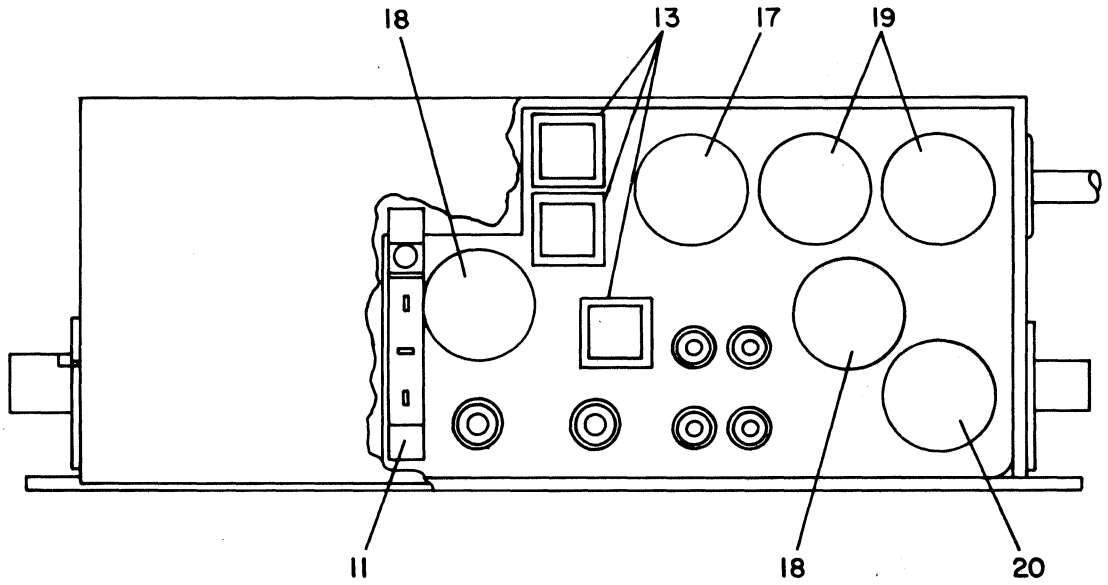
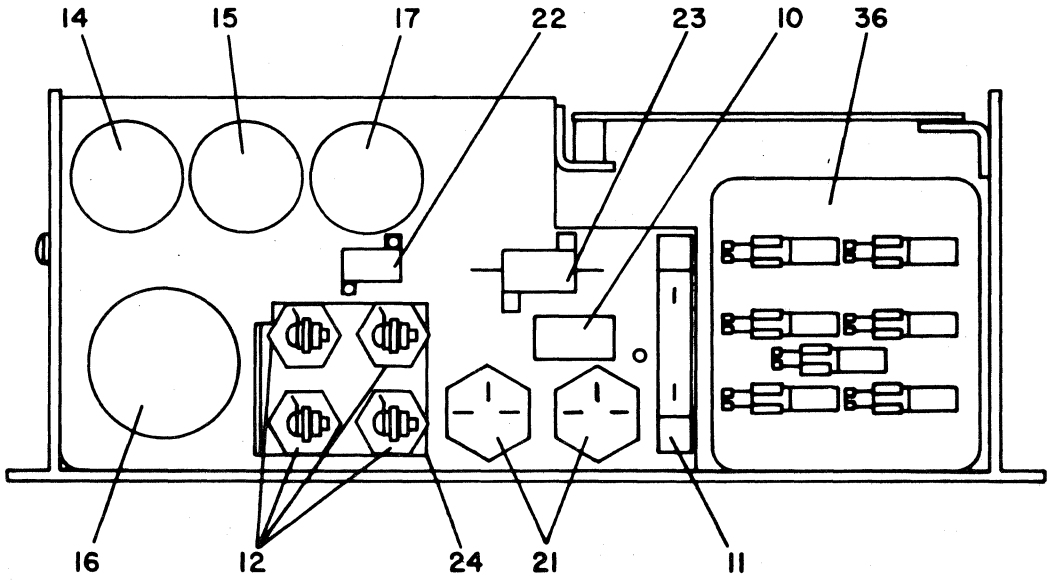


FIGURE 6-7. DC CONVERTER POWER SUPPLY (A3) (1 OF 2)



VIEW A-A



VIEW B-B

FIGURE 6-7. DC CONVERTER POWER SUPPLY (A3) (2 OF 2)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6- 7	A3	3	POWER SUPPLY, DC CONVERTER (SEE FIG 6-4 FOR NHA)	90536	7059925-00	REF	
7-1		4	CONNECTOR, PLUG, ELEC, MALE 3-13 CONTACT	71468	7902651-05 TO BE ESTAB	1	
7		5	CONTACT, ELEC, MALE (AP)	71468	7902559-02 DM53745-8	AR	
7	A1	4	CAPACITOR ASSEMBLY	90536	7059956-00	1	
7-2	C1 C2 C6 THRU C9 C14	5	CAPACITOR, FXD, ELCT, 35V 47UF, +-10PCT	81349	7902696-48 M39003-01-2312	7	
7-3	C3 C10	5	CAPACITOR, FXD, ELCT, 20V 100UF, +-10PCT	81349	7902696-41 M39003-01-2301	2	
7-4	C5 C12	5	CAPACITOR, FXD, ELCT, 10V 220UF, +-10PCT	81349	7902696-17 M39003-01-2265	2	
7-5	C13	5	CAPACITOR, FXD, CERAMIC, 100V 0.10UF, +-10PCT	81349	7903309-91 CK15BX104K	1	
7-6	A2	4	CAPACITOR ASSEMBLY, +5V	90536	7059955-00	1	
7-7	C1 THRU C14	5	CAPACITOR, FXD, ELCT, 10V 220UF, +-10PCT	81349	7902696-17 M39003-01-2265	14	
7-8	A3	4	CIRCUIT CARD ASSEMBLY CONTROLLER CONVERTER (SEE FIG 6-14 FOR NLA)	90536	7059941-01	1	
7		4	SCREW, MACH, PAN HD, 6-32UNC-2A 5/16 L (AP)	96906	4912531-01 MS51957-27	2	
			SCREW, MACH, PAN HD, 6-32UNC-2A 3/4 L (AP)	96906	4912531-06 MS51957-32	2	
			WASHER, FLAT, NO 6 (AP)	96906	4912548-01 MS15795-805	4	
7-9	A4	4	CHOKE PLATE ASSEMBLY	90536	7059957-00	1	
7-10	C1	5	CAPACITOR, FXD, GL, DIELECTRIC 300V, 5100PF, +-10PCT	07115	4912284-16 CY20C512K	1	
7-11	CR1 CR9	5	RECTIFIER, SIMICONDUCTOR DEVICE DOUBLER AND CT ASSEMBLIES	12969	7903528-00 655-082-1	2	
7-12	CR2 THRU CR5	5	SEMICONDUCTOR DEVICE, DIODE, SI MEDIUM PWR, 30A, 50V	56289	7901637-05 11D177-C3100R1	4	
7-13	CR6 CR7	5	RECTIFIER, SEMICONDUCTOR, SI 10 BRIDGE, 10A, FAST RECOVERY	12969	7903582-00 655-080-1	3	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6- 7			POWER SUPPLY, DC CONVERTER		CONTINUED		
	CR8						
7-14	L1	5	CHOKE	90536	7059959-00	1	
7-15	L2	5	CHOKE	90536	7059959-01	1	
7-16	L3	5	CHOKE	90536	7059958-00	1	
7-17	L4 L5	5	CHOKE	90536	7059959-02	2	
7-18	L6 L7	5	CHOKE	90536	7059959-03	2	
7-19	L8 L9	5	CHOKE	90536	7059959-04	2	
7-20	L10	5	CHOKE	90536	7059959-05	1	
7-21	Q1 Q2	5	TRANSISTOR, NPN, SI, HIGH PWR 100W, 300V	21845	7901448-01 SDT8821	2	
7-22	R1	5	RESISTOR, FXD, WW, 5W, 182 OHM +-1PCT	81349	7901859-57 RE60G1820	1	
7-23	R2	5	RESISTOR, FXD, WW, 10W, .100 OHM +-1PCT	81349	7902323-96 RE65GR100	1	
7-24	W1	5	BUS, TERMINAL	90536	7511230-00		
7-25	C1 C2	4	CAPACITOR, FXD, ELCT, 150V 120UF, -15 +30PCT	56289	7901635-13 112D127-C3150Y1	2	
7-26	CR1	4	SEMICONDUCTOR DEVICE, DIODE 300MW, 1A, 200V	81349	7902067-00 1N3611	1	
7-27	J1	4	BRACKET, CONN, 20 PIN	90536	7059950-00	1	
7-28	Q1	4	TRANSISTOR, NPN, SI, DARLINGTON POWER, 100V	04713	7904256-00 MJ4035	1	
7-29	Q2	4	INTEGRATED CIRCUIT, VOLTAGE REGULATOR	18324	7904270-01 LM309K	1	
7-30	R1	4	RESISTOR, FXD, WW, 5W, 150 OHM +-1PCT	81349	7901859-54 RE60G1500	1	
7-31	R2	4	RESISTOR, FXD, WW, 5W, 392 OHM +-1PCT	81349	7901859-67 RE60G3920	1	
7-32	W1	4	BUS BAR, CONNECTOR TAB, 5V	90536	7059964-00	1	
7-33	W2	4	BUS BAR, GROUND	90536	7059965-00	1	
7-34	W3	4	BUS BAR, GROUND CAPACITOR	90536	7059969-00	1	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 7			POWER SUPPLY, DC CONVERTER		CONTINUED		
7		4	SCREW, MACH, PAN HD, 6-32UNC-2A 5/16 L (AP)	96906	4912531-01 MS51957-27	AR	
			WASHER, LOCK, I/T, NO 6 (AP)		4912552-01 COML	AR	
			WASHER, LOCK, HEL, NO 6 (AP)	96906	4912550-01 MS35338-136	AR	
			NUT, PLAIN, HEX, MACH 6-32UNC-2B (AP)		4912544-01 COML	AR	
7-35	T1	4	TRANSFORMER, +5V	90536	7059948-00	1	
7-36	T2	4	TRANSFORMER	90536	7059949-00	1	
7		4	SCREW, MACH, FLAT HD, 6-32UNC-2A 0.375 L (AP)	96906	7903133-16 MS24693-C26	10	

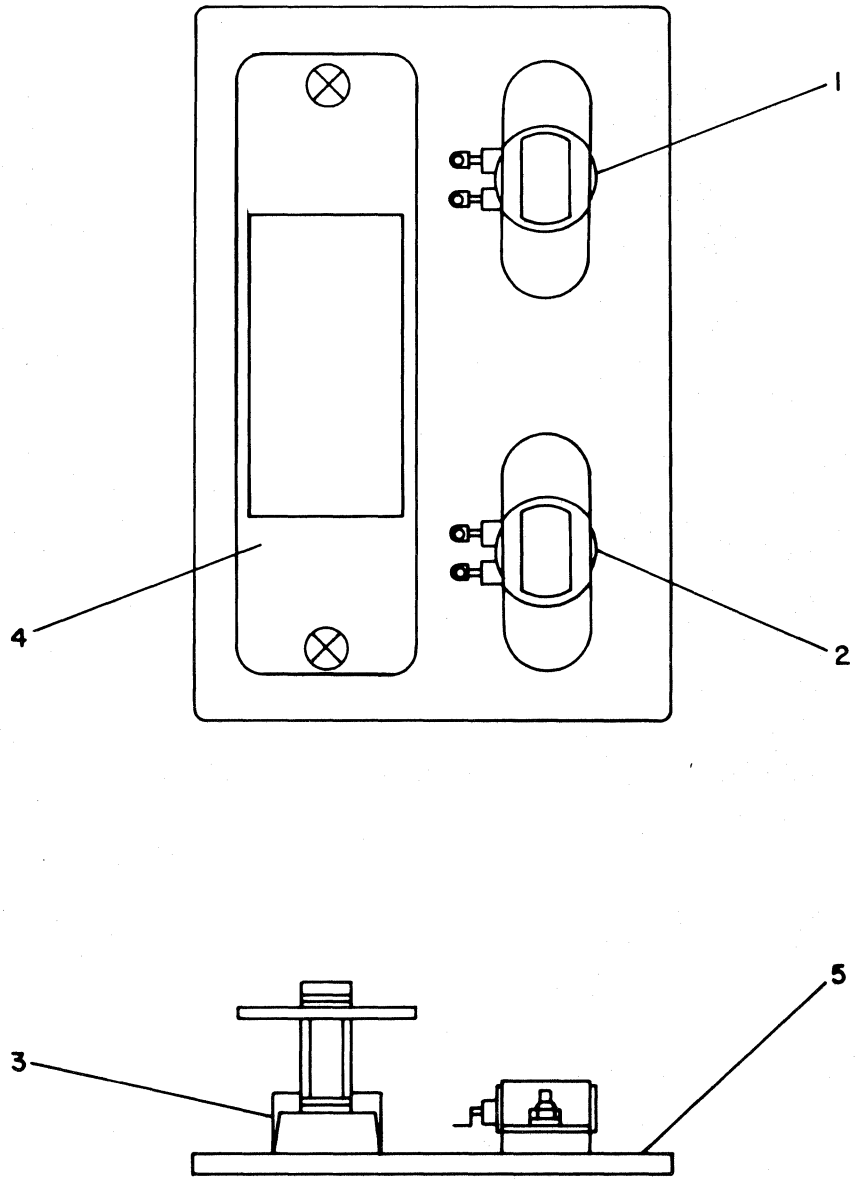


FIGURE 6-8. TEMPERATURE SENSOR ASSEMBLY (A10, A11, A12)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6- 8	A10 A11 A12	3	TEMPERATURE SENSOR ASSEMBLY (SEE FIG 6-1 FOR	90536	7059802-00	REF	
8-1	S1	4	SWITCH, THERMOSTAT, SPST, TEMP RISE, CLOSE 147 +-5 DEG F	73803	7901851-03 M221F147050541	1	
8-2	S2	4	SWITCH, THERMOSTAT, SPST, TEMP RISE, CLOSE 115 +-4 DEG F	73803	7901851-10 M221F115040541	1	
8		4	SCREW, MACH, FLAT HD, 2-56UNC-2A 0.44 L (AP)	96906	906009-05 MS51959-6	4	
			WASHER, FLAT, NO 2 (AP)	96906	4912548-10 MS15795-804	4	
			NUT, SELF LOCKING, HEX 2-56UNC-3B (AP)	72962	906056-01 79LH1660-26	4	
8-3	TB1	4	TERMINAL BOARD, BARRIER TYPE	81349	911813-03 26TB10	1	
			SPACER, PLATE (AP)	90536	7085124-00	2	
8-4		4	COVER, TERMINAL BOARD	90536	7059819-01	1	
8		4	SCREW, MACH, PAN HD, 6-32UNC-2A 3/8 L (AP)	96906	4912531-02 MS51957-28	2	
			WASHER, LOCK, HEL, NO 6 (AP)	96906	4912550-01 MS35338-136	4	
			WASHER, FLAT, NO 6 (AP)	96906	4912548-11 MS15795-806	2	
8-5		4	BOARD, TEMPERATURE SENSOR	90536	7059803-00	1	

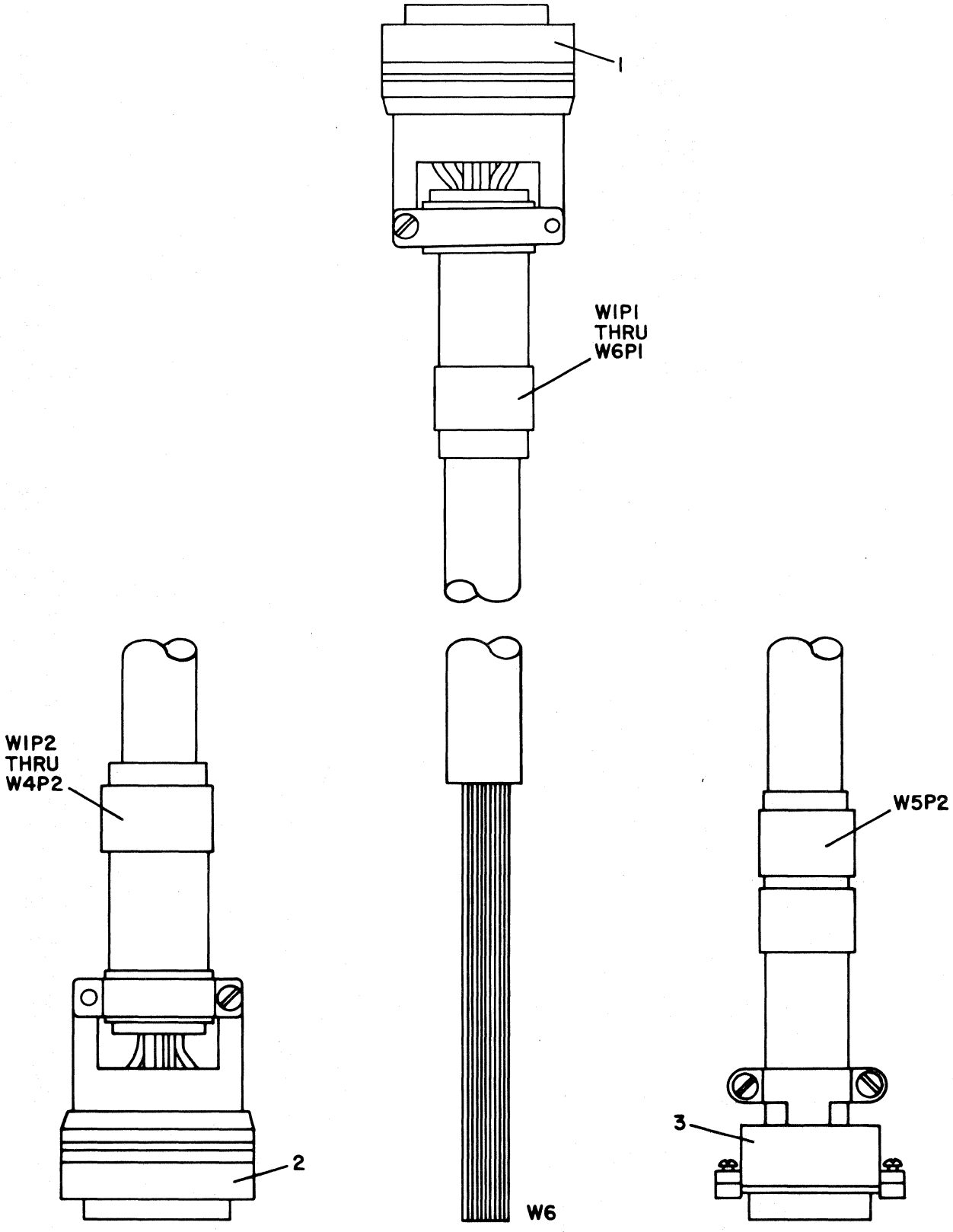


FIGURE 6-9. POWER CABLE ASSEMBLY (W1 THRU W6)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6- 9	W1	3	CABLE ASSEMBLY, POWER	90536	7059885-00	REF	A
	W2		CABLE ASSEMBLY, POWER	90536	7059885-01	REF	B
	W3		CABLE ASSEMBLY, POWER	90536	7059885-02	REF	C
	W4		CABLE ASSEMBLY, POWER	90536	7059885-03	REF	D
	W5		CABLE ASSEMBLY, CONTROL UNIT PWR	90536	7059893-00	REF	E
	W6		CABLE ASSEMBLY, CONTROL UNIT PWR (SEE FIG 6-1 FOR NHA)	90536	7059886-00	REF	F
9-1	W1P1	4	CONNECTOR, PLUG, ELEC, MALE 21 CONTACT	96906	7900590-01 MS3126F22-21PW	1	A
	W2P1		CONNECTOR, PLUG, ELEC, MALE 21 CONTACT	96906	7900590-02 MS3126F22-21PX	1	B
	W3P1		CONNECTOR, PLUG, ELEC, MALE 21 CONTACT	96906	7900590-03 MS3126F22-21PY	1	C
	W4P1		CONNECTOR, PLUG, ELEC, MALE 21 CONTACT	96906	7900590-04 MS3126F22-21PZ	1	D
	W5P1		CONNECTOR, PLUG, ELEC, MALE 21 CONTACT	96906	7900590-00 MS3126F22-21P	1	E
	W6P1		CONNECTOR, PLUG, ELEC, FEMALE 21 CONTACT	96906	7900591-00 MS3126F22-21S	1	F
9-2	W1P2 THRU W4P2	4	CONNECTOR, PLUG, ELEC, FEMALE 21 CONTACT	96906	7900591-00 MS3126F22-21S	1	ABCD
9-3	W5P2	4	CONNECTOR, RCPT, ELEC, FEMALE 5 CONTACT, 2 CAVITIES	71468	7902558-00 DAM-7W2S	1	E
9		4	CONTACT, ELEC, FEMALE, 16 AWG (AP)	71468	7902560-02 DM53744-7	2	E

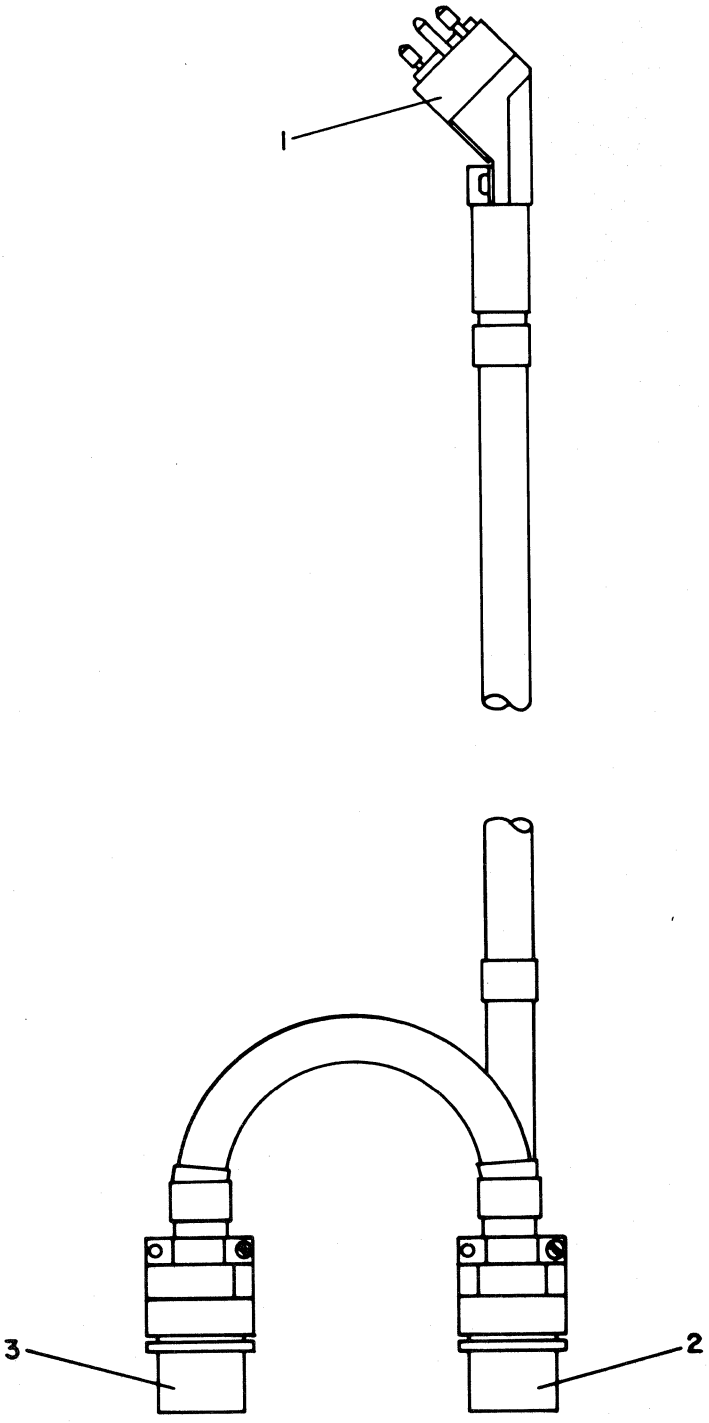


FIGURE 6-10. INPUT/OUTPUT CABLE ASSEMBLY
(W7, W8, W9, W11)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6-10	W7	3	CABLE ASSEMBLY, INPUT/OUTPUT	90536	7059887-00	REF	A
	W8		CABLE ASSEMBLY, INPUT/OUTPUT	90536	7059887-01	REF	B
	W9		CABLE ASSEMBLY, INPUT/OUTPUT	90536	7059888-00	REF	C
	W11		CABLE ASSEMBLY (SEE FIG 6-1 FOR NHA)	90536	7059890-00	REF	D
10-1	P1	4	CONNECTOR, PLUG, ELEC, FEMALE 120 CONTACT	90536	7078161-00	1	
10		5	CONTACT, ELEC, FEMALE, MINIATURE 20-30 AWG (AP)	00779	7902072-01 85967-4LP	120	
			SCREW, MACH, PAN HD, 6-32UNC-2A .500 L (AP)		4912524-04 COML	2	
			WASHER, LOCK, HEL, NO 6 (AP)	96906	4912550-01 MS35338-136	2	
			WASHER, FLAT, NO 6 (AP)	96906	4912548-01 MS15795-805	2	
			BOLT, EXTERNALLY RELIEVED BODY (AP)	90536	7084870-00	2	
			WASHER, LOCK, HEL, NO 10 (AP)	96906	4912550-03 MS35338-138	2	
			WASHER, FLAT, NO 10 (AP)	96906	4912548-02 MS15795-807	2	
10-2	J1	4	CONNECTOR, RCPT, ELEC, CIR SUBMINIATURE, MALE, 85 CONT	81349	7902698-00 M81511-01EF01P1	1	AB
10-3	J2	4	CONNECTOR, RCPT, ELEC, CIR SUBMINIATURE, MALE, 85 CONT	81349	7902698-01 M81511-01EF01P2	2	C

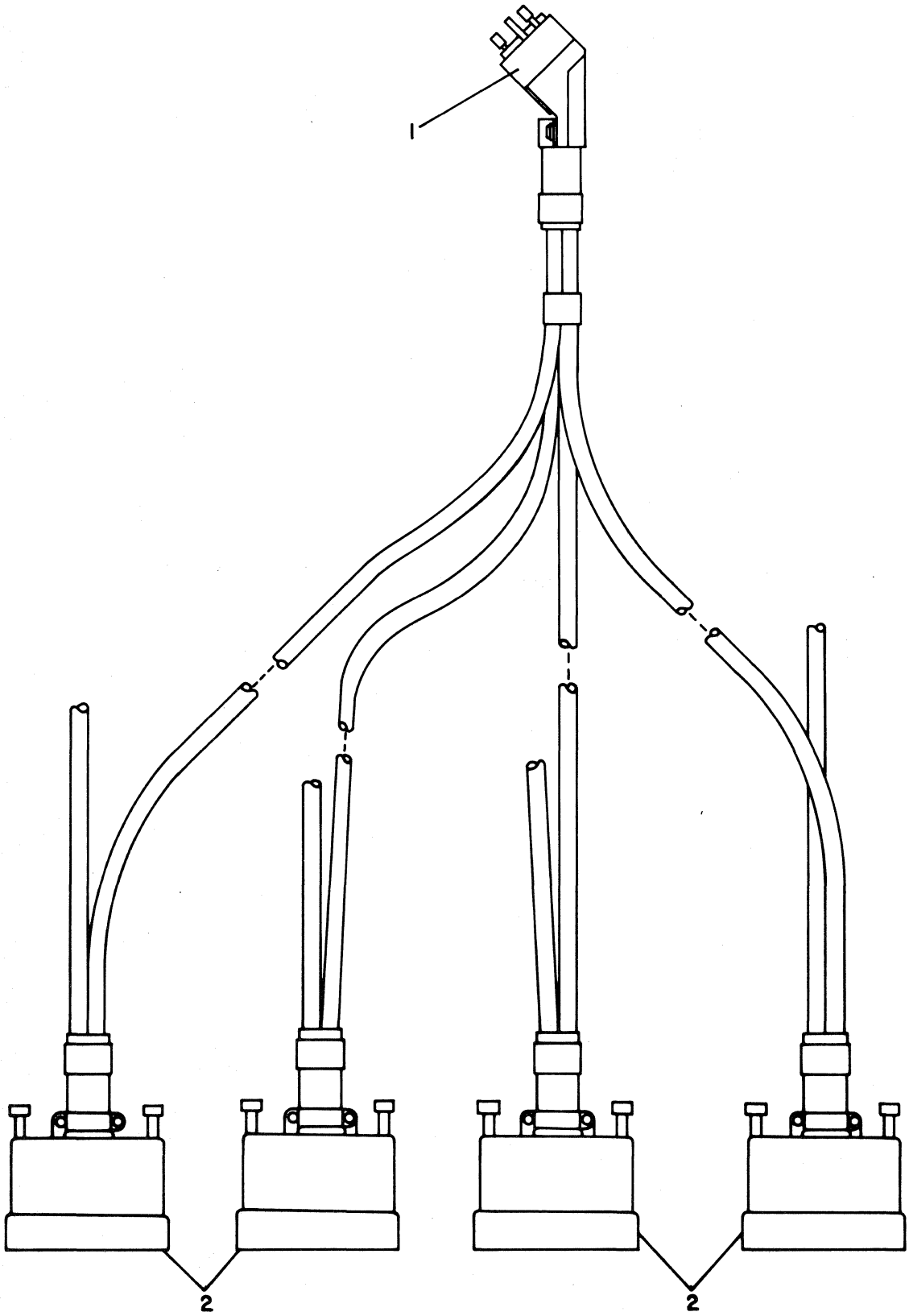


FIGURE 6-11. CABLE ASSEMBLY (W10)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6-11	W10	3	CABLE ASSEMBLY (SEE FIG 6-1 FOR NHA)	90536	7059889-00	REF	
11-1	W10P5	4	CONNECTOR, PLUG, ELEC, FEMALE 120 CONTACT	90536	7078161-00	1	
11		5	SCREW, MACH, PAN HD, 6-32UNC-2A .500 L (AP)		4912524-04 COML	2	
			WASHER, LOCK, HEL, NO 6 (AP)	96906	4912550-01 MS35338-136	2	
			WASHER, FLAT, NO 6 (AP)	96906	4912548-01 MS15795-805	2	
			BOLT, EXTERNALLY RELIEVED BODY (AP)	90536	7084870-00	2	
			WASER, LOCK, HEL, NO 10 (AP)	96906	4912550-03 MS35338-138	2	
			WASHER, FLAT, NO 10 (AP)	96906	4912548-02 MS15795-807	2	
			CONTACT, ELEC, FEMALE, MINIATURE 20-30 AWG (AP)	00779	7902072-01 85967-4LP	AR	
11-2	W10P1 THRU W10P4	4	INSULATOR, ELEC, CONN, MALE 50 CONTACT	81312	911447-00 XAC-50PC-1306	4	
11		4	CONTACT, ELEC, CONN, MALE SIZE .062 (AP)	96906	7903062-00 MS17803-16-20	140	

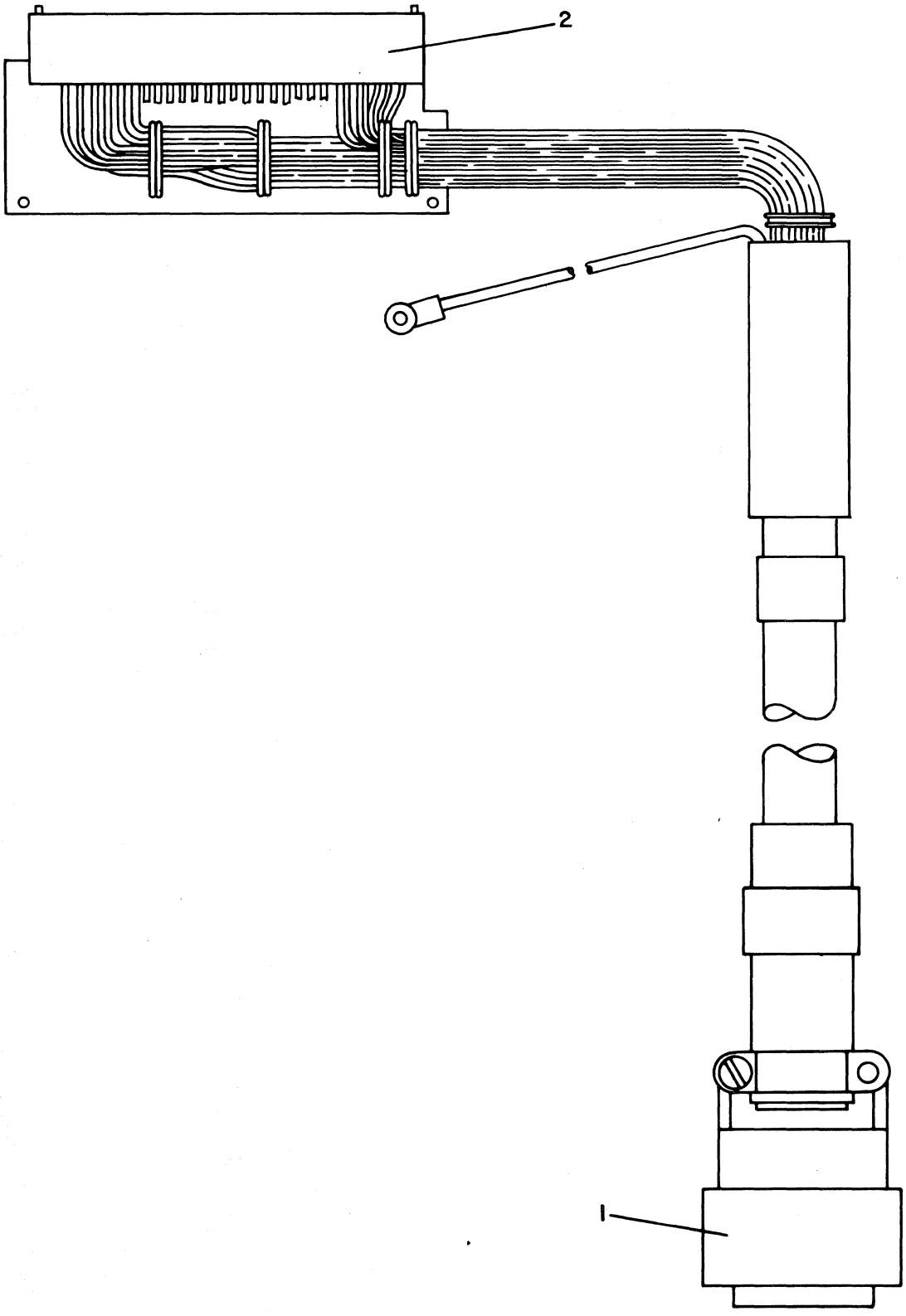


FIGURE 6-12. READ CABLE ASSEMBLY (W12 THRU W15)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6-12	W12	3	CABLE ASSEMBLY, READ	90536	7059880-00	1	
	W13		CABLE ASSEMBLY, READ	90536	7059880-01	1	
	W14		CABLE ASSEMBLY, READ	90536	7059880-02	1	
	W15		CABLE ASSEMBLY, READ	90536	7059880-03	1	
			(SEE FIG 6-1 FOR NHA)				
12-1	P1	4	CONNECTOR, PLUG, ELEC, FEMALE		7904288-00	1	
			39 CONTACT	96906	MS3126F20-39SW		
12		4	CONTACT, ELEC, FEMALE, 22-26 AWG		7903402-00	AR	
				22526	47706		
12-2	P2	4	CONNECTOR, PLUG, ELEC, 56 CONT	90536	7096411-00	1	

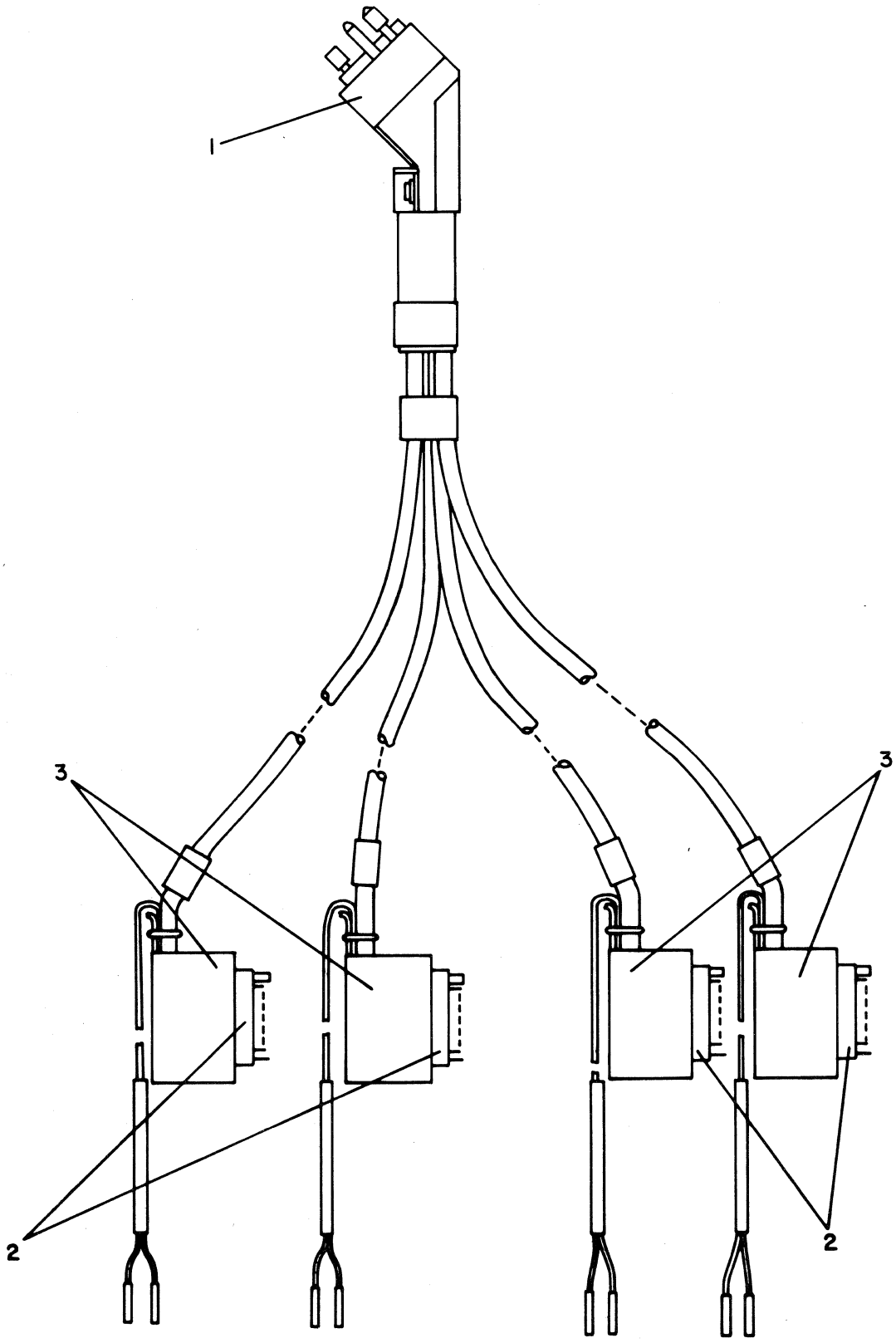


FIGURE 6-13. WRITE CABLE ASSEMBLY (W16)

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6-13	W16	3	CABLE ASSEMBLY, WRITE (SEE FIG 6-1 FOR NHA)	90536	7059892-00	REF	
13-1	W16P1	4	CONNECTOR, PLUG, ELEC, FEMALE 120 CONT	90536	7078161-00	1	
13		5	SCREW, MACH, PAN HD, 6-32UNC-2A .500 L (AP)		4912524-04	2	
					COML		
			WASHER, LOCK, HEL, NO 6 (AP)		4912550-01	2	
				96906	MS35338-136		
			WASHER, FLAT, NO 6 (AP)		4912548-01	2	
				96906	MS15795-805		
			BOLT, EXTERNALLY RELEIVED BODY (AP)	90536	7084870-00	2	
			WASHER, LOCK, HEL, NO 10 (AP)		4912550-03	2	
				96906	MS35338-138		
			WASHER, FLAT, NO 10 (AP)		4912548-02	2	
				96906	MS15795-807		
			CONTACT, ELEC, FEMALE, MINIATURE		7902072-01	AR	
				00779	85967-4LP		
13-2	W16P2 W16P4 W16P6 W16P8	3	CONNECTOR, RCPT, ELEC SUBMINIATURE, MALE, 29 CONT	81312	7903322-00 SLE29PNSS	4	
13-3		3	SHELL, CONNECTOR	90536	7059813-00	4	

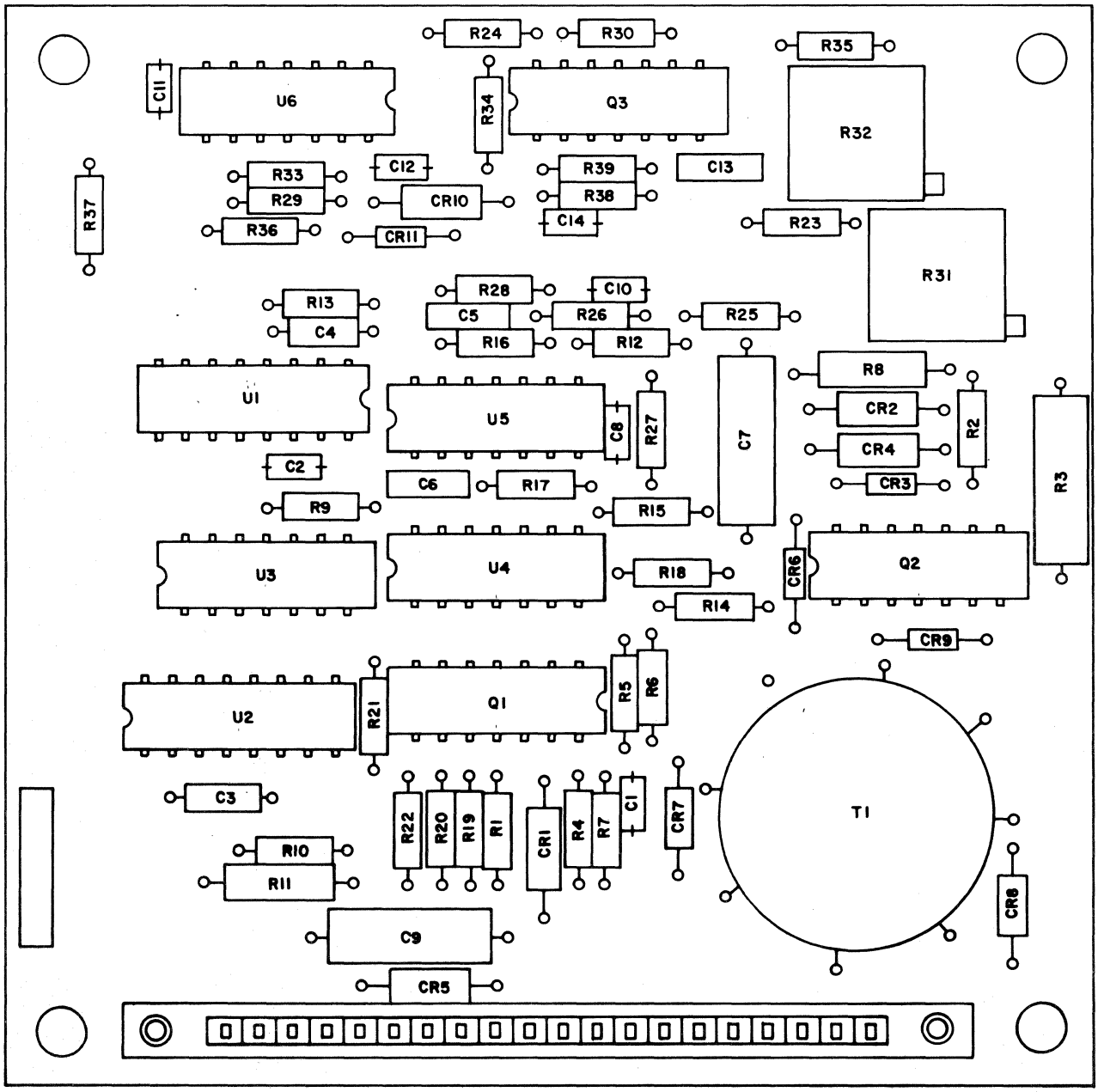


FIGURE 6-14. CONVERTER CONTROLLER CIRCUIT CARD ASSEMBLY

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6-14		4	CIRCUIT CARD ASSEMBLY CONTROLLER, CONVERTER (SEE FIG 6-7 FOR NHA)	90536	7059941-01	REF	
14	C1 C10	5	CAPACITOR, FXD, CER, DIELECTRIC 100V, .010UF, +-10PCT	81349	7901102-48 CK05BX103K	2	
14	C2 C12	5	CAPACITOR, FXD, CER, DIELECTRIC 200V, 330PF, +-10PCT	81349	7901102-18 CK05BX331K	2	
14	C3 C4	5	CAPACITOR, FXD, CER, DIELECTRIC 25V, 1000PF, +-5PCT	81349	7903421-37 CK31BT103J	2	
14	C5 C13	5	CAPACITOR, FXD, CER, DIELECTRIC 50V, 1.0UF, +-10PCT	81349	7901102-109 CK06BX105K	2	
14	C6	5	CAPACITOR, FXD, CER, DIELECTRIC 50V, .22UF, +-10PCT	81349	7901102-101 CK06BX224K	1	
14	C7	5	CAPACITOR, FXD, ELCT, 35V 6.8UF, +-10PCT	81349	7902696-43 M39003-01-2304	1	
14	C8 C14	5	CAPACITOR, FXD, CER, DIELECTRIC 50V, .10UF, +-10PCT	81349	7901102-60 CK05BX104KM	2	
14	C9	5	CAPACITOR, FXD, ELCT, 10V 39UF, +-10PCT	81349	7902696-12 M39003-01-2259	1	
14	C11	5	CAPACITOR, FXD, CER, DIELECTRIC 50V, 22000PF, +-10PCT	81349	7901102-52 CK05BX223K	1	
14	CR1	5	SEMICONDUCTOR DVC, DIODE, SI VR, 20V	81349	7900259-25 1N968B	1	
14	CR2 CR4	5	SEMICONDUCTOR DVC, DIODE, SI VR, 6.8V	81349	7900258-11 1N754A	2	
14	CR3 CR6 CR9 CR11	5	SEMICONDUCTOR DVC, DIODE, SI SW, 500MW, 75V	03508	7901009-00 DJXR499	4	
14	CR5	5	SEMICONDUCTOR DVC, DIODE, SI VR, 1W, 20.0, +-5PCT	71590	7900552-11 R5148-12	1	
14	CR7 CR8	5	SEMICONDUCTOR DVC, DIODE, 300MW 1A, 400V	81349	7902067-01 1N3612	2	
14	CR10	5	SEMICONDUCTOR DVC, DIODE, SI VR, 6.2V	81349	7900258-10 1N753A	1	
14	P1	5	CONNECTOR, RCPT, ELEC, FEMALE 20 CONTACT	90536	7131819-00	1	
14	Q1 Q2	5	SEMICONDUCTOR DVC SET, SI, XSTR QUAD, PAIR	04713	7904255-00 MHQ6002	3	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO / MFR PART NO	QTY PER ASSY	USED ON
6-14			CIRCUIT CARD ASSEMBLY		CONTINUED		
	Q3						
14	R1 R30	5	RESISTOR, FXD, FILM, 1/4W 750 OHM, +-2PCT	81349	7902753-28 RLR07C751GM	2	
14	R2 R25 R36	5	RESISTOR, FXD, FILM, 1/4W 2.4K OHM, +-2PCT	81349	7902753-40 RLR07C242GM	3	
14	R3	5	RESISTOR, FXD, WW, 3W, 51 OHM +-5PCT	81349	910509-24 RW69V510	1	
14	R4	5	RESISTOR, FXD, FILM, 1/4W 2.7K OHM, +-2PCT	81349	7902753-41 RLR07C272GM	1	
14	R5 R6 R39	5	RESISTOR, FXD, FILM, 1/4W 2.0K OHM, +-2PCT	81349	7902753-38 RLR07C202GM	1	
14	R7 R34	5	RESISTOR, FXD, FILM, 1/4W 430 OHM, +-2PCT	81349	7902753-22 RLR07C431GM	2	
14	R8	5	RESISTOR, FXD, FILM, 1/2W 1200 OHM, +-2PCT	81349	7902750-49 RLR20C122GM	1	
14	R9	5	RESISTOR, FXD, FILM, 1/4W 22K OHM, +-2PCT	81349	7902753-63 RLR07C223GM	1	
14	R10 R24	5	RESISTOR, FXD, FILM, 1/4W 100K OHM, +-2PCT	81349	7902753-79 RLR07C104	2	
14	R11	5	RESISTOR, FXD, FILM, 1/2W 20K OHM, +-2PCT	81349	7902750-78 RLR20C203GM	1	
14	R12 R17 R20 R37	5	RESISTOR, FXD, FILM, 1/4W 1.0K OHM, +-2PCT	81349	7902753-31 RLR07C102GM	4	
14	R13 R38	5	RESISTOR, FXD, FILM, 1/4W 10K OHM, +-2PCT	81349	7902753-55 RLR07C103GM	2	
14	R14 R15 R19	5	RESISTOR, FXD, FILM, 1/4W 200 OHM, +-2PCT	81349	7902753-14 RLR07C201GM	3	
14	R16	5	RESISTOR, FXD, FILM, 1/4W 680 OHM, +-2PCT	81349	7902753-27 RLR07C681GM	1	
14	R18 R21 R28	5	RESISTOR, FXD, COMP, 1/4W 10 OHM, +-5PCT	81349	7902751-14 RCR07G100JM	3	
14	R22	5	RESISTOR, FXD, FILM, 1/4W 510 OHM, +-2PCT	81349	7902753-24 RLR07C511GM	1	

FIG & INDEX NO	REF DESIG	IND	DESCRIPTION	MFR CODE	UNIVAC PART NO MFR PART NO	QTY PER ASSY	USED ON
6-14			CIRCUIT CARD ASSEMBLY		CONTINUED		
14	R23	5	RESISTOR, FXD, FILM, 1/4W 5.1K OHM, +-2PCT	81349	7902753-48 RLR07C512GM	1	
14	R26 R27	5	RESISTOR, FXD, FILM, 1/4W 3.0K OHM, +-2PCT	81349	7902753-42 RLR07C302GM	2	
14	R29	5	RESISTOR, FXD, FILM, 1/4W 3.3K OHM, +-2PCT				
14	R31 R32	5	RESISTOR, VARIABLE, WW, 3/4W 2K OHM, +-5PCT	81349	7901477-05 RT22C2P202	2	
14	R33	5	RESISTOR, FXD, FILM, 1/4W 470 OHM, +-2PCT	81349	7902753-23 RLR07C471GM	1	
14	R35	5	RESISTOR, FXD, FILM, 1/4W 8.2K OHM, +-2PCT	81349	7902753-53 RLR07C822GM	1	
14	T1	5	TRANSFORMER, DRIVER	90536	7059961-00	1	
14	U1 U2	5	INTEGRATED CIRCUIT, MULTIVIBRAT DUAL, RETRIGGERABLE, RESETTABLE MONO	04713	7903777-00 MC8602P OR MC8602L	2	
14	U3	5	INTEGRATED CIRCUIT, FLIP-FLOP JK, SINGLE, EDGE TRIGGERED	04713	7904189-01 MC7470P	1	
14		5	PRINTED WIRING BOARD, CONTROLLER CONVERTER	90536	7059940-00	1	

PART NUMBER	FIG & INDEX	PART NUMBER	FIG & INDEX	PART NUMBER	FIG & INDEX
BC2206F-0-1	6- 4-11	MS17325-1	6- 2-8	M11B-8743A	6- 2-18
CH09A1NF224K	6- 4-12	MS17803-16-20	6-11	M221F115040541	6- 8-2
CK05BX103K	6-14	MS18209-387	6- 2-5	M221F147050541	6- 8-1
CK05BX104KM	6-14	MS21044-C04	6- 2	M39003-01-2259	6-14
CK05BX223K	6-14	MS21044-C04	6- 4	M39003-01-2265	6- 7-4
CK05BX331K	6-14	MS21044-C08	6- 1	M39003-01-2265	6- 7-7
CK06BX105K	6-14	MS21044-C08	6- 4	M39003-01-2301	6- 7-3
CK06BX224K	6-14	MS21044-C3	6- 1	M39003-01-2304	6-14
CK15BX104K	6- 7-5	MS21044-C4	6- 1	M39003-01-2312	6- 7-2
CK31BT103J	6-14	MS24693-C26	6- 7	M39019-5-80	6- 2-4
CM7333	6- 2-6	MS24693-C272	6- 4	M81511-01EF01P1	6-10-2
CY20C512K	6- 7-10	MS24693-C274	6- 1	M81511-01EF01P2	6-10-3
DAM-7W2P	6- 4-8	MS24693-C275	6- 1	RCR07G100JM	6-14
DAM-7W2S	6- 9-3	MS24693-C294	6- 4	RE60G1500	6- 7-30
DCM-27W2S	6- 4-9	MS24693-C296	6- 1	RE60G1820	6- 7-22
DJXR499	6-14	MS24693-C298	6- 1	RE60G3920	6- 7-31
DJX499	6- 2-25	MS24693-C52	6- 4	RE65GR100	6- 7-23
DLR-8744A	6- 2-22	MS25252-C7A	6- 2-7	RLR07C102GM	6-14
DLR-8746A	6- 2-20	MS3102R20-15P	6- 2-35	RLR07C103GM	6-14
DM53744-7	6- 4	MS3102R20-15PW	6- 2-34	RLR07C104	6-14
DM53744-7	6- 9	MS3126F20-39SW	6-12-1	RLR07C201GM	6-14
DM53745-8	6- 7	MS3126F22-21P	6- 9-1	RLR07C202GM	6-14
DRL-8745A	6- 2-23	MS3126F22-21PW	6- 9	RLR07C223GM	6-14
D0110551	6- 4	MS3126F22-21PX	6- 9	RLR07C242GM	6-14
D0110551	6- 4	MS3126F22-21PY	6- 9	RLR07C272GM	6-14
LM309K	6- 7-29	MS3126F22-21PZ	6- 9	RLR07C302GM	6-14
MC7470P	6-14	MS3126F22-21S	6- 9	RLR07C431GM	6-14
MC8602P OR	6-14	MS3126F22-21S	6- 9-2	RLR07C471GM	6-14
MC8602L		MS35338-136	6- 4	RLR07C511GM	6-14
MHQ6002	6-14	MS35338-136	6- 7	RLR07C512GM	6-14
MJ4035	6- 7-28	MS35338-136	6- 8	RLR07C681GM	6-14
MS15795-803	6- 4	MS35338-136	6-10	RLR07C751GM	6-14
MS15795-804	6- 2	MS35338-136	6-11	RLR07C822GM	6-14
MS15795-804	6- 3	MS35338-136	6-13	RLR20C122GM	6-14
MS15795-804	6- 8	MS35338-137	6- 2	RLR20C203GM	6-14
MS15795-805	6- 4	MS35338-137	6- 3	RL42S104G	6- 2-28
MS15795-805	6- 7	MS35338-138	6-10	RT22C2P202	6-14
MS15795-805	6-10	MS35338-138	6-11	RV2NAYSD105A	6- 6-4
MS15795-805	6-11	MS35338-138	6-13	RW69V510	6-14
MS15795-805	6-13	MS51957-17	6- 2	R5148-12	6-14
MS15795-806	6- 3	MS51957-18	6- 3	SBS-A9	6- 2-15
MS15795-806	6- 8	MS51957-27	6- 4	SBS-A9	6- 6-10
MS15795-807	6- 4	MS51957-27	6- 7	SDT8821	6- 7-21
MS15795-807	6-10	MS51957-28	6- 8	SLE29PNSS	6-13-2
MS15795-807	6-11	MS51957-29	6- 3	SSBLB05AL07	6- 2-21
MS15795-807	6-13	MS51957-32	6- 7	SSBLB05AL07	6- 6-1
MS15795-808	6- 4	MS51957-43	6- 2	SSBLB05CL07	6- 6-2
MS15795-810	6- 1	MS51957-44	6- 3	XAC-50PC-1306	6-11-2
MS15795-810	6- 4	MS51957-46	6- 1	1N3611	6- 7-26
MS15795-841	6- 1	MS51957-47	6- 4	1N3612	6-14
MS15795-841	6- 2	MS51958-64	6- 4	1N753A	6-14
MS15795-841	6- 3	MS51958-65	6- 2	1N754A	6-14
MS15795-842	6- 1	MS51959-6	6- 8	1N968B	6-14
MS15795-842	6- 2	MS75028-23	6- 6-6	11D177-C3100R1	6- 7-12
MS16109-36-1-5N	6- 2-16	MS91528-1N2B	6- 6-5	112D127-C3150Y1	6- 7-25
MS16109-36-2-2N	6- 2-13	MS91528-1P2B	6- 2-24	13AT417T2	6- 6-9
MS16996-21	6- 4	MT1B-8742A	6- 2-19	13AT418T2	6- 6-8

PART NUMBER	FIG & INDEX	PART NUMBER	FIG & INDEX	PART NUMBER	FIG & INDEX
7059959-04	6- 7-19	7091890-01	6- 1	7900362-14	6- 2-14
7059959-05	6- 7-20	7091890-01	6- 5-44	7900499-00	6- 2-8
7059961-00	6-14	7091895-01	6- 5-17	7900552-11	6-14
7059963-00	6- 4-3	7092000-01	6- 5-39	7900590-00	6- 9-1
7059964-00	6- 7-32	7092030-01	6- 5-35	7900590-01	6- 9
7059965-00	6- 7-33	7092165-01	6- 5-40	7900590-02	6- 9
7059966-00	6- 4-7	7092175-01	6- 5-30	7900590-03	6- 9
7059967-00	6- 4-4	7092180-00	6- 5-31	7900590-04	6- 9
7059967-01	6- 4-6	7092185-01	6- 5-32	7900591-00	6- 9
7059969-00	6- 7-34	7092190-00	6- 5-33	7900591-00	6- 9-2
7059978-00	6- 1-26	7092195-01	6- 5-34	7900608-00	6- 2-29
7059978-01	6- 1-27	7092200-01	6- 5-36	7900611-00	6- 2
7059978-02	6- 1-28	7092205-01	6- 5-37	7900612-00	6- 2
7059979-00	6- 1-29	7092240-00	6- 1	7900635-00	6- 6-9
7059979-01	6- 1-30	7092240-00/01	6- 5-46	7900635-01	6- 6-8
7059979-02	6- 1-31	7092240-01	6- 1	7900838-19	6- 4-12
7059979-03	6- 1-32	7092245-00	6- 1	7900925-00	6- 2-17
7059979-04	6- 1-33	7092245-00	6- 5-47	7900925-00	6- 6-11
7059979-05	6- 1-34	7092250-00	6- 1	7900925-01	6- 6-7
7059979-06	6- 1-35	7092250-00/01	6- 5-45	7901009-00	6- 2-25
7059983-00	6- 1-38	7092250-01	6- 1	7901009-00	6-14
7059983-00	6- 1	7092255-01	6- 5-48	7901084-01	6- 4-14
7059983-01	6- 1	7092400-01	6- 5-18	7901102-101	6-14
7059992-00	6- 1	7092405-01	6- 5-19	7901102-109	6-14
7059993-00	6- 1	7092410-01	6- 5-20	7901102-18	6-14
7078161-00	6-10-1	7092415-01	6- 5-21	7901102-48	6-14
7078161-00	6-11-1	7092420-01	6- 5-22	7901102-52	6-14
7078161-00	6-13-1	7092425-01	6- 5-23	7901102-60	6-14
7084870-00	6-10	7092430-01	6- 5-38	7901448-01	6- 7-23
7084870-00	6-11	7092435-01	6- 5-26	7901477-05	6-14
7084870-00	6-13	7092440-01	6- 5-27	7901635-13	6- 7-25
7085124-00	6- 8	7092445-01	6- 5-28	7901637-05	6- 7-12
7091500-01	6- 5-29	7092450-01	6- 5-24	7901851-03	6- 8-1
7091775-01	6- 5-41	7092455-01	6- 5-25	7901851-10	6- 8-2
7091785-01	6- 5-42	7092460-01	6- 5-43	7901859-54	6- 7-30
7091805-01	6- 1	7092465-01	6- 5-55	7901859-57	6- 7-22
7091805-01	6- 5-1	7092470-01	6- 5-56	7901859-67	6- 7-31
7091810-01	6- 1	7092475-01	6- 5-54	7902067-00	6- 7-26
7091810-01	6- 5-2	7092480-01	6- 5-52	7902067-01	6-14
7091815-01	6- 1	7092485-01	6- 5-51	7902072-01	6-10
7091815-01	6- 5-3	7092490-01	6- 5-53	7902072-01	6-11
7091820-01	6- 1	7092495-01	6- 5-50	7902072-01	6-13
7091820-01	6- 5-4	7096411-00	6- 6-3	7902253-00	6- 2-5
7091830-01	6- 5-5	7096411-00	6-12-2	7902323-96	6- 7-23
7091835-01	6- 5-6	7118224-00	6- 4-5	7902558-00	6- 9-3
7091840-01	6- 5-7	7131819-00	6-14	7902558-05	6- 4-9
7091845-01	6- 5-8	72L2-1-1AB	6- 4-14	7902559-02	6- 4
7091850-01	6- 1	7511230-00	6- 7-24	7902559-02	6- 7
7091850-01	6- 5-9	7601768-01	6- 1-36	7902560-02	6- 4
7091855-01	6- 5-10	7601768-02	6- 1	7902560-02	6- 9
7091860-01	6- 5-11	79LH1660-26	6- 8	7902651-00	6- 4-8
7091865-01	6- 5-12	7900003-03	6- 2-16	7902651-05	6- 7-1
7091870-01	6- 5-13	7900003-09	6- 2-13	7902651-05	6- 7-20
7091870-01	6- 5-49	7900182-96	6- 2-28	7902696-12	6-14
7091875-01	6- 5-14	7900258-10	6-14	7902696-17	6- 7-4
7091880-01	6- 5-15	7900258-11	6-14	7902696-17	6- 7-7
7091885-01	6- 5-16	7900259-25	6-14	7902696-41	6- 7-3

PART NUMBER	FIG & INDEX	PART NUMBER	FIG & INDEX
7902696-43	6-14	7904256-00	6- 7-28
7902696-48	6- 7-2	7904270-01	6- 7-29
7902698-00	6-10-2	7904288-00	6-12-1
7902698-01	6-10-3	7904291-00	6- 1-1
7902750-49	6-14	7904320-00	6- 2-18
7902750-78	6-14	7904321-00	6- 2-19
7902751-14	6-14	7904322-00	6- 2-20
7902753-14	6-14	7904322-01	6- 2-23
7902753-22	6-14	7904322-02	6- 2-22
7902753-23	6-14	7904335-09	6- 2-9
7902753-24	6-14	7904348-00	6- 2-6
7902753-27	6-14	7904590-00	6- 1-3
7902753-28	6-14	8TB10	6- 3-3
7902753-31	6-14	85967-4LP	6-10
7902753-38	6-14	85967-4LP	6-11
7902753-40	6-14	85967-4LP	6-13
7902753-41	6-14	900126-12	6- 2-30
7902753-42	6-14	903654-06	6- 1
7902753-48	6-14	905418-04	6- 2-35
7902753-53	6-14	905418-05	6- 2-34
7902753-55	6-14	906009-05	6- 8
7902753-63	6-14	906056-01	6- 8
7902753-79	6-14	906905-06	6- 3-1
7903062-00	6-11	908552-07	6- 2
7903070-47	6- 2-4	908552-09	6- 3
7903132-31	6- 2	909862-01	6- 3-2
7903132-32	6- 3	909902-00	6- 2-7
7903133-16	6- 7	910161-04	6- 3-3
7903133-35	6- 4	910509-24	6-14
7903133-49	6- 4	911447-00	6-11-2
7903133-51	6- 1	911607-00	6- 4
7903133-52	6- 1	911813-03	6- 8-3
7903133-68	6- 4	912052-02	6- 6-5
7903133-70	6- 1	912070-02	6- 2-24
7903133-72	6- 1		
7903140-24	6- 6-4		
7903167-03	6- 1-2		
7903193-10	6- 2-12		
7903193-11	6- 2-11		
7903193-13	6- 2-10		
7903309-91	6- 7-5		
7903322-00	6-13-2		
7903402-00	6-12		
7903421-37	6-14		
7903528-00	6- 7-11		
7903582-00	6- 7-13		
7903777-00	6-14		
7903797-02	6- 6-6		
7903823-00	6- 2-21		
7903823-00	6- 6-1		
7903823-03	6- 6-2		
7903825-04	6- 2-15		
7903825-04	6- 6-10		
7904171-00	6- 4-11		
7904189-01	6-14		
7904208-01	6- 4		
7904255-00	6-14		