INSTRUCTION BOOK
for

BOGART COMPUTING SYSTEM NAVY MODEL CXPK

VOLUME 2 OF 12 VOLUMES

SECTION 4 THEORY OF OPERATION

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SECTION 4

THEORY OF OPERATION

4-1. INTRODUCTION TO BASIC COMPUTER THEORY.

a. GENERAL. The Navy Model CXPK (BOGART) equipment is a single-address general-purpose digital computer designed for operation requiring high speed, great programming versatility, and small compact size. Its internal memory consists of a 4096-word magnetic core storage which is capable of storing a 24-bit word as a whole, or any eight-bit third of a word. The eight-bit or third-of-a-word feature allows the memory to store a total of 12,288 individual eight-bit words.

The functions of BOGART include manipulating data, differentiating various forms of data and performing analytic, counting, and arithmetic operations. The specific operations which the computer performs are determined by a program which defines the sequence of instructions necessary to execute a desired operation. The computer has a library of 57 instructions available to the programmer (see Volume 1). Most of these instructions can be modified during the operation of the machine by any of seven different B-box registers.

To attain high computing speed, the computer operates in the parallel mode, i.e., all digits of a word are operated upon simultaneously. Internal arithmetic operations are in the binary system. The basic word size is 24 binary digits or bits and this word may be an instruction, operand, or an arbitrarily coded quantity.

The physical make-up of equipment consists of the main computer in one air-cooled cabinet, an operation console, electric typewriter cabinet, paper-tape cabinet, converter cabinet, and other optional external equipment. Communication of the main computer with a variety of optional external equipment is made possible by the use of the External Function Register, Input Register, Output Register and converter. Special features built into the computer allow computation to proceed while a unit of the external equipment is operating.

In this volume the emphasis of explanation is placed on what each circuit does logically rather than how each circuit operates electrically in the accomplishment of its function. This approach is taken because of the relatively simple electronic principles involved. The system generally is built of a great number of similar circuits and stages which are adequately explained in the early paragraphs of this section; thus, a general treatment of computer circuits is given which applies to most of the systems operating within the equipment. Where unique circuits are encountered, their operation is described at the point of use rather than in the general theory paragraphs.

b. TERMS AND ABBREVIATIONS. - Because of the complexity of the computer system and equipment, a thorough knowledge of the terms and abbreviations used is essential to the understanding of the system. Sections covering Circuit Symbol Assignments, Glossary of Special Abbreviations and List of Computer Terms should be read preliminary to the reading of this manual. The List of Computer Terms is included as an appendix to Volume 1.

(1) CIRCUIT SYMBOL ASSIGNMENTS. - Many abbreviations used in this text are the same as those used in the Logic Design Equations (Volume 5). The alphabetical code was assigned to similar circuits within the computer system. The 26 capital letters and 5 lower-case letters are assigned as follows:

CIRCUIT SYMBOL ASSIGNMENTS

A -- ACCUMULATOR REGISTER. - The Accumulator, A, is a 24-bit register with multiply step and left shift properties. The A-register has two main functions:

1) As an arithmetic register, A holds the sum, difference, partial product, and partial dividend (and remainder) in the corresponding arithmetic operations.

2) A acts together with Q to form an extended accumulator.

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B -- INDEX REGISTER. - The Index Registers are 15-bit, B-box registers (B_1 through B_7) used to store quantities that modify the m and k portions of the instructions. In addition to the above, during the repeat sequence, B_7 is used as follows: The right 12 bits, k, store the repeat count, while the remaining three bits, m, contain information on whether the address of the repeated instruction is advanced by one, decreased by one, or remains the same for each time the instruction is repeated.

C -- CLOCK CONTROL. - The Clock Control, C is a circuit that controls timing used in the control of all logical circuits.

D -- MAIN CONTROL TRANSLATOR. - The Main Control Translator interprets the six-bit c portion of the instruction and sets the appropriate E cores.

E -- TRANSLATOR CONTROL. - The E cores obtain information from the main control translator and are part of the second level control.

F -- EXTERNAL FUNCTION REGISTER. - The External Function Register, F, is a 15-bit register that controls selection of input and output equipment.

G -- OPERATING CONTROLS. - The Operating Controls consist of the Run, Step, High-Speed, and Re-sync circuits.

H -- MAIN ADDER. - The Main Adder is used to add the contents of X to A.

I -- INPUT REGISTER. - The Input Register, I, is a seven-bit register used as a temporary storage for data received from input equipment.

J -- U-REGISTER ADDER. - The U-register Adder is used to add the contents of B to U.

K -- SHIFT COUNTER. The Shift Counter, K, is a six-bit counter-register used to control shifting operations.

L -- INDICATOR LIGHTS. - The indicator lights are located on the indicator display panel and show the contents of the registers.

M -- MANUAL SWITCHES. - These switches are found on both the control panel and indicator display panel.

N -- FIRST LEVEL CONTROL. - The first level control, N, controls the normal circulation of registers and the control of transmissions between registers.

O -- OUTPUT REGISTER. The Output Register, O, is a seven-bit register used as a temporary storage for data in transit to the output equipment.

P - PROGRAM ADDRESS COUNTER. The Program Address Counter, P, is a 12-stage additive counter which is used to generate successive addresses at which the instructions of the computer's program can be found.

Q - AUXILIARY ARITHMETIC REGISTER. The Auxiliary Arithmetic Register, Q, is a 24-bit register with both multiply step and left shift properties. Its functions are as follows:

1) As an arithmetic register, Q holds the multiplier, quotient, and logical multiplier in the corresponding arithmetic operations.

2) As an assembly register, Q is capable of receiving six bits at a time and by shifting, ultimately assembling a 24-bit word. It also can disassemble a word by the reverse process.

R - MAGNETIC STORAGE TIMING. - These cores control the transfer of information between the Z-register and the Magnetic Core Storage system.

S - STORAGE ADDRESS REGISTER. - The Storage Address Register, S, is a 12 bit register used to store Magnetic Core Storage system addresses while words are being read from or written into storage.

T -TRANSLATOR. - This translator interprets the contents of the m and b portions of the U-register.

U -- PROGRAM CONTROL REGISTER. - The Program Control Register, U, is a 24-bit register composed of the following sections:

c -- INSTRUCTION CODE. The Instruction Code, c is a six-bit section consisting of $U_{18} \ldots U_{23}$ of an instruction word specifying which

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of the 57 instruction sequences is to be executed.

b -- B DESIGNATOR. - The Designator, b, is a three-bit section consisting of $U_{15}...U_{17}$ of an instruction word which specifies the particular B-register (B1 through B7 or none) that is to be used to modify the y portion of the original instruction to obtain Y.

y -- UNMODIFIED SECTION. The unmodified section, y, is the original $U_{00}...U_{14}$ bits of an instruction word.

Y -- MODIFIED SECTION. - The modified section, Y is the 15-bit y as modified by the contents of a B-box specified by the B designator.

m -- INSTRUCTION MODIFIER. - The Instruction Modifier, m, is a three-bit section consisting of $U_{12}...U_{14}$, and is obtained after modifying y. The Instruction Modifier, (m=0 to m=7) may be used as a Storage Field designator which specifies the particular portion of the operand which will be used in the execution of the instruction. This enables the computer to operate on a 24-bit word or any eight-bit third of a word. Input and Output instructions use the m designator to determine if the whole word, or a section thereof, is to be placed in or taken from memory.

As an Instruction Modifier, m, provides a means of obtaining eight optional choices on Jump instructions and Selective Stop. The Instruction Modifier, m, also provides three modifications for the Repeat instruction.

k -- BASE EXECUTION ADDRESS. - The Base Execution Address, k, is a 12-bit section consisting of $U_{00}...U_{11}$ of the modified section Y and has the following functions:

1) Specifies the particular storage address of the operand to be used in the instruction sequence.

2) During a shift instruction, the right 6 bits of k contain the number of shifts.

3) The k portion combined with m can be used as operand.

V -- SEQUENCE CONTROL. - These cores are second level controls used to pass information to the first level controls.

W -- CIRCULATION BIT. - The circulation bits are one-stage registers that can be used for time delay.

X -- EXCHANGE REGISTER. - The Exchange Register, X, is a 24-bit register that has the following functions:

1) Can be complemented by use of the X^{39} buffer.

2) As an exchange register, X handles nearly all internal transmission of words between various sections of the computer.

3) As an arithmetic register, X holds the addend, subtrahend, multiplicand and divisor in the corresponding arithmetic operations.

Z - STORAGE TRANSFER REGISTER. - The Storage Transfer Register, Z, is a 24-bit register used as a temporary storage for words being written into or read from the Magnetic Core Storage.

(2) GLOSSARY OF SPECIAL ABBREVIATIONS. - The following system of abbreviations, not included in the Circuit Symbol Assignments, has been developed to facilitate the explanation of the computer logic:

GLOSSARY OF ABBREVIATIONS

(A)	The 24-bit word in A
Instruction	A word, represented by $i_{23}...i_{00}$, which causes the computer to perform one or more of its operations. It usually consists of an Instruction Code, c, a B Designator, b, an Instruction Modifier, m, and an Execution Address, k
L(Q)(X)	Denotes the logical (bit-by-bit) product of (Q) and (X)

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MC	A prefix denoting Magnetic Core, used to designate signals belonging to the Magnetic Core Storage System
MCS	Magnetic Core Storage System
MT	Magnetic Tape System
NI	Next Instruction
Operand	A word on which an operation is performed
(X)	The 24-bit word in X
(Y)	The contents of storage at address Y
RNI	Read Next Instruction

Symbols

$\longrightarrow$	(Arrow) Transmit, such as (Z) X
( )	(Parentheses) denotes the content(s) of .
$'$	(Prime) denotes "the complement of" such as X , etc.
$\oplus$	Denotes the logical (bit-by-bit) sum of two quantities
$(A)_i$	Initial contents of the Accumulator
$(A)_f$	Final contents of the Accumulator

c. FUNDAMENTALS OF COMPUTER LOGIC.

(1) BOOLEAN ALGEBRA. - A brief review of the basic principles of Boolean Algebra is presented because it is extensively used as an aid in the analysis and design of magnetic switch circuits. Boolean Algebra provides a means for:

1) representing a switching circuit without drawing the circuit

2) quickly finding a multitude of different circuits that will perform any desired switching function

3) the elimination of redundant circuits

With Boolean logic, the circuit designer has a powerful tool to aid in designing new circuits and in simplifying those already in use.

(a) BASIC SYMBOLS. - In Boolean Algebra there are only two different quantities, or values, which come into consideration; these quantities are "0" and "1". Each of the variables, termed "literals", in the Boolean equation can assume only one of these two numerical values, corresponding to the active "1" state or the passive "0" state. A Boolean expression is a function of one or more literals representing a combination of switching elements. Algebraic operations used in these expressions are multiplication, addition, and negation. The symbols used in the algebra are shown in Table 4-1 (Glossary of Boolean Terms).

Multiplication and addition symbols are used to denote AND and OR respectively, so that many of the rules of conventional algebra may be applied to the expressions. For representing the AND operation by multiplication, parentheses and/or grouping are preferred instead of the dot or X notation. A bar over a letter in a Boolean expression denotes negation.

There are two types of Boolean equations: 1) identities, and 2) transfer formulas. An identity consists of two equivalent expressions separated by an equality sign. For example, the equation $(A+B)\,C = AC + BC$ is an identity, which states that either A or B in combination with C is equivalent to either A in combination with C or B in combination with C; while on the other hand, the equation $C = A + B$ is a transfer formula, which states that at some particular instant, a 1 is transferred to element C if a "1"is in either element A or B.

(b) BOOLEAN THEOREMS. - A Boolean expression may be reduced to its simplest equivalent by applying the theorems of Table 4-2. This procedure is noteworthy, because it not only provides means of understanding the circuitry, but also provides means of simplifying magnetic switch circuits, thus reducing the number of components necessary to perform the operations specified by a

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particular transfer equation. For Example, the transfer equation D = AB + B + C can be reduced to its equivalent D = B + C by applying the the theorems of Table 4-2 to eliminate the redundant expression AB. Because the right side of the reduced transfer equation is simpler than the right side of the original equation, a circuit built by using the simplified equation uses less components and yet performs the same logical functions.

The theorems are also applied to convert the final simplified expressions into standard forms, i.e., forms which are more readily adaptable to magnetic switch cores. For example, the transfer equation D = AB + $C\overline{B}$ can be reduced to the formula D = (A + C) ($\overline{B}$) which is applicable to the magnetic core AND NOT circuit shown in Figure 4-5.

The proofs of these theorems are all of a similar nature. As an example, a simple proof of Theorem 11 is presented below.

Theorem 11 contains three literals, each capable of being in either the "0" or the "1" state. The various combinations of "1's" and "0's" for these literals are listed in the Conditions column of Table 4-3. In the Left-Hand Expression column, the logical value of the left-hand side of the expression for each ABC condition is registered. Similar values also are registered in the Right-Hand Expression column next to each ABC condition, to represent values obtained from the right-hand expression of the theorem. It is apparent that the left-hand and right-hand values are equivalent for each ABC condition; therefore the two expressions are identical.

TABLE 4-3
PROOF OF THEOREM 11

$$A + BC = (A + B)(A + C)$$

Conditions A B C	Left-Hand Expression	Right-Hand Expression
0 0 0	0	0
0 0 1	0	0
0 1 0	0	0
0 1 1	1	1
1 0 0	1	1
1 0 1	1	1
1 1 0	1	1
1 1 1	1	1

(2) LOGICAL EQUATIONS THEORY. - The logical equations which satisfy the basic magnetic switch core circuits are as follows:

$C = A$

$C = AB$

$C = A+B$

$C = A\bar{B}$

In each case the left-hand side of the equation is a function of the expression to the right of the equality sign and may have either of the values "0" or "1". Assuming that A, B, and C are cores to which values may be assigned, the value assigned to core C is derived from the logical operation expressed by the particular combination of the cores A and B, each of which may be assigned values of "0" or "1". The equations are termed transfer formulas in which the equality sign indicates the transfer of the value of the expression on the right of the equality sign to the expression on the left of the sign.

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The logical operations expressed by these equations are as follows:

1) C = A

This is a simple transfer formula in which the assigned value of core A is transferred to core C. Thus, C = A is assigned values as follows:

A	C
0	0
1	1

2) C = AB (C = A and B)

The function AB is termed an AND expression: A value of "1" is transferred to core C if both of the cores A and B are assigned the value of "1" .

Thus, C = AB is assigned values as follows:

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

The AND expression may be expanded to include any number of variables to which the values of "0" or "1" may be assigned.

This logical operation is represented by any of the symbols indicating the arithmetic operation of multiplication.

3) C = A+B (C = A or B)

The function A+B is commonly termed an OR expression: A value of "1" is transferred to core C if either (or both) of the cores A or B are assigned the value of "1". Thus, C = A+B is assigned values as follows:

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

The OR expression may be expanded to include any number of variables to which the values of "0" or "1" may be assigned.

4) $C = A\overline{B}$ (C = A and not B)

The function $A\overline{B}$, or AB^{-1} as it is referred to in the following text, is termed an AND NOT expression: A value of "1" is transferred to core C if core A is assigned the value of "1", and core B is not assigned the value of "1"; or, C assumes the value of "1" if both A and NOT B, (B^{-1}), have the value of "1". Thus $C = (AB^{-1})$ ls assigned values as follows:

A	B	B^{-1}	C
0	1	0	0
0	0	1	0
1	1	0	0
1	0	1	1

The logical AND operation of the expression is represented by any of the symbols indicating the arithmetic operation of multiplication.

(a) APPLICATIONS TO COMPUTER EQUATIONS. - The logical equations discussed previously can be used to express the operations of the magnetic switch core circuitry and indicate the states of the cores involved by assuming the following correlations:

1) Magnetic cores can be in either the "0" or the "1" state.

2) The answer to the question of whether or not a value of "1" is to be transferred to core C is determined by the states of the cores A and B and the logical operations of the functions.

3) The transfer of a value of "1" to core C is accomplished by the coincident application of Read and Transfer pulses to the circuitry.

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NOTE

THROUGHOUT THE REMAINING PORTION OF THIS INSTRUCTION BOOK, THE BAR NEGATION SYMBOL (EXAMPLE $\overline{B}$) WILL BE REPLACED BY A NEGATIVE SUPERSCRIPT (EXAMPLE B^{-1}). THIS SIMPLIFIES WRITING OF EQUATIONS WITH THE ELECTRIC TYPEWRITER

(b) MAGNETIC SWITCH TRANSFER FORMULAS. - A logical equation is used to describe the function of each magnetic switch core. Because of the number of cores in the computer and their operation at four different clock times of a cycle, special symbols, each designating one particular core, are used in these logical equations. All these equations are formulated in one of two standard forms; the terms which express the basic AND and OR circuits have been described previously.

1 SYMBOLS. - A typical symbol for a core is shown in Figure 4-1, along with an interpretation of the associated superscript and subscript characters. This symbol is used in the logical transfer formulas to represent a core in the Auxiliary Arithmetic Register (Q).

2 STANDARD FORMS OF TRANSFER EQUATIONS. - The standard types of transfer equations are used as follows:

The logical OR expression, $C = A + B$
The logical AND NOT expression, $C = AB^{-1}$

Each of these consists of a left-hand term consisting of a symbol for one core, and a right-hand logical expression consisting of not more than four AND clauses, each consisting of not more than four core symbols.

a OR EQUATION. - The OR equation $C = A + B$ is applicable to a basic OR circuit as shown in examples 1 and 2.

EXAMPLE 1

$$X^{00}_{00} = X^{30}_{00}\,N^{30}_{00} + X^{30}_{04}\,N^{30}_{01} + X^{30}_{08}\,N^{30}_{02} + X^{30}_{16}\,N^{30}_{03}$$

EXAMPLE 2

$$X^{10}_{01} = X^{00}_{01}\,N^{00}_{00} + X^{00}_{00}\,Q^{00}_{01}\,N^{00}_{04} + U^{30}_{01}\,N^{30}_{05}$$

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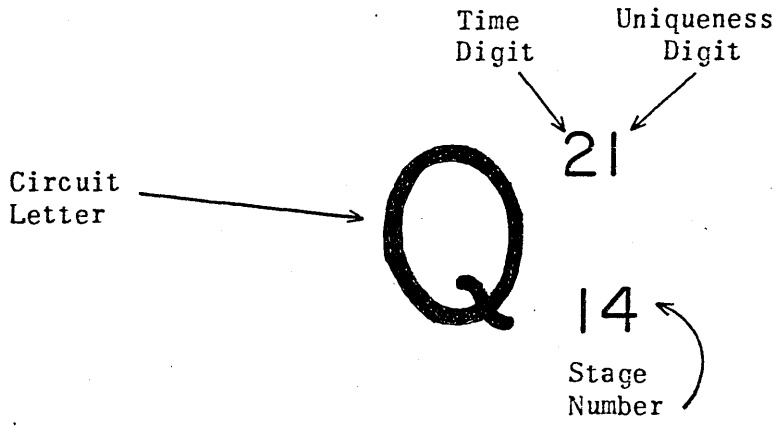

Circuit Letter	One letter is used to designate all cores belonging to a particular register or control system. (Circuit letters are listed in Circuit Symbol Assignments.)
Stage Number	Two subscript numerals indicate the register stage or control circuit subdivision to which a core belongs. For example, in the Q-register, these numbers range from 00 to 23, to correspond with the 24 stages of Q.
Time Digit	The first superscript numeral indicates the particular Read Pulse (0, 1, 2, or 3) applied to read the core.
Uniqueness Digit	This digit is 0 unless two or more cores have the same circuit letter, stage number, and time digits. If this condition exists, the symbols are assigned different uniqueness digits so that each core will be represented by a unique symbol.

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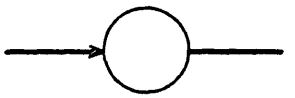
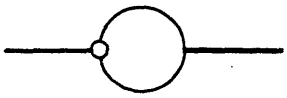
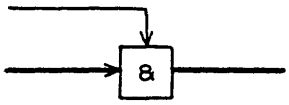
Figure 4-1. Core Symbols



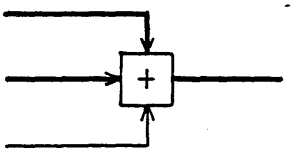
A 1/2 inch circle is used to indicate a magnetic switching core.



A 3/32 inch circle on the rim of a switching core is used to indicate negation or a logical "NOT" circuit.

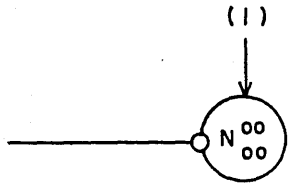


A 1/4 inch square, with (&) inserted, is used to indicate a logical AND circuit.

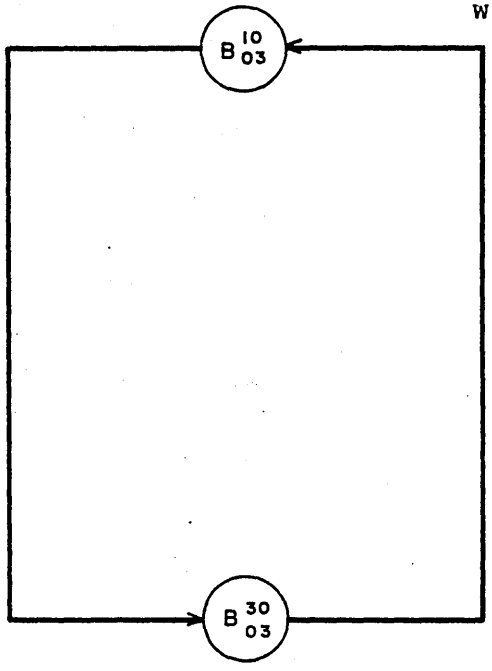


A 1/4 inch square, with (+) inserted, is used to indicate a logical OR circuit.

A heavy inked line terminated by a barbed arrow is used to indicate the path of information.



A light pencil line terminated by an 'N' core is used to indicate the path of control pulses. Core symbols, and identifying time and stage numbers, are placed within the 1/2 inch circle. An "unconditional set" terminates at the circle with an arrow head, and shows the pulse time (in parentheses) adjacent to the line.



Normal circulation is indicated by a rectangle connecting the cores of any stage in a register.

Information movement is counter-clockwise.

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Figure 4-2. Standard Logic Symbols

In each example, the AND clauses on the right side represent Read outputs from the elements of the clause and Set inputs to the core indicated by the symbol on the left side. Within each AND clause, all symbols have the same time digit. As stated previously in the subparagraph on the basic OR circuit, the operation of the OR circuit is cyclic, and consists of the following steps:

Time n - 2	SET INPUTS
n - 1	SET INPUTS
n	READ OUTPUTS
n + 1	- - - -

By noting the time digits for each of the core symbols, it can be seen that Example 1 satisfies this cycle as follows:

at time 2	NO SET INPUTS TO X^{00}_{00}
3	FOUR SET INPUTS TO X^{00}_{00}
0	READ X^{00}_{00}
1	- - - -

Example 2 satisfies the cycle as follows:

at time 3	ONE SET INPUT to X^{10}_{01}
0	TWO SET INPUTS to X^{10}_{01}
1	READ X^{10}_{01}
2	- - - -

The logic diagrams for these switching circuits are shown in Figures 4-3 and 4-4.

b AND NOT EQUATION. - The AND NOT equation $C = AB^{-1}$ is applicable to the basic AND NOT circuit. An example is given below.

EXAMPLE 3

$$X^{20}_{01} = \left(N^{01}_{08} + A^{00}_{01}\ N^{00}_{07} + I^{00}_{01}\ N^{00}_{08}\right)\left(X^{10}_{01}\ N^{10}_{09}\right)^{-1}$$

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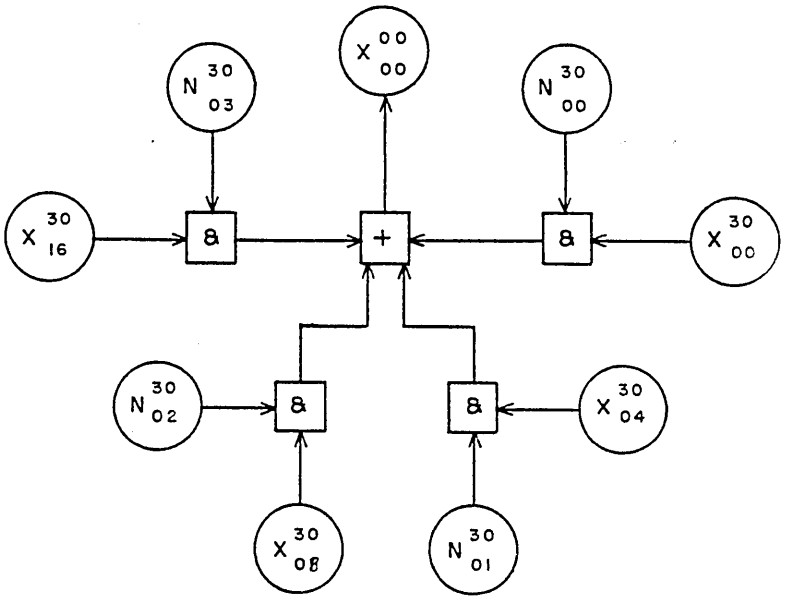

Figure 4-3. Logic Diagram of an AND circuit.

$$X^{00}_{00} = X^{30}_{00}\ N^{30}_{00} + X^{30}_{04}\ N^{30}_{01} + X^{30}_{08}\ N^{30}_{02} + X^{30}_{16}\ N^{30}_{03}$$

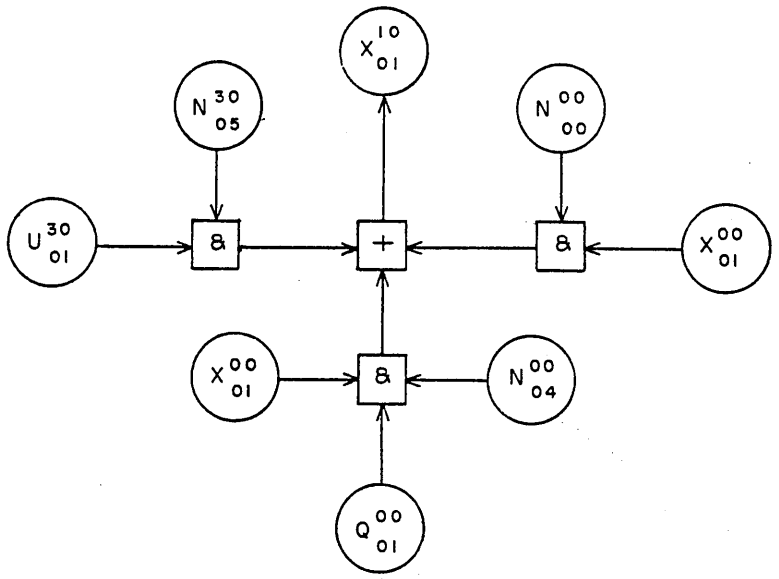

Figure 4-4. Logic Diagram of an OR circuit.

$$X^{10}_{01} = X^{00}_{01}\ N^{00}_{00} + X^{00}_{01}\ Q^{00}_{01}\ N^{00}_{04} + U^{30}_{01}\ N^{30}_{05}$$

On the right side of this example all AND clauses in the first parenthesis have the same time digits, and all AND clauses in the second parenthesis have time digits one clock time later than the time digits in the first parenthesis. Each AND clause in the first parenthesis represents Read outputs from the elements of the clause and a Set input to the core to the left, and each AND clause in the second parenthesis represents Read outputs from the elements of the clause and a Clear input to the core to the left. The -1 superscript notation on the second parenthesis denotes negation. The superscript -1 notation is the only manner in which negation appears in the logical transfer equations for the computer.

As stated previously in the subparagraph on the basic AND NOT circuit, the operation of the basic AND NOT circuit is cyclic and consists of the following steps:

Time n - 2	SET INPUTS
n - 1	CLEAR INPUTS
n	READ OUTPUTS
n + 1	- - -

By noting the time digits for each of the core symbols, it can be seen that example 3 satisfies this cycle as follows:

At time 0	THREE SET INPUTS to X^{20}_{01}
1	ONE CLEAR INPUT to X^{20}_{01}
2	READ X^{20}_{01}
3	- -

The logic diagram for this switching circuit is shown in Figure 4-5.

(3) MAGNETIC SWITCH CIRCUITS.

(a) MAGNETIC CORE. - Each magnetic switch contains a core, which is a ring composed of 20 wraps of 1/8 mil thick permanent magnet alloy.

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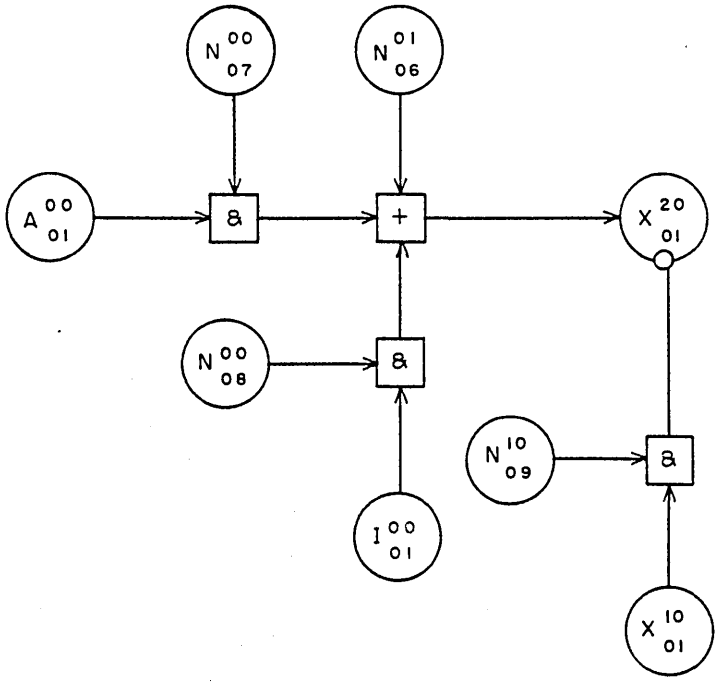

$$X^{20}_{01} = \left(N^{01}_{06} + A^{00}_{01}\ N^{00}_{07} + I^{00}_{01}\ N^{00}_{08}\right)\left(X^{10}_{01}\ N^{10}_{09}\right)^{-1}$$

Figure 4-5. Logic Diagram of an AND NOT circuit.

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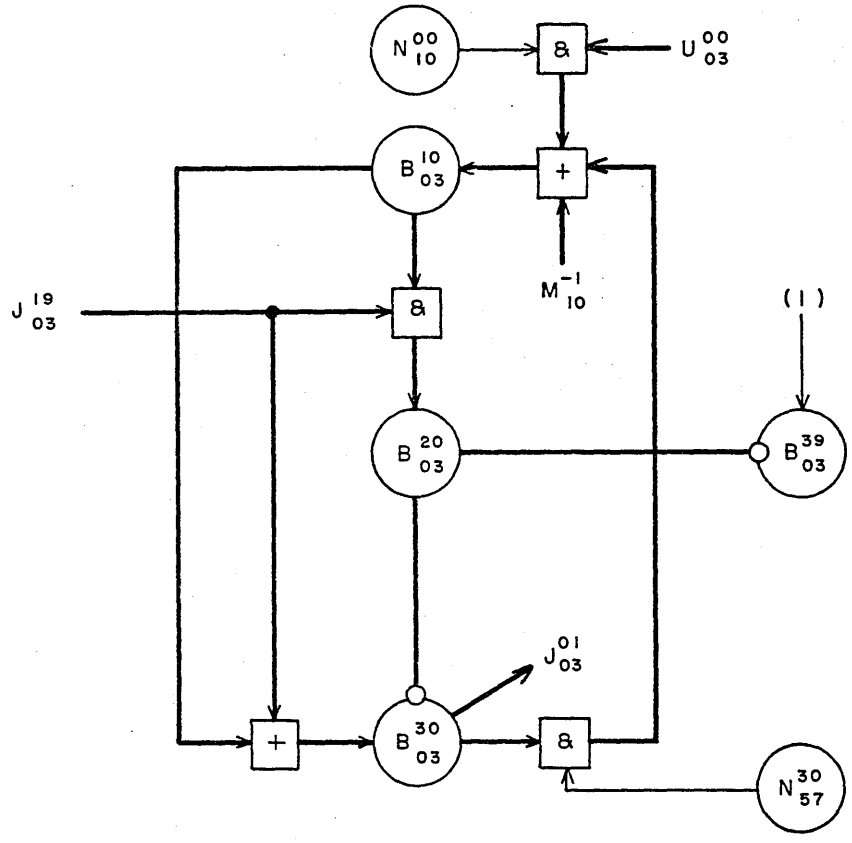

The equations listed below are illustrated above in the typical circuit of a logic diagram.

$$B^{10}_{03} = B^{30}_{03}\, N^{30}_{57} + U^{00}_{03}\, N^{00}_{10} + M^{-1}_{10}$$

$$B^{20}_{03} = B^{10}_{03}\, J^{19}_{03}$$

$$B^{30}_{03} = (B^{10}_{03} + J^{19}_{03})\,(B^{20}_{03})^{-1}$$

$$\text{---}\ J^{01}_{03}\ B^{10}_{03}$$

$$B^{39}_{03} = (B^{20}_{03})^{-1}$$

All cores to the right of the equal sign are considered inputs to the core on the left.
Cores listed in the line below the inputs are considered outputs from the core above on the left.

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Figure 4-6. Complete Stage of B-register

The ring has an inner diameter of 1/10 inch and a thickness of 1/32 inch. Three wire windings with turns ratios of N:N:2.5N are wound on the core and the entire assembly is potted in casting plastic.

A schematic diagram of a type "E" core assembly is shown in Figure 4-7. The 2.5N-turn winding is called the "read" winding, and the other two are called the "set" and "clear" windings.

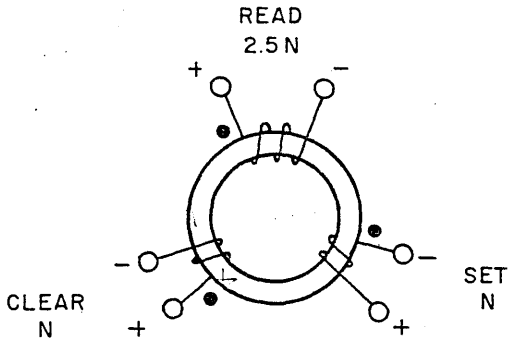
The core is a bistable device capable of storing a "1" or "0" , depending upon the direction of remanent magnetization in the core. In general, the "0" state is produced when a positive pulse is applied to the "dot" end of a winding (see Figure 4-7), and the "1" state is produced when a positive pulse is applied to the opposite end of the winding. Note that the set winding is of opposite polarity to the read and clear windings.

The hysteresis loop for the core material is shown in Figure 4-8.

(b) CRYSTAL DIODES. - Each magnetic switch contains, in addition to the core, from 10 to 15 germanium diodes. The unique property of electrical one-way conduction of diodes makes them useful in the design of logical computer circuits. However, one undesirable characteristic requires special circuit design.

It was generally assumed that germanium diodes would exhibit a large back resistance immediately upon application of a reverse voltage after the diode had been conducting in the forward direction; unfortunately this is not true. Germanium diodes require a finite time to recover to their static back resistance value after reversal of the applied voltage. This time is known as "diode back recovery time".

This enhancement period allows a relatively large decaying reverse current to flow through the magnetic core and may partially reset the core to another value. Where many parallel diodes contribute to this reverse current, as is



Terms:

READ 2.5 N - A Read winding of 100 turns

CLEAR N - A Clear winding of 40 turns

SET N - A Set winding of 40 turns

(•) - (dot) Used to denote a certain end of the winding.

A positive current applied to the "dot" end of a winding produces a "0" state.

A positive current applied to the "opposite" end of a winding produces a "1" state.

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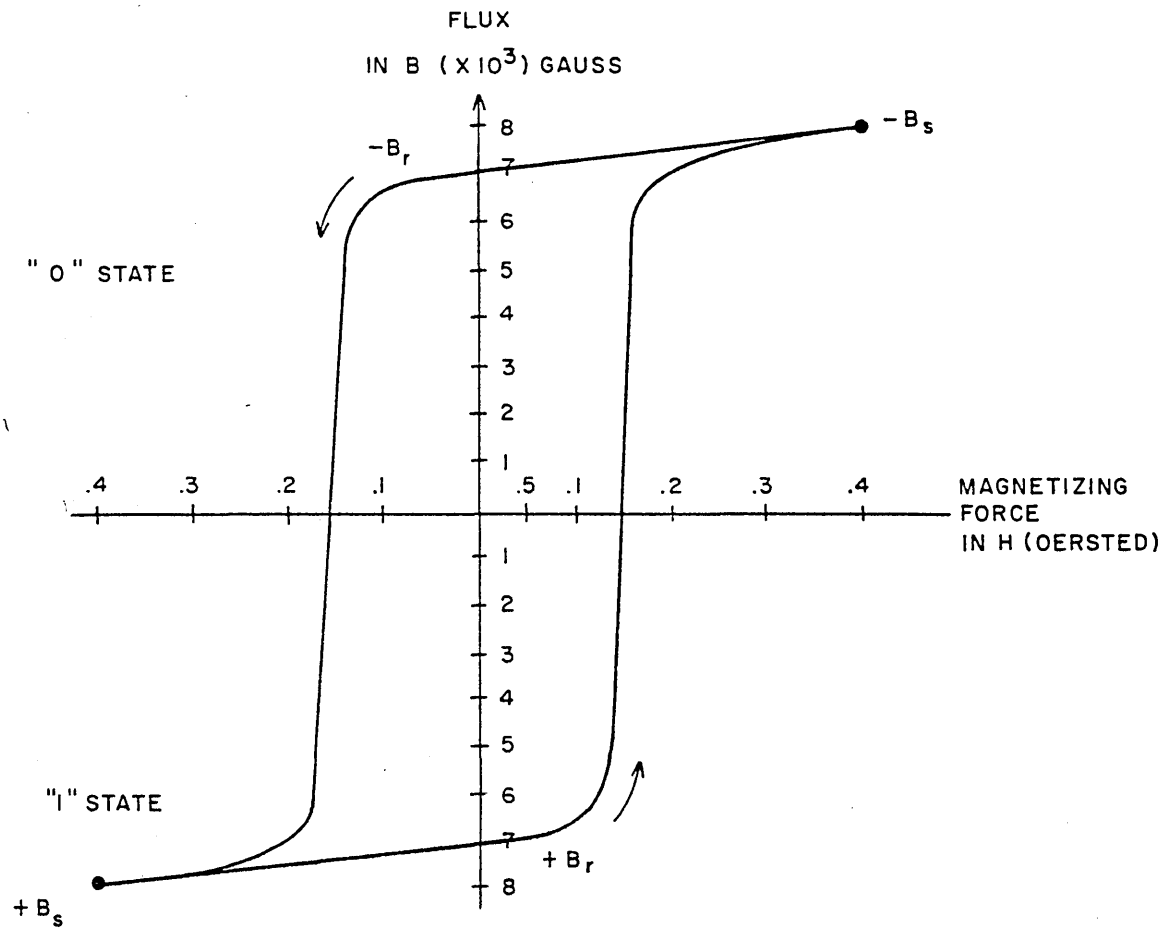
Figure 4-7. Diagram of Magnetic Switch Core



Terms:

$+B_s$ - Saturation flux density in the "1" direction
$+B_r$ - Remanent flux density in the "1" direction
$-B_s$ - Saturation flux density in the "0" direction
$-B_r$ - Remanent flux density in the "0" direction

Writing a "0".

When a positive current is applied to the "dot" end of the winding, assuming that the core is in the "1" state at $+B_r$, the flux state of the core shifts along a major hysteresis loop to point $-B_s$. When the positive current is removed, the core shifts to point $-B_r$ or stable "0" position.

Writing a "1".

When a positive current is applied to the "opposite" end of the winding (see Figure 4-7), assuming that the core is in the "0" state at $-B_r$, the flux state of the core shifts along a major hysteresis loop to point $+B_s$. When the positive current is removed, the core shifts to point $+B_r$ or stable "1" position.

Figure 4-8. Hysteresis Loop of Core Material

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the case with the output diodes on the magnetic switch printed-circuit card, the reverse drive may be sufficient to completely shift a core.

This condition is corrected by deriving a one-microsecond transfer pulse and a two-microsecond read pulse from separate sources. The effect of the enhancement current, caused by the reverse voltage at the end of the transfer pulse, is eliminated by the read pulse existing one microsecond after the termination of the transfer pulse. The characteristic of the diode is such that very little back voltage is generated after one microsecond. With a back recovery time of one microsecond there can be no enhancement current interference after the termination of the two-microsecond read pulse. These pulses are fully described in another paragraph of this chapter.

(c) READ AND TRANSFER PULSES. - The cores in a magnet switch circuit are interconnected so that information is transferred sequentially from core to core by pulses. In each core, the receipt of pulses on the set or clear windings is "remembered" until a pulse on the read winding transmits the remembered bit to the next core.

The Set, Clear, and Read operations of the cores are controlled by two types of pulses: Read Pulses and Transfer Pulses. These pulses, distributed to the cores simultaneously, are of a four-phase cycle. During a cycle, each pulse of each type is given a time, denoted by 0, 1, 2, and 3. For example, the four transfer pulse phases of each cycle ard denoted by TP0, TP1, TP2, and TP3. Thus, the sequence of the operations (set, clear, read) of each core is cyclic.

Wave forms of these pulses are shown in Figure 4-9. While no two of the four transfer pulses (TP0 through TP3) coincide, it should be noted that the four read pulses (RP0 through RP3) overlap by one microsecond. Also note that the first half of RP0 coincides with TP0, the first half of RP1 coincides with TP1, etc.

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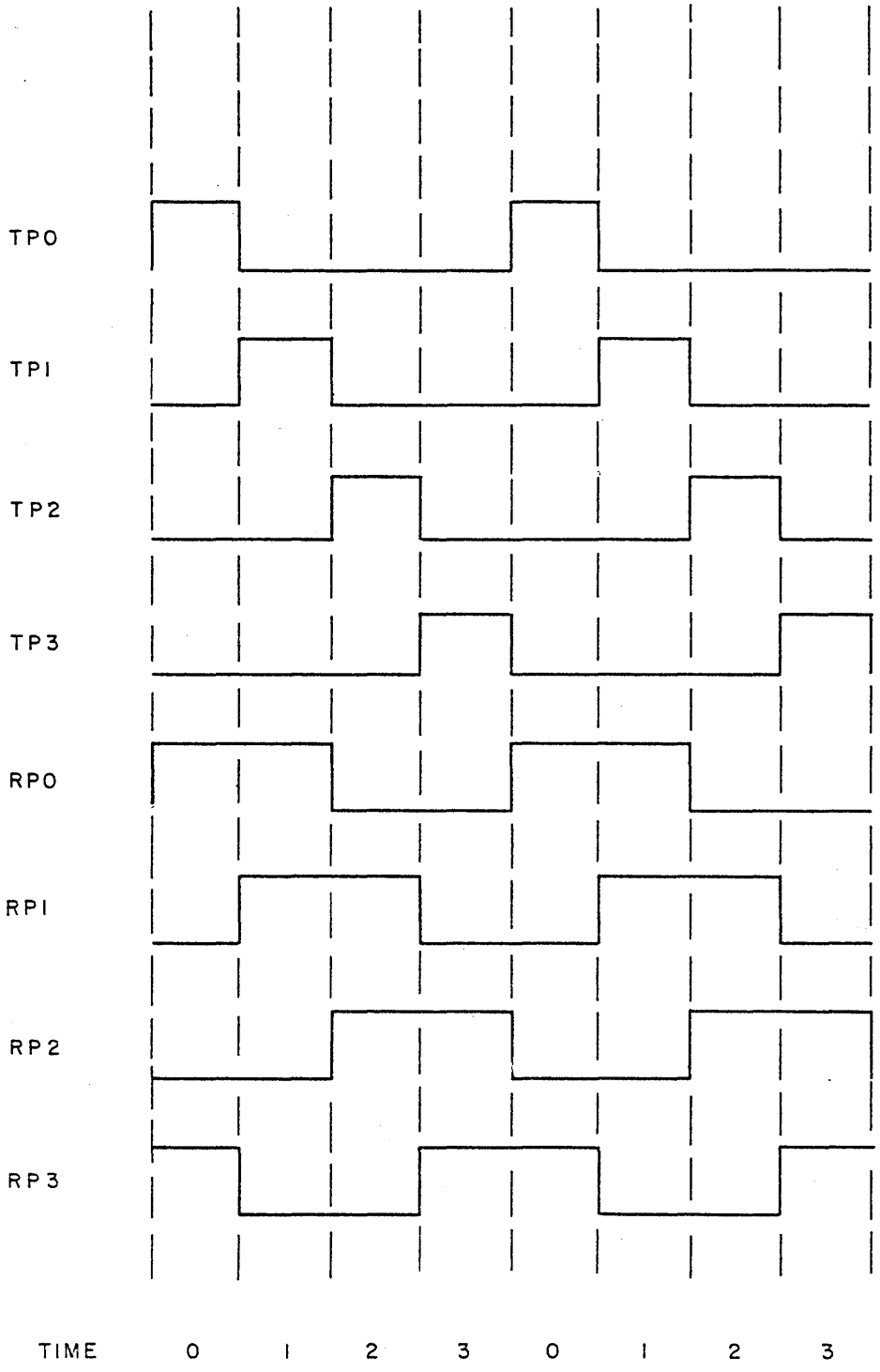

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Figure 4-9. Phase Relationships of Transfer Pulses (TP) and Read Pulses (RP).

(e) BASIC CIRCUITS.

1. BASIC TRANSFER CIRCUIT. - This circuit is a basic block around which all of the other logical circuits are built. The function of this circuit is to transfer the information in core A to core B. Figure 4-10 shows a schematic diagram of the basic transfer circuit. If core A contains a "1", then upon simultaneous application of a read pulse and a transfer pulse, core B is set to the "1" state and core A is cleared to the "0" state. If core A contains a "0", then upon application of the pulses, core B is left in the "0" state and core A is cleared to the "0" state. In either case, B must be initially in the "0" state.

This operation satisfies the Boolean equation B = A, which states that, at some particular instant, B is set to "1" if A contains a "1", or B is left in the "0" state if A contains a "0". The step-by-step operations occurring in the circuit are explained below.

a. TRANSFER OF A 1 . - Assume that core A contains a "1" and is therefore at $+B_r$ on its hysteresis loop, and that core B contains a "0" and is at $-B_r$ on its B-H loop (see Figure 4-8). Also assume that a positive pulse applied to the dotted end of a core winding produces a flux change in the direction $+B_r$ to $-B_r$ and that a positive pulse applied to the opposite terminal produces a flux change in the direction $-B_r$ to $+B_r$.

In the following explanation all references are made to the Basic Transfer Circuit, Figure 4-10, unless otherwise noted.

A steeply rising positive (+24 vdc) two-microsecond read pulse, as shown in Figure 4-9, is applied to R_1. When this clock pulse reaches ground potential, diode D1 conducts and causes a current flow through the 2.5N turn winding on core A. This current causes the magnetic flux in core A to start changing in the direction $+B_R$ to $-B_R$. The flux changes induce a voltage across Read

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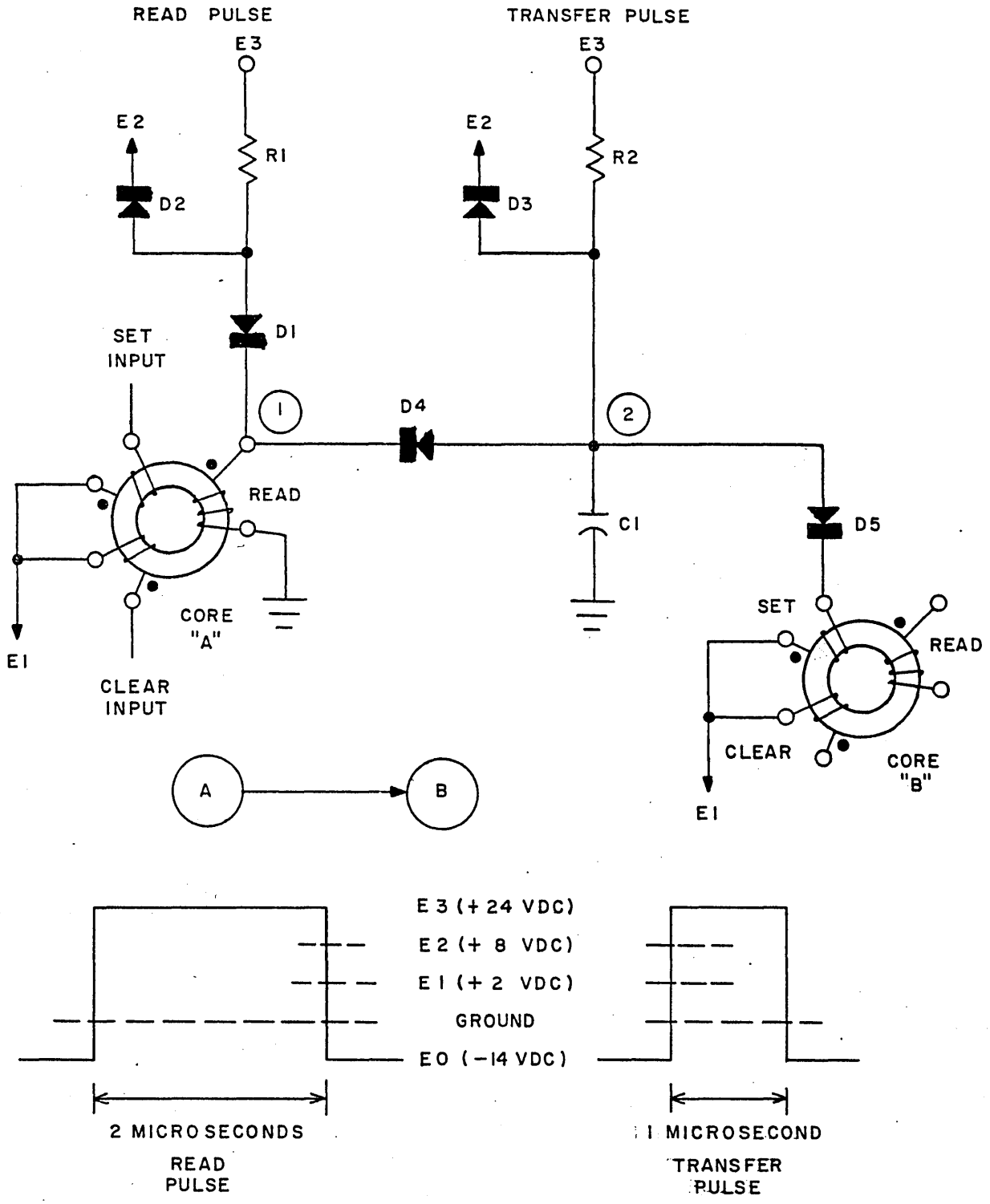

Figure 4-10. Basic Transfer Circuit (B = A)

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coil A which is clamped at E_2 (+8 vdc) by diode D_2. Since the 2.5N turn read winding of A is of relatively large inductance, the switching proceeds rather slowly and back emf at point ① is maintained for about 0.8 microseconds. Point ① is held at +8 vdc during the entire time core A is switching. When the flux in core A has reached $-B_S$, the voltage at point ① momentarily drops to zero.

A one-microsecond transfer pulse (+24 vdc), occurring during the first half of the read pulse and starting simultaneously with the read pulse, is applied through R_2 to point ②. The voltage at point ② rises exponentially at a rate determined by R_2C_1. When this voltage reaches E_1 (+2 vdc), diode D_5 conducts causing core B to start switching from $-B_r$ to $-B_s$. Diode D_4 does not conduct because point ① is already at +8 vdc. Diode D_3 conducts when point ② reaches +8 vdc, thus clamping it at +8 vdc. This causes core B to switch at the constant voltage $E_2 - E_1$ (+60 vdc) until the flux in core B has changed from $-B_r$ to $+B_s$. When the flux in core B reaches $+B_s$, the induced voltage in the set winding falls to zero, and point ② therefore drops to a +2 vdc.

When core A has switched from $+B_R$ to $-B_S$ and point ① is momentarily at ground potential, diode D_4 conducts and point ② falls below +2 vdc, thus preventing D_5 from conducting. The current then flowing in core A is $\frac{E_3}{R_1} + \frac{E_3}{R_2}$. When the transfer pulse is ended, diode D_4 stops conducting and current in the read winding of core A drops to $\frac{E_3}{}$. Finally, when the read pulse drops from E_3 to ground, diode D_1 is cut off, and the flux in core A changes from $-B_S$ to $-B_R$.

b. TRANSFER OF A "0". - Reference is made to Figure 4-10 and 4-12 in considering the case where core A contains a "0" and Core B contains a "0". Under this condition both cores A and B contain a residual flux of $-B_r$ on their hysteresis loops. It is desired to transfer the "0"

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from core A to core B. This is accomplished by creating a minimum disturbance of the magnetic state of core B while core A is being pulsed in the direction $-B_r$ to $-B_s$ on its B-H loop, which is the same direction in which core A was pulsed for a "1" transfer.

To cause this transfer a read pulse is applied to core A (Figure 4-10). At the time the read pulse reaches ground potential, diode D_1 conducts, and a current flows in the read coil which produces a flux change in core A from $-B_r$r to $-B_s$. This flux change induces a voltage in read coil A, causing the voltage at point "1" to rise (as shown in Figure 4-12). This voltage will be clampled at E until the flux in core A reaches $-B_s$. This switching is completed rapidly so that the voltage at point (1) drops from +8 vdc to ground potential in about 0.1 microseconds and remains there until diode D_4 is caused to conduct by the potential at point (2).

It is for the case of a "0" transfer that capacitor C_1 produces its most useful effect; C_1 delays the rise of the transfer pulse voltage at point (2) so that it does not reach ground potential until the voltage at point (1) (produced by the $-B_r$ to $-B_s$ flux change in core A) has fallen to zero. The transfer pulse causes point (2) to rise exponentially toward $+E_3$ at a rate determined by R_2 C_1 until it reaches ground potential. When the voltage at point (2) reaches ground potential, diode D_4 conducts and causes a further flux change in core A. Since core A is already at $-B_s$, the flux change is very small, and consequently the voltage pulse produced at points (1) and (2) is very small. No noticeable current from the transfer pulse passes through diode D_5 and therefore no change can occur in core B.

When the read pulse is terminated, core A settles to $-B_r$ (the "0" state) and core B remains in its initial "0" state.

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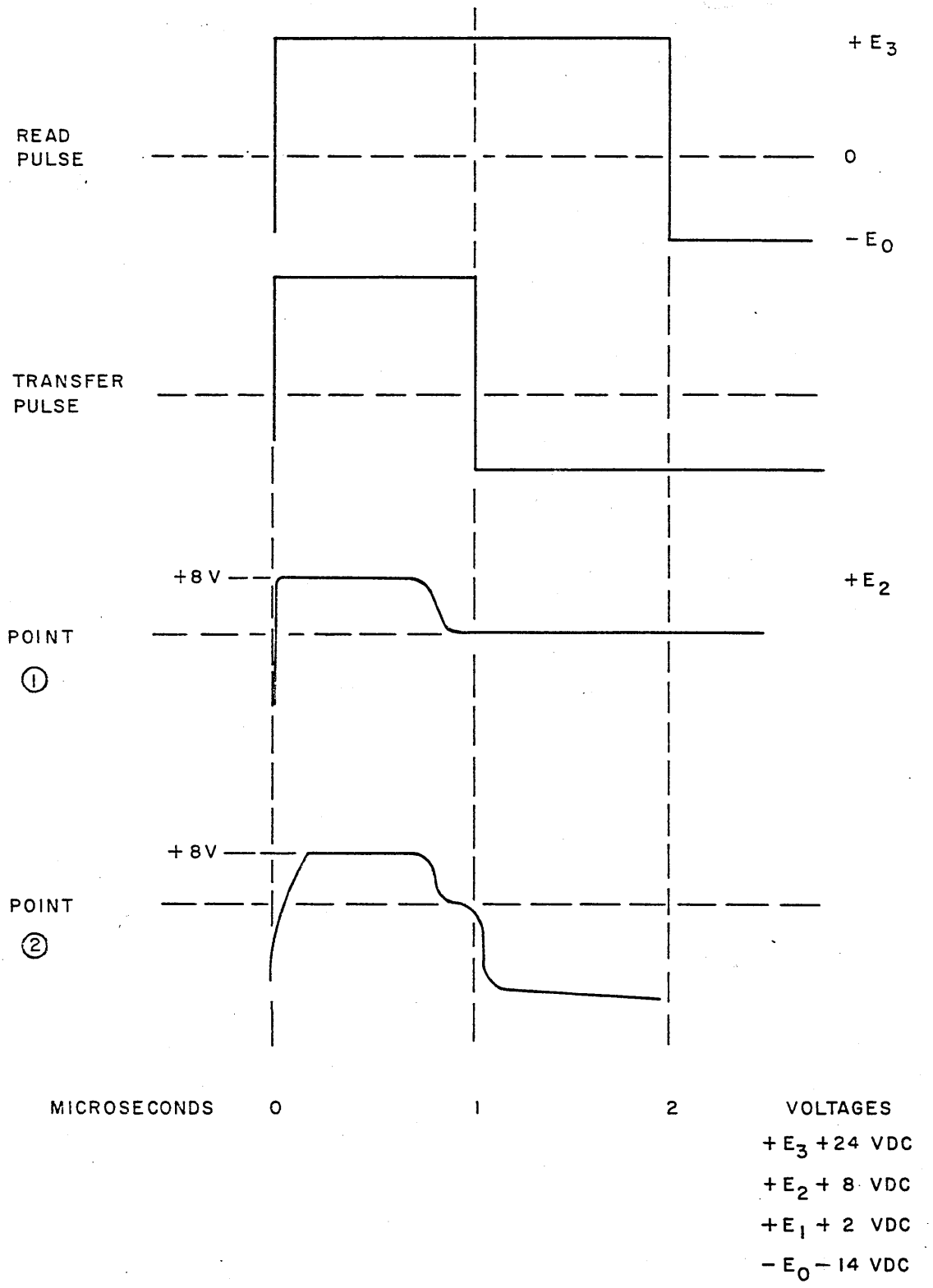

Figure 4-11. Waveforms for Basic Transfer Circuit: Transfer of a "1".

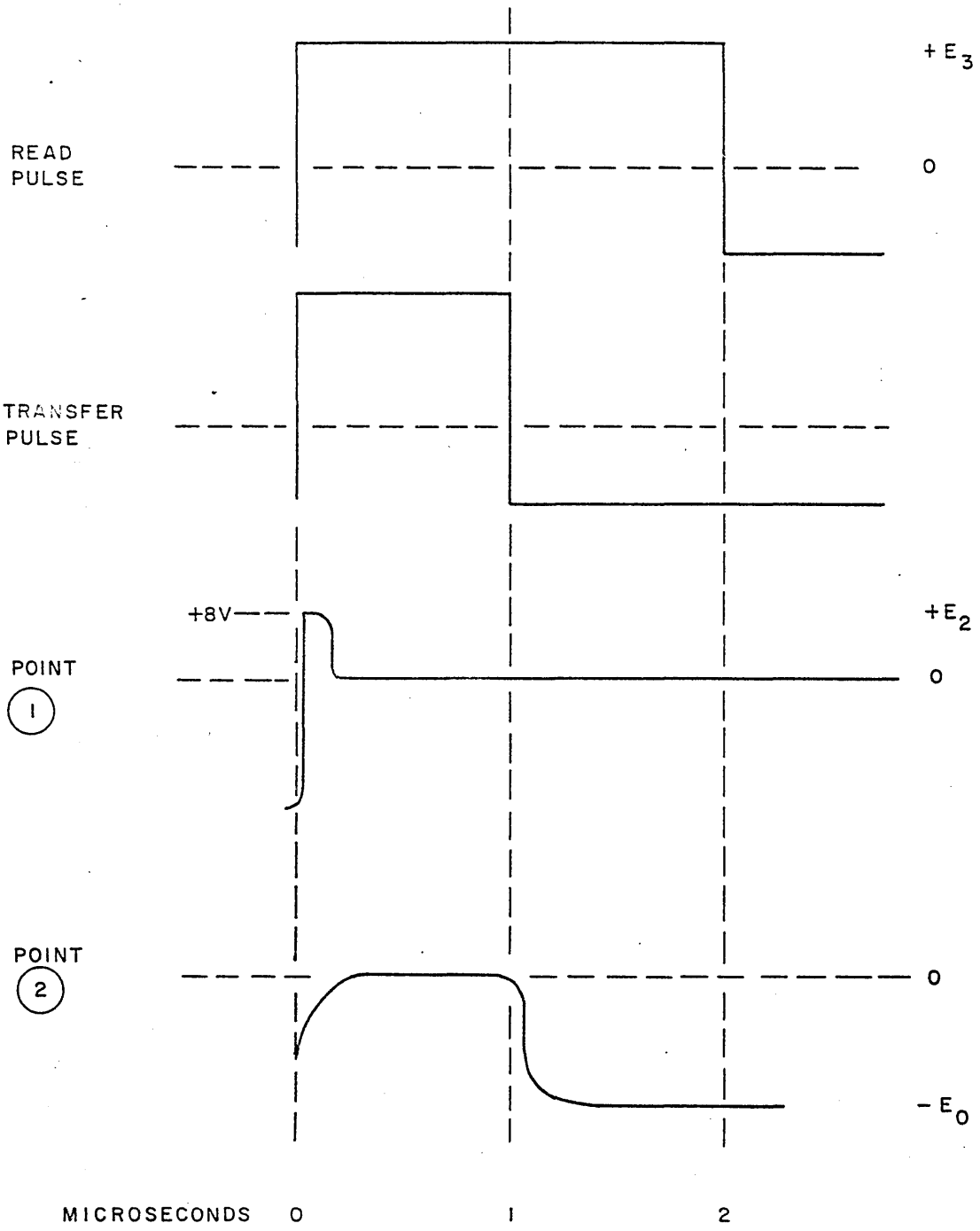

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Figure 4-12. Waveforms for Basic Transfer Circuit: Transfer of a "0".

2. CORRELATION OF EQUATIONS AND BASIC CIRCUITS. - The four-phase cycle timing mentioned previously is an integral part of the operations of each core. Each core has an assigned "read" time; i.e., it receives read pulses from a pulse distributor at only one designated time during a cycle. These Read outputs from a core become inputs to other cores at the same cycle time, or as applied to a logical equation C = f (A,B). Outputs from cores of the terms A and B become inputs to a core C according to the states of the cores of A and B and the logical operations of f (A B). Then at some subsequent assigned time, pulses as applied to a core C become Read outputs from C and inputs to other cores in the circuit. The cyclic operation of the inputs and outputs to a core C as applied to the basic circuits, C = f (A,B), is explained in the following paragraphs.

The read time of a core C is designated as time n of the cycle with the inputs being received at the times n - 1 and n - 2. The time n + 1 is reserved because the readout operation occupies two successive time periods. Therefore, the magnetic switch cannot receive any inputs for two timing periods after the beginning of its read pulse.

3. BASIC AND CIRCUIT. - The basic circuit for satisfying the logical equation

$$C = AB$$

where C, A and B represent the cores C, A, and B, respectively, is shown in Figure 4-13. In this circuit, the outputs of A and B are connected directly to the same Set input of C. This circuit can be enlarged so that up to four switch outputs can be connected in an AND union by simply soldering the output lines together.

When the basic AND circuit is used in the four-phase system, all outputs to the AND junction must occur at the same clock time. Thus the timing cycle

for the core C would be as follows:

Time	n - 2	SET INPUTS
	n - 1	SET INPUTS
	n	READ OUTPUTS
	n + 1	- - - -

The operation of the circuit shown in Figure 4-13 is as follows: 1) If both A and B contain a "1", their respective output diodes (D4) will be blocked by the emf set up in the read coils, and the TP will be forced through the set winding of C: 2) if, however, either of the input cores contains a "0", the associated output diode will not be blocked, and the TP will be shunted away from the C set winding through the read winding(s) containing the "0".

4. BASIC OR CIRCUIT. - The basic circuit for satisfying the logical transfer equation

$$C = A + B$$

where C, A, and B represent the cores C, A, and B, respectively, is shown in Figure 4-14. This circuit operates on the same principle as the basic transfer circuit, except that the transfer of a "1" to core C can be made from core A or core B, either or both transfers occurring at either of two consecutive times. Outputs from the read windings of cores A and B are connected through a crystal OR circuit to the set winding of core C.

This circuit can be enlarged so that up to four read outputs can be connected as Set inputs to the OR circuitry.

When the basic OR circuit is used in the four-phase system, the timing cycle of the switch C is as follows:

Time	n - 2	SET INPUT
	n - 1	SET INPUTS
	n	READ OUTPUTS
	n + 1	- - - -

This signifies that the OR circuit can receive one or more Set inputs during any two consecutive clock times, and that a Read output from the core must

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occur immediately after the two times reserved for the set pulses.

Each element A and B of the OR expression could be in itself an AND expression since all Read outputs from an AND equation must occur at the same pulse time.

5. BASIC AND NOT CIRCUIT. - The basic AND NOT circuit, shown in Figure 4-15, satisfies the logical transfer equation $C = AB^{-1}$ where C, A, and B represent the cores C, A, and B, respectively.

This circuit works on a four-phase time negation principle. The timing cycle for the core C would be as follows:

Time n - 2	SET INPUTS
n - 1	CLEAR INPUTS
n	READ OUTPUTS
n + 1	- - - -

The operation of the circuit shown in Figure 4-15 is as follows: 1) If A contains a "1" , C is set to "1" at time N; then 2) if at time N + 1 B does not contain a "1", C is unaltered.

The elements A and B may be AND or OR expressions if the timing restrictions previously explained for these expressions are adhered to.

Quite frequently it is desired to be able to obtain the complement of a given function. To perform this type of logical operation using magnetic switches, it is necessary unconditionally to set a switch at time n-2, then negate the switch at time n - 1 if the function is "1". If the function is not "1", then this particular switch remains set to "1". This type of circuit satisfies the following logical transfer equation: $\overline{C} = (1)\ (B)^{-1}$

(e) APPLICATION TO COMPUTER USE

1. GENERAL. - The smallest physical unit in the computer is the printed-circuit card. The majority of these cards are of the magnetic switch type, in which a magnetic switch core is mounted on a printed-circuit card, along with the crystal AND and OR circuitry associated with the set and

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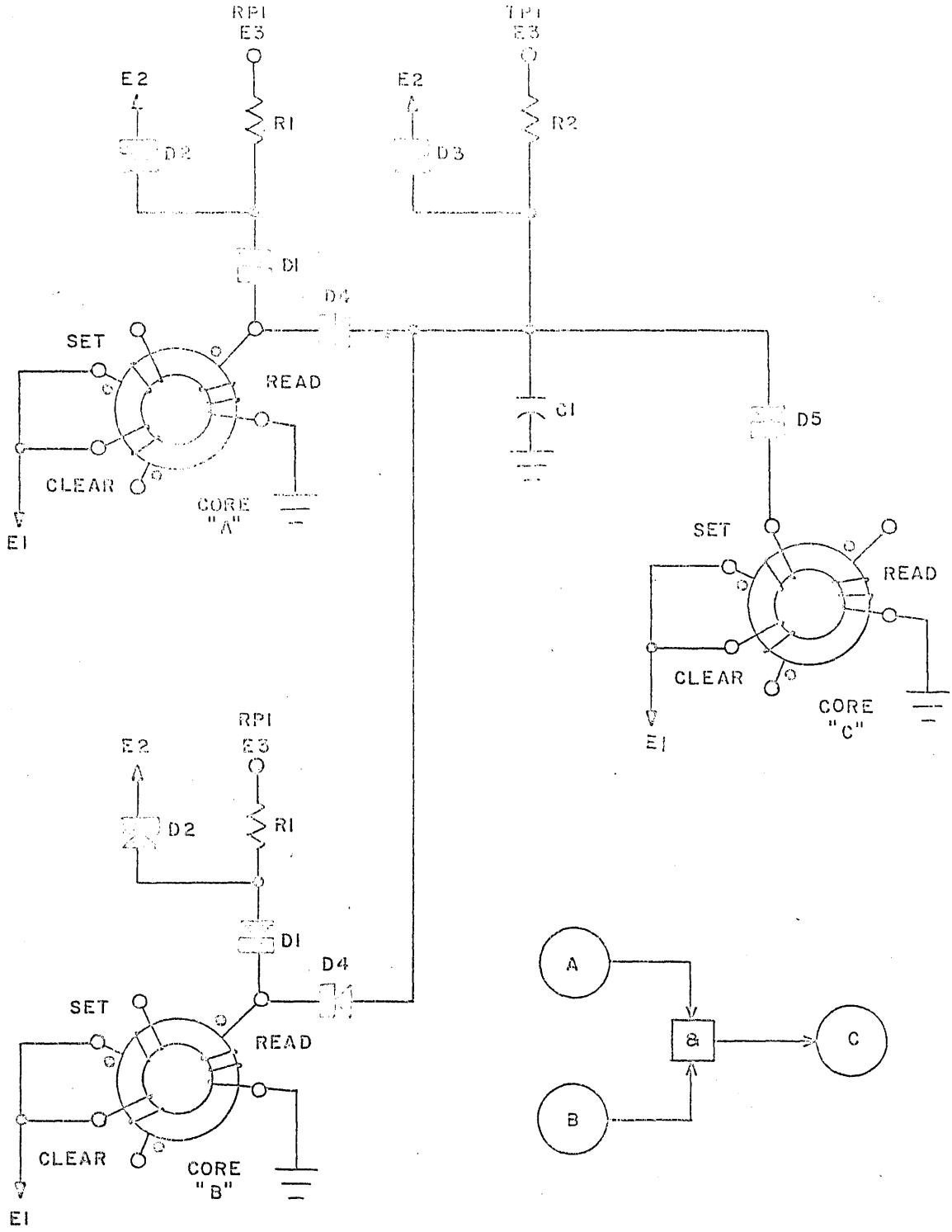

Figure 4-13. Basic AND Circuit: C = A·B

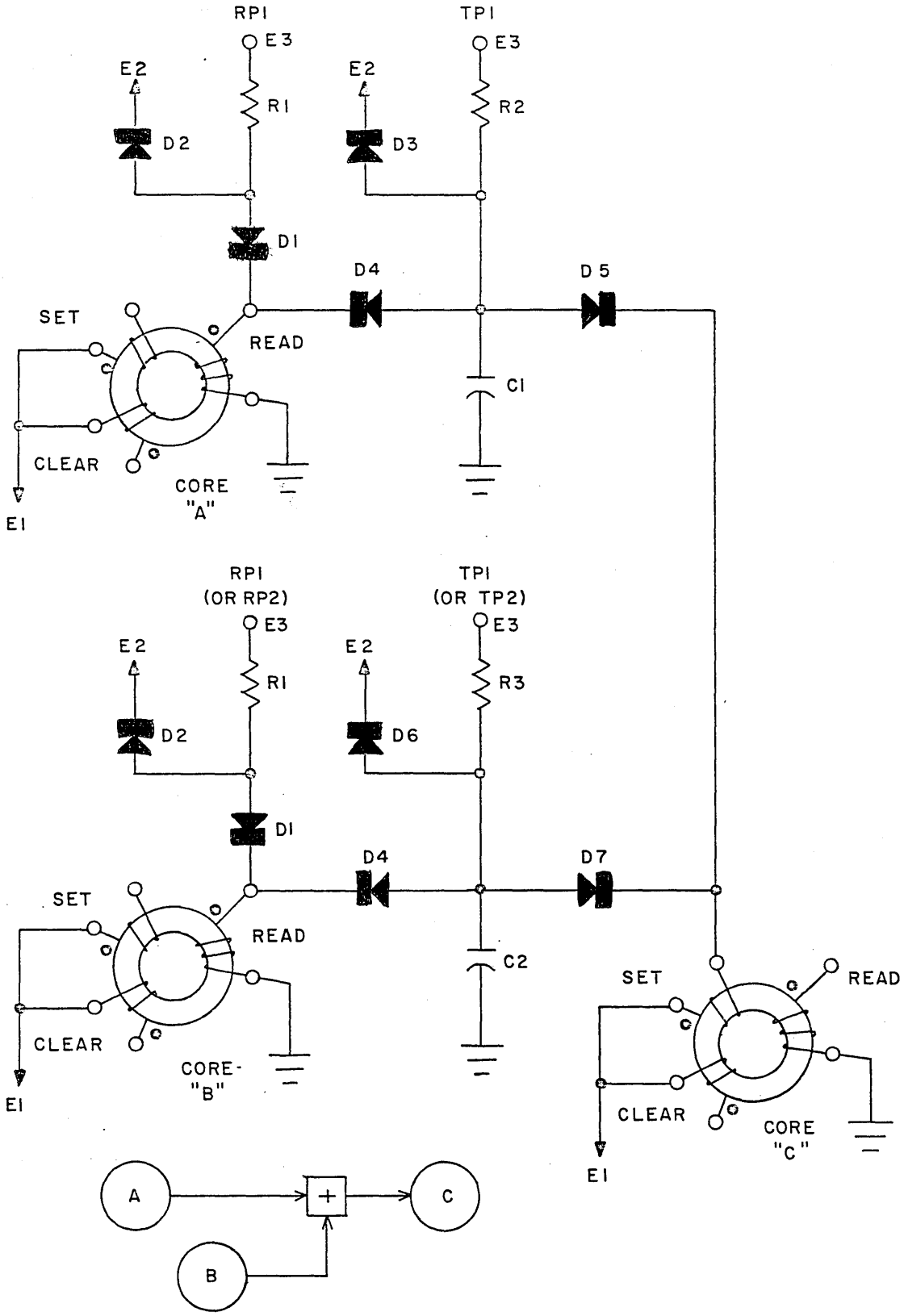

Figure 4-14. Basic OR Circuit: C = A+B

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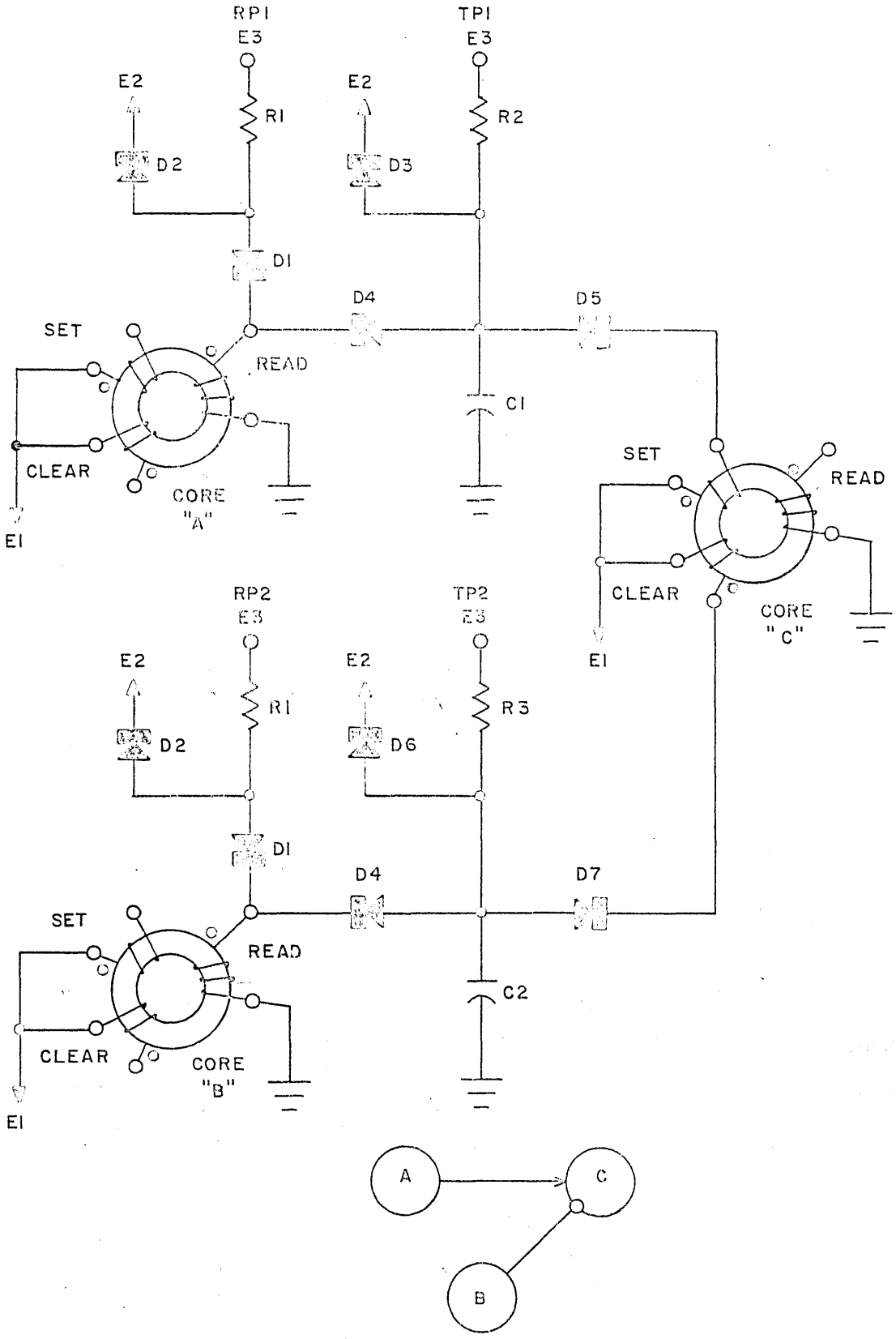

Figure 4-15. Basic AND NOT Circuit: $C = (A) \cdot (\overline{B})$

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clear inputs to the core. One edge of the card is fastened to a 15-pin connector. Thus, to form a circuit satisfying a logical transfer equation, it is only necessary to choose cards having the proper AND and OR input circuitry, plug these into a chassis containing a number of 15-pin jacks, and interconnect the jacks in the chassis.

2. PRINTED-CIRCUIT CARDS. - The magnetic switch cores, being the basic building blocks of the computer logic, are placed on standard size 2 x 2-1/2 printed-circuit cards along with associated resistors, crystals, and capacitors. On one side of the card is fastened a 15-pin connector, see Figure 4-16. Each card can have a maximum of four inputs, and each card has a total of nine inputs and outputs combined. Pins 1 to 5 are always used for output, pins 6-8 are either input or output depending on the card type, pin 9 is always used for input, pin 10 is connected to the +8 vdc power supply, pin 11 is the +2 vdc supply, and pin 12 is connected to ground. Pin 13 is used for either the clear pulse or the second tranfer pulse, pin 14 connects the first transfer pulse, while the read pulse is connected to pin 15. There are 16 different switch card types used in the computer. A typical card, type 3015, and its schematic are shown in Figures 4-16 and 4-17.

Other printed-circuit types used in the main computer chassis and in the external equipment are listed and explained in Maintenance , Volume 4, section 6.

3. CHASSIS. - The standard chassis is a 3 by 1-1/2 frame that contains 180 15-pin jacks with associated wiring and power supplies. The jacks are arranged in twenty horizontal rows and nine vertical columns. Wires with taper pin connectors are plugged into the jacks on the back of the chassis (see Figure 4-18) and the printed-circuit cards are plugged into

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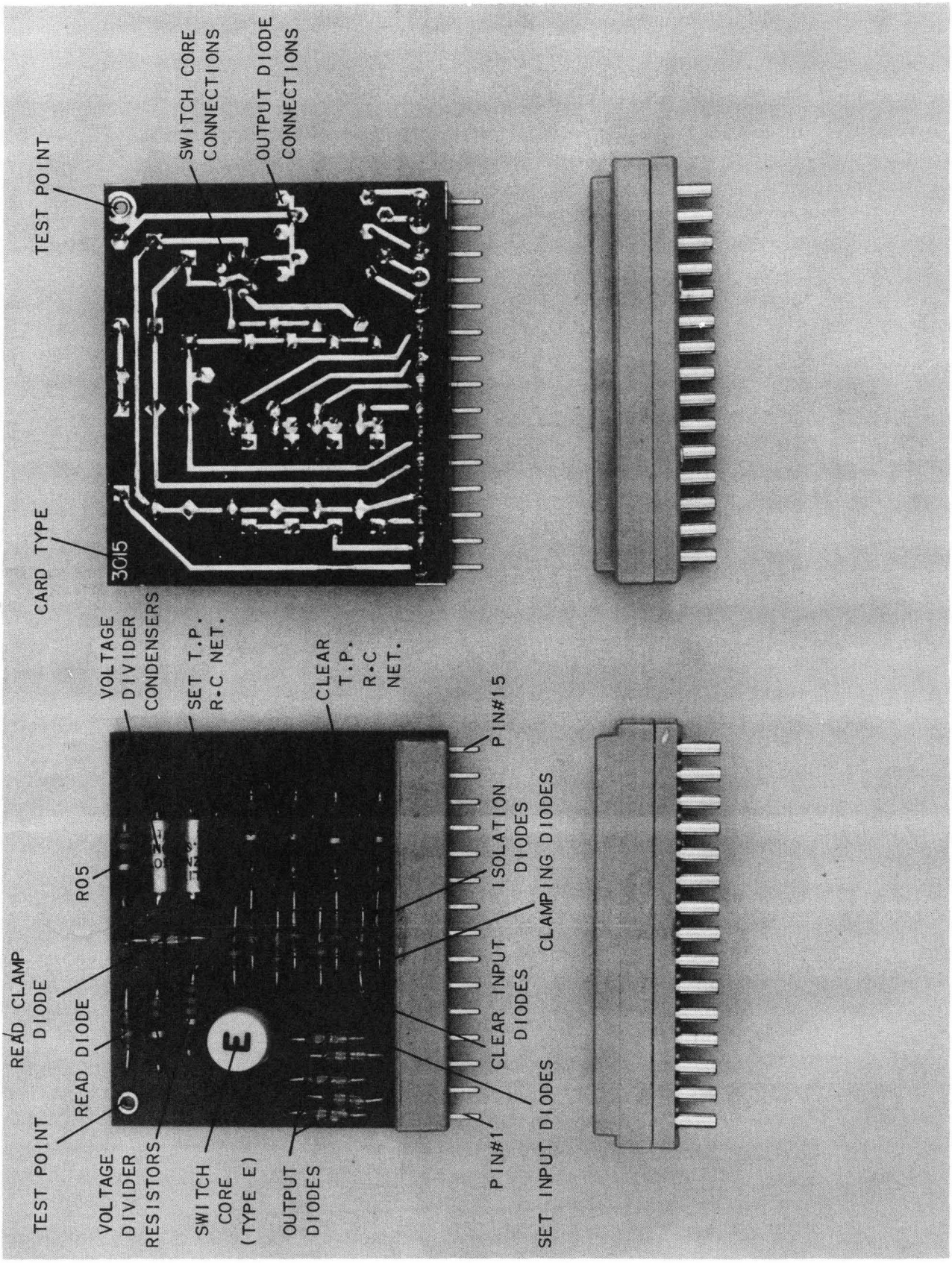

Figure 4-16. Printed Circuit Card, Type 3015

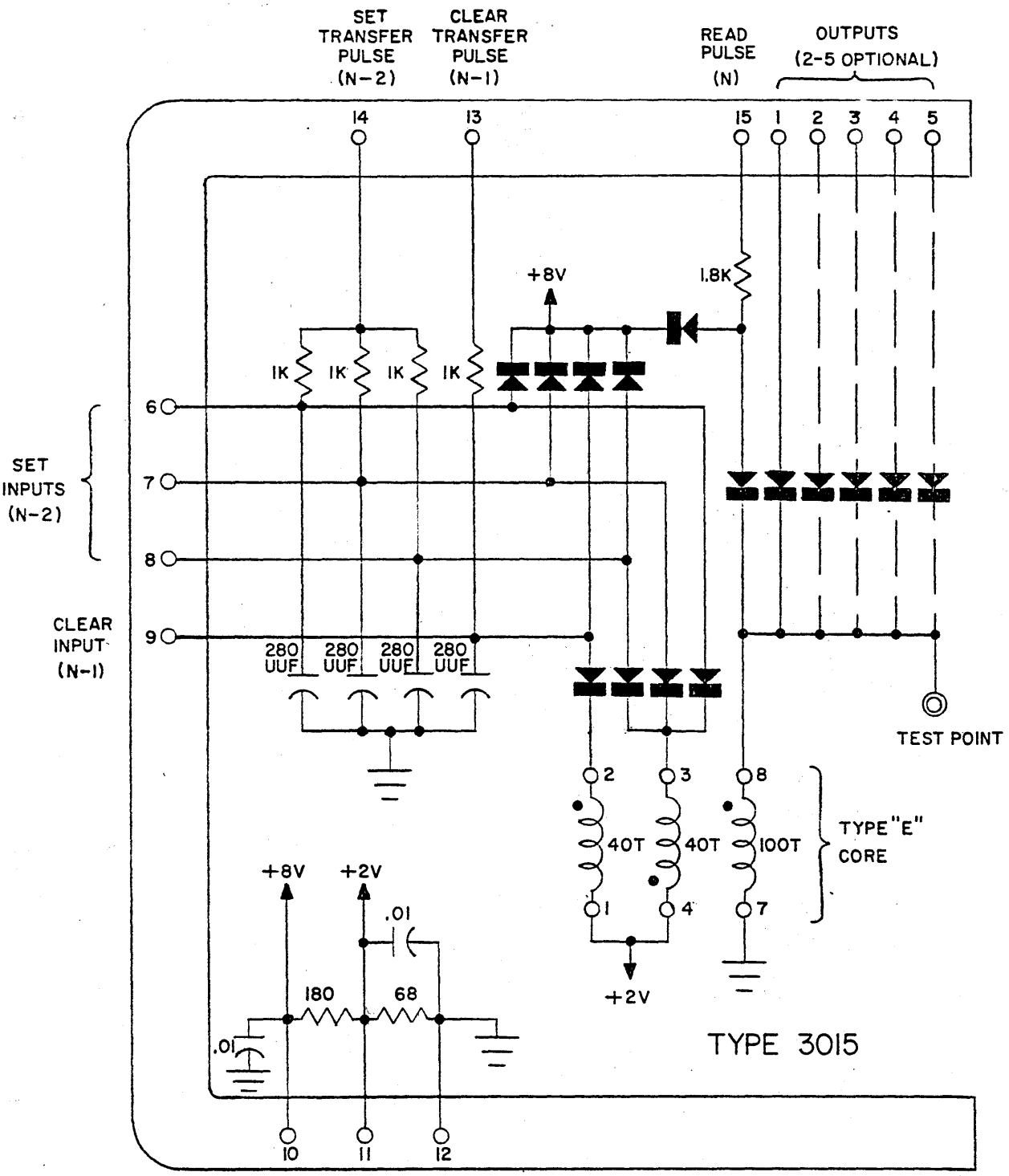

Figure 4-17. Schematic Diagram, Card Type 3015

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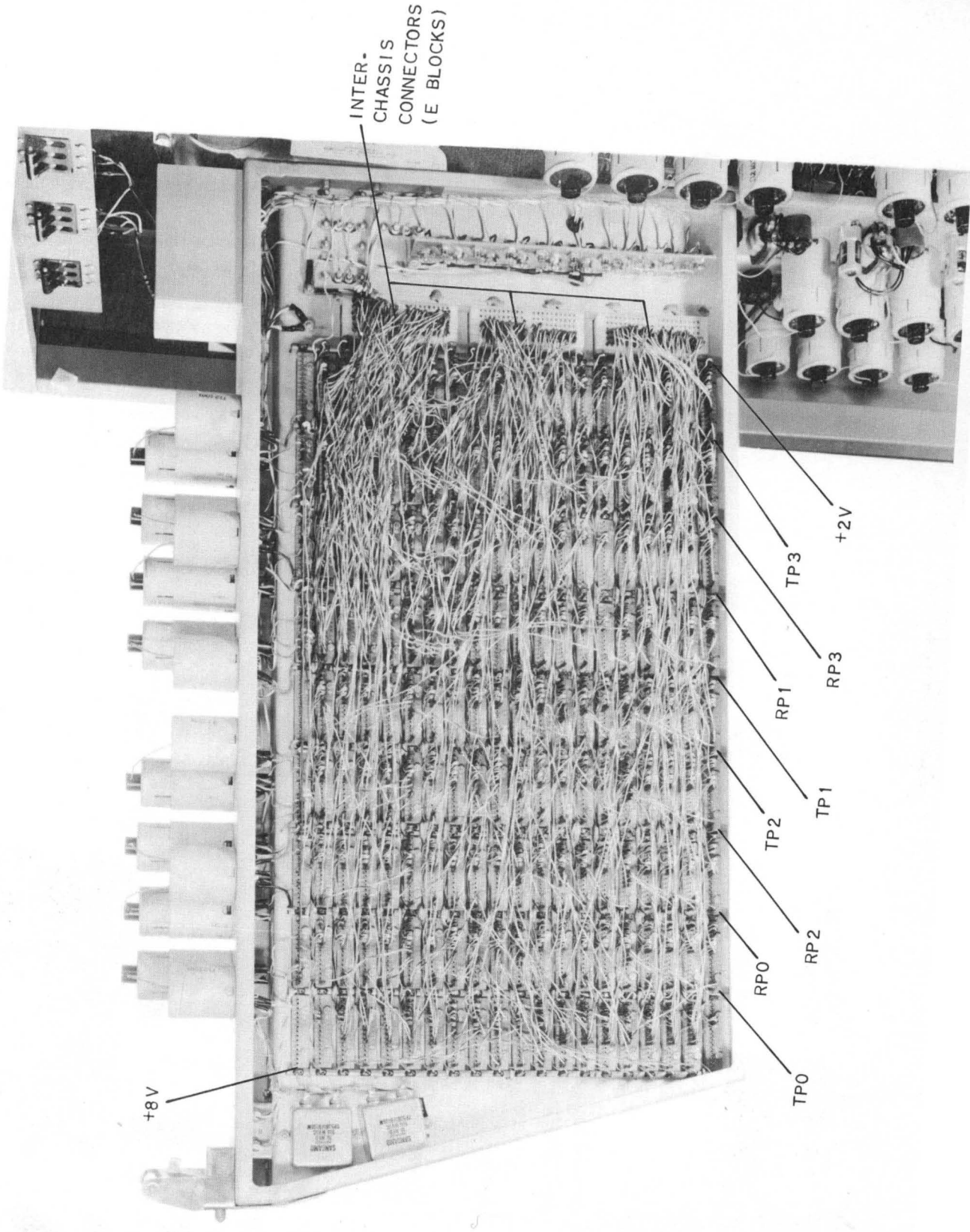

Figure 4-18. Standard Chassis, Rear View

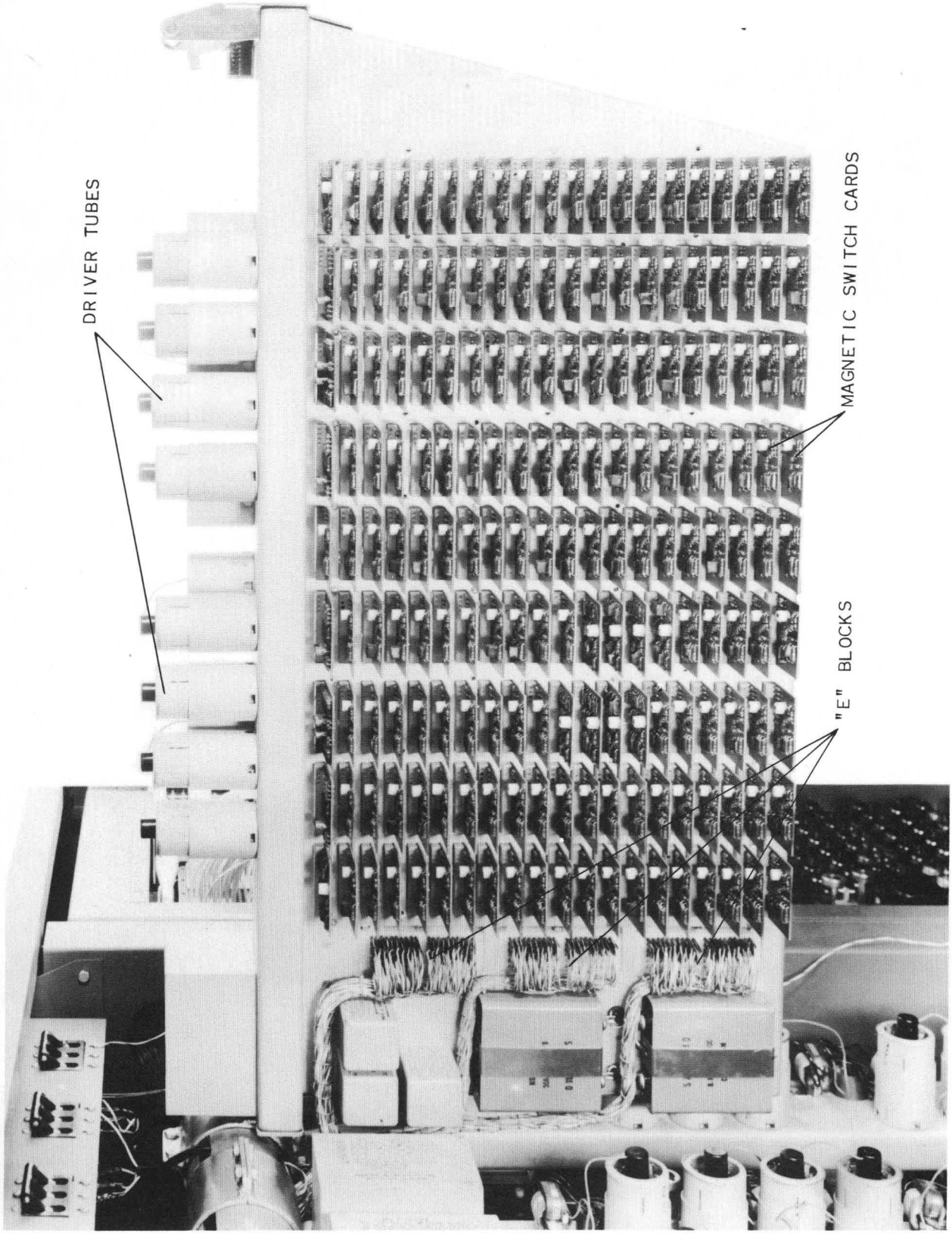

Figure 4-19. Bogart Standard Chassis (Front View)

the jacks on the front of the chassis (see Figure 4-19). The logic elements are connected by point-to-point wiring and all connections leading in or out of the chassis are terminated at E-blocks. The power supply is located on the top of the chassis.

The chassis found within the main cabinet are suspended in a vertical position from a support tube and wire duct. They are held in that position by lever latches on the bottom of the chassis. All the chassis can be manually lifted to a horizontal position when the thumb latch is released and can be held horizontally by a spring retention system, thus making all cards and taper pin connections easily accessible for maintenance. The external equipment contains various other types of chassis but all use the standard size printed-circuit cards with taper pin connectors.

d. LOGICAL ORGANIZATION. - The computer is composed of four major logical sections; the Control Section, the Arithmetic Section, the Storage Section, and the Input-Output Section. Each of these sections is further divided into logical systems which are the subjects of the principal subparagraphs. All those systems which serve as adjuncts to the logical circuitry, such as power supply, power distribution, protective interlocks and cooling system, are included in the Power and Mechanical Section.

4-2. CONTROL SECTION

a. GENERAL. - The Bogart control section is composed of the Master Clock, Program Control Register, Program Address counter, the Command Logic circuits, the Fault Detection circuits, and the Manual controls.

The Master Clock generates the read and transfer pulses which control the transfer of all information within the main machine. The Program Control Register contains the instruction to be performed and indicates how the instruction is to be modified. The Program Address Register controls the sequence

in which the instructions are to be used. The command logic circuits are the basic logic circuits used with each instruction. The fault detection circuitry recognizes a number of faults and stops the machine. The manual controls consist of the controls used by the operator when the machine is in normal use.

b. MASTER CLOCK SYSTEM. - The logic used in the Computer is controlled by a four-phase cycle system of pulses. During a cycle each pulse is given a time , denoted by 0, 1, 2, and 3. The two basic pulses used in Bogart are the read and transfer pulse. The read pulse is a square wave that is positive for two microseconds and negative for two microseconds. The transfer pulse is a square wave that is positive for one microsecond and negative for three microseconds. Figure 4-9 shows the waveforms of the pulses.

The transfer and read pulses controlling the magnetic core switches on any computer chassis are driven by a pulse driver assembly that is mounted on the same chassis. Each driver assembly produces a four-phase system of read and transfer pulses as shown in Drawing 87649; Volume 8, page 31. All driver assemblies are synchronized so that corresponding pulses coincide throughout the computer. This synchronization is achieved by connecting all driver assemblies to a single clock source.

(1) DRIVER ASSEMBLIES. - Each driver assembly produces outputs on eight lines designated as RP0, RP1, RP2, RP3, TP0, TP1, TP2, and TP3, respectively, in accordance with Drawing 87649. Each driver assembly receives inputs on lines designated as rp0, rp1, rp2, and rp3,* respectively. Thes rp signals have the form of the corresponding RP signals, but require further processing (especially amplification) before they can be used to switch cores. Similarly, unamplified transfer pulses are given tp designations in the explanation that

*Lower case read pulse designations (rp) correspond to the input pulses to the driver assemblies while upper case (RP) denotes driver assembly outputs.

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follows. Each driver assembly consists of two read pulse generators and four transfer pulse generators, as shown in Drawing 87738; Volume 11, page 8.

(a) READ PULSE GENERATORS. - Each read pulse generator (Drawing 87738) is a push-pull amplifier that receives a pair of phase-opposed rp signals from the clock and amplifies them to give the corresponding RP signals. The output transformers of both read pulse generators are pulse transformers which are special-purpose transformers that receive square-wave inputs and produce corresponding square-wave outputs.

(b) TRANSFER PULSE GENERATORS. - Each transfer pulse generator combines two successive rp inputs in an AND circuit to form one tp signal. The tp signal is then amplified to form the required TP signal. All four transfer pulse generators are shown in Drawing 87738. The operation of all four is illustrated by the TP0 generator (the V01 circuit). Diodes CR01 and CR02 comprise an AND circuit; only when both are cut off (by simultaneous positive signals at pins 1 and 3) does the control grid potential become positive to permit conduction through V01. Inspection of Drawing 87738 shows that this grid signal, representing the logical product of rp3 and rp0, is a tp0 signal. Polarity reversals in V01 and T02 mutually cancel, so the final TP0 pulses are positive.

(2) MASTER CLOCK. - the Master Clock, Drawing 87655, Volume 11, page 7, generates the basic read pulses which are converted into the final read and transfer pulses. The clock consists of a 500 kc square-wave generator, two pulse formers, and four AND blocks connected as shown in Drawing 87649, volume 8, page 31.

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The square-wave generator produces two phase-opposed 500 kc signals, as indicated in the logic diagram. (Each circled number on the diagram indicates the idealized waveform of the adjacent signal.)

Figure 4-20. Clock Timing Diagram

The pulse formers are not true flip-flops, but they act as flip-flops during normal clock operation. If input ⑦ to Pulse Former 1 is pulsed, ③ becomes positive and ⑤ becomes negative. This condition persists until another pulse at ⑦ causes another polarity reversal. Alternate pulses at ⑦ and ⑨ cause phase-opposed 250 kc, square-wave outputs to appear at ③ and ⑤.

(a) CLOCK OPERATION. - For a brief period after it is turned on, the clock is in an abnormal condition. This condition is soon corrected and the clock settles to normal operation. The explanation that follows begins by showing that normal operation is self-sustaining and concludes with an account of how normal operation is initiated.

1. NORMAL OPERATION. - Normal operation of the clock is clarified by comparison of the waveforms and diagram of Figure 4-20. Waveforms ① and ④ are combined in AND 1 to produce ⑨ . Waveforms ① and ⑥ are combined in AND 2 to form ⑦ . Application of ⑦ and ⑨ to their respective input terminals cause pulse former 1 to alternate in such a manner that waveforms ③ and ⑤ are produced at the output terminals. Comparison with Drawing 87649 shows that these outputs (at ③ and ⑤) are rp0 and rp2 signals, respectively. Similar analysis of the right-hand portion of the network shown in Figure 4-20 shows that pulse former 2 produces rp1 and rp3 signals at its ④ and ⑥ outputs, respectively.

The above paragraph describes normal operation and shows that such operation will continue if started. The account of each pulse former, however, assumes that the other is already operating properly, i.e., the account of pulse former 1 assumes that ④ and ⑥ are available; the account of pulse former 2 assumes that ③ and ⑤ are available. To complete the explanation, a description of how the clock starts is required.

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Normal operation of the clock implies only these condition:

1) rp0 and rp2 constitute a phase-opposed pair of 250 kc square-waves.

2) rp1 and rp3 constitute another phase-opposed pair of 250 kc square-waves.

3) rp1 lags rp0 by 90° (one microsecond).

Study of Figure 4-20 shows that each of the four possible modes of starting leads to normal operation as defined above.

2. STARTING OPERATION. - The following account of how the clock starts suffices to complete an explanation of clock logic. The description is simplified by overlooking some of the abnormal conditions that occur during starting. The first minute (approximately) of clock operation is more erratic than could be inferred from this account.

In the absence of signals from the pulse formers, the rp lines assume a quiescent potential that is intermediate between the extreme values of the normal rp waveforms. This starting potential partially enables all four AND blocks so that they can only feebly conduct signals from the square-wave generator to the pulse formers.

If the first pulse from the square-wave generator probes ANDs 1 and 2, it will pass with attenuation to both input terminals of pulse former 1. The pulse at ⑦ tends to drive output ③ positive, while the pulse at ⑨ tends to drive ⑤ positive. This condition of opposed inputs is unstable; one input ultimately prevails and the pulse former is switched to one state or the other.

If the pulse at ⑦ prevails so that output ③ is switched to the positive state, AND 4 becomes fully enabled while AND 3 becomes fully disabled. The next pulse ② from the square wave generator passes through AND 4, switching Output ④ of pulse former 2 to the positive state. Pulse former 2 thereupon

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fully enables AND 1 and fully disables AND 2. As a result, the clock begins normal operation.

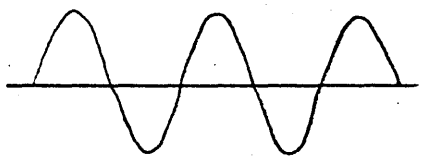
The above two paragraphs describe the initiation of normal operation, assuming the first pulse former to be switched is pulse former 1 and that output ③ of this pulse former is switched to the positive state. Neither of these assumptions is necessary; a similar analysis applies to any of the four possible cases. Normal operation ensues regardless of which pulse former is the first to be switched and regardless of which state this pulse former first assumes.

(b) CLOCK CIRCUITRY. - Operation of the clock is explained above in terms of logic blocks. The purpose of this section is to show how these blocks are implemented in electronic circuitry.

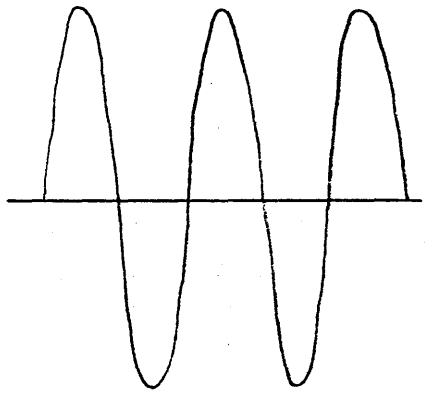
1. SQUARE-WAVE GENERATOR. - The square-wave generator includes an oscillator and a shaper. The oscillator produces two phase-opposed 500 ks sine waves. The positive loops of the sine waves are shaped to give nearly square pulses by first amplifying them so that the waveforms are very steep near the base, and then clipping off the rounded tops. Figure 4-21 clarifies this point and shows that the negative loops are not similarly clipped; the shape of the tips of the negative pulses is unimportant.

The oscillator is a type 4001 card (shown at J09B1 on Drawing 87655). The two phased-opposed 500 kc sine-wave outputs are obtained at pins 13 and 3, respectively.

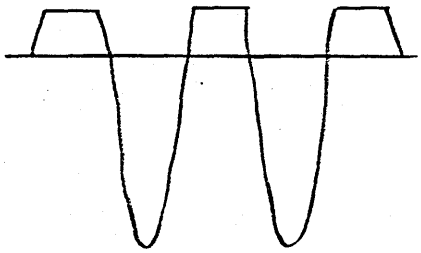
The shaper is a type 4002 card, shown at J09A1. It is explained above that shaping consists of two sequenced steps: amplifying and clipping. The shaper performs only the amplifying step; clipping takes place at each of the cards to which the shaper output is sent. The shaper consists of two one-stage triode amplifiers: V02A, which amplifies the pin-4 input, and V02B,



(a) Oscillator Output



(b) Amplified Oscillator Output



(c) Clipped Output

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Figure 4-21. Clock Oscillator Waveforms

which amplifies the phase-opposed pin-2 input. The two shaper outputs, corresponding to ① and ② of Figure 4-20, are obtained at pins 11 and 13, respectively.

2. THE FOUR AND BLOCKS. - The four AND blocks of Figure 4-20 are contained on four type 4003 cards at J09A2, J09A5, J09A6, and J09A9, respectively. It is explained above that the pin-13 input to these cards (from the shaper) requires clipping to square the positive pulses. This clipping is performed separately on each card by diode CR05.

The AND function is performed by diodes CR01 and CR02; only when both diodes are cut off (by simultaneous positive inputs at pins 13 and 14) does the potential at pin 10 become positive. The idealized pin-10 waveforms for ANDs 1, 2, 3, and 4 are ⑨ , ⑦ , ⑩ , and ⑧ , respectively, of Figure 4-20. In each case, the pin 10 signal consists of one microsecond square pulses spaced by three microseconds.

The pulse-former requires relatevely strong negative pulses to switch the state of its outputs. The pin-10 pulses are accordingly amplified and inverted by the 6AN5 tetrode before their subsequent transmission to the pulse former. This process is not indicated in the logic diagram because it includes no logical operations. The tetrode merely changes the electrical form of each pulse to make it acceptable to the pulse former. The idealized waveform at the pin-9 final output of each AND card corresponds to the pin 10 waveform, inverted.

3. THE STARTING PARTIAL ENABLE. - During normal operation, the potential at pin 14 (of each of the 4003) is either about +5v or about -35v. If it is +5v, the AND is enabled (signals can pass from pin 13 to pin 9); if it is-35v, the AND is disabled (signals cannot pass from pin 13 to 9). When the clock is first started, however, the pin-14 potential is

quiescent at -14v. This potential is the partial enable referred to above. The resulting conduction through CR01 lowers the pin-10 potential enough to reduce conduction through the tetrode, but not enough to cut it off. Thus, the first signals at pin 13 reach pin 9, but at less than normal amplitude.

(c) PULSE FORMERS. - Each pulse former includes two type 4004 cards and one pulse transformer. The explanation that follows refers to pulse former 1, but applies to both pulse formers.

1. CROSSED INPUT CONNECTION. - The connections between AND 1, AND 2, and the pulse former input terminals are shown in Figure 4-20 by a pair of crossed lines below the pulse former. Drawing 87655 shows, however, that this intersection actually occurs within the pulse former. The outputs of ANDs 1 and 2 are applied to the right and left-hand cards, respectively (pin 5 in each case). The intersection is formed by the lines that connect pin 5 (through CR01) of each type 4004 card to pin 4 of the other.

2. THE V07-V09 MULTIVIBRATOR COUPLINGS. - The plate of V07 is coupled through T03, R09 (J09A3), and CR02 (J09A3) to the control grid of V09. The plate of V09 is similarly coupled to the control grid of V07. These plate-to-grid cross-couplings account for the similarity of the pulse former to a flip-flop. A (negative) trigger pulse applied to the control grid of V07, for example, cuts V07 off so that a positive signal passes from the plate of V07 to the control grid of V09. The resulting increase in conduction in V09 causes a negative signal to pass from the plate of V09 to the plate of V09 to the grid of V07. This negative signal reinforces the trigger pulse and prolongs its effect so that V07 remains cut off and V09 remains highly conducting even after the trigger-pulse ends. The pulse former remains in this state until (one microsecond later) a trigger pulse at the grid of V09 switches it to the opposite state.

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3. INSTABILITY OF PULSE FORMERS. - Because each of the plate-to-grid cross-couplings includes a transformer link (T03), only a changing signal at the control grid of one tetrode can be conveyed (with inversion, etc.) to the control grid of the other tetrode. For this reason, the pulse former is not stable in either of the output states; it always drifts toward the quiescent state. This is the property that distinguishes the pulse former from a flip-flop; the pulse former is not bistable. During normal operation this distinction is not important because the pulse former is switched between its output states at a rate that is large in comparison with the rate at which it drifts toward the quiescent state.

The quiescent potential at the control grids of V07 and V09 is high enough (-14v) to cause both tetrodes to be overdriven. If the pulse former were allowed to remain in the quiescent state, both tetrodes would be damaged.

(3) RESYNCHRONIZING CIRCUITS. - In this and future discussions involving switch core logic, the convenient expression "X sets (core) Y" will often be used in place of the longer phrase, "core X transfers a '1' to core Y". Similarly, expressions in the passive voice, e.g., "core X is set", shall be understood to mean "a '1' is transferred to core X".

(a) THE RESYNCHRONIZING DELAY COUNTER (RDC). - The resynchronizing delay counter (RDC) sends one pulse every 128 microseconds (32 clock cycles) to various magnetic switch type resynchronizing delays (RD) controlling outputs from manual select switches, external fault lines, etc. (See Drawing 87206, Volume 8, page 32.) Two unconditionally set cores (G^{33}_{04}, G^{37}_{04}) read out every clock cycle but the 32nd, and send enabling pulses to the RD circulation bits (run, step, stop, etc.). These two cores are designated $(RDC)^{-1}$.

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During the RDC cycle, if an input signal is no longer available, the associated RD bit must be cleared. This is done by clearing the enabling cores (G^{33}_{04}, G^{37}_{04}) through RDC output cores G^{21}_{04} and G^{22}_{04} thus stopping the RD bit circulation. Functioning of the RDC is as follows:

Core G^{11}_{00} is unconditionally set, but reads out only on alternate cycles because of the negating action of G^{01}_{00}. During the first cycle G^{11}_{00} sets G^{21}_{00}, which starts its associated circulation bit (G^{01}_{01}- G^{21}_{01}). When G^{21}_{00} is set again during the third cycle it will AND with G^{21}_{01} to set G^{31}_{01}, the core controlling the second stage of the counter. G^{31}_{01} starts its circulation bit (G^{11}_{02}- G^{31}_{02}) and also clears the first stage.

Four clock cycles later (cycle 7), through action explained above G^{31}_{01} is again set; then, together with G^{31}_{02}, it sets the control core in the third stage (G^{01}_{02}). The G^{21}_{03}- G^{01}_{03} circulation bit is started at the beginning of cycle 8, and when G^{01}_{02} is set once again during cycle 15, G^{01}_{02} G^{01}_{03} will set G^{11}_{03} (stage 4 control core). This action occurs at the start of cycle 16. During cycle 32, G^{11}_{04} G^{11}_{03} sets output cores G^{21}_{04} and G^{22}_{04}, and the process is repeated.

A tabulation of action by stages, where X represents circulation and X^{-1} denotes negation, is given on page 55 for the 32 clock cycles. Cycles on which G^{11}_{00} reads out are also shown by X.

(b) RESYNCHRONIZING DELAY (RD). - Coincidence between central computer clock pulses and various asynchronous signals (manual push buttons, Resume and Respond signals from peripheral devices, etc.) is, at best, haphazard. If, for example, a Resume from a piece of external equipment were to occur at the precise moment necessary to AND with the proper clock pulse, the resultant pulse would be of sufficient magnitude and duration to perform its assigned function. On the other hand, a slight delay of the incoming signal

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Cycle	G_{oo}^{11}	1	2	3	4
1	X	X			
2		X			
3	X	X^{-1}			
4			X		
5	X	X	X		
6		X	X		
7	X	X^{-1}	X		
8			X^{-1}	X	
9	X	X		X	
10		X		X	
11	X	X^{-1}		X	
12			X	X	
13	X	X	X	X	
14		X	X	X	
15	X	X^{-1}	X	X	
16			X^{-1}	X^{-1}	X

Cycle	G_{oo}^{11}	1	2	3	4	
17	X	X			X	
18		X			X	
19	X	X^{-1}			X	
20			X		X	
21	X	X	X		X	
22		X	X		X	
23	X	X^{-1}	X		X	
24			X^{-1}	X	X	
25	X	X		X	X	
26		X		X	X	
27	X	X^{-1}		X	X	
28			X	X	X	
29	X	X	X	X	X	
30		X	X	X	X	
31	X	X^{-1}	X	X	X	
32			X^{-1}	X^{-1}	X^{-1}	OUTPUT

might, when combined with the clock pulse, result in either no output at all, or a runt pulse of decreased duration and magnitude which might or might not be able to perform its designated task.

In order to assure signals from asynchronous devices being of proper amplitude and duration, the incoming asynchronous signal is introduced into a "build-up register" (resynchronizing delay circulation bit) under the control of

a special resynchronizing pulse. The signal so introducted circulates in this resync delay until it has had time to build up to full value or decay to a negligible level. A second resync pulse issued after 128 microseconds allows the signal pulse to leave the circulation bit and proceed down its assigned path. Since most asynchronous input signals last for a period considerably greater than the interval between resync pulses, the resync circulation bit will be kept in a "1" state, as long as the input signal line is up, by the recurring resync pulses.

Such a resynchronizing device is shown in conjunction with the Selective Jumps and Stops on Drawing 87206, Volume 8, page 32.

When Selective Stop 3 switch is on (M^{-8}_{74}), and RDC output from G^{36}_{04} will AND with M^{-8}_{74} to set the associated resync circulation bit (G^{10}_{73}- G^{30}_{73}). The circulation path is enabled by the $(RDC)^{-1}$ pulses from G^{37}_{04}. The next RDC pulse from G^{36}_{04} will AND with G^{30}_{73} to produce an output which is synchronized with the rest of the clock system. Output pulses from G^{30}_{73} will continue as long as M^{-8}_{74} is up, as explained above. When M^{-8}_{74} is released, (G^{10}_{73}- G^{30}_{73}) will continue circulating until the next RDC pulse, which will clear G^{37}_{04}, thereby stopping the resync circulation bit.

In some instances it is important that only one output pulse be issued for each discrete input signal, regardless of the length of such signals. A single pulse RD of this type is shown controlling the low-speed oscillator on Drawing 87206, Volume 8, page 33. This circuit utilizes a Common Resync bit which ordinarily circulates as long as the Resync Delay bit contains a "0". Action of the circuit is as follows:

The Common Resync bit is started circulating by G^{20}_{95}, which is unconditionally set. At some point on the positive swing of the low-speed oscillator (Y^{38}_{00}) its wave coincides with the RDC pulse from G^{32}_{04} to set G^{10}_{96}. (The negation

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of G^{20}_{95} by G^{10}_{96} has no bearing on the circuit at this time, since (G^{10}_{95}- G^{30}_{95}) is already circulating.) Normal circulation of the Resync Delay bit is enabled by $(RDC)^{-1}$ pulses from G^{33}_{04}. The next RDC pulse from G^{32}_{04} and will AND with G^{30}_{95} G^{30}_{96} to set G^{00}_{96}, which emits one output pulse, and at the same time clears the Common Resync circulation bit (G^{10}_{95}-G^{30}_{95}). This circulation bit remains cleared as long as the Resync Delay bit (G^{10}_{96}- G^{30}_{96}) is circulating, thus preventing repeated output pulses from G^{00}_{96}.

When Y^{38}_{00} is no longer sufficiently positive to AND with G^{32}_{04}, the Resync Delay bit will be cleared (during the next RDC cycle) as explained above, and G^{20}_{95} will again initiate Common Resync circulation. The circuit thus is prepared for the next asynchronous input signal from the oscillator.

c. PROGRAM CONTROL

(1) GENERAL. - The program control section consists of the Program Control Register, the B-registers, the U-register adder, the P-register, the program control sequences, and the translators. The Program Control Register, generally called the U-register, contains the instruction to be executed and its modifiers. The B-registers, along with the U-register adder, are used to modify the contents of U. The P-register determines which instruction will be placed in the U-register, and the program control sequences are used to alter the step-by-step advancement of the P-register. The translators are used to indicate the values in the U-register and to set the proper controls.

(2) U-REGISTER. - The U-register (Program Control Register) shown on Drawing 87077, Volume 8, pages 24 and 25, is a 24-bit switch core register. It contains the instructions with their various modifiers and, therefore, controls all operations performed in the main computer. The U-register is composed of four sections: the instruction code, the index designator, the instruction modifier, and the base execution address sections.

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(a) INSTRUCTION CODE. - The instruction code or c, Figures 4-23, is contained in the upper six-bits of the U-register, $U_{18}...U_{23}$, see Figure 4-22. It specifies which instruction is to be executed, thus enabling the main control translator to set the proper controls for completing the instruction sequence.

1. BASIC PROPERTIES OF $U_{18}...U_{23}$. - The basic storage elements of each bit are four magnetic switch cores.

2. TRANSMISSIONS TO AND FROM $U_{18}...U_{23}$. - Before transmission to $U_{18}...U_{23}$, this section of the register is cleared by N_{36} control cores.

CORE U^{00}. - This core receives information from Z^{30} under the control of N_{33} cores. It transmits information to the Main Control Translator.

CORE U^{09}. - This core receives the complement of Z^{30} under the control of N_{33} cores. It transmits information to the Main Control Translator.

CORE U^{10}. - This core transmits its contents to the Main Control Translator.

CORE U^{30}. - The core can be set by the manual pushbutton on the indicator display panel and has an output to the indicator display lights.

(b) INDEX DESIGNATOR. - The index designator, or b, Figure 4-23, is contained in bits $U_{15}...U_{17}$. These bits determine which B-box is to be used during an instruction, see Figure 4-24.

1. BASIC PROPERTIES OF $U_{15}...U_{17}$. - The basic storate elements of each bit are three magnetic switch cores.

2. TRANSMISSION TO AND FROM $U_{15}...U_{17}$. - Before transmission to $U_{15}...U_{17}$, this section of the register is cleared by N_{36} cores.

CORE U^{00}. - This core receives information from Z^{30} under control of the N_{33} core. It has outputs to the T cores in the b translator.

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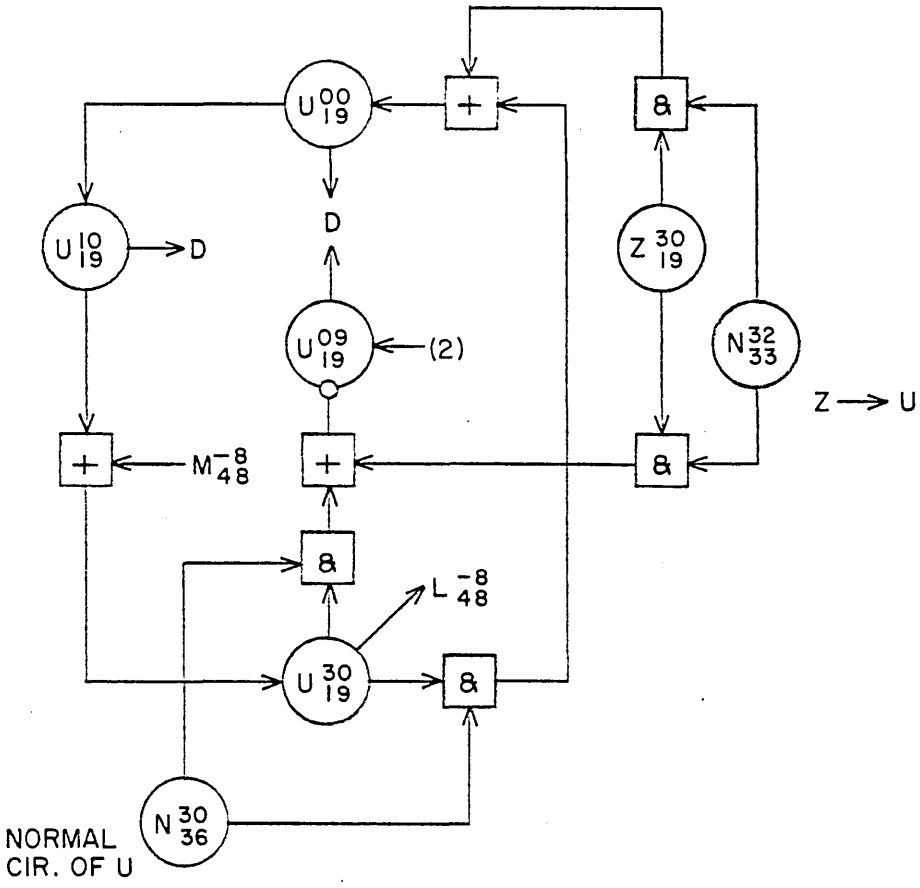

TWENTIETH STAGE OF U—REGISTER ("c")

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Figure 4-22. Twentieth Stage of U-register ("c")

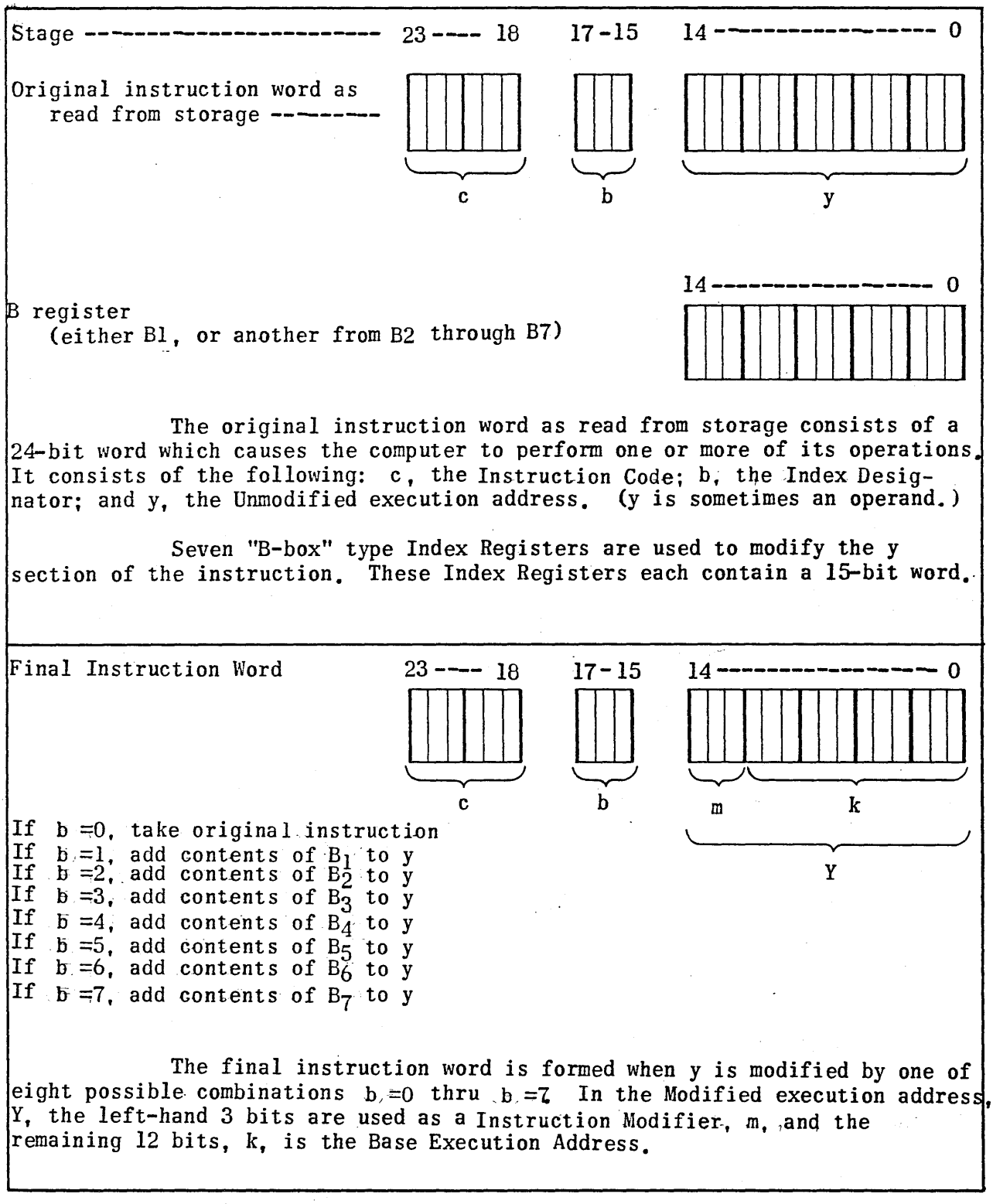
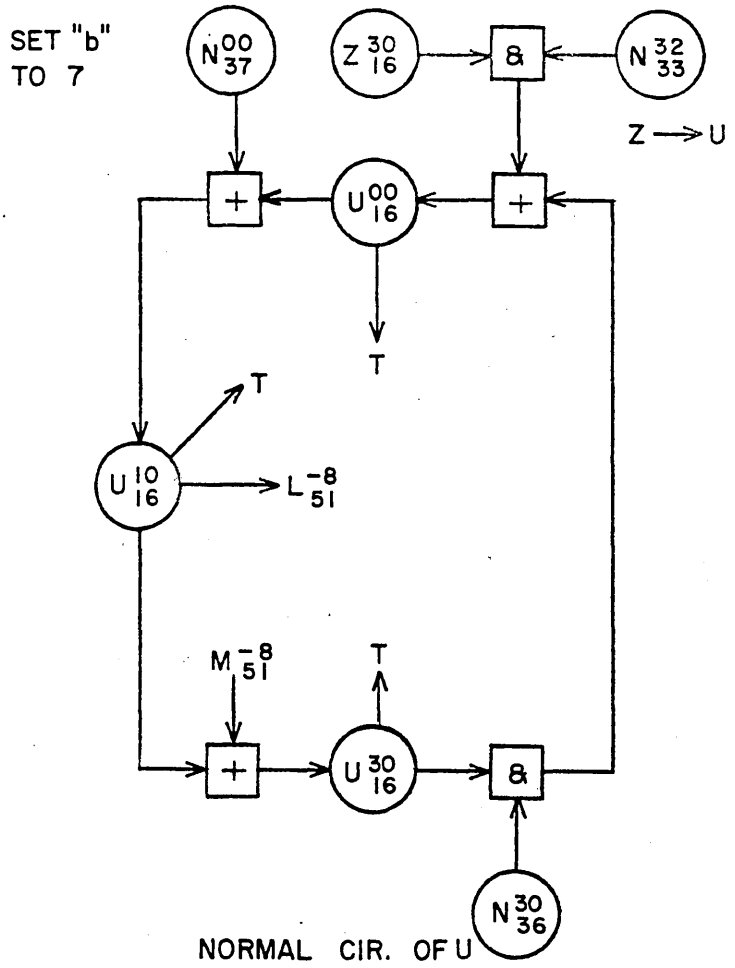


Figure 4-23. Portions Of An Instruction Word



SEVENTEENTH STAGE OF U-REGISTER ("b")

PX 804

Figure 4-24. Seventeenth Stage of U-register ("b")

CORE U^{10}. - This core receives information from Set b to 7 under the control of N_{37} cores. It also has outputs to the T cores and indicator lights.

CORE U^{30}. - This core transmits information to the T cores in the b translator, and can be manually set from the indicator display panel.

3. SET b TO 7. - The Set b to 7 control is used during the repeat instruction. The control consists of one core, N^{00}_{37}, which places a "1" in each bit of b, thus producing an octal 7.

(c) INSTRUCTION MODIFIER. - The instruction modifier, m, is contained in bits $U_{12}...U_{14}$. These three bits send information to the m translator, which in turn designates the path to be taken when an instruction has several options. The m portion can be modified by the B-boxes. When used with the base execution address, it is considered as part of a five-digit octal number with m being the highest-order bit. The five-digit number, if unmodified, is designated by y; but if the contents of a B-box were added to the fifteen bits before they were used, the five-digit number is designated by Y. A typical bit is shown in Figure 4-25.

1. BASIC PROPERTIES OF $U_{12}...U_{14}$. - The basic storage elements of each bit are four magnetic switch cores.

2. TRANSMISSION TO AND FROM $U_{12}...U_{14}$. - Before transmissions to $U_{12}...U_{14}$, this section of the register is cleared by N_{30} cores.

CORE U^{10}. - This core transmits information to the U-register adder and receives information from Z^{30} under the control of N_{33} cores.

CORE U^{20}. - The contents of X^{10} are transferred to this core under the control of N_{34} cores. Information is sent to the U-register adder, the T cores in the m translator, the V cores (second-

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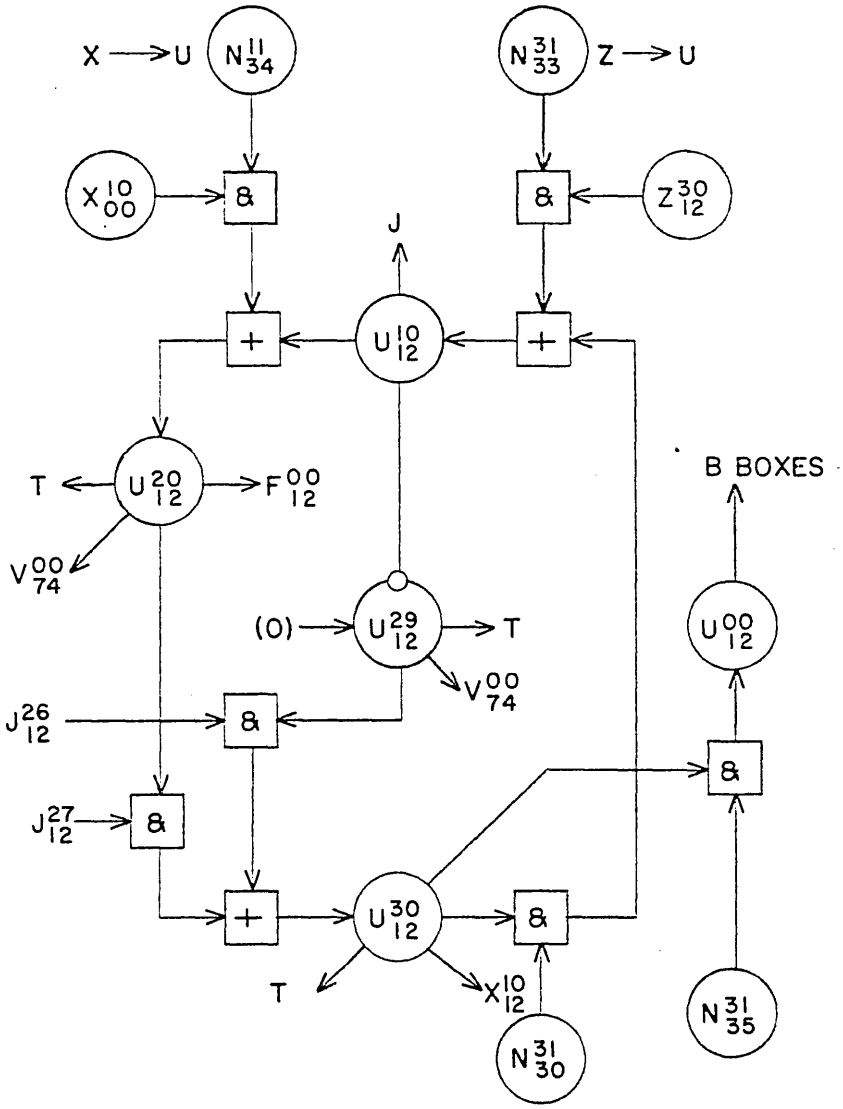

TWELFTH STAGE OF THE U-REGISTER ("m")

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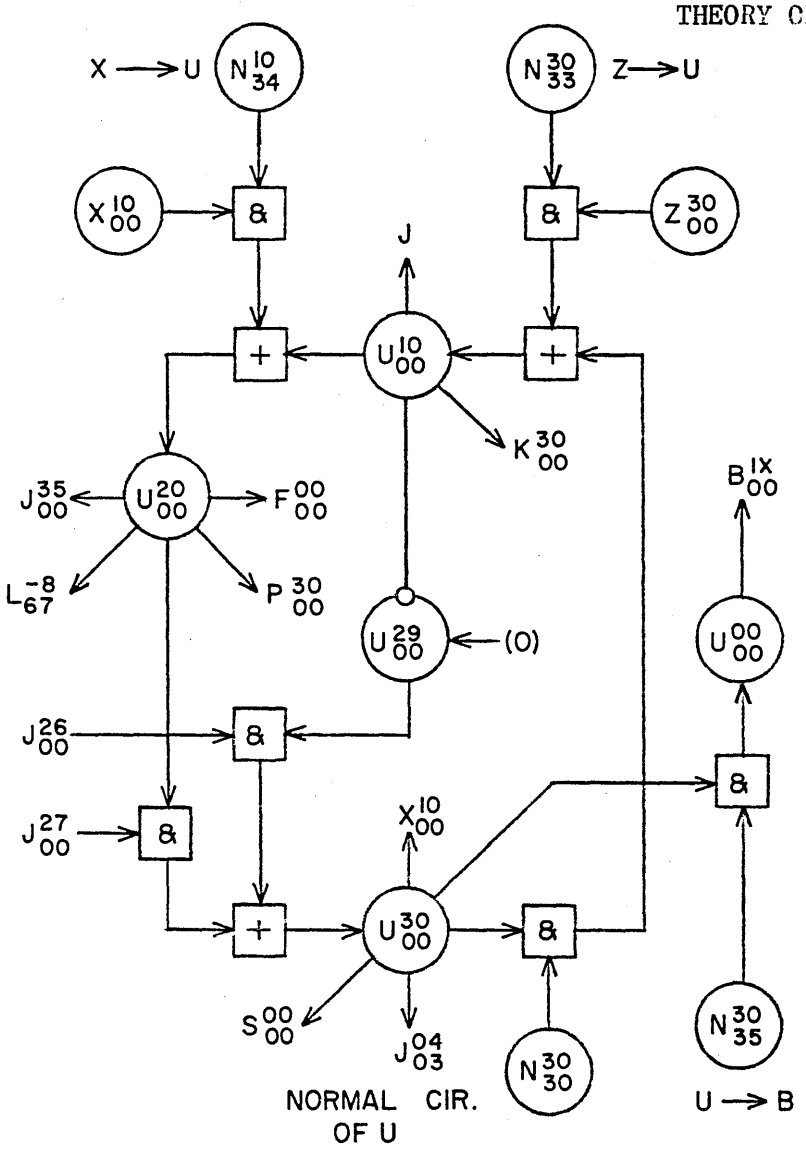
Figure 4-25. Twelfth Stage of the U-register ("m")



FIRST STAGE OF THE U-REGISTER ("y")

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Figure 4-26. First Stage of the U-Register ("y")

level control cores), and also the F-register. Transmission to F^{00} is controlled by N_{68} cores.

CORE U^{29}. - The complement of U^{10} is contained in this core. It has outputs to the m translator and second-level controls.

CORE U^{30}. - This core receives information from the U-register adder, and transmits its contents to the m translator, X-register and the B-box buffer, U^{00}. The transmission to X^{10} is controlled by N_{14}, while transmission to the B-box buffer is controlled by by N^{31}_{35}.

CORE U^{00}. - This core, acting as a B-box, receives its information from U^{30} under the control of N^{31}_{35}. Outputs from U^{00} go to B-boxes 1 through 7 under control of N_{61} through N_{67}.

(d) BASE EXECUTION ADDRESS. - The base execution address or k is contained in the lower twelve bits of the U-register, $U_{00}...U_{11}$, see Figure 4-26. This section can be modified by adding to it the contents of a B-box. During instructions involving memory, k contains the memory address which is to be used. On jump instructions, k designates the next instruction address in the program sequence. Combined with m, it is used as a five-digit octal number that can be used with many instructions. The lower six bits of k designate the number of shifts to be performed during shift instructions, and k also advances the storage address during the Load Mode sequence.

1. BASIC PROPERTIES OF $U_{00}...U_{11}$. - The basic storage elements of each bit are four magnetic switch cores.

2. TRANSMISSIONS TO AND FROM $U_{00}...U_{11}$. - Before transmissions to $U_{00}...U_{11}$, this section is cleared by N_{30} control cores.

CORE U^{10}. - This core transmits information to the U-register adder and receives information from Z^{30} under the control of N_{34} cores.

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Bits $U_{00}...U_{05}$ send information to K^{30} under control of the N_{85} cores.

CORE U^{20}. - This core receives information from X under control of N_{34} cores The contents of this register are sent to P^{30} under the control of N_{49} cores, to F^{00} under the control of N_{68} cores, and to the B-adder.

CORE U^{29}. - The complement of U^{10} is contained on this core. Its output is to U^{30}.

CORE U^{30}. - This core receives information from the B-adder and sends information to the B-boxes, U-register adder, X-register, and S-register. The transmission to X^{10} is controlled by N_{14}, the transmission to S^{00} is controlled by N_{28}, and the transmission to the specified B-box through buffer U^{00}_{00} is controlled by $N_{61}...N_{67}$ depending on the B-box designated. Core U^{30} is set manually by an input from a pushbutton on the indicator display panel (through the U-register adder).

(3) INDEX REGISTERS. - The Index Registers, more generally called B-boxes, shown in Drawing 87074, Volume 8, page 21 and Drawing 87076, Volume 8, page 23, are seven registers, each composed of 15 stages (see Figure 4-27). The B-boxes are used to store values that can be added to the m and k portions of the U-register, thus modifying the contents of m and k. B-box 7 is unique in that its lower twelve bits, $B_{7(00...11)}$, serve as a repeat counter and the upper three bits, $B_{7(12...14)}$, serve as a modifier during the repeat sequence.

(a) BASIC PROPERTIES OF B. - The basic storage elements of each bit are two magnetic switch cores.

(b) TRANSMISSIONS TO AND FROM B. - When transmissions are made to and from B, the B-box to be used is designated in the b portion of the U-

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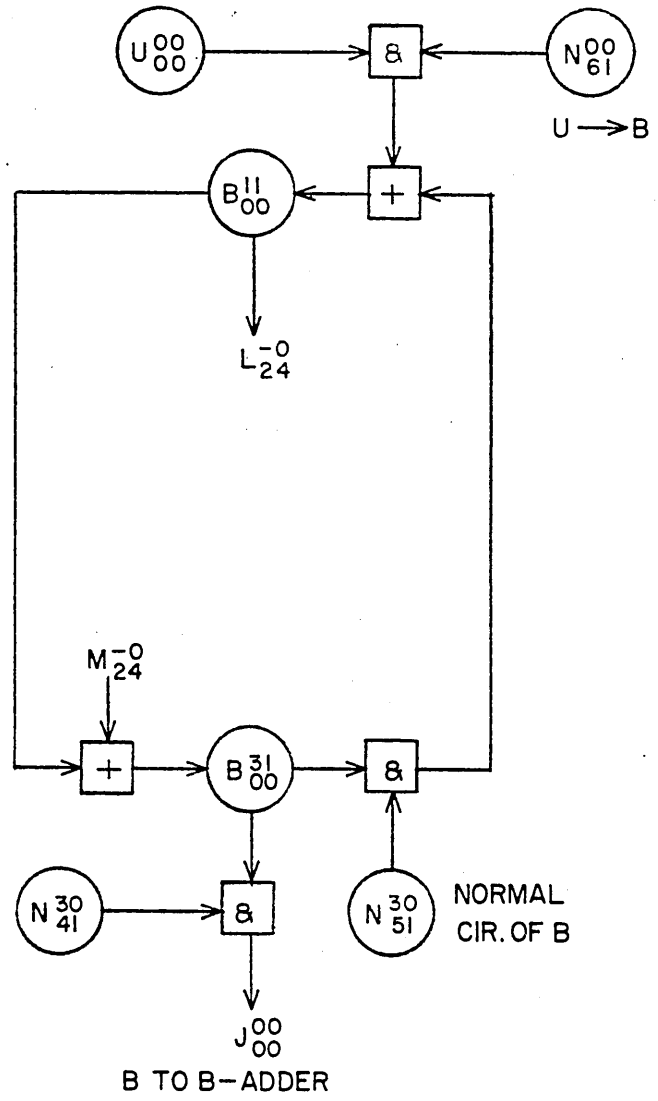

FIRST STAGE OF B-BOX ONE

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Figure 4-27. First Stage of B-Box One

register. In transmissions to B, the specified B-box is cleared by $N_{51}...N_{57}$, depending on the B-box to be used.

CORE B^{1x}. - This core receives information from U^{00} under the control of $N_{61}...N_{67}$, depending on the B-box specified.

CORE B^{3x}. - This core transmits its contents to the U-register adder under the control of $N_{41}...N_{47}$, depending on the B-box specified.

(c) B_7 REPEAT COUNTER. - The lower twelve bits of B_7 act as the Repeat Counter. Each time a repeated instruction is executed, a signal (J^{18}) is sent to B_7, which decreases the contents of the lower twelve bits of B_7 by one. This continues until the contents of $B_{7(00...11)}$ are zero. Then the B_7 repeat counter signals that the instruction has been repeated the proper number of times (V^{30}_{21} = "1"), and the program advances to the next instruction.

(d) B_7 REPEAT MODIFIER. - The B_7 repeat modifier is composed of the upper three bits of B_7, denoted as (B_7). If, during repeated instructions, the octal value of $m(B_7)$ is 0, 2, 4, or 6, the contents of U are unchanged; but if the value of $m(B_7)$ is 1 or 3, the contents of m and k are increased by one after each repeat while if $m(B_7)$ equals 5 or 7, the contents of the m and k portion of the U-register are decreased by one.

(e) B-BUFFER. - The B-buffer, J^{00} and J^{01} cores, contains the contents of the B-box designated by the b portion of the U-register. The B-buffer has its outputs to the U-register adder. The contents of the selected B-box are sent to the B-buffer under control of the N_{4x} cores.

(4) U-REGISTER ADDER. - The U-register adder, shown on Drawing 87077, Volume 8, page 26, is a two's complement adder. It is used to add the contents of a B-box to the lower fifteen bits of the U-register, to increase or decrease the contents of U during Repeat instructions, and to advance the storage address during the Load Mode sequence. In addition, the adder is used when the contents

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of U are compared to the contents of a B-box during instructions 05 and 06.

(a) U-REGISTER ADDER LOGIC. - When adding the contents of two bits, there are four possible combinations to be considered (see Example 1).

0	1	0	1
+0	+0	+1	+1
0	1	1	0 + 1 to carry

Example 1

It is noted that adding "0" to a bit does not change the content of that bit, but adding a "1" to a bit reverses the original contents of that bit. The U-register adder, following this logic, toggles* a bit of U when the corresponding bit of the B-box contains a "1". It also is noted that a "1" added to a "1" produces a carry. This carry is generated to the next higher-order bit and reverses the contents of that bit. If the bit already contains a "1", another carry is generated to its next higher-order bit and the process continues until the carry signal is applied to a bit that contains a "0". (See Example 2.)

1 0 1 0 1 1	U-register
0 0 0 1 1 0	B-box
1 0 1 1 0 1	toggle bits of U
0 1 1 1 0 0	apply carry signal
1 1 0 0 0 1	

Example 2

Each bit that has a carry signal applied to it is then toggled, thus giving the final answer. However, when a carry condition is produced in the fifteenth bit, U_{14}, the carry signal is disregarded and is not sent to any other bit.

(b) ADD B TO U. - The B-box to be added to U is designated by the b portion of the U-register. The contents of the specified B-box are sent

*The word "toggle", when used in computer logic, means "reverses the state of".

to the B-buffer (J^{00} and J^{01} cores) under control of the N_{4X} cores. Then the contents of the B-buffer are sent to the adder under control of the N_{38} cores and the bit-by-bit addition is completed. The N_{31} and N_{32} cores then sense the carry conditions and toggle the appropriate bits, thus giving the final answer.

(c) INCREASE U. - During the Repeat sequence, if $m(B_7)$ is equal to 1 or 3, the contents of the lower fifteen bits of U are increased by one each time the repeated instruction is executed. This is accomplished by adding one (N_{40}^{02} core) to the first stage of the U-register each time the repeated instruction is executed. The N_{40}^{02} core is set during Repeat sequences when $m(B_7)$ equals 1 or 3.

(d) DECREASE U. - During the Repeat sequence, if $m(B_7)$ is equal to 5 or 7, the contents of the lower fifteen bits of U are decreased by one each time the repeated instruction is executed. By adding a negative zero (all "1's") to U, the contents of U can be decreased by one since the carry condition on U_{14} is disregarded (see Example 3).

	0 1 1 0 1 0	contents of U
	1 1 1 1 1 1	add a negative zero
1	0 1 1 0 0 1	contents of U decreases by one
1	is disregarded	

Example 3

Using this logic, when $m(B_7)$ is 5 or 7, the N_{40}^{01} cores (negative zero) are added to U.

(e) COMPLEMENT U. - The lower fifteen bits of the U-register are complemented by toggling each bit of the U-register. This is done through the U-register adder by setting the N_{40}^{01} cores as in (d) above, and clearing the Enable Carry cores (N_{32}). The result is a bit-by-bit addition without carry generation, (see Example 4).

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0 1 1 0 1 0	contents of U
1 1 1 1 1 1	add negative zero without carries
1 0 0 1 0 1	

Example 4

A special feature of this complementation is that true complement of positive zero (all"0's") is a negative zero (all"1's") and vice versa.

(f) COMPARE U. - On certain instructions the contents of U are compared with the contents of a B-box. In order to do this, the contents of U are complemented and then the contents of B are added to the complement of U. However, the answer will not be correct unless U is increased by one as required by a two's complement system. Therefore, when B is compared to U, an Add One to U signal (J^{13}_{00}) is generated to produce the two's complement of the original contents of U.

(g) ADVANCE STORAGE ADDRESS. - During the Load Mode sequence, the U-register acts as the Storage Address Counter. The first address is inserted in k ($U_{00}...U_{11}$). Then, when a word is assembled in Q, k is sent to the S-register. The S-register selects the address, the word is stored, and an Add One to U signal, J^{13}_{00}, is sent to U, increasing the value of k by one. This puts the next succeeding address to be used in the k portion of the U-register.

(5) P-REGISTER. - The Program Address Counter, P, is an additive 12-stage binary counter whose principal function is to indicate the address of the next instruction. It is also used as a load check counter during Load Mode.

Information from P goes to the S-register and, in the case of return jumps, may be transferred to the Z-register for storage in memory. The logic diagram of the P-register is shown on Drawing 87075, Volume 8, page 22.

(a) BASIC PROPERTIES OF P. - The basic storage elements of each bit are two magnetic switch cores.

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1. TRANSMISSIONS TO AND FROM P. - Before transmissions to P, the register is cleared by the N_{48} control cores.

CORE P^{10}. - This core transmits information to Z^{20} under control of the N_{74} cores.

CORE P^{30}. - This core receives information from U^{20} under control of the N_{49} cores, and transmits its contents to S^{00} under the control of N_{29} cores.

2. ADVANCE P BY ONE. - The P-register is increased by one at the end of each instruction. This is accomplished by including a binary adder in the P-register.

(b) OPERATION MODE. - Whenever the computer is master cleared, the P-register is set to zero. If an address other than zero is wanted, the computer must be programmed with a jump instruction or the P-register must be manually set.

At the conclusion of each instruction, the contents of P are advanced by one unless the preceding instruction called for a repeat, skip, or jump. If this was the case, P does not read the next instruction, but reads the instruction as stated in the Program Control Sequence chapter of this section.

(c) LOAD MODE. - During the selected Load Mode operation, the Program Address Counter is not used as an address counter. Addresses are inserted directly into the Storage Address Register from the 12 lower-order bits of the U-register.

The P-register is used as the Load Check Counter during Load Mode operations. Each time the programmer uses a Check Address and the address checks, P (as the Load Check Counter) is advanced by 1.

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(6) PROGRAM CONTROL SEQUENCES. - After each instruction is executed, the P-register is advanced to the next sequential instruction unless the preceding

instruction called for a repeat, skip, normal jump, or return jump.

(a) REPEAT. - The Repeat sequence prevents the P-register from advancing until the instruction contained in U has been executed the number of times designated by B_7.

(b) SKIP. - The Skip sequence advances the contents of the P-register two places, thus skipping the next sequential instruction.

(c) NORMAL JUMP. - The Normal Jump replaces the contents of P with k, thus taking the next instruction from address k.

(d) RETURN JUMP. - The Return Jump places the contents of the P-register in memory at address k, and then changes P to + 1, thus reading the next instruction from address k + 1.

(7) TRANSLATORS. - The contents of the c, b, and m portions of the U-register are translated to determine which controls are to be used. The main translator (D and E cores) is used to translate the c portion. The b translator (T cores) indicates the value of b, and m is translated by the m translator (T cores).

(a) MAIN CONTROL TRANSLATOR. - The main control translator uses combinations of AND, OR, and NOT to set the various instruction control cores, E, corresponding to the instruction code found in $U_{18}...U_{23}$. Figure 4-28 gives an example of a similar translation using three bits of U. A "1" in U_{20} and a "1"in U_{18} will set D_{03}. Therefore, D_{03} is set on instruction 05 or 07. A "0" in U_{18} or U_{19} will set D_{02} during instructions X0, X1, X2, X4, X5, or X6.* Core D_{01} is set only during instruction X6. The AND between D_{02} and D_{03} enables E_{10} during instructions X5, X6 and X7. The complete main control translator, operating with six bits of U, uses similar logic when enabling the E

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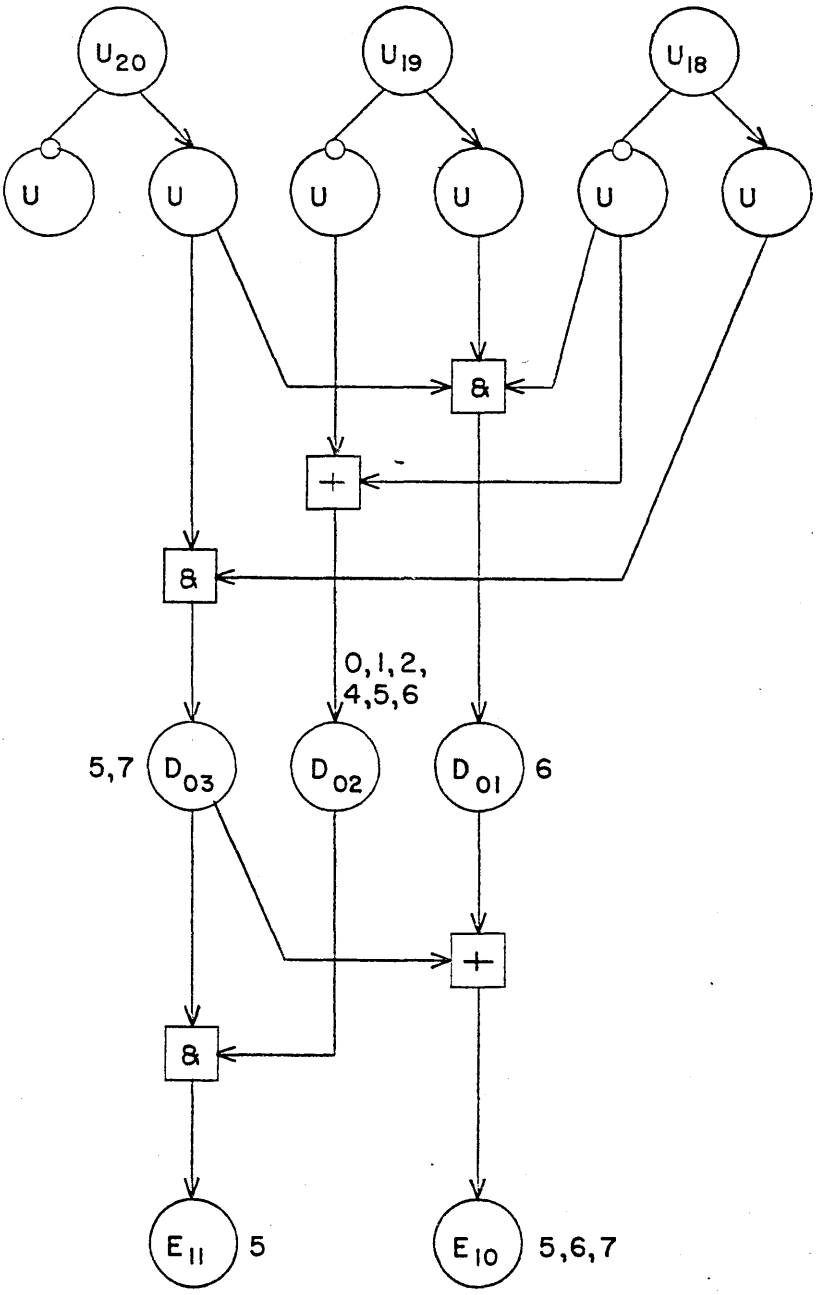
*The X designations indicate that the first digit translations are not shown on this example.



MAIN CONTROL TRANSLATOR

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Figure 4-28. Main Control Translator

cores on specified instructions.

(b) b TRANSLATOR. - The b translator, shown in Drawing 87077, Volume 8, page 27, designates which B-box is to be used and sets the appropriate controls.

(c) m TRANSLATOR. - The m translator, shown in Drawing 87077, Volume 8, page 27, interprets the value of m. The m translator (T cores) is used during read, write, jump, input, and output instructions.

d. PROGRAM CONTROL CIRCUITS

(1) FIRST-LEVEL CONTROLS CORES. - The first-level control cores, or N cores, control the transmission of information in the registers, adders, shift steps, etc. This control is shown in Example 1.

The N^{30}_{11}, N^{10}_{10} control cores enable X to circulate. When N^{30}_{14} is set, the contents of U^{30}_{00} are transmitted to X^{10}_{00}. Similarly, N^{00}_{16} enables the information in Z^{00}_{00} to be transferred to X^{10}_{00}.

The contents of X^{10}_{00} can be transmitted to U^{20}_{00} when N^{10}_{34} is set. Thus, the first-level control cores control all transmissions of information within and between the registers.

(2) SECOND-LEVEL CONTROL CORES. - The second-level control, or V cores, control the logic sequence and timing in an instruction. By following Sequence and Timing Chart 87675, Volume 9, page 2, the function of the V cores, as well as the E, N, and W cores in an actual instruction operation can be shown. Before time one, Add B to U or ABU is set, and the pulse begins circulating between W^{00}_{02} and W^{20}_{02}. The translation of instruction 01 enables the E^{20}_{01} and E^{10}_{02} translator cores to be set every fourth microsecond. At relative time one, the instruction step bit, or G^{20}_{51}, is set and the pulses from W^{20}_{02}, G^{20}_{51} and E^{20}_{01} meet the AND and set V^{00}_{16}, which in turn sends a pulse to V^{10}_{16}. The V^{10}_{16} core sets the Read Next Instruction circulation bit, negates the Repeat

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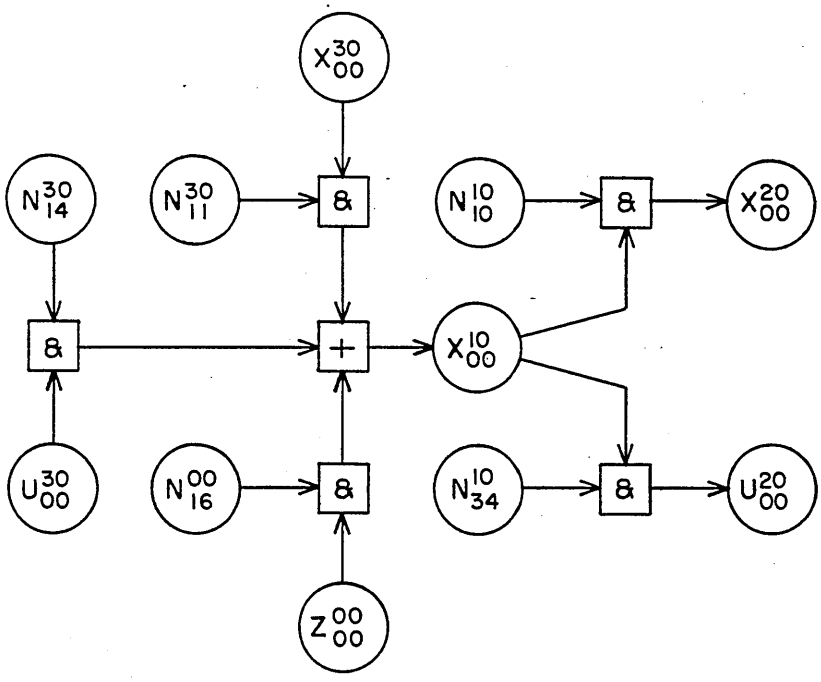

EXAMPLE I

Sequence Control, and meets the AND condition with E^{10}_{02}, setting V^{30}_{16} at relative time six. Cores V^{10}_{14}, V^{10}_{15}, and the U to B Circulation bit are set at time eight by V^{30}_{16}. Depending on the B-Box designated, V^{10}_{14} or V^{10}_{15} will AND with the T core that designates the B-box to be entered and negate the N core which controls the circulation in the selected B-box, thus blocking the transmission from B^{30} to B^{10} at time ten. Meanwhile, V^{10}_{15} also sends a pulse that satisfies the AND condition with W^{10}_{07}, clearing the U to B circulation bit and enabling the transmission of U^{00} to B^{10} at time ten. Although the first-level control cores enable all the actual transmissions throughout the machine, the second-level control

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cores are equally important because they place the transmissions of information in the right sequence at the proper time.

(3) ADDRESS MODIFICATION. - The address modification chain, shown in Drawing 87209, Volume 8, page 4, starts when a new instruction is sent to the U-register. Upon receiving the new instruction, the U-register sends information to the main control translator, the b translator, and the m modifier translator. These determine the proper control cores to be used. After the controls are selected, the designated B-box is added to U except in instructions 01, 03, 05, and 06. When these steps are completed, the instruction is ready to go through its unique sequence.

After the Z to U transmission (N_{33}^{10}), the upper six bits ($U_{18}...U_{23}$) send information to the main control translator (D cores) which in turn sets the instruction control cores (E cores) as explained under Main Control Translator.

The next three higher-order bits ($U_{15}...U_{17}$) go to the **b translator (T cores)** where they select the B-box to be used in modifying the instruction or, as in the case of instructions 01, 03, 04, and 06, they select the B-box upon which an operation is to be performed.

Finally, the next three higher-order bits go to the **m modifier** translator (T cores) where the value of m is determined. While these translations are being completed, the Add B to U circulation bit (W_{02}^{00}.. W_{02}^{20}) is set. The next instruction step sets the B to Adder Control (N_{36}), enabling the contents of the B-box specified in the instruction to go to the B-box adder. Then the Digit Carry Control (N_{31}) and Enable Carry Control (N_{32}) are set, which completes the addition of the specified B-box to the lower 15 bits of U ($U_{00}...U_{14}$). This sometimes changes the value of m, which then requires another translation.

After B has been added to U, the specified instruction follows its unique path, as designated by the E cores. Instructions 01, 03, 05, and 06 do not

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contain the ADD B to U sequence, but instead follow a special path designated by E cores immediately after clearing the Add B to U circulation bit.

Each instruction locates its unique path by sensing the conditions of the E cores associated with the address modification chain. The chain is composed of the following cores: V^{30}_{07}, V^{00}_{07}, V^{10}_{07}, V^{10}_{08}, V^{30}_{08}, V^{10}_{67}, V^{30}_{67}, and V^{10}_{68}.

For example, during instruction 13, cores E^{00}_{40} and E^{10}_{32} are set. As the instruction follows through its modification chain, core V^{00}_{07} ANDs with E^{00}_{40} setting V^{10}_{40}, which initiates the Write sequence. Further along the modification chain, core V^{10}_{07} ANDs with E^{10}_{32} setting V^{20}_{39}, which initiates the A to X sequence. The address modification continues to completion (V^{10}_{68}), but no additional sequences are initiated since all other E cores associated with the address modification chain are cleared.

(4) S-REGISTER. - The S-register, shown in Drawing 87073, Volume 8, page 20, is the 12-bit Storage Address Register. Whenever information is transferred to or from memory, it is transferred to or from the address as designated by S (see Figure 4-29).

(a) BASIC PROPERTIES OF S. - The basic storage elements of each bit are two magnetic switch cores.

(b) TRANSMISSIONS TO AND FROM S. - Before transmissions to S, the register is cleared by the N_{27} cores.

CORE S^{00}. - This core receives information from U^{30} under the control of N_{28} cores (U to S) and from P^{30} under the control of N_{29} cores (P to S). It transmits information to the address translator in memory.

CORE S^{20}. - This core receives information from the manual pushbutton on the indicator display panel.

(5) READ OPERAND SEQUENCE. - The Read Operand sequence, as shown in

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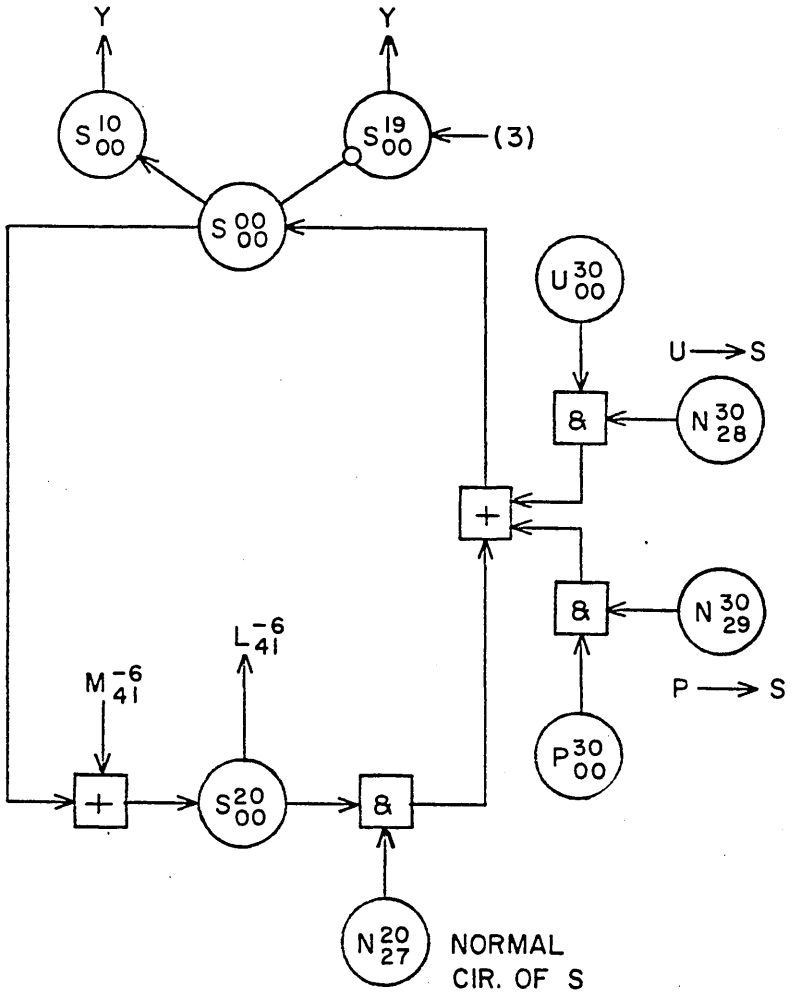

FIRST STAGE OF S-REGISTER

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Figure 4-29. First Stage of S-register

Drawing 87209, Volume 8, page 8, and Drawing 87734, Volume 9, page 113, reads an operand from memory and uses it during the instruction sequence. When memory signals it is ready to resume its read/write sequence, the contents of U containing the operand address are sent to the Storage Address Register, and the memory cycle is initiated. Memory then sends the operand, found at the specified address, to the Z-register. The Z-register in turn sends the information back to the same address in memory two microseconds later. Z then transmits its contents to X in a manner determined by the value of m. An analysis of the sequence is given below.

When the Read Operand circulation bit (W^{20}_{03}- W^{00}_{03}) and the Storage Resume circulation bit (W^{20}_{90}- W^{00}_{90}) are both set, indicating the memory sequence can be initiated, the next command step pulse will clear both circulation bits and will initiate the Read Operand sequence.

The sequence first clears the Normal Circulation Of S control (N^{10}_{27}) and sets the U to S control (N^{20}_{28}) enabling the twelve lowest-order bits of U to be transferred to S. When the address has been transmitted to S, the Storage Address Register sends information to the address translator in memory. Meanwhile, the Read Operand sequence negates the Normal Circulation Of Z control (N^{00}_{70}) clearing Z, sets the Z to X circulation bit (W^{10}_{10}- W^{30}_{10}), initiates the memory sequence, and ANDs with the Read Probe to set the Memory to Z controls (N^{20}_{75}, N^{21}_{75}, N^{22}_{75}, N^{23}_{75}). The memory sequence enables the address translator to select the correct X and Y lines as specified by S, energize these lines, read the operand at the specified address in memory, and send the operand to Z. Z in turn reads the operand back to memory during the following clock cycle. The next command step enables the Z to X transfer by clearing the Z to X circulation bit (W^{30}_{10}), clearing Normal Circulation of X control (N^{20}_{11}) and, depending on the value of m, setting the correct Z to X controls. The operand or a

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portion of it is then placed in X and the Read Operand sequence is thereby completed.

The transmission of Z to X is controlled by the following m factors.

If m = 0, use the entire 24-bit word.

If m = 1, use a 24-bit word whose lowest-order eight bits correspond to the right eight bits of the word in storage and whose higher-order bits are the same as the eighth bit.

If m = 2, use a 24-bit word whose lowest-order eight bits correspond to the center eight bits of the word in storage and whose higher-order bits are the same as the sixteenth bit.

If m = 3, use a 24-bit word whose lowest-order eight bits correspond to the left eight bits of the word in storage and whose higher-order bits are the same as the twenty-fourth bit.

If m = 4, use a 24-bit word whose lowest-order 15 bits correspond to the right 15 bits of the word in storage, and whose highest-order nine bits are zero.

If m = 5, use a 24-bit word whose lowest-order eight bits correspond to the right eight bits of the word in storage and whose higher-order bits are zero.

If m = 6, use a 24-bit word whose lowest-order eight bits correspond to the center eight bits of the word in storage and whose higher-order bits are zero.

If m = 7, use a 24-bit word whose lowest-order eight bits correspond to the left eight bits of the word in storage and whose higher-order bits are zero.

(6) WRITE SEQUENCE. - The Write sequence, as shown on Drawing 87209, Volume 8, page 10, and Drawing 87734, Volume 9, page 113, writes a new word or changes some portion of a word in memory. When memory signals it is ready to resume its read/write sequence, the portion of U containing the address of the word to be changed is sent to the Storage Address Register, and the memory cycle is then initiated. Memory sends the unchanged portion of the word to Z, and X completes the rest of Z with the changes to be made. Then Z sends the changed word to memory.

When the Write circulation bit (W^{00}_{13}- W^{20}_{13}) is set and the Storage Resume

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circulation bit (W^{00}_{90} - W^{20}_{9C} is set, indicating the memory sequence can be initiated the next command step pulse will clear both cirulation bits. This sequence first clears the Normal Circulation of S control (N^{10}_{27}) and sets the U to S control (N^{20}_{28}) enabling the twelve lowest-order bits of U to be transferred to S.

When the address is contained in S, the Storage Address Register send information to the address translator in memory. Meanwhile, the Write sequence initiates the memory cycle, negates the normal Circulation of Z control (N^{00}_{70}) and transfers X to Z in a manner determined by the value of m. The memory sequence enables the address translator to select the specified X and Y lines, energizes these lines, reads the word in storage, and sends the portion of the word that is not to be changed, designated by m, to the Z-register. Z in turn sends the changed back to the same address in memory during the following clock cycle.

The change in the word in memory depends on the following m factors.

If m = 0, write a 24-bit word corresponding to the 24-bit word in the register.

If m = 1 or 5, write a 24-bit word with the right eight bits corresponding to the right eight bits of the register and the other bits remaining the same as in the original word in memory.

If m = 2 or 6, write a 24-bit word with the middle eight bits corresponding to the right eight bits of the register and the other bits remaining the same as in the original word in memory.

If m = 3 or 7, write a 24-bit word with the left eight bits corresponding to the right eight bits of the register and the other bits remaining the same as in the original word in memory.

If m = 4, write a 24-bit word with the right 15-bits corresponding to the right 15 bits of the register and the other bits remaining the same as in the original word in memory.

(7) READ NEXT INSTRUCTION SEQUENCE. - The Read Next Instruction sequence, as shown in Drawing 87209, Volume 8, page 12, and Drawing 87734, Volume 9, page 113, reads a new instruction from memory when the preceding instruction has been completed. When memory signals it is ready to resume its

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read/write sequence, the contents of the P-register are sent to the Storage Address Register, P is advanced by one, the memory cycle is initiated, the contents of memory at the specified address are sent to Z, and then Z is transferred to U.

When the Read Next Instruction circulation bit (W^{20}_{00}- W^{00}_{00}) is set and the Storage Resume bit (W^{20}_{90}- W^{00}_{90}) is set, the next command step pulse clears both circulation bits and initiates the Read Next Instruction sequence. This sequence first clears the Normal Circulation of S control (N^{10}_{27}) and sets the P to S control (N^{20}_{29}), transferring the contents of P to S. When (P) have been transferred to S, the P-register is advanced by one (V^{20}_{12}).

Next the memory cycle is initiated, the Normal Circulation of Z control (N^{00}_{70}) is negated, and the Z to U circulation bit (W^{10}_{01}- W^{30}_{01}) is set. The memory sequence enables the address translator to select the correct X and Y lines, energize them, read the instruction in memory, and send the instruction to Z. The instruction is transmitted back to memory during the following clock cycle. If K is not zero and the shift control is set, the Z to U circulation bit waits until one of the conditions is removed and then continues the sequence. The Z to U circulation bit (W^{30}_{01}) is cleared, the Normal Circulation of U controls (N^{20}_{30}, N^{20}_{36}) are negated, and the Z to U control core (N^{10}_{33}) is set, which transfers the contents of Z to U.

(8) REPEAT SEQUENCE. - The Repeat sequence, shown in Drawing 87209, Volume 8, page 5, is sensed at the end of each instruction just before the Read Next Instruction sequence. If the Repeat Sequence Control is set ($B_7 \neq 0$) it causes the instruction to be executed again. Each time the instruction is executed, B_7 is decreased by one, and when (B_7) equals zero, the Repeat Sequence Control is cleared and the next instruction is read. It may be noted that when an instruction is to be repeated, B_7 contains the number of times

the instruction is to be repeated.

When the Repeat Sequence Control circulation bit (W^{00}_{12}- W^{20}_{12}) is set, any instruction, after performing its unique operations, sends a pulse to V^{30}_{33} and V^{30}_{19}. These cores sense the value of B_7. If B_7 is not zero, V^{30}_{33} initiates another execution of the instruction and also increases by one, decreases by one, or does not change $U_{00}...U_{14}$, depending on the value of the m portion of B_7($B^{27}_{12}...B^{27}_{14}$). Also, if B_7 is not zero, V^{30}_{19} acts through V^{00}_{23} to initiate the Back B_7 control (J^{19}_{00}) which subtracts one from B_7; but if B_7 is zero, then V^{30}_{19} clears the Repeat Sequence Control circulation bit (W^{20}_{12}) and sets the Read Next Instruction circulation bit (W^{20}_{00}- W^{00}_{00}).

(9) SKIP SEQUENCE. - The Skip sequence advances the program address by two, thus skipping the next sequential instruction following the Skip instruction. A skip is accomplished by sending two Advance P signals (V^{20}_{12}) before initiating a Read Next Instruction sequence.

(10) NORMAL JUMP SEQUENCE. - The Normal Jump sequence, shown in Drawing 87209, Volume 8, page 9, changes the address in the P-register to k, thus making the next instruction selected the instruction found at the address given in $U_{00}...U_{11}$.

If the proper conditions for the normal jump exist, the U to P circulation bit (W^{10}_{20}- W^{30}_{20}) is set. The next command step ANDs with W^{10}_{20} and sets V^{20}_{51} which clears the U to P circulation bit (W^{30}_{20}). Then V^{20}_{51} sets the V^{30}_{51} core which blocks the circulation of P by negating N^{00}_{48} (Normal Circulation of P), and also sets the N^{00}_{49} core (U to P) which transmits the contents of $U_{00}...U_{11}$ to the P-register.

(11) RETURN JUMP SEQUENCE. - The Return Jump sequence, shown in Drawing 87209, Volume 8, pages 9 and 10 stores the contents of P at address k and reads the next instruction from address k + 1.

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If the proper conditions for a return jump are present, the Write circulation bit (W^{00}_{13}- W^{20}_{13}) is set. When the Storage Resume circulation bit (W^{00}_{90}- W^{20}_{90}) is set, the next command step sets V^{30}_{43} which clears both circulation bits and sets the U to S control cores, thereby transmitting the contents of $U_{00}...U_{11}$ to S. At the same time, V^{20}_{43} clears Normal Circulation of S control core N^{10}_{27} and sets V^{10}_{43}, thus initiating the Read sequence. Two clock cycles later, the P to Z control cores N^{10}_{74}, N^{11}_{74} are set through V^{30}_{50}. Core V^{30}_{50} also sets the U to P circulation bit (W^{10}_{20}- W^{30}_{20}). The next command step pulse clears U to P (W^{30}_{20}), clears P (N^{00}_{48}), and sets the U to P control (N^{00}_{49}). Then before the next instruction is read, P is advanced by one (V^{20}_{12}).

The Trace Jump Control initiates a special return jump called Return Jump to Zero. It is similar to the return jump, except that it stores the contents of P at address 0000 and reads the next instruction from address 0001. This is accomplished by setting the Trace Jump circulation bit (W^{10}_{21}- W^{30}_{21}) which blocks the transmission of U to S and U to P.

(12) SELECTIVE STOP SEQUENCE. - The Selective Stop instruction (instruction 76) stops the computer at the completion of the instruction if certain conditions exist (Drawing 87731, Volume 9, pages 107 and 108, and Drawing 87206, Volume 8, page 32). These conditions are: m = 0 or 4 (T^{30}_{10}); m = 1 or 5 (T^{30}_{11}) and Selective Stop 1 switch; m = 2 or 6 (T^{30}_{12}) and Selective Stop 2 switch; or m = 3 or 7 (T^{30}_{13}) and Selective Stop 3 switch.

The re-sync delay pulse (G^{36}_{04}) will AND with the Selective Stop switches 1, 2, or 3 when they are in lock or momentary position. This sets the Re-sync Selective Stop 1, 2, or 3 circulations bits (G^{30}_{71}- G^{10}_{71}), (G^{30}_{72}- G^{10}_{72}), (G^{30}_{73}- G^{10}_{73}) which in turn will AND with the next re-sync delay pulse (G^{36}_{04}) to set the Selective Stop 1, 2, or 3 circulation bits W^{10}_{71}- W^{30}_{71}, W^{10}_{72}- W^{30}_{72}, or W^{10}_{73}- W^{30}_{73}. The Selective Stop circulation bits are cleared by the following $(RDC)^{-1}$ pulse.

However, when a Selective Stop circulation bit is set, the corresponding m condition is set, and the Stop instruction senses the stop conditions (V^{30}_{79}); then an Indicate Stop circulation bit (W^{30}_{80}- W^{10}_{80}), (W^{30}_{81}- W^{10}_{81}),(W^{30}_{82}- W^{10}_{82}) or (W^{30}_{83}- W^{10}_{83}) is set. Indicate Stop 0 circulation bit (W^{30}_{80}- W^{10}_{80}) is set if m = 0 or 4, regardless of the state of the selective stop switches.

Any of the Indicate Stop circulation bits initiates a Stop pulse (G^{30}_{70}). this pulse is initiated every four microseconds until the Indicate Stop circulation bits are cleared. The Stop pulse (G^{30}_{70}) negates G^{20}_{52}, thus delaying the Read Next Instruction sequence. When the Read Next Instruction circulation bit (W^{00}_{00}- W^{20}_{00}) is set, V^{10}_{82} is set. This core ANDS with the Stop pulse (G^{10}_{70}) to clear the High-Speed Register (G^{00}_{06}- G^{20}_{06}), the Instruction-Step Register (G^{00}_{05}- G^{20}_{05}), and the Command-Step Register (G^{00}_{04}- G^{20}_{04}). (See Volume 8, page 32).

(13) MASTER CLEAR SEQUENCE. - The Master Clear control, initiated by the Master Clear switch shown in Drawing 87209, Volume 8, page 15, clears all the registers and circulation bits shown on the Indicator Display panel, except for the Read Next Instruction (RNI) circulation bit (W^{00}_{00}- W^{20}_{00}), which is set by the Master Clear. The Output Resume circulation bit (W^{10}_{66}- W^{30}_{66}) and the External Function Resume circulation bit (W^{10}_{67}- W^{30}_{67}) are also set by the Master pulse, so that the first of either the Output or External Function instructions following a Master Clear does not have to wait for the Resume to be initiated.

The Load Mode switch, when in the PT Load position, also issues a Clear pulse which differs from the Master Clear only in that it does not clear the Clear Q Load Mode circulation bit (W^{00}_{98}- W^{20}_{98}) or the Load Mode Selected circulation bit (W^{10}_{99}- W^{30}_{99}), but does clear the Read Next Instruction circulation bit (W^{00}_{00}- W^{20}_{00}).

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(14) SENSE A CONTROL. - The Sense A control, shown in Drawing 87209, Volume 8, page 7, checks the A-register to determine if it is positive, negative zero, or not zero. This sequence is used to determine conditions for the A-skip instructions. However, A is also sensed during Multiply Step and during Check Address in the PT Load sequence.

(a) A IS ZERO. - When A is zero, V^{30}_{70} is set which enables V^{00}_{99}. Cores V^{00}_{99} and E^{00}_{56} (Instruction 64 or Load Mode) set Advance P (V^{20}_{12}) and clear the Repeat Sequence control (W^{00}_{12}- W^{20}_{12}).

(b) A IS NOT ZERO. - When A is not zero, V^{30}_{69} is set. This enables W^{00}_{99} (Load Mode) to set Load Check Fault (W^{10}_{42}- W^{30}_{42}), and it enables E^{00}_{57} (Instruction 65) to set Advance P and clear the Repeat Sequence control.

(c) POSITIVE A. - Positive A exists when A^{39}_{23} is set. Core A^{39}_{23} ANDs with V^{30}_{96} (step) to set V^{00}_{97} which ANDs with E^{00}_{26} (Instruction 61) to set Q to 1 (N^{20}_{18}) and initiates the Read Next Instruction sequence. Core V^{00}_{97} also ANDs with E^{00}_{54} (Instruction 66) to set Advance P and clear the Repeat Sequence control.

(d) NEGATIVE A. - Negative A exists when A^{30}_{23} is set. The negative A enables E^{00}_{55} (Instruction 67) to set Advance P and to clear the Repeat Sequence control. Negative A also enables E^{00}_{26} (Instruction 61) to set Toggle A (W^{00}_{17}- W^{20}_{17}).

(15) CLEAR A CONTROL. - The Clear A sequence, consists of clearing each bit of A. All registers are cleared before information is transmitted to them, but on certain instructions it is necessary to have A clear without immediately sending information to A. This is accomplished by using the Clear A circulation bit (W^{00}_{14}- W^{20}_{14}) which can be set only when E^{30}_{31} (Instruction 11, 12, 35, 37, 45, 47, 50, 54) is enabled. When Clear A is set, the next command step negates clear A (W^{20}_{14}) and the Normal Circulaton of A control (N^{20}_{00}), thus clearing all bits of A.

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e. FAULT DETECTION. - The main machine checks a number of operations for faults. When it senses a fault, it stops the machine. Among the faults checked are illegal instruction, illegal input or output, wrong address during Load Mode, and illegal external function code.

(1) MAIN CONTROL TRANSLATOR FAULT. - The Control Translator Fault, shown in Drawing 87206, Volume 8, page 33, indicates that an illegal instruction is contained in the U-register. E^{20}_{09} (Instruction 00, 10, 20, 30, 40, 63, 77) indicates that the c portion of the U-register contains an illegal code. When this instruction leaves the Add B to U circulation bit (W^{00}_{02}- W^{20}_{02}) it ANDs with E^{20}_{09} and sets the Main Control Translator Fault circulation bit (W^{10}_{41}- W^{30}_{41}). This in turn allows the Main Fault circulation bit (W^{10}_{40}- W^{30}_{40}) to stop the computer.

(2) INPUT FAULT. - The Input Fault, shown in Drawing 87209, Volume 8, page 33, indicates that new information was sent to the I-register before the information already in the I-register could be sent to X. If two External Select functions are programmed without an intervening Input instruction, an input fault will occur. (See Drawing 87726, Volume 9, page 95). When the Input Loaded light is down, an Input Resume negates the Normal Circulation Of I control (N^{10}_{59}), enables the External to I control (N^{20}_{69}), and sets the Input Resume circulation bit (W^{10}_{65}- W^{30}_{65}) which in turn lights the "1"indicator of the Input Loaded light (ILD). When the Input Loaded light is lit, indicating the I-register contains information not yet received by the X-register, the machine is in the Input Lockout condition. The Input Loaded (ILD) "1" indicator remains lit until a command step is initiated which negates the Normal Circulation of X control (N^{00}_{10}) and sets I to X control (N^{20}_{15}). When the contents of I have been sent to X, the Input Resume circulation bit (W^{10}_{65}- W^{30}_{65}) is cleared and the Input Loaded light is returned to the "0"condition. If an Input Resume

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is received while the (ILD) "1" indicator is lit, the Input Resume will AND with V_{90}^{00} to set the Input Fault circulation bit (W_{42}^{10}- W_{42}^{30}).

The Input Fault in turn sets the Main Fault circulation bit (W_{40}^{10}- W_{40}^{30}) which stops the machine.

(3) OUTPUT FAULT. - The Output Fault, shown in Drawing 87209, Volume 8, page 33, indicates that the external equipment sent back an Output Resume without first receiving an Output Enable. (See Drawing 87727, Volume 9, page 100.) If an Output Resume comes into the machine when the Output Loaded light (OLD) shows a "0", indicating that no Output Enable was sent to external equipment, the Output Resume will AND with V_{32}^{20} (Not Output Enable) to set the Output Fault circulation bit (W_{44}^{10}- W_{44}^{30}). The Output Fault allows the Main Fault circulation bit (W_{40}^{10}- W_{40}^{30}) to stop the main computer.

(4) LOAD CHECK FAULT. - The Load Check Fault, shown in Drawing 87733, Volume 9, page 111, and 87206, Volume 8, page 33, indicates that the information is being stored at the wrong address during the Load Mode sequence. When Load Mode calls for a check address, the address contained in the U-register must agree with the address indicated by the tape. In order to do this, the address indicated by the tape is complemented and put in the A-register. Then the contents of U are added to A and, if the sum is zero, the two addresses are identical. Therefore, when A is not zero, the addresses do not check and a Load Check Fault is indicated. When the address contained in U has been added to the complement of the address indicated by the tape, the Sense A circulation bit (W_{32}^{00}- W_{32}^{20}) is set. The next step sets V_{96}^{30} which checks the A-register. If the A-register is not zero (V_{69}^{30}), the Load Check Fault circulation bit (W_{43}^{10}- W_{43}^{30}) is set, which in turn allows the Main Fault (W_{40}^{10}- W_{40}^{30}) to stop the computer.

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(5) EXTERNAL FAULT. - The External Fault, shown in Drawing 87206, Volume 8, page 34, indicates that a low-temperature fault has occurred in the main cabinet or that an illegal external function code is present in the F-register during the External Function instruction. Since the typewriter pedestal is always included in the system package as an Input/Output device, it contains the circuitry for recognizing these illegal codes. This is accomplished by sensing the presence of more than one 1 in the three highest-order bits of the F-register.

If an External Function instruction is programmed and the highest-order octal digit position of F contains 3, 5, 6, or 7, a signal appears on the External Fault line (Y^{30}_{94}). Similarly, any of the eight low-temperature thermostats in the main cabinet will send a signal to Y^{30}_{94} when the temperature exceeds 95°F. Either of these signals sets the External Fault Resync circulation bit (G^{10}_{45}- G^{30}_{45}) which, in turn, sets the External Fault circulation bit (W^{10}_{45}- W^{30}_{45}) shown in Drawing 87206, Volume 8, page 33. The External Fault bit then turns on the Temperature Fault (TFT) light on the indicator display panel, and energizes the Main Fault circulation bit (see below), which stops the computer.

(6) MAIN FAULT. - The Main Fault, shown in Drawing 87206, Volume 8, page 33, indicates that either an external fault, output fault, input fault, load check fault, or main control translator fault has been sensed in the machine. When one of these faults is sensed, a signal is sent to the Main Fault circulation bit (W^{10}_{40}- W^{30}_{40}), which in turn issues a Fault pulse. The Fault pulse then clears the Run bit (G^{20}_{00}) and stops the computer.

f. OPERATING CONTROLS. - The manual operating controls for the main machine are located on the switch panel of the console.

(1) CONSOLE CONTROL PANEL. - The Bogart control panel is located on the console below the indicator display panel. It contains two toggle-type

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Figu
4-

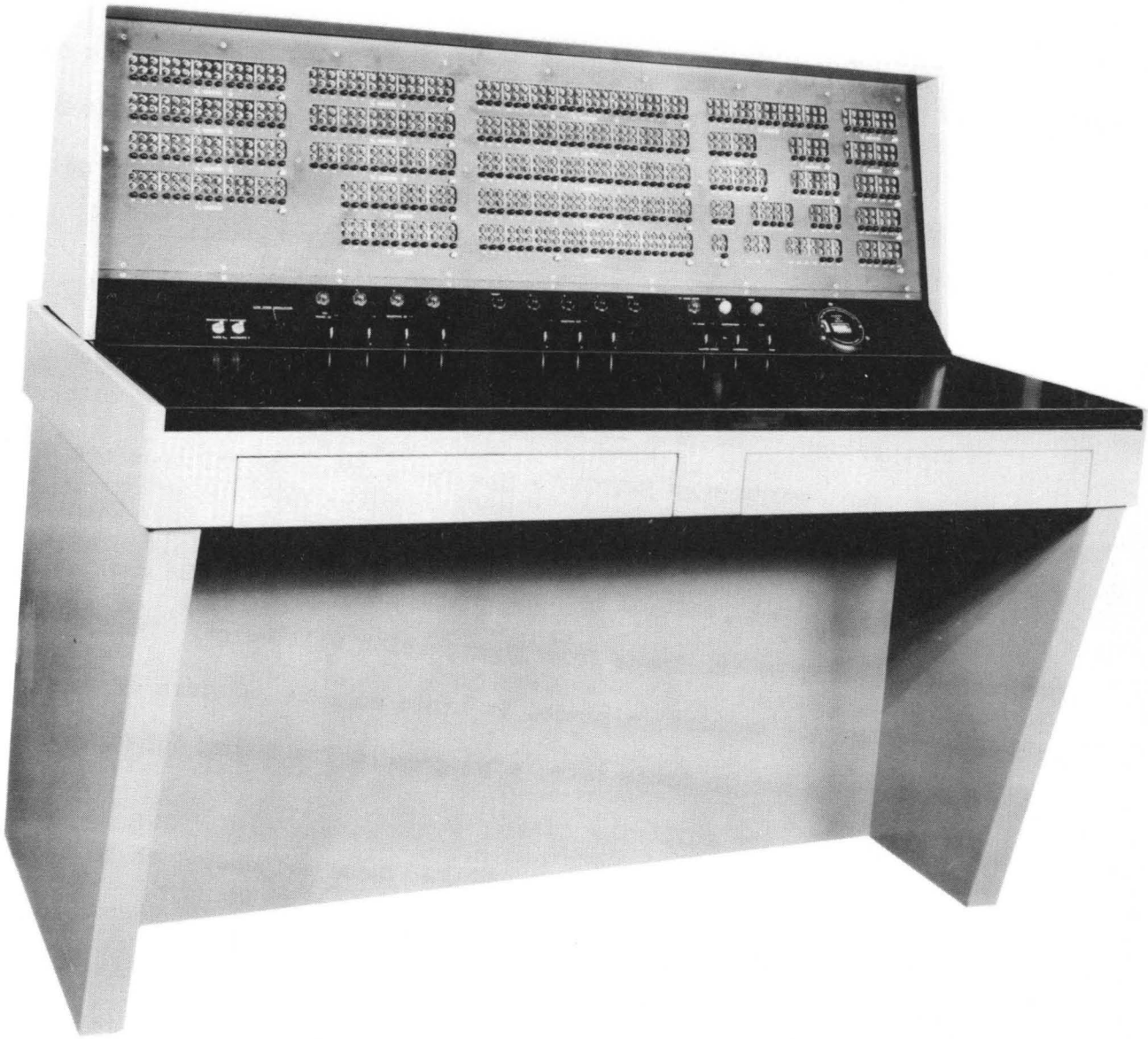

Figure 4-30. Computer Console

switches, ten lever-type three position switches, a low-speed oscillator control, a running time meter, and twelve indicator lights arranged as shown in Figure 4-30.

(a) BACK B_7 DISCONNECT. - The Back B_7 Disconnect switch, when turned on, prevents B_7 from being decreased. It is kept in the down or OFF position during normal operation and is turned ON for maintenance reasons only.

(b) ADVANCE P DISCONNECT. - The Advance P Disconnect switch, when turned on, prevents P from being advanced. It is kept in the down or OFF position during normal operation and is turned on for maintenance reasons only.

(c) LOW-SPEED OSCILLATOR. - When the machine is not in the high-speed mode, the low-speed oscillator controls the frequency of command or instruction step pulses. The rate is increased by turning the control clockwise.

(d) TRACE JUMP SWITCH. - The Trace Jump control consists of a lever-type three-position switch with an indicator light above it. When the switch is in the up-lock position or down-momentary position, the machine is in trace mode indicated by the Trace Jump light, which will be on. The first jump instruction after the machine is placed in trace mode is a Return Jump to Zero. When the machine is not in trace mode, a programmed Trace Jump (instruction 73) has no effect on the following jump.

(e) SELECTIVE JUMP SWITCHES. - These switches lock in the up position, are momentary in the down position, and are off in the normal position. When a switch is on, the corresponding indicator light is lit. During Selective Jump (instruction 75), if m=1 or 5 and Selective Jump 1 is on; m=2 or 6 and Selective Jump 2 is on; or m=3 or 7 Selective Jump 3 is on a jump will be executed.

(f) FAULT LIGHT. - When a fault is sensed by the computer, the computer stops and the Fault light turns on.

(g) SELECTIVE STOP SWITCHES. - These switches lock in the up position, are momentary in the down position, and are off in the normal position. During Selective Stop (instruction 76) if m=1 or 5 and Selective Stop 1 is on; m=2 or 6 and Selective Stop 2 is on; or m=3 or 7 and Selective Stop 3 is on, the machine stops and the corresponding light is turned on.

(h) STOP LIGHT. - During Selective Stop (instruction 76) if m=0 or 4, the machine stops and the Stop light is turned on.

(i) PAPER TAPE LOAD AND MASTER CLEAR. - This switch is locked in the PT LOAD or up position, momentary in the MASTER CLEAR or down position, and off in the normal position.

1. PAPER TAPE LOAD. - The up or lock position is the PT Load mode. In this position the computer is prepared to accept coded paper-tape inputs. The PT Load switch issues its own Master Clear signal.

2. MASTER CLEAR. - The down or momentary position is the MASTER CLEAR position. This switch issues a signal that sets all registers and circulation bits to zero, except for the Read Next Instruction, Storage Resume, Output Loaded and External Function Loaded bits. The RNI bit remains set so that the computer will read the next instruction when restarted.

(j) HIGH-SPEED/INSTRUCTION/COMMAND SWITCH. - This switch is locked in both the up and down positions.

1. INSTRUCTION STEP. - The up-lock position is the Instruction Step mode of operation. During this mode, whenever the Step switch is actuated, the computer executes the instruction, reads the next instruction, and stops until the Step switch is actuated again. If the Run switch is on, the computer goes through instruction steps under the control of the low-speed oscillator.

2. HIGH-SPEED. - The center, normal position is the HIGH-SPEED position. When the Run switch is actuated in this mode of operation the computer proceeds at high speed until the next programmed stop or until the Step switch is activated. When the Step switch is momentarily placed in the down position, the computer continues in the High-Speed mode but stops after the execution of the instruction in control.

3. COMMAND STEP. - The down-lock position is the COMMAND STEP position. In this mode of operation the computer executes the next command when the Step switch is depressed. If the Run switch is actuated, the computer is pulsed through the commands by the low-speed oscillator.

(k) RUN/STEP. - This switch is momentary in both the up and down positions.

1. RUN. - The up-momentary position is the RUN position. The action of this switch is dependent upon the computer's present mode of operation.

2. STARTING OPERATION. - The machine is started by placing the switch in the RUN position. If the high-speed switch is in the High-Speed mode of operation, actuating the Run switch causes the computer to proceed at high speed. During Instruction Step and Command Step modes of operation, the computer will be stepped through the instruction steps or command steps by the low-speed oscillator. After starting, subsequent movement of the switch to the RUN position has no effect on the operation of the computer.

3. STEP. - The down-momentary position is the STEP position. The action of this switch is also dependent upon the computer's present mode of operation.

4. FORCE STOP. - The computer, regardless of the mode of operation, can be stopped by momentarily placing the Step switch in the down

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position. The computer continues in operation until it has completed the next unit of operation and then comes to a stop. In the case of High-Speed and Instruction Step modes, the computer stops after the execution of the instruction in control. If the Step switch is pressed again, the computer executes one more instruction and stops. This process is repeated each time the Step switch is actuated.

In the Command Step mode of operation the computer stops after completing the present command that is being executed. Each time the Step switch is pressed, the computer executes another command step of an instruction and stops.

(1) RUNNING TIME METER. - This meter, calibrated in tenths of a second, records the machine's operating time. It has a modulus of 10^4 - .1 seconds.

(2) INDICATOR DISPLAY PANEL. - The indicator display panel shows the condition of all the registers and command bits. The conditions are shown by pairs of neon lights; the upper light, when on, indicates the bit contains a "1", and the lower light indicates the bit contains "0". The black pushbuttons insert a "1" in the corresponding bit, while the white pushbuttons clear the corresponding bits or groups of bits. The display panel is mainly for maintenance and register information.

(3) INTERLOCK PRECAUTIONS. - When the computer is in the Run mode (Run light on), the pushbuttons on the indicator display panel are inoperative. The relay which lights the Run light also disconnects the +8V supply from the indicator display panel pushbuttons. The High-Speed/Instruction/Command and PT Load/Master Clear switches on the control panel are also inoperative when the computer is in the Run mode.

g. OPERATING CONTROL CIRCUITS. - These circuits control operations in the main computer and are shown in Drawing 87206, Volume 8, pages 32-34.

(1) BACK B_7 DISCONNECT CONTROLS. - When the Back B_7 switch is placed in the up-position (M^{-6}_{02}), it negates the V^{30}_{31} core preventing the logical AND from setting the V^{00}_{23} core which issues the Back B_7 signal. Thus, when this switch is up, the contents of B_7 are not decreased.

(2) ADVANCE P DISCONNECT CONTROLS. - When the Advance P switch is placed in the up-position (M^{-6}_{03}), it negates the V^{00}_{13} core preventing all three logical ANDs which could set the V^{20}_{12} core. If the V^{20}_{12} core is not set, P cannot be advanced, and the contents of the P-register remain unchanged.

(3) LOW-SPEED OSCILLATOR CONTROLS. - The low-speed oscillator controls permit one pulse to be sent to the Run controls each time the oscillator becomes positive.

The Common Re-sync circulation bit (G^{10}_{95}- G^{30}_{95}) is set by G^{20}_{95} whenever the Re-sync Low-Speed Oscillator circulation bit (G^{10}_{96}- G^{30}_{96}) is not set. The resync delay pulse (G^{32}_{04}) forms an AND with the positive phase of the low-speed oscillator (Y^{38}_{00}) to set the Re-sync Low-Speed Oscillator circulation bit (G^{10}_{96}- G^{30}_{96}). This bit remains set until the output of the low-speed oscillator goes negative.

The Re-sync Low-Speed Oscillator circulation bit and the Common Re-sync AND with the next re-sync delay pulse (G^{32}_{04}) to set G^{00}_{96}. The G^{00}_{96} core negates the Common Re-sync circulation bit which cannot be re-set until the Re-sync Low-Speed Oscillator circulation bit is cleared.

The G^{00}_{96} core also sets G^{20}_{96} which initiates the low-speed oscillator pulse.

(4) TRACE JUMP CONTROL. - The Trace Jump control consists of a three-position lever switch. When the switch (M^{-6}_{00}) is either in the up or down position, it will AND with the re-sync delay pulse (G^{32}_{04}) to set the Common Re-sync circulation bit (G^{10}_{30}- G^{30}_{30}). The next re-sync delay pulse then ANDs with the Common Re-sync bit (G^{30}_{30}) and sets the Trace Jump Re-sync circulation bit (G^{30}_{31} - G^{10}_{31}). This bit sets the Trace Jump indicator light (Y^{11}_{77}), sends one pulse

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to the Trace Jump circulation bit (W^{10}_{21} - W^{30}_{21}) thus setting it, and also sets the G^{00}_{32} core during every clock cycle. The G^{00}_{32} core has an output to the Main Control Translator which enables the Trace Jump instruction (73) to set the E^{30}_{85} core. This core enables the Trace Jump instruction to set the Trace Jump circulation bit at the end of each Trace Jump instruction.

When the Trace Jump switch is put in the normal position, both the Common Re-sync circulation bit (G^{10}_{30} - G^{30}_{30}) and the Trace Jump Re-sync circulation bit (G^{10}_{31} - G^{30}_{31}) are cleared by the re-sync delay pulse (G^{21}_{04}). The Trace Jump instruction, therefore, does not set the Trace Jump circulation bit when the Trace jump switch is in the normal position.

(5) SELECTIVE JUMP CONTROL. - The Selective Jump controls are shown in Drawing 87206, Volume 8, page 32. Since all three switches have similar logic, it is unnecessary to trace the logic of switches two and three. When switch one is in the up or down position (M^{-8}_{81}), it ANDs with the re-sync delay pulse (G^{39}_{04}) and sets the Re-sync Selective Jump 1 circulation bit (G^{10}_{61} - G^{30}_{61}). This circulation bit ANDs with the next re-sync pulse (G^{39}_{04}) and sets the Selective Jump 1 circulation bit (W^{10}_{61} - W^{30}_{61}). The Selective Jump 1 circulation bit turns on the light on the indicator display panel (L^{-8}_{81}), but the light on the switch panel is connected directly to the Jump 1 switch. When the Selective Jump switch is in the normal position, the Re-sync Selective Jump 1 and Selective Jump 1 circulation bits are cleared when the re-sync delay pulse negates G^{35}_{05}, thus interrupting normal circulation.

(6) FAULT CONTROLS. - The Main Fault circulation bit (W^{10}_{40} - W^{30}_{40}) lights both the FLT light (L^{-8}_{93}) on the indicator display panel and the Fault light (Y^{10}_{99}) on the switch panel. It also sends a fault pulse which negates the step (G^{20}_{02}) pulse and run (G^{20}_{00}) pulse. It also sets G^{30}_{12} which negates the High-Speed Register (G^{00}_{06} - G^{20}_{06}), the Instruction Step Register (G^{00}_{05} - G^{20}_{05}), and the

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Command Step Register (G^{00}_{04} - G^{20}_{04}).

(7) SELECTIVE STOP CONTROLS. - The Selective Stop controls are shown in Drawing 87206, Volume 8, page 32. Since all three switches have similar logic, it is unnecessary to trace the logic of switches two and three. When switch one is in the up or down position (M^{-8}_{76}), it will AND with the re-sync delay pulse (G^{36}_{04}) to set the Re-sync Selective Stop 1 circulation bit (G^{10}_{71} - G^{30}_{71}). This bit (G^{30}_{71}) ANDs with the next re-sync delay pulse (G^{36}_{04}) and sets the Selective Stop 1 circulation bit (W^{10}_{71} - W^{30}_{71}) which in turn sets the ST1 light (L^{-8}_{76}) on the indicator display panel. If a Selective Stop (instruction 76) is programmed and m = 1 (T^{30}_{11}), these conditions AND with the Selective Stop 1 circulation bit, setting the Indicate Stop 1 circulation bit (W^{10}_{81} - W^{30}_{81}). This bit lights the Stop 1 light (Y^{10}_{81}) located on the switch panel and sends a stop pulse (G^{30}_{70}) to the Run controls. When Read Next Instruction (V^{10}_{82}) is enabled, it ANDs with the stop pulse clearing the High-Speed Register, the Instruction Step Register, and the Command Step Register, thus causing the computer to stop. This sequence is shown in Drawing 87206, Volume 8, page 33.

(8) PAPER TAPE LOAD CONTROLS. - The Paper-Tape Load control issues a Master Clear and enables the machine to receive inputs from punched paper tape.

The normal position of the Load Mode switch completes an AND with the re-sync delay pulse (G^{32}_{04}) to set the Common Re-sync PT Load Clear circulation bit (G^{10}_{97} - G^{30}_{97}) which in turn ANDs with the next re-sync delay pulse (G^{34}_{04}) to set PT Load Clear circulation bit (W^{10}_{97} - W^{30}_{97}).

The PT Load position (G^{30}_{98}) of the Load Mode switch forms a logical AND with the re-sync delay pulse (G^{34}_{04}) to set the Re-sync PT Load circulation bit (G^{10}_{99} - G^{30}_{99}). This bit completes an AND with the next re-sync delay pulse to set the PT Load circulation bit (W^{10}_{99} - W^{30}_{99}) which enables the controls for paper tape loading. The PT Load Clear (W^{30}_{97}) and the Re-sync PT Load (G^{30}_{99})

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AND with the re-sync delay pulse (G^{32}_{04}) to set G^{00}_{97}. The G^{00}_{97} core issues a Master Clear, sets the Clear Q Load Mode circulation bit (W^{00}_{98}- W^{20}_{98}), and negates the PT Load Clear circulation bit.

The PT Load (W^{30}_{99}) and the Common Re-sync PT Load Clear (G^{30}_{97}) AND with the re-sync delay pulse (G^{34}_{04}) to set G^{00}_{99}, clearing the PT Load circulation bit, the Command Step Register (G^{00}_{04}), the Instruction Step Register (G^{00}_{05}- G^{20}_{05}), High-Speed Register (G^{00}_{06}- G^{20}_{06}), and (G^{00}_{07}- G^{20}_{07}).

(9) STEP CONTROL. - Bogart can be made to perform individual instructions (instruction step) or parts of instructions (command step) and then stop. These sequences are controlled by the Instruction/High-Speed/Command switch and the Run/Step switch on the control panel. The logic for the step sequences is performed by the G cores, shown in Drawing 87206, Volume 8, pages 32 and 33.

(a) COMMAND STEP. - The command step initiates a series of operations which continue until the next command step point. At this point the machine stops and waits for the next command step pulse. The command step signal is initiated when the machine is in the Command mode and the Step switch is put in the momentary-down position.

The re-sync delay pulse (G^{21}_{04}) clears the Step Re-sync circulation bit (G^{10}_{02}- G^{30}_{02}) and the Run Re-sync circulation bit (G^{10}_{00}- G^{30}_{00}). The re-sync delay pulse (G^{38}_{04}) ANDs with the normal position (M^{-2}_{01}) of the Run-step switch to set the Common Re-sync circulation bit (G^{10}_{01}- G^{30}_{01}). The Run-Step switch, when put in the momentary-down position (M^{-2}_{02}), ANDs with a re-sync delay pulse (G^{38}_{04}) to set the Step Re-sync circulation bit (G^{10}_{02}- G^{30}_{02}). This circulates until the next re-sync delay pulse (G^{38}_{04}) ANDs with both the Step Re-sync (G^{30}_{02}) and the Common Re-sync (G^{30}_{01}) to set G^{00}_{02}. The re-sync delay pulse (G^{33}_{04}) also stops the Step Re-sync circulation bit (G^{10}_{02}- G^{30}_{02}) by clearing G^{33}_{04} $(RDC)^{-1}$ as explained in paragraph b(3). The G^{00}_{02} core clears the Common Re-sync circulation bit (G^{10}_{01}- G^{30}_{01})

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and initiates the step pulse (G^{20}_{02}). The step pulse sets G^{30}_{03} which clears the Indicate Stop circulation bits (W^{10}_{80}, W^{10}_{81}, W^{10}_{82}, W^{10}_{83}).

When the Instruction/High-Speed/Command switch is in COMMAND position (M^{-4}_{02}), it sets G^{20}_{20} which sets G^{30}_{20}. This core ANDs with the step pulse to set G^{10}_{09}. This, in turn, initiates the address modification chain (G^{00}_{51},G^{20}_{51}, and G^{30}_{51}), the command chain (G^{00}_{50}, G^{10}_{50}, G^{20}_{50}, G^{30}_{50}, G^{02}_{50}), the read next instruction chain (G^{01}_{50}- G^{20}_{52}), clears the Command Register (G^{00}_{07}- G^{20}_{07}), and initiates the stop pulse (G^{30}_{12}). The stop pulse clears the High-Speed Register (G^{00}_{06}- G^{20}_{06}), the Instruction Step Register (G^{00}_{05}- G^{20}_{05}), and the Command Step Register (G^{00}_{04}- G^{20}_{04}).

Either the command chain, address modification chain, or the read next instruction chain enables a series of operations which continue until the sequence of operations calls for another command step pulse. The machine then stops and waits for the next Step pulse.

(b) INSTRUCTION STEP. - The instruction step executes the operations designated by the instruction contained in U, puts the next sequential instruction in U, and then stops until another step pulse is initiated. The instruction step signal is initiated when the machine is in Instruction or High-Speed mode and the Step switch is put in the momentary-down position.

The re-sync delay pulse (G^{21}_{04}) clears the Step Re-sync circulation bit and the Run Re-sync circulation bit. The re-sync delay pulse ANDs with the normal position (M^{-2}_{01}) of the Run/Step switch to set the Common Re-sync circulation bit. The Run/Step switch, when put in the momentary-down position (M^{-2}_{02}), will AND with a re-sync delay pulse (G^{38}_{04}) to set the Step Re-sync circulation bit. This circulation until the next re-sync delay pulse (G^{38}_{04}) ANDs with both the Step Re-sync (G^{30}_{02}) and the Common Re-sync (G^{30}_{01}) to set G^{00}_{02}. The re-sync delay pulse (G^{21}_{04}) also stops the Step Re-sync circulation bit by interrupting the normal circulation path. The G^{00}_{02} core clears the Common Re-sync circula-

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tion bit and initiates the step pulse (G^{20}_{02}). The step pulse sets G^{30}_{03} which clears the Indicate Stop circulation bits through G^{00}_{60}.

When the Instruction/High-Speed/Command switch is in the Instruction position (M^{-4}_{00}) or High-Speed position (M^{-4}_{01}), it sets G^{30}_{21} which ANDs with the step pulse G^{30}_{03} to set G^{10}_{08}. This in turn, initiates a stop pulse (G^{30}_{12}) which clears the High-Speed Register (G^{00}_{06}- G^{20}_{06}), the Instruction Step Register (G^{00}_{05}- G^{20}_{05}), and the Command Step Register (G^{00}_{04}- G^{20}_{04}). Core G^{10}_{08} also initiates the command chain, the address modification chain, the Read Next Instruction chain, and sets the Command Register. The Command Register initiates the command chain and Read Next Instruction chain every clock cycle, thus performing command step sequences until the Add B to U circulation bit is set, which indicates that the instruction has been completed and a new instruction is in the U-register. When the Add B to U circulation bit is set the machine stops because Add B to U must AND with the address modification chain before another sequence can be initiated.

(c) HIGH-SPEED. - High-Speed mode uses the same controls as explained in the previous section (instruction step).

(10) RUN CONTROL. - When Bogart is in the Run mode, the speed at which it steps through instruction or command sequences is controlled by the low-speed oscillator. The computer is in Run mode when the Instruction/High-Speed/Command switch is not in High-Speed and when the Run/Step switch is in the momentary Run position. The logic in the Run sequence is performed by G cores, as shown in Drawing 87206, Volume 8, pages 32 and 33.

(a) COMMAND STEP. - This control initiates a command step sequence each time the low-speed oscillator sends a pulse to the control section.

The re-sync delay pulse (G^{21}_{04}) clears the Step and Run Re-sync circulation bits. The re-sync delay pulse (G^{38}_{04}) ANDs with the normal position (M^{-2}_{01}) of

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the Run/Step switch to set the Common Re-sync circulation bit. The Run/Step switch, when put in the momentary-up position (M^{-2}_{00}), will AND with a re-sync delay pulse (G^{38}_{04}) to set the Run Re-sync circulation bit (G^{10}_{00}- G^{30}_{00}). This circulates until the next re-sync delay pulse (G^{38}_{04}) ANDs with both the Re-sync (G^{30}_{00}) and the Common Re-sync (G^{30}_{01}) to set G^{00}_{00}. The re-sync delay pulse (G^{21}_{04}) also clears the Run Re-sync circulation bit while G^{00}_{00} clears the Common Re-sync circulation bit. The G^{00}_{00} core then initiates the run pulse (G^{20}_{00}). If a stop pulse is being initiated in the machine, the run pulse ANDs with the stop pulse (G^{20}_{70}) to clear the Indicate Stop circulation bits through G^{00}_{15}. When the Instruction/High-Speed/Command switch is in the COMMAND position (M^{-4}_{02}) the run pulse will AND with G^{20}_{20} setting the Command Step Register. Each low-speed oscillator pulse (G^{20}_{96}) ANDs with the Command Step Register (G^{20}_{04}) to set G^{30}_{10}, initiating the address modification chain, the command chain, and the Read Next Instruction chain. Therefore, the machine runs through one command step sequence each time the low-speed oscillator pulse is initiated.

(b) INSTRUCTION STEP. - The Instruction Run combination completes an instruction each time the low-speed oscillator initiates a pulse.

The re-sync delay pulse (G^{21}_{04}) clears the Step and Run Re-sync circulation bits. The re-sync delay pulse (G^{38}_{04}) ANDs with the normal position (M^{-2}_{01}) of the Run/Step switch to set the Common Re-sync circulation bit. The Run/Step switch, when put in the momentary-up position (M^{-2}_{00}), will AND with a re-sync delay pulse (G^{38}_{04}) to set the Run Re-sync circulation bit. This bit circulates until the next re-sync delay pulse (G^{38}_{04}) ANDs with both the Run Re-sync and the Common Re-sync to set G^{00}_{00}. The re-sync delay pulse (G^{21}_{04}) also stops the Run Re-sync circulation bit while G^{00}_{00} clears the Common Re-sync circulation bit. The G^{00}_{00} core then initiates the run pulse, G^{20}_{00}. If a stop pulse is being initiated in the machine, the run pulse ANDs with the stop pulse (G^{20}_{70}) to clear the Indicate Stop circula-

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tion bits through G^{00}_{15}.

When the Instruction High-Speed Command switch is in the INSTRUCTION position (M^{-4}_{00}) the run pulse ANDs with G^{20}_{22}, setting the Instruction Step circulation bit. This bit ANDs with each low-speed oscillator pulse (G^{20}_{98}) to set G^{30}_{11} which in turn initiates the address modification chain, the command chain, the Read Next Instruction chain, and sets the Command Register circulation bit. The Command Register in turn initiates the command chain and the Read Next Instruction chain every four microseconds. This enables one complete instruction to be performed after each low-speed oscillator pulse.

(11) HIGH-SPEED/RUN CONTROL. - The High-Speed control initiates the command chain, the address modification chain, and the Read Next Instruction chain every four microseconds. This is the normal mode of operation.

The re-sync delay pulse (G^{21}_{04}) clears the Step and Run Re-sync circulation bits. The re-sync delay pulse (G^{38}_{04}) ANDs with the normal position (M^{-2}_{01}) of the Run/Step switch to set the Common Re-sync circulation bit (G^{10}_{01}- G^{30}_{01}). The Run/Step switch, when put in the momentary-up position (M^{-2}_{00}), will AND with a re-sync delay pulse (G^{38}_{04}) to set the Run Re-sync circulation bit. This circulates until the next re-sync delay pulse (G^{38}_{04}) ANDs with both the Run Re-sync and the Common Re-sync to set G^{00}_{00}. The re-sync delay pulse (G^{21}_{04}) also stops the Run Re-sync circulation bit. The G^{00}_{00} core then initiates the run pulse (G^{20}_{00}). If a stop pulse is being initiated in the machine, the run pulse ANDs with the stop pulse to clear the Indicate Stop circulation bits through G^{00}_{15}. When the Instruction/High-Speed/Command switch is in the HIGH-SPEED position (M^{-4}_{01}), the run pulse ANDs with G^{20}_{21} to set the Command Register circulation bit and the High-Speed Register circulation bit. The Command Register initiates the command chain and the Read Next Instruction chain every fourth microsecond, while the High-Speed Register initiates the address modification chain every fourth microsecond.

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4-3. ARITHMETIC SECTION

a. GENERAL. - The Arithmetic Section is composed of the following subdivisions: The X-register, X; the Q-register, Q; the Accumulator, A; Main Adder, H; Shift Control circuitry; Arithmetic sequences; and Arithmetic Sequence controls.

The X-register, Q-register, and A-register generally are referred to as arithmetic registers because of their function during arithmetic operations. In addition, these registers are used to perform other functions not directly associated with arithmetic operations. These auxilliary uses are discussed in a subparagraph for each of the registers.

The arithmetic section uses special procedures derived from fundamental processes of one s complement binary arithmetic to perform the arithmetic and logical operations involved in the execution of the computer s repertoire of instructions. Fundamentally, the Arithmetic Section executes five basically different unit operations, as follows: addition, in which a number in X is added to a number in A; shifting, in which numbers in A or Q or both are appropriately shifted one place to the right or one or four places to the left; complementing of the contents of X, which is performed in an X-buffer and reverses the state of the contents which was contained in each stage of the X-register; bit-by-bit multiplication, in which corresponding bits of X and Q are multiplied together and the bit-by-bit product stored in X; and complementing of A, in which each bit of A is complemented. The complement of positive zero (all stages cleared) will produce no change in the register, since negative zero (all "1's") is not generated in the A-register. The reason for this is explained in Volume 1, Appendix B, Number Systems.

These unit operations are employed separately to form an arithmetic or logical sequence, or they are integrated in various combinations with one another

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to form more complex sequences of operation.

b. X-REGISTER. - The X-register is so called because of its function as the central exchange register of the computer. It is a 24-stage switch core register that can transmit its one s complement. Each stage consists of four magnetic switch cores and their associated circuitry. As an exchange register, X handles nearly all internal transmissions of words between various sections of the computer. As an arithmetic register, X holds the addend, subtrahend, multiplicand, logical product and divisor during the corresponding arithmetic operations. A single stage of the X-register is shown on the following page in Figure 4-31 and the entire X-register is shown in Diagram 87071, Volume 8, page 18.

TRANSMISSIONS TO AND FROM X. - In all the transmissions to the X-register, except in the case of L(Q)(X), X is cleared by normal circulation cores N_{11} or N_{10}. The four switch cores of the X-register are involved in the various transmissions as shown under each core.

(a) CORE X^{10}. - This core is involved in the transmissions of X to U, U to X, and Z to X.

1. U to X. - The 15-bit address portion of the U-register is transmitted to X^{10}_{00}- X^{10}_{14} under the control of N_{14} (U to X control core).

2. Z to X. - Operands are transmitted from Z to X in such a manner that operations may be performed on any one of five portions of the 24-bit word, depending upon the m value (instruction modifier) of the instruction being executed.

m=0 Parallel transmission of 24 bits from Z to X.

m=1 Transmission of right eight bits of information from $Z_{00}...Z_{15}$ to $X_{00}...X_{07}$. Information in Z_{07} is extended to X_{08} through X_{23} making a full 24-bit word.

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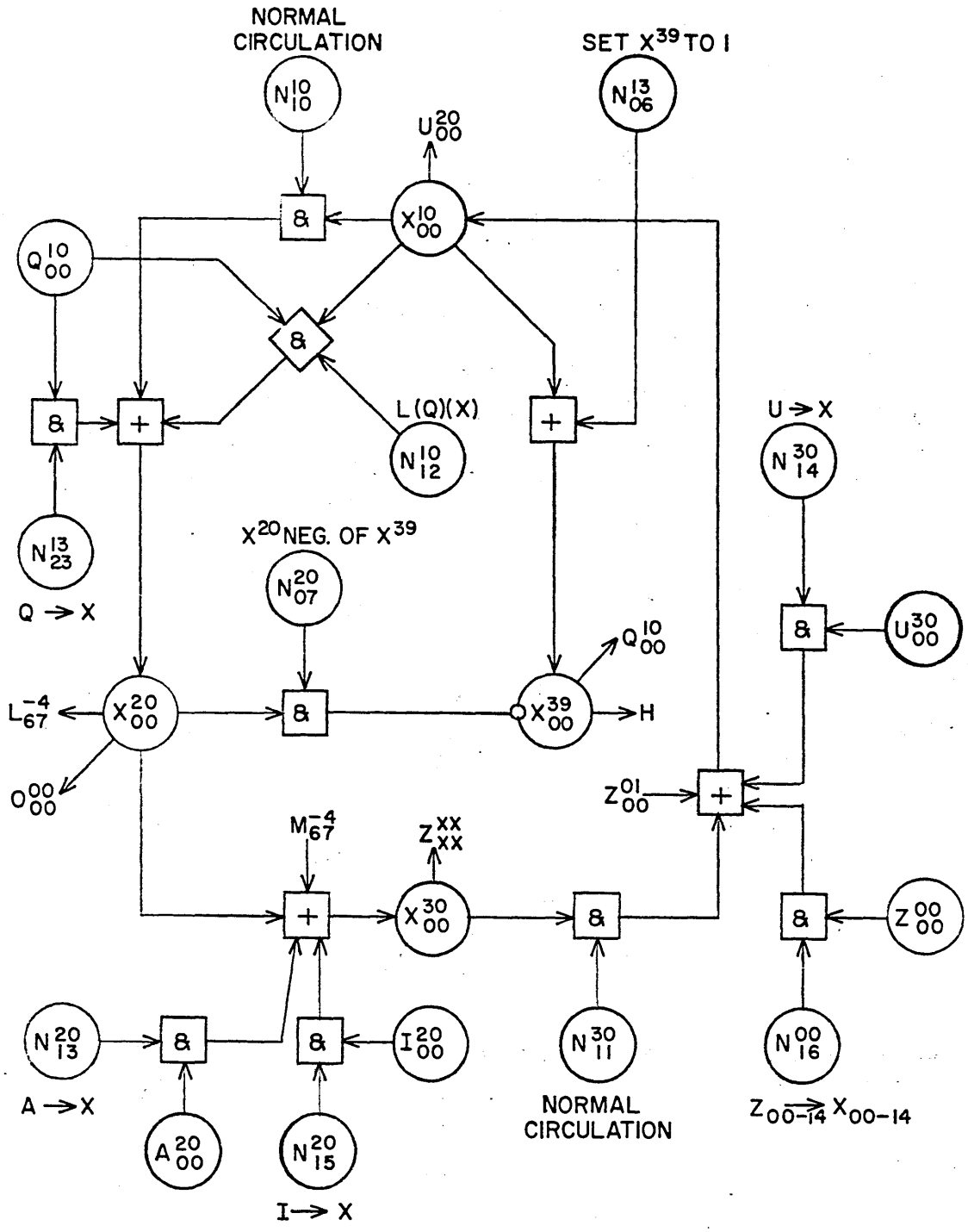

FIRST STAGE OF X – REGISTER

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Figure 4-31. First Stage of X-register

m=2 Transmission of center eight bits of information from $Z_{08}...Z_{15}$ to $X_{00}...X_{07}$. Information in Z_{15} is extended to X_{08} through X_{23} making a full 24-bit word.

m=3 Transmission of left eight bits of information from $Z_{16}...Z_{23}$ to $X_{00}...X_{07}$ Information in Z_{23} is extended to X_{08} through X_{23} making a full 24-bit word.

m=4 Transmission of right 15 bits $Z_{00}...Z_{14}$ to $X_{00}...X_{14}$. There is no extension and bits $X_{15}...X_{23}$ remain zero.

m=5 Transmission of the right eight bits $Z_{00}...Z_{07}$ to $X_{00}...X_{07}$. There is no extension and bits $X_{08}...X_{23}$ remain zero.

m=6 Transmission of center eight bits of information from $Z_{08}...Z_{15}$ to $X_{00}...X_{07}$. There is no extension and bits $X_{08}...X_{23}$ remain zero.

m=7 Transmission of left eight bits of information from $Z_{16}...Z_{23}$ to $X_{00}...X_{07}$ There is no extension and bits $X_{08}...X_{23}$ remain zero.

3. X to U. - The contents of $X^{10}_{00}...X^{10}_{14}$ are transmitted to the 15-bit address portion of the U-register under the control of N_{34} (X to U control core).

4. X to X^{39} BUFFER. - The contents of X^{10} are sent to the X^{39} buffer during every clock cycle.

(b) CORE X^{20}. - This core controls the panel indicator lights and is used in the transmissions Q to X, L(Q)(X), X to 0, and Negation of X^{39}.

1. Q to X. - The (Q to X Control Core) N_{23} permits the parallel transmission of a 24-bit word from Q^{10} to the X^{20} core of the X-register.

2. L(Q)(X). - The normal circulation control core N_{10} blocks normal circulation in X, while N_{12}, the logical (Q)(X) control core, controls the logical bit-by-bit multiplication path. A logical AND of Q^{10}

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and X^{10} transmits the information so that where "0's"are stored in Q, the corresponding stages of X are cleared to "0". Where"1's" are stored in Q, the corresponding stages of X are left undisturbed. The effect is that a "0" in Q, times either a "0" or a "1" in X, leaves a "0" stored in X and that a "1" in Q, times either a "0" or a "1" stored in X, leaves X undisturbed.

3. X to 0. - $X^{20}_{00}...X^{20}_{06}$ transmits seven bits of information to the Output Register controlled by N^{20}_{60} (X to 0 control core) during the Output instruction.

4. NEGATION OF X^{39} BUFFER. - This operation is controlled by N_{07} (negation of X^{39} control core), which acts with X^{20} to negate X^{39}, thus forming the complement of X in the X^{39} buffer.

5. PANE L LIGHT. - X^{20} lights the respective indicator panel neon light for each X-register stage.

(c) CORE X^{30} - This core receives information from the A-register, I-register, or Manual Set button, and transmits that information to the Z-register.

1. A to X. - Parallel transmission of 24 bits of A to X is received in X^{30} when N_{13} (A to X control core) is set.

2. I to X. - The I-register transmits seven bits of input information to X under the control of N^{20}_{15} (I to X control core) during Input instructions and Load Mode control.

3. X to Z. - Information for Storage is transmitted from X to Z under control of N_{71}, N_{72}, or N_{73} (X to Z control cores) and one of the following conditions of instruction modifier m:

m=0 Parallel transmission of 24 bits from X to Z

m=1 or 5 Transmission of right eight bits of information from $X_{00}...X_{07}$ to right eight bits of Z ($Z_{00}...Z_{07}$).

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m=2 or 6 Transmission of right eight bits of information from $X_{00}...X_{07}$ to center eight bits of Z ($Z_{08}...Z_{15}$).

m=3 to 7 Transmission of right eight bits of information from $X_{00}...X_{00}$ to left eight bits of Z ($Z_{16}...Z_{23}$).

m=4 Transmission of right 15 bits of information from $X_{00}...X_{14}$ to 15 bits of Z ($Z_{00}...Z_{14}$).

Manual set. Core X^{30} in each stage can be set to 1 by manual switch buttons located on the indicator display panel.

(d) CORE X^{39}. - This core contains either X or its complement at all times. This core is referred to as the X^{39} buffer and transmits information to Q or the main adder.

1. X Q. - Parallel transmission of 24 bits of X to Q is controlled by N_{26} (X to Q control core).

2. ADD X to A. - All transmissions to A are added to the contents of the A-register by passing through the main adder. There is no direct X to A transmission path.

3. COMPLEMENT X. - The basic unit operation of complementing X is accomplished when N_{03} (Set X^{39} to 1) is set and all bits of X^{39} are set. Then all of the X^{20} cores which contain a "1" form a logical AND with N_{07} (negation of X^{39}) to negate the X^{39} cores in those stages, thus reversing the state of each X-register stage regardless of what it stored previously. This complementation does not affect the original contents of the X-register.

(2) OPERATION AS A CENTRAL EXCHANGE REGISTER. - As a central exchange register, X is involved in almost all internal transmissions of data. The following listing summarizes the various transmissions in which X is involved:

Two-way transmissions	One-way transmissions
X<=>Q (24 bit transmission)	X->O (seven bit output)
X<=>U (15 bit transmission)	A->X (24 bit transmission)
X<=>Z (depending upon m)	I->X (seven bit input)
	Add X to A->A (24 bit transmission)
	L(Q)(X)->X (24 bit transmission)

(3) OPERATION AS AN ARITHMETIC REGISTER. - As an arithmetic register, X holds the addend, subtrahend, multiplicand, and divisor in the corresponding arithimetic operations. In logical addition and logical multiplication, X holds the logical addend, logical multiplicand, and retains the logical product.

c. Q-REGISTER. - The Q-Register is so-called because it holds the quotient during the division operation. It is a 24-bit register that has right and left-shift properties. Each stage consists of two magnetic switch cores and their associated circuitry. As an assembly register, Q is capable of receiving six bits at a time and shifting these to the left to assemble a 24-bit word as is done in loading operations. During the writing operation, 24-bit words are disassembled by a similar operation in Q. As an arithmetic register, Q performs shifting operations and holds the multiplier, quotient, and logical multiplier during arithmetic operations. Inter-connections between the stages provide Q with left circular (one and four-place) shift properties, and right-shift (multiply step) properties. A single stage of the Q-register is shown in Figure 4-32, and the entire Q-register is shown in Diagram 87069, Volume 8, page 16.

(1) TRANSMISSIONS TO AND FROM Q. - In the transmissions to Q, the Q-register is cleared by N_{24} or N_{20} (normal circulation control cores). The first stage of Q can be set by N^{20}_{18} (Set Q_{00} to "1"). The Q^{19}_{00} core senses a "0" in the first stage of Q and is used in Multiply Step.

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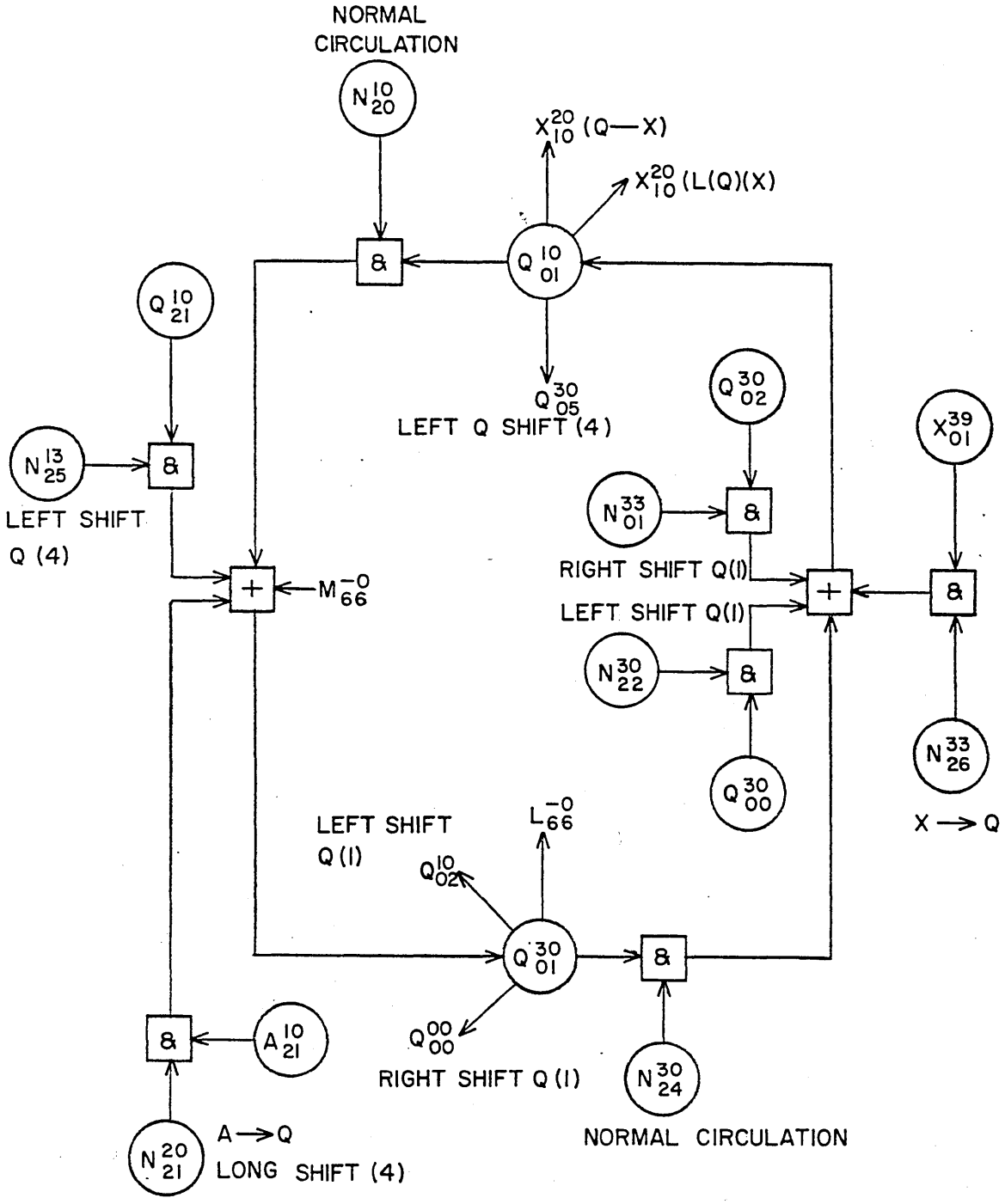

SECOND STAGE OF Q —REGISTER

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Figure 4-32. Second Stage of Q-register

(a) CORE Q^{10}. - This core receives X to Q, Right Shift Q One and Left Shift Q One information. Shifting is discussed in a later paragraph. Information sent out from this core includes Q to X, L(Q)(X), and Shift Q Four.

1. X to Q. - Parallel transmission of 24 bits of information from X to Q under control of N_{26} (X to Q control core).

2. Q to X. - Parallel transmission of 24 bits of information from Q to X under control of N_{23} (Q to X control core).

3. L(Q)(X). - The logical bit-by-bit multiplication path is controlled by N_{12} control cores. A logical AND of Q^{10} and X^{10} transmits the information so that where "0's"are stored in Q, the corresponding stages of X are cleared. Where "1's" are stored in Q, the corresponding stages of X are left undisturbed. The effect is that a "0" in Q, times eigher a "0" or a "1" in X, leaves a "0" stored in X, and that a "1" in Q, times either a "0" or a "1" stored in X, leaves X undisturbed.

(b) CORE Q^{30}. - This core receives information from the Left Shift Q Four, A to Q Long Shift Four, or Manual Set button. Information is sent to the indicator display panel, Left-Shift Q One, and Right-Shift Q One.

1. PANEL LIGHT. - Q^{30} lights the respective indicator panel neon light for each Q-register stage.

2. MANUAL SET. - Core Q^{30} in each stage can be set by manual switch button on the indicator display panel.

(2) SHIFTING. - Information in Q can be shifted in the following manner:

(a) ONE-PLACE, LEFT-CIRCULAR SHIFT OF Q. - This shift causes the information in Q to be shifted left by one place, and the contents of Q_{23} to be shifted to Q^{10}_{00}. This shift is controlled by N_{22}.

(b) FOUR-PLACE, LEFT-CIRCULAR SHIFT OF Q. - This shift causes

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the information in Q to be shifted left by four places, with the contents of Q^{10}_{23}, Q^{10}_{22}, Q^{10}_{21}, and Q^{10}_{20} shifted to Q^{30}_{03}, Q^{30}_{02}, Q^{30}_{01}, and Q^{30}_{00}. The operation is is controlled by N_{25}.

When A and Q are combined into an extended 48-bit register the following shifts are possible:

(c) ONE-PLACE, LONG LEFT-CIRCULAR SHIFT OF A AND Q. - This shift causes the information in A and Q to be shifted left by one place with the contents of Q^{30}_{23} shifted to A^{00}_{00} and contents of A^{30}_{23} shifted to Q^{10}_{00}. This shift is controlled by N_{03}, N_{02} and N_{22} cores.

(d) FOUR-PLACE, LONG LEFT-CIRCULAR SHIFT OF A AND Q. - This shift causes the information in A and Q to be shifted left by four places with the contents of Q^{10}_{23}, Q^{10}_{22}, Q^{10}_{21}, and Q^{10}_{20} being shifted to A^{30}_{03}, A^{30}_{02}, A^{30}_{01}, and A^{30}_{00} and contents of A^{20}_{23}, A^{20}_{22}, A^{20}_{21}, and A^{20}_{20}, being circularly shifted back to Q^{30}_{03}, Q^{30}_{02}, Q^{30}_{01}, and Q^{30}_{00} under the control of N_{21}, N_{05}, and N_{25} cores.

(e) ONE-PLACE, Q AND Q RIGHT SHIFT. - This shift, used in Multiply Step, causes the information in A and Q to be shifted right by one place with the contents of A_{00} being shifted to Q_{23} and the contents of Q_{00} being shifted off the end and lost. The N_{01} cores control this shift.

(3) OPERATION AS AN ASSEMBLY REGISTER. - During loading operations Q assembles 24-bit words, six bits at a time. Seven bits are first stored in the Input Register and when enabled by N^{20}_{15} are transferred to $X^{30}_{00}...X^{30}_{0e}$.

During the assembly operation only six bits are transferred from X to Q. Q is then shifted left one four-place shift and two one-place shifts. This process is repeated four times until the complete 24-bit word is present in Q.

During output operations, a 24-bit word is transmitted to Q from X. Q is then shifted six places to the left, with the six higher-order bits of the word initially stored in Q being shifted to $Q_{05}...Q_{00}$.

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This information is then transferred to the first six stages of X and when control core N_{60}^{20} is enabled the information is transferred to the O-Register. The process continues until the entire 24-bit word in Q has been transferred to external equipment. A new word is then inserted into Q from X, and the disassembly operation described above is repeated.

(4) OPERATION AS AN ARITHMETIC REGISTER. - During arithmetic operations, the Q-register contains the multiplier, quotient, and logical multiplier.

d. ACCUMULATOR. - The Accumulator is so-called because the results of many arithmetic operations are formed by accumulation in A. It is a 24-bit subtractive accumulator-register with shifting properties. Each of the 24 stages consists of four magnetic switch cores with interconnections to give A its right and left-shift properties. As an arithmetic register, A performs shifting and accumulating operations and holds the sum, augend, minuend, difference, partial product, and partial dividend (remainder) during arithmetic operations. A single stage of the A-register is reproduced in Figure 4-33 while the entire A-register is shown on Logic Diagram 87070, Volume 8, page 17.

(1) TRANSMISSIONS TO AND FROM A. - All numbers inserted into A are transmitted from the X-register, through the main adder, by the basic addition process. In all such transmissions from X, a 24-bit number is added to A (modulus $2^{23}-1$)

(a) CORE A^{00}. - Core A^{00} receives information from Q to A Long Left-Shift One, Right-Shift (Multiply Step), and Left-Shift A One. Information is sent to the Main Adder and panel lights from A^{00}.

(b) CORE A^{20}. - Information is received by A^{10} from the Main Adder and manual push button. Output destinations include the X-register and negation for A^{39} (complement of A).

(c) CORE A^{30}. - Core A^{30} receives information from Left-Shift A

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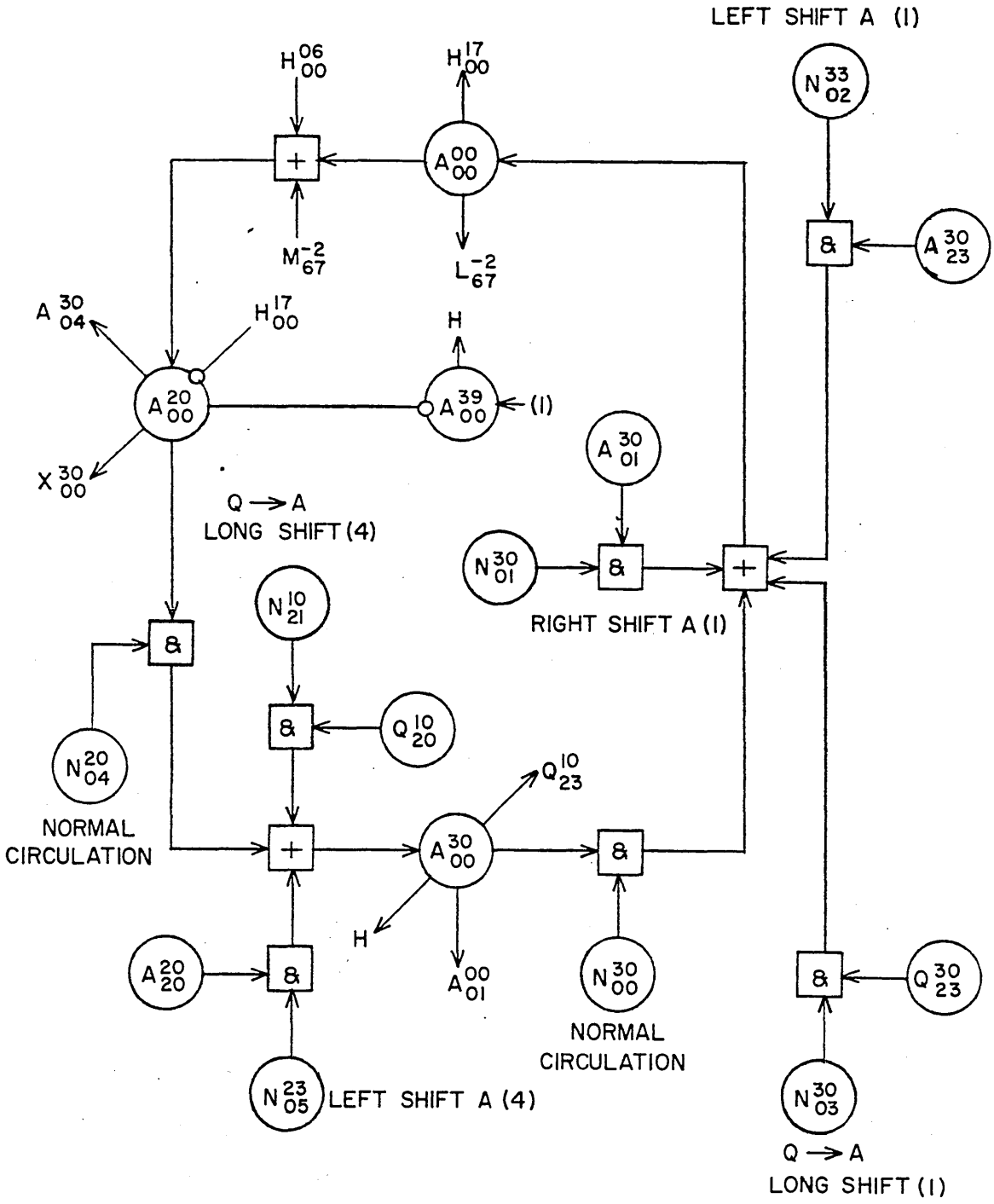

FIRST STAGE A—REGISTER

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Figure 4-33. First Stage of A-register

Four, Q to A, and Long Left-Shift One (Multiply Step).

(d) CORE A^{39}. - This core provides the complement for A for use in the Main Adder.

(2) SHIFTING. - A number stored in A can be shifted in the following manner:

(a) ONE-PLACE, LEFT-CIRCULAR SHIFT OF A. - This shift causes the information to be shifted by one place, and the contents of A^{30}_{23} to be shifted to A^{00}_{00}. This shift is controlled by N_{02}.

(b) FOUR-PLACE, LEFT-CIRCULAR SHIFT OF A. - The information in A is shifted left by four places, and the contents of A^{20}_{23}, A^{20}_{22}, A^{20}_{21}, and A^{20}_{20} are shifted to A^{30}_{03}, A^{30}_{02}, A^{30}_{01}, and A^{30}_{00}, respectively. The Left-Shift Four is controlled by core N_{05}. As an extended 48 bit register of A and Q, the following shifts are possible:

(c) ONE-PLACE, LONG LEFT-CIRCULAR SHIFT OF A AND Q. - This shift causes the information in A and Q to be shifted left by one place with the contents of Q^{30}_{23} shifted to A^{00}_{00} and contents of A^{30}_{23} shifted to Q^{10}_{00}. This shift is controlled by N_{03} cores.

(d) FOUR-PLACE LONG LEFT-CIRCULAR SHIFT OF A AND Q. - The information in A and Q is shifted left by four places with the contents of Q^{10}_{23}, Q^{10}_{22}, Q^{10}_{21}, and Q^{10}_{20} being shifted to A^{30}_{03}, A^{30}_{02}, A^{30}_{01}, and A^{30}_{00} and the contents of A^{20}_{23}, A^{20}_{22}, A^{20}_{21}, and A^{20}_{20}, being circularly shifted back to Q^{30}_{03}, Q^{30}_{02}, Q^{30}_{01}, and Q^{30}_{00} under control of N_{21} cores.

(e) ONE-PLACE A AND Q RIGHT-SHIFT. - This shift, used in Multiply Step, causes the information in A and Q to be shifted right by one place with the contents of A_{00} being shifted to Q_{23} and the contents of Q_{00} being shifted off the end and lost.

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(3) OPERATION AS AN ARITHMETIC REGISTER. - The basic unit operation of addition and its relationship to the Accumulator is discussed in the chapter on Addition. For the arithmetic processes, the Accumulator contains the augend, sum, minuend, difference, product, remainder, logical augend, and logical sum.

e. SHIFT CONTROL CIRCUITRY. - The computer has various shifting properties including left-shift A, left-shift Q, long shift A and Q, and right-shift A and Q. The left-shift and long shift can be shifted a maximum of 63 places per instruction, while the right-shift can be shifted only one place per instruction.

Shifting operations controlled by the Arithmetic Section involve the following circuits: the Shift Counter (K), the second-level control for left-shifts, first-level control for four-place left-shifts, first-level control for one-place left-shifts, Back K control, and Right-Shift control. These registers and controls are shown on the following drawings: K-register, Drawing 87076, Volume 8, page 23; and Shift Controls, Drawing 87209, Volume 8, page 11. The following paragraphs describe each of the shift control circuits and illustrate the shifts that can be accomplished.

(1) SHIFT COUNTER. - The Shift Counter, K-register, is a six-bit subtractive counter and storage register. The register is divided into two sections, with the two lower-order bits controlling the one-place left shifts and the remaining four bits controlling the four-place left shifts. The A or Q-register or both together can be shifted left to a maximum of 63 places (K-register modulus 2^6-1). This amounts to a total of three one-place left shifts and 15 four-place left shifts.

(a) TRANSMISSIONS TO AND FROM K. - The K-register is built of six stages each consisting of five magnetic switch cores and their associated circuitry. The K-register is cleared by the N_{84} lower core before new informa-

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tion is transmitted to K from the U-register or Set K to 6 control cores.

1. CORE K^{30}. - Information is received from U^{10} under the control of the N_{85} control core. This information which corresponds to the required number of shifts is placed in the six lower bits of U before it transferred to K. Core K^{30} sends a pulse to V^{00}_{58} and V^{00}_{57} (second-level control) that enables a one or four-place shift and blocks I to X, Q to X, and Z to U transmissions.

2. CORE K^{10}. - These cores provide information for the K-register indicator lights and may be set by manual push buttons from the indicator panel.

3. CORES K^{19}, K^{29}, K^{09}. - These cores are not involved in any transmissions in or out of the K-register but are used in the subtractive logic.

(b) SET K TO 6. - The Set K to 6 procedure is used in Input and Output instructions and during Load mode. The K-register is the control for the shifting that is used during assembly and disassembly of a 24-bit word. This 24-bit word is sent to the Input or Output register six bits at a time. To assemble a word, the content of the Input register (six bits) is sent to the Q-register, then the K-register is set to 6, and the Q-register is shifted to the left by six bit positions to make room for the next six-bit transmission from I. This process is executed three times to allow space for the 24 bits in Q. The entire 24-bit word is then transmitted to the X-register.

To disassemble a word the 24-bit word is first transmitted from X to the Q-register, then, K is set to 6, Q is circularly shifted to the left six bit-positions, and the lower six bits of Q are sent to the Output register. This process is executed four times, thus disassembling the 24-bit word.

The Set K to 6 control simply puts a "1" in the second and third stages of

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the K-register producing the value of 000110 in binary notation which is equivalent to an octal 6.

(c) OPERATION AS A COUNTING REGISTER. - The K-register counts by decreasing itself by one for each operation and is known as a subtractive counter. The K-register is divided into two sections for logical purposes. After each one-place shift, the number in the lower two-bit section, K_{0-1}, is decreased by one; after each four-place shift, the number in the upper four bits, K_{2-5}, is decreased by one.

The one-place shift counter for K_{0-1}, shown in Figure 4-34, uses the following logic. After each one-place shift, V^{00}_{55} (Back K_{0-1} control) sends a signal to K^{19}_{00}, which subtracts one from the K-register by toggling the necessary stages of K. This is accomplished by having the K^{19}_{00} signal AND with the signal that indicates a "1" in K^{10}_{00}, thereby setting core K^{29}_{00}, which in turn negates K^{30}_{00}.

If K_{00} contains a "0", K^{09}_{00} (unconditionally set at each time 2) is not cleared and produces a logical AND with V^{00}_{55} to borrow from the second stage of the K-register. K^{19}_{00} at the same time sets stage 0. Since K_{00} (under these conditions) contains a "1", the first step is repeated. As long as either stage K_{00} or K_{01} contains a "1", the K^{30} core of the affected stage will AND with the back K pulse (N^{30}_{83}) to set V^{00}_{55}, thus continuing the toggeling action.

When all stages are in the "0" state, N^{30}_{83} (Back K control) is prevented from setting V^{00}_{55} and this "0" condition is also sensed by V^{00}_{57}, which in turn prevents another command step sequence in the shift control logic (see Drawing 87209, Volume 8, page 11).

The four-place Shift Counter section uses a similar procedure for decreasing the contents of K_{2-5}.

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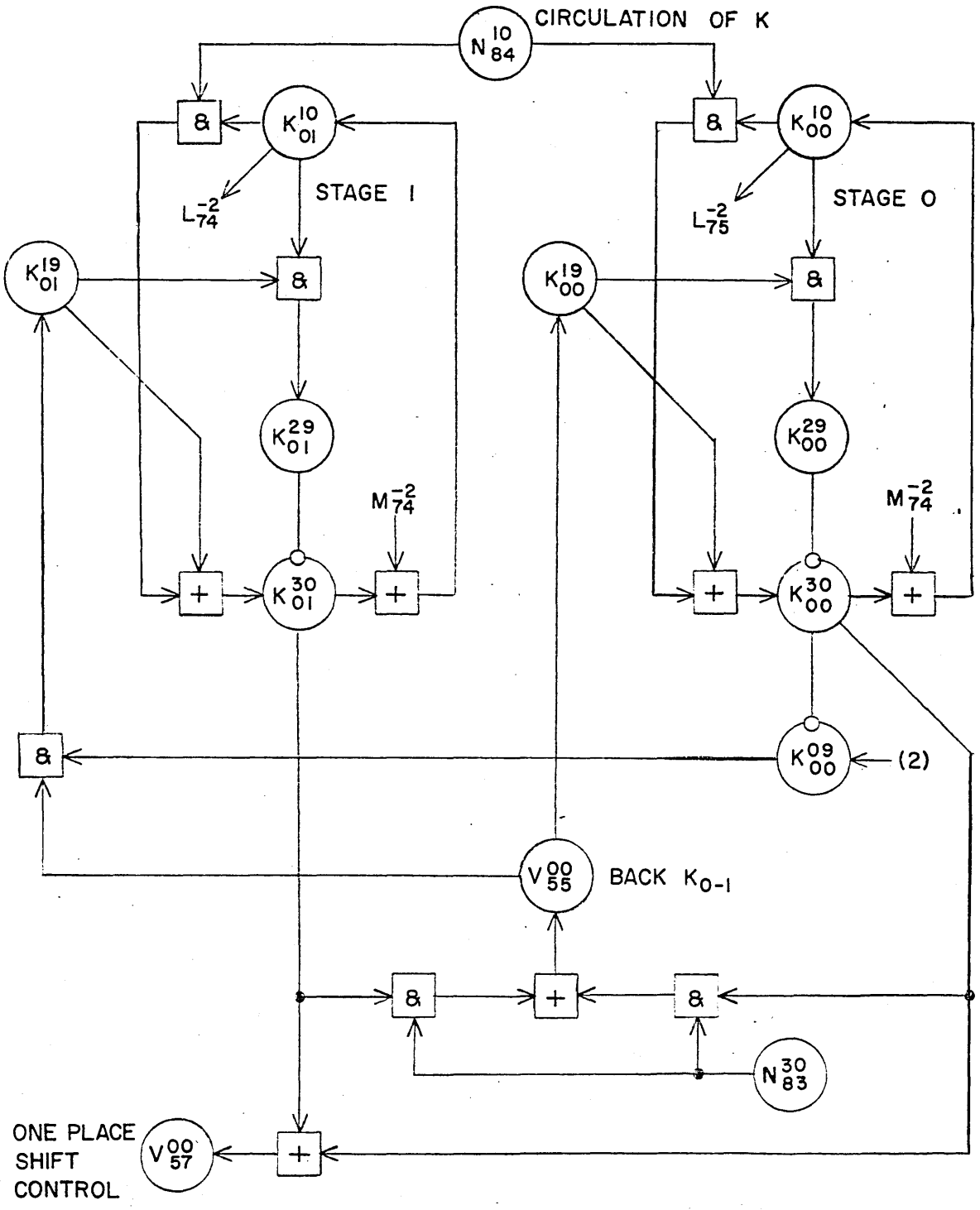

Figure 4-34. Shift Counter

(2) SECOND-LEVEL CONTROL FOR LEFT SHIFTS. - As soon as the translation indicating a shift instruction is processed, core E^{30}_{53} completes the AND circuit and sets the Shift bit (SFT). The next command step clears the Shift bit, transmits the shift count from U to K, and sets the Shift control bit (SHC). (This sequence of events can only occur if (K) = 0.) The information in the Shift control bit then ANDs with either of the two lower-order bits of K to enable a one-place left shift, and also ANDs with any of the four higher-order bits of K to enable a four-place left shift.

(3) FIRST-LEVEL CONTROL FOR ONE-PLACE SHIFTS. - The logical AND of the Shift Control bit, the first or second bits of K, and a command step pulse set V^{20}_{57}, which supplies information to the first level control for one-place left shifts. Then, according to the instruction selected, one of the N control cores for shifting is set, and either A or Q, or both, have their circulation blocked and are shifted one place to the left. These shifts may be either shifts within a register or long circular shifts involving both the A and Q registers.

Figure 4-35 shows the first-level control for left (one-place) circular shift of Q. Core N^{30}_{24} is cleared and core N^{30}_{22} is set by a logical AND of the second-level control and the translation of the current instruction. This blocks normal circulation of Q and enables the passage of information from Q^{30}_{02} (stage 2) to Q^{10}_{03} (stage 3) of the Q-register, thus producing a one-place left-circular shift of Q.

The one-place left-circular shift of A, or Long Shift One, is similar to the above shift except that each shift has its own control cores. See Drawing 87209, Volume 8, page 11.

(4) FIRST-LEVEL CONTROL FOR FOUR-PLACE LEFT SHIFTS. - The logical AND of the Shift Control bit, any of bits 02 through 05 of K, and a command step pulse sets V^{20}_{58}, which supplies information to the First-Level Control for four-

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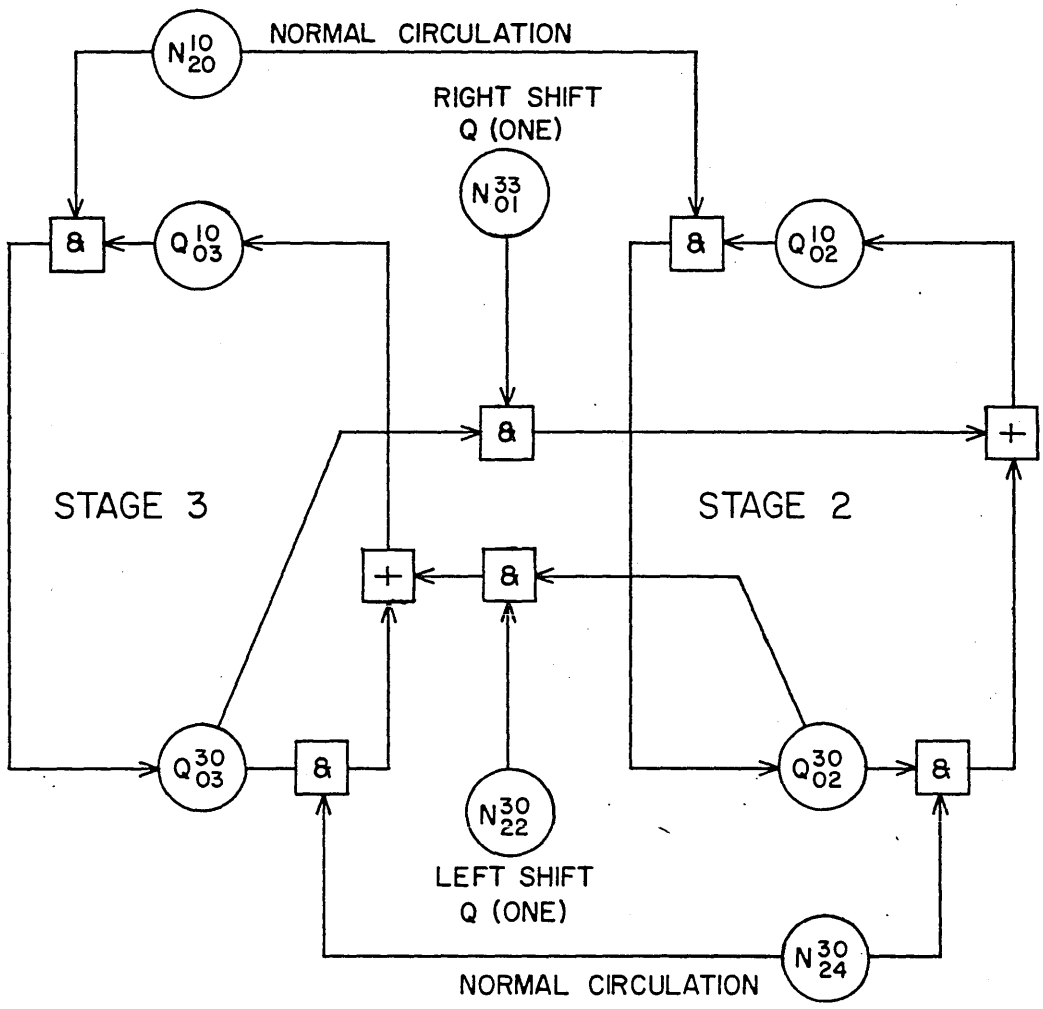

Figure 4-35. 2nd Level Controls for Shifting

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place left shifts. Then, according to the instruction selected, one of the N control cores for shifting is set and either A or Q, or both, have their circulation blocked and are shifted four places to the left. The four-place shifts may be either circular shifts within a register or long circular shifts involving both the A and Q-registers.

Figure 4-36 illustrates the four-place shift within the Q-register. Under the control of N^{10}_{25} (Left Shift Q Four) information is transferred from Q^{10}_{00} (stage 0) to Q^{10}_{04} (stage 4), and from Q^{10}_{04} to Q^{30}_{08} (stage 8), thus producing a four-place left shift of Q.

The four-place left shift of A (Long Shift A and Q Four) is similar to the above shift except each shift has its own control cores. See Figure 4-37 and Drawing 87209, Volume 8, page 11.

(5) CONTROL FOR RIGHT SHIFT (MULTIPLY STEP). - This circuit, illustrated in Figure 4-35 controls the one-place right shift of the Multiply Step instruction. None of the other shift controls are used during the Multiply Step sequence.

When Instruction 60 is programmed, the Shift Multiply Step bit (SMS) is set. This bit, upon the re-occurrence of another command step, will set N^{20}_{01} (Right-Shift control). Core N^{20}_{01}, in turn, sets a number of N_{01} cores, which allows the information in A and Q to be shifted one place to the right. For example, core N^{33}_{01} permits transfer of information from Q^{30}_{03} (stage 3) to Q^{10}_{02} (stage 2).

(6) BACK K CONTROL. - Each time a command step is issued to the second-level control cores, the N^{30}_{83} control core is set. This core ANDs with each of the six bits of the K-register. If a "1" exists in either the first or second stage of K, the V^{00}_{55} core is set which subtracts one from that total count. If a "1" exists in any of the upper four bits of K, core V^{00}_{58} is set.

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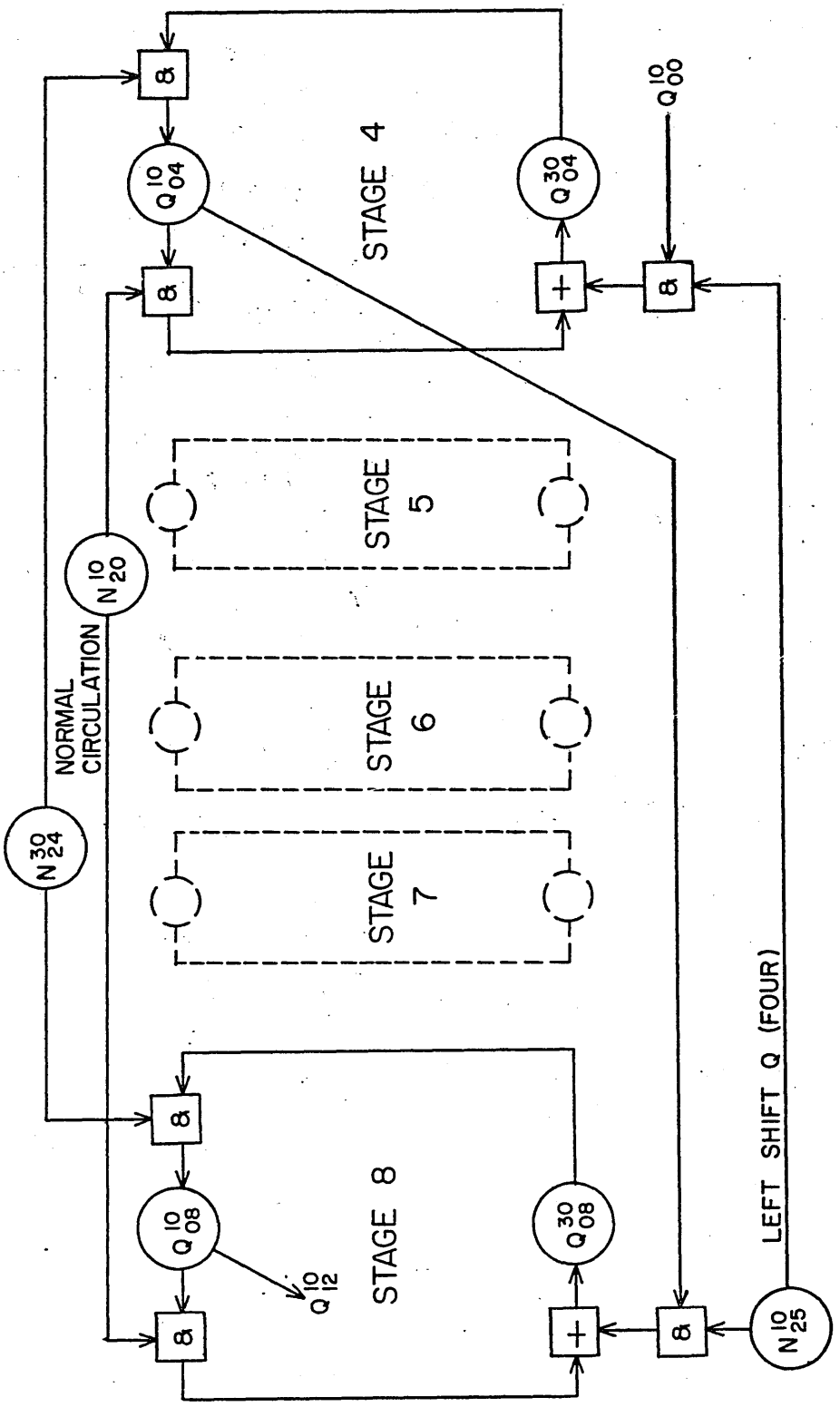

Figure 4-36. Four-Place Shift Control (Q)

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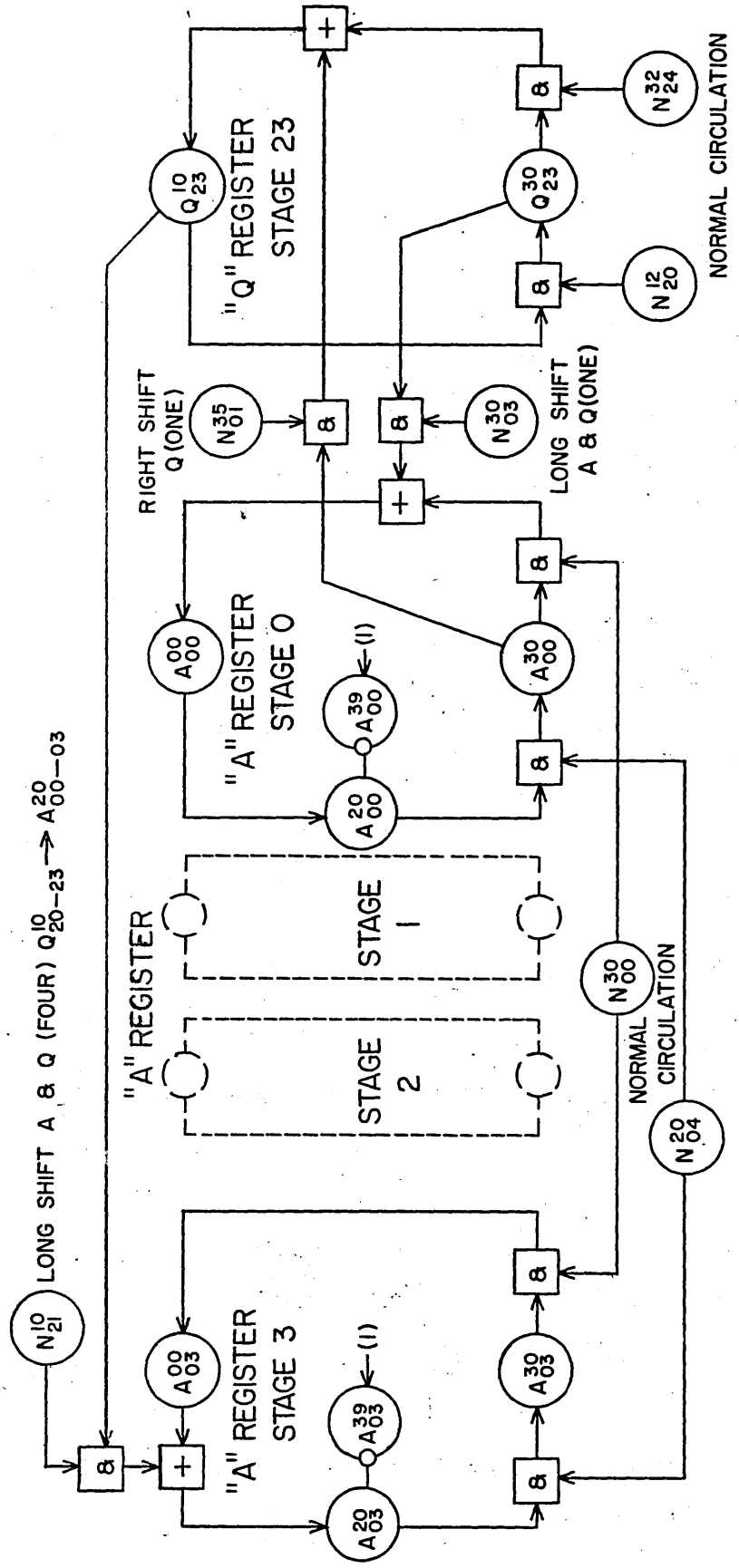


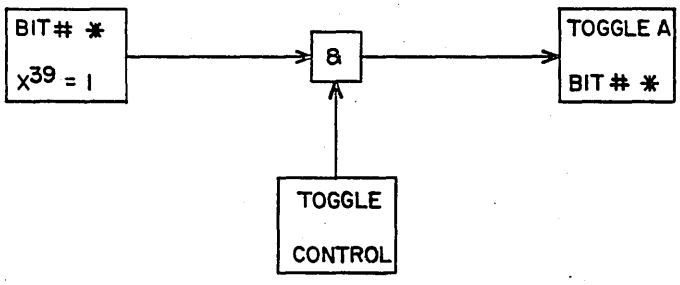
Figure 4-37. Four Place Shift Control (A & Q)

This core causes one to be subtracted from the total count in the upper four bits of K.

f. MAIN ADDER. - The main adder, H, is so-called because of its function in the arithmetic section of the computer.

(1) BASIC PROPERTIES OF THE ADDER. - The adder is a 24-stage parallel adder constructed of approximately 90 magnetic switch cards. The adder is subtractive in nature and uses one s complement arithmetic. All transmissions to A, except during shifting operations, must pass through this adder structure. Drawings concerning the main adder are contained in Volume 8, pages 29 and 30.

(2) LOGIC OF MAIN ADDER. - The main adder is a subtractive type adder that does bit-by-bit subtractions and generates borrow conditions. The bit-by-bit subtraction is accomplished by toggling the corresponding bit of A whenever an X^{39} bit contains a "1" as shown in Example 1.



Example 1.

A borrow condition is set whenever "1" is subtracted from "0", or as the computer senses it, a borrow condition is set whenever a "1" is subtracted and the difference is "1". Since a bit can only borrow from a bit containing a "1", the main adder must find a higher-order bit containing a "1" whenever a borrow is generated. In order to generate all the borrow conditions of the 24-bit A-register in one clock cycle (four micro-seconds), the main adder divides the A-register into eight 3-bit groups. The lower four of these eight groups (representing bits A_{00} through A_{11}) are combined at the next higher level to

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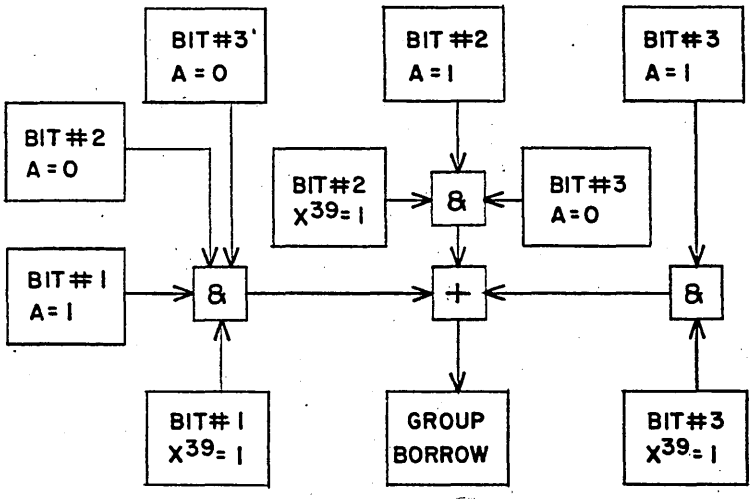
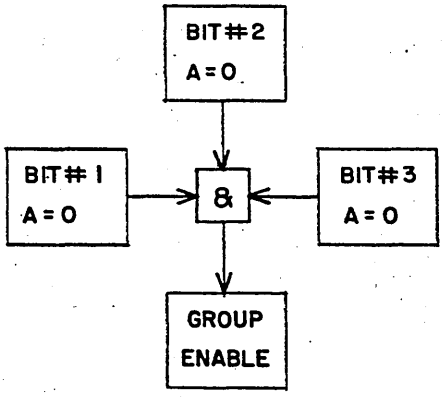
produce a lower-half borrow (or enable) signal. Similarly, the groups representing A_{12} through A_{23} combine to form the upper-half borrow (or enable). Finally, the upper and lower-half signals produce the end borrow and/or middle borrow signals. Borrow generation in any of the three above-mentioned levels is the result of a borrow signal in one of the low-order groups accompanied by enable signals in the succeeding higher-order groups, or a borrow from the highest-order group alone. At the group level, a borrow generation will occur under three conditions of X and A. These are diagrammed in Example 2. Note that corresponding bits of A and X^{39} must both be "1" to effect borrow generation. Since A was toggled for X^{39} = "1", that stage of A must have initially been "0". This is logical, since a borrow is produced only by subtracting "1" from "0". The three conditions may be summarized as follows:

A borrow is generated at the group level if corresponding bits of A and X^{39} are "1", and this combination is accompanied by "0's" in the succeeding higher-order stages of A (if any). Notice that bits of A which are of a lower order



Example 2



Example 3

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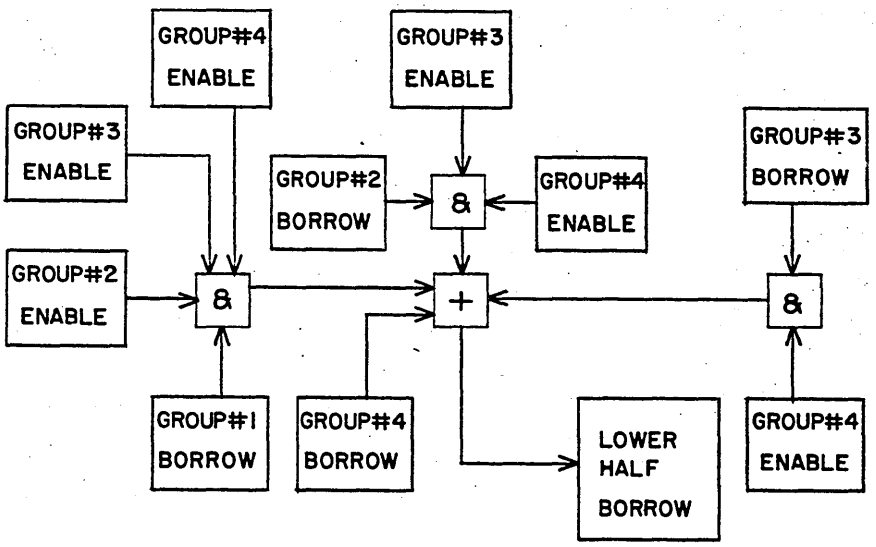
than the borrow-generating stage have no effect upon borrow generation. A group enable is generated when all the bits of a group contain "0's" after the toggle, as shown in Example 3.

The upper and lower-half borrows are set when a group borrow is set and the higher-order groups in that half of the A-register contain "0's". The logic that covers these conditions is shown in Example 4.

The upper and lower-half enables are set when the corresponding halves of the A-register contains all "0's" as shown in Example 5.

The end or middle borrows are generated when one-half of the register wants to borrow from the other or when one-half of the register wants to borrow from the other half, but finds all "0's" in that half, and so must borrow from itself. The end borrow generates a borrow condition to the lower half and the middle borrow generates a borrow condition to the upper half. These borrows are illustrated in Example 6.

Each group has a borrow condition set on it in certain instances. The first group in a half of the register is borrowed from when the end borrow or middle borrow is set as in Example 7.



Example 4

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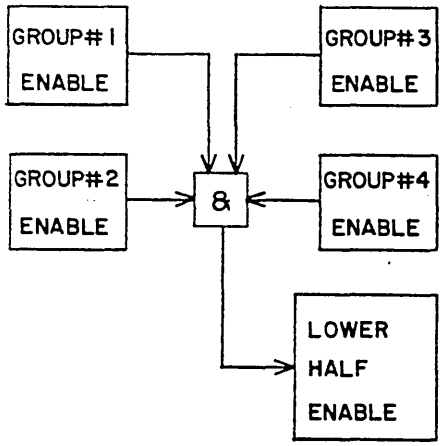
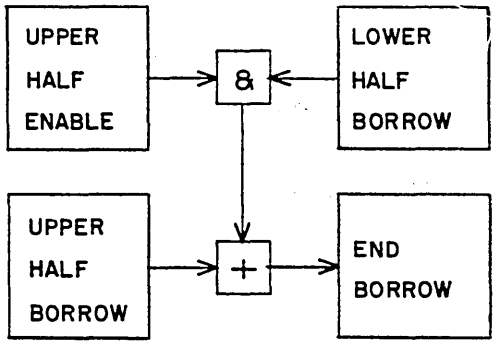
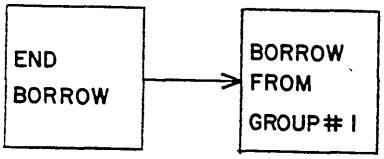


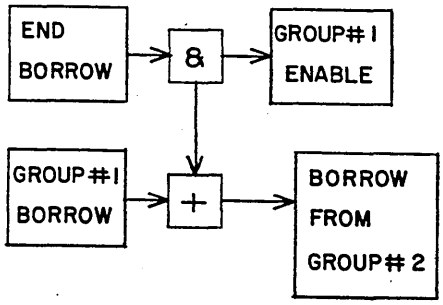
Example 5



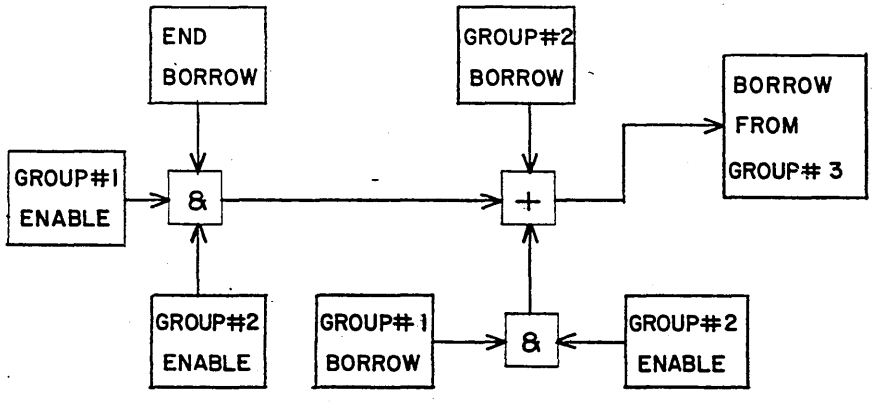
Example 6



Example 7



Example 8



Example 9

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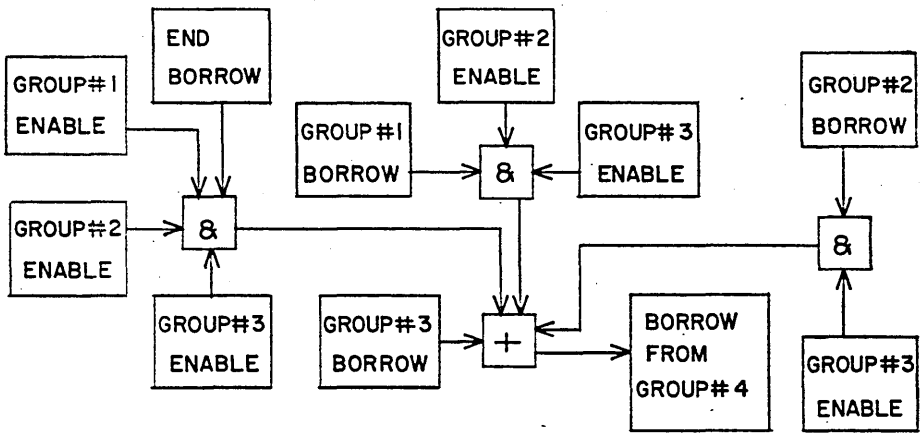
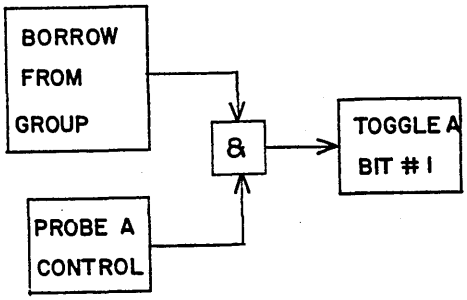
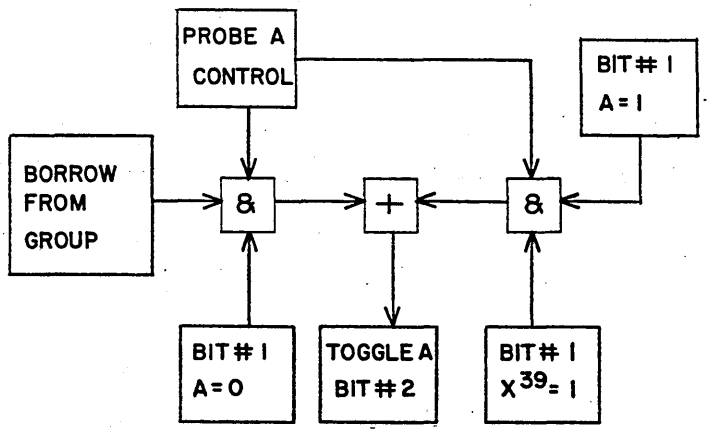


Example 10



Example 11



Example 12

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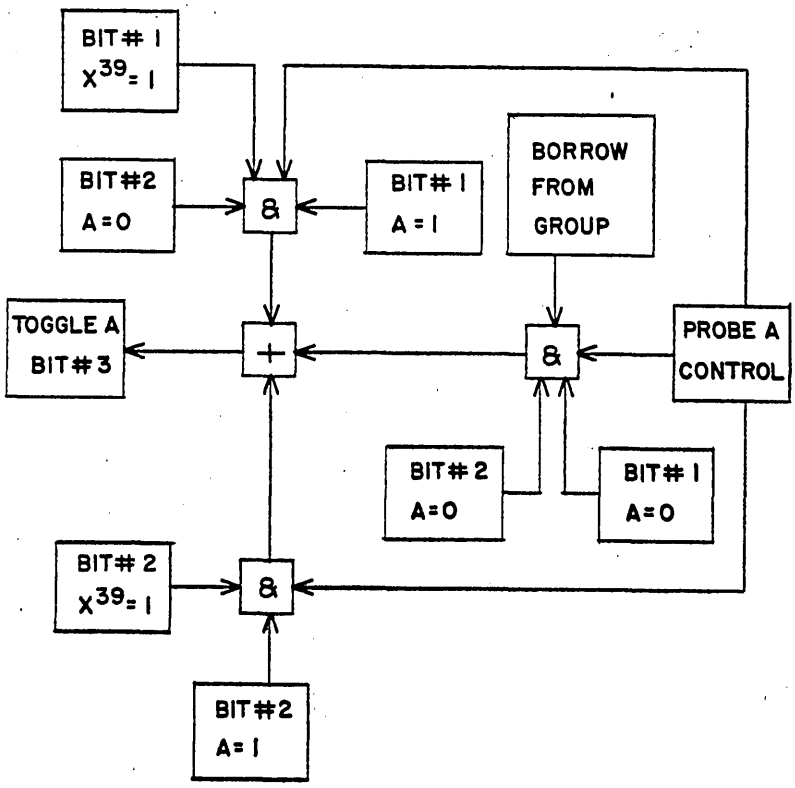
The second, third, and fourth groups in each half of the register are borrowed from if a preceding group generates a borrow and any intervening groups contain "0's". For illustrations of these groups see Examples 8, 9, and 10.

When a digit is borrowed from a bit, that bit is toggled. The first bit of a group is borrowed from only when the borrow from a preceding group is set as shown in Example 11. The borrows are completed when the probe control is set.

The second bit is borrowed from when the borrow from a preceding group is set and the first bit of A contains a "0", or when the first bits of A and X^{39} contain "1" as shown in Example 12.

The third bit receives a borrow when the borrow from a preceding group is set and bits 1 and 2 contain "0", or when A-bit 1 and X^{39}-bit 1 both contain "1" and A-bit 2 contains "0", or when A-bit 2 and X^{39}-bit 2 both contain "1". This is illustrated in Example 13.



Example 13

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g. ARITHMETIC SEQUENCES. - The computer can be programmed for any of the individual sequences or combinations of sequences of the following mathematical processes: addition, subtraction, multiplication, division, and logical products. Examples for each of the arithmetic sequences are given in the appropriate paragraph.

(1) ADDITION. - The basic unit operation of addition is perhaps the most important operation of the Arithmetic Section. The computer uses one's complement arithmetic in the arithmetic section except for the minus zero. In this system a negative number is represented by complementing each bit of a positive number. (See Volume 1, Appendix B, Number Systems .) For example, plus five is 000101 and minus five 111010. A negative zero (all "1's") causes subtractive errors in the accumulator; hence, the computer does not generate negative zero under normal arithmetical operations. In certain cases, using instructional means, a negative zero can be generated in the accumulator.

The fact that the Accumulator is of a subtractive nature tends to complicate the comprehension of addition. The apparent contradictory facts that A is subtractive and that a fundamental operation of the computer is addition can be reconciled by examining the rules of binary subtraction and the nature of the X^{39} to A transmission which inserts a number into the Accumulator.

Binary Subtraction Table

1-0=1	
1-1=0	
0-0=0	
0-1=1	with a borrow required from the next higher-order bit.

The above table shows that a "0" subtracted from either a "0" or a "1" does not alter the "0" or the "1" in any way; and a "1" subtracted from a "0"or a "1" in each case reverses the value of the bit, and in the case of "1" subtracted from "0", initiates a borrow from the next higher-order bit. If the

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results of the above table are applied to X and a subtractive A, rules for subtraction can be formulated as follows:

1) If no subtractive "1" signal is received from a stage in X, the state of the corresponding stage of A, whether "0" or "1", is not changed.

2) If a subtractive "1" signal is received from a stage in X, the state of the corresponding stage of A is reversed, and if a stage in A is changed from a "0" to a "1", a borrow is initiated from the next higher-order stage of A.

The operation of the main adder is best understood by taking an example and following it through to completion. The main adder, the X-register, and the A-register are shown in Drawings 87208, 87071, and 87070 respectively, (Volume 8, pages 29, 30, 18 and 17 respectively).

A typical example of one's complement addition, as shown in the following example, illustrates all the steps involved.

STEP 1. The Augend, octal number 2255, is located in the A-register.

STEP 2. The Addend, octal number 1504, is located in the X-register.

STEP 3. The formation of the complement of X is completed in X^{39}.

The third step in the addition process is the transfer of X to X^{39} buffer (refer to Drawing 87071). Here the value of X is completed so that X^{39} actually holds the complement of X. The original number still remains in the X-register and is not changed during the addition process.

RULES OF ADDITION

Rule 1. A bit in an Accumulator stage is changed from "0" to "1" or from "1" to "0" (complemented) only if the corresponding bit of the X-Register is "0".

Rule 2. A BIT BORROW is generated if a bit in an Accumulator stage is changed from "0" to "1", as a result of Rule 1.

Rule 3. A GROUP BORROW is generated if Rule 2 applies and in addition the higher-order stages of A (if any) within the group contain "0's".

Rule 4. A RAPID-BORROW is propagated to the next higher-order group if a GROUP BORROW SIGNAL is set.

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EXAMPLE OF ADDITION

Step	Group 4	Group 3	Group 2	Group 1	Register	Function
1.	0 1 0	0 1 0	1 0 1	1 0 1	A	AUGEND
2.	0 0 1	1 0 1	0 0 0	1 0 0	X	AUGEND
3.	1 1 0	0 1 0	1 1 1	0 1 1	X^{39}	-X in X^{39} buffer
4.	1 0 0	0 0 0	0 1 0	1 1 0	A	A=(-X); Toggle A
5.	1 0 0	0 0 0	0 1 0	1 1 0	A	Set bit-by-bit Borrow conditions
6.	1 0 0	0 0 0	0 1 0	1 1 0	A	Set Group Borrow conditions
7.	1 0 0	0 0 0	0 1 0	1 1 0	A	Probe A; complete borrows
8.	0 1 1	1 1 1	1 1 0	0 0 1	A	SUM

STEP 4. Every bit in A corresponding to a bit that contains a "1" in X^{39} is toggled. The fourth step in the addition process is actually a bit-by-bit subtraction, performed by application of the rules previously described. A signal toggles each bit in A that corresponds to a bit in X^{39} containing a "1". If any particular bit in X^{39} contains a 0 , its corresponding bit in A is not toggled and remains unchanged. Because X^{39} (complement of X) was used in the subtraction instead of X, it is apparent that the Add X to A signal effectively subtracts the complement of X, not the actual contents of X, from A. Since in one's complement binary notation the complement of a number is the negative of that number, the net result initiated by Add X to A can be expressed by the following notation:

$$A-(-X)=A+X$$

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This equation implies that even though A is subtractive, the overall operation initiated by Add X to A is additive. The 24th bit of A (Stage A_{23}) may be considered the sign bit. When the sign bit contains a "1", the number is considered negative; if the sign bit contains a "0" the number is considered positive.

Step 5. Setting of the Bit-by-Bit Borrow conditions. According to rule number 2 a borrow is necessary if a bit in the accumulator is changed from "0" to "1". Reproduced below are steps 1 and 4 from the example of addition.

	Group 4	Group 3	Group 2	Group 1	
Step 1	0 1 0	0 1 0	1 0 1	1 0 1	Augend in A-register
Step 4	1 0 0	0 0 0	0 1 0	1 1 0	Toggled A
	1		1	1	Bits changed from "0" to "1"
Step 5	1 0 0	0 0 0	0 1 0	1 1 0	Bit-by-bit borrow conditions

A bit-by-bit borrow situation is indicated by (↙).

Step 1 shows the original number in the A-register and Step 4 shows this number after being toggled by X^{39}. Three bits of A were changed from "0" to "1" and, therefore, according to rule 2, a borrow will be propagated to the next higher-order bit. The center bit of group 1 propagates a borrow to the left-most bit of group 1, and the center bit of group 2 attempts to obtain a borrow from the left-most bit of group 2. The left-most bit of the fourth group cannot borrow from a higher-order, so it sets a condition for a group borrow as shown below in Step 6. The logic for this bit-to-bit borrow is produced in the main adder. Whenever a "1" occurs in the corresponding bits of both the A-register after toggle and

the X^{39} buffer, a borrow signal is generated which toggles the next higher-order bit in A. If the next higher-order bit in A is "0" after the toggle in Step 4, that bit and the next higher-order bit will both be toggled.

STEP 6. Setting of the Group Borrow Condition. - Certain combinations of bits in each three-bit group of A and X^{39} produce a borrow which must be obtained from the next higher three-bit group. The signal produced by this condition is called a Group Borrow signal. The three combinations that produce group borrow signals in accordance with Rule 3 above are:

(1)	(2)	(3)	
1 - -	- 1 -	- - 1	X^{39}
1 - -	0 1 -	0 0 1	A-register after Toggle

In the addition example, the following combinations of X^{39} and A occur.

Group 4	Group 3	Group 2	Group 1	
1 1 0	0 1 0	1 1 1	0 1 1	X^{39}
1 0 0	0 0 0	0 1 0	1 1 0	A-register after Toggle A
(1)		(2)		Type Combination

Group 4 is an example of type (1) condition and group 2 is an example of type (2) condition, both of which produce group borrow signals. Notice that group 1 also generates a bit-by-bit borrow within the group, but since conditions favor satisfying the borrow within that group, no group borrow signal is generated. Any group such as group 3 with all zeros in A will produce an automatic group enable which allows the group borrow to be carried directly over to

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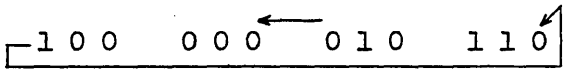
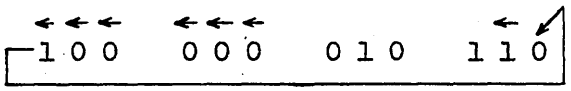
the next higher-order group. The following group borrows will occur as indicated by arrows (←——).



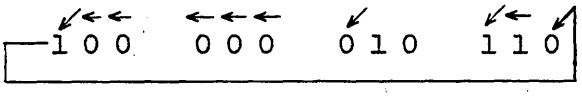
Group borrow conditions

These two group borrow conditions sense each bit, and where a "0" is stored it produces an enable which allows the borrow signal to be passed over to the next higher-order bit. The highest-order group produces an enable for an end-around borrow to the lowest-order bit. The completed group borrow conditions are illustrated below.



Set group borrow conditions

STEP 7. Probe A for completion of borrows. - In this operation each bit of A is probed to see if it has either a bit-by-bit borrow condition (↙) or a group borrow condition (←——) set.



Both bit-by-bit and group borrows

Each bit that has a borrow condition set on it is complemented by the probe A signal. When the bits having a borrow set are complemented the following sum is obtained:

STEP 8. 0 1 1 1 1 1 1 1 0 0 0 1 SUM

The final sum for the addition problem is in octal form and is found in the accumulator.

(2) SUBTRACTION. - The Subtract X from A routine is essentially the same as Add X to A except that the number in X^{39} buffer is not complemented.

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SUBTRACTION EXAMPLE

Step	Group 4	Group 3	Group 2	Group 1	Register	Function
1	0 1 1	1 1 1	1 1 0	0 0 1	A	Minuend
2	0 0 1	1 0 1	0 0 1	1 0 0	X	Subtrahend
3	0 1 0	0 1 0	1 1 1	1 0 1	ADDER	Toggle A (A-X)
4	0 1 0	0 1 0	1 1 1	1 0 1	ADDER	Bit-by-bit borrows set
5	0 1 0	0 1 0	1 1 1	1 0 1	ADDER	Set Group borrow condition
6	0 1 0	0 1 0	1 1 1	1 0 1	ADDER	Probe A; Complete borrows
7	0 1 0	0 1 0	1 0 0	1 0 1	A	Difference

STEP 1. The Minuend, octal number 3761, is located in the Accumulator.

STEP 2. The Subtrahend, octal number 1514, is located in the X-register.

STEP 3. Every bit in A corresponding to a bit in X that contains a "1" is toggled. The bits in A corresponding to 0 s in X are not toggled and remain unchanged.

STEP 4. A bit-by-bit borrow is necessary if a bit in the Accumulator is changed from a "0" to a "1". This condition is indicated by an arrow (↙). The left-most bit in group 1 meets the borrow condition but since there is no higher-order bit in the first group it is necessary to generate a group borrow. The first bit of group 2 meets the borrow condition and a borrow is set on the second bit of this group.

STEP 5. The group borrow generated above is shown xy an arrow (←——).

STEP 6. Probing of A for the completion of borrows is the last step. Each bit of A is sensed to see if it has either a bit-by-bit borrow condition (↙), or a group borrow condition set (←——). Each bit that has a borrow condition set is complemented by the probe A

signal.

STEP 7. The final difference for the subtraction problem, octal 2245, is found in the Accumulator.

(3) MULTIPLICATION. - Multiplication is accomplished by using the Repeat and Multiply steps. Since the machine is designed to multiply positive numbers only, the programmer must compensate for this when using numbers which are negative.

Binary multiplication consists of adding the partial products that were obtained from each bit of the multiplier. If the bit in the multiplier contains a "1", then the partial product is equal to the multiplicand; but if the bit in the multiplier contains a "0" the partial product is zero. An example follows:

BINARY MULTIPLICATION

010011	Multiplicand
011101	Multiplier
010011	Partial Product of first bit
000000	Partial Product of second bit
010011	Partial Product of third bit
010011	Partial Product of fourth bit
010011	Partial Product of fifth bit
000000	Partial Product of sixth bit
01000100111	Final Product

The multiply step process follows this logic by adding X (multiplicand) to A (partial product) when the right-most bit of Q, or Q_{00} (multiplier), contains a "1" and by leaving A unchanged when Q_{00} contains a "0". At the end of each multiply step, A and Q are shifted one place to the right with the right-most bit of A shifted into the left-most bit of Q and with Q_{00} shifted off the register.

The product is obtained by repeating the multiply step until every bit in the multiplier containing a "1" has been shifted off the Q-register. This leaves the product partially in A and Q.

If the multiply step is executed 24 times, the final product will be in Q with the higher-order bits extended in A. If the multiply step is executed less

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than 24 times, the A and Q-registers must be shifted to obtain the final product.

The multiplication operation can be explained better by following the example shown on the following page.

EXAMPLE 1.

Step	A-Register	Q-Register	X-Register
1.	0 0 0 0 0 0	0 1 1 1 0 1	0 1 0 0 1 1
2.	0 1 0 0 1 1	0 1 1 1 0 1	Q_{oo}=1, so add X to A (see additions)
3.	0 0 1 0 0 1	1 0 1 1 1 0	Right shift one and repeat
4.	0 0 1 0 0 1	1 0 1 1 1 0	Q_{oo}=0, so A is unchanged
5.	0 0 0 1 0 0	1 1 0 1 1 1	Right shift one and repeat
6.	0 1 0 1 1 1	1 1 0 1 1 1	Q_{oo}=1, so add X to A
7.	0 0 1 0 1 1	1 1 1 0 1 1	Right shift one and repeat
8.	0 1 1 1 1 0	1 1 1 0 1 1	Q_{oo}=1, so Add X to A
9.	0 0 1 1 1 1	0 1 1 1 0 1	Right shift one and repeat
10.	1 0 0 0 1 0	0 1 1 1 0 1	Q_{oo}=1, so add X to A
11.	0 1 0 0 0 1	0 0 1 1 1 0	Right shift one

At this point, an examination of the multiplier shows that we have completed the required number of Add X to A sequences, and additional Multiply Step operations will serve only to shift the contents of A and Q. Five of the required six right shifts have been completed, so that one right shift remains if the answer is to be in its correct numerical sequence.

Two alternatives present themselves. We may continue with the remaining Multiply Step operation, thus completing the required number of right shifts, or we may choose to shift left the appropriate number of places necessary to

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restore the answer to its correct form. Shifting right one place will give:

11.	0 1 0	0 0 1	0 0 1	1 1 0
12.	0 0 1	0 0 0	1 0 0	1 1 1

Right-shift one for final product

(Option I)

This is the correct answer. In order to obtain the same answer by left shifting, eleven shifts will be required:

11.	0 1 0	0 0 1	0 0 1	1 1 0
12.	0 0 1	0 0 0	1 0 0	1 1 1

Left-shift eleven for final product

(Option II)

Notice that the sum of the shifts in both the options was twelve (1 + 11). The option to choose is obviously the one with the least number of shifts (less than six in this case). For the case of the 24-bit registers, the sum would be 24, and the option to select would be that which was less than 12.

RULES OF MULTIPLICATION

1) If Q_{oo} contains a "1", add X to A and right shift A and Q.

2) If Q_{oo} contains a "0", right shift A and Q.

3) Repeat the multiply step until the multiplier has been shifted off the Q-register.

4) After the multiplier has been shifted off the Q-register, the final product is in A and Q, with the most significant bits in A.

STEP 1. The A-register is clear; the Q-register contains the multiplier, octal number 35; and the multiplicand, octal number 23, is found in the X-register.

STEP 2. The right-most bit or Q_{oo} contains a "1", so X (multiplicand) is added to A (partial product). The actual addition of X to A is discussed thoroughly in the addition section.

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STEP 3. A and Q are shifted right one place with the right-most bit of A being shifted into the left-most bit of Q and the right-most bit of Q shifted off the end. The multiply step is then repeated.

STEP 4. Since Q_{oo} contains a "0", A (Partial product) is left unchanged.

STEP 5. A and Q are shifted right and the multiply step is repeated.

STEP 6. Because Q_{oo} contains a "1", X is added to A.

STEP 7. A and Q are shifted right and the multiply step is repeated.

STEP 8. Q_{oo} contains a "1" so X is added to A.

STEP 9. A and Q are shifted right and the multiply step is repeated.

STEP 10. Since Q_{oo} contains a "1", X is added to A.

STEP 11. A and Q are shifted right. Since all the bits of the multiplier containing a "1" have been shifted off the register, the multiply step need not be repeated.

STEP 12. (Option I) Since but one right-shift remains to put the product in its final form, the multiply step is repeated.

STEP 12. (Option II) A and Q were shifted to the right five places, so A and Q are circularly long-shifted left a total of five places, plus the number of places in the Q-register (6), or a total of 11.

STEP 13. The final product, octal number 1047, is found in the A and Q registers, with the lower-order bits being in Q.

A-register		Q-register		
0 0 1	0 0 0	1 0 0	1 1 1	binary
1	0	4	7	octal

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We may convert this octal answer to its decimal equivalent by use of the octal-to-decimal conversion table:

$8^4 = 4096$

$8^3 = 512$

$8^2 = 64$

$8^1 = 8$

$8^0 = 1$

thus:

8^3	8^2	8^1	8^0
1	0	4	7

becomes:

$8^3 = 512 \cdot 1$ or 512

$8^2 = 64 \cdot 0$ or 0

$8^1 = 8 \cdot 4$ or 32

$8^0 = 1 \cdot 7$ or 7

adding:

$$\begin{array}{r} 512 \\ 32 \\ 7 \\ \hline 551 \end{array} = 19{\cdot}29$$

(4) DIVISION. - Division is accomplished by executing the divide step the same number of times as the total number of bits in the Q-register. Since negative numbers introduce errors when divided, the programmer must compensate for negative numbers.

In division, the quotient tells how many times the divisor is contained in the dividend. To carry out the divide operation the divisor is simply subtracted from the left-most bit of the dividend or the first partial dividend. If the remainder is zero or positive, the divisor must have been contained once

in that partial dividend and so a "1" could be placed in the left-most bit of the quotient. Then the left-most bit of the dividend is placed on the right of the remainder, forming the next partial dividend to be opereated on.

If the remainder were negative, the divisor was greater than that partial dividend and the quotient must contain a "0" in the left-most bit, signifying that the divisor was not contained in that partial dividend. Then, the negative remainder is added to the divisor to obtain the original partial dividend and the left-most bit of the dividend is placed on the right of the partial dividend to obtain the next partial dividend.

The division operation performed by the machine adheres closely to the preceding logic. Since there is a slight deviation, a Bogart division operation will be followed through to completion in Binary Division - Example 2. Since the Q-register in the example is a six-bit register, the divide step must be repeated six times. The adding and subtracting involving X and A are thoroughly explained in the addition and subtraction sections.

STEP 1. The A-register is clear; the Q-register contains the dividend, octal number 50, and the X-register contains the divisor, octal number 3.

STEP 2. A and Q are long-shifted one place with the left-most bit of Q shifting into the right-most bit of A. This puts the first partial dividend in A.

STEP 3. X (divisor) is subtracted from A (partial dividend) to find if A is larger than X. Since A_{05} (sign bit) contains "1", the difference of X from A is negative and X is greater than A. When X is greater than A, the corresponding bit of Q or Q_{00} remains a "0". During this step the partial dividend has been changed to a negative number.

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BINARY DIVISION - EXAMPLE 2

Step	A-Register	Q-Register	X-Register
1	0 0 0 0 0 0	1 0 1 0 0 0	0 0 0 0 1 1
2	0 0 0 0 0 1	0 1 0 0 0 0	Long Shift A and Q one
3	1 1 1 1 0 1	0 1 0 0 0 0	Subtract X from A, A_{05}=1
4	0 0 0 0 0 1	0 1 0 0 0 0	Add X to A (Restore)
5	0 0 0 0 1 0	1 0 0 0 0 0	Long Shift A and Q one
6	1 1 1 1 1 0	1 0 0 0 0 0	Subtract X from A, A_{05}=1
7	0 0 0 0 1 0	1 0 0 0 0 0	Add X to A (Restore)
8	0 0 0 1 0 1	0 0 0 0 0 0	Long Shift A and Q one
9	0 0 0 0 1 0	0 0 0 0 0 1	Subtract X from A, A_{05}=0 so set Q_{00} to 1
10	0 0 0 1 0 0	0 0 0 0 1 0	Long Shift A and Q one
11	0 0 0 0 0 1	0 0 0 0 1 1	Subtract X from A, A_{05}=0 so set Q_{00} to 1
12	0 0 0 0 1 0	0 0 0 1 1 0	Long Shift A and Q one
13	1 1 1 1 1 0	0 0 0 1 1 0	Subtract X from A, A_{05}=1
14	0 0 0 0 1 0	0 0 0 1 1 0	Add X to A (Restore)
15	0 0 0 1 0 0	0 0 1 1 0 0	Long Shift A and Q one
16	0 0 0 0 0 1	0 0 1 1 0 1	Subtract X from A, A_{05}=0 so set Q_{00} to 1
17	0 0 0 0 0 1	0 0 1 1 0 1	Final quotient and remainder

RULES OF DIVISION

1. Long shift A and Q one to obtain partial dividend.
2. Subtract X from A. If A is positive set Q_{00} to "1". If A is negative, leave Q_{00} set to "0" and add X to A.
3. Repeat the Divide step as many times as there are bits in Q (24).

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STEP 4. Since the partial dividend cannot be negative, X is added to A, thus giving the original partial dividend. Divide step is now repeated.

STEP 5. A and Q are long-shifted one place to the left putting the second partial dividend in A.

STEP 6. Subtract X from A. Since A_{05} contains a "1", A is less than X so Q_{00} remains a "0".

STEP 7. Add X to A to get a positive partial dividend and repeat divide step.

STEP 8. A and Q are long-shifted left to put the third partial dividend in A.

STEP 9. Subtract X from A. A is equal to or greater than X because A_{05} contains a "0", so Q_{00} must be set to "1". Then the divide step is repeated.

STEP 10. Since A is still positive, X is not added to A. Shift A and Q left one place to obtain the fourth partial dividend.

STEP 11. Subtract X from A. A_{05} is "0", so set Q_{00} to "1" and repeat divide step.

STEP 12. Shifting A and Q left puts the fifth partial dividend in A.

STEP 13. After subtracting X from A, A_{05} contains a "1", so let Q_{00} remain "0".

STEP 14. Add X to A to get the positive partial dividend and repeat divide step.

STEP 15. The sixth partial dividend is placed in A, after A and Q are long-shifted one place to the left.

STEP 16. Subtracting X from A makes A_{05} a "0". Therefore, Q_{00} must be set to "1". Since the divide step has been repeated six times, the

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operation is completed except for finding the positive remainder.

STEP 17. If A_{05} contained a "0" after step 16, then A contains the remainder; but if A_{05} contains a "1", then X must be added to A to give the remainder. The final quotient, octal number 15, is found in Q with the remainder, octal number 1, found in A.

(5) LOGICAL PRODUCT. - The logical product is the result of a bit-by-bit multiplication. In other words a "0" times either a "1" or "0" puts a "0" in the corresponding bit, while "1" times "1" puts a "1" in the corresponding bit. An example of the logical product is given below:

ORIGINAL

X-register	1 1 0 0	(Logical multiplicand)
Q-register	1 0 1 0	(Logical multiplier)

FINAL

X-register	1 0 0 0	(Logical product)
Q-register	(unchanged)	

The operation of L(Q)(X) circuitry is described in the section under Arithmetic Sequence Controls.

h. ARITHMETIC SEQUENCE CONTROLS. - The Arithmetic Sequence Controls are a collection of eleven sequence generating circuits. Each of these circuits directs the execution of a whole or part of an arithmetic sequence. All of these controls are shown on the Command Logic Diagrams in Volume 8.

(1) X to X^{39} BUFFER CONTROL. - The X^{39} core contains the information in X or its complement at all times. The information in X is sent to X^{39} during every clock cycle but when the appropriate controls are set (shown in Drawing 87071, Volume 8, page 18, and Drawing 87309, Volume 8, page 6) this information is complemented before X^{39} is read out. This is accomplished by setting all X^{39} bits to "1" and then negating any bit of X^{39} where X^{20} contains

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a "1". Core V^{30}_{83}, set only when E^{20}_{70} (instructions 11, 12, 14, 3X, 44, 51, 60 62), E^{10}_{71} (instruction 24), or E^{20}_{72} (instructions 45, 47, 61, 64, 65, 66, 67) is enabled, initiates the complement of X in X^{39}. It enables the Set X to 1 controls (N^{13}_{06}, N^{00}_{06}) and then sets the Negation of X^{39} control (N^{00}_{07}), thus putting the complement of X in X^{39}.

(2) TOGGLE A CONTROL. - The Toggle A sequence, shown in Drawing 87209, Volume 8, page 6, and Drawing 87208, Volume 8, pages 29 and 30, complements a bit in A whenever the corresponding bit of X^{39} contains a "1". The Toggle A enables a "1" in X^{39} to set the corresponding bit of A to "1" unless that bit of A already contains a "1", in which case the bit is cleared. The Toggle A control (N^{10}_{09}) is set only after the Toggle A circulation bit (W^{00}_{17}- W^{20}_{17}) is set, when E^{30}_{79} (instructions 34, 44, 62) is enabled, or when Load Mode is selected. The Toggle A circulation bit can be set only if E^{20}_{16} (instructions 35, 36, 37, 45, 46, 47), E^{20}_{18} (instructions 11, 31, 41, or Load Mode), or E^{30}_{19} (instructions 12, 32, 33, 34, 35, 37, 42, 43, 44, 45, 47, 52, 56, 60, 61, 62, 64, 65, 66, 67) is enabled or after the Logical (Q) (X) circulation bit has been set. The Toggle A control enables X^{39} to set H^{06}, which puts a "1" in A^{20}. If A already contains a "1", H^{06} will AND with A^{00} to set H^{17}, which negates A^{20}.

(3) PROBE A CONTROL. - The Probe A control, shown in Drawing 87209, Volume 8, page 6, and Drawing 87308, Volume 8, pages 29 and 30, enables a borrow condition in the main adder, (as described under adder) to toggle the corresponding bit of A. The Probe A circulation bit (W^{00}_{18}- W^{20}_{18}) is set only when E^{30}_{20} (instructions 11, 12, 3X, 4X, 51, 55, 60, 61, 64, 65, 66, 67) or E^{30}_{21} (instruction 14) is enabled. The next command step clears Probe A circulation bit and sets Probe A control (N^{10}_{08}) enabling borrows to be completed.

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(4) COMPLEMENT A CONTROL. - The Complement A sequence, shown in Drawing 87685, Volume 9, page 13, and Drawing 87209, Volume 8, page 6, complements the contents of the A-register, but the complement of positive zero (A-register contains all "0's") remains positive zero. A negative zero (A-register contains all "1's") introduces errors in computation and is not formed in the A-register by complementation. If any bit of A contains a "1" all the bits of A will be toggled, but if no bit in A contains a "1", none of the bits in A will be toggled. The Complement A sequence is carried out by setting Probe A control through enabling E^{30}_{21} (instruction 14), then setting each bit of X^{39}, thus putting a borrow condition on every bit of A whenever any bit of A contains a "1". Then the Probe A control (N^{10}_{08}) is set and every bit of A is complemented. If no borrow conditions were set, A remains positive zero.

(5) SET A TO PLUS ONE CONTROL. - The Set A to Plus One sequence, shown in Drawing 87209, Volume 8, page 6, clears A and X, sets the first bit of X^{39} to "1", and then enables the Toggle A control, which complements the first bit of A, setting it. In this sequence, the first bit of X^{39} is set during every clock cycle by E^{30}_{75} (instructions 14, 34, 62).

The Normal Circulation of X control (N^{20}_{11}) is negated when E^{00}_{76} (instructions 14, 34, 44, 62) is enabled. The Normal Circulation of A control (N^{20}_{00}) is negated when E^{30}_{78} (instructions 34, 44) is enabled. Then E^{30}_{79} (instructions 34, 44, 62) enables the Toggle A control (N^{10}_{09}) to be set which in turn allows the first bit in A to be toggled, making the value of A equal to plus one.

(6) SET A TO MINUS ONE CONTROL. - The Set A to Minus One sequence, shown in Drawing 87209, Volume 8, page 6, clears A and X, sets all but the first bit of X^{39}, and then enables the Toggle A control which complements every bit of A except the first bit, thus giving A the value of minus one.

In this sequence E^{30}_{74} (instructions 14, 44, 62) sets every bit of X^{39},

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except the first bit, to one during each clock cycle. The Normal Circulation of X control (N^{20}_{11}) is negated when E^{00}_{76} (instructions 14, 34, 44, 62) is enabled.

The Normal Circulation of A control (N^{20}_{00}) is negated when E^{30}_{78} (instructions 34, 44) is enabled. Then E^{30}_{79} (instructions 34, 44, 62) enables the Toggle A control (N^{10}_{09}) to be set. This in turn allows every bit but the first bit in A to be toggled, making the value of A equal to minus one.

(7) A TO X CONTROL. - The A to X sequence, shown in Drawing 87209, Volume 8, page 6, transmits information from A to X. This transmission is permitted when E^{10}_{32} (instructions 13, 26, 53, 57), E^{30}_{73} (instruction 62), E^{30}_{41} (instructions 33, 34, 36, 37, 43, 44, 46, 47, 55) or E^{30}_{22} (instructions 54, 56, 57) is enabled. When any one of these cores is enabled, the Normal Circulation of X control (N^{00}_{10}) is negated, thus clearing X to zero, and the A to X control (N^{00}_{13}) is set, thus enabling the transmission of A to X.

(8) SET Q_{00} CONTROL. - The Set Q_{00} sequence, shown in Drawing 87209, Volume 8, page 7, comes during Divide Step whenever X is subtracted from A and the difference is positive. Therefore, the Set Q_{00} to One control (N^{20}_{18}) is enabled only when E^{00}_{26} (instruction 61) and positive A (A^{39}_{23}) are both present.

(9) Q to X CONTROL. - The Q to X sequence, shown in Drawing 87209, Volume 8, page 6, transmits information from Q to X. This transmission is permitted only when E^{10}_{15} (instructions 23, 24, 35, 36, 37, 45, 46, 47) is enabled or during an input operation (V^{00}_{66}). When one of these conditions exists, the Normal Circulation of X control (N^{00}_{10}) is negated, clearing X to zero, and the Q to X control (N^{30}_{23}) is set, enabling Q to be transmitted to X. During an output instruction, the contents of the lower six bits of Q are sent to X. This is accomplished by first setting the Q to X circulation bit (W^{10}_{27} - W^{30}_{27}). Then the next command step (G^{10}_{50}) after the contents of K are zero

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(V^{10}_{05}) enables N^{13}_{23} (Q_{0-5} to X control) to be set, which transfers the contents of the lower six bits of Q to the X-register.

(10) X TO Q CONTROL. - The X to Q sequence, shown in Drawing 87209, Volume 8, page 7, transmits information from X to Q. The X to Q circulation bit (W^{00}_{25}- W^{20}_{25}) can be set only when E^{20}_{43} (instruction 26), E^{20}_{67} (instruction 21), E^{20}_{62} (instruction 24) or E^{20}_{68} (instructions 22, 72) is enabled. The next command step after the X to Q circulation bit is set clears X to Q (W^{20}_{25}), negates the Normal Circulation of Q control (N^{20}_{24}), and sets the X to Q control (N^{20}_{26}) thus enabling X to be transmitted to Q.

(11) LOGICAL PRODUCT OF (Q) AND (X) CONTROL. - The logical product of (Q) and (X), shown in Drawing 87209, Volume 8, page 7, and Drawing 87071, Volume 8, page 18, allows a bit of X to remain in the "1" state when both that bit and the corresponding bit of Q contain a "1". If any bit in X or its corresponding bit in Q contains a "0", then that bit in X is cleared. The Logical (Q)(X) circulation bit (W^{00}_{24}- W^{20}_{24}) can be set only when E^{20}_{29} (instructions 53, 57) or E^{30}_{30} (instructions 50, 51, 53, 54, 55, 57) is enabled. The next command step pulse after the Logical (Q)(X) circulation bit has been set clears the Logical (Q)(X) circulation bit (W^{20}_{24}), negates the Normal Circulation of X control (N^{00}_{10}), and sets the Logical Products of Q and X controls (N^{10}_{12}, N^{11}_{12}, N^{12}_{12}) through V^{30}_{62}. These controls enable Q^{10} to AND with X^{10} which sets X^{20}, thus completing the logical product sequence.

4-4. STORAGE SECTION

The storage section consists of: a Storage Address Register (S), the Storage Transfer Register (Z), the Memory Access Control Section, the Digit Plane Control Section, and the Magnetic Core Memory Plane Assembly. (See Magnetic Core Storage System Logical Diagram 87000, Volume 8, page 35.) Each of the

memory planes has 4096 magnetic cores which are capable of storing either "1" or a "0".

a. STORAGE ADDRESS REGISTER. - The Storage Address Register (S) contains the address at which a memory word is located. It transmits this address, which designates the correct X and Y lines to be energized, to the MCS current diverters. This register receives information from either the U-register or P-register. The S-register receives information from the U-register through the P-register. Additional information on the S-register is given under the section on Control in the Theory of Operation (Volume 2), paragraph d(4), and in Drawing 87073, Volume 8, page 20.

b. STORAGE TRANSFER REGISTER. - The Storage Transfer Register (Z), shown in Drawing 87072, Volume 8, page 19, is used as a memory buffer. During all MCS sequences, the contents of the memory are transferred through the Z-register. During the Write sequence a partial transmission of X to Z can be performed, depending upon the value of m. This storage Field Designator, m, permits the partial changing of the contents of a storage address. During the Read sequence, a partial transmission of Z to X can also be performed, depending upon the value of m. This permits the transfer of a portion of memory to X, or a portion of memory to X, or a portion of X to memory.

(1) BASIC PROPERTIES OF Z. - The basic elements of each stage are three magnetic switch cores. Figure 4-38 is a reproduction of the fourth stage of the Z-register.

(a) CORE Z^{00}. - This core receives information from X under the control of the N_{71} cores. It also sends information to the Start Inhibit cores (R^{10}) and to the X-register when m = 0m 0, or m = 4.

(b) CORE Z^{20}. - This core receives information from P and can be set manually by the pushbutton on the indicator display panel. The P to Z

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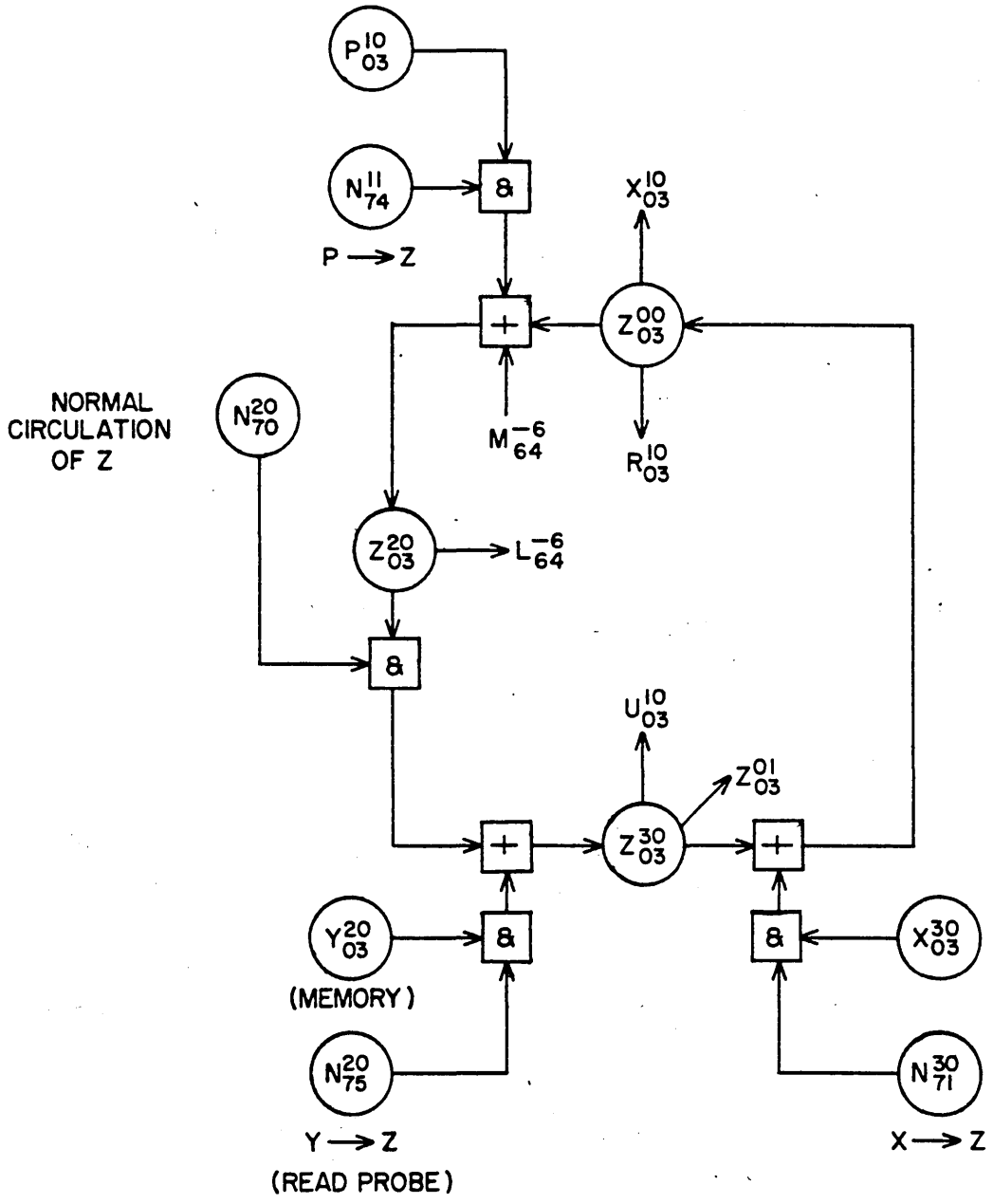

FOURTH STAGE OF Z—REGISTER

EQUATION

$$Z^{00}_{03} = X^{30}_{03}\ N^{30}_{71} + Z^{30}_{03}$$

$$Z^{20}_{03} = P^{10}_{03}\ N^{11}_{74} + M^{-6}_{64} + Z^{00}_{03}$$

$$Z^{30}_{03} = Y^{20}_{03}\ N^{20}_{75} + Z^{20}_{03} + N^{20}_{70}$$

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Figure 4-38. Fourth Stage of Z-register

transfer is controlled by the N_{74} cores. Core Z^{20} also sends information to the light on the Indicator Display panel.

(c) CORE Z^{30}. - Information received by this core comes from memory under the control of the N_{75} cores. This core sends information to the U-register and, depending upon the value of m, to the Q^{01} cores (see Z-register buffer, below).

(2) Z-REGISTER BUFFER. - The Z-register buffer contains the Z^{01}, Z^{02}, and Z^{03} cores. These cores operate during partial transmissions between memory and X (i.e., whenever the field designator m is not 0 or 4). The Z-register buffer is shown in Drawing 87072.

(a) CORES Z^{01}_{00} ... Z^{01}_{07}. - These cores receive information from the stages in Z which hold the bits to be transferred to the eight lower-order positions of X. For example, when m = 1 or 5, Z^{01}_{00} receives information from Z^{30}_{00}; when m = 2 or 6, Z^{01}_{00} receives information from Z^{30}_{08}; when m = 3 or 7, Z^{01}_{00} receives information from Z^{30}_{16}.

These cores send information to the corresponding eight stages of X. In addition, Z^{01}_{07} has outputs to stages 08 through 11 of the X-register as part of the bit-extension feature incorporated in partial transmissions where m = 1, 2, or 3.

(b) CORES Z^{02}_{07}, Z^{03}_{07}. - These two cores receive information from the Z^{30} core which contains the highest-order bit in the eight-bit group currently being transmitted to X. In effect, they produce, along with the supplemental outputs from Z^{01}_{07}, a 16-bit extension of the information contained in Z^{01}_{07}.

(3) TRANSMISSION TO AND FROM Z. - Before transmissions to Z, the register is always cleared by the N_{70} cores.

(a) Z TO X. - During the Read sequence the Z to X transfer can

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lower eight different paths. All 24-bits of Z can be sent to X, the lower 15 bits of Z can be sent to X, or any eight-bit third of Z can be sent to the lower eight bits of X. When a third of Z is transferred to the X-register, the upper bits of X can be made all "1's" or all "0's". See Storage Field Designators, m, as listed below.

If m = 0, transfer the entire 24-bit word from Z to X.

If m = 1, transfer a 24-bit word from Z to X whose lowest-order eight bits correspond to the right eight bits of the word in storage and whose higher-order bits are the same as the eighth bit.

If m = 2, transfer a 24-bit word from Z to X whose lowest-order eight bits correspond to the center eight bits of the word in storage and whose higher-order bits are the same as the sixteenth bit.

If m = 3, transfer a 24-bit word from Z to X whose lowest-order eight bits correspond to the left eight bits of the word in storage and whose higher-order bits are the same as the twenty-fourth bit.

If m = 4, transfer a 24-bit word from Z to X whose lowest-order 15 bits correspond to the right 15 bits of the word in storage, and whose highest-order nine bits are zero.

If m = 5, transfer a 24-bit word from Z to X whose lowest-order eight bits correspond to the right eight bits of the word in storage and whose higher-order bits are zero.

If m = 6, transfer a 24-bit word from Z to X whose lowest-order eight bits correspond to the center eight bits of the word in storage and whose higher-order bits are zero.

If m = 7, transfer a 24-bit word from Z to X whose lowest-order eight bits correspond to the left eight bits of the word in storage and whose higher-order bits are zero.

(b) X TO Z. - During the Write sequence the X to Z transfer can follow five different paths. All 24 bits of X can be sent to Z, the lower 15 bits of X can be sent to Z, or the lower eight bits of X can be sent by any eight-bit third of Z. These paths are determined by m as listed below:

If m = 0, write a 24-bit word corresponding to the 24-bit word in the X-register.

If m = 1 or 5, write a 24-bit word with the right eight bits corresponding to the right eight bits of the X-register and the other bits remaining the same as in the original word in memory.

If m = 2 or 6, write a 24-bit word with the middle eight bits corresponding to the right eight bits of the X-register and the other bits remaining the same as in the original word in memory.

If m = 3 or 7, write a 24-bit word with the left eight bits corresponding to the right eight bits of the X-register and the other bits remaining the same as in the original word in memory.

If m = 4, write a 24-bit word with the right 15 bits corresponding to the right 15 bits of the X-register and the other bits remaining the same as in the original word in memory.

(c) STORAGE TO Z. - Any word, or portion thereof, which is to be retained in storage must, during the storage reference (memory) cycle, be transferred to Z for subsequent restoration in memory. Bits not so transferred will be lost. During the Write sequence these latter bits are replaced with designated portions of the word in the X-register, as explained above. During Write, therefore, the Storage to Z transfer has five options whereby only

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those bits which it is desired to restore to memory in their original state are transferred to Z:

If m = 0, no bits are transferred (entire word replaced).

If m = 1 or 5, all but the right eight bits are transferred.

If m = 2 or 6, all but the middle eight bits are transferred.

If m = 3 or 7, all but the left eight bits are transferred.

If m = 4, only the left nine bits are transferred.

During the Read sequence the entire word is read out of Storage into Z, and options such as those shown above are not needed.

c. MAGNETIC CORE STORAGE SYSTEM. - The Bogart Magnetic Core Storage System (MCS) is a non-volatile, high-speed, random-access storage medium consisting of 24 core memory planes, each containing 4096 magnetic cores, and the associated addressing and driving circuits. Each of the core memory planes is connected to a corresponding stage of the Z-register. The MCS system has a capacity of 4096 24-bit words, each of which is individually addressed. The storage addresses assigned to MCS are 0000 through 7777, inclusive, in octal notation. In addition, it is possible virtually to triple the number of unique addresses through the use of a storage field designator which permits storage of three individually addressed eight-bit words in each 24-bit memory location.

(1) GENERAL. - Each bit of the 24-bit Z-register is connected to an individual core memory plane consisting of 4096 magnetic cores. Information is always transferred from the Z-register to an MC address on an MC Write operation, and information is always transferred from an MC address to the Z-register on an MC Read operation.

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The Magnetic Core Storage System is shown on Drawing 87000, Volume 8, page 35, and on Drawing 87001, Volume 8, pages 36 and 37. The MC System consists of the following five principal sections:

1) The Magnetic Core Memory Plane Assembly (28 4096-core Memory Planes)

2) The Memory Timing Chain

3) The Magnetic Core Storage Address Location System

4) The Magnetic Core Access Control

5) Digit Plane Control Section

The Magnetic Core Memory Plane Assembly consists of 28 separate core memory planes of 4096 magnetic cores assembled on an etched circuit board with their associated X and Y drive lines, inhibit line, and sense line. Four planes, whose sense and inhibit lines are not connected, are used as spares. However, the X and Y drive lines of the spare memory planes are connected, since the drive lines of all planes are connected in series. Each memory plane has 64 X drive lines and 64 Y drive lines (see Figure 4-39). The sense line threads each core of the memory plane once in a symmetrically balanced arrangement so as to achieve maximum cancellation of noise outputs from partially selected cores.

The Memory Timing Chain consists of twelve basic magnetic switch core transfer circuits which control the Read and Write operations of the Magnetic Core Storage System. Additional magnetic switch core circuits under the control of the Memory Timing Chain are used to control the read probe, start inhibit, and start disturb functions.

The MCS address location system operates on the 12-bit binary address from the S-register to select one X and one Y drive line which intersect at the storage location being addressed.

The Magnetic Core Access Control system and the X and Y drive line translation system are controlled by the Memory Timing Chain. The Read and Write pulses for the X and Y drive lines are induced in the secondary winding of a

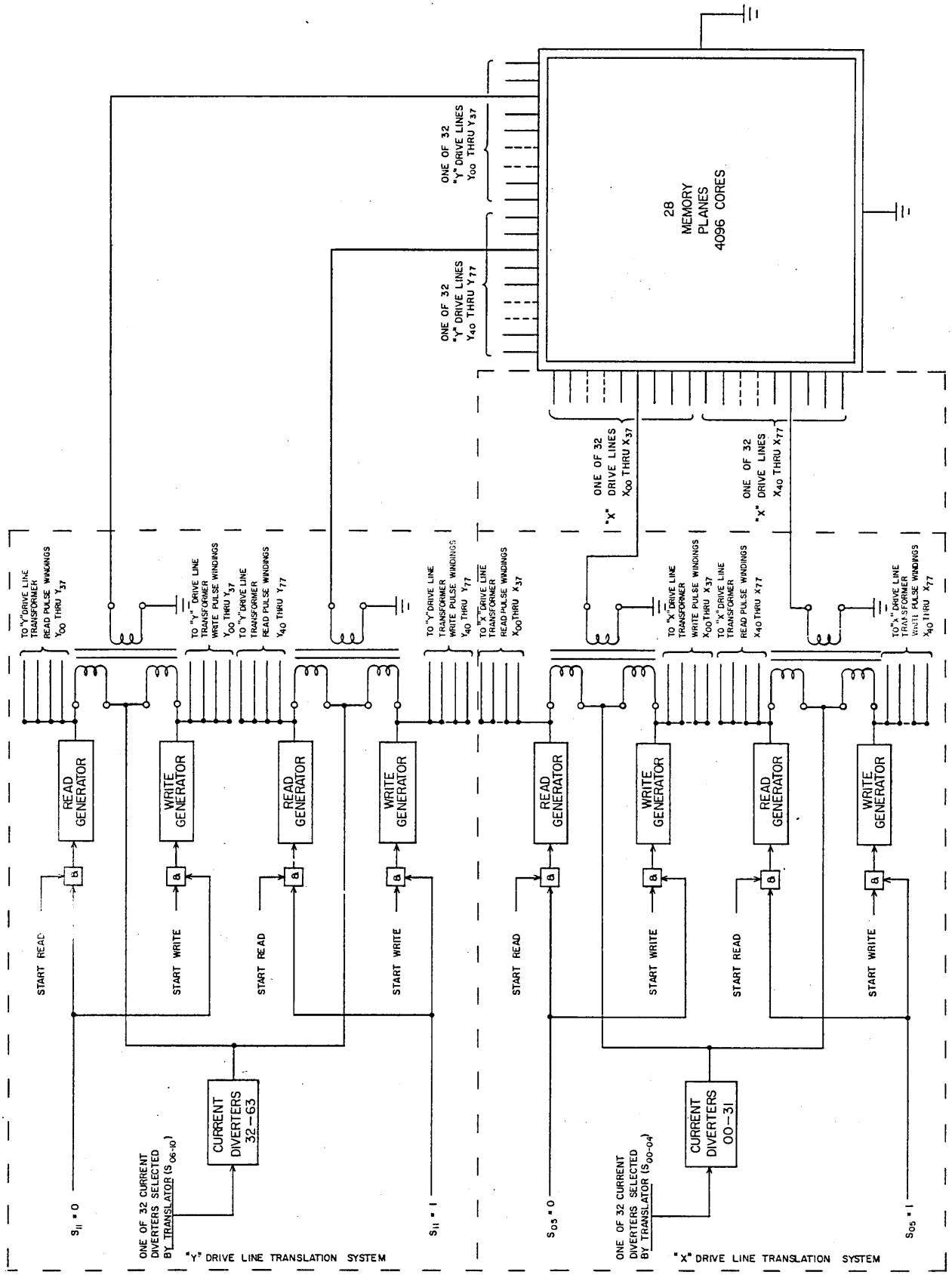

Figure 4-39. X and Y Drive Lines

drive line transformer. The X and Y Read/Write current generator circuits are part of the X and Y drive line translation system. A simplified diagram of the X and Y drive line system is shown in Figure 4-39.

There are 64 X drive line transformers and 64 Y drive line transformers. The primary winding of each X and Y drive line transformer has two sections: one for the Read Current pulse, and one for the Write Current pulse. The MCS address translation system is divided into two identical sections: one for the X drive lines, and one for the Y drive lines. The six bits controlled by cores S^{00}_{00} to S^{00}_{05} are used to select the X drive lines, and the six bits controlled by cores S^{00}_{06} through S^{00}_{11} are used to select the Y drive lines. The lower-order five bits of the MCS address which control the X drive line selection are used to turn on the current diverter connected to the two drive lines designated by the binary numbers whose lower-order five bits are identical. The sixth bit of the MCS address for the X and Y drive lines is used to turn on a current generator which completes the final selection. The lower-order five bits of the X portion of the MCS address and the lower-order five bits of the Y portion of the MCS address turn on a current diverter which is connected to the primary winding of two separate drive line transformers. The highest-order bits of the X and Y drive line portions of the MCS address are used to turn on the Read and the Write current generators connected to the other ends of the primary winding of the selected drive line transformers. Thus, only one X and one Y drive line are selected during each MCS reference.

The Digit Plane Control, under the control of the Z-register, controls the writing of a "0" or a "1" in a particular plane by turning the inhibit/disturb current generator to ON or OFF. The Inhibit Current pulse is turned on when writing a "0" in a core and is not turned on when writing a "1" in a core. The Disturb Current pulse is automatically turned on at the end of every MCS

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reference. During a MCS Write operaton the Z-register communicates directly with the Digit Plane Control. When the addressed core is read out during a Read operation, the sense "1" signal sets the Z-register circulation bit to "1". The Z-register in turn controls the Restore step of the Read operation.

Each core is a small toroid of ferrite material possessing an almost rectangular hysteresis loop. Four wires pass through each core as shown in Figure 4-40: a vertical X wire, a horizontal Y wire, a diagonal S wire, and a horizontal I wire. The core is a bistable device capable of storing a "1" or a "0", depending upon the state of remanent magnetization of the core. In general, the "1" state is produced in a core when the resultant magnetizing force of coincident current pulses on the X and Y wires is of one polarity through the core. The "0" state is produced when the resultant magnetizing force of coincident current pulses on these wires is of the opposite polarity through the core.

Reading or writing is accomplished by a sequence of current pulses through the matrix wires. The specific pulse sequences for reading or writing both a "1" and "0" are shown in Figures 4-41 through 4-46. It should be noted that the waveforms and hysteresis loops in Figures 4-41 through 4-46 are exaggerated so that the actual operation paths of the minor hysteresis loops can be shown. In actual operation, the change in the remanent state of magnetization in the core for half-magnitude pulses is very small, and points L and H, and F and D are very close together.

When information is read out of a magnetic core memory address the core is forced to the "0" state as shown in Figures 4-45 or 4-46. If the interrogated core is initially in the "0" state, a very small output signal is generated, because the remanent state of magnetization of the core is changed very little. If the interrogated core is initially in the "1" state, a large output

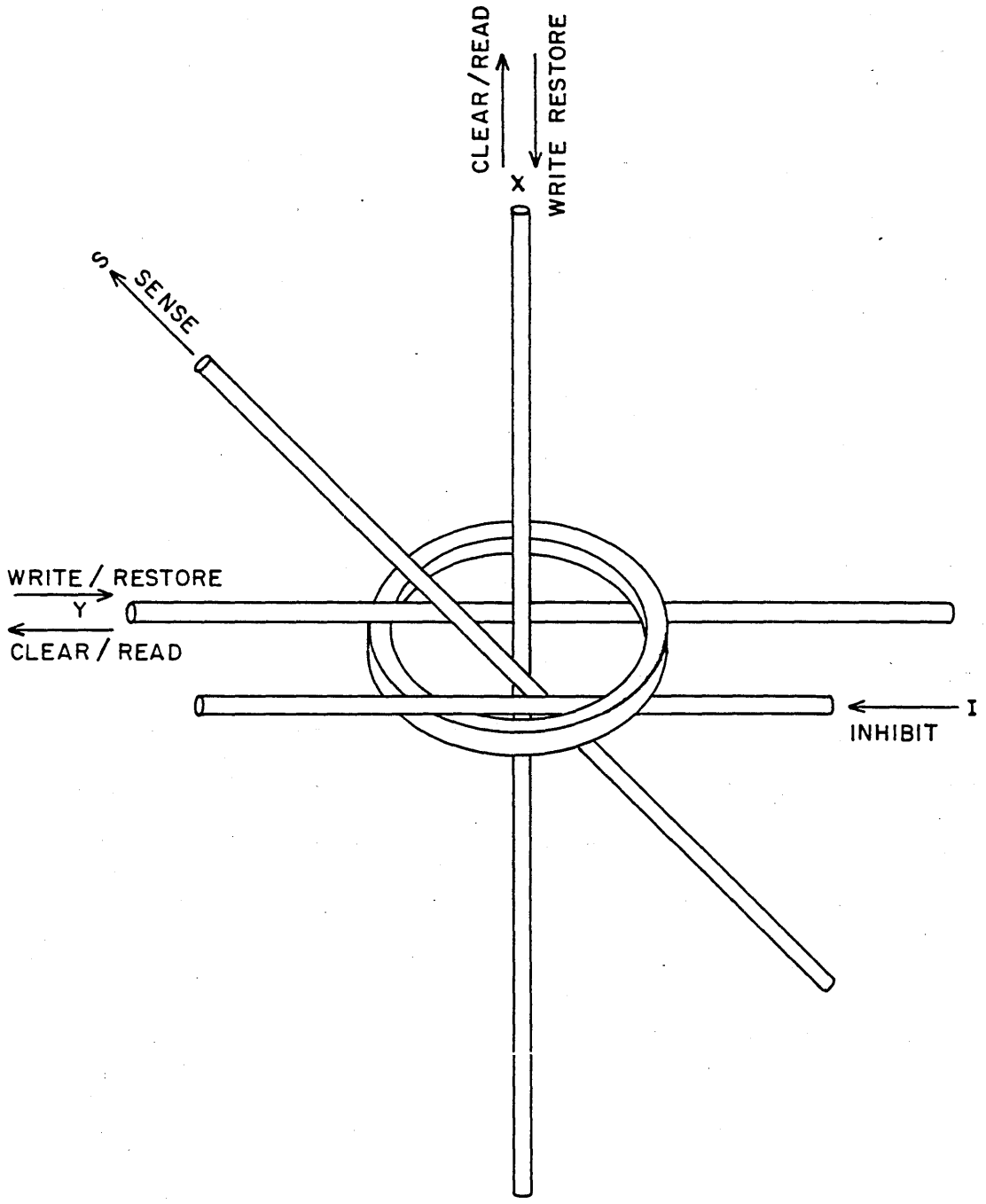

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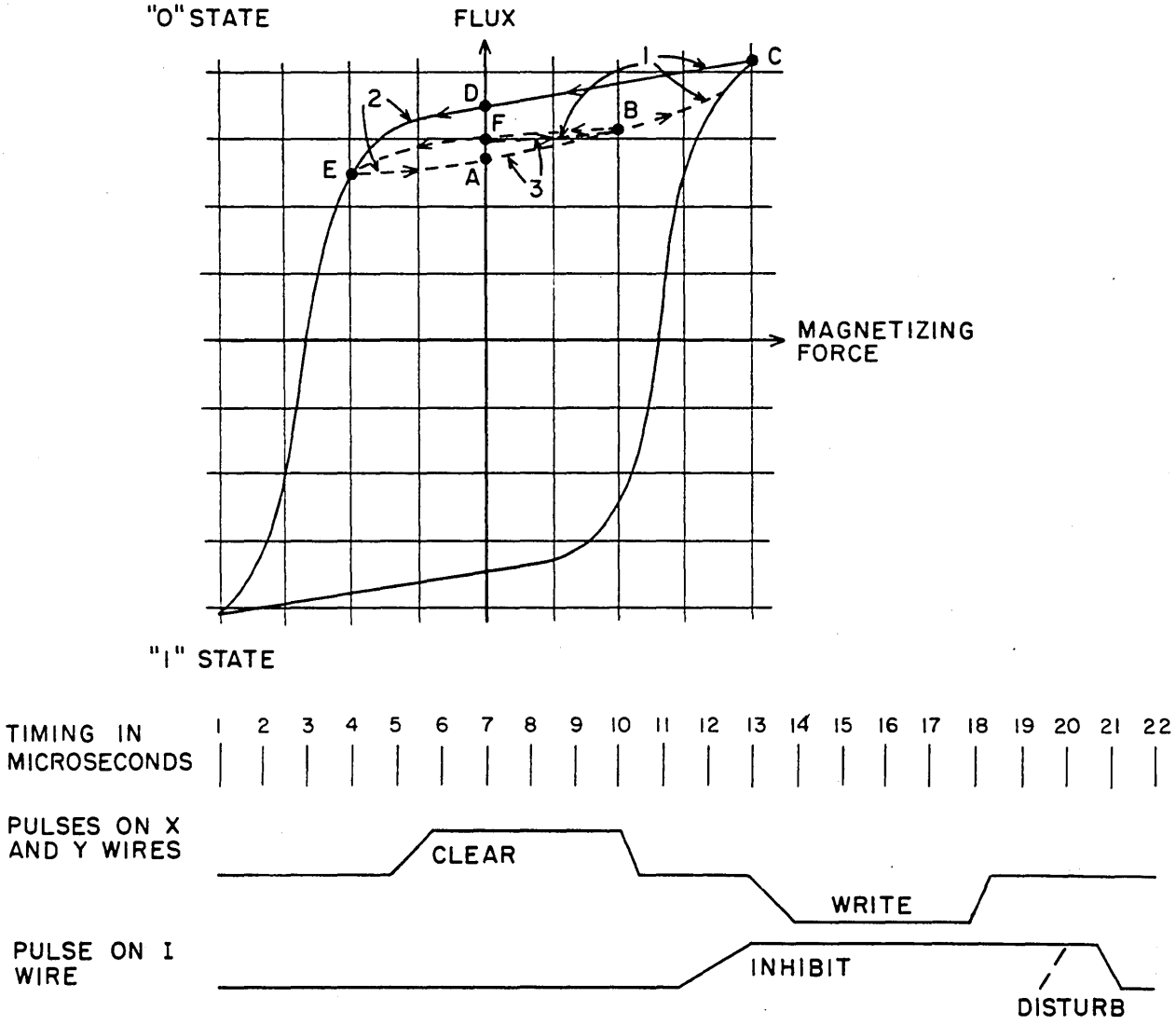
Figure 4-40. Typical Magnetic Core and Control Wires. (Arrows indicate direction of current flow during reading or writing.)



STEPS (See illustrations above)

Step 1 (CLEAR) - X and Y CLEAR pulses shift core state from F to C to D.

Step 2 (WRITE) - A half magnitude inhibit pulse on the I wire cancels the effect of either an X or Y half magnitude pulse so that the core state is shifted from D to E to A.

Step 3 (DISTURB) - Disturb pulse on I wire shifts core state from A to B to F along a minor hysteresis loop. (Additional half pulses run the core around the closed minor loop from F to E to A to B to F or from F to B to F.)

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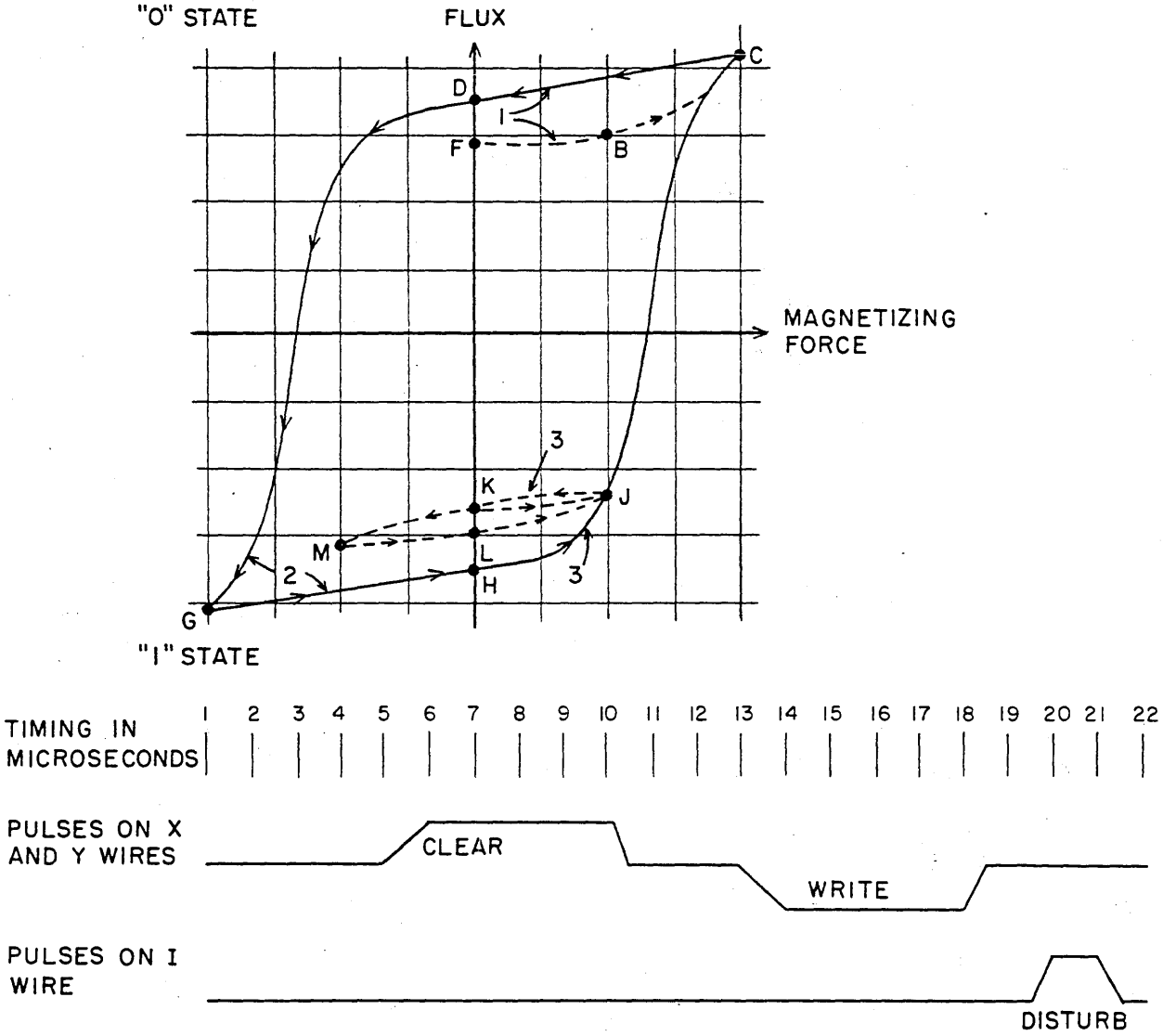
Figure 4-41. Writing a "0" When the Core was in the "0" State



STEPS (See illustrations above)

Step 1 (CLEAR) - X and Y CLEAR pulses shift core state from F to C to D.
Step 2 (WRITE) - X and Y WRITE pulses shift core state from D to G to H.
Step 3 (DISTURB) - DISTURB pulse on I wire shifts core state from H to J to K along a minor hysteresis loop. (Additional half pulses run the core around the closed minor loop from K to M to L to J to K or from K to J to K.)

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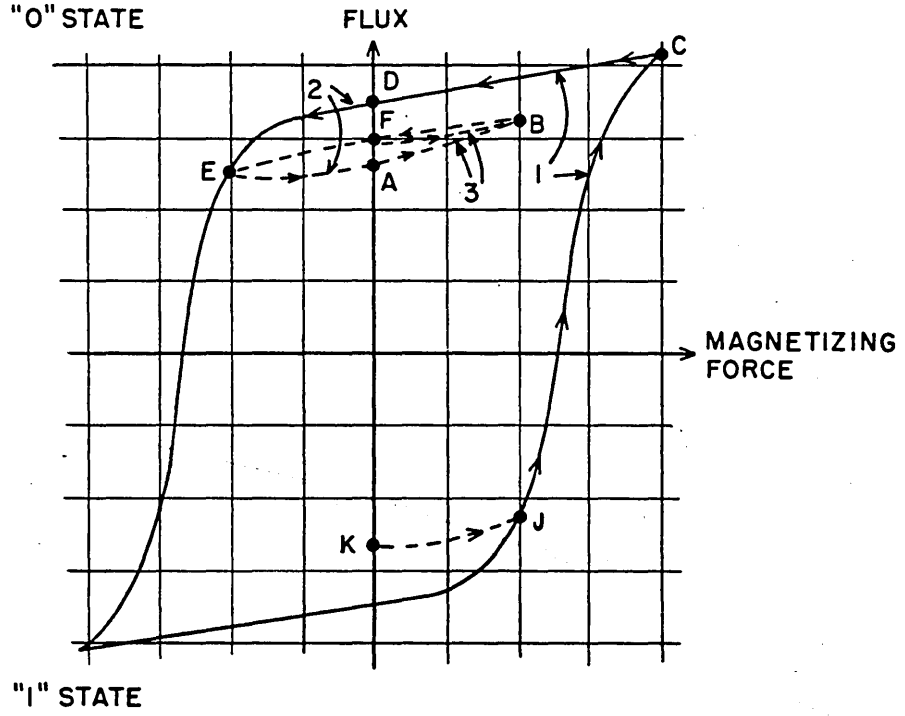
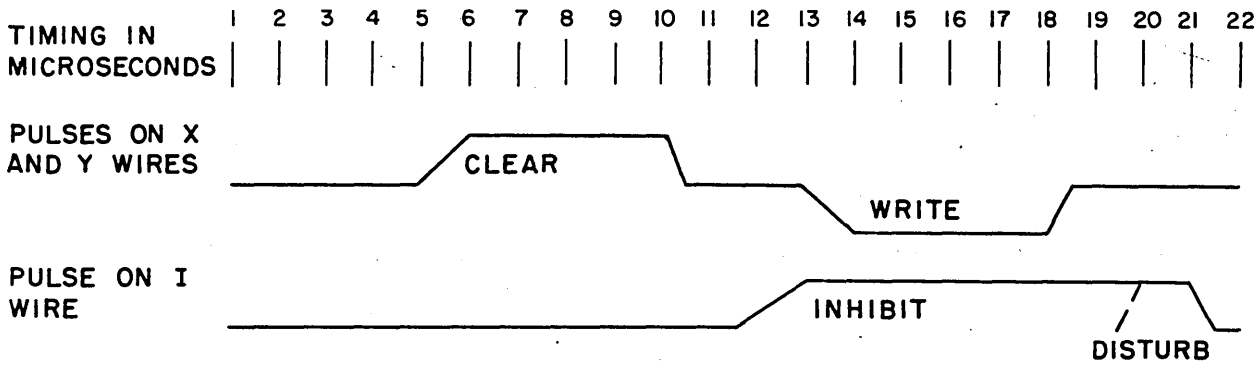
Figure 4-42. Writing a "1" When the Core Was in the "0" State





STEPS (See illustrations above)

Step 1 (CLEAR) - X and Y CLEAR pulses shift core state from K to C to D.

Step 2 (WRITE) - A half magnitude inhibit pulse on the I wire cancels the effect of either an X or Y half magnitude WRITE pulse so that the core is shifted from D to E to A along a minor loop.

Step 3 (DISTURB) -- DISTURB pulse on the I wire shifts core state from A to B to F. (Additional half pulses run the core around the closed minor loop from F to E to A to B to F or from F to B to E.)

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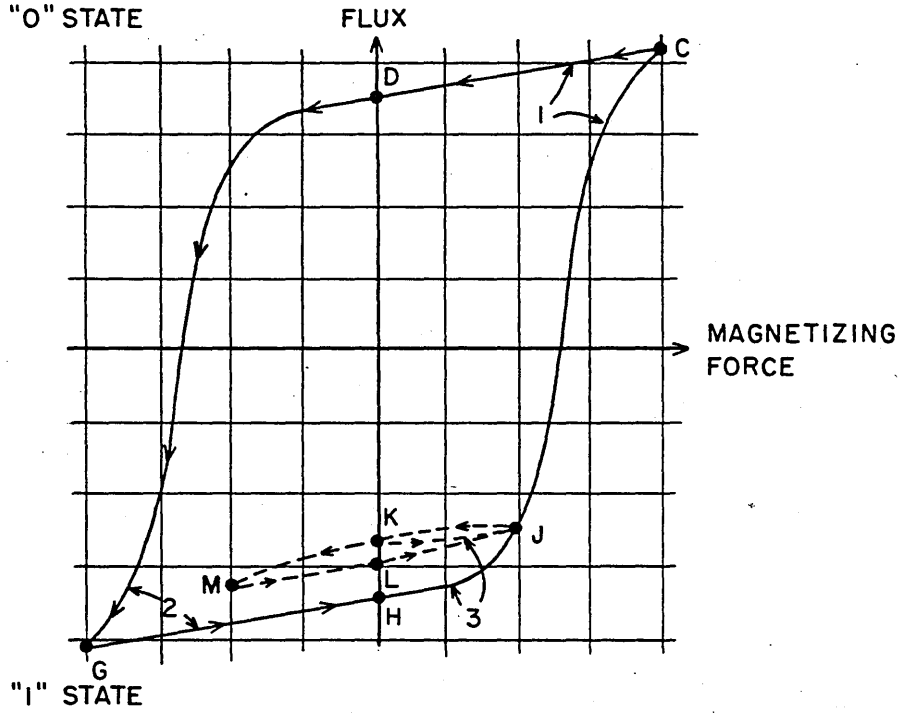
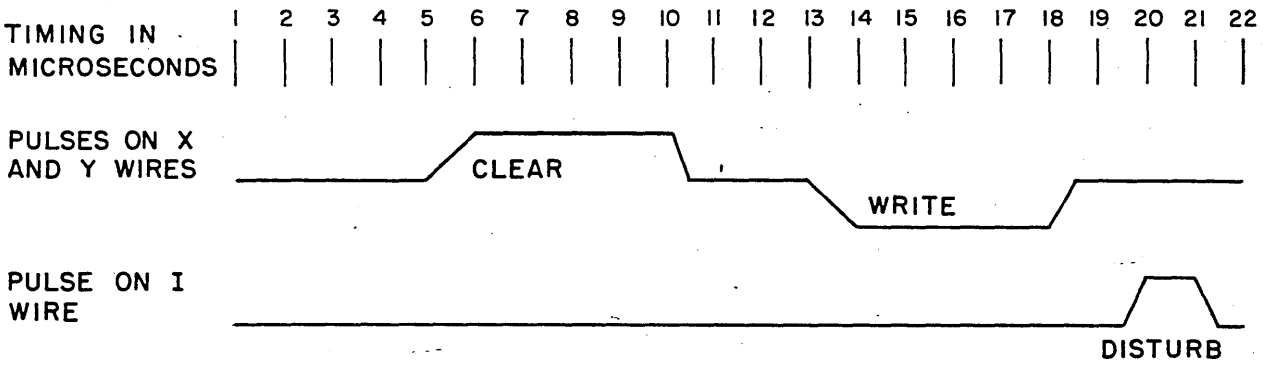
Figure 4-43. Writing a "0" When the Core Was in the "1" State





STEPS (See illustrations above)

Step 1 (CLEAR) - X and Y CLEAR pulses shift core state from K to C to D.

Step 2 (WRITE) - X and Y WRITE pulses shift core state from D to G to H.

Step 3 (DISTURB) - DISTURB pulse on I wire shifts core state from H to J to K along a minor hysteresis loop. (Additional half pulses run the core around the closed minor loop from K to M to L to J to K or from K to J to K.)

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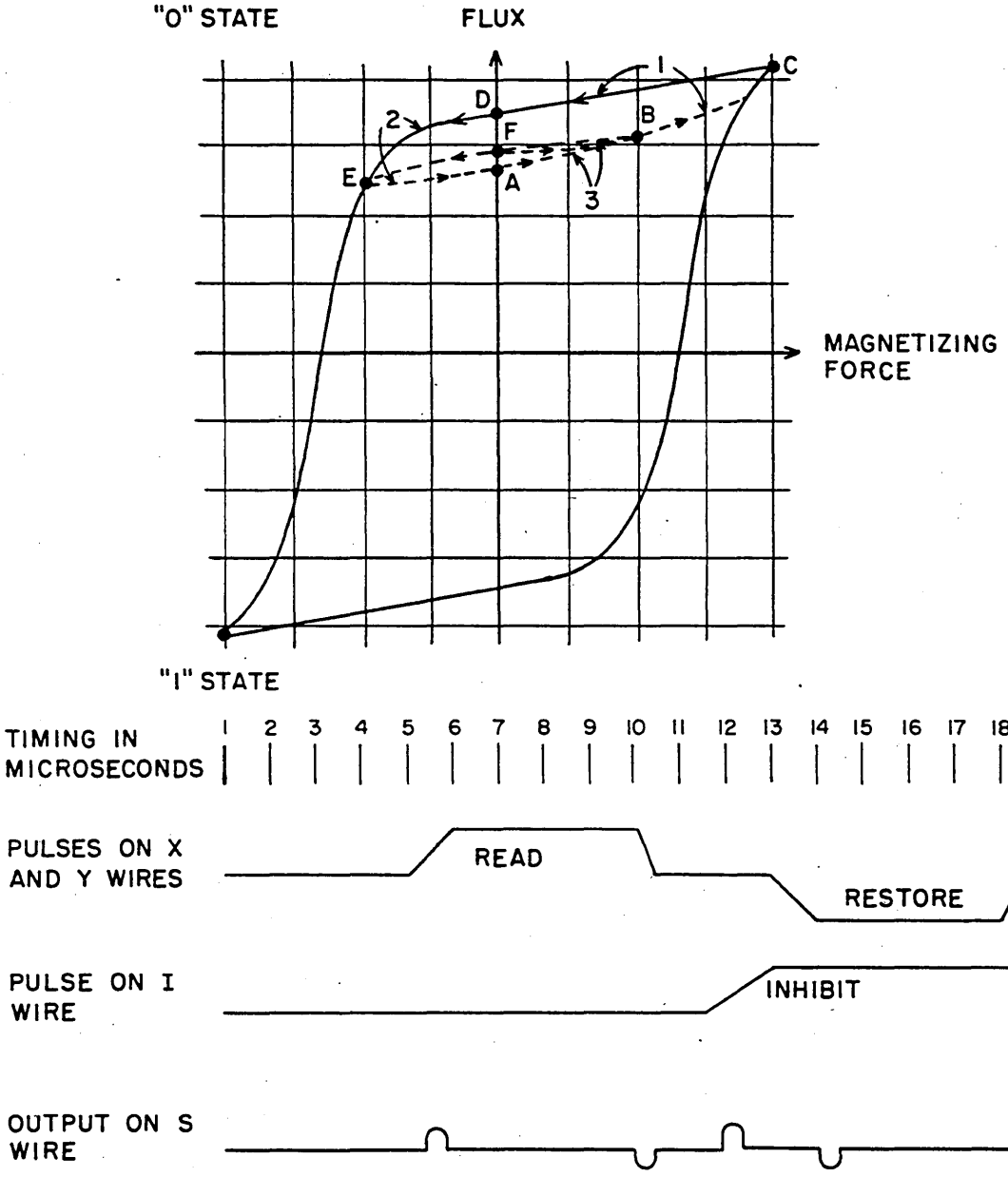
Figure 4-44. Writing a "1" When the Core Was in the "1" State



STEPS (See illustrations above)

Step 1 (READ). - X and Y READ pulses shift core state from F to C to D. (No appreciable output is produced on the S wire.)

Step 2 (INHIBIT). - A half magnitude INHIBIT pulse on the I wire cancels the effect of either an X or Y half magnitude RESTORE pulse so that core state is shifted from D to E to A.

Step 3 (DISTURB). - DISTURB pulse on I wire shifts core state from A to B to F along a minor hysteresis loop. (Additional half pulses run the core around the closed minor loop from F to E to A to B to F or from F to B to F.)

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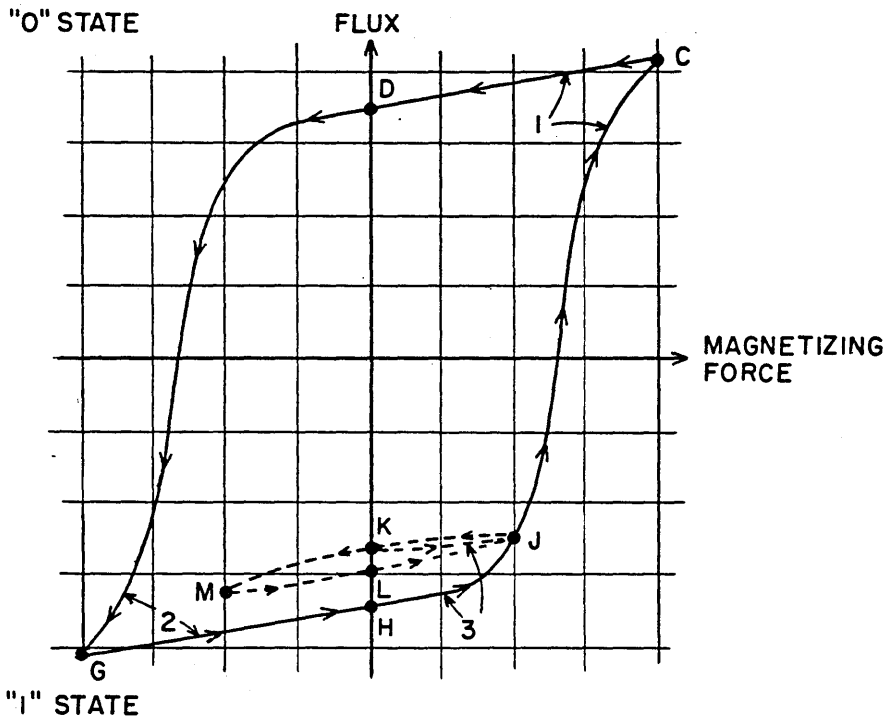
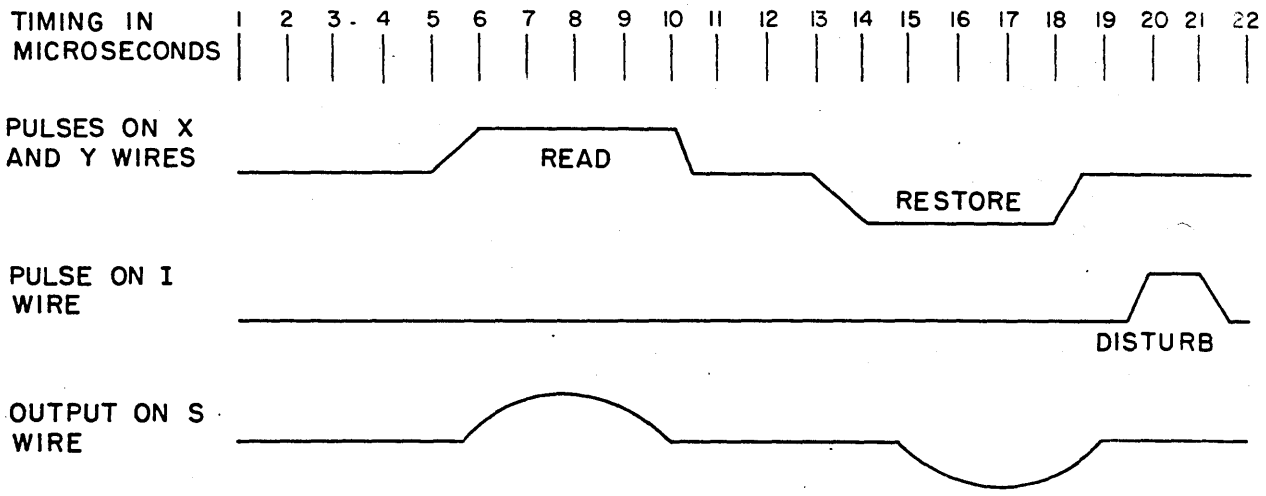
Figure 4-45. Reading a Core in the "0" State





STEPS (see illustrations above)

Step 1 (READ). - X and Y READ pulses shift core state from K to C to D, and a "1" output is produced on the S wire.

Step 2 (RESTORE).- X and Y RESTORE pulses shift core state from D to G to H.

Step 3 (DISTURB).- DISTURB pulse on I wire shifts core state from H to J to K along a minor hysteresis loop. (Additional half pulses run the core around the closed minor loop from K to M to L to J to K or from K to J to K.)

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Figure 4-46. Reading a Core in the "1" State

signal is generated, because the core is forced from the "1" to the "0" state. The sense amplifier is biased to amplify "1" signals and reject "0" signals. The sense "1" signal and the Read Probe pulse are combined in a logical AND circuit to produce an output which is used to set the associated Z-register core to "1".

In a Write sequence, the information previously in the core is read out (or cleared) and destroyed before the new information is written; hence the term "clear" is used for the first step of the Write sequence. The same pulses are used to read out the information in the core during the Read sequence. The pulses in the positive direction on the X and Y drive lines are, therefore, called the Clear/Read pulses. All of the cores in the chosen magnetic core memory address are forced initially to the "0" state in either a Read or a Write sequence.

In a Read sequence, the information in the core is read out of the core and retained in the Z-register. The next step after the read pulse during a Read sequence is the Write or Restore step. The information previously in the core, which was read out of the core, is written back into the core by the Restore pulse under the control of the Z-register. The same pulses are used either to write or restore information in the core. The pulses on the X and Y drive lines which are in the opposite direction (negative direction) to the Clear/Read pulses are therefore called the Write/Restore pulses.

The writing of information in a single core is accomplished in three steps, as shown in Figure 4-43 through 4-46. These may be designated as the CLEAR, the WRITE, and the DISTURB steps.

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STEP 1 (CLEAR). - The clear step is executed by the coincidence of the pulses on one X and Y wire. The amplitude of these pulses is such that the combined effect of both pulses

is sufficient to switch the core from the "1" to the "0" state if the core is initially in the "1" state. The occurrence of a pulse on only one of these wires does not change the state of the core. This choice of amplitude provides the AND logic function that is used to select one particular core during writing.

STEP 2 (WRITE). - After the clear step has switched the core to "0", the write step is executed. This either leaves the core in the "0" state or switches the core to the "1" state. If a "1" is to be written, two simultaneous pulses are applied to the selected X and Y wires to switch the core to the "1" state. These pulses are also of an amplitude which requires that both must be present simultaneously to change the state of the core. If a "0" is to be left in the core, the two coincident current pulses are applied to the X and Y wires, but their effect upon the core is opposed by the presence, on the I wire, of an Inhibit pulse of opposite polarity occurring simultaneously with the X and Y pulses. The amplitude of the conditionally present Inhibit pulse is approximately equal to half the sum of the amplitude of the pulses used on the X and Y wires. A pulse of this value reduces the effect of the X and Y magnetizing forces sufficiently to prevent the writing of a "1".

STEP 3 (DISTURB). - The third, or disturb, step is executed by a Disturb pulse applied to the I wire. If the core is in either the "0" or the "1" state, the Disturb pulse alters the

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state of the core along a minor hysteresis loop so that the flux state settles to a "0" or a "1" value which is stable in the presence of additional positive half pulses produced during references to other cores in the system.

The reading of information from a core is also accomplished in three steps, as shown in Figures 4-45 and 4-46. These may be designated as the READ, RESTORE, and DISTURB steps.

STEP 1 (READ). - The read step is similar to the first step of writing in that it is executed by the coincidence of two current pulses on the X and Y wires. If the core was initially in the "1" state, the resulting flux change occurring when the core is switched from "1" to "0" produces a Voltage pulse on the S wire. Therefore, during this step the reading of "1"is represented by the presence of a Voltage pulse, and the reading of a "0" is represented by the absence of a Voltage pulse on the S wire. When the first or read 2 step causes the core to switch from the "1" to the "0" state, the information stored is transferred to the Z-register. Thus, it is necessary to restore the core to the "1" state so that additional readouts may be made from the core. This is accomplished by the second or restore step.

During each MCS cycle the cummulative effect of the pulses on the selected X and Y drive lines is felt only by the addressed core in each plane. All other 126 cores along the selected lines in each plane will be affected by either the X or the Y pulse, but not both. These cores will not be switched, however, since the presence of both X and Y pulses is required to do so. The X or Y pulse, when occurring singly, is called a "half-pulse".

STEP 2 (RESTORE). - The restore step is similar to the second step of writing. If a "1" was read from the core, restoration is accomplished by two coincident current pulses on the X and Y wires. These pulses are of opposite polarity to the Read pulses and are also present on X and Y if a "0" was read. However, if a "0" was read, the effect of the Restore pulses upon the core is cancelled by the presence of an Inhibit pulse on the I wire, and the core is left in the "0" state.

STEP 3 (DISTURB). - The third, or disturb, step is identical to the third step of the writing sequence.

(2) MAGNETIC CORE MEMORY PLANES. - Each core memory plane consists of 4096 magnetic cores and their control wires, positioned in a square 64-by-64 array so that the wires all lie in the same plane. The cores are held in position by the wires, which are soldered to a square etched circuit frame. A typical magnetic core memory plane is shown in Figure 4-47.

In each of the core memory planes all 4096 cores transmit to, and receive information from, a single stage of the Z-register. This system arrangement is economical in that it permits the 4096 cores to share common S and I wires. Furthermore, the 64-by-64 arrangement requires only 64 X wires and 64 Y wires for 4096 cores. The diagonal S wire passes back and forth over each X and Y wire an even number of times so that transients produced in the sense winding by inductive coupling to the X and Y wires tend to cancel each other. The path of the sense wire is also arranged so that signals from unselected cores tend to cancel each other. The pulses induced on the sense wire may be of either polarity, depending upon the position of the selected core.

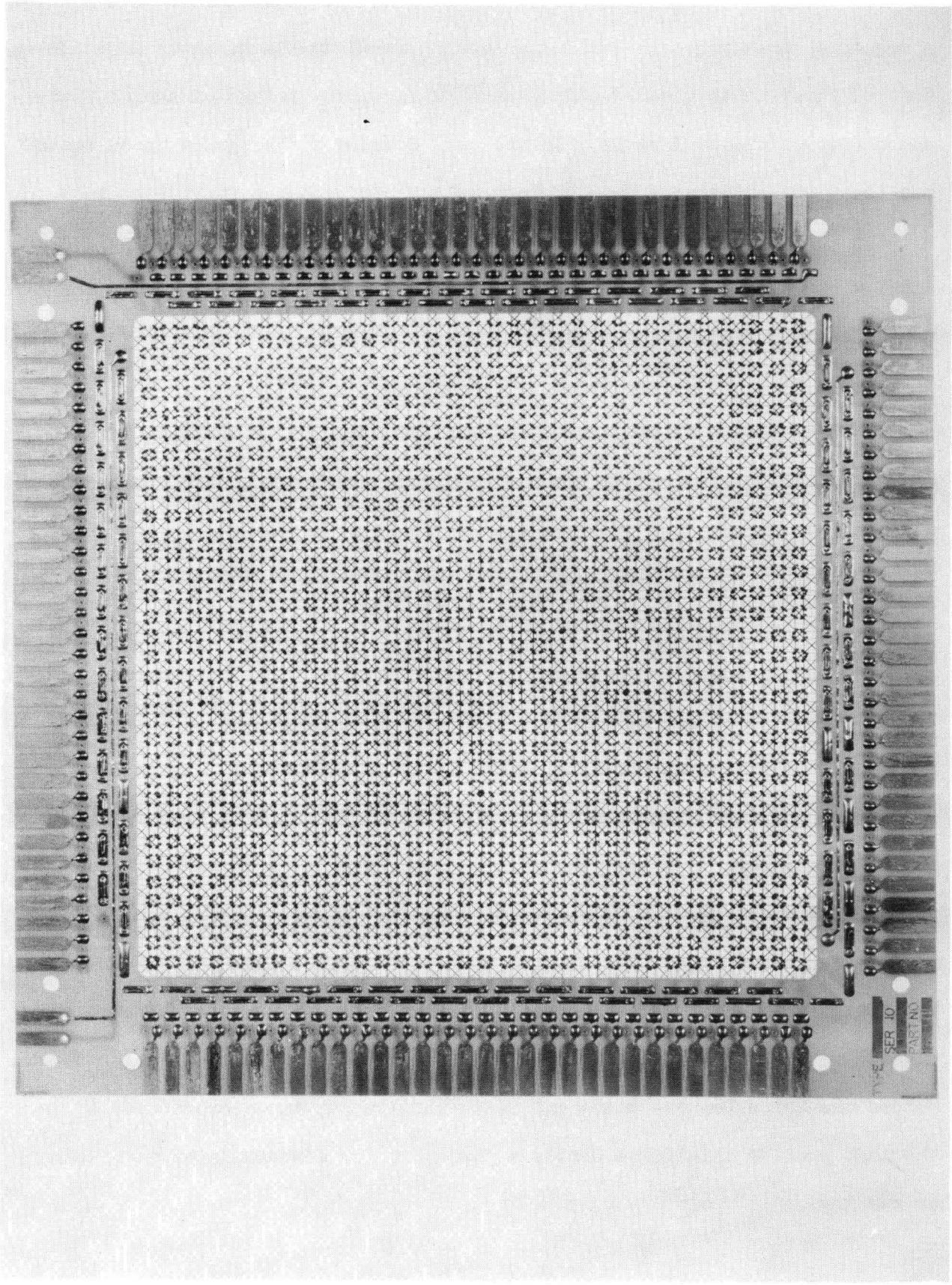

Figure 4-47. Typical 4096-Core Matrix Plane, Top View

When writing (or reading) is to be performed in a particular core address, a magnetic core Write (or Read) sequence produced by the Magnetic Core Access Control first sends Clear/Read pulses simultaneously to one of the 64 X wires and to one of the 64 Y wires. In the core located at the junction of these two lines the additive effect of both pulses performs the first step of writing (or reading) by forcing the core to the "0" state. On the pulsed X and Y wires, 126 other cores each receive only a half-pulse, and therefore are not affected.

When a core which contains a "1" is changed to a "0", the pulse induced on the diagonal S wire is recognized and amplified by the sense amplifier. (Although pulses are induced on the S wire during a Write sequence, these are not utilized by the system.) The sense pulse which is recognized by the sense amplifier is sent to the Z-register under the following conditions:

1) If the pulse is induced as a result of a Read operation, or
2) If the pulse is induced as a result of a partial Write operation and the pulse represents a bit which is to be retained in memory.

If the pulse represents a bit which is to be replaced by new information from the X-register, the Read Probe core (N_{75}) affecting that bit will not permit its passage to Z, and the bit will be lost.

Next, a Write/Restore pulse of the opposite polarity on the same X and Y wires attempts to force the selected core to the "1" state. If the core is to be left in the "0" state, and Inhibit/Disturb pulse is sent to the core memory plane I wire to inhibit the writing of "1". The Inhibit/Disturb pulse starts before the Write/Restore pulse and lasts until about two microseconds after it. The last part of this pulse performs the third (or disturb) step of writing or reading.

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If the core is to be set to "1", a short Disturb pulse is sent to the core memory plane I wire instead of an Inhibit/Disturb pulse. The core is set to "1" when the Disturb pulse is used instead of the Inhibit/Disturb pulse because it starts after the Write/Restore pulse ends. Step 3 of writing or reading is then performed by the Disturb pulse.

(3) MAGNETIC CORE MEMORY PLANE ASSEMBLY. - The Magnetic Core Memory Plane Assembly consists of a vertical stack of 28 core memory planes. Four memory planes are spares. This assembly is shown in Figure 4-48.

Four connectors between each of the 28 core memory planes provide 128 series paths through the X and Y wires for the X and Y current pulses. The X and Y drive lines are identified in octal notation on the terminal boards and in the unit signal diagrams, and are always referred to in this text in octal notation. The 128 wires for the X and Y drive lines are designated X_{00} through X_{77} and Y_{00} through Y_{77}. All X and Y drive lines are connected to ground after they pass through the memory planes. At the opposite end of the Core Memory Plane Assembly, each X and Y drive line is brought out to a separate terminal, and the current diverter circuits in the translator system are connected to these terminals through a drive line transformer. On the edge of each core memory plane, two tabs provide connections for the I wire, and two tabs provide connection for the S wire.

(4) MEMORY TIMING CHAIN. - The Memory Timing Chain is a series of 12 basic magnetic switch transfer circuits which produce a series of time pulses spaced one or two microseconds apart each time core R^{05}_{01} is set by an Initiate to Memory pulse from the computer. The timing sequence of the Memory Timing Chain pulses is shown in Figures 4-49 and 4-50. The Memory Timing Chain is shown in Logical Diagram 87000, Volume 8, page 35, and Timing Sequence Diagram 87734, Volume 9, page 113. The theory of operation of the basic transfer

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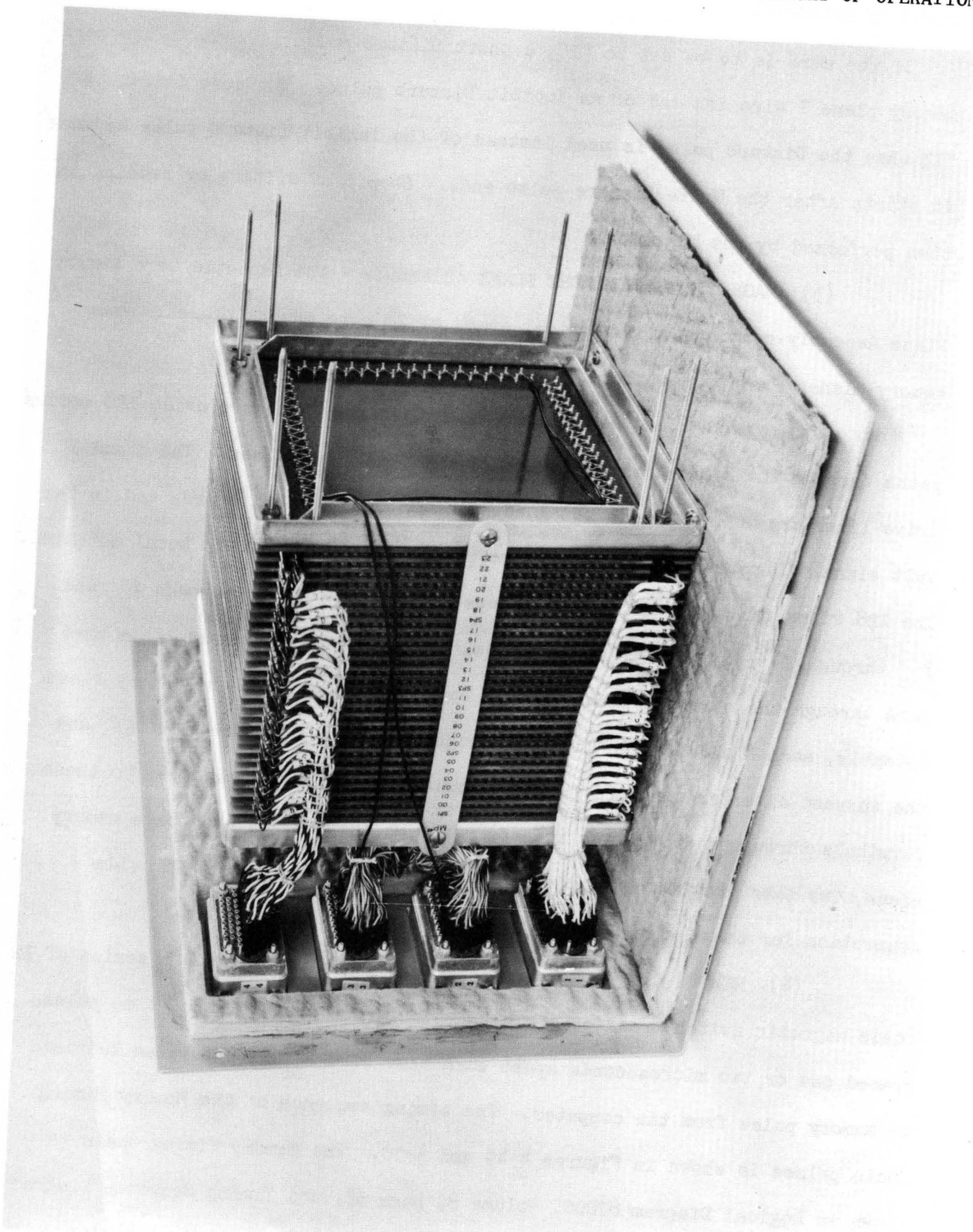

Figure 4-48. Magnetic Core Memory Plane Assembly

Figure 4-49

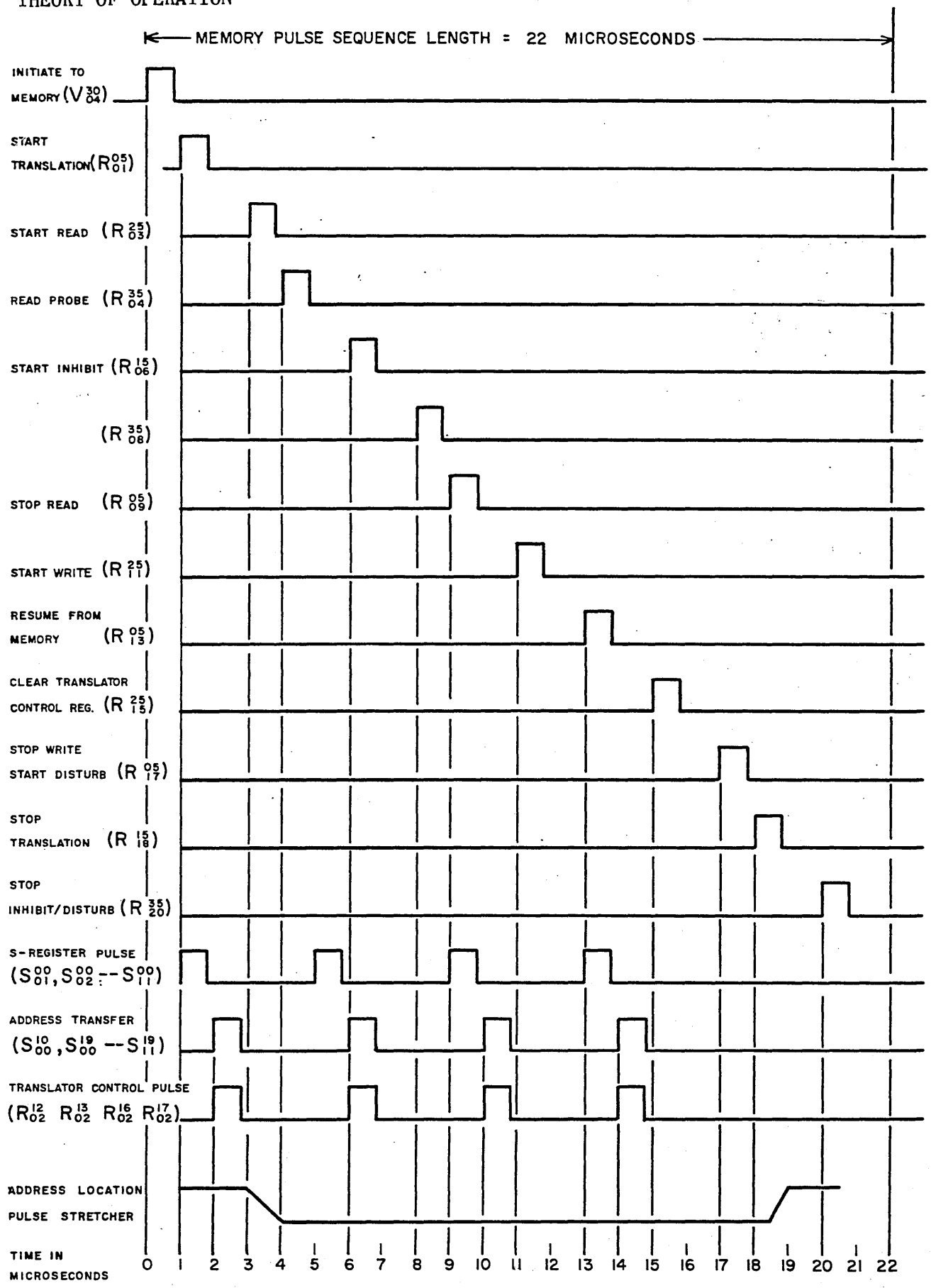

Figure 4-49. Magnetic Core Storage System Control Pulses

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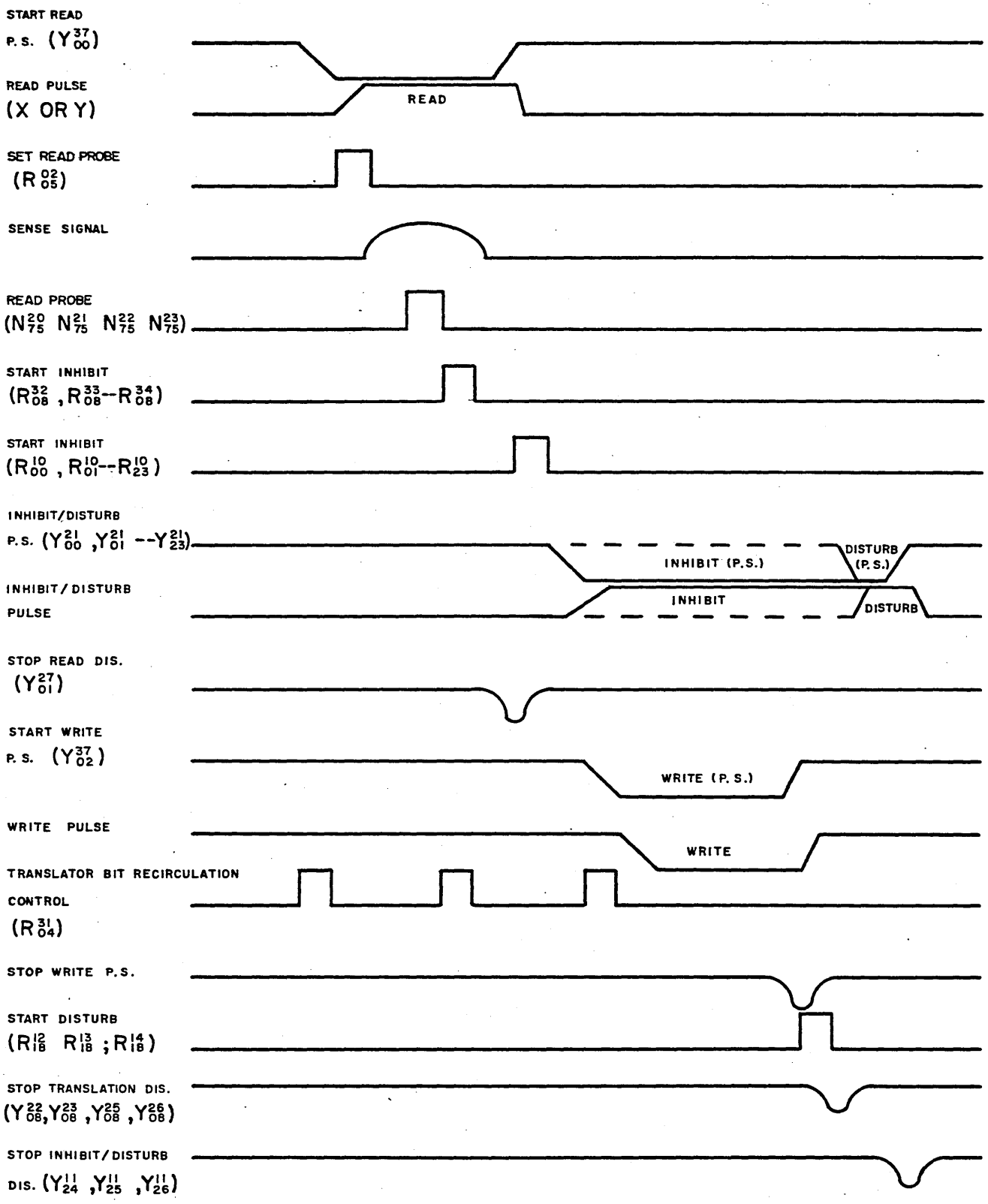

Figure 4-50. Magnetic Core Storage System Control Pulses (Cont.)

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circuit is explained in Volume 2, section 4, Theory of Operation.

The stage number portion of each magnetic switch core symbol in the Memory Timing Chain indicates the time in microseconds that an Output pulse begins in that stage relative to the zero time reference. (The zero time reference of each Memory Timing Chain magnetic switch core stage number is the beginning of the readout time of the Initiate to Memory core V^{30}_{04}.) The timing sequence scale in microseconds for each Memory Timing Chain stage is indicated in Timing Sequence Diagram 87734. The times indicated on this scale are referred to in this section to explain the operation of the Memory Timing Chain and the Memory Access Control Section.

Each magnetic switch core shown in the Magnetic Core Storage System Timing Sequence Diagram 87734 produces an output pulse at the time indicated by the timing scale. The magnetic switch cores, R^{11}_{02} and R^{31}_{04}, of the Translator Bit Recirculation Control section produces a series of four outputs and are therefore shown four times on the timing sequence diagram. The translator bit recirculation control core R^{31}_{04} is connected to produce a series of three control pulses spaced four microseconds apart during each MCS reference. The negation lead of this core receives a pulse which stops the Translation Bit Recirculation Control sequence on the fifteenth microsecond (time 15) of the current memory sequence. Therefore, when the translator bit recirculation control core R^{31}_{04} is read out on the sixteenth microsecond (time 16) of the current memory sequence, no signal is produced to reset the translation pulse stretcher stages and the Translator Bit Recirculation Control sequence ends.

The function of the Memory Timing Chain is to produce a series of timed pulses which are used to control the Read and Write operations performed in the memory. An Initiate To Memory Signal, occurring during each Read or Write sequence, transfers a "1" to Memory Timing Chain core R^{05}_{01} and initiates the

Memory Timing Chain sequence. The "1" which was stored in R^{05}_{01} by the Initiate to Memory signal is transferred to each core in the Memory Timing Chain in sequence to produce the required Memory Timing Chain signals. When the "1" is transferred from R^{05}_{01} to R^{25}_{03} (at time 1) a "1" also is transferred to cores R^{17}_{02}, R^{16}_{02}, R^{13}_{02}, R^{12}_{02}, and R^{11}_{02}. The next transfer pulse, TP1, reads out the "1" in these cores at time 2. Output signals are therefore produced in these cores which are combined in the logical AND circuits of the translator with the output signals of the translator cores S^{19}_{00}, S^{10}_{00} ... S^{19}_{11}, S^{10}_{11}. The outputs of the selected logical AND circuits energize the desired pulse stretcher circuits. However, these pulse stretcher circuits cannot maintain the required output signal voltage for the duration of a Memory Reference sequence. Therefore, the translator bit recirculation control core R^{31}_{04} produces an output signal every four microseconds (at times 04, 08, and 12) which is used to reset cores R^{17}_{02}, R^{16}_{02}, R^{13}_{02}, and R^{12}_{02}. At times 2, 6, 10, and 14 the "1's" in these cores are read out and produce simultaneous output signals with the signals of the Address Transfer Channel cores S^{19}_{00}, S^{10}_{00}, ... S^{19}_{11}, S^{10}_{11}. The pulse stretcher circuits on the outputs of the energized logical AND circuits are therefore energized every four microseconds (at times 2, 6, 10, and 14) to maintain the required translator output voltage. Core R^{31}_{04} is cleared at time 15 by Memory Timing Chain core R^{25}_{15} which reads out the "1" that was stored in this core at time 14. Therefore, when R^{31}_{04} is read out at time 16, no output signal is produced and the Translator Bit Recirculation Control sequence is terminated until the next memory reference is initiated.

The translation of the MCS address is not actually complete until time 3, when the signal from Memory Timing Chain core R^{25}_{03} energizes the Start Read pulse stretcher Y^{37}_{00}. The energization of this pulse stretcher completes the selection of the read current generators RGX1, RGX2, RGY1, or RGY2 by energiz-

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ing two of the logical AND circuits which are connected to them. Selection of the proper X and Y read current generators is determined by the contents of the highest-order bits in the X and Y portions of the MCS address. If a "1" is contained in bit S^{00}_{05} of the X drive line portion of the MCS address, read current generator RGX2 is turned on; if a "0" is contained in bit S^{00}_{05}, read current generator RGX1 is turned on. The Y drive line read current generator is selected in a similar manner.

The bits of the memory word which are transferred to the Z-register during an MCS Read reference are controlled by the Read Probe cres N^{20}_{75}, N^{21}_{75}, N^{22}_{75}, and N^{23}_{75}. These cores produce Read Probe signals when the signals Initiate Read MCS (0-7), Initiate Read MCS (8-14), Initiate Read MCS (15), and Initiate Read MCS (16-23) are combined in the logical AND circuits with the Start Read Probe signal from core R^{02}_{05}. The bits of the memory word containing "1's" are transferred to the Z-register at time 7 if a Read Probe signal is present at the logical AND circuit connected to the output of the sense amplifier stage.

The "1's" which were transferred to Z during an MCS Read reference at time 7 are read out of the Z^{30} cores at time 8 and transferred to the Z^{00} cores. At time 9 the "1" signals from the Z^{00} cores are used to clear the corresponding Start Inhibit cores R^{10}_{00}, R^{10}_{01}, ... R^{10}_{22}, R^{10}_{23}. These start inhibit cores are set at time 8 by the outputs from the start inhibit control cores (R^{32}_{08}, R^{33}_{08}, and R^{34}_{08}). These start inhibit control cores are set at time 6 by the start inhibit control pulse which is produced by Memory Timing Chain core R^{15}_{06}.

The inhibit current is turned on automatically for each memory plane unless there is a "1" to be written in that plane. If a "1" is to be written in a plane, the negation input of the start inhibit core controlling that plane will receive a "1 "signal from the associated Z^{00} core. When the start inhibit

cores are read out at time 10, the cores which were negated do not produce output signals and the start inhibit pulse stretchers connected to these outputs are not turned on. The inhibit current, therefore, is not turned on in those planes, and "1's" are written.

The Write/Restore current pulse sequence is initiated at time 11 by a pulse from the Memory Timing Chain core R^{25}_{11}. The Start Write pulse from this core turns on the Start Write pulse stretcher Y^{37}_{02}. The energization of this pulse stretcher completes the selection of the Write Current Generators WGX1, WGX2, WGY1, or WGY2 by energizing two of the logical AND circuits which are connected to them. The X and Y write current generators which are turned on are determined by the contents of the highest-order bits of the X and Y portions of the MCS address. If a "1" is contained in bit S^{00}_{05} of the X drive line portion of the MCS address, write current generator WGX2 is turned on; and if a "0" is contained in bit S^{00}_{05}, write current generator WGX1 is turned on. The Y drive line write current generator is turned on in a similar manner.

The Resume from Memory pulse is produced by Memory Timing Chain core R^{05}_{13} at time 13.

The Translator Bit Recirculation Control sequence is terminated at time 15 by a pulse from Memory Timing Chain core R^{25}_{15}, which is connected to the negation terminal of core R^{31}_{04}.

The Stop Write pulse is produced by the Memory Timing Chain core R^{05}_{17} at time 17. Because of the delay which exists in developing the pulse discharger action, this pulse is required one microsecond in advance of the time that the Write current pulse begins to decrease.

The Start Disturb pulse is also generated at time 17 by R^{05}_{17}, and sets cores R^{12}_{18}, R^{13}_{18}, and R^{14}_{18} at time 17. These cores are read out at time 18 to produce 24 separate Start Disturb pulses: core R^{12}_{18} produces start disturb pulses for

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memory planes 0-7; core R^{13}_{18} produces start disturb pulses for memory planes 08-15; and core R^{14}_{18} produces start disturb pulses for memory planes 16-23. It is necessary to initiate the start disturb pulse at time 17 because 24 separate outputs are required to control the Disturb pulse in each of the 24 core memory planes. Each magnetic switch core can produce a maximum of eight output pulses. Therefore, it is necessary to set the three start disturb control cores R^{12}_{18}, R^{13}_{18}, and R^{14}_{18} at time 17 to produce the 24 separate start disturb pulses when these cores are read out at time 18.

The Stop Translation pulse is produced by the Memory Timing Chain core R^{15}_{18} at time 18. The stop translation pulse energizes the stop translation pulse dischargers Y^{26}_{08}, Y^{25}_{08}, Y^{23}_{08}, and Y^{22}_{08}. The inherent time delays in the stop translation pulse discharger circuits, Translator pulse stretcher circuits and the Current Diverter circuits are such that the current diverters are not turned off until about time 19.

The Stop Inhibit/Disturb pulse is produced by the Memory Timing Chain core R^{35}_{20} at time 20. It energizes the stop inhibit/distrub pulse discharger circuits Y^{11}_{24}, Y^{11}_{25}, and Y^{11}_{26}. The stop inhibit/disturb pulse discharger circuits discharge the Inhibit/Disturb pulse stretcher circuits Y^{21}_{00}, Y^{21}_{01}, ... Y^{21}_{22}, Y^{21}_{23}, which turn off the inhibit/disturb current generator circuits, thereby terminating the current MCS reference.

(5) MC ADDRESS SELECTION SYSTEM. - The circuits used in address selection are represented by shorthand block-type symbols in Logical Diagram 87001, Volume 8, pages 36 and 37. The address selection system for the X drive lines is identical to that used for the Y drive lines. The X and Y drive line address selection systems therefore perform a 2^6 translation of the 12-bit MCS address ($2^6 \times 2^6 = 2^{12} = 4096$) to select one X and one Y drive line. The address of the selected core in each core memory plane is located at the inter-

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section of the selected X and Y drive lines. Since the X drive line address selection system is identical to that for the Y drive line address selection system, only the X drive line system is explained in this text.

Each X drive line is connected to the secondary winding of a separate drive line transformer. The primary winding of each X drive line transformer has two sections, one for the Read current pulse and one for the Write current pulse. Each section of the primary winding is connected to a common point which is then connected to a current diverter. There are 32 current diverter circuits; therefore, each current diverter circuit serves two drive lines as shown in Drawing 87001, Volume 8, page 36.

The X drive line address selection system is divided into three distinct translators, 2^3, 2^2, and 2^1. The 2^3 translator is controlled by the three lower-order bits of the S-register, S^{00}_{00}, S^{00}_{01}, and S^{00}_{02}; the 2^2 translator is controlled by the next two higher-order bits, S^{00}_{03} and S^{00}_{04}; and the 2^1 translator is controlled by the highest-order bit, S^{00}_{05}.

Each current diverter is turned on by the decoded results of the 2^3 translator and the 2^2 translator ($2^3 \times 2^2 = 2^5$). The final selection of the X drive line is determined by the highest-order bit, S^{00}_{05} ($2^3 \times 2^2 \times 2^1 = 2^6$).

The contents of S^{00}_{05} determines which read and write current generators are turned on. If S^{00}_{05} contains a "0", the read current generator RGX1 and the write current generator WGX1 are turned on. If S^{00}_{05} contains a "1", the read current generator RGX2 and the write current generator WGX2 are turned on. Both read current generators, RGX1 and RGX2, and both write current generators, WGX1 and WGX2, are connected through the primary windings of the drive line current transformers to the current diverter circuits.

The circuits used to produce the Clear/Read and Write/Restore pulses for each X and Y drive line consist of a read current generator and a write current

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generator, each connected to the primary winding of the drive line transformer. One of the transformer primary windings is used to produce the Clear/Read pulse, and the other is used to produce the Write/Restore pulse. Because of the manner in which the transformers are connected, the signal on the output line of the transformer is either a clear/read pulse (during the first step in a memory cycle) or a write/restore pulse of the opposite polarity (during the second step of a cycle).

During an MCS reference each Storage Address Register stage produces specific signals which begin at the same time as the Start Translation signal from the Memory Timing Chain core R^{05}_{01}, and are repeated four times at four-microsecond intervals. Therefore, the clear/read and write/restore operations are performed in only one MC address during each storage reference.

The lower-order six bits of the MCS address controlled by cores S^{00}_{00}, S^{00}_{01}, S^{00}_{02}, S^{00}_{03}, S^{00}_{04}, and S^{00}_{05} are decoded to select and turn on the desired X drive line current. The higher-order six bits of the MC address controlled by cores S^{00}_{06}, S^{00}_{07}, S^{00}_{08}, S^{00}_{09}, S^{00}_{10}, and S^{00}_{11} are decoded to select and turn on the desired Y drive line current.

The three lower-order bits of the MCS address represented by the signals designated XXXXX0, XXXXX1, XXXXX0X, XXXX1X, XXX0XX, and XXX1XX on the Address Selection Diagram 87001, Volume 8, page 36, are combined in an octal (2^3) translator to produce the translated signals designated XXX000, XXX001, XXX010, XXX011, XXX100, XXX101, XXX110 and XXX111.

The next two higher-order bits of the MCS address are controlled by cores S^{00}_{03} and S^{00}_{04}, and they are represented by the signals designated XX0XXX, XX1XXX, X0XXXX, and X1XXXX. These signals are combined in the four three-input logical AND circuits (binary to quaternary translator) to produce the partial translation signals designated X00XXX, X01XXX, X10XXX, and X11XXX.

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The translated signals of the above described translators (2^2 and 2^3) are combined in a decoder (system of two-input logical AND circuits) to produce 32 separate decoded signals designated X00000, X00001, X00010, ... X11101, X11110, X11111 ($2^2 \times 2^3 = 2^5 = 32$). These 32 decoded signals are used to turn on the 32 current diverters in the X drive line address selection system.

The highest-order bit, controlled by S^{00}_{05}, is used to turn on one of the current generators RGX1, RGX2, WGX1, or WGX2, as previously explained. Since each current diverter is connected to both read current generators (RGX1 and RGX2) and both write current generators (WGX1 and WGX2), the final selection of the X portion of the MCS address is made by turning on one of these current generators ($2^2 \times 2^3 \times 2^1 = 2^6 = 64$). The Y drive line selection is produced in a similar manner. Ths, a specific setting of the S-register selects but one of the 4096 unique addresses available ($2^1 \cdot 2^2 \cdot 2^3 \times 2^1 \cdot 2^2 \cdot 2^3 = 2^{12} = 4096$).

The operation of the address selection system when selecting the octal address 1111 is described in the following example. The S-register signals designated XXXXX1, XXXX0X, and XXX0XX, together with the Translation Bit Recirculation Control signal, are combined in the 2^3 translator to produce the translated signal, XXX001. The S-register signals XX1XXX, X0XXXX, and the Translation Bit Recirculation Control signal are combined in the 2^2 translator to produce the translated signal, X01XXX. These translated signals are combined in the logical AND circuits in the 2^5 decoder to produce the decoded signal, X01001. This decoded signal turns on the current diverter stage designated DX^{11}_{51}. The S-register signal, 0XXXXX, is combined in a logical AND circuit with the Translator Bit Recirculation Control signal to produce a signal which energizes the pulse stretcher circuit Y^{36}_{00}, and turns on the read current generator RGX1 and the write current generator, WGX1. These generators each

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produce a current pulse in the primary of the current transformer TX_{11} through the current diverter circuit DX^{11}_{51}. The pulses induce a current pulse in the secondary winding of transformer TX_{11}, which is connected to the X_{11} drive line. The selection of Y_{11} drive line is produced in a similar manner. It should be noted that the only way the selection of the X_{11} drive line differs from the selection of the X_{51} drive line is in the signal from S^{00}_{05}. If S^{00}_{05} contains a "1" the read current generator RGX2, and the write current generator WGX2 are turned on. This pair of generators produces current pulses in transformer TX_{51} instead of transformer TX_{11}. Therefore, a current pulse is induced in the X_{51} drive line instead of the X_{11} drive line when S^{00}_{05} contains a "1" instead of a "0".

(6) MEMORY ACCESS CONTROL

(a) GENERAL. - During each storage reference the Memory Access Control circuits produce signals for operating the Digit Plane Control circuits and for turning on the Read, Write, Inhibit and Inhibit/Disturb current pulses. Identical Memory Timing Chain pulses are produced during each MCS reference; however, the Read and Write operations which occur in the memory are controlled by the signals: Initiate MCS read probe (0-7); Initiate MCS read probe (8-14); Initiate MCS read probe (15); Initiate MCS read probe (16-23) and certain command signals from the computer.

(b) OPERATION FOR WRITE SEQUENCE. - A write sequence will initiate MCS Clear and MCS Write steps in memory. Memory Timing Chain core R^{35}_{04} sets R^{02}_{05} at time 4. Simultaneously, translations from the m (field modifier) portion of the U-register set the appropriate Initiate Read Probe cores T^{00}_{20}, T^{00}_{21}, T^{00}_{22}, T^{00}_{23}, depending upon the bits of memory word in which it is desired to write. At time 5 the Initiate MCS Read Probe signals which are present are combined in the logical AND circuits with outputs from R^{02}_{05} to set the

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corresponding Read Probe cores (N_{75}). Signals from the energized read probe cores are combined in logical AND circuits with the signals from bits of the referenced memory word containing "1's" which set the corresponding stages of the Z-register. Therefore, only those bits of the selected address which are not to be replaced with new information are transferred to the Z-register during the Clear step. New information may be written in any one of the five combinations of bits shown on the following table.

MCS WRITE SEQUENCES

SEQUENCE	INITIATE SIGNALS
MCS Write (0-7) (m = 1 or 5)	Initiate to Memory; Initiate MCS Read Probe (8-14); Initiate MCS Read Probe (15); Initiate MCS Read Probe (16-23)
MCS Write (8-15) (m = 2 or 6)	Initiate to Memory; Initiate MCS Read Probe (0-7); Initiate MCS Read Probe (16-23)
MCS Write (16-23) (m = 3 or 7)	Initiate to Memory; Initiate MCS Read Probe (0-7; Initiate MCS Read Probe (8-14); Initiate MCS Read Probe (15)
MCS Write (0-14) (m = 4)	Initiate to Memory; Initiate MCS Read Probe (15); Initiate MCS Read Probe (16-23)
MCS Write (0-23) (m = 0)	Initiate to Memory

During the MCS Write step all bits of Z, including the bits of the memory word which are not being replaced and the new bits of the memory word from X, are transferred to the memory cores.

(c) OPERATION FOR READ SEQUENCE. - A Read sequence will initiate MCS Read and MCS Restore steps in memory. The steps function as described in (b) above, with this exception:

Since the MCS Read step can only transmit an entire 24-bit word from memory to Z, all the Initiate Read Probe signals, 0-7, 8-14, 15, 16-23 must be present.

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The U-register stages holding the m designator are by-passed for this case, and the above-mentioned T^{00} cores are set through a pulse from the Read Operand command sequence (V^{20}_{06}). This is shown on Command Logic Diagram 87209, Volume 8, page 8. The control of the portion of the word which is used by the computer during a MCS Read reference is performed in the N control cores in the Z-register buffer.

(d) MEMORY ACCESS CONTROL SUB-SECTIONS. - The Memory Access Control Section is divided into the following sub-sections on a functional basis:

1) Translator Bit Recirculation Control
2) Read Probe Control
3) Start Inhibit Pulse Control
4) Start Disturb Pulse Control
5) Stop Translation Pulse Discharger Control
6) Stop Inhibit/Disturb Pulse Discharger Control

The other circuits which are in the Memory Access Control Section are Start Read Pulse Stretcher, Stop Read Pulse Discharger, Start Write Pulse Stretcher, and Stop Write Pulse Discharger. The timing sequence of these control circuits has been described previously in paragraph 4 of this section, Memory Timing Chain.

1. TRANSLATION BIT RECIRCULATION CONTROL. - The function of this section was described under paragraph 4, Memory Timing Chain, above.

2. READ PROBE CONTROL. - The function of this section was described under (b), Operation for Write Sequence, above.

3. START INHIBIT PULSE CONTROL. - The function of the Start Inhibit Pulse control section, consisting of cores R^{32}, R^{33}, and R^{34}, is to expand the Start Inhibit signal from the Memory Timing Chain, R^{15}, into 24

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separate signals for the digit plane controls: Start Inhibit DPC-0 through DPC-23. Since the basic magnetic core switch transfer circuit can produce a maximum of eight outputs it is necessary to use the three transfer circuits R^{32}_{08}, R^{33}_{08}, and R^{34}_{08} to produce the required 24 Start Inhibit Control signals.

4. START DISTURB PULSE CONTROL. - The function of the Start Disturb Pulse control section, consisting of R^{12}_{18}, R^{13}_{18}, and R^{14}_{18}, is to expand the Start Disturb signal from Memory Timing Chain core R^{05}_{17} into 24 separate signals for the digit plane controls: Start Disturb DPC-0 through DPC-23. Because of the above-mentioned switch core limitations it is necessary to use the three transfer circuits R^{12}_{18}, R^{13}_{18}, and R^{14}_{18} to produce the required number of signals.

5. STOP TRANSLATION PULSE DISCHARGER CONTROL. - The function of the Stop Translation pulse discharger control section is to terminate the translation of the current MCS address so that a new storage reference can be initiated as soon as possible. Therefore, the Stop Translation signal from Memory Timing Chain core R^{15}_{18} is produced at time 18 so that the current MCS address is terminated at time 19. The current MCS address translation is thus terminated almost immediately after the termination of the Write/Restore current pulse and prior to the beginning of the Disturb Current pulse.

6. STOP DISTURB PULSE CONTROL. - The function of the Stop Disturb Pulse control section, consisting of the pulse discharger circuits designated Y^{11}, Y^{11}, and Y^{11}, is to turn off the Inhibit/Disturb current generator circuits in the Digit Plane Control section at the end of each MCS reference. The Inhibit/Disturb current generator circuits are held in the ON condition by the Inhibit/Disturb pulse stretcher circuits in the Digit Plane Control section. The Stop Disturb Pulse control section produces the signals Stop Inhibit/Disturb DPC-0 through DPC-23, which turn off the Start

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Inhibit/Disturb Current pulse stretchers.

7. START READ PULSE STRETCHER. - The function of the Start Read pulse stretcher circuit, Y^{37}_{00}, is to produce a signal which controls the length of the Read Current pulse during each MCS reference. This pulse stretcher is energized by the Start Read signal from Memory Timing Chain core R^{25}_{03} at time 3.

8. STOP READ PULSE DISCHARGER. - The function of the Stop Read pulse discharger circuit, Y^{27}_{01}, is to terminate the Read Current pulse during each MCS reference. It is energized by the Stop Read signal from Memory Timing Chain core R^{05}_{09} at time 09.

9. START WRITE PULSE STRETCHER. - The function of the Start Write pulse stretcher circuit, Y^{37}_{02}, is to produce a signal that controls the length of the Write Current pulse during each MCS reference. The pulse stretcher is energized by the Start Write signal from Memory Timing Chain core R^{25}_{11} at time 11.

10. STOP WRITE PULSE DISCHARGER. - The function of the Stop Write pulse discharger circuit, Y^{27}_{03}, is to control the termination of the Write Current pulse during each MCS reference. The circuit is energized at time 17 by the Stop Write signal from Memory Timing Chain core R^{05}_{17}.

(7) DIGIT PLANE CONTROL CIRCUITS. - A separate Digit Plane Control circuit is associated with each of the 24 Magnetic Core Memory Planes. The Digit Plane Control circuit controls the writing of a "0" or a "1" in the core being addressed by controlling the Inhibit Current pulse. The Inhibit Current pulse is turned on to write a "0" in a core, and is not turned on when writing a "1" in a core.

(a) OPERATION DURING A WRITE SEQUENCE. - During an MCS Write sequence, the Z-register operates as a 24-bit Memory Data Register which

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temporarily stores the information to be written in an MCS address.

During the MCS Write sequence the operations performed in each Digit Plane Control circuit depend upon whether a "0" or a "1" is to be written. Because each Digit Plane Control circuit is electrically identical to the other 23 circuits, only the functioning of Digit Plane Control-0 circuit is explained below.

An MCS Write reference is produced by an Initiate to Memory signal which produces writing operations in certain bits of the selected MCS address. The information which was in each bit of the selected MCS address is read out of the cores and destroyed. The "1" signals produced in the sense amplifier circuits by the Clear Current Pulse sequence are not recognized and transmitted to the Z-register during a write reference, because no Read Probe signals are present for the designated bits of the selected address which are to receive new information.

The Inhibit Current control core R^{10}_{00} in the Digit Plane Control-0 circuit controls the Inhibit Current pulse. The inhibit current generator control core, R^{10}_{00}, is set to "1" at time 8 by the Start Inhibit Current core, R^{32}_{08}. If a "1" is to be written in bit-0 of the selected MCS address, the Z-register bit-0 control core, Z^{30}_{00}, is set to "1" by the computer prior to the beginning of the current MCS reference. The "1" in Z^{30}_{00} is transferred to Z^{00}_{00} at memory time 8. When Z^{00}_{00} is read out at time 9, the resulting "1" signal clears the inhibit current control core R^{10}_{00}. As a result, the "0" signal produced by core R^{10}_{00} at time 10 does not energize the Start Inhibit pulse stretcher Y^{21}_{00}, and the inhibit current generator IG00 is not turned on. A "1" is therefore written in bit-0 of the selected MCS address.

If a "0" is to be written in bit-0 of the MCS address, Z^{30}_{00} is cleared by

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the computer prior to the beginning of the current MCS reference. Therefore, when core Z^{00}_{00} is read out at time 9, the resulting "0" signal does not clear the inhibit current control core R^{10}_{00}.

When the inhibit current control core R^{10}_{00} is read out at time 10 the resulting "1" signal energizes the Start Inhibit pulse stretcher Y^{21}_{00}, and turns on the inhibit current generator circuit IG00. A "0" is therefore writtten in bit-0 of the selected MCS address.

(b) OPERATION DURING A READ SEQUENCE. - During a Read sequence the Z-register functions as a 24-bit restoration register that controls the Restore step, which restores the information destroyed by the reading operation.

Prior to the beginning of each Read sequence, the computer clears all stages of the Z-register to receive MCS Read signals from the selected address. During a Read sequence the operations performed in each Digit Plane Control circuit depend upon whether or not a "1" is read from the associated core memory plane. Because each Digit Plane Control circuit is similar electrically to the 23 other ciricuits, only the functioning of Digit Plane Control-0 circuit is explained below.

If a "1" is present in the selected address of core memory plane 0, a Sense signal is present on the memory plane sense wire during the first, or Read step of the sequence. This signal attempts to the pass through the logical AND circuit at the output of the sense amplifier. The sense "1" signal passes through this logical AND circuit because a Read Probe-0 pulse is also present, and sets the Z-register core Z^{30}_{00}. The MCS Restore step that occurs during a Read sequence functions in exactly the same manner as the MCS Write step previously explained in paragraph 7a.

If a "0" is present in the selected address of memory plane 0, no Sense signal is present on the core memory plane sense wire during the first, of

Read step of the sequence. Therefore, no Sense signal passes through the logical AND circuit at the output of the sense amplifier, and the Z-register core Z^{30}_{00} remains in the cleared state. The MCS Restore action has been explained above.

4-5. INPUT-OUTPUT SECTION

The Input-Output Section of the main computer consists of the I-register, O-register, F-register, C-register, and the communication lines. The I-register contains input information, the O-register contains output information, the F-register contains external function codes, and the C-register is a control register for input, output, and load mode sequences. The sequence of operation is controlled by enable, resume, disconnect, sense, and fault lines. These lines are included in the communication lines, and the remainder of the communication lines carry information to and from the I, O, and F-registers.

The theory of operation of each of the external devices is given in External Equipment , Volume 3, section 5.

a. INPUT. - The computer can receive information from an electric typewriter, photoelectric reader, high-speed reader, or the converter. The information is received in the I-register by one of two procedures. An input instruction transmits information during a regular computer program, but the Load Mode sequence can send information to the main machine before a program is initiated. The C-register controls the input operations and an External Disconnect signal is used to stop repeated input instructions.

The input sequences are much slower than the regular computer program, and if input instructions are programmed faster than the input device supplies data, execution is delayed until the data is available. As a means of saving computer time, an External Function Select signal is initiated

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and the computer goes on exceuting other instructions until such time as the Sense Input Lockout indicates that the Input register is loaded. Then an input instruction is executed which transfers the information from I to magnetic storage. As soon as the information is transferred to memory, another Select signal is generated. With the photoelectric reader as input, for instance, Bogart can execute at least 100 instructions with no loss of input speed.

(1) I-REGISTER. - The Input Register, shown in Drawing 87078, Volume 8, page 28, is a seven-stage register that receives information from the external equipment. The converter and the electric typewriter send information to the lower six bits only, but the high-speed mechanical reader and the photoelectric reader send information to all seven bits. A typical stage of the I-register is shown in Figure 4-51.

(a) BASIC PROPERTIES OF I. - The basic storage elements of each bit are two magnetic switch cores.

(b) TRANSMISSIONS TO AND FROM I. - The I-register is cleared by Core N_{59}^{20} before each input transmission.

1. CORE I^{00}. - Information is received from Y^{28} under the control of N_{69}^{20}.

2. CORE I^{20}. - Transmissions are made to X_{0-6} under the control of N_{15}^{20}.

(2) INPUT SEQUENCE. - The Input sequence, shown in Drawing 87726, Volume 9, pages 95-97, transmits information from the external equipment to the magnetic storage section. The information is received in storage as a six-bit, seven-bit, or twenty-four bit word.

(a) SIX-BIT WORD. - If $m \neq 0$ or 4 and the electric typewriter

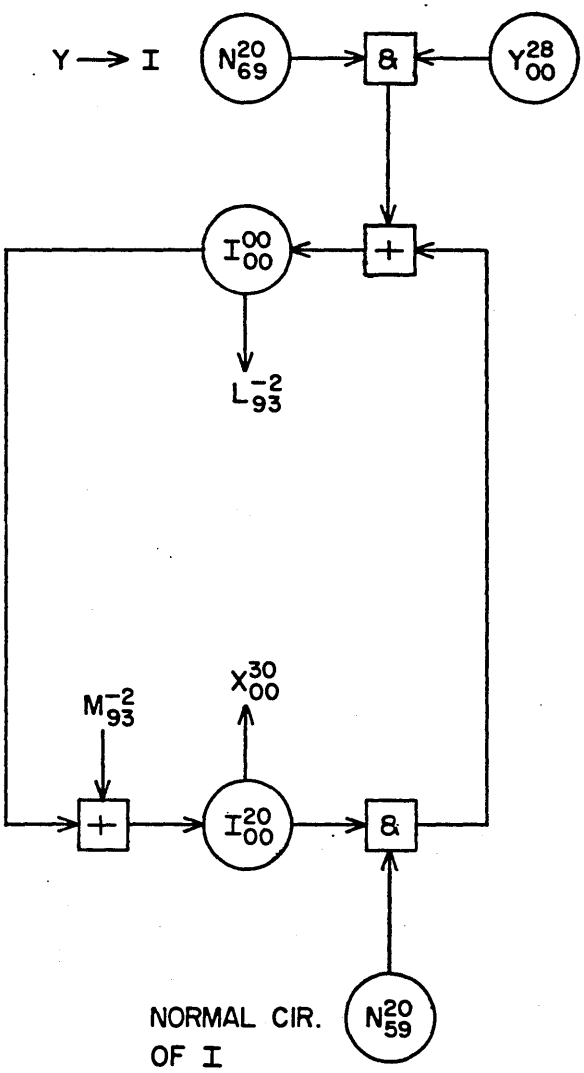

Figure 4-51. First Stage of I-register

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or the converter is selected as input, then six bits of information are transferred to the magnetic storage each time an input instruction is programmed.

When an input instruction is programmed, the Add B to U circulation bit (W^{00}_{02} - W^{20}_{02}) initiates the input sequence. First, the y portion of the U-register is modified and then V^{30}_{87} sets the Input Enable circulation bit (W^{10}_{31} - W^{30}_{31}) and the I to X circulation bit (W^{10}_{26} - W^{30}_{26}). The Input Enable circulation bit sends an Input Enable signal to the external equipment while the I to X circulation bit checks for an Input Resume signal.

If the I-register is loaded and an Input Resume signal was already received, the Input Resume bit (W^{10}_{65} - W^{30}_{65}) is set as indicated by the ILD light on the indicator display panel. A previous Input Resume occurs only if a Select Input function was previously programmed or if the input was repeated. If the I-register was not previously loaded and an Input Resume signal was not previously received, then the computer must wait until the external equipment receives the Input Enable signal, reads a character, and transfers the character with an Input Resume signal to the main cabinet. When the Input Resume signal is received, the Input Resume circulation bit is set and the computer is ready to proceed. If two Input Resumes are received before the contents of I can be sampled, then the Input Fault circulation bit (W^{10}_{42} - W^{30}_{42}) is set and the computer stops.

The I to X circulation bit (W^{10}_{26} - W^{30}_{26}) and the Input Resume circulation bit form a logical AND to set V^{20}_{87} which clears N^{00}_{10} (Normal Circulation of X control) and sets N^{20}_{15} (I to X control) thus transferring the six bits of information from I to X. A seventh bit of information is also transferred but since the converter and the electric typewriter transfer only six bits of

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information to I, the seventh bit of I always contains a zero and is not recognized. After the contents of I have been stored in X, V_{89}^{00} forms a logical AND with T_{51}^{00} ($m \neq 0,4$) to set the Write circulation bit (W_{13}^{20}- W_{13}^{00}). If the input instruction is not to be repeated, the Input Enable circulation bit (W_{31}^{10}- W_{31}^{30}) is also cleared at this time. Clearing of the Input Enable circulation bit as a result of the above conditions allows the last Input Enable signal to be sent to the external equipment for only twelve microseconds. Since the signal is short, it is ignored by the external equipment and no information is transferred to the main cabinet.

The Write circulation bit initiates the write sequence, and the information contained in the magnetic storage as determined by the value of m. If the instruction is to be repeated, the sequence starts over.

(b) SEVEN-BIT WORD. - If $m \neq 0$ or 4 and either the high-speed or photoelectric reader is selected as input, then seven bits of information are stored in magnetic storage. The procedure for receiving seven bits of information is similar to the procedure for receiving six-bits of information. The difference occurs because the photoelectric and high-speed readers transfer seven-bits of information to the I-register. Therefore, the contents of the lower seven bits of X will be recognized as information and placed in magnetic storage.

(c) TWENTY-FOUR BIT WORD. - If $m = 0, 4$, then four six-bit words are assembled in Q to form a complete twenty-four bit word, which is stored in the magnetic storage. If the high-speed reader or the photoelectric reader is used as an input device the information in the seventh bit is ignored.

When an Input instruction is programmed, the Add B to U circulation bit (W_{02}^{00}- W_{02}^{20}) initiates the Input sequence. First the lower 15 bits of U are

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modified by adding the contents of a specified B-box. Then V_{87}^{30} sets V_{52}^{10} which clears N_{80} (Normal Circulation of C) and sets N_{87}^{30} (Set C to d'd). When T_{10}^{30} (m = 0,4) is set, N_{24}^{20} (Normal Circulation of Q) is also cleared, making the contents of Q equal to "0". Core V_{87}^{30} also sets the Input Enable circulation bit (W_{31}^{10}- W_{31}^{30}) and the I to X circulation bit (W_{26}^{10}- W_{26}^{30}). The Input Enable circulation bit sends an Input Enable signal to the external equipment while the I to X circulation bit checks for an Input Resume. The Input Resume signals are received as explained under Six-Bit Word. When the Input Resume circulation bit is activated, it ANDs with the I to X circulation bit (W_{26}^{10}- W_{26}^{30}) to set V_{87}^{20} which in turn clears N_{10}^{00} (Normal Circulation of X control), sets N_{15}^{20} (I to X control), clears N_{80}^{30} (Normal Circulation of C control) and at the same time enables N_{81} (Shift C control). This sequence puts the contents of the seven-bit I-register into X and shifts the contents of C to d'c. Both T_{10}^{00} (m = 0,4) and T_{63}^{20} (C is not d'd) are set. When these cores are set, the contents of the lower six bits of X are sent to Q, the contents of Q are shifted left six places, and the I to X circulation bit is enabled. When the next Input Resume is received, the Input Resume circulation bit is set, the contents of I are sent to X, C is shifted to contain d'b, the contents of the lower six bits of X are sent to Q. Q is shifted left six places, and the I to X circulation bit is again enabled. The next Input Resume initiates the same sequence, shift C to d'a, and sets the I to X circulation bit. The Q-register now contains information in its upper 18 bits and the C-register contains d'a. When the next Input Resume signal is received by the main machine, the contents of I are sent to X and C is shifted to contain d'd. This sets T_{62}^{20} (C is d'd) and T_{64}^{00} (C is not a or b). Then the information in the lower six bits of X is sent to Q, so Q now contains a twenty-four bit word. If the instruction

is not to be repeated, the Input Enable circulation bit (W^{10}_{31}- W^{30}_{31}) is cleared. Clearing the Input Enable circulation bit as a result of the above conditions allows the final Input Enable signal to be sent to the external equipment for only twelve microseconds. A short signal such as this is ignored by the external equipment.

Next the N^{00}_{10} core (Normal Circulation of X) is cleared, while N^{30}_{23} (Q to X control), and the Write circulation bit (W^{00}_{13}- W^{20}_{13}) are set. Then if m=0, a twenty-four bit word is placed in magnetic storage, and if m=4, information is stored in the lower fifteen bits of the memory section.

(3) LOAD MODE SEQUENCE. - The Load Mode sequence, shown in Drawing No. 87733, volume 9, pages 110-111, provides a means for loading the magnetic storage without using program control. The address and information that is to be sent to memory is put on punched paper tape and read by either the high-speed reader or photoelectric reader.

When the Load Mode/Master Clear switch located on the Bogart switch panel is put in the LOAD MODE position, all the registers are cleared and the Clear Q Load Mode circulation bit (W^{00}_{98}- W^{20}_{98}) is set. Then N^{20}_{24} (Normal Circulation of Q) is cleared, and the Input Enable and I to X circulation bits are set. An input Enable is then sent to the selected input equipment, enabling it to read the first frame. When the external equipment is ready to transmit information to the I-register, an Input Resume signal is sent to the computer which clears N^{10}_{59} (Normal Circulation of I), while the Input Resume circulation bit and Core N^{20}_{69} (Input to I) are set, transferring the data in the first frame. As soon as the Input Resume and the Input Enable circulation bits are set, the sequence is ready to proceed.

At this point the tape's seventh level (control level) determines what

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type of information is contained on the tape. There are three possible combinations: Insert Address (d'ad), Check Address (d'bd), and Enter Data (d'd) as shown in the example below. The d' position is the d position of the preceding word. For more information about the tape, see Paper Tape section in volume 3.

DIRECTION OF TAPE →

d c b a d'	d c b a d'	d c b a d'	
o o o	o o o	o o	Level 6 Control level
Insert Address(d'ad)	Check Address(d'bd)	Enter Data(d'd)	

Example 1.

(a) INSERT ADDRESS (d'ad). - The Insert Address sequence puts the first storage address in the lower twelve bits of U. If it is the first information on the tape, it must be preceded by a d' in the preceding frame. This d'sets the value of the C-register to d at the time the first frame is read.

Proceeding with the Load Mode sequence after the Input Resume and the I to X circulation bits are set, the information in I is sent to X, the C-register is shifted to contain c, and the upper bit of I is checked for a "1". Since level six of the first frame of the insert address sequence contains a "1", the d level of the C-register is set and the C now contains cd. The information in the lower six bits of X is then transferred to the Q-register, Q is left-shifted six places, and the I To X circulation bit is set. When the information in the second frame is read, the Input Resume circulation bit is set. Then the contents of I are sent to X, the

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C-register is shifted to bc, and since level six of the second frame contained a "0", C remains bc. The information in the lower six bits of X is sent to the Q-register, Q is left-shifted six places and the I to X circulation bit is set. The Input Resume circulation bit is set when the third frame has been read. The information in I is now transferred to X, the C-register is shifted to ab and is unchanged because level six of the third frame is "0", the lower six bits of X are sent to the Q-register, Q is left-shifted six places, and the I to X and Input Enable circulation bits are again set. When the last frame is read, the Input Resume circulation bit is set, the contents of I are sent to X, and the C-register is shifted to d'a. The last frame contains a "1" in the control level, so the C-register is changed to d'ad. The information in the lower six bits of X is sent to Q, the Input Enable signal is terminated, the contents of Q are transferred to X, the information in the lower fifteen bits of X is sent to U, and the Clear Q Load Mode circulation bit (W^{00}_{98}- W^{20}_{98}) is set, preparing the machine to read the next four frames of information. The U-register now contains the first address and the computer is ready to accept subsequent information.

(b) CHECK ADDRESS (d'bd). - The Check Address sequence checks the address in U to determine if the U-register has been advancing the address each time. This is accomplished by putting the correct address in A and then subtracting the actual address contained in U. If the difference is zero, the address checks, but if the difference is not zero, a Load Check Fault is recognized and the computer stops. Each time the address checks, the P-register is advanced by one.

Proceeding with the Load Mode sequence after the Input Resume circulation bit and the I to X circulation bit are set, the information in I is sent to X,

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the C-register is shifted to contain c, and since the upper bit of I contains a "0" , C is unchanged. The contents of the lower six bits of X are sent to the Q-register, Q is left-shifted six places, the I to X circulation bit is set, and when the Input Resume signal is received signifying that the contents of the second frame is now in I, the Input Resume circulation bit is set. Then I is sent to X, the C-register is shifted to b, and since the control level of the second frame contains a "1", the contents of C are changed to bd. The contents of X_{0-5} are transferred to Q, Q is left-shifted six places, the next frame of information is received in I, the contents of I are sent to X, C is shifted to ac and unchanged by level six of the third frame, X_{0-5} is again sent to Q, and Q is left-shifted six places. When the information from the last frame is received in the I-register, the contents of I are sent to X, and C is shifted to d'b. Since the control level of the last frame contains a "1", the contents of C are changed to d'bd. The information in the lower six bits of X is sent to Q, the Input Enable signal is terminated, the contents of Q are sent to X and transferred to A, the U to X circulation bit (W^{10}_{15}- W^{30}_{15}) is set, and the Clear Q Load Mode circulation bit is activated in preparation for the next four frames of information. After the U to X circulation bit is set, the contents of U are sent to X, and X is subtracted from A. If the contents of A are zero, the P-register is advanced by one and the Load Mode sequence continues. However, if A is not zero, the Load Check Fault circulation bit (W^{10}_{43}- W^{30}_{43}) is set, and the computer stops.

(c) ENTER DATA (d'd). - The Enter Data sequence stores the information in magnetic storage at the address designated by U, and then advances U to the next address.

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Preceding with the Load Mode sequence after the Input Resume circulation bit and the I to X circulation bit are set, the information in I is sent to

X, C is shifted to c and is left unchanged because the control level contains a "0". The contents of X_{0-5} are sent to Q, Q is left-shifted six places, and when I is loaded with information from the second frame, the contents of I are sent to X. The C-register is shifted to b, level six of the second frame is "0" so C is unchanged, information in X_{0-5} is transferred to Q, Q is left-shifted six places, and the I register receives information from the third frame. The contents of I are transmitted to X, C is shifted to a and unchanged because level six is "0", and the contents of X_{0-5} are sent to Q. Then Q is left-shifted six places. When the information in the last frame is sent to I, the contents of I are transferred to X, and C is shifted to d'. Level six of the last frame contains a "1" which changes the contents of C to d' d. Q receives information from X_{0-5} and then transfers its entire contents to X. The Input Enable signal is terminated, the Clear Q Load Mode circulation bit (W^{00}_{98} - W^{20}_{98}) is set, and the Write circulation bit (W^{00}_{13} - W^{20}_{13}) is set. The Clear Q Load Mode circulation bit prepares the computer to receive the next block of information, while the Write circulation bit initiates the Write sequence which stores the contents of X in memory at the address specified by U, and advances U to the next address.

(4) C-REGISTER. - The C-register, shown in Drawing 87206, Volume 8, page 34, is a five-stage register that controls the assembling of 24-bit words during input instructions or Load Mode, the disassembling of 24-bit words during output instructions, the inserting of addresses during Load Mode, and the checking of addresses during Load Mode. The five stages are lettered from left to right as d', a, b, c, d. The register has left-shift properties and also has an a to d end around shift.

(a) BASIC PROPERTIES OF C. - The basic storage elements of each bit are two magnetic switch cores.

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(b) STAGE d'. - This stage receives information from N_{87} (set C to d'd). It is cleared when N^{31}_{80} is cleared.

(c) STAGE a. - This stage shifts information to d' during input or output instructions under control of N^{31}_{81} (Shift C) and to d' during Load Mode under control of N^{32}_{81} (C). It is cleared when N^{30}_{80} is negated.

(d) STAGE b. - This stage shifts information to a under control of N^{30}_{81} (Shift C) and is cleared when N^{30}_{80} is negated.

(e) STAGE c. - This stage shifts its contents to b under control of N^{30}_{81} (Shift C) and is cleared when N^{30}_{80} is negated.

(f) STAGE d. - This stage shifts its contents to c under control of N^{30}_{81} (Shift C). It receives information from I^{00}_{06} during Load Mode sequence and is cleared by N^{30}_{80}.

(5) EXTERNAL DISCONNECT. - The External Disconnect sequence, shown in Drawing 87726, Volume 9, page 95, is initiated when a selected input device is unable to transfer information to the computer.

The External Disconnect signal clears the I to X circulation bit, clears the Repeat Sequence Control circulation bit, and initiates the Read Next Instruction sequence.

b. OUTPUT

(1) O-REGISTER. - The Output register, shown in Drawing 87078, Volume 8, page 28, is a seven-stage register that sends information to the external equipment. The converter and the electric typewriter receive information from the lower six bits of the O-register, but the high-speed punch receives information from all seven bits. A typical stage of the O-register is shown in Figure 4-52.

(a) BASIC PROPERTIES OF O. - The basic storage elements of each bit are two magnetic switch cores.

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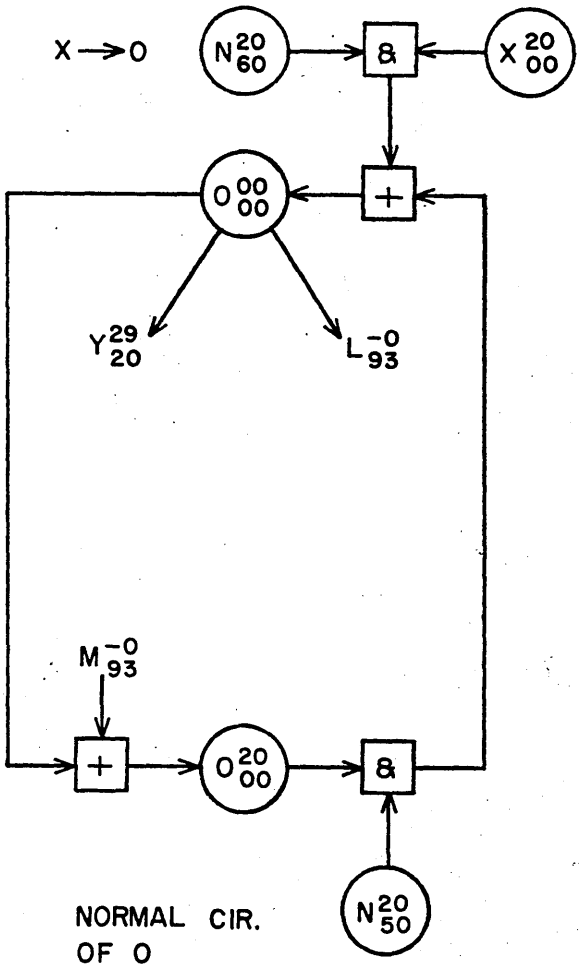

FIRST STAGE OF O-REGISTER

Figure 4-52. First Stage of O-register

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(b) TRANSMISSION TO AND FROM O. - Before transmission to O the register is cleared by N_{50}^{20}.

1. CORE O^{00}. - Inputs from X_{0-6} are controlled by N_{60}^{20} and information is transferred to the external equipment.

2. CORE O^{20}. - This core can be set by the manual push-button on the indicator display panel.

(2) OUTPUT SEQUENCE. - The Output sequence, shown in Drawing 87727, Volume 9, pages 98-100, transfers information from the magnetic storage to the external equipment. The information is taken from magnetic storage either as a six-bit word, seven-bit word, or a 24-bit word which is disassembled and sent out in six-bit increments.

(a) SIX OR SEVEN BIT WORD. - If m $\neq$ 0 or 4 and the electric typewriter or the converter is selected as input, then six bits of information are transferred to the selected equipment. If the high-speed punch is selected and m $\neq$ 0 or 4, then seven bits of information will be transferred each time an output instruction is programmed.

When an output instruction is programmed, the Read Operand circulation bit (W_{03}^{00}- W_{03}^{20}) initiates the Read sequence which takes information from magnetic storage as designated by m and puts the information into the lower eight bits of X. The X to O circulation bit (W_{28}^{10}- W_{28}^{30}) is then set.

The Master Clear sequence sets the Output Resume circulation bit (W_{66}^{30}- W_{66}^{10}) so the first output instruction after the Master Clear sequence does not wait for an Output Resume signal. On the other hand, if there was a previous output instruction, the computer must wait until it receives an Output Resume signal indicating that the external equipment has recorded the previous output data and is ready for more information. The Output Resume signal sets the Output Resume circulation bit. When the X to O circulation bit and the Output Resume

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circulation bit are set, the 0-register will be cleared and the contents of the lower seven bits of X sent to the 0-register. The Output Enable signal is then sent to the external equipment. When the electric typewriter or the converter are selected and receive an Output Enable signal, they sample the contents of the lower six bits of the 0-register; but if the high-speed punch was selected and receives an Output Enable signal, it samples the contents of all seven bits of the 0-register.

(b) TWENTY-FOUR BIT WORD. - If m = 0 or 4, a complete 24-bit word is taken from memory, disassembled, and sent to the selected output six bits at a time.

When an output instruction is programmed, the Read Operand circulation bit (W^{00}_{03}- W^{20}_{03}) initiates the Read cycle which takes a 24-bit word from memory when m = 0, puts the information in X, and sets the X to Q circulation bit (W^{00}_{25}- W^{20}_{25}). Next, the contents of X are set to Q, the C-register is set to d'd and shifted to d'c, the shift circuitry is set, Q is shifted left six places, and the Q to X circulation bit (W^{10}_{27}- W^{30}_{27}) is set. Next, the lower six bits of Q are sent to X, and the X to 0 circulation bit (W^{10}_{28}- W^{30}_{28}) is set.

The Output Resume circulation bit (W^{10}_{66}- W^{30}_{66}) is set when the conditions exist as described in the paragraph on Six or Seven-bit Words.

When the X to 0 circulation bit and the Input Resume circulation bit are set the contents of X are sent to the 0-register, and since only six-bits of information were sent from Q to X, the seventh bit of the 0-register will always contain a zero. The Output Enable signal is sent to the external equipment and it samples the contents of the 0-register. Then since C is d'c, the C-register is shifted to contain d'b, Q is left-shifted six places, the lower six-bits of Q are sent to X, and the X to 0 circulation bit is set. When an

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Output Resume signal is received, the contents of X are transferred to the O-register, and an Output Enable signal is initiated. Because C is d'b, C is shifted to d'a, Q is left-shifted six places, the lower six bits of Q are sent to X, the contents of X are sent to the O-register when an Output Resume signal is received, and an Output Enable signal is sent to the external equipment. The contents of C are d'a, so C is shifted to contain d'd, Q is left-shifted six places, the information in the lower six bits of Q is sent to X, and when an Output Resume signal is received, the contents of X are transferred to the O-register. An Output Enable signal is sent to the external equipment, and since C contains d'd, the output sequence is completed.

c. EXTERNAL FUNCTION. - The External Function enables the computer to select and operate the output equipment through the program by using various codes. These codes are first put in the F-register, then the computer signals the external equipment that the F-register contains a code, and finally the external equipment completes the specified operation.

(1) F-REGISTER. - The F-register, shown in Drawing 87073, Volume 8, page 20, is a fifteen-stage register that controls external operations. A typical stage of the F-register is shown in Figure 4-53.

(a) BASIC PROPERTIES OF F. - The basic storage elements of each bit are two magnetic switch cores.

(b) TRANSMISSIONS TO AND FROM F. - Before transmissions are made to F, the register is cleared by N^{20}_{58}.

1. CORE F^{00}. - This core transmits information to the external equipment.

2. CORE F^{20}. - This core receives information from the U-register under the control of N_{68}.

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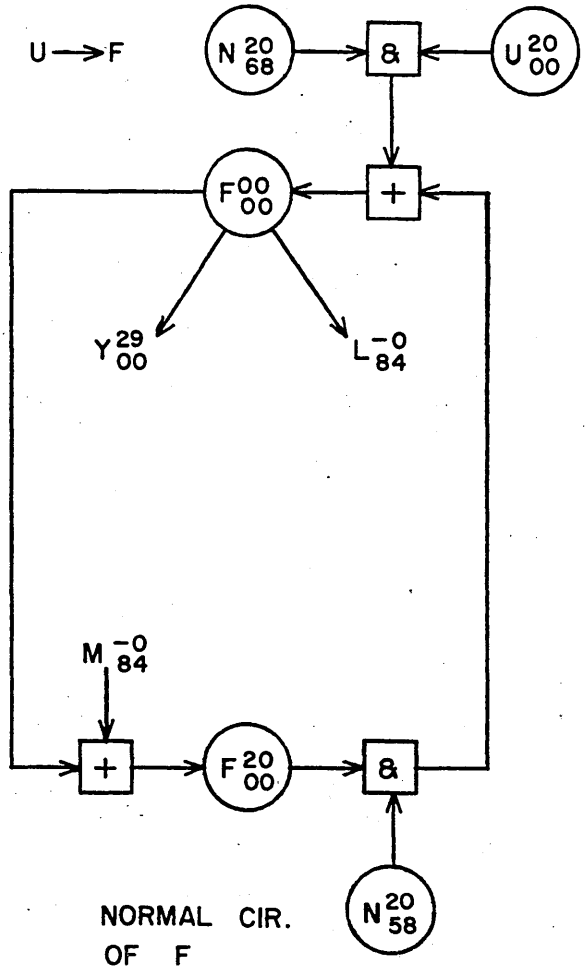

FIRST STAGE OF F-REGISTER

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Figure 4-53. First Stage of F-register

(2) EXTERNAL FUNCTION CODES. - On all external function instructions the 15-bit F-register contains the control code which is interpreted by the external equipment according to the following conventions:

xxx	xxx	xxx	xxx	xxx	F-register (binary)
X	X	X	X	X	F-register (octal)
a	b	c	d	e	

Let the symbols a, b, c, d, and e represent the octal digit positions in the F-register in descending order. Then the following are generalized interpretations for the individual digits of the external function codes.

(a) CLASS DESIGNATION. - This digit is constantly monitored by all external units. When a class designation other than zero is specified, the unit designated in the remainder of the code is to supercede the currently assigned unit in the specified class. This means that the currently assigned unit in that class must recognize this fact and disconnect itself from the line. The octal digit assignments specifying the various classes are:

0 (EXTERNAL CONTROL). - This condition indicates that an external control function is to be executed. The external control generally consists of power switching rather than switching of information signals. In the converter, however, three functions not considered strictly power switching are preceded by "0". These are: Write Tape Mark, Rewind Last-Selected Unit, and Backspace Last-Selected Unit.

1 (INPUT or READ SELECTION). - The presence of the Input or Read function indicates that a new external input is to be connected to the input lines.

2 (OUTPUT or WRITE SELECTION). - The presence of the Output or Write function indicates that a new external output is to be connected to the output lines.

4 (SENSE SELECTION). - The presence of the Sense function indicates that a new external unit is to be connected to the external sense line.

3, 5, 6, 7 (EXTERNAL FAULT). - The presence of any one of these conditions will cause the external fault line to be energized.

(b) CONTROL DESIGNATION. - This digit of the external function code designates which of the external control units will interpret the remainder of the digits. The following list assigns a value for this digit to each of the types of external equipment.

1) RELAY CONTROL

2) TYPEWRITER CONTROL

3) PAPER TAPE CONTROL

4) CONVERTER CONTROL

(c) FUNCTION DESIGNATION. - The Function digits are interpreted by the various external control units and specify the particular function to be performed by that unit.

In the case of control designators (digit b) other than 4, these functions consist of starting or stopping motors and energizing or dropping relays. For control designation 4 (converter) the functions are as follows:

0 - perform function (digit a) on last-selected unit

1 - perform function (digit a) on selected card reader

2 - perform function (digit a) on selected tape unit

3 - perform function (digit a) on card punch

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4 - perform function (digit a) on printer

Since the Sense condition (digit a=4) will not change the status of any piece of equipment, the control designator is not important (as evidenced by X in the c digit position) for this operation.

(d) SUB-UNIT DESIGNATION. - These digits are interpreted by the various external units and may have a different meaning in each case. For the magnetic tape portion of converter control, this specifies the number of the tape unit; for relay control, this specifies the relay number.

(e) Same as (d) above.

(f) LEGAL CODES. - The following is a list of codes recognized by the external equipment and the function of each code. An X represents an insignificant octal digit for the case being considered.

0 X X X X	EXTERNAL CONTROL
0 1 X X X	External Relay Control
0 1 1 0 1 0 1 5 0 1	Energize Relay One
0 1 1 0 2 0 1 5 0 2	Energize Relay Two
0 1 1 0 3 0 1 5 0 3	Energize Relay Three
0 1 2 0 1 0 1 6 0 1	Release Relay One
0 1 2 0 2 0 1 6 0 2	Release Relay Two
0 1 2 0 3 0 1 6 0 3	Release Relay Three
0 2 X X X	Typewriter Control
0 2 1 X X 0 2 5 X X	Start Motor
0 2 2 X X 0 2 6 X X	Stop Motor

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0 3 X X X Paper Tape Control

0 3 1 X 1 0 3 5 X 1	Start Photoelectric Reader Motor
0 3 1 X 2 0 3 5 X 2	Start High-Speed Reader Motor
0 3 1 X 4 0 3 5 X 4	Start High-Speed Punch Motor
0 3 1 X 7 0 3 5 X 7	Start ALL Motors
0 3 1 X 5 0 3 5 X 5	Start Photoelectric Reader/High-Speed Punch Motor
0 3 1 X 6 0 3 5 X 6	Start High-Speed Reader/High-Speed Punch Motor
0 3 2 X 1 0 3 6 X 1	Stop Photoelectric Reader Motor
0 3 2 X 2 0 3 6 X 2	Stop High-Speed Reader Motor
0 3 2 X 4 0 3 6 X 4	Stop High-Speed Punch Motor
0 3 2 X 7 0 3 6 X 7	Stop ALL Motors
0 3 2 X 5 0 3 6 X 5	Stop Photoelectric Reader/High-Speed Punch Motor
0 3 2 X 6 0 3 6 X 6	Stop High-Speed Reader and High-Speed Punch Motor

0 4 X X X Converter Control

0 4 0 0 0 0 4 0 1 0 0 4 0 2 0 0 4 0 3 0	Turn off I/O indicator of last-selected unit
0 4 0 0 1 0 4 0 1 1 0 4 0 2 1 0 4 0 3 1	Write Tape mark on last-selected tape

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0 4 0 0 2 0 4 0 1 2 0 4 0 2 2 0 4 0 3 2	Rewind last selected tape
0 4 0 0 3 0 4 0 1 3 0 4 0 2 3 0 4 0 3 3	Turn on I/O Indicator of last-selected unit
0 4 0 0 4 0 4 0 1 4 0 4 0 2 4 0 4 0 3 4	Backspace last selected unit
0 4 1 0 0 0 4 1 2 0 0 4 1 4 0 0 4 1 6 0	Select Card reader
0 4 2 0 0 0 4 2 2 0 0 4 2 4 0 0 4 2 6 0	Select tape unit 0
0 4 2 0 1 0 4 2 2 1 0 4 2 4 1 0 4 2 6 1	Select tape unit 1
0 4 2 0 2 0 4 2 2 2 0 4 2 4 2 0 4 2 6 2	Select tape unit 2
0 4 2 0 3 0 4 2 2 3 0 4 2 4 3 0 4 2 6 3	Select tape unit 3
0 4 2 0 4 0 4 2 2 4 0 4 2 4 4 0 4 2 6 4	Select tape unit 4
0 4 2 0 5 0 4 2 2 5 0 4 2 4 5 0 4 2 6 5	Select tape unit 5

0 4 2 0 6 0 4 2 2 6 0 4 2 4 6 0 4 2 6 6	Select tape unit 6
0 4 2 0 7 0 4 2 2 7 0 4 2 4 7 0 4 2 6 7	Select tape unit 7
0 4 2 1 0 0 4 2 3 0 0 4 2 5 0 0 4 2 7 0	Select tape unit 8
0 4 2 1 1 0 4 2 3 1 0 4 2 5 1 0 4 2 7 1	Select tape unit 9
0 4 3 0 0 0 4 3 2 0 0 4 3 4 0 0 4 3 6 0	Select Card Punch
0 4 4 0 0 0 4 4 2 0 0 4 4 4 0 0 4 4 6 0	Select Printer

1 X X X X INPUT SELECTION

1 2 X X X Typewriter Input

1 2 X X X Select typewriter input

1 3 X X X Paper-Tape Input

1 3 X X 1 1 3 X X 5	Select Photoelectric reader input
1 3 X X 2 1 3 X X 6	Select High-Speed reader input

1 4 X X X Converter Input

1 4 1 0 0 1 4 1 2 0 1 4 1 4 0 1 4 1 6 0	Read cards

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1 4 2 0 0 1 4 2 2 0	Read tape unit 0 (coded)
1 4 2 0 1 1 4 2 2 1	Read tape unit 1 (coded)
1 4 2 0 2 1 4 2 2 2	Read tape unit 2 (coded)
1 4 2 0 3 1 4 2 2 3	Read tape unit 3 (coded)
1 4 2 0 4 1 4 2 2 4	Read tape unit 4 (coded)
1 4 2 0 5 1 4 2 2 5	Read tape unit 5 (coded)
1 4 2 0 6 1 4 2 2 6	Read tape unit 6 (coded)
1 4 2 0 7 1 4 2 2 7	Read tape unit 7 (coded)
1 4 2 1 0 1 4 2 3 0	Read tape unit 8 (coded)
1 4 2 1 1 1 4 2 3 1	Read tape unit 9 (coded)
1 4 2 4 0 1 4 2 6 0	Read tape unit 0 (binary)
1 4 2 4 1 1 4 2 6 1	Read tape unit 1 (binary)
1 4 2 4 2 1 4 2 6 2	Read tape unit 2 (binary)
1 4 2 4 3 1 4 2 6 3	Read tape unit 3 (binary)
1 4 2 4 4 1 4 2 6 4	Read tape unit 4 (binary)
1 4 2 4 5 1 4 2 6 5	Read tape unit 5 (binary)
1 4 2 4 6 1 4 2 6 6	Read tape unit 6 (binary)

1 4 2 4 7
1 4 2 6 7 Read tape unit 7 (binary)

1 4 2 5 0
1 4 2 7 0 Read tape unit 8 (binary)

1 4 2 5 1
1 4 2 7 1 Read tape unit 9 (binary)

2 X X X X OUTPUT SELECTION

2 2 X X X Select Typewriter Output

2 2 X X X Select typewriter output

2 3 X X X Select Paper-Tape Output

2 3 X X X Select High-Speed punch output

2 4 X X X Converter Output

2 4 2 0 0
2 4 2 2 0 Write tape unit 0 (coded)

2 4 2 0 1
2 4 2 2 1 Write tape unit 1 (coded)

2 4 2 0 2
2 4 2 2 2 Write tape unit 2 (coded)

2 4 2 0 3
2 4 2 2 3 Write tape unit 3 (coded)

2 4 2 0 4
2 4 2 2 4 Write tape unit 4 (coded)

2 4 2 0 5
2 4 2 2 5 Write tape unit 5 (coded)

2 4 2 0 6
2 4 2 2 6 Write tape unit 6 (coded)

2 4 2 0 7
2 4 2 2 7 Write tape unit 7 (coded)

2 4 2 1 0
2 4 2 3 0 Write tape unit 8 (coded)

2 4 2 1 1
2 4 2 3 1 Write tape unit 9 (coded)

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2 4 2 4 0 2 4 2 6 0	Write tape unit 0 (binary)
2 4 2 4 1 2 4 2 6 1	Write tape unit 1 (binary)
2 4 2 4 2 2 4 2 6 2	Write tape unit 2 (binary)
2 4 2 4 3 2 4 2 6 3	Write tape unit 3 (binary)
2 4 2 4 4 2 4 2 6 4	Write tape unit 4 (binary)
2 4 2 4 5 2 4 2 6 5	Write tape unit 5 (binary)
2 4 2 4 6 2 4 2 6 6	Write tape unit 6 (binary)
2 4 2 4 7 2 4 2 6 7	Write tape unit 7 (binary)
2 4 2 5 0 2 4 2 7 0	Write tape unit 8 (binary)
2 4 2 5 1 2 4 2 7 1	Write tape unit 9 (binary)
2 4 3 0 0 2 4 3 2 0 2 4 3 4 0 2 4 3 6 0	Punch Cards
2 4 4 0 0 2 4 4 2 0 2 4 4 4 0 2 4 4 6 0	Print on Tabulator

4 X X X X SENSE SELECTION

4 1 X X X Sense Relay Control

4 1 X 0 1 Sense Relay One

4 1 X 0 2 Sense Relay Two

4 1 X 0 3 Sense Relay Three

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4 1 X 1 1
4 1 X 3 1 Sense Switch One
4 1 X 5 1
4 1 X 7 1

4 1 X 1 2
4 1 X 3 2 Sense Switch Two
4 1 X 5 2
4 1 X 7 2

4 1 X 1 3
4 1 X 3 3 Sense Switch Three
4 1 X 5 3
4 1 X 7 3

4 3 X X X Sense Paper-Tape Control

4 3 X X 1
4 3 X X 5 Sense No Tape in Photoelectric Reader

4 3 X X 2
4 3 X X 6 Sense No Tape in High-Speed Reader

4 4 X X X Sense Converter Control

4 4 X X 0 Sense any (of the following) conditions

4 4 X X 1 Sense Read/Write Check

4 4 X X 2 Sense I/O Indicator

4 4 X X 3 Sense Short Transfer

4 4 X X 4 Sense Long Transfer

(3) EXTERNAL FUNCTION SEQUENCE. - The External Function sequence, shown in Drawing 87725, Volume 9, page 94, sends an External Function code to the external equipment initiating a specified operation.

The External Function (instruction 70) sets the Add B to U circulation bit (W^{00}_{02} - W^{20}_{02}) which, when cleared, adds the contents of the specified B-box to the lower fifteen bits of U and sets the External Function circulation bit (W^{10}_{30} W^{30}_{30}).

The Master Clear sequence sets the External Function Resume circulation bit (W^{10}_{67} - W^{30}_{67}) so the first external function instruction after the master

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clear sequence does not wait for an External Function Resume signal. If there was a previous external function instruction, the computer must wait for an External Function Resume signal signifying that the previous function is completed. The External Function Resume signal sets the External Function Resume circulation bit (W^{10}_{67} - W^{30}_{67}).

When the External Function circulation bit and the External Function Resume circulation bit are set, the contents of the lower fifteen bits of U are sent to the F-register, an External Function Enable signal is generated, and the contents of the F-register are sampled by the external equipment.

(a) EXTERNAL COMMUNICATION LINES. - There are a total of 38 communication lines between the main machine and peripheral equipment. These lines are directly coupled and are of identical electrical characteristics. (See Drawing 87543, Volume 12, page 2.)

1. FUNCTION LINES (15). - These lines originate in the main cabinet and are continually monitored by the external equipment. The electric typewriter receives information from 14 lines; 11 lines send information to the high-speed reader, high-speed punch, and photoelectric reader, while the converter receives information from all 15 lines.

2. FUNCTION ENABLE LINE (1). - The External Function Enable line originates in the main computer and goes to all external equipment. This line is energized in the execution of an external function instruction and signals the external equipment that the F-register lines are ready for translation.

3. FUNCTION RESUME LINE (1). - The External Function Resume line originates in the external equipment and terminates in the main cabinet. This line signals the computer that the external function has been performed.

4. INPUT LINES (7). - The input lines originate in the external equipment and terminate in the computer. Only six input lines transfer information from the converter and electric typwriter, but the high-speed reader and photoelectric reader send information through seven input lines.

5. INPUT ENABLE LINE (1). - This line originates in the main cabinet and signals the external equipment that an input operation should proceed. This line is energized directly by the input instruction code in the main cabinet and remains energized until the instruction is completed. It signals the external equipment that the computer is ready for more information.

6. INPUT RESUME LINE (1). - The Input Resume originates in the external equipment and terminates in the computer. This line is activated and de-activated at a rate determined by the input equipment and is asynchronous with the main machine. The line is activated at the time the input lines are to be sampled and de-activated any time before the next sample period. It signals the main computer that the external equipment is ready to transmit more information.

7. OUTPUT LINES (7). - The Output lines originate in the computer and go to each piece of output equipment. Only six output lines go to the converter and electric typewriter, but all seven lines go to the high-speed punch.

8. OUTPUT ENABLE LINE (1). - The Output Enable originates in the computer and signals the external equipment that an output operation should proceed. This line monitors the 0-register lockout and is energized as long as the register contains output information.

9. OUTPUT RESUME LINE (1). - The Output Resume line originates in the external equipment and terminates in the main computer. This

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line is activated and de-activated by the external equipment and is asynchronous with the main machine. The line is activated at the time the output lines are sampled and de-activated any time before the next sample period. It signals the computer control that the output register is available for a new entry.

10. EXTERNAL SENSE LINE (1). - The External Sense line originates in the external equipment and terminates in the main computer. This line monitors an external condition as specified by a previous external function and is available for sensing by the Sense Jump instruction.

11. EXTERNAL DISCONNECT LINE (1). - The External Disconnect originates in the external equipment and is energized in the event that the external unit can no longer participate in a transmission with the computer It clears the Repeat bit register and initiates the Read Next Instruction sequence after the completion of the current instruction cycle.

12. EXTERNAL FAULT LINE (1). - This line originates in the electric typewriter and terminates in the main cabinet. It is energized when an external code of 3 X X X X, 5 X X X X, 6 X X X X, or 7 X X X X is called for. When energized it causes the computer to stop operation and turn on the Temperature Fault (TFT) light. Fault lines to the Converter and PT Cabinet are included in the External Communications Cable, but are not connected to those units.

4-6. POWER AND COOLING

a. GENERAL. - The Bogart computer is designed to operate on the power usually available from power companies in the U.S.: 115 vac, 60 cps one-phase power, and 208 vac, 60 cps, three-phase power. The 115 vac is used directly to operate certain non-computing elements such as blowers, interlock relays, etc. In order to obtain a voltage which is free from power surges, reliably constant, and more easily filtered after rectification, the 208 vac is converted

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to 200 vac, 400 cps, three-phase power by a motor-generator combination. This power is then voltage-regulated and distributed to various transformers and power supplies.

In order to prevent excessive ambient temperatures from damaging components, a cooling system is furnished with the Bogart computer. The heat produced by power dissipation in electronic circuits (especially vacuum-tube filaments) is carried off by forced convection of water-cooled air.

b. POWER SUPPLY AND DISTRIBUTION. - The main power supply for the Bogart computer consists of a motor-generator which furnishes regulated a-c power to all units. Each unit then converts the a-c power into its required a-c and d-c voltages by using transformers and rectifier circuits.

The various motors are run by unregulated a-c power from the house wiring. Fuses and circuit breakers are used for overload protection.

(1) PRIMARY POWER DISTRIBUTION. - The house wiring furnishes 208 vac, three-phase, 60 cps and 115 vac, one-phase, 60 cps power for operation of the computer. The 208 vac power supply, shown in Drawing 87741, Volume 11, page 5, operates the motor-generator that supplies the 200 vac, 400 cps power. This power is regulated by the exciter-regulator before it reaches the computing equipment. The 115 vac power is distributed and used as described in 115 vac Distribution section.

(a) MOTOR-GENERATOR. - This unit furnishes 400 cps a-c power to the main computer. A 25-horsepower induction type motor, operating on 208 vac, three-phase, 60 cps, drives the generator at 3510 RPM. The generator is a 15 kva, 200 volt, 400 cps, three-phase inductor alternator. (See Figure 4-54).

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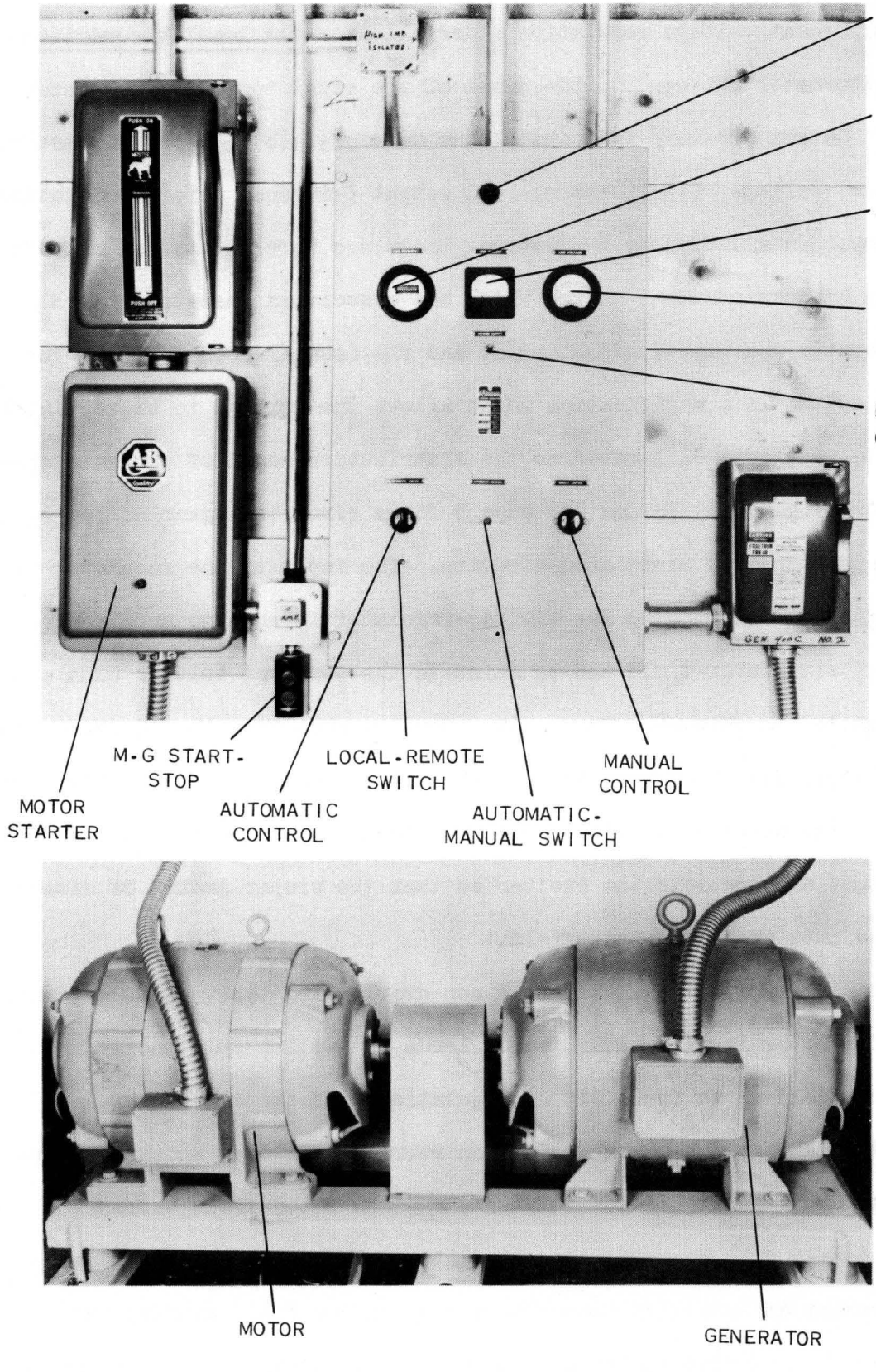

Figure 4-54. Motor Generator and Exciter Regulator Controls

(b) EXCITER-REGULATOR. - The exciter-regulator provides a plus or minus one percent voltage regulation under all balanced loading conditions within the alternator rating. On the panel of the regulator are found three meters: (a) Output ammeter, indicating Line Current; (b) Output voltmeter, indicating Line Voltage, (c) Vibrating-reed output frequency meter, indicating Line Frequency. In addition to the meters, there are three switches, one Off/On switch, an Automatic/Manual switch which has associated rheostat controls for both Automatic and Manual adjustments, and the Local/Remote Switch. The Local/Remote switch is a modification which allows the voltage to be regulated by a remote voltage control located on the distribution panel of the main computer. See Drawing 87741, Volume 11, page 5 for a circuit diagram of the motor-generator, regulator, and associated circuits. The input to the regulator is 115 vac, single-phase, 60 cps. The exciter-regulator is used to supply direct current to the alternator field and to maintain the terminal voltage constant as load is applied or removed. The exciter section rectifies the 60-cycle power and delivers direct current to the alternator field. The regulator section rectifies the alternator output voltage, compares it to a standard direct current voltage, and controls the exciter so that the proper amount of direct current is fed into the alternator field.

The electronic exciter-regulator is a non-overloading type. That is, with unity power factor or lagging power factor loads, it will supply increasing current to the field up to the limit of regulation. If the alternator is loaded beyond this point, no more excitation current will flow and the alternator will act as if excited constantly with maximum rated field current. No immediate damage will occur to the alternator unless this condition is continous, whereby an excessive temperature rise in the field winding may occur. During this condition, the alternator output voltage will drop sharply,

recovering as the load is reduced to the machine rating.

(2) STANDARD CHASSIS POWER SUPPLY. - The regulated 200 vac supply is distributed to each of he chassis as shown in Drawing 87742, Volume 11, page 6. There it is converted into +450v, +200v, +8v, and 6.3 vac power supplies, as shown in Drawing 87203, Volume 11, page 1. The +450v supply is produced from the 200 vac supply through a step-up, delta-wye transformer and a full-wave rectifier circuit. The +200v supply is produced from the 200 vac supply through a delta-wye transformer and a full-wave rectifier circuit. The +450v and +200v power supplies are used in producing the Read and Transfer Pulse circuits.

The +8v supply is produced from the 200 vac supply through step-down, delta-star transformer and a full-wave rectifier circuit. This supply is furnished to bus bars which distribute the +8v to the circuit cards. The +8v from Chassis 10100 is also used on Console manual switches as shown in Drawing 121279. The 6.3 vac four-ampere supply is produced from the 200 vac source through a step-down, delta-wye filament transformer and is distributed to each of the eight vacuum tubes.

(3) CLOCK CHASSIS POWER SUPPLY. - The clock chassis uses the same power supplies as the main chassis as described in the preceding section. However, it also uses a 6.3 vac, 10-ampere power supply which is produced from the regulated 200 vac supply through a step-down, delta-delta filament transformer and furnished to bus bars located on the chassis. This circuit is shown in Drawing 87740, Volume 11, page 2.

(4) CENTRAL POWER SUPPLY. - The regulated 200 vac power supply is converted into +150v, +60v, +8v, -14v, -25v, -100v, -125v, -165v, 6.3 vac, and various bias voltages as shown in Drawing 121290, Volume 11, pages 3 and 4.

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These voltages are distributed to each chassis that is associated with memory. The +150v +60, -100v, -125v, and -165v supplies are produced from the 200 vac supply through step-down, delta-wye transformers and full-wave rectifier circuits. The Read, Write and Inhibit bias voltages are taken from the -125v source and controlled by Helipots R01, R02, and R03, Drawing 87742, mounted on the circuit breaker panel in the main cabine.

The +8v, -14v and -25v supplies are produced from the 200 vac supply through step-down, delta-star transformers and full-wave rectifier circuits. The Sense Amplifier bias voltage is taken from the +8v supply and is controlled by Helipot R04 mounted on the main cabinet.

The 6.3 vac supply is produced from the regulated 200 vac supply through a step-down, delta-wye filament transformer. This supply is distributed to bus bars.

(5) CARD VOLTAGE SUPPLIES. - Some electronic circuits in Bogart require voltages other than those produced by transformer-rectifier circuits. These circuits have low power and stability requirements, so that voltages obtained from resistors used as voltage dividers are sufficient.

Stability to high-frequency load variation is provided by a small condenser in parallel with the load. All voltage divider type supplies are located on the printed-circuit cards which they serve.

Each standard magnetic switch card has a voltage divider which produces +2 volts from the +8 volt supply. The +2 volts power is also produced on the Manual Set and Indicator Light (M.L.) cards.

All transistor switch cards and resynchronization delay cards 4009 and 4010 hold dividers which produce -3 volts from the -15 volt supply.

Type 4012 line drivers, and 9118 and 9122 pulse stretchers, contain divider-type supplies which produce +5 volts from the +8 volt supply.

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Card type 4005 contains a +100 volt divider supply and no other circuitry. The +100 volts is produced from the +200 volt supply.

(6) 115V AC DISTRIBUTION. - The unregulated 115 vac, single-phase, 60 cps power supply is taken directly from house wiring and used to operate various pieces of equipment.

The 115 vac supply is distributed to four service outlets, the memory warming coils, and four 1/8 HP blower motors in the main cabinet, as shown in Drawing 87742, Volume 11, page 6. This supply is also sent to the Running Time Meter in the console cabinet as shown in Drawing 87745, Volume 11, page 11, and to the external equipment.

The 115 vac supply is used in the typewriter cabinet to run the electric typewriter motor, as shown in Drawing 121299, Volume 12, page 23. The 115 vac supply is dissributed in the paper-tape cabinet to the photoelectric reader motor, the high-speed reader motor, the high-speed punch motor, the two fan motors, and the high-speed light.

c. PROTECTIVE MECHANISMS

(1) OVERLOAD PROTECTION. - Fuses and a-c circuit breakers are used in the Bogart computer to prevent the flow of excessive currents which might damage components. An a-c circuit breaker opens the circuit in the presence of excessive current, and is reset by simply setting the handle back to the ON position. It can be used optionally as a switch. Indicators in the form of small colored lights are used to signify various conditions throughout the computer.

(a) PRIMARY SOURCE. - Primary overload protection is provided by a 50-ampere House Protection Circuit Breaker (Drawing 87741, Volume 11, page 5) in the output lines of the 200 vac, 400 cps alternator which protects

the motor-generator system as well as the computer.

(b) MAIN CABINET. - AC circuit breakers are pyramided within the main cabinet so that each individual chassis is protected from damage, and the overall current is limited to a safe value. This protection system is shown in Drawing 87742, Volume 11, page 6.

The 200 vac, 400 cps power is run directly into the main cabinet, where it is divided to go to the external equipment and to the circuits of the main cabinet. When power is supplied to the main cabinet, the two red Power On lights on the front of the cabinet are lit. A 25-ampere circuit breaker (CB20) is included in the lines of the interior of the main cabinet, so that if the total current to the main cabinet components exceeds 25 amperes, the power is removed from these circuits. An identical circuit breaker (CB22) protects the external equipment from overall current exceeding 25 amperes.

Each chassis (10100-11900) within the main cabinet is protected by its individual 1.5-ampere circuit breaker (CB01-19). When any one of these chassis circuit breakers is open, the Tripped Breaker indicator light, located above the line voltmeter on the distribution panel, is illuminated.

In addition to the 200 vac, 400 cps power, the main cabinet is wired for 115 vac, 60 cps power. This is sent to the motors, etc., in the external equipment, and is used by the blower motors within the main cabinet. Each branch of this circuit contains a 25-ampere circuit breaker mounted on the distribution panel: CB21 for the main cabinet, CB23 for the external equipment.

(2) EMERGENCY SWITCHES AND INTERLOCKS) - In addition to fuses and circuit breakers which protect the electrical components in the system, the following means are provided to insure the safety of personnel and are shown in Drawing 87742:

(a) EMERGENCY OFF SWITCHES. - Four of these switches, located

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on the circuit breaker panel directly behind each of the cabinet doors, can be used to remove 400-cycle power from the entire system by interrupting the holding-coil circuit to the motor generator set. These red pushbuttons are evenly spaced along the panel so as to be readily accessible to persons working in or near the main cabinet.

NOTE

THESE EMERGENCY BUTTONS DO NOT REMOVE
115 VAC, 60 CPS POWER FROM ANY UNITS
IN THE SYSTEM)

(b) TEMPERATURE INTERLOCKS

1. LOW-TEMPERATURE THERMOSTATS. - Evenly spaced along the back of the circuit breaker panel are eight low-temperature thermostats. When the temperature of the air surrounding one or more of these devices exceeds 95°F., the thermostat trips and a relay puller in the console is energized, causing the Temperature Fault indicator (FLT) on the display panel to register a "1" instead of a normal "0". At the same time, one or more of the eight amber indicators on the front of the panel are illuminated, indicating which thermostat has been affected by the excessive temperature. The fault stops the computer as explained previously. When the air around the low-temperature thermostat falls below 94°F., the device automatically is reset, and the amber light is extinguished.

2. HIGH-TEMPERATURE THERMOSTATS. - The brackets which support the third and the seventh low-temperature thermostats also carry the high-temperature thermostats. When the temperature in the cabinet exceeds 120°F., either of these two devices will open the holding-coil circuit to the motor generator, thereby removing 400 cycle power from the entire system. These interlocks do not affect the 115 vac, 60 cps distribution to the computer or its auxiliary equipment.

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d. COOLING SYSTEM

(1) DESCRIPTION. - The cooling system requires 46°F. to 50°F. cooling water and a room temperature at approximately 80°F. maximum at 60 percent relative humidity or lower.

The cooling system of the main computer cabinet consists of a water cooling coil and four blowers which circulate the air in a closed type system. The water-cooled air streams enter the chassis side of the cabinet through adjustable overlapping grills located at the bottom of each bay and recirculate through the cooling coil.

Special grilled tops and bottoms are provided for the cabinets in case the contractor has air cooling plenums available on which to mount the electronic cabinets.

The other cabinets of the computer system are individually air cooled by blowers which circulate the room air.

The portion of the main computer cabinet in back of the chassis houses air filters, one water coil, four blowers, water flow controls, and a condensate drainage system. The air filters, which prevent dust from enetering the equipment, are oil-coated aluminum anodized filters of the type that can be cleaned and re-used. Four blowers, with a capacity of about 1,800 cfm., are driven by four 1/8 HP motors. One six-row, five-foot, counter-flow water coil is located between the filters and blowers. The rate of water flow through the coils is determined by the temperature of the air as it enters the cooling coils. The temperature is detected by a thermostat which, in turn, controls a modulating valve in the input water line. If the water content of the room air is relatively high, and the cabinet doors are opened, the moisture is removed by condensation on the cooling coils as the air temperature is dropped below the dew point. The condensate is collected and carried away by a floor drain. In the

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closed system an equilibrium is soon reached and if the doors remain closed very little condensate will be formed.

(2) AIR CONDITIONING DATA. - Requirements and data for the air conditioning system are as follows:

Cooling water temperature (Input)	50°F. max.
Cooling water pressure (Input)	60 psig min. 100 psig max.
Pressure drop through cooling system	40 psig max.
Rise in temp. of cooling water during heat exchange	9°F.
Air temperature in computer	64°F. to 80°F.
Maximum allowable relative humidity	60%
Blower capacity	1,800 cmf

It is to be noted that the temperature in the main computer cabinet must be kept under 95°F. since low-temperature interlocks are provided to prevent operations at higher temperatures.

If the temperature should exceed 120°F. the high-temperature interlock will cut off the power supply.

The customer must supply the cold water, insulated cold water pipes, and condensate drain pipes. It is recommended that the condensate drain be at least a 3/4 inch pipe. This is a gravity system with the condensate collecting pan located about 6 1/4 inches above the floor. Although the cold water connections to the computer are 1 1/4 inch NPT (male), the cold water pipes running to and from the computer and cold water pump should be of such a size as to provide a pressure drop of 40 psig through the computer cooling coils to allow control with the modulating valve. Pressures greater than 100 psig should be avoided.

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