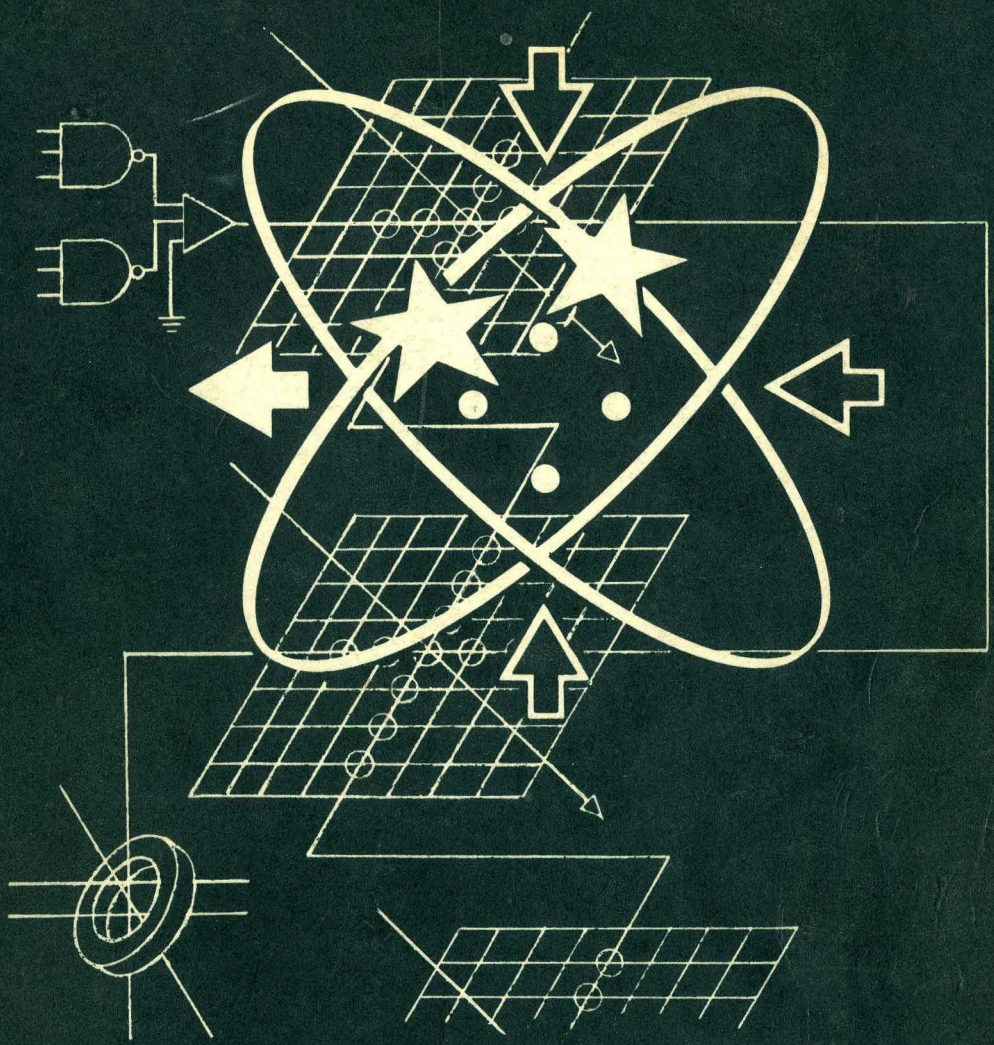
DATA SYSTEMS TECH 3&2 VOL. 1 RTM & NRCC

NAVEDTRA 10201-B1



DATA SYSTEMS TECHNICIAN 3&2 VOL. 1

NAVAL EDUCATION AND TRAINING COMMAND

RATE TRAINING MANUAL AND NONRESIDENT CAREER COURSE

NAVEDTRA 10201-B1

PREFACE

This Rate Training Manual and Nonresident Career Course (RTM/NRCC), *Data Systems Technician 3 & 2,* NAVEDTRA 10201-B1 (of which this is volume 1 of two volumes), is intended to serve as an aid for personnel who are seeking to acquire the theoretical knowledge and operational skills required of candidates for advancement to the rate of Data Systems Technician Third and Second Class.

This volume contains information on security, general maintenance, test equipment, the NTDS Unit Computer (CP-642-B/USQ-20(V)), and NTDS Peripheral Equipment. Volume 2, NAVEDTRA 10201-C, is classified CONFIDENTIAL and contains information on NTDS Display (AN/UYA-4), NTDS Transmission Equipment, NTDS Interface and Conversion Equipment, NTDS System Operation and Testing, Basic Data Processing Systems, and the NTDS Model IV Conversion.

This training manual and nonresident career course was prepared by the Naval Education and Training Program Development Center, Pensacola, Florida, for the Naval Education and Training Command. Special credit is given to the following commands for their reviews during the preparation of the manual: Fleet Combat Direction System Training Center, Pacific; Fleet Combat Direction System Training Center, Atlantic; Naval Sea System Command, Washington, D.C.; Combat Systems Technical Schools Command, Mare Island; U.S.S. America (CV-66); U.S.S. Ranger (CVA-61); and U.S.S. Dalhgren (DDG-43).

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THE UNITED STATES NAVY

GUARDIAN OF OUR COUNTRY

The United States Navy is responsible for maintaining control of the sea and is a ready force on watch at home and overseas, capable of strong action to preserve the peace or of instant offensive action to win in war.

It is upon the maintenance of this control that our country's glorious future depends; the United States Navy exists to make it so.

WE SERVE WITH HONOR

Tradition, valor, and victory are the Navy's heritage from the past. To these may be added dedication, discipline, and vigilance as the watchwords of the present and the future.

At home or on distant stations we serve with pride, confident in the respect of our country, our shipmates, and our families.

Our responsibilities sober us; our adversities strengthen us.

Service to God and Country is our special privilege. We serve with honor.

THE FUTURE OF THE NAVY

The Navy will always employ new weapons, new techniques, and greater power to protect and defend the United States on the sea, under the sea, and in the air.

Now and in the future, control of the sea gives the United States her greatest advantage for the maintenance of peace and for victory in war.

Mobility, surprise, dispersal, and offensive power are the keynotes of the new Navy. The roots of the Navy lie in a strong belief in the future, in continued dedication to our tasks, and in reflection on our heritage from the past.

Never have our opportunities and our responsibilities been greater.

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CREDITS

Preparation of this manual was aided by the cooperation and courtesy of McGraw-Hill, Inc. This company furnished the Glossary of Terms appearing in Appendix I.

CHAPTER 1

ADVANCEMENT AND SECURITY

This training manual has been prepared for military personnel of the regular Navy and the Naval Reserve. It is intended as an aid to advancement in rating, and as a source of information on the various aspects of the Data Systems Technician (DS) rating. The professional standards used in the preparation of this manual are contained in NAVPERS 18068 (series), *Manual of Navy Enlisted Manpower and Personnel Classifications and Occupational Standards.* It is recommended that the Data Systems Technician Section of Occupational Field 12, Data Systems, NAVPERS 18068, be studied for an understanding of the various skills and knowledge required of a technician in the DS rating.

This manual systematically covers several digital systems maintained by the DS rating. The Data Systems Technician is normally assigned to the role of performing intermediate level maintenance within his assigned system. In this way he supports the activities of the operator ratings working with the same equipment, notably the Data Processing Technicians (DPs), Operations Specialists (OSs), Intelligence Specialists (ISs), and Radiomen (RMs). In some cases, the DS may also be assigned to operator duties and even assist programmers or perform programing duties as part of his job.

This manual is too limited to deal with all aspects of the DS rating. Of the many data processing systems in use by the Navy, only a comparatively few can be presented in sufficient detail to be instructive. The Data Systems Technician is responsible for more than the individual equipment that make up his system. He is responsible for the various equipment interfaces that exist when these different units of equipment are combined into a single system. It is essential that the DS become aware of these system concepts and learn to identify the individual equipment that may be responsible for abnormal system performance.

Naturally, system concepts vary from one system to another. Most details of system operation come only from long experience with an individual system. Yet this is still a key area that has to be touched on in some detail. As a result, this manual will cover systems, the equipment in several systems, and the interface (system concepts) that should be apparent in most of the installations of those systems. In order to thoroughly understand this material, the DS must already be familiar with the contents of the *Navy Electricity Electronics Training Series (NEETS),* NAVEDTRA 10087 (series) *Basic Electronics, Volumes I and II,* and NAVEDTRA 10088 (series) *Digital Computer Basics.* Refer to NAVEDTRA 10052 (series) *Bibliography for Advancement Examination Study* for the applicable *NEETS* modules and Basic Electronics chapters for paygrades E-4 and E-5.

SECURITY

Security is a general term that covers such things as barring unauthorized personnel from access to restricted areas, preventing information of a classified or restricted nature from finding its way into unfriendly hands, and being able to account for the storage, movement, and receipt of material of a classified or restricted nature. Most individuals in the technical ratings, such as Data Systems Technicians, are conscious of security in terms of classified written data that must be maintained under lock and key when not in use. All classified material will fall into one of three groups: Confidential, Secret, or Top Secret. Equipment, or portions of equipment, or applications of equipment may

also be classified as Confidential or higher, though, in general, most of the equipment covered by the DS is considered unclassified.

A rule of thumb is that the equipment itself and the existence of programs for certain applications are generally unclassified unless noted otherwise. The exact nature of operational programs, their past, current, and future use in terms of scheduling or situation response, and the contents of the data base (retained data) and the data inputs and outputs are all generally regarded as classified unless noted otherwise. The Data Systems Technician can talk about what he does as part of his job, but he cannot talk about what his system does when it is doing its job, unless the system application is unclassified, or the listeners are cleared for and have a need for that information.

Handling of Classified Material

All classified documents must be handled according to the highest classification of their contents. Frequently, documents will be composed of paragraphs of different classifications. A preceding letter in parentheses indicates the highest level of classification for the contents of that paragraph, i.e., (U) for unclassified, (C) for Confidential, (S) for Secret, and (T) for Top Secret. Classified documents also require a stamp at the top and bottom of each page showing the highest classification for the contents of that page. The entire document must be stamped on both the front and back covers, (top and bottom) with the highest classification in the contents. A lower classified portion that is removed from a text containing information of a higher classification can be restamped to the lower classification. Figures and tables have a preceding ( ) containing a classification marking to indicate the classification of the contents, and a trailing ( ) containing a classification marking to indicate the title classification.

Burning and powdering of the ashes, or mulching are accepted ways of disposing of Confidential material. This material is not singled out in this text. A determination of which material does not require Confidential handling can usually be made by referring back to the appropriate technical manual, or by consulting with the division officer or security officer. The rule-of-thumb given previously generally applies.

Other Types of Security

Security should also have another meaning to the DS. As a maintenance technician, he has access to equipment valued at many thousands of dollars. His system may be valued at upward to several million dollars. It is his responsibility to provide a reasonable amount of assurance that his equipment is not tampered with by unqualified personnel. He should safeguard his spaces and only allow visitors who are escorted, and then only when the nature of the visit is clearly understood.

The DS also has the responsibility of safeguarding his tools and test equipment. These items were assigned to his care and responsibility, and the frequent loss, theft, misplacement, and abuse of tools clearly suggests that too many technicians are not doing their part in safeguarding and preserving tools for future use. In an effort to improve the safeguarding of tools and test equipment, a system of accountability should be instituted where the responsible individual is is clearly identified. Tools that are borrowed or loaned should be signed for, and signed for again on their return. In this manner it is always possible to trace the movement of missing tools and test equipment, and, hopefully, to secure their return. When not in use, tools and test equipment should be locked up.

SYSTEM COVERAGE

Over half of the DSs in the Navy are assigned to NECs (Navy Enlisted Classifications) associated with the NTDS (Naval Tactical Data System). Not all of these DSs are actually working with the NTDS, but they are at least familiar with some of the equipment used in NTDS. This is the largest single grouping by systems that exists for the DS rating at present. To cover system concepts, it is necessary to cover a system, and NTDS is the logical choice for that system. There are several other reasons for selecting NTDS as a representative system, and these include: (1) NTDS is a system of considerable importance in the Navy, (2) NTDS is a large system in which many individual equipment units and system concepts can be covered, (3) NTDS is a real-time system, one of two primary system distinctions covered in this text, and (4) NTDS is a valid concept, so much so that the equipment in the system installations are being refurbished for an anticipated additional lifetime of ten years or more.

It is realized that individuals working with the equipment and systems covered in this text have an additional advantage over individuals who do not. This is unfortunate, yet unavoidable. The only way this situation could be avoided entirely would be to develop and work with a hypothetical system. Even if this approach could be used, some individuals would protest that it is pointless to cover a system in detail that they would never see, never work on, because it simply does not exist.

In itself, NTDS does not represent the whole world of data processing. Chapter 5 of Vol. 2 will deal with other equipment and systems of the Navy that receive DS support. The coverage in this area is not as extensive as that given to NTDS. One reason is that many of the concepts covered in the earlier chapters are still valid, and do not require repeating. Another reason is that some details have been sacrificed in order to permit a broader field coverage. Some systems could not be covered at this time because the information was not available within the time span required for preparing this manual. Other systems were not covered because the percentage of DSs providing support was considered too low, or the system appeared on the verge of a major change with no concrete details of what the final status would be.

CHAPTER CONTENTS

A brief summary of the contents and an explanation of why that material is included is presented for each chapter.

VOLUME 1

CHAPTER 2.–This is the maintenance chapter. There are certain things that become generalized (troubleshooting, repair, etc.) which can then be considered apart from their source. An effort is made to collect a representative group of these generalities, which can then be used to further analyze the maintenance role of the Data System Technician. Troubleshooting, for instance, is usually either tracing malfunction symptoms back to their probable causes, or attempting to change those symptoms by physical changes in the circuitry. Repair involves the development of a number of skills, and the use of these skills vary from one repair job to another. The factors that govern these decisions are discussed in chapter 2.

CHAPTER 3.–This is the test equipment chapter. A number of test equipment types have been firmly adopted into the DS field, and this chapter deals with these. A number of newer equipment types have also made their appearance in the civilian world, but have not been accepted into the Navy community at this time. While these may be mentioned at different points in this text in terms of their capabilities, they are not included as a part of this chapter, since their use at present is confined to the civilian world.

CHAPTER 4.–The heart of every computerized system is the computer, processor, central processor, or whatever it may be called. The NTDS, which has been selected as the vehicle by which system concepts will be taught in this text, is built up around one of a number of computers. These include the CP-642A, the CP-642B, and the newest computer, the UYK-7(V). This text concentrates on the CP-642B computer rather than dealing with the

redundant features of the several computer types. Nearly all computer types are broken down into five main functional groups as covered in NAVEDTRA 10088 (series) ***Digital Computer Basics.*** **The CP-642B computer is being covered in addition to the CP-789 computer that is covered in NAVEDTRA 10088 (series), because, first, the CP-642B has many times the processing capabilities of the CP-789, and second, the CP-642B computer is also the central computer of several other systems covered in the final chapters of this manual.**

CHAPTER 5.—Peripheral ("side") equipment is that equipment used to extend the basic capabilities of the computer. Peripheral equipment includes a wide range of equipment types, such as keyboards, displays, paper tape readers and punches, magnetic storage devices, optical readers, printers, and many others. In this text, for NTDS, a restricted definition of peripheral and input/output (I/O) devices is introduced, because the peripheral equipment provided for NTDS does not include equipment covered in chapters 1 through 3 of Vol. 2.

VOLUME 2

CHAPTER 1.—The display equipment covered in this chapter includes the most common equipment found in the NTDS system, but each NTDS installation is tailored to meet the needs and capabilities of the ship that it is situated aboard. As a result, the presence and quantities of each type of display device on each installation are beyond the scope of this manual. In some cases, older or more recent versions of display devices will appear in various installations in place of the equipment covered here.

CHAPTER 2.—NTDS transmission equipment is an area of equipment coverage that in many cases is being handled more by ETs (electronic technicians) than by DSs. However, DSs continue to have responsibilities in this area, and the concept of several systems linked together by the transfer from one system to another is an important system concept in the NTDS world. Therefore, one chapter of this manual is devoted to transmission equipment and transmission principles.

CHAPTER 3.—NTDS is not a "stand alone" system, but has numerous tie-ins with surveillance and weapon systems aboard each craft. The interconnection of equipment built to different standards is often accomplished by interface equipment designed for that purpose. The conversion of data from one form to another is often involved, so this chapter is referred to as NTDS Interface/Conversion Equipment.

CHAPTER 4.—Programs written for digital systems generally fall into one of two categories. Operational programs are intended to make the computerized system perform some task, other than self-maintenance. Maintenance programs direct system operations inward to checking and analyzing equipment performance against predetermined standards. These programs include methods of communicating the results to operator and maintenance personnel, so that problem areas can be traced quickly and corrected. This chapter discusses some of the program conventions used in NTDS.

CHAPTER 5.—NTDS is a real-time system, a term that will be explained in more detail later. Basically it means that the system is designed to provide responses to a situation that is in the process of occurring. In this chapter, the equipment required of a nonreal-time system will be discussed. A nonreal-time system acts on accumulated data, some of which may be taken from a real-time situation, but its responses are more in terms of analyzing, organizing, and simplifying the structure of the accumulated data for increased human comprehension. The features of a nonreal-time system vs. a real-time system are discussed in more detail in both chapters 5 and 6.

CHAPTER 6.—This chapter covers the NTDS MODEL IV conversion. Only a few of the major changes are mentioned. All functions of the NTDS are now incorporated in core memory and can be activated simply by placing the consoles in the desired mode. The identification (ID) portion of MODEL IV has many more capabilities than MODEL III.

Comments on the scope of this text and the material covered can be sent directly to the writers by using the mailing address provided with the correspondence course (NRCC). These comments are read and retained on file. If they include suggestions on areas of the rating that need better coverage, they should also mention document sources for necessary details. If this is done, future errata sheets and revisions will be able to incorporate these suggestions into an improved manual.

ADVANCEMENT

As the DS advances from one paygrade to another, his responsibilities change. Third class petty officers are considered to be equipment-oriented in their understanding. By the time they have advanced to second class petty officer, they are expected to have absorbed enough system concepts to be true system technicians. Advancement will also bring on certain military responsibilities, such as providing leadership, making essential decisions, planning ahead for contingencies, and coping with personnel problems instead of just equipment problems. As further advancement follows, many technicians find that the areas of management and administration become their full-time jobs, and equipment maintenance is performed by junior technicians. Senior technicians are still able to provide training, advice, and technical assistance when it is required, but the junior technician will find that once he has proven his ability, he will have a great deal of independence and responsibility in his daily work.

Good leadership results in team effort. Team effort is the key to good maintenance; so it is essential that leadership qualities be developed along with technical competence. Most technicians find that working together in pairs produces excellent results. Different ideas can be exchanged and improved. One technician can be working at the equipment itself while the other follows his progress in the technical manuals and offers advice. Several of the more difficult processes are simplified by having two pair of eyes to observe and two pair of hands to assist. Then once the problem is corrected, which usually involves gaining a greater insight into the equipment behavior, the technicians involved should share their new understanding with others. A discussion of the entire problem and the various steps taken in finding a solution would act to improve the general background each technician needs to be efficient in.

Leadership is not just the ability to lead others, but also to accept the leadership of others and to contribute to the total effort. Good leadership can be found where the individuals accept their roles as part of a team and work together to the same ends.

ENLISTED RATING STRUCTURE

The two main types of ratings in the present enlisted rating structure are general ratings and service ratings.

GENERAL RATINGS identify broad occupational fields of related duties and functions. Some general ratings include service ratings; others do not. Both Regular Navy and Naval Reserve personnel may hold general ratings.

SERVICE RATINGS identify subdivisions or specialties within a general rating. Although service ratings can exist at any petty officer level, they are most common at the PO3 and PO2 levels. Both Regular Navy and Naval Reserve personnel may hold service ratings.

THE NAVY ENLISTED ADVANCEMENT SYSTEM

Many of the rewards of Navy life are earned through the advancement system. The basic ideas behind the system have remained stable for many years, but specific portions may change rather rapidly. It is important to understand the system and follow changes carefully. **NAVMILPERSCOM Notices 1418 will normally record any changes that occur.**

The normal system of advancement may be easier to understand if it is broken down into two parts:

1. Those requirements that must be met before an individual may be considered for advancement.
2. Those factors that actually determine whether or not that individual will be advanced.

Qualifying for Advancement

In general, to QUALIFY (be considered) for advancement, the individual must first:

1. Have a certain amount of time in pay grade.
2. Demonstrate an adequate knowledge of the material in any mandatory rate training manuals. This may be determined by successfully completing the appropriate NRCCs or, in some cases, by successfully completing an appropriate Navy school.
3. Demonstrate the ability to perform all the task requirements for advancement by completing the Personnel Advancement Requirement (PAR) Program, NAVPERS 1414/4.
4. Be recommended for advancement by the commanding officer.
5. Petty officer third and second candidates must also demonstrate knowledge of military subjects by passing a locally administered MILITARY/LEADERSHIP examination based on the naval standards for advancement (from NAVPERS 18068 series).
6. Demonstrate knowledge of the technical aspects of the rate by passing a Navywide advancement examination based on the occupational standards applicable to the DS rate (from NAVPERS 18068 series, those standards listed at and below the sought-for rate level).

Figure 1-1 gives a detailed view of the requirements for advancement of active duty personnel; figure 1-2 gives this information for inactive duty personnel. Remember that the occupational standards are subject to frequent change. Check with the division officer or training officer to be sure that the most recent standards are used.

If an individual can meet all of the above requirements satisfactorily, he becomes a member of the group from which advancements in rate will be made.

Who Will Be Advanced?

Advancement is not automatic. Meeting all of the requirements makes an individual eligible, but does not guarantee his advancement. Some of the factors that determine which persons, out of all those QUALIFIED, will actually be advanced in rate are the score made on the advancement examination, the length of time in service, the performance marks earned, and the number of vacancies being filled in a given rate.

If the number of vacancies in a given rate exceed the number of qualified personnel, then ALL of those qualified will be advanced. More often the number of qualified people exceeds the vacancies. When this happens, the Navy has devised a procedure for advancing those who are BEST qualified. This procedure is based on combining three personnel evaluation systems:

Merit rating system (annual evaluation and CO recommendation)

Personnel testing system (advancement examination score—with some credit for passing previous advancement exams)

Longevity (seniority) system (time in rate)

Simply, credit is given for how much the individual has achieved in the three areas of performance, knowledge, and seniority. A composite, known as the final multiple score, is generated from these three factors. All of the qualified candidates from a given advancement examination population are then placed on one list, based on this composite figure, the highest achiever first, and so on down to the last qualified person in the population. For candidates for E4, E5, and E6, advancement authorizations are then issued, beginning at the top of the list, for the number of persons needed to fill the existing vacancies. Candidates for E7 whose final multiple scores are high enough will be designated PASS SELBD ELIG (Pass Selection Board Eligible). This means that their names will be placed before the Chief Petty Officer Selection Board, a NMPC board charged with considering all so-designated eligible candidates for advancement to CPO. Advancement authorizations for those being advanced to CPO are issued by this board.

Who, then, are the individuals who are advanced? Basically, they are the ones who achieved the most in preparing for advancement.

Requirements	E-1 to E-2	E-2 to E-3	E-3 to E-4	E-4 to E-5	E-5 to E-6	E-6 to E-7	E-7 to E-8	E-8 to E-9
Time in Rate	6 mos.	6 mos. as E-2	9 mos. as E-3	12 mos. as E-4	36 mos. as E-5	36 mos. as E-6	36 mos. as E-7	36 mos. as E-8
School	RTC (CO may advance up to 10% of company)	none	Class "A" for AME, BU, CE, CM, CTA, CTI, CTM, CTO, CTR, CTT, DT, EA, EO, EW, FTB, GSE, GSM, HM, IS, JO, MN, MT, MU, PR, RP, SW, UT	Naval Justice School for LN2	none	Navy School for AGC, MUC	Navy School for MUCS	none
PAR NAVPERS 1414/4	none	none	PAR (Personnel Advancement Requirement) must be completed for advancement to E-4 through E-7				none	none
Performance Test	none	none	Specified ratings must complete applicable performance tests before taking Navywide advancement examination				none	none
Nonresident Career Course and RTM	none	Required for E-3 and all petty officer advancements unless waived because of completion of Navy school. Courses need not be completed but once; i.e., those who complete the 3 & 2 course for PO3 need not complete same course again for advancement to PO2.				Nonresident Career Courses and recommended reading. See NAVEDTRA 10052 (series)		
Military/ Leadership Examination	none	none	Must be passed before advancement exams for E-4 and E-5 candidates		none	none	none	none
Examinations	Locally prepared tests	NETPDC exams or locally prepared test	Navywide advancement examinations required for advancement to E-4 through E-7				none	none
Selection Board	none	none	none	none	none	Navywide CPO or SCPO/MCPO Selection Board		
Obligated Service Required	There is no set amount of obligated service required either to take the Navywide advancement examination or to accept advancement to paygrades E-1 through E-6					All CPO candidates must have two years remaining obligated service to accept appointment to a CPO paygrade		
Enlisted Performance Evaluation	As used by CO when approving advancements		Counts toward performance factor credit in advancement final multiple for all E-4 through E-9 candidates					
CO recommendation	All Navy advancements require the commanding officer's recommendation for advancement							
Authorization for advancement	Commanding Officer		Naval Education and Training Program Development Center authorization required for advancement to E-4 through E-9 in addition to command approval					

Figure 1-1.—Active duty advancement requirements.

REQUIREMENTS*	E1 to E2	E2 to E3	E3 to E4	E4 to E5	E5 to E6	E6 to E7	E7 to E8	E8 to E9
TOTAL TIME IN GRADE	6 mos.	6 mos.	9 mos.	12 mos.	36 mos.	36 mos.	36 mos.	36 mos.
TOTAL TRAINING DUTY IN GRADE†	14 days	14 days	14 days	14 days	42 days	42 days	42 days	42 days
PERFORMANCE TESTS			Specified ratings must complete applicable performance tests before taking examination.					
DRILL PARTICIPATION	Satisfactory participation as a member of a drill unit in accordance with NAVMILPERSCOMINST 5400.42 series.							
PERSONNEL ADVANCEMENT REQUIREMENT (PAR) NAVPERS 1414/4			Personnel Advancement Requirements (PAR) NAVPERS 1414/4 must be completed for advancement to E4 through E7					
RATE TRAINING MANUAL (INCLUDING MILITARY REQUIREMENTS)	Completion of applicable course or courses must be entered in service record.							
EXAMINATIONS**	Locally prepared tests.	See below	Navywide examinations required for all E4 through E7 advancements. Military leadership exam required for E4 and E5.					
SELECTION BOARD						Navywide CPO or SCPO/MCPO Selection Board		
AUTHORIZATION	Commanding Officer		NAVEDTRAPRODEVCEN					

*Recommendation by Commanding officer required for all advancements.
†Active duty periods may be substituted for training duty.
**For E3, NAVEDTRAPRODEVCEN exams or locally prepared tests may be used.

Figure 1-2.—Inactive duty advancement requirements.

They were not content to just qualify; they went the extra mile in their training, and through that training and their work experience they developed greater skills, learned more, and accepted more responsibility.

While it cannot guarantee that any one person will be advanced, the advancement system does guarantee that all persons within a particular rate will compete equally for the vacancies that exist.

How to Prepare for Advancement

What must a person do to prepare for advancement? Study the occupational standards, work on the task requirements, study the required rate training manuals, and study other material that is required for advancement in the DS rate. To prepare for advancement, the individual will need to be familiar with: (1) the *Manual of Navy Enlisted Manpower and Personnel Classifications and Occupational Standards*, (2) the Personnel Advancement Requirement (PAR) Program, (3) a publication called ***Bibliography for Advancement Examination Study,*** NAVEDTRA 10052 and (4) applicable rate training manuals. The following sections describe them and give some practical suggestions on how to use them in preparing for advancement.

OCCUPATION STANDARDS

The *Manual of Navy Enlisted Manpower and Personnel Classifications and Occupational Standards*, NAVPERS 18068 series, contains the rating occupational and naval standards for advancement to each pay grade in section I. Contained in section II are the Navy Enlisted Classification Codes. This manual replaces the "quals manual" and the NEC manual.

NAVAL STANDARDS are requirements that apply to all ratings rather than to any one particular rating. Naval requirements for advancement to third class and second class petty officer rates deal with military conduct, naval organization, military justice, security, watch standing, and other subjects which are required of petty officers in all ratings.

OCCUPATIONAL STANDARDS are requirements that are directly related to the work of each rating.

Both the naval requirements and the occupational standards are divided into subject matter groups.

The candidate is required to pass a Navywide military/leadership examination for E-4 or E-5, as appropriate, before he takes the occupational examinations. The military/leadership examinations are administered on a schedule determined by the commanding officer. Candidates are required to pass the applicable military/leadership examination only once. Each of these examinations consists of 100 questions based on information contained in *Military Requirements for Petty Officers 3 & 2*, NAVEDTRA 10056 (series), and in other publications listed in ***Bibliography for Advancement Examination Study,*** NAVEDTRA 10052 (series).

The Navywide occupational examinations for pay grades E-4 and E-5 contain 150 questions related to occupational areas of the DS rating.

If the candidate is working for advancement to second class, he should also remember that he may be examined on third class standards as well as on second class standards.

NAVPERS 18068 series is kept current by means of any necessary changes. The occupational standards for the DS rating, which are covered in this training manual, were current at the time the manual was printed. By the time this manual is studied, however, the standards for the DS rating may have been changed. Never trust any set of standards until it has been checked against an UP-TO-DATE copy in the NAVPERS 18068 series.

Personnel Advancement Requirement (PAR) Program NAVPERS 1414/4

The Personnel Advancement Requirement (PAR) Program is a new program initiated to replace the Record of Practical Factors (NAVEDTRA 1414/1).

The former "quals" were stated in terms of practical factors and knowledge factors. The

new occupational standards, are presented only as task statements. This new format of the occupational standards does not lend itself to the practical factor checkoff list concept of the Record of Practical Factors. As a result, a new form and new concept of determining eligibility for advancement has been developed. The Personnel Advancement Requirement (PAR) (NAVPERS 1414/4) will replace the Record of Practical Factors. This new system allows a command to evaluate the overall abilities of an individual in a day-to-day work situation and eliminates the need to complete a mandatory, lengthy, and detailed checkoff list.

The E-8 and E-9 are exempted from the program as there are other means of selection for advancement to these paygrades. The E-3 apprenticeships are so broad as to make the development of a single PAR impractical.

Each rating PAR lists the requirements for advancement to paygrades E-4 through E-7 in one pamphlet. It contains descriptive information, instructions for administration, special rating requirements, and advancement requirements in the following sections:

Section I – Administration Requirements

Section II – Formal School and Training Requirements

Section III – Occupational and Military Ability Requirements

Section I contains the individuals length of service, time in rate, and a checkoff for the individual having passed the E-4/E-5 Military Leadership Examination.

Section II contains a checkoff entry for the individual having completed the Military Requirements Navy Training Course and the applicable Navy Training Course for the rating.

Section III is a checkoff list of task statements. Items in this section are to be interpreted broadly and do not demand actual demonstration of the item, or completion of alternate local examination, although demonstration is a command prerogative. Individuals are evaluated on their ability to perform the task whether it be by observation of ability in related areas, training received or, if desired, by demonstration.

PAR forms are stocked in the Navy Supply System, and listed in **NAVSUP** publication 2002.

Until completed, the NAVPERS 1414/4 is usually held by the division officer. After completion, it is forwarded to the personnel office for insertion in the individual's service record. If personnel are transferred before qualifying in all task requirements, the incomplete form should be forwarded with their service record to their next duty station. They can save themselves a lot of trouble by making sure that this form is actually inserted in their service record before being transferred. If the form is not in their service record, they may be required to start all over again and requalify in the task requirements which have already been checked off.

NAVEDTRA 10052

Bibliography for Advancement Examination Study, **NAVEDTRA 10052, is a very important** publication for any enlisted person preparing for advancement. This bibliography lists required and recommended rate training manuals and other reference material to be used by personnel working for advancement.

NAVEDTRA 10052 is revised and issued once each year by the Chief of Naval Education and Training. Each revised edition is identified by a letter following the NAVEDTRA number. When using this publication, be SURE it is the most recent edition.

If extensive changes in standards occur in any rating between the annual revisions of NAVEDTRA 10052, a supplementary list of study material may be issued in *TIPs (Training Information Procedures for E.S.O.'s).* When preparing for advancement, check to see whether changes have been made in the standards for the DS rating. If changes have been made, see if a *TIPs* has been issued to supplement NAVEDTRA 10052 for the DS rating.

The required and recommended references are listed by pay grade in NAVEDTRA 10052. If working for advancement to third class, study the material that is listed for third class. If working for advancement to second class, study the material that is listed for second class; but remember that the references listed in the third class level are still testable at the second class level.

In using NAVEDTRA 10052, notice that some rate training manuals are marked with an asterisk (*). Any manual marked in this way is MANDATORY—that is, it must be completed at the indicated rate level before an individual is eligible to take the Navywide examination for advancement. Each mandatory manual may be completed by (1) passing the appropriate nonresident career course that is based on the mandatory training manual; (2) passing locally prepared tests based on the information given in the training manual; or (3) in some cases, successfully completing an appropriate Navy school.

Do not overlook the section of NAVEDTRA 10052 which lists the required and recommended references relating to the naval standards for advancement. Personnel of ALL ratings must complete the mandatory military requirements training manual for the appropriate rate level before they can be eligible to advance.

The references in NAVEDTRA 10052 which are recommended but not mandatory should also be studied carefully. ALL references listed in NAVEDTRA 10052 may be used as source material for the written examinations, at the appropriate rate levels.

Rate Training Manuals

There are two general types of rate training manuals. RATING manuals (such as this one) are prepared for most enlisted ratings. A rating manual gives information that is directly related to the occupational standards of ONE rating. SUBJECT MATTER manuals or BASIC manuals give information that applies to more than one rating.

Rate training manuals are revised from time to time to keep them up-to-date technically. The revision of a rate training manual is identified by a letter following the NAVEDTRA number. A particular edition of a training manual can be identified by checking the NAVEDTRA number and the letter following this number in the most recent edition of *List of Training Manuals and* ***Correspondence Courses,*** **NAVEDTRA 10061 (series). (NAVEDTRA 10061 is actually a catalog that lists all current training manuals and courses. This catalog is useful when planning a study program.)**

Each time a rate training manual is revised, it is brought into conformance with the official publications and directives on which it is based; but during the life of any edition, discrepancies between the manual and the official sources are almost certain to arise because of changes to the latter which are issued in the interim. Always refer to the appropriate official publication or directive. If the official source is listed in NAVEDTRA 10052, the Naval Education and Training Program Development Center uses it as a source of questions in preparing the Fleetwide examinations for advancement. In case of discrepancy between any publications listed in NAVEDTRA 10052 for a given rate, the examination writers will use the most recent material.

Rate training manuals are designed to help individuals prepare for advancement. The following suggestions may help in making the best use of this manual and other Navy training publications when preparing for advancement:

1. Study the naval standards and the occupational standards for the DS rating before studying the training manual, and refer to the standards frequently while studying. Remember,

the manual is studied primarily in order to meet these standards.

2. Set up a regular study plan. It will probably be easier to stick to a schedule by studying at the same time each day. If possible, schedule all studies for a time of day when interruptions or distractions can be avoided.

3. Before beginning to study any part of the manual intensively, become familiar with the entire book. Read the preface and the table of contents. Check through the index. Thumb through the book without any particular plan, looking at the illustrations and reading bits here and there that appear interesting.

4. Look at the training manual in more detail, to see how it is organized. Look at the table of contents again. Then, chapter by chapter, read the introduction, the headings, and the subheadings. This will present a pretty clear picture of the scope and content of the book. While looking through the book in this way, ask some questions:

- What do I need to learn about this?
- What do I already know about this?
- How is this information related to information given in other chapters?
- How is this information related to the occupational standards?

5. Get a general idea of what is in the training manual and how it is organized, then fill in the details by intensive study. In each study period, try to cover a complete unit—it may be a chapter, a section of a chapter, or a subsection. The amount of material that can be covered at one time will vary. If the subject is well known, or if the material is easy, quite a lot can be covered at one time. Difficult or unfamiliar material will require more study time.

6. In studying any one unit—chapter, section, or subsection—write down the questions that occur during study. Many people find it helpful to make a written outline of the unit as they study, or at least to write down the most important ideas.

7. Relate the information in the training manual to knowledge already acquired. When reading about a process, a skill, or a situation, try to see how this information ties in with past experience.

8. When a unit is finished, take time out to see what has been learned. Look back over notes and questions. Maybe some of those questions have been answered. There still may be some that are not answered. Without looking at the training manual, write down the main ideas gotten from studying this unit. Don't just quote the book. If these ideas cannot be expressed in an individual's own words, the chances are he has not really mastered the information.

9. Use nonresident career courses whenever possible. The courses are based on rate training manuals or on other appropriate texts. As mentioned before, completion of a mandatory rate training manual can be accomplished by passing a nonresident career course based on the rate training manual. It may be helpful to take other courses, as well as those based on mandatory manuals. Taking a course helps a person master the information given in the training manual, and it also helps him see how much he has learned.

10. Think of the future while studying the rate training manuals. Work is being done for advancement to third class or second class right now, but some day the effort will be toward higher rates. Anything extra that can be learned now will help both now and later.

SOURCES OF INFORMATION

Besides training manuals, NAVEDTRA 10052 lists official publications which may be examined. Do not try studying just the sections required, but become as familiar as possible with all publications used.

One of the most useful things that can be learned about a subject is how to find out more about it. No single publication can provide all the information needed to perform the duties of the DS rating. Learn where to look for accurate, authoritative, up-to-date information on all subjects related to the naval requirements for

advancement and the occupational standards of the DS rating.

PUBLICATIONS YOU SHOULD KNOW

The detailed information you need for advancement and for everyday work is contained in sources mentioned throughout this text and in a bibliography in the rear section of this manual. Some are subject to change or revision from time to time, some at regular intervals, others as the need arises. When using any publication that is subject to change or revision, be sure to get the latest edition. When using any publication that is kept current by means of changes, be sure to get a copy in which all official changes have been made. Studying canceled or obsolete information will not help. Instead, it is likely to be a waste of time, and may even be seriously misleading.

TECHNICAL PUBLICATIONS

In addition to the publications mentioned here that would directly assist the candidate seeking advancement, the DSs are required to become familiar with a great many technical documents, including 3M manuals, COSALs, COSBALs, equipment technical manuals, **EIMBs, EIBs, SOMs (System Operations** Manuals), etc.

Equipment technical manuals, PODs, COSALs, and COSBALs are unique to each command. Because of this, DSs up for advancement will not be required to know them in detail in preparing for the advancement exam, except where material from these sources appears in this manual. EIMBs, EIBs, 3M documentation, and manuals or portions of manuals referenced by this text, or given in the bibliography for DSs are valid sources for material used in the preparation of the advancement exams.

TRAINING FILMS

Training films available to naval personnel are a valuable source of supplementary information on many technical subjects. Training films are listed in the *United States Navy Film Catalog* NAVAIR 10-1-777 (formerly NAVWEPS 10-1-777), published in 1969. Copies may be ordered in accordance with the Navy Stock List of Forms and Publications, NAVSUP 2002. Monthly supplements to the Film Catalog are distributed to catalog holders.

When selecting a film, note its date of issue listed in the Film Catalog. Procedures sometimes change rapidly. Thus, some films become obsolete rapidly. If a film is obsolete only in part, it may sometimes be shown effectively if before or during its showing trainees are shown which procedures have changed.

CHAPTER 2

MAINTENANCE

This chapter is a debarkation point for data systems. In effect, it is like the swimming coach who said, "All right; you were just told how easy it is to learn to swim. Now it is time to get your feet wet."

This chapter contains general maintenance information which may not always match up to a given situation. Data systems will be covered in terms of specific equipment and specific applications. It is realized that technicians who have been trained in the areas to be covered have an advantage, but there are enough areas covered that no one has a total advantage. The importance of stressing specifics is well-known. This text must commit itself to one system in order to reach a level where both specifics and generalities can be stressed. The logical choice is the Naval Tactical Data System (NTDS), with emphasis on the AN/UYA-4(V) display subsystem of NTDS, rather than the older equipment of the AN/SYA-1(V), AN/SYA-4(V), and AN/UYA-1(V) display subsystems.

The NTDS is the primary computerized system supported by the DS rate. It is the data system involving the most DS NECs, the system the Navy has the greatest commitment to, and the system with the greatest percentage of DSs assigned. It is also a system that provides a sufficient variety of equipment types so that a thorough exposure to the data systems field is possible. To round out the subject area, the text will depart from NTDS in the final chapters of Vol. 2 to provide a glimpse of the non-NTDS equipment and systems. The remainder of this chapter will deal with the additional skills and knowledge required by the technician. It will also mention source material that is available to the technician.

Many technicians carry a pocketsized note book into which they enter bits of information they may need later. It might be a good idea to begin one at this point if one has not already been started. However, do not attempt to copy information from sources where it can be easily located again. Useful types of information include people's AUTOVON numbers and commercial telephone numbers, equipment designations, hard-to-find stock numbers,where assistance can be found for specific situations, a quarterly ship schedule, a quick reference guide to the contents of various publications, and so on.

Transition

The Navy is committed to the system concept. Therefore, all equipment must be system orientated. As new equipment is developed that will perform more efficiently in the system, the less efficient equipment will be replaced, or a new system will be phased in.

Integrated Circuits (IC)

The integrated circuit is small, fast, long lasting, reliable, with low power requirements, high current capacity (with proper heat dissipation), high temperature stability, and very little heat dissipation. ICs are less expensive to produce than a comparable circuit of discrete components.

To the maintenance technician, the arrival of ICs (integrated circuits) means a change in the emphasis on his training and maintenance role. Many of these changes have already begun to be felt.

Integrated circuits come in various sizes, shapes, and appearances. They can have any number of pins, and may even have a metal case that is used on some of them as a connector. Some of them dissipate a great deal of heat, and require heat sinks (large finned metal areas) to aid in cooling. ICs with similar appearances often involve entirely different circuits, and must be identified by the numbers printed on them. ICs which appear different may sometimes have the same function, and in some cases one can even substitute for the other. There are tube substitution and transistor substitution handbooks to identify many of the tubes or transistors for which a reasonable substitute exists. The transistor handbook would include all solid-state devices in mass production. Tube and transistor circuits are not compatible, and with only a few exceptions, tubes and transistors are not interchangeable. These few exceptions involve solid-state devices that are designed to replace specific tubes, such as high voltage rectifiers, and require that the solid-state device be designed to be physically and electrically compatible with the tube being replaced.

IC "packages" or "chips," as the complete IC with leads attached is usually called, are identified by purpose, method of construction, number of pins, and basic shape, among other ways. Some of the terms associated with the basic shape are flat packs, dual in-line, and TO-5. These shapes and terms were usually introduced by one major manufacturer or another, and have since become standards by which a number of manufacturers have designed their own devices. More and more standardization is coming into the area of packaging, but there are already a large number of styles involved.

Problems involving ICs are usually centered around the power supply. Transient voltage spikes, current surges, poor regulation, and voltage variations can cause problem symptoms or actual damage to the circuitry. The use of test equipment, test lead lengths, impedance of test equipment, and added lengths of card extenders may induce secondary symptoms that are not consistent with the actual behavior of the equipment when it is not being tested. These problems increase substantially as switching speeds become faster in the design of certain equipment. When removing and replacing integrated devices, only the proper miniature component repair equipment should be used. Without proper care, there is a strong possibility of damage to the IC device. In handling unmounted chips, care should be taken to avoid differences in voltage potential, as even the slightest static charge could ruin some IC devices. Contact with your hands or tools which are magnetized is an example. A conductive carrier, or a carrier having a conductive overlay, would be used to protect voltage-sensitive ICs. Another important consideration when replacing ICs is the sequence in which the connections are made. The V_{dd} (device supply) connection should always be made before the V_{ss} (ground) is attached.

ELECTRONIC SOLDERING

One of the problem areas that has surfaced with the widespread introduction of transistor circuits, and the more recent arrival of integrated circuits, has been in regard to the repair or replacement of these much smaller scale components. All factors related to the soldering of solid-state circuitry have much more critical tolerances. Not only are the circuit elements smaller, but the time element has changed. Small circuits heat faster, cool faster, and require an increased speed of work in order to prevent exposure to excessive heat. Improved illumination is required, and often some form of magnification is essential when performing repairs. An increased amount of coordination between the scale of work as viewed under magnification and the hands is a necessary part of miniaturized repair. The technician requires both extreme patience and a strong sense of perfection in order to perform well in this area. He must take great pains to learn to do this work right.

Emphasis on Microelectronic Soldering

In 1964, the demand for improved electronic maintenance support for aircraft systems led to the establishment of miniature circuit repair training for Aircraft Intermediate Maintenance Departments. By 1969, a second

program involving a four-week course in miniature and microelectronic repair techniques known as AMRIP (Avionic Module Repair Improvement Program) was established. The Naval air arm had excellent results following the implementation of these programs, with increased aircraft availability and substantial dollar savings.

In 1973, the Chief of Naval Material was directed by the CNO to establish a similar program for the remainder of the Naval community. This led to the establishment of the Miniature Electronics Repair Program (MERP) in 1974. The MERP program is the one that will be of primary concern to DSs.

At present, the MERP program is a two-week course that parallels the first two weeks of material taught in the AMRIP course. An expansion in the MERP course covers the first three weeks of the AMRIP course, and the acronym will be changed from MERP to MMERP (Miniature/Microminiature Electronics Repair Program), also known as the 2M program. In addition, the first three days of instruction will hopefully be inserted into the curriculum of all class "A" electronics courses at the various school commands.

MERP and MMERP are not intended as training vehicles for all electronics personnel, but they are intended to cover miniature and microelectronics equipment supported by all nonavionics ratings. Essentially, select personnel from the various electronics ratings attend one of several training courses offered at various locations (EIB 932 gives a basic course breakdown), and upon successful completion of the course, are certified as being qualified for performing intermediate operational level of repairs in emergencies—that is, those repairs that normally are done aboard ship or have previously required the turn-in of parts or tender availability in order to accomplish. In addition, MERP trained technicians may also be required to perform repair of items normally thrown away or exchanged when an exceptional situation arises. The certification program also requires that MERP trained technicians be recertified periodically by MOTU (Mobile Technical Unit) personnel who are qualified inspectors with MERP training, or other qualified personnel possessing a current inspector's certificate. This insures that each technician's qualifications are current, and that he continues to keep pace with changes in repair techniques and equipment technology.

EIB 953 contains a list of the tools required to make up a miniature Electronic Repair Kit. Items are requisitioned individually to replace lost or broken tools. The basic repair kit will not be provided to ships without MERP trained technicians, but it is composed of items that can be obtained through the Navy supply system. In addition, Appendix II provides the MERP course bibliography. This is being done so that interested personnel can learn the proper maintenance support that will be required for the new family of miniature circuit components that are being installed in much of the new equipment the Navy is acquiring.

SOLDERING COMMON METALS FOUND IN ELECTRONICS.—Copper is the most common metal for conductors, though some demand exists for silver, which is a slightly superior conductor, or for gold, which is more resistive to corrosion, easier to form, and which can be drawn into extremely small diameter wire. Solder can be used on all of these metals. Brass and tin alloys are often used as terminals and connectors and are easily soldered, but steel and aluminum are perhaps the two most common materials used in chassis construction. Steel does not solder well unless properly coated or "plated" with another metal, such as cadmium, and it is virtually impossible to solder aluminum with a tin-lead alloy. Other alloys and fluxes are sometimes available for these and other soldering applications. A different soldering technique and temperature range may also be required.

One industrial technique frequently employed is the electrolytic plating of one metal over another, to form a thin outer shell. The results can overcome disadvantages inherent in either metal alone. The outer shell, or "plating," might be a better electrical conductor, more resistive to corrosion, or provide a more durable surface. The inner metal might be a "base" (more common, cheaper) metal, or offer greater strength or ease of forming. In general, electrolytic plating is done for one or more of the following reasons: (1) economic, (2)

endurance, (3) improved electrical characteristics, (4) corrosion resistance, or (5) appearance. With plated metals, it is sometimes possible to provide a satisfactory electrical connection based on the characteristics of the outer metal shell only. In other instances, this may not be sufficient. Cadmium-plated steel (identified by a yellow tint) is frequently found aboard ship, since the cadmium offers good corrosion resistance to a salt-laden atmosphere.

FLUXES.–Rosin is a mild, nonconductive salt flux commonly used in soldering electronic circuits. Acid or strong salt fluxes should not be used with electronic circuits since corrosion is sure to continue following the soldering process. Exposed acid can be neutralized, but any absorbed acid, or acid contained in pockets in the solder, will continue to work at bordering surfaces. Even rosin flux should be removed after soldering by wiping tacky or stained surfaces with isopropyl alcohol.

Solid solder is solder without a flux core. Flux core solder has a hollow center in which the flux is located in semisolid or paste form. When heat is applied, the paste becomes liquid and flows over the area to which the solder is being applied. Multicore solders are superior to single-core solders since the smaller diameter cores restrict the flux flow and prevent an uneven flow rate, or the draining of flux from a solder length. Five-core rosin solder is usually preferred in electronics. As a general rule, do not attempt to use any single core solder in electronics work if its composition is uncertain, since it is probably an acid core solder. A clean cut through the solder will show what type of core it has.

Fluxes also come in liquid, paste, powder, or solid form. The choice of flux depends upon the size of the job and the soldering technique being used.

Basic Steps in Soldering

The first step in soldering is to determine exactly what the specific soldering job involves. From this, the soldering technique, the soldering compound, the type of flux, the amount of heat, the choice of soldering aids, and other necessary tools must be determined. The technician is taught how to recognize features of a task that indicate a certain technique is best; then, he is given rule of thumb procedures to follow when using that technique.

The second step is to prepare the surface for soldering. This includes removing paint or insulation, any oxidation, and forming a strong mechanical link between the surfaces being joined. This mechanical link increases the life of a solder connection and reduces the possibility of fractures which may occur during the plastic stage while cooling. It also provides better heat conduction and distribution via surface conduction which is important in forming a good solder connection.

The third step is to apply heat. In electronics, the heated tip of a soldering iron is most frequently used to transfer heat to the prepared surfaces. When this is done, the tip will cool slightly as the surface heats.

The length of time it takes to heat the surfaces to be soldered is controlled by a number of physical conditions:

(1) Ratio of physical sizes between tip and area to be soldered
(2) Initial temperature of the tip
(3) Contact surface area through which the heat transfer will occur (size, contour, and cleanliness)
(4) Ability of the iron to supply more heat to the tip as the tip begins to cool (measured in watts)
(5) Ability of the metal surface to dissipate the heat applied through itself, or to radiate it away

The size of the job determines the size of the iron. Also, the size and shape of the tip are determined by the size of the job and the degree of heat transfer efficiency required. Very large soldering irons and all soldering guns have wattage ratings in the hundreds of watts. Very few of these are found around the Data Systems shops, since they are far too large for most applications. Most electrical and electronic soldering is performed with soldering irons rated at about 15 - 35 watts. Many very small electronic circuits such as integrated circuits and

some transistorized circuit boards might required soldering irons rated as low as 3 - 6 watts.

NOTE: Even small soldering irons will reach temperatures of several hundred degrees, and can inflict painful and even serious burns on unwary individuals. Use extreme care in handling even a supposedly "cold" soldering iron–always hold it by its handle.

If the flux is to be applied to the surfaces separately, on large soldering jobs, it is usually applied while heating the surfaces. The flux should liquefy as the surface heats and coat it smoothly. The rosin does not give a clear indication of the heat involved, but when it begins to smoke, this is usually an indication that too much heat is being applied. Another indication is shown when the metal surfaces where the heat is being applied begins to darken, and if the application of heat continues, even for a short period, these areas may turn blue. Care should be taken to prevent this from happening, as the changing color indicates rapid oxidation from extreme heat, and this will hamper the joining process. Overheating is a critical problem with microelectronic circuit repairs.

The fourth step in soldering is applying flux and solder. The solder will melt from contact with the tip, but will not flow properly until the surface to be soldered has also reached the right temperature. As soon as sufficient solder is applied, the solder junction should be left to cool slowly. Keeping the iron applied longer than necessary will not harm the solder connection itself, but the heat being dissipated along a wire could alter the electrical characteristics of the insulation, or eventually reach and destroy a heat sensitive component, such as a diode, transistor, or IC. Heat sinks are used to "soak off" (draw off) some of the unwanted heat, and are placed between heat sensitive components and the soldering point. Beeswax is sometimes applied as an indicator of potential overheating at critical points. The beeswax would be applied to the metal surfaces where heat conduction would most likely occur, and in front of components which could be damaged by heat. The beeswax will melt when temperatures rise at that point, giving a visible warning which must be heeded before further heat conduction affects the components in question.

If the melted solder is applied for too long, it will "wick" (act with capillary attraction) its way along the stranded wire, which is widely used in electronic circuits for its flexibility. This wicking action will harden the flexible wire, making it more likely to break. The solder wicking action will also cause heat to flow along that wire. A solder flow running up under the insulation could expose the insulation to high temperature. The insulation may melt, lose its resistance, or end up hiding a break in the hardened wire which can not be seen. Heat sinks are also used in controlling this wicking action.

Another technique frequently employed with stranded wire to reduce "wicking" (and to some extent, overheating from prolonged heat application) is a process called "tinning." Tinning involves applying solder separately to the wire and to the area to which it is to be joined. Immediately after being tinned, each is allowed to cool. When brought into direct metal contact, heat is again applied until the solder surfaces melt and flow together, at which point the heat is immediately removed again. Without proper care and properly designed connections, tinning can result in poor mechanical linkages and a large number of fractured solder connections.

Sometimes "wicking" is used deliberately as a means to draw excessive solder away from a junction, out along a scrap piece of stranded wire or copper braiding placed there for that purpose.

Blowing air on a solder connection to speed its cooling can result in a fracture of the solder caused by the metal contraction of the rapidly cooling exterior shell while the inner portion of the solder is still in an expanded plastic state. While cooling, all components must be held rigidly in place to prevent fractures. The various stages of cooling are noted visually in the following order:

(1) "quicksilver"–solder in liquid state
(2) "shiny"–outer shell in plastic state
(3) "skinned over"–Transformation of outer shell from plastic to solid state
(4) "dull"–outer shell in solid state

The inner core can generally be assumed to have reached its solid state in about the same length of time as it would take to repeat these four steps. Analysis of the final appearance of a solder connection can disclose the nature of the junction achieved, and details of this analytical process are shown in a module of the Navy Electricity-Electronics Training Series (NEETS).

The fifth step in electrical soldering is a visual, then an electrical inspection. The area has to be cleaned of excess flux and excess solder. The solder junction must be inspected carefully for a proper finish. Stranded wires must still be flexible and not stiff. The solder flow must be checked to be sure it covers the area adequately. Then after all this, insulation must be replaced and a resistance check of the circuit made. Finally, the entire circuit should be checked under normal or simulated operating conditions.

GENERAL SOLDERING FOOTNOTES.—The probable cause of most soldering failures involves either improper surface preparation or improper heat application.

There are many ways to classify soldering techniques. This text refers to only three. These are (1) nonelectrical soldering, (2) general electrical and electronic soldering, and (3) microelectronic soldering techniques. Only microelectronic soldering will be covered by this text, although data systems technicians must know the other areas also.

Military Specification Soldering Process, General Specification for, MIL-S-6872B of 14 June 1968, deals with a wide range of soldering applications, most of which are nonelectrical. However, it refers frequently to the specific electrical characteristics of the various solders and fluxes used by the military. The specifications given are mandatory within the Department of Defense, and are very helpful to the technician when attempting an unfamiliar soldering task.

MICROELECTRONIC SOLDERING TECHNIQUE: REFERENCES.—Several good references on microelectronic soldering techniques are:

(1) NAVSHIPS 0967-LP-000-0160, *Electronics Installation and Maintenance Book, General Maintenance Book,* Sections 5-6; (2) NAVSHIPS 0967-311-5010, *Microelectronic Maintenance Manual;* and (3) NAVPERS 10085-B, *Tools and Their Uses,* which contains information of a general nature, much of which is probably repeated elsewhere, but still a useful guide.

The National Aeronautics and Space Administration (NASA) has published two very well prepared manuals. These are NHB 5300.4(3A), *Requirements for Soldered Electrical Connections;* and NASA SP-5002, *Soldering Electrical Connections, A Handbook.* Both manuals give detailed coverage on electrical soldering.

Soldering Alternatives

Despite its several advantages, soldering is not the only means of joining metals together. Reliance on temporary connections using male and female connectors continues, and alternative ways of forming permanent wire junctions in equipment are on the increase. The chief advantage of these alternate methods is the increased use of automated equipment during assembly stages. The technician may also find that he receives several advantages in trying to maintain equipment with solderless techniques. These will be pointed out at the appropriate time.

Only two alternate methods, wire wrapping and crimping, will be discussed here. Wire wrapping is the technique most frequently employed in electronic equipment that is not dependent upon solder connections. It is highly regarded for the ease with which the basic technique can be learned and used. It is often considered superior to soldering when in-equipment repairs or modifications (field changes) are required. In the electrical field and in some electronic areas, the process of crimping has become widely used. It is also somewhat easier to use than soldering.

WIRE WRAPPING.—Basically, wire wrapping is simply winding a solid wire tightly

around a stiff pin to provide a good junction. Equipment using the wirewrap technique have long square pins at the rear of the female connectors used for logic card inserts. These pins are long enough to allow one, two, or even three wires to be wrapped on them individually in separate wraps. (A "wrap" is defined here as a series of turns of a single solid wire about a post.) The female connectors are then interconnected from pin to pin by a small, solid, insulated wire. This insulated wire may or may not be color coded. Machine-wrapped assemblies usually do not contain color coded wiring, while hand-wired assemblies do. (Color coded wire is an advantage in hand-wired assemblies, since each wire becomes more distinctive and fewer errors are likely to result.)

In addition, machine-wired assemblies are usually distinctive in their layouts. Wires do not always run point-to-point as usually occurs in hand-wired assemblies. The insulation used on some of the wiring is Teflon, which has the undesirable trait of gradually flowing away from any point of continued pressure—a process described as "cold flow." Teflon-insulated wire in contact with a pin may eventually result in an intermittent short occurring at that point. Meline (another insulating material which is more resistive to cold flow, but which does not have the very high temperature characteristics of Teflon) has become more widely used because of the cold flow problem.

The principle behind wire wraps is a simple one. In order for proper conduction to occur between two metals, it is first necessary to penetrate the oxide coating that has formed on both surfaces. The pins used in the wire wraps are squared off, with corner edges that will penetrate the oxide coating of the wire when it is properly wound on the pin. The edges will also lose their oxide coating when they penetrate into the surface of the wire. The junction that is formed is strong, gas-tight (tight enough to seal out gasses, in addition to liquids), and resistive to corrosion.

The technique in doing wire wraps is also fairly simple. First, a special solid conductor insulated wire is required. The wire is a composition of a silver alloy with a copper coating, and the insulation is usually either Teflon or Meline. Silver offers an advantage in that its oxide is almost as conductive as the pure metal. Teflon offers an advantage of very high temperature stability and ease of cutting (for stripping by automatic machinery). Meline withstands continued exposure to pressure much better than Teflon. The use of solid conductor wire insures that the coil will form tightly about the pin and remain that way without appreciable slippage.

A simple hand tool is required to coil the wire on the pin. A specific length of wire is first stripped of its insulation. The end of the wire is then placed in either a long shallow groove along the barrel of the wire-wrap tool, or inserted in the smaller of the two holes that appear at the end of the barrel (fig. 2-1). The center hole at the end of the barrel is next slipped down over the pin. When the barrel is rotated about the pin, the wire will twist about the pin. As the wire twists about the pin, the stripped portion of the wire that is being held in the groove (or in the other base hole) will next be drawn down to twist and coil around the pin. The barrel of the wire-wrap tool rotates as a result of finger, hand, or motor action, depending upon the tool's design. The coiling action of the wire on the pin automatically lifts the tool sufficiently to continue the wire coil up the pin, provided pressure on the tool is not excessive, as this would cause the coils to "bunch," or overlap.

The size of the pin and the size of the wire used require proper size holds (or hole and groove). Wires used in wire-wraps can range from 18 gauge to 30 gauge in size, with pin sizes varying accordingly. The groove (or hole) for the wire is carefully sized to provide the exact amount of tension needed to form a secure wrap when the tool is used properly.

The number of turns required to form a satisfactory wrap varies, from four complete turns for 18-gauge wire, to seven and a half complete turns for 30-gauge wire.

Wire wraps are normally removed with a wire-wrap removal tool (fig. 2-2). This prevents

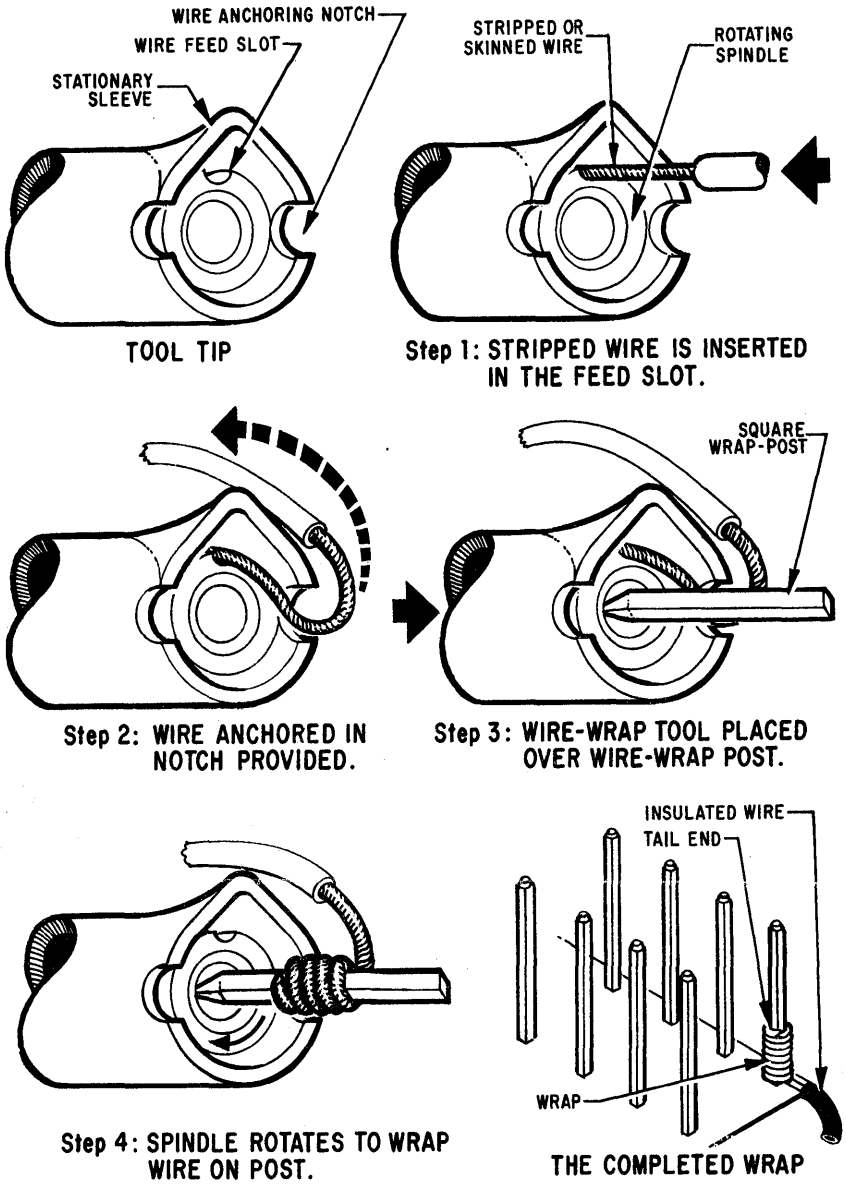
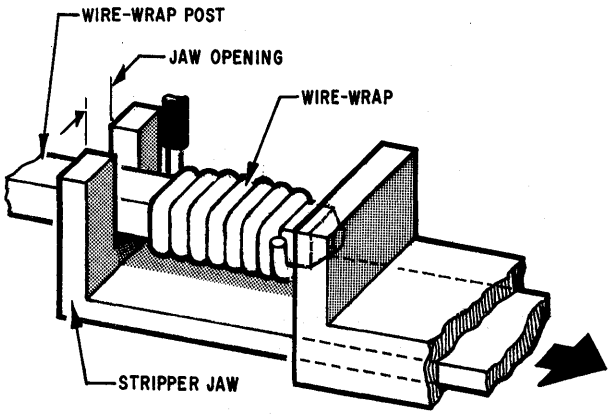


Figure 2-1.—Basic Wire-Wrap Procedure.

stress and possible damage to the wire-wrap post. However, if it is necessary to remove the wire by hand, the important thing to remember is to unwrap the wire without applying stress to the post. This can best be accomplished by gently uncoiling the wire with a slight rotating movement over the point of the post, and insuring that the manner in which the wire is removed does not cause movement of the post itself (fig. 2-3). If a post is bent, it will probably break when an effort is made to straighten it. If a post breaks, it is necessary first to make sure that the broken length is not left in the wiring to cause possible shorts, and then to take the necessary steps to install a new post. Normally, inner wire wraps are placed near the bottom of



NOTES:

1. STRIPPER (WIRE-WRAP REMOVAL TOOL) IS INSERTED WITH JAW OPENING UNDER WIRE-WRAP, AND BASE OF TOOL IS ALIGNED WITH POST HEAD.
2. STRIPPER ACTION CAUSES STRIPPING JAW TO MOVE TOWARD TOOL BASE.
3. TAPER AT END OF WIRE-WRAP POST CAUSES WRAP TO LOOSEN AS WRAP IS FORCED UP THE WIRE-WRAP POST.
4. STRIPPER WILL NOT DAMAGE POST, IF STRIPPER IS KEPT ALIGNED TO THE POST DURING STRIPPER ACTION.
5. WRAP CAN BE REMOVED INTACT WITHOUT NEED OF UNWRAPPING, TO PREVENT POSSIBLE DAMAGE TO THE POST BY UNCOILING ACTION IF DONE MANUALLY.

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Figure 2-2.—Wire-Wrap Removal with Wire-Wrap Removal Tool.

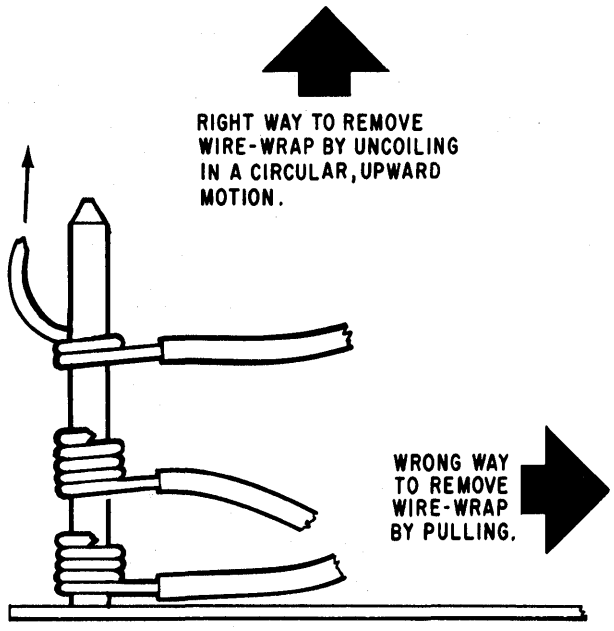

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Figure 2-3.—Method of Removing a Wire Wrap Manually.

the post to insure that additional wraps can be added easily as future needs dictate. If a lower wire wrap must be removed, each wrap above it must be removed first. At no time should a wire wrap be removed by attempting to pull it along its axis (see figure 2-3). Remember, each wrap is easily identified because it is formed from the multiple turns of a single solid wire. However, it is possible to place a number of wraps on a single pin, the number of wraps depending upon the wrap lengths and the pin length. At no time would one wrap be wound directly over another wrap, or would two wires be twisted together and used to form a single wrap. The first method might loosen the gas-tight seal of the inner wrap; while at the same time, the outer wrap would not form a gas-tight seal since there are no sharp angles to break through the oxide coatings on both wires. The second method cannot succeed, since wire-wrap tools cannot maintain proper tension on the twisted wire. Wire-wrap pins can also be pulled loose in their mounting, causing poor continuity or an open circuit. Personnel must exercise some care when making wire-wrap repairs or changes.

When wrapping a wire, a machine or handtool should be used. Figure 2-4 shows some of the types of handtools currently available for this purpose. There are several ways in which wire wraps can be done INCORRECTLY. Here is a list of the most common, which can only be identified visually (figure 2-5):

(1) Insufficient tension on wire—results in loose connection (detected by open spaces between adjacent turns)

(2) Overtension on wire—results in loose connection (detected by turn overlaps and insufficient surface contact with the pin)

(3) Insufficient number of turns (less than five)—poor contact (insufficient wire was stripped first)

(4) Insulation does not extend to pin—increased chances of shorts or wire breaks (too much wire was stripped)

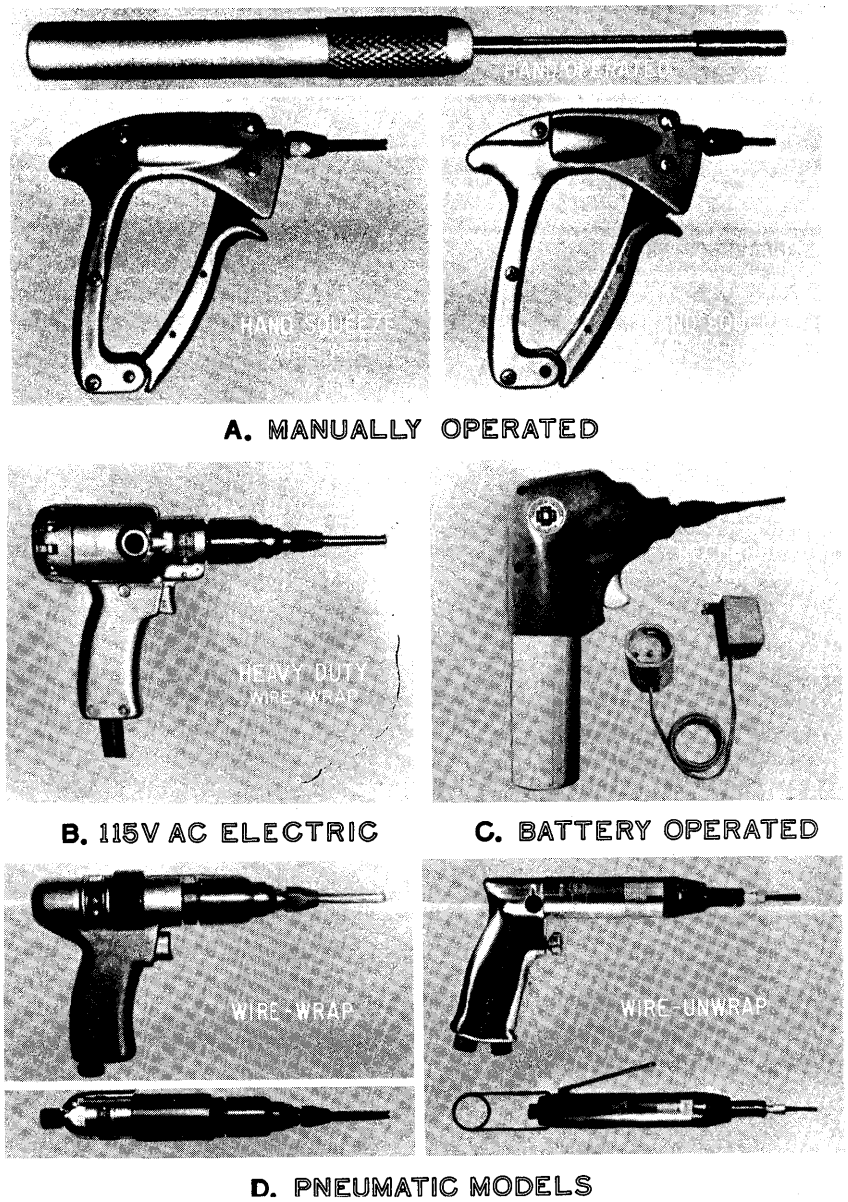

Figure 2-4.—Examples of Wire-Wrap Tools.

(5) Reuse of an uncoiled wrap–each reuse increases likelihood of wire breaks

(6) Attempts to wrap by hand–insufficient and uneven tension results in poor contact.

A good wire wrap can be identified (fig. 2-5) by four to seven and a half snug turns of wire with the insulation about the bottommost one or two turns, no spacing between adjacent turns, no bunching as one turn attempts to cover another, and no observable nicks in the wire. The number of turns is determined by the wire gauge. Larger diameter wires and pins require fewer turns, and smaller diameters mean more turns.

In some equipment, such as the RD-281 Disk File (covered later), the techniques of wire

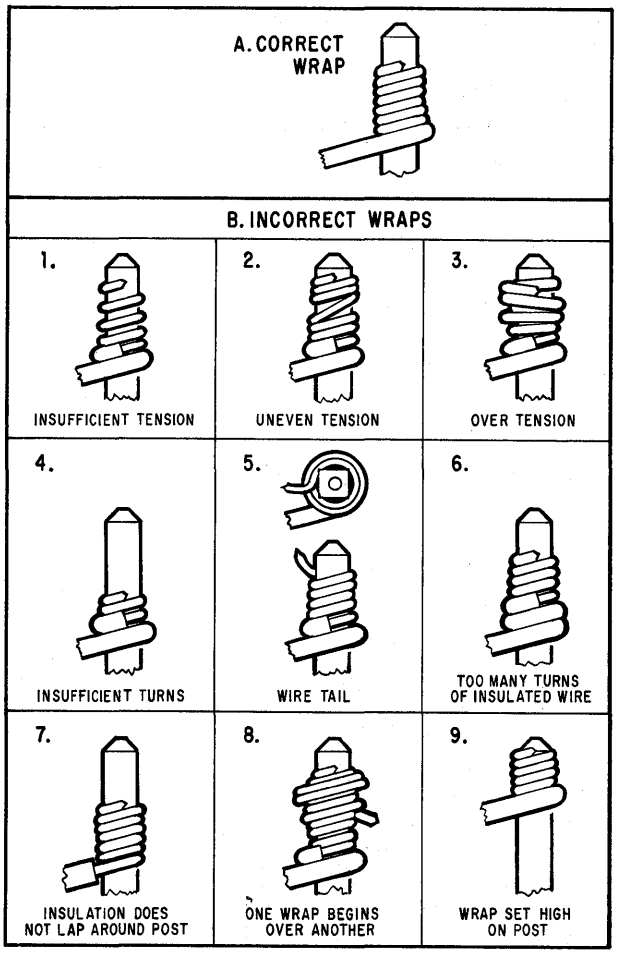

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Figure 2-5.—Correct Vs. Incorrect Wire Wraps.

wrap and soldering are combined to insure a very stable connection.

Some of the advantages of wire wrap are:

(1) Simplified technique for repairs (wires are merely uncoiled to remove, replaced with the proper simple tools)

(2) No solder spill (makes repairs possible without removing components)

(3) No danger of components overheating as during soldering

(4) More in-equipment repairs and faster repair times

(5) No danger of burning personnel (as from a hot soldering iron)

(6) Durable electrical contact (as good as have been achieved with good soldering technique, and superior to those connections made with poor soldering technique)

Some of the disadvantages of wire wraps are:

(1) Use of solid wire (increased likelihood of wire breakage)

(2) Problems with insulation

(3) Unsuitable to subminiature assemblies

(4) Lack of a wire color code in machine-wrapped assemblies

(5) The necessity of clipping off the wrapped portion of the wire and stripping the insulation back to expose new wire in making the next wrap. (If the wire is too short to permit this, it must be replaced. The reason the same portion of wire is not reused in the new wrap is that this area will have been weakened structurally by nicks from its previous use, and will be weakened further if reused.)

A number of useful tools, and techniques for using them, have been developed for doing wire wraps. An excellent text on wire-wrapping techniques is Code Ident 10001 NAVORD OD 23446, *Wire-Wrap Assemblies, Description and Use of Tools and Documentation,* an ordnance manual used by the Fire Control Technicians (FTs). Another document that covers wire-wrap techniques is MILSTD (military standard) 1130, Connections, Electrical, Solderless, Wrapping.

Personnel are advised to use caution in working with wire-wrap assemblies. These assemblies look like a bed of nails, and people have been injured by simply not taking precautions. A number of injuries occur to the face, when the technician attempts to get a good look at it from the side. This exposes the eyes to a needless hazard. Use sufficient lighting to make out details, small mirrors where feasible, and wear safety goggles if a first-hand view from this position is necessary.

CRIMPING.—Crimping is a technique of joining two metals by compression, which is a type of hammering process. A crimp is a permanent clamp that is crushed inward to seal enclosed metals together. A crimping tool is used to provide sufficient leverage to complete the compression process. Crimping is commonly used to join wires to terminal lugs, bond

multiwire ribbon cables into multipin connectors, or to splice two wires together. Crimping offers advantages in speed and simplicity, works with both solid and stranded wire (especially in large diameters), and does not destroy a wire's ability to flex outside the crimp, as might occur from a requirement to use only solid wire (as in wire wraps), or from a solder wicking action in flexible wire. On the other hand, crimps are more difficult to remove, can not be reused (which makes them poor choices as fixed parts replaceable modules), and their use can result in more wire nicks. Wire nicks provide increased opportunity for wire flexing and breaking. Crimping and wire wrapping are generally unsuited for subminiature assemblies.

A technique used in NTDS display equipment encompasses both wire-wrap and crimping principles. This is the termi-point technique used in AN/UYA-4(V) equipment, where a flexible wire is substituted for solid wire, and a clip (a type of crimp) is then applied over the coiled flexible wire to secure it firmly to the pin. A termi-point insertion tool is used instead of a wire-wrap tool, and a termi-point removal tool is necessary when removing the wire clips. Typical termi-point and various crimping devices are shown in figure 2-6.

SOURCES OF TOOLS AND ADDITIONAL INFORMATION.—EIB (Electronics Information Bulletin) number 872 contains a list of miniature component repair tools to be used when repairing the CP-967 computer. These tools make up a basic microelectronic repair kit. In addition, earlier EIBs give stock numbers for tools needed for teletype repair, etc. Reference to these bulletins is useful in acquiring the tools that are essential to proper maintenance. NAVSHIPS 0967-LP-000-0160, EIMB, General Maintenance Book, also gives a suggested tool kit composition. However, only the EIB comes close to providing enough stock numbers for actually ordering these tools through the Navy Supply System.

The Navy supply system is extremely large. It handles a tremendous amount of material. In order to compress its fantastic inventory down into a series of usable documents, some sacrifice in detail may occur. It is this lack of detail that often makes it difficult to select the appropriate item when trying to order directly from the supply system catalogs. Technicians frequently find it necessary to attempt to identify precisely what is desired by some other means, such as checking with other repair facilities, or browsing through SERVMARTS.

Technicians in the field can help themselves and each other by attempting to improve the amount and quality of information that is exchanged between various commands and work shops. The EIBs are published by NAVSEC (Naval Ships Engineering Center), and these are an obvious means of distributing useful information of this nature. The back sheet of some EIBs is a comment and tear-off letter addressed to NAVSEC, and can be freely used to pass on useful information for possible publication. Any individual, who has information that would be of interest to the electronic ratings (ETs, DSs, FTs, and others), should feel free to use this means of passing his information along.

Microelectronic Soldering

Microelectronic circuits have unique characteristics that must be considered when being repaired. They are very small, making them difficult to see in detail, and many standard tools are far too bulky and clumsy to use. They are very susceptible to heat damage, and special soldering irons with small tips and low wattages are required. They can be damaged by a drop of only a few inches on hard surfaces, or by being rapped too sharply with some object. The conductive leads are thin ribbons of metal, easily torn, broken, or burned. The thin metal ribbons that are bonded to the printed circuit boards between components will come loose from the board if overheated.

Many printed circuit board components and metal runs are permanently sealed under a plastic, varnish, or epoxy coating. The coating is used to help the circuit withstand environmental stresses and atmospheric corrosion. The coating used in military equipment is usually standard coating. This coating has to be removed for repairs, and replaced by a similar coating when finished. Because heat can be destructive to solid-state devices, many are protected by metal devices called heat sinks or heat shields (depending upon the manner in which they protect the components).

Figure 2-6.—Termi-Point and Bendix Crimping Tools. 124.534

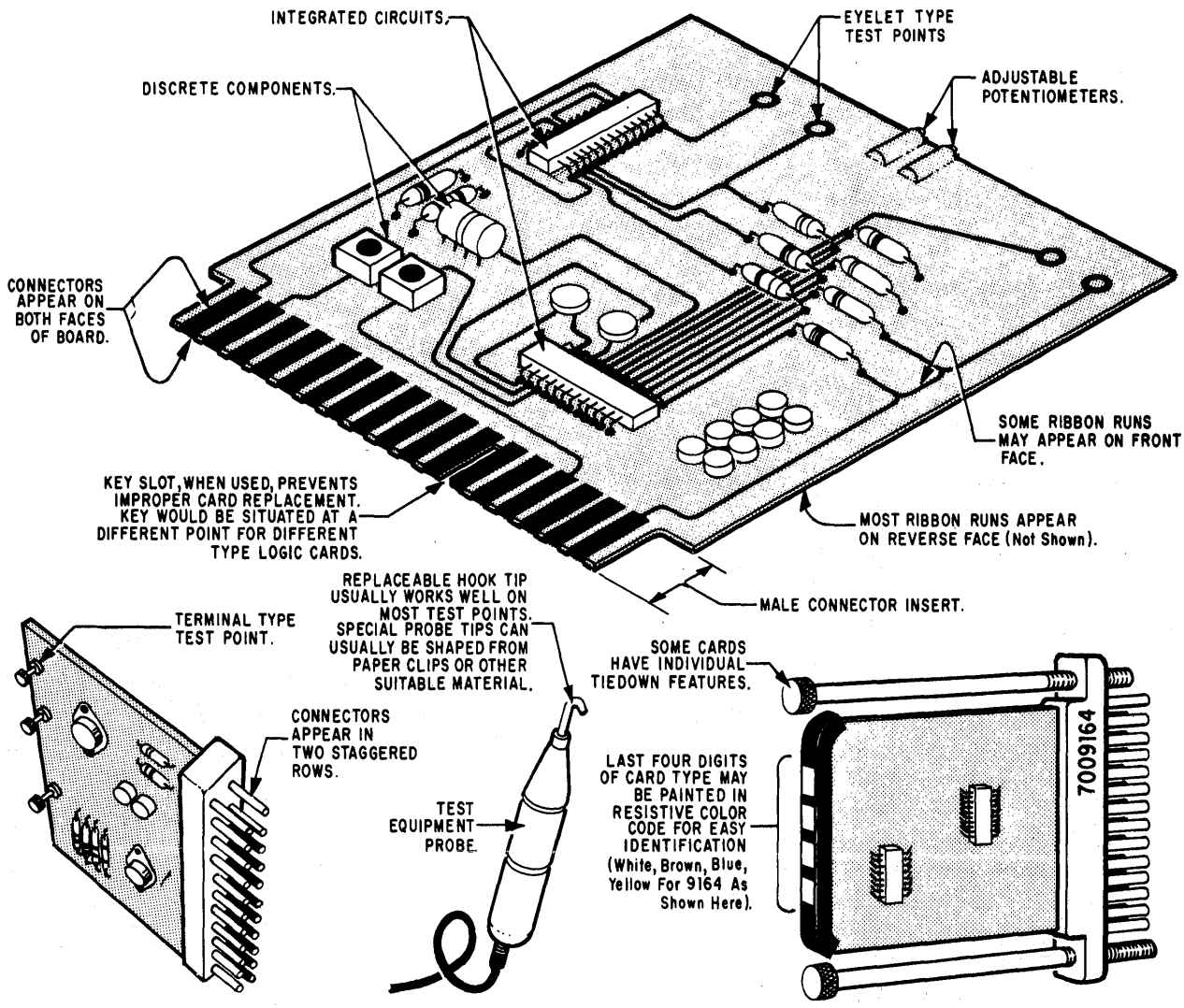

Figure 2-7.–Examples of Logic (Printed Circuit) Cards. **124.535**

Some high power transistors require chemical bonding to their heat sinks in order to improve the heat transfer that occurs between them. Special chemicals are required to form these bonds, and other chemicals may be required to remove them. The technician has a responsibility for the equipment that he supports. This includes insuring that these special considerations are understood, that whatever may be required is close at hand, and that the work is adequately performed.

Many microelectronic circuits function at extremely high speeds, or utilize square wave pulses which have high frequency components. The high frequency characteristics of these circuits can be seriously affected by either improper component replacement, or improper printed-circuit card repairs.

Improper handling or repairs may also permanently damage PCs. A large number of repaired printed circuit boards fail on the first try when reinstalled in the equipment, after having already been passed as being serviceable by poor postrepair testing techniques. Often, such techniques involve resistive or passive (d.c.) voltage checks, and do not check high frequency

characteristics of the circuit board's components. These must be checked under in-circuit conditions. Others fail very rapidly in service when subjected to environmental stress. The biggest single cause of failures in most cases is an improper soldering technique. Poor testing techniques are the principal reason marginal or bad cards go back into the equipment to create further problems.

PRINTED CIRCUIT BOARDS.—The art of developing printed circuit boards has gone in several directions at once. As a result, the data system technician will have to know many types of printed circuit board assemblies. Some boards are soldered into their final connections, while others rely on multipin connectors to complete the hookup. Some boards are single-layered, meaning only one side of the board has a developed pattern of ribbon runs. Others may have their components assembled at such a high density that multilayered boards must be assembled together with two or more layered ribbon run patterns cross-connected at different points.

In general, the state of microelectronic circuit board repair has advanced sufficiently that a high percentage of any of these circuit boards can be repaired. However, a large number of these boards are thrown away, possibly for lack of training, tools, or both. In some cases, replacing a part in a PC assembly can be more expensive than replacing the entire PC assembly. In other cases, an inefficient repair rate would appear not to justify the replacement cost.

Some circuit cards are turned in to a repair facility for repairs, and many of these are done on a direct exchange basis. As the cards are repaired, they are added to the pool that is used to support the exchange system.

A limited number of boards are considered classified. These must be handled, stored, and disposed of accordingly. The procedures for disposing of damaged boards should be established by senior personnel according to the guidelines passed down to them. Once these procedures are in force, they should be understood and adhered to by all DS personnel.

CARDS.—A card (also printed circuit card or logic card) is a form of printed circuit board with male or female connectors at one end so that the entire board acts as a single plug-in module (see figure 2-7).

Equipment requiring a number of cards group the cards together into an orderly arrangement. Each card type is identified by a number, and some cards even show this number in colored bands using the resistive color code (figure 2-8 and table 2-1). This technique makes

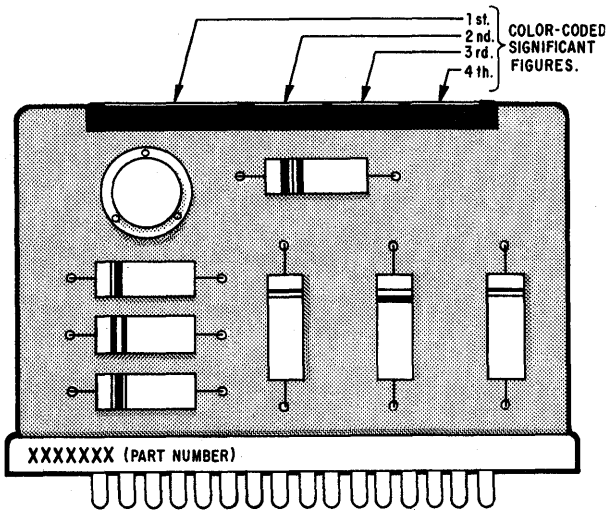

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Figure 2-8.—Logic Card Identification by Color Code.

Table 2-1.—Color Code Values (Adapted from Standard Color Code)

SIGNIFICANT FIGURE	COLOR
0	BLACK
1	BROWN
2	RED
3	ORANGE
4	YELLOW
5	GREEN
6	BLUE
7	VIOLET
8	GREY
9	WHITE

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it possible to check the card number, the card type, and from this, the general function of the card by merely viewing the outer edge of the card without removing it.

Some manufacturers cut slots, called keyways, into the plug-in side of the card to prevent one card type from being replaced with a different card type (fig. 2-7). The female connector that the card would be inserted into will have a built-up key to match the keyway.

Card Designations.–Depending upon the equipment design, most cards are installed in one or more plug-in chassis or racks (fig. 2-9). Locating and changing cards is made easier this way. Some chassis are easy to get to. Others are hard to reach when in their normal positions. Any chassis is accessible when the equipment is shut off and opened up, but for best troubleshooting results, the chassis should be accessible when the power is turned on. For equipment which is not accessible at this point, special adapters and connectors (such as logic extension cables) are usually available as troubleshooting aids.

An X - Y coordinate system is usually used to show where a specific card is located in the equipment. The row the card is in is usually identified by a letter, and the card is identified by a number. For example, B22 would be row B (2nd row) on a chassis, the 22nd card in that row. This number is not to be confused with the

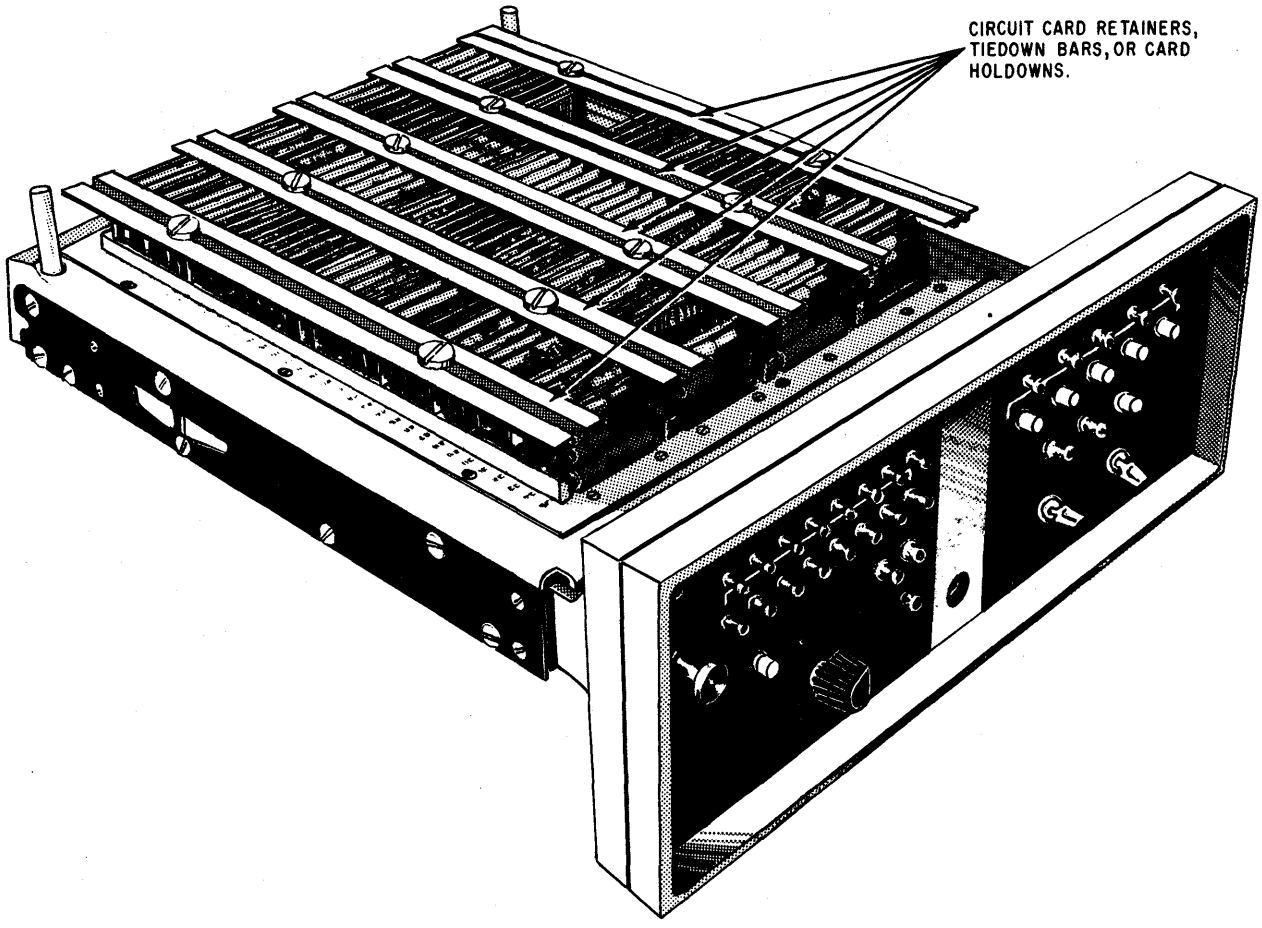

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Figure 2-9.–OA-7984/UYK Console Logic Chassis Assembly.

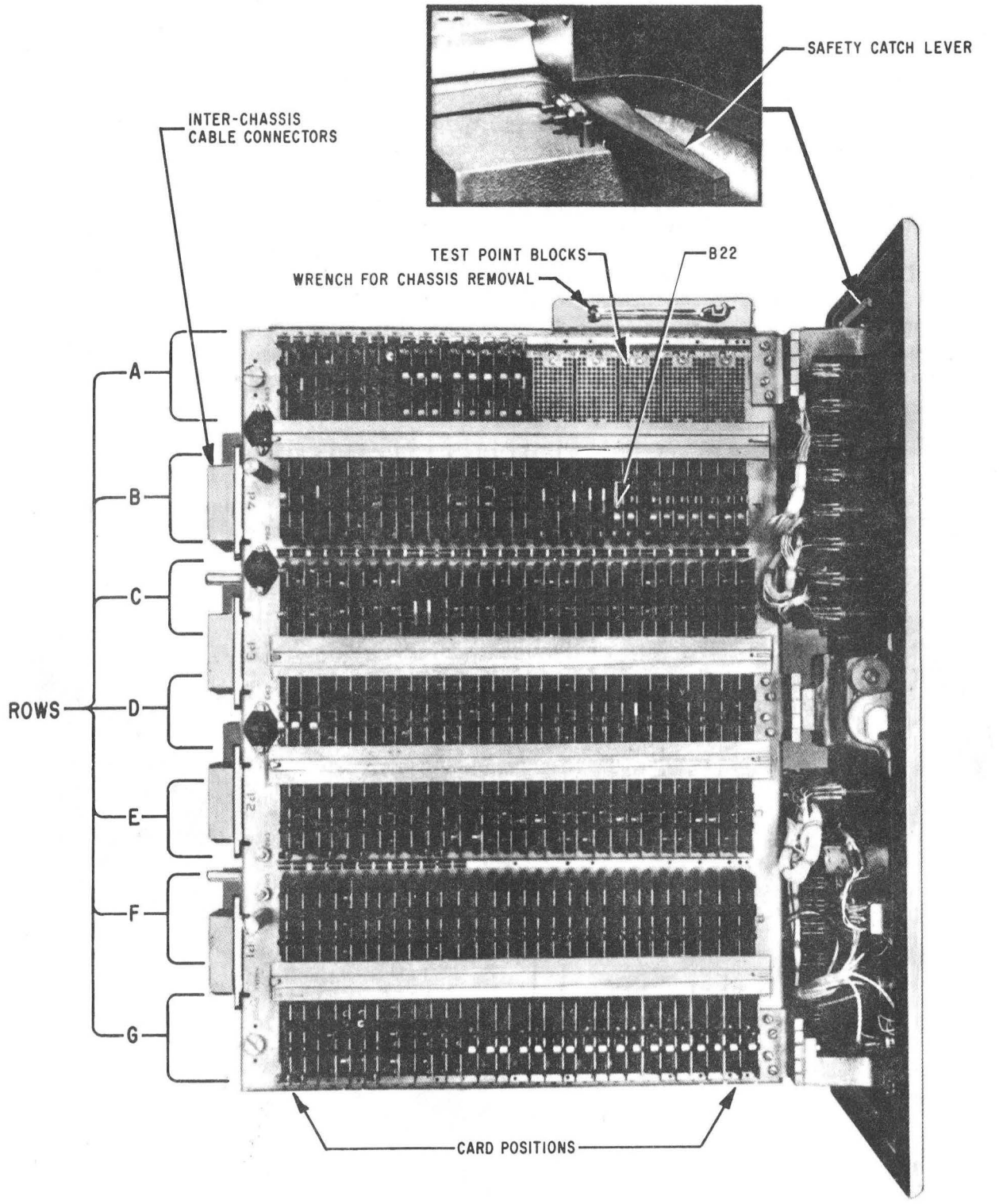

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Figure 2-10.—Logic Chassis A1A1 for RD-270(V)/UYK Magnetic Tape Unit (Removed).

card type number. Larger equipment may have more than one chassis. In this case, a chassis identifier normally precedes the B22, such as A1B22 for chassis A1. Sometimes the equipment is broken up into different subassemblies, in which case both a subassembly and a chassis identifier are required. As an example, A1A1B22 is subassembly A1, chassis A1, row B, card 22 (fig. 2-10). In many logic prints, the A1A1 appears in large type at the right side of the print page, with the B22 indicated in a corresponding logic symbol on that page.

Sometimes a circuit indicator precedes the row-card designator. Ø1B22 would mean the first circuit of card B22, while the logic print page would be chassis A1A1. In each case, there is usually a foreword in the prints which will show what system of circuit designation is being used. There should also be a figure in one of the technical manuals giving the logic chassis designations and where they are located in the equipment.

Some circuit cards have test points where test equipment probe tips can be inserted (fig. 2-11). They may be indicated by another designator on the card numbering system, such as B22B. This means test point B of card B22. In some cases, test point B would be the second from the top. In other cases, it may correspond to a general location on the card. The techniques used for designating 1, 2, 3, or 5 test points are as follows:

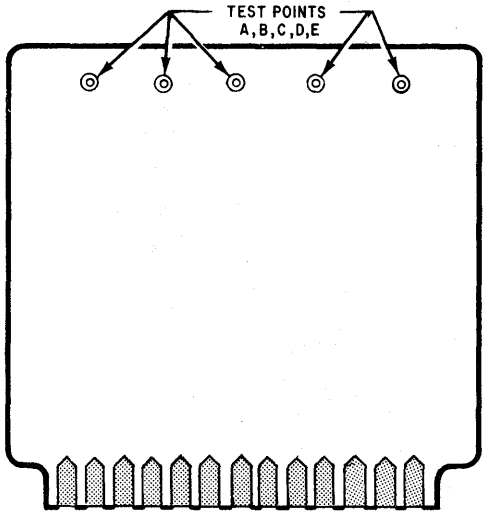

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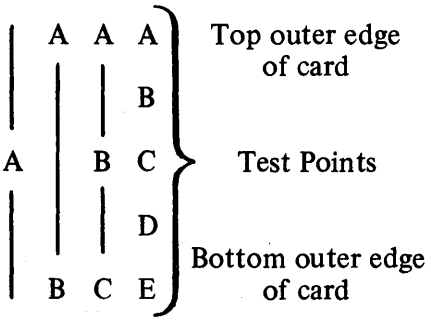
Figure 2-11.–An Example of Test Point Designation.

Method 1:



The specific technique used with each equipment type is shown in the technical manual.

Some circuits either provide no test points, or the test points are not aligned with the outer edge of the card. If there are test points, they are usually numbered by hundreds with the most significant digit corresponding to the circuit number on the card (TP101 and TP102 with circuit 1; TP201, TP202, and TP203 with circuit 2; etc.) (see figure 2-12). In smaller equipment, the test points may be numbered consecutively as they appear in the logic prints, regardless of physical placement.

Pin Connections.–Most pin connections for logic cards provide an electrical and physical connection between the logic card and the chassis. Some equipment provide card guides and locking or tiedown bars so that logic cards will not suffer intermittent problems as a result of vibrations from the ship's movements (fig. 2-9). There may be 22, 26, 32, 86, or more pins involved on each card, depending upon the design of the equipment. Each pin is uniquely numbered or lettered so that it can be identified. The system of pin designation is in the technical manual, and is the same for every connector of that type in the equipment. Additional information on connector pin designation and cable makeup can be found in NAVSHIPS 0967-LP-000-0110, EIMB, *Installation Standards Book*, and NAVSHIPS 0967-LP-000-0140, EIMB, *Reference Data Book*.

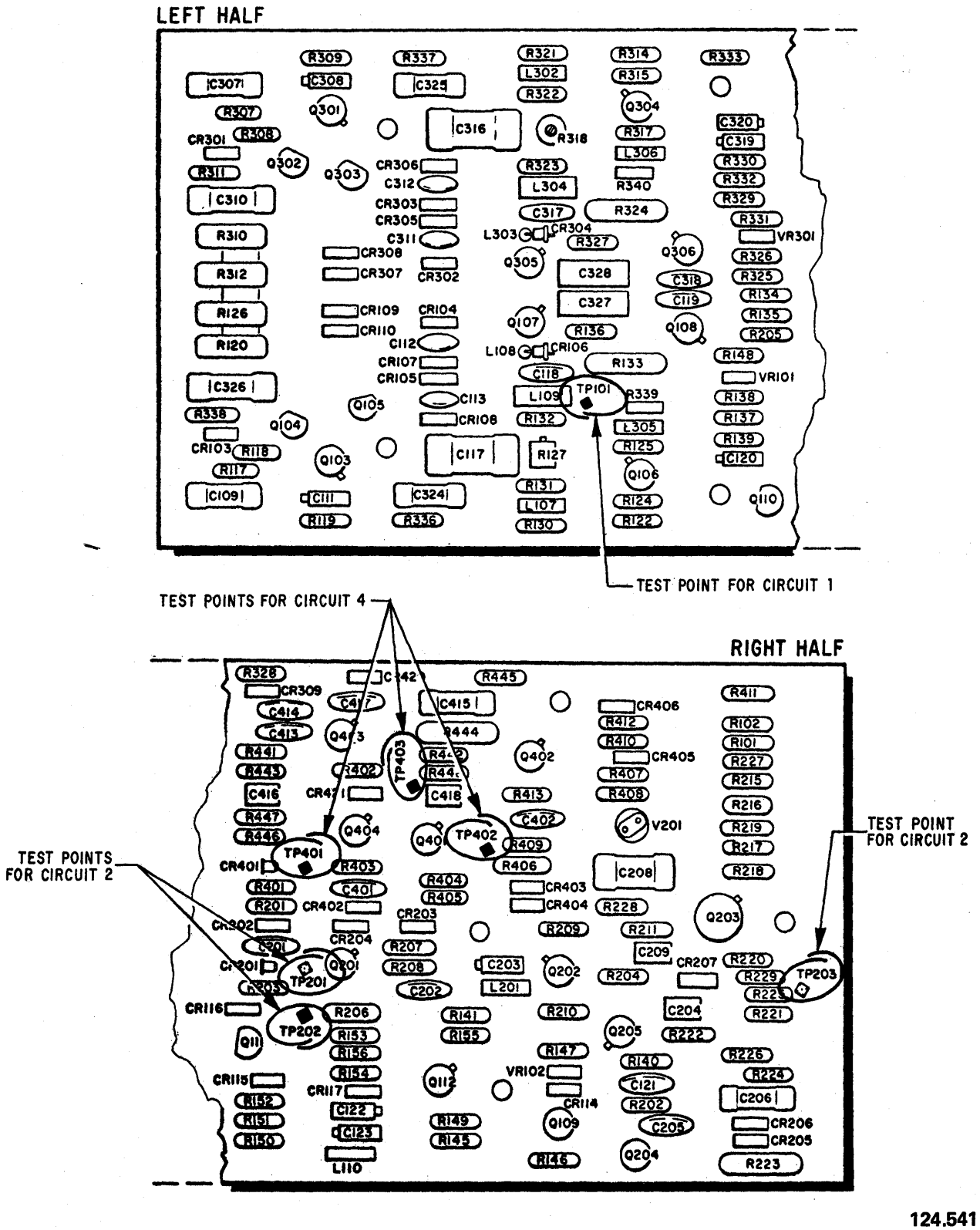


Figure 2-12.—Circuit Board A3A1 for AN/USM-281A Oscilloscope.

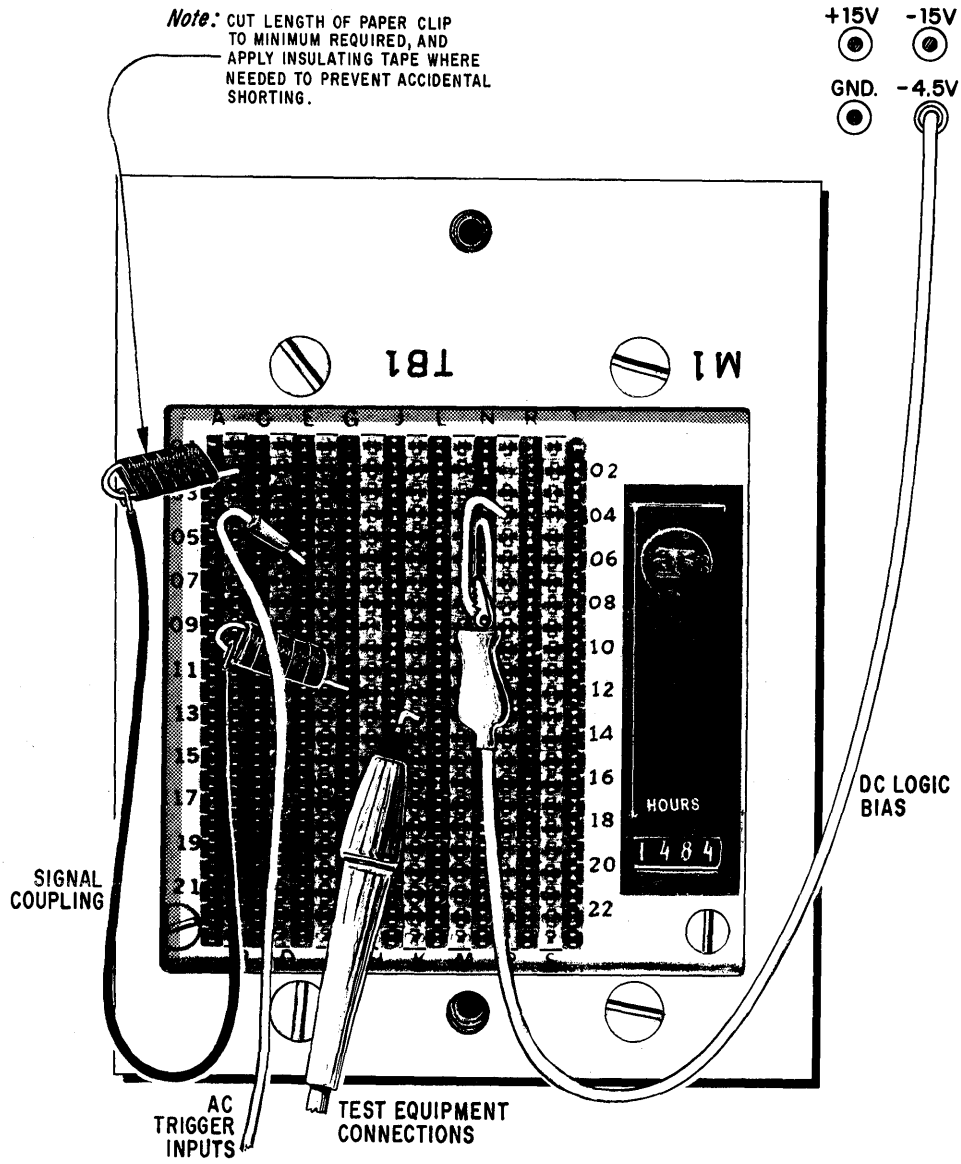


Figure 2-13.–Examples of Test Block Applications.

Test Points.–Most troubleshooting must be traced through the equipment while it is performing some type of redundant operation. To trace a signal with an oscilloscope, make sure that the circuit suspected of malfunctioning is activated. The trace on the face of the cathode-ray tube (crt) will be the composite of repeated pulse trains through the circuit. Some of the newer test equipment have an oscilloscope with logic. These "logic analyzers" as they are called, often use a memory where the basic characteristics of a single pulse can be stored. The logic features can use this information to reconstruct the trace outline, which is then continuously regenerated on the face of the crt. A logic analyzer may even be able to "detect" individual traces that differ widely from the norm. Logic analyzers often

include other features, but these vary markedly from one type to another, and it is not possible to generalize.

To use an oscilloscope or logic analyzer properly, the probe must be attached to a voltage point, which is a conductor, somewhere in the circuit. Usually only the input and output voltage (signal) waveforms are of immediate interest, while source voltages (supplied power and bias waveforms) are not. Some printed circuit cards have metal eyelets or posts centered in the metal ribbon runs through which the input or output signals are conducted. The probe tip can be hooked onto the post, or replaced with a hook fitting that can hang from the eyelet while the signal is fed to the test equipment. Another technique is to use a probe with a flexible hollow tip that can be fitted down over an extended metal pin or post, as is found in the interiors of some equipment.

Some equipment use a technique where an extra multipin female or male connector is fed by input and output waveform connections. The connector is placed at a convenient position where probe tips can be inserted or hung while the circuit is under test or when troubleshooting (fig. 2-13). The test points (for the pins) or test blocks (for the whole connector) are usually grouped in one location for convenience (fig. 2-14). Another system of X - Y coordinates is required to locate a specific pin. In this case, a chassis-test block-test point system is usually used. Sometimes the chassis is left off since the test block is usually on the same chassis as, though not necessarily in the immediate vicinity of, the circuit under test. The equipment manufacturer may reverse the letter-number technique of designating X - Y coordinates so that there is no confusion between the system used to designate the card location, and the system used to designate a test point.

Some types of equipment do not have built-in test points for their cards. Or sometimes it is necessary to observe signals that are not coupled to a card test point or chassis test block. When this happens, it is often necessary to resort to the use of a card extender. A card extender is a logic card having a male connector at one end and a female connector at the other. The logic card under test is inserted into the female connector of the card extender, then the card extender is inserted into the logic card's normal position. The extra length provided by the leads between the male and female connectors of the card extender provides access to the ribbon runs and component leads on either side of the logic card. Usually the card extender will also offer test points for each connector pin (fig. 2-15). Card extenders are easily identified in that they only contain opposing male and female connectors, leads, and test points. They usually have no logic elements of their own.

IC insertion sockets may be used in future equipment. These sockets can be successfully mounted on the printed circuit card separately; then, the IC is inserted into the socket. This technique was adopted for CMOS ICs, which are very susceptible to static voltages. CMOS ICs may not be used in every case, as the technique can be applied equally well to other forms of ICs. This approach increases the ease with which repairs can be made to a circuit, but it also exposes the circuit to an increased rate of corrosion. These insertion sockets will probably be found in limited logic applications and low frequency circuits. However, some manufacturers are able to "crimp" the pins into their sockets during the assembly stage, which can provide good corrosion resistance. Certain metal platings may also be used to improve conductivity. Removing ICs from crimped sockets, or working with certain metal platings may involve techniques not covered in this text. The correct procedure can usually be obtained from the equipment manufacturer.

Several new devices are now available for testing ICs in a circuit. These range from clip-on testers that use LEDs (light-emitting diodes) to indicate current flow in each IC pin, to much larger logic testers to which the module (such as a printed circuit card or logic card) is directly connected. The module is then subjected to test inputs with monitored outputs.

There has always been an effort to use the equipment to check itself. Digital computers are particularly adaptable to this form of testing, and provide excellent diagnostic capabilities when testing online equipment. Unfortunately, not every test result can be accepted on the basis of its indications. This is particularly true where a failure in the test equipment would give the same indications as the equipment under test.

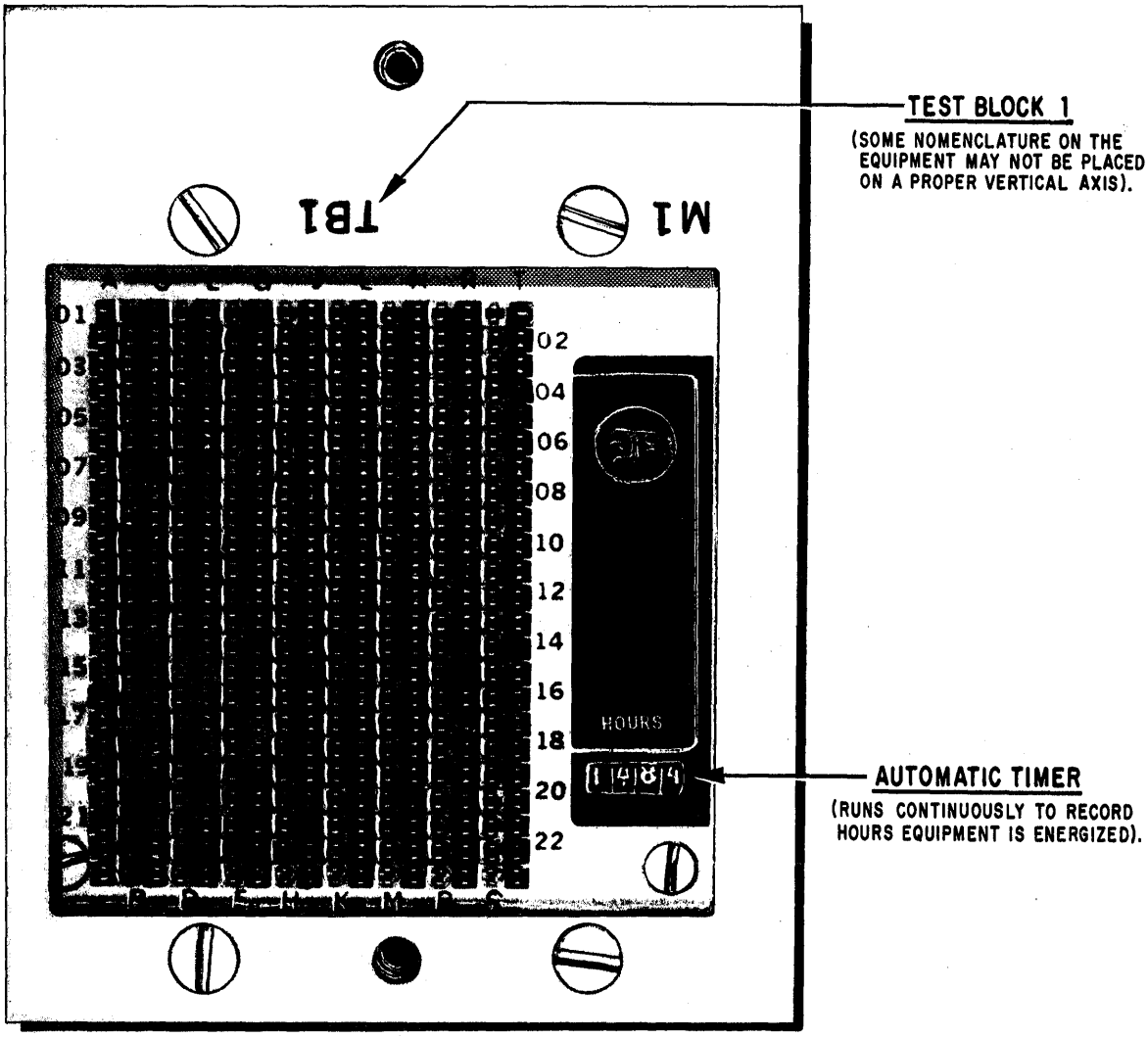


Figure 2-14.–Typical Test Block, AN/UYK-7(V) Computer Set.

This problem is usually more predominant in equipment that perform internal checks upon themselves, since the same circuitry used during the testing might be producing the problem. More reliable results can frequently be obtained with equipment tested by external means. Many types of special devices have been developed as testers and diagnostic aids to other equipment. These use their own logic, or in some cases, function under computer program control.

Whatever test equipment is used by the technician, it is his responsibility to become familiar with its function and operation, to care for it, and in some cases, even to perform repairs on it. If his test equipment is not working properly, he will not be able to depend on it in performing his other duties. Test equipment malfunctions must be reported to his superiors and corrective measures started as soon as possible.

Troubleshooting

The circuitry used on most printed cards form complete functional groups. If circuit

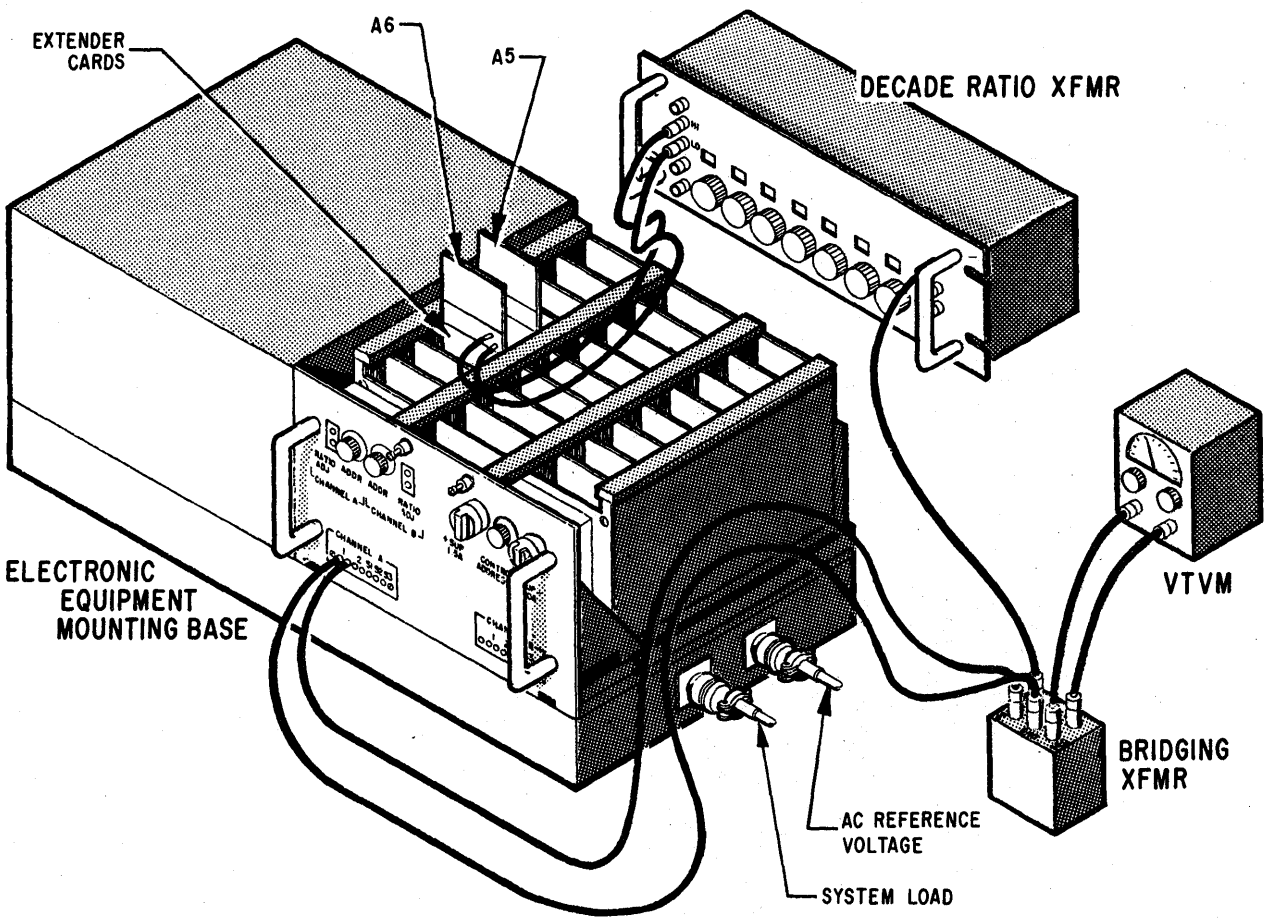


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Figure 2-15.—Ratio Adjustment Test Setup Using Extender Cards (Equipment is CV-1980B/USQ-20(V) DAC).

density is high enough, several functional groups may be found on each card. One card may have several AND functions, or several OR functions, or it may contain some other type of logic function groups. Each card type is usually identified by a unique number. Cards with the same number can be interchanged in many cases. In other cases, they can be exchanged, but only after variable components such as pots (adjustable resistors) on them are readjusted to compensate for different circuit applications.

The number code used with many cards may be followed by a letter, such as 7030A or 2123B. This usually represents a modification or improved version of the basic card type. In most cases, the card function remains the same and the newer card can be substituted for the older version. In some cases, the older version may also be used to replace the newer version. More often, the older version of the card will be reworked into the newer circuit version, and relettered by hand to indicate the circuit revision.

The resistive color code is used to help identify the card. The edge of the card that can be seen will have four color bands to represent the last four digits of the number code (figure 2-8 and table 2-1). This helps verify that each card slot contains the correct card type, without the need of removing the cards to check.

Some equipment use a more positive control over their cards with a "key" used with the

female connector in the card slot. The key must align properly with a key way cut into the face of the male connector on the card before the card can be inserted into the card slot completely. This helps prevent a card from accidentally being put into the wrong card slot (see figure 2-7).

In troubleshooting, when the problem is narrowed down to a single card, the normal procedure is to replace the suspected bad card with another of the same type to verify the source of the problem. If a spare card is not available, the suspected bad card can be exchanged with the same card type (provided no adjustable components are involved) that is in a different location of the equipment. However, a bad card would then cause a different indication of trouble as it affects the new area of equipment, and its behavior in this new area should be anticipated first.

In isolating malfunctions, the card exchange technique can be very useful if properly employed. Sometimes it is very difficult to pinpoint the precise area where a malfunction occurs. By systematically replacing the circuit cards most strongly suspected, the problem can often be found and corrected quickly. Speed is a primary consideration in many types of repair work, and in these cases, the fastest way is usually the preferred way of getting a repair accomplished. The card exchange technique is also one of the most useful ways that has been developed for isolating intermittent problems. The intermittent problem, which comes and goes in cycles, has usually vanished by the time the technician is prepared to look for it with his maintenance programs and test equipment. One failure every few hundred thousand operations or so would be sufficient to disable many digital devices by causing unrecoverable errors every few minutes.

In many cases, the intermittent problem will eventually increase in frequency and duration, until a point is reached where it becomes a "hard" problem and endures long enough to be detected and corrected. In other cases, the computer can be reprogrammed with short, specialized programs which are suited to locating the specific problem at hand. This task is within the ability of most DSs to perform when the need arises. In still other cases, specialized test equipment can be acquired that will add more flexibility to efforts to detect the problem while the system continues to function at its normal job. However, assuming that none of these events take place, the technician is still far from helpless in trying to cope with problems of an intermittent nature. He can begin to systematically isolate all the areas where the problem can originate. Within each of these areas, he can establish areas of higher probability where the malfunction is more likely to occur.

He can do all this just from the vast store of experience he has acquired with the system and with the equipment within the system. Once he has succeeded in doing this, the technician may still find that there are usually many possible areas were the malfunction could occur, yet he may have reached the limits of his experience, his programs, and his test equipment. At this point he may again resort to systematic exchange techniques to find the problem.

TECHNICAL MANUALS.—The technical manuals (TMs) used with Navy equipment are usually provided to the Navy by the equipment manufacturer. In some instances contract specifications require that the manual meet certain military standards. In other instances the Government may accept the existing civilian TM version, and these are more likely to contain unfamiliar terminology or unique symbology peculiar to civilian applications. In addition, the civilian version may be arranged in a different order, and may contain some information that is not necessary to its military application, while not including other material that would be of benefit to personnel providing military maintenance support.

Technical manuals vary in many ways, such as in color, dimensions, order of contents, or thoroughness of detail. Some are several volumes thick, while others may be nothing more than pamphlets. In general, the logic prints and schematics (electronic diagrams), along with maps of subassembly areas, are usually double-page in size. These will usually appear as either foldouts near the back of the technical manual, or may be placed separately in an oversized binder. Most TMs employ some form of looseleaf binding to simplify major revisions.

Many TMs are organized into sections. These sections provide a one-step-at-a-time approach to the equipment, and are arranged to coincide with the arrival of a new device in a system:

Section 1: General Information (Introduction)

Section 2: Installation (gives standards and instructions for packing, shipping, unpacking, and installing equipment)

Section 3: Operator's Section (explains basic operator functions)

Section 4: Principles of Operation (explains equipment operation in detail)

Section 5: Troubleshooting (provides basic offline troubleshooting techniques and symptoms)

Section 6: Repair (gives standards of repair, techniques, useful hints)

Section 7: Parts List (identifies each component by name and either Federal supply number or manufacturer stock number)

Section 8: Functional Schematics (logic prints, power supply schematics, etc.)

Section 9: (If included) Wire List–shows point-to-point wire contacts

Most technicians will report to duty stations where the equipment is already installed. However, it would be a good idea to become familiar with the installation section of the manual. A part of the technician's responsibility is to maintain the equipment, particularly grounding straps, RFI shielding, and other physical aspects, in the installation standards.

In addition to the one, two, three, or four volumes that contain these eight sections, some equipment may have supplementary volumes. Magnetic tape units, for example, often have a subcontractor's manual provided for the mechanics, since these are not covered in detail in the main text. Another volume containing an equipment's wire lists may not be available locally, but it should be obtainable through the Naval Supply System if a problem in the equipment wiring is suspected. Supply requisitions for publications should be addressed to Naval Publications and Forms Center, Philadelphia, PA 19120. In addition, requests for NTDS publications or publications on NTDS-related equipment should first be forwarded to NAVSECNORDIV (Naval Ship Engineering Center, Norfolk Division) code 6623, Norfolk, VA.

There are many program documents prepared for the various systems, which are in addition to the technical manuals. These software manuals (as they are called) detail the function of various programs and provide precise information on operator and user involvement.

Many of the symptoms that are reported to the DS are in terms of apparent problems with these programs. The DS will find that he will require a working knowledge of the system software (operational, utility, and maintenance programs and documentation) in order to provide adequate maintenance support. Most maintenance programs are documented with step-by-step operating procedures, program symptom breakdowns, and even a program listing to show the manner in which the equipment is tested. These are in addition to his obvious need to become familiar with available equipment (technical) manuals.

Most technical manuals have dependable logic prints, and provide a reliable basis for locating discrepancies in the text. For instance, a conflict may arise between the text and flowchart. By consulting the logic prints, it is possible to determine which of the two is correct. Two areas of the text may contradict each other. A timing diagram is traced, a check of the logic prints verifies the result, and the matter is resolved. Most logic prints are almost infallible. They usually act as the ultimate answer to conflicts that arise in the text.

Chassis maps cover those diagrams and tables that show and list the various assemblies, subassemblies, chassis, test point blocks, card slots, and even card placements (by type and circuit) in the equipment. They work in

conjunction with the logic prints (or schematics) in locating those areas and components of the equipment being referred to. The parts list show exploded views of the equipment, identify each component down to the smallest screw, and give the source and part or stock number needed when reordering that item. Wire lists usually just give terminal points of wire connections, so that continuity checks to verify each wire placement can be performed when necessary. These are usually very accurate.

However, in the final anaylsis, NO source is absolutely infallible. In order to correct any faults and oversights, and to question apparent contradictions, a positive feedback program is required. Discrepancies, conflicts, and oversights are all reportable items that, if submitted, could eventually result in a superior technical manual. The technician can use the mail-in comment sheet that appears on the back of some EIBs (Electronics Information Bulletin), or he can use the feedback forms that are used with the 3M system to report any observed discrepancies. Either way, he will eventually be contacted usually within a matter of weeks, and given a response regarding the disposition of the matter. If he requires immediate assistance because of the consequences of this discrepancy, he may make an official phone call or office visit (subject to the approval of his command).

The technician must also make sure that the latest technical manual revision (called a change) is properly inserted and documented. He must verify that the manual is designed to support the exact version of the equipment that he is maintaining. Failure to do these things will eventually lead to someone trying to fix something with the wrong version of a TM, or an obsolete or improperly maintained technical manual, and this can only result in further problems.

Training Considerations

Typically, the technician receives most of his training from service schools, his shipmates, and supervisors. He also uses documents, such as EIMBs, technical publications, rate training manuals, and correspondence courses based on the rate training manuals for advanced training in his field. The equipment technical manuals will teach him the specifics of the equipment he supports. There are equipment MRCs (Maintenance Requirement Cards) to guide him in performing routine maintenance. The MRCs state when the maintenance is to be done, how long it should take, who will do it, what tools and equipment are needed, as well as providing detailed step-by-step instructions.

Additional assistance can also be gotten from the division officer, or the EMO (electronics material officer). There are MOTUs (Mobile Technical Units) staffed by qualified personnel with a vast background of experience in the field and who have demonstrated that they are themselves competent technicians. MOTU personnel will render technical assistance when requested to do so. MOTU units respond automatically to requests indicating that technical assistance is required on casualty reports (CASREP TECH ASSIST). In addition, MOTU personnel will conduct on-site training upon request, and assist in every way possible to evaluate and upgrade the maintenance effort that fleet personnel are capable of. When requested to provide technical assistance to a system experiencing difficulties, MOTU personnel attempt to help the system personnel in their efforts to locate and correct the problem. They do not normally take over and conduct the entire maintenance effort themselves. This approach of helping rather than replacing system personnel serves a more useful purpose, first, in taking advantage of the efforts that the system personnel have already put into trying to isolate and deal with the problem source, and second, in that the joint effort will establish a basis by which permanently assigned personnel will be able to benefit from the experience.

The Navy also has a number of engineering centers where additional assistance can be obtained. The engineering centers are not chartered to provide the same type of assistance as given by the MOTU units. Instead, they are more concerned with ways in which equipment, systems, and material support can be improved. If problems appear to go beyond areas where a simple repair can produce results, then the

engineering center would be very interested to learn what problems are being encountered. Perhaps a certain item will not give reliable service, or perhaps the capabilities of the equipment suffer due to some installation problem. Perhaps a replacement item being procured for the supply system is inferior, or does not seem to be the right replacement part.

The engineering centers have a special interest in any subject that affects the whole system, or which may affect more than one installation. In addition, they like to stay informed and keep in touch with personnel, particularly maintenance personnel, from the various systems that they help support. The input that they get from the fleet can become the starting point for a feasibility study, or for an R&D (research and development) effort intended to upgrade the material aspect of the fleet. The MOTUs act to improve the manpower resources, while the engineering centers are concerned more with the material condition and capabilities.

Because there are a number of engineering centers that have their own specific areas of interests, it is important to know which engineering center has an interest in the particular system being supported. NAVSEC (Naval Ship Engineering Centers) has an interest in nearly all systems that involve ships. They also review all technical feedback forms and EIB (Electronic Information Bulletin) comment sheets that are submitted.

In addition to publishing the EIBs, NAVSEC also publishes the EIMBs, and material considered to be of permanent interest is taken from the EIBs and republished in the FCIG (field change identification guide) and the Service Note sections of NS 0967-000-0010 Communications Book of the EIMBs. The FCIG section identifies the field change nomenclature with the purpose of the change, the serial numbers of the equipment affected, and a means of verifying if the change has been installed. The Service Notes section is organized by equipment (including data systems equipment), and discusses problems that have occurred related to that equipment, and techniques and tools that are helpful in working with that equipment. NAVSEC also verifies requests for technical manuals submitted through the Navy Supply System.

NAVAIRENGCEN (Naval Air Engineering Center) is concerned with airborne systems, weapons, and support. The ACLS (Automated Carrier Landing System) and LCC-IC and CV-IC (Amphibious Command Ship Intelligence Center and Aircraft Carrier Intelligence Center) are just three of the systems that NAVAIRENGCEN has an interest in, and with which DSs are involved in the maintenance. In many of these areas, NAVAIRENGCEN has a working agreement with NAVSEC that allows NAVSEC configuration control and technical support of these airborne support or interface systems.

NAVELEXSYSENGCENs (Naval Electronics System Engineering Centers) are concerned with a great many areas that are also of interest to DSs. Among these are: (1) Involvement with a number of shore based (civilianized) data processing systems, (2) test equipment standards, calibration, restoration, procurement requirements, and validation, and (3) automated test equipment for checking such things as components, circuits, computers and related equipment, also for testing detection and navigation equipment.

Other commands can sometimes offer needed assistance. Ships that have identical equipment but different system configurations can probably provide the best assistance for specific equipment problems. Ships with similar systems, even though the equipment differs, are another excellent source of information, expecially if the problem seems to be generalized to the entire system. Even commands with different equipment and different systems can sometimes be of vital assistance if they have trained personnel available. The odds of finding a technician with a background that covers the area where the problem exists are usually very good if an adequate effort is made to find him. The DS can obtain help in this search by going through his supervisor, LPO (leading petty officer), division officer, department head or CSO (combat

systems officer), and through other elements of the chain of command.

As a rule of thumb, the technician is expected to use his own initiative and begin with the information sources closest to him. He should keep his superiors informed of his progress, so that they can provide assistance in matters that may require their personal attention.

When a ship is in port and individuals are free to move around to some extent, semiofficial contacts between personnel in the various commands, especially with technicians in the MOTUs and engineers in the engineering centers, may prove to be very beneficial. The exchange of information that is possible by these contacts can measurably improve the DS's understanding of his field and his system, and can aid these support commands in their efforts to meet the needs of the fleet.

Intersystem Responsibilities

Many DS systems relate to other systems. The power and the chilled water that is used to energize and cool electronic equipment are two systems that the computer system is dependent upon. Likewise, a real-time system is dependent upon other systems for its input and output. One system may parallel another, or its final stage of operations (output) may serve as the lead-in point (input) of another system.

Combat systems, as one unified structure, is a new concept in the Navy. At present, there are many technical ratings that support different portions of the combat system aboard most ships. This means that in order for the whole system to be supported properly, each of these ratings must know its responsibilities and the responsibilities of the other involved ratings. Another important consideration is that all the rating responsibilities must carefully dovetail so that there are no gaps in the maintenance support being provided. In order to do this properly, there must be a high degree of coordination and cooperation between each shop and each rating. In order to achieve this end, the combat system concept was evolved, and the unification point of a combat systems officer (CSO) is required.

In addition to his other responsibilities, the CSO coordinates the activities of the various ratings assigned to the combat system. He resolves disputes that may arise, and establishes guidelines and determines areas of responsibilities. Technicians in the various ratings can work to the same end by establishing personal contacts and working to provide mutual support. There are occasions when one system has to be configured in a certain way, or set up to provide test data, so that another system can be checked out properly. There are other occasions when a signal discrepancy is traceable beyond the boundaries of one system and probably exists in the other system also. These situations make it essential that the technicians in the different ratings establish a spirit of cooperation and coordinate their efforts in a joint effort to handle these occasions properly. Another occasion when close cooperation is required is when providing maintenance support to some piece of equipment that is tasked to two or more ratings. The OJ-212 modified teletype is one example of such coverage, with OSs (Operations Specialists) providing operator maintenance support, DSs providing electronic maintenance support, and RMs (Radiomen) providing support of the teletype mechanics.

If a problem exists in terms of obtaining adequate coverage for systems or equipment having multirating support, it is often caused by a failure to establish and maintain personal interrelationships between each rating involved. If a technician finds that he is unable to cope with problems because the support from other ratings is not there, then he should consider doing one of two things: (1) Either he can try to bridge the apparent gap himself, or (2) he can take the problem to his immediate senior and request that his senior attempt to resolve the apparent difficulty.

Most often, breakdowns in multirating support can be traced to simple things, like a breakdown in communications, when someone simply forgot to pass the word along, or a garble in the message that conveys the wrong meaning. Sometimes personal differences crop up and make mutual support difficult, but a good

technician should learn to put personal differences aside and concentrate on the job at hand.

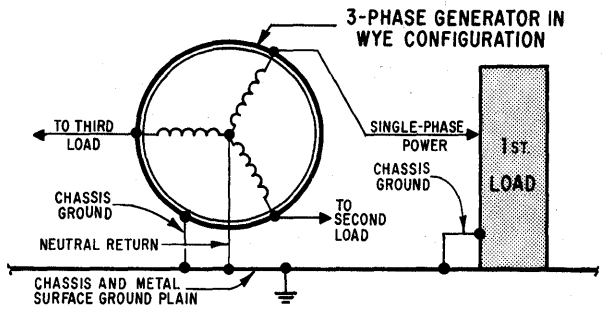
Technicians would do well to familiarize themselves with the basic functions and concepts of the other systems that they must depend upon. An increased familiarity means a better understanding of the problems being experienced with those systems, and a greater ability to provide assistance or to identify symptomatic effects in their own systems.

Input Power

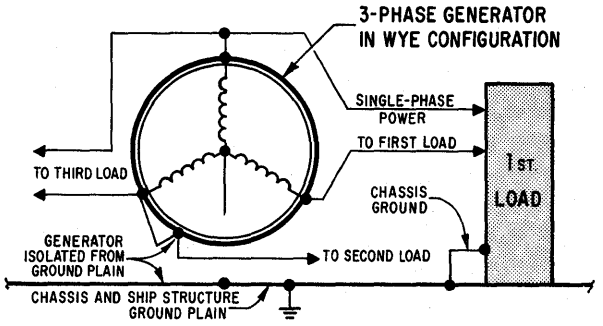
With the possible exception of motor generator sets and controllers, DSs generally have little responsibility for the electrical power system that provides power to their spaces and their equipment. As a consequence, many DSs are unaware of the electrical power system being used. This state of ignorance can have some tragic or otherwise undesirable consequences if a casualty occurs in the power supplied to a DS-maintained space.

ELECTRICAL SYSTEMS USED BY THE NAVY.—Basically, there are two electrical systems to be considered. The first system, which will be referred to as the shore system, is actually used at most shore sites (including commercial facilities) and in aircraft systems. This is the 3-phase 4-wire generator system (fig. 2-16) consisting of three windings, each having a different phase voltage developed across it; a neutral return, that potentially is midway between the three voltage phases and forms a common return; and a system ground. The voltage between the neutral return and ground is usually insignificant. In many installations, the two are made common by the method of installation and/or by combining them with common junctions in equipment used in the system. The shore system offers the advantage of two voltage potentials: the output across any two phases, and a second voltage across any single phase and the neutral return. Because the phase angle between any two windings is 120°, the 2-phase voltage is only 1.73 (2 x sin 120°) times the voltage of a single phase, rather than twice the single phase voltage as might be expected.

The second system, referred to here as the shipboard system, consists of a 3-wire isolated ground generator system (fig. 2-16). It does not use a neutral return, and the ground consists of grounding all the external metal surfaces in the installation together with the exception of the generator. The generator itself is isolated (insulated) from the system ground. Since there is no neutral return and the ground does not provide a return path for current flow, the system is regarded as less likely to suffer a severe casualty when compared to the shore system.



A. 3-PHASE, 4-WIRE GENERATOR SYSTEM PROVIDING NEUTRAL RETURN (Shore Installations and Aircraft).



B. 3-PHASE ISOLATED GROUND SYSTEM FOR SHIPBOARD USE.

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Figure 2-16.—Shore and Shipboard Generator Systems.

Note that the problems between shore system and shipboard system equipment are one way. Common neutral-ground shore equipment cannot be used safely aboard ships, but shipboard-approved equipment can be used without restrictions in a grounded shore installation. Also note that in some older sites, receptacles were used without a ground connection, and that any 3-prong device can be safely used in a 2-prong receptacle only with an approved ground adapter, and that the ground

wire must be properly grounded to the receptacle before the 3-prong plug is inserted. The grounding pin should never be removed from a 3-prong plug in order to permit its use in a 2-prong receptacle. For additional safety, electrical safety mats or seamless linoleum floors are used in electrical spaces immediately around the electrical equipment to reduce hazards to personnel. These should not be removed without proper authorization, and should be in position whenever the equipment is worked on.

In addition to safety considerations, the DS should be familiar with input power since he may be tasked to provide support to at least one element of the system—the MG/controller set that converts 60 Hz to 400 Hz in many system environments. A discussion of MG/controller sets follows in the next section.

60-HZ VS. 400-HZ INPUT POWER.—A large percentage of the militarized equipment supported by DSs utilize 120 V a.c. or 240 V a.c. at 400 Hz instead of the more conventional 60 Hz. The 400 Hz offers an advantage over 60 Hz, in that the power supplies in individual equipment for converting a.c. to d.c. can be made much smaller, while retaining the same power capacity. It can be demonstrated that an increase in frequency would require a corresponding decrease in the size of many components. (Smaller values of L, C, or mutual inductance can be shown to be a function of smaller component size, as well as other factors.)

It is worth noting at this point that transformers are designed to function properly at certain frequencies or frequency ranges, and that power transformers intended for 60-Hz applications, as an example, would not normally be used at 400 Hz, or vice versa. Also, power supplies intended for use at one frequency are not suitable for use at a significantly lower frequency, since in most cases this will result in poor filtering of the lower frequency ripple.

CONVERTING 60 HZ to 400 HZ.—A transformer can be used for converting one a.c. voltage level to another. A delta-Y transformer

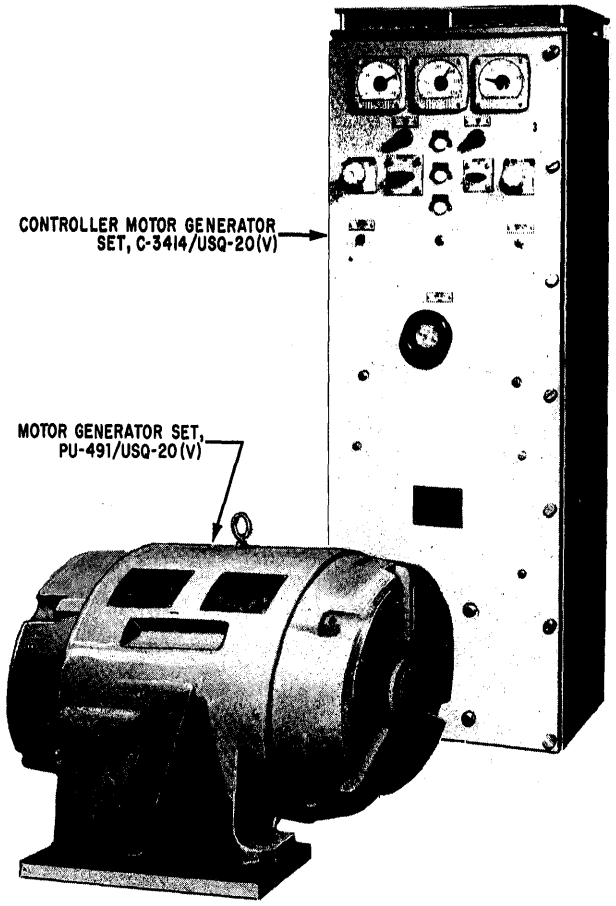

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Figure 2-17.—Typical MG (Motor Generator) Set.

can be used to alternate between 3-phase and single-phase power. Single-phase power can even be taken directly across two phases of a 3-phase source. Frequency multiplication, however, cannot be achieved by any of these means. A stabilized oscillator-controlled amplifier circuit can convert d.c. to some a.c. frequency for small and medium sized power supplies.

Recent advances in solid-state physics and fabrication technology have resulted in static frequency converters that have no moving mechanical parts. In the recent past the only widespread means of obtaining frequency multiplication within a large scale system involved a motor generator (MG) set, consisting of a 60-Hz motor and a 400-Hz generator, and a

controller to regulate the voltage and frequency output (fig. 2-17). The use of MG sets is widespread in the Navy at present, although newer installations are gradually seeing more and more of the static frequency converters. It can be anticipated that the Navy will continue to rely upon the existing MG sets for some years, while gradually phasing in newer equipment intended for the same purpose.

Basically, an MG set is an electro-mechanical device which consists of a 60-Hz motor connected to a 400-Hz generator by a single shaft. An MG set controller serves as a governor and can vary the applied voltage to hold the 400-Hz output fairly constant despite changes in the load. The controller also provides over- and under-voltage protection for the set. The motor-generator arrangement has been designed into one housing, and the windings for the motor may be wound about the same armature as the windings for the generator. Continued advances in the design have resulted in a smaller unit of greater efficiency. One type of MG set employs brushes, since the design requires the 400 Hz to be taken from the generator wound on the armature shaft.

Another type of MG is brushless since its generator field effect is produced on the armature, and the voltage developed is available from the case windings. The DSs provide operator-type maintenance, such as those tasks assigned by PMS, on the MG sets used with their systems, while the EMs have the responsibility, (in most cases), for corrective maintenance. However, this arrangement may not always hold true, and sometimes the DSs are also tasked with corrective maintenance for their MG sets and controllers. Extensive repairs usually involve assistance from a repair facility. The group having corrective maintenance responsibilities act as coordinators in obtaining the needed assistance.

Cooling

Another aspect of the various systems and equipment covered in this text is cooling. Electronic circuits, both tube and solid-state, consume electrical power and produce heat as a byproduct. Solid-state devices consume less energy and produce less heat as a general rule, but this feature is offset by utilizing higher circuit densities in solid-state technology, or using solid-state devices in power applications. The life span and performance characteristics of tube and solid-state circuits are altered in unfavorable ways when they are exposed to excessive heat.

The two most common ways of cooling equipment are: (1) forced air cooling, and (2) water cooling. Fans provide forced air cooling, and the equipment is designed for maximum ventilation possible in the space allowed. Air filters are required in most forced air applications in order to remove airborne contaminants. Many electronic components are sealed away from contaminants, but a thick dust buildup in the equipment is harmful, since this will insulate the surfaces it covers and prevent heat from radiating away properly. Even the use of filters presents problems, since they retain the airborne contaminants. This will eventually result in the filters becoming clogged, and cause a reduction of air flow in the equipment. This is resolved by frequent inspection, cleaning, and replacement of the filter elements.

Water cooling may be accompanied by forced air cooling. However, water cooling is extremely effective in a properly designed and maintained system.

CHILL WATER SYSTEMS.–Chilled water is used in water cooled equipment. Heat transfers are accomplished through large tubing coils called heat exchangers. The heat is drawn off from the coil by chilled water being pumped around the coils.

Some of the equipment is designed to be either air cooled or water cooled. An RD-270(V) magnetic tape unit, for instance, may be air cooled in one installation and water cooled in another installation. The two may function the same, but the maintenance requirements differ slightly.

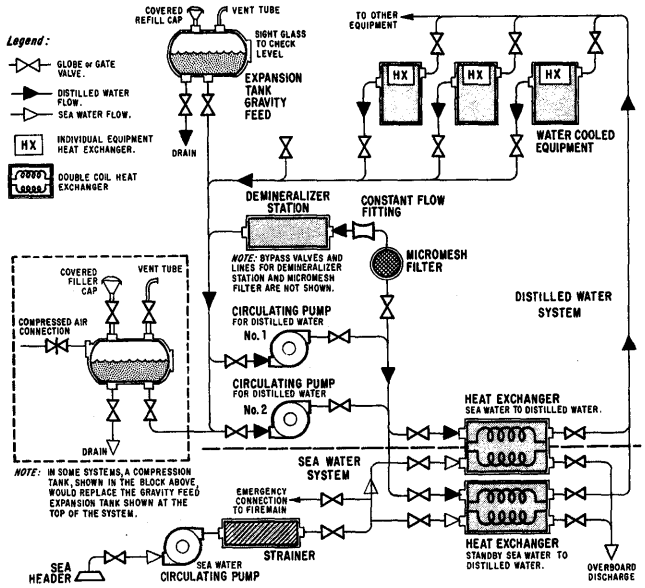

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Figure 2-18.–Simplified Shipboard Chilled Water System.

Refer to figure 2-18. Each water cooled device has a built-in heat exchanger through which the chilled water circulates in the equipment. Two water lines connect the heat exchanger in the equipment into the chilled water system. Where these lines must connect to the device, the use of a high pressure flexible hose with a quick-disconnect coupler is required. Rigid lines would not survive the vibration and shock each device must be capable of enduring. Many devices are shock mounted, which allows more independent movement in the device.

One water line acts as a chilled water inlet; the other line is a return line for the warm water. Each line should have a handvalve to secure water flow to the equipment. These valves should remain open except when water is leaking in the equipment, or the quick-disconnect hoses are being replaced. The power to the equipment will normally be shut off to prevent overheating when the chilled water connected to it is secured–unless an emergency condition exists which warrants risking an overtemperature condition in the equipment.

The water used in the secondary portion of the chilled water system (the portion actually connected to equipment) is supposed to be distilled or demineralized. This helps prevent metal corrosion in the cooling system, and helps prevent a reduction in the cooling system efficiency that would be caused by a restricted water flow in the tubing, or a loss of heat transferability, either of which could result from a coating buildup in the lines of the system. Despite reasonable care, some contaminants will enter the system anyway.

In order to remove foreign material from contaminated water, it is necessary to filter out the material in suspension, and then break the chemical bonds that hold some of the material in solution. In order to do this, the water is circulated through a filter trap, and then run through a demineralizer. Both of these units are usually located at the lowest point of the chilled water system, on the theory that the foreign material will eventually work its way to the system's low point. The lowest point in the system is also likely to be the point where the heat exchangers and the water pumps are located in order to chill and circulate the water. The heat exchangers, pumps, filter trap, and demineralizer, along with various gauges, valves, switches, and control mechanisms, will probably be situated in a single space marked Pump Room.

The chilled water system uses an extremely tight mesh filter referred to as a micromesh filter. This makes it possible for even the smallest particle to be trapped and removed from the system. The filter trap is actually situated in an arterial line of the system that parallels the main recirculatory route. Once the

filter has removed enough suspended material to severely restrict the flow in this branch line, it is necessary to replace the filter. This process must be repeated and repeated, until the flow meters indicate that the water in the system has been reasonably cleared of all suspended particles. It will be necessary to periodically check the flow meters and the filter, and to replace the filter as necessary.

The demineralizer is capable of testing the water to see approximately how much mineral content is present. The tester may operate by measuring the specific resistance of a given quantity of water. Water, in its purest state, is a good nonconductor with a very high resistive value. However, as more and more mineral content is found in it, its resistive value drops, and it can even reach a point of being a good conductor.

The demineralizer itself may use electrolysis, chemicals, or some other technique for separating the mineral content of the water from the water solution. The DS may or may not have PMS responsibilities in these areas.

The primary side of the cooling system provides all cooling aboard ship, from refrigeration to air conditioning. It can easily be overextended in tropical climates when the ship is moored or anchored in shallow, stagnant waters. It may also suffer when strainers become clogged, caused by water pollution, and be forced to reduce suction or even to shut down. This often makes it necessary to shut down nonessential equipment (both air and water cooled) to reduce cooling requirements, and to secure some of the air conditioning. These steps are usually not necessary until the ship berths, moors, or anchors. Cooling that should continue would be for refrigeration and for essential equipment, such as NTDS, communications, and navigational aids.

There may be several secondary chilled water systems. One system may cover several different electronic system areas. The responsibility for maintaining the secondary systems is usually placed on maintenance personnel in one of the electronic rates (this includes DSs). Personnel responsible for a secondary chilled water system must know what equipment/systems/ratings are affected by a change in chilled water status.

Water contracts and expands with changes in temperature. As the average temperature in the closed loop of the secondary chilled water system varies, so does the volume of water required in the system. This problem is resolved by the use of an expansion tank mounted above the highest point of the chilled water system. If the average temperature increases, the overflow expands into this tank. If the temperature falls, additional water is drawn from the expansion tank.

If leaks exist in the chilled water system, they will be apparent from a steady decline of water in the expansion tank. If the water level in the expansion tank falls too low, air will enter the chilled water system. Air in the chilled water system will cause surging in the pumps and motors, loss of cooling efficiency, and may result in damage to the system. More distilled water must be added to the expansion tank to prevent this from occurring. A careful monitoring of the chilled water system is essential, and a sufficient quantity of distilled water must be kept on hand for this purpose.

A leak in the equipment can be potentially dangerous due to the electrical power involved. If an equipment leak is suspected, power to the equipment must be secured at or before the point where it enters the equipment, and not simply secured at the front panel. The leak must be fixed and the equipment thoroughly dried before power can be restored. Fortunately, the use of distilled and demineralized water in the system significantly reduces the possibility of extensive damage from corrosion. If false decks (one deck placed over another with a gap between) are used in water-cooled spaces, the possibility of a hidden leak between the decks must be considered and searched for if a water loss is found in the system. It is very important to know the equipment, systems, and spaces where that secondary system is involved in order to isolate leaks.

The maintenance technicians utilizing chilled water cooling in their equipment must be familiar with indicators used with the chilled

water system. These include temperature gauges, flow meters, water purity testers, various automated alarms, and backup systems. They must verify alarm conditions, reset and test alarm circuits, and perform normal maintenance on the chilled water system, including isolating leaks, replacing defective hoses, evaluating meter readings, checking water purity, replacing the micromesh filters, and adding distilled water to the system as required.

CHAPTER 3

TEST EQUIPMENT

In this chapter representative general purpose test equipment, such as oscilloscopes, meters, counters, and transistor testers, will be discussed. This equipment will be described as to its general characteristics, including primary operating controls, with details of the simplified block diagrams.

Shipboard test equipment aids in the analysis of system, unit, circuit, and component performance by permitting measurements which may be compared with manufacturer's established standards. Equipment allowances are based upon providing each ship enough test equipment with a wide enough capability to correct most shipboard maintenance problems.

TEST EQUIPMENT MAINTENANCE

Since test equipment is designed to meet precise standards, its maintenance is generally more critical than that of other equipment. Most ships will have only limited capability for comparing test equipment to precision standards. This limited capability should not be used as a license to neglect proper maintenance of test equipment.

Where no precision measurement capability is involved, the obvious mechanical problems should be taken care of as a matter of routine. Defective test leads, power cables, knobs, lamps, blower motors, hardware and internal batteries can and should be replaced or repaired as needed. Certain test equipment circuits not directly affecting precision measurements, such as mechanical switching and some types of amplifiers, can be repaired with simple test equipment.

Where precision measurement capability is affected, shipboard maintenance responsibility usually is limited to determining the state of the test equipment. This may be done by comparing one equipment with another of equal or greater accuracy; for example, oscilloscopes may be compared against signal generators or frequency standards. Another alternative is to check test equipment against a "standard" whose value can be respected as accurate, such as comparing a series of ohmmeter readings against a selection of precision resistors.

Once malfunctions have been determined, the precision measuring instruments are normally turned over to a calibration facility for repair and calibration. The procedures for getting a piece of test equipment repaired vary depending on the ship's type command. One rule that should be followed prior to turning in test equipment is that the equipment should be thoroughly cleaned, including air filters, and hardware discrepancies (missing handles, knobs, etc.) should be corrected.

TEST EQUIPMENT SAFETY PRECAUTIONS

Some test equipment employs voltages of lethal potential. This may be true even for equipment using batteries for primary power, particularly if a d.c.-to-d.c. converter is used. Test equipment which employs cathode-ray tubes may use internal potentials on the order of 15,000 volts or more. Even in those cases where the current capability of the voltage source is not sufficient to be injurious in itself, the reflex action of the technician on being shocked may cause him to jerk away and injure himself.

Safety precautions, as set forth in Section 3 of the General EIMB (NAVSEA 0967-000-0100), should always be observed.

While test instruments can be expected to give reasonably accurate results under almost any conditions in which they are likely to be used, certain precautions, in addition to those to protect the instrument, are necessary. A few of the major precautions are listed here:

1. Instruments should not be used in proximity to transformers, generators, magnetic tubes such as magnetrons, and any conductors of heavy current in order to avoid errors from stray magnetic fields.
2. To obtain the most accurate results, instruments should always be used in the position in which they would normally be calibrated. Portable instruments are usually calibrated with the scale in a horizontal plane and panel types in the position in which they will be installed.
3. Never use an instrument which sticks at any part of its scale or which has a zeroing error.
4. Avoid parallax errors when taking readings. Some instruments have a scale mirror and, when the pointer and the image are in alignment, readings should be free of parallax.
5. As most measuring instruments are calibrated for a particular job, the accompanying instruction sheets should be consulted whenever any doubt arises about their use.

Test equipment, particularly portable test equipment, is often subjected to adverse operating and storage conditions. Most military test equipment is fitted with protective cases, but ruggedness may conflict with accuracy and portability. Therefore, when handling or stowing test equipment, do not be misled by the size and appearance of the carrying case. (Test equipment should be treated with the respect due a delicate instrument if confidence in its accuracy is to be retained.)

Sometimes large test equipment is provided with blower motors. Air filters or screens for the blowers should be kept clean, and protective covers for ventilation ports, if any, should be kept open and unobstructed while the test equipment is in use.

Use of a test equipment probe with equipment other than that for which it was designed may result in considerable error. It should be noted that there are 1:1, 10:1, 50:1, and 100:1 probes available. As an example, a 10:1 probe utilizes a lead-in resistor with a value 9 times higher than the input impedance of the test equipment, thus acting as a voltage divider to reduce the input signal to 1/10th its original value. Any difference in the internal impedance of the probe and input circuits of the equipment prohibits substitution without calibration. An adjustable capacitive "shunt" is built into some probes to provide a high frequency bypass when necessary to prevent input signal waveform distortion.

Test probes which are not designed for specific test equipment should not be used with that equipment, because they may not have sufficient capacitive adjustment to preserve the waveshape of the observed signal. A sound rule is to use all test probes only with the equipment for which they were designed.

USE OF SHORTING BAR ON ELECTRONIC TEST INSTRUMENTS

The following applies specifically to the Fluke Differential Voltmeters; however, it is generally applicable to all test instruments with grounding bars (fig. 3-1).

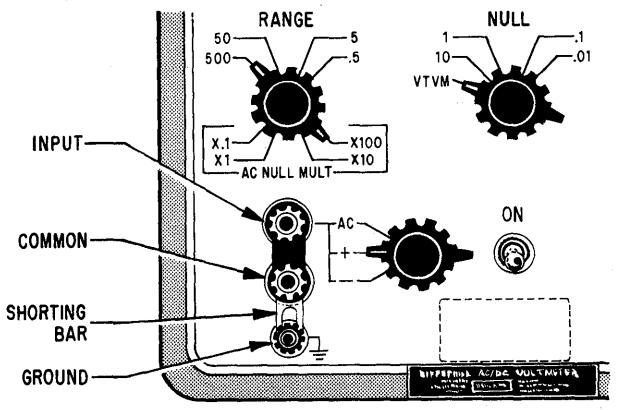

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Figure 3-1.–Fluke differential voltmeter.

The Fluke Differential Voltmeter series instruments are equipped with a three-wire line cord, the ground wire being connected directly to the chassis. Therefore, the ground post of these meters is connected directly to Earth ground potential whenever the three-wire line cord is properly mated with a properly grounded a.c. power receptacle. For this reason it is imperative that personnel using these meters check for conflicts in grounding before connecting the common side of the input to the ground binding post with the shorting bar.

The following procedures should be followed when making voltage measurements with these types of test equipment.

When To Use
The Shorting Bar

The shorting bar should be connected across the common and ground post (fig. 3-1) when the meter is being used to measure voltages in equipment having the chassis as the common ground. This practice eliminates the possibility of personnel coming between a grounded and an ungrounded chassis.

NOTE

PARTICULAR CARE SHOULD BE EXERCISED WHEN TAKING MEASUREMENTS ON EQUIPMENT HAVING A TWO-PRONG POWER CONNECTION PLUG. TWO-PRONG PLUGS ARE NOT AUTHORIZED FOR SHIPBOARD USE.

When checking equipment that uses a two-prong power cord, only the test lead connected to the input terminal of the differential voltmeter should be connected to the chassis of the equipment. Energize the equipment to be measured. If the meter reads line voltage, the plug of the equipment should be reversed. The lead attached to the common and ground terminal of the differential voltmeter should then be connected to the chassis of the equipment. Proceed with subsequent measurements; if no line voltage is measured after energizing the equipment, leave the plug inserted as it is, and connect the common and ground lead of the differential voltmeter to the equipment chassis. Proceed with measurements.

When Not To Use
The Shorting Bar

The shorting bar should not be connected to the common terminal when making the measurements described as follows:

1. When measuring voltages in an equipment having a B minus common ground line. Connection of this B minus ground line with the ground terminal will result in damage to the equipment being tested and possible injury to personnel.
2. When measuring a.c. potentials having both sides of the line "hot" with respect to ground.
3. When measuring signal levels below a few millivolts. This prevents the flow of ground currents in the test leads which would cause an error in the desired reading.
4. When measuring any power line voltage.

PERSONNEL SAFETY PRECAUTIONS

The following personnel safety rules should always be followed when making test measurements:

(1) MAKE SURE you are NOT GROUNDED whenever you are adjusting equipment or measuring equipment.

(2) In general, USE ONE HAND only when servicing live equipment.

(3) If test meter must be held or adjusted while voltage is applied, GROUND the case of the meter before starting measurement, and DO NOT touch the live equipment or personnel working on live equipment while you are holding the meter. Some moving vane type meters should not be grounded. These should not be held during measurements.

(4) DO NOT FORGET that high voltages MAY BE PRESENT across terminals that are normally low voltage, due to equipment

breakdown. Be careful even when measuring low voltages.

(5) DO NOT use test equipment known to be in poor condition.

(6) High-voltage high-capacity capacitors should be discharged with a grounding probe. Where neither terminal of a capacitor is grounded, short capacitor terminals to each other after securing power.

APPLICATION OF TEST EQUIPMENT

As a technician, you may be required to put new equipment into operation, perform preventive maintenance, or take corrective measures to repair faulty equipment. There are many types of simple and complex test equipment to help do these jobs efficiently.

When breakdowns occur, proper use of available test equipment allows technicians to check voltages, currents, or frequencies to align or repair equipment quickly. This test equipment includes multimeters, electronic voltmeters, oscilloscopes, transistor checkers, module test sets, electronic counters and similar devices. Portable test equipment will be discussed in this chapter. The module test sets are described in applicable chapters.

Personnel safety hazards, maintenance hints, and other information on specific test equipment models are contained in the Test Equipment Handbook of the EIMB. You should ensure that you become familiar with both this handbook and the EIB, which frequently contains information on test equipment use.

OSCILLOSCOPES

The cathode-ray oscilloscope is an instrument which allows the technician to observe waveforms in testing electronic circuits. If voltage waveforms are to be observed, an ELECTROSTATIC cathode-ray tube (CRT), which employs voltage to deflect the electron beam, is used.

Some oscilloscopes may use an ELECTROMAGNETIC CRT, which employs current to deflect the electron beam. This type of oscilloscope is used for special applications, other than general testing, where its properties make it more suitable than the electrostatic-deflection type.

The electrostatic-deflection cathode-ray oscilloscope is one of the most useful and versatile of test instruments. It is essentially a device for displaying graphs of rapidly changing voltages, but it is also capable of giving information concerning frequency values, phase differences, and voltage amplitude. It is used to localize sources of distortion by tracing signals through electronic circuits, and to isolate troubles to particular stages in equipment.

The construction features of the CRT, its operation, and circuitry of an elementary oscilloscope are discussed in detail in *Basic Electronics, Volume 2,* NAVEDTRA 10087-C (or Navy Electricity-Electronics Training Series (NEETS), applicable module.) Review this book if you are in doubt as to the operation of an elementary oscilloscope.

Oscilloscopes are used to produce a graphical display of simple and complex voltage variations which contain frequency components ranging from zero to 50 MHz. To simplify operation and the interpretation of the display, the instrument provides calibrated vertical sensitivities, triggered internal sweeps, calibrated sweep times, beam position indicators and a calibrator.

Most oscilloscopes consist of a major unit and any one of several plug-in units. The major unit contains the power supplies, horizontal amplifier, sweep generator, main vertical amplifier, CRT, calibrator, and the controls associated with these circuits. The plug-in units are single-channel, multichannel, or special feature preamplifiers to the main vertical amplifier and are selected depending on the display desired; e.g., a multichannel plug-in unit provides two separate traces on the CRT and thus allows two functions to be displayed simultaneously. An instruction manual is provided with each plug-in unit that gives detailed instructions for operating that specific plug-in unit in conjunction with the oscilloscope.

The voltage or current waveform is normally represented in a graphically displayed two-dimensional (horizontal and vertical) plane with no depth involved. The horizontal (X) axis

on the oscilloscope will represent elapsed time or waveform duration in either whole or parts of a second. The vertical (Y) axis will represent amplitude, quantity, or intensity of the subject waveform in either whole or parts of volts or amperes. Any portion of the waveform extending above the present horizontal (zero amplitude) reference line is considered positive, while any portion below the horizontal reference line is considered negative.

When analyzing and interpreting any waveform on the screen of a cathode-ray tube, bear in mind that the unknown signal is always plotted as a function of another signal whose characteristics are known.

The calibrated scale (graticule) of the CRT is accurately marked with horizontal and vertical 1-centimeter divisions, with 2-millimeter graduations on both the center horizontal and the center vertical lines. To obtain a useful display, it is necessary for the spot to be deflected horizontally at a known rate so that any horizontal distance on the calibrated scale represents a definite, known period of time. The trace formed by the deflection of the spot across the CRT is known as the horizontal sweep. Since the horizontal deflection of the spot bears a definite relationship to time and provides the means for making time measurements, the horizontal sweep is also known as the time base. Newer oscilloscopes usually feature two independent time-base units: Time Base A and Time Base B. Either of the two time bases may be displayed on the oscilloscope screen at any time.

Linear Time Bases

In most oscilloscope applications, the unknown signal is applied to the vertical axis; the horizontal axis is used for the known function, the characteristics of which are usually linear with respect to time. When the horizontal sweep time base is adjusted to synchronize with the unknown signal applied to the vertical deflection plates, the time variation or waveform of that signal is traced upon the cathode-ray tube. It is advisable to manipulate the scope controls to obtain three complete periods of the waveform being inspected. This procedure would permit an inspection of the central portion of the display without making allowances and assumptions concerning signal extremities.

Nonlinear Time Bases

Nonlinear time bases are special types of sweeps that are usually limited to specialized engineering and research applications, except for the line sweep. The line sweep is normally available on most oscilloscopes. Circular, spiral, and radial sweeps generally require additional circuitry external to the oscilloscope.

Using time base signals in the form of sine waves allows an easy and accurate measurement of phase angles and frequency calibration of electronic equipment. The pattern obtained from the use of a horizontal sine wave time base to display another sine wave on the vertical axis is called Lissajous pattern.

Synchronizing

While it may be possible to obtain a stationary display of one or two signals on the screen by adjusting the sweep time control using internal sweep circuits, it does not mean the display will remain stationary indefinitely. Fluctuations in line voltages, sweep voltages, or test signal voltages, may cause the display to lose this synchronism.

In most oscilloscopes a method of locking the oscilloscope sweep generator to the frequency of the test signal solves this problem. A portion of the test signal is injected through an "external trigger in" jack and applied to the input of the sweep generator to synchronize or trigger the sweep at the test signal frequency.

Oscilloscope Safety Precautions

When using or maintaining oscilloscopes, it is advisable not to operate it with the case removed. Check the instruction manual for additional safety precautions or warnings such as

exposed high voltage points and areas where high voltage could exist if certain failures occur. Removing the case to check operation may not only expose voltages to cause fatal shock, but the reduced shielding of the instrument may also allow stray pickups from external fields to be amplified and displayed on the scope. This could lead to wasted time in troubleshooting sweep circuits for nonexisting problems.

Extreme caution should be used when handling cathode-ray tubes. The glass envelope encloses a high vacuum, and undue stresses or rough handling can cause serious injury due to tube implosion. When required to handle a broken cathode-ray tube, avoid contact with the internal fluorescent coating of the tube as it is extremely toxic.

Some oscilloscopes have a beam location control which stops the sweeps and permits a dot (spot), to appear on the screen. Horizontal and vertical front panel controls are used to center the spot; thus, the signal waveform to be observed will appear across the center of the screen. Do not turn the intensity of the scope to the brightest position (clockwise) when looking for the sweep or beam. The energy of the electron beam concentrated in a small area will burn the screen coating if the sweeping beam is slow or a spot remains in a stationary position.

Ensure that the oscilloscope and the equipment being tested are properly grounded. Common grounding is a good practice to eliminate electrical shock hazards between several different pieces of equipment and produce clear displays that are free of stray noise signals. When checking radiofrequency signals, the length of the ground lead can affect the oscilloscope displays as the inductive reactance factor of the ground lead may place the oscilloscope circuits above RF ground.

When dealing with circuits designed to operate above ground, use oscilloscopes that have the chassis isolated from the case, use caution during measurements, and break the connection as soon as the measurement is completed. Immediately replace any power cord or plug on which the ground wire or pin has been removed.

AN/USM-281A OSCILLOSCOPE

The AN/USM-281A Oscilloscope (fig. 3-2) is a direct coupled, wideband oscilloscope that provides a visual display of simple and complex waveforms. In addition to displaying waveforms, the oscilloscope provides the user with the capability of accurately measuring rise time of a waveform, waveform magnitude, time difference between any two points on a displayed waveform and accurate time comparison of two separate waveforms. The oscilloscope consists essentially of three operating units, the oscilloscope assembly mainframe, a Dual Trace plug-in unit and a Time Base and Delay plug-in unit.

OSCILLOSCOPE ASSEMBLY.—The oscilloscope assembly provides the circuitry (low voltage and high voltage power supplies) for projecting a beam onto the CRT screen and the controls to adjust intensity, focus and horizontal position of the beam on the CRT. This unit also contains a horizontal amplifier (with front-panel controls for accepting an internal or external signal) to amplify the selected time base signal and provide a linear deflection voltage to the horizontal plates of the CRT. The oscilloscope assembly also contains the power switch, scale illumination control and two calibrator output jacks.

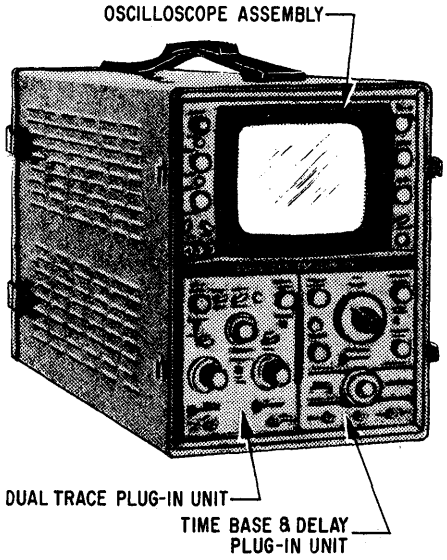

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Figure 3-2.—Oscilloscope AN/USM-281A.

TIME BASE AND DELAY GENERATOR.—This assembly generates the accurate main time base and delay time base voltages used for horizontal deflection during normal (internal) operation. Front panel controls provide a choice of four modes of operation; main sweep only, mixed sweep, delayed sweep and single sweep. With the sweep mode selected, the front panel controls provide a choice of 23 sweep speeds for the main sweep, and 18 sweep speeds for the delayed sweep. The time base assembly also provides controls for selecting automatic (free-running or triggered by a signal above 50 Hz) or triggered time base, trigger source, polarity, level, frequency range and a calibrated ten-turn control for precise measurement of the delay time to the start of the delayed sweep.

DUAL CHANNEL VERTICAL AMPLIFIER.—This plug-in unit permits observation of one waveform on either of two channels, or allows simultaneous viewing of two separate waveforms. For displaying two simultaneous waveforms the vertical amplifier provides two alternate sweep modes for viewing high speed traces and a chopped dual sweep for viewing slower displays. By selecting the desired alternate sweep mode, each trace can be triggered automatically from the combined channel input or by the B channel input signal only for accurate time comparison of the two input signals. In the chopped mode, the sweep is triggered automatically from the channel B input signal, and switching occurs at a 400 kHz rate. Automatic track blanking during switching time eliminates undesirable switching transients. The dual channel vertical amplifier also provides for combining two waveforms on one trace to produce the algebraic sum or difference of the two waveforms.

PRIMARY OPERATING CONTROLS

Refer to figure 3-3. The controls for the oscilloscope assembly are located on the upper half of the oscilloscope. The HORIZONTAL POSITION control is made up of two knobs, one for fine adjustment and the other for coarse. The MAGNIFIER switch determines the gain of the horizontal amplifier and is used to expand the trace. The DISPLAY switch determines which time base signal is applied to the horizontal amplifier. The INT position selects the internal time base; the EXT CAL position connects the HORIZONTAL amplifier input to the EXT INPUT connector, and the EXT SENS position connects the horizontal amplifier input to the EXT INPUT connector through a variable resistor. The a.c.-d.c. switch determines the type of coupling for an external signal. The other controls on the left of the oscilloscope assembly such as INTENSITY and FOCUS are self-explanatory.

The controls for the time base and delay generator are found on the lower right portion of figure 3-3. The SWEEP MODE switch is used to determine the type of main sweep operation. In the NORM position, it provides a sweep only when a trigger signal is present. In the AUTO position it provides a free running sweep when no trigger is present or a triggered sweep if a trigger signal greater than 50 Hz is present. This is the normal operating position for the AN/USM-281A (check operating instructions for other oscilloscopes). The SINGLE position provides only one sweep when triggered. The MAIN VERNIER and DELAYED VERNIER are fine adjustments for the main and delayed sweep speeds. The main TIME/DIV switch selects the main sweep speed. The TRIGGER LEVEL controls determine the voltage level of the input waveform at which the main or delayed sweep will be triggered. The DELAY (DIV) control is used with the main TIME/DIV switch to determine the delay time before the start of the delayed time base. The delay time is the product of the setting of these two controls.

The Dual Trace amplifier controls are found on the lower left portion of figure 3-3. The A POSITION and B POSITION controls determine the position of the A and B sweep in the vertical plane. The DISPLAY switch selects the type of vertical display to be used. There are six different displays available which use either the A or B displays or combinations of both. The VOLTS/DIV controls consist of a switch and variable resistor to control the calibrated input attenuation for both channel A and B amplifiers.

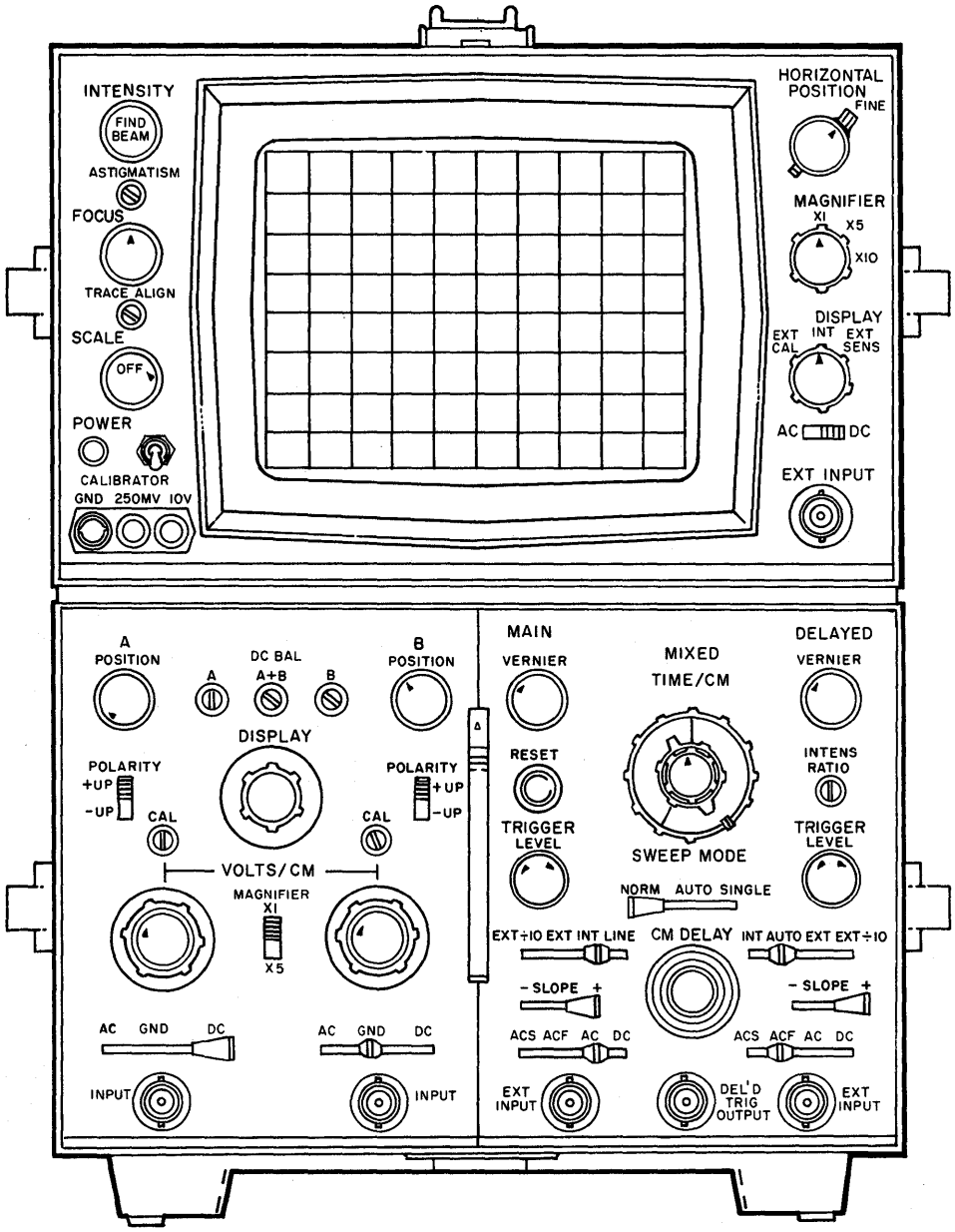

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Figure 3-3.–AN/USM-281A, front panel.

The input voltage is determined by multiplying the number of divisions displayed on the graticule by the setting of the switch. The VERTICAL MAGNIFIER switch is used to expand the vertical trace. The POLARITY switches select the polarity of the vertical display. In the +UP position, the positive portion of the input waveform will be up; in the -UP position the negative portion will be up. For a more detailed explanation of these and the other controls for the AN/USM-281A, refer to the *Operator's Manual* 0969-125-0120.

OVERALL FUNCTIONAL DESCRIPTION

The oscilloscope requires three signals to produce a usable display on the CRT. These are intensity, horizontal deflection, and vertical deflection. Refer to figure 3-4. The circuitry for producing intensity is included in the oscilloscope assembly and consists of the low and high voltage supplies and the gate amplifier. The circuitry for producing internal horizontal deflection consists of the horizontal amplifier contained in the oscilloscope assembly; and the internal trigger amplifier, main and delayed trigger generators, and main and delayed sweep generators located in the time base and delay generator. The oscilloscope assembly also contains a horizontal preamplifier for accepting external horizontal deflection signals. The circuitry for producing vertical deflection is located in the dual channel vertical amplifier and consists of a channel A and B attenuator and preamplifier, a channel A and B input amplifier and gate control, a main amplifier, a multivibrator, and a sync amplifier.

HORIZONTAL AMPLIFIER.—The horizontal amplifier section (includes horizontal preamplifier) accepts an external or internal time base signal and amplifies the signal to the voltage level required to produce the horizontal displacement of the CRT beam.

GATE AMPLIFIER.—The gate amplifier accepts an unblanking gate signal from the time base and delay generator (during internal operation), a chopped blanking signal from the dual channel vertical amplifier (during chopped mode), and a Z-AXIS signal (when applied from an external source). A Z-AXIS signal is a special signal used to modulate the CRT beam intensity. This signal is applied to the Z-AXIS connector on the rear panel of the oscilloscope. These signals are averaged and amplified by the gate amplifier, and the output is applied through the high voltage supply to the control grid of the CRT. This control signal causes the CRT beam to be cut off during retrace, during switching when operating in the dual channel chopped mode and produces intensity modulation of the CRT beam when a Z-AXIS input is applied.

CALIBRATOR.—The calibrator is a free-running multivibrator that oscillates at a 1 kHz frequency and provides a square wave output to the front-panel connectors. The calibrator outputs are useful in adjusting and troubleshooting the oscilloscope. The calibrator has no internal function.

MAIN AND DELAYED SWEEP AND MAIN AND DELAYED GATE OUTPUT AMPLIFIERS.—These four amplifiers are single-stage, emitter-follower amplifiers that accept the main sweep, main gate, delayed sweep, and delayed gate signals and provide a low impedance output to four rear-panel connectors. These amplifiers have no internal function.

DUAL CHANNEL VERTICAL AMPLIFIERS AND ATTENUATORS.—This section includes the A and B input attenuators and preamplifiers, A and B amplifiers and gate control, delay line, and the output amplifier. Each input attenuator provides 12 levels of compensated attenuation and applies a reduced signal to its respective input amplifier (includes preamps). The input amplifiers convert each input to a differential signal and apply an amplified output signal through a gate control circuit and delay line to the output amplifier. The gate control circuit is controlled by the multivibrator and (depending on the setting of the vertical DISPLAY switch) determines which signal (channel A and/or channel B) is applied to the output amplifier. The delay line delays the signal 160 nsec to allow the internal trigger signal from the sync amplifier enough time to start the sweep. The output amplifier boosts the signal to the level necessary to drive the vertical deflection plates of the CRT.

MULTIVIBRATOR.—The multivibrator provides the control signal to the gate control circuit and determines which vertical channel is displayed. In the chopped mode of operation the multivibrator is free-running and switches at a 400 kHz rate to alternately switch the A and B channels on and off. In this mode the output of the multivibrator is also applied to a blanking amplifier to provide a blanking signal through

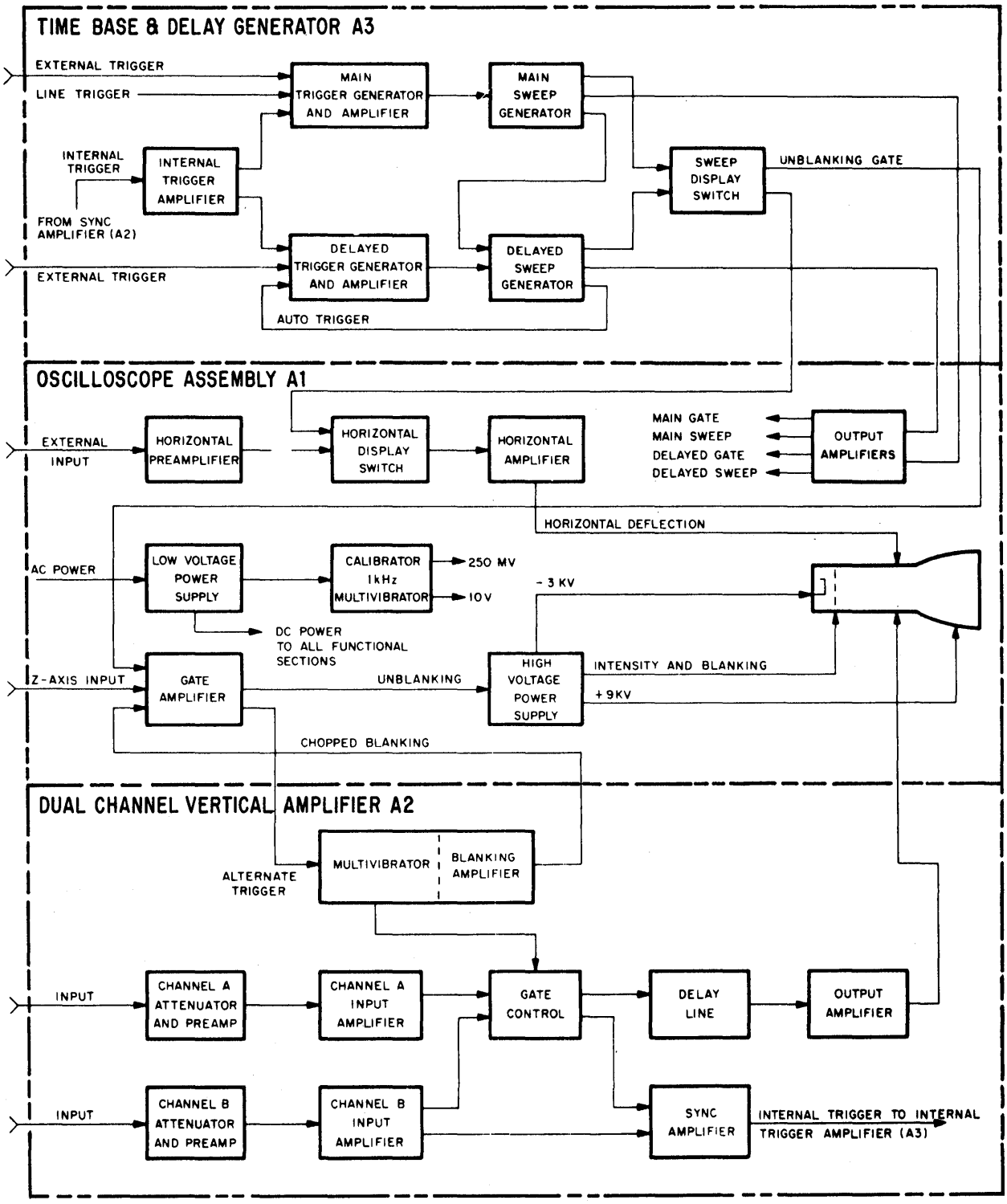

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Figure 3-4.—AN/USM-281A, functional block diagram.

the gate amplifier to the CRT during switching time. In the two alternate modes of operation, the multivibrator is bistable and switches only when triggered by the time base triggering signal (from the gate amplifier in the oscilloscope assembly). This causes the multivibrator to switch channels at the completion of each sweep. In the A+B mode of operation the multivibrator allows the outputs of both channels to pass through the gate control circuit and apply their combined output to the output amplifier.

SYNC AMPLIFIER.–The composite vertical signal from the gate control, and the signal from the channel B amplifier are applied to the sync amplifier. The sync amplifier (depending on the setting of the vertical DISPLAY switch) amplifies one of these input signals and converts it to a single-ended output. The output signal is coupled to the time base and delay generator where it may be used to trigger the sweep. In the ALT, A+B, A and B modes of operation, the composite vertical signal is amplified by the sync amplifier and coupled to the time base and delay generator. In the ALT B TRIGGER and CHOP B TRIGGER modes of operation the channel B signal is amplified by the sync amplifier and supplied to the time base and delay generator.

MAIN TRIGGER GENERATOR AND AMPLIFIER.–The main trigger generator (depending on the setting of the main trigger source switch) receives a trigger signal from an internal, external or line source. If the internal source is selected, the trigger signal from the sync amplifier is amplified and compared to the trigger level set by the trigger level control. The resultant output is a sharp negative trigger pulse to the main sweep generator. If the main trigger generator receives no input trigger while in the NORM or SINGLE mode, it produces no trigger output. In the AUTO mode, the trigger generator produces a trigger output in the absence of an incoming trigger signal.

MAIN SWEEP GENERATOR.–The main sweep generator consists of the main gate generator, the main integrator, a hold-off circuit and the main Schmitt Trigger (not shown in figure 3-4). When the main sweep generator receives trigger from the main trigger generator and amplifier, it produces a negative rectangular gate pulse. The gate pulse is applied to the sweep display switch, then to the gate amplifier in the oscilloscope assembly to unblank the CRT. At the same time, the main sweep generator produces a positive going sawtooth (sweep) voltage at a rate determined by the setting of the main TIME/DIV switch. This signal is applied through the sweep display switch (in the MAIN and MIXED modes) to the horizontal amplifier in the oscilloscope assembly to drive the horizontal deflection plates. Depending on the sweep length adjustment, the sweep output will switch and cut off when it reaches a preset level. After a delay, the circuits reset and return to a ready condition. The next trigger pulse then causes the sweep to repeat the cycle. In the SINGLE mode of operation, the gate can only be reset by pressing the RESET pushbutton.

DELAYED TRIGGER GENERATOR AND AMPLIFIER.–The delayed trigger generator and amplifier section receives a signal from an internal (INT), external (EXT) or AUTO source depending on the setting of the Delayed Trigger Source Switch. Whether the internal or external source is selected, the delayed trigger generator and amplifier amplifies the incoming trigger signal, compares it to the preset trigger level set by the delayed TRIGGER LEVEL control and produces a sharp negative output pulse to the delayed sweep generator. When the AUTO trigger source is selected, the delayed trigger generator section is disabled, and the delayed sweep generator returns a positive trigger pulse to the delayed trigger generator and amplifier section. This signal is then amplified and inverted to provide a negative trigger signal to the delayed sweep generator.

DELAYED SWEEP GENERATOR.–The delayed sweep generator consists of a delayed gate generator, a delayed integrator, a sweep comparator and a delayed Schmitt trigger (these are not shown in fig. 3-4). The delayed sweep output is applied through the sweep display switch to the horizontal amplifier only in the MIXED and DELAYED sweep modes. In the MIXED mode both the main and delayed sweeps

are applied to the horizontal amplifier. In the DELAYED mode, only the delayed sweep is displayed. The main sweep signal is received and compared to a voltage level set by the DELAY (DIV) control. When the main sweep voltage exceeds the set level, a positive output pulse is provided to reset and enable the appropriate circuits in the delayed trigger generator and amplifier section. If the AUTO source is selected, a positive output pulse is provided to the delayed trigger generator and amplifier section as previously described. When the delayed trigger generator and amplifier circuits are enabled, the first trigger pulse starts the sweep cycle. The delayed sweep cycle is terminated when the sweep voltage reaches a predetermined level and switches the delayed trigger and amplifier section to the disabled gate condition.

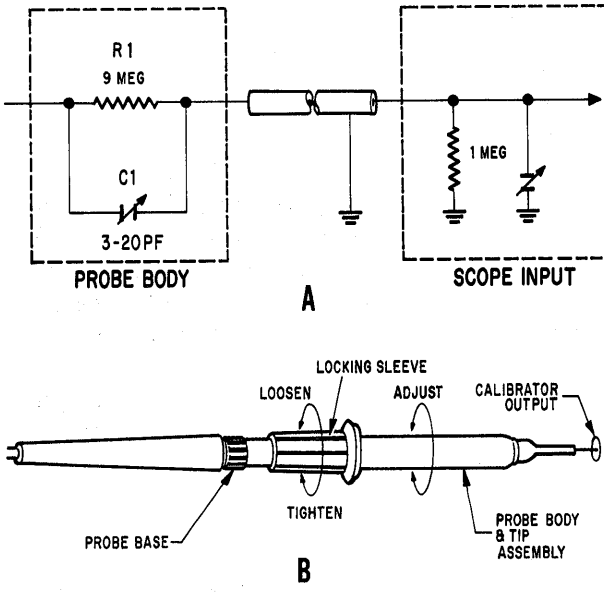
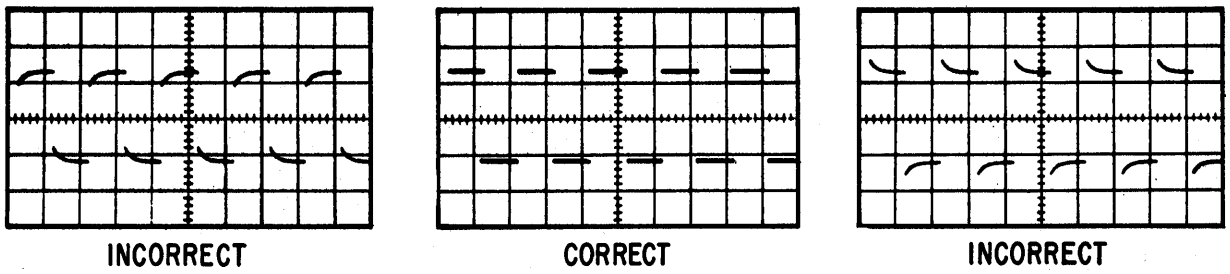


Figure 3-5.—A. Basic attenuation probe, B. Test probe compensation adjustment. 124.402

TEST PROBE COMPENSATION

The test probes normally used with the AN/USM-281A Oscilloscope are 10 to 1 attenuation types. The internal resistance of a 10:1 probe is nine times greater than the input resistance of the equipment. Thus, use of the probe provides a series voltage divider which has a total resistance 10 times greater than that of the input circuit without the probe connected. Additionally, the probe has a variable capacitance across its internal resistance which must be adjusted in order to accurately measure high frequency signals or fast rising waveforms. Figure 3-5A is a schematic diagram of a 10:1 probe, and it shows the probe body connected by a shielded wire to the input terminals of an oscilloscope.

To compensate the probe, touch the probe tip to the oscilloscope calibrator output connector and display several cycles of the signal on the CRT. Loosen the flanged locking sleeve several turns (fig. 3-5B). Adjust for the correct waveform by turning the probe body and tip assembly while holding the knurled section at the base of the probe. Figure 3-6 shows waveforms for a 1-kHz oscilloscope calibrator. After obtaining the correct waveform, hold the probe body and tip assembly and carefully tighten the locking sleeve. Make final adjustment



124.403

Figure 3-6.—Waveforms from 1-kHz oscilloscope calibrator.

by holding the locking sleeve and probe body while turning the probe base.

If you are not the last person to have used the probe, you should check the compensation prior to using the probe. The probe should also be compensated each time it is transferred to another oscilloscope or plug-in unit.

MULTIMETERS

During troubleshooting, a technician is often required to measure voltage, current, and resistance. To eliminate the necessity of obtaining three or more meters, the multimeter is used. The multimeter combines a voltmeter, ammeter, and ohmmeter in one unit. Multimeters are of the electronic and nonelectronic type and are discussed briefly in *Basic Electronics*, NAVEDTRA 10087-C (or Navy Electricity-Electronics Training Series (NEETS), applicable module.)

MULTIMETER AN/PSM-4

Multimeter AN/PSM-4 (fig. 3-7) is a portable, nonelectronic volt-ohm-milliammeter. It can be used to make d.c. current, d.c. resistance, and d.c., a.c., and output voltage measurements. The complete unit includes test probes which may be used with their prod tips, or the tips can be fitted with alligator clips or with a telephone plug to simplify contact arrangements and connections. A high voltage probe is also included, which makes it possible to read voltage up to 5,000V d.c. This probe contains a warning light to indicate the presence of high voltage.

Multimeter AN/PSM-4 is designed to make the following electrical measurements:

1. Direct currents up to 10 amperes
2. Resistances up to 30 megohms
3. D.C. voltages up to 5,000 volts
4. A.C. voltages up to 1,000 volts (RMS)
5. Output voltages up to 500 volts (RMS)

The following discussion and the associated block diagrams treat the general circuitry within the instrument part of the multimeter as it is arranged when used to measure voltage, current, or resistance.

D.C. Voltmeter Circuits

The block diagram of the circuit in Multimeter AN/PSM-4 which is used for measuring d.c. voltages is shown in figure 3-8. The circuit is selected with function switch S-101, in either its DIRECT or REVERSE DCV position (fig. 3-7). For voltages up through 500 volts, a range is selected with range switch S-102 (only one position shown in figure 3-8). For the 1000 volt range, the red test lead connects into the special 1000V d.c. jack (fig. 3-7), and the range switch is not in the circuit. For the 5000-volt range the high voltage probe (not shown) connects the special 5000V d.c. jack, and places its resistance in series with the meter movement. For any range, the total resistance in series with the meter movement will regulate the meter current to provide a proportional current to indicate the amount of voltage in the circuit.

A.C. and Output Voltage Circuit

The circuits which measure a.c. and output voltages (fig. 3-9), are selected with the ACV and OUTPUT positions of function switch S-101. For voltages up through 500 volts, a range is selected with range switch S-102. For the 1000 volt range, the red test lead connects the special 1000 VAC jack, and the range switch, S-102, is not in the circuit. The a.c. voltage impressed across the circuit between the red and black test lead tries to send current through the resistance of the circuit in both directions, but the rectifier allows only one direction of current flow through the meter movement. The meter is calibrated to indicate the RMS value of the a.c. voltage applied to the instrument circuit.

D.C. Current Circuits

The circuit which measures d.c. currents is selected with the DC μA MA AMPS position of

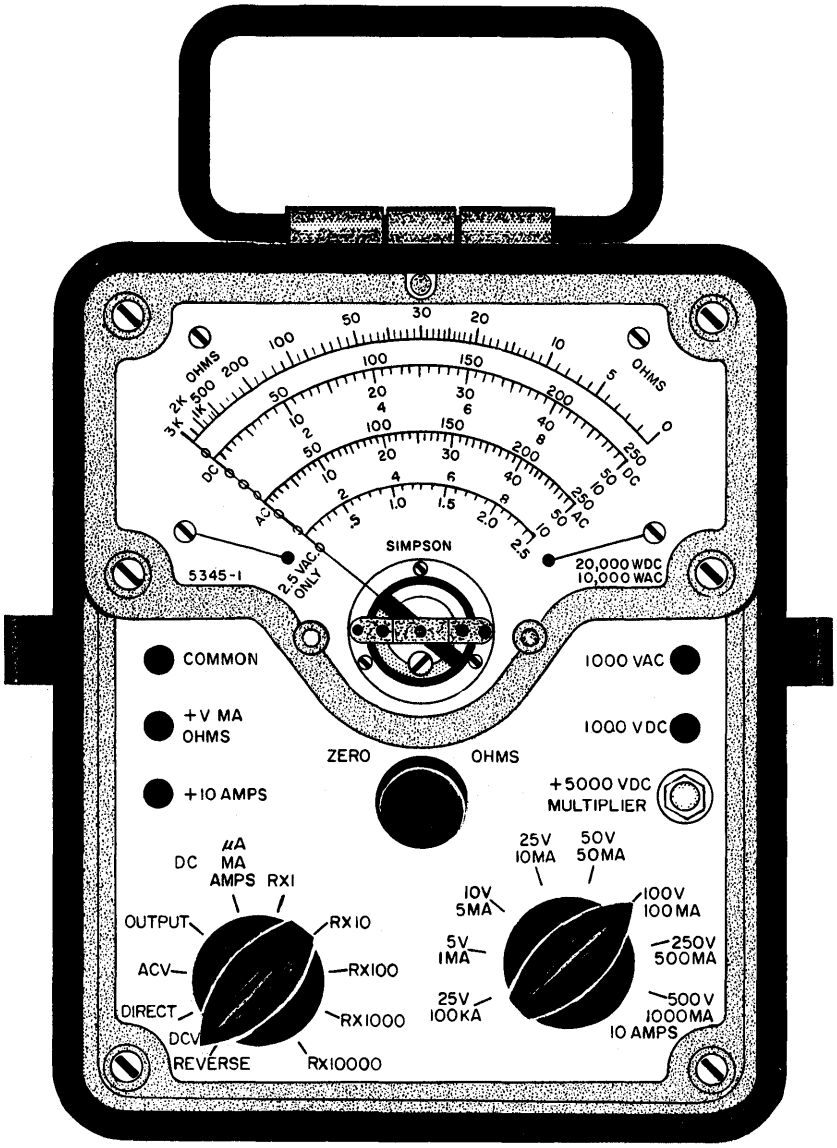


Figure 3-7.—AN/PSM-4 Multimeter, front panel. 4.133

function switch S-101 (fig. 3-7). For currents up to 1000 milliamperes, the range is selected with range switch S-102 (fig. 3-10). For the 10 ampere range, the red test lead connects the special 10 AMPS jack, and range switch S-102 is not in the circuit. Each range provides a parallel shunt resistance for the meter movement, and the circuit current divides between these two parallel paths. The proportional part which passes through the meter movement indicates the total circuit current.

Ohmmeter Circuits

The ohmmeter circuit (fig. 3-11) and its ranges are selected with function switch S-101. The ranges are Rx1, Rx10, Rx1000, and Rx10000. An internal battery furnishes the power for all resistance measurements. For each range, the circuit is arranged so the meter will indicate zero ohms, and full scale deflection when the red test lead and the black test lead are shorted together. When you connect a resistance between the test

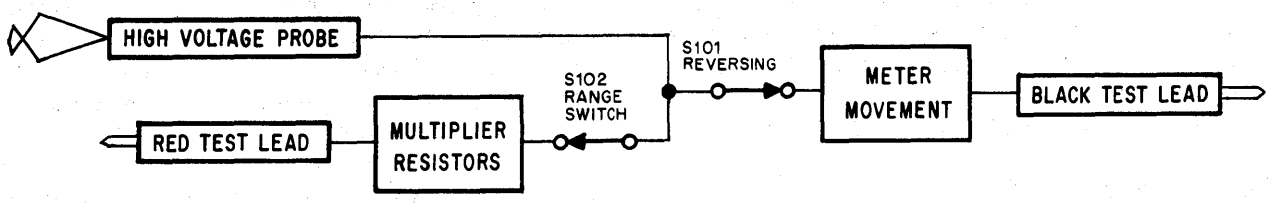


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Figure 3-8.--Functional block diagram of d.c. voltage circuits.

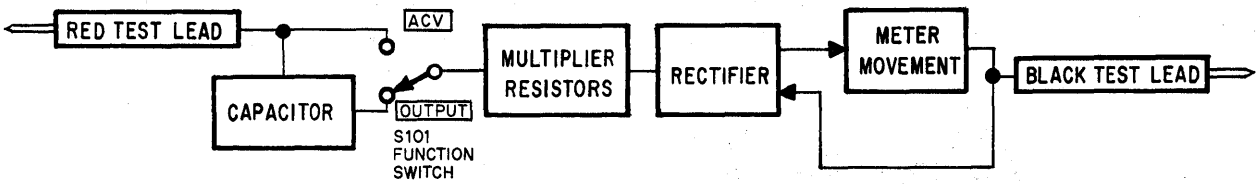

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Figure 3-9.—Functional block diagram of a.c. and output voltage circuits.

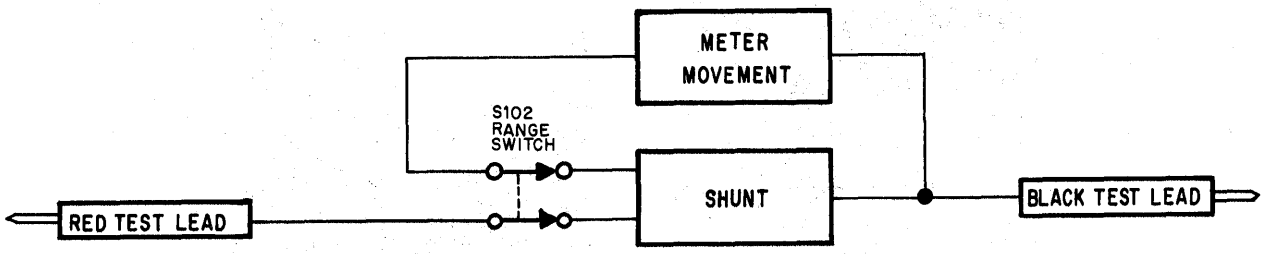

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Figure 3-10.—Functional block diagram of d.c. current circuits.

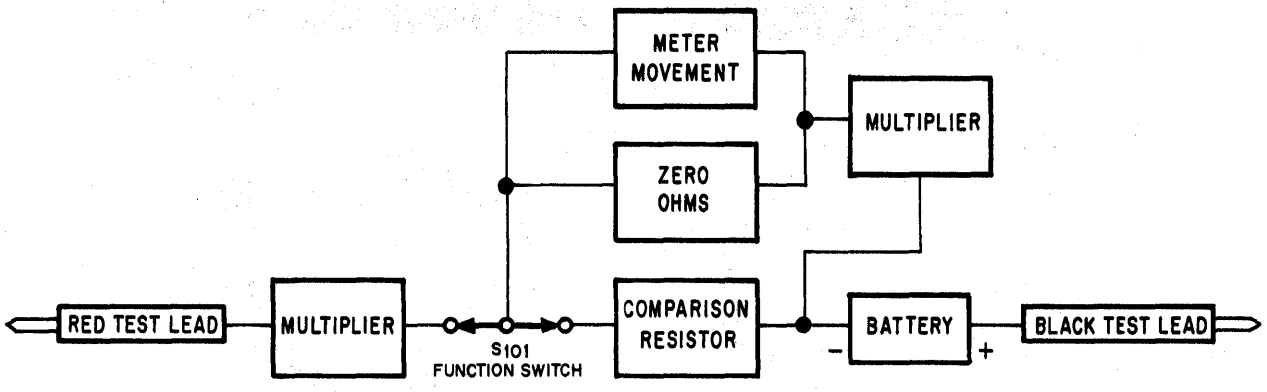

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Figure 3-11.—Functional block diagram of ohmmeter circuits.

leads, this resistance will be in series with the instrument circuit, and less current will flow through the meter movement. The amount of reduced meter deflection indicates how much resistance is between the test leads.

Function Switch S-101

Function switch S-101 (fig. 3-7) located in the lower left-hand corner of the front panel, selects the type of circuit for which the instrument is connected. There are two positions for d.c. volts, direct and reverse. The normal position is direct. When using the meter to make a d.c. voltage measurement and a connection is made which causes the meter to read backwards (deflection of the pointer to the left), set switch S-101 to reverse and the pointer will be deflected upscale. To read alternating current voltages, set switch S-101 to the ACV position. A rectifier within the instrument rectifies the a.c. voltage to an equivalent d.c. value, and the meter indicates the RMS value of the applied voltage. To read the a.c. portion of mixed a.c. and d.c. voltages, set switch S-101 at OUTPUT. Set switch S-101 at DC μA MA AMPS to read direct current. As mentioned previously, switch S-101 also serves as a range switch for resistance measurements.

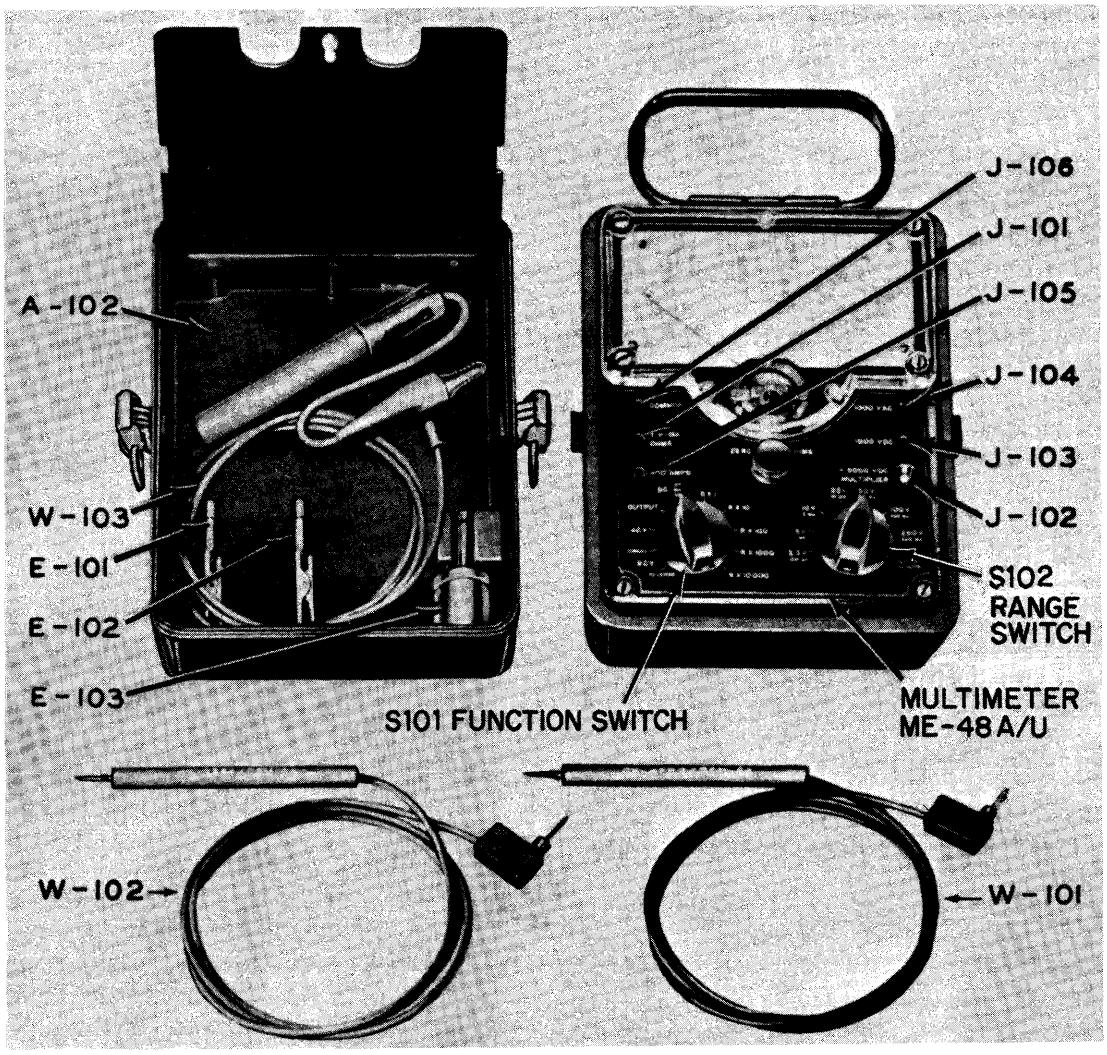

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Figure 3-12.—Controls, jacks, leads and accessories.

Range Switch S-102

This eight-position range switch located in the lower right corner of the front panel permits the selection of voltage and current ranges. The full scale value for each range switch position is marked on the front panel.

Zero Ohms Control

The ZERO OHMS control is located near the center of the front panel. Each time the function switch S-101 is placed in a position to read resistance, short the test leads together and rotate the ZERO OHMS control knob to make the pointer read full scale, or zero ohms. If you cannot bring the pointer to full scale, replace the battery in the rear of the case.

Test Leads and Test Jacks

There are two test leads, W-101 and W-102 (fig. 3-12) which are needed for all measurements except those which require the 5000V d.c. range. Test lead W-101 is red, and test lead W-102 is black. Unless otherwise specified, connect black test lead W-102 in the common jack, J-106, and connect the red test lead W-101 in the +V MA OHMS jack, J-101. For the 1000V d.c. range, place red test lead W-101 in the 1000V d.c. jack, J-103. For the 1000V a.c. range, place red test lead W-101 in the 1000V a.c. jack, J-104. Use the red test lead to contact the positive side of the source for d.c. measurements and the black test lead to contact the negative side. For the 5000V d.c. range, use black test lead, W-102 in the common jack, J-106, and use the high voltage test lead, W-103, screwed on over recessed post J-102, +5000V d.c. multiplier. For the 10 ampere range, place red test lead, W-101, in the special +10 AMPS jack, J-105.

Accessories E-101, E-102, and E-103

There are two alligator clips, E-101 and E-102, which the operator may use to screw on over the end of test leads W-101 and W-102. This is for the convenience of the operator. There is a telephone plug, E-103, which may be used to connect both the test leads, W-101 and W-102, to contacts within a two-contact telephone jack. This permits easier connection to the jack contacts for any electrical measurement because the operator can make the measurement directly through an equipment panel without opening the case of the equipment. The red test lead W-101, connected in the red insulated jack (not shown) on the rear of the telephone plug E-103, contacts the tip of the plug. The black test lead, W-102, connected in the black insulated jack (not shown) on the rear of the telephone plug, E-103, contacts the sleeve of the plug.

ELECTRONIC MULTIMETER

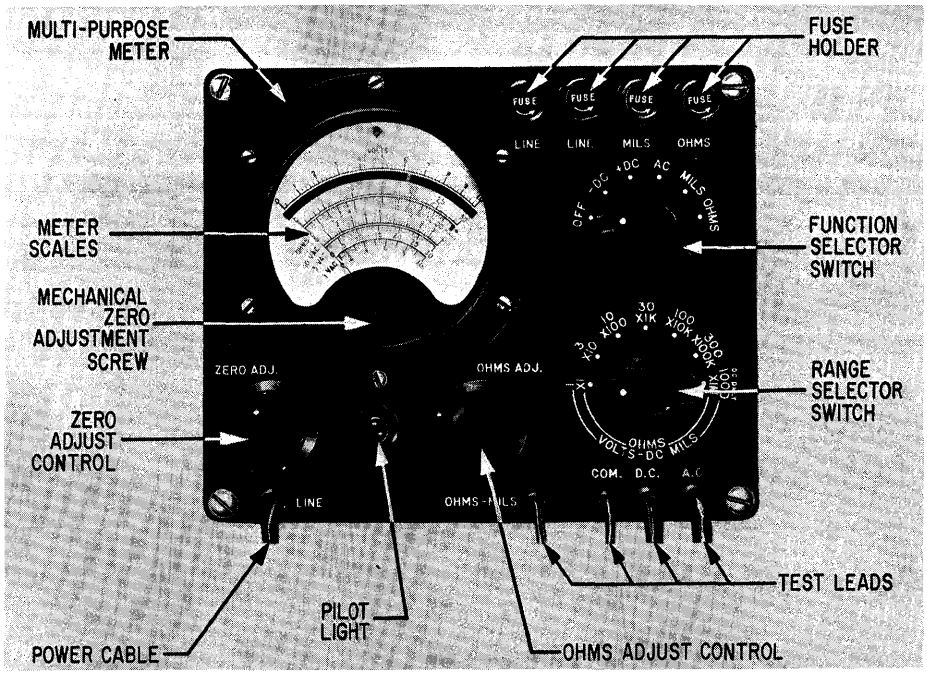
The AN/USM-116C is a portable (17 pounds) electronic multimeter used for general servicing of electronic equipment. It is designed for use where precise voltage, current and resistance measurements are required. It has a high input impedance which permits voltage measurements to be made with only a small amount of loading on the circuit under test.

The AN/USM-116C is capable of making the following range of measurements:

1. A.C. volts - 0.01 to 300 rms (effective)
2. D.C. volts - 0.02 to 1,000 (+ or -)
3. D.C. current - 20 μA to 1,000 mA
4. Resistance - 0.2Ω to 1,000 MΩ

Front Panel Controls

Figure 3-13 illustrates all the controls necessary for proper operation of the multimeter. These controls include the FUNCTION SELECTOR switch which selects the type of measurement to be made. The RANGE SELECTOR switch determines the desired range of a particular measurement. There are multiplication factors to be considered when making some measurements. Check the technical manual (NAVSEA 0969-126-8010) for these figures. The OHMS ADJ. control permits proper



The Hickok Electrical Instrument Company

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Figure 3-13.—AN/USM-116C front panel.

calibration of the ohmmeter ranges. The ZERO ADJ. is a dual control. Adjustment of the black knob serves to balance the multimeter for proper accuracy when measuring d.c. volts, a.c. volts and ohms. The red knob of the ZERO ADJ. control permits secondary adjustment of the low a.c. voltage ranges. The face of the meter contains six scales. The three lower scales are used with the 1, 3, and 10 a.c. volt ranges. The blue OHMS scale is used for all resistance measurements. All other measurements of a.c. volts, d.c. volts and d.c. milliamperes are made on the two top scales. The purpose of the mirror on the meter face is to eliminate parallax errors. When reading the meter, view the scale so that the pointer coincides exactly with the image in the mirror.

There are four permanently mounted test leads feeding out of the bottom of the control panel. Two of these leads are unshielded and used for making RESISTANCE AND CURRENT tests. One of the shielded leads is a ground lead marked COM, and the other is labeled OHMS-MILS. One of the shielded leads (red test probe) is used to measure d.c. volts. The other shielded lead is used for measuring a.c. and is connected to an RF probe. There is a special ground lead to be connected to the a.c. probe when measuring RF voltages.

Refer to the AN/USM-116C technical manual for detailed instruction on how to make various measurements.

FUNCTIONAL BLOCK DIAGRAM

Figure 3-14 is a block diagram of the multimeter. As previously stated, the multimeter can measure a.c. and d.c. voltages as well as resistance and current. When measuring a.c. voltages, the signal must first be rectified by a diode in the a.c. probe. The signal must be rectified because the meter circuit is sensitive only to d.c. voltages.

The Function Selector switch determines which function is being used by selecting either the VOLTAGE ATTENUATOR, the OHMS MULTIPLIER or the MILS ATTENUATOR.

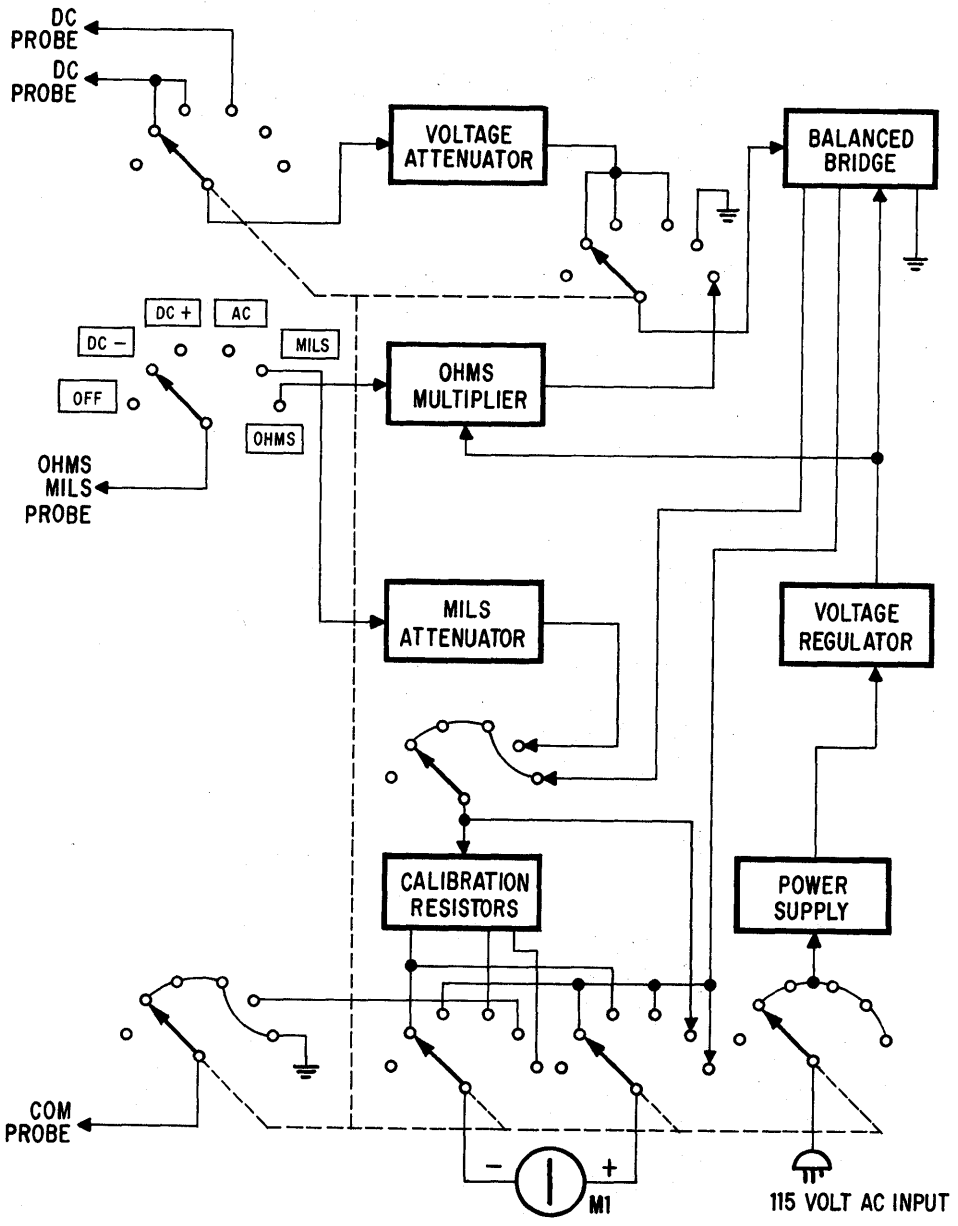

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Figure 3-14.—AN/USM-116C functional block diagram.

When the Voltage Attenuator is selected, the a.c. or d.c. voltage is applied across a voltage-divider network so that the total input impedance of the multimeter remains constant when the position of the Range switch is changed for various levels of input voltage. The meter is then connected across a BALANCED BRIDGE network through the CALIBRATION RESISTORS. With no input, the bridge is balanced and the meter reads zero. When the bridge is unbalanced by an input voltage, the meter pointer is deflected. The amount of

deflection is proportional to the value of the input voltage.

The ohmmeter section also uses the bridge circuit. When an unknown resistance is placed between the OHMS-MILS lead and the COM lead, the bias voltage on the balanced bridge, through the OHMS MULTIPLIER, decreases in proportion to the unknown resistance. The value of the unknown resistance determines the degree to which the bridge is unbalanced and, therefore, the magnitude of the meter pointer deflection. No battery supply is required for the ohmmeter circuitry.

The milliammeter function does not make use of the bridge circuit. The range switch connects various calibration resistors (shunts) across the meter to increase the range of current measurements. The VOLTAGE REGULATOR is used to maintain the B+ supply voltage to the balanced bridge at a constant value despite changes in line voltage.

MODEL 803D DIFFERENTIAL VOLTMETER

The 803D (fig. 3-15) is a highly accurate, portable and compact differential voltmeter used for precise measurement of almost any a.c. or d.c. voltage. Its general function is to compare an unknown voltage with an internal reference voltage, and to indicate the difference in their values. It is capable of being used as a vacuum tube voltmeter, as a precision potentiometer, and as a megohmmeter for measurement of high resistance. It can also be used to measure the variations (positive and

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Figure 3-15.—Model 803D Differential Voltmeter.

negative) from a specified voltage level. One feature that should be emphasized is that no current is drawn from the unknown source for d.c. measurements when balance is attained. Thus, the determination of the unknown d.c. potential is independent of its source resistance. In simpler terms, the 803D will not load the circuit under test once a balance (NULL) condition has been reached.

The 803D may be used for measurements of d.c. voltages from 0 to 500 volts and a.c. voltages from 0.001 to 500 volts. However, high accuracy measurements to 30,000 volts d.c. are possible with precision voltage dividers. It also has a polarity switch for equal convenience in measuring positive or negative d.c. voltages and an adjustable recorder output which makes the 803D particularly useful for monitoring the stability of almost any a.c. or d.c. voltage.

Operating Controls

The front panel controls of the 803D are shown in figure 3-15. The OPERATE/CALIBRATE switch is spring loaded to the OPERATE position. The CALIBRATE position is used to calibrate the internal 500V d.c. reference supply. In this position, a representative sample of the reference voltage is compared to the voltage of an internal standard battery. The CALIBRATE control is used with the OPERATE/CALIBRATE switch to vary the output of the 500V d.c. reference supply. The reference supply is accurately set by adjusting the CALIBRATE control for zero meter deflection. The RANGE switch selects the desired voltage range or an A.C. NULL MULTIPLIER. Full scale ranges of 500, 50, 5 and 0.5 volts are available.

The NULL switch is set to the VTVM position for determining the approximate value of unknown voltage prior to differential measurements. Five null ranges of 10, 1, 0.1, 0.01, 0.001 volts may be used for differential measurements. For the D.C. mode, the null ranges represent full scale differences between the unknown voltage and the amount of precision internal reference voltage that is set on the voltage readout dials. In the A.C. mode, the NULL range switch times the applicable A.C. NULL MULT setting, represents the full scale difference between the unknown voltage and the amount set on the voltage dials. The A, B, C, D, and E voltage readout dials provide an in-line readout of the amount of internal reference voltage necessary to null the unknown voltage. The DECIMAL LIGHTS on the front panel serve as decimal points for the voltage readout dials. A different light illuminates for each position of the RANGE switch.

Operation

The 803D is capable of several different types of operation. The D.C. Differential voltmeter operation will be discussed in this text. Other operations are discussed in detail in the Model 803D technical manual.

After turning the 803D on and allowing a warmup period of at least ten minutes, adjust the internal 500-volt reference supply for zero meter deflection, by using the CALIBRATE control. The ten-minute warmup period is especially important because it allows the meter components time to stabilize.

Connect the unknown voltage to the input binding posts. If one side is grounded, always connect it to the lower input post (middle post). With the NULL switch in the VTVM position turn the RANGE switch to the lowest range that will allow an on-scale reading and note approximate value of unknown voltage as indicated on upper meter scale.

If meter reads to the left, turn A.C.-D.C. polarity switch to the negative position. The meter needle will deflect to the right. This is because polarity of unknown voltage is negative.

Noting the position of illuminated decimal light, set five voltage readout dials to approximate voltage determined previously. For example, if approximate voltage is 35 volts, the decimal light between the B and C voltage readout dials will be illuminated. Therefore, set A dial to 3, B dial to 5, and C, D, and E dials to 0.

Set NULL switch to successively more sensitive null ranges, as indicated in table 3-1, and adjust voltage readout dials for zero meter deflection in each null position. When the meter needle indicates to the right, the voltage under

Table 3-1.–Recommended NULL Settings.

INPUT VOLTAGE RANGE	*RECOMMENDED NULL SETTING
50-500	10 then 1 (then 0.1 for voltages from 50 to 100 volts)
5-50	1 then 0.1 (then 0.01 for voltages from 5 to 10 volts)
0.5-5	0.1 then 0.01 (then 0.001 for voltages from 0.5 to 1 volt)
0-0.5	0.01 then 0.001

*Any null range may be used with any input voltage range; recommended settings are those most useful.

measurement is greater than the voltage set on the voltage readout dials. When the indication is to the left, the voltage is less than that set on the readout dials.

Read the measured voltage directly from the five voltage readout dials.

BLOCK DIAGRAM

Figure 3-16 shows the block diagram for the 803D A.C./D.C. Differential Voltmeter. As seen in this figure, the circuit consists basically of an a.c. to d.c. converter, a d.c. vacuum tube voltmeter (vtvm), and a 0 to 500 volt d.c. reference supply.

The overall operation of the 803D may be summarized as follows. To measure the approximate value of a d.c. voltage, the unknown voltage is connected directly to the d.c. vtvm.. To accurately measure a d.c. voltage, the unknown voltage is connected across the series combination of the d.c. vtvm and the 0 to 500 volt d.c. reference supply. The reference supply voltage is then adjusted with the five voltage readout dials until it matches the unknown voltage as indicated by the vtvm. All a.c. measurements are made by first converting the a.c. input voltage to a d.c. voltage by means of the a.c. to d.c. converter. The 803D then operates essentially the same as for approximate and accurate d.c. measurements.

D.C. VACUUM TUBE VOLTMETER

The d.c. vtvm is composed of an attenuator, a null detector, and a meter. The heart of the d.c. vtvm is the null detector in which the d.c. signal input is modulated, amplified, rectified, and finally filtered to produce a d.c. output. The output current from the null detector is indicated on a meter that has taut-band suspension. This suspension does away with all friction associated with meter pivot stickiness. Thus, any tendency for the meter pointer to stick at one point of the scale and then jump to another point is completely eliminated. The attenuator is used to reduce the voltage span of each range to a common range usable by the NULL DETECTOR, to produce proper meter deflection.

500 VOLT REFERENCE SUPPLY

When the 803D is used for differential voltage measurements, an internal voltage is nulled or matched against the unknown voltage. An extremely accurate reference voltage is, therefore, required. This is obtained from the 0 to 500 volt reference supply. The 0 to 500 volt reference supply is composed of a well regulated 500 volt power supply, a range divider and a five decade attenuator. The output of the 500 volt power supply is applied directly to the attenuator for the 500 volt d.c. range. In the 50, 5, and 0.5 volt d.c. range, the range divider reduces the voltage to 50, 5, and 0.5 volts before it is applied to the attenuator. For any a.c. range, the range divider always reduces the voltage to 5 volts. The attenuator divides its input voltage (500, 50, 5, or 0.5 volts) into

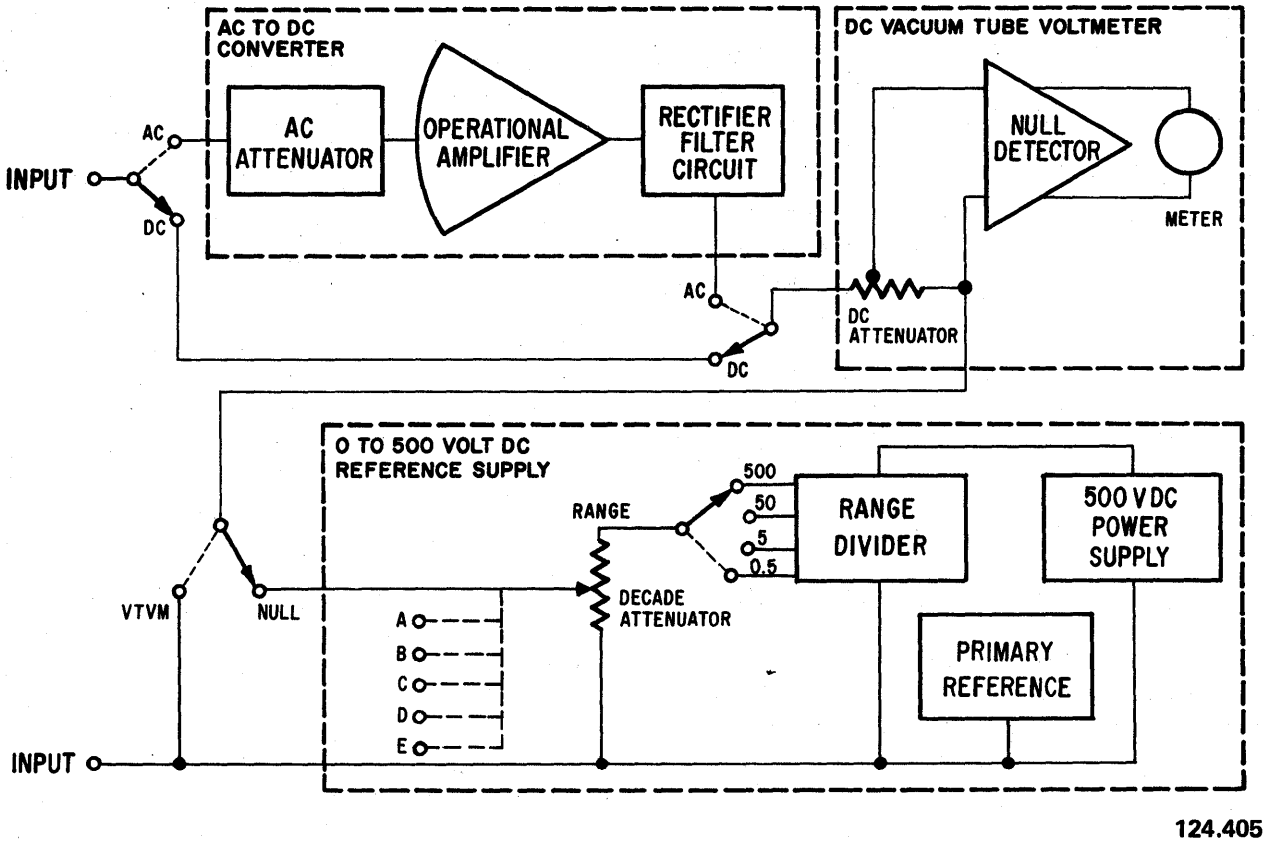


Figure 3-16.—Model 803D, functional block diagram.

50,000 equal increments, any number of which may be selected by setting the five decades with the voltage readout dials. The output of the attenuator, therefore, provides an extremely accurate reference voltage. The primary reference (fig. 3-16) is a battery used to calibrate the 500 volt supply.

A.C. TO D.C. CONVERTER

The a.c. to d.c. converter is composed of an attenuator, an operational amplifier, and a rectifier-filter circuit. A diode in the rectifier-filter circuit is used to convert the unknown a.c. into pulsating d.c., which is then filtered to obtain a d.c. voltage that is proportional to the average value of the a.c. input voltage. The output however, is calibrated to indicate the RMS value of a pure sine wave. An operational amplifier containing three resistance-capacitance coupled amplifier stages with high negative feedback is used to make the rectification characteristics of the diodes linear and stable. The attenuator is used to reduce the a.c. input voltage by a factor of 10 or 100, as required to restrict the operational amplifier input to 5 volts maximum for full scale inputs of 50 and 500 volts respectively.

FREQUENCY COUNTER

The AN/USM-207 is a portable, solid-state electronic counter for the precision measurement and eight-digit numerical display of: the frequency and period of a cyclic electrical signal, the frequency ratio of two signals, the time interval between two points on the same or different signals, and the total

number of electrical impulses (totalizing). The unit also provides output signals of the following types:

1. Standard signals from 0.1 Hz to 10 MHz in decade steps derived from a 1 MHz frequency standard, frequency dividers, and a frequency multiplier
2. Input signals divided in frequency by factors from 10 to 10^8 by a frequency divider
3. Digital data of the measurement in four-line binary-coded-decimal form with decimal point and control signals for operation of printers, data recorders, or control devices
4. A 1 MHz output from a frequency standard.

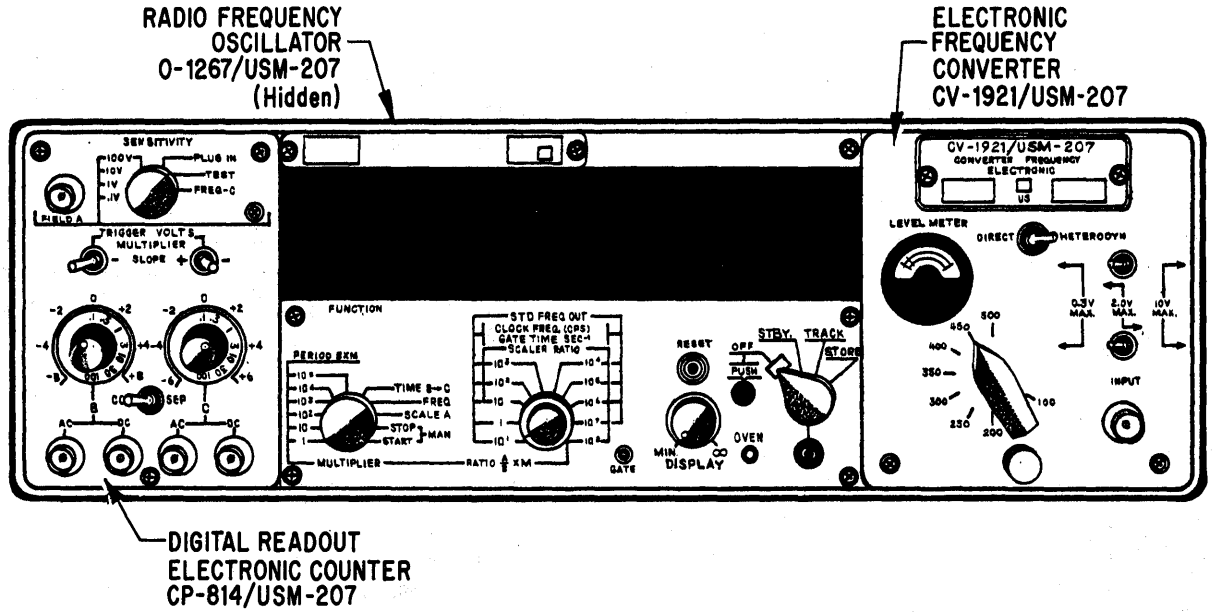
General Description

The AN/USM-207 (fig. 3-17) consists of a major counter assembly, two plug-in assemblies installed in recesses on the front and rear panel, and a group of accessory cables and connectors stored in the detachable front cover.

The major assembly Digital Readout Electronic Counter CP-814/USM-207 contains the input amplifiers, gate control, display, reset and transfer control, frequency multipliers, time base dividers, decade and readout boards, numerical display tubes, decimal point and units indicators, power supply and regulator, and controls associated with these circuits.

The Radiofrequency Oscillator O-1267/USM-207 plug-in assembly develops a 1 MHz signal and includes its own power supply. The oscillator includes the 1 MHz output receptable which may be used as a source of that frequency when the oscillator is connected to a.c. power through the basic counter or when connected to the power line independently of the counter. The counter may be operated without the oscillator in totalizing, scaling the input signal, time interval with external clock, and frequency ratio measurements. For other measurements the counter does not require the oscillator when a separate external 100 kHz or 1 MHz signal is connected. In either of these two situations, the oscillator may be left in the counter or removed. The oscillator plugs in to the right rear of the counter.

The Electronic Frequency Converter CV 1921/USM-207 plug-in assembly permits measurement of frequencies up to 500 MHz,



162.7

Figure 3-17.—AN/USM-207 front panel.

using the heterodyne principle (*Basic Electronics*, NAVEDTRA 10087-C, Vol. 1, Ch. 16 or Navy Electricity-Electronics Training Series (NEETS), applicable module.) The unit consists of broadband amplifier, mixer, multiplier, and controls and indicators associated with these circuits. When measurements other than heterodyne frequency measurements are made, the converter is not required, but need not be removed. The converter also permits the measurement of signals from 35 MHz to 100 MHz with a greater sensitivity than possible with the basic counter. The converter plugs into the right front of the counter.

Front Panel Controls

Refer to figure 3-17. The FREQ. A input connector accepts an external signal for frequency and frequency-ratio measurements, for totalizing, and for obtaining scaled outputs. The SENSITIVITY switch selects source of input signal in frequency, frequency ratio (numerator) and totalizing modes of operation. The digital display indicates numerical results of measurement with an automatically positioned decimal point. The LEVEL meter indicates in the green when the level of the signal applied to the converter INPUT connector is sufficient to provide a valid digital readout. It indicates in the red when the input signal level is questionable, incorrectly attenuated, or the mixing frequency is incorrect. The FREQUENCY TUNING-MC switch selects a mixing frequency for heterodyne frequency measurement. This switch operates with the LEVEL meter. When the POWER switch is set to OFF, all power is removed from the counter circuits. When set to STBY, power is applied to the radiofrequency oscillator only. When set to TRACK, power is applied to all counter circuits and the digital display shows a continuous display of the changing count. When set to STORE, power is applied to all counter circuits, and the digital display remains constant during the count and changes only when the final count changes after any gate period. The DISPLAY control is used to increase the length of time that the count is displayed as the control is rotated from the MIN. position clockwise. The measurement automatically recycles after the display time. When switched to the extreme clockwise ∞ position, the count is displayed until the RESET switch is pushed.

The STD FREQ OUT switch is dual control. The red switch selects the standard frequency output that appears at the STD FREQ OR SCALE OUT connector (on rear panel). The black switch (time base) has four uses. It will select the CLOCK FREQ that is counted when period and time-intervals are measured. It will select the GATE TIME when measuring frequency. It will select a SCALER RATIO by which the input signal is divided when used with the FUNCTION switch. It will also select the frequency ratio measurement in the 10^8 position when used with the FUNCTION switch. The time base switch in conjunction with the FUNCTION switch position selects the unit of measurement and decimal point that are displayed in frequency, period, and time-interval measurements. The FUNCTION switch selects measurement or scaling mode of operation in conjunction with positions of SENSITIVITY switch and time base switch as follows:

The d.c. and a.c. connectors for each channel accept an external signal for period, frequency-ratio and time-interval measurements. The two switches above the connectors are dual purpose. The inner knobs are the channel MULTIPLIER switches which select a multiplier for the channel TRIGGER VOLTS controls (outer knobs). The outer knobs select any voltage from +6 to -6 volts which when multiplied by the channel MULTIPLIER switch setting will determine the exact triggering point of the input signal for the selected channel.

There is a PRINTER connection (not shown) on the rear panel that supplies signals representing the digital data output of the measurement including the decimal-point position in four-line binary-coded decimal form. Included in the output are control signals for the operation of printers, other data recorders, or control devices, and a reset inhibit line to prevent reset of the counter during data recording.

Functional Description

Figure 3-18 is the overall functional block diagram of the counter. To make a measurement

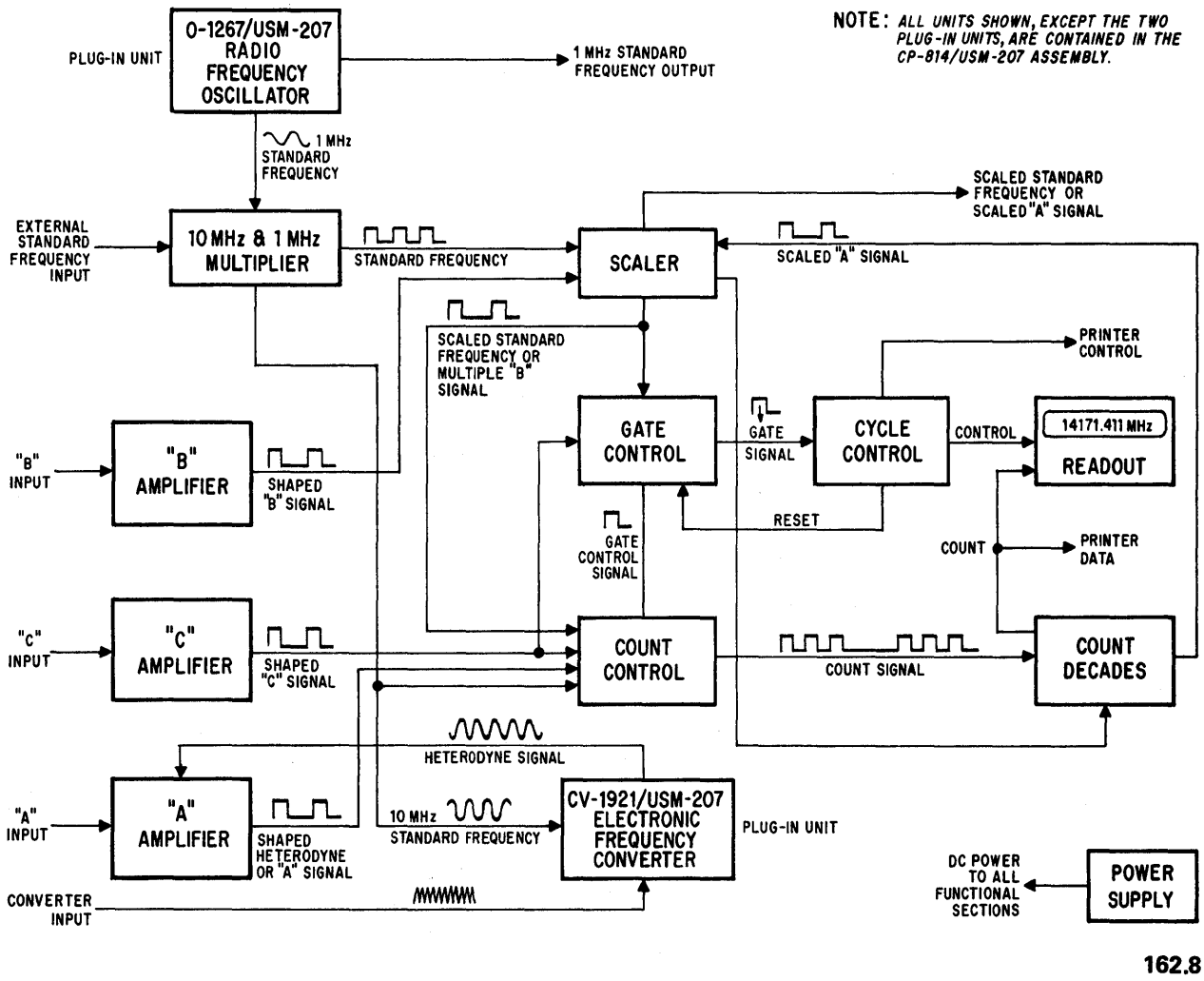


Figure 3-18.—AN/USM-207, functional block diagram.

requires two types of information; a count signal, and a gate control signal. These two signals may be generated within the instrument, or they may be supplied from outside sources. The type of measurement the counter will make depends upon the relationship of these two signals. In any function the instrument counts the count signal for a period of time determined by the gate control signal. Routing of these signals within the instrument is accomplished by logic circuits. These logic circuits are controlled by means of the front panel controls.

The radiofrequency oscillator (O-1267/USM-207) generates a signal of precise frequency for use throughout the counter or to provide a precise 1 MHz signal for use outside the equipment.

The electronic frequency converter accepts radiofrequencies between 100 MHz and 500 MHz and converts them to radiofrequencies between 5 MHz and 100 MHz for measurement by the basic counter.

The "A", "B", and "C" amplifiers amplify and shape the respective input signals for use throughout the counter.

The 10 MHz and 1 MHz multiplier multiplies the frequency and shapes the signal generated by the radiofrequency oscillator. It also provides

precise timing signals to the various functional sections of the basic counter and to the frequency converter.

The scaler consists of a series of decade dividers and gating systems which provide divided standard frequencies and control signals depending on the type of measurement the instrument is making.

The gate control generates the gate control signal. This signal determines the length of time that the count decades will count the count signal.

The count control provides the proper count signal to the count decades, as selected by the setting of the front-panel switches.

The cycle control produces all signals necessary to display the measurement results on the readout and to recycle the counter.

The count decades count the count signal when permitted to do so by the gate control.

The result of their counting becomes the final reading displayed by the readout at the end of each measurement.

The readout receives binary-coded-decimal (BCD) data from the count decades, decodes this data into decimal form and drives the readout indicator tubes. The readout also contains memory circuits which function when the counter is operated in the "Store" mode.

The power supply supplies all d.c. power required by the basic instrument and the converters and consists of seven d.c. supplies. Five of these supplies (+18 volts, +12 volts, +6 volts, -6 volts, and -12 volts) are regulated, and two (+180 volts and +45 volts) are unregulated.

TESTING SEMICONDUCTOR DEVICES

Because of the reliability of semiconductor devices, servicing techniques developed for transistorized equipment differ from those normally used for electron tube circuits. Electron tubes are usually considered to be the circuit component most susceptible to failure, and are, therefore, normally the first components to be tested. Transistors, however, are capable of operating in excess of 30,000 hours at maximum rating without failure and are often soldered in the circuit in much the same manner as resistors and capacitors.

Replacing a semiconductor diode or transistor of questionable condition with one known to be good is a simple means of determining the device's state. This technique should be used only after you have made voltage and resistance measurements to make certain that there is no circuit defect that might damage the substitute semiconductor device. If more than one defective semiconductor is present in the equipment section where trouble has been localized, this method becomes cumbersome, since several semiconductors may have to be replaced before the trouble is corrected. To determine which stages failed and which semiconductors are not defective, all of the removed semiconductors must be tested. This can be accomplished by observing whether the equipment operates correctly as each of the removed semiconductor devices is reinserted into the equipment.

TESTING DIODES

Semiconductor diodes, such as general purpose germanium and silicon diodes, power silicon diodes, and microwave silicon diodes, may be tested most effectively only under actual operating conditions. However, crystal rectifier testers are available to determine direct-current characteristics which provide an indication of crystal-diode quality.

A common type of crystal diode test set is a combination ohmmeter-ammeter. Measurements of forward resistance, back resistance, and reverse current may be made with this equipment. The condition of the diode under test can then be determined by comparison with typical values obtained from test information furnished with the test set or from the manufacturer's data sheets. A check which provides a rough indication of the rectifying property of a diode is the comparison of the diode's back and forward resistance at a specified voltage. A back-to-forward resistance ratio is greater than 10:1 and a forward-resistance value of less than 50 ohms is common. To insure correct ratios and resistance

values, compare the diode being checked against a known good diode of the same type.

Testing With Ohmmeter

A convenient test for a semiconductor diode requires only an ohmmeter. The forward and back resistance can be measured at a voltage determined by the battery potential of the ohmmeter and the resistance range at which the meter is set. When the test leads of the ohmmeter are connected to the diode, a resistance will be measured which is different from the resistance indicated if the leads are reversed. The smaller value is called the forward resistance, and the larger value is called the back resistance. If the ratio of back-to-forward resistance is greater than 10:1, the diode should be capable of functioning as a rectifier. However, you should keep in mind that this is a very limited test that does not take into account the action of the diode at voltages of different magnitudes and frequencies.

Testing With An Oscilloscope

An oscilloscope can be used to graphically display the forward and back resistance characteristics of a crystal diode. A circuit used in conjunction with an oscilloscope to make this test, is shown in figure 3-19. This circuit uses the oscilloscope line test voltage as the test signal. A series circuit composed of resistor R1 and the internal resistance in the line test circuit decreases the 3-volt open circuit test voltage to a value of approximately 2 volts, peak to peak. The test signal applied to the crystal diode is also connected to the horizontal input of the oscilloscope. The horizontal sweep will then represent the voltage applied to the diode under test. The voltage developed across current-measuring resistor R2 is applied to the vertical input of the oscilloscope. Since this voltage is proportional to the current through the diode under test, the vertical deflection will indicate crystal current. The resulting oscilloscope trace for a normal diode will be similar to the curve shown in figure 3-20.

To test zener diodes, a higher voltage than the oscilloscope line test signal must be used. This test can be made with a diode test set or with the circuit shown in figure 3-21. In this circuit, rheostat R1 is used to adjust the input voltage to a suitable value for the zener diode being tested, and resistor R2 limits the current through the diode. The signal voltage applied to the diode is also connected to the horizontal input of the oscilloscope. The voltage developed across current-measuring resistor R3 is applied

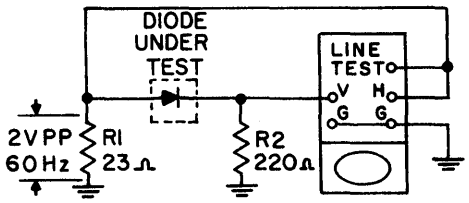


Figure 3-19.—Testing semiconductor diode with oscilloscope. 162.117

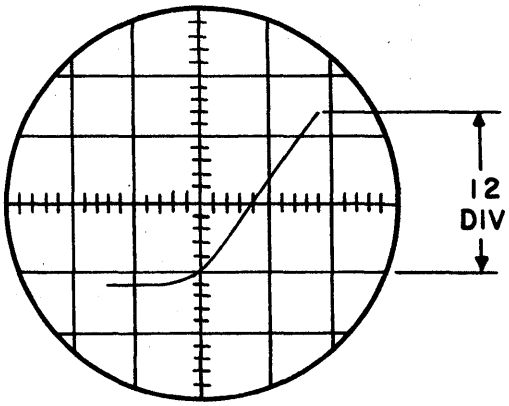
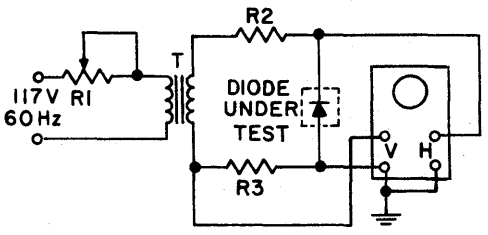


Figure 3-20.—Characteristic curve of a semiconductor diode. 162.118

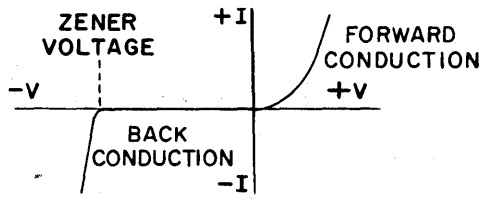


162.119

Figure 3-21.—Testing zener diode.

to the vertical input of the oscilloscope. Therefore, the horizontal sweep will represent the applied voltage, and the vertical deflection will indicate the current through the diode under test. Figure 3-22 shows the characteristic pattern of a zener diode; note the sharp increase in current at the zener voltage (avalanche) point. For the zener diode to be acceptable, this voltage must be within the limits specified by the manufacturer.

Instructions for constructing a simple in-circuit semiconductor diode and a transistor tester (used in conjunction with an oscilloscope) are contained in EIB 815 of 15 November 1971.



162.120

Figure 3-22.—Zener diode characteristic curve.

TESTING TRANSISTORS

When trouble occurs in transistorized equipment, power supply voltage measurement, waveform checks, signal substitution or signal tracing methods are normally the first tests made. If a faulty stage is isolated by one of these test methods, voltage, resistance, and current measurements can be made to locate defective parts. When making these measurements, you must make certain that the voltmeter resistance is high enough to have no appreciable effect upon the voltage being measured, and that current from the ohmmeter will not damage the transistor. If the transistors are not soldered into the equipment, it is usually advisable to remove the transistors from their sockets during a resistance test. Transistors should be removed from or reinserted into their sockets only after power has been removed from the stage, since damage by surge currents may otherwise result.

Procedures for removing soldered-in transistors are discussed in chapter 2. Transistor circuits other than pulse and power amplifier stages are usually biased so that the emitter current is from 0.5 to 3 milliamperes, and the collector voltage is from 3 to 15 volts. The emitter current can be measured by opening the emitter connector and inserting a milliammeter. When making this measurement, you should expect some change in bias due to the meter resistance. The collector current can often be determined by measuring the voltage drop across a resistor in the collector circuit and calculating the current. If the transistor itself is suspected, it can be tested with an ohmmeter or transistor tester as described in the following paragraphs.

Resistance Test

An ohmmeter can be used to test transistors by measuring the emitter-collector, base-emitter, and base-collector forward and back resistances. A back-to-forward resistance ratio on the order of 500:1 should be obtained for the collector-to-base and emitter-to-base measurements. The forward and back resistances between the emitter and collector should be nearly equal. All three measurements should be made for each transistor tested, since experience has shown that transistors can develop shorts between the collector and emitter and still have good forward and reverse resistances for the other two measurements.

Because of shunting resistances in transistor circuits, you will normally have to disconnect at least two transistor leads from the associated circuit for this test. You must exercise caution during this test to make certain that current during the forward resistance tests does not exceed the rating of the transistor. Ohmmeter ranges which require a current of more than 1 milliampere should not be used for testing transistors. Many ohmmeters are designed so that on the RX1 range 100 milliamperes or more can flow through the electronic part under test.

Transistor Tester

Laboratory transistor test sets are used in experimental work to test all characteristics of transistors. For maintenance and repair, however, it is not necessary to check all of the transistor parameters. A check of two or three performance

characteristics is usually sufficient to determine whether a transistor needs to be replaced. Two of the most important parameters used for transistor testing are the transistor current gain (Beta) and the collector leakage or reverse current (Ico). These are discussed in *Basic Electronics, Vol. I,* NAVEDTRA 10087-C (or Navy Electricity-Electronics Training Series (NEETS), applicable module).

Semiconductor Test Set AN/USM-206-A (fig. 3-23) is a rugged field type tester designed to test transistors and semiconductor diodes. The set will measure the Beta (amplification factor) of a transistor, the resistance appearing at the electrodes and the reverse current of a transistor or semiconductor diode, a shorted or open diode, the forward transconductance of a field effect transistor, and the condition of its own batteries.

In order to assure that accurate and useful information is gained from the transistor tester, the following preliminary checks of the tester should be made prior to testing any transistors:

With the POLARITY switch (fig. 3-23) in the OFF position of the meter pointer should indicate exactly zero. (When required, rotate meter adjust screw on front of meter to fulfill this requirement). The POLARITY switch must always be left in the OFF position, when measurements are not actually being made, to prevent battery drain.

Always check the condition of the test set batteries by disconnecting the test set power cord, placing the POLARITY switch in the PNP position and placing the FUNCTION switch first to BAT(1) then to BAT(2). In both BAT positions the meter pointer should move so as to indicate within the red BAT box.

BETA MEASUREMENTS.—If the transistor is to be tested out of the circuit, plug it into the test jack located on the right-hand side below the meter shown in figure 3-23. If the transistor is to be tested in the circuit, it is imperative that at least 300 OHMS exist between E-B, C-B, and C-E for accurate measurement. Initial setting of the test set controls is:

(a) Function Switch to BETA
(b) Polarity Switch to PNP or NPN (dependent on type of transistor under test)

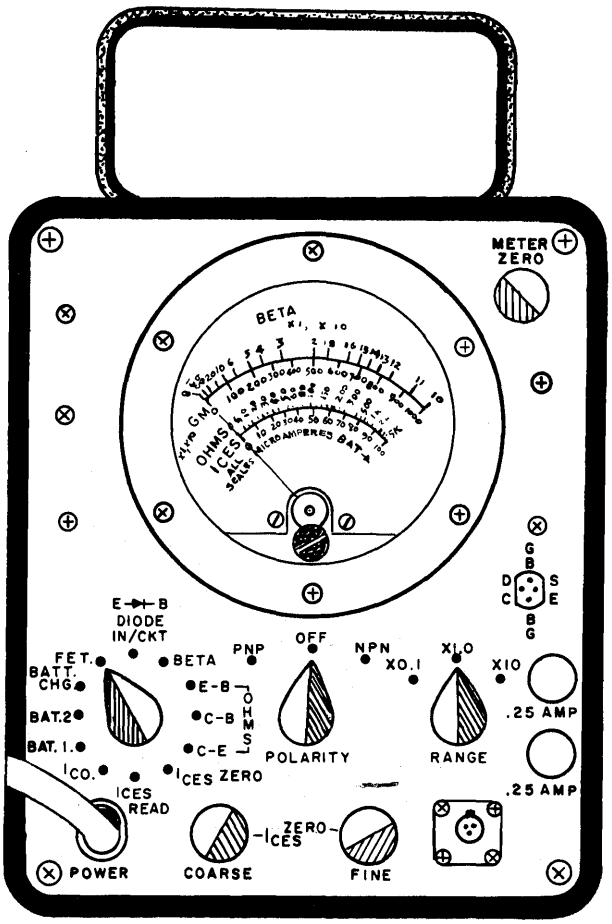


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Figure 3-23.—AN/USM-206A front panel.

(c) Range Switch to X10
(d) Adjust meter zero for zero meter indication (transistor disconnected).

NOTE: The polarity switch should remain OFF while transistor is connected to or disconnected from the test set. If it is determined that the Beta reading is less than 10, reset the range switch to X1 and reset the meter to zero.

After connecting the yellow test lead to the emitter, the green test lead to the base and the blue test lead to the collector, plug the test probe (not shown) into the jack located at the lower right hand corner of the test set. When

testing grounded equipment, unplug the 115V a.c. line cord and use battery operation. Beta reading is attained by multiplying the meter reading times the range switch setting. Refer to the Transistor Characteristics book provided with the tester to determine if the reading is normal for the type of transistor under test.

ELECTRODE RESISTANCE MEASUREMENTS.–Connect the in-circuit probe test leads to the transistor with the yellow lead to the emitter, the green lead to the base, and the blue lead to the collector. Set the function switch to the OHMS E-B position and read the resistance between the emitter and base electrode on the center scale of the meter.

To read the resistance between the collector and base and the collector and emitter, set the function switch to OHMS C-B and OHMS C-E. These in-circuit electrode resistance measurements are used to correctly interpret the in-circuit Beta measurements. The accuracy of the BETA X1, X10 range is ±15% only when the emitter to base load is equal to or greater than 300 ohms.

ICO MEASUREMENTS (COLLECTOR LEAKAGE TEST).–Adjust meter zero control for zero meter indication. Plug the transistor to be tested into the jack or connect test leads to the device under test. Set the PNP/NPN switch to correspond with the transistor under test. Set the function switch to ICO, the range switch to X0.1, X1 or X10 as specified by the transistor data book for allowable leakage. Read leakage on bottom scale, and multiply by the range setting figure as required.

DIODE MEASUREMENTS.–Diode qualitative in-circuit measurements are attained by connecting the green test lead to the cathode and the yellow test lead to the anode. Set the function switch to Diode IN/CKT and the range switch to X1. (Insure that the meter has been properly zeroed on this scale.) If the meter reads down scale, reverse the polarity switch. If the meter reads less than midscale, the diode under test is either open or shorted. The related circuit impedance of this test is less than 25 ohms.

PRECAUTIONS.–Transistors, although generally more rugged mechanically than electron tubes, are susceptible to damage by excessive heat and electrical overload. The following precautions should be taken in servicing transistorized equipment:

1. Test equipment and soldering irons must be checked to make certain that there is no leakage current from the power source. If leakage current is detected, isolation transformers must be used.
2. Ohmmeter ranges which require a current or more than 1 milliampere in the test circuit should not be used for testing transistors.
3. Battery eliminators should not be used to furnish power for transistor equipment because they have poor voltage regulation and, possibly, high ripple voltage.
4. The heat applied to a transistor, when soldered connections are required, should be kept to a minimum by using a low-wattage soldering iron and heat shunts, such as long-nose pliers on the transistor leads.
5. All circuits should be checked for defects before a transistor is replaced.
6. The power should be removed from the equipment before replacing a transistor or other circuit part.
7. When working on equipment with closely spaced parts, conventional test probes are often the cause of accidental short circuits between adjacent terminals. Momentary short circuits, which rarely cause damage to an electron tube, may ruin a transistor. To avoid accidental shorts, the test probes can be covered with insulation for all but a very short length of the tips.

CHAPTER 4

NTDS UNIT COMPUTER CP-642B/USQ-20(V)

The Digital Data Computer CP-642B/USQ-20(V) (fig. 4-1) is a general-purpose, stored-program, real-time, digital computer capable of processing large quantities of complex data where heavy input/output communication is required. The computer is suitable for such real-time applications as missile guidance and tactical control and display. It can be connected simultaneously to a variety of peripheral equipment. Such equipment includes teletypewriters, magnetic tape units, high-speed printers, card read/punch units, display and display interface equipment, radar and radar adapting interfaces, paper tape units, and manual entry devices. The computer is also capable of communicating with a wide variety of other asynchronous external devices in real-time applications. Other compatible peripheral equipment includes: video processors, various types of displays, digital-to-analog and analog-to-digital converters, X-Y plotters, and high-speed radio transmission links. Its primary use in the Navy today is as the unit computer for the Naval Tactical Data System.

CHARACTERISTICS

The CP-642B consists of four functional sections: control, arithmetic, memory and input/output and is capable of 30-bit (whole word) or 15-bit (half-word) computer word operation. These words are internally stored in one of three internal memory areas.

The computer has a valid repertoire of 62 flexible single address instructions that may be modified by seven index registers (B registers). The mathematical and logical operations are accomplished using parallel one's complement subtractive arithmetic. Its input/output section can communicate on 16 I/0 channels with provisions for high speed or low speed interface with all I/0 transfers in parallel. The internal real-time clock has a frequency of 1024Hz, and provisions are available for using an external clock.

FRONT PANEL CONTROLS

The maintenance and control console (fig. 4-2), located on the upper front of the computer, includes indicator lamps which display a detailed report of the internal status of the computer and controls to permit manual initiation of various operations. During normal operation, it is not necessary to monitor this panel.

The front panel shown in figure 4-2 has been divided into three sections (I, II, III) for ease of explanation.

Switches and Indicators

The maintenance panel provides manual controls for selecting the following special modes of operation:

1. Execution of one program instruction for each depression of a switch.
2. Execution of consecutive program instructions at a slow controllable rate.
3. Execution of one master clock phase each time a switch is depressed.
4. Execution of consecutive master clock phases at a slow controllable rate.
5. Operation that is normal except that the computer does not stop for a programmed STOP

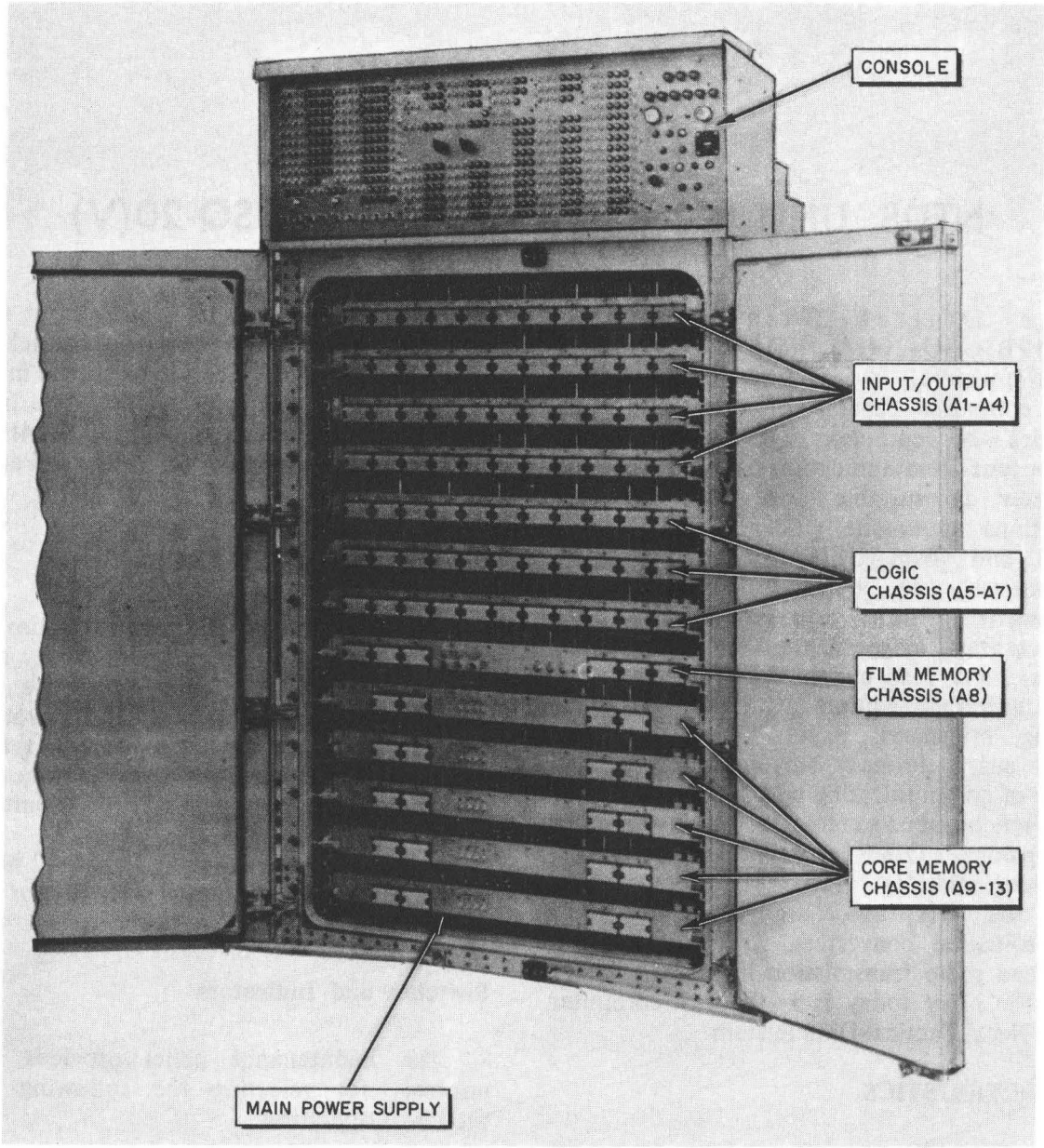

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Figure 4-1.—CP-642B/USQ-20(V) digital computer.

instruction (called abnormal high-speed operation).

Although the operation of the computer is automatic, the manual controls may be used to suspend normal operation of the computer without affecting subsequent operations. There are switches which are used to affect the entire computer operation, control parts of the computer operations, provide certain jump and/or stop conditions and govern speed of operation.

III II I

CHASSIS 1 CHASSIS 2 CHASSIS 3 CHASSIS 4

OD EK ACK
ID ACK
OD ACT
OD MON
ID ACT
ID MON
EF ACT
EF MON
MN PRI
SUB PRI
P

EF DESIGNATORS
MUL DIV SEQ
SUB SEQ
READ Y
STORE Y
INTERCHANGE 4
CLOCK PHASE

MAIN TIMING
ACTIVE SEQUENCE

K3
K2
C
R
B
S
Q
A
D
X
Z
U

RTC EI EF OD ID TRANS
EI EF OD ID FM EIM EFM ODM
DISCONNECT
JUMP
STOP
RTC ADV P B7 1 2 3 5 6 7

f j k b y

PRIMARY
26V DC
90V DC
54V DC
115V REGULATED
1 AMP
115V UNREGULATED
15 AMP
FUSE

ON
OFF
COMPUTER POWER
BLOWER POWER

FAULT
MARGINAL CHECK
LOCAL CONTROL
WARNING
RUN
COMPUTER ON TIME

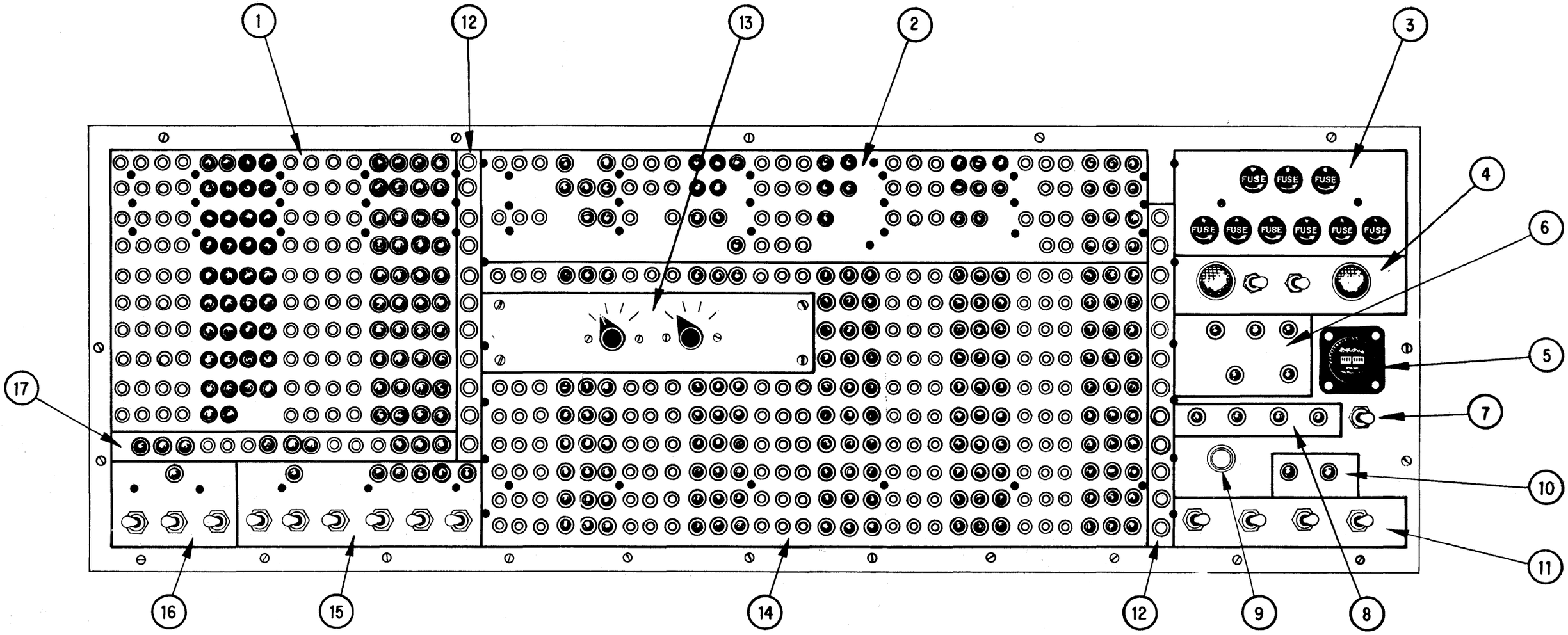
MODE
LOAD
PHASE STEP
OP STEP
RUN
MASTER CLEAR

RESTART SPEED CONTROL
PROGRAM I II

STOP
PHASE REPEAT
AUTOMATIC RECOVERY
START/ STEP

Figure 4-2.—CP-642B maintenance panel—Continued.

124.408



LEGEND:

1. 1/0 BIT INDICATORS
2. TIMING BIT INDICATORS
3. VOLTAGE FUSES
4. POWER CONTROLS
5. RUNNING TIME METER
6. STATUS INDICATORS
7. MASTER CLEAR
8. MODE INDICATORS
9. RESTART SPEED CONTROL
10. BOOTSTRAP PROGRAM INDICATORS
11. OPERATING CONTROLS
12. CLEAR PUSHBUTTON SWITCHES
13. C REGISTER SELECTOR SWITCHES
14. REGISTER BIT INDICATORS
15. JUMP/STOP INDICATORS & SWITCHES
16. DISCONNECT INDICATOR & SWITCHES
17. ADDRESS REGISTER INDICATORS

Figure 4-2.—CP-642B maintenance panel.

Mode Switches (Section I)

The computer is operative in any one of several modes (LOAD, PHASE STEP, OP STEP or RUN). The indicator-switch controls allow the operator to select a specific computer operating mode. Pressing the LOAD indicator-switch locks out all interrupts and places the computer in a condition for initial program loading from a selected peripheral device.

Pressing the PHASE STEP switch allows the computer to be operated on a one-clock-phase-at-a-time basis. This mode is normally used for maintenance.

Pressing the OP STEP switch allows the computer to execute one instruction at a time. This mode is usually used for program debugging.

Pressing the RUN indicator-switch (Section I) allows the computer to operate at normal high speed. Each of the mode indicator-switches will glow when depressed.

Start-Step/Restart (Section I)

Once a mode selection has been made, the computer is started by operating the START-STEP/RESTART switch. Table 4-1 summarizes the action performed by the various selections.

Stop (Section I)

The STOP switch, when operated, disables the high-speed operation of the computer. It also extinguishes the RUN indicator.

In computers where an applicable field change (modification) has been installed, the STOP switch in its UP position will effect Bootstrap Memory and inhibit Bootstrap Mode of operation. (These terms will be discussed in detail later.)

The PHASE REPEAT switch forces the repetition of the selected clock phase at a high-speed operation rate. The PHASE REPEAT switch is active only if the PHASE STEP mode has been selected.

Table 4-1.—Summary of RESTART/START-STEP switch functions

MODE	START-STEP	RESTART
Run	Initiates high speed operation	Allows self-recovery from program stops
Op Step	Allows the execution of one instruction each time the switch is operated	Allows initiation of one instruction at a repetition rate controlled by the RESTART SPEED CONTROL and low speed oscillator
Phase Step	Generates one clock phase each time the switch is operated	Generates clock phases at a rate controlled by the RESTART SPEED CONTROL and low speed oscillator
Load	Initiates high speed operation starting at address 00540 (executes bootstrap)	NOT USED

Automatic Recovery (Section I)

The AUTOMATIC RECOVERY switch directs the computer's activity after a program fault. In the up position, all interrupts are locked out, a jump is initiated to address 00540 and the selected Bootstrap program is executed.

If a program fault occurs with the switch in the center position, a jump to address 00000 is executed. The program starting at that address is then performed.

Master Clear (Section I)

With the computer not in the RUN mode, depressing the MASTER CLEAR pushbutton will clear (reset) most of the flip-flops in the computer, including the register indicators. If the computer is in the RUN mode, only the FAULT indicator will be cleared if the MASTER CLEAR switch is depressed. This feature prevents the computer from being inadvertently cleared during run.

Programs I and II (Section I)

The PROGRAM I or II pushbutton indicators are used to select the Bootstrap program which will be executed during manual initiation in the LOAD mode. They also indicate the Bootstrap program to be used when referenced by the AUTOMATIC RECOVERY switch, and they light the associated green indicator when selected.

Restart Speed Control

The RESTART SPEED CONTROL is a potentiometer that is used to vary the speed of operation when the computer is in the PHASE STEP or OP STEP modes and the START-STEP/RESTART switch is in the up position.

Run (Section I)

The green RUN indicator glows when the computer is in high-speed operation. Pressing the STOP switch during high-speed operation will extinguish the RUN indicator.

Fault (Section I)

The red FAULT indicator glows whenever the computer encounters a program fault or attempts to execute an instruction from control memory. Instruction function codes 00 and 77 are illegal and will cause a fault condition and a fault interrupt within the computer if they are executed. The FAULT indicator, once lighted, can be extinguished only by pressing the MASTER CLEAR switch.

Marginal Check (Section I)

The MARGINAL CHECK indicator indicates that the computer is in a memory margin check condition. Margin check will be discussed later in this chapter.

Local Control (Section I)

The LOCAL CONTROL indicator is lighted to indicate that the computer is being operated from the maintenance panel. The computer can also be operated remotely from another equipment. The remote equipment will be discussed in another chapter.

Overtemp Warning (Section I)

When lighted, the OVERTEMP WARNING pushbutton-indicator indicates an overtemperature condition inside the computer cabinet (115°F). When this temperature is reached, an overtemperature alarm horn sounds and can be reset by pressing the OVERTEMP WARNING pushbutton indicator.

C1-C2-C3-C4 (Section II)

The two C register rotary switches allow switching between the four C registers and the C register indicator-switches. The left switch permits the upper 15-bits to be displayed, and the right switch displays the lower 15-bits.

Register Indicator-Switches (Section II)

The indicator-switches labeled K3, K2, C, R, B, S, Q, A, D, X, Z and U display the bit

positions of the associated register. Each of the bit positions may be set manually, but the whole register must be cleared at the same time by the clear pushbutton to the right of the register. Most of these registers are not addressable by the program and are used for internal operations of the computer. The contents are displayed on the front panel for ease of troubleshooting.

Designator Indicator-Switches (Section II)

The designator indicator-switches are particularly useful when troubleshooting the computer if the technician is familiar with the information that is displayed in them. Generally, these indicators specify a timing point in a predetermined sequence of events. For example, the row of indicators labeled MAIN TIMING are the indicators for the flip-flops of the timing chain. Flip-flops of timing chains are identified by an abbreviation of the timing chain name and the flip-flop nomenclature (e.g., flip-flop 00T11/01T11 of the main timing chain becomes MTT11).

The timing chains shown on the front panel are:

(1) MAIN TIMING - main timing chain
T11 - T63
(2) c - C sequence
T11 - T63
(3) af - A final sequence
T41 - T63
(4) bf - B final sequence
T41 - T61
(5) Mul/Div Seq - Multiply/Divide/Square Root Subsequence
(6) SUB SEQ - made up of three minor timing chains-
Interchange AQ
Ready Y
Store Y

Each of the three timing chains and associated sequences will be discussed later in this chapter.

The indicators labeled ACTIVE SEQ are used to denote the sequence that is currently being performed: Af, Bf, Df, or I/0. The AfEn (A Final Enable) indicator, when set, indicates that the A final sequence has been enabled. In the Op Step mode this indicator-pushbutton must be depressed.

The EF DESIGNATORS lights are used to specify the channel number for external function acknowledges and output data acknowledges.

The r designator is used with a repeat instruction to specify how the operation is to be repeated. Bit 3 set indicates that the r designator is active, and bits 0 through 2 determine which of seven different methods is to be used. A detailed explanation of the functions of the r designator may be found in the operator's section of the appropriate technical manual.

The g designator is used for extended arithmetic operations. Each of the indicators is from a flip-flop in the arithmetic sequences that may or may not be set at various times:

a - Abort flip-flop
b - B = 0 flip-flop
ah - Arithmetic Hold flip-flop
bh - Bf Inhibit flip-flop

The CLOCK PHASE indicators specify which master clock phase is currently active During normal operation these indicators will al appear to be lighted due to the frequency of the clock.

I/O Indicator-Switches (Section III)

All the information displayed in these indicators deals with I/0 control signals. The I/0 channels are numbered 0 through 17_8 (right to left) with groups of four channels on each I/0 chassis. The control signals are labeled down one side of the array of switches. The following signals are from flip-flops that specify a particular function on the indicated channel.

(1) OD/EF ACK—Output Data/External Function Acknowledge
(2) ID ACK—Input Data Acknowledge
(3) OD ACT—Output Data Active
(4) OD MON—Output Data Monitor
(5) ID ACT—Input Data Active
(6) ID MON—Input Data Monitor
(7) EF ACT—External Function Active
(8) EF MON—External Function Monitor

The MN PRI indicators are for the main priority scheme of the computer, and they indicate which channel on which chassis has precedence.

The SUB PRI (subpriority) indicators are from flip-flops that determine the operating mode (input or output) of the I/0 section. The signal names for these indicators are:

(1) EI–External Interrupt
(2) EF–External Function
(3) OD–Output Data
(4) ID–Input Data
(5) FM–Fault Monitor Interrupt
(6) EIM–External Interrupt Monitor
(7) EFM–External Function Monitor
(8) ODM–Output Data Monitor

The TRANS (I/0 translator) indicators provide a visual indication of the current I/0 operating mode. The indicator labels mean:

(1) RTC–Real Time Clock
(2) EI–External Interrupt
(3) EF–External Function
(4) OD–Output Data
(5) ID–Input Data

All I/0 signals, what they do and how they operate, will be discussed later in this chapter.

The P register falls into the same category as the registers in section II of the front panel.

Disconnect (Section III)

The operation of the disconnect circuit involves an indicator and three switches. Selecting any of the three switches (RTC, ADV P, or B7) causes the red DISCONNECT indicator to glow. Selecting the B7 switch inhibits decrementing the B7 register during the repeat mode of operation. Selecting the ADV P switch inhibits the incrementing of the P register. Selecting the RTC switch inhibits incrementing the real-time clock.

Jump (Selective)

The red JUMP indicator glows when any or all of the three Selective Jump switches (1, 2, or 3) are selected. Selecting the switches allows manual selection or omission of predetermined program sections in conjunction with the 61 or 65 instructions. (See table 4-2.)

Stop (Selective)

The red STOP indicator glows when any or all of the Selective Stop switches (5, 6, or 7) are selected. Selecting the switches allows program monitoring when used in conjunction with appropriate 61 and 65 instructions. The red STOP 5, 6, or 7 indicators glow when a corresponding switch is selected, and another indicator glows when the program stop occurs.

Program Stop

The red 4-stop indicator will glow whenever the computer reaches a programmed stop other than a key stop (selective stop). This normally will be at the end of a subroutine when some action is required by the operator, such as supplying additional data required for the solution of the problem. Also, the stop at the end of a program is normally a 4-stop.

INSTRUCTIONS

A large repertoire of instructions (table 4-2) provides the means for directing the computer to perform the mathematical operations involved in solving problems in real-time. Single address instructions are employed, most of which have an execution time of 8 to 12 microseconds. The computer can also be instructed to perform the data processing necessary for initiating and maintaining communications between, or control of, compatible external equipment.

Short routines can be manually entered into the computer by operating the appropriate console controls. Lengthy programs are entered into computer via a peripheral device such as a punched paper tape reader or a magnetic tape unit.

The instructions contained in the program provide the computer with constants, decision-making capabilities, and an input/output capability. During operation, the program instructions are usually obtained from memory and performed in a sequential manner.

Table 4-2.—CP-642 function codes

a. f-MNEMONICS

OCTAL CODE	INSTRUCTION	MNEMONIC (MEMORY AID)	BRIEF DESCRIPTION OF OPERATION PERFORMED BY THE INSTRUCTION	SPECIAL CONSIDERATIONS
ØØ	(Fault interrupt)	ERR	Fault light; Ø → P Reg.	
Ø1	RIGHT SHIFT Q	R.SH.Q or RSH.Q	Shift (Q) right by Y; Sign extend Q_u, truncate Q_L	
Ø2	RIGHT SHIFT A	R.SH.A or RSH.A	Shift (A) right by Y; Sign extend A_u, truncate A_L	
Ø3	RIGHT SHIFT AQ	R.SH.AQ or RSH.AQ	Shift (AQ) right by Y; Sign extend A_u, truncate Q_L	
Ø4	COMPARE	COMP	Sense j; $(A)_j = (A)_f$	see table 4-2b
Ø5	LEFT SHIFT Q	L.SH.Q or LSH.Q	Shift (Q) left by Y; Q_u ends-around into Q_L	
Ø6	LEFT SHIFT A	L.SH.A or LSH.A	Shift (A) left by Y; A_u ends-around into A_L	
Ø7	LEFT SHIFT AQ	L.SH.AQ or LSH.AQ	Shift (AQ) left by Y; A_u ends-around into Q_L	
1Ø	ENTER Q	ENT.Q	Y → Q	
*	CLEAR Q	CLR.Q	Ø → Q	k = Ø, B = Ø, Y = Ø
11	ENTER A	ENT.A	Y → A	
*	CLEAR A	CLR.A	Ø → A	k = Ø, B = Ø, Y = Ø
12	ENTER B_j	ENT.B_n CLR.B_n	Y → B_j Ø → B_j	
*	NO OPERATION	NO.OP	---	j = Ø
13	----			13$\hat{k}$ = 3-max of 36 μsec 13$\hat{k}$ = Ø,1,2 - 8 μsec
*	EXTERNAL FUNCTION $C\hat{j}$ W/MONITOR	XF(M).C_n	Y → (14Ø + $C\hat{j}$); w(Y) → $C\hat{j}$ EF lines; internal interrupt when done	$\hat{k}$ = Ø
*	EXTERNAL FUNCTION $C\hat{j}$ W/MONITOR (FORCED)	XF(FM).C_n or XF (MF).C_n	Y → (14Ø + $C\hat{j}$); w(Y) (forced) → $C\hat{j}$ EF lines; internal interrupt when done	$\hat{k}$ = 1
*	EXTERNAL FUNCTION $C\hat{j}$	XF.C_n	Y → (14Ø + $C\hat{j}$); w(Y) → $C\hat{j}$ EF lines	$\hat{k}$ = 2
*	EXTERNAL FUNCTION $C\hat{j}$ (FORCED)	XF (F).C_n	Y → (14Ø + $C\hat{j}$); w(Y) (forced) → $C\hat{j}$ EF lines	$\hat{k}$ = 3
14	STORE Q	STR.Q	Q → Y	
*	COMPLEMENT Q	CPL.Q	$\overline{Q_n}$ → Q_n	k = Ø
15	STORE A	STR.A	$\overline{A}$ → Y	
*	COMPLEMENT A	CPL.A	$\overline{A_n}$ → A_n	k = 4
16	STORE B_j	STR.B_n	(B_j) → Y	j = Ø; STORES ZEROS IF k = Ø - 4
*	CLEAR Y	STR.Ø	Ø's → Y [store +Ø]	
*	SET Y	STR.1	1's → Y [store -Ø]	J = Ø; STORES ONES IF $\hat{k}$ = 5 - 7
17	----			17$\hat{k}$ = 2-max of 36 μsec 17$\hat{k}$ = Ø, 1 - 3 μsec 17$\hat{k}$ = 3 -12 μsec $\hat{k}$ = Ø,1
*	IF EXTERNAL FUNCTION BUFFER BUSY (OR NO EFR's) ON $C\hat{j}$, THEN JUMP	XF.BUSY.JP.C_n	IF $C\hat{j}$ busy; Y → P Reg.	
*	INPUT ONE WORD $C\hat{j}$: HOLD UNTIL RECV'D	INP(F)HOLD.C_n	$C\hat{j}$ INPUT → Y; force IDA; program holds until complete	$\hat{k}$ = 2
*	EXTERNAL INTERRUPT $C\hat{j}$ → Y	STR.X.INT.C_n	$C\hat{j}$ X.INT; (52Ø + $C\hat{j}$) → Y; enable $C\hat{j}$ X.INT	$\hat{k}$ = 3

Table 4-2.–CP-642 function codes–Continued

a. f-MNEMONICS (continued)

OCTAL CODE	INSTRUCTION	MNEMONIC (MEMORY AID)	BRIEF DESCRIPTION OF OPERATION PERFORMED BY THE INSTRUCTION	SPECIAL CONSIDERATIONS
2Ø	ADD A	ADD.A	(A) + Y → A	
21	SUBTRACT A	SUB.A	(A) - Y → A	
22	MULTIPLY	MUL	(Q)Y → AQ	
23	DIVIDE	DIV	(AQ) ÷ Y → Q; Remainder → A	
*	SQUARE ROOT	SQRT	$\sqrt{(AQ)}$ → Q; Remainder → A	k = 7 square root execution time = 52 μsec
24	REPLACE A + Y	RPL.A+Y	(A) + Y → A&Y	
25	REPLACE A - Y	RPL.A-Y	(A) - Y → A&Y	
26	ADD Q	ADD.Q	(Q) + Y → Q	see table 4-2c
27	SUBTRACT Q	SUB.Q	(Q) - Y → Q	see table 4-2c
3Ø	ENTER Y + Q	ENT.Y+Q	Y + (Q) → A	
31	ENTER Y - Q	ENT.Y-Q	Y - (Q) → Q	
32	STORE A + Q	STR.A+Q	(A) + (Q) → Y&A	
33	STORE A - Q	STR.A-Q	(A) - (Q) → Y&A	
34	REPLACE Y + Q	RPL.Y+Q	(Y) + (Q) → Y&A	
35	REPLACE Y - Q	RPL.Y-Q	(Y) + (Q) → Y&A	
36	REPLACE Y + 1	RPL.Y+1	(Y) + 1 → Y&A	
37	REPLACE Y - 1	RPL.Y-1	(Y) - 1 → Y&A	
4Ø	ENTER LOGICAL PRODUCT	ENT.LP	L[Y(Q)] → A	see table 4-2c
41	ADD LOGICAL PRODUCT	ADD.LP	L[Y(Q)] + (A) → A	
42	SUBTRACT LOGICAL PRODUCT	SUB.LP	L[Y(Q)] - (A) → A	
43	COMPARE MASK	MASK.COMP	(A) - L[Y(Q)] ; sense j; then (A) + L[Y(Q)] ; $A_i = A_f$	use normal j values (A) unchanged
44	REPLACE LOGICAL PRODUCT	RPL.LP	L[(Y)(Q)] → Y&A	see table 4-2c
45	REPLACE A + LOGICAL PRODUCT	RPL.A+LP	L[(Y)(Q)] + (A) → Y&A	
46	REPLACE A - LOGICAL PRODUCT	RPL.A-LP	(A) - L[(Y)(Q)] → Y&A	
47	STORE LOGICAL PRODUCT	STR.LP	L[(A)(Q)] → Y; $(A)_i = (A)_f$	(A) is not changed
5Ø	SELECTIVE SET	SEL.SET	Set $(A)_n$ for $Y_n = 1$	
51	SELECTIVE COMPLEMENT	SEL.CPL	Complement $(A)_n$ for $Y_n = 1$	
52	SELECTIVE CLEAR	SEL.CLR	Clear $(A)_n$ for $Y_n = 1$	
53	SELECTIVE SUBSTITUTE	SEL.SUS	$Y_n \rightarrow A_n$ for $(Q)_n = 1$	

Table 4-2.—CP-642 function codes—Continued

a. f-MNEMONICS (continued)

OCTAL CODE	INSTRUCTION	MNEMONIC (MEMORY AID)	BRIEF DESCRIPTION OF OPERATION PERFORMED BY THE INSTRUCTION	SPECIAL CONSIDERATIONS
54	REPLACE SELECTIVE SET	RPL.SEL.SET	Set $(A)_n$ for $Y_n = 1$; → Y&A	
55	REPLACE SELECTIVE COMPLEMENT	RPL.SEL.CPL.	Complement $(A)_n$ for $Y_n = 1$; results in Y&A	
56	REPLACE SELECTIVE CLEAR	RPL.SEL.CLR	Clear $(A)_n$ for $Y_n = 1$; → Y&A	
57	REPLACE SELECTIVE SUBSTITUTE	RPL.SEL.SUB	$(Y)_n \rightarrow (A)_n$ for $(Q)_n = 1$; → Y&A	
6Ø	JUMP (Arithmetic)	----	Jump to Y per special interpretation of j: also	see table 4-2d
*	CLEAR INTERRUPT LOCKOUT (J = Ø,1)	CIL CIL.JP	(If j = Ø) → CIL (If j = 1) → CIL; Y → P Reg.	
61	JUMP (Manual)	----	Jump to Y per manual keys 1, 2, or 3; Jump & Stop for keys 5, 6, 7 (See special j interpretation).	see table 4-2d
62	JUMP ON $C\hat{j}$ ACTIVE INPUT BUFFER	JP.INPACT.C_n	If input buffer busy $C\hat{j}$; Y → P Register	If jump condition is not satisfied, execution time is 4 μsec
63	JUMP ON $C\hat{j}$ ACTIVE OUTPUT BUFFER	JP. OUTACT.C_n	If output buffer busy on $C\hat{j}$; Y → P Register	
64	RETURN JUMP (Arithmetic)	----	(P Reg) → Y_L; NI at Y + 1 (special j interpretation)†	See table 4-2d
65	RETURN JUMP (Manual)	----	(P Reg) → Y_L; NI at Y + 1 (special j interpretation)†	If return jump condition is not satisfied, execution time is 4 μsec
66	----	(see following)	----	----
*	TERMINATE $C\hat{j}$ INPUT BUFFER	TERM.INP.C_n	terminate input buffer on $C\hat{j}$	$\hat{k} = Ø$
*	ENABLE ALL INTERRUPTS	ALL.INT	enable all internal (monitor) and external (equip status) interrupts	$\hat{k} = 1$, b = Ø
*	DISABLE ALL INTERRUPTS	NO. INT	disable all internal-external interrupts	$\hat{k} = 1$, b ≠ Ø
*	ENABLE ALL EXTERNAL INTERRUPTS	ALL.X.INT	enable all external interrupts	$\hat{k} = 2$, b = Ø
*	DISABLE ALL EXTERNAL INTERRUPTS	NO.X.INT	disable all external interrupts only; does not effect monitors	$\hat{k} = 2$, b ≠ Ø
*	ENABLE $C\hat{j}$ EXTERNAL INTERRUPT	X.INT.C_n	enable external interrupt on $C\hat{j}$	$\hat{k} = 3$, b = Ø
*	DISABLE $C\hat{j}$ EXTERNAL INTERRUPT	NO.X.INT.C_n	disable external interrupts on $C\hat{j}$ only; does not effect monitors	$\hat{k} = 3$, b ≠ Ø
67	----			
*	TERMINATE $C\hat{j}$ OUTPUT BUFFER	TERM.OUT.C_n	terminate output buffer on $C\hat{j}$	$\hat{k} = Ø$
*	TERMINATE $C\hat{j}$ EF OUTPUT BUFFER	TERM.XF.OUT.C_n	terminate external function buffer on $C\hat{j}$	$\hat{k} = 1$
*	TERMINATE ALL INPUT/OUTPUT/EF BUFFERS	TERM.ALL	terminate all buffers	$\hat{k} = 2$
7Ø	REPEAT	RPT	Repeat NI Y times (see special j interpretation)	see table 4-2e
71	B SKIP ON $B\hat{j}$	B.SK.B_n or BSK.B_n	If $(B\hat{j}) = Y$; skip NI, clr $B\hat{j}$ If $(B\hat{j}) \neq Y$; add 1 to $B\hat{j}$, execute Next Inst.	

†NOTE: On Return Jumps (64 & 65 instructions): P Reg contains current address when instruction is read from memory, but will contain address + 1 when instruction is executed.

Table 4-2.—CP-642 function codes—Continued

a. f-MNEMONICS (continued)

OCTAL CODE	INSTRUCTION	MNEMONIC (MEMORY AID)	BRIEF DESCRIPTION OF OPERATION PEFORMED BY THE INSTRUCTION	SPECIAL CONSIDERATIONS
72	B JUMP ON B_j	B.JP.B_n or BJP.B_n	If $(B_j) = Ø$; execute NI If $(B_j) \neq Ø$; subtract 1 from B_j, jump to Y	
73	INPUT BUFFER ON C_j (without monitor mode)	INP.C_n	$Y(k) \rightarrow (1ØØ + C_j)$; initiate input on C_j	
74	OUTPUT BUFFER ON C_j (without monitor mode)	OUT.C_n	$Y(k) \rightarrow (12Ø + C_j)$; initiate output on C_j	
*	EXTERNAL FUNCTION OUTPUT BUFFER ON C_j (w/o monitor)	XF.OUT.C_n	$w(Y) \rightarrow (14Ø + C_j)$; initiate EF output on C_j	$k = 2$
75	INPUT BUFFER ON C_j (with monitor mode)	INP(M)C_n	$Y(k) \rightarrow (1ØØ = C_j)$; initiate input on C_j; enable interrupt address $(4Ø + C_j)$	
76	OUTPUT BUFFER ON C_j (with monitor mode)	OUT(M)C_n	$Y(k) \rightarrow (12Ø + C_j)$; initiate output on C_j; enable interrupt address $(6Ø + C_j)$	
*	EXTERNAL FUNCTION OUTPUT BUFFER ON C_j (W/monitor)	XF.OUT(M)C_n	$w(Y) \rightarrow (14Ø + C_j)$; initiate EF output on C_j; enable interrupt address $(5ØØ + C_j)$	$k = 2$
77	(Fault interrupt)	FAULT	fault light; $Ø \rightarrow$ P Reg	

NOTE: This table is not compiler or assembler oriented in its use of MNEMONICS. The MNEMONICS used were selected to supply concise information on the machine language instruction. MNEMONICS starting as STR or RPL use the respective Store or Replace k-values. All others, except as noted, use the Read k-values.

b. k-MNEMONICS

NORMAL READ K-VALUES	MNEUMONIC
Read instructions (Ø1-12, 2Ø-23, 26, 27, 3Ø, 31, 4Ø-43, 5Ø-53, 6Ø-65, 7Ø-72):	
k = Ø: $\overline{Y}u$ = Ø's; $\overline{Y}L$ = Y	(blank)
k = 1: $\overline{Y}u$ = Ø's; $\overline{Y}L$ = (Y)L	L
k = 2: $\overline{Y}u$ = Ø's; $\overline{Y}L$ = (Y)u	U
k = 3: $\overline{Y}$ = (Y)	M
k = 4: $\overline{Y}u$ = same bits as Y14; $\overline{Y}L$ = Y	X
k = 5: $\overline{Y}u$ = same bits as Y14; $\overline{Y}L$ = (Y)L	XL
k = 6: $\overline{Y}u$ = same bits as Y29; $\overline{Y}L$ = (Y)u	XU
k = 7: $\overline{Y}u$ = (A)	A

For instructions 22, 52, and 53, k = 7 is not used.

Table 4-2.—CP-642 function codes—Continued

b. k-MNEMONICS (continued)

NORMAL STORE K-VALUES	MNEMONIC
Store instructions (14-16, 32, 33, 47):	
k = Ø: Store operand in Q.*	Q
k = 1: Store operand L in YL, leaving (Y)u undisturbed.	L
k = 2: Store operand L in Yu, leaving (Y)L undisturbed.	U
k = 3: Store operand in Y.	M
k = 4: Store operand in A.**	A
k = 5: Store complement of operand L in YL, leaving (Y)u undisturbed.	CPL*L
k = 6: Store the complement of operand L in Yu, leaving (Y)L undisturbed.	CPL*U
k = 7: Store the complement of operand in Y (storing the complement of Bj is the same complement as for a 30-bit register).	CPL*M

* A 14ØØØØØØØØ instruction complements (Q)
** A 15Ø4ØØØØØØ instruction complements (A)

REPLACE INSTRUCTION K-VALUES	MNEMONIC (Notes)
Replace instructions (24, 25, 34-37, 44-46, 54-57):	
k = Ø: Not used.	--
k = 1: Read portion - Yu = Ø's; YL = (Y)L. Store portion - Stores operand L in UL leaving (Y)u undisturbed.	L
k = 2: Read portion - Yu = Ø's; YL - (Y)u Store portion - Stores operand L in Yu leaving (Y)L undisturbed.	U
k = 3: Read portion - Y = (Y). Store portion - Stores operand in Y.	M
k = 4: Not used.	--
k = 5: Read portion - Yu = same bits as Y14; YL = (Y)L Store portion - Stores operand L in YL leaving (Y)u undisturbed.	XL (X in A only)
k = 6: Read portion - Yu = same bits as Y29; YL = (Y)u Store portion - Stores operand L in Yu leaving (Y)L undisturbed.	XU (X in A only)
k = 7: Not used	--

c. b-MNEMONICS

NORMAL b DESIGNATORS	MNEMONIC
b = Ø: Do not modify y.	(blank)
b = 1: Add (B1) to y.	B1
b = 2: Add (B2) to y.	B2
b = 3: Add (B3) to y.	B3
b = 4: Add (B4) to y.	B4
b = 5: Add (B5) to y.	B5
b = 6: Add (B6) to y.	B6
b = 7: Add (B7) to y.	B7

Table 4-2.—CP-642 function codes—Continued

d. j-MNEMONICS

NORMAL J VALUES	MNEMONIC	NOTE: These are the ship-MNEMONICS referred to in Table 4-2c.
j = Ø, Do not Skip NI (Next Instruction).	(blank)	
j = 1, Skip NI.	SKIP	
j = 2, Skip NI if (Q) is positive. *†	SKIP.Q.POS or SKIP.QP	
j = 3, Skip NI if (Q) is negative. *†	SKIP.Q.NEG or SKIP.QN	
j = 4, Skip NI if (A) + Ø (positive zero). †	SKIP.A.ZERO or SKIP.AZ	
j = 5, Skip NI if (A) ≠ Ø. †	SKIP.A.NOT.ZERO.or SKIP.ANZ	
j = 6, Skip NI if (A) is positive. †	SKIP.A.POS or SKIP.AP	
j = 7, Skip NI if (A) is negative. †	SKIP.A.NEG or SKIP.AN	

*If f = 4Ø or 44 and j = 2, skip if even parity. If f = 4Ø or 44 and j = 3, skip if odd parity.
†When f = 26 or 27, a special interpretation is given the values of j. They are:

j = 2, Skip NI if (A) is positive.	j = 5, Skip NI if Q is not zero.
j = 3, Skip NI if (A) is negative.	j = 6, Skip NI if Q positive
j = 4, Skip NI if Q is zero.	j = 7, Skip NI if Q negative

B-INDEX INSTRUCTIONS (12, 16, 71, 72)	NOTE: B-Index instructions do not utilize j values as skips
j = Ø, No index register-computer substitutes all zeros for a BØ.	
j = Ø, j value indicates B register (B_n is B_j)	

COMPARE (Ø4 INSTRUCTION)	MNEMONIC	NOTE: The following instructions use j-MNEMONIC instead of f-MNEMONIC for the instruction MNEMONIC in Table 4-2e.
j = Ø, Do not skip NI.	(blank)	
j = 1, Skip NI.	SKIP	
j = 2, Skip NI if Y ≤ (Q).	SKIP.Y.LE.Q	
j = 3, Skip NI if Y ≥ (Q)	SKIP.Y.GR.Q	
j = 4, Skip NI if Y ≤ (Q) and Y > (A).	SKIP.Y.OUT.AQ	
j = 5, Skip NI if Y ≥ (Q) or Y ≤ (A).	SKIP.Y.IN.AQ	
j = 6, Skip NI if Y ≤ (A).	SKIP.Y.LE.A	
j = 7, Skip NI if Y >(A).	SKIP.Y.GR.A	

ARITHMETIC JUMPS (6Ø & 64)	MNEMONIC (6Ø inst.)	MNEMONIC (64 inst.)
j = Ø, do not jump*	CIL	NO·RJP
j = 1, jump*	CIL·JP	RJP
j = 2, jump if bit 29 of Q-register clear	JP·Q·POS or JP·QP	RJP·Q·POS or RJP·QP
j = 3, jump if bit 29 of Q-register set	JP·Q·NEG or JP·QN	RJP·Q·NEG or RJP·QN
j = 4, jump if A-register clear	JP·A·ZERO or JP·AZ	RJP·A·ZERO or RJP·AZ
j = 5, jump if any bit in A-register set	JP·A·NOT·ZERO or JP·ANZ	RJP·A·NOT·ZERO or RJP·ANZ
j = 6, jump if bit 29 of A-register clear	JP·A·POS or JP·AP	RJP·A·POS or RJP·AP
j = 7, jump if bit 29 of A-register set	JP·A·NEG or JP·AN	RJP·A·NEG or RJP·AN

* Any enabled interrupt can be honored after CIL or CIL·JP is executed. When an interrupt is honored, all other interrupts are locked out until the next CIL or CIL·JP is executed. CIL or CIL·JP also clears bootstrap mode.

Table 4-2.—CP-642 function codes—Continued

d. j-MNEMONICS (continued)

MANUAL JUMPS (61 & 65)	MNEMONIC (61 inst.)	(65 inst.)
j = Ø, jump	JP	RJP·KEY or RJP·M
j = 1, jump if JUMP 1 switch up	JP·KEY1	RJP·KEY1
j = 2, jump if JUMP 2 switch up	JP·KEY2	RJP·KEY2
j = 3, jump if JUMP 3 switch up	JP·KEY3	RJP·KEY3
j = 4, jump; then stop	JP·STOP	RJP·STOP
j = 5, jump; stop if STOP 5 switch up	JP·STOP5	RJP·STOP5
j = 6, jump; stop if STOP 6 switch up	JP·STOP6	RJP·STOP6
j = 7, jump; stop if STOP 7 switch up	JP·STOP7	RJP·STOP7

Repeat (7Ø) Instruction - modifies NI by j while repeating NI by Y		MNEMONIC
	Read, Store, or read cycle of a Replace Inst.	store cycle when NI is a Replace Inst.
j = Ø, NI unmodified		(blank)
j = 1, Y of NI increased by 1 upon each successive re-execution of NI		INC
j = 2, Y of NI decreased by 1 upon each successive re-execution of NI		DEC
j = 3, Y of NI increased by b of NI upon re-execution of NI		B·INC
j = 4, NI unmodified	Y of NI modified by B6 during store sequence for Replace inst.	(B6)
j = 5, Y of NI increased by 1 upon each successive re-execution of NI	Y of NI modified by B6 during store sequence for Replace inst.	INC(B6)
j = 6, Y of NI decreased by 1 upon each successive re-execution of NI	Y of NI modified by B6 during store sequence for Replace inst.	DEC(B6)
j = 7, Y of NI increased by b of NI upon re-execution of NI	Y of NI modified by B6 during store sequence for Replace inst.	B·INC(B6)

NOTE: Modifications to NI do not change the NI as it is stored, only as it is executed.

Table 4-2e. MNEMONIC format

instruction MNEMONIC . k-MNEMONIC (B_n + Y). skip MNEMONIC

However, a program decision may direct the computer to either skip an instruction or to exit from the present routine and enter another. The routine is terminated when either a predetermined event or conclusion is reached, or when all of the instructions have been performed.

Terms and Symbols

Before a discussion of instruction word format, there are some terms and symbols that should be completely understood. These terms and symbols are not particularly unique to the CP-642B computer but may be found in some of the other data processing systems throughout the Navy and civilian business world.

The symbol ⇒ should be interpreted as "means" or "implies that." (e.g., 1 ⇒ one).

The symbol *a* is to be interpreted as meaning any register or memory location.

(a)	⇒	the content of *a*.
(a)i	⇒	the initial content of *a*.
(a)f	⇒	the final content of *a*.
a_n	⇒	the n^{th} bit of *a*.
$(a)_n$	⇒	the n^{th} bit of the content of *a*.
a_u	⇒	the upper 15-bits of *a*.
a_L	⇒	the lower 15-bits of *a*.
operand	⇒	that which is operated upon.
y (lower case)	⇒	operand designator–lower 15-bits of the instruction word–U_L
Y (upper case)	⇒	address of the operand–usually formed by y + (index register)
(Y)	⇒	the contents of memory address Y
$\underline{Y}$	⇒	the operand (regardless of source)
$L\underline{Y}$ (a)	⇒	the logical product of $\underline{Y}$ and the contents of a register or memory location.

Instruction Word Formats

An instruction word for the CP-642B Computer is made up of parts called designators. Each designator specifies a particular function for the computer to perform for that specific instruction. The CP-642B uses a fixed instruction word length of 30-bits divided into five designators labeled f, j, k, b and y.

There are two types of formats for the CP-642B instructions, Format I or normal and Format II or input/output. A general format for the instruction words and associated explanations for the designators are shown in table 4-3.

FUNCTION CODE DESIGNATOR (f).–The f designator (bits 2^{29} - 2^{24}) is always the upper six bits of the instruction word. It specifies the general operation to be performed by the computer. All values from 01 - 76 inclusive are defined in the instruction repertoire (table 4-2). Codes 00 and 77 are illegal function codes and if executed cause a fault interrupt and a jump to the address specified by the setting of the AUTOMATIC RECOVERY switch.

BRANCH CONDITION DESIGNATOR (j).–The j designator (bits 2^{23} - 2^{21}) of a normal instruction word is primarily used for jump and skip determinations (if certain predetermined conditions are satisfied), for index (B) register specification (for certain instructions) and for repeat status interpretation (for certain other instructions). Examples of skip determinations for some function codes are shown below:

j = 0–Do not skip the next instruction (NI)

j = 1–Skip NI

j = 2–Skip NI if (Q) is positive

j = 3–Skip NI if (Q) is negative

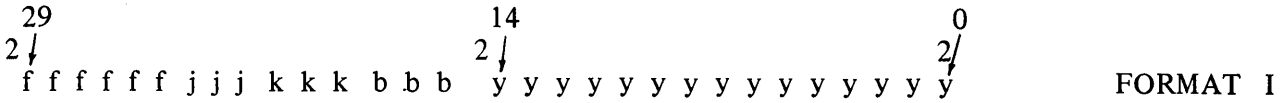
j = 4–Skip NI if (A) is zero (positive zero)

j = 5–Skip NI if (A) is non-zero

j = 6–Skip NI if (A) is positive

j = 7–Skip NI if (A) is negative

Table 4-3.—Instruction word format



FORMAT I (Normal)

FORMAT II (I/O)

Designator	Name	Interpretation	
		Format I	Format II
f	Function code designator	Specifies operation to be performed by instruction	Same
j	Branch condition designator	(1) Jump or skip operations (2) Index (B) register specification (3) Repeat	Specifies I/0 channel number Called $\hat{j}$ (j cap or j hat)
k	Operand interpretation designator	Specifies where the operand is to come from and/or where it is to be stored	Same Called $\hat{k}$ (k cap or k hat)
b	Address modification designator (index designator)	Specifies B register to be used for address modification	Same
y	Operand designator	May be the operand or the address of the operand	Same

Specific examples of j values may be found in the technical manual in section three. When the branch condition involves the sign of the quantity in A or Q, the evaluation examines the sign bit; therefore, positive zero (all zeroes) is considered a positive quantity, and negative zero (all ones) is considered a negative quantity.

For input/output instructions, the $\hat{j}$ designator (table 4-3) (bits 2^{23} - 2^{20}) specifies the channel number for that instruction. Bit 2^{23} assumes a value of eight, bit 2^{22} a value of four, bit 2^{21} a value of two and bit 2^{20} a value of one; thus, the $\hat{j}$ designator provides for all channel numbers from $0 - 17_8$. See the technical manual, section three, for details on which instructions use the j designator.

OPERAND INTERPRETATION DESIGNATOR (k).—The k designator (bits 2^{20} - 2^{18}) specifies for the function code exactly where the operand (that which is to be operated on) will come from before and where it will be stored after the instruction is executed and whether it is 15 or 30-bits in length. The k designator functions directly with the y designator to obtain the correct values.

The $\hat{k}$ designator occupies only bits 2^{19} and 2^{18} since it is used in I/0 instructions only and the $\hat{j}$ designator uses bit 2^{20}. The k designator performs essentially the same function for I/0 instructions that the $\hat{k}$ designator does for normal instructions.

The operand interpretation is made for the three classes of instructions that the CP-642B computer uses: Read, Store and Replace. Those instructions that read an operand but do not replace it after the arithmetic is performed are called Read instructions. Those instructions that do not read an operand but store it are called Store instructions. Instructions which do both are called Replace instructions.

Store class instructions in the Repertoire of Instructions have STR as the first 3 letters of the MNEMONIC code, and Replace instructions are identified by RPL as the first 3 letters of the MNEMONIC code. All other codes are classified as Read Instructions.

Examples of k designator uses in a normal instruction are shown below:

k = 0 — Store operand in Q. (A 1400000000 instruction complements (Q).)

k = 1 — Store operand L in YL, leaving (Y)u undisturbed.

k = 2 — Store operand L in Yu, leaving (Y)L undisturbed.

k = 3 — Store operand in Y.

k = 4 — Store operand in A. (A 1504000000 instruction complements (A).)

k = 5 — Store complement of operand L in YL, leaving (Y)u undisturbed.

k = 6 — Store the complement of operand L in Yu, leaving (Y)L undisturbed.

k = 7 — Store the complement of operand in Y (storing the complement of B, is the same complement as for a 30-bit register).

INDEX DESIGNATOR (b).—The b designator (bits 2^{17} - 2^{15}) is used to specify which, if any, of the index registers (B) will be used to modify the operand designator, y, to form Y = y + (Bb). This operation exploys an additive accumulator; therefore, a quantity consisting of all zeroes cannot result unless the bits of both y and (Bb) are all zeroes.

The effects of the various values of the b designator are as follows:

b = 0 — Do not modify y.

b = n — Add (Bn) to y. (n = 1 through 7).

OPERAND DESIGNATOR (y).—The operand designator (bits 2^{14} - 2^0) may be the operand or the address of the operand depending on the function code and the value of k. If it is the address of the operand, it is usually added to the value in the index register specified by the b designator to obtain a final address.

In the operator's section of the technical manual, there is a table that explains fully the

operations performed by each of the instructions and includes the operations of each designator for a particular function code. You should refer to this table or a repertoire card when attempting to program the computer. DO NOT ATTEMPT TO MEMORIZE THE INSTRUCTIONS.

SIMPLIFIED BLOCK DIAGRAM

Figure 4-3, the simplified block diagram of the CP-642B, shows the primary signal transfer paths between the four computer sections.

Control Section

The control section contains the registers, designators, modifiers and special circuits necessary to control the main timing of all computer operations; obtain the instruction words and operands from memory; direct arithmetic functions; make jump, skip or abort decisions; and to respond to manual intervention.

Main timing control is achieved through the main timing sequences. A free running timing chain generates the timing signals for such events as initiating memory functions, skip decisions and other functions which require regulated timing. Sequencing is closely associated with main timing and is accomplished through eight sequence control flip-flops which provide main timing function control enables (called A, B, D and I/O enables). When combined with the main timing signals, these enables supply the commands for computer operation.

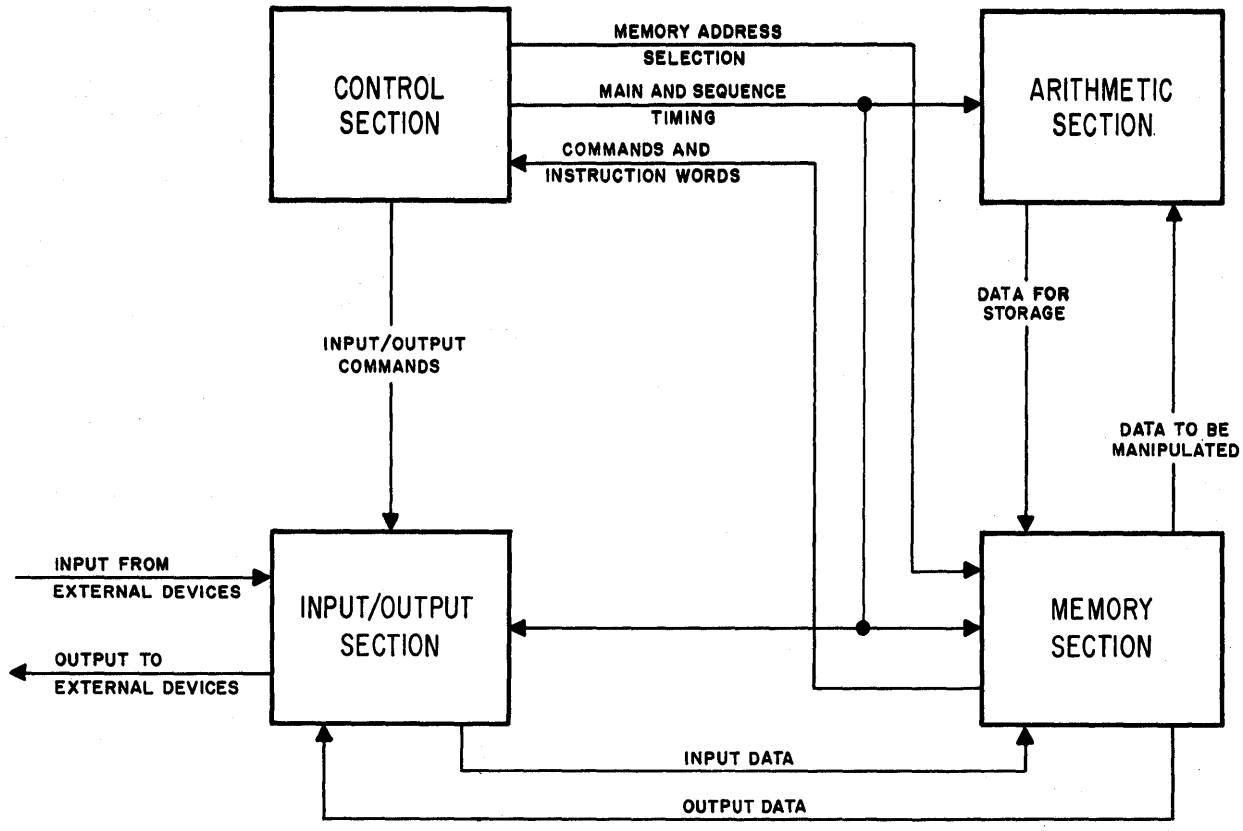


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Figure 4-3.–CP-642B simplified block diagram.

Arithmetic Section

The arithmetic section contains the registers and modifiers required to perform the arithmetic or other logic operations specified by the instruction word. Communication between the arithmetic section and the other sections of the computer is primarily through the X and D registers. The registers of the arithmetic section hold the data to be manipulated and provide temporary storage for the result. The main matrix of the arithmetic section is the arithmetic subtractor which provides the logical sum or difference of the data contained in the X and D registers. The arithmetic section also contains auxiliary timing circuitry to control such arithmetic functions as multiply, divide, square root, and shifting, which require additional function time.

INPUT/OUTPUT SECTION

The input/output section, normally referred to as the I/0 section, provides the communication path which enables the computer to process data in conjunction with peripheral equipment. Cables provide the connections for channeling information from the computer to the external devices, and for the transfer of information from these devices to the computer. Several memory locations are reserved to contain the operating capabilities for the I/0 channels. Internal control functions and timing provide the enables to perform essentially independent operation of the I/0 section once the mode of operation is initiated by the computer control section. The two modes of operation are input and output.

The input mode of operation is initiated when the computer requests input data from associated external devices. On signal, a specific channel is enabled, and the transfer of data is accomplished.

The output mode of operation is initiated when the computer specifies the transfer of data to an external device. The output channel associated with the designated device is enabled and the data transferred to the device.

The I/0 section contains a priority system for channel activation, allowing the highest numbered channel the highest priority. A subpriority is established which is dependent upon the function to be performed. These functions, in the descending order of priority, are real-time clock, external interrupt, external function, output data, and input data.

MEMORY SECTION

The memory section supplies the storage capability of the computer, the logic circuitry to write information into this storage, and the read circuitry to retrieve the information from storage. The memory section is capable of storing 32,768 30-bit words and consists of three distinct memory systems. Each of these systems, main memory, control memory, and bootstrap, is associated with the storage of a particular type of information.

Main Memory

The main or core memory contains 32,672 storage locations. Ninety-seven of these locations are special purpose and provide seven distinct functions. Table 4-4 lists these functions and the memory addresses with which they are associated. All other main memory locations are used for instruction and data storage. The main memory has a read-restore cycle time of four microseconds.

Control Memory

Control memory, a variable, thin-film memory, serves as the storage medium for indexing and input/output control. It consists of 64 storage locations, with a read-restore cycle time of 667 nanoseconds. Fifty-six of the storage locations are used for specific I/0 functions and are listed in table 4-4.

Bootstrap Memory

The bootstrap memory is a 667-nanosecond permanent memory consisting of 64 30-bit words. This memory provides for the automatic initial-loading of programs, or for automatic recovery in the event of program failure. There are 32 address locations in the bootstrap memory, but there are two 32-word permanent storage programs. Either of the programs can be

Table 4-4.—Memory Assignment

MEMORY	MEMORY ADDRESSES	FUNCTION
Main	00000	Fault Entrance
	00001 - 00017	Unassigned
	00020 - 00037	External Interrupt Entrance
	00040 - 00057	Input Monitor Interrupt Entrance
	00060 - 00077	Output Monitor Interrupt Entrance
Control	00100 - 00117	Input Buffer Control Registers
	00120 - 00137	Output Buffer Control Registers
	00140 - 00157	External Function Buffer Control Registers
	00160	Real-Time Clock
	00161 - 00167	B1 through B7 Index Registers
	00170 - 00177	Unassigned Film Locations
Main	00200 - 00477	Unassigned Core Locations
	00500 - 00517	External Function Monitor Interrupt Entrance
	00520 - 00537	External Interrupt Code Storage
Bootstrap	00540 - 00577	NDRO Bootstrap Program I
	00540 - 00577	NDRO Bootstrap Program II
Main	00600 - 00617	Intercomputer Time-Out Interrupt Entrance
	00620 - 77777	Unassigned Core

manually selected. The addressing of the memory is controlled by the SØ register, and data is read out of the bootstrap memory via the ZØ register. The routines stored in bootstrap memory are fixed at the time of manufacture and cannot readily be altered.

Where an address has been identified as Control or Bootstrap memory, the use of Main memory for that address has been suppressed and either a thin-film or hardwired (belt buckle) memory substituted respectively. Control (thin-film) memory is faster than Main memory, but is inhibited internally from being read up as an instruction (a forced ØØ code occurs in the upper 6 bits when this is attempted). When addresses 161-167 are referenced as B-Indexes, the upper 15 bits of the address are automatically cleared. In other modes of addressing, all 30 bits of control memory can be utilized as a normal memory cell. Bootstrap (belt buckle) memory is normally referenced as a constant. Belt buckle memory cannot be modified by attempting to store data into that memory location. Bootstrap I or Bootstrap II are available at the throw of a switch on the front panel. If the AUTO switch is elevated to the UP position and left there, belt buckle memory will be suppressed entirely and Main Memory is available with no restrictions for these addresses (main memory for address

00540-00577 is called SHADOW MEMORY when Bootstrap memory is suppressed in this fashion).

CONTROL SECTION FUNCTIONAL BLOCK DIAGRAM

The control section of the computer, figure 4-4, allows computer operation under either manual or program control through the generation of specific sequencing and enables. During manual operation, circuit conditions are displayed on the operator's control panel. Control of these conditions is accomplished through the use of pushbutton switch-indicators and several control switches which allow stepping slowly through various functions in performing an instruction. During this procedure, a study can be made of the lighted indicators to isolate possible logic malfunctions.

Under program control, the computer performs instructions of an entire program at a high rate of speed, stopping only at programmed stops. During either manual or program control, the control section supplies timing, translation, and sequencing required for all computer functions.

Instruction Word Translation

The U register holds the instruction that is presently being executed. It receives its input from the memory data register (Z) and effectively breaks the instruction word down into its five components: f, j, k, b and y.

Function Code Translation

Because the instruction word is transferred to and stored in the U register, the upper six bits of U provide the inputs to the f code translator. The f translation is accomplished in three general areas. Some circuits translate for the upper octal digit of f, some translate for the lower digit and still others combine these two digits to translate for the specific value of f.

Although there is no f register, the upper six bits of the U register are arbitrarily assigned bit identification with f. This assignment is made as shown below.

U REGISTER BIT	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
f TRANSLATOR BIT	2^5	2^4	2^3	2^2	2^1	2^0

Thus, the set or cleared condition of a U register bit will reflect a like condition of the corresponding f bit. Assume, as an example, that bits 2^{27}, 2^{25} and 2^{24} are set in the U register. This will reflect a set condition of f bits 2^3, 2^1, and 2^0 and result in an $f = 13_8$ code.

U REGISTER BIT	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	
BIT							001 011 = 13_8
CONTENT	0	0	1	0	1	1	
f TRANSLATOR BIT	2^5	2^4	2^3	2^2	2^1	2^0	

Branch Condition Designation Translation

The branch condition designator, j, translation works in the same manner as the f code translator and produces enables to appropriate circuits throughout the computer. The uses of the j and $\hat{j}$ designators have been discussed previously.

Operand Interpretation Translation

The operand interpretation designator, k, specifies the manner in which the operand is treated. Outputs from these stages are applied to the k translator for interpretation. The k translator translates for the value of the k designator and combines this value with values of f to provide specific function translation.

Index Modification Translation

The b designator specifies which B register, if any, is to be used to modify the operand designator, y. The seven B registers used for indexing/incrementing/decrementing are

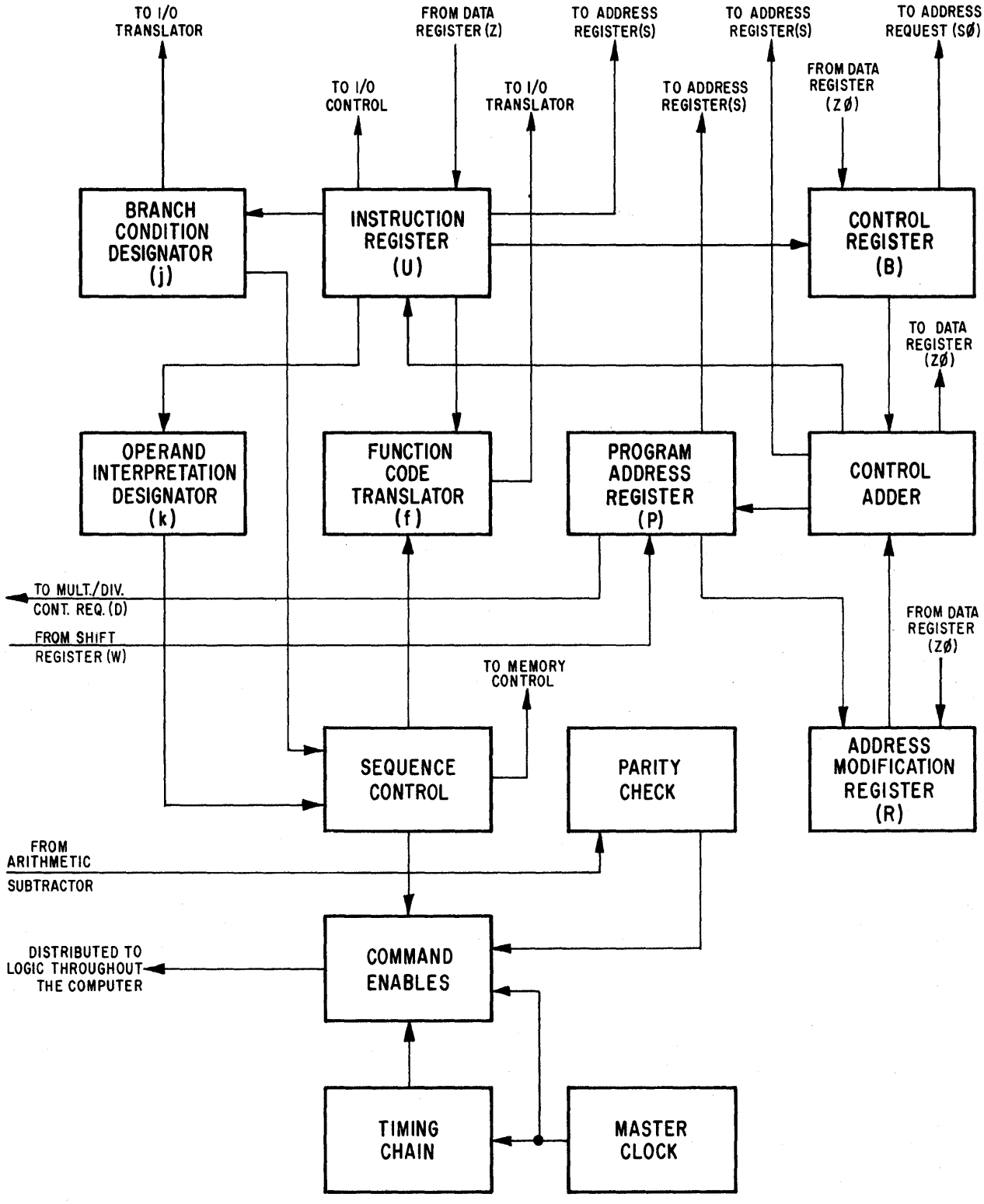

Figure 4-4.–Control section functional block diagram.

actually addresses in the control memory. A word is read from the control memory by transmitting its address to the SØ register. The SØ register translates the address bits so the proper address is referenced. In the case of a B register selection, U15, U16, and U17 are transmitted to the SØ register with the result that the address specified by the b designator is read up. The content of the control memory address specified by the b designator is read up. The contents of the control memory address specified by the b designators are referred to as Bb. If b = 0, no Bb is referenced and y is not modified. The modification of y is done by adding Bb to y to form a new quantity referred to as Y.

Operand Address Interpretation

The operand address designator, y, is the lower 15 bits of the instruction word stored in U. Although its usual function is to specify the memory address for reading or storing the operand, it can also be used for other functions. The two conditions that specify the use of y are the instruction being performed and the value of the k designator. The f codes have been divided into three groups, each utilizing k in a different manner.

For read instructions, when k = 0 or 4, y + Bb is used directly as the 15-bit operand and no memory reference is made. When k = 7, the contents of the A register are used as the 30-bit operand. In this case y is not used, and again no memory reference is made. When k = 1, 2, 3, 5, or 6, y + Bb specifies the memory location of the operand.

For store instructions when k = 0 or 4, y is not used, as the operand is stored directly in the Q register or the A register, respectively. When k = 1, 2, 3, 5, 6, or 7, y + Bb specifies the memory location for storage.

For replace instructions, when k = 1, 2, 3, 5, or 6, y + Bb specifies the memory location of the operand. After operations specified by the instructions are completed, the result is returned to memory address y + Bb. The values of k = 0, 4, and 7 are not used for replace instructions.

A memory address is selected by transmitting Y to the S register. The S register and its associated translator select the specific memory address.

Summary

An instruction word is a 30-bit quantity read from memory and contained in the U register. It is composed of f, j, k, b, and y designators. The f designator specifies the function to be performed; y is used in selecting the memory address of the operand (or may be the operand); j, k, and b designators are used to modify and/or control the functions of the instruction.

Timing and Sequence Control

Computer timing and operation are dependent primarily upon clock timing pulses, generated by the master clock, and enables generated by instruction format and switch settings.

Sequence control, resulting from the interpretation of the instruction word, generates command enables to allow sequential control of computer operation to perform the directed task.

MASTER CLOCK.—The master clock (basically a delay line oscillator) normally operates at a high rate of speed and generates timing pulses for the computer. However, under certain mode selections, the speed of the master clock is controlled by the setting of the lower speed oscillator or RESTART SPEED CONTROL on the operator's front panel.

The period of the master clock is about 680 ns (fig. 4-5). Within this period are four evenly-spaced pulses called clock phases (Ø). Each clock phase is an L for about 130 ns (measured at the 50% amplitude points of the clock phase waveform).

Console Controls

The console controls supply inputs to the logic of the computer and to indicators that monitor operation.

A remote panel may be used to control the computer. When this remote panel has active control of the computer, the computer controls are inhibited from the remote panel. The

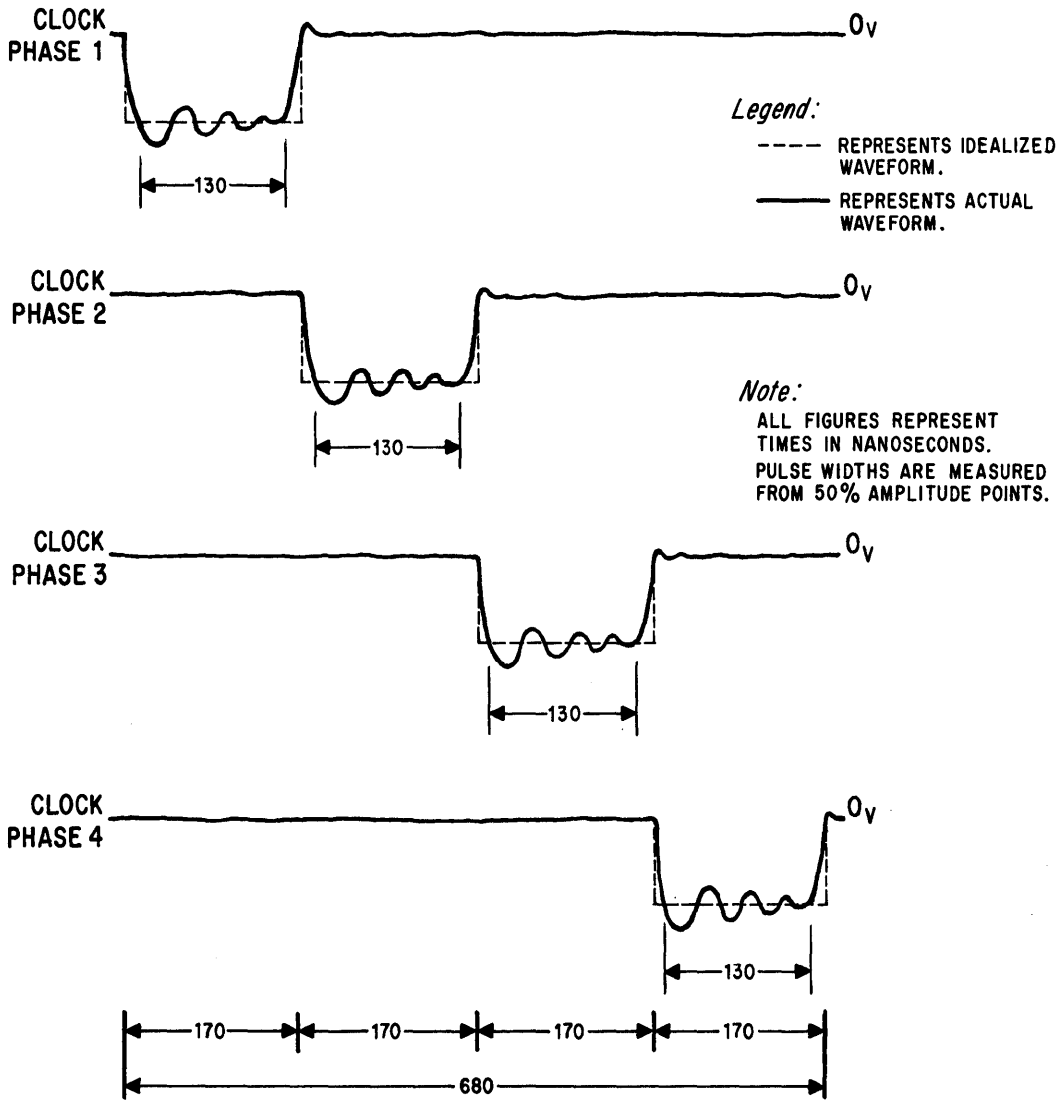

Figure 4-5.–Master clock outputs, idealized waveform.

operation and results of the controls are the same for remote control or local (computer) control. Console controls are not shown in figure 4-4.

Main Timing

The main timing circuitry consists of 12 flip-flops which, under direction from the sequence control circuit, provide timing enables to perform instructions.

Main timing is functionally divided into two time divisions, MTi (initial main timing) and MTf (final main timing). The events controlled by each division are dependent upon the enables received from the sequence control circuits.

MTi.–MTi consists of six flip-flops and operates with the A, B, and D enables from sequence control or from the function or other designators. For example, when MTi operates with Ai enables, the next instruction is read

from the selected memory address and placed in U. This sequence occurs for each instruction. When MTi operates with Bi or Di enables, most computer functions are further enabled through function code translation or by other designators.

MTf.–MTf consists of six flip-flops and operates with enables from sequence control. MTf provides timing for the store portion of replace and return jump instructions. It also provides timing for miscellaneous functions of other instructions.

Sequence Control

Sequence control consists of eight flip-flops that provide enables (primarily to MT) to accomplish certain events. There is an enable flip-flop that allows operation to begin and recycle if certain conditions exist. An Input/Output Request flip-flop provides enables to accomplish the I/0 function and to inhibit non-I/0 functions. The six remaining flip-flops that are used for non-I/0 functions are labeled according to the sequence they are used with: Ai (A sequence initial), Af (A sequence final); Bi; Bf; Di; Df.

Each instruction is executed according to the sequence of operation for automatic operation of the computer. The main timing chain with A sequence enables from sequence control will read the next instruction and perform preliminary operation modification. MT with B enables obtains the operand and initiates arithmetic functions. MT with D enables performs the store functions for certain store instructions.

There is a C sequence that is run independently of MT. It provides timing to perform the arithmetic and logical functions specified by the current instruction. It also initiates the following subsequences:

Read Y–obtains the specified operand
Store Y–controls the store function
Interchange AQ–controls interchange of contents of A and Q.

The C sequence may also initiate the multiply/divide/shift sequence which enables setting the Arith Hold flip-flop for certain shift instructions or multiply, divide or square root instructions. The C sequence also enables the skip evaluation to be made for the instructions that require functions controlled by the C sequence and initiates the commands that transfer data between registers and modifying circuits.

Refer to the appropriate technical manual for detailed explanations of all sequences and subsequences.

Control Adder

The control adder is used with the registers of the control section to modify the contents of those registers (normally address modification). The control adder is an additive matrix that may be used as an adder or counter. The normal adder operation is altered by preventing end-around carries to produce a counter circuit. During adder operations (+1) + (-1) = +1. During counter operations (+1) + (-1) = +0.

Program Address Register

The program address register, P, is used to store the address of the memory location to be referenced. Through use of the R register and the control adder, the contents of P are incremented to provide successive memory addressing.

Control Register

The control register, B, is used to increment the contents of P through use of the SET B = +1 command. Through the control adder, the B register also functions as an adder input register to update the contents of UL or Z. This B register (control register) SHOULD NOT BE CONFUSED with the seven B registers (index registers) contained in memory.

Address Modification Register

The R register is used to modify the contents of the P register through use of the

control adder. Inputs are from either the P or Z register with an output to the control adder for modification by the contents of the B register.

ARITHMETIC SECTION

The arithmetic section contains the logic required to perform such operations as add, subtract, multiply, divide, square root, parity, shifting and other logical or arithmetic functions. The arithmetic section functions under commands from the control section (primarily the C sequence).

All arithmetic operations, except for square root, are performed with either positive or negative numbers identified by bit 29, called the sign bit. If the number to be manipulated is negative, the sign bit is set (1). For positive numbers the sign bit is clear (0). Initial and final sign corrections assure the correct sign of the result. For square root operations, no sign bit is used, and the entire 30 bits are treated as a positive number. Shifting operations are performed during the transfer of data between registers and/or selectors.

The timing of arithmetic functions such as multiply or divide is controlled by a timing chain which is initiated by the C sequence. Those functions which require an unusually long time for performance set the Arith Hold flip-flop, which inhibits other operations until the completion of the arithmetic process.

Registers

Figure 4-6, the arithmetic section functional block diagram, illustrates registers, the subtractor, selectors, shift counters and shift control.

The A register is called the accumulator (a register in which the result of an arithmetic or logic operation is formed). It is a 30-bit addressable (may be addressed by the program) register. It holds the augend prior to and the sum after the add operation. For the subtraction operation it holds the minuend before and the difference after. There are other add and subtract operations that do not use the A register (e.g., ADD Q, SUBTRACT Q).

The D register is an exchange register used internally in the arithmetic section. It is nonaddressable and 30 bits in length. The D register holds the addend or subtrahend in add or subtract operations.

The add operation is typical of the relationship between the A and D registers. The augend and addend are initially contained in A and D. Before the addition is performed, (A) is transmitted to X. X and D are then combined by the subtractor network (complement arithmetic) to form the sum of the two numbers in a parallel manner, and the result is transferred to A.

The Q register is also a 30-bit addressable register that is used primarily during multiply and divide operations. The A and Q registers may be combined to form a 60-bit addressable register that will hold the product after multiplication or a 60-bit dividend prior to division operations. The contents of A and Q may also be shifted left or right, either individually or as one double-length 60-bit word. The Q register holds the multiplier prior to multiplication or the quotient after division (the remainder is sent to A).

The X and W registers are 30-bit nonaddressable registers. These registers are used for the exchange of data within the arithmetic section and for communicating with the remaining sections of the computer. The W-register is not displayed on the control panel of the computer; the A-, Q-, X-, and D-registers have indicators which allow the operator to inspect the contents of these registers during debugging and maintenance operations.

The S1 and S2 selectors are control gates that allow an increased number of inputs to A and W to be used.

The K registers (K1, K2, K3) function as a shift counter for all arithmetic operations that involve shifts (multiply, divide, square root and shift instructions).

Subtractor

The subtractor is a logic matrix that combines the contents of the X and D registers to produce the difference or logical sum of their outputs. The subtractor uses one's complement binary arithmetic.

The logic of the subtractor accepts the input from the D register in complemented form to perform its operation. This may be shown as:

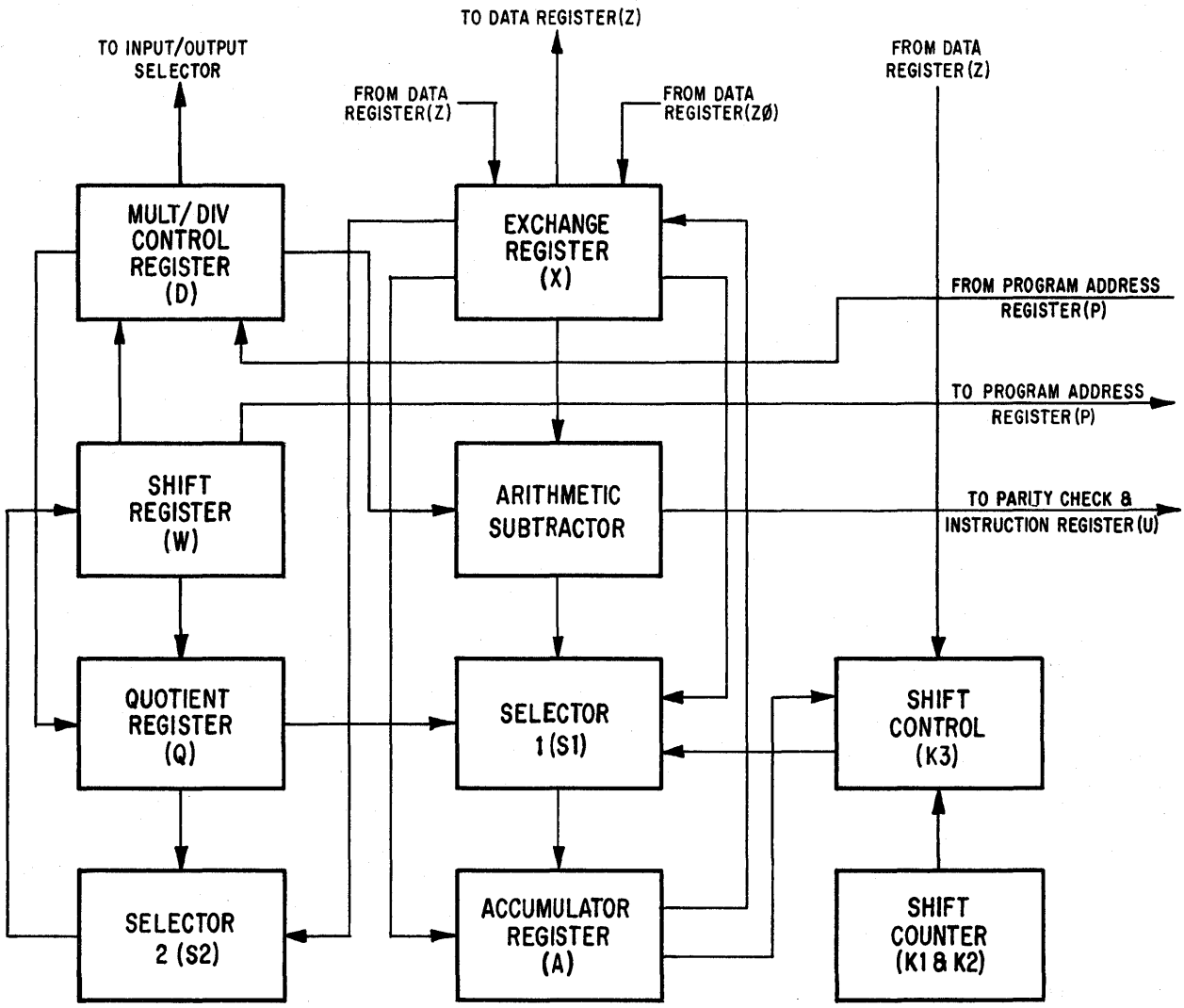

Figure 4-6.—Arithmetic section functional block diagram. **164.173**

X - (-D)

D REGISTER COMPLEMENT

SUBTRACTIVE PROCESS

OR X + D EQUIVALENT PROCESS

The arithmetic process of addition is thus performed by the subtractor. If subtraction of two numbers is directed, the complement of the subtrahend is initially placed in the D register, and the operation thus becomes:

X - (-D′)

COMPLEMENT OF SUBTRAHEND

APPARENT COMPLEMENT

SUBTRACTIVE PROCESS

OR X - D EQUIVALENT PROCESS

The operation of the subtractor is divided into two parts, the formation of the half-subtract (HS), and the sensing and performing of any borrows which are present. Although both functions occur at the same time, they will be explained separately.

The half subtract result is formed in a bit-by-bit subtraction with no regard for borrows. Table 4-5 shows the four possible input combinations to a subtractor stage and their HS and $\overline{HS}$ results. $\overline{HS}$ is the complement of HS.

The first entry in table 4-5 shows the contents of both the X and D registers as 1. The subtractor performs a 1 - 0 operation (the subtractor actually uses D′) to produce an HS of 1. The second entry also produces an HS of 1. However, the second entry produces a difference of 1 with a borrow from a higher-order stage. For the HS result, borrows are disregarded. The third and fourth entries produce a difference of 1 with a borrow from a higher-order stage. For the HS result, borrows are disregarded. The third and fourth entries produce an HS of 0. These HS and $\overline{HS}$ results are ANDed with the generated borrow request signals to produce the final answer.

As shown in table 4-5, the result of the first entry can satisfy a borrow. Therefore, if a borrow is requested of this stage, it can satisfy the borrow without generating a borrow. The second entry in the table is the combination which generates a borrow. When this condition exists, a signal informs the next higher order that a borrow is being requested. Entries three and four neither generate nor satisfy a borrow but rather propagate, to the next higher-order stage, any borrow which may be requested of it. The signal, in this case, is called a borrow enable.

The following six-bit example illustrates these conditions. The first, or lowest-order stage can satisfy a borrow. The second stage generates a borrow which is propagated through stage three to be satisfied by stage four. Stage five neither generates nor satisfies a borrow, and the sixth stage generates a borrow which is satisfied by the first stage.

PROBLEM:

```
    0 0 1 1 0 1
+   0 1 1 0 0 1
    1 0 0 1 1 0
```

SUBTRACTOR SOLUTION:

```
      G P S P G S
      0 0 1 1 0 1
    - 1 0 0 1 1 0
Line 1 → 1 0 1 0 1 1   HALF SUBTRACT
Line 2 → 0 0 1 1 0 1   BORROWS
Line 3 → 1 0 0 1 1 0   RESULT (SUM)
```

Complemented

G—Generates a borrow
P—Propagates a borrow
S—Satisfies a borrow

Where there is no borrow, the HS is the final result. Where a borrow is present, the $\overline{HS}$ is the final result. In other words, if a bit in line 2 is zero (no borrow), the corresponding bit in line 1 (HS) will be the final results in line 3. If a bit in line 2 is a one (borrow), the complement of the corresponding bit in line 1 ($\overline{HS}$) is the final result in line 3.

In computer logic, the HS can be obtained as an exclusive OR output of the corresponding

Table 4-5.–Subtractor input combinations and HS results

ACTUAL CONTENTS	SUBTRACTOR INPUT	HS	$\overline{HS}$	CONDITION
X D				
(1) 1 1	1 - 0	1	0	Satisfy borrow
(2) 0 0	0 - 1	1	0	Generate borrow
(3) 1 0	1 - 1	0	1	Propagate borrow
(4) 0 1	0 - 0	0	1	Propagate borrow

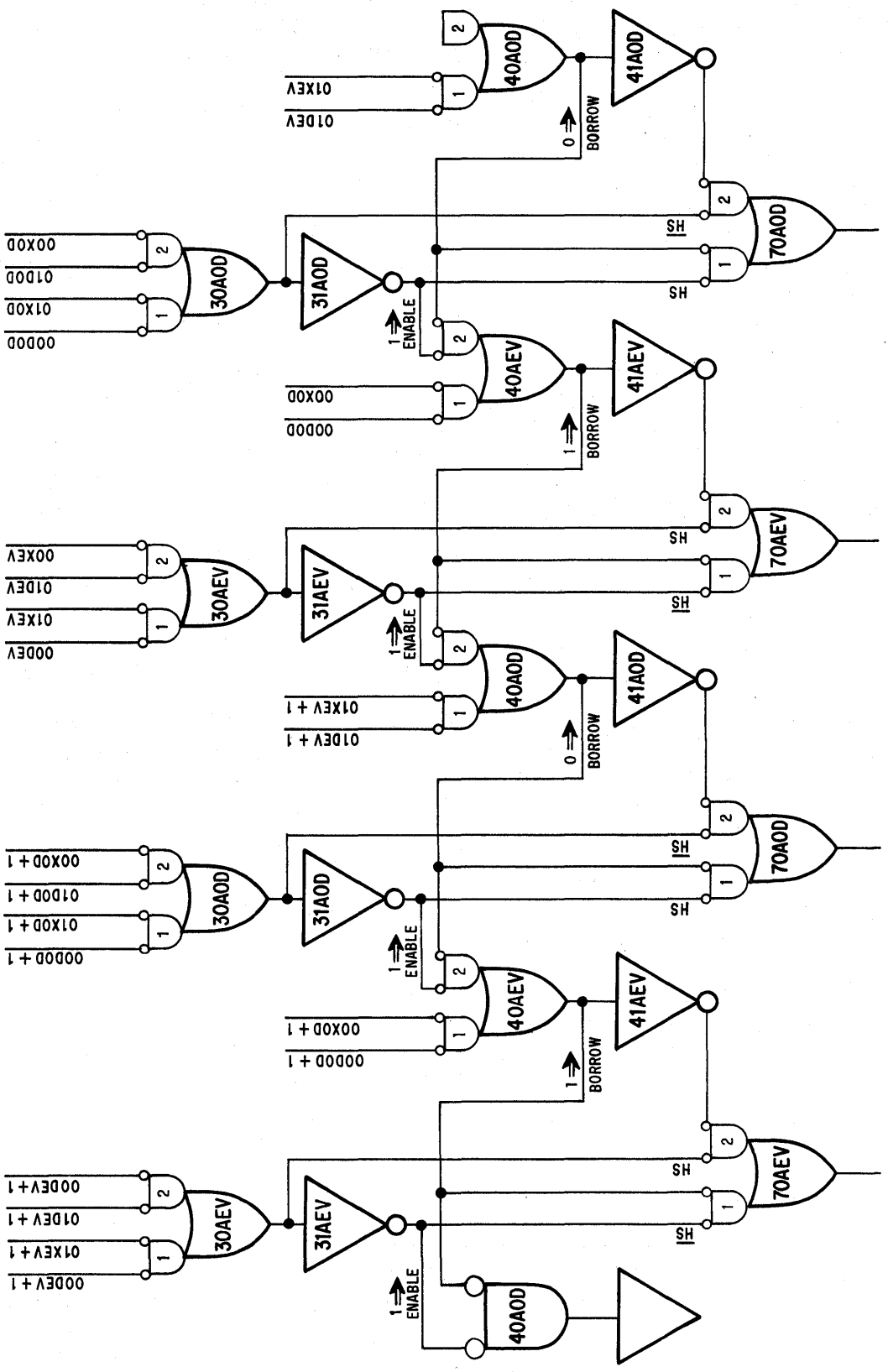

Figure 4-7.—Four typical subtractor stages.

minuend and subtrahend bits. The borrow will always be an exact reflection of the minuend, in fact it may be the minuend in the circuits.

Each stage of the subtractor contains an input circuit which, properly enabled, will generate a borrow; a circuit used as an inverter, which generates HS and enable signals; a circuit which checks the borrow status; and an output circuit. Figure 4-7 shows four typical subtractor stages. The signal level for borrows from odd-numbered stages is: H ⇒ BORROW while from even-numbered stages L ⇒ BORROW. All odd-numbered stages are similar as are all even-numbered stages.

The $\overline{HS}$ is formed by inverting the 30A– output through 31A–. The HS and $\overline{HS}$ are ANDed, together with borrow information from the next lower-order stage, to produce the final output from that stage through 70A–. This final output is actually the complement of the answer and is inverted through S1 and placed in the A register.

The borrow status of each stage is determined by the 40A– circuit. A borrow from any stage results either when this stage is generating a borrow or when a borrow is requested from this stage and is not satisfied but is propagated to the next higher-order stage. The only combination which will generate a borrow is X = D = 0. The only combination which will satisfy a borrow is X = D = 1. The remaining two combinations, X ≠ D, will enable borrows to be propagated. Examination of the inputs of 40AOD shows how a borrow signal is generated. If both inputs to the #1 AND are low, indicating that X00 = D00 = 0, a high out of 40A0D indicates, to 40AEV, that a borrow has been generated. If either the X00 or D00 inputs are high, the inputs to the #1 AND of 40A0D will not generate a borrow. However, depending upon the input from 40AEV to the #2 AND of 40A0D, the stage is capable of propagating a borrow to a 40AEV. If X00 = D00 = 1, the #2 AND of 70AEV is enabled by the output from 30AEV, and any borrow generated by 41AEV will be satisfied by this stage.

The subtractor is divided into five 6-bit SECTIONS to speed up the arithmetic process. Figure 4-8 illustrates the sections and bit positions. If a borrow request is generated within a section and not satisfied within that section, it is applied to the next section as an intersection (between sections) borrow request. This request is generated by the highest-order stage within the section generating the request or by a lower-order stage generating a borrow request which is propagated by the higher-order stage or stages within that section. The intersection borrow requests are applied to the lowest-order stage of each section.

If none of the stages within a section will either satisfy or generate a borrow, the section will produce a section borrow enable. Thus, if a borrow request is applied to that section, it will be propagated to the next section. For example, if a borrow request is generated by section I and sections II and III are enabled, the request will be applied to section IV. An important point to remember is that the subtractor is capable of using an end around borrow. That is, if section III generates a borrow and section IV and V cannot satisfy the borrow, the request will be propagated to section I.

MEMORY SECTION

The memory section is composed of three separate and distinct memory systems which function together to store all the required data within the computer. Each memory system has its own special function and type of storage. The main memory, which is the largest, is a core storage memory which is used for the storage of

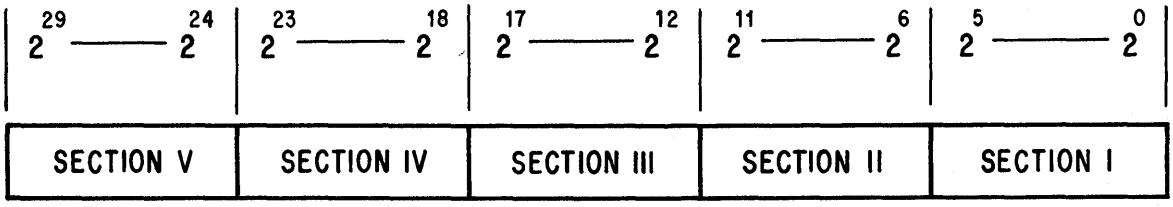

Figure 4-8.–Subtractor sections. 124.413

programs, constants, and input/output data. The control memory is a high-speed thin-film memory which serves as the storage medium for indexing and input/output control. The bootstrap memory is used for the storage of critical instructions and constants, and it also provides for automatic recovery in the event of program failure and for automatic initial loading of programs.

Altogether there are 32,768 possible 30-bit locations; 32,672 of these are in main memory, 64 in control memory, and 32 in bootstrap memory. The 32 bootstrap addresses actually contain 64 words. Two different programs of 32 words may be selected by means of the PROGRAM I/PROGRAM II pushbutton-indicators on the console when in the load mode. For all other conditions, one or the other may be selected by means of the switch on the program switch module on chassis A5.

Main Memory

The main memory section of the computer consists of five identical memory chassis (chassis A9 through A13) and the control memory chassis (chassis A8), which contains the S register and translator, the Z register, the data buffer register, and the memory control circuits.

Each main memory chassis contains a portion of the magnetic core storage system. This system has high speed, random-access, and nonvolatile characteristics. With this high-speed capability, speed of operation is compatible with the other computer sections; being random-access, data may be referenced in a nonsequential manner; and, being nonvolatile, the system retains its data when power is removed from the computer.

All main memory chassis are identical, and each stores a six-bit segment of the 30-bit word. Every storage location is assigned a separate address (000008-777778), with addresses 00100-00177 reserved for control memory and 00540-00577 for bootstrap memory. A 30-bit word in storage can be divided into two 15-bit words, the upper 15 bits (Mu) and the lower 15 bits (ML). By means of programming and the use of the k designator, each 15-bit word can be handled separately.

Figure 4-9 is a simplified block diagram of the main memory system. When a specific storage location in memory is referenced, the S register contains a 15-bit address word that

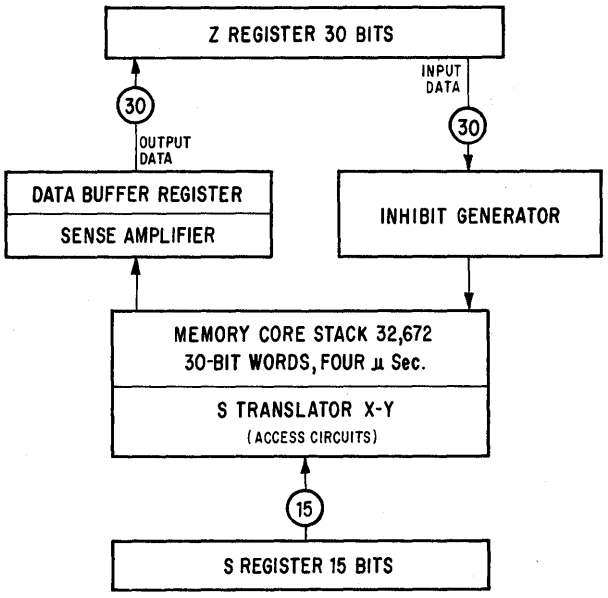

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Figure 4-9.—Main memory block diagram.

specifies one of the storage locations. The data transmission into or out of the selected storage location is through the Z register. The control and input/output sections of the computer have independent access to the storage registers through the use of the S register and translator, the Z register, and memory control.

The time required for one main memory reference (basic memory cycle time) is four μs. After a given function initiates memory, it is approximately one μs before the delivery of data from storage (readout time). All timing relationships in the memory section are established by memory control and the basic timing of the computer.

Magnetic Cores

Before exploring how the main memory system works, it is necessary to review the physical construction of a magnetic core memory. The operations of the components of a core memory will also be briefly discussed.

The magnetic cores are the basic elements of the main memory system used in the CP-642B. A magnetic core is a bistable device capable of

storing a 1 or a 0, depending upon the polarity of its residual magnetization. The cores are made of ferrite material and have an outside diameter of 0.050 inches, an inside diameter of 0.030 inches, and a thickness of 0.0125 inches. The characteristics of these cores are such that approximately 400 mA of current for a period of 1.2 microseconds is required to switch them from one stable magnetic state to the other. The coincident current switching technique is employed to switch the cores. Four lines pass through each core (fig. 4-10 and 4-11): An X read/write drive line, a Y read/write drive line, a vertical or horizontal inhibit line, and a diagonal sense line.

The state of magnetization of a core is induced by the current in the X and Y drive lines. If the core is in the 1 stage of magnetization and if the magnetizing force on the X and Y drive lines is great enough, it will drive the core to the 0 state, thus causing a change in flux within the core. Any change in flux of a core induces a voltage in all lines

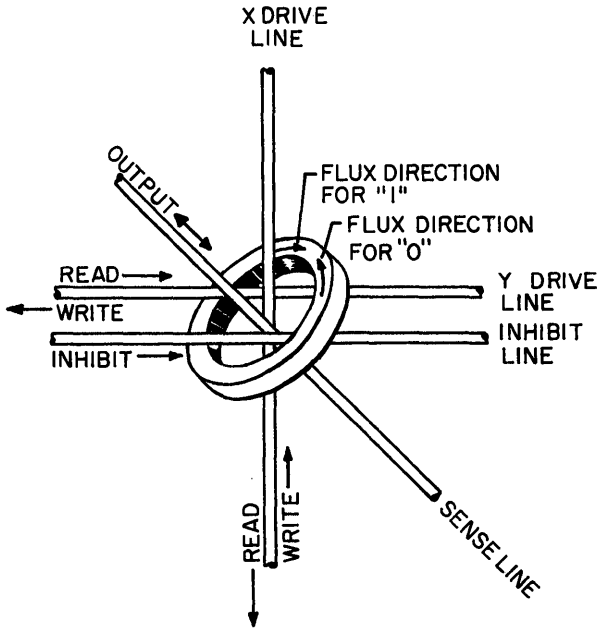

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Figure 4-11.—Typical magnetic core, inhibit line Y oriented.

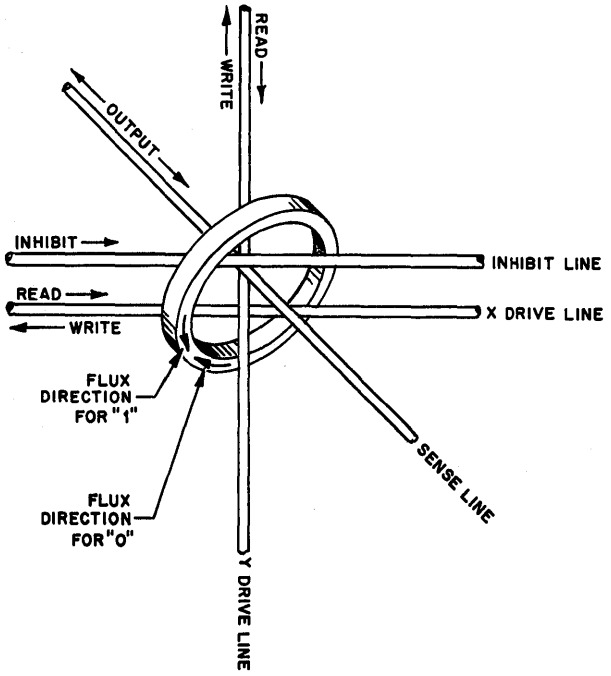

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Figure 4-10.—Typical magnetic core, inhibit line X oriented.

passing through the core. Therefore, the induced voltage on the sense line is sampled to see if there is an output (over 30 millivolts) indicating that the core was in the 1 state and has been switched. Because the state of the core is determined in this manner. the current pulse producing this magnetizing force is called a read pulse.

If, on the other hand, the core was originally in the 0 state, the magnetizing force will only disturb the state of the core, and no appreciable flux change will occur. Therefore, no output will be observed on the sense line.

In both the above cases the core will be in the 0 state after it has been read. This is known as destructive readout, and the initial condition must be restored. This is accomplished by applying a coincident current on the X and Y drive lines which is opposite in polarity to the read pulses. If a 1 was stored in the core previous to the read step, these coincident current pulses drive the core to its 1 state, thus restoring the information which was read. If a 0

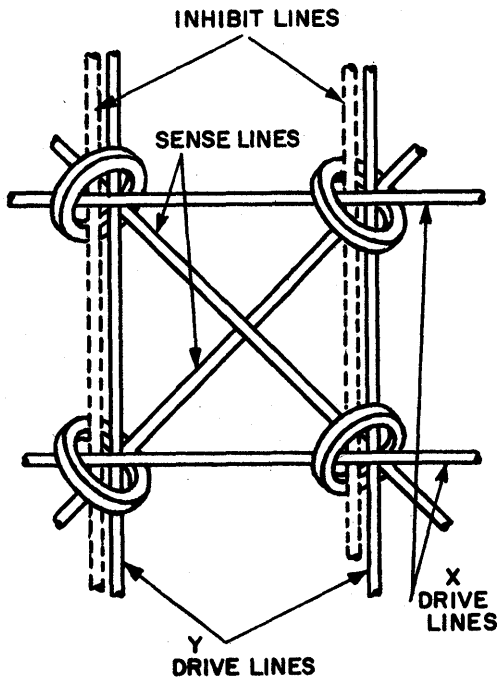

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Figure 4-12.—Basic construction of a magnetic core matrix.

was stored in the core previous to the read step, a current is applied to the inhibit line which is opposite in polarity and overlaps the time duration of the pulse on the Y drive line. This pulse reduces the effect of the X and Y pulses sufficiently to prevent the core from being driven to the 1 state, and the core remains in the 0 state. The pulses associated with the restore function are called write or restore pulses and are nearly equal in amplitude but opposite in polarity from the read pulses.

To write into the core, or change its state, the read pulses are again applied to the X and Y drive lines and the core is read. But, since the information read out of the core during this step is not retained, the effect is to clear all the cores to the 0 state in preparation for the write step.

The write step is similar to the restore step described above. During the write step, coincident current pulses on the X and Y drive lines drive the core to its 1 state of magnetization. However, if a 0 is to be written, a current pulse is applied to the inhibit line which is opposite in polarity to that of the pulse applied to the Y drive line. This pulse reduces the magnetizing force of the X and Y pulses and prevents writing a 1.

MEMORY PLANE.—The memory plane is the basic unit of the memory stack. It has 16,384 magnetic cores that are located at the intersection of the horizontal and vertical conductors. Figure 4-12 is a simplified view of an intersection and shows X and Y drive line orientation. Two memory planes with 4 quadrants each are required to store all the main memory addresses for one bit position. The X and Y drive lines terminate at tabs along the edges of the plane. Each memory plane has four inhibit lines and four sense lines that pass through all cores and are brought out to solder terminals at the four corners of the plane.

A memory plane is divided into four quadrants (fig. 4-13). Each quadrant contains a

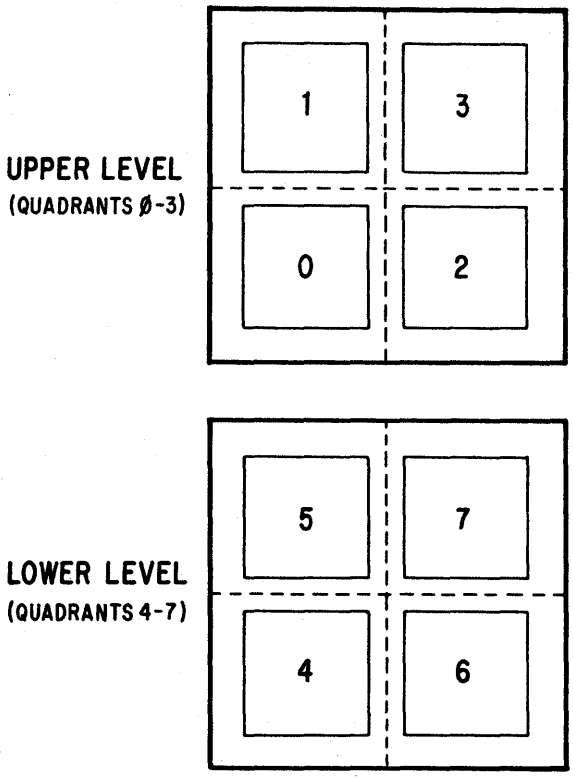

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Figure 4-13.—Memory plane, quadrant designations.

64 x 64 array of core (fig. 4-14) and has its own inhibit and sense lines. An inhibit line is threaded vertically (parallel to the X drive lines) or horizontally (parallel to the Y drive lines) through all of the cores in a quadrant. The inhibit line is threaded vertically in quadrants, 1, 2, 5 and 6 (fig. 4-10) and horizontally in quadrants 0, 3, 4 and 7 (fig. 4-11). This method of threading the inhibit lines equalizes the loading effect on the drive lines by the inhibit lines. A sense line is also threaded through all of the cores in a quadrant. The sense line is oriented to allow maximum noise cancellation when a core is switched.

MEMORY STACK.—The storage elements of the main memory are contained in the five memory stacks. There is one stack on each of the five memory chassis. Each stack contains all of the 32,672 addresses required for the storage of a six-bit segment of a 30-bit word. A stack contains 12 memory planes, two endboard assemblies, and a center board (fig. 4-15). The memory stack is divided into two parts that are referred to as the upper level (the module side of a chassis) and the lower level (the wiring side of a chassis). Each level contains six memory planes separated by the center board, and an endboard assembly. The memory planes are

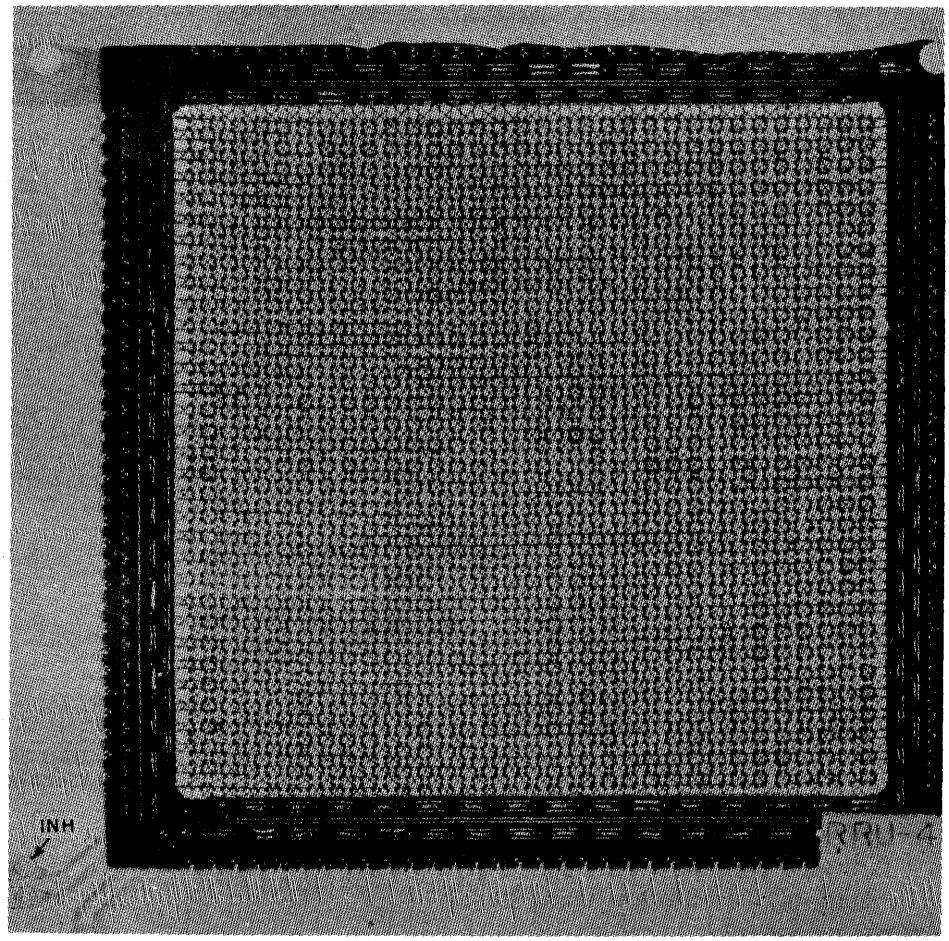

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Figure 4-14.—Memory quadrant (64 x 64 array).

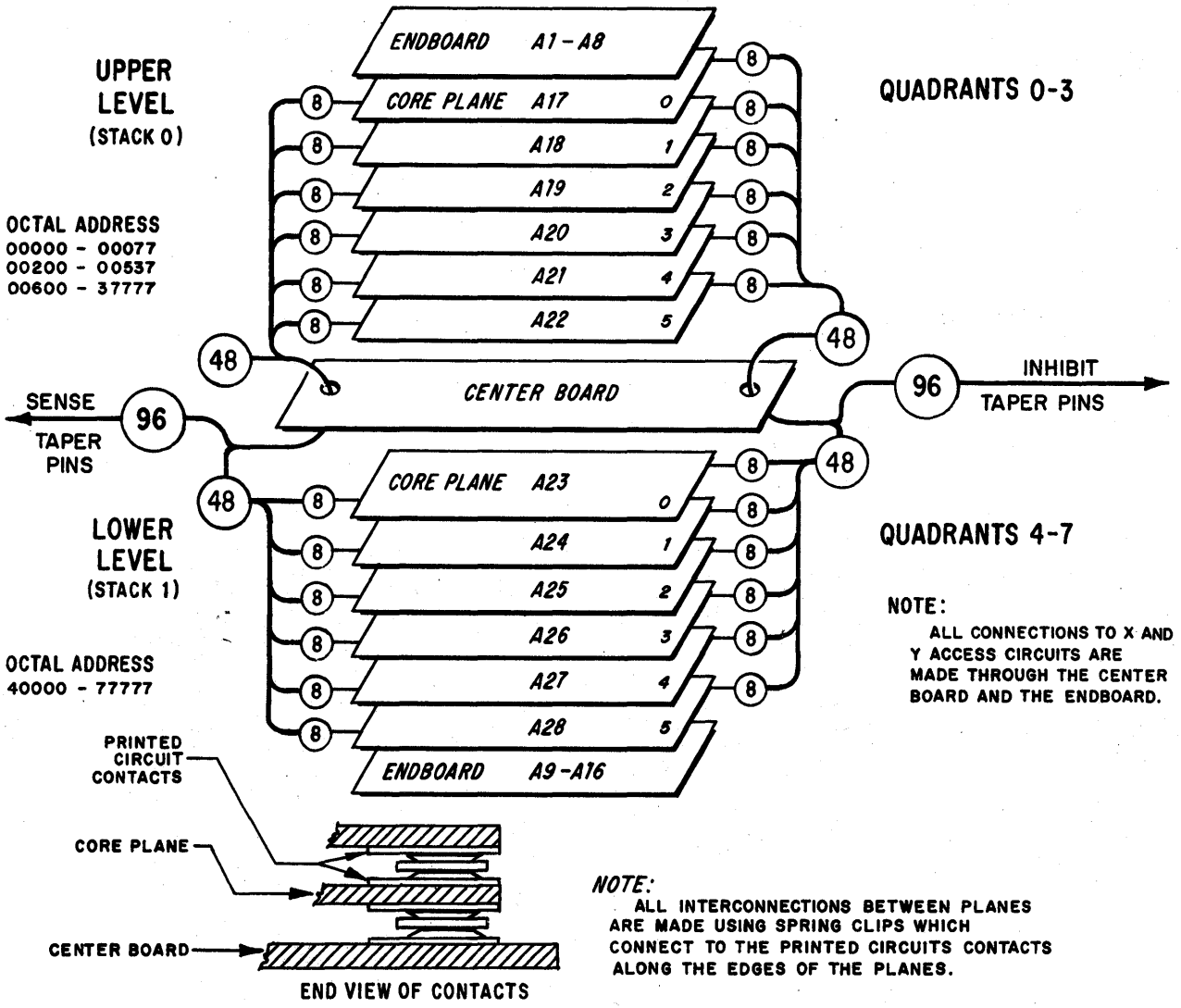

Figure 4-15.—Memory stack.

interconnected by spring clips that are also used to connect adjacent memory planes to the center board and to the endboard assemblies.

CENTER BOARD.—The center board is a printed circuit board that connects the X and Y drive lines on the memory planes to the X and Y selector transformer secondaries.

END BOARD.—The endboard assembly consists of eight printed wiring cards and mounted diode modules. Each module contains 16 diodes used to terminate the drive lines.

Core Selection

The main memory of the computer is a current-operated, magnetic core storage system. The operation described previously for the selection of one core is applied with refinements to the selection of a word (30 bits) from any

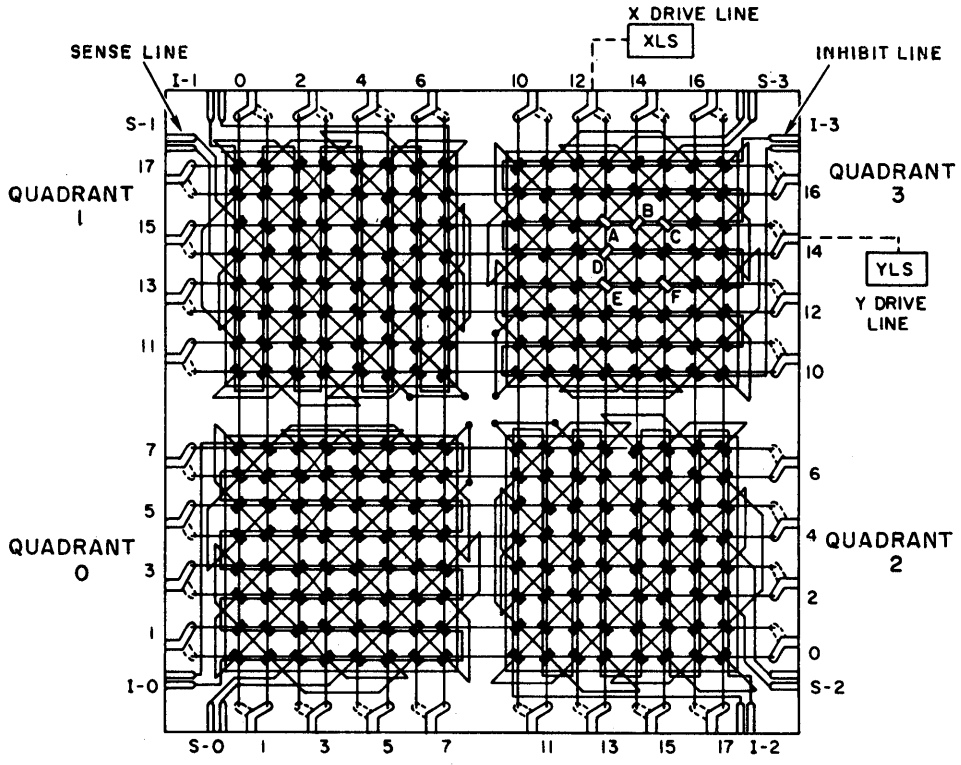

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Figure 4-16.—Simplified diagram of a 16 x 16 magnetic core array.

address in memory. Figure 4-16 illustrates a simplified magnetic core plane containing a 16 x 16 array of cores. The memory planes used in the computer contain four 128 x 128 arrays.

Selectable conductors (X and Y drive lines) thread through each core in each row and column. Any one of the magnetic cores in the matrix may be selected (addressed) by pulsing a given row and column. In the sequence of events which follows, a coincident half-amplitude current pulse is generated in each selected row and column. The core at the intersection of the row and column (selected core) receives a total of two half-amplitude current pulses. For example, assume core A on figure 4-16 has been selected or addressed. It receives a net full-amplitude pulse when coincident half-amplitude current pulses are impressed on its intersecting X and Y drive lines. All other cores in the same row or in the same column as core A receive half-amplitude current pulses (cores B, C, D, and E). These cores are half-selected. The remaining cores, neither half-selected nor fully selected, are referred to as unselected cores (core F).

The binary information (0 or 1) stored in a core is determined by the polarity of its magnetization. The information is extracted from a selected core when two coincident half-amplitude read current pulses switch the magnetization of the core. In read pulse polarity, if the core holds a 1, the magnetization in the core is reversed, and a voltage (55 millivolts peak) is induced in the sense line. When the selected core is in the 0 state, an insignificant voltage (10 millivolts maximum) is induced in the sense line when the read pulses are applied. The small induced voltage indicates no flux reversal and is sensed as a 0.

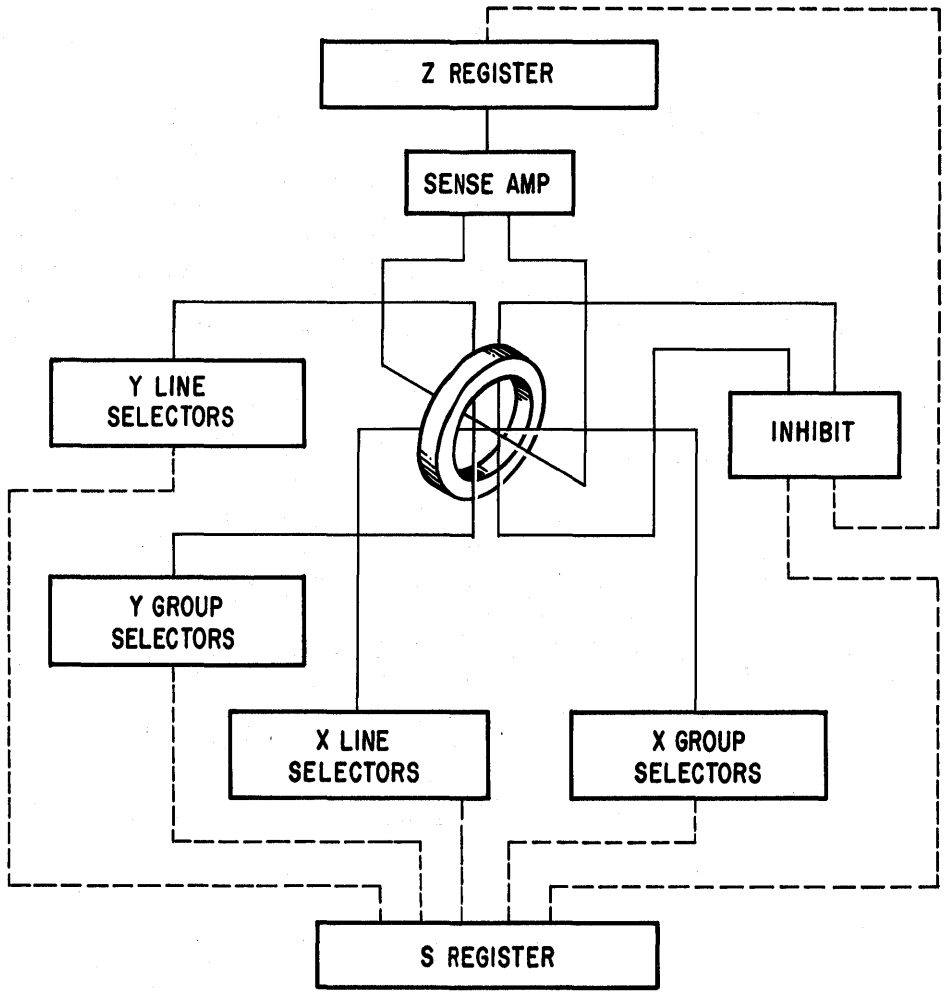

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Figure 4-17.—Memory address translation.

Address Translation

Figure 4-17 is a simplified block diagram of the memory address translation circuits. The X and Y group selectors, the X and Y line selectors and the inhibit selector make up the S translator. The S translator breaks down the contents of the S register into enables for a specific address. The translator is enabled when either the read or write flip-flop in memory control is set.

The group selectors enable the primary and secondary of a selected drive current transformer. The output of the drive current transformer is to a group of eight drive lines. The line selectors determine which specific drive line is selected. By using combinations of these group and line selectors, any address in memory may be selected for either read or write.

The sense amplifiers connect the outputs from the memory planes to the Z register. Each sense circuit connects the output of the sense windings in a bit-plane (two memory planes) to a stage in the sense register. The sense register, in turn, connects to the Z register.

The inhibit circuits are used during the write cycle to prevent writing into a wrong address in memory by counteracting X and Y drive line pulses for core selection.

Control Memory

The control memory is a 64 word, 30-bit, thin-film memory with an access time of 333 ns and a total cycle time of 667 ns. Both the 30-bit data words and the 7-bit addresses are transferred to and from control memory in parallel.

The control memory is located on chassis 8, which also contains memory control and the S and Z register. Film memory is composed of the logic circuitry and the film stack.

THIN-FILM STACK.—The thin-film stack has a Unifluxor (Bootstrap Memory) plane mounted above the thin-film planes (fig. 4-18). The four thin-film planes are mounted above the transformer diode boards in locations A3 through A6, and the transformer diode boards are mounted on the bottom (wiring) side of the chassis. The interconnections between boards and the connections between the thin-film planes and the logic circuitry are accomplished by using plugs which connect directly to the etched surfaces on the edge of the memory planes.

THIN-FILM PLANE.—Each thin-film plane consists of two covers, two wiring arrays, a spacer, and four substrates (fig. 4-19). The substrates are held in place by the spacer, which also serves to separate the wiring arrays. A wiring array is placed above and below the spacer containing the substrates, and the covers are attached, thus securing the complete thin-film plane.

The transformer diode boards are identical for both bootstrap memory and control memory. The bootstrap transformer diode board is on the bottom at location A1, and the one for control memory is above it at location A2.

THIN-FILM STORAGE.—The storage media for the control memory consists of a ferromagnetic material (permalloy) deposited as film spots on a substrate of thin glass. This is

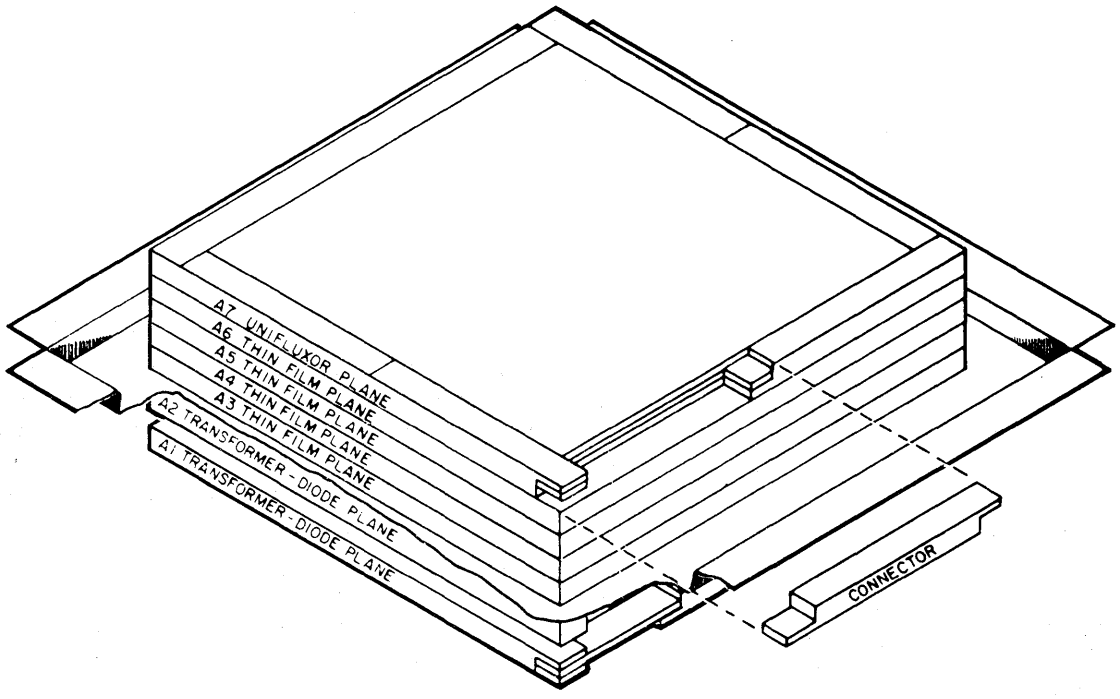

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Figure 4-18.—Thin film stack.

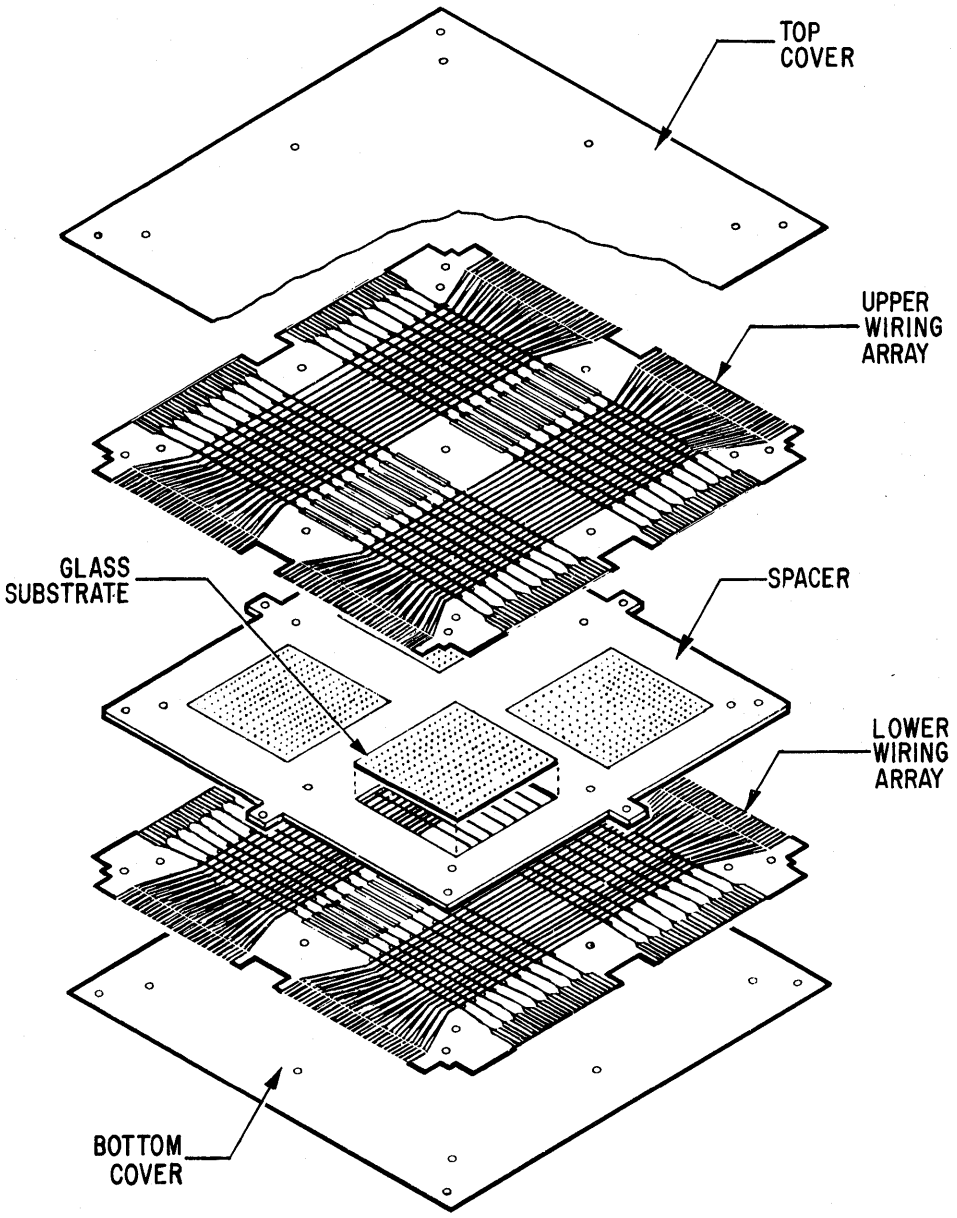

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Figure 4-19.—Thin film plane.

commonly called thin-film memory. These permalloy film spots are 50 mils in diameter and 1,000 angstroms (0.000004 inches) thick. The geometry of these film spots permits the magnetic state of the spot to be switched in nanoseconds by a small amount of power. Since the film spots have two preferred states of magnetization, they readily store binary information.

The film spots, which provide the storage media, are deposited on the glass substrate in a vacuum chamber. After the air is removed from the chamber, a shutter arrangement is opened, and vapors resulting from molten permalloy pass

through a mask and are deposited on the substrate. The pattern of the spots on the substrate is determined by the shape of the mask, and the thickness of the spots is determined by the shutter's opening time.

A magnetic field is applied parallel to the surface of the substrate while permalloy spots are being deposited. Each film spot then becomes easier to magnetize along an axis parallel to that in which the magnetic field was applied (preferred axis).

The film spot is well suited for storing binary data since it has a stable stage of magnetization in each direction parallel to the preferred axis (fig. 4-20). If the direction of magnetization (M) is rotated through 180 degrees starting from the preferred axis, the following phenomenon occurs. There is first a torque pulling the magnetic vector back toward the preferred axis; then, as it passes a point perpendicular to the preferred axis, there is a forward torque on the magnetic vector. This torque is produced by the residual magnetic field (A) which was produced during the deposition of the spots.

If no magnetic fields are applied to the film spot, the residual magnetism (A) causes the magnetic vector to be parallel to the preferred axis (fig. 4-20A). If only a longitudinal field (B) is applied, a magnetic field parallel to the preferred axis in either direction has negligible effect on the magnetic state of the spot (fig. 4-20B). If only a transverse field (C) is applied, a magnetic field perpendicular to the preferred axis causes the magnetic vector to rotate 90 degrees, as shown in figure 4-20C. If fields are applied such that the magnitude of A plus B equals C, the position of the magnetic vector will be as illustrated in figure 4-20D. If C is removed from the spot, the direction of magnetization becomes the same as the direction of B. If B is then removed, the spot remains in this position until C is again applied. Thus, the direction of B determines the direction of the final stable state of magnetization of the film spot.

A magnetic field is produced concentrically around a flow of current; it is, therefore, possible to switch a film spot by passing current through drive lines placed close to the spot. The drive and sense lines are etched on Mylar sheets which are carefully aligned and attached to phenolic boards to give required strength to the line array.

Figure 4-21A shows a film spot and the line array on one side of it. An identical set of these lines is placed on top of the film spot. Connectors for the line array are wired in a manner such that the sense and bit lines each form one turn around the spot and the word lines form two turns.

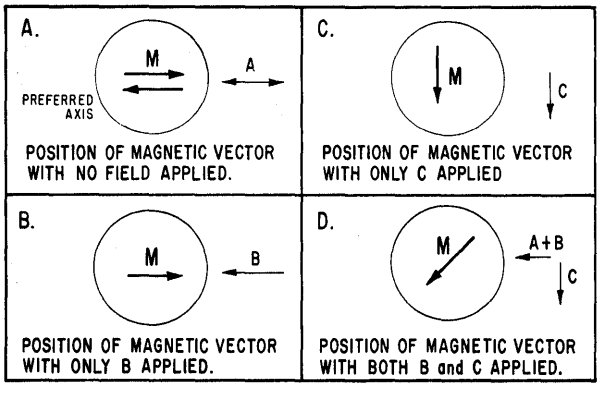

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Figure 4-20.—Film spot, vector rotation diagram.

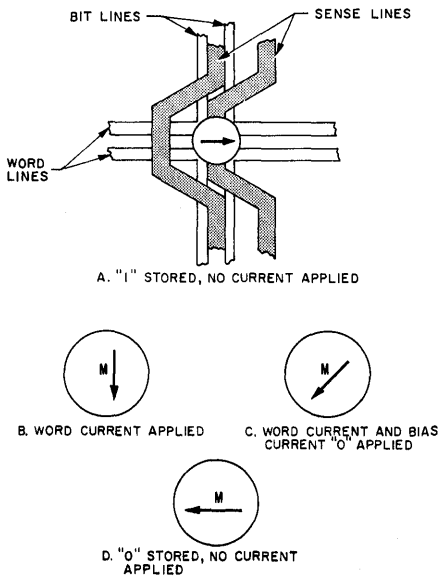

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Figure 4-21.—Film spot switching.

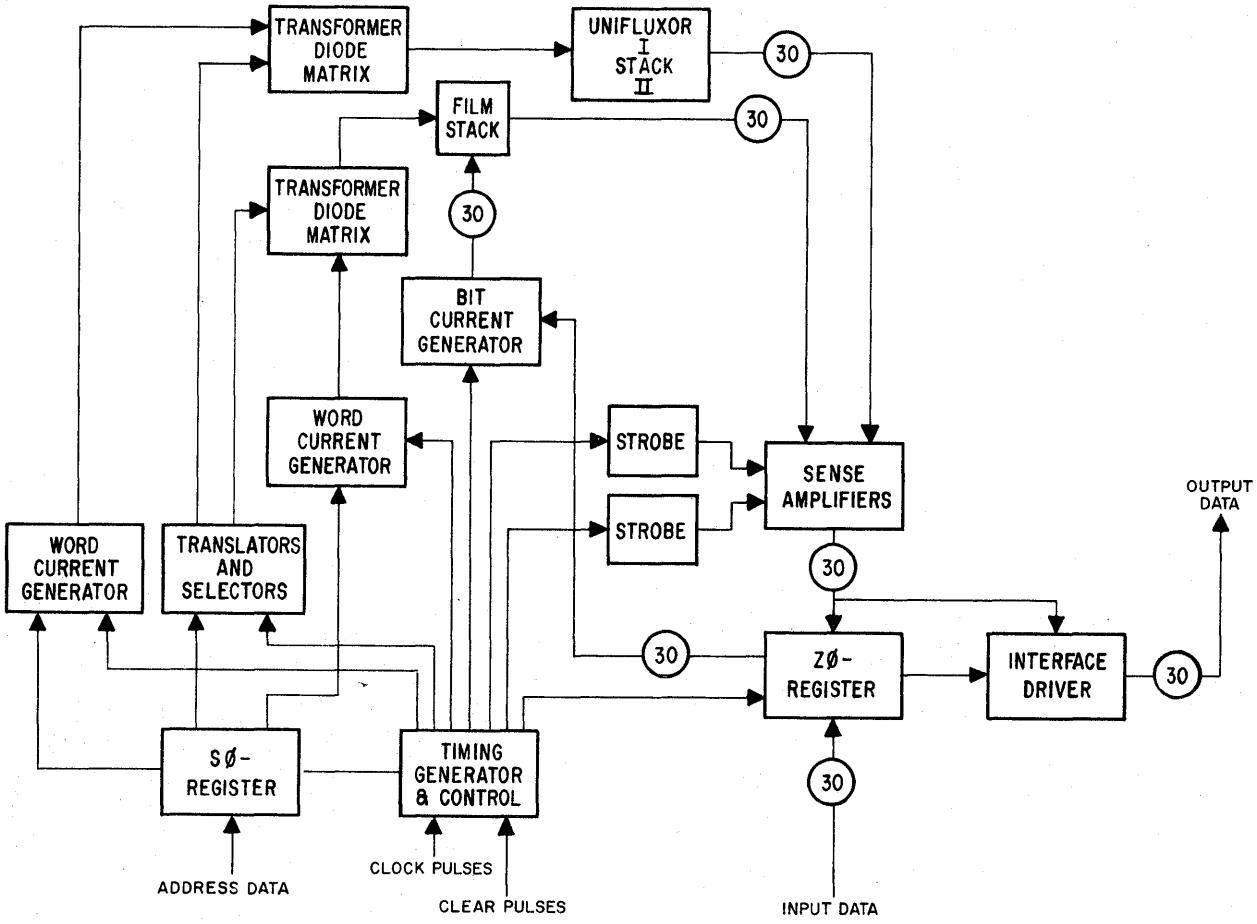

Figure 4-22.—Control and bootstrap memories.

The arrow on the film spot in figure 4-21A shows the stable state magnetic vector with a 1 stored. If word current flows down the word lines, the magnetic vector rotates 90 degrees as shown in figure 4-21B. The magnetic vector is made to rotate towards the 0 stable state by a magnetic field produced when current flows through the bit lines (fig. 4-21C). After the word current is removed, the vector completes the 180 degree rotation from the 1 state. Thus, a 0 is stored as shown in figure 4-21D.

If a 1 is to be stored in the spot, current applied to the word lines is in the same direction, but the current applied to the bit lines is reversed. Thus, the magnetic field around the bit lines reverses, and the magnetic vector is rotated toward the 1 state. If the word current and then the bit current are removed, the stable state of magnetization will represent a 1.

Control memory is a destructive readout memory in that the reading of any control memory location changes the contents of that address. During a readout, only the word lines are enabled, producing a magnetic field perpendicular to the preferred axis. This field rotates the magnetic vector to a position perpendicular to the preferred axis. The sharp change in the magnetic field around the spots when the word lines are activated causes a voltage to be induced in the sense lines. The magnitude of this voltage depends upon the rate of change in magnetic flux resulting from the

switching process. For a given film spot, the output for a 1 is negative and for a 0 is positive or vice versa. The arrangement of the sense lines is such that, for a given bit, the polarity of a 1 at the sense line output changes as the address changes; for example, bit 15 at address 3 is a positive for a 1, while bit 15 at address 4 is negative for a 1. By ANDing a strobe pulse with the output from the appropriate side of the sense amplifier, a 1 is read from the memory. No output from the AND circuit indicates a 0 has been read.

CONTROL MEMORY WORD SELECTION.–Whereas the core memory is bit-oriented, the control memory is word-oriented (fig. 4-22). Word "oriented" means that a complete 30-bit word is selected and driven by one word line. The word drive line which has been activated by a word line transformer switches all 30 bits to determine their output. The word drive current is applied in the same direction during both read and write. During a write cycle, the bit current is also applied, but this is automatically supplied to all bits at one time. If, for instance, bit 0 of ZØ contains a 1, a bit current indicative of a 1 is passed through all the film spots in position 0. The bit current has a negligible effect on the spots that have not been selected by a word current because it produces a magnetic field in the same direction as B in figure 4-20.

The word drive lines are threaded across four substrates located on two adjacent control memory planes. The substrates have a total of 36 film spots for each word, 30 of which are used. The word drive current passes across the top wiring array and back across the bottom; this essentially doubles the magnetic field produced between the two wiring arrays (fig. 4-23). The bit lines are arranged at right angles to the word lines.

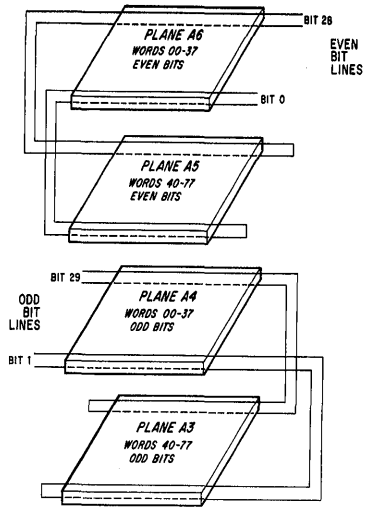

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Figure 4-23.–Film memory word drive line routing.

Control Memory Operations

The control memory operations are read, write and restore. Write and restore are basically the same function; the only difference is whether or not the information written back into the memory is the same as was read out or whether it is new information.

Each time control memory is initiated, a complete read/write cycle is performed. The address, supplied by the control section, determines which word line is activated. During the read portion of the cycle, the data register (ZØ) is cleared. The ZØ register is loaded by either the film stack outputs or the control section, or both. During the write portion of the cycle, the contents of the ZØ register are stored in the specified film stack locations.

To read the memory (fig. 4-22), an address must be supplied to the SØ register, an initiate signal must be issued from memory control, and a read enable must be provided. The address in SØ is translated to enable the proper word line transformer, and the output of the film spots is sent to the sense amplifiers.

When the sense amplifiers are strobed, the outputs are gated in the ZØ register. Strobed refers to a timing pulse called the strobe pulse which is used to ensure the optimum signal level before the data is transferred. The output pulse from a film spot is not of sufficient duration or amplitude to set a standard flip-flop; therefore, a holding flip-flop is used. This flip-flop stores the data received from the sense amplifiers until after it has been sent to the ZØ register; then it is cleared.

If the sense amplifiers are not strobed, the film stack outputs will not be gated into the ZØ

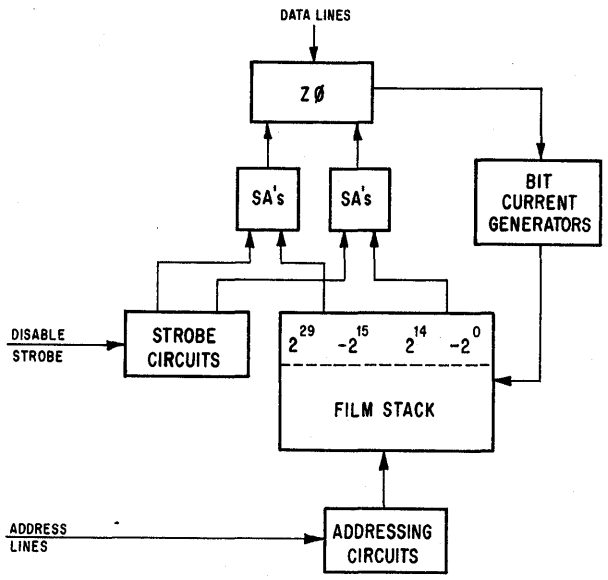


Figure 4-24.—Control memory block diagram.

register, and the data will not be restored to the film stack. Figure 4-24 shows that this strobe disable may be applied to the upper half, the lower half, or the entire word. During a read operation, both sets of sense amplifiers are enabled, and the entire word is gated into the ZØ register. During a write operation, data from the control section is loaded into the disabled portion(s) of ZØ, and the entire word is written back into the film stack. By applying the disable to half the word, it is possible to modify half the word without affecting the other half. This function of control memory is very important to the control and input/output sections indexing operations. Reset circuits clear the holding flip-flops so that they may be available to store the information received during the next read cycle.

The data contained in the ZØ register is unconditionally gated to the bit generators by timing pulses. The word current is still being applied to the selected word, so that, when the bit current is produced, the information held in the ZØ register will be written back into the film spots. Following the write/restore cycle, the word current and bit current are removed.

Address Translation

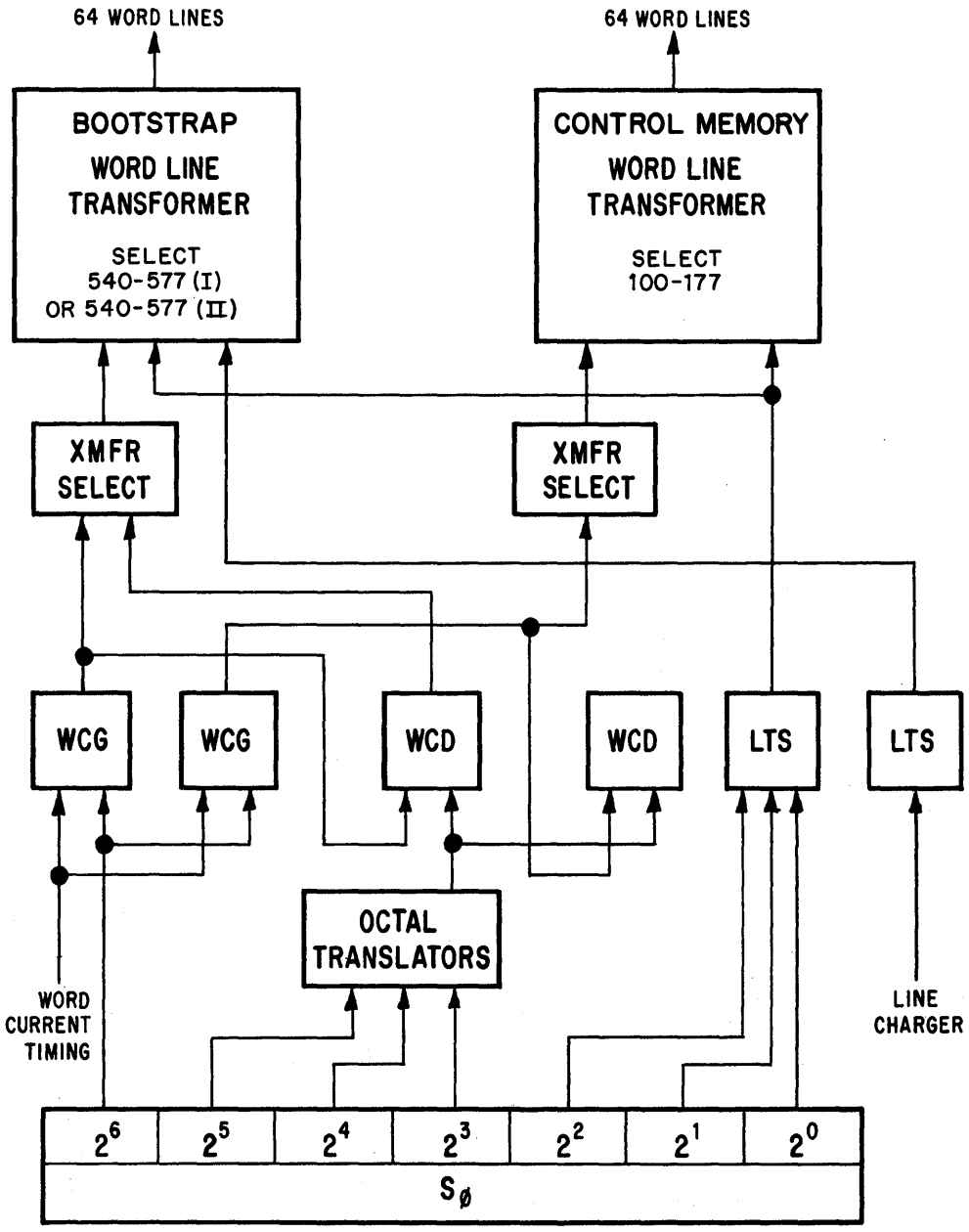
The control memory address register (SØ) is a seven-bit register which is loaded by the control section SØ selector at the same time control memory is initiated. This address may originate in either the control section or the input/output section, but it must pass through the SØ selector gates which are logically located in the control section. Control memory addressing circuits are shown in the block diagram on figure 4-25.

WORD CURRENT GENERATOR (WCG).—There are two word current generators which are used for the bootstrap and control memories. The most significant SØ address bit (2^6) determines which WCG is selected. Address group 100-177 selects control memory; bootstrap addresses 540-577 select Program I or Program II. The WCG outputs enable the word current diverters and supply the primary current for the transformer selectors.

WORD CURRENT DIVERTER (WCD).—The 16 word current diverters select the primaries of the transformer selectors for bootstrap and control memory. Bits 03, 04, and 05 of the SØ register and the outputs from the WCG select the WCD. All the transformer selector primaries are supplied current from the WCG, but only the primary which is enabled by the selected WCD will pass current and produce an output.

LINE TRANSFORMER SELECTORS (LTS).—The eight line transformer selectors enable one of the eight word line transformers from the group designated by the transformer selectors. The stages of SØ concerned with line selection are 00, 01, and 02. At the completion of the write portion of the memory cycle, the line charger drives the LTS output to -15 volts (the stable state) in preparation for the next memory cycle.

WORD LINE TRANSFORMERS.—The 128 word line transformers are located on the transformer diode boards. There are 64 word line transformers for control memory and 64 for bootstrap (two 32-word programs). The word line transformers generate the word current



124.421

Figure 4-25.—Thin film memory addressing block diagram.

which is used to read or write in the control memory, and to read only in the bootstrap memory.

Timing and Control

Control memory timing is taken from a tapped delay line with a total duration of about 500 ns. Once the memory cycle is initiated, it proceeds to completion independent of computer timing. The control section supplies the address, sets the inhibit flip-flops which determine to what portion of the data the strobe disables apply, initiates control memory, loads ZØ (write operation), and samples the contents of ZØ (read operation).

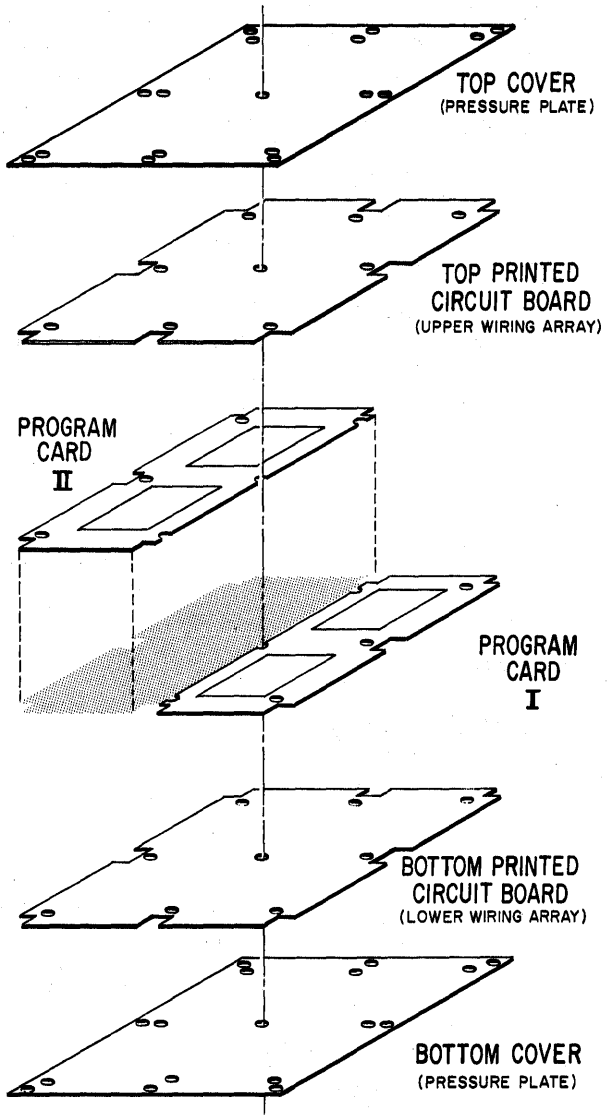


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Figure 4-26.—Exploded view of a Unifluxor plane.

Enabling and disabling of the word and bit lines is controlled by the word timing and bit timing flip-flops. The specified word line is enabled before the read portion of the cycle and remains enabled until the completion of the write portion. The bit lines are enabled only during the write/restore portion of the memory cycle.

BOOTSTRAP MEMORY

Bootstrap memory is a 667-nanosecond cycle time Unifluxor memory which has a permanent or nondestructive readout (NDRO) type of storage. It is used primarily for program fault recovery and provides initial loading of programs. There are two programs in bootstrap memory which are supplied at the time of manufacture.

Bootstrap memory employs linear storage elements which consist of a wiring array and two program cards, as shown in figure 4-26. The word lines and sense lines are etched on two plastic cards known as upper and lower wiring arrays. These lines are accessed and sensed by the circuitry associated with the control memory. Each program card has 32 words of 30

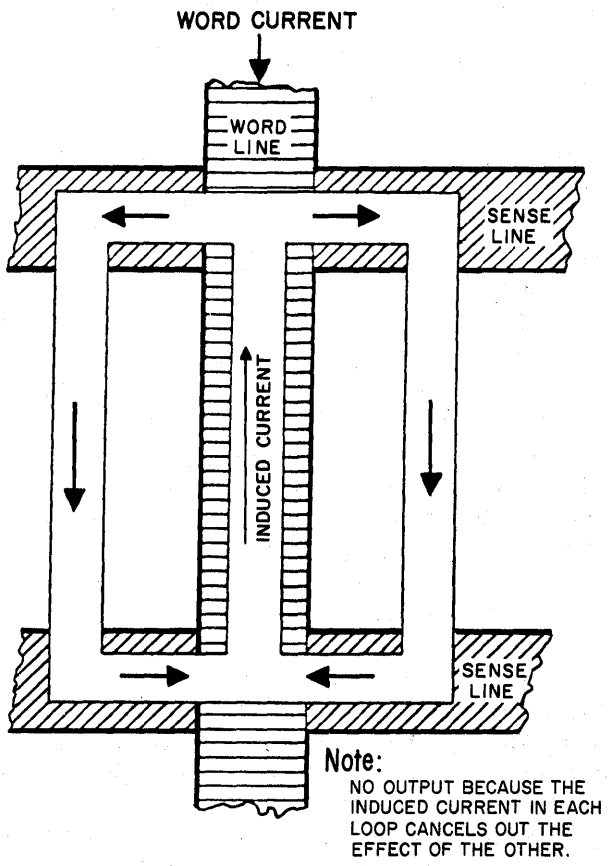

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Figure 4-27.—Belt buckle drive and sense lines.

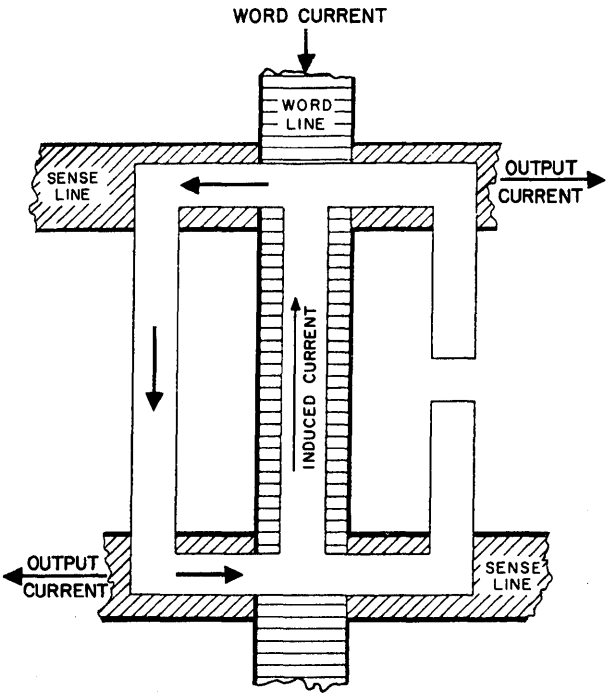

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Figure 4-28.—A belt buckle that contains a "0"

bits each. The stored information is in the form of copper "belt buckles" etched on the program card. The program cards are positioned between the wiring array cards and a cover is placed over them. This complete assembly is called a Unifluxor plane. The Unifluxor plane is mounted above the thin-film planes on chassis A8. The transformer diode board associated with the bootstrap memory is located at A1, and the Unifluxor plane itself is located at A7.

Theory of Operation

The principle used for the storage of data in the bootstrap memory is that a current through a conductor will induce a nearly equal but opposite current in another conductor placed very close and parallel to it.

The program cards are placed on top of the wiring array and positioned so that the common loop of the belt buckle is directly over the word drive line as shown for one bit in figure 4-27. When a current is applied to the drive line, an opposite current is induced in the belt buckle. This current will flow around both sides of the belt buckle, and the net effect on the sense lines will be negligible. If one loop is cut, however, no current can flow around that side, and the result will be as shown in figure 4-28. This case represents a 0. If the opposite side is cut, the result will be as shown in figure 4-29. This case results in a 1, because the output on the sense lines is not inverted. Each word on a program card is made up of 30 such belt buckles which are opened on one side or the other to represent binary information. It is impossible to internally alter or change the information contained on these cards, but it is possible to replace the program card with another one.

Program Selection

In the load mode of operation, the PROGRAM I/PROGRAM II pushbutton indicators are pressed to select either of the two

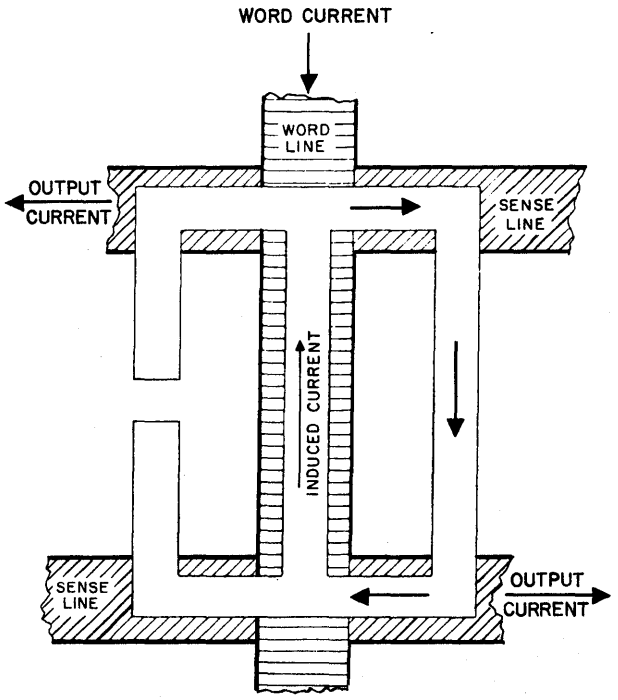

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Figure 4-29.—A belt buckle that contains a "1".

programs. For other bootstrap references, the toggle switch at chassis location A5 is used to select either program for automatic recovery.

MEMORY REPAIRS

Some memory stacks have been damaged beyond economical repair by field maintenance personnel. In view of this damage field maintenance personnel have been requested not to attempt repairs of these stacks.

The EIMB Communications Handbook (NAVSEA 0967-000-0010), in the Service Notes under CP-642B/USQ-20(V) Computer memory failures, or EIB No. 811 detail instruction on how to arrange replacement of a failed memory stack. Also, EIB 873 gives details for turning in a failing memory chassis and obtaining a replacement.

INPUT/OUTPUT SECTION

The transfer of data to and from the computer is via 16 input and 16 output channels with the data being transferred in a 30-bit parallel mode. These are octally numbered as 0 - 17_8. The 16 channels are constructed on four chassis, each of which contains four identical I/0 channels. Channels 0 - 3 are on chassis 4, channels 4 - 7 are on chassis 3, channels 10_8 - 13_8 are on chassis 2, and channels 14_8 - 17_8 are on chassis 1. Any or all of the four chassis can be designated a high-speed (up to 250 kHz transfer rate per channel) chassis or a slow-speed (up to 40 kHz transfer rate per channel) chassis by the changing of the fast interface/slow interface circuit cards. Changing a chassis to either fast or slow interface effects all four channels on that chassis. The I/0 section functions asynchronously with the computer program. It operates in one of two modes, input or output. In either mode, the peripheral equipment can either request data or command transfers. (Commands in the input mode are referred to as interrupts, and in the output mode as external function words.) In addition, the I/0 section is capable of processing various internally generated interrupts. It becomes apparent that with the 16 channels, various types of requests and various types of interrupts, some priority system must be established since the I/0 section can process one request or interrupt on one channel only at any given time. The I/0 section utilizes three basic priority systems. Function priority is used to establish which request or interrupt is to be processed first, in the event that more than one request or interrupt is present simultaneously. Group priority is used to establish which chassis containing a request for priority will be acknowledged first. Channel priority is used to establish which channel on a particular chassis will be granted priority. After a request has been granted priority, the I/0 section sends a signal to the external equipment indicating that the request has been processed.

Data Format

The three types of information transferred between the I/0 section and the peripheral units are data words, control words, and external interrupt words.

(1) DATA WORDS.–These words represent ALPHANUMERIC data. Input data words are data entered into the computer from the peripheral units. Output data words are data sent to the peripheral units from the computer. Data transfer is in a 30-bit parallel mode.

(2) CONTROL WORDS.–Control words consist of bit-position coded, 30-bit words accompanied by an external function signal. Control words are sent from the computer to peripheral units and specify the type of operation a peripheral unit is to perform.

(3) EXTERNAL INTERRUPT WORDS.–External interrupt words consist of bit-position coded, 30-bit words accompanied by an external interrupt signal. Interrupt signals are sent from the peripheral units to the computer. Their purpose is to divert the computer's attention to a special condition which exists on a corresponding I/0 channel. The accompanying interrupt word from the peripheral equipment will then inform the computer of the normal/abnormal conditions that caused the status interrupt.

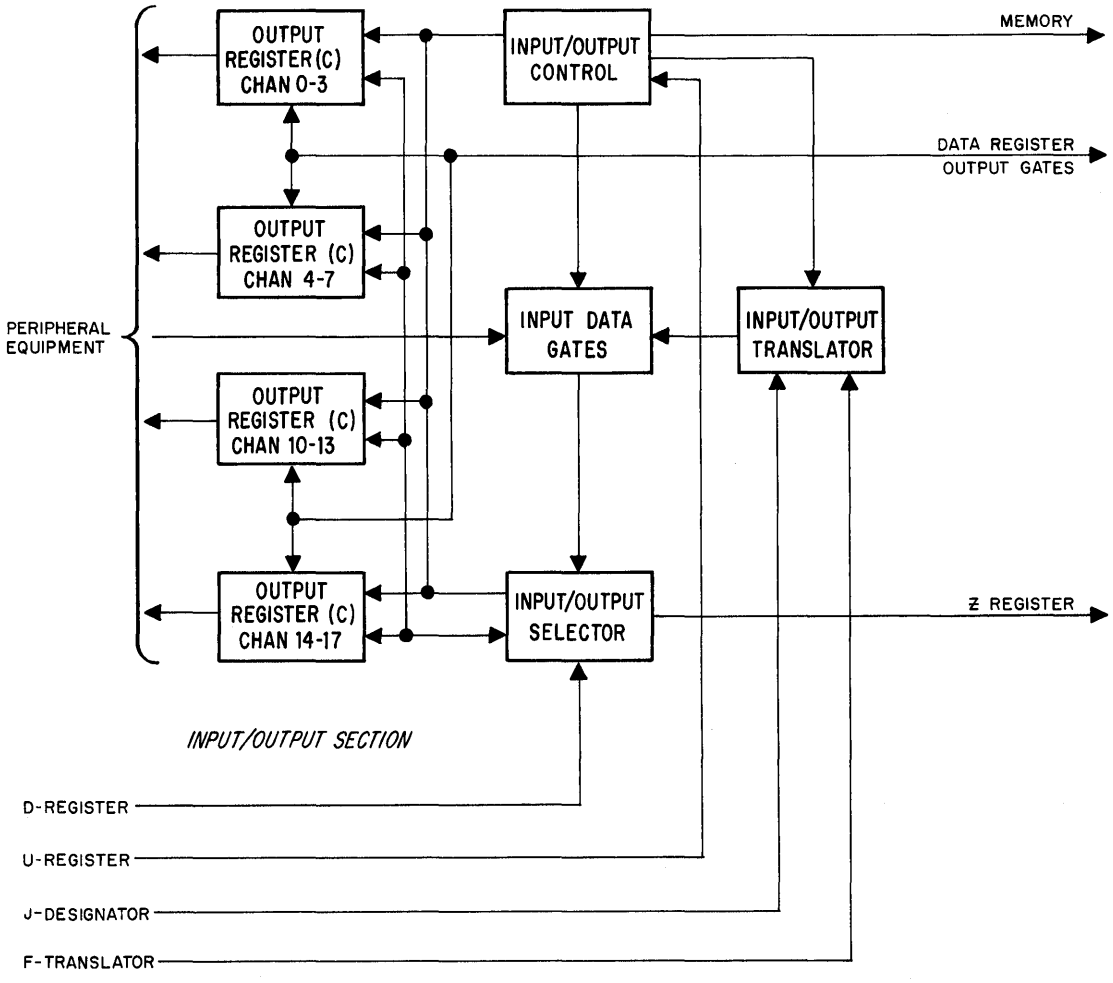

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Figure 4-30.–I/O section simplified block diagram.

SIMPLIFIED BLOCK DIAGRAM

A simplified block diagram of the I/0 section is shown in figure 4-30. The diagram represents the logic required to depict the operation of an input/output channel. In some cases, one block represents sixteen identical circuits, one for each I/0 channel. In other cases, one block either represents four identical blocks, one for each chassis, or circuits which are common to all channels.

I/0 CONTROL.–The input/output control circuits provide the gating, timing, and monitor control for input/output data transfers. These circuits also initiate control signals and select control lines for data transfers.

The computer program selects the appropriate input or output mode of operation through the use of the appropriate programmed instruction.

Input instructions are f = 73 and f = 75 or the related instructions f = 17, 62, and 66. Output instructions are f = 74 and f = 76 or related instructions f = 13, 63, and 67.

INPUT DATA GATES.–The input data gates provide a storage medium for input data to the computer until such time as the computer

logic is capable of processing this data as directed by the I/0 control circuitry.

The circuits contained in this section are the input amplifiers, input data gates, ID (input data) one-shots and request gates. These circuits provide the logic to transfer data from a peripheral device to the computer.

The input amplifiers provide line isolation and signal amplification. The input gates allow the selection of the appropriate data for processing by the logic circuitry. The one-shot flip-flops ensure that input requests or interrupts are processed only once.

I/0 SELECTOR.–The I/0 selector provides the necessary gating, through program generated enables, for signals and data from the I/0 section to memory. Input signals to the selector include data from peripheral equipment or the D register and are routed to either the upper or lower 15 bits of the Z register.

I/0 TRANSLATOR.–The I/0 translator provides translation to establish the priority of the input signal and the priority of the channel requesting the I/0 function. Through this translation, the translator develops the enables used by the I/0 section to process the specified function on the specified channel.

The channel priority network is actually broken down into two parts. The channel selector selects one of four channels, 0 through 3, within a group or chassis. The group selector selects one of the four I/0 groups or chassis, A1 through A4. Each chassis contains a channel selector, but the group selector is common to all chassis. The purpose of channel priority is to determine the priority level of the channels in the event that more than one channel attempts to process the same request or interrupt simultaneously. The chassis are numbered A1 through A4. Chassis A4 contains channels 0 through 3, chassis A3 contains channels 4 through 7, chassis A2 contains channels 10 through 13, and chassis A1 contains channels 14 through 17. The channel selector always grants priority to the highest-numbered channel within a group. The group selector always grants priority to the highest-numbered group. Thus, channel 17 has the highest priority, and channel 0 has the lowest priority.

A single function priority scheme is used to service all 16 channels. The function priority is composed of two distinct groups, requests and interrupts. The purpose of the function priority is to determine which request or interrupts are present simultaneously. The priority and access circuits evaluate the requests function priority according to an established sequence, as follows:

(1) Advance real-time clock
(2) External function
(3) Output request
(4) Input request
(5) External interrupt
(6) External function monitor interrupts
(7) Output monitor interrupt
(8) Input monitor interrupt.

If two or more channels simultaneously request the same type of function, the priority and access circuits assign channel priority in descending order of channel numbers.

In addition, force instructions and real-time clock requests have priority over all other requests or interrupts.

Each channel contains an ID (Input Data) Active, OD (Output Data) Active, and EF (External Function) Active flip-flop to indicate that the computer program has determined his channel ready to perform the stated function. The active flip-flops are set through either program or manual control and are cleared by either program control or master clear.

The request gates are used as an AND function to allow a request to pass only if all required conditions are met.

Each channel contains External Function Monitor (EF MON), Output Data Monitor (OD MON), Input Data Monitor (ID MON) and External Interrupt Monitor (EI MON) flip-flops to generate, via I/0 priority, an internal interrupt when the specified buffer operation has been completed. These flip-flops, set through program control, are cleared by program control, translator control after the interrupt has been granted priority, or by master clear.

OUTPUT REGISTERS.–One output, or C, register is provided for each group or chassis to store output data until the associated peripheral device is capable of processing it.

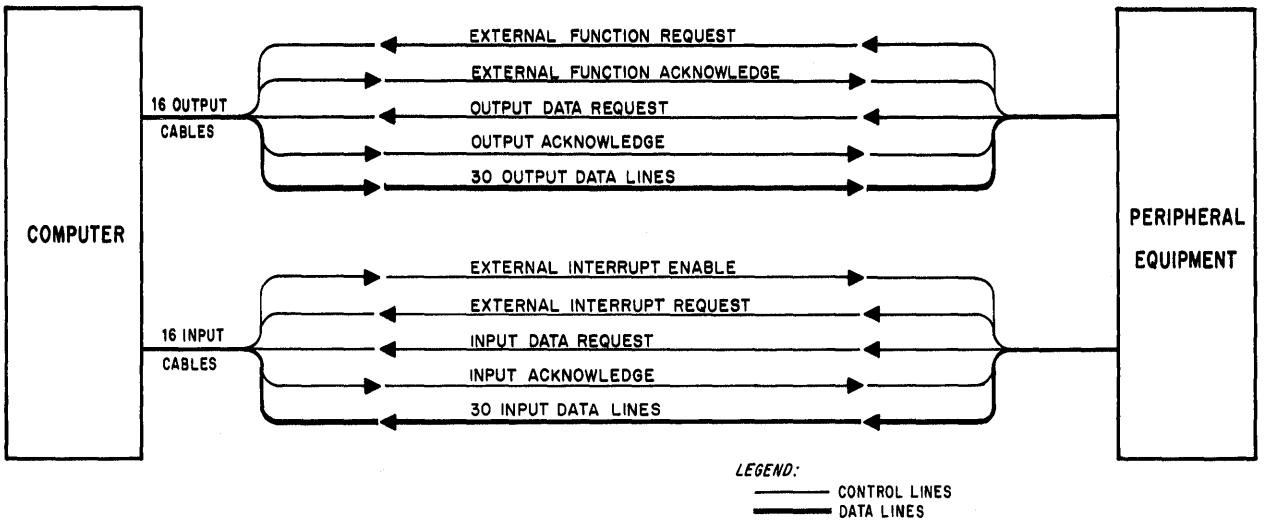

Figure 4-31.—Computer to peripheral equipment cabling.

COMPUTER TO PERIPHERAL DATA AND CONTROL SIGNALS

Each input and output channel is connected to its peripheral equipment by cables, as shown in figure 4-31. Each cable has data lines and control lines. The data lines are used to carry the data to or from the computer, and the control lines serve as a means of identifying the type of data on the data lines and as a synchronizing control between the two units of equipment. The output cable control lines are labeled:

(1) External Function Request
(2) External Function Acknowledge
(3) Output Data Request
(4) Output Acknowledge.

The input cable control lines are labeled:

(1) External Interrupt Enable
(2) External Interrupt Request
(3) Input Data Request
(4) Input Acknowledge.

Notice the direction of information flow in figure 4-31. The data request signals are always sent from the external equipment to the computer. The acknowledge signals are always sent from the computer to the external equipment. Table 4-6 describes the computer to peripheral equipment control lines.

Sequence of Events

All references to input and output are made from the standpoint of the computer; input is input to the computer and output is output from the computer.

Output Data

(1) Computer initiates output buffer for given channel.
(2) Peripheral equipment sets the output data request line, indicating that it is in a condition to accept data.
(3) Computer detects the output data request.
(4) Computer (at its convenience) places information on the data lines.
(5) Computer sets the output data acknowledge line, indicating that the data is ready for sampling.
(6) Peripheral equipment detects the output data acknowledge.
(7) Peripheral equipment samples the data lines.

Table 4-6.—Computer to peripheral control signals

FUNCTIONAL NAME	WORD TRANSFER CABLE	WORD TRANSFER DIRECTION	DEFINITION	EFFECT
External Function Request	O	PE ⟶ C	Peripheral equipment ready to accept an external function.	Computer sends an external function to peripheral equipment.
External Function Acknowledge	O	PE ⟵ C	An external function word is on the data lines ready to be sampled.	Peripheral equipment control unit decodes function word.
Output Data Request	O	PE ⟶ C	Peripheral equipment ready to receive next output word.	Computer forms next output word and sends output acknowledge.
Output Acknowledge	O	PE ⟵ C	A data word is on the data lines ready to be sampled.	Initiates cycle whereby peripheral equipment accepts and processes output word.
External Interrupt Enable	I	PE ⟵ C	Computer can accept an external interrupt.	Peripheral equipment interrupts the computer if necessary.
External Interrupt	I	PE ⟶ C	Control information is on the data lines	Causes computer program to jump to a subroutine for that channel.
Input Data Request	I I	PE ⟶ C	A data word is on the data lines ready to be sampled.	Computer accepts input word and sends input acknowledge.
Input Acknowledge	I	PE ⟵ C	Computer has accepted the word on the data lines.	Initiates cycle whereby peripheral equipment produces next input word.

NOTE: C ⟶ Computer; PE ⟶ Peripheral Equipment; O ⟶ Output; I ⟶ Input

(8) Peripheral equipment may drop the output data request any time after detecting the output data acknowledge.
(9) Computer drops the output data acknowledge after a specified time.

Items 2 through 9 of this sequence are repeated for every data word until the number of words specified as the difference between the initial address and final address (i.e. upper 15 bits = final address, lower 15 bits = initial address) of the output buffer word has been transferred.

Throughout the discussion of computer I/0 control signal and data flow, reference will be made to the computer performing some action "at its convenience." Convenience, in this context, should be interpreted as meaning no higher priority work to be performed.

Input Data

(1) Computer initiates an input buffer for a given channel.
(2) Peripheral equipment places a data word on the data lines.
(3) Peripheral equipment sets the input data request line to indicate that it has data ready for transmission.
(4) Computer detects the input data request.
(5) Computer samples the data lines at its convenience.
(6) Computer sets the input acknowledge line indicating that it has sampled the data.
(7) Peripheral equipment senses the input acknowledge line.
(8) Peripheral equipment may drop the input data request line any time after detecting the input acknowledge.
(9) Computer drops the input acknowledge line after a specified time.

Items 2 through 9 of this sequence are repeated for every data word until the number of words specified in the input buffer has been transferred.

External Function (Normal)

(1) Computer initiates an external function buffer for a given channel.
(2) Peripheral equipment sets the external function request line when it is ready to accept the external function code.
(3) Computer detects the external function request.
(4) Computer, at its convenience, places the external function code on the data lines.
(5) Computer sets the external function acknowledge line to indicate that the external function code is ready for sampling.
(6) Peripheral equipment detects the external function acknowledge and samples the external function code.
(7) Peripheral equipment may drop the external function request any time after detecting the external function acknowledge.
(8) Computer drops the external function line after a specified time.

External Function (Forced)

Same as External Function (normal) except that the computer does not require an external function ready signal from the peripheral equipment, so the computer will not be delayed by steps 2 and 3.

External Interrupt

(1) Computer sets the external interrupt enable when it is ready to accept an external interrupt for a given channel.
(2) Peripheral equipment detects the external interrupt enable.
(3) Peripheral equipment places the external interrupt word on the data lines.
(4) Peripheral equipment sets the external interrupt request line to indicate that an external interrupt code is on the data lines.
(5) Computer detects the external interrupt request signal and, at its convenience, stores the external interrupt word.
(6) Computer drops the external interrupt enable.
(7) Peripheral equipment detects the drop of the external interrupt enable and clears the external interrupt request line and the data lines. The input acknowledge to

an external interrupt request will be initiated at the same time that the external interrupt enable is cleared. The simultaneous occurrence of these conditions should be used by peripheral equipment to differentiate between an interrupt acknowledge and a data acknowledge.

Computer to Computer Data and Control Signals

Any channel for which the intercomputer circuit card has been inserted can communicate with another computer (identification of these cards will be discussed later in the chapter). A similarity exists between intercomputer channels and normal channels. The two cables are identical, but the control line titles are different from the titles of a computer to peripheral channel. Interpretation of the data lines is similar and all voltage levels are the same. Figure 4-32 illustrates the interface between two computers. Control line title and functions are shown in table 4-7. Note that the control signals in the input cable are the same for intercomputer communication as for communication with peripheral equipment. In the output cable, ready and resume signals are used to control the intercomputer transfer of data.

Sequence of Events

Computer A is transmitting to computer B as shown in figure 4-32.

Intercomputer Command Word Transfer

(1) Computer B sets the external interrupt enable when it is ready to accept a command word from computer A.
(2) Computer A recognizes the external interrupt enable as an external function request and places the external function code on the data lines.
(3) Computer A sets the external function acknowledge to indicate that the external function code is on the data lines.
(4) Computer B, at its convenience, recognizes the external function acknowledge as an external interrupt request and accepts the command word.
(5) Computer B clears the external interrupt enable line, stores the command word in the status word location, and sets the input acknowledge line.

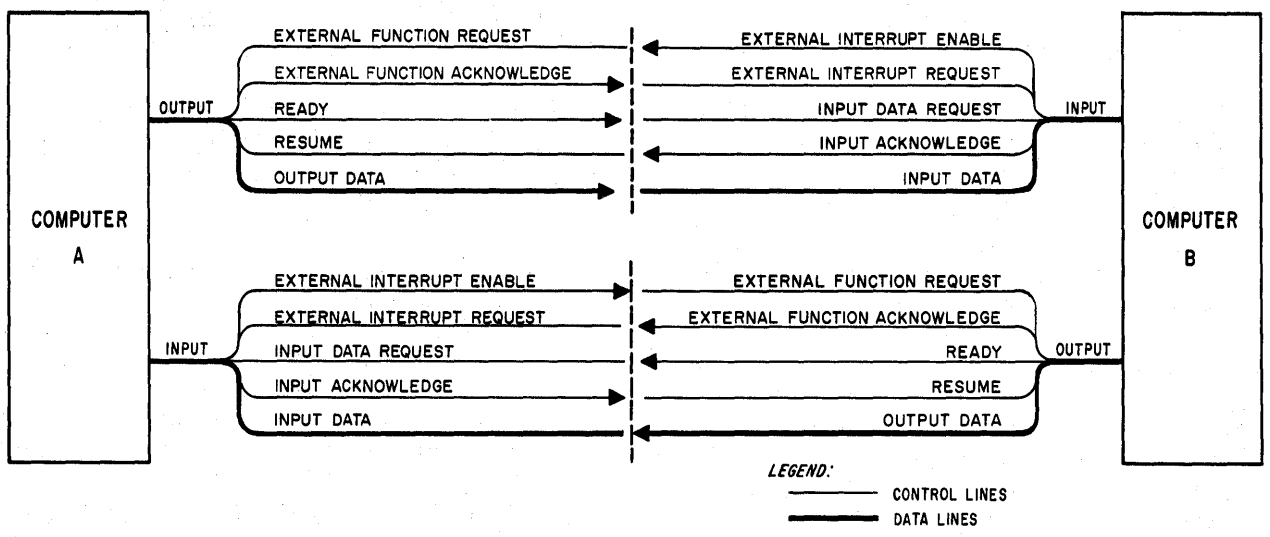

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Figure 4-32.—Intercomputer cabling.

Table 4-7.–Intercomputer control signals

FUNCTIONAL NAME	WORD TRANSFER CABLE	WORD TRANSFER DIRECTION	DEFINITION	EFFECT
External Function Request	O	Rx → Tx	Receiving computer is ready to accept an external function word.	Transmitting computer sends an external function to receiving computer.
External Function Acknowledge	O	Tx → Rx	An external function word is on the data lines ready to be sampled.	Appears as an external interrupt request to receiving computer.
Ready	O	Tx → Rx	A data word is on the data lines ready to be sampled.	Appears as an input data request to receiving computer.
Resume	O	Rx → Tx	Computer has received last word.	Transmitting computer produces next output word.
External Interrupt Enable	I	Rx → Tx	Receiving computer is ready to accept an external function word.	Appears as an external function request to transmitting computer.
External Interrupt Request	I	Tx → Rx	An external function word is on the data lines ready to be sampled.	Causes computer program to jump to subroutine for that channel.
Input Data Request	I	Tx → Rx	A data word is on the data lines ready to be sampled.	Receiving computer accepts input word and sends input acknowledge.
Input Acknowledge	I	Rx → Tx	Computer has accepted the word on the data lines.	Appears as a resume to transmitting computer.

Note:
Tx → Transmitting computer
Rx → Receiving computer
O → Output
I → Input

(6) Computer A recognizes the input acknowledge as a resume and clears the external function acknowledge line.

Intercomputer Data Transfer

(1) Computer B initiates an input buffer, and computer A initiates an output buffer for the required channel.
(2) Computer A places data on the data lines.
(3) Computer A sets the ready line to indicate that the data is on the lines.
(4) Computer B recognizes the ready signal as an input data request signal and, at its convenience, accepts the data word.
(5) Computer B sets the input acknowledge line.
(6) Computer A recognizes the input acknowledge as a resume signal and clears the ready and data lines.

The cycle is repeated for each word to be transferred.

Input/Output Operations

Once the I/O operations have been initiated by program control, the I/O section operates independently without program reference. To initiate an I/O function, or buffer, the program sets the active flip-flop for the desired function and the specified channel. The program also stores a control word in a fixed memory location which will be used to determine the memory address or addresses to be used during the buffer operation. At this point, the I/O section assumes full control of the buffer process, and program control is released to perform other computer functions. Once the channel has thus been activated, it can accept the specified function request from the peripheral device. Each time the request is received, one 30-bit word is processed, and the control word is updated and checked for termination. If the current address word and the final address word are identical, the active flip-flop is cleared and the buffer process is complete.

INPUT DATA REQUEST (IDR).–When an input buffer is required, program control sets the ID ACT flip-flop for the specified channel and stores the I/O control word at the specified address for the desired channel. When the peripheral device has placed a data word on the input data lines, it sets the input data request line. At the input data request date, the request is ANDed with the active flip-flop, the one-shot, and the input available. The input available indicates that the input acknowledge register is not being used. The output of the input data request gate goes to the channel priority register, and the inversion of the output goes to the function priority register. Channel priority selects the proper channel within the group. Function priority, besides selecting the proper function, also selects the proper group. After the group has been selected, an output of group priority is used to initiate the I/O sequence. The outputs of channel and group priority are translated to supply enables which allow the I/O sequence to process this request by the following sequence.

(1) Read the control word.
(2) Clear the one-shot flip-flop. This ensures that the IDR line must be cleared and reset before another IDR can be processed on this channel.
(3) Clear the active flip-flop if this is the last word to be read in.
(4) Write the word on the data lines into memory.
(5) Update the control word.
(6) Write the control word back into its assigned address.
(7) Send an input acknowledge signal to the peripheral device.

This sequence is repeated for each IDR until the active flip-flop is cleared.

OUTPUT DATA REQUEST (ODR).–When an output buffer is required, program control sets the OD ACT flip-flop for the specified channel and stores the I/O control word in the specified address for the desired channel. When the peripheral device is ready to accept data from the computer, it sets the output data request line. At the output data request gate, the request is ANDed with the active flip-flop, the one-shot, and the output available (indicating

that the output acknowledge register is not being used). The output of the output data request gate goes to special priority and from there to channel and function priority. Channel priority selects the proper channel within a group. Function priority is used to select the proper group. When the group has been selected, an output is used to start the I/0 sequence. The translations of the outputs are used to allow the I/0 sequence to process the request by the following sequence of events.

(1) Read the control word.
(2) Clear the one-shot flip-flop. This ensures that the ODR line must be cleared and reset before another ODR can be processed on this channel.
(3) Clear the active flip-flop if this is the last word to be transferred.
(4) Read the word from the address specified and place it on the data lines.
(5) Update the control word.
(6) Write the control word back into its assigned address.
(7) Send an output acknowledge signal to the peripheral device.

This sequence is repeated for each ODR from a peripheral device until the active flip-flop is cleared.

EXTERNAL INTERRUPT REQUEST (EIR).—The EIR flip-flop is cleared by master clear or program control. The external interrupt hold (EI Hold) flip-flop is set by master clear or program control. When the EIR flip-flop is clear and the EI Hold flip-flop is set, the computer sends an external interrupt enable signal to the peripheral equipment indicating that the computer is capable of accepting an external interrupt on this channel. When the peripheral equipment desires to interrupt the computer program, it sets the EIR line. The EIR from the peripheral device is ANDed with EI Hold flip-flop set, EIR flip-flop clear, channel active, input available, and the one-shot at the EI request gate. The output of the EI request gate is transmitted to the channel priority register to determine priority of the channel. The inversion of the EI request gate goes to the function priority register to determine priority of the function. After priority has been determined, the I/0 sequence is started. Translations of the outputs of channel and function priority supply the enables which allow the I/0 sequence to process a request by the following sequence.

(1) Clear the one-shot flip-flop. This ensures that the EIR line must be cleared and reset before another EIR can be processed for this channel.
(2) Store the status word contained on the input data lines in the address reserved for external interrupt code storage for this channel.
(3) Set the EIR flip-flop. This removes one of the enables to the external interrupt gate and drops the external interrupt enable line to the peripheral equipment which indicates to the peripheral equipment that the computer can no longer accept any interrupts on this channel.
(4) The set side of the EIR flip-flop is ANDed with the clear side of the EI hold flip-flop and the channel active signal clear to request priority to interrupt the computer program. From this point on, this interrupt functions as any other I/0 interrupt.

I/0 Interrupts

An interrupt is a control signal which diverts the attention of the computer to an extraordinary event or set of circumstances. Many levels of control can be exercised by the numerous forms provided. The interrupts from external sources serve primarily to synchronize the computer program with the readiness of peripheral devices, including other computers, to transmit or receive data and to notify the computer when an error has occurred. Internal interrupts serve primarily to synchronize the computer program with termination of input/output transfers and to signal the occurrence of an error.

An interrupt causes the next instruction to be procured from a fixed address corresponding to the interrupt source. This fixed address serves as a subroutine entrance by containing a return

jump instruction. The return jump instruction transfers the contents P + 1, which is the address of the instruction that would have been executed, to the first address of the subroutine, thereby providing the subroutine exit. Program control is transferred to the second address. Basically, there are two types of interrupts, external and internal. The internal interrupts (monitor interrupts) are generated when the monitor and inhibit flip-flops are set. Whenever it is desired to have an interrupt upon termination of a buffer function, the monitor flip-flop is set by program control. The inhibit flip-flop will always be set unless it is desired that no interrupts be accepted for a given channel. When the buffer is terminated (current address equals ending address), monitor control will cause the EI Active flip-flop to be set. At this time, the interrupt requests channel and function priority. The special address (interrupt entrance address) is transferred to S from the channel and function translators. This causes the next instruction for the computer program to be read from this address.

Operating Modes

The computer program initiates and controls the input/output mode of operation and selects the proper I/0 channel to be set in the active mode. The modes available are the input mode, output mode, interrupt mode, and the buffer mode.

INPUT MODE.–The input mode is initiated by a programmed instruction when either the computer receives an external interrupt and the associated external interrupt code word or when it receives an input data request and the associated data word.

When an input data request is received from a peripheral device, it enters the appropriate request circuits. To honor the request, the computer enables the appropriate channel to gate the request to the priority circuitry. The priority logic determines the priority rating of the request and also supplies the memory address which indirectly specifies where the data is to be either read from or stored.

The function selected by priority is an input data transfer; the data present at the input amplifiers for the selected channel is gated into the Z register and stored in memory. The computer sends an input data acknowledge (ID ACK) signal to the unit which sent the data. Upon receiving the acknowledge signal, the peripheral unit drops the input data request line.

OUTPUT MODE.–The output mode is initiated when the programmed instruction specifies a data transmission to a peripheral device. The I/0 section translates the program instruction, accesses memory, places the data in the appropriate output C register, and energizes the specified external function or output data acknowledge control line to notify a particular external equipment that a data buffer is present. The data transfer consists of either an external function code word accompanied by the external function signal or data words accompanied by an output data request. The manner in which the computer initiates an output control word transmission is dependent upon the capability of the receiving peripheral device to generate an external function request signal. For peripheral equipment which cannot generate an external function request, the computer requires an f = 13 instruction (k - 1, 3) to generate the external function signal and control word. Therefore, the transmission of a control word is synchronous with the computer program.

When the peripheral equipment is capable of generating an external function request, the signal interrupts the main computer program and causes the computer to select the appropriate I/0 channel. Once the communication link has been established, the computer returns to the main program, and the transfer of output data proceeds without program reference until completed.

If the function selected by priority was an output data transfer or external function transfer, the data is transferred from memory via the Z register to the C registers for transmission to the peripheral unit.

INTERRUPT MODES.–Provision is made to permit interruption of a running program by an event which may occur asynchronously with the program. Both external and internal interrupts may be generated. Either type of interrupt

causes the computer to discontinue the running program and to execute the instruction located in one of the permanently assigned external or internal interrupt entrance registers listed in table 4-4

External Interrupts

An external interrupt results from an external unit placing a signal on an external interrupt line. The accompanying bit-position coded, 30-bit word on the data lines defines the special condition which exists at the external unit originating the signal. When an external interrupt transmission is recieved, computer program control is transferred to a special subroutine for processing the interrupt. The interrupt causes the computer to discontinue the normal sequence and to execute the instruction obtained from the core memory address (00020 +$\hat{j}$) corresponding to the interrupt source (table 4-4).

Address 00020 + $\hat{j}$ serves as a subroutine entrance by containing a return jump instruction. The return jump instruction transfers the contents of P (address of next instruction) to the first address of the subroutine, thereby providing a subroutine exit. Program control is then transferred to the second subroutine address, and the interrupt is processed.

Internal Interrupts

Two types of internal interrupt signals are produced by the I/0 section. Internal interrupts are generated whenever a buffer, which has been initiated with a monitor, terminates at the end of the transfer. Fault interrupts are caused by either executing an illegal function code (f = 00 or 77) or by a time-out interrupt on any of the intercomputer channels.

Buffer with Monitor

During a buffer with monitor, data words are transferred sequentially, starting at a given address through a terminal address, on the specified input or output channel. Completion of the buffer causes an internal monitor interrupt to the input, output, or external function monitor interrupt entrance register (table 4-4) assigned to the input or output channel. The monitor interrupt entrance register contains the next instruction. As an example, a monitor interrupt entrance register may contain the following type of instruction.

650nn nnnnn–exit to an interrupt subroutine for remedial action.

This subroutine ends with a 601nn or 66 instruction which clears the internal interrupt mode; then returns control to the main routine.

During the transmission of external function and/or output data words between computers, the transmitting computer holds the word in the output register associated with the specified channel until a resume signal is received or until a specified time has elapsed. Failure to receive a resume signal within the specified time causes a time-out interrupt to the intercomputer time-out interrupt entrance register assigned to the computer (table 4-4). Unless otherwise specified, the time-out interrupt is generated after a time period of one to two seconds has elapsed. The length of time period is computed by: time = $1/1024 \times 2^N$ seconds, where N may be any integer from 0 to 30. Note that only on intercomputer channels will time out interrupts occur.

Buffer Without Monitor

During a buffer without monitor, data words are transferred sequentially, starting at a given address through a terminal address on the specified input or output channel. No monitor interrupts occur at the completion of the buffer.

FUNCTIONAL SCHEMATICS

The functional schematics are detailed block diagrams of the logic circuits that are required to perform a specific function. Figure 4-33 illustrates the basic symbols that are used in making up the functional schematic for the CP-642B.

The inverter or driver (fig. 4-33A) is an amplifier that causes signal inversion. The logic term, 10J09, is the notation that identifies that unique logic circuit. The card type notation,

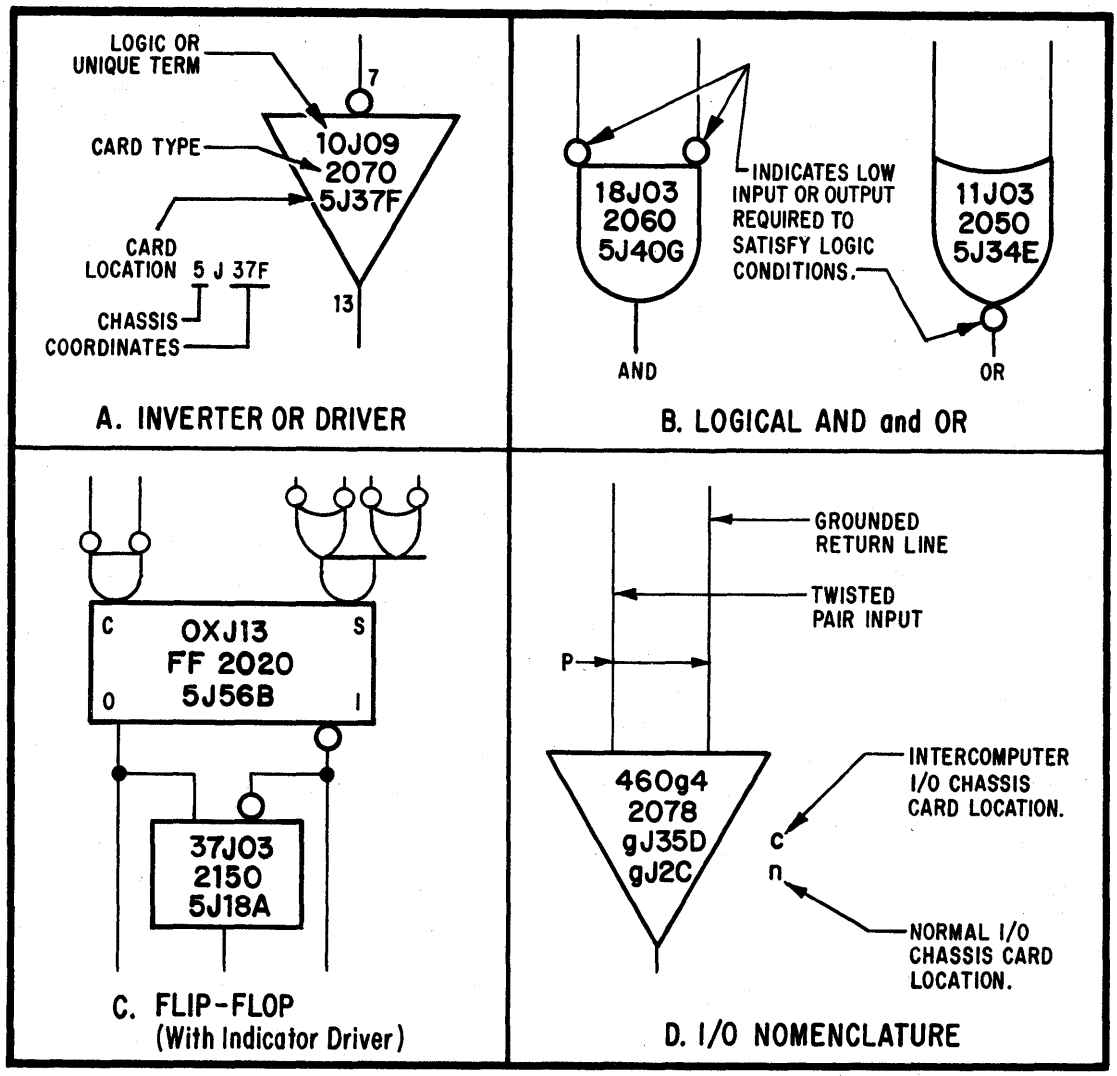

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Figure 4-33.—Typical logic symbols.

2070, identifies the type of card (of a possible 83 different types). The card location term, 5J37F, specifies the jack on a chassis that the card is to be plugged into. Card locations will be discussed later in this chapter.

Figure 4-33B illustrates the logic symbols that are used for AND and OR circuits. The small circles on the inputs and outputs are used to indicate that a low logic level is required to satisfy the logic condition.

Figure 4-33C shows the symbology for a flip-flop and a special circuit called an indicator driver (used to light front panel neon lamps). In the logic term OXJ13, the X is to be replaced with a 1 to specify the set side, or a 0 for the clear side.

Figure 4-33D illustrates the special nomenclature used with I/O chassis printed circuit cards. In the logic term 46Qg4, the lower case g is used to indicate that the chassis number should be inserted in place of the g to refer to a

specific chassis. This eliminates duplication of I/0 chassis functional schematics. The lower case c and n beside the symbol are used to indicate whether the chassis is an intercomputer I/0 chassis or a normal I/0 chassis.

Figure 4-34 is a representative functional schematic. The input signal description, source logic element, and source figure number are normally located on the top of the schematic. The input signal description for pin 14 of 11J03, L ⇒ MC, is interpreted as "a low signal level means master clear." Clock phases are identified by ∅ and the phase number, e.g., ∅2. The signal output logic destination, figure number and signal description are usually located at the bottom of the page.

PARTS LOCATIONS

Figure 4-35 illustrates the locations of the movable plugs and the memory and logic chassis for the CP-642B. The movable plugs mate to corresponding jacks mounted on the sides of the chassis. The plugs are numbered sequentially from the front of the cabinet to the back on the left and right sides, respectively, then from top to bottom.

The main power supply for the computer is located under chassis A13 and is mounted on the cabinet bottom. This power supply provides the d.c. voltages used by the computer logic and memory circuits. There is a separate console power supply that produces the voltages for the indicators, switches and relays on the operator's console.

The plenum assembly on the rear of the cabinet is an air space that also holds the blowers and heat exchanger (for a water cooled cabinet). Removal of the blower and/or heat exchanger requires that an inner plate (referred to as inner skin) inside the computer cabinet be removed. Refer to the appropriate technical manual for these procedures.

The I/0 and power connections are shown in figure 4-36. These plugs are mounted on top of the computer cabinet, and the top cover must be removed to have access to them.

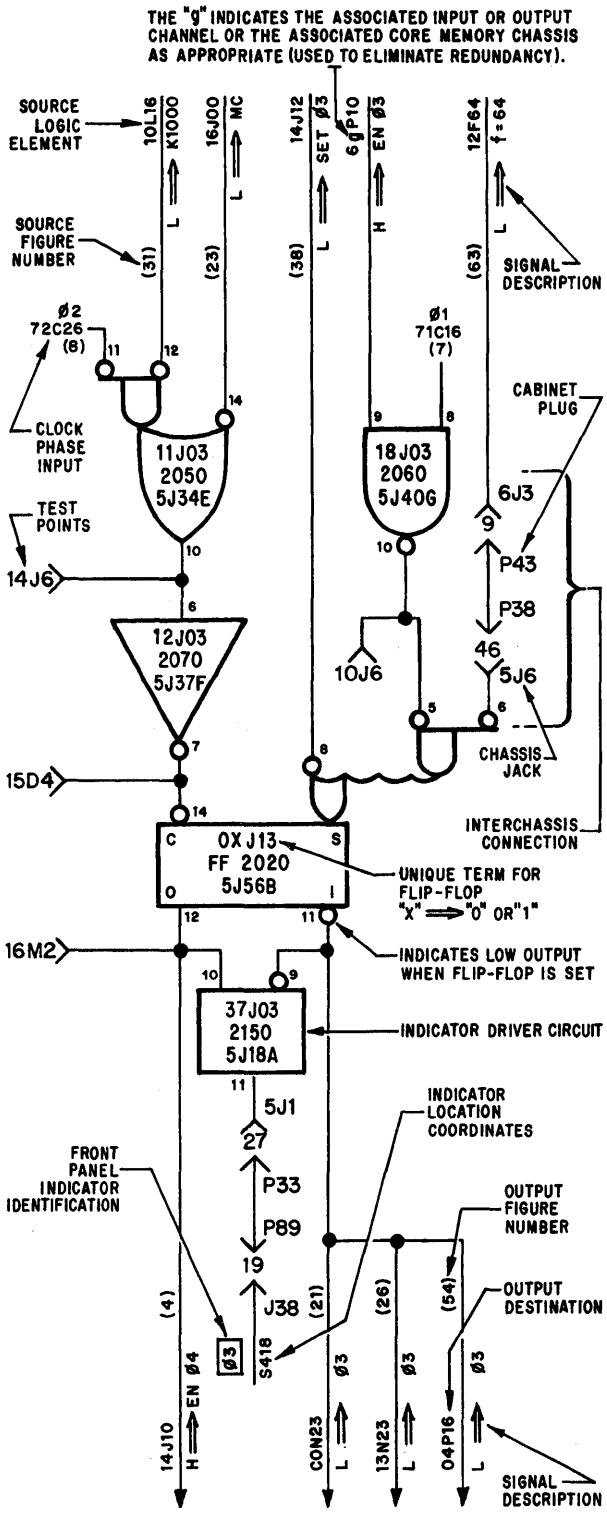

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Figure 4-34.—Representative functional schematic.

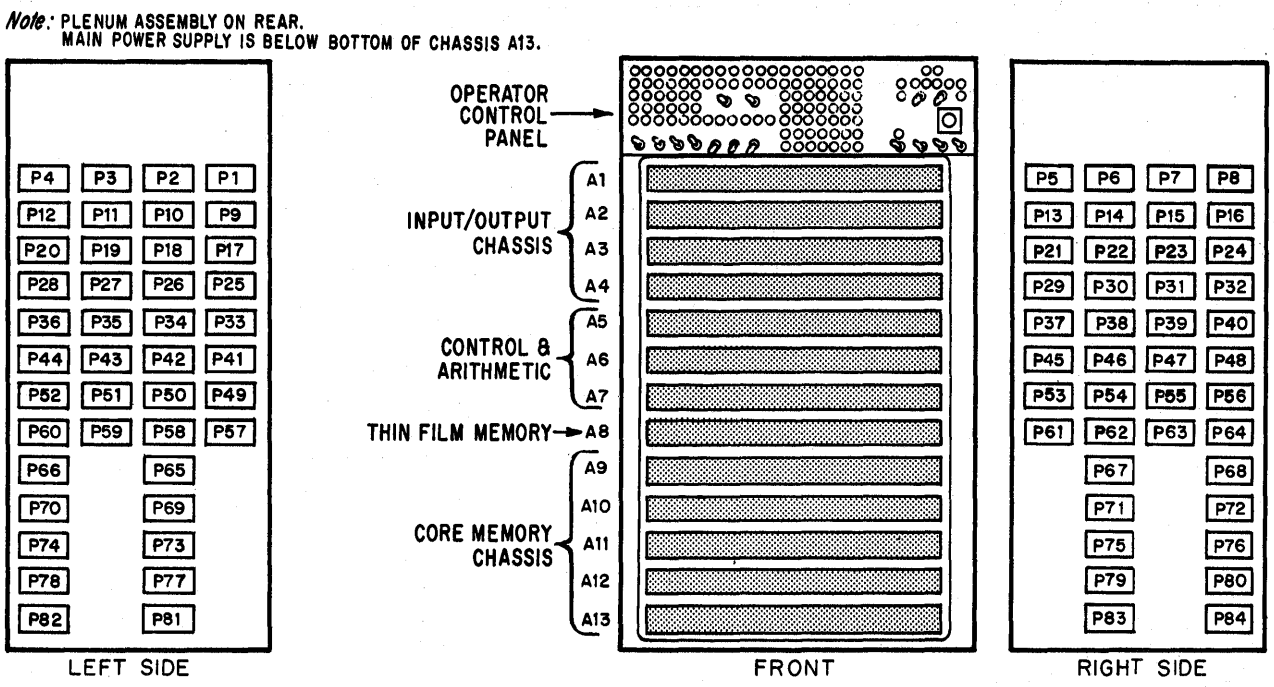


Figure 4-35.—Chassis and plug locations.

Test Point Location

Each logic element has a test point at its output (fig. 4-34) that is connected to a test block on the front of each chassis as illustrated in figure 4-37A. From the test point designation on the functional schematic, the test point can be located exactly. For example, test point 10J6 of logic element 18J03 (fig. 4-34) is located on test block 10 (fig. 4-37A) coordinated J6 (fig. 4-37B). The chassis number is not specified in the test point designator since it is the same as the logic element.

CARD LOCATION ON A CHASSIS

Each computer chassis is divided into seven card rows (A through G) and 62 card columns. Figure 4-38 is a diagram of a partial chassis map that is used to locate a specific card.

MANUAL OPERATIONS

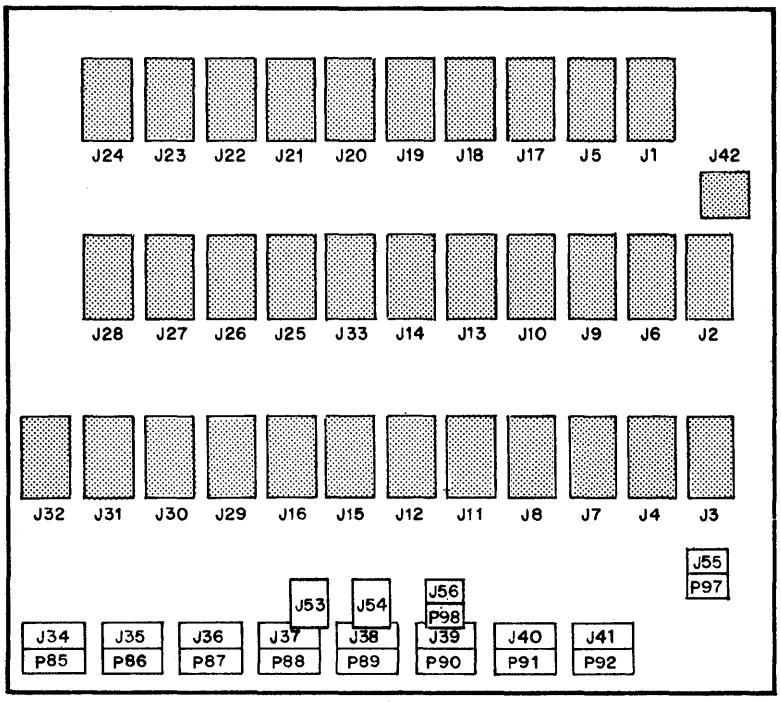
The computer logic provides for manually writing into and reading from memory using the front panel controls. These provisions are intended for use during maintenance procedures and for testing and debugging programs. The following steps detail how to use these provisions with the Q register. However, similar operations are accomplished using the A register and its related instructions.

Manual Write, Single Word

(1) Master clear the front panel
(2) Set AfEn in Active Seq indicators
(3) Set U = 14030 yyyyy (Store Q to address specified by yyyyy)
(4) Set Q = word to be stored
(5) Press OP STEP
(6) Press START-STEP. Computer stores word in Q to address specified by UL.

Manual Write, Consecutive Words

(1) Master clear the front panel
(2) Set AfEn



Legend:

CABINET CONNECTOR	FUNCTION
J1 and J17	CHANNEL 0 INPUT/OUTPUT
J2 and J18	CHANNEL 1
J3 and J19	CHANNEL 2
J4 and J20	CHANNEL 3
J5 and J21	CHANNEL 4
J6 and J22	CHANNEL 5
J7 and J23	CHANNEL 6
J8 and J24	CHANNEL 7
J9 and J25	CHANNEL 10
J10 and J26	CHANNEL 11
J11 and J27	CHANNEL 12
J12 and J28	CHANNEL 13
J13 and J29	CHANNEL 14
J14 and J30	CHANNEL 15
J15 and J31	CHANNEL 16
J16 and J32	CHANNEL 17
J33	COMPUTER SET CONTROL INTRODUCER
J34 THROUGH J41 & P85 THROUGH P92	INTER-CHASSIS CONNECTORS
J42	EXTERNAL REAL-TIME CLOCK
J53	MOTOR GENERATOR (REGULATED 400Hz POWER)
J54	SHIPS POWER (UNREGULATED 400Hz POWER)
J55/P97	AC POWER DISTRIBUTION
J56/P98	BLOWER POWER DISTRIBUTION

CABINET CONNECTOR	FUNCTION
J1 and J17	Channel 0 Input and Output
J2 and J18	Channel 1
J3 and J19	Channel 2
J4 and J20	Channel 3
J5 and J21	Channel 4
J6 and J22	Channel 5
J7 and J23	Channel 6
J8 and J24	Channel 7
J9 and J25	Channel 10
J10 and J26	Channel 11
J11 and J27	Channel 12
J12 and J28	Channel 13
J13 and J29	Channel 14

CABINET CONNECTOR	FUNCTION
J14 and J30	Channel 15
J15 and J31	Channel 16
J16 and J32	Channel 17
J33	Computer Set Control Introducer
J34 through J41 and P85 through P92	Inter-Chassis Connectors
J42	External Real-Time Clock
J53	Motor Generator (Regulated 400-Hz Power)
J54	Ships Power (Unregulated 400-Hz Power)
J55/P97	AC Power Distribution
J56/P98	Blower Power Distribution

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Figure 4-36.—I/O and power connections.

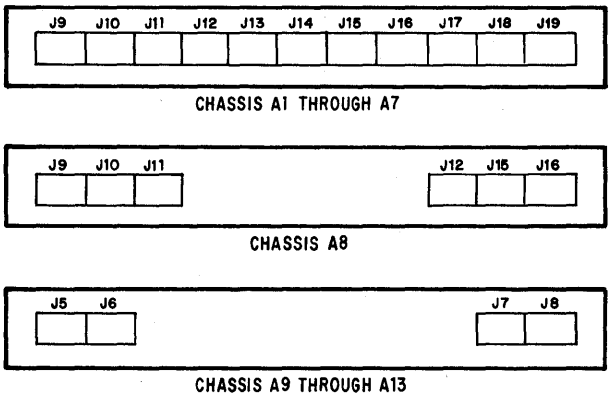

Figure 4-37.—Test point locations.

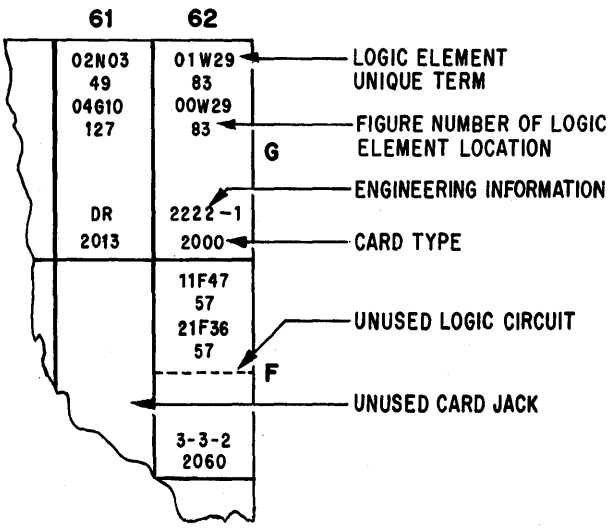

Figure 4-38.—Partial chassis map.

(3) Set U = 70100 00003 (Repeat next instruction—the repeat count of 3 is used only to enable the repeat mode)
(4) Set DISCONNECT B7 up
(5) Press OP STEP
(6) Press START-STEP (Activates repeat mode)
(7) Set U = 14030 yyyyy (yyyyy = lowest address of desired storage locations)
(8) Set Q = word to be stored
(9) Press START-STEP. Computer stores word in Q to address specified by UL. To store additional words at consecutive addresses, clear Q, enter new word in Q and press START-STEP.

Manual Read, Single Word

(1) Master clear the front panel
(2) Set AfEn
(3) Set U = 10030 yyyyy (Enter Q with contents of address specified by yyyyy)
(4) Press OP STEP
(5) Press START-STEP. Computer enters Q with (yyyyy).

Manual Read, Consecutive Words

(1) Master clear the front panel
(2) Set AfEn
(3) Set U = 70100 00003
(4) Set DISCONNECT B7 up
(5) Press OP STEP
(6) Press START-STEP
(7) Set U = 10030 yyyyy (Enter Q with contents of address specified by yyyyy. yyyyy = lowest address of storage locations)
(8) Press START-STEP. Computer enters Q with (yyyyy). To read next sequential address, press START-STEP.

MANUAL TESTS

There are several manual tests that are used to assist in trouble isolation. These tests use the manual read and write procedures previously described. Some of the tests are briefly described in the following paragraphs. Detailed description and operating procedures are left to the appropriate technical manuals.

55 Test

This test exercises the computer's ability to write any desired pattern of ones and zeros into all core memory without using any memory address to store the test. This test uses a repeated 55 instruction that is manually loaded in U. It does not write into control memory and can perform its operations at any cycle rate. The 55 test requires that test point 5J11H4 be grounded. Grounding any other test point may cause memory damage.

Memory Capacity Test

The memory capacity test checks core memory by causing the quantity stored at each address to be the address itself. Therefore, when memory is read out, the contents will be the same as the address.

Magnetic Core Cycling Test

This test permits the checking of a particular word and its associated circuitry. The program continually reads the same address so that the waveforms can be checked to isolate the malfunctioning circuits.

Core-Read Marginal Check

The core-read marginal check uses the 55 test to check memory under marginal conditions. By means of the margin switches, the signals to the sense amplifiers are increased (low margins) or decreased (high margins) in width. With an increase in width, less signal is clipped, and with a decrease in width, more signal is clipped and less signal is available to the amplifier; therefore, greater sensitivity is required of the amplifier to pass the signal.

Repetition Rate Test

This test establishes that the memory is capable of operating properly at a maximum repetition rate. It uses a repeated enter Q instruction which has a cycle time of four μs (250,000 memory references per second).

Cycle Time Test

The cycle time test checks the control memory cycle time by measuring the time between the leading and trailing edges of a signal to ensure that the cycle time is less than 700 ns at 50 percent amplitude.

SUMMARY

The CP-642B is divided into the four functional sections explained in some detail in this chapter: Control, Arithmetic, Memory and Input/Output. In the simplest terms each of these sections performs the operations that are generally associated with its name.

The control section provides the timing, instruction translation, and coordination of operations between the other sections. The arithmetic section performs the arithmetic logical operations of the computer. The I/O section allows the computer to communicate with peripheral devices or other computers. Although it relies on the control section for timing, the I/O section has its own control function and may operate in parallel with the rest of the computer. The memory section provides the computer with permanent storage area for programs, constants, and buffered I/O data.

CHAPTER 5

NTDS PERIPHERAL EQUIPMENT

Peripheral equipment handles data before or after the computer uses it. The terms ancillary or auxiliary equipment are synonymous. Peripheral equipment covers all on-line (i.e., communicates directly with the computer) equipment, and in some applications, might also include off-line equipment. However, in this text, peripheral equipment will only refer to on-line equipment. Off-line equipment is considered to be in a separate category known as electronic accounting machines (EAM). Within the NTDS, the identifier "peripheral equipment" is further restricted to equipment that can load, store, or directly control the computer program(s).

NTDS peripheral equipment includes the **RD-243 Magnetic Tape Unit, the RD-231A Paper Tape Cabinet (Unit), the OJ-212(V1)** Teletypewriter, the C-3675A System Monitoring Panel, and the MX-3195 Universal Keyset. The peripheral equipment block diagram shown in figure 5-1 illustrates the manner in which these devices are usually connected in the NTDS.

This block diagram may vary slightly between installations with the addition of switching units. The keyset central multiplexer (KCMX) unit shown in figure 5-1 is usually considered a data conversion device and will be treated as such later in this text. For now, think of the KCMX as an interface or switching equipment that will select a keyset and pass the information to the computer.

MAGNETIC STORAGE

Magnetic storage is an important aspect of data processing. In order to adequately explain even one piece of magnetic storage equipment (the RD-243 Magnetic Tape Unit), it is first necessary to survey the entire subject area.

PRINCIPLES OF MAGNETIC STORAGE

Magnetic storage principles are generally based upon the fact that a current can be generated in a conductor when there is a change in the lines of force that cut through it. Conversely, change a current in a conductor, and there is a change in the lines of force that emanate from it. Rotating a conductor in a magnetic field creates a current. Changing the physical distance between a conductor and a source of magnetic flux also produces a current.

TYPES OF MAGNETIC STORAGE DEVICES.—Of the four general types of magnetic storage devices, three (tape drives, disk files, and drum units) depend upon a change in the physical distance between a conductor (a read/write head) and a source of magnetic flux (the magnetic oxide surface) to induce a current that is detected by read circuits.

Core memories (the fourth type) are rigid structures in which X-Y drive currents combine to force the core at their cross-coordinate to change state if a logic "1" exists there. The impedance given to the drive currents while a "1" core changes state affect the induced current in the sense line. This causes the read circuits to set a corresponding "1" in the memory register (Z register). This destructive readout technique for core memories requires a write operation to follow a read operation to replace the contents.

The other three types of magnetic storage devices do not destroy memory contents with a

Also, disk files and drum units exist that far exceed the storage capacity attributed to tape drives.

On data recovery times, magnetic core memories are often regarded as the fastest, though in actual fact many disk files and drum units are faster. However, some provision is required to make superfast equipment compatable with slower equipment, since I/O transfer times are set by the speed of the slower equipment. Additionally, the computer's data transfer rate is not a constant, but varies with the demand for memory access from the clock, control, arithmetic, and I/O sections.

If the demand is high, the data transfer rate per I/O channel decreases. If the computer's rate drops below the minimum level that the magnetic storage device is able to maintain, a loss data error will occur on read operations, or a missed frame error will occur during write operations. These errors are usually detected by the magnetic storage device's logic and indicated to the computer as a status bit in the external interrupt word that follows a data transfer.

PRINCIPLES OF MAGNETIC STORAGE DEVICES

Magnetic storage devices, such as magnetic tape drives, disk files, and magnetic drums generally rely upon a few simple precepts. The first is that a change in flux induces a current. The second is that a change in distance between two objects, with at least one of them being magnetized, will produce a change in flux. These two principles enable read/write heads to supply a current when fixed magnetic patterns on a prerecorded surface move past them. This is the basic read operation. A third precept, that an electrical current will produce a magnetic field, enables the read/write heads to realign the patterns of magnetic flux on the tape, file, or drum surface when a current is driven through the coils in the heads. If information is contained in the magnetic patterns, this would be a write operation. If the pattern is essentially neutral, it is considered an erase operation. Direct Current erase operations convert all flux patterns to the same polarity for the length and width of the surface where they are applied. Alternating Current erase operations scramble the domains on the surface so much that no discernible magnetic pattern remains. Chapter 6 of *Digital Computer Basics* amplifies magnetic recording principles.

BASICS OF MAGNETIC STORAGE DEVICES.–In most magnetic storage devices, the heads, whether erase, read, write, or read/write, are "fixed" during a read or write operation. The relative motion between heads and surface is supplied by mechanics to the oxide surface. This surface is generally a form of "rust" of a metal alloy having desirable magnetic characteristics. The oxide is uniformly spread and adhered to some type of backing, and may also be coated in some applications. In disk files and drums the backing is usually a rigid surface. With tape drives, the backing is a strong, flexible tape, such as Mylar, which is wound on a reel. Magnetic recording surfaces are delicate, sensitive to dust and other airborne contaminants, and subject to wear whenever physical contact results in friction.

Disk files and drum units offer superior protection to their surfaces in comparison to tape drives. Therefore, comments in this text on maintenance and in chapter 8 of *Digital Computer Basics* are primarily in regard to tapes. One additional note concerning all oxide surfaces: Do not handle unless necessary. Avoid touching the oxide surface, particularly with disk files and drums. Human skin contains oils and acids; it sheds and carries contaminants, and is, in general, harmful to both the oxide surface and the precision mechanics used in the equipment. Clean thoroughly all surfaces after contact following prescribed techniques.

Mylar tape is sensitive to extremes of heat, sweating and sticking together on the reel and even shrinking and shriveling when overheated. Mylar may become stiff or even brittle when too cold. The flexible adhesive may soften, sweat, or run when overheated, or harden and lose its flexibility or ability to adhere when chilled. Increased molecular activity caused by heat or by sudden impact could cause domain realignment of the oxide coating and subsequent loss of information. Excessive strain on the tape will cause it to elongate, losing its uniform width and thickness. Airborne contaminants, which may be gaseous, droplets, or particles in nature,

may be attracted to the tape by static charges built up through tape movement and friction. These contaminants may chemically or mechanically attack the tape or transport.

Lack of proper maintenance and prolonged neglect of tape transports and/or magnetic tapes will result in deteriorated equipment and system performance.

MAGNETIC TAPE MAINTENANCE RESPONSIBILITIES

The basics of magnetic tape are covered in chapter 6 of *Digital Computer Basics*. Additionally, there are certain terms, tests, tape upgrading techniques, and equipment used in providing improved tape performance and increased lifespan.

There are also certain tests, test tapes, and both electrical and mechanical adjustments that are designed to maintain magnetic tape drives (also called transports) at optimum performance levels. Tape maintenance is normally a data processing technician responsibility, though DSs are responsible for their own maintenance tapes. Tape drives are a DS maintenance responsibility, though DPs often perform normal cleaning tasks as a part of their operator responsibilities. In addition, DSs may be required to support equipment needed by DPs in their tape maintenance program. A grasp of the entire subject area is required for proper maintenance support.

MAGNETIC TAPE MAINTENANCE.—There are several steps involved in magnetic tape maintenance, each one covered by a term. The term will be followed by a brief description of the step involved.

Storage.—Storage containers are provided for magnetic tape reels. These help reduce the possibility of contaminants or humidity from affecting tapes. Tapes are always stored on end rather than on their side to prevent possible reel warpage or tape settlement on one reel edge. Extreme tape settlement can cause an elongated crease in the tape surface the full length of the tape.

Cleaning.—Tape cleaning is accomplished by machine, not by hand. Some tape transports provide a limited degree of tape cleaning effort. Others provide none. A special machine, the tape cleaner, is provided where required for this function. The tape cleaner normally performs two functions: First, the oxide side of the tape is "shaved" by a series of razor edges to remove loose oxide and embedded particles. Next, the tape on both sides is wiped down with a cleaning solution and wiped again to remove any oxide or contaminants that remain. The cleaning solution may be applied by a dip, a wick-feed, or an impregnated gauze surface.

Ethyl alcohol (90% or better) is often used as a cleaner for both tapes and tape drives, though the recommended agent should be used whenever possible. Tape cleaners do not alter the magnetic flux patterns of a tape, and theoretically can clean even tapes containing saved information. However, this is not a normal procedure and should not be attempted until a test effort supports the possibility, and even then only if an actual need exists.

Stripping.—Different sections of the tapes wear at different rates. The section near the beginning of the tape label receives the greatest amount of wear, with the wear rate progressively dropping off in sections toward the middle, then again toward the last part of the tape. Stripping a tape involves cutting away enough of the leading section of tape to remove an excessively worn or badly damaged area.

Maintenance tests generally reveal a high incidence of errors where a tape section has gone bad. When no errors are encountered, entry into a good section of the tape is indicated, and the tape can be stopped, separated, and the bad section removed from the takeup reel and discarded. The good section can then be looped securely by several turns onto the takeup reel and a new BOT label inserted. For best results, some of the good section should be discarded also to eliminate areas that are approaching the wear limit. This will extend periods between stripping actions and will also result in fewer tape errors when operating. Tapes less than 600 feet long are generally discarded as being too limited in storage area. However, these tapes can still serve DSs as "mechanics" tapes to be discussed later.

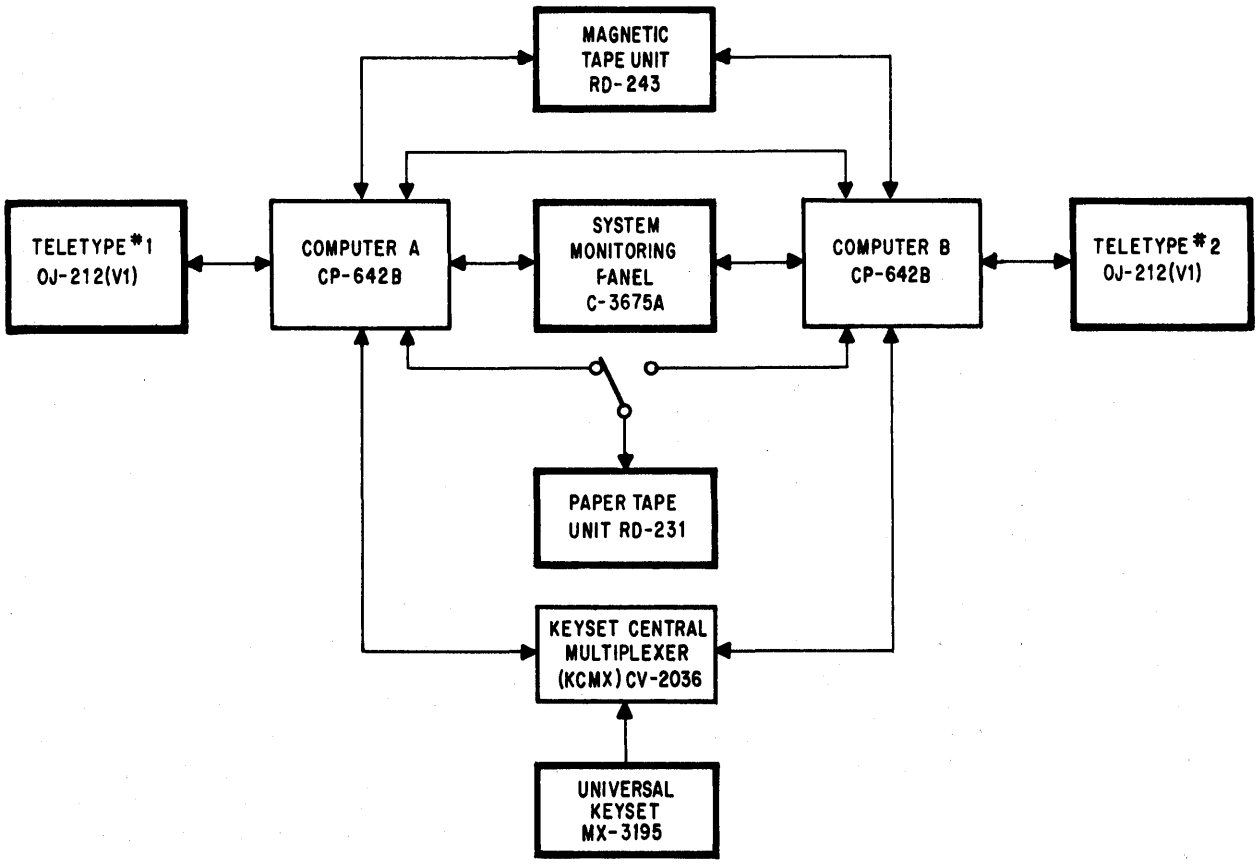

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Figure 5-1.–NTDS peripheral equipment block diagram.

read operation. Data is recorded as magnetized spots on the surface. The change in flux patterns between adjacent spots on the surface is detected by the read/write head as a very small current. There is no change in the spots themselves (unless a current is being supplied to the head from the electronic section on a write or erase operation). Lines of force created by write currents would cause a change in the magnetic patterns on the surface and, if strong enough, would entirely cancel the previously recorded pattern. When write or erase currents are too weak, some of the prerecorded domains on the surface retain their polarity. This causes a condition known variously as sound-on-sound (audio recordings), print-through, or add-on recording. This is not a desirable condition in magnetic recording of digital information.

If a write current is too strong, the expanded flux field will overlap adjacent fields or surface areas and produce a condition known as crosstalk. This is not a desirable condition either.

BASIC RECORDING TECHNIQUES.–The principles of RZ (return to zero) and NRZ (nonreturn to zero) recording techniques are covered in chapter 6 of *Digital Computer Basics*. In general, NRZ is found in newer equipment since it allows for higher bit densities on the recording surface. RZ and NRZ recording techniques are incompatible with each other. RZ detects the direction of flux change between adjacent spots as either a 1 or a 0. NRZ detects the fact that there was a change, in either direction, as a 1 (no change is a zero). RZ

requires an initial period during write operations to switch to a zero polarity if a "1" is to follow another "1", or to switch to a one polarity if a "0" is to follow a "0". During read operations, the logic must be inhibited from reading data during each initial phase.

If a read enable occurs during the wrong half-portion of a RZ initial and data frame, a "1-0" or a "0-1" sequential pattern would not be read at all, while a "1-1" or a "0-0" pattern would be read as a 1's complement for each bit. To prevent this, RZ devices often incorporate a timing track to aid the logic in determining which are the data frames. These timing tracks are called sprocket tracks with most RZ-type tape drives, and are called clock tracks with disk files or drum units. Some NRZ-type devices also use timing tracks. As an example, most RZ or NRZ disk files and drum units have clock tracks. Equipment with timing tracks usually keeps count of the number of clock phases encountered in the timing track during a read operation. If a clock phase is lost somewhere, the count at the end will be odd. Some equipment even checks to see if two polarity changes in the timing track are consecutively in the same direction. Such occurrences are not normal and are reported by the equipment to the computer as sync (synchronous) errors in the equipment's external interrupt word. Sync errors mean some of the data read may be invalid as a result of reading the wrong half-cycle.

REDUNDANCY.—Redundancy begins with a certain number of information bits. Any additional bits required which can aid in detecting a loss, gain, or change in the information bits are redundant in nature. There are different types of redundancy in use. Some are a hardware function (produced automatically by the equipment). Some are a software option (programmed into the computer). In general, if a single redundant bit is used to indicate that all data bits were summed and found to be even or odd, it is called a parity bit. Odd parity is named because all data bits were summed and found even, but by setting the parity bit the total (including the parity bit) became odd. Even parity converts odd count sums to even. Lateral parity in tape drives is the parity bit within each frame. Longitudinal parity is the parity bit(s) that follows a complete block of data. A check-sum is normally a software function where an extra word is put on at the end of a data block, which is the sum of all the words in the block. On a read operation, the words are summed again and compared with the last word read by the computer program—or the complement of the sum is used, causing the total of all words read to always add to zero.

Redundant mode is a hardware function and is so named because every data bit is written or read twice, either bit-by-bit, octal-by-octal, frame-by-frame, or word-by-word. The format depends upon the equipment design.

MAGNETIC STORAGE DEVICES

As mentioned previously, there are currently four widespread types of magnetic storage devices. The magnetic core memory, already discussed, is one type. The RD-243 Magnetic Tape Unit is another type, and will be discussed in this chapter. A disk file, the RD-281, will be covered in chapter 5 of *DS 3 & 2, Vol. 2.* The Navy does not employ magnetic drum units on a large scale, and these will not be dealt with in this text. An introduction to magnetic storage devices appears in chapter 6 of *Digital Computer Basics.*

TERMINOLOGY.—Several imprecise terms are utilized in familiarizing personnel with the capabilities and limitations of a particular device. Words like large, medium, or small memory capacity; or high, medium, or low speed; or fast, medium, or slow access or data recovery times are not uncommon. These are comparison terms and most often are based upon (1) how this device compares to other equipment of similar design, (2) how it compares to other types of peripheral equipment within a system configuration, or (3) how it compares to the computer itself. Magnetic storage devices are generally compared to other magnetic storage devices. As an example, tape drives are often regarded as having the largest memory capacity, with core memories having the smallest of the four types. Yet computer core memories are regarded as medium or large when compared with the storage capacity of other peripheral devices.

Sections of tapes are not spliced together to create new tapes for several reasons: First, tape splices are generally the weakest point in a tape and could separate, resulting in tape spill, possible transport damage, and loss of data on either side of the separation where respliced if cutting or trimming is required. Second, tape splices are poor areas for performing write or read operations and appear as "bad spots," which must be programmed around. Third, the wear factor for spliced sections of tape will not be proportional, but will be universally bad or poor at this point. If any section wears out, another splice would be required, with continuing decline in performance and reliability. Information on a tape is generally lost whenever any of these actions are taken.

Tape Cling.—Tapes can build up static charges under a variety of conditions, and they also can adhere layer-to-layer from changes caused by temperature, humidity, or long shelf life. This tendency to cling can seriously affect tape performance and must be coped with. The first step is to determine the probable cause(s) if possible. The second step is to restore any tapes immediately required by the operating system. The third step is to take corrective steps to cope with the cause(s). The fourth step is to insure that all tapes are properly restored to usefulness. The foregoing steps will probably be a joint operator/maintenance personnel operation.

Probably the best single solution to tape cling is to use the tape cleaner. The unwrap-wrap, unwrap-wrap action of moving the tape from one reel to another and back will eliminate static cling, while the cleaning action should counteract cling from other causes. Another technique is to perform a series of wrap-unwrap operations with the tape transport. This can be accomplished at high speed with transports having both wind and rewind functions. For transports having only a rewind function, the feed reel can sometimes be mounted on its reverse face as the takeup reel and rewound onto an empty reel mounted as the feed reel. The reels would then be switched to their normal positions, reversing the faces in the process (the feed reel would now have the correct face out). A second rewind would restore the tape properly to the feed reel. A third technique is to gently rap the tape reel against some fixed surface, rotating and alternating between the two sides from time to time. This is accomplished in somewhat the same manner of rapping a tight jar top with a knife handle to loosen it. This may loosen some static cling and cause the tape layers to shift. It may even loosen cling or adhesion due to other causes. However, severe rapping could result in information loss. A fourth technique is to simply transfer stored tapes to a suitable environment and to check them periodically to see if they have recovered.

Degaussing.—Degaussing a tape involves a machine that applies a varying strength a.c. induced magnetic field to a tape. The result will be the total destruction of any stored data on the tape and the complete nullification of all magnetic flux patterns.

The domains will be scrambled, and the tape will be totally unpolarized. Degaussing a tape can serve two purposes: (1) it provides for a complete tape erasure when desired, and (2) it eliminates the accumulation of stray flux patterns on the tape that result in a rise in background tape noise levels. These flux patterns can sometimes resist the efforts of the small tape transport erase head to cancel them.

Certification.—Certifying a tape is the final stage in most tape maintenance programs. Tape certification involves the use of a tape certifier machine that performs digital and analog evaluations of a tape against calibrated standards which are far in excess of the operational requirements for most tape transports. Every fraction of the tape is subjected to intense scrutiny as to its ability to record high bit densities, retain flux patterns, and be demagnetized. The tape certifier will shave and clean the tape prior to testing it, check background noise levels, and check bit parallelism (skew) across the tape. It also leaves the tape completely erased.

The tape certifier permits operator monitoring and intervention when any spot on the tape fails to pass. The operator is shown the exact failing spot, can determine the cause through a microscope, and can take appropriate action. It could be a small particle embedded

that can be cleaned or gently scraped away. It could be a pinhole in the tape or a spot where all the oxide wore away, in which case the tape may be separated with the smaller section discarded, or with both sections retained on separate reels.

Any tapes that are certified as being error-free will probably give months of satisfactory service. Tapes that are certified and found to be of too poor a quality for use can either be given to maintenance if needed, or destroyed. Tape destruction for systems running classified material is normally to strip the tape entirely off the reel and have it burned with other classified documentation.

Tapes that are certified as marginal in some respects are evaluated individually. Some experience is needed with the equipment, the tapes, and with system requirements before a determination can be correctly made on tapes in this category. Certifying a tape does not just measure its capabilities, but does a great deal to restore its full potential.

The machines mentioned here are not universally employed. Many commands cannot provide them to every computer system. Some are available periodically, to outside requests. In general, DPs provide operator functions for these machines, and DSs provide for maintenance. The tape certifier, in particular, requires extensive maintenance effort to keep it functioning at optimum levels.

TAPE TRANSPORT MAINTENANCE.—Every tape transport is somewhat unique. It is built to certain tolerances. It is also subject to wear, deterioration, and component value changes. With these variables in mind, certain adjustments are designed into the equipment, certain tests were devised to determine when readjustment was necessary, and certain standards were established to insure that the end product was the one desired. The Data Systems Technician is responsible for knowing which tests to use, what adjustments to make, and insuring that the equipment is kept up to standards. Basically, there are two classes of adjustments for tape transports, electrical and mechanical. The order of adjustments would normally be to perform all electrical checks and adjustments that are independent of mechanical settings, to then perform the mechanical adjustments, and finally, to perform the mechanically-sensitive or compensating electrical adjustments.

The technical manuals are usually very thorough in this area, and additional guidelines on maintenance frequency and procedures are provided by 3-M Maintenance Requirement Cards (MRCs).

Adjustments.—While procedures vary from one design to another, and may even differ between systems, certain types of adjustments tend to always surface. Among these adjustments are:

electrical:	voltage levels delays	
mechanical:	mechanical head skew transport adjustments stop-start times	(using a "mechanics" tape)
electrical:	read levels	(using a "skew" tape)
	write levels	(using a "levels" tape)
	electrical head skew:	
	read skew	(using a "skew" tape)
	write skew	(using a "levels" tape)*

*Setting write levels and write skew, and using a "levels" tape creates a "ls" tape.

A "mechanics" tape is one that is unsuitable as a storage medium because of poor quality. It is ideal for making mechanical adjustments, because these sometimes result in further tape damage that would ruin an otherwise good tape.

A "skew" tape is an exceptional quality tape that has been prerecorded with all ls data under exacting laboratory conditions. It provides a universal standard for tape transport adjustments. It should never be written on unless replaced and downgraded to the status of a "levels" tape.

A "levels" tape is any tape believed or found to be of exceptional quality. It has uniform width and thickness, the oxide surface is

apparently unblemished, and consistent signal levels can be observed by oscilloscope for the width and length of the tape. A levels tape is necessary to accurately set write levels, and to provide a "ls" tape (sort of an in-house "skew" tape).

The word "skew" means to be distorted or to have an oblique course. This accurately describes the relationship the bits that form each frame of data across the different tape tracks can assume to each other if tracks of the head are not aligned properly across the tape. Unfortunately, common usage has distorted the original meaning of this word when referring to magnetic tape units. "Properly skewed," for instance, must be read as meaning that any skew has been corrected. Two other words, "deskew" and "reskew," have been introduced in some literature on this subject. In some instances these have only succeeded in making the matter more complicated. For correct usage, these three words should be employed in the following ways:

Skew—A transport is "skewed" if its tracks are not aligned parallel to each other. A tape can be "skewed" if it is not running straight across the heads, or if the bits forming each frame are not aligned parallel to each other.

Deskew—A transport or tape has to be "deskewed" when any problems regarding skew have been corrected.

Reskew—A process of removing any artificial methods of deskewing so that the natural skew of the transport can be used as the starting point of deskewing adjustments.

The tape used in deskewing adjustments is known both as a "skew tape" and as a "deskewing tape." The use of deskewing is obviously a better choice, since this tape has no skew. However, common usage has made "skew tape" acceptable.

When reading this text, or any other on this subject, remember that these three words are sometimes used interchangeably, and that the meaning of the word must be taken from its context.

Compatibility.—The overall purpose for these various adjustments and tapes can be expressed in one word: compatibility. The goal is to achieve uniform tape recordings that can be read by any tape transport that is designed to handle a tape of that nature. Compatibility must be achieved in two directions. One direction is time. Previously written tapes must still be readable in the present, and currently written tape will have to be readable in the future. The other direction is a lateral exchange between tape transports. This lateral exchange is marked by three milestones: (1) achieves compatibility with a single transport's own read and write circuits, (2) achieves compatibility between all transports within a system, and (3) achieves compatibility between systems. An extension from each milestone along the time axis is a necessary stop. Expressed in sequence, the steps would read as follows:

(1) Establish compatibility between the read and write circuits of each transport, once the read circuits have been adjusted to the standard provided by the skew tape.

(2) Insure that the transport can still process representative tapes it previously wrote and can still pass maintenance tests.

(3) Insure that the transport is compatible with other transports in the system by exchanging tapes. Reading each other's "ls" tapes and scoping the skew and levels circuits would provide some indications of the degree of compatibility, but a better way is to use a compatibility test that reads blocks of test data from a tape, then adds blocks of test data to be also read by it and by the next transport. These test tapes are called compatibility tapes.

(4) Insure that the transport is still compatible with prior tapes written by the other transports. Old "ls" tapes, or old compatibility tapes can be used for this purpose. Loading old program tapes or processing old data tapes might be sufficient if no better technique is at hand.

(5) Insure that the transports in one system are compatible with those of another system. Here a need exists for standardized test data tapes and compatibility programs, or program tapes, or processible data tapes will have to suffice. If none of these can be provided or used, an exchange of "ls" tapes may have to take place.

(6) *Same as (5), except the emphasis is again on older tapes.

Obviously, each step greatly increases the amount of testing that must be done. A compromise is required at some point between what is needed, what is wanted, and what would just be nice to have. Experience on the equipment will result in the deletion of steps that are apparently excessively redundant or nonindicative of problem areas, and the standardization of the remaining steps for that system. If the maintenance requirements specified by the MRC cards do not reflect the needs that experience dictates, then a 3-M procedure exists for making this fact known at the appropriate levels.

Logs.—Tape logs may be of further assistance to both operating and maintenance personnel. A basic tape log may be developed from the following headers:

(1) Recorded On (date and transport)
(2) Read On (date and transport)
(3) Comments (sync errors, parity errors, warped reel, unusable-permanent error, etc.)
(4) Initials

Each tape entry would normally start with a single Recorded On entry. As the tape accumulates Read On entries and Comments, a history of both the tape and the transports will unfold. Tapes that show a poor history should be recopies or regenerated (output recreated as a result of a program operation). The tape should then undergo testing to determine if the tape itself caused the problems or if the writing transport made a bad recording. Several tapes showing up bad on just one drive would strongly suggest that drive needs some attention. Tapes with exceptionally good histories should be noted and set aside as possible "levels" tapes when they are finally "scratched." (Scratched is the process of releasing a saved tape so that new information can be stored on it. A scratch tape differs from a blank tape only in that the blank tape has also been completely erased or degaussed.)

This technique of maintaining a log for correlation is a good practice, not just for tapes but for equipment too. Good technicians are usually able to retain and organize current events in their heads and can spot these correlations mentally, but this mental exercise is not possible for everyone and certainly does not do several important things: First, it does not provide a history of the system for later reference. Second, it does not make full use of the facts and observations other personnel may have. Third, it does not help other individuals to acquire the same ability to assemble and correlate facts.

Establishing Intersystem Compatibility.—An occasion may arise when a one-time exchange between two systems is required. A case in point would be one ship requiring a new copy of the operational program from another ship. Operational commitments may prevent a second chance for a tape exchange. The problem is actually one with two parts: (1) provide a good program tape for the second ship, and (2) establish intersystem compatibility for the purpose of this transfer.

The solution, therefore, is also in two parts: (1) write a good copy using a "levels" tape and the best (highest demonstrated degree of compatibility) transport, and (2) generate a "ls" tape on that same transport to accompany it. In this way, if the program tape is found to be incompatible in the second system, a single transport can be readjusted using the "ls" tape as if it were a "skew" tape. Then, the program tape can be read and copied onto a tape mounted on the second system's best transport.

Following this, the readjusted transport (picked because it is currently thought to be the "worst" in the system) would undergo readjustments based on the normal skew tape. These adjustments will, of course, improve its performance and would probably be required shortly anyway. The process from start to end, barring complications other than establishing compatibility, will probably take less than half a working day. Most of the time required would involve adjustments of the one transport. On

*Steps (5) and (6) are only pursued when a tape exchange between two or more systems is regarded as commonplace.

exchanges of this sort, the receiving system has to either provide its own tapes or swap two tapes in exchange. The latter methods requires less time for the two ships to be in contact.

The principles discussed here are pretty much machine independent, though they do not pertain in equal degree to every type of tape transport. In fact, they may even apply to tape certifiers where adjustment procedures were discussed (after all, they also are tape handlers).

TAPE FORMATS AND HEAD ARRANGEMENTS.–Several heads are in contact with a tape surface simultaneously. One is an erase head which is used to clear a tape section of previous data before new data is written on it. It is deenergized during read operations. There may be just one other head on a particular transport. If so, it is a dual function read/write head. That is, it responds to flux variations on a read operation, and generates new flux patterns during a write operation. It always appears after the erase head, or there may be two heads in addition to an erase head. In this case, both are functionally read/write heads, but one is probably exclusively used as a read head and the other exclusively as a write head. The order of heads for this system would be erase-write-read. This permits the tape to be erased, then written on, then checked by the read head in a single write operation. This technique is known as read-after-write and can only be employed by transports having three or more heads. Most three-head transports do a [---, ---, read] during a read operation. However, some use the write head during a read operation too. This permits a [----, read, read] (tell me twice) operation, a [---. checkread, read] operation, or [----, read, checkread] operation. Checkread operations are used as comparisons for the data detected by the read head.

The read and write heads are multitrack heads. The erase head is a single track head that erases the full width of the tape.

PHYSICAL FORMAT OF THE TAPE.– The number of tracks a tape transport has, whether it is using the RZ or NRZ recording technique, whether the supply (or feed) reel is A-wound (oxide side in) or B-wound (oxide side out), the size and shape of the tape hubs, or the width of the tape, all these factors and others, depend upon equipment design and specifications. Here again, certain consistencies emerge. The area on a tape which is required to produce one bit of information per track is usually called a frame, whatever its actual size. Its size is usually measured as the number of bits per track (or frame count) per inch and is called bit (or frame) density.

A frame would consist of all the bits, either ones or zeros, that are parallel across the number of tracks. A group of frames on a tape, which is separated from other groups of frames by unrecorded sections of tape, is referred to as a block (or record). However, since the word "record" takes on a different meaning in software applications, only the term "block" will be employed here. The unrecorded sections between blocks are called interblock gaps (IBGs, or IRGs if "record" terminology is employed). Blocks vary in size, depending upon the number of computer words they contain. IBGs are constant in size, being approximately 3/4" long for most tape equipment. No matter what its tape speed is, a transport must be able to stop, then start again within a single IBG area. It must stabilize at normal tape speeds before encountering the leading edge of the next block. This makes stop-start mechanical adjustments very critical in tape equipment, especially as tape speeds go up.

Read/Write Functions.–A computer word is usually much larger than the number of tracks in a transport. Therefore, tape transport logic separates the computer word into "bytes" and writes each byte as one or more separate frames. It also supplies any parity or redundancy bits requested, and there may be a separate sprocket track for timing purposes. Sprocket tracks when used appear near the center of the tape to reduce the degree of skew error if a problem exists in the transport's adjustment.

Computer words are normally written with the most significant byte first. The order in which computer words are reassembled depends upon whether a read forward or a read reverse function is being used. Write functions only occur while going forward, but read functions for many transports can be selected for either

direction. The problem would then be for the computer program to correct the order of bytes and word sequences once the data is read into the computer.

All the words contained in one block on tape are usually accomplished in one write operation. Each write operation normally produces a separate block. Most techniques for writing a block of data involve a computer output buffer operation. Most techniques for reading back the data involve computer input buffer operations. Computer input operations may read all or just part of the data contained in one tape block.

Tape Labels.—Two physical labels are affixed to either end of the tape. One is called a beginning of tape (BOT) label; the other is the end of tape (EOT) label. Most transports use highly reflective glue-backed labels which are attached to prescribed areas of the tape, while the RD-243 Magnetic Tape Unit (the tape transport covered later in this chapter) uses a transparent tape insertion. The standard way of "sensing" these labels is a photoelectric arrangement where light is reflected from (or passed through) the label and used to trigger an output from a photoelectric cell. Many transports may also use a special one-frame block of data on the tape which is detected by the logic circuits for the transport as a special condition called a tape mark or file mark. The transport can either read or write this special mark on the tape, and will write the mark when instructed to do so with a function word, or generate a status condition automatically when reading the file mark.

Since they are blocks of data, FMs (file marks) are separated from adjacent data blocks by IBGs. Programmed applications usually involve the use of FMs to group data blocks into "files" on the tape. The end of the last file is commonly identified by two consecutive FMs. This makes it unnecessary to erase any data left on the tape beyond this point, a step that would be necessary if no software limit were set on the tape to prevent the current program from accidentally accessing data that may still exist from previous tape applications. The use and recognition of file marks is not designed into the RD-243 logic.

SOFTWARE TERMINOLOGY.—Special data blocks are used in some systems to provide information on either the tape (called a tape label) or on a file (called a file label). Computer subroutines write or respond to these data blocks as special conditions in much the same manner that transport logic looked at file marks.

Records (as data blocks were once known) are now considered to be the sum amount of information known on a particular subject. Records may require one or more blocks of data when recorded on tape. In thinking of an office file, a data block corresponds to a sheet of paper. A record corresponds to one or more sheets of paper stapled together (a letter would be an example of a record). A file corresponds to a manila folder containing one or more records. A file drawer corresponds to the physical limits of storage one reel of tape possesses.

These correlations are nearly universal because most current forms of data storage are developed directly from the office file concept. The only significant changes are: much faster and more reliable processing, full use of automated equipment, and tremendous increases in data storage limits at all levels (block, record, file, and tape). Even tape storage can be compacted to about the scale of library stacks, resulting in tremendous data storage potential in a limited physical area.

COMMONLY USED TERMS WHEN GROUPING BINARY NUMBERS.—There are six terms that are commonly used to describe the manner in which binary data is usually grouped. Some of these groupings are physical, meaning that equipment handling binary data have been designed to work with so many bits of data at one time. Other groupings are merely figurative, meaning that the binary information is thought of, or treated, as if it belonged to a group by personnel working with it or programs designed to handle it. An example of a physical grouping would be a computer word. A computer is designed to handle so many bits of information as a single unit, called a word, and the size of the word is determined by the computer under discussion. The CP-789 computer uses an 18-bit word, and also has a 36-bit double-word capability. The CP-642B

computer has a 30-bit word, with 15-bit half-word capability. An example of a figurative grouping of data is the method of mentally grouping binary bits by threes, and "reading" the result as if it were an octal number.

The six terms commonly used to describe binary groups are: (1) bit, (2) word, (3) frame, (4) byte or date byte, (5) codes, and (6) fields or data fields. The first three are physical terms: Bit refers to a single physical binary position, word refers to a physical dimension of the computer to handle a composite unit of binary bits, and frame is a dimension of tape equipment to read or write several bits simultaneously using separate channels or "tracks" on the tape. The fourth term, byte, can refer to either a physical or figurative grouping of binary data. An octal byte would be three bits used together. A hexadecimal byte would be four bits used together. A byte could also represent the number of bits that can be stored in a frame of tape, or be subunits of a computer word when it is uniformly broken up into smaller units by executing various logical instructions. A byte can also consist of "n" number of bits, grouped together to represent 2^n unique numerical values, called "codes." It would require only 26 unique codes to represent the letters of the alphabet, A-Z, another ten codes to represent the numbers 0-9, and whatever number of additional codes would be necessary to represent punctuation marks, arithmetic operations (+, -, x, ÷, =), and any other specialized symbology desired ($, %, &, #, @). A byte that represents data contained in 2^n bits is usually referred to as a "data byte" to prevent any accidental confusion with a byte description representing a physical dimension, if both occur in the same literature.

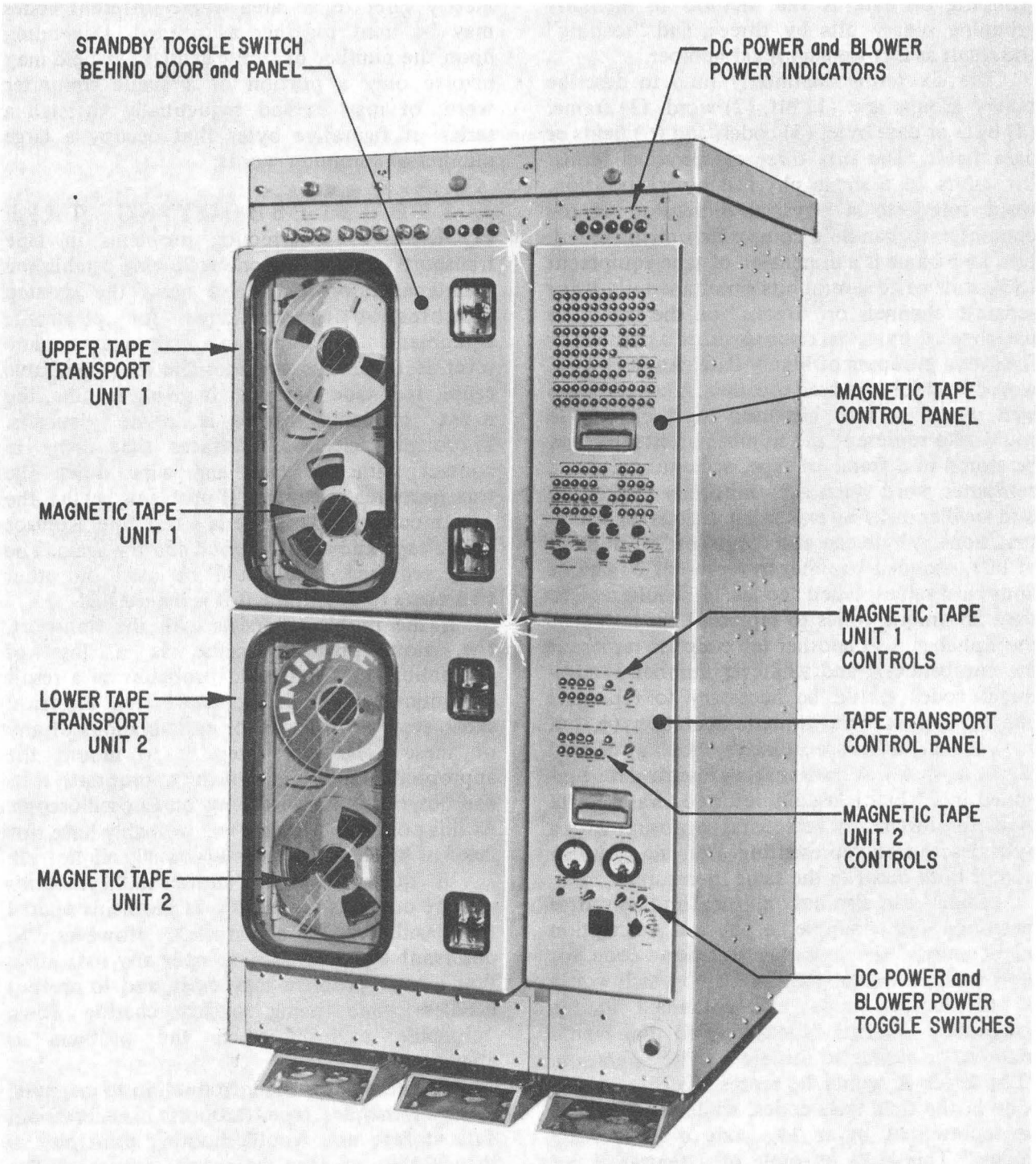
"Code" can also have physical and figurative meanings. For example, a physical description might state, "the external function code for performing a write operation . . .," which would be the unique code bits contained in the computer's external function word that would cause some device to initiate a write operation. "The letter A would be represented by an 06_8 code in the field data codes, while it could also be represented by a 24_8 code if using XS-3 Codes." This is an example of a figurative use for the word code. The terms "field" or "data field" refer to groups of codes that have some connection with each other. Sometimes the codes within a field may be modified or replaced, in which case the term "field" may merely refer to an area where different codes may be used together as needed. Depending upon the number of codes involved, a field may involve only a portion of a single computer word, or may extend sequentially through a series of figurative bytes that occupy a large number of computer words.

TROUBLESHOOTING TAPE EQUIPMENT.– Correcting problems in tape transports should be done following established maintenance practices and using the six-step troubleshooting technique for electronic equipment. An important maintenance time saver is to always consider the most probable cause. If a tape transport is giving trouble, the most probable cause is oxide deposits. Thoroughly clean all surfaces that come in contact with the tape and wipe down the transport area in general. If problems persist, the next most probable cause is a bad tape. Replace with a tape known to be good and try again. The suspected bad tape could be used on other transports to determine if it is indeed bad.

If the problem persists with the transport, the most probable cause is a loss of compatibility. This would probably be a result of a minor change in stop-start time, electrical skew, read/write levels, or combinations of any of these. The next step is to mount the appropriate tapes and run the appropriate tests and observe signal waveforms on an oscilloscope. At this point the problem will probably have surfaced or will have been systematically eliminated.

In equipment of this nature, logic problems do not occur as frequently as problems related to cleanliness or adjustment. However, an observant eye is needed to spot any indication that a logic problem may exist, and to prevent needless time being wasted chasing down "probable causes" when the problem is elsewhere.

This completes the introduction to magnetic storage principles, tape transports in general, and data storage and troubleshooting principles as they pertain to tape transports in general. The next section will go into the particulars of one specific type of tape transport, the RD-243 Magnetic Tape Unit.



124.203

Figure 5-2.—RD-243/USQ-20(V) Magnetic Tape Unit.

RD-243/USQ-20(V) MAGNETIC TAPE UNIT

The RD-243 Magnetic Tape Unit shown in figure 5-2 is a large capacity, medium speed auxiliary storage device used primarily for program loading. Real-time data can also be extracted from the system and retained by the RD-243 for later processing and interpretation.

The RD-243 is a return-to-zero dual transport, each having one erase and one read/write head (no read-after-write capability). It uses 1/2″ width tape on UNIVAC hubs with "B" WIND (oxide side out). On this tape it will format frames consisting of six data tracks, a sprocket (timing) track, and an eighth track used for an odd parity bit (parity mode) or as a second sprocket track (redundant mode). The two transports function independently of each other. Extracted data from the system would not be stored on the same tape with the programs. The program tape normally stays mounted while the system is in use to facilitate a manual reload if a program fault occurs.

One or two computers can communicate with the RD-243, as illustrated in figure 5-1. This capability is a logic function known as duplex control. Only one of the computers can be in control of or communicate with the RD-243 at any given time. Data transfers between the computer and the magnetic tape unit (MTU) use 30 parallel bits.

Data is recorded (written) onto the tape only when tape motion is forward. Data may be read in either forward or reverse tape direction. Read and write operations have a tape velocity of 112.5 inches per second; rewind operations (high speed reverse motion) move tape at 225 inches per second.

FRONT PANEL CONTROLS

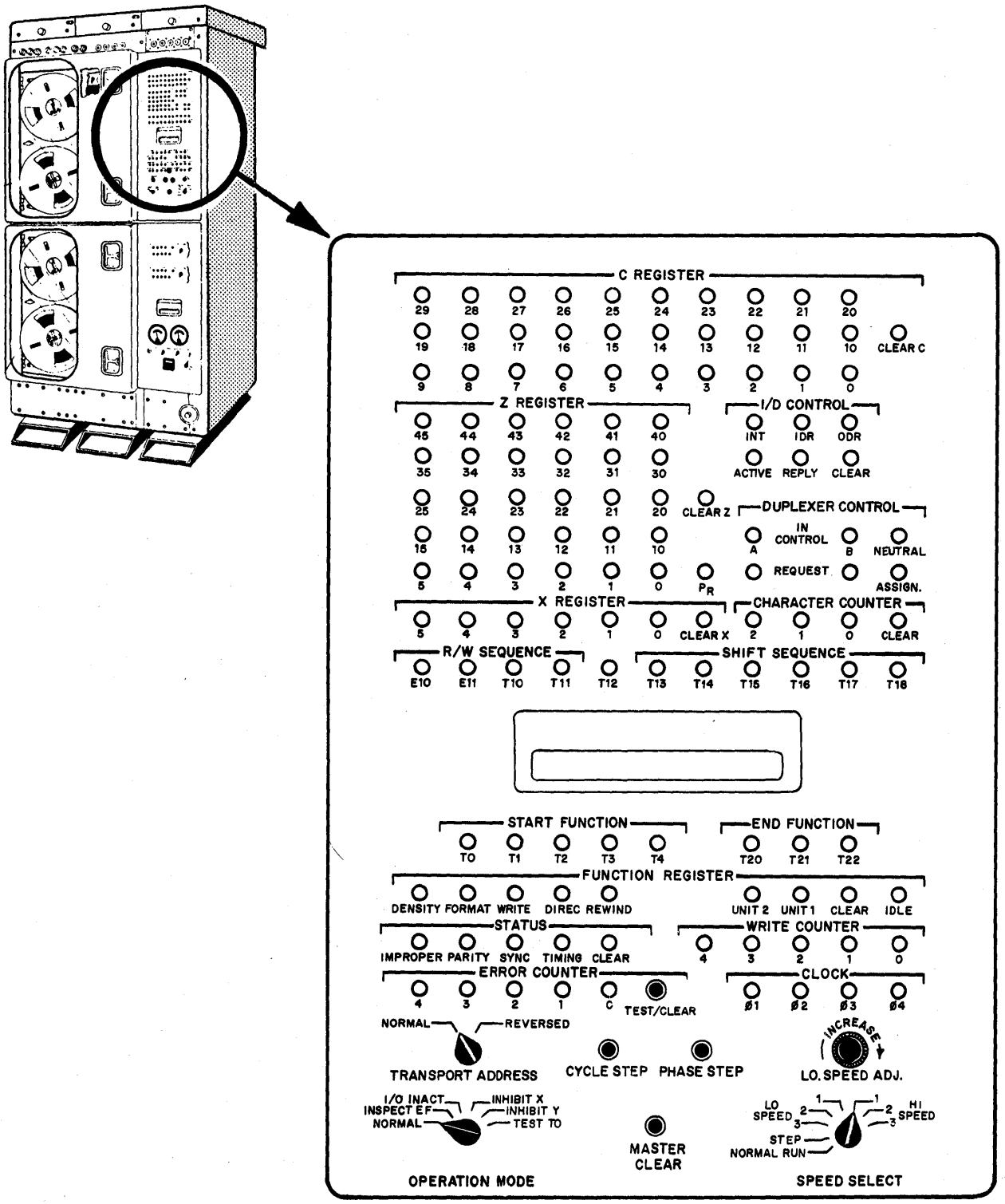
On the front of the MTU are two control panels, magnetic tape control panel (fig. 5-3) and tape transport control panel (fig. 5-4). The magnetic tape control panel is used to control the overall operation of the MTU. The OPERATION MODE switch is used in the Normal position for operation. The other positions of the switch are used for testing the MTU. The SPEED SELECT switch (and LO SPEED ADJ) control the master clock rate. Normal Run is the operating position of this switch; the other positions are used for testing. The TRANSPORT ADDRESS switch determines which tape transport is designated 1 or 2. In the normal position, the upper tape transport is 1 and the lower transport is 2. In the reversed position, the transport numbers are reversed with number 2 then being considered on top, number 1 on the bottom. These transport numbers must be used when programming the MTU. The MASTER CLEAR pushbutton is used to clear all registers and control circuits.

The CYCLE STEP and PHASE STEP pushbuttons are used when the SPEED SELECT switch is in the step position. Pushing the CYCLE STEP button will cause the clock to generate one complete cycle running from Ø1 through Ø4. Pushing the PHASE STEP button will cause generation of a single sequential clock phase (Ø1, Ø2, Ø3, or Ø4).

Depressing, then releasing the TEST/CLEAR pushbutton will test the error counter, then clear the ERROR COUNTER indicators. The STATUS indicators are used to indicate the condition of the MTU. TIMING, SYNC, and PARITY are used to indicate errors occurring with tape motion. The IMPROPER indicator is lighted when the program attempts to have the tape transport execute an illegal operation. Improper conditions exist when any of the following actions are attempted:

(1) Neither transport is selected
(2) Both transports are selected
(3) The selected transport cannot perform the indicated function because:
  (a) tape at EOT (for move FWD instruction)
  (b) tape at BOT (for move REV* instruction)
  (c) master tape mounted (file protect ring inserted in supply reel rim) (for WRITE instruction)
  (d) tape transport power off (any instruction)
  (e) not in AUTO mode (any instruction)

*REWIND is used to initialize a transport by placing it at BOT. For this reason the logic is inhibited from detecting an improper condition if the tape is already situated there. No tape motion would occur beyond tape labels in any case.



124.432

Figure 5-3.—Magnetic tape control panel.

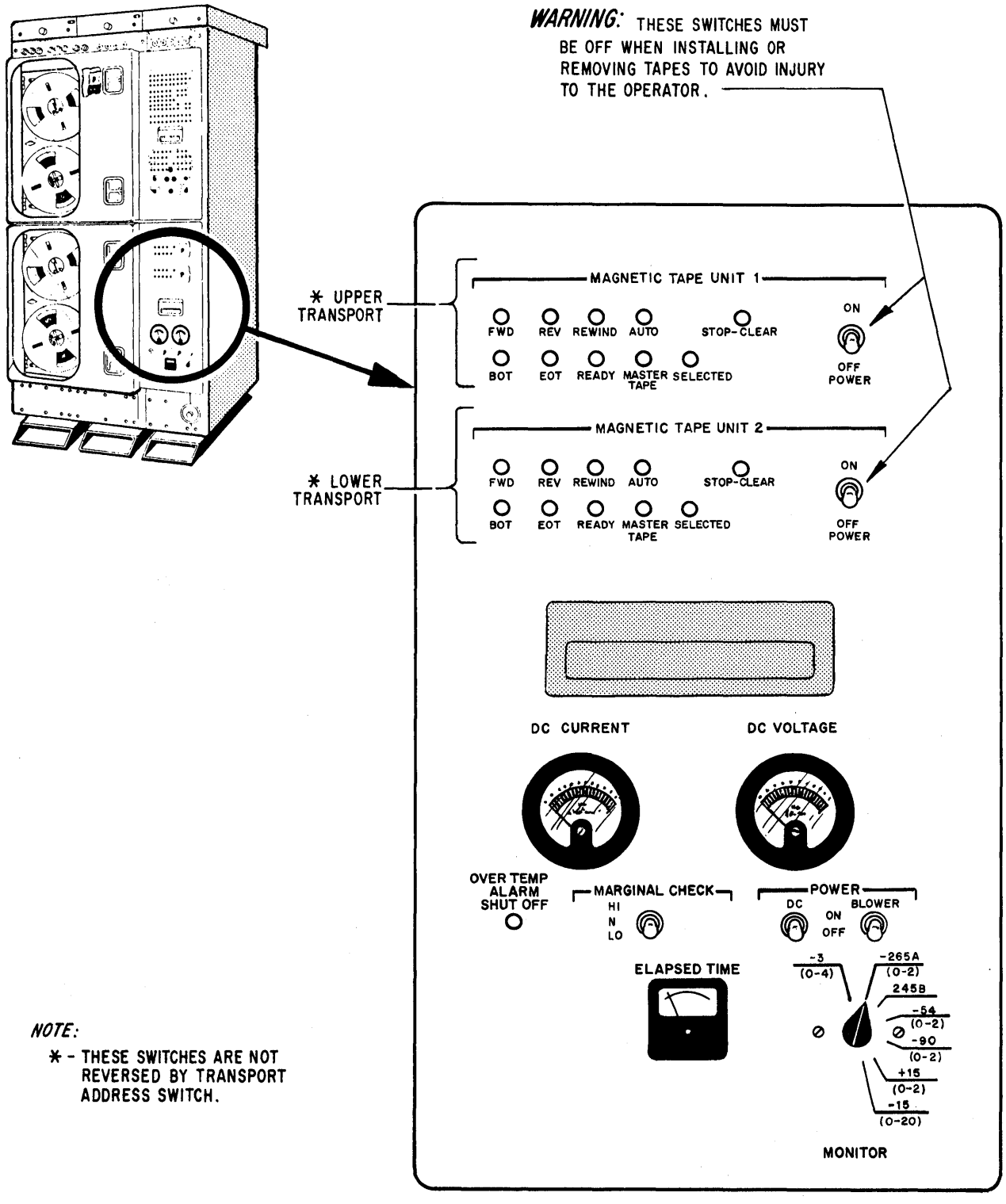
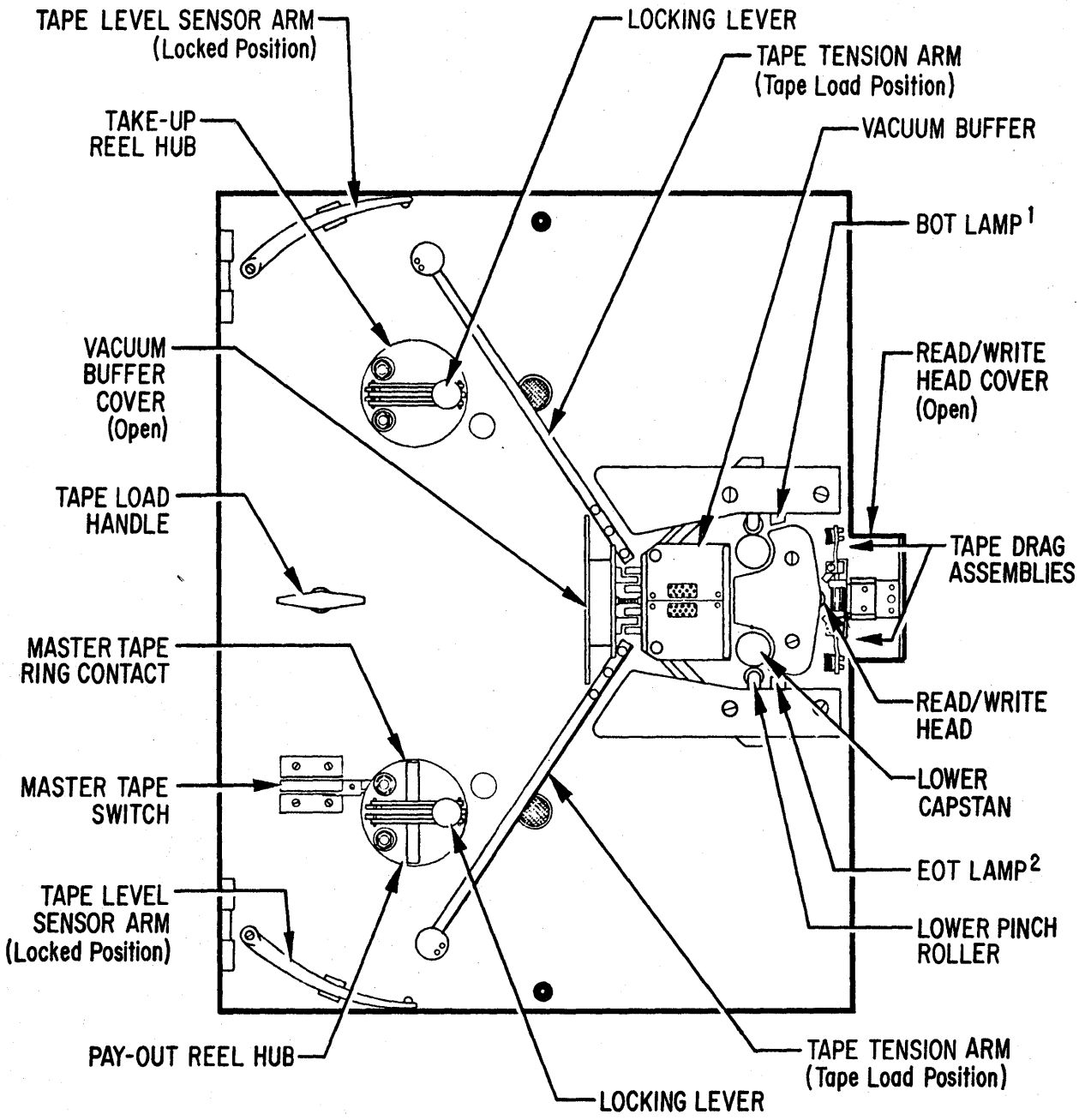


Figure 5-4.–Tape transport control panel.



Note:

1. SENSES CLEAR LEADER AT BEGINING OF TAPE.
2. SENSES CLEAR LEADER AT END OF TAPE.

124.434

Figure 5-5.—Tape transport with reels removed, covers open and tape tension arms in load position.

The FUNCTION REGISTER indicates which tape transport is performing what function. The START FUNCTION and END FUNCTION indicators display information pertaining to the control status of the MTU. The other indicators are for the registers and timing chains concerned with data transfer to and from the MTU.

The tape transport control panel (fig. 5-4) controls tape motion on a selected tape transport. There are four power switches on this panel. The two on the top control the power to the upper and lower tape transports. The transport switch must be in the OFF position when a tape is being mounted or removed to prevent possible damage to tape and/or injury to personnel. The DC CURRENT and DC VOLTAGE meters are used with the MONITOR switch to check the power supplies of the MTU. These meters only give approximate values and should not be used for power supply alignment. The ELAPSED TIME meter displays the time power has been applied to the MTU.

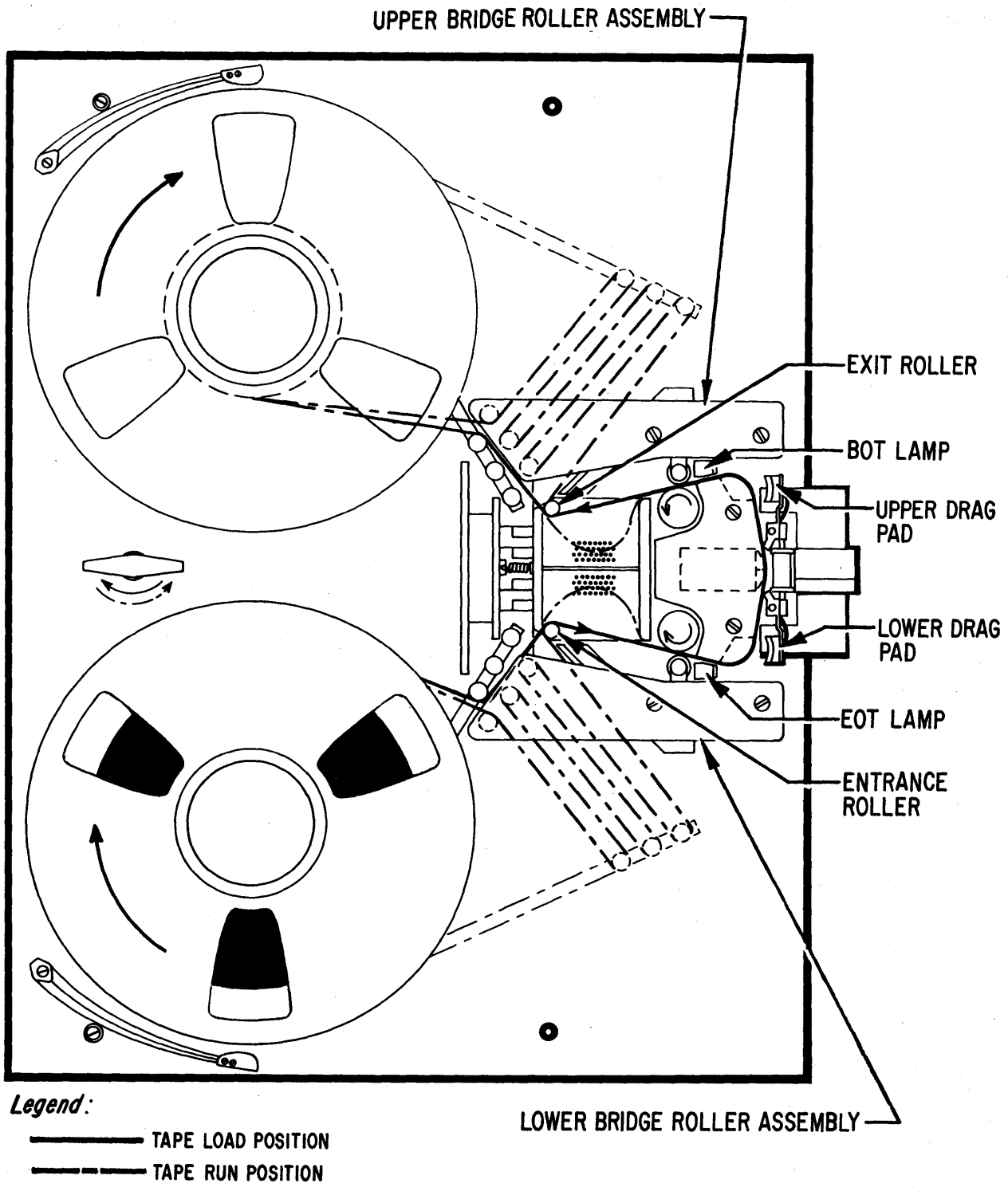
The pushbutton-indicators for the top and bottom units perform identical functions. The STOP/CLEAR button stops tape motion and removes the tape transport from the automatic mode, which puts it in the manual mode. The FWD, REV and REWIND buttons cause tape motion in the desired direction. Depressing AUTO places the tape transport in the automatic mode. It then becomes available for computer reference and is operational. The SELECTED indicator indicates that the tape transport is being referenced. The MASTER TAPE indicator is illuminated when a magnetic tape reel with a master tape ring is mounted on the lower tape mount. A master tape ring is a small flat ring that is inserted in the rim of a tape reel to prevent writing on the tape, and limits its use to movement and read operations. The ring depresses a microswitch beside the lower tape mount and disables the write function for that transport. Most tape transports, other than the RD-243, require that the ring be inserted in the groove on the back side of the inner reel rim in order to perform a write, rather than to inhibit it. This change occurred in newer transport systems because the "ring-in write lockout" technique might result in inadvertent writes on protected tapes if the ring accidentally fell out during handling without immediate detection. The new approach required that the ring be inserted to enable a write operation, and a ring that accidentally was missing caused no serious consequences. Thus, a ring that is called a WRITE LOCKOUT RING for transports similar to the RD-243, would more correctly be referred to as a WRITE RING for systems using the later technique.

When illuminated, the READY light indicates that the transport is operational. The EOT (End of Tape) and BOT (Beginning of Tape) indicators are illuminated when the tape is at these points and the clear sensor area on the tape is over the appropriate sensor lamp.

Tape Transport Mechanics

Refer to figures 5-5, 5-6, and 5-7. The mechanical system that drives the tape in the RD-243 MTU will be briefly described.

The tape reels provide the necessary tape storage for the system. The hubs rotate in either direction, to feed or take up the tape as needed. The tension arms control the speed and direction of the respective hub rotations. As shown, the tension arms are centered in their range of movement. If a capstan/pinch roller assembly pulls the tape away from the tension arm, the arms draws in and causes the hub to rotate to provide more tape to the tension arm. At the same time, the excess tape is being added to the opposing tension arm, causing it to move out. The outward movement causes the hub on that side to rotate and take up the excess tape. The farther the tension arms move from their centered positions, the faster the respective hub rotates until a balance is achieved between tape being pulled away and tape being added to the tension arm. The tension arms are, therefore, a coarse tape buffer system that absorb and release tape as necessary between the reel/hubs and the capstan/pinch roller assemblies. If the tape should bind or break, the effect would be to cause the tension arms to do one of three things: (1) be stabilized near the center range, (2) be drawn to the innermost position, or (3) be extended to the outermost position. The most likely result is that the arms will be thrown to their outermost positions. Because of this, limit switches at the extreme inner and outer range limits of tension arm movement will



49.362

Figure 5-6.—Tape threading diagram.

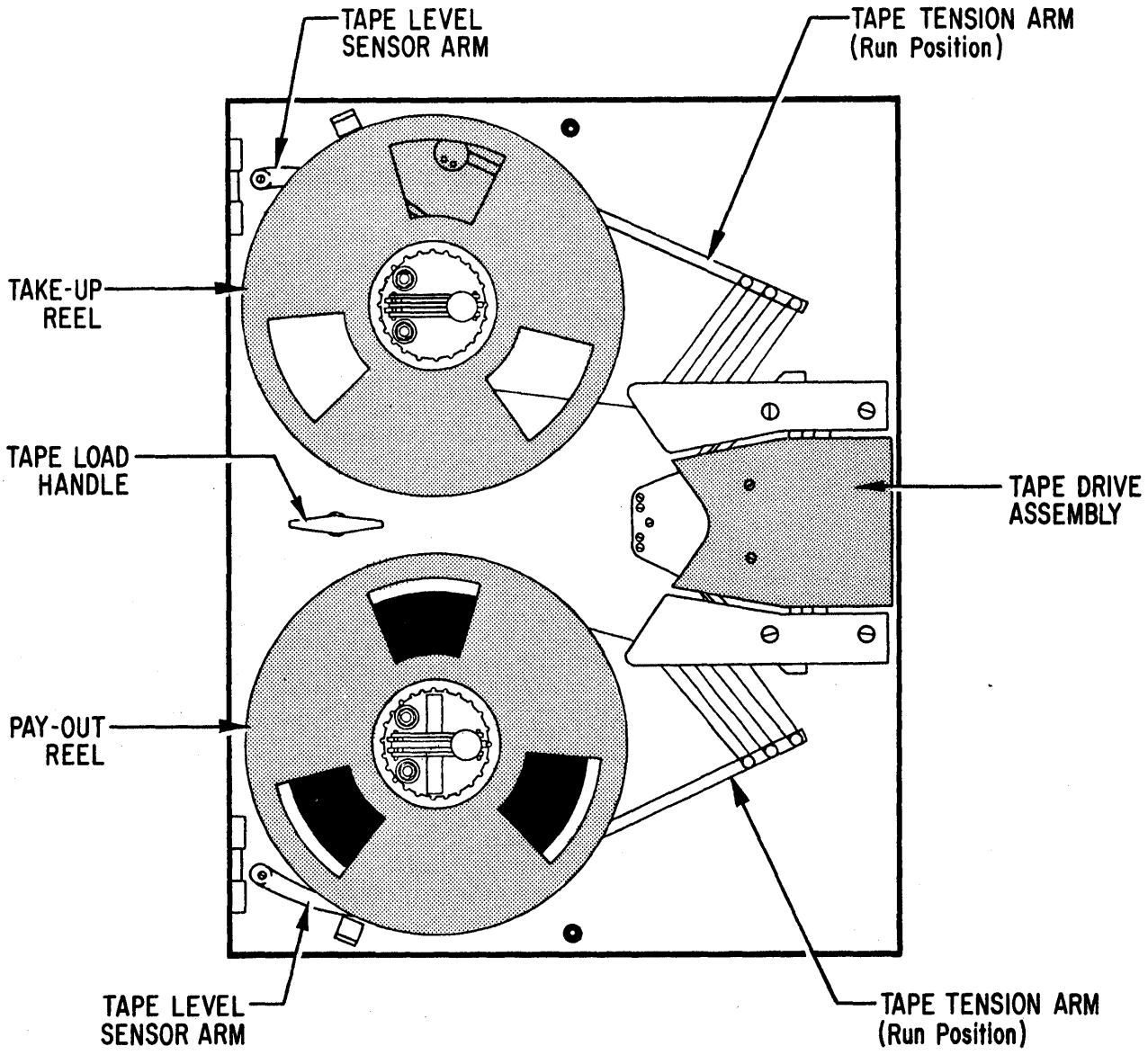


Figure 5-7.—Tape transport, ready condition.

automatically shut the transport down, and automatic brakes in the hubs will prevent further tape movement until the situation is corrected.

An additional buffering system appears between the tension arms and the capstan/pinch roller stations. A small vacuum chamber maintains a small loop of tape within it to further smooth out the effects of abrupt changes in the tape movement. The vacuum chambers are referred to as the fine buffering system.

All tape movement is initiated by the capstan/pinch roller assemblies. Tape is pulled across the heads by the capstan/pinch roller assembly mounted on the receiving side. To change the direction of the tape movement, it is

only necessary to energize the pinch roller assembly on the opposing side, and cause the tape to be pulled across the head in the opposite direction. The capstan/pinch roller assemblies are referred to as the primary drive mechanics.

The capstans provide a constant tape speed, the pinch roller assemblies provide capstan/tape contact, the vacuum chambers act as a fine buffer system to isolate the tension arm adjustments from the primary drive mechanics, and the tension arms further isolate changes in hub movement from affecting the primary drive mechanics. The drag pads provide a constant braking force to the tape and precisely stop the tape in a specified distance once the activated capstan/pinch roller assembly is released.

As soon as power is removed from a transport, a brake is applied to both hubs. This is to prevent accidental tape spillage if the tape breaks. A break in the tape would free the tension arms, which would abruptly fly to their outermost positions and activate an emergency power off switch. This would cause the hubs to stop rotating immediately. Whenever power is being supplied to the transport, the hubs are positioned by servo mechanics. Attempting to turn the hubs or reels by hand will change the amount of tape maintained in the corresponding tension arm. This will produce a tension arm movement and result in an error voltage that will cause the hub to rotate to correct the condition if possible. Attempting to turn a reel or hub either by hand or by manipulating the tension arm with transport power on may cause tape breakage or even bodily injury due to a whiplash response. To cause tape movement with the power on, use the manual FWD, REV, or RWD controls provided. When power is off, the tape can be moved by manually turning the hubs, although some resistance will be felt from the hub brakes. To prevent strain on the tape, rotate each hub simultaneously using both hands.

The sensor arms ride (follow) the tape down into the reels and detect when approximately 1/4 of the tape remains (about 100 feet). In some MTUs, the take-up reel sensor arm slows high speed forward movement and generates a low tape (NEAR EOT) status condition, while the supply reel sensor arm slows high speed reverse (RWD) movement and generates a high tape (NEAR BOT) status condition. The RD-243 MTU does not report high or low tape status, and only uses the take-up reel arm to slow its only high speed instruction, which is RWD. The supply reel sensor arm is not used in the RD-243 application of this transport, and the sensor arm may be taped back against its stop for convenience with no adverse effect on equipment performance.

MOUNT A TAPE

The parts involved in tape mounting are referred to by the nomenclature shown in figures 5-5, 5-6, and 5-7.

(1) Turn tape transport power to OFF. Place the tape level sensor arms against the stops. The arms should lock in this position. These arms are used to prevent a whiplash effect on the tape when it is stopped, by slowing down the tape when there is only a 1/4-inch thickness of tape left on the reel (approximately 100 feet of tape left).

(2) Raise the locking lever on the upper hub to an approximately vertical position by grasping the knob in the center of the hub and pulling straight out.

(3) Place an empty tape reel on the take-up (upper) hub. Note that a notch on the inner diameter of the reel hole will be engaged by the projection on the lower front end of the locking lever when the hub is locked.

(4) Lock the reel to the hub by returning the locking lever to its original horizontal position.

(5) Repeat step 2 with the lower hub.

(6) Mount the program tape on the lower (payout) hub. Note that the free end of the tape hangs down from the right side of the reel.

(7) Lock the reel to the hub as in step 4. Ensure that the projection on the lower front of the locking lever is engaged properly with the notch on the reel.

(8) Rotate the tape load handle clockwise. Ensure that the tape tension arms are toward the center of the tape transport.

(9) Pull the tape upward from the left side of the payout reel to the left side of the take-up reel, press the free end of the tape against the inner hub area of the take-up reel. A finger may be used if cutouts in the reel side allow access,

or the eraser end of a pencil can sometimes hold the tape to the inner hub surface. A very common approach is to allow the free tape end to dangle over the inner hub curvature and to rotate the hub rapidly, which will cause the tape to adhere to the hub portion of the reel. Gradually add more tape while rotating the reel until the overlaps hold the tape firmly. Do not slip the free end of the tape into the slot in the reel. Do not secure the tape in any manner.

(10) Holding the tape against the reel's inner hub, turn both reels by hand and wind the tape until the free end is held in place by the tape overlapping itself. Then rotate both reels by hand clockwise to wind on three more turns of tape. Threading the tape in this manner does have one drawback: The tape can be damaged if allowed to rub against the tape load handle. This is not a critical problem if care is taken and only the tape leader is involved. The leader is that portion of the tape that appears before the BOT label, or after the EOT label. The labels are transparent tape inserts for the RD-243 MTU. To prevent the tape from rubbing against the tape load handle, some of the tape slack can be looped over the lower roller on the lower tension arm, and left there while tape is wound manually between the reels.

(11) Open the vacuum buffer cover and the read/write head cover.

(12) Rotate the payout reel clockwise to obtain a loop of about two feet in the tape.

(13) Beginning at the top, near the takeup reel, lay the tape into the tape load position shown in figure 5-6.

(14) Ensure that the tape lies in the grooves between the tension arm rollers and the stationary rollers which are part of the bridge roller assemblies. Ensure that the tape is in the back grooves above and below the tape head and is flush against the tape read/write head. Ensure that the tape passes under the BOT lamp and above the EOT lamp; it may easily get threaded wrong at these positions, especially at the EOT lamp, because of slack.

(15) Rotate the payout reel counterclockwise to take up any slack in the tape.

(16) Close the vacuum buffer cover and the read/write head cover.

(17) Rotate the tape load handle 180° counterclockwise.

(18) Manually rotate the take-up reel counterclockwise until its tape tension arm is in the run position shown in figure 5-7.

(19) Manually rotate the payout reel clockwise until its tape tension arm is in the run position shown in figure 5-7.

(20) Look for the transparent (clear) part of the tape leader. Rotate the reels as necessary to position the transparent part of the tape leader [this is the BOT (Beginning-of-Tape) indication] onto the take-up reel.

(21) Release the tape level sensors from lock position.

(22) Place MAGNETIC TAPE UNIT 1 (or UNIT 2) POWER toggle switch to ON (fig. 5-4). At this point the sounds of electric motors and of air suction should become apparent. After a momentary pause, the tension arms and hubs should jump into motion to compensate if the tension arms are not in their midrange arc correctly. This brief activity should cease, and the position of the tape in the transport should be briefly scanned for apparent problems. Opening the vacuum chamber cover should cause slight jerking in both tension arms as the tape loop is lost in both vacuum buffer chambers. The same jerky action of both tension arms will show that a tape loop reformed in the respective vacuum buffer chamber when the cover is closed again. Once this initial inspection is complete, the transport is ready to be tested manually. Until a motion command is involved, the only activity of the transport that should be apparent is the continued suction of air, and the nonstop rotation of the capstans. (The vacuum pump and capstan motor are always energized when power is applied to the transport.)

(23) Depress MAGNETIC TAPE UNIT 1 (or UNIT 2) FWD indicator button. This engages the forward (upper) pinch roller. Allow tape to run forward for 10 to 20 seconds, examining it as it runs to ensure that tape is correctly seated in the grooves around the tension arms, rollers, and read/write head.

(24) Depress STOP-CLEAR indicator button to stop the tape. Make any needed corrections in threading after turning power OFF. Then restore power to the transport and repeat step (23).

(25) Depress the appropriate REWIND indicator button to rewind tape. This engages both the reverse pinch roller and the high speed

winding in the capstan motor. REWIND motion should be twice as fast as FWD motion, unless just a few tape wraps are on the take-up (upper) reel. Tape will stop when clear leader passes under BOT lamp. Make any needed corrections in threading after turning power OFF. Repeat steps 23, 24, and 25 until tape runs smoothly.

(26) Depress MASTER CLEAR button once.

(27) Depress MAGNETIC TAPE UNIT 1 (or UNIT 2) AUTO indicator button. Observe that indicator is illuminated. If indicator is illuminated, MAGNETIC TAPE UNIT 1 (or 2) is ready for automatic operation by the computer.

TAPE REMOVAL

To remove tape from the transport, complete the following steps:

(1) Stop tape movement and initiate the manual mode for the appropriate transport by pressing its STOP-CLEAR button. (NOTE: Though the manual controls for the transports are marked for MTU 1 and MTU 2 on the tape transport control panel, these controls are not affected by the normal-reverse switch on the MTC panel. The upper switches, marked for MTU 1, always correspond to the upper transport, even when it has been readdressed as MTU 2 by use of the reverse position on the normal-reverse switch. The same holds true for the lower manual controls with respect to the lower transport.) Initiating the manual mode means that the transport can still respond to commands generated by the manual pushbuttons and switches on the tape transport control panel, but not to commands from the magnetic tape control panel or from the computer. The AUTO light for the appropriate transport will be extinguished.

Unlike alternate ways of stopping tape movement (power off, MASTER CLEAR, or forcing an End of Function sequence), the STOP-CLEAR button does not run the risk of tape damage (as might an abrupt power off), affect the alternate transport (as would a MASTER CLEAR), or involve current operations (as would forcing an End of Function sequence). It is the ONLY method that should be employed to effect manual control over one transport while the other transport is to be left accessible by the computer. Tape movement should stop immediately, at which point depress the manual REWIND button. Wait until the tape's rewind motion stops.

(2) Set the MAGNETIC TAPE UNIT 1 (or 2) POWER toggle switch to OFF. Move the sensor arms back against their stops so that they are free of the reel rims.

(3) Rotate tape load handle 180° clockwise. (Tape tension arms move toward center at this time, leaving loops of slack sticking out.)

(4) Rotate take-up reel clockwise to remove slack at upper tape tension arm.

(5) Rotate payout reel counterclockwise to remove slack at lower tape tension arm.

(6) Open vacuum buffer cover and read/write head.

(7) Gently pull tape away from and free of read/write head, vacuum buffer, entrance and exit rollers, and tape tension arms. Allow the freed tape to hang in a slack loop.

(8) Rotate the payout reel counterclockwise to take up the slack loop. Make sure that the tape will not drag against the tape load handle (see one method for preventing this in figure 5-6, view A).

(9) Manually rotating both reels counterclockwise, rewind the remainder of the tape onto the payout reel. A recommended method for doing this is to turn both reels by hand at the same time, maintaining even tension on the tape so that a smooth motion occurs (the tips of the fingers will provide sufficient friction to turn the reels if they are pressed firmly against the side of the reel. A small circular indentation in the reel plastic can be used for a pivot point.)

(10) Lift the hub locking lever.

(11) Remove the reel of tape. Replace reel in can and store in accordance with ship's procedure.

OPERATIONAL CHARACTERISTICS

The MTU is placed in an operational condition by an operator who mounts the tapes, turns on the power and sets up the normal operating mode. After these manual operations,

the MTU may be controlled by the program. Generally, all programmed use of the MTU must conform to a standard reference sequence—obtain control of the MTU, perform the desired functions and release control of the MTU.

All programmed commands from a computer to the MTU are sent in a 30-bit EXTERNAL FUNCTION word (fig. 5-8). The lower three bits are used by the duplexer section of the MTU to establish or release control of the MTU. All the other bits are used by the tape transport control section to determine the tape transport to be used, the density of storage (number of bits per inch), the type of format (NTDS or Parity) and the operation to be performed. The MTU logic has priority circuits that permit one designated operation to have preference over another. For instance, duplex functions override anything else designated, Master Clear overrides any of the motion read or write instructions, and selecting both transports simultaneously generates an improper condition that overrides either transport being selected. In addition, request control overrides release local, while release local and release remote, or release remote and request control, can be executed simultaneously. The latter is the normal procedure for one computer to "demand" control from the other. Only the function determined to have precedence by the logic will be performed.

An interrupt is sent to the computer to indicate a STATUS word is on the lines after

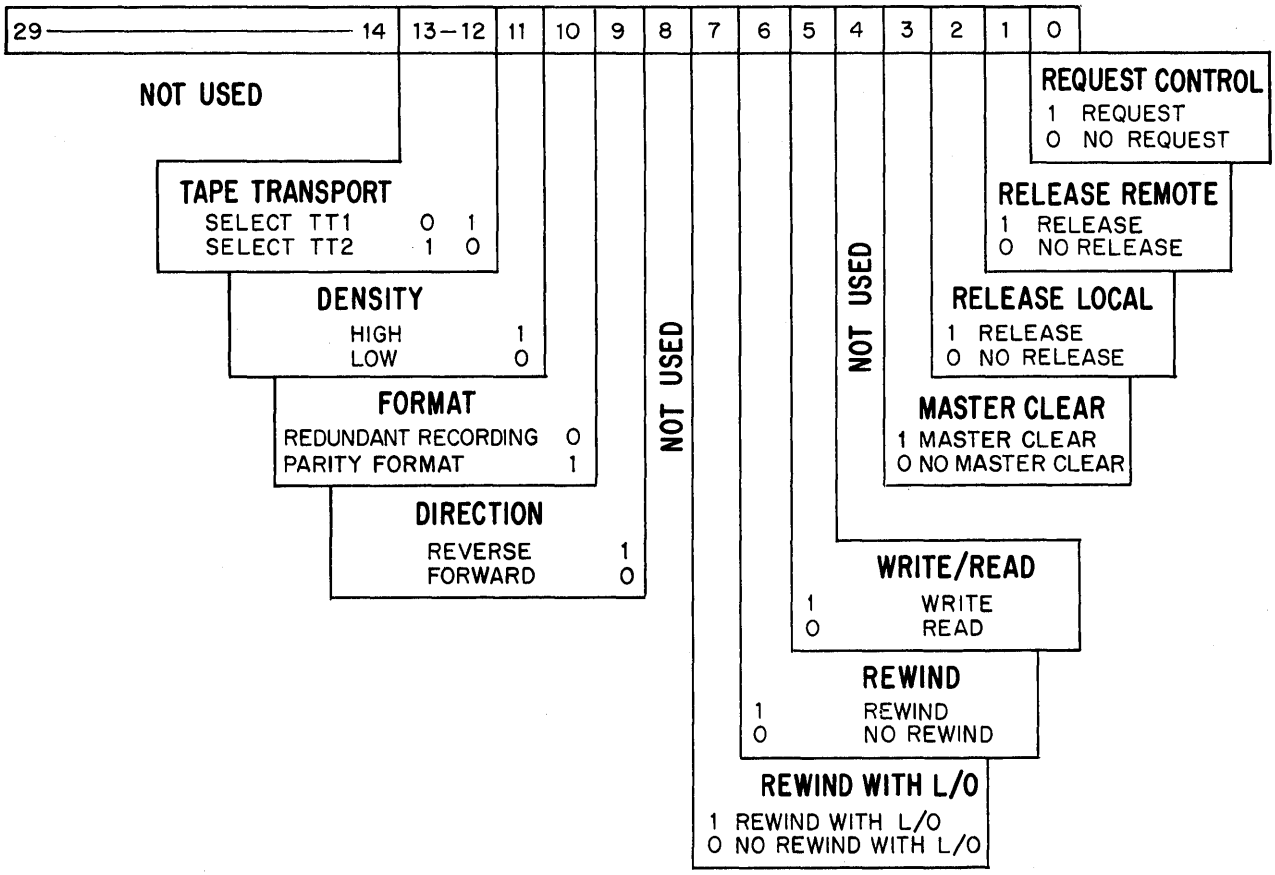


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Figure 5-8.—External Function word format.

each operation, except Master Clear, Release Remote, or Release Local. The status word informs the computer of any normal and/or abnormal conditions that may have occurred following the previous operation. With two exceptions, the status word will always follow the completion of the previous operation. The first exception is the detection of an improper condition, in which case the previous operation is simply aborted. The second exception would be for a rewind operation, in which case the status word interrupt occurs immediately after the rewind motion is initiated, instead of being delayed until the tape reaches BOT and stops. The bit structure of the Status word enables the computer to determine if the previous operation was successfully completed and if the computer is in control of the MTU. The Status word format is shown in figure 5-9. The program must check that the interrupt from the previous operation has been received before a second External Function is sent.

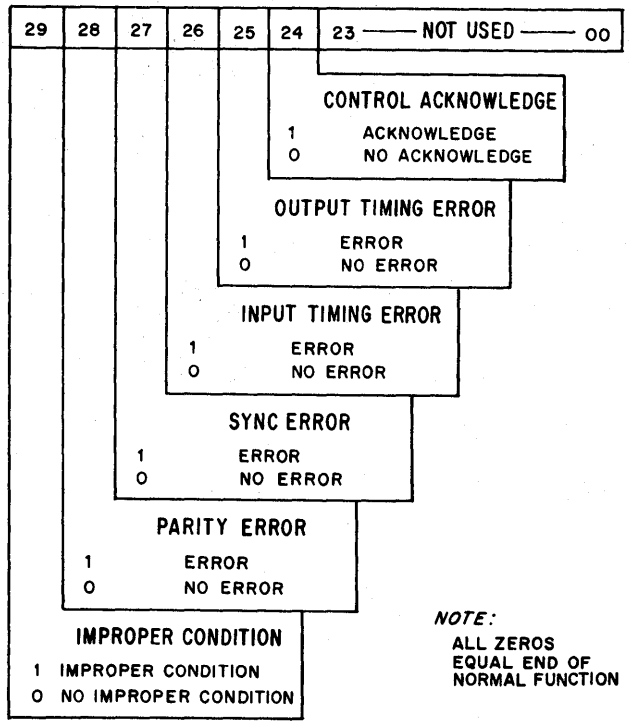

Figure 5-9.—Status word format.

Write Procedures

The controlling computer must always execute a Write function in the forward direction and in the following sequence:

(1) Initiate an Output Buffer on proper output channel (the size of the buffer will determine the length of block to be written).

(2) Send an external function word with the Write and other pertinent bits selected.

(3) Receive and process the status word interrupt.

Read Procedures

The Read function requires the following sequence of the events:

(1) Initiate an Input Buffer on the proper input channel (size of the buffer area should be large enough to cover the length of block to be read and preferably be the exact size of the data block).

(2) Send an external function word with the Read and other pertinent bits selected.

(3) Receive and process the status word interrupt.

In the Write and Read procedures, step 2 need not immediately follow step 1 but may occur at any time thereafter. The important point to remember is that the buffer (input or output) must be initiated prior to the external function (Read or Write) being sent. The reason for this is that if the MTU is prepared to write or read data before the computer has successfully initiated a buffer, an output timing error or input timing error will occur. By initiating a buffer first, these timing problems should not occur.

Tape Formats

Figure 5-10a shows approximately how a tape section would appear if it were dipped into a container of magnetic film developer and then exposed to air, allowing the fluid to evaporate. The tiny metal particles held in suspension by the fluid are responsive to magnetic lines of force and would align themselves according to

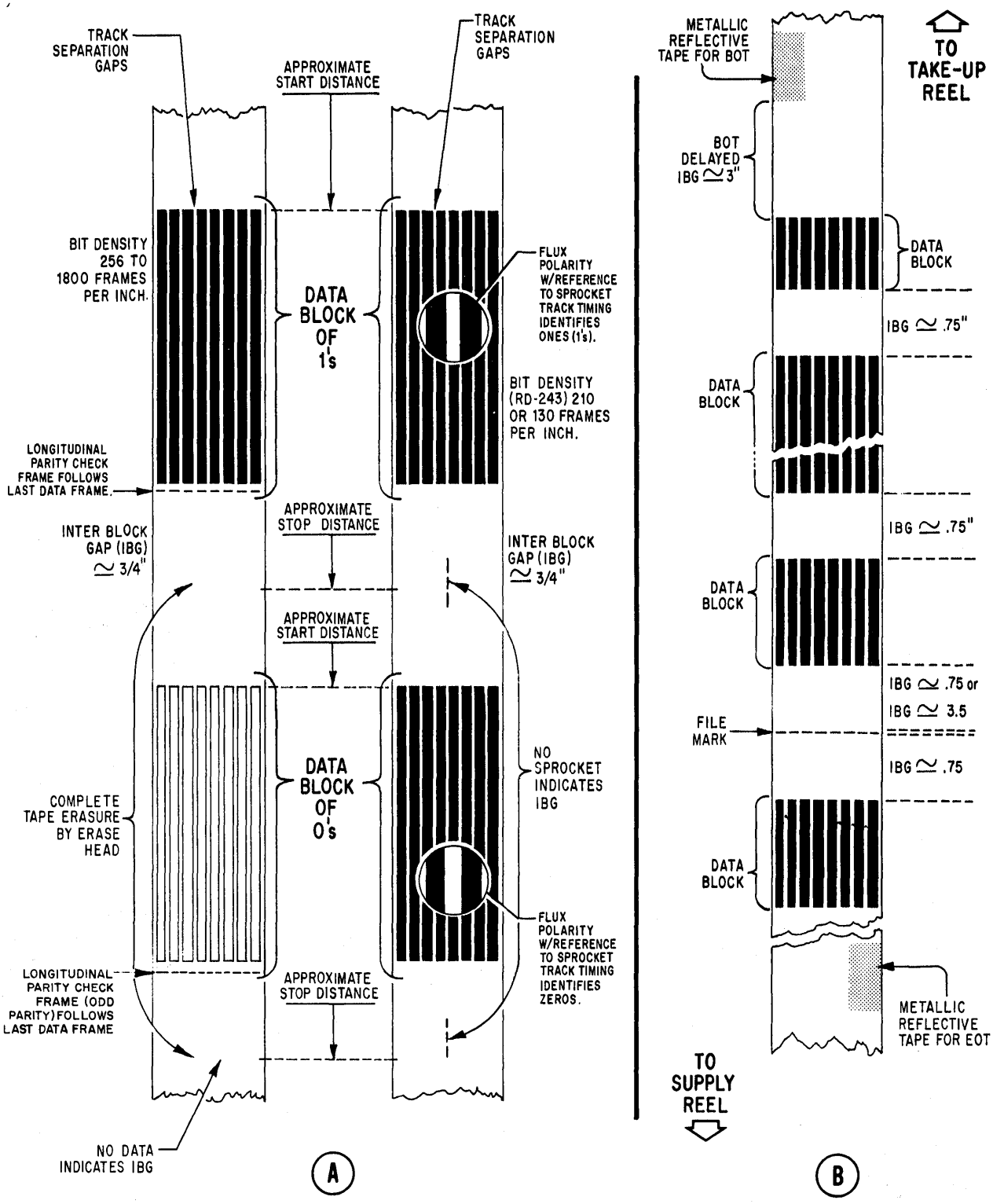

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Figure 5-10.—Views of Magnetic Tape Recording. a. Non-Return to Zero vs Return to Zero, b. Tape Layout.

the flux patterns on the tape. These particles are easily smeared or wiped away, but would transfer intact to the surface of a clear adhesive tape if it were applied carefully. Warning: This section of tape will be unacceptable for further read/write operations and must be detached from the remainder of the reel of tape before being developed.

Figure 5-10b shows the general layout of a tape if its entire length (many hundreds of feet) could be viewed at once. The BOT and EOT labels are detected with photosensing devices. Some transports use a reflective gummed tape that can be affixed directly to the tape (usually the nonoxide side). The RD-243 uses a transparent section of 1/2" Mylar tape 2 or 3 inches long, spliced into the oxide-coated tape. Enough tape extends beyond these labels in both directions to wrap firmly about the two reels.

The blocks of data are not normally viewable but are shown for clarification. Records (consisting of one or more blocks) are a software function and not apparent in this view. Normally, the first block would identify the total number of blocks in the record, or the last block would contain data identifying itself as the end-of-record block, or record size would be standardized as one or more blocks of data for that system.

File marks (not available with the RD-243) separate files (groups of records) on the tape. Some systems use two adjacent file marks with no data blocks between them to mark the end-of-files (no valid data beyond this point). An end-of-files identifier prevents a continuing search to the end of tape (EOT) label when the data field has been exceeded. It also prevents accidental processing of any data that is on the tape beyond the point of the last file.

The data storage limits of magnetic tape are highly variable. Some of the more obvious factors are the bit densities of each block that is written, the number of tracks used on the tape for data storage, the overall length of the tape, and the number of blocks that can be written into the tape's overall length.

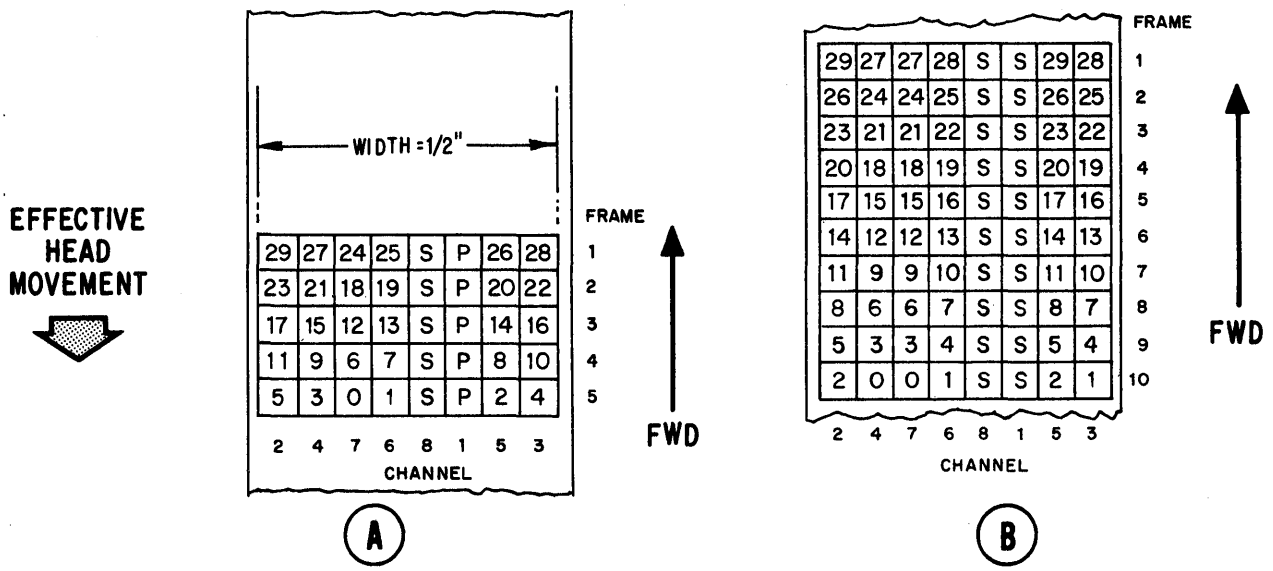
Other influential factors are the format in use (Parity or Redundant), the number of frames per block (which affects the block size), and any special formatting or redundancy features that are introduced automatically by the system software. Another consideration is that a 1,200-foot tape is usually less than 1,200 feet, partly due to wraps on each reel before the BOT and EOT labels are affixed, and partly because its overall length may be shortened further by strippings, where bad portions of tape are removed from the total length.

As a general rule, the shortest block of data that can be written on magnetic tape would consist of one computer word, since this is the minimum output that most computers can achieve in terms of data. The maximum block length would be the maximum number of words that the computer can output in one continuous buffer, which for the CP-642B computer, would be its total memory, or 32,768 words. Use of the Redundant format would double the frame count in the block, which would also double the block length. (Actually, programming techniques exist that permit a continuous buffer output to be achieved with most computers, but this software feature is usually limited to a few maintenance program applications, and calls for the computer to continuously transmit repetitive data outputs. The lower limit of one complete word, and the upper limit of the entire computer memory contents, are considered valid in practical applications).

Recording Formats

The RD-243 is capable of recording data in either of two formats, Redundant (also called NTDS) or Parity (also called UNIVAC) format. Both formats rely on channel 1 (figure 5-11) being odd parity. Bit position 2^{10} of the external function word (fig. 5-8) is used to select the format which will be used.

PARITY FORMAT.—Figure 5-11a shows one 30-bit word (bits 29 through 0) written on tape in Parity format. Each 30-bit computer word is written in five 6-bit frames. Using Parity format, information is written by the program in blocks of 24 words to be compatible with other systems. Each frame contains six data bits (channels), a parity (P) bit (channel), and a sprocket (S) bit (channel), which is used for timing.



LEGEND:

NUMBERS = 2^n VALUE OF COMPUTER WORD.

S = SPROCKET (TIMING TRACK).

P = PARITY (SET IF TOTAL OF DATA BITS IN FRAME IS EVEN, CLEAR IF TOTAL OF DATA BITS IN FRAME IS ODD.

NOTE: TRACKS ARE STAGGERED FOR REDUNDANT (NTDS) MODE WRITEUP.

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Figure 5-11.–Tape Formats. a. Parity Format, b. Redundant Format.

REDUNDANT FORMAT.—Using Redundant format, information is written on tape in blocks that may vary in size, depending upon factors contained in the program. The length of a block is established by the program when the buffer is initiated. As illustrated in figure 5-11b, each frame on tape contains six data tracks (channels), two sprocket (S) bits (channels), and three data bits, each one duplicated in two different tracks. This method requires ten data frames to store one computer word. Channels 1-8 in figures 5-11a and 5-11b correspond to the tape head channel numbers.

DENSITY.—The density of recorded data is determined by bit 2 of the external function word (fig. 5-8). This refers to the number of recorded bits per inch or frames per inch of tape. High density recording is 210 frames per inch (1680 bits per inch). Low density is 130 frames per inch (1040 bits per inch). The density in bits per inch takes into account that two channels per frame are used either as sprocket bits or sprocket and parity bits. The actual number of computer words that can be stored in each inch of tape excluding IBGs) can be determined by the two following methods:

1. Using the recording density given in frames per inch apply the following formula;

$$\frac{\text{recording density (frames per inch)}}{\text{frames per computer word*}} = \text{computer words per inch}$$

*In the redundant mode where two data tracks represent one bit, the RD-243 would require twice as much tape (excluding IBGs) to write the same number of words as were written in the parity mode.

2. Using the recording density given in bits per inch, apply the following formula;

$$\frac{\text{recording density (bits per inch)}}{\text{Data Levels (bits per frame)**} \times \text{Frames per computer word*}}$$

*See previous explanation of redundant and parity modes of operation.

**There are eight channels per frame of tape on the RD-243 of which six are data bits in the parity format.

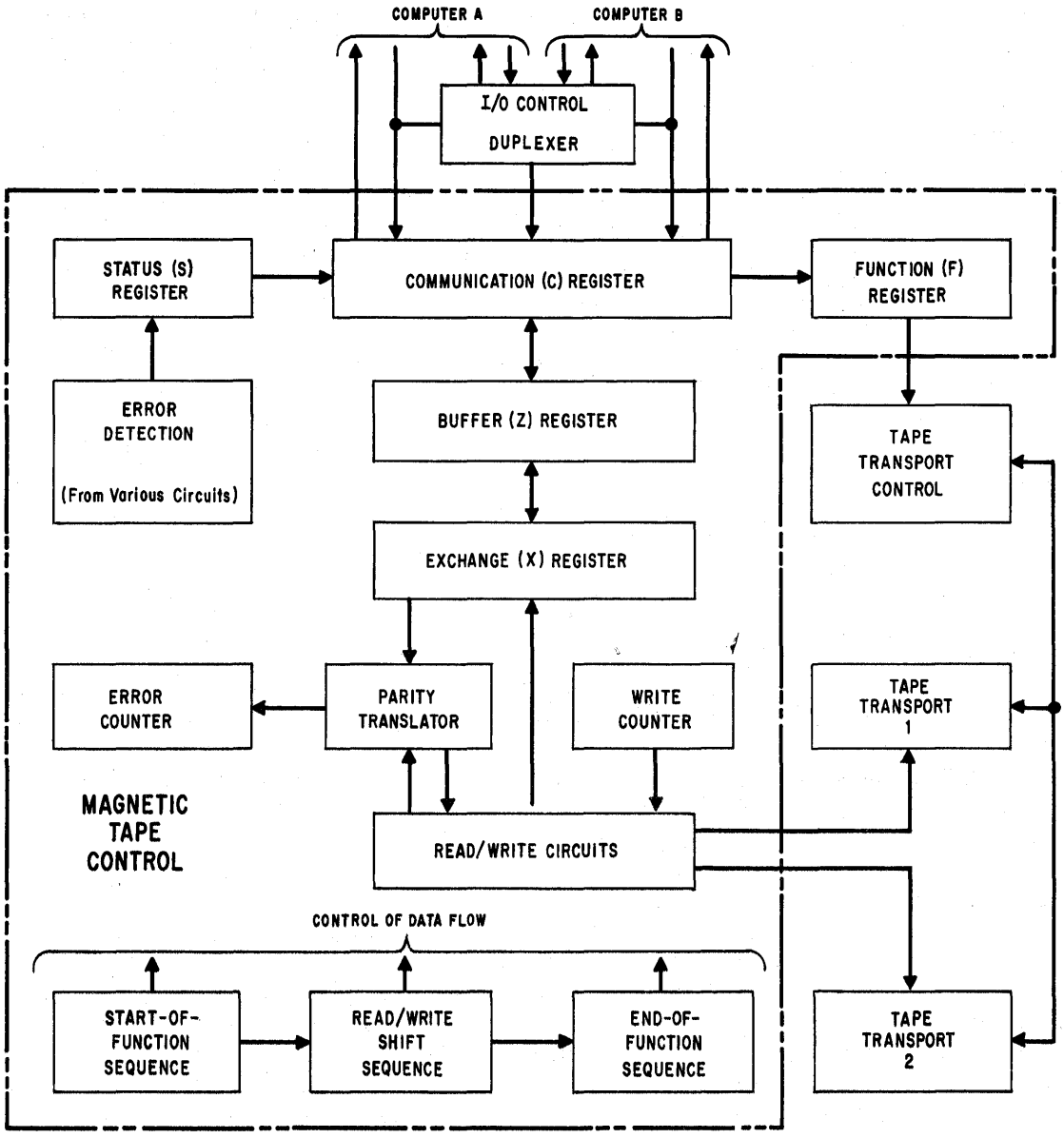

Figure 5-12.—MTU functional block diagram.

BLOCK DIAGRAM

The MTU is made up of four major sections (fig. 5-12): a duplexer, a tape transport control, a magnetic tape control, and two tape transports. The duplexer allows the MTU to be time-shared between two computers without the aid of manual switching. The magnetic tape control transfers data, under control of a computer, in either direction, between the computer and the magnetic tape handlers. In a write operation, the magnetic tape control disassembles 30-bit computer words into either of the two formats suitable for recording on

tape. In a read operation, the data from the tape is reassembled into 30-bit words and sent to the computer. There are circuits within the magnetic tape control which perform timing error or improper condition detection as well as parity checks. The tape transport control accepts data from the computer, via the magnetic tape control, and determines if the specified tape transport can perform the requested function. If the function can be executed, it then provides the necessary control signals to the tape transport. Also contained within the tape transport control are manual controls for tape selection and movement. The tape transport section contains the tape drive mechanism and read/write heads.

Duplexer

The duplexer ensures that only one computer is communicating with the MTU at any time. It interprets requests for control by a computer (external function codes) to determine if the request can be met. It is a function of the duplexer to grant or refuse control of the MTU to computers which request it. Control will be granted upon request when the MTU is in a neutral state (i.e., not being controlled by either computer). For example, if computer A requests control and the MTU is under control of computer B, the request will be "remembered"; control will be granted to computer A when computer B releases control. It is also possible for one computer to take control away from the other by using the Release Remote external function. This external function is provided for use in the event of a malfunction, either equipment or program, in the controlling computer.

The input/output control section of the duplexer is also used to send Input Requests, Output Requests and Interrupt signals to the computer, and receives Input Acknowledge, Output Data Acknowledge, and External Function signals from the computer. It uses the Output Data Acknowledge and External Function signals from the computer to provide enables for gating computer output data, and external function codes (other than duplexer control codes) into the Communication (C) register of magnetic tape control. The Input Acknowledge signal from the computer is used to determine when the input data and Input Request signal, or status interrupt word and Interrupt Signal may be dropped from the C register and control lines, respectively

Magnetic Tape Control

Magnetic tape control (MTC) interprets computer external function codes to determine the type of operation required and communicates with the tape transports. Another function of MTC is the assembly of computer words from frame data (bytes) when reading from tape, and the disassembly of computer words into frame data (bytes) when writing on the tape. MTC uses the Start of Function, Read/Write Shift and End of Function sequences to aid in controlling the MTU.

START OF FUNCTION SEQUENCE.–The Start of Function sequence decodes the external function codes of the controlling computer and determines if MTU conditions will allow the new operation to proceed. It initiates appropriate delays to allow the tape transports to get up to speed, either generates a long gap (if at BOT), or the second half of a short gap to separate blocks of data on the tape, etc. It then initiates the Read/Write Shift sequence.

READ/WRITE SHIFT SEQUENCE.– If a write operation is specified, the Read/Write Shift sequence requests a data word from the computer. For Write (parity or UNIVAC mode), the Read/Write Shift sequence disassembles the 30-bit data words into five six-bit groups (or bytes) for writing onto the magnetic tape, beginning with the upper six-bits and proceeding to the lower six-bits. As the disassembly process begins on the current word, a request for another word is transmitted to the computer. Writing continues until the computer fails to respond to an Output Request within a specified time, at which time the Read/Write Shift sequence exits to the End of Function sequence.

For a Read operation, the Read/Write Shift sequence assembles every five frames of data contained on the magnetic tape into a 30-bit computer word, and repeats this operation for as many frames as there are in a single block of

data (actually, until an IBG is detected by the absence of sprocket bits). The function word for the read operation must specify the format in which information is written on the tape.

A Write (Redundant or NTDS mode) operation would cause the Read/Write Shift Sequence to disassemble the received 30-bit word into three-bit groups (half-bytes) 10 times, and to duplicate each bit within the six-bit frame when writing it. Read (Redundant) operations would reassemble ten frames of data into one 30-bit computer word, using a "1" in either bit position as a data "1" in assembling the half-bytes. When MTC has fully assembled a 30-bit word, an Input Request is transmitted to the computer to initiate a data transfer. If the Input Request is already up, indicating that the previously assembled word was never accepted by the computer, a timing error exists and will be indicated by the Input Timing Error (ITE) bit in the status register being set at this point. The previous data word is lost when the currently assembled word is transferred to the C register for output to the computer. The Input Request signal remains up to signal the computer that a word is still ready for input by the computer. The Input Timing Error status, in the interrupt word that the computer will receive once the read operation is complete, will inform the computer that one or more words were not included in the buffer and were lost due to timing problems or the use of a buffer that was smaller than the number of assembled words found in the data block.

An Output Timing Error (OTE) occurs when the first computer word has not been received at the point where the first frame of data is to be written. Not having a word to write inhibits a proper write, but has still caused tape motion and some erasure by the tape head. Another OTE condition will occur when a subsequent word has not been received from the computer at the correct point of disassembling and writing it. This OTE condition is inhibited from appearing in the status word since the failure of the computer to respond with another output word may simply mark the end of the buffer. The MTC's End of Function sequence would terminate to write operation with an IBG. However, if an Output Data Acknowledge signal is received from the computer after the End of Function sequence is initiated, an OTE status would be indicated in the interrupt word, showing that a timing problem occurred in that the unwritten portion of the buffer was not available soon enough to the MTC for it to include it in the data block being written. For the RD-243 (and other MTUs covered in this text), only one data block can be written per external function write instruction. Assembly begins on the next word while waiting for the computer to acknowledge receipt of the current word on its input lines. Reading continues until an extended absence of data indicates an End of Block. If MTC contains an incomplete word at an End of Block, an OUT OF SYNC error is transmitted to the computer in the status word at the End of Function.

END OF FUNCTION SEQUENCE.—The End of Function sequence causes MTC to be reset for the next operation (new external function code). It initiates a delay to provide the first half of the End of Block spacing on the tape [which is also known as interblock gap (IBG)] and also causes a Status word interrupt (End of Normal Function) to be sent to the computer. (Interblock gaps are discussed in detail in chapter 5 of *DS 3 & 2, Vol. 2,* as they relate to the RD-270(V) Magnetic Tape Unit.)

REGISTERS AND COUNTERS OF THE MTC.—MTC is made up of the following registers and counters, with the appropriate switches and indicators for each mounted on its front panel (upper right panel of MTU):

(1) Communications register—The communications (C) register is a 30-bit input/output buffer register for data exchange with the controlling computer. All data, nonduplex external function codes*, and Status words must pass through this register when coming from or going to the computer. (*Duplex codes involving the lower three bits of the external function word from the computer are not gated into the C register, but are gated directly into the duplex section of the MTC. The reason for this is that the MTU will ignore any nonduplex commands from a computer that is not in control, but must be able to respond to

duplex commands from either computer at all times. This is the reason simulated "external function" operations involving duplex codes are not effective when manually inserting them into the C register, and the reason why manual control of the duplex section must be done directly through the duplexer control on the MTC panel (fig. 5-3).)

(2) Function register–The function (F) register receives the external function codes (nonduplexer) from the C register and retains the specified function during the operation, while informing tape transport control of the action desired.

(3) Status register–The status (S) register accumulates, from various circuits, any error information which will be sent through the C register, accompanied by an interrupt signal, to the controlling computer at the end of the ordered function. An interrupt condition, which involves sending the current status conditions as an interrupt word to the computer (if not inhibited by computer programming), may indicate present or previous errors under different circumstances. An improper condition, for instance, usually occurs at the start of a new operation, and usually involves an external function word that indicates an operation is to be performed that is invalid under current circumstances. This might be described as a "present condition," since the presently desired operation has not been (and will not be) performed. A write operation, which might generate errors involving OTEs (output timing errors), parity, or timing problems, would be sent to the computer after the write operation was completed. The interrupt might also indicate a normal termination of a write operation. Depending upon the viewpoint, this might be considered a "previous" operation or the "currently completed" 'operation. A read operation, on the other hand, might have status indications that not only refer to the read operation itself, but might reflect any errors of the previous write operation that placed that block of data on the tape. A status word following a read operation would indicate either an AND condition, where both the preceding write and the read operation are completed properly, or it would indicate a NOR condition, where either the read OR the preceding write did NOT complete properly.

(4) Buffer register–The buffer (Z) register is a 30-bit register used for assembly and disassembly of computer words. For assembly (reading), it receives the data frames one at a time from X and shifts them to their proper position to form a complete word. For disassembly (writing), it receives the computer word from the C register and shifts it into the X register six bits at a time for writing on tape, beginning with the upper byte or half-byte.

(5) Exchange register–The exchange (X) register (6-bits) function varies with the mode of operations (Read or Write) and with the format in use. In Read operations, X receives data from the Read/Write heads six bits at a time (one frame of data) and transfers a byte of half-byte of data to Z where a complete 30-bit word is assembled. The operation is reversed for Write operations. It uses the Parity Translator for generation of parity bits and checking for errors. It also uses a Write Counter to control frame periods.

(6) Parity Translator–The parity translator is used when writing in Parity format to supply an odd parity bit for each frame. When reading Parity format, it checks each frame for odd parity. If any frame shows even parity, it indicates an error to the error counter and the S register. When writing in Redundant format, the parity translator's output is always a "1" for each frame. Since a constant "1" matches the bit in the sprocket track in all respects, this bit is referred to as the "redundant" sprocket bit for the redundant mode.

(7) Error Counter–The error counter counts signals from the parity translator whenever a parity error is detected. The content of the error counter is displayed on the front panel, and no other use is made of it.

(8) Write Counter–The Write Counter is used for controlling the frame period during write operations and for measuring elapsed time in both read and write operations. This enables the detection of timing errors and End of Block.

(9) Read/Write circuits–These circuits handle the data words between the eight channels on the read/write head and the X register for each tape transport.

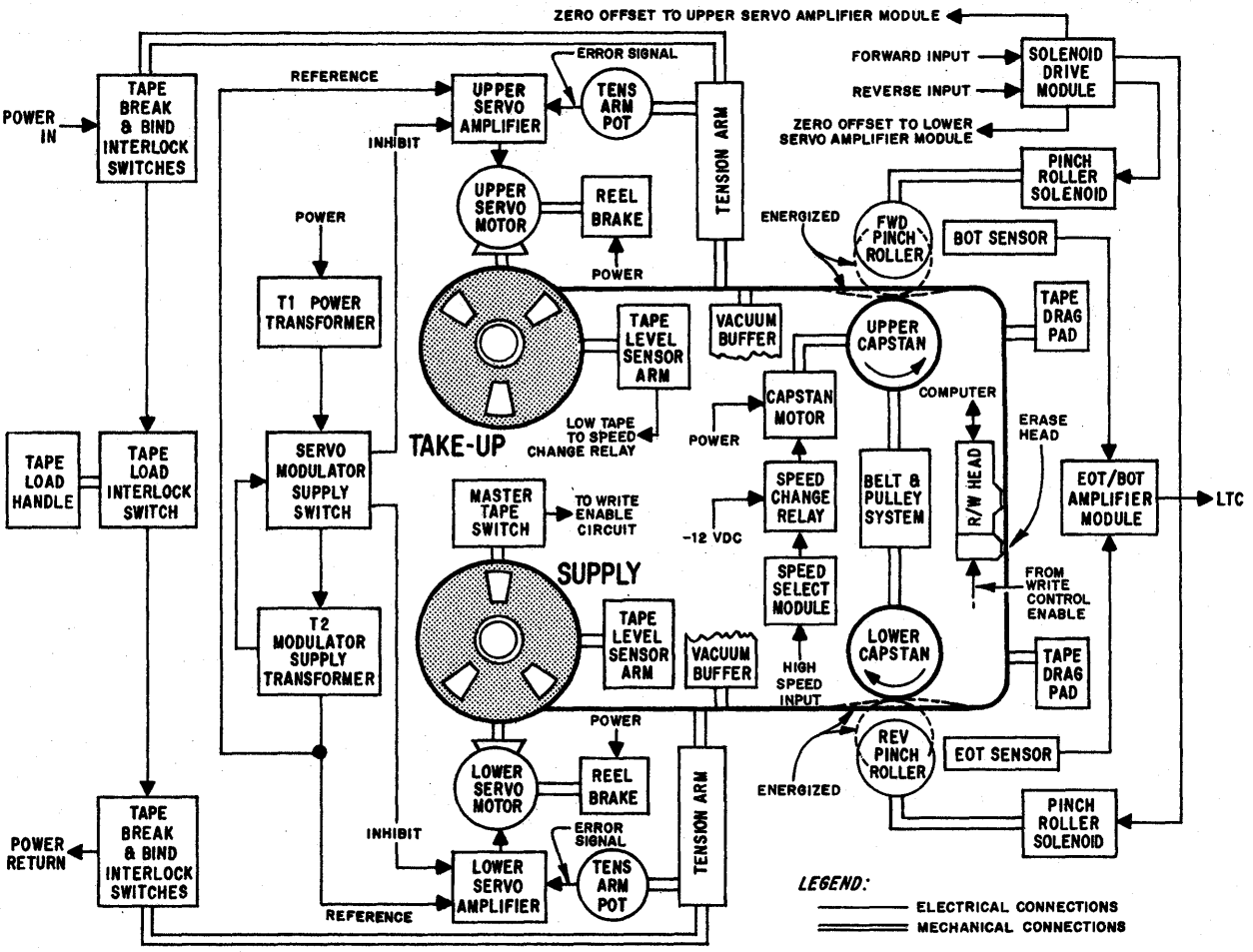

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Figure 5-13.—Tape transport block diagram.

Tape Transport Control

Tape transport control determines if the specified tape transport can perform the function requested by MTC. If the function is legal, tape motion is initiated; if not, MTC is informed that an improper condition exists and the function cannot be executed (e.g., a write command at EOT).

Tape Transports

The mechanical components of the transports consist of:

(1) A tape storage and supply system (tape reels)

(2) A servo system that controls the tape reels (tape hubs)

(3) A servo control mechanism (primary inputs taken from placement of the tension arms)

(4) Two tape buffer systems (two tension arms and two vacuum chambers) to isolate the coarse movements of the servo system from the primary drive mechanics

(5) Primary drive mechanics, consisting of two 2-speed capstans and two pinch roller assemblies (the capstans provide instant tape acceleration and constant tape speed, while the pinch roller assemblies determine the direction of tape movement)

(6) Tow positive braking systems (drag pads for the tape; automatic power-off brakes for each hub)

(7) Tow heads: one erase, and one read/write (no read-after-write capability) head with 8 tracks on it

(8) Condition sensing elements that will detect BOT, EOT, low tape supply, tape breakage, or binding, tape load and write lockout conditions. Figure 5-13 is a functional block diagram of the tape transport.

Associated with each tape transport is a drive electronics unit that contains the plug-in modules used with the transport. These modules determine such things as:

(1) Rotating speed and direction of each hub servo motor (primary inputs from the tension arms)

(2) Which pinch roller (forward or reverse) is to be energized

(3) If BOT or EOT is sensed

(4) If write lockout is set

Tape transport operations are controlled by the computer via the MTC and tape transport control (TTC) logic. For maintenance and testing purposes, operation of each tape transport may be controlled manually.

TAPE STORAGE AND SUPPLY.— Primary tape storage is provided by two 10-1/2 inch tape reels mounted on hubs. Tape threaded between tension arm rollers and bridge rollers provides secondary tape storage to buffer the effects caused by sudden changes in tape motion. Other secondary buffer storage areas are provided by the vacuum buffer chambers (fig. 5-5) which smooth out any remaining jerkiness not handled by the tension arms. These secondary tape storage systems isolate the slower responding tape reels from the quick-response primary drive mechanics.

Tape motion is caused when the solenoid in one of the pinch roller assemblies is energized, bringing the attached pinch roller in to press the magnetic tape against the adjacent revolving capstan. This action causes the motion of the capstan to be transferred to the tape. The two capstans are powered by a single capstan motor, but revolve in opposite directions, so one pinch roller acts as the forward pinch roller, and the other acts as the reverse pinch roller. Tape motion will continue as long as the pinch roller keeps the tape against the capstan, and the capstan is revolving. The pinch rollers and the capstans make up the primary drive mechanics for the transport.

The tape storage and supply system adds tape to and removes tape from the primary drive mechanics at a rate determined by the operating speed of the capstans when a pinch roller assembly is energized. The amount of tape on the tension arms is initially determined by the primary drive mechanics (which causes outward or inward deflection of the tension arms). The deflection of the tension arms, in turn, controls the servo hub motors, and these, in turn, rotate the tape reels. Movement of the tape reels compensates for the shift of tape from one tension arm to the other and brings the tension arms back toward their midrange positions. Starting, stopping, and direction of rotation of the servo hub motors is controlled solely by the position of the tension arms with respect to their midranges.

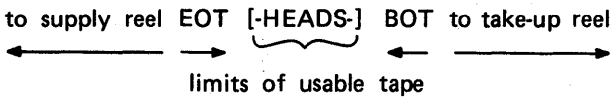
When the FWD pinch roller is energized, so that the tape moves from the bottom tension arm to the upper tension arm, the lower tension arm moves inward from its midrange position as tape is drawn from it, and the upper tension arm moves outward from its midrange position as tape is added to it. Movement of these tension arms is detected by a potentiometer on each tension arm shaft assembly. The potentiometer generates an error signal, the polarity of which depends on whether the amount of tape on the tension arm decreases or increases, and whether the resulting direction of offset was inward or outward. The error signal is amplified and fed to the appropriate direction windings of the servo hub motor closest to that particular tension arm. The servo hub motor rotates, and its direction of rotation will either draw tape from the tension arm if it has excess tape on it (outward movement of the tension arm), or add more tape to the tension arm if it has lost tape (inward movement of the tension arm). As the tension arm moves farther from its midrange position, the speed of the servo hub motor closest to it increases. Eventually, a point is reached where

the speed of the servo hub motor is sufficient to cause tape/reel speed to equal tape/tension arm speed, and the tension arm will be stabilized in its arc of movement. This condition will continue with only slight changes until the engaged pinch roller is deenergized, at which time the tension arms return to their midrange positions as a result of the reels still rotating, but this return will result in the movement of the servo hub motors and tape reels first slowing, then stopping, as the tension arms move to their midranges.

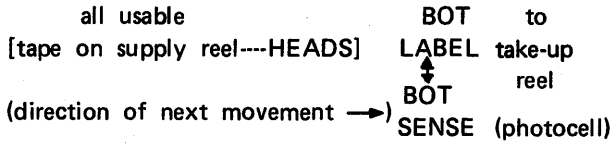
Changes in tape direction are controlled by the pinch roller assemblies and the opposite direction of rotation of the respective capstans. Once tape begins moving, the tension arms are offset by changes in the amount of tape that "plays" between the tension arm rollers and the bridge rollers. Movement of each tension arm controls the respective tape hub servo motor, causing the tape to be fed or taken up on the tape reels as needed. However, misfortunes sometimes occur. The tape can break, or bind and wrap tightly about one of the capstans, or suffer other mishaps. The mechanics of the transport must be protected as much as possible from damage that could be incurred when one of these things happens. The most probable result of any irregular operation would be that the tape would break. If this occurs, the tension arms will lose their tape restraints, and fly outward toward their outer stops. Dashpots have been installed to slow this movement and absorb some of the excess energy before the stops are reached. Limit switches are also effected near the outer extremes of the tension arm movement and automatically shut off all power to the transport. Finally, the hub brakes are automatically engaged by the power loss and prevent further hub movement, effectively preventing the reels from spinning feeely and spilling tape all over the deck.

The photoelectric cells used in detecting BOT (beginning of tape) and EOT (end of tape) are intended primarily to insure that the tape cannot run off of either reel once it has been properly mounted. Tape movement is automatically inhibited immediately upon reaching the EOT label when moving forward, and inhibited immediately upon reaching BOT when rewinding or moving in reverse. Thus, from BOT it is only possible to go forward, and from EOT it is only possible to rewind or go in reverse. The BOT label also provides the initial reference point from which all subsequent blocks of data, separated by IBGs, can be located.

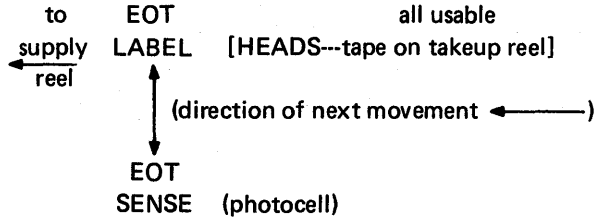
The positions of the BOT and EOT photocells place the BOT detection point above the heads, and EOT below the heads. When BOT is sensed, most of the tape is on the supply (lower) reel, and only the leader is on the take-up (upper) reel. Tape movement at this point can only be from the supply reel to the take-up reel (generally upward movement). The EOT photocell, mounted below the heads, stops tape as soon as all the usable tape has been transferred to the take-up reel. Since each photocell is positioned at the lag end of the direction of movement that it is meant to control, the clear cellophane labels will be detected before they reach the vicinity of the heads, and the oxide-coated tape will stop with the heads always within the region between the two labels. The effect would be like this:



The long arrows indicate which direction the reels are in from the heads. The short arrows indicate the direction of tape movement controlled by the photocell station mentioned above each. The brackets mark the limits of tape movement across the heads. If tape were at BOT after loading, it would look like this:



If the tape were at EOT, it would look like this:



When the tape is in use, the heads can be positioned anywhere within the limits of the two brackets:

[tape on supply reel--HEADS--tape on takeup reel]

VACUUM BUFFER.—The vacuum buffer (fig. 5-5) isolates tape on the tension arms from the tape in the drive system. The buffer has two chambers, each of which has a large rectangular vacuum port in which the tape forms a loop. The tape loops in through the open side as air is drawn through the small circular port in the corner and the series of tiny bleeder ports located on the rear wall of each chamber.

When power is applied to the tape transport, a partial vacuum, created by the vacuum blower motor sucking air through the circular and bleeder ports, draws a loop of tape into the upper and lower chambers as shown by the dotted line in figure 5-6, view B. Vacuum pressure is such that tape tension created by the tension arm springs is balanced when the tape loop in each chamber leaves approximately half the tiny bleeder ports uncovered (outside the seal created by the tape loop).

If too many bleeder ports are left uncovered, the vacuum will drop in the sealed off portion of the vacuum chamber and allow the tension arms to pull some of the tape from the chamber. If too much tape is removed, the additional bleeder ports that are then covered will increase the vacuum suction in the chamber and cause more tape to be drawn from the tension arm. The vacuum chambers smooth out small, jerky movements of the tape and prevent possible tape slippage and positioning errors at the heads, while the tension arms compensate for major tape movements. The entrance and exit rollers (fig. 5-6, view B) insure that the tape stays positioned over the entire open end of the vacuum chambers.

When a forward command is applied to the system, the lower chamber is the supply chamber (removed tape ——→ increased vacuum) and the upper one is the take-up (added tape ——→ lower vacuum) chamber. Reverse commands create the opposite condition. As soon as the inertial (resistance to change) of the tension arms is overcome during changes in tape motion, the loop will quickly return to its balance point.

TAPE LEVEL SENSOR ARMS.—The tape (upper) sensor arm is positioned against the tape to prevent a whiplash effect of the tape from occurring during a RWD (high speed movement) of the tape by a sudden stop at BOT. Contacts of the upper tape sensing arm (fig. 5-13) switch are used to deenergize the speed change relay during a rewind operation when only a 1/4″ thickness of tape remains on the take-up reel. The lower arm is not in use for the RD-243.

DASHPOTS.—Dashpots, a form of shock absorber, prevent the tension arms from striking their stops with great force if the tape breaks. The dashpots help prevent two possible aftereffects that might follow a violent stop of the tension arms. First, they help prevent the tension arms from being bent. Second, they help prevent the tension arm cables in the rear of the transport from bouncing and possibly jumping free of their pulleys. The tension arm cables link the tension arms to the tape load handle. Evidence that a cable has jumped its pulleys is seen when a tension arm remains against its outer stop and is not pulled in by a turning of the tape load handle. This problem is easily corrected when it occurs by releasing the tape load handle (turning it to the point of least tension), gaining access to the rear of the transport, and while the affected tension arm is brought in away from its outer stop manually, taking the slack in the cable and placing it back over the pulley.

TAPE DRIVE.—A single two-speed a.c. capstan motor is coupled by a belt and pulley arrangement to both the upper and lower capstans on the drive plate assembly. The motor is energized when 60 Hz power is applied to the tape transports. The capstans are continuously rotating, the upper capstan counterclockwise and the lower capstan clockwise. Tape is not driven until the forward (upper) or reverse (lower) pinch roller solenoid is energized, causing the respective pinch roller to force tape against a rotating capstan. The pinch roller solenoids are energized when a select (Forward

or Reverse) signal is issued by the computer (or manually from the front panel). This signal is applied to ground through the solenoid drive module in the drive electronics unit. Since approximately 3 amps are required by the solenoid to force the pinch roller against the capstan, be careful when working on or around the pinch roller solenoid.

SPEED CHANGE RELAY.–The speed change relay applies power to the high-speed winding of the single capstan motor that controls both capstans when energized. This relay is energized only by the Rewind select signal from the computer or the front panel, and results in a rewind tape speed of 225 ips. The relay is deenergized by the upper high-tape sensor arm and results in rewind tape motion being slowed from 225 ips to 112.5 ips.

HUB MOTORS.–Power for turning the tape hubs is delivered by upper and lower servo motors. Each motor has two fields (one each) to provide for clockwise (CW) and counterclockwise (CCW) rotation so that tape may be payed out or taken up from storage in either direction. In the event that power is suddenly removed from the tape transport (e.g., tape breakage), a spring loaded brake will stop the reel motors.

READ/WRITE HEAD.–An eight track magnetic head provides the write and read sensing elements for the MTU. The head is mounted on a base that is attached to the drive plate. The head, mounting base, and tape through guides mounted on the base are precision machined, and repair is considered beyond the capabilities of field personnel; therefore, the head must be replaced as a unit. These heads are very expensive, while a complete overhaul including recrowning of the head surface is approximately one-fifth the cost of a replacement. When a tape head is removed, do not strip it of any parts before shipping it to a repair facility. The EIMB Communications Handbook (NAVSHIPS 0967-000-0010) service notes, and EIB 689 and 753 have detailed instructions on replacing the read/write heads. EIB 796 is a reference pertaining to removal of piece parts from the head.

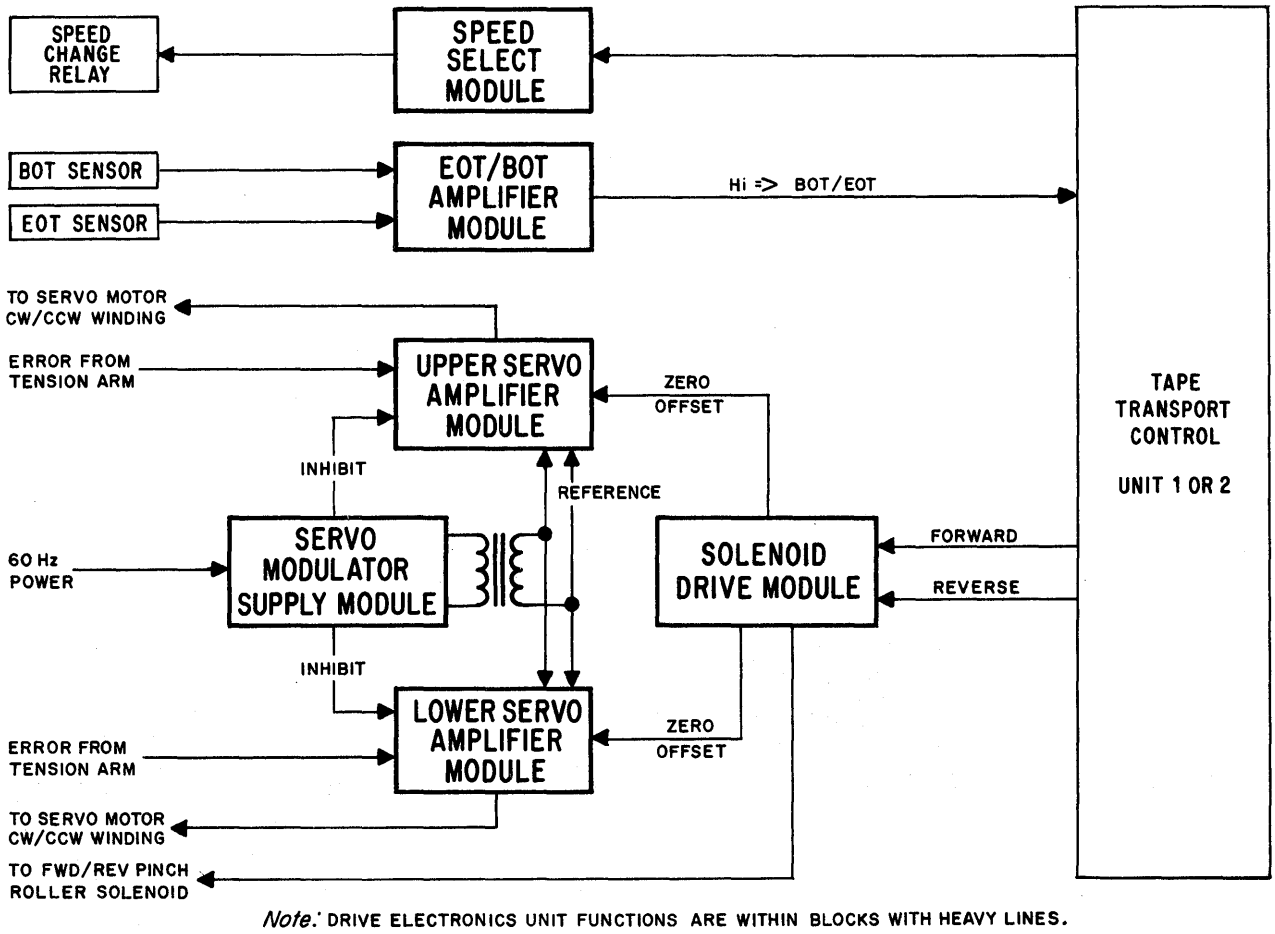
Drive Electronics Unit

There are two drive electronics units, one behind the transport area for each transport. These can be assessed by loosening the Allen head bolts in the right corners of the respective transport and swinging the transport out on the hinge that supports the left side. Each drive electronics unit contains most of the analog circuitry required by the mechanics of the respective transport, and these are mounted on six separate printed circuit cards, or "modules" as they are frequently called because of their analog natures and large sizes. Of the six modules, five can be assessed and removed from the front of the drive electronics unit with the transport swung open. The sixth is mounted to the rear of the others and is not accessible from the front. Each module is of the "plug-in" type, and suitable extension cards are available if it is necessary to access points on a module during troubleshooting or adjustment. Figure 5-14 is a simplified block diagram of the drive electronics unit.

SOLENOID DRIVE MODULE (fig. 5-14).–Circuits for energizing the forward or reverse pinch roller solenoid, and for generating the zero offset signals used in the servo amplifiers, are contained on the solenoid drive module. A forward or reverse signal from the tape transport control (TTC) is applied to the solenoid drive module and causes an output to one end of the forward or reverse pinch roller solenoid. This completes the energizing circuit through the solenoid and causes appropriate tape motion. The zero offset signal output determines the servo amplifier operating reference voltage and results in offsetting the tension arms while tape is being driven.

SPEED SELECT MODULE (fig. 5-14).– The speed select module has circuitry used to energize or deenergize the speed change relay. The speed change relay has been discussed previously in this chapter.

EOT/BOT AMPLIFIER MODULE (fig. 5-14).–The EOT/BOT amplifier has two identical circuits, one for BOT and one for EOT signals. These signals are amplified and coupled to TTC by the EOT/BOT amplifier.



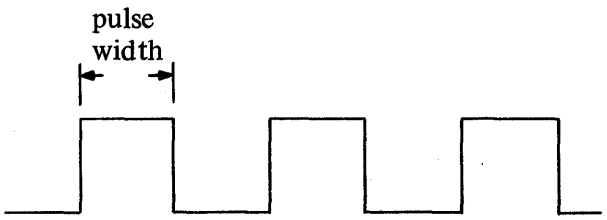
124.442

Figure 5-14.–Drive electronics unit simplified block diagram.

SERVO MODULATOR SUPPLY MODULE (fig. 5-14).–The servo modulator supply generates square wave reference and inhibit signals for the servo amplifier modules. The reference signal directs the error signal (from the tension arms) to the proper amplifier, and the inhibit signal directs the power output from the servo amplifier to the cw or ccw winding of the servo motor.

The servo system uses constant amplitude, variable width square wave pulses to regulate the speed of the servo motors. When a very low speed is required, the pulses look like this:

As the speed is increased, the pulses look like this:



The average voltage is, therefore, raised, even though the peak voltage does not vary. The servo modulator supply module generates the square wave reference voltage. The servo amplifier takes the reference voltage and varies the pulse width according to the potentiometer

value derived from the tension arm position offset. The direction of the offset determines which winding, cw or ccw, receives the voltage input in each servo motor.

This technique produces much better control of the servo motors at low speeds than can be achieved with a variable d.c. voltage. The peak voltage value insures that the motor does turn at low speeds, while the narrow pulse prevents continued acceleration to peak speed. As a result, the servo motor alternates between an acceleration period and a coasting period, with the length of each period dependent upon the pulse width ratio. The mass of the motor produces an inertia that smooths out the disjointed motion into an average speed, which is proportional to the average voltage.

SERVO AMPLIFIER MODULE (fig. 5-14).—Two servo amplifier modules control the direction and speed of the servo motors that drive the upper and lower tape reels. These servo amplifiers operate under control of the solenoid drive and servo modulator supply modules. Each servo amplifier receives an error signal proportional to the extent the respective tension arm is displaced from its null position, and converts the error signal into power to drive the respective servo motor. The reference signal sends the error signal to the correct amplifier, and the inhibit signal directs the power output to the proper directional winding in the servo motor. The zero offset signal into the servo amplifiers determines the operating reference voltage and the directional offsets of the tension arms during tape motion.

MANUAL OPERATIONS

There are several manual or offline operations that may be used for testing or maintenance requirements. These procedures are based on the assumption that the tape transports have been checked and are operating properly. Successful completion of the manual operations indicates that the magnetic tape control and the tape transports are operating correctly, with the possible exception of those circuits used in I/O transfers with the computer(s) and the duplex functions. The offline procedures consist of a general preparatory sequence of steps that are modified for individual operations (e.g., Write, Parity Format, Low Density, TT1).

When using the offline procedures, or any test procedure, check for errors using the error indication circuits. The Status register will directly display error types. By observing the contents of the C register during a Read operation, erratic operation of the Read (or the previous Write) operation may be noted. Timing errors, although indicated by the Status register, are best analyzed when they occur during computer controlled operations because the front panel controls cannot be switched fast enough during manual operations, and this may generate invalid timing error indications. The general preparatory sequence and some of the individual operations are discussed in the following paragraphs. Figures 5-3 and 5-4 illustrate the controls that are used for manual operations.

The basic reasoning behind manual testing is NOT to free the computer for other work. When the computer is available, it should be used as a means of testing online equipment since it is much more effective at doing this. However, if the computer is not available, then manual testing can be used as a means of testing most of the equipment parameters that are required for computer operations. This excludes the I/O and duplex capabilities of the equipment, and the I/O section in the computer related to that channel. Therefore, the objective normally involved with manual testing is to try and duplicate those parameters (functions and circuits) that are required for computer operations as closely as possible, even though exact duplication is clearly not possible.

General Preparatory Sequence

The objective of a manual operation is to reemploy most of the circuitry needed for online operations again in the offline mode. This will help verify that these circuits are working properly. For this reason, the manual mode requires that an external function word for the desired operation be manually inserted into the C register, and then for the RD-243, be made to act on that word as if it came from one of the computers. The following is the procedure by which this can be done:

(1) At the Speed Select switch, select any speed other than STEP (actually, the step

position could be used, but the numerous inputs then required from either the CYCLE STEP or PHASE STEP switches limit use of this position except for specific maintenance situations).

(2) Depress Master Clear.

(3) Rewind the desired transport in order to initiate FWD operations from BOT. Otherwise, move tape forward for several minutes for REV or RWD operations.

(4) Set selected tape transport in Automatic.

(5) Set Tape Transport Address to correspond to the transport number that will be used in the external function word (step 9).

(6) At the duplexer controls under the In Control, depress either A or B.

(7) Set the Operation Mode switch to Inspect EF. This permits an external function word to be inserted manually into the C register.

(8) Under I/O CONTROL, depress REPLY. This will condition the logic to respond as if the contents of the C register were an external function word received from a computer at the completion of step (10).

(9) In the C register, manually set the external function bits required to initiate a specific function (fig. 5-8). This is the step at which the general sequence will vary for the type operation desired.

(10) Rotate the Operational Mode switch to I/O Inact. This inhibits I/O signals with the computer and also initiates tape motion. The contents of the C register (which currently still contains the external function instruction from step (9)) will be the source of data first written on tape during execution of a write operation.

(11) For a write operation, the C register may now be cleared or its contents altered at any time to write a specific word on tape. If unchanged, the function code from step (9) will remain and also be used as the data word.

At this point, the technician can elect to insert his own test data through the C register for a write operation, or read back and compare his own test data with either a forward or a reverse read operation. Since tape is already in motion at this point, the function code that had been inserted into the C register would occupy the first portion of the block being written for a write operation. It will also be the first data reentered into the C register on a subsequent read, and the last data read from the tape on a reverse read. A read operation will always show the function code used during the previous write operation, since this is the information that was actually recorded on tape.

A standard pattern used in testing a transport manually is to start a write operation, then clear the C register to eliminate the write code in it. Then, one by one, each data bit of the C register is set by pressing the correct indicator button, maintaining an even rhythm from one to the next. When all the bits of the C register are lit, the clear button is pressed again to blank the register. The write operation is then terminated (as will be explained shortly). The next operation might be a reverse read of that same data block. If this occurs, the data being read from tape will be in exactly the opposite sequence, word for word, of the data as it was written in that block. This means the following should be observed for the previous block:

(i) Cleared C register (all bits extinguished, although tape is moving)

(ii) All bits lit (end of bit sequence encountered first)

(iii) Each bit going out in sequence, in rhythm, in the opposite order as were lit during the write

(iv) All bits extinguished again (entered the area written after the first time the C register was cleared during the write)

(v) Write Function code bits in C register

(vi) Tape stops, with C register clear

If the next operation is a forward read, to go over the same data block again, the appearance of the C register should be exactly the same as during the write, and the tape will stop at the end with the C register clear again. A final adjustment is made to the assembled word to put it in the same bit order as written before sending it to the computer for a read reverse operation. This means every word has all 30 bits in the same internal order, although the word order changes between forward and reverse read operations.

At the end of any read or write operation, the final act of the MTC logic is to clear the C register prior to the preparation and sending of the interrupt word to the computer. If in the manual (offline) mode, no interrupt word is

prepared or sent to the computer. If online, the C register is again cleared once the interrupt word is accepted by the computer. The C register, therefore, normally appears in a cleared state, except when actually involved in read or write operations.

For a write operation, tape motion will continue until EOT is detected, or until step 12 is executed. In the read mode, tape motion will also cease at an End of Block (IBG detected).

(12) To terminate a write operation, set the Operation Mode switch to INSPECT EF. This will terminate the transfer of the C register contents to the read/write head and initiate an EOF (end of function), which will produce an EOB (IBG).

(13) Depress I/O Control Clear to clear Int and Active, which are set at EOF.

(14) Depress Neutral. Return to step (8) if another operation is to be initiated.

An alternative sequence replaces steps (7)–(10), and (12)–(14). If this sequence is used, the Operation Mode switch remains in the I/O Inact position. Substitute the following steps for (7)–(10) above.

(7) Set the desired function code into the Function Register directly by use of the Density, Format, Write, Direct, Rewind and Unit 1 or Unit 2 pushbutton switches.

(8) Insure that a conflicting set of conditions does not exist when the buttons are pressed. Otherwise, the RD-243 will generate an Improper Condition after step (10).

(9) For write operations, place the desired data word to be written into the C register at this point.

(10) Press the T2 pushbutton under the start function sequence. This initiates the start function sequence after the point where the C register contents would normally be transferred to the Function Register, so the condition of the function remains as set in step (7). The tape will begin moving at this point. Step (11) remains the same.

For steps (12)–(14), substitute the following step:

(12) Depress T20 in the End Function sequence.

Each method has its own advantage. The first one most closely parallels the approach used when under computer control. The second is slightly easier to use, and avoids problems that sometimes appear when attempting to switch the operation Mode switch quickly from one position to another. Switching the Operation Mode switch too slowly can produce invalid errors in the status bits and the error counter. Switching too strenuously has sometimes resulted in damaged switches or knobs.

The first method in performing various operations will be described.

Write Operations

To perform a "Write 1's–Parity format–Low Density–1 Block–on TT1" operation, execute steps 1 through 8 of the general preparatory sequence. Then perform the following steps:

(9) Set bits 12, 10, and 5 in the C register

(10) Set the Operation Mode switch to I/O Inact

(11) Set all the bits in C

(12) Terminate the function after three or four seconds.

This sequence will write one block of "1's" in parity format and low density. A whole tape of "1's" may be written by omitting step 12. This technique is especially useful in preparing some of the test tapes used during some of the alignment and maintenance procedures. (Note: This does not include skew tapes–see earlier portion of chapter for explanation of tapes.)

Read Operations

Magnetic tape on the RD-243 may be read either forward or reverse. If the tape is to be read in the forward direction, it must be positioned at the beginning of the block to be read. If it is to be read reverse, the tape must be positioned at the end of the block to be read.

With the same tape correctly positioned, it may be reverse read by performing steps 7 through 10 of the general sequence and modifying step 9 by setting bits 12 (for TT1, or 13 for TT2), 10, and 9. When tape motion

begins, all bits of C will be set, but only bits 12 (if TT1, or 13 if TT2), 10, and 5 will be set when tape motion stops. This, of course, is the function word recorded at the beginning of the previous write operation. Note that the bit order is unchanged during a reverse read, but that the word order is backwards. Check the Status register for a parity or sync error and the Error Counter for any accrued parity errors.

In the read forward operation, with the tape correctly positioned, bits 12 and 10 of the C register must be set in step 9. During and after tape motion, the indications are the same as a read reverse operation, except that the C register contents will appear in reversed sequence.

Special Write Techniques:

(1) Slow-Speed Writes–Once a write operation has been initiated, the Speed Select switch can be rotated to any low-speed position to observed word disassembly (data transfer from C to Z) as the information is being written on tape. Tape motion remains constant, so slowing the write circuitry down effectively reduces the bit density on the tape by a wide margin. This data cannot be recovered correctly on subsequent reads, so this procedure is only of benefit for analyzing behavior of the circuitry during a write operation.

(2) Checking the error counter, or counting frames per block–Depressing and holding the Parity indicator during a write operation will cause improper parity to be written on tape. This step causes the parity bit to be generated for every frame of data, regardless. A subsequent read would then encounter parity errors in those frames where the data bits are of odd parity, and the parity bit is set. This information may be used to check the error counter during a subsequent read operation because improper parity is detected on the improper parity frames. By making every frame odd parity during the write, the error counter can be made to show the total number of bytes read.

(3) Repeated manual operations–It is possible to write short blocks of data on tape, or to read these blocks again in either direction, at a rate controlled by the manipulation of the Operational Mode switch. This technique requires that bits governing the function desired be held set (or left clear) in the C register, while the Operational Mode switch is manipulated back and forth between Inspect EF and I/O Inact positions. These bits form the manual function code in the Inspect EF position, and also form the data in the I/O Inact position for a write operation. For a subsequent read operation, either forward or reverse, these bits form the manual function code in the Inspect EF position, and will include bits governing the previous write being set as data is read from tape in the I/O Inact position. The size of the blocks is determined by the length of time the switch is left in the I/O Inact position. Any subsequent read of these blocks will require that the entire block be accessed and the following IBG be entered. Basically, this means that repeated manual reads cannot be accomplished at a faster rate than was used during the write, although no limitation restricts the use of slower read rates if desired. The method by which one person can perform a write or forward read is to fan the fingers of either hand (normally the right) over the buttons of the C register to hold the necessary buttons of the C register depressed, while at the same time holding the REPLY button depressed with the thumb (the thumb has to be doubled back slightly if using the right hand). The other hand is then left free to manipulate the Operational Mode switch. The status indications are not affected by bits in the C register being held depressed. A problem occurs when an attempt is made to perform repeated manual reverse reads. C9, which controls reverse operations, is too far from the REPLY button for most individuals to reach both with one hand without straining. This makes it necessary for two hands to manipulate the C register and the REPLY button. Another person would then have to assist with the Operational Mode switch. One person can do this operation, but this necessitates grounding a testpoint in the chassis for the C9 flip-flop. It is usually more convenient just to have two people work together at this point.

(4) Manual erase operation (d.c. type erasure of tape)–A tape may be completely erased on the RD-243 in the following manner:

(a) Depress In Control, A or B

(b) Depress Write indicator on the Function Register. This will set a write

condition into a portion of the circuitry and enable the erase head. T2 is NOT pressed, so the rest of the write operation is inhibited. Once tape motion is initiated (next step), the erase head will erase the tape, but no data, sprockets, or parity bits will follow.

(c) On the transport control panel, depress SELECTED and FWD for the tape transport holding the reel of tape to be erased.

(d) Tape erasure will continue until tape motion is stopped, either by a STOP-CLEAR, MASTER CLEAR, or detection of EOT.

Special Read Techniques

Refer to step C under special write techniques above. Reading a series of short blocks continuously and/or checking the fast reversal characteristics of the transports may be done by depressing and holding Reply, bits C12 or C13 and C11 (if parity format). Direction is controlled by bit C9. After selecting I/O Inact with the Operation Mode switch, tape motion forward or reverse is controlled by bit C9 while holding the others constant. Parity errors are recorded by the Error Counter. Sync errors may be observed in the Status register. The Sync indicator lights briefly between successive blocks if sync errors are occurring.

Details of the manual operations previously described and many others may be found in the troubleshooting section of the appropriate technical manual. The procedures discussed are but a few of the many troubleshooting aids that are available to a good technician who will stop to think for a few minutes before starting to work.

ADJUSTMENTS AND ALIGNMENTS

The adjustments of a magnetic tape system are intended to achieve optimum performance of the system when used with available tapes, and while conforming to the standard tape format that has been adopted for the equipment and the system. The standard format involves the size of the IBGs, bit density, type of labels used, etc. There are many different indications that these adjustments may need to be performed: Status and/or program indications, poor start/stop time, no tape motion, tape reels "jitter" when stopped, tension arms not centered with no tape motion, a chattering noise from the pinch roller when tape is moving, etc. These are just a few of the ways that it is possible to tell if some adjustment is needed. An unusual note to the air suction sound (a low pitch instead of the normal high pitch, or a harsh vibrant sucking sound) would suggest that a tape loop is not properly formed in one of the vacuum chambers.

The possibility of needed repairs must always be considered, and careful watch must be maintained for telltale signs. A squeal, or rubbing sound might indicate a bad bearing. The sounds of a labored motor or the absence of a familiar sound might mean binding parts or blown fuses. A cool circuit or motor might mean loss of input power. Overheating can be detected by checking relative heat outputs from the same elements in similar equipment, and especially by smell if severe overheating or burning is evidenced. Skin touch, or measuring heat rise close to uncalloused skin is usually adequate for checking relative heats. Avoid directly touching any area that could be energized or that might be subjected to severe overheating until adequate safeguards have been taken. Secure power to equipment whenever possible, and approach area gingerly to check for sudden sharp rises in temperature. Have a qualified individual nearby to assist and to act as safety man in case of injury. Because of strong air circulation currents found in most installations, smoke is often not visible, and the apparent source of the heat may be quite a distance from the actual source. In this case, only by getting very close to the source can the sense of smell be completely trusted, or the forced air circulation system be momentarily secured. The smell of something overheating or burning should be reacted to instantly. Even though it may be difficult to pinpoint the source of a burn smell, the smell itself is usually the first clear indication of a major malfunction in some item of equipment. It is important to isolate the source before the smell becomes generalized to a large area.

The detail of how to make these adjustments and repairs is left to the appropriate technical manuals; only a brief discussion of the purpose for certain adjustments is made in this text. The terms that have become associated with the adjustments will also be explained.

Special Tools

All the adjustments for the RD-243 Tape Transports can be made with standard tools that should be available in any electronics maintenance shop (with the possible exception of the four spring scales). Because there has been some difficulty in obtaining these scales, the current Federal Stock Numbers are provided here.

	Mfg. part number	FSN
0 - 16 ounce scale	Chatillon No. 516-500	6635-717-1307
0 - 2 pounds	Chatillon No. 516-1000	6635-791-5915
0 - 20 pounds	Chatillon No. 719-20	6635-647-3371
0 - 50 pounds	Chatillon No. IN50	6670-675-4987

Check these stock numbers prior to ordering to ensure that they are still valid.

Terminology

An adjustment in computer terminology has been required with the growth of the data processing field. For example, the computer (through the medium of the MTU) writes a stream of 30-bit words onto a magnetic tape during a buffered output operation. These words are grouped on the tape with no separation between the last frame of one word and the first frame of the next. When the last word is written, the write operation stops, but the tape continues moving a short distance, which erases a small section of tape that follows the written frames of data.

Initially, these grouped frames of data, representing one or more computer words, were called a record, and the erased gap between the records was called an interrecord gap (IRG). Now because of a terminology change these groups of frames are referred to as a block, the gap as an IBG, and groups of blocks pertaining to the same subject as a record. Groupings of records become a file, and files are usually separated on magnetic tape by file marks (a single even-parity frame of data containing a 17_8 code not available with the RD-243).

Another example of a terminology change is write protect rings (also called file protect rings). These rings seat in the back of the supply tape reel in a transport such as the RD-243, and when installed, cause an interlock to prevent a write operation from occurring on that tape. The trouble is the rings sometimes fall out or are inadvertently removed, allowing write operations to occur on saved tapes, which erase the previous contents. A technological change now requires most tape mechanisms (the RD-243 is an exception) to have a ring installed before a write operation can occur—no ring means no write. Rings for these transports are identified as write rings.

The combined Start/Stop distance of a transport determines the size of the IRG during a write operation, and permits the transport to hesitate between blocks with the option of moving in either direction during a read operation. The Stop/Start distance is a function of the Start/Stop times, which must be adjusted and measured properly in order to achieve proper transport operation.

The instrument used in measuring Start/Stop times is the oscilloscope, and an oscillator (usually a built-in feature of most MTUs) is used to generate a repetitive sequence that can be viewed on the crt. The oscillator output is fed into the motion controls of the transport (FWD or REV) and to the Trigger input circuit (Sync circuit) of the oscilloscope. The trace shown on the cathode-ray tube (crt) is taken from a read amplifier circuit of one of the tracks of the read/write head (a two head transport) or the read head (a three head transport).

The crt will show one of two displays, the Start time or the Stop time (figure 5-15),

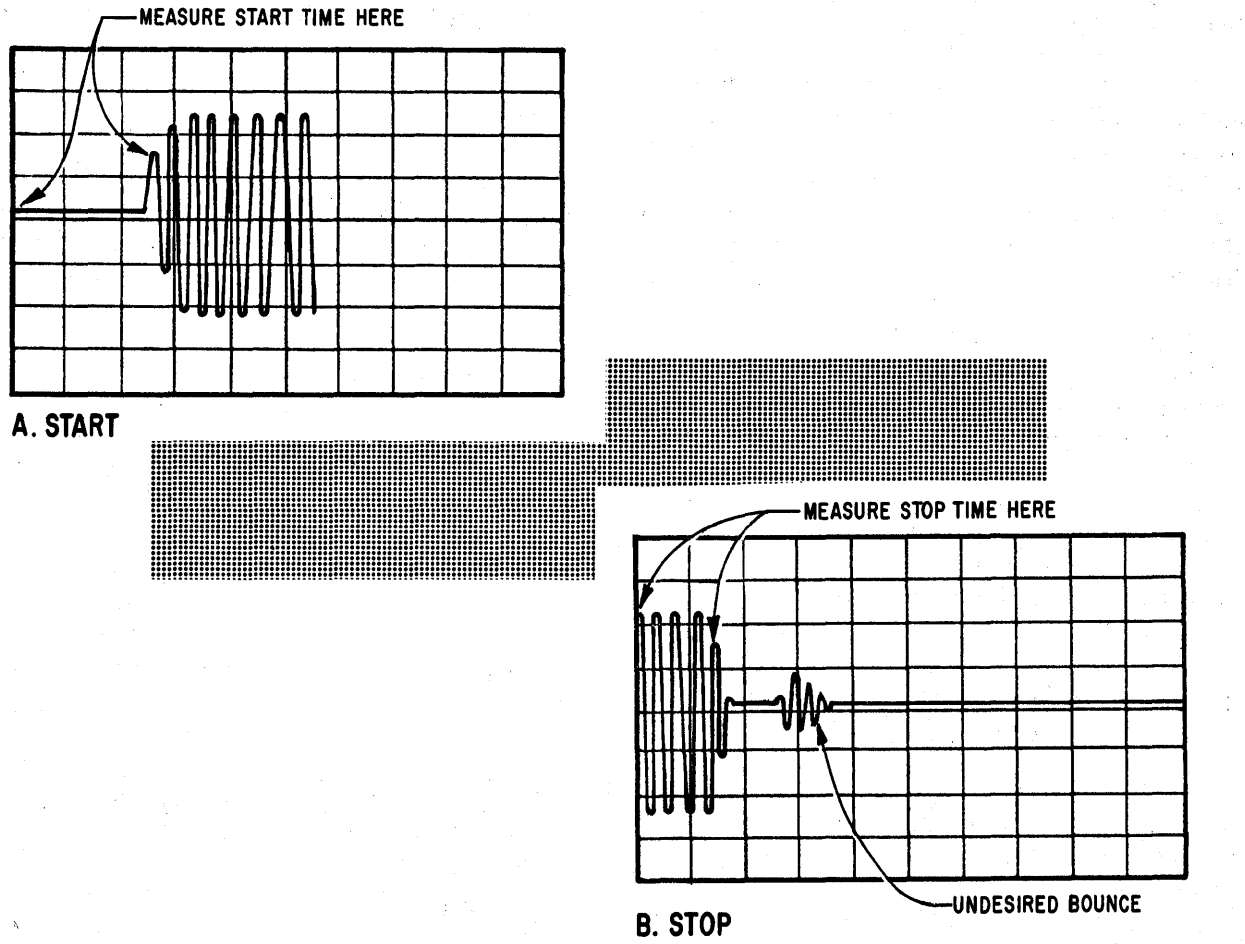


Figure 5-15.—Start/stop time waveforms.

depending upon the synchronization of the oscilloscope, which is done using the + or - Slope adjustment. Actual measurement is made between the time the circuit is told to start (or stop) the tape motion, which is also the sync input, and the time the tape motion actually starts (or stops). The trace shows the data received through the head during periods of tape motion. This measurement is the physical time it takes the transport to respond to commands from its motion control circuits, and these must be adjusted mechanically. The centimeter grid on the face of the crt and the TIME/CM switch setting determine the time interval being measured. For the RD-243, the Start time should be set at 1.8 ±0.1 ms; Stop time should be 1.2 ±0.1 ms. The oscillator in the MTC logic is variable, and can be connected by jumper wires to other test points. An output of at least 10 Hz is necessary in order to build a useful display on the crt. The highest frequency output of the oscillator circuit should be limited by the maximum variations the tape mechanics can withstand before problems are likely to result.

In order to receive a useful output from the read head when making these adjustments, a tape with all 1's data and no IBGs is required. Because mechanical adjustments that may severely affect the tape in use are in progress during the setting of stop-start time, it is strongly recommended that a tape be used that is judged unsuitable for any other function ("mechanics" tape).

Bias

As with other circuit types, transistor circuits can be thought of as requiring two distinct voltage level inputs for proper operation: the operational voltage level, which controls behavior of components in the circuit itself, and the input or "trigger" voltage level, which must alter the circuit function. To some extent, these two voltage levels are interdependent, and both have a certain tolerance range. This means that as long as the voltages do not exceed the limits of that range, the circuit should function as intended. A bias is a means of adjusting the voltage threshold at which the circuit will be "triggered" by an input voltage. The trigger bias adjustments in the RD-243 determine the sensitivity of the read circuitry in reading data from tape: too sensitive, and background noise on the tape may be picked up; not sensitive enough, and some of the data may be lost. The bias adjustments for the marginal test levels are used to set the high and low marginal voltages. (Chapter 2 discussed marginal testing and its use in locating "aging" components.) If improperly set, the marginal test will not reliably indicate potential problem areas.

Time Delay

There are five time delays associated with the RD-243: Read, Reversal, Stop, Erase, and Write. These delays are used to insure that the respective section of tape is positioned over the read/write and erase heads at the correct point in time for the intended operation.

Drag Pad

The drag pad adjustments are set to provide eight to nine ounces of pressure on the tape as it is moving across the read/write heads. The purpose of the drag pads is to provide braking force to the tape to stop it quickly when the pinch rollers deenergize. The drag pads are always in contact with the loaded tape and interact slightly with pinch roller measurements, and with each other (one drag pad acts primarily as a FWD brake while the second serves as the REV brake). Figure 5-6 illustrates the position of the drag pads with the read/write head door open.

Bridge Rollers

These adjustments are used to obtain proper tracking of the tape through the bridge roller assemblies and to or from the tape reels. The bridge roller assembly locations are shown in figure 5-6.

EOT/BOT Sensors

These adjustments set the levels required to cause an output from the EOT/BOT amplifiers and stop tape motion.

Dashpots

These are adjusted to ensure that the tension arms strike each stop gently, but still move rapidly without any hesitation. The dashpots prevent tension arm damage and untracking of the tension arm cable if the tape breaks or the tape load handle is released improperly.

Reel Brakes

The reel brake adjustment checks the drag produced by the reel brakes to stop the tape reels when power is interrupted. This prevents tape spill by the feed reel and tape breakage by the other reel if the tape was moving when power was lost.

Vacuum Buffer Chamber

There is an adjustment screw for each of the four small circular ports in the vacuum chamber. The adjustment of these screws is a critical factory adjustment, and they are to be altered only by factory personnel. There are several conditions that could adversely affect the formation of the proper tape loops in the vacuum chamber. Some of these are: dirty buffer area, air leakage caused by a loose divider located between the vacuum buffer chambers, or a bad vacuum blower motor.

Mechanical Head Skew

Checks of head alignment would occur at this point if required. Normally, head alignment will only change if the head has been replaced. While the equipment technical manual is more precise about how a specific head adjustment is to be accomplished, there are some general rules to be followed. First of all, as with any object, the head exists on three axes simultaneously. These can be labeled top-to-bottom, left-to-right, and front-to-back. There are two measurements associated with each axis. One is the distance the head lies along that axis. The second is the angle of tilt the head has along that axis. For instance, the head has to be a certain distance out from the transport surface. This is distance along the front-to-back axis.

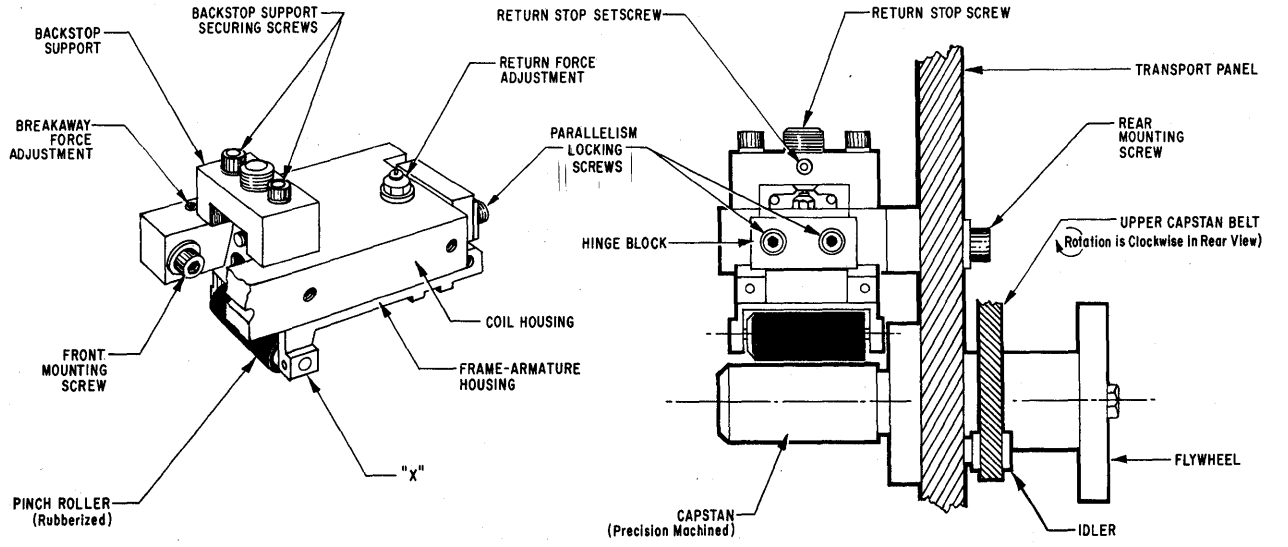
The degree of tilt is supposed to be 0° from the perpendicular (or 90° ±0°) to be exactly skewed on that axis. This particular adjustment is normally done with shims (bits of metal inserted as spacers). Changing this adjustment could very easily affect either or both of the other two axes, causing the head to sit too high or low, too far left or right, or even to tilt slightly clockwise or counterclockwise. Changing the alignment on one axis means carefully checking all three axes to insure they are within the tolerances specified. Be sure to follow the procedure given in the technical manual when replacing or adjusting a head.

Pinch Roller Checks and Adjustments

Adjustment of the pinch roller solenoid assembly (fig. 5-16) is divided into five procedures: skew, return force, parallelism, drive force and capstan clearance. Each of these procedures has its own set of checks and adjustments.

SKEW.—Skew refers to the angle at which tape passes over the read/write head. "Perfect" skew (i.e., 0° skew, or a non-skew condition) is such that the parallel lines of the tape edges are perpendicular to a line across and parallel with the read/write segments of the head. The angle with which the pinch rollers contact the capstans (tape moves between the pinch roller and the capstan) will affect the tape motion and skew.

Watch the tape as it travels to a pinch roller from the tape troughs on the tape head assembly; a buckling of one edge may be



124.444

Figure 5-16.—Pinch roller solenoid assembly (Upper assembly shown).

noticed. Check for severely out of round pinch rollers when tape is moving by listening for an audible clattering sound. Out of round pinch rollers may also be detected by adjusting the pinch roller to make positive contact with the capstan and manually turning the pinch roller to determine if uniform resistance is felt at all points. Check for a visible groove (in the pinch roller) the width of the tape. Look for grooved or marked capstans. Check for a wobbling action (vertical end play) by rapidly energizing and deenergizing the pinch rollers. Check for loose or worn capstan belts. Use a machinist's square to determine if the pinch roller is square with the drive plate.

RETURN FORCE.—Return force is a measurement of the pinch roller's ability to quickly move away from the tape when the pinch roller solenoid is deenergized. If the force is too weak, movement away from the tape may be slow and cause unwanted tape movement and result in a slow stop time. If the force is too strong, it will work against the solenoid driving force and decrease its effectiveness (this could affect start time). The return force is checked at point X of figure 5-16 and should be between 13 and 15 ounces. Parallelism may be affected by this adjustment.

PARALLELISM.—This refers to the relationship between the pinch roller and the capstan; proper operation requires them to be as perfectly parallel to each other as possible. Clearance between the pinch roller and the capstan should be the same at both ends of the pinch roller. Deviation, which is the amount by which parallelism is off, should not exceed 0.001 inch. Recheck the return force after this adjustment is made.

DRIVE FORCE.—Drive force is the actual pressure that the pinch roller exerts on the tape to move tape between the pinch roller and the capstan. Drive force is used to overcome return force when the solenoid is activated and the pinch roller is brought into contact with the tape. Drive force is, therefore, stronger than return force, but must be measured as the difference of the drive force and the return force. In addition, drive force varies in strength directly with the distance the pinch roller moves. The farther the pinch roller moves towards the tape, the stronger the drive force as a result of increased proximity of the magnetic fields in the solenoid. When properly positioned, the drive force will register between 7-9 pounds when the solenoid is energized and the pinch roller is in contact with the tape. This is verified by using a spring scale to attempt to pull an energized pinch roller away from tape and stop tape movement. The attempt is to make the pinch roller just barely "break away" from the tape, and as a result, the drive force measurement is also known as the breakaway force measurement. Point "X" in figure 5-16 is used for measuring breakaway force.

PINCH ROLLER TO CAPSTAN CLEARANCE.—This adjustment affects the start time of the tape, and the amount of drive force exerted on the tape. If the deenergized position of the pinch roller is too far from the capstan, start time will be slow because of excessive travel of the pinch roller while energizing the pinch roller solenoid. This slowness will cause the electronic delays to lapse too soon, before tape is up to speed. In addition, the increased gap will result in too much pressure on the tape, which can stretch tape, wear down the pinch roller surface, and cause the pinch roller bearings to go bad. If the pinch roller is too close to the capstan, excessively fast start time may cause premature movement of tape. This will increase the IBG, or the lesser tape pressure may cause tape slippage. The pinch roller to capstan clearance should be 0.006 ±0.001 inch.

Electrical Head Skew

Another form of misalignment could be caused by minor variations between channels on a head as a result of slightly imprecise machining, wear, and other factors. Delay lines can retard the faster channels to synchronize them with the slower ones. This is called electrical deskewing (or just electrical skew). To check mechanical skew with an oscilloscope, electrical skew should be "reskewed" or nullified (reduced to zero effect), and a tape read that possesses good frame alignment.

Normally, this would be a skew tape, but skew tapes are not available for the RD-243. A compromise is necessary at this point, and usually this means that one transport is selected to generate a "ls" tape, which will be used by all the transports in the system as if it were a skew tape. Selecting the best transport should be based on judgment gained from working with these particular transports. It can be verified by writing a "ls" tape on each transport and reading each tape in turn on each transport, then selecting the tape that shows up the best on the most transports. The tapes when written require the transports to be electrically skewed. When read, the transports should be electrically reskewed (have the electrical skew nullified). Electrical deskewing should then proceed from the worst drive up to the best drive.

Admittedly, there is a great deal of work and effort involved here. The alternative to not making the effort is to not establish a compatibility standard within the system, then to always be faced with tapes that can only be read on certain drives, older tapes that can no longer be read by the system, and uncertainty as to whether new tapes will be readable in the future.

The RD-243, with one d.c. erase head and one 8-track read/write head, cannot have its write circuits electrically skewed separately. It does not have the data that would be picked up by a separate read head with which it could monitor a write operation (read-after-write function). If a transport's read circuits are skewed to a system compatibility standard, and compatibility is lost between the transport's read and write functions in the process, then that transport should be restricted to read operations only until the situation is verified. A head replacement might eventually be required if the problem appears to be in that area. By restricting this transport to "read only" operations, it will not be responsible for incompatible tapes being introduced into the system. The RD-243 is also a low density machine. Some transports must be able to read or write densities as high as several thousand BPI (bits per inch). The RD-243, with either 130 or 210 BPI, does not have especially critical skew requirements. In other words, some degree of compatibility should always be present. At some point, sufficient compatibility will be obtained within a system to make further extensive effort unnecessary. If a proper foundation has been established, maintaining system compatibility will be comparatively easy from that point on. The transport initially selected for the simulated skew tape should make two all ls tapes. One would be a system ls tape by which all transports in the system would be adjusted. The second would be a standard ls tape, which is held in reserve. When the system ls tape appears to have aged beyond desirable limits, a transport would be reskewed, using the standard ls tape. It would review ls tapes written by each transport in the system. The best ls tape would be selected as the new system ls tape. More than one standard ls tape and/or systems ls tape can be created and maintained if desired. None of these tapes should be labeled as a skew tape, since none of them will actually have sufficient control in their production to be that exact.

Changes will continue to creep into the system, but some changes counteract each other, while others can be slowed or prevented from being as extreme in their effects. A program of preventive maintenance scheduling that staggers the periods when each transport is skewed so that only one is done at a time will not cause serious consequences. Doing them all simultaneously may result in total loss of compatibility with older tapes. If it becomes apparent under normal usage that one drive cannot read certain tapes, steps can be taken to correct the situation. On the other hand, if none of the drives can read certain tapes (and this is more likely to occur if they are all reskewed at about the same time), there is very little that can be effectively done to correct the situation.

Tape Transport Cleaning

The technical manual recommends that the transports be cleaned every eight hours of operation. Experience with system transports indicates that more frequent cleaning may be required, depending upon demands on the equipment and conditions of the tapes.

One indication that the tape transports may need cleaning is the Parity error display on the front panel. If Parity errors occur, clean the

transports before troubleshooting for logic or mechanical malfunctions.

Maintenance Programs

In most systems, maintenance programs are stored on magnetic tape. This is particularly true in NTDS, where the only alternate way of loading programs is through the painstaking task of reading them from paper or Mylar tape on the OJ-172(V)/UYK I/O console, the RD-231A/USQ-20(V) or through the paper tape reader in the teletypewriter. In NTDS, maintenance programs are maintained on one tape (or set of tapes), while the system operating programs (OP programs) are maintained elsewhere. A library of master maintenance tapes should always be kept separate from working copies of the maintenance tapes. This will insure that a usable copy of the maintenance programs are available to be reproduced if a working copy is inadvertently damaged.

Maintenance programs are discussed in detail in chapter 4 of *DS 3 & 2, Vol. 2.* However, since magnetic tape is the storage medium, it might be best to cover the sequence required to obtain a specific program and load it into the computer in the NTDS system while the concepts of magnetic tape storage are still fresh in your mind.

The following steps establish a basic procedure for either a system or a maintenance program from magnetic tape:

(1) perform computer's RD-243 bootstrap. This loads the first block of data found on the tape mounted on transport #1 (either normal or reverse).

(2) upon successful load of the first block of data (which is the utility program), control is transferred automatically from the bootstrap program to the utility program.

(3) manually insert required parameters into the utility program (via the computer's front panel or the system monitoring panel) to designate which utility function is to be employed and in what manner.

One of the utility program's functions is the ability to call other programs from the same tape by use of a "call number." The call number corresponds to the position the program occupies on the tape with respect to the utility program. Call number 1 is the next program. Call number 12 is eleven programs beyond call number 1. In this manner any number of programs can exist on one tape and be available to the operators or maintenance personnel. Documentation should give the parameters, functions, and call number of each program available within a system. Some programs are designed to exist in the computer memory alongside the utility program. This permits use of the utility program again when the next program is wanted. Some programs overload the utility program and do not contain the ability to call other programs themselves. It would be necessary to rebootstrap the computer to obtain other programs when this occurs. See chapter 4 of *DS 3 & 2, Vol. 2,* for additional information on programs.

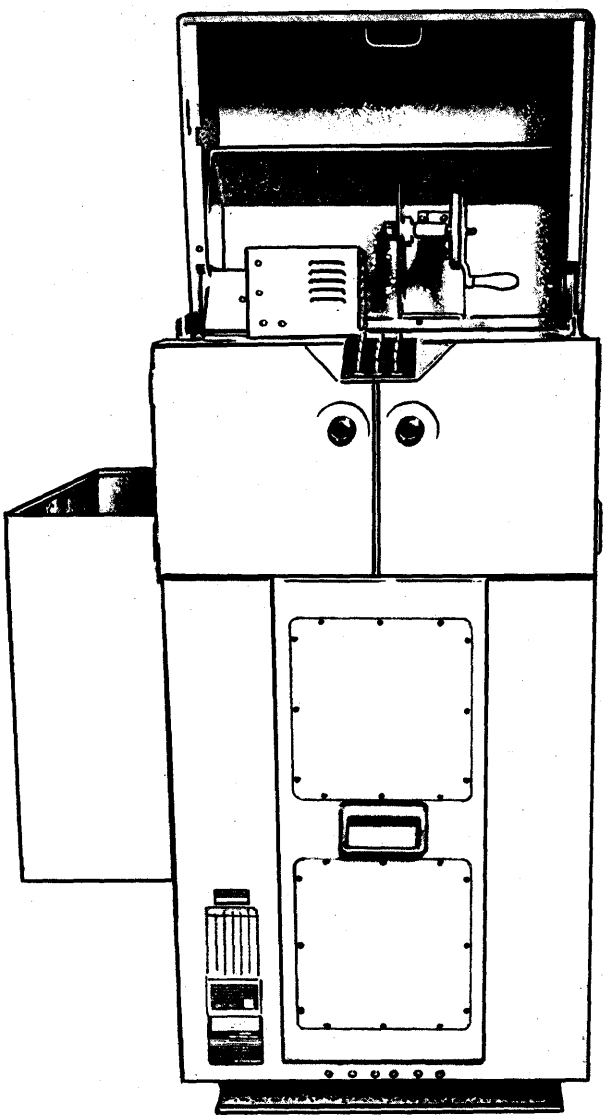
RD-231A/USQ-20(V) PAPER TAPE UNIT

The RD-231A Paper Tape Unit (PTU) shown in figure 5-17 is used in a computer system as a peripheral device for reading or punching information for a computer. It may also be used offline as a tape duplicating device. The computer data is stored by punching holes into a ribbon of tape. The photoelectric reader is connected to the computer by one normal input cable and is adapted to function as an input device. The high speed punch (HSP) is adapted to function as an output device.

The PTU is connected to one normal computer output cable which carries punch data and external function codes and one normal computer input cable which carries reader data. In a multicomputer installation, the PTU cables are connected to manual switches to facilitate switching the PTU between computers.

Data transfer between computer and PTU takes place in the buffer mode with one frame (seven bits) being transferred during each buffer operation.

These seven bits occupy the lower portion of the computer I/O word. For more efficient use of a computer's memory, a software program would normally be required to assemble and disassemble PTU frame data during I/O operations. For example, a 30-bit computer



124.215

Figure 5-17.—RD-231A/USQ-20(V) Paper Tape Unit.

would have five six-bit bytes of data per 30-bit word:

Byte 1	Byte 2	Byte 3	Byte 4	Byte 5

30-bit computer word

The program would have to break this format down into five separate I/O words with the byte data in the lower 6 bits, and add an odd parity bit (P) in the 2^6 position (paper tape's seventh level position) in order for each byte to become an odd parity frame on tape:

	Upper 23 bits	Lower 7 bits
Word 1:	Ignored	P Byte 1
Word 2:	Ignored	P Byte 2
Word 3:	Ignored	P Byte 3
Word 4:	Ignored	P Byte 4
Word 5:	Ignored	P Byte 5

30-bit I/O word format

The PTU would only accept the lower 7 bits, and from these five words, would punch the following frames of data:

Frame 1:	P Byte 1
Frame 2:	P Byte 2
Frame 3:	P Byte 3
Frame 4:	P Byte 4
Frame 5:	P Byte 5

7 bits

When reading a tape that had been punched in this format, the computer would have to read a frame of tape and check for odd parity five times, then assemble those five bytes that have been recovered back into a single 30-bit word. The usual practice is to use the A, Q, and AQ left and/or right shift instructions when breaking the word down into bytes, or when assembling a word from bytes. Refer to table 4-2 concerning shift instructions for the CP-642B computer, or to NAVEDTRA 10088 (series), ***Digital Computer Basics,*** for shift instructions for the CP-789 computer. The punch and reader circuits for the PTU are independent of each other, and read and punch operations can be done simultaneously.

The reader can be seen (fig. 5-17) protruding through the top of the cabinet on the left-hand side. The tape guide mechanism of the reader is level with the top plate of the cabinet. The door below and directly in front of the reading station provides access to a tape reel holder. A punched tape is inserted in the reel holder which positions the tape for threading through the reader. The reel holder is mounted on a sliding track. When the track is extended outward, a tape reel placed on the axle of the holder will be in the correct position for feeding into the reader. Tape is advanced through the reader from the front to the back of the cabinet. After having been read, the tape spills into a receptacle provided at the left side of the cabinet.

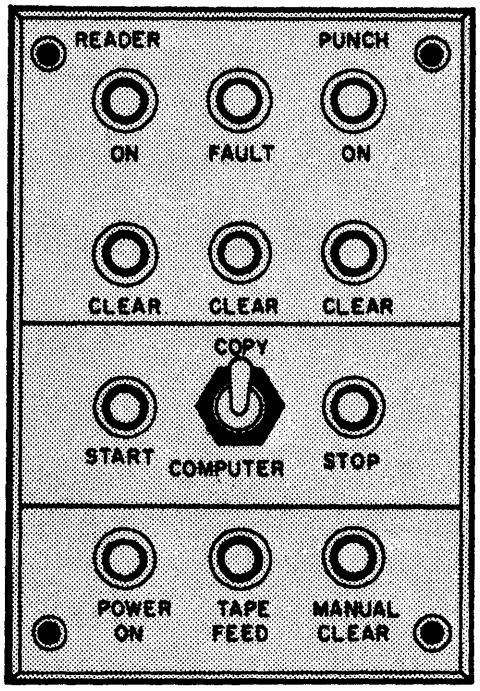
The high speed punch (HSP) unit is located in the right-hand section of the cabinet behind the door. The punch unit is mounted on a sliding track that may be extended outward to allow maintenance. The blank tape used by the punch is stored in a reel holder attached to the punch frame. A pully arrangement guides the movement of the tape from the supply reel to the punching station. From the punching station, the punched tape passes through a steel conduit and empties into the receptacle at the side of the cabinet.

FRONT PANEL CONTROLS

The operating controls (fig. 5-18) are located on a descending slope of the cabinet face and are made up of switch indicators and one toggle switch. The Reader On, Punch On and their associated Clear pushbuttons act as on-off controls for the reader and punch. The Fault indicator is lighted only by command from the computer (indicates Reader-to-Computer error). The associated Clear button is used to clear the Fault indicator.

The Computer-Copy toggle switch and the Start and Stop buttons are used in offline operation. In the offline mode, a tape is placed in the reader, and the toggle switch is set to Copy. Then the Start button is depressed, and the punch unit copies the information from the reader. The Stop button is used to stop the copy operation.

The Power On indicator is lighted when power is applied to the PTU. The power switch is located directly behind the control panel on top of the cabinet. The Tape Feed switch is used



124.445

Figure 5-18.—PTU front panel controls.

to feed blank tape from the punch (make a leader). The Manual Clear switch is used to master clear all operations.

OPERATIONAL CHARACTERISTICS

The PTU is capable of utilizing paper tape in 5/8, 7/8, or 1 inch widths. These widths correspond to 5-, 7-, or 8-level tapes. In NTDS, all the paper tapes are of the 7-level 7/8 inch type or 5-level 5/8 inch TTY tape. This seven level tape is illustrated in figure 5-19. A frame of tape is made up of the holes in a line across the tape. Tape levels are parallel to the tape edge. The tiny holes labeled FH are the feed holes (10 per inch) which appear once per frame, and are used to pull the tape through the punch. They are also used for frame timing in the tape reader. A seven level tape contains two octal digits (bioctal) with one level extra. This utility level may be used for parity or control information, as desired. If used for parity information, the seventh level provides a means of distinguishing zero data frames from blank (no data) frames. The leader portion of the paper tape would normally be composed of blank frames, which when read into the

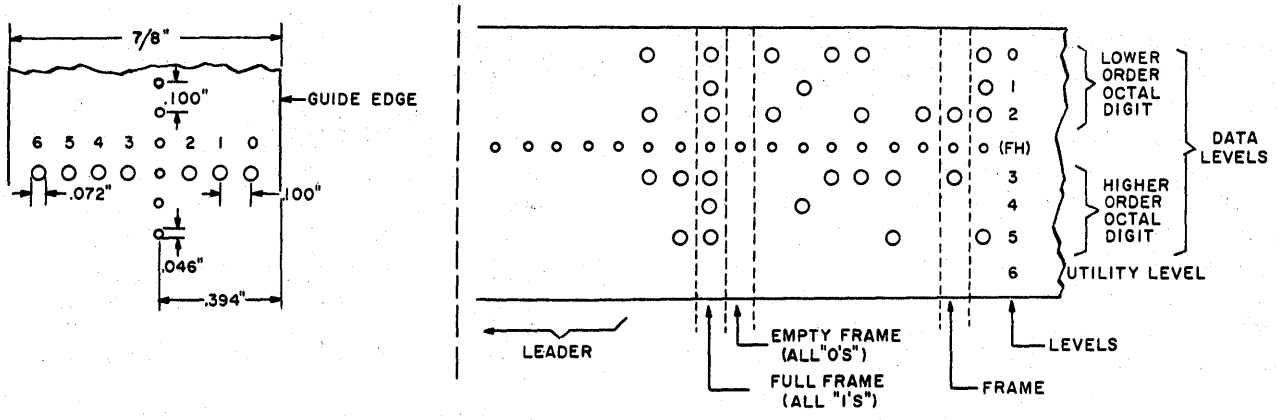


Figure 5-19.—Seven level punched tape. 164.48

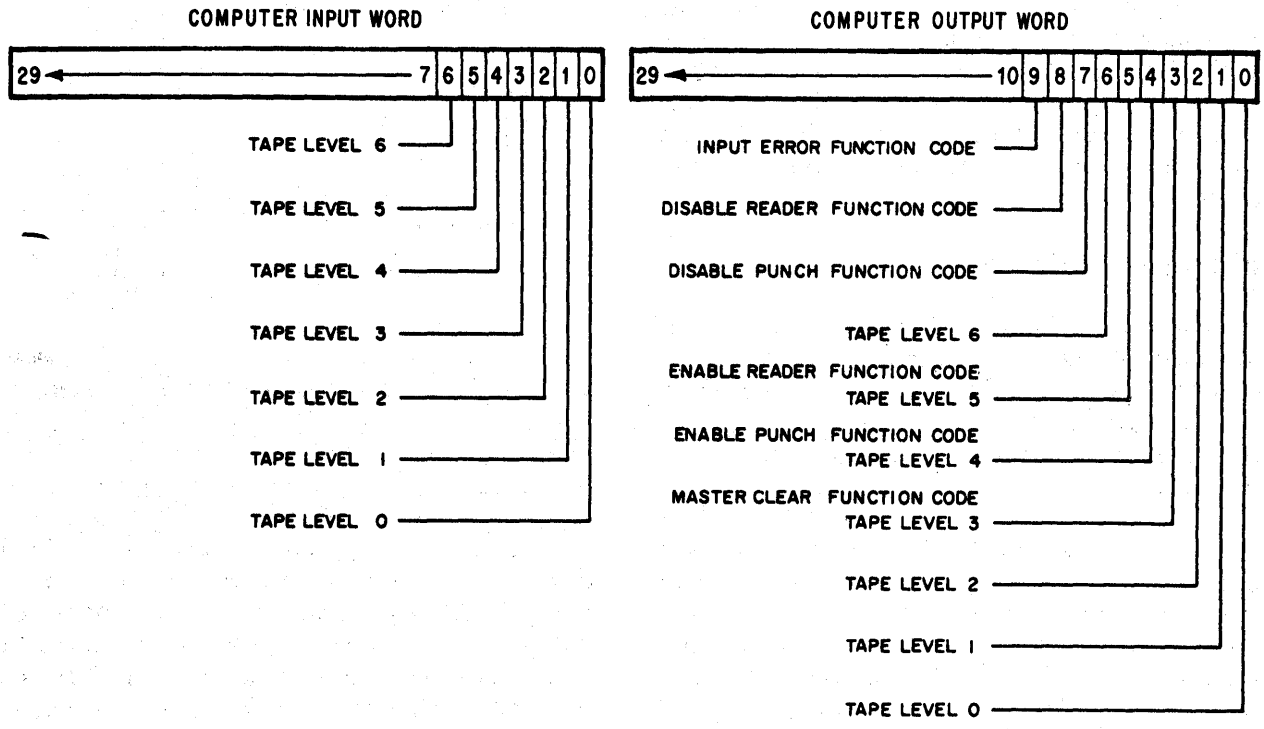


Figure 5-20.—PTU word format. 124.446

computer (or written by the computer) would be $\emptyset\ \emptyset\emptyset\emptyset\ \emptyset\emptyset\emptyset_2$ in positions 2^6 through 2^0 of the input (or output) word. If odd parity data were contained in the frame, the computer would read (or write) $1\ \emptyset\emptyset\emptyset\ \emptyset\emptyset\emptyset_2$ for zeros data in that frame, where the 1 would be the parity bit. The position of each frame is marked by the presence of a feed hole, since this is an automatic function of the punch feed cycle. If a section of tape does not contain feed holes, or if the FH circuity malfunctions or the photolamp is out for any reason, it would be as if the entire width of tape were blank and no data levels existed on the tape as far as the reader circuitry is concerned. Tape movement would be continuous until either a feed hold were sensed, or tape had been completely run out of the reader.

The use of a parity bit, or some other form of redundancy to verify punched tape data, is considered essential in most applications. The

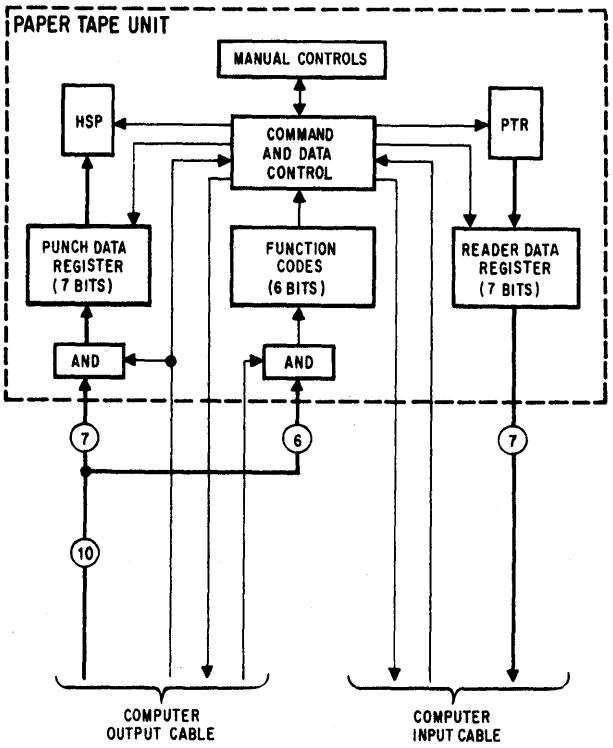
addition of verifying data must be a software function, since neither the punch station nor the reading station has the physical capabilities of performing this fucntion itself. Punched data is normally verified by having the completed tape inserted into the reading station and read back into the computer, where the inputted data can be checked frame by frame against the data just outputted. Once a tape has been verified as being punched properly, the verifying data that was inserted into the tape format by the punch program can be used to verify a proper read of the tape when performed by other programs.

The computer communicates with the PTU by external function words and data words. The formats for these words are shown in figure 5-20. Note that data (input/output) is contained only in the lower seven bit positions. This corresponds to the tape levels. The computer output word also is used to carry the external function commands.

BLOCK DIAGRAMS

The block diagram for the RD-231 is illustrated in figure 5-21. When the computer desires to begin an operation, it must select the desired equipment (reader or punch) by use of the external function codes to gate the information to or from the PTU.

The photoelectric reader (fig. 5-22) detects each level of the tape by means of eight photocells mounted beneath the tape. Each photocell responds to light from the single lamp mounted above the tape if a hole exists in its corresponding level. One of these photocells is used to detect the feed holes (one for each frame) which are used to synchronize reading of the other levels in that frame. By using a smaller hole for the feed hole, the reader is able to read tapes correctly despite minor problems that may affect skewing of the holes in each frame. The smaller feed hole also reduces the intensity of the detected light for the feed holes, and a dim or dirty lamp will be evidenced by failure to detect frames (no timing pulse) before a point will be reached where data loss from any of the other photocells is likely to occur. Once a frame of data is read from the tape, the reader logic then

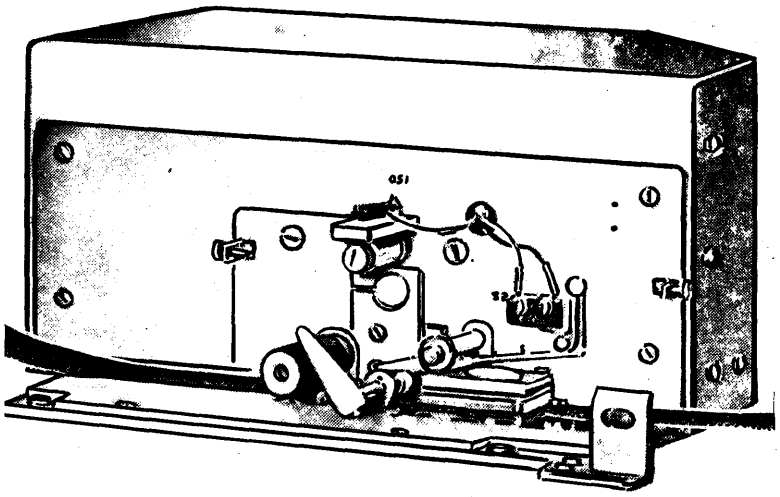


124.447

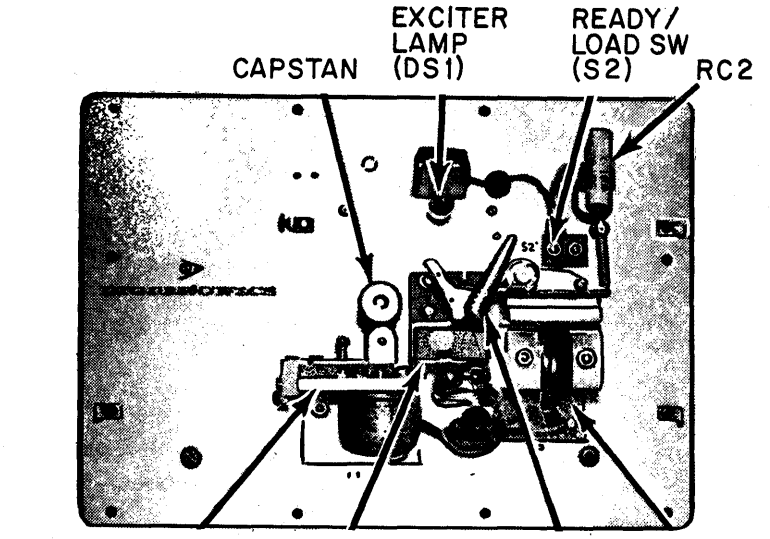
Figure 5-21.—PTU functional block diagram.

transmits the information found punched in the tape to the computer. This transfer is done via the reader data register, and the transfer is done one frame at a time. An Input Data Request (IDR) is generated by the command and data control section for each frame sent to the computer. The computer accepts the information as a 30-bit word, with the upper bits that are not in use appearing as zeros. An Input Acknowledge from the computer informs the control section when the frame has been accepted.

The HSP receives data from the computer via its data register. It converts the data signals received into the mechanical energy needed to punch a corresponding pattern of holes into one frame on the tape. An Output Data Request (ODR) is then generated by the control section to inform the computer that the punch is ready to accept another transmission.



A. DIGITRONICS READER WITH READER MECHANISM DUST COVER REMOVED



B. DIGITRONICS READER WITH TAPE GUIDE PLATE REMOVED

124.448

Figure 5-22.—Digitronics Photoelectric reader.

The control panel is used to indicate the status of operations, and when desired allow manual control of these operations.

DIGITRONICS PHOTOELECTRIC READER

The photoelectric reader unit is made up of a tape feed mechanism, an optical projection system, a light-sensitive reading device, and a transistor amplifier section. The photoelectric reader unit is capable of reading 240 frames per second.

The function of the reader, as a unit, is to sense the information contained on a punched tape and to present this information in the form of electrical signals to the logic portion of the paper tape unit. To perform this function, the reader is provided with a tape feed mechanism which moves the tape past the reading station (composed of the optical projection system and the light-sensitive reading device). When a frame of information is moved into the reading station, the light generated by the optical projection system passes through the holes punched in the tape. The light passing through the punched holes activates the photodiodes that are directly below the tape. The photodiodes which make up the light-sensitive reading device, generate an electrical signal which is amplified by the transistor amplifier section and sent to the logic circuits.

Reading Station

The reading station is designed to read punched frames of data from either paper tape or opaque Mylar plastic tapes. It will then either make the information read from the tape available for computer input, if in the COMPUTER mode (i.e., configured to communicate with a computer); or the reading station can make read data available to the punch station for copying tapes, when in the COPY mode. The reading station consists of the optical projection system and the light-sensitive reading device.

The tape used with the reading station can be either 5-level or 7-level tape. Each level refers to the number of data levels that can be used with the tape. For instance, a 5-level tape means that each frame can consist of data bits 2^0 through 2^4 (plus the feed hole level). Each level also refers to the width of the tape, where each level represents 1/8 inch. For this reason the 5-level tape is 5/8 inch wide, and a 7-level tape is 7/8 inch wide.

The number of tape levels used does not have to be the maximum allowed for the tape width. The standard tape available for use with the RD-231A PTU is 7/8 inch paper tape. This tape can be used for 5, 6, or 7 levels. The RD-231A contains a 5-LEVEL/7-LEVEL selector switch on the top which determines which level will be accepted by the reader. Another method used to limit the number of data levels in use on a paper tape is the software features of the program used with the RD-231A. If a data level is not to be used during a read operation, the program should ignore the corresponding data bit in the received data word. If a data bit is not to be used during the punch operation, the corresponding data bit of the computer word must always be zero. For those data bits that have no corresponding data level on the tape (2^8-2^{29}), any ONEs data is ignored during a punch operation, and these bits are read back as all ZEROs during a read operation.

Use of fewer than five levels of data is technically feasible, but usually undesirable, since this would require increased tape length to retain the same volume of information. Five levels were standardized years ago for the teletype systems, and the retention of 5-level capability in the RD-231A permits continued compatability with this standard. Six-level tape can be used for bioctal code or TTY code with a parity bit and 7-level tape can be used for bioctal code with a parity bit or ASCII code.

The most commonly used tape format is bioctal 7-level tape. The bioctal data appears in the lower or rightmost six bits and the seventh level can be used as a "utility" bit. Depending upon the program involved, the utility level can be designated for use as a marker to indicate which frame contains the upper six bits of a new data word. It can be used as a parity bit to maintain odd parity for each level, or it can be used in whatever other manner is desired by the programmer.

In addition to the data levels on the tape, there is also a feed hole level that always appears between data levels 2^2 and 2^3. The feed hole level occurs once per frame of data, and is smaller than the hole used for a data level. One additional photocell is required to detect the feed holes, and this provides the timing that is used

when each frame of data is read. A space for the feed hole is achieved by allowing only 1/10 inch of width on the tape for the actual data level, instead of using the 1/8 inch width that would be indicated by the tape width. This allows enough additional space for a feed hole in each data frame.

The photoelectric reader reads the content of one frame of data from the tape at the command of the computer. The Input Acknowledge signal from the computer allows the reader to advance the tape to the next frame of data and to read its contents. The tape is positioned by a capstan/pinch roller mechanism and brake mechanism. The tape feed flip-flop on the logic chassis controls the operation of the pinch roller solenoid and the brake solenoid. When the tape feed flip-flop is set, the pinch roller solenoid relay puller is energized. When the tape feed flip-flop is clear, the brake solenoid relay puller is energized. The capstan drive motor is energized whenever power is applied to the paper tape reader and a reader enable external function word is sent by the associated computer. In normal operation, the commands from the computer to read the next frame usually follows so closely behind the deactivation of the pinch roller solenoid that the solenoid does not have sufficient time to deenergize. The result is that during input operations with its associated computer (usually, but not always, involving a multi-address buffer), the tape moves continuously through the reader. Otherwise, movement would be marked by starts and stops which is what occurs when the paper tape unit is in the COPY mode of operation. This happens because the punch operates at 60 frames per second.

As long as primary power is applied to the paper tape unit, the incandescent lamp in the photoelectric reader is on. The capsan motor, however, which turns the tape drive capstan, is not started until the reader is selected, either manually or by the computer, as an input device. When the tape to be read is threaded into the reader, any portion of the tape leader may be positioned over the reading station. Selection of the reader starts the drive motor, and the tape moves forward automatically until a feed hole is encountered. The presence of light sensed by the feed hole photodiode activates the tape feed control circuit to stop the tape. The tape comes to rest with the feed hole and data holes (if the frame is not empty) positioned directly over the photodiodes unless a subsequent request for another frame of data is present.

Tape Feed Mechanism

The reader tape feed mechanism is composed of the pinch roller assembly, the tape guide assembly, and the brake assembly. The pinch roller assembly drawing (figure 5-23A) shows an exploded view of the pinch roller assembly. When the tape feed flip-flop is set in the control logic, a logic LOW from the clear side of the tape feed flip-flop is inverted and sent as a HIGH to activate the relay puller card, which in turn activates the pinch roller solenoid. The pinch roller clamps the paper tape to the rotating capstan and moves the tape forward. As soon as a feed hole is sensed by the photodiode read assembly, a logic signal is transmitted via two delay lines to the clear side of the tape feed flip-flop. When the tape feed flip-flop is cleared, a logic HIGH from the clear side of the tape feed flip-flop is inverted and is transmitted as a LOW to the pinch roller solenoid relay puller, which causes the deactivation of the pinch roller solenoid. At the same time as a LOW is sent to the relay puller card for the pinch roller solenoid, a HIGH is sent to the brake assembly solenoid relay puller which energizes the brake (fig. 5-23B). This stops forward tape motion with the tape lined up in the tape reading station. The tape feed flip-flop controls both the brake solenoid and the pinch roller solenoid so that only one of these solenoids can be activated at a time. As mentioned previously, during normal operation the tape moves through the tape-feed mechanism at such a rapid speed that it is in continuous motion from the start to the end of the tape. The tape guide assembly provides a means of adjusting the width of the tape path for various sizes of paper tapes. It contains a switch (READY/LOAD SWITCH-S2) (fig. 5-22), which disables the pinch roller solenoid relay puller when the tape guide is not set to the READY position. This keeps tape from being inadvertently read when the tape guide is not properly closed.

When data read from this frame of tape is sent to the associated computer, the computer sends an Input Acknowledge signal back to the paper tape unit to indicate that it has read the data. The IA through the reader control circuits

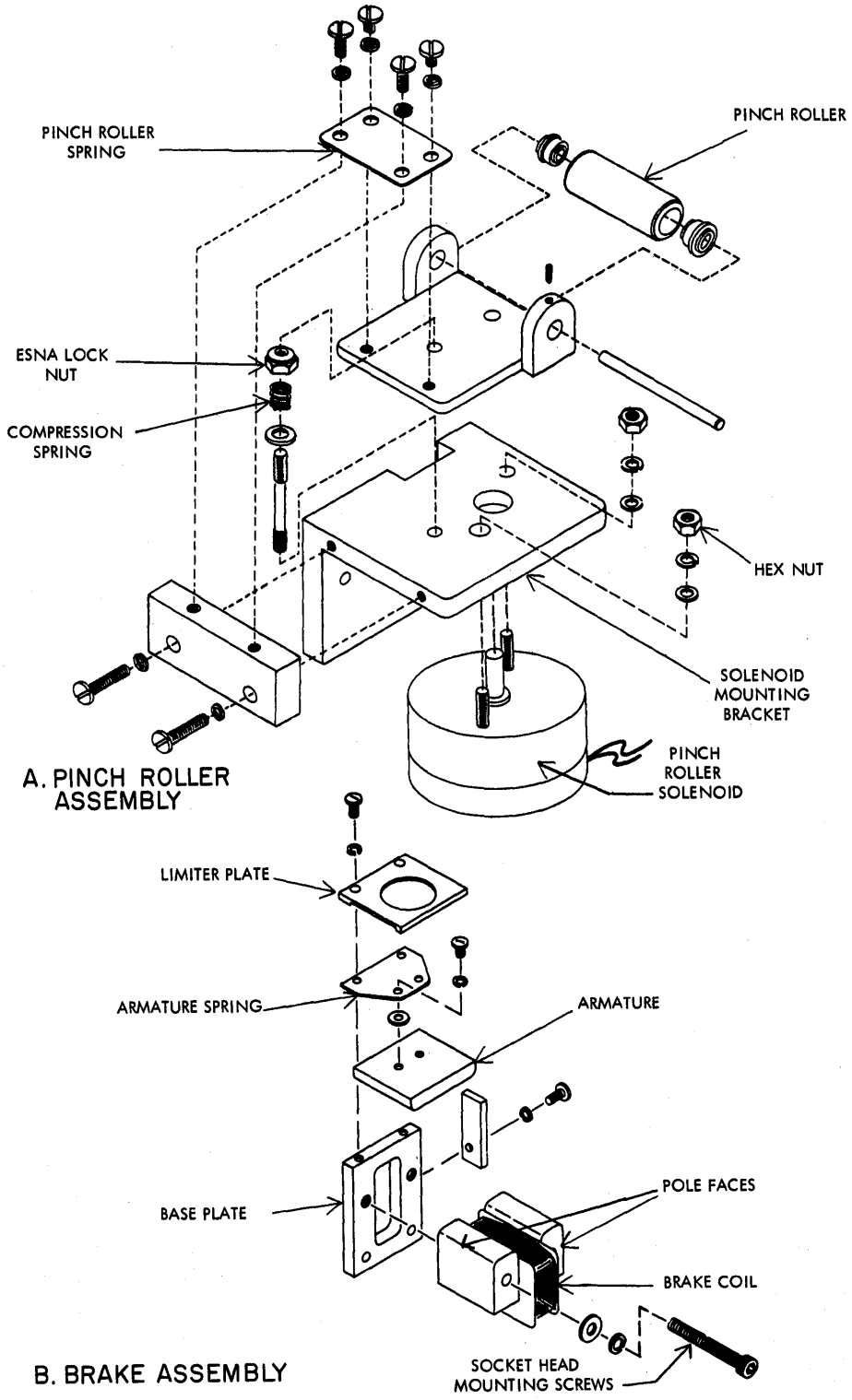


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Figure 5-23.—Exploded view of Reader tape feed mechanisms.

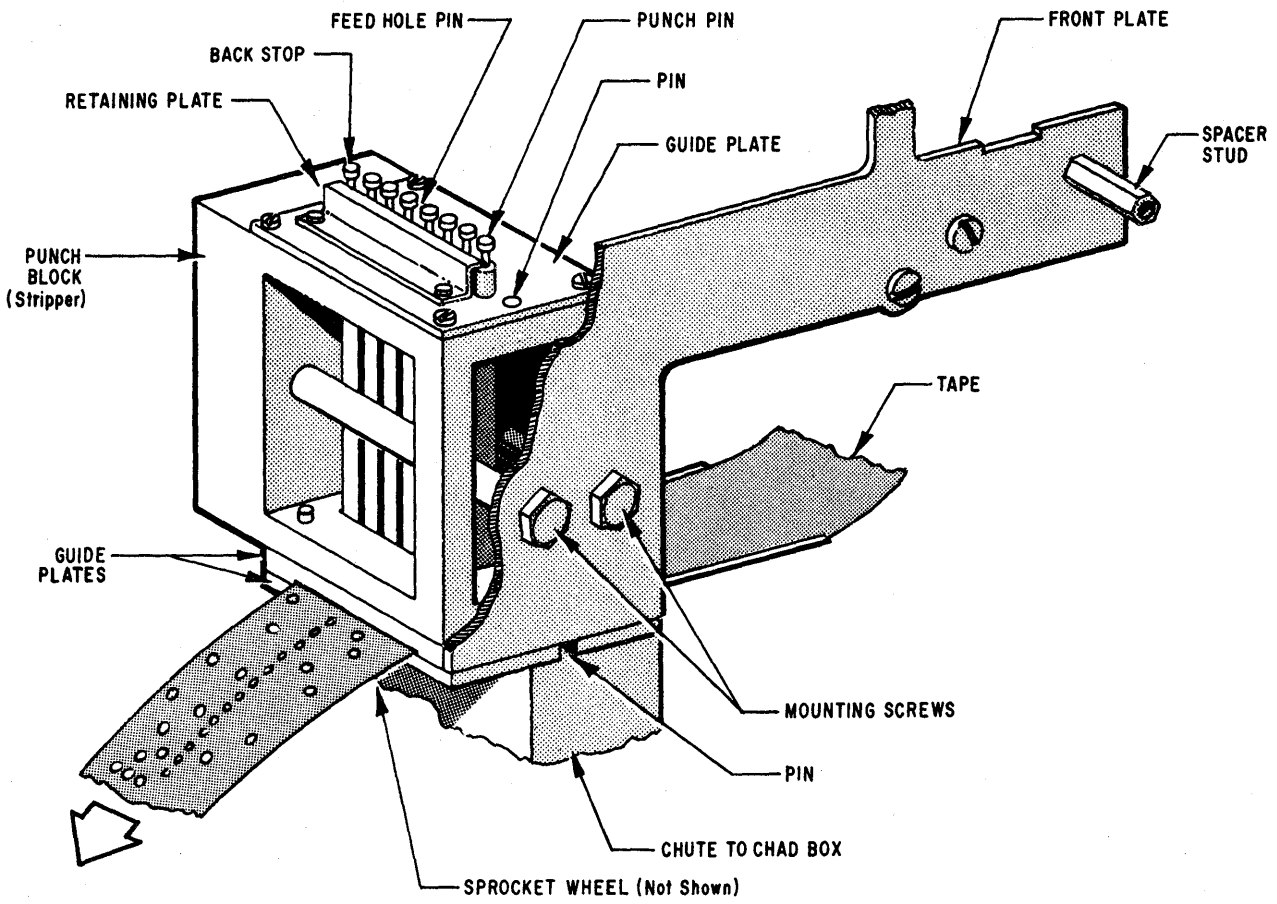

Figure 5-24.—Punch block.

sets the tape feed flip-flop and the tape is again placed in motion until a feed hole is detected. As previously described, the tape-feed flip-flop will be cleared, the brake applied, data sent to the computer and the entire cycle will be repeated until the tape has been completely read.

HIGH SPEED PUNCH

The HSP is a device that transposes 7 bits of computer data into a pattern of holes punched in a tape at a rate of 60 frames per second. Figure 5-24 illustrates the punch block assembly. The mechanical action of moving the punch pins is controlled by electromagnets (fig. 5-25), one for each of the eight levels on the tape (one feed hold, six data, and one utility level). These magnets are energized by the punch control circuits according to a pattern specified by the computer. If the magnet is energized, the movement of its armature allows unimpeded travel of the punch pin for that level. The activation of the punch magnets must be synchronized so that the data pattern may be established before punching. This synchronization is controlled by the magnetic revolver. The magnetic revolver is made up of a plate attached to one end of the punch motor with a magnetic disc mounted on the plate. A slotted frame with two reading heads surrounds the plate and magnetic disc. When the plate rotates, the magnetic disc passes the reading heads and generates the required timing signals. The timing signals indicate the relative position of the punching mechanism in

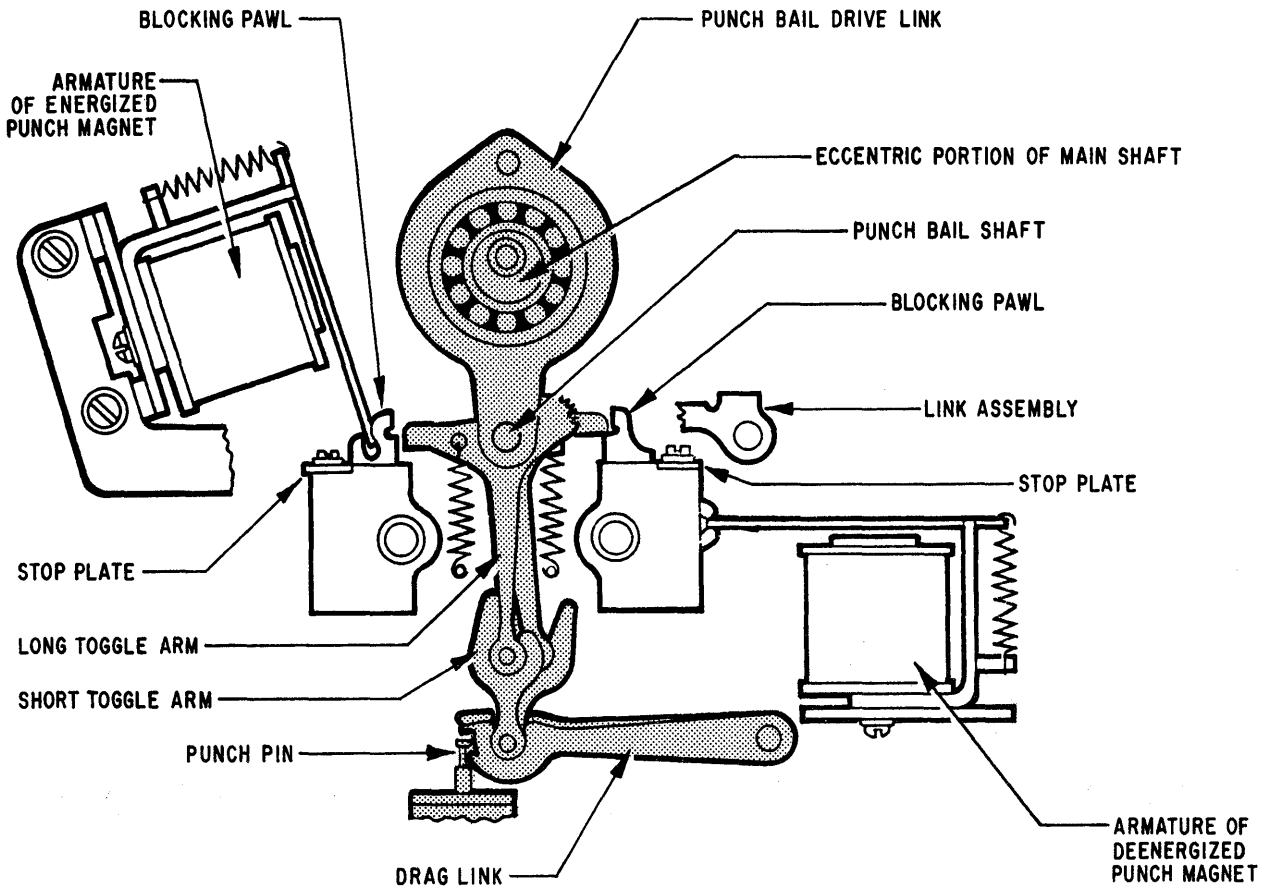

Figure 5-25.—Punching mechanism.

its cycle. The tape is punched when the tape is stopped, and output data from the computer is accepted while the tape is advancing.

When the punch is selected, the punch motor is turned on and the punching mechanism begins its cycle of operations. The registers are cleared and an Output Data Request signal is sent to the computer by a pulse from Reading Head 2, indicating that the punch is prepared for the first transmission. A frame of data is then transmitted to the punch data register by the computer, and the information is accompanied by an Output Acknowledge signal which gates the data into the register. A pulse from the magnetic disc passing Reading Head 1 allows the information to be punched. A subsequent pulse from Reading Head 2 clears all registers, and another Output Data Request signal is generated.

Punching Station

While reading the following discussion of the punching station, note and keep in mind the relationship of the punch pins shown in figures 5-24 and 5-25. The pins shown by both figures are the same pins.

The blocking pawls for the tape feed mechanism and the punching mechanism are used to prevent their respective actions from occurring. When a blocking pawl is considered "engaged," it has engaged the linkage involved in a manner that will cause the driving force of the linkage to be deflected to one side, instead of

being applied to the task at hand as when the blocking pawl is not engaged. The linkage is able to flex to one side through several pivot points, similar in function to the human leg with its thigh, knee, and ankle joints. The side movement would correspond to a "knee bend," and, in fact, the centermost joint is referred to as the "knee." A look at the punching mechanism (fig. 5-25) shows an eccentric drive mechanism (the punch bail drive link) to provide up-down motion to the linkage, a long toggle arm (the "thigh"), the knee, and a short toggle arm (the "leg"). The "ankle" portion of the short toggle arm terminates in a drag link, which acts to keep the linkage aligned over the punch pins. The punch pins are then driven down through the paper tape on a down motion of the linkage (similar to the stomping action of the human leg when the knee is kept stiff), and lifted again on the up motion of the linkage by an underlip on the drag link. The outer knee shown in figure 5-25 would flex to the left when bent, and the linkage for the next pin is shown flexed to the right. By alternating the directions for knee movement from pin to pin, a more compact design was possible.

The blocking levers on the upper portion of the long toggle arms have springs attached to keep the knee stiff when the blocking pawl is not engaged, and a hole is to be punched (see point A in figure 5-25). This same blocking lever would be engaged by the blocking pawl to provide twisting action on the long toggle arm's upper pivot that results in a knee bend and no hole punched (see point B in figure 5-25). The armatures of the respective punch magnets are energized on ls data, which disengages the blocking pawl for the corresponding linkage, and permits a hole to be punched in the appropriate level of tape. The punch magnets are deenergized on Øs data, so the blocking pawl for the respective linkage is left engaged, the knee bends, and no hole appears in the respective level. When no data is present to be punched, the blocking pawls are all engaged, and the motion of the eccentric drive is wasted in knee bends for all the linkages except the feed hole linkage. The feed hole linkage does not use a blocking pawl, so the punch pin is driven up and down continuously for feed holes. The punch pin for feed holes will move up and down through the same hole in the paper unless tape feed occurs.

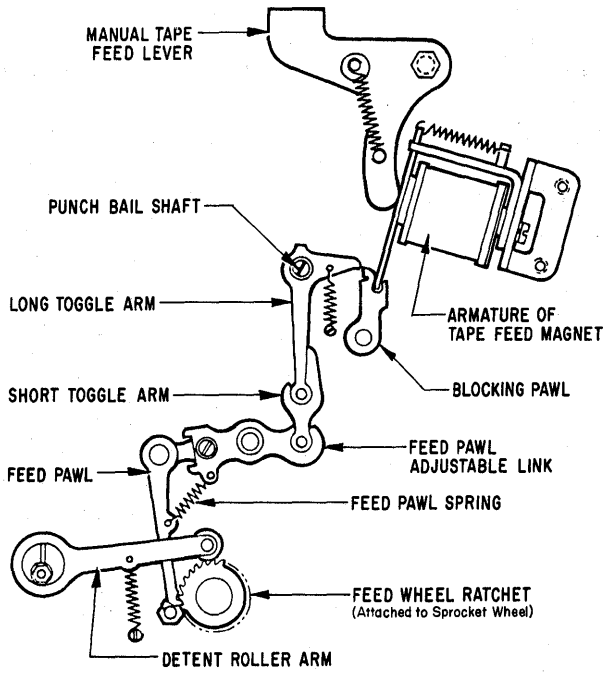

Figure 5-26.—Tape feed mechanism.

The blocking pawl for the tape feed mechanism is shown in figure 5-26. Like the linkage for the punch pins, there is a long and short toggle arm, knee, and magnet with armature. There is also an eccentric drive for up-down motion which is connected to the upper pivot of the long toggle arm, but this is not shown in figure 5-26. The "ankle" of the short pivot arm is connected through additional linkage to a ratchet that turns a toothed gear. The ratchet will move up and down to advance the tooth gear in precise increments of one tooth per frame per revolution of the shaft, provided that the blocking pawl is not engaging the blocking lever. Energizing the tape feed magnet will, therefore, cause the ratchet gear to turn to advance tape during the period when tape is not being punched (down motion with ratchet engaged), and to stop tape during periods when tape is being punched (up motion with ratchet disengaged), as long as the tape feed magnet remains energized.

A manual lever is shown in figure 5-26 that will move the tape feed magnet's armature to disengage the tape feed blocking pawl when pressed. This permits tape to be run out through the punch whenever and as long as this lever is pressed down. Since the feed hole pin is constantly being driven, tape that is run out this way will have feed holes it it. Tape created in this way is frequently referred to as a "leader" to distinguish it from unpunched tape. Since a no-hole frame of data would appear as Øs data, the use of a special tape format, such as odd parity, is frequently employed to distinguish Øs data from leader tape.

In addition, the tape feed magnet may be energized by a remote pushbutton switch mounted on the control panel. Thus, tape may be advanced without opening the door of the cabinet.

ADJUSTMENT AND LUBRICATION

Mechanical malfunctions can usually be prevented by proper adjustments and/or lubrication of the moving parts. Specific adjustment and lubrication details are discussed at length in the appropriate technical manual. However, there are some general rules that should be observed.

Before attempting any adjustment procedures for the HSP, rotate the motor shaft slowly in its normal direction (clockwise from the front). Check for freedom of movement and to ensure that there is no binding of the parts. While making the required adjustments, remember that improper adjustments may cause the equipment to be seriously damaged in a matter of seconds if power is applied. Rotate the shaft again to check for binding before applying power. Read the applicable portion of the technical manual before attempting any adjustment. After the adjustment, retighten any screws or nuts that were loosened to facilitate the adjustment.

The HSP should be thoroughly lubricated every month or 160 hours of use, whichever occurs first. Avoid overlubrication so that oil or grease will not drop or be thrown on other parts. Also, make certain that no oil or grease accumulates between the armatures and magnet pole faces or between contact points. Wipe excess lubricant from the armatures and pivot points. Use only SAE 10 (light machine oil) oil or light grease for lubricant.

The punch should be cleaned after every eight hours of punching. Cleaning is accomplished by removing the front cover and using a vacuum cleaner. Remove as much of the dust and tape chips as possible with the vacuum; then blow the remaining dust and tape chips from the punch. After cleaning, apply one drop of oil to each punch pin entering the punch block.

OJ-212(V1)/UYK TELETYPEWRITER

The OJ-212 Teletypewriter, also called TTY, is the only input/output device in the NTDS that provides a permanent record (hard copy) of data exchanges. Because of the slow speed of the teletype units, the TTY use is restricted to maintenance testing, whereby it provides a simple means of communication between the computer and a maintenance technician. The only on-line application of the TTY in NTDS is with Link 14. The information that is printed for Link 14 will be discussed in greater detail later in the text. Data presentation by the TTY may be either a printed page or a punched tape.

The OJ-212, previously known by the designation of AN/UGC-13 (MOD), is made up of six basic units: a keyboard, a page printer, a typing reperforator, an auxiliary typing reperforator, a transmitter-distributor and an adapter. The teletype is shown in figure 5-27.

(1) Keyboard—A set of manually operated keys which generate coded electrical impulses that can be sent to the other teletype units, as specified by the front panel controls.

(2) Transmitter-Distributor—This unit reads perforated paper tape and converts the data into coded electrical impulses which can be sent to the other TTY units or the computer via the keyboard. It is also controlled by the front panel.

(3) Page Printer—This unit accepts TTY codes from the keyboard, transmitter-distributor (T/D) or the computer and prints the characters

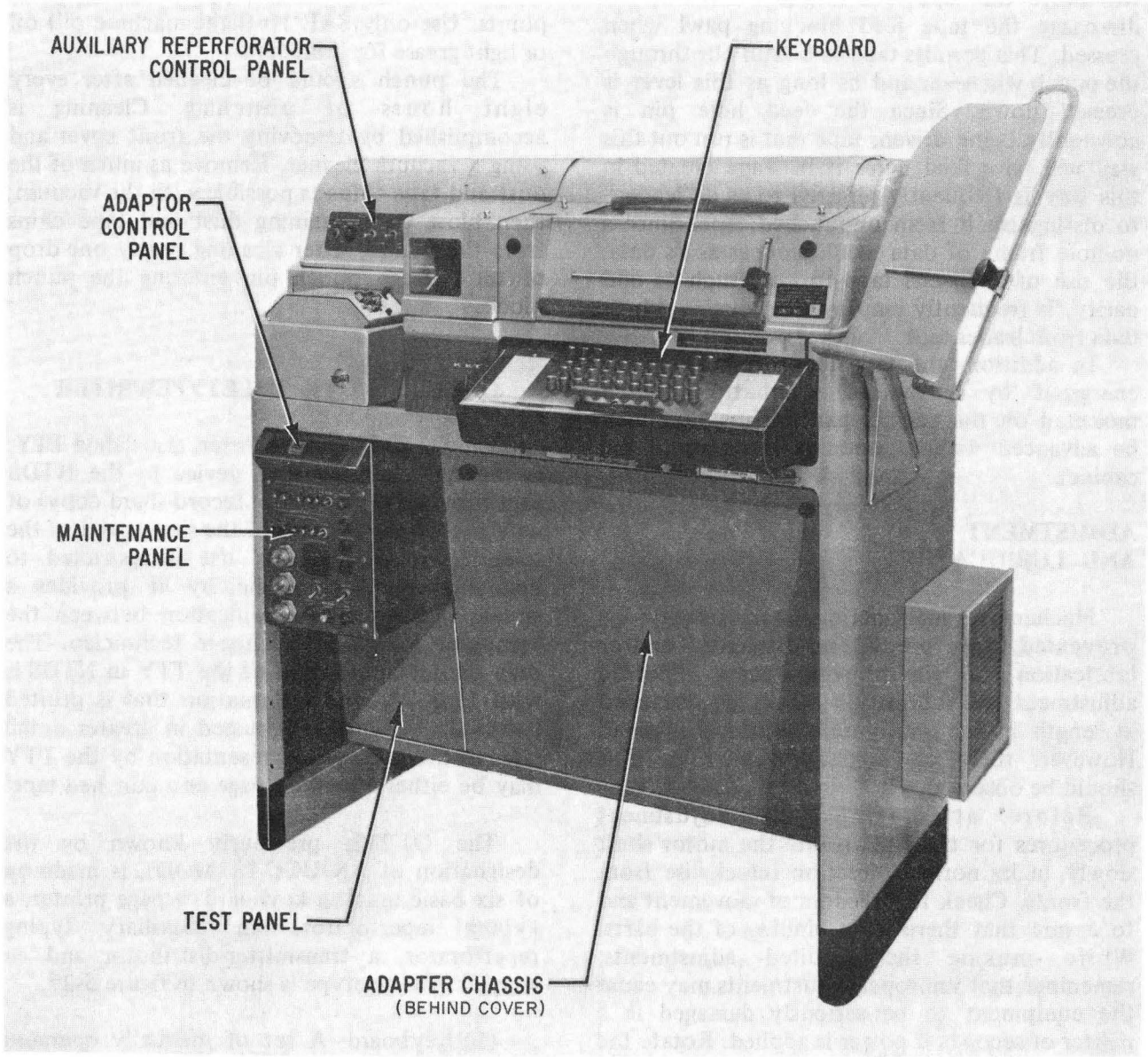

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Figure 5-27.—AN/UGC-13(MOD) Teletypewriter.

or executes the specified functions (e.g., line feed or carriage return).

(4) Typing Reperforator—The typing reperforator accepts TTY codes from the keyboard or the T/D and punches the character code on paper tape. It also prints the character on the tape above the hole pattern.

(5) Auxiliary Typing Reperforator—This device performs the same operations as the typing reperforator. It is used to monitor external data lines while an operator is using the keyboard to prepare tapes on the typing reperforator.

(6) Adapter—Since the TTY uses standard teletype (5 Level) codes in a serial markspace

pattern and the computer uses parallel digital codes, an adapter logic chassis is provided to convert from teletype to computer format and from computer to teletype format. This logic chassis is normally the only maintenance interest in the TTY of the Data Systems technicians. Usually the mechanical units of the TTY are maintained by Radiomen with a teletype repair NEC.

BASIC TELETYPE CIRCUIT

The basic teletype circuit or loop is shown in figure 5-28. The power supply produces a constant level d.c. current (referred to as loop current) that is used to drive the printer. Depressing any key on the keyboard will permit current flow in a specific format that will cause an associated character to be printed or function to be performed.

Teletype Signals

The format of the signal generated by pressing a key is illustrated in figure 5-29. The signal is divided into seven time units. The shaded area of figure 5-29 represents mark pulses, which are periods of current flow, and the clear area represents space pulses, which are periods of no current flow. Of the seven units of a teletype signal, five are numbered and called intelligence units. The first unit is the start pulse and is always a space. A space is distinguishable since periods of nontransmission involve current flow. The last unit is the stop pulse and is always a mark. These seven units make up the start-stop method of teletype communication. The start-stop pulses are used to synchronize the teletype machines, and the intelligence pulses hold the information. Notice that the first six units in figure 5-29 are the same length, but the seventh (stop) unit is longer. Each of the first six units requires 13.47 msec for transmission, and the seventh requires 19.18 msec in 100 word per minute teletype communications. The unit time decreases as the word per minute reference increases (Table 5-1). Keep in mind that the teletype codes are serial data as opposed to computer parallel data.

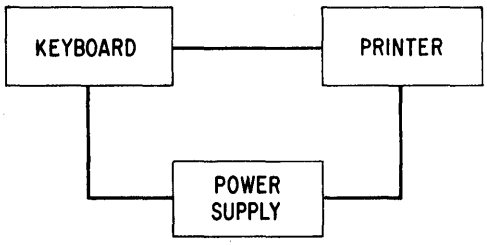

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Figure 5-28.—Basic teletype loop.

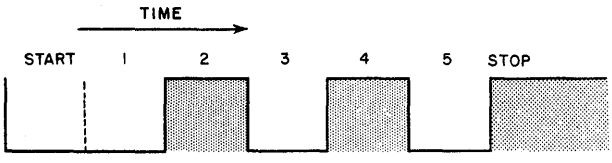

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Figure 5-29.—Mark and space signals in teletype.

The mark-space codes for all the characters and functions of a teletype are illustrated in figure 5-30. The octal codes on the right of the chart are the codes sent by the computer to produce the corresponding teletype code. The teletype codes shown are standard and used in all teletypes. The octal codes may or may not be unique for the OJ-212 machine. The start-stop pulses are generated automatically by the adapter each time a computer code is sent.

The basic teletype is designed to work in conjunction with other machines of the same nature. The keys on the keyboard each code pulse trains that open and close a series loop connecting all the keyboards together. Thus, any key pressed on any of the connected keyboards affects the total circuit. The printer and the reperforators are also connected in the loop, and these react to the voltages developed across their impedances by the loop current. A single variable voltage source for the circuit is adjusted to provide the necessary loop current needed for proper circuit operation. The source voltage must be raised to compensate for additional machines and/or increased line losses, or lowered

Table 5-1.—Transmission Speeds and Time Allocations for 5-Unit Printing Telegraph Code Patterns

Start-Stop Code Pattern (Total No. of Pulses per Character)	Nominal Speeds and Pulse Lengths							Where Used
	Transmitting Speeds			Pulse Lengths in Milliseconds		Receiving Shaft Speed in RPM	Milliseconds per Character	
	Operations per Minute	Average Words per Minute	Baud	Start and Five Code Pulses	Rest Pulse			
7.42 Unit	368*	61.33	45.45	22	31	420	163	Bell System—U.S.
7 Unit	390*	65	45.45	22	22	420	154	Western Union—U.S.
7.5 Unit	400†	66.67	50	20	30	461.5	150	CCITT Standard—Europe
7.42 Unit	404†	67.33	50	20	28.4	461.7	148.4	U.S. Military, for Inter-operation with Allies
7 Unit	428.6†	71.43	50	20	20	461.5	140	Former CCITT Standard—Europe
7.42 Unit	460	76.67	56.88	17.57	25	525.7	130.43	U.S.—All Commercial and Military Users
7.42 Unit	600‡	100	74.2	13.47	19.18	685	100	U.S.—All Users
7 Unit	636‡	106	74.2	13.47	13.47	685	94.3	U.S. Military—Limited Use

*These two codes are compatible.
†These three codes are compatible.
‡These two codes are compatible.

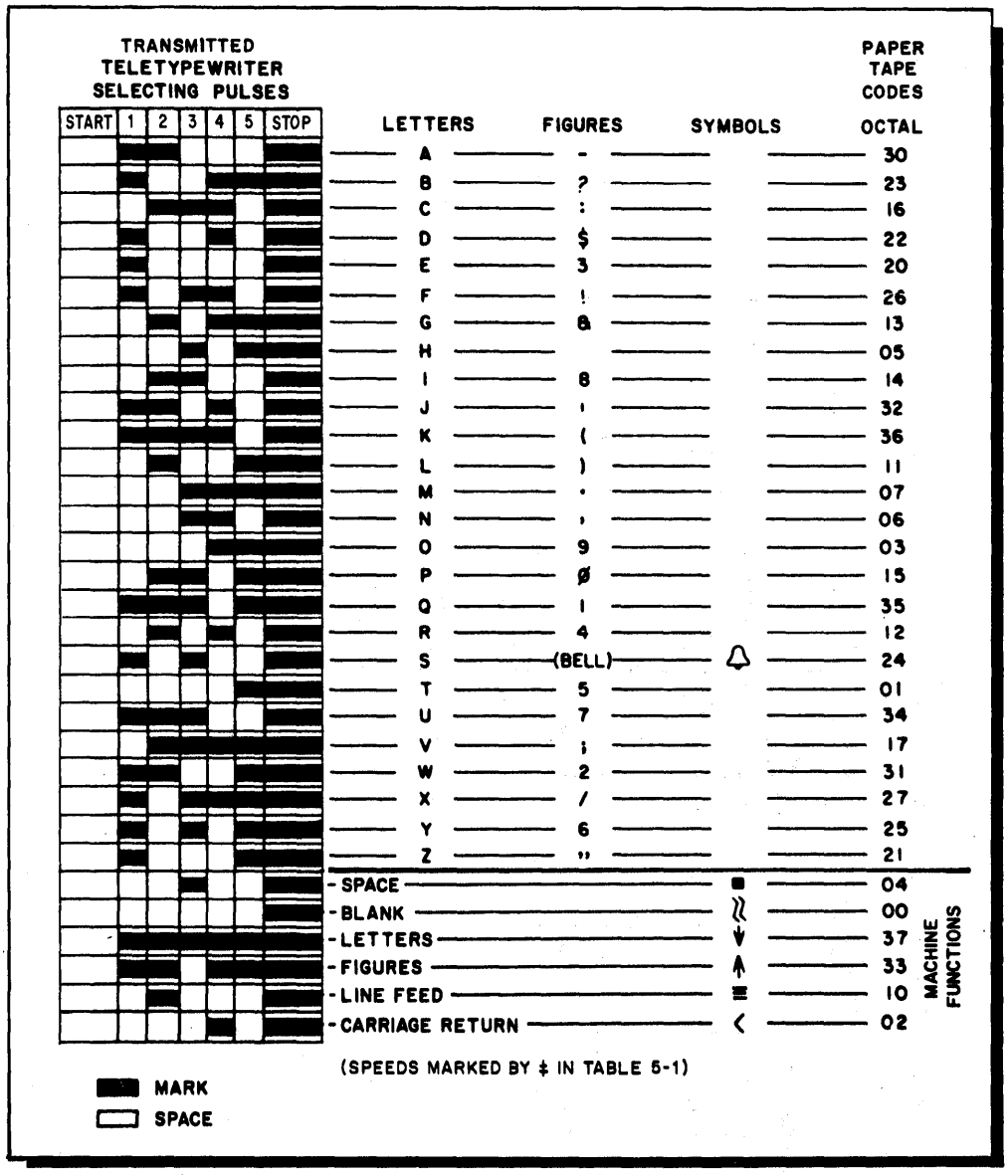

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Figure 5-30.—Teletypewriter codes.

when machines are removed or the total impedance of the circuit decreases from other causes.

With the addition of the adapter, the OJ-212 becomes an independent machine capable of communicating with a computer. The adapter provides a source voltage adequate for establishing the loop current for the keyboard, printer, and both reperforators. The adapter also performs serial to parallel conversion on computer input data, and parallel to serial conversion on computer output data. This is in addition to providing the necessary I/O format for communications with the computer.

Because of the constant current/variable voltage aspect of closed teletype loops, the term "voltage" is not usually employed in discussing circuit function. The term "loop current" is commonly employed instead. Circuit conditions are then categorized as "marks" (periods having loop current) and "spaces" (periods when an open circuit inhibits loop current).

FRONT PANEL CONTROLS

There are five sets of controls for the OJ-212. Three are used to control the teletype equipment, and two control the adapter.

The keyboard controls are illustrated in figure 5-31. Most keys have dual functions that depend upon the previous selection of either the letters (LTRS) or figures (FIGS) key. Once shifted to LTRS, the equipment remains so shifted until the FIGS key is operated, and once shifted to FIGS, it remains so shifted until the LTRS key is depressed. All letters are upper case; lower case letters are not used. Each key depressed, except those in the top row which accomplish local functions only, will cause a TTY code to be generated, as shown in figure 5-30.

A three-position control switch, mounted to the left of the keyboard (fig. 5-27), is used to select teletype equipment for operation. The operating positions of this switch are labeled K, K-T, and T. In the K (keyboard) position, the keyboard generates the signals which are fed to the printer. The tape perforator is inoperative, and the tape reader is not connected to the printer. In the K-T (keyboardtape) position, the keyboard generates the signals, and the tape perforator simultaneously punches a tape. The tape reader is connected to the printer. When the control switch is in the T (tape) position, keyboard entries are punched on tape, and no signals are sent from the keyboard to the printer. The printer can receive signals from the computer, while the tape is being punched, or the printer may receive signals from the tape reader. It should be obvious that data flow can only be from an input source, such as the keyboard, and to an output section, such as the printer, tape perforator, or auxiliary

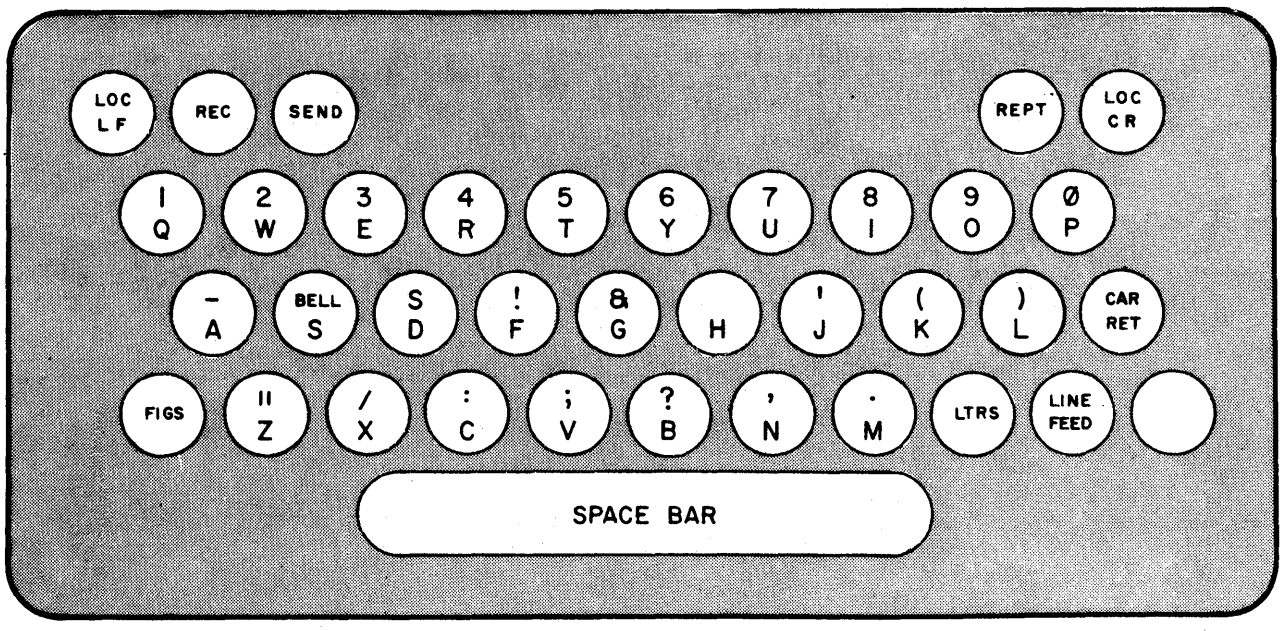

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Figure 5-31.—Keyboard.

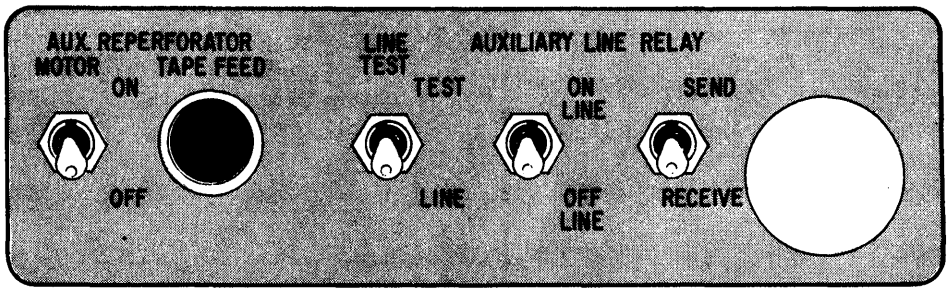

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Figure 5-32.—Auxiliary reperforator control panel.

reperforator. The computer, which has both input and output capabilities, can access portions of the OJ-212 at its convenience if it is online, and consistent with the switch settings and functional roles played by various sections of the OJ-212. The auxiliary reperforator control panel (fig. 5-32) is used to control operations of the auxiliary reperforator and also controls the output from the teletype for Link 14 operations. The Motor and Tape Feed switches are used to turn on the auxiliary reperforator and to produce a tape leader at the beginning and end of a punched tape. The auxiliary reperforator is not affected by the position of the K, K-T, T switch, but always copies the input provided to the printer. The Line/Test adapts the printer and keyboard for line-loop or test-loop operations. It must be in the Line position for Link 14 operations. The Auxiliary Line Relay switches (On-Line/Off-Line and Send/Receive) control the actual output of the OJ-212 to external equipment. The switches must be in the On-Line and Send positions for Link 14 operations.

The adapter control panel (fig. 5-33) and the adapter maintenance panel (fig. 5-34) function together to control the operations of the adapter unit. A row of four indicator/switches on the adapter control panel provides the operation with information necessary for use of the TTY with the computer. The Computer Request will be lighted when the computer trys to communicate with the adapter in the test mode (fig. 5-34). The Motor Enable, Input and Output indicators will illuminate when they are performing their associated function or when they are depressed. They allow manual control of the TTY in the same manner as the computer controls the TTY with external function codes.

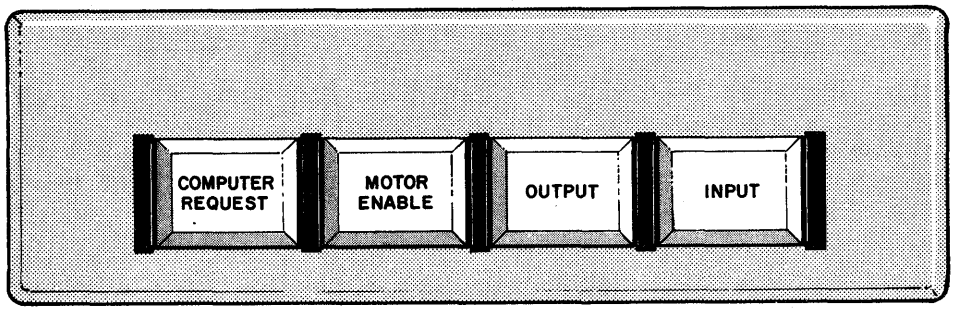

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Figure 5-33.—Adapter control panel.

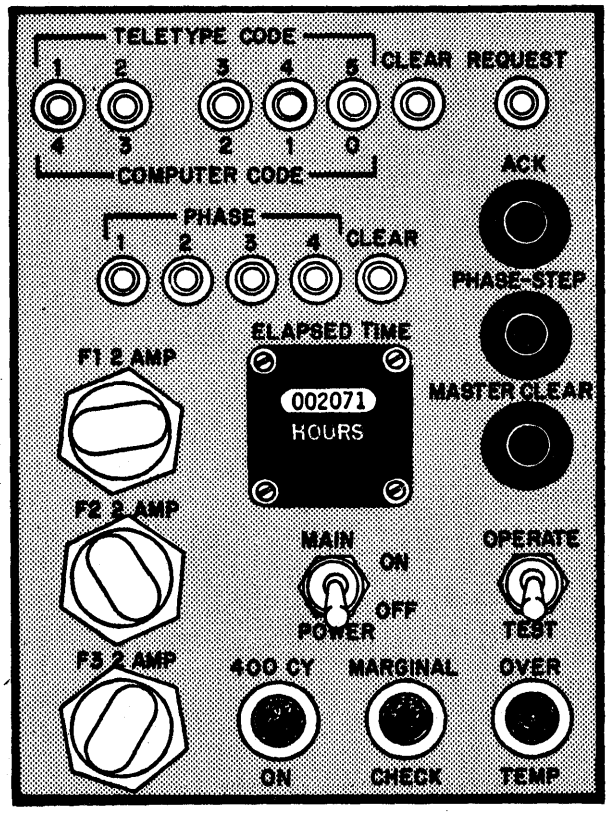

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Figure 5-34.—Adapter maintenance panel.

The adapter maintenance panel includes numerous switches and indicators for both operational and maintenance use. The Operate/Test switch controls the mode of operation, and acts exactly as the online/offline switch found with other equipment. When this switch is in the Test position, no data will be exchanged with the computer. In the Operate position, the equipment will receive or transmit data to the computer. The Teletype Codes/Computer Codes indicators indicate the parallel data and control codes being transmitted or received by the adapter. The Request indicator is lighted when the adapter is prepared to receive data from the computer. The Ack switch, when depressed, simulates a computer output data acknowledge signal (for maintenance purposes only). It is enabled only when the Test/Operate switch is in Test position.

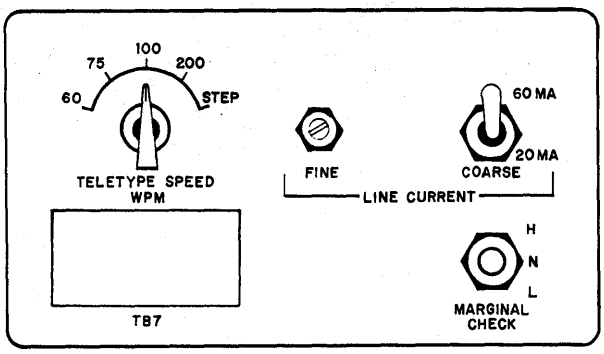

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Figure 5-35.—Test panel.

The test panel (fig. 5-35) is located on the adapter chassis behind the dust cover. The Teletype Speed WPM switch provides the coarse adjustment for changing the length of the start, stop, and intelligence pulses of a teletype signal. The Line Current Coarse and Fine controls provide adjustments for setting the teletypewriter line current for either 60 mA or 20 mA operation. Current of 60 mA is used in most applications, including NTDS.

By select use of the various panels and the keyboard (all shown in figure 5-27), the operator or maintenance technician can perform a variety of online and offline operations. Since online functions are software dependent (vary from program to program), the greatest flexibility is found in using the offline functions. Any input portion (computer, keyboard, or tape reader) can be made to address one or more output portions (computer, printer, typing reperforator, or auxiliary reperforator). This provides a convenient means for manual operations for the purpose of duplicating tapes, making minor changes to duplicated tapes, creating new tapes, obtaining printed copies of tapes, etc.

OPERATIONAL CHARACTERISTICS

Information which is received by or prepared on the TTY can either be printed on a roll of page width paper or punched on 5-level paper tape. The tape used in the TTY contains five data levels (the feed hole level is not

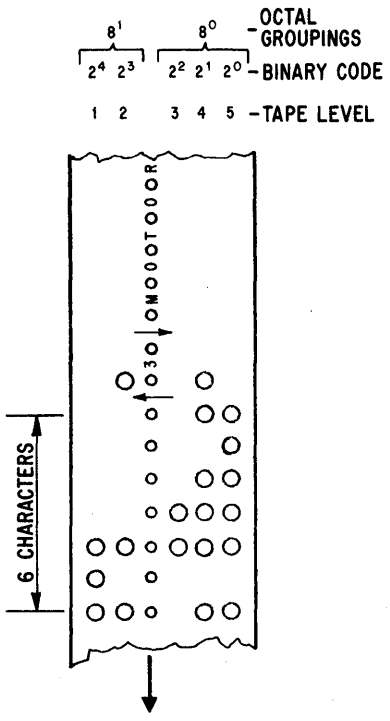

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Figure 5-36.–TTY paper tape.

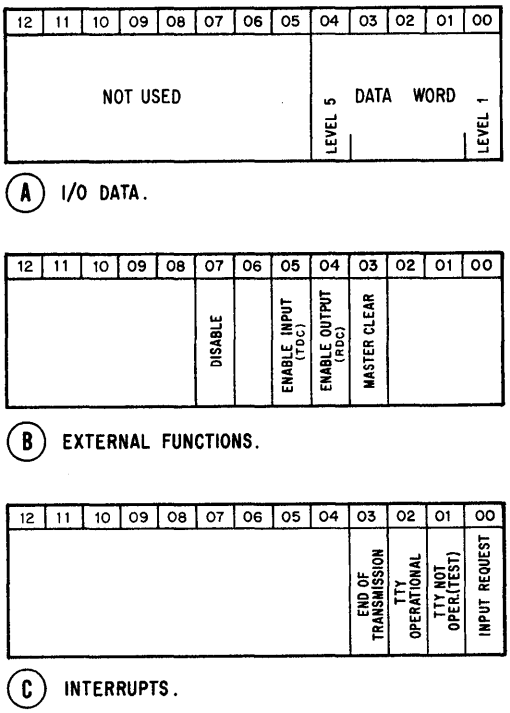

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Figure 5-37.–Data and control formats.

counted since its presence is automatic and for timing only) (fig. 5-36). A hole on the tape represents a "one" and no hole punched represents a "zero." The tape is thus coded in binary notation with one partial and one complete octal digit in each frame that correspond to the paper tape code in figure 5-30 (maximum count = 37_8). The feed holes between levels 2 and 3 are used to position and advance the tape in either of the reperforators or the tape reader. In addition to the punched holes, the tape also contains printed characters. These printed characters lag behind the punch frame by 6 1/2 frames because of the mechanical displacement of the punch and printing units. The extra 1/2 frame insures a readable character by causing the print to appear between frames.

The data word and control word formats are shown in figure 5-37. The TTY sends and receives data words in five bit codes; therefore, only the lower five bits of the I/O lines are used as illustrated in figure 5-37A. The external function (fig. 5-37B) and interrupt (fig. 5-37C) words are used to control operation of the TTY and to inform the computer of the current status of the TTY.

ADAPTER BLOCK DIAGRAM

Since the TTY is unable to communicate directly with the computer, an adapter unit has been provided which converts data flow between the TTY and computer. Data conversion is from parallel (computer) to serial (TTY) or from serial to parallel form. The adapter circuits are divided into six functional areas: the data flow register, the control interface, the function translator, a timing chain, clock timing and (Manual) controls. These areas and the TTY block diagram are illustrated in figure 5-38.

Data Flow Register (DFR)

This register does the actual format conversion of the information. It shifts data

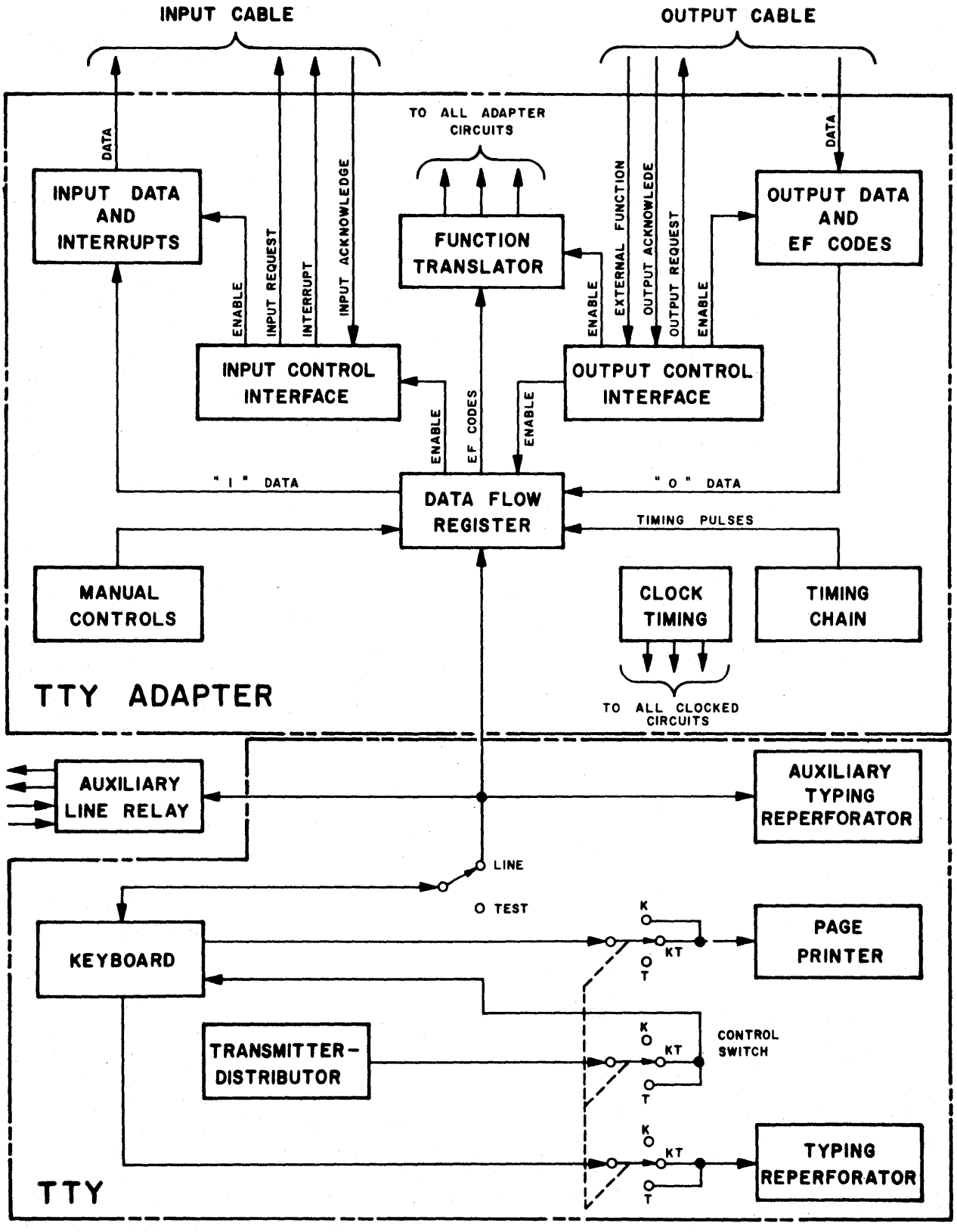


Figure 5-38.—TTY and adapter block diagram. 124.453

codes received from the computer, one bit at a time, to the TTY under control of the timing chain. For input to the computer, serial bits from the TTY are sequenced into the data flow register (DFR) under control of the timing chain. Another function of this register is to handle various control codes (external functions and interrupts) which are sent and received by the adapter.

Control Interface

This section handles the control signals to and from the computer which are necessary for the transfer of data between the TTY and the computer. All incoming data is synced with the adapter clock timing. The Output Acknowledge signal will disable the Output Request signal, start the Timing Chain and enable data into the DFR. The Input Acknowledge signal disables either the Input Request or the Interrupt signal.

Function Translator

The function translator translates the external function codes sent by the computer into enable signals to perform the function that is specified by the program. External function codes are stored in the DFR when the external function signal is received by the control interface unit.

Timing Chain

The timing chain produces timing signals that are used to select, in proper sequence, the data bits which are sent from the adapter to the TTY. The timing chain also diverts the data coming from the TTY into proper bit positions in the DFR. When inputting to the computer, a start pulse from the TTY enables the timing chain. When the complete TTY code is assembled, a stop pulse disables the timing chain and causes an Input Request signal to be generated by the Input control interface circuits. When receiving data from the computer, the Output Request is enabled until an Output Acknowledge is received. The Output Acknowledge disables the Output Request and enables the timing chain. The timing chain will then produce start and stop pulses for the TTY. When the stop pulse is generated, the Output request signal will again be enabled.

Clock Timing

The clock timing circuits generate the timing signals necessary for the proper operation of all clocked adapter circuits.

Manual Controls

The manual controls provide control of the various operations performed by the adapter. These controls also contain circuits which allow the computer to control the power for operating the TTY motors and to produce control signals and interrupt codes which are sent to the computer.

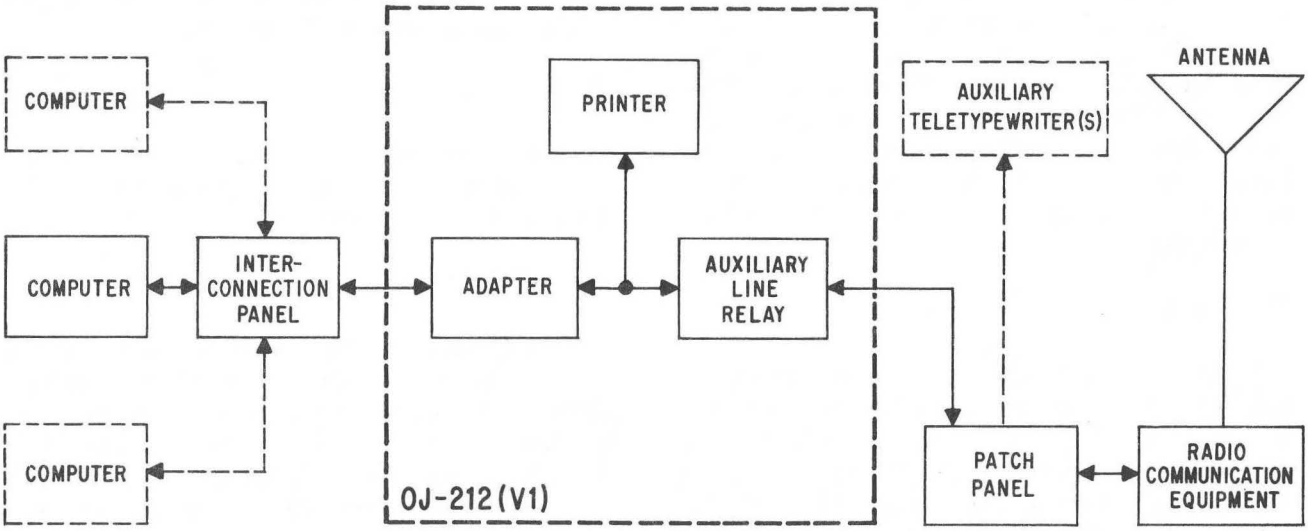
Auxiliary Line Relay

The lower portion of figure 5-38 shows the block diagram for the TTY and adapter. The Auxiliary line relay is built into the TTY cabinet, and all information to external equipment (communications or other teletypes) passes through it. The auxiliary line relay makes the OJ-212 compatible with other teletype equipment. To operate with Link 14 communications equipment, the output of the TTY is connected, through the auxiliary line relay and a patch panel, to the transmitter and receiver as illustrated in figure 5-39.

Changing Paper

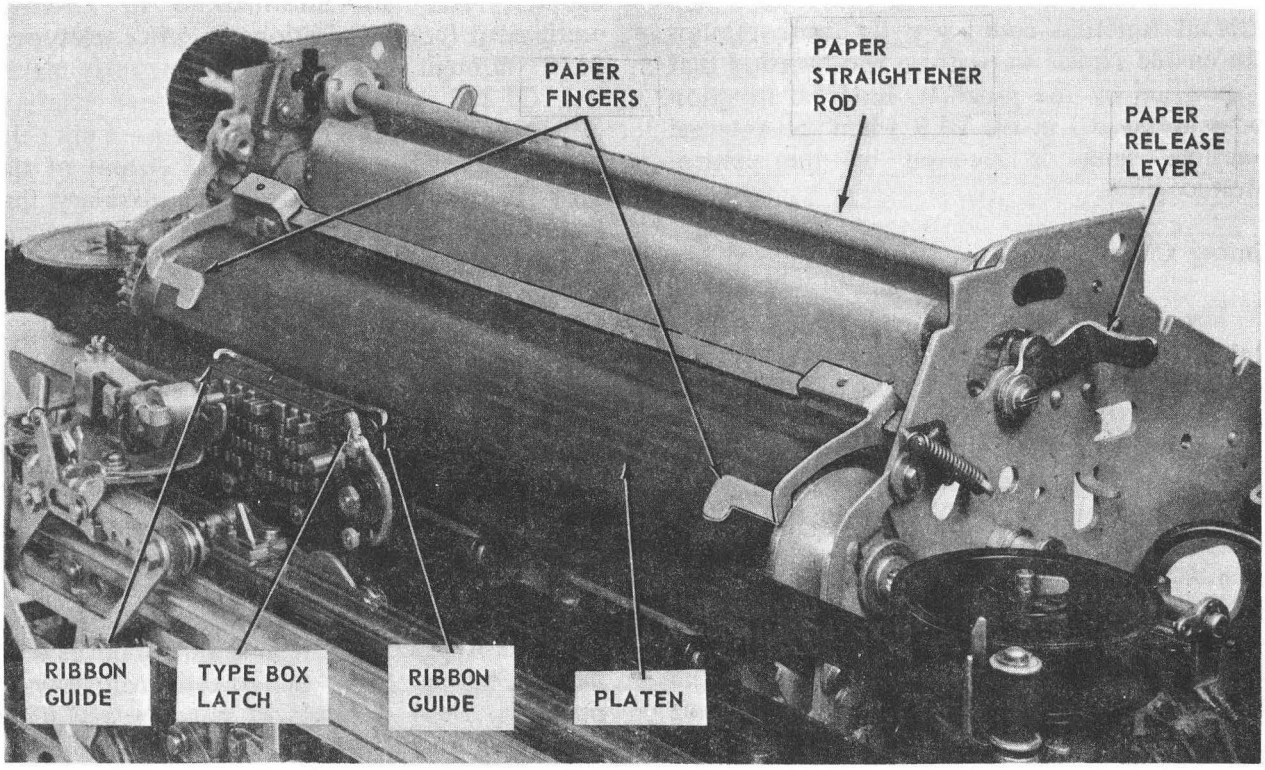
To insert a new roll of paper in the machine, first shut off the power. Press cover release pushbutton and lift cover. (Refer as necessary to figs. 5-40 and 5-41.) Push back paper release lever, lift paper fingers, and pull paper from platen.

Lift the used roll from machine and remove spindle from core of used roll. Insert spindle in new roll. Replace spindle in spindle grooves with paper feeding from underneath roll toward operator. Feed paper over paper straightener rod, down under platen, and up between platen and paper fingers. Pull paper up a few inches beyond top of platen, and straighten it as though straightening paper in a typewriter. Then



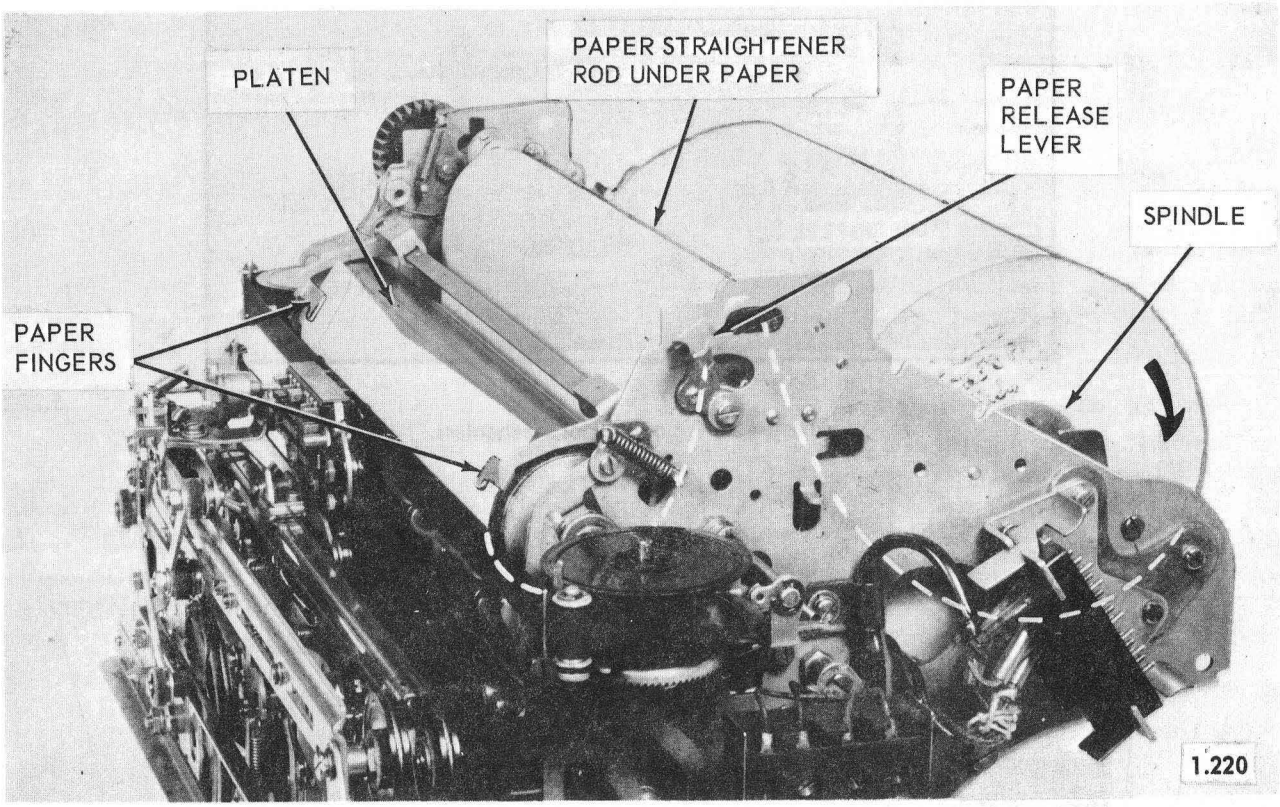
1.219

Figure 5-39.—Teletypewriter system for NTDS.



1.220

Figure 5-40.—Paper roll removed.



1.221

Figure 5-41.—Paper roll inserted.

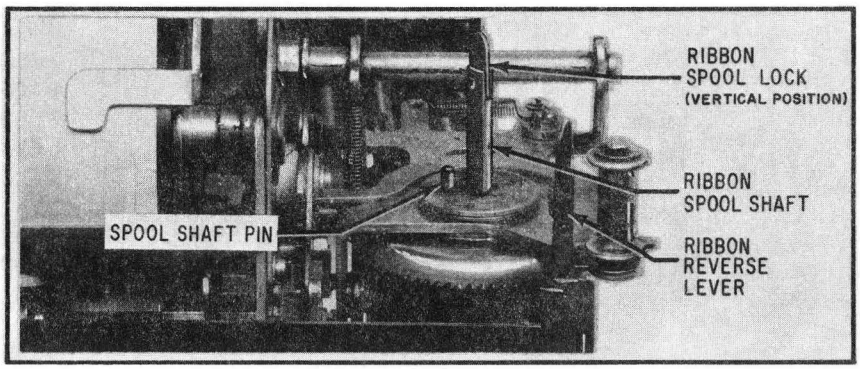
lower paper fingers onto paper and pull paper release lever forward.

While inserting paper, avoid disturbing the ribbon or the type box latch. After paper is in place, check to see that ribbon still is properly threaded through ribbon guides. Also check to make certain that type box latch has not been disengaged. It should be in a position holding the type box firmly in place. Close cover. Open window lid by sliding latches together. Bring up the end of the paper and close window lid with paper feeding out the top of it.

Changing Ribbons

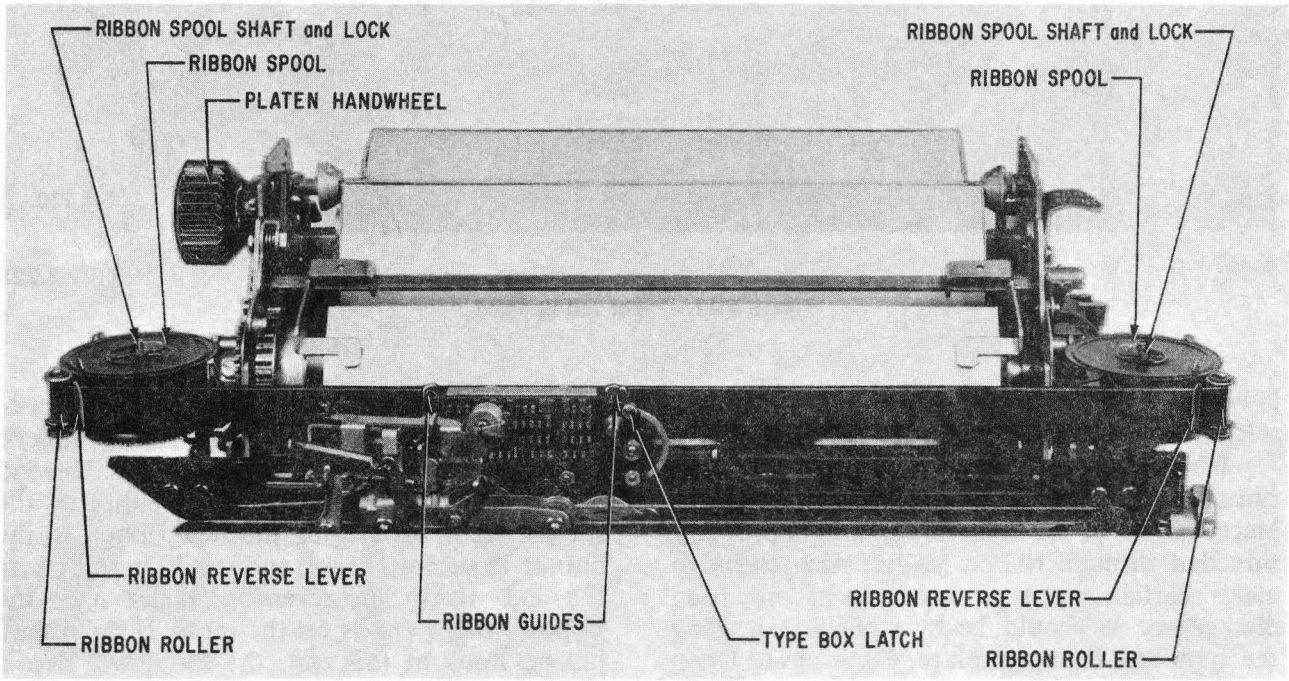
To replace a worn ribbon in the typing unit, press the cover release pushbutton and lift the cover. (Refer as necessary to fig. 5-42 and 5-43.) Lift the ribbon spool locks to a vertical position, and remove both spools from ribbon spool shafts. Remove the ribbon, the ribbon rollers, ribbon reverse levers, and ribbon guides. Unwind and remove the old ribbon from either of the spools. Hook an end of the new ribbon to the hub of the empty spool, and wind the ribbon on the hub until the reversing eyelet near the ribbon's other end is on the spool. If the ribbon has no hook at this end, the spool will have a barb that should be used to pierce the ribbon to secure it to the second spool.

Replace both spools on ribbon spool shafts, making sure that they settle on spool shaft pins and that the ribbon feeds from the front of the spools. Turn down ribbon spool locks to a horizontal position to lock spools in place. Thread ribbon forward around both ribbon rollers, through the slots in the ribbon levers and ribbon guides. Take up slack by turning free



1.222

Figure 5-42.—Ribbon spool mechanism.

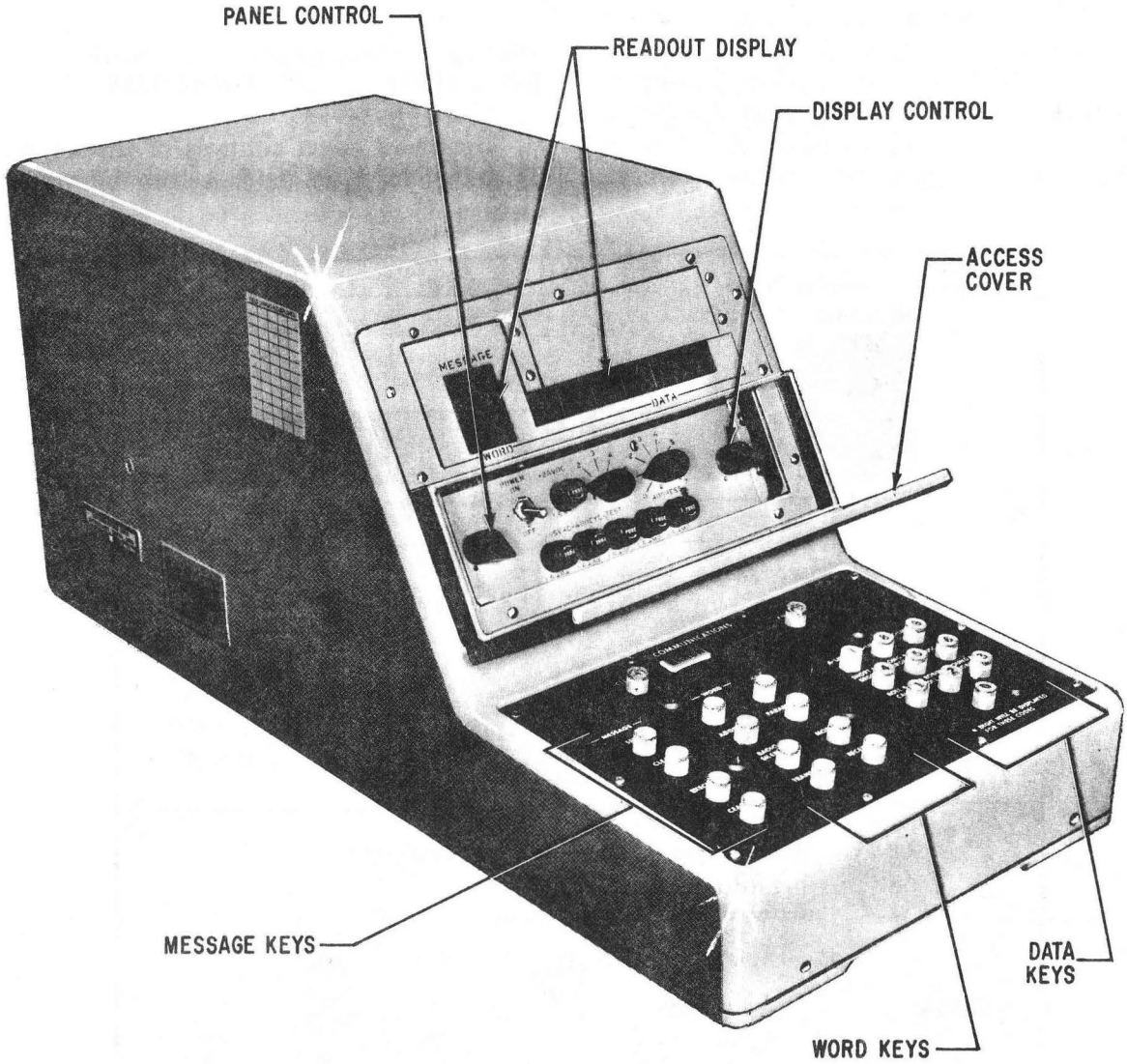


124.461

Figure 5-43.—Ribbon inserted.

spool. After slack has been taken up, check to make certain that ribbon still is properly threaded through ribbon guides, and that the reversing eyelet is between spool and the reverse lever. Also see that the type box latch has not been disengaged. It should be in position, holding the type box firmly in place.

Turn the paper up a few inches by pressing down and turning platen handwheel. Close cover. Open window lid, bring up the end of the



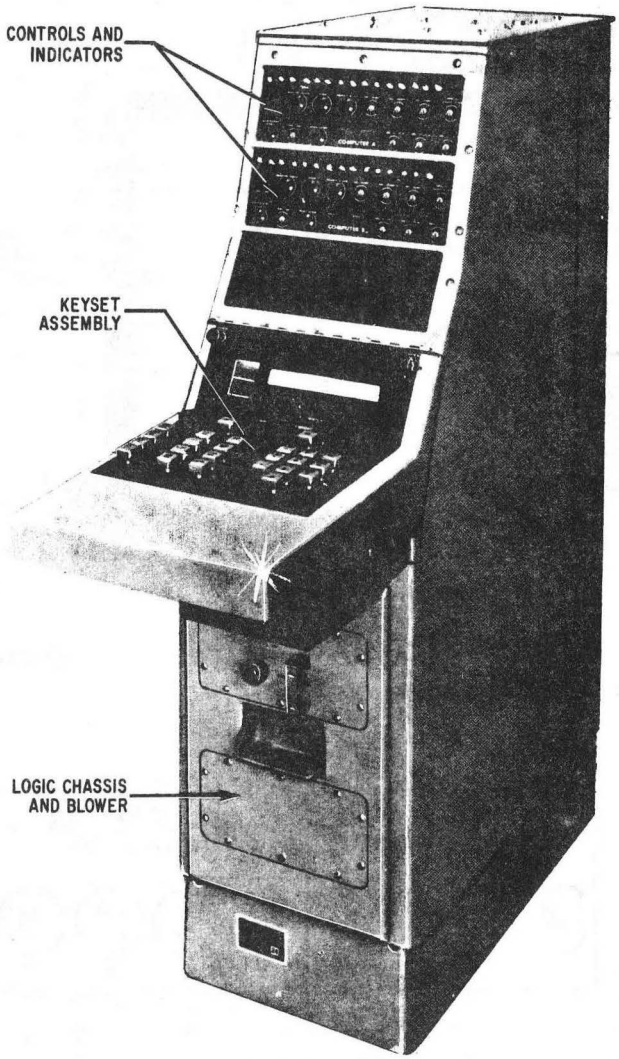
124.209

Figure 5-44.–MX-3195(V)/USQ-20(V) Digital Data Introducer.

paper, and close window lid, with paper feeding out on top of it.

MX-3195(V)/USQ-20(V) DIGITAL DATA INTRODUCER

The digital data introducer (universal keyset or simply keyset) shown in figure 5-44 provides a means of supplying the NTDS computers with manually entered data which is characterized by a relatively low data rate (volume and speed). The keyset is interfaced to the NTDS computer through the keyset central multiplexer (KCMX), discussed in chapter 3 of *DS 3 & 2, Vol. 2.* The keyset is designed to provide standardized keyboard and readout (visual indicator) facilities which may be easily adapted to various subjects when manual entry of data or control information



124.210

Figure 5-51.—C-3675A/USQ-20(V) System Monitoring Panel.

identical functions; therefore, only the C-3675A will be discussed in this text.

The SMP is a self-contained computer control and monitoring device, incorporating features of a keyset, but also providing a means of establishing remote control of and monitoring the more significant operations of each computer in a particular data processing system. A system may consist of two, three or four computers, that can be controlled by one SMP. Computer operations performed by the SMP are divided into the following three groups.

(1) Remote computer operations—A group of system monitoring controls is provided which duplicates some of the major computer controls for each computer, such as bootstrap, master clear, run, stop, etc. These functions are found on the SMP monitor control panel.

(2) Computer function commands—These commands are generated by the SMP keyset and are used for directing a portion of the operational program in a particular computer to perform certain operational functions. These are software functions, as opposed to the hardware functions available at the monitor control panel, and as such these are only functional with the appropriate software (the system program is loaded).

(3) Fault and computer indications—A group of indicators is provided which displays the communications faults between the computer and associated peripheral units or within the computer itself. These indicators also display amplifying information necessary to operate and monitor the computer system.

FRONT PANEL CONTROLS

Up to four separate monitor control panels (fig. 5-52) provide duplicate computer controls, one for each system computer. These controls permit the operator to load, reload, or control programs and to start, stop, or modify (by use of the selective stop or jump switches) the computing operations in any of the system computers. The monitoring panel also displays amplifying information for determining what conditions are occurring in a computer or system.

This is done using the neon indicator register on the upper portion of the monitor control panel. This 15-bit register coincides with the upper 15 bits of the computer output channels assigned to the SMP. The computer can place an external function on the associated channel EXF line and this will cause the SMP to display the upper 15 bits of the function word. The SMP will continue to display the last word received until another

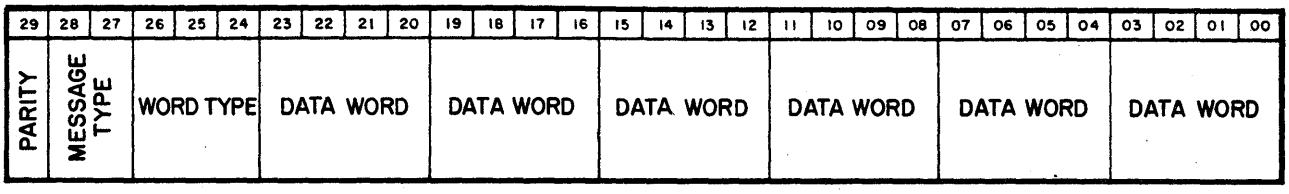
panel are the message, word, and data displays. These displays are broken down into positions, and each position is marked by a slightly frosted lens upon which images can appear. The source of these images is the 12-lamp module and film clip that are mounted behind each display position. When one of the lamps is lit, the light from it will shine through a corresponding part of the film mounted in front of it, and cause the film image to appear in reverse on the back of the frosted lens. The operator, who is seated facing the other surface of the lens, sees the image correctly. The image may be of words, numbers, characters, or messages, or it may be a colored background that can be used in conjunction with another image if two lamps are lit simultaneously, causing both to appear together. It is even possible to construct unique symbols or character shapes with the overlap feature of a 12-lamp projection display in some applications, though this is not done with the MX-3195(V). The message and word display are predetermined by the overlay and are usually code words. The data displays are either code words or numerals (0-9). An error caused by hitting several keys simultaneously may go undetected if a valid code results; however, an invalid code will cause a red lamp to be lighted and result in a red display (flood) for that digit position.

Beneath the displays are the Panel and Display brightness controls. These switches control the brightness of the lights for the display and keyboard panels. The rectangle between the Panel and Display switches is actually a recessed area of the front panel and has a hinged cover.

The Test switch is a rotary switch that is used to select the keyset operating mode. Position 1 is the normal operating mode, and positions 2 through 5 are test positions. The keyset address is a two octal digit number. The program selects the most significant digit (MSD) of the address, and the Address switch determines the least significant digit (LSD) of the address. The Address switch has a round can like cover that should be left in place to prevent accidental changing of the address. The Test and Address switches are an excellent place to start troubleshooting the keyset. If the keyset appears to be malfunctioning, check these switches to ensure that they are in the correct positions before taking further measures.

The four Message buttons permit entry of the primary identifier for the data word. This identifier places the data word within a unique grouping of words which together supply a prescribed block of information to the computer program. The eight Word buttons permit entry of a secondary identifier for the data word. This identifier indicates to the program the particular meaning of the data in the data word. The ten Data keys are used to enter six decimal numbers. The data entered may be purely numeric as indicated by the ten decimal numbers engraved on the keys or may include certain data subcoding that would be indicated on the plastic overlay. The keys on this keyboard must be used in a certain order. One Message key must be selected first, then one Word key followed by any six Data keys. Any other order will produce a no data (input ignored) condition. The bit positions for a keyset data word are shown in figure 5-46.

The Clear button clears the Error indicator, the data storage register and all the readout displays. The Error indicator is lighted on



124.463

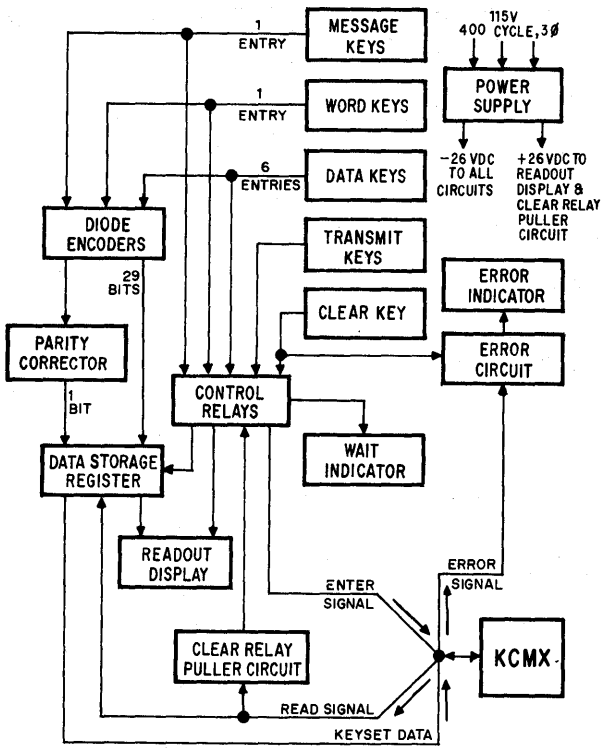
Figure 5-46.—Keyset data word.

computer command and indicates that an error (parity or format) has been detected in a previous data entry. Operator response is normally to reenter the correct data. The Wait light will stay lit from the time the Transmit key was momentarily depressed, until the keyset is interrogated by KCMX. During the time this light is on, all keys on the keyset are locked out, and the only method of clearing the keyset is by placing the Test switch in position 3 or by turning the power off and then on. The Transmit button initiates the control logic which results in the data word being transmitted to KCMX. Operation of this key DOES NOT force transmission; it merely indicates that data is ready and waiting for computer controlled interrogation. If the Transmit key is depressed before all Data entries are made, zeros will automatically be entered as the remainder of the Data entry. Depressing the Transmit key locks out the other keys until the data word has been accepted by KCMX.

The number of keysets will vary, depending on the particular installation. At present, five are being used in NTDS. The keysets are connected in series and are interrogated sequentially. Since there is no address identifier in the keyset data word itself (fig. 5-46), the computer's program associates the data word with a unique address in the KCMX (chapter 3 of Vol. 2). The KCMX may also be selected to transmit keyset data to the computer as interrupt data, in which case a portion of the data word is replaced, by the KCMX, with a unique identifier showing which keyset originated it. If the data does not conform to expected standards, the program produces a reasonableness error, lights the Error light on the keyset and rejects the data.

BLOCK DIAGRAM

The block diagram for the keyset is shown in figure 5-47. A typical keyset data entry is made by selecting nine keyboard keys in a fixed sequence: 1 message, 1 word, 6 data, then transmit. Each key, except for transmit, is assigned a binary code, as it is depressed by the diode encoder circuits. The Message, Word and Data entries are translated to two, three, and four-bit (respectively) binary numbers and placed in the data storage register for temporary



124.464

Figure 5-47.—Keyset block diagram.

storage prior to transmission to KCMX. During the data entry, parity corrector circuits maintain odd parity for the binary coded information being assembled in the data storage register for subsequent transmission (fig. 5-46).

The order of data entry is restricted to a fixed sequence due to the action of the control relays, which, in turn, enable and disable the three groups of keyboard keys. The control relays also control the order in which the readout displays are selected. The data entry is considered complete and correct if the code words and decimal information intended for transmission to KCMX are indicated in the readout displays. An error occurring in the data entry process will be indicated by incorrect data shown in the readout display.

Data transfer is initiated by depressing the Transmit button, causing an Enter signal to be placed on the keyset's Enter line to the KCMX. Depressing the Transmit button disables the

keyboard data keys and lights the Wait indicator until a Read signal is received from the KCMX.

Data transfer occurs when the computer requests (external function code) that the KCMX interrogate the keyset. As a result of this interrogation, the keyset's Enter line is monitored. If the Enter signal is present, KCMX transmits the Read signal, which effectively connects the keyset's data storage register to the data cable. The Read signal transfers the data from the storage register to KCMX. The KCMX then transmits the data word to the NTDS computer, using normal I/O interface signals.

The order of interfacing signals (signals between the different equipment) must, therefore, be:

(1) Keyset to KCMX: "I am holding a message for you" (ENTER signal is up)

(2) Computer to KCMX: "Interrogate Keyset for possible data for me" (external function acknowledge (EFA) signal up for KCMX function code)

(3) KCMX to Keyset: "I can accept your message now" (READ signal returned to Keyset)

(4) KCMX to Computer: "I have a Keyset message for you" (input data request (IDR) signal up)

(5) Computer to KCMX: "Message received" (input acknowledge (IA) signal up)

Of course, it is understood that each step is dependent upon the successful completion of the previous steps. Otherwise, the sequence would vary as the presence or absence of data, or the need for that data, dictates.

The keyset senses the end of the Read signal and initiates a partial clearing of its circuits through the clear relay puller circuit. The Control relays, Wait indicator, and Data portion of the Readout Display are cleared; however, the data remains displayed in the Message and Word units to remind the operator as to the subject of the last data entry. An Error signal will be sent to the keyset (depending on KCMX's mode of operation) if KCMX detects a parity error in the data transmission or by the computer via KCMX if bad parity or wrong data is detected.

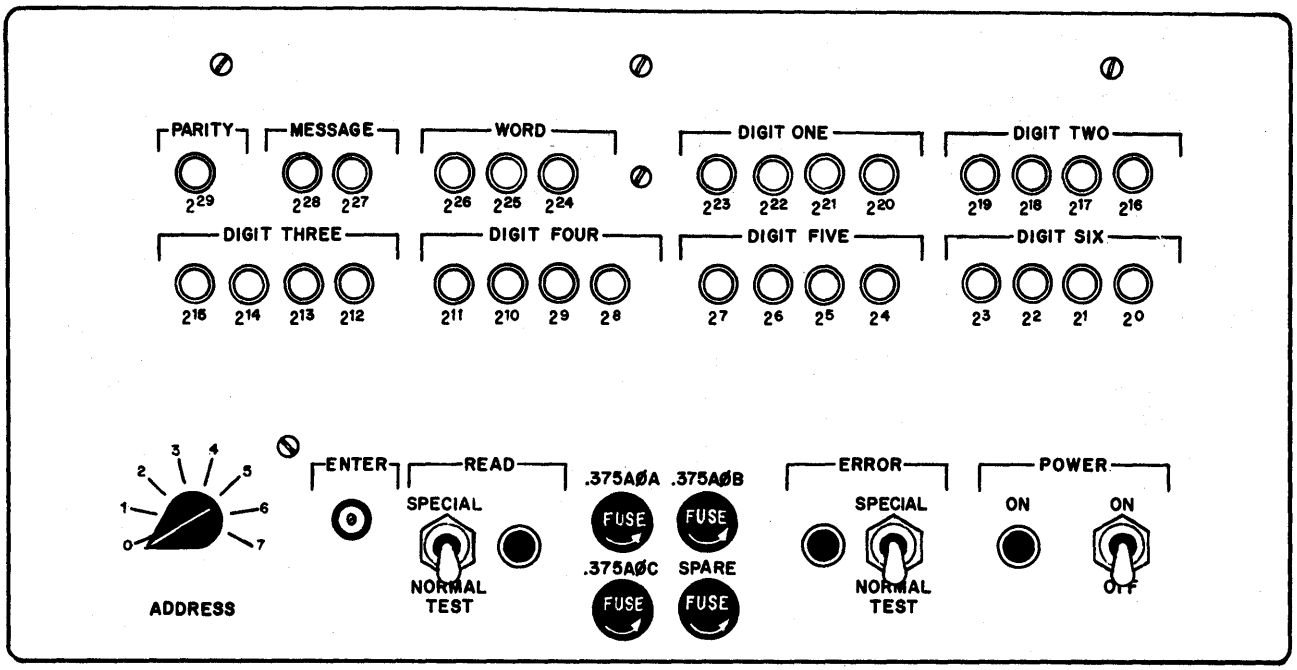
A new data entry is possible only after the keyset has been master cleared by the Clear button. This clears the Message and Word displays and the Error indicator if it was illuminated.

TROUBLESHOOTING

Generally, incorrect operation of the keyset will be evidenced in several ways; the data entry will not be correctly displayed in or cleared from the Readout Displays. The KCMX, or computer, may indicate a high percentage of data transmissions have bad parity or lack reasonableness from a given keyset. In the first case, the trouble probably is in the keyset. In the second case, the trouble may be due to faulty operation of KCMX, faulty data cables and connectors, or the trouble may be in the keyset. Additional indications of faulty operation will be noted by failure of the Wait and Error indicators to operate correctly.

There are two special purpose units of test equipment that may be used to troubleshoot the keyset. The Introducer Tester TS-1539/USQ-20(V), or "keyset tester", is used to supply the signal and monitor functions normally provided by KCMX. The Converter Tester TS-1538/USQ-20(V) is used in conjunction with the keyset tester to check the keyset operation under marginal input power conditions.

The keyset tester (front panel shown in figure 5-48) provides a means of testing a keyset apart from the KCMX, and of isolating a fault to the keyset while eliminating the KCMX, and possibly the data cables, as a source of the fault. The data cables must be suspected too, if the malfunction seems to exist between two pieces of equipment joined by data cables. Any multiwire cables used with test equipment are highly suspect, since they are attached and removed frequently. When troubleshooting data cables, it is advisable to think in terms of a possible open lead, shorted pins, lost ground return, or loose (intermittent) connection in either connector as perhaps causing the symptoms that have been observed. This is particularly true if the cables have recently been moved or replaced. Cable runs can sometimes be bypassed in an effort to isolate problems to the cable itself, but the only means of actually locating problems within the cable is with a series of resistive readings to determine



124.465

Figure 5-48.—Keyset tester control panel.

continuity (current paths) between identical pins in each connector and resistive readings from either end of the connector to other connectors and to the shielding to determine if any shorts have occurred. This is a time consuming task, but it is absolutely necessary if problems are suspected in a cable.

Sometimes a cable will be found that has unused leads left either open or shorted. These indicate a sloppy attitude in assembling the cable, but would not be indications of a defective cable. This makes it necessary to verify the function (if any) each pin connector has been assigned when checking a cable.

One technique that can be used with long cables is to short two pins at one end momentarily while checking continuity between the identical two pins at the other end with a meter. A low resistance should be read when the pins are shorted, and an open circuit should be read when the short is removed. This technique requires two technicians working harmoniously together with carefully coordinated movements, signals, or an adequate means of communication between them.

The keyset tester is equipped with the following features:

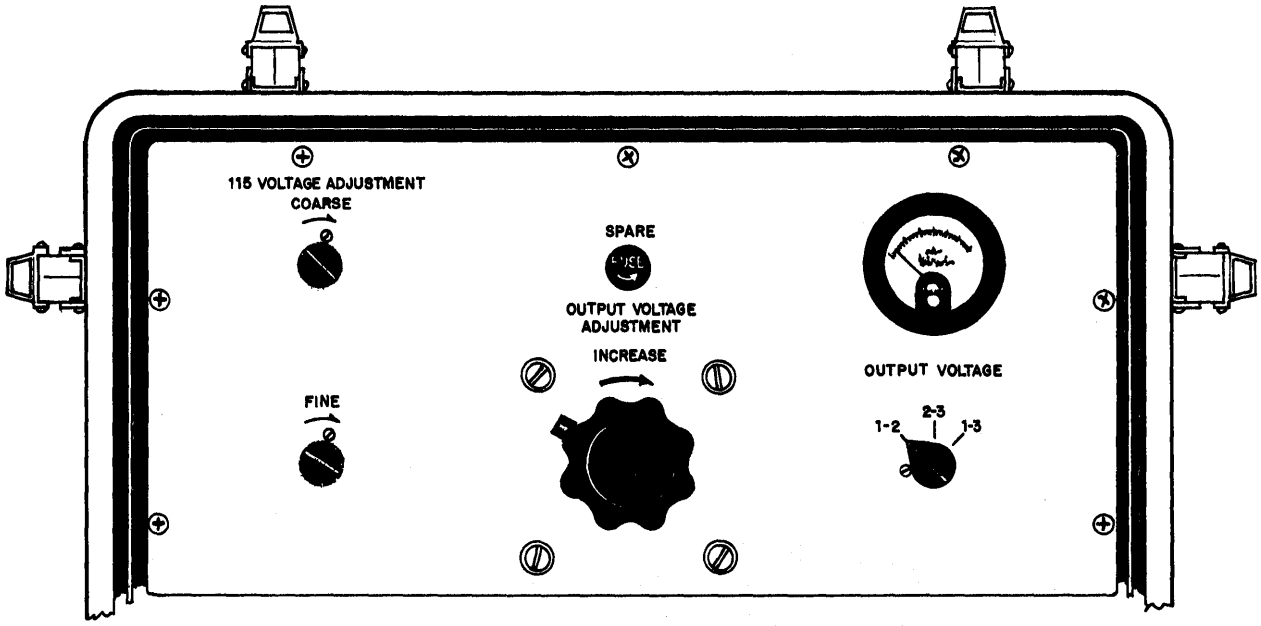
(1) It contains a 30-bit display to visually indicate the output of the data storage register.

(2) It provides either an intermittent or a constant Read signal for transferring the contents of the data storage register to the keyset tester. The Read signal also checks the clear relay puller circuit.

(3) It provides either an intermittent or a constant Error signal for activating the keyset error holding circuit.

(4) It is capable of checking the isolation diodes associated with each storage element of data storage register.

The converter tester (front panel shown in fig. 5-49) has three primary functions. It will provide 1) manual control of input line voltage to the equipment under test, 2) meter indication of line-to-line output voltages, 3) a variable source impedance for decreasing the positive 15-volt d.c. output of the equipment under test. The converter tester can be used to test other NTDS equipment such as the RD-243 magnetic



124.466

Figure 5-49.—Converter tester control panel.

tape unit. Refer to the appropriate technical manuals for instructions.

Figure 5-50 illustrates the manner in which the special test equipment and the keyset are connected to perform marginal testing. Information is entered into the keyset and displayed on the keyset tester to be checked for accuracy. Then the keyset is cleared or an error signal is sent from the test set with the results of both operations being observed on the equipment. The converter tester may be used to vary the voltages as needed to simulate failing or marginal components and introduce additional factors in the troubleshooting.

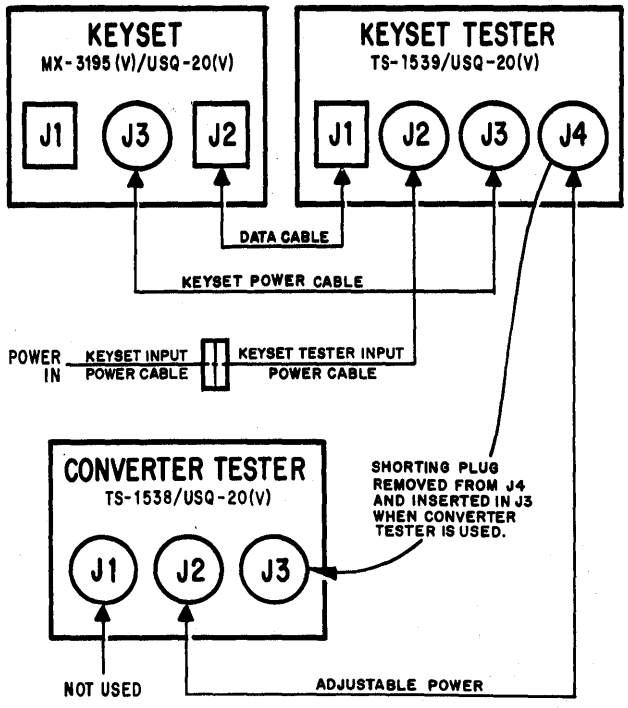
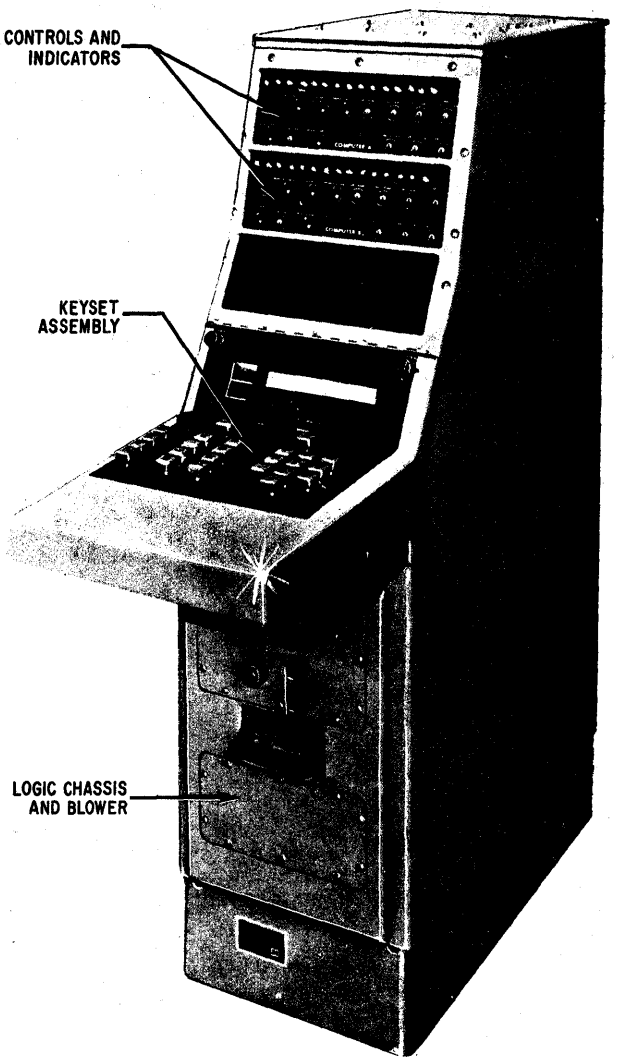


Figure 5-50.—Cabling diagram for marginal operation testing. 124.467

C-3675A/USQ-20(V) SYSTEM MONITORING PANEL

The C-3675A shown in figure 5-51 is one of five system monitoring panels (SMP) presently being used with the NTDS. The major differences between these five SMP's are limited to cabinet construction and physical locations of some of the computer control switches. All five operate the same way logically and perform



124.210

Figure 5-51.—C-3675A/USQ-20(V) System Monitoring Panel.

identical functions; therefore, only the C-3675A will be discussed in this text.

The SMP is a self-contained computer control and monitoring device, incorporating features of a keyset, but also providing a means of establishing remote control of and monitoring the more significant operations of each computer in a particular data processing system. A system may consist of two, three or four computers, that can be controlled by one SMP. Computer operations performed by the SMP are divided into the following three groups.

(1) Remote computer operations—A group of system monitoring controls is provided which duplicates some of the major computer controls for each computer, such as bootstrap, master clear, run, stop, etc. These functions are found on the SMP monitor control panel.

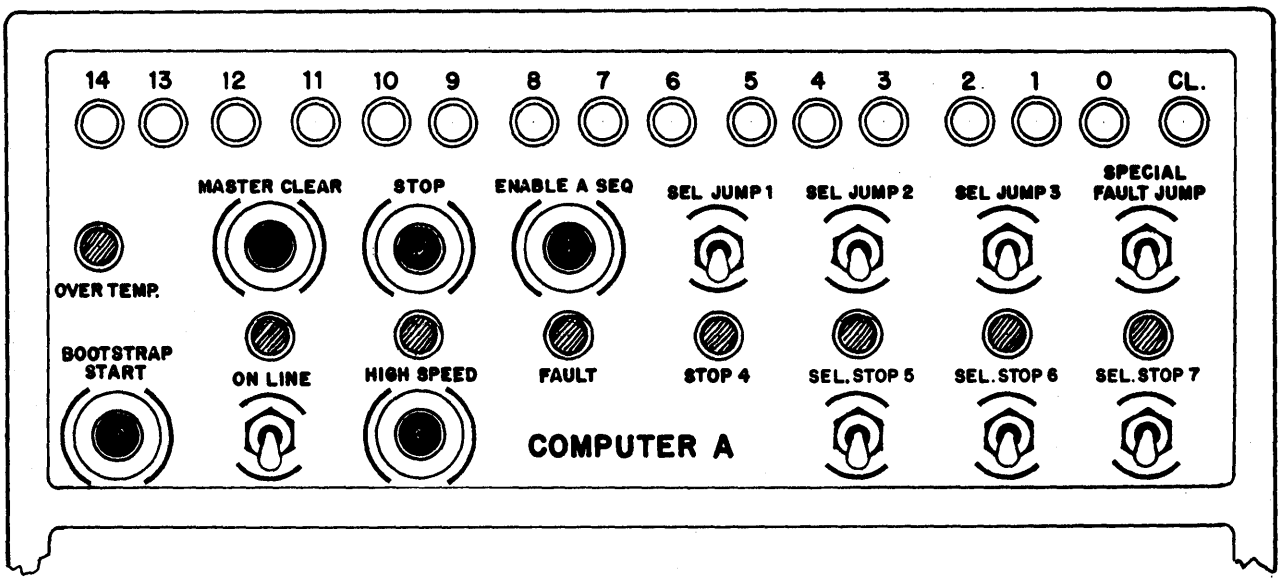
(2) Computer function commands—These commands are generated by the SMP keyset and are used for directing a portion of the operational program in a particular computer to perform certain operational functions. These are software functions, as opposed to the hardware functions available at the monitor control panel, and as such these are only functional with the appropriate software (the system program is loaded).

(3) Fault and computer indications—A group of indicators is provided which displays the communications faults between the computer and associated peripheral units or within the computer itself. These indicators also display amplifying information necessary to operate and monitor the computer system.

FRONT PANEL CONTROLS

Up to four separate monitor control panels (fig. 5-52) provide duplicate computer controls, one for each system computer. These controls permit the operator to load, reload, or control programs and to start, stop, or modify (by use of the selective stop or jump switches) the computing operations in any of the system computers. The monitoring panel also displays amplifying information for determining what conditions are occurring in a computer or system.

This is done using the neon indicator register on the upper portion of the monitor control panel. This 15-bit register coincides with the upper 15 bits of the computer output channels assigned to the SMP. The computer can place an external function on the associated channel EXF line and this will cause the SMP to display the upper 15 bits of the function word. The SMP will continue to display the last word received until another



124.468

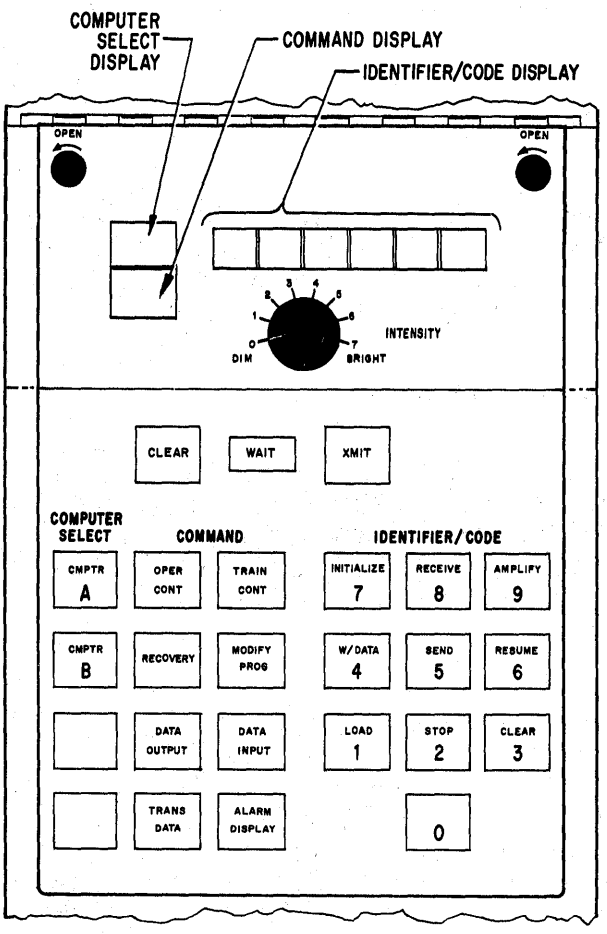
Figure 5-52.—Monitor control panel.

word is sent. The computer program is able to use this feature as a means of communicating information to the operator. For example, the utility program uses rapidly shifting strings of light to show tape motion of the program tape transport. If the string is moving left ("up") in the register, the tape is moving forward. If the string moves right ("down") in the register, the tape is moving backward. Another example is the blinking of bit 16 (LSB of the neon indicators) to indicate that the operational program has been loaded but has not yet been started ("initiated") in the corresponding computer. When bit 16 for each computer is flashing, the operator knows he can then initiate the multicomputer program. This is discussed in further detail in chapter 4 of Vol. 2. The fact that the program is running is indicated by a changing display.

The 15 neon indicators across the top of the panel also provide a visual display of information which reflects the operation (proper or improper) of a particular computer, subsystem or peripheral device. They also provide computer reply indications for the SMP operator. Indications will vary, depending upon function and program involved, but in many cases can be interpreted easily in that they are intended to help the operator keep his place as he makes a series of entries. For instance, if three entries were required, the program might show a ØØØØ1, ØØØØ2, and ØØØØ3 prior to each entry. Or the program might show ØØØØ1, ØØØØ2, ØØØØ4, in which case the first bit represents the first entry, the second bit represents the second entry, etc. If computer addresses are involved, the display might be of the present address being referenced, or the next address to be referenced.

Whatever the indication is, it usually means that a change to the contents is performed each time to mark when the manually entered data via the keyset portion of the SMP has been acted on by the computer. If the indications cannot be readily understood by the operator in terms of the task being performed, the program documentation should provide some explanation, or the operator can ask any of the OS personnel, since they are usually capable of answering such questions.

The information displayed by these indicators is constantly updated by the operational program when it is running. The On Line toggle switch activates the monitoring panel controls for the associated computer and causes the computer maintenance panel controls to be disabled, provided that the Local/Remote switch on the computer maintenance panel is in the remote position, and that the computer is not running on margins (chapter 4). The Bootstrap Start and Special Fault Jump switches correspond to the Auto Recovery switch (down and up positions respectively). The other indicators and switches correspond to the labeling and operations of the indicators and switches on the computer maintenance panel.



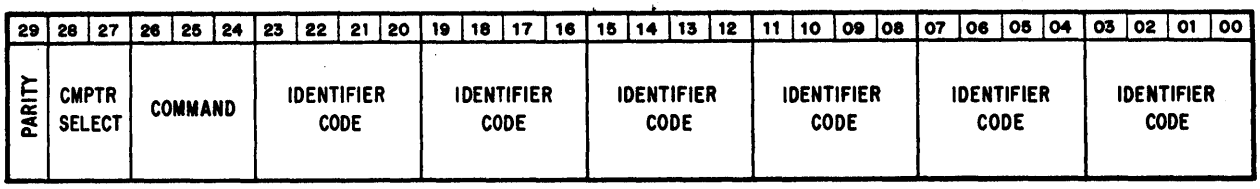
124.469

Figure 5-53.—SMP keyset panel.

The keyset panel and display indicators (fig. 5-53) are located immediately beneath the monitor control panels. This keyset keyboard is used in the same manner as the keyset previously described, except the labels are different. The Computer Select keys (4) determine which computer is to be referenced. One of the Computer Select keys must be the first entry. One of the eight Command keys must be the second entry. Any six of the Identifier/Code keys may be selected as the third button action, in which case the Identifier (as it is called) acts to modify the command (second input). The remaining five inputs could be a data code to be used in conjunction with the command/identifier by the designated computer, or they might be further identifiers, depending upon the program interpretation. The functions of the Command and Identifier/Code keys are dependent upon the installation requirements of the system program. The function of the Transmit and Clear buttons and the Wait indicator have previously been described. Note that there is no Error indicator on this keyset. Data entry errors are displayed in the neon indicators of the monitor control panel. The error display is usually 77777_8 (all bit indicators lighted), but this is a program function and may be changed. The keyset entry prior to transmission is displayed in the keyset display indicator panel above the keyboard.

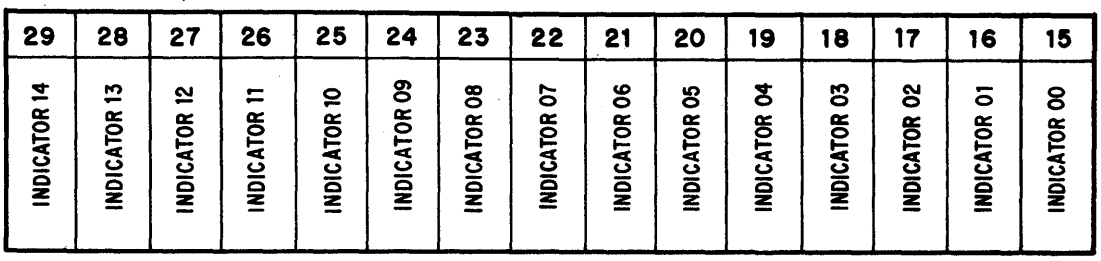
OPERATIONAL CHARACTERISTICS

The SMP operates as a peripheral device in a computer system, and as such it must use external functions (from the computer) and interrupts (from the SMP) to transfer data. Data from the SMP are called Action Codes and contain the information entered at the keyset. Action Code format (fig. 5-54) is the same format (bit positions) as the data from any keyset, but again the labels are different. To transmit information from an operator to the computer, the information must first be entered into the keyset and displayed in the Identifier/Code displays (fig. 5-53). After it is verified and corrected, the Transmit button is depressed, and an interrupt signal is generated. This interrupt lights the Wait indicator and notifies the computer that data is on the lines to



124.470

Figure 5-54.–SMP action code format.



124.471

Figure 5-55.–SMP external function code word format.

be sampled. The computer samples the data when time is available and sends an Input Acknowledge signal. The Input Acknowledge clears the Wait indicator and the Identifier Code displays. The Computer Select and Command displays remain activated to speed inputting of several related data entries.

The computer communicates output data to the SMP by external function codes. The format for these codes is shown in figure 5-55. The computer sets the appropriate bits positions, then sends the external function command. The bits set in the external function word light selected indicators of the Channel indicators on the monitor control panel (fig. 5-52). The light patterns that appear in the Channel indicators are a function of the program and must be interpreted and/or evaluated by the operator. The normal pattern, used with the NTDS operational program, is to have the Channel indicators for on-line equipment blinking at a two-second rate to indicate proper operation. An error for a specific I/O channel is indicated by a constantly set light for that channel. The error indication must be amplified (get more data about error from program) by the operator using the keyset. This amplifying information is then interpreted by the operator to determine the specific equipment or program problem.

BLOCK DIAGRAM

Figure 5-56 is a simplified block diagram of a two computer SMP. The Channel Indicators are used to present to the operator data from the computer. This data is Anded with the External Function in the indicator logic circuits, and the outputs are used to light the neon indicators.

The Computer Remote controls are duplicates of computer switches and the indicators. These switches control computer operations from the SMP. The Control Indicators display various conditions in the computers as they are operating (e.g. Fault, Over Temp, Stops, etc.).

The keyset assembly operates in the same fashion as the MX-3195. The data storage relays

operate as a data storage register and hold the information to be transferred to the computer. The interface circuits for the data lines are necessary to make the data storage relays compatible with computer input circuits.

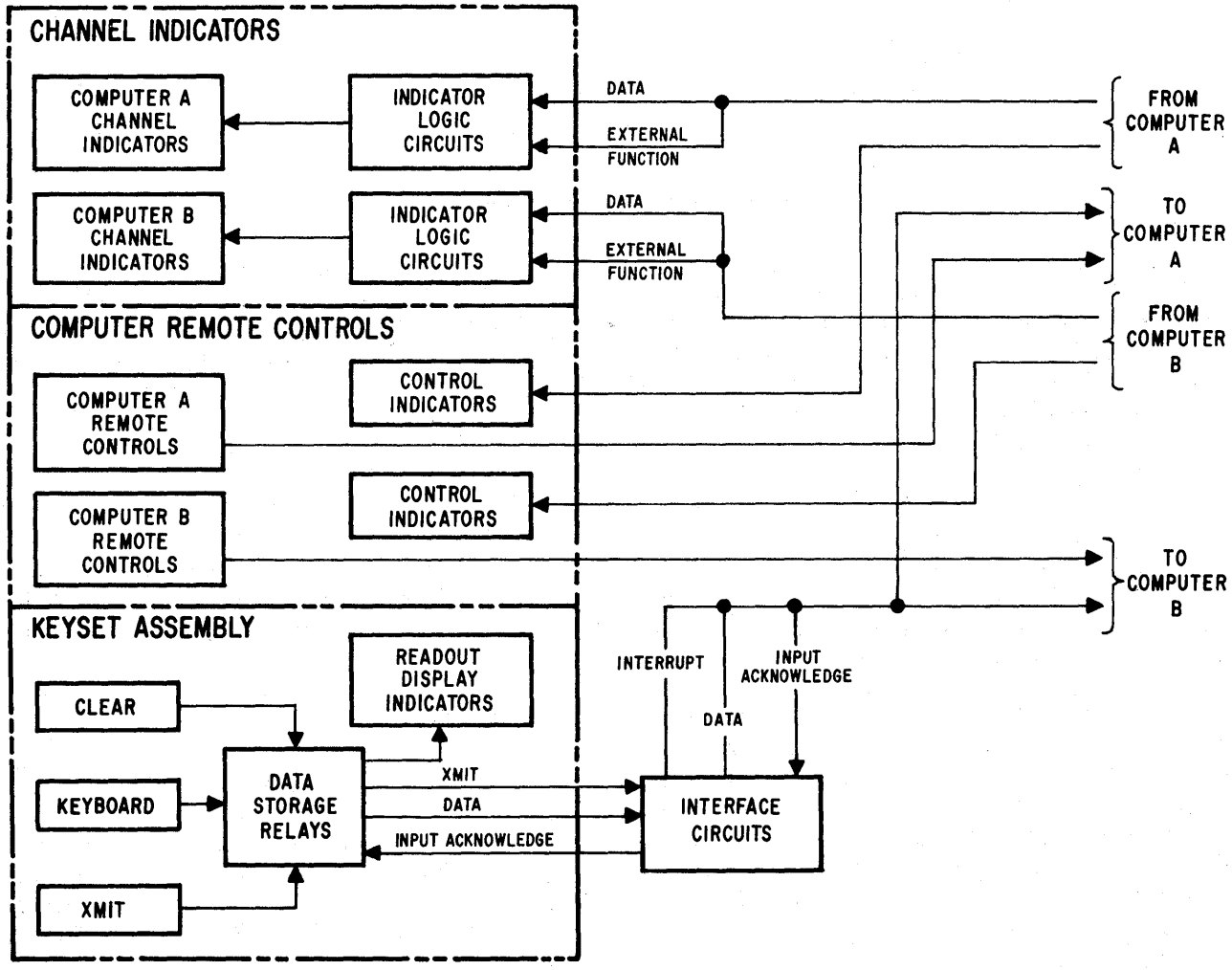
TROUBLESHOOTING

There are no special troubleshooting methods, techniques or test equipment that are used with the SMP. Logical troubleshooting techniques and the available test programs should resolve most malfunctions of the SMP.

Logic Symbology For Peripheral Equipment

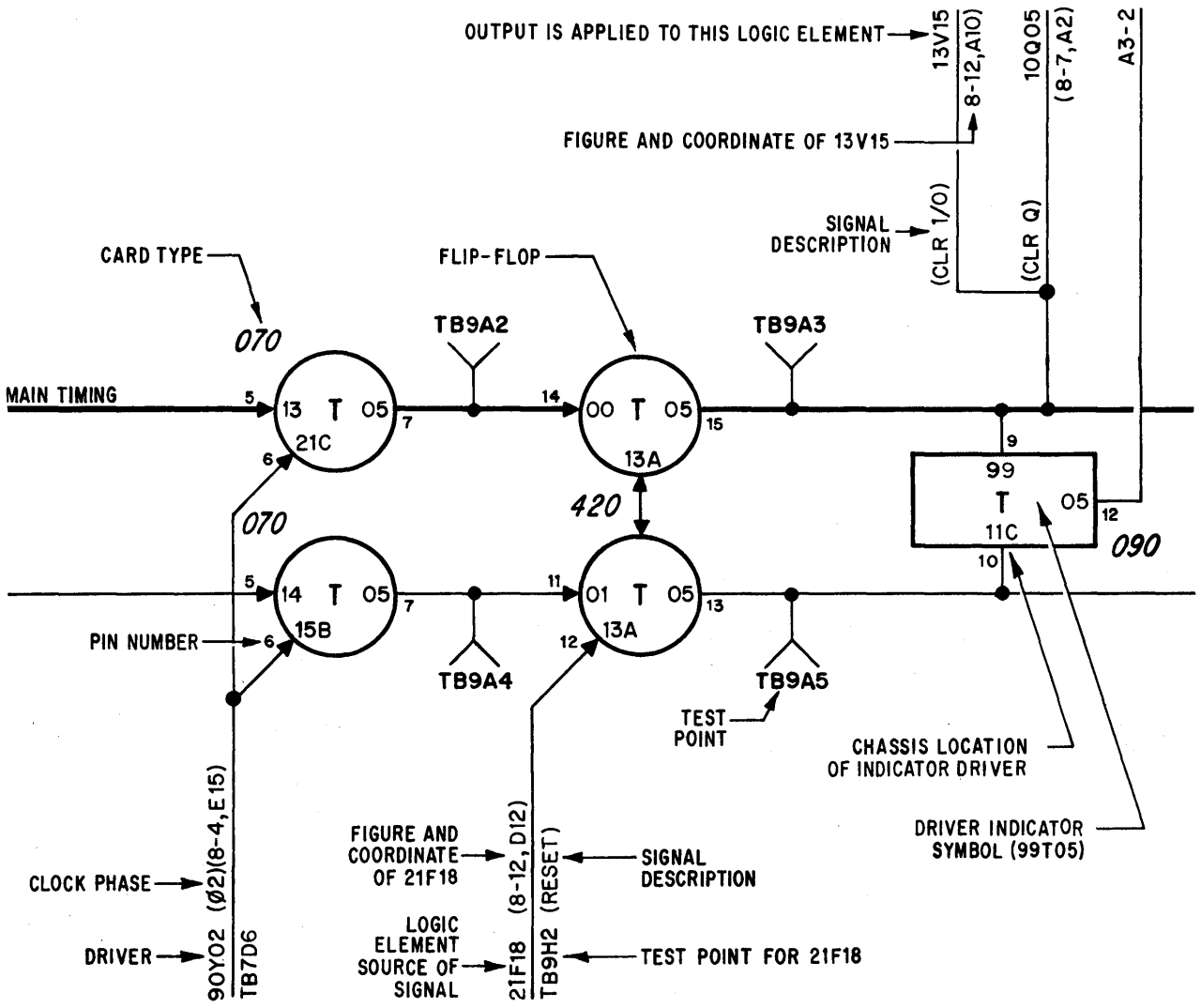
The logic symbology used in the functional schematics for the peripheral equipment discussed in this chapter is shown in figure 5-57. The symbology for the CP-642B Computer was produced according to Mil-Specs. The symbology for the peripheral devices is called NOR or bubble logic and was completed prior to Mil-Specs. Any "1" in produces a "0" out; all the inputs must be "0" to produce a "1" output.

The inputs to the functional schematics are usually from the left side or bottom of the page, and each line is labeled with the figure and



124.472

Figure 5-56.—SMP block diagram.



124.473

Figure 5-57.—Logic symbology.

coordinates of the source logic element. The output test point for the source logic element is also given, and some of the inputs are labeled with a signal description. The outputs are from the top or right edge of the page and are labeled in the same manner as the inputs.

The logic elements on a functional schematic are labeled with nomenclature unique to those symbols. The card type and chassis map locations are also shown. The test point and chassis map designations correspond to those used in the CP-642B.

APPENDIX I

AN ABBREVIATED GUIDE TO ELECTRONICS ABBREVIATIONS

The use of abbreviations and acronyms in electronics literature enhances the reading, the writing, and the comprehensibility of information exchange. However, the pervasiveness of such terms has made understanding more difficult for many readers who are not familiar with specialized aspects of the technology under discussion. This alphabetized list of more than 150 terms has been compiled from a large group of technical periodicals. Since new abbreviations are constantly being generated, readers can add new definitions as they are encountered.

a-d	analog to digital
ADS	address data strobe
AIM	avalanche-induced migration
ALU	arithmetic/logic unit
ANSI	American National Standards Institute
AOI	AND/OR invert
ASCII	American Standard Code for Information Interchange
ATE	automatic test equipment
ATS	automatic test system
BBD	bucket-brigade device
BCD	binary-coded decimal
Boram	block-oriented random-access memory
b/s	bits per second
CAD	computer-aided design
CAM	content-addressable memory
CATT	controlled avalanche transit time
CCD	charge-coupled device
CML	current-mode logic
C-MOS	complementary-metal-oxide semiconductor
CMRR	common-mode rejection ratio
CPU	central processing unit
CROM	control read-only memory
CRT	cathode-ray tube
CRC	cyclic redundancy check
CVD	chemical-vapor deposition
CVT	constant-voltage transformer
d-a	digital to analog
DAS	data-acquisition system
DFA	digital fault analysis
DI	dielectric isolation
DIP	dual in-line package
DMA	direct memory access
DMAC	direct-memory-access control
DMM	digital multimeter
D-MOS	double-diffused metal-oxide semiconductor
DMS	dynamic mapping system
DMUX	demultiplexer
DPM	digital panel meter
DTL	diode-transistor logic
DVM	digital voltmeter
Earom	electrically alterable read-only memory
EBCDIC	extended binary-coded-decimal interchange code
ECL	emitter-coupled logic
EDP	electronic data processing (or processor)
EFL	emitter-follower logic
EFTS	electronic funds-transfer system
EOC	end of conversion
EPROM	erasable programable read-only memory
EROM	erasable read-only memory
ESS	electronic switching system

Extnd	extended data transfer
FDM	frequency-division multiplex
FET	field-effect transistor
FFT	fast Fourier transform
FIFO	first in, first out
FPLA	field-programable logic array
F-PROM	field-programable read-only memory
GDS	graphic data system
HiNIL	high-noise-immunity logic
HTL	high-threshold logic
IC	integrated circuit
ICE	in-circuit emulator
IDS	input-data strobe
IEC	infused emitter coupling
I^2L	integrated injection logic
I/O	input/output
J-FET	junction field-effect transistor
JI	junction isolation
Laput	light-activated programable unijunction transistor
LASCR	light-activated silicon controlled rectifier
LCD	liquid-crystal display
LED	light-emitting diode
LIC	linear integrated circuit
LIFO	last in, first out
LNA	low-noise amplifier
LPTTL	low-power transistor-transistor logic
LRU	least recently used
LSB	least significant bit
LSI	large-scale integration
MDS	microprocessor-development system
MESFET	metalized semiconductor field-effect transistor
MHL	microprocessor host loader
MIS	metal insulator silicon
MLA	microprocessor language assembler
MLB	multilayer board
MLE	microprocessor language editor
MNCS	multipoint network control system
MNOS	metal-nitride-oxide semiconductor
Modem	modulator/demodulator
MOS	metal-oxide semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
μP	microprocessor
MPU	microprocessor unit
MSB	most significant bit
MSI	medium-scale integration
MTBF	mean time before failure
MTD	mass tape duplicator/verifier
MTTF	mean time to failure
MUX	multiplexer
NAND	inverted AND gate
NDRO	nondestructive readout
n-MOS	n-channel metal-oxide semiconductor
NOR	inverted OR gate
NRZ	non-return to zero
NRZI	non-return to zero inverted
OCR	optical character recognition
ODS	output data strobe
OEM	original-equipment manufacturer
OPAL	operational performance-analysis language
PAR	program-aid routine
pc	printed circuit
pcb	printed-circuit board
PDP	plasma display panel
PIA	peripheral interface adapter
PLA	programable logic array
PLL	phase-locked loop
PM	phase modulation
PMG	permanent-magnet generator
p-MOS	p-channel metal-oxide semiconductor
POS	point of sale
PPI	plan-position indicator also, programable peripheral interface
PRACL	page-replacement algorithm and control logic
PROM	programable read-only memory
PTH	plated-through holes
PUT	programable unijunction transistor
RALU	register and arithmetic/logic unit
RAM	random-access memory
RIM	read-in mode
RMM	read-mostly mode
ROM	read-only memory
RTL	resistor-transistor logic
R/W	read/write
SBS	silicon bilateral switch
SC	semiconductor
SCA	subchannel adapter
SCR	silicon controlled rectifier
SDLC	synchronous data-link control
S/H	sample and hold
SIP	single in-line package
SOS	silicon-on-sapphire
SSI	small-scale integration
SUS	silicon unilateral switch
TBMT	transmitter buffer empty
TTL	transistor-transistor logic
T^2L	transistor-transistor logic

TTY	teletypewriter
TWT	traveling-wave tube
UART	universal asynchronous receiver/ transmitter
URCLK	universal receiver clock
Usart	universal synchronous/ asynchronous receiver/ transmitter
USRT	universal synchronous receiver/ transmitter
UTCLK	universal transmitter clock
UUT	unit under test
VCO	voltage-controlled oscillator
VIL	vertical injection logic
VTR	video-tape recorder
XOR	exclusive-OR gate

APPENDIX II

MINIATURE COMPONENT REPAIR BIBLIOGRAPHY

National Aeronautics and Space Administration Publications (NASA):

1. *Reliable Electrical Connections (Soldering), Technology Handbook,* Office of Technology Utilization, NASA, Washington, D.C. 20402, 1967

2. NHB 5300.4(3A) *Requirements for Soldered Electrical Connections,* 1968 ed., Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402

3. NASA SP-5002 *Soldering Electrical Connections,* 4th ed., 1967, Superintendent of Documents, U.S. Government Printing Office, Washington, D.C. 20402

4. NASA TM X-53335 *The Effect of Gold Plating On Soldered Connections,* NASA Technical Memorandum, Office of Technology Utilization, NASA, Washington, D.C. 20402, 1965

NAVAIR Publications (Manuals):

1. NA 00-25-544 *List of Specifications and Standards (Book Form),* Approved by the Naval Air Systems Command, July 1970

NAVPERS Publications (Manuals):

1. NAVPERS 93394 *Servicing Techniques for Transistorized and Printed Circuits,* January 1967

NAVWEPS Publications (Manuals):

1. NW 00-15PA-1 *Soldering for Electric and Electronic Application,* 1961

2. NW 00-15PA-1A *Training, Qualification, and Certification Guide for Solderer–Inspector Personnel,* 1965

Commercial Publications:

1. *Design Guidelines for Producibility and Repairability of Electronic Assemblies,* PACE Inc., 9337 Fraser St., Silver Spring, Maryland 20910

2. *General Operating and Maintenance Instructions–Sodr-X-Tractor SX300,* PACE Inc., 9337 Fraser St., Silver Spring, Maryland 20910

3. *Solder–Its Fundamentals and Usage,* 3rd ed., Kester Solder Co., 4201 Wrightwood Ave., Chicago, Illinois 60639

4. *Solders and Soldering,* Howard H. Manko, McGraw-Hill Book Co., New York, New York 10036

5. *The PACE Rework and Repair (R&R) Technology Series,* Vol. 1, 2, 4, 5, 6, 7, and 8, PACE Inc., 9337 Fraser St., Silver Spring, Maryland 20910

APPENDIX III

PARTIAL LISTING OF POSITIVE AND NEGATIVE POWERS OF TWO

	14	0.00006103515625
	13	0.0001220703125
	12	0.000244140625
	11	0.00048828125
	10	0.00097656625
	9	0.001953125
	8	0.00390625
2^{-N}	7	0.0078125
	6	0.015625
	5	0.03125
	4	0.0625
	3	0.125
	2	0.25
	1	0.5
	0	1.0
	1	2
	2	4
	3	8
	4	16
	5	32
	6	64
	7	128
	8	256
	9	512
	10	1024
	11	2048
	12	4096
	13	8192
	14	16384
2^{N}	15	32768
	16	65536
	17	131072
	18	262144
	19	524288
	20	1048576
	21	2097152
	22	4194304
	23	8388608
	24	16777216
	25	33554432
	26	67108864
	27	134217728
	28	268435456
	29	536870912
	30	1073741824
	31	2147483648

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