

UNIVAC[®]
HIGH-SPEED PRINTER

DESCRIPTION
AND
THEORY

PX 616

JULY 1957

Remington Rand Univac

DIVISION OF SPERRY RAND CORPORATION

UNIVAC PARK, ST. PAUL 16, MINNESOTA

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i. INTRODUCTION

This Manual has been produced as an aid to personnel receiving training on the technical aspects of the Remington Rand Univac High-Speed Printer, and as a guide in logical fault-determination. A thorough understanding of the logics involved in the operation of the HS Printer will be of invaluable assistance in determining the area involved in any particular fault.

The Manual should be read in conjunction with the "Programmer's and Operator's Manual for the High-Speed Printer" also published by Remington Rand Univac Division of Sperry Rand Corporation, as the text herein makes frequent reference to Operator's or Programmer's procedures. A knowledge of these procedures is necessary in order to understand the problems that may be encountered by these personnel in operating the Printer.

Although the text of the Manual is, for the most part, devoted to logical theory, it has been necessary at times, due to the very nature of the machine, to explain the operation of a particular area of the equipment by means of electronic or mechanical theory. For a person who may be unfamiliar with the fundamentals of these fields, such portions of the text have been marked at the beginning and end of the section with a single and double asterisk respectively. By passing by these portions, such persons will not necessarily be deprived of a knowledge of portions of the equipment which may be beyond their scope.

The Manual does, however, presuppose a knowledge of binary computation on the part of all readers, and, if this prerequisite is not existent, it is recommended that any good text on the subject be consulted. Further information respecting the Remington Rand Uniservo, which is mentioned frequently in the text and is an operating adjunct to the HS Printer, may be obtained by referring to Remington Rand publications specifically written for the Uniservo.

In many places throughout the text, specific typographic symbols have been mentioned without enclosing the symbol itself in quotes, as is the usual method of representation. For example, "..... the hammer prints the symbol % when the solenoid is actuated....." This apparent omission has been purposely applied, inasmuch as including the quotation marks may confuse the reader by implying that the quotation marks themselves are included in the printing operation in the example given, a condition which could quite conceivably occur.

In nearly every instance throughout the text, following the discussion of certain Printer functions, one or more practical examples are given in order to amplify the explanation. It should not be considered that the examples quoted are the only possible situations that may occur, the examples being merely representative of such situations. It is considered also that by detailing these examples a very thorough idea of the circuit logic may be imbued in the reader, this being of considerable value in fault determination.

Figure A, at the end of the Manual, which logically represents the whole High-Speed Printer system less power supply, should be referred to constantly in studying the text, together with such individual area drawings that are included throughout the Manual.

ii. GLOSSARY and ABBREVIATIONS

The terms and expressions used in this Manual are germane to the Univac High-Speed Printer, and do not necessarily reflect the general use of these terms as expressed in other Univac publications or the computer field in general. Wherever possible, if a term or expression has two or more meanings or has equal use throughout the Univac system, all possible alternatives are given.

The use of abbreviations has been kept to a minimum in this text although in cases where a term, expression or symbol appears in numerous places within a Section or sub-Section, the word is written in full initially, with the abbreviation in parentheses following. Subsequent repetitions of the expression throughout the remainder of the Section will usually be abbreviated.

Adder	See Quarter Adder.
Address	Refers to the selection of a particular Memory location. Address line, Address gate are associated terms.
Alert	Refers to a preparatory signal, usually on a gate. The final enabling or permitting signal will not be identified as an "alert."
All-Out Detector	A circuit which notes the condition of all Check tubes, to insure that each is extinguished when required.
Amplifier	A circuit used to invert and develop a signal of some specifically required amplitude.
Bad Spot	An area on Univac magnetic tape that is faulty due to some reason. Holes are punched two and one-half inches prior to the appearance of a bad spot on a tape, and two and one-half inches following a bad spot, and each two and one-half inches throughout the bad spot. A photo-electric cell detects the faulty area and activates the appropriate circuits.
Binary Counter	Refers to a bi-stable device that is used for counting. One used alone can count to two; two can count to four; three can count to eight. The Univac code and the majority of counting in this equipment is based on a binary counting system.
Block	A unit of measure used in the Univac system. A block equals 720 characters, sixty words, or six blockettes.

Blockette	A unit of measure used in the Univac system. A blockette equals 120 characters, ten words, or one-sixth of a block.
Brake, Paper Feed	A device located on the Paper Feed clutch assembly and used to stop the rotation of the Paper Feed Tractors.
Brake, Servo	A device located on the servo clutch assembly for the purpose of stopping rotation of the capstan.
Breakpoint	A Univac character representing a flexible "stop" signal. It may be observed visually by actuating a switch located on the Supervisory Control Panel.
Buffer	A device permitting a signal to pass in only one direction. When several signals are brought together to a common output a buffer will be used to prevent each signal from passing back along another path. In this sense the buffer acts as an isolating medium.
Capstan	The device used to move the tape past the Read Head.
Carriage	A mechanical component used to move the print wheel and ribbon to and from the paper and print head area.
CC	Charge Capacitor
CE	Charge Error.
Center Drive	The drive-shaft assembly controlling the feeding of tape.
Channel	1) A term used to designate an area of the magnetic tape on which one particular binary digit of the Univac code is present, e.g., Sprocket Channel. 2) An area of the paper loop used in the programming of the Printer.
CIF	Clear Input Flip-flops.
Character	A Univac unit of measure, composed of seven binary digits standing for one digit, alphabetic, or special symbol. Twelve characters equal one word, one hundred and twenty equal one blockette.

Clear	To restore a storage or memory device to a prescribed state, usually zero.
Clear Pulse	A signal from the Code Wheel which synchronizes the Code Wheel Generator with the Code Wheel.
Clutch, Paper Feed	The device used to couple the paper drive tractors to the typewheel drive motor.
Clutch, Servo	The unit which engages the capstan and the center drive motor on the Uniservo.
Code Generator	A six-stage binary type counter with six outputs that correspond to the Univac code. The Code Wheel Generator is controlled by the Code Wheels.
Code Wheels	Three wheels with polished flat portions. The wheels are used to synchronize the print wheel to the print head print circuits.
Commutator, Paper Feed	Three commutators having two, three, and six polished flat areas, and used to control paper spacing.
Comparator	A device used to compare the output of the Code Wheel Generator with the information stored in the Memory. A signal is produced when the information agrees, which causes a printing action to occur.
Computer Digit	A special High-Speed Printer function. The Univac code contains certain characters which are considered "non-printable." The characters are usually function symbols or symbols which initiate an operation. The Computer Digit function will recode a non-printable character to a character that may be printed.
Counter, Main	A series of seven binary counters used to select Address lines and to count index pulses. A count may be made to a total of one hundred and twenty-eight.
Counter, Ring	A loop of interconnected bi-stable elements such that one, and only one is in a specified state at any given time, and such that, as input signals are counted, the position of the one specified state moves in an ordered sequence around the loop. In the High-Speed Printer this is a six-stage counter for Multiline operation.
CV	Control Voltage.

De-ion	A signal which alerts the Keyed B+ circuit and provides a Not Reading (NR) signal.
Delay Flop (DF)	See "Circuit Symbols" section of this manual.
Delay Flop, Retriggerable (RDF)	See "Circuit Symbols" section of this manual.
Delay Line	A device used to delay a signal a definite amount of time. (See SP ₁ , SP ₂).
Differentiator (Dif, D)	A device, the output of which is proportional to the derivative of the input signal. Spec., an RC circuit with a time constant equal to one tenth or less of the input signal. The output that is used, leading edge or trailing edge, will be determined by LE or a TE being lettered within the symbol. (See also "Circuit Symbols" section of this Manual).
Digit	A unit of measure equal to one character. One hundred and twenty digits comprise a blockette.
Enable	As used in this text, a permissing signal which permits a pulse (or signal) to pass a gate. Depending upon circumstances a gate may require more than one enable in order to pass a signal (be enabled).
Extinguish, -ed	Non-conducting, dark, off.
Fast-Feed	A machine function used to move the paper a pre-determined distance non-stop. There are six fast-feed circuits on the High-Speed Printer.
Field	Zones specified by plugboard connections where it may be desired to suppress zeros to the left of the most significant digit in any numerical portion of a blockette.
Fire, -ed	Conducting, ignited, on.
Flip-Flop	A device having two stable states and two inputs. The circuit remains in either state until caused to change to the other state by application of the corresponding signal.
Function Table	A circuit designed to accept information coded by one method and convert this information to another code. For example, binary to decimal.

Function Table One	The function table used to decode Univac non-printable characters into the particular special function each is required to perform, also known as "Special Symbols Decoder."
Gate	A circuit having an output and some or many inputs so designed that the output is energized when certain input conditions are met. In this Manual the first signal to a gate is usually referred to as an alerting signal or an alert, and the signal completing the gate requirements is referred to as a final enable.
General Clear (GC)	An operating function to clear the machine to a static condition.
Head Amplifiers	Components within the Uniservo amplifying the information received from magnetic tape.
Home Paper	The machine operation used to correctly position the printer form in relation to the paper loop.
Hub	The receptacle for a plugboard interconnecting cable assembly. More frequently referred to as a "jack" in this text.
ICD	Inhibit Center Drive.
Inhibition, Inhibit	A signal, (usually placed on a gate), which prevents an output from occurring. Also known as a "disable."
Integrator, Integrating, Int	An RC circuit with a time constant equal to ten times, or greater, than the applied signal.
IS	Initial Start signal.
Jam, Jamming	A continuing voltage level which prevents other signals from influencing a circuit.
Jam Clear	A signal used to clear the Input Flip-Flops.
Keyed B+	A signal from the Memory regulated power-supply which is used to extinguish the trailing edge of the output of the Memory tube. It is used to "clear" the Memory.
LE	Leading Edge.
L Function Table	The smaller, eight line output section of the Minor Address function table.

L Lines	The output lines of the L Section Minor Address function table.
Major Address Function Table	The function table used to decode the Minor Address function table outputs in order to select the various address lines.
Memory	A part of the equipment composed of 840 Memory units arranged in 120 groups of seven, in which 120 characters, or one blockette, may be stored.
Memory Location	A device composed of seven Memory cells in which one character may be stored.
Memory Unit	A bistable electronic unit in which a binary digit of information may be stored.
M Function Table	The major section, fifteen line output of the Minor Address function table.
Minor Address Function Table	The function table used to change the binary output of the main counter into a code suitable for the Major Address Function Table, in order to select a correct Address line.
MRS	Manual Read Start.
MTO	Multiline Time Out.
Multiline	A machine operation that permits one blockette of information to be printed on from two to six lines.
Mylar Tape	A special plastic tape used as a buffer between the Read Head and the metal magnetic tape. The Mylar protects the Head from dirt and wear.
Mylar Drive	A motor unit used to move the Mylar Tape over the Read Head at constant rate.
NR	Not Reading signal.
Odd-Even Pulse, Signal, (O.E)	The odd-even or check pulse has been added to the Univac code for purposes of checking. All characters must have an odd number of binary digits. This is accomplished by the addition of an odd-even pulse when required.
Paper Loop	A punched paper tape loop composed of seven channels and used to control Fast-Feed and Home Paper operations.

PC	Print Check.
PCG	Probe Code Generator.
Permissive	See "Enable."
Plugboard	A unit that permits versatile operation of machine functions by means of a flexible inter-connection system composed of metal-protected cables, similar to a telephone patchboard.
PM	Probe Memory Signal. The context or symbolic representation in this Manual will preclude the possibility of this abbreviation being confused with the abbreviation for "Photomultiplier."
PM	Photomultiplier tube.
P-PM	Print, minus Probe Memory.
PP	Prevent Print.
Print Actuator	A solenoid-operated device that actuates the print hammers. Located on the Print Head, there are 130 of these components.
Print Cycle	The operation during which comparison and printing occurs.
Printer	A synonym used throughout the text of this Manual to denote the High-Speed Printer.
Print Hammer	One of 130 metal hammers that are sharply forced against the Print Wheel by the print actuators. The hammers are located on the Print Head.
Print Head	This chassis, located on the Printer unit, contains 130 print hammers and 130 print actuators. The Print Head and the Print Wheel perform the actual printing operation.
Print Location	The HSP has 130 circuits that control the actuating of 130 print-hammers. Each of these circuits is composed of a Check thyatron and a Print thyatron tube. These circuits are referred to as Print Locations.
Print, No Read (PNR)	A Printer operation that permits the repeated printing of information stored in the Memory. New information is not read-in during this operation.

Print Wheel	A series of sixty-five wheels, each containing two rows of type. Each row of type contains the fifty-one printable characters. The wheel rotates at a speed of 750 rpm.
Quarter Adder (QA)	A circuit used in the odd-even checking of the binary digits read from the tape. Two inputs, or no input results in a lack of output, whereas an input to either side results in an output.
Read Cycle	A major machine operation devoted to reading one blockette from magnetic tape and storing it in the Memory.
Ribbon Feed	The unit which holds the ribbon and controls the rate of travel of the ribbon.
Read Head	The device used to read eight channels from the magnetic tape. Located on the front panel of the Uniservo.
Read (One-Blockette) Backward	A machine operation, manually controlled, that permits the unit to read one blockette of information backward, then stop.
Read (One-Blockette) Forward	A machine operation, manually controlled, that permits the unit to read one blockette of information forward, then stop.
Read, No Print (RNP)	A machine operation, manually-controlled, which permits the unit to read information without printing.
RS	Read Start.
Servo	A term used to refer to the Uniservo.
Set	Used to denote an electronic function whereby a bistable device (usually a flip-flop) is placed in a particular state. The opposite condition may be termed "restore."
SCD	Start Center Drive.
SP, SP Pulse	Sprocket pulse, the eighth channel on the magnetic tape.
SP ₁	The sprocket pulse, delayed five microseconds.
SP ₂	The sprocket pulse delayed 7.5 microseconds.

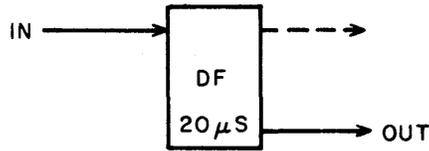
Switch (SC)	All switches marked SC are located on the Supervisory Control Panel.
Switch (TC)	All switches marked TC are located on the Test Control Panel or Power Supply unit.
Tape	A term used in referring to the magnetic tape used to store Univac information.
Tape Load	A machine operation used to bring the magnetic tape under the Read Head of the machine.
TE	Trailing Edge.
Tractor	The mechanical unit used to move the paper past the Print Head.
Uniservo	An auxiliary unit of the Univac system which accomplishes actual reading and writing on magnetic tape.
Univac	A term used to refer to the Central Computer. Also a term used to refer to the Central Computer system and auxiliaries.
Word	An ordered set of characters equal to twelve digits. Sixty words comprise one block.
Zero Suppression	An automatic machine function used to prevent the read-in of zeros for certain controlled fields or locations within a blockette.
ZCD	Zero Cross Detector. A unit for the detection of impulses received from the Odd-Even wheel photocell. The output from ZCD (1 or 2) performs a subsequent function.

iii. CIRCUIT SYMBOLS

Circuit symbols used in this Manual conform as closely as possible to those that have been used by Field Maintenance personnel since the inception of the High-Speed Printer. Although many of these symbols are not the same as those used in the present Univac system, it has been deemed wise not to use the newer symbols, inasmuch as Field personnel are presently more conversant with the original symbols.

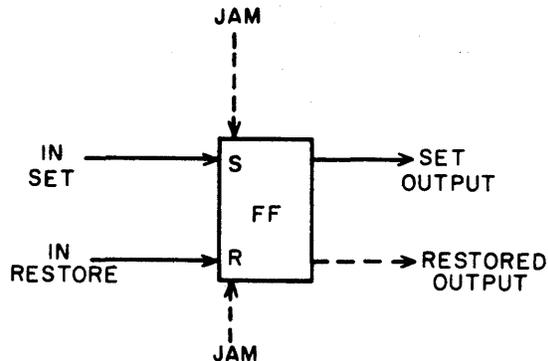
For those readers who may be unfamiliar with this type of symbol representation, the following will indicate the use of special circuit symbols in this text.

1. DELAY FLIP-FLOP



The above representation of a Delay Flip-flop appears throughout this manual. The dotted output is infrequently utilized. Essentially, once triggered, the output from this flip-flop will be from the dotted arrow point for the period of delay, which is determined by the circuit constants. This delay is always indicated within the block. Upon termination of the delay, the output will switch to the "out" side shown, and will remain in this state until again triggered. Technically known as a one-shot multivibrator.

2. FLIP-FLOP



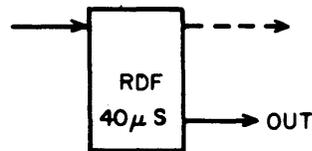
The flip-flop indicated above is a bistable device and will remain in one of two states until an input signal, a pulse, triggers it to the opposite state. If an output is taken from one side, designated the "set" side, this output will be present for the duration of the input. When "restored", the output from the set side ceases, with the "restored" output prevailing. The latter output is less frequently used in the High-Speed Printer, and is therefore

shown dotted in this example. An instance where it is used, however, is in flip-flop FF3, the Center Drive Control.

A constant signal level will force this circuit to remain in one state, and is referred to in this text as a "jam" or "jamming" signal. This state may be either on the "set" or "restored" side.

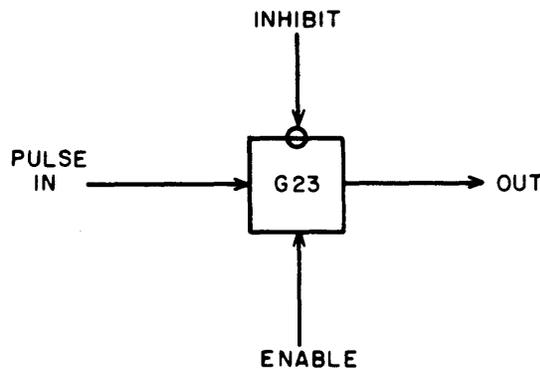
Technically known as a trigger-type multivibrator.

3. RETRIGGERABLE DELAY FLIP-FLOP



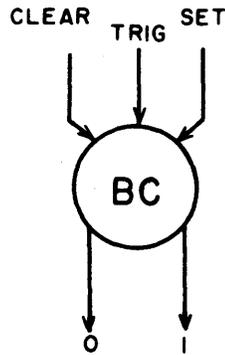
An output will appear from the Retriggerable Delay Flip-flop as long as input pulses are received prior to the completion of the delay period, determined by the circuit constants. Following the final input pulse, the flip-flop will return to its normal state when the delay period has expired.

4. GATE



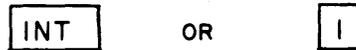
The function of a gate in the High-Speed Printer is to permit pulses to pass a point in a circuit if certain conditions exist, this usually being several inputs from various sources received simultaneously. A d-c voltage, referred to as an enable (or permissive signal), enables the gate. If a pulse from another source samples the gate this pulse will pass through. However, if the gate is inhibited, as represented by the circled input above, the gate is unable to pass the pulse. The inhibit is usually a voltage level, which prevents the gate from operating. More than one enable may be required by a gate in order that a pulse may sample the gate and immediately pass.

5. BINARY COUNTER



The binary counter above is a flip-flop as used in other Univac units, but is represented as shown. A signal (usually a pulse) on the "set" side will set the flip-flop or counter to the "1" state; a signal on the clear side will clear the counter to "0". A signal on the "trigger" input will cause the flip-flop to change to the state opposite to that which it maintains at the moment.

6. INTEGRATOR



An integrating circuit is shown in this manual by the above symbol.

7. DIFFERENTIATOR



In a similar manner, a differentiating circuit will appear as shown. Both integrating and differentiating circuits as used in the High-Speed Printer do not differ from commonly accepted theory. (See "Glossary and Abbreviations").

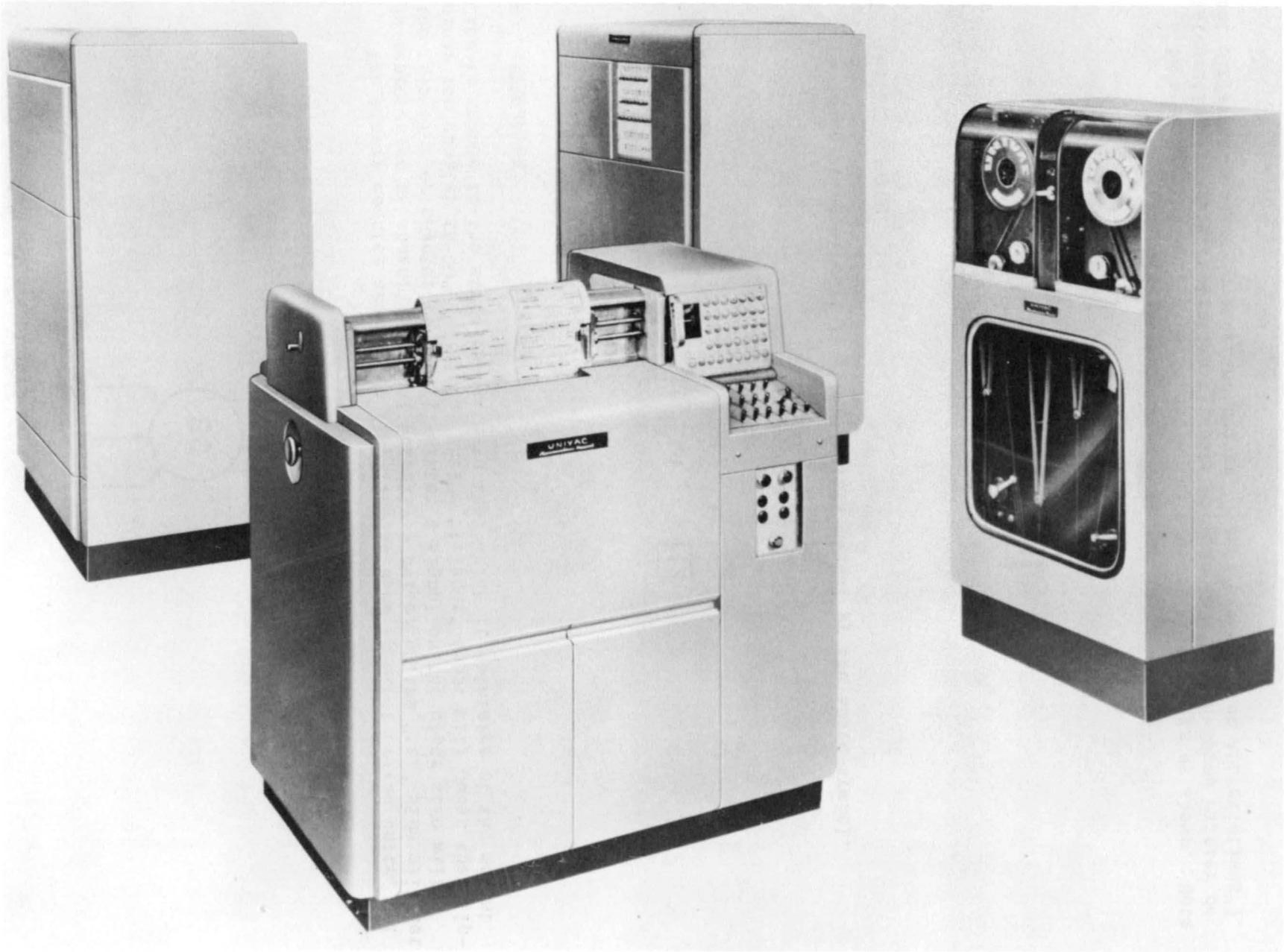


Figure 1-1. Univac High-Speed Printer
PX 616

HIGH-SPEED PRINTER
OF THE
UNIVAC SYSTEM

SECTION 1
GENERAL DESCRIPTION

1. GENERAL

The High-Speed Printer (Figure 1-1) of the Univac System converts information stored on a metal or plastic tape into a visible printed record. The Printer is completely self-checking, and requires a minimum of operator intervention.

Special editing features of the Printer greatly reduce the need for computer time in editing the tape. The use of plugboards permits virtually complete freedom of output format. Non-significant zeros may be eliminated automatically in preselected locations. Information may be repeated within a line, or on as many as six successive lines; thus information contained in one blockette on the input tape may be subdivided and printed out in any desired format on up to six lines of print. The Printer uses any sprocket-fed paper, either blank or pre-printed, four to twenty-seven inches wide, to a maximum weight of card stock.

2. SPECIFICATIONS

Area required:	400 sq ft
Power:	18 kva, 60-cycle a-c, 195 to 208v single- phase
Cooling:	
Chilled water	45F
Rate of flow	8 gpm
Pump head	80 ft
Code Used:	Univac binary excess-three (XS3) code with parity check

PRINTER UNIT

Size:	31-7/8" long x 47 1/2" wide x 48" high
Floor Area:	10.8 sq ft
Weight:	800 lbs

Number of pairs of typewheels:	65
Number of Characters Available:	Alphabetical - 26
	Numerical - 10
	Miscellaneous - <u>15</u>
	51 Total

Printing Speed:

Maximum Characters per minute	78,000
Lines (Blockettes) per minute	200, 400 or 600 (Standard)

Machine Cycle:

Time to print one line	100 milliseconds
Read Cycle	20 milliseconds
Print Cycle	80 milliseconds

Horizontal Character Spacing:

Characters per inch	10
Characters per line	130

Vertical Line Spacing:

Lines per inch	Single-space	6
Lines per inch	Double-space	3
Lines per inch	Triple-space	2

Paper Type: Any sprocket-fed paper, blank or pre-printed.

Paper Speed: 22 ips

Paper Width:

Minimum	4 in
Maximum	27 in

Ribbon: Paper or inked fabric

Ribbon Speed:

Carbon	10 ips
Nylon	6 ips

Paper Loop (Fast-Feed Control):

Channels	7
Length	11 to 22 in
Vertical hole spacing	6 per in

Ribbon Width: 13-5/8 in

Special Features:

- a. Fast-Feed: Advance paper 100 lines per second without printing
- b. Multiline: Print Data from a blockette on more than one line
- c. Plugboard Edit Control

Checking circuits:

- Odd-even error
- 120 error
- Print error
- Address-line error
- Fast-feed error

HIGH-SPEED TAPE TRANSPORT

Size: 21-3/4" long x 29-1/4" wide x 60" high

Floor Area: 5 sq ft

Weight: 650 lbs

Power Dissipated: 1.5 kw

Cooling: Two air blowers

Reel Size: 1500 ft

Pulse Density: 50 pulses per in (from Unityper)
128 pulses per in (from Central Computer Uniservo)

Number of blocks per reel: 1250

MEMORY UNIT

Size: 50-3/4" long x 32-3/4" wide x 68-3/16" high

Floor Area: 11.1 sq ft

Weight: 2000 lbs

Cooling: Air blown over water-cooling condensers and throughout unit.

POWER AND CONTROL UNIT

Size: 50-3/4" long x 32-3/4" wide x 68-3/16" high

Floor Area: 11.1 sq ft

Weight: 1200 lbs
Cooling: Air blown over water-cooling
condensers and throughout unit

3. PHYSICAL DESCRIPTION

The High-Speed Printer consists of four major parts: Uniservo, Memory, Control and Printer units. The complete equipment is shown in Figure 1-1.

a. UNISERVO. - The Uniservo (or Tape reader) reads the information stored on magnetic tape by the Central Computer. This information is channeled through the control unit to the Memory unit, where it is stored until after it is printed-out by the Printer unit. The Uniservo reads the tape one blockette at a time. During reading time, tape moves over the Read Head at 100 inches per second. The tape is brought from rest to the reading speed of 100 inches per second within five milliseconds. Signals from the Control unit govern the starting and stopping of the tape before and after each blockette.

b. CONTROL. - The Control unit contains the main power supply, together with most of the control and checking circuitry. The Test Control panel located on the Control unit contains switches and indicators used in testing and maintaining the Printer, and in directing the sequence and mode of operation of the Printer.

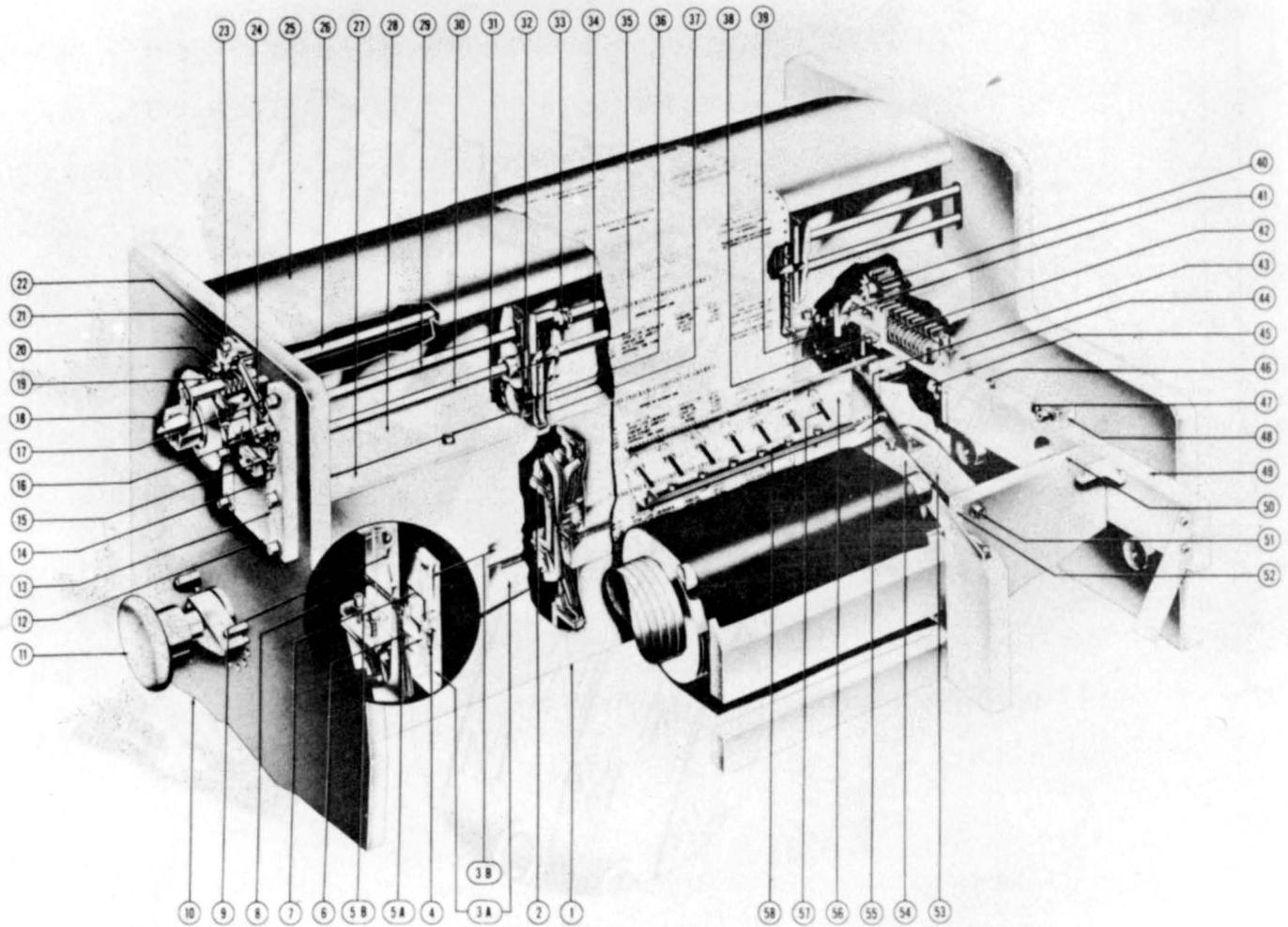
c. MEMORY. - Information read from the tape by the Uniservo is stored in the Memory unit until completion of the printing operation. Included in the Memory unit are the memory addressing circuits, output circuits, special function circuits, plugboard, and plugboard relays.

d. PRINTER. - The Printer unit contains all the mechanical assemblies used in the printing operation. These assemblies include the Print Head and type-wheels which do the actual printing, and the paper and ribbon feed assemblies. The Supervisory Control panel on the Printer unit contains the switches and indicators used in normal Printer operation.

Basic operation of the Printer unit involves the synchronized operation of the following mechanical assemblies:

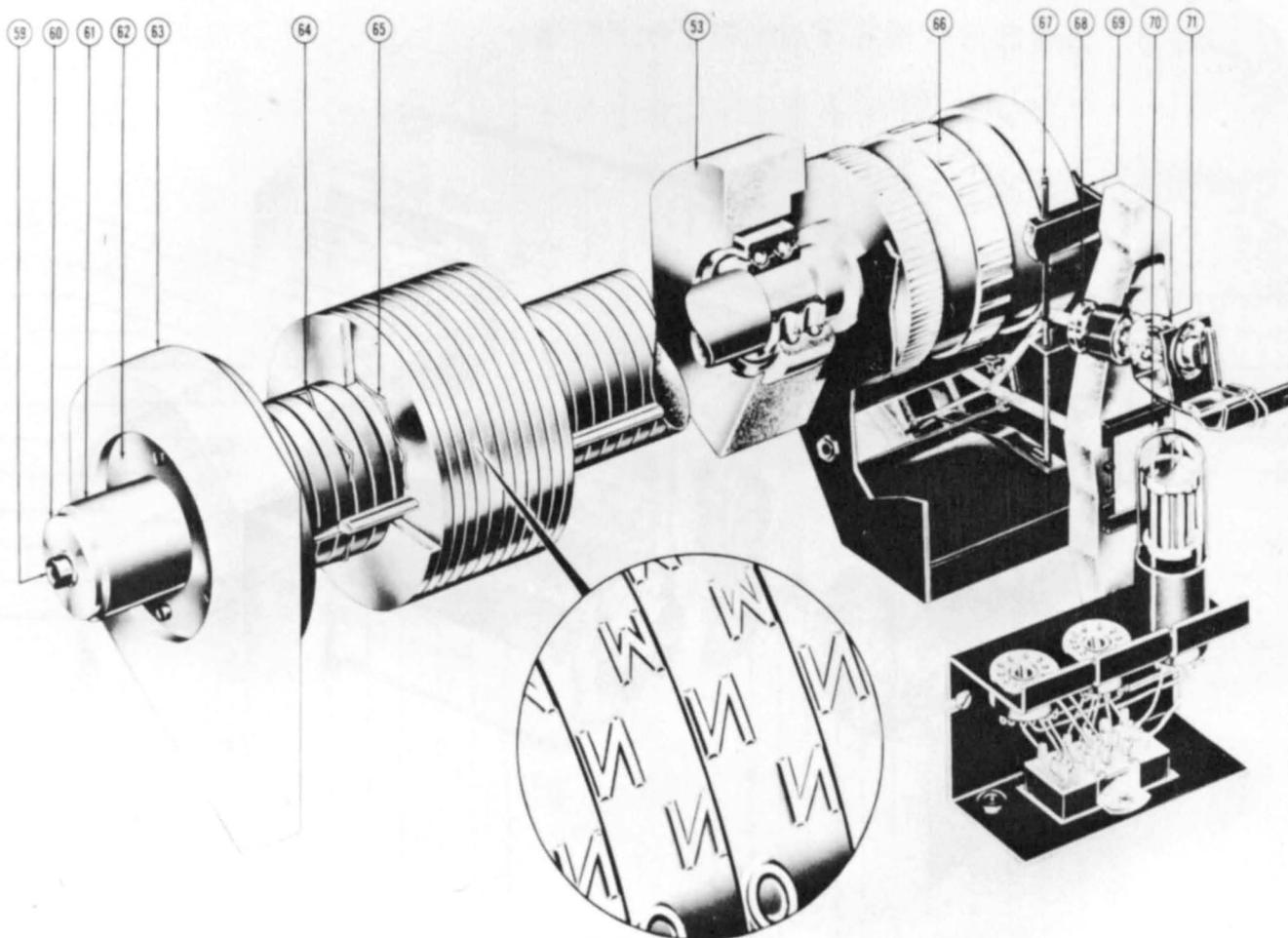
The PRINT HEAD (Figure 1-2) contains 130 hammer-actuator assemblies, one for each print location. The actuator forcefully moves the hammer toward the associated typewheel at a precise instant selected by the electronic circuitry.

The TYPEWHEEL SHAFT ASSEMBLY (Figure 1-3) contains 65 double-columned typewheels and a Code Wheel with three independent polished optical facets. Each typewheel has two separate 51-character columns of type around the circumference. Opposite each column is one hammer-actuator assembly on the Print Head. The 65 typewheels print a 130-character line of print, with each typewheel printing in two adjacent print locations. The Code Wheel (Figure 1-3) establishes synchronization between the rotating typewheels and the character-selection circuits. The typewheel shaft is housed in a motor-driven carriage assembly (Figure 1-2) which moves in or out of printing position according to the setting of the CARRIAGE IN-CARRIAGE OUT switch on the Supervisory Control panel.



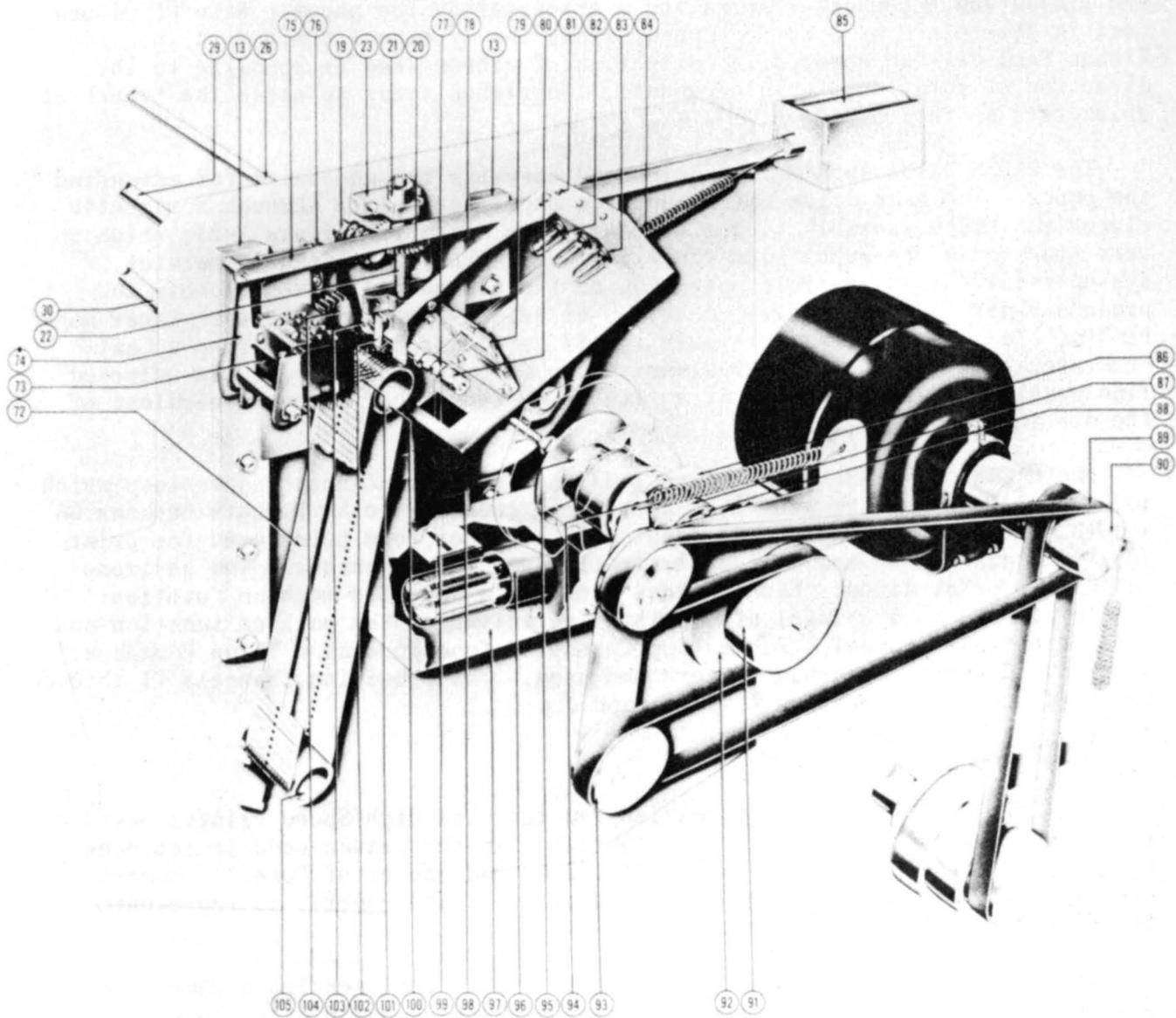
- | | |
|--|-----------------------------------|
| 1 - Printer Head Cover Plate | 19 - Slide Control Worm |
| 2 - Actuator Mounting Channel | 20 - Slide Worm Gear |
| 3A - Hammer Mount - Lower | 21 - Slide Screw Thrust Collar |
| 3B - Hammer Mount - Upper | 22 - Slide Control Screw |
| 4 - Hammers | 23 - Thrust Block |
| 5A - Hammer Guides - Lower | 24 - Interceptor Lever |
| 5B - Hammer Guides - Upper | 25 - Paper Lead-off Hood |
| 6 - Hammer Return Spring | 26 - Cross Shaft |
| 7 - Actuator Mounting Screws | 27 - Horizontal Dust Shield |
| 8 - Actuator Stop Screws | 28 - Vertical Dust Shield |
| 9 - Actuator Stop Backing Spring | 29 - Tractor Shaft |
| 10 - Left L-frame End Plate | 30 - Tractor Guide Rod |
| 11 - Eccentric Shaft Knob | 31 - Tractor Chains |
| 12 - Form Register Slide, Left | 32 - Tractor Guide Collar |
| 13 - Register Slide Ways | 33 - Tractor Drive Collet |
| 14 - Form Register Slide Stop, Lower Actuating Screw | 34 - Collet Location Clamp Screws |
| 15 - Actuating Screw Bracket | 35 - Tractor Guide Set Screw |
| 16 - Lever Actuating Pins | 36 - Tractor Idler Sprocket |
| 17 - Form Register Slide Stop, Upper Actuating Screw | 37 - Paper Retaining Gates |
| 18 - Form Register Slide Operating Crank | 38 - Limit-switch Mounting Plates |
| | 39 - Traverse Limit-switches |
| | 40 - Traverse Pinion |

Figure 1-2. Print Head Assembly
PX 616



- | | |
|--|---|
| 41 - Carriage Limit-switch Trippers | 63 - Left Pillow Block |
| 42 - Traverse Rack Springs | 64 - Typewheel Retaining Springs |
| 43 - Eccentric Shaft Eccentrics | 65 - Typewheel Spacing Springs |
| 44 - Traverse Racks | 66 - Code Wheel |
| 45 - T-frame Adjusting Screws | 67 - Timing Find Adjustment Screw |
| 46 - Rack Supports | 68 - Lens |
| 47 - Carriage "Out" Stop Screw | 69 - Code Wheel Housing |
| 48 - Carriage "Out" Stop Block | 70 - Photocell Shutter Slides |
| 49 - Traverse Bars | 71 - Lamp |
| 50 - T-frame Mounting Plate | 72 - Sliding Drum Guide Rail |
| 51 - Pillow Block Attachment Screws | 73 - Brush Holder Block |
| 52 - Edges of Cut-out in 65 | 74 - Brush Actuating Lever |
| 53 - Right Pillow Block | 75 - Brush Actuating Link |
| 54 - Upper Ribbon Guide | 76 - Brush Holder Stop Screw |
| 55 - Eccentric Shaft | 77 - Clutch Commutator Mirrors |
| 56 - Plexiglass Visor | 78 - Form Register Slide, right |
| 57 - Back-stop Brushes | 79 - Clutch Optical System Cylindrical Lens |
| 58 - Brush Clamp Screws | 80 - Clutch Output Shaft Extension |
| 59 - Cap Screw for Puck Driving Sleeve | 81 - Lamp Socket Set Screw |
| 60 - Washer for Puck Driving Sleeve | 82 - Clutch Optical System Lamps |
| 61 - Puck Driving Sleeve | 83 - Lamp Sockets |
| 62 - Bearing Retaining Ring | |

Figure 1-3. Typewheel Shaft Assembly
PX 616



- | | |
|---|--|
| 84 - Actuator Return Spring | 95 - Brake Operating Sleeve |
| 85 - Brush Actuating Solenoid | 96 - Clutch Optical System Photocell |
| 86 - Clutch Magnet Clamp Ring | 97 - Clutch Optical System Photocell Housing |
| 87 - Clutch Coil and Magnet Assembly | 98 - Clutch Optical System Chimney |
| 88 - Clutch Armature and Thimble Assembly | 99 - Clutch Optical System Slit |
| 89 - Clutch Drive Belt | 100 - Paper Loop Drum |
| 90 - Clutch Driving Pulley, Motorshaft | 101 - Paper Loop Brushes |
| 91 - Clutch Driven Pulley | 102 - Tractor Driving Pinion |
| 92 - Clutch End Plate | 103 - Clutch Shaft Outboard Bearing |
| 93 - Clutch Belt Tensioning Idler | 104 - Tractor Shaft Driven Gear |
| 94 - Clutch Clamp Ring Screw | 105 - Paper Loop Sliding Drum |

(See Figures 1-2 and 1-3 for other call-out numbers.)

Figure 1-4. Paper Feed and Optical System
PX 616

The RIBBON FEED ASSEMBLY (Figure 1-2) controls feed of the ribbon past the Print Head. The ribbon is located between the typewheels and the paper; when a hammer from the Print Head strikes the paper, it forces the paper against the ribbon and typewheel, imprinting a character on the paper. Rate of ribbon feed is determined by printing speed, since the typewheel shaft furnishes the ribbon feed driving power. The direction of ribbon feed is opposite to the direction of rotation of the typewheel; the ribbon tends to clean the typewheel characters as they pass.

The PAPER DRIVE ASSEMBLY (Figure 1-4) contains the mechanism for advancing the paper. The main drive motor supplies paper-feed power through a magnetic clutch and brake assembly to the tractor drive assembly (Figure 1-2), which in turn transports the paper past the Print Head. The paper feed commutator system (Figure 1-4) controls operation of the clutch and brake assembly to produce paper feed in single-, double-, or triple-space increments. Paper may be "fast-fed" over areas where printing is not desired. Even during a Fast-Feed operation, however, paper always moves an exact multiple of the selected line spacing. Paper advances at a rate of 22 inches per second regardless of the distance moved.

The PAPER LOOP ASSEMBLY (Figure 1-4) contains a continuous paper loop which advances in synchronism with the paper. The loop may be any length between 66 and 132 lines, depending on the length of the paper form being used for printing. The paper loop is divided vertically into twelve channels and horizontally into print lines. Each channel controls a specific machine function; a hole punched in a channel at a print line initiates the machine function controlled by that channel. Paper loop Channel 7 functions as a "Stop Homepaper" command. Channels 8 through 12 are not used. The remaining Channels (1 through 6) are described in Section 2, paragraph 4.d.

4. BASIC OPERATION

a. UNIVAC CODE. - The information fed into the High-Speed Printer must be expressed in the Univac code. Each character in the Univac code is represented by seven binary digits and always contains an odd number of "ones". Numerics are expressed in excess-three binary code; i.e., each numeric is represented by its binary value plus three.

In Univac code, the seven binary digits (bits) representing a character are divided into three groups: the body, zone, and check pulse. The body is formed by levels 1, 2, 3 and 4 of the input tape; the zone by levels 5 and 6; and the check pulse by level 7. Characters are written as shown in the following example for the character "A".

	7	65	4321	Tape Level
Univac Code Notation	0	01	0100	
	Check Zone	Body	Code Group	
	Pulse			

The body and zone determine the character represented. The check pulse insures that the total number of ones in a character is always odd -- the check pulse contains a one only when the total number of ones in the body and zone is even.

Since the body has 16 possible combinations and the zone has four, the two together may form a maximum of 64 possible combinations. Of these 64 combinations, all but one are used; because of a Central Computer requirement, the Printer does not use the combination 1 11 1111. In the 63 combinations used by the Printer, 51 represent printable symbols found on the typewheel, and the remaining 12 represent non-printable special symbols. The combinations are grouped as follows:

<u>Printable Symbols</u>	<u>Non-Printable Symbols</u>
10 Numeric	4 Fast Feeds (FF I, FF II, FF III, FF IV)
26 Alphabetic	1 Multiline (ML)
15 Punctuation	1 Stop
	1 Breakpoint (BP)
	5 Ignores

All of the printable symbols are found on the typewheel; as each symbol passes the Print Head, its code combination is produced by the Code Generator and applied to the Comparator.

None of the special symbols appear on the typewheels, nor are the code combinations of the special symbols produced by the Code Generator. When a special symbol enters the Printer from the tape, it is recognized and identified as such by a function table which prevents the symbol from entering the Memory, and initiates operation of the special function circuitry for the particular symbol. In normal operation, therefore, special symbols are not printed-out; those for Fast-Feed, Multiline, Stop, and Breakpoint initiate special Printer functions, while ignore symbols produce spaces in the printed copy wherever they occur. When, for test purposes, it is desired to locate and identify the special symbols on the tape, they may be printed-out using the Computer Digit mode of operation. In Computer Digit operation, all special symbols are first altered to printable combinations, then fed into Memory and printed-out along with the printable symbols.

Table 1 shows the complete Univac code as used with the High-Speed Printer. The special non-printable symbols are enclosed by parentheses in the "character" column. The print-out characters for the special symbols are listed in the "Computer Digit" column. Note that for each numeric the zone is "00", and the body is a binary number three greater than the value of the numeric.

b. OPERATION. - The typewheel drum (containing 65 typewheels) rotates continuously. Opposite each of the 130 type columns on the typewheel drum is a print hammer. Between the typewheel drum and the print hammers are the ribbon and the paper, in that order. When a print hammer is thrown forward by its actuator, it presses the paper and ribbon against the typewheel, imprinting a character from the typewheel onto the paper. During one revolution of the typewheel drum, one complete column of type passes by each print hammer; one line of print (130 characters) can thus be printed in just one typewheel revolution. After each line has been printed, the paper feed mechanism advances the paper

the desired number of spaces, and another line is printed. The ribbon advances at a rate proportional to the speed of the typewheel.

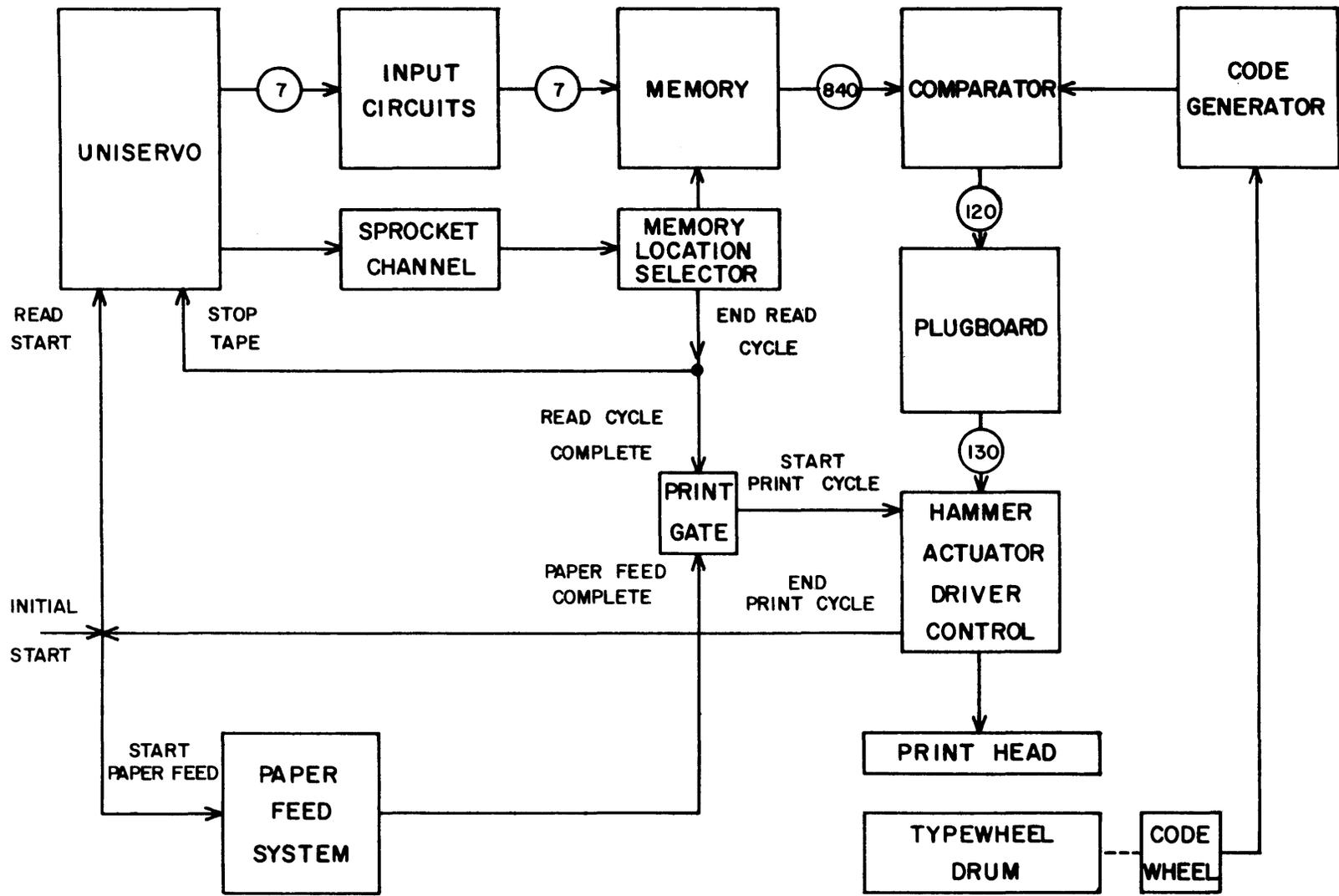
Proper operation of the High-Speed Printer requires that the mechanical assemblies function in synchronism with the electronic circuitry, so that the information on the tape is correctly transformed into a printed output of the desired format. The simplified block diagram (Figure 1-5) illustrates the basic components of the High-Speed Printer. In a normal printing operation, one blockette is read from the tape, stored in the Memory, transposed and translated into the desired format, and printed. Each printing operation involves the completion of two cycles: a Read Cycle and a Print Cycle.

The beginning of a Read Cycle initiates the paper feed, and starts the Uniservo. The paper drive advances paper until the desired printing location is reached. The Uniservo reads a blockette into the input circuitry serially, one character at a time. The input circuitry transfers the blockette into Memory. When the entire blockette (120 characters) has been read and stored into Memory, the Uniservo stops, and the Read Cycle ends. The blockette remains stored in Memory until after completion of the Print Cycle.

The end of the Read Cycle initiates a Print Cycle. The characters stored in Memory appear continuously as inputs to the Comparator. Also applied to the Comparator input is the Code Generator output, consisting of a coded combination identifying the typewheel character currently approaching the print hammers. The Comparator contains 120 identical comparator stages; each stage compares the Code Generator output with the seven-bit character stored in one specific Memory location. Each Comparator stage has a separate output line which can be connected through the plugboard to one or more hammer actuator drivers. The plugboard thus determines the output format, since it connects each Memory location through its associated Comparator stage to one or more print locations.

A Comparator stage generates an output signal when the associated character in Memory is identical to the Code Generator output. This Comparator output signal alerts the hammer actuator drivers in the print locations selected for that Comparator stage by the plugboard. At the instant when a typewheel character is opposite the print hammers, a print signal samples all hammer actuator drivers, firing those which have been alerted by the Comparator. The fired drivers force the associated hammers against the typewheel, printing the character in all of the affected print locations. As each new typewheel character approaches the print position, the Code Generator sets up the appropriate code combination, and the Comparator alerts a new set of hammer actuator drivers. As each of the typewheel characters approaches and passes the print hammers, the sequence of alerting the appropriate hammer actuator drivers from the Comparator and firing the alerted drivers with a print signal is repeated. During one typewheel revolution, all 51 characters pass the print hammers, and each Memory location containing a printable character generates one Comparator output signal when the character stored coincides with the Code Generator output. When one typewheel revolution has elapsed since the beginning of the Print Cycle, one line has been printed, and the cycle ends. At this time a Read Start signal initiates a Read Cycle, and a new printing operation begins.

Figure 1-5. Simplified Block Diagram, HSP
PX 616



c. SPECIAL FUNCTIONS. - Several of the special machine functions which add to the versatility and operating efficiency of the High-Speed Printer are discussed briefly in this paragraph. More detailed explanations of the operations are included in Section 2.

FAST-FEED - The Fast-Feed circuitry makes it possible to advance paper any desired number of spaces in one move without operator intervention. During a Fast-Feed operation, the paper drive system moves paper at the same rate (22 inches per second) as in normal line spacing. Of the five Fast-Feed circuits, four of them (Fast-Feed I through Fast-Feed IV) require the appropriate Fast-Feed symbol to be located as the first character in a blockette in order to start the Fast-Feed, and a hole in the proper paper loop channel to stop the Fast-Feed. Fast-Feed V starts and stops from holes in the paper loop. The six paper loop channels and the function of each are listed below.

<u>PAPER LOOP CHANNEL</u>	<u>FUNCTION</u>
1	STOP FAST-FEED I
2	STOP FAST-FEED II
3	STOP FAST-FEED III
4	STOP FAST-FEED IV
5	START FAST-FEED V
6	STOP FAST-FEED V

A Fast-Feed symbol (FF I, FF II, FF III or FF IV) at the beginning of the blockette commences paper spacing from an initial position. A hole encountered in the associated paper loop channel (Channel 1, 2, 3 or 4) stops the paper on the print line succeeding the hole location. A hole encountered at a given line in Channel 5 starts a Fast-Feed V from that line; the Fast-Feed V stops at the print line following the first Channel 6 hole encountered.

MULTILINE - A Multiline symbol in the first, second, or last character position of a blockette initiates operation of the Multiline circuitry. Under Multiline operation, one blockette is printed-out in any predetermined format on up to six successive print lines. A new Multiline symbol must be included in each blockette to be Multilined.

Plugboard and relay connections control the output format during Multiline operation. The plugboard is plugged in advance to determine the number of lines to be printed and the format of the information to be printed on each line.

STOP - A Stop symbol anywhere in a blockette stops Printer operation by preventing the beginning of a Print Cycle. When a Stop symbol enters from the tape, the read-in to Memory of the blockette containing the Stop symbol is completed, but the information contained in the blockette is not printed. The Printer must be started manually to resume operation at the point where it was stopped.

BREAKPOINT - The effect of a Breakpoint symbol in a blockette is identical to that of the Stop symbol, except that a Breakpoint symbol will have no effect unless the **BREAKPOINT** switch is selected on the Supervisory Control panel. A Breakpoint symbol in a blockette is therefore an optional stop; it is ignored unless selected by the **BREAKPOINT** switch.

ZERO SUPPRESSION - The Zero-Suppression circuits replace non-significant zeros with spaces in pre-selected fields of the printed output. The Zero Suppression plugboard determines the location and size of each field where zeros are to be suppressed. Different fields may be selected for Single Line and Multiline operation.

d. **ERROR-DETECTION CIRCUITS.** - The High-Speed Printer contains numerous error-detection circuits to insure accurate transformation of information from the magnetic tape to the printed page. When a circuit or mechanical assembly fails to operate correctly, the associated error circuit functions to stop the Printer. The indicator for the error circuit lights, making possible rapid diagnosis and repair of the faulty circuit. The error circuits are described briefly below. More detailed descriptions are included in Section 2, together with numerous examples of operation.

ODD-EVEN ERROR DETECTOR - The Odd-Even error detector checks each character read from the tape to determine that it contains an odd number of binary "ones." If not, the error circuitry generates a "Prevent Print" signal, and the O.E. CHECK neon indicator lights. The Read Cycle is completed, but the Print Cycle cannot start.

120 ERROR DETECTOR - The Memory has a capacity of 120 characters. During each Read Cycle, a complete blockette containing 120 characters should normally be read into Memory. If more, or less than 120 characters are read-in, the error detector generates a Prevent Print signal, and the 120 CHECK indicator lights. (The ADDRESS CHECK indicator also lights, but should be ignored when the 120 CHECK indicator is "on"). When the error is a less-than-120 error, the Uniservo does not stop at the end of the blockette where the error occurs, but reads-in the succeeding blockette also, this extra blockette not being entered into Memory. The setting of the Memory Address Counter is usually helpful in determining whether a greater-than-120 or less-than-120 error occurred.

ADDRESS-LINE ERROR DETECTOR - Before each character is read into Memory, a Memory Address is normally selected for the character by the Memory address circuitry. Failure of the Memory address circuits to select a Memory location for every character read-in results in the generation of a Prevent Print signal by the Address-Line error detector, and the lighting of the ADDRESS CHECK indicator. The Read Cycle is completed, but the Print Cycle does not start. The Address-Line error detector protects only against failure of the Memory address circuits to select any address at all for an input character. Should one or more incorrect addresses be selected, multiple read-in to one or more addresses would occur, resulting in the storage of one or more non-printable combinations. Such an error would not appear during the Read Cycle as an Address Line error, but would occur as a Print Check error following print-out.

PAPER FEED ERROR DETECTOR - Since the paper feeds at 22 inches per second, any failure of the paper-stop circuitry could result in the feeding of a

tremendous amount of paper before the error could be detected by the operator and paper-feed stopped manually. The paper-feed error detector prevents the feeding of more than 22 inches of paper in any one paper-feed operation. If a paper-feed does not stop within one second (22 inches), the paper-feed error detector stops the paper drive, generates a Prevent-Print signal, and lights the P.F. CHECK indicator. Paper movement cannot start again until the START switch is actuated.

FAST-FEED ERROR DETECTOR - A tape-initiated Fast-Feed has precedence before a Fast-Feed V, by eliminating a Fast-Feed V if one is already in progress, and by preventing the initiation of a new one as long as the tape-initiated Fast-Feed lasts. Failure of a tape-initiated Fast-Feed to take precedence before the Fast-Feed V results in a Fast-Feed error, which generates a Prevent Print signal and lights the FAST FEED CHECK indicator. Read-in of the current blockette is, however, completed. Normal printing operations may be resumed after a Fast-Feed error by actuating the START switch.

CHARGE ERROR DETECTOR - Each hammer actuator driver fires during the Print Cycle through an associated capacitor that has been charged during the Read Cycle from a +600 volt d-c source. The start of a Print Cycle normally causes removal of the charging voltage from the capacitors. Each driver can therefore fire just once through its capacitor during a Print Cycle. If the Start Print Cycle signal fails to remove the charging voltage, the Charge Error detector removes the charging voltage, starts paper feed, stops index pulses originating from the Code Generator, and lights the CHARGE CHECK indicator. The Printer stops in the middle of a Print Cycle, and paper is spaced.

PRINT ERROR DETECTOR - Associated with each print location are two tubes: a hammer actuator driver, and a check tube. Each check tube monitors the printing operation in the associated print location. At the end of the Print Cycle, the check tube will be out unless an abnormal printing operation has occurred. An abnormal printing operation could be the result of a non-printable combination stored in the Memory, failure to print a character, printing of an incorrect character, or printing of a character where there should be none. All of the check tubes are connected to the All-Out detector. When all check tubes are extinguished at the end of a Print Cycle, the All-Out detector generates an All-Out signal, signifying that a normal print operation has occurred. If one or more check tubes are conducting at the end of a Print Cycle, no All-Out signal develops, and a Print Error signal is generated. The Print Error signal starts paper-feed, generates a Prevent Print signal, and lights the PRINT CHECK indicator (the A.O. DET. CHECK indicator is out). Examination of the printed line, the check tubes, and other components is usually helpful in diagnosing the cause of the Print Error.

ALL-OUT DETECTOR - Failure of the All-Out detector results in the generation of a continuous All-Out signal, regardless of the state of the check tubes. The All-Out error detector checks the All-Out detector output at the beginning of each Print Cycle. If an All-Out signal is present, indicating failure of the All-Out detector, the Printer stops; all indicators will then be out with the exception of the A.O. DET. CHECK indicator, and the address counter will read 121.

5. CONTROLS AND INDICATORS

Controls and indicators are located on three panels: the Supervisory Control panel, Test Control panel, and Power Control panel. The Supervisory Control panel on the Printer unit controls normal Printer operation. The Test Control panel on the power supply unit is used in diagnosing and locating faults. The Power Control panel on the power supply unit is used to adjust and check the power supply. The following paragraphs explain the functions of the controls and indicators located on the three control panels.

a. SUPERVISORY CONTROL PANEL. - The Supervisory Control panel contains one bank of switches and one bank of indicators, in addition to controls for the application of power. Figure 1-6, Supervisory Control Panel Controls, identifies the controls that are located on the Supervisory Control panel. Table 2 lists the controls and the functions of each.

The Supervisory Control Indicators, Figure 1-7, are located immediately above the Supervisory Control switches. These are used as aids in observing Printer operation and in diagnosing faults. The indicators and the functions of each are as follows:

1. FIRST ROW - 1ST DIGIT INDICATORS. - The seven indicators display the contents of the first Memory location. The check pulse indicator is at the left, followed by two indicators for the zone, and four indicators for the body of the Univac character. An illuminated indicator, representing a "1" in the Univac code, indicates that the corresponding Memory tube is not conducting. When d-c power is first applied, all 1ST DIGIT indicators should light. One important use for the 1ST DIGIT indicator lies in the determination of the proper procedure to follow when an odd-even error occurs. It is necessary to know in this case, before operation can be resumed, whether a Fast-Feed symbol was in the first digit position or not, and if so, whether it was observed.

2. SECOND ROW - MAIN COUNTER INDICATORS. - The seven indicators display the condition of the Main Counter. The most significant digit (2^6) is represented by the left indicator, the least significant digit (2^0) by the right. After d-c power is first applied, all MAIN COUNTER indicators should be extinguished. After a 120-error occurs, these indicators may be used to determine whether a greater-than-120, or less-than-120 error has occurred.

3. THIRD ROW. - All indicators in the third row must be out before printing can start. The indicators are represented as follows:

HOME PAPER - Lights when the HOME PAPER switch is on.

TAPE LOAD - Lights when the TAPE LOAD switch is on.

REWIND - Lights when the REWIND switch is on.

NO D.C. - Lights when no d-c power is present. The indicator does not light unless a-c power is present.

CARRIAGE OUT - Lights when the carriage is not fully in the normal operating position.

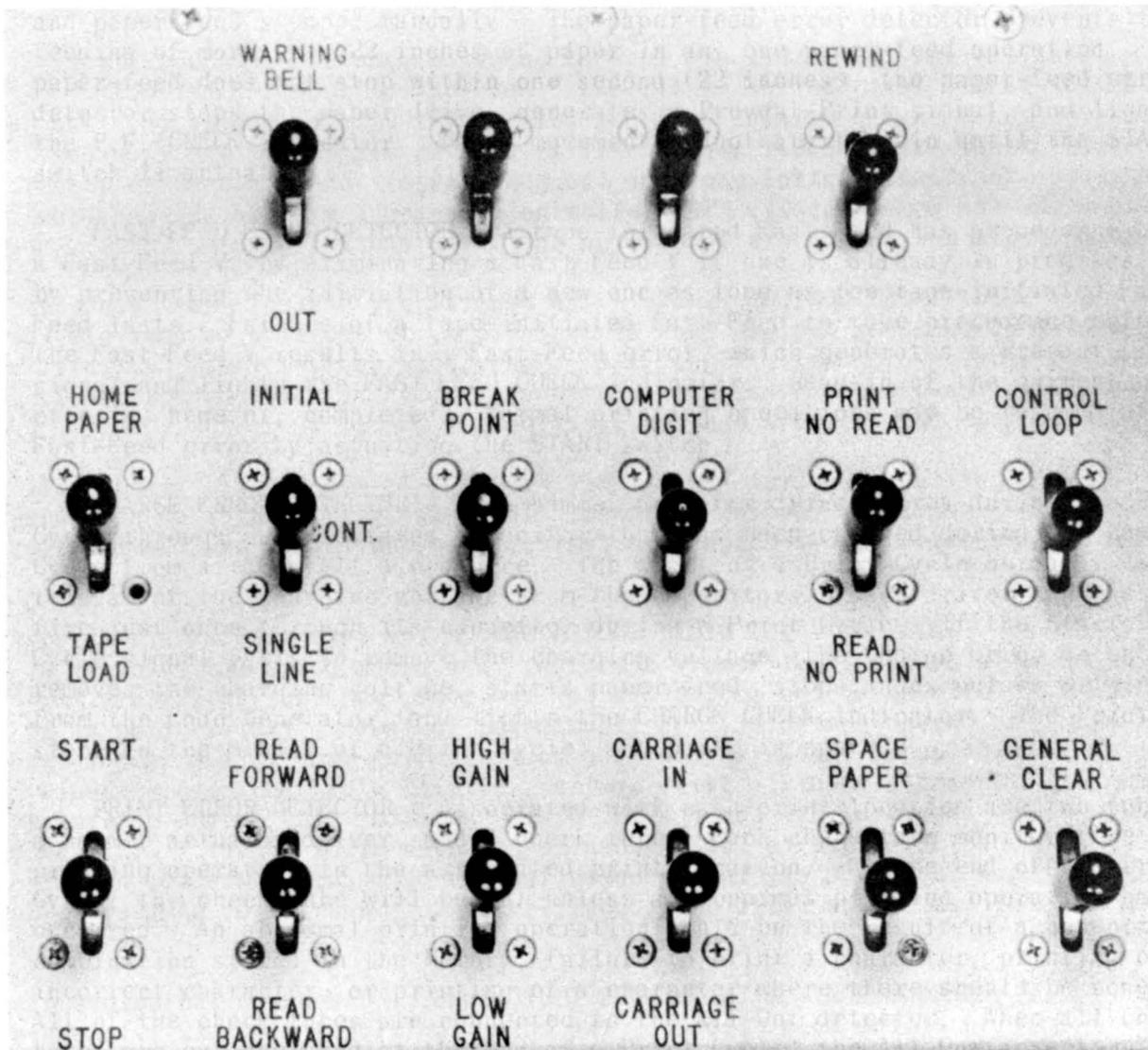


Figure 1-6. Supervisory Control Panel Controls
PX 616

4. FOURTH ROW. - The purpose of these indicators is self-explanatory.

FAST-FEED - Lights when a Fast-Feed operation is in progress.

MULTILINE - Lights when a Multiline symbol is received; indicates that the Printer is performing, or is about to perform, a Multiline operation.

NORMAL STOP - Lights when any condition other than an error stops the Printer. These conditions include:

(a) STOP switch on.

(b) Stop symbol encountered on tape during either Normal or Read, No Print operation.

(c) Breakpoint symbol encountered during either Normal or Read, No Print operation with the BREAKPOINT switch actuated.

(d) Fast-Feed I symbol encountered during a Read, No Print operation initiated by the READ FORWARD/READ BACKWARD switch.

(e) End of "read-one-blockette-forward" or "read-one-blockette-backward" operation.

(f) End of Single Line operation.

(g) End of Space Paper operation.

(h) End of Home Paper operation.

(i) Out of Paper condition.

(j) Out of Ribbon condition.

(k) Out of Tape condition.

OUT OF PAPER - Lights when end of paper supply is reached. NORMAL STOP indicator also lights.

OUT OF RIBBON - Lights when the end of the ribbon roll is reached. NORMAL STOP indicator also lights.

OUT OF TAPE - Lights when the end of the tape is reached. NORMAL STOP indicator also lights.

5. FIFTH ROW. - The fifth row contains the error indicators:

A.O. DET CHECK - Lights when an All-Out detector error occurs. Indicates error only when it is the only error indicator lit, and the STOP indicator is not lit.

P.F. CHECK - Lights when a paper-feed error occurs.

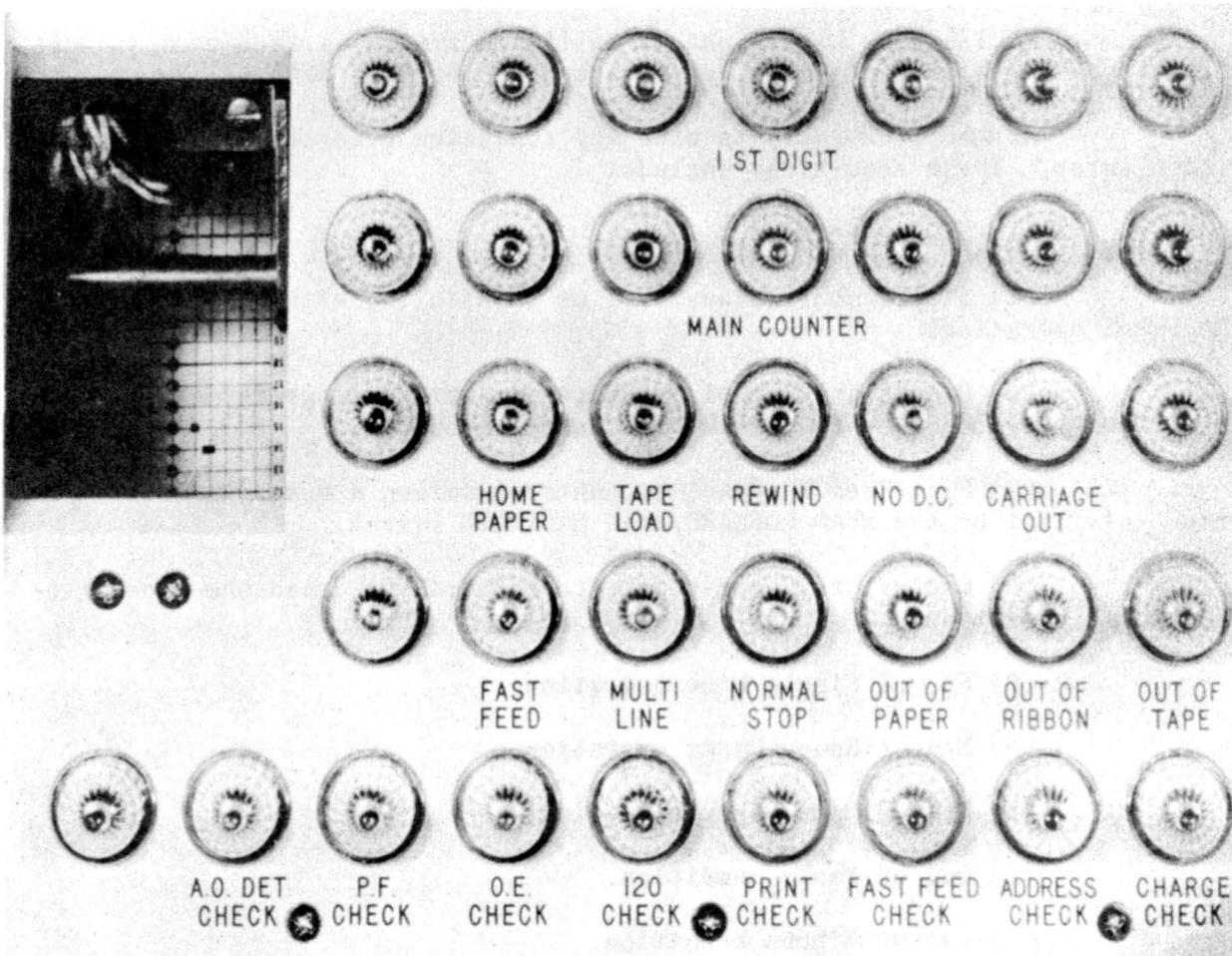


Figure 1-7. Supervisory Control Panel Indicators
PX 616

O.E. CHECK - Lights when an odd-even error occurs.

120 CHECK - Lights when either a greater-than-120 or less-than-120 error occurs.

PRINT CHECK - Lights when a print error occurs.

FAST FEED CHECK - Lights when a Fast-Feed error occurs.

ADDRESS CHECK - Lights when an Address Line error occurs.

CHARGE CHECK - Lights when a charge error occurs.

b. TEST CONTROL PANEL. - The Test Control Panel contains the switches and indicators used in maintenance of the High-Speed Printer. The Test Control panel switches and the functions of each are given in Table 3.

The Test Control Panel indicators and functions are described below:

INPUT FLIP FLOPS - The seven indicators display the states of the seven input flip-flops. These are used in conjunction with the INPUT FLIP FLOPS switches to set the Input flip-flops to the desired configuration. The check pulse indicator is at the left, followed by two zone indicators and four body indicators for the Univac character. A lit indicator represents a "1" set into the associated flip-flop.

MAIN COUNTER - The seven indicators display the condition of the Main Counter. They are used in conjunction with the MAIN COUNTER switches to set the Main Counter to a desired condition. The most significant digit (2^6) is represented by the left indicator, the least significant (2^0) by the right.

PRIMARY FUSES - Each of the four indicators (P.S., MEMORY, PRINTER, SERVO) indicates the presence of one or more defective primary fuses in the associated unit.

SECONDARY FUSES - Each of the four indicators (P.S., MEMORY, PRINTER, SERVO) indicates the presence of one or more defective secondary fuses in the associated unit.

OVERHEAT - Each of the four indicators (P.S., MEMORY, PRINTER, SERVO) lights when the temperature in the associated unit reaches an unsafe value. At the same time, primary power is removed from the entire Printer.

TEMP. WARNING - The indicator lights when the temperature in any unit approaches an unsafe value. At the same time, the warning bell rings. If the temperature continues to rise until it reaches the unsafe value, the OVERHEAT indicator lights for the affected unit, and primary power is removed from the entire Printer.

C.W. BIAS - The indicator lights when the -500 volt supply to the Code Wheel drivers fails completely or becomes more positive than -475 volts d-c.

c. POWER CONTROL PANEL. - The Power Control Panel is somewhat of a misnomer for this section of the equipment, inasmuch as the only major control function available at this panel is the Marginal Check control described in Section 2 under "Power Control Circuits." The remaining components on this panel indicate the status of various portions of the equipment as follows:

LINE COUNTER - This counter operates through the action of DF24, which actuates relays causing the counter to register the count each time a line is printed on the Printer. On late models of the High-Speed Printer this indicator is located on the Test Control Panel.

HEATERS INPUT METER - This meter indicates the a-c voltage to the primary of the heater transformers. The Marginal Check potentiometer controls this primary voltage, the output of which is indicated on the meter.

PERCENT DEVIATION METER - Voltage deviation from normal is indicated on this meter. The voltages to which this refers are those selected by the two selector switches positioned to the right of the meter.

LETTERED AND NUMBERED ROTARY SWITCHES - These are the switches referred to in the foregoing paragraph. Through the selection of these switches a possible seventy-two voltages may be checked, although certain positions remain blank in present models of the Printer. One switch is positioned at any of six positions (A through F), and the other is then switched through each one of twelve numbered positions. Any deviation from established limits (indicated on a plastic strip beside the switches) will be indicated on the PERCENT DEVIATION meter.

ELAPSED TIME METERS - Two meters, one for a-c, and one for d-c, indicate the number of hours the Printer has operated, 1) with a-c voltage applied, and 2) with the d-c voltage circuits energized to the Printer. The latter time accrues whenever the ON switch at the Supervisory Panel is actuated.

SECTION 2

LOGICAL OPERATION

1. POWER CONTROL CIRCUITS

Refer to Figure 2-1, Power Control Circuit, in following the description which is given below. A general outline of the equipment and operational function of the power controls has been given in Section 1-5 under "Power Control Panel."

The primary a-c power is applied to the primary of the AC ON switch SC22, the Agastat time delay relay, the FAULT TEST switch TC31, and the WARNING BELL switch SC32. The output of the Agastat timer relay applies the a-c power to the cooling fan motors in the Memory and Control units. The a-c power from the secondary side of the Agastat timer energizes the fan motors immediately when the AC ON switch is actuated, and continues to supply voltage to these components until a period of two minutes following the switching-off of a-c power is completed. This permits the cabinet temperature to be lowered to a safe limit prior to the circulation of air.

The FAULT TEST switch TC31 is used to indicate the type and location of a faulty fuse, should power not be available in either the AC or DC ALARM systems.

When the AC ON switch SC22 is actuated, primary power is applied to the cooling fans, filament circuits and Timer No. 1. Timer No. 1, which has a 30-second delay, retains the output chassis voltage at half-power for this period. Power is applied in this manner due to the extremely high initial filament current drain caused by the great number of tubes in the Printer.

As Timer No. 1 recovers, the output circuits are placed on full power and Timer No. 2 is actuated. Timer No. 2 permits an additional 30-second delay to occur as an additional delay for the filament circuits. This delay permits the various tubes to reach optimum operating temperature prior to the application of plate voltage.

When the delay of Timer No. 2 has expired, the power circuit is completed to the primary side of the DC ON switch, in addition to the READY light which informs operating personnel that the equipment is prepared for the application of d-c power.

Connected in series with the AC ON switch are the AC ALARM and OVERHEAT controls. A failure of any primary fuse, or an overheat condition in any of the four Printer units will open the a-c circuit.

The Marginal Check Potentiometer is used for fault determination and operational limit control. This potentiometer permits the filament voltage on the control circuits to be lowered as much as 15 per cent, thus producing a marginal operating condition in illusive or intermittent faults.

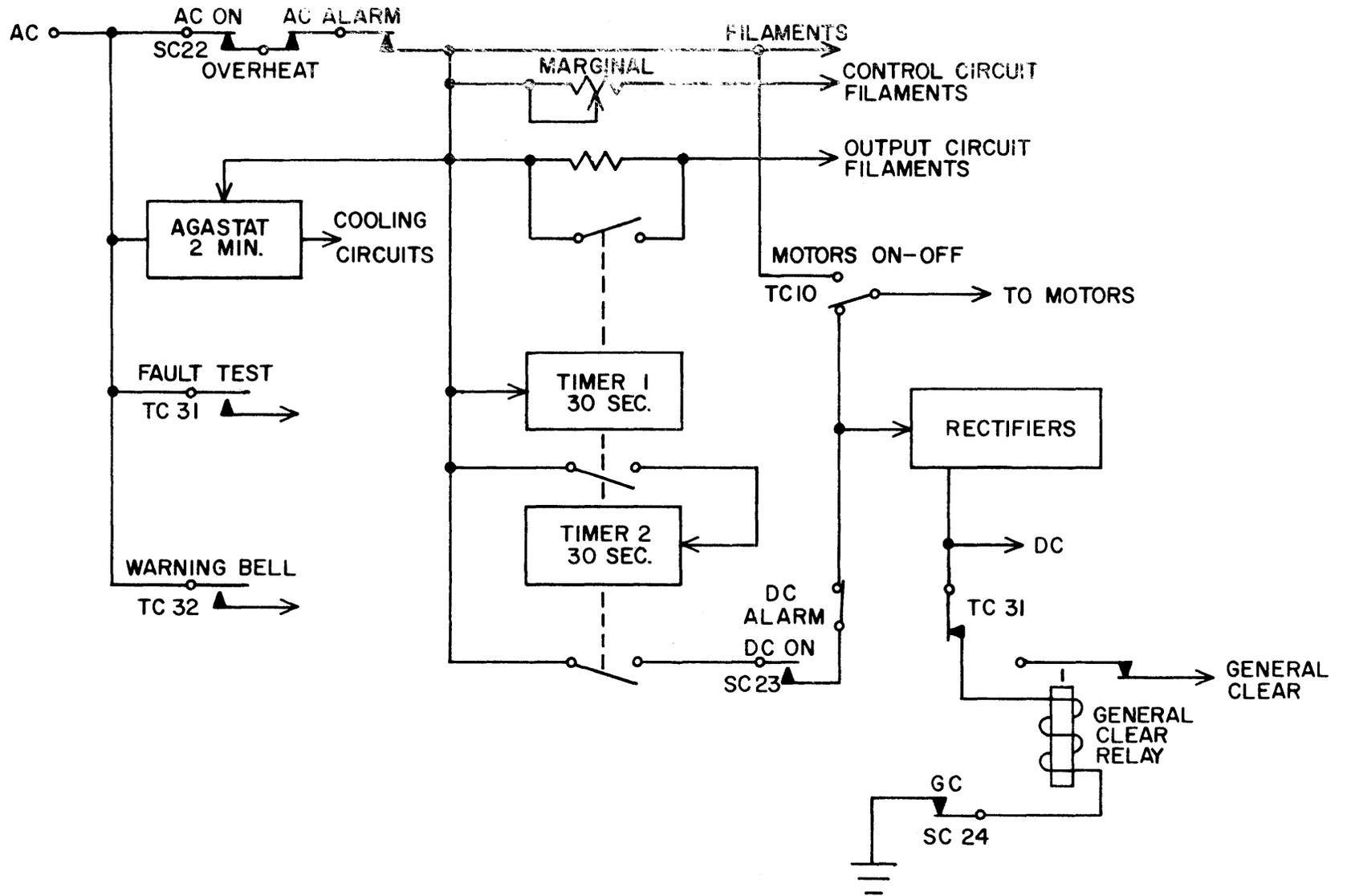


Figure 2-1. Power Control Circuit
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The MOTORS ON-OFF switch allows the motors in the Printer unit to operate without the application of secondary power.

When the DC ON switch SC23 is closed, the secondary power reaches the rectifiers and a d-c output is available. When this occurs, the General Clear relay is actuated as SC24 is a normally closed switch, as is TC31, the FAULT TEST switch. If either TC31 or SC24 is depressed (opened), the General Clear relay will open with a General Clear function occurring. This will clear all flip-flops with the exception of FF21, clear the Memory, the Memory Address counter, the Multiline ring counter, and will in addition, extinguish the Check thyratrons in the output circuits.

2. MACHINE SYSTEMS

a. TAPE CIRCUITS (See Figure 2-2).

UNISERVO - The Uniservo is explained in detail in the Uniservo instruction book. The basic Uniservo components to be considered at this time include the Center Drive clutch and brake assembly, the reading head (Read Head), and the head amplifiers. The clutch and brake assembly moves tape past the reading head at a speed of 100 inches per second, starting and stopping the tape as directed by the tape control circuitry. The reading head senses the information stored on the tape, converting it into electrical signals to be amplified by the head amplifiers.

TAPE DRIVE CONTROL - Starting and stopping of the tape is controlled by the Center Drive flip-flop (FF3). With the flip-flop in the restored state, the brake is energized and the tape is at rest; the Not-Reading line is also energized, preventing noise from entering the read-in circuits. With the flip-flop in the set state, the clutch is energized and tape moves past the reading head.

START TAPE SIGNALS - The differentiated delayed output from either Delay-Flop 1 (DF1), or DF17 sets the Center Drive flip-flop, thus starting the tape. The tape reaches full speed approximately 2.5 milliseconds later.

The same inputs which set DF1 also initiate a Clear Memory operation which lasts for 5.5 milliseconds. Since no information can be read into Memory during the Clear Memory operation, it is necessary that no information pass the Read Head until the Memory has been cleared. DF1 delays the setting of the Center Drive flip-flop for 2.5 milliseconds. This interval, plus the time required for the tape to reach full speed after starting, allows time for completion of the Clear Memory operation before information is read from the tape. The differentiated undelayed output of DF1 restores FF10, which is part of the Stop Tape and 120-error detector circuitry. The following signals set DF1 and initiate a Clear Memory operation:

1. Tape Load, occurring when the TAPE LOAD switch is actuated.
2. Initial Start, occurring when the INITIAL START switch is operated.
3. Read Start, occurring during normal operation at the end of a printing operation.

4. End of Multiline, occurring at the completion of a Multiline operation.
5. Read Forward, Read Backward, or Rewind, occurring when the READ FORWARD, READ BACKWARD, or REWIND switches are actuated.

A Bad Spot signal sets DF17. The restored output occurring 20 milliseconds later sets the Center Drive flip-flop, starting the tape. The Bad Spot signal does not initiate a Clear Memory operation.

The following signals restore the Center Drive flip-flop, which stops the tape:

1. End of Tape Load.
2. End of a normal Read Cycle.
3. Rewind Tape End (TE) signal, occurring when the REWIND switch is returned to neutral while a Rewind operation is in progress.
4. Read Backward TE signal, occurring when the READ BACKWARD switch is returned to neutral while a Read Backward operation is in progress.
5. End of rewind signal occurring when the end of tape is detected during a Rewind or Read Backward operation.
6. End of a Bad Spot occurring after the end of a Tape Load operation.
7. General Clear.

b. PAPER FEED SYSTEM (See Figure 2-3). - The paper feed mechanism is driven from the typewheel shaft drive motor through a magnetic clutch and brake assembly similar to the tape drive assembly. With the clutch energized, paper is moved at a rate of approximately 22 inches per second; with the brake energized, paper drive is stopped. Paper may be advanced only between Print Cycles, since it must be at rest while printing occurs. The paper commutator system, driven in synchronism with the paper, insures that the paper always advances an integral number of line spaces even during a Fast-Feed operation. Paper may be single, double, or triple-spaced; the desired spacing is selected by plugboard connection. The normal paper-spacing circuitry is discussed at this point without considering the Fast-Feed or Paper Feed Error circuitry in detail. Fast-Feeds and the Fast-Feed control circuits are discussed fully in this Section under 4.d.; the Paper Feed Error circuits are detailed under 5.d.

Figure 2-4 illustrates the energizing circuitry for the Clutch and Brake assembly. Consider the circuit with the Brake energized: Brake tube V3 is conducting, Clutch tube V1 and Brake fast-charge tube V4 are at the cut-off point. With V1 cut off, the voltage on the V1 plate and on the Clutch actuating capacitor C1 is approximately equal to the supply voltage.

A Start Paper Feed signal, in setting FF4, fires V1 and sets fast-charge delay-flop DF25. Clutch actuator capacitor C1 discharges rapidly, supplying a high initial clutch-setting current through V1 and the clutch solenoid. Paper advances, and continues to advance, as long as FF4 remains set. The drop in V1

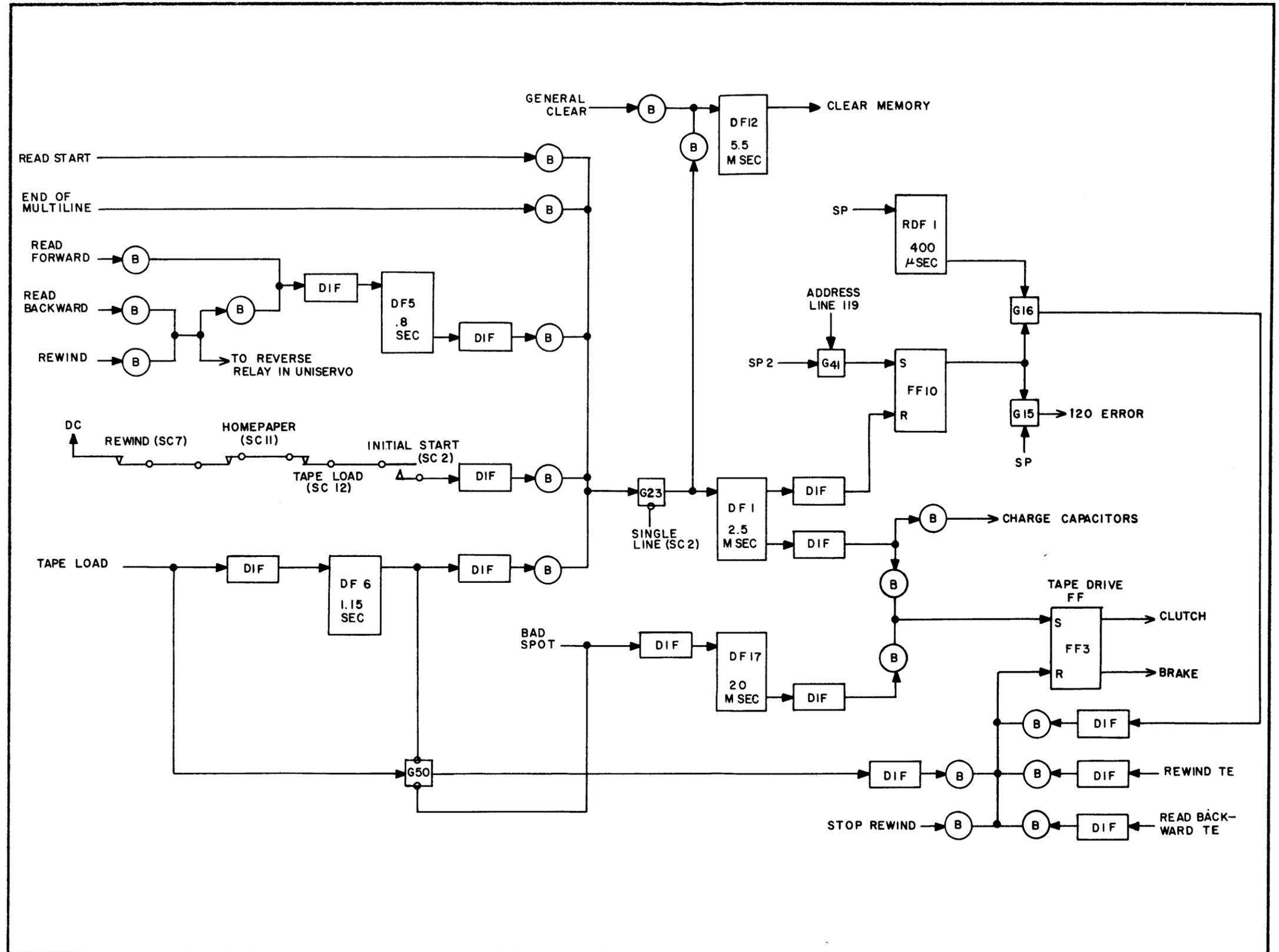
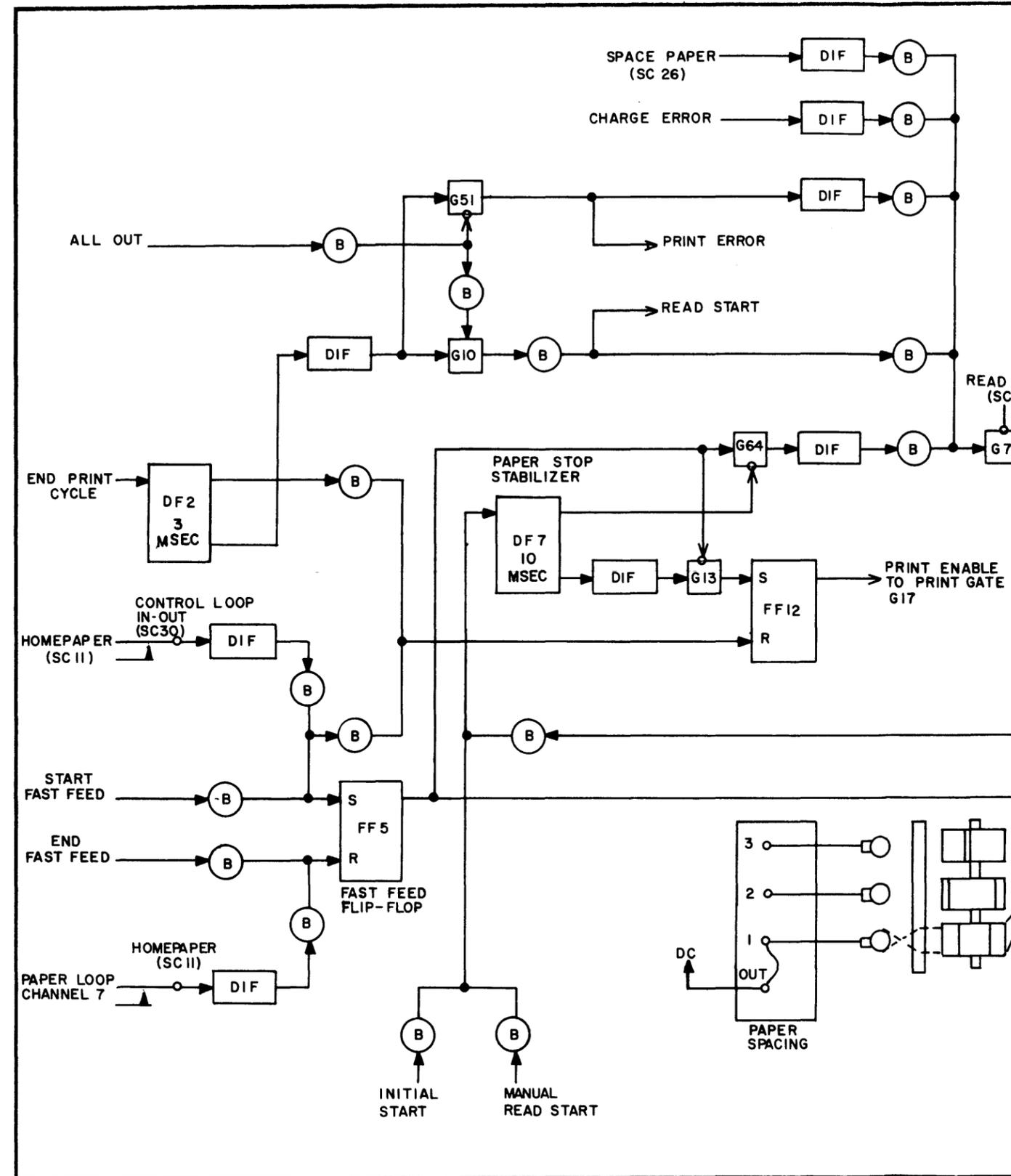
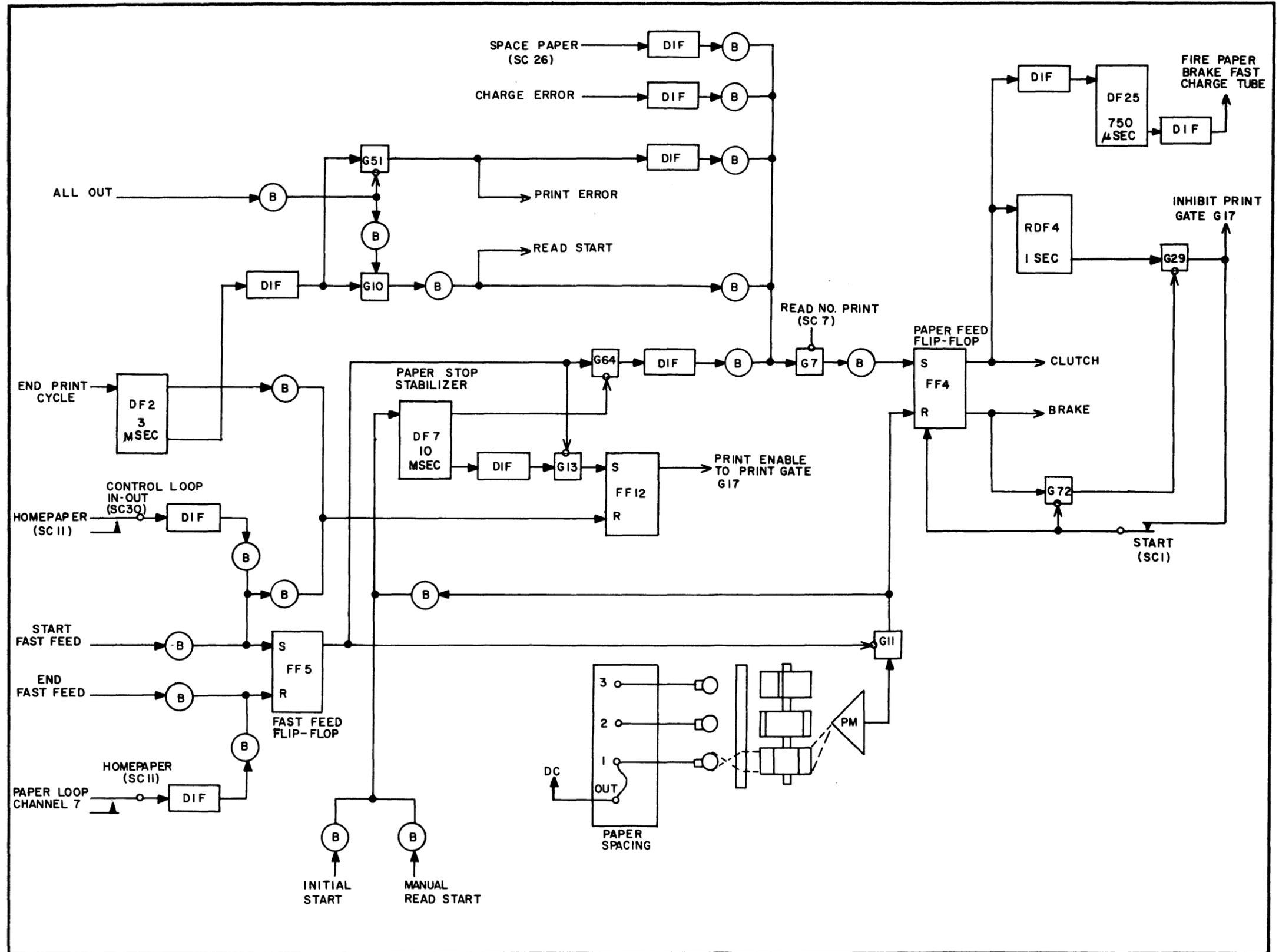


Figure 2-3. Paper Feed System
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Feed System

plate voltage resulting from the firing of V1 is coupled through the crossover network C5 and R5 to the V3 plate circuit, cutting off V3 and releasing the Brake. Delay-flop DF25 allows 750 microseconds for complete de-energization of the Brake before triggering the Brake actuating capacitor fast-charge circuitry.

The Brake must be ready for energization again when an End Paper Feed (EPF) signal arrives to restore FF4, as feeding the paper a single space requires 7.6 milliseconds; the Brake must therefore be ready for energization when the EPF pulse arrives at that time. Brake actuating capacitor C2 must be fully-charged when the Brake starts energizing. When V3 is cut off by the firing of V1, C2 begins to charge toward the supply voltage limit through R2. As the time constant of this charging circuit is about eight milliseconds, 40 milliseconds will elapse before C2 reaches full charge through this circuit. The Brake fast-charge circuitry permits C2 to reach full charge within three milliseconds following the recovery of DF25. The recovery of DF25 fires V4, the Brake fast-charge tube. In firing, V4 shunts out R2 to provide a fast-charge path for C2. When C2 reaches full charge, V4 cuts off, and the Brake circuitry is ready for energization. Should Brake tube V3 fire before V4 cuts off, fuse F2 will blow, breaking the d-c supply line.

When the paper has advanced the desired number of spaces, an EPF signal restores FF4, firing V3. The discharge of the Brake actuating capacitor supplies a high initial Brake-energizing current through the Brake solenoid. The reduction in the plate voltage of V3 resulting from the firing of V3 is coupled through R5 and C5 to the V1 plate, cutting off V1 and releasing the Clutch. Paper feeding stops, and C1 charges to the value of the supply voltage in preparation for the next Start Paper Feed (SPF) signal. Clamping diode D1 holds the V4 cathode at or above +30 volts, thus preventing the drop in V3 plate voltage from firing V4.

All Start Paper Feed signals set the paper feed flip-flop through gate G7, which is inhibited when the READ NO PRINT switch is operated. The following signals generate SPF signals:

1. Space Paper, occurring when the SPACE PAPER switch is actuated. Paper is spaced one, two, or three spaces, depending upon the spacing manually selected on the plugboard.
2. Home Paper, occurring when the HOME PAPER switch is operated. Paper advances to the beginning of the next preprinted form as indicated by a hole in Channel 7 of the paper loop. The Home Paper operation is described in detail later in this Section in conjunction with the Fast-Feed circuits.
3. Read Start, occurring after the completion of a normal Print Cycle during continuous operation.
4. Print Error, occurring after the completion of a Print Cycle during which a Print Error occurred.
5. Charge Error, occurring when a Charge Error is detected.

6. Start Fast-Feed, occurring when a Start Fast-Feed signal from the paper loop sets Fast-Feed flip-flop FF5.

All EPF signals, including those at the end of a Fast-Feed or Home Paper operation, originate from the paper feed indexing system consisting of the paper feed commutator and a light-photocell arrangement. Three independent cams are located on the paper-feed commutator, which have two, three, and six polished optical facets each, respectively. Associated with each cam is a lamp, the power source being supplied through a plugboard connection. Inasmuch as the commutator makes one revolution for each inch of paper movement, lighting the lamp associated with the six-facet cam will produce one light pulse for each 1/6-inch, or single space, of paper movement. In a similar manner, the two- and three-facet cams produce one light pulse per triple and double space when the respective lamps are lit. Thus, paper spacing is selected by connecting the desired lamp through the plugboard to the power source. In order to change the spacing selection, the secondary power is turned off, the plugboard is removed, and the required change completed. (Maintenance and operating procedures strongly recommend that plugboard changes are not effected while the plugboard is in the equipment.) The EPF pulses from the paper feed indexing system pass gate G11 to the restore side of FF4. Gate G11 is inhibited by the set side of the Fast-Feed flip-flop FF5, which is set when a Fast-Feed or Home Paper operation is initiated. The end of a Fast-Feed or Home Paper operation is indicated by the presence of a hole in the appropriate channel on the paper loop. The hole generates an End Fast Feed or End Home Paper signal, restoring FF5 and removing the inhibition from G11. This permits the next End Paper Feed pulse to restore FF4.

The Paper Stop Stabilizer performs the dual function of delaying printing until the paper is at rest after a paper feed, and of preventing the occurrence of more than one fast-feed during a 10 millisecond period.

The End Paper Feed pulse energizes the Paper Drive Brake by restoring FF4, and also energizes the Paper Stop Stabilizer by setting delay-flop DF7. After 10 milliseconds, when the paper has come to rest, the differentiated delayed output from DF7 sets FF12 through gate G13 -- unless G13 is inhibited by a Fast-Feed. The set output of FF12 is applied as an enable to print gate G17, indicating that the paper feed system is ready for the initiation of a Print Cycle. If all other conditions necessary for printing are present, G17 generates a Start Print Cycle signal, and one line is printed.

At the completion of the Print Cycle, the End Print Cycle signal restores FF12, removing the FF12 enable from print gate G17. Printing cannot again occur until the End Paper Feed pulse following the completion of the next paper feed sets DF7, to again initiate a Paper Stop Stabilizer sequence.

DF7 may also be set by an Initial Start (IS) or Manual Read Start (MRS) signal occurring after a General Clear operation. These signals set DF7 in lieu of an End Paper Feed signal, which does not occur as paper is not fed during either operation. The two signals, (IS or MRS) set DF7 not for the purpose of allowing time for paper stabilization, but rather to supply a signal to set FF12, thus permitting the generation of a Start Print Cycle signal by G17.

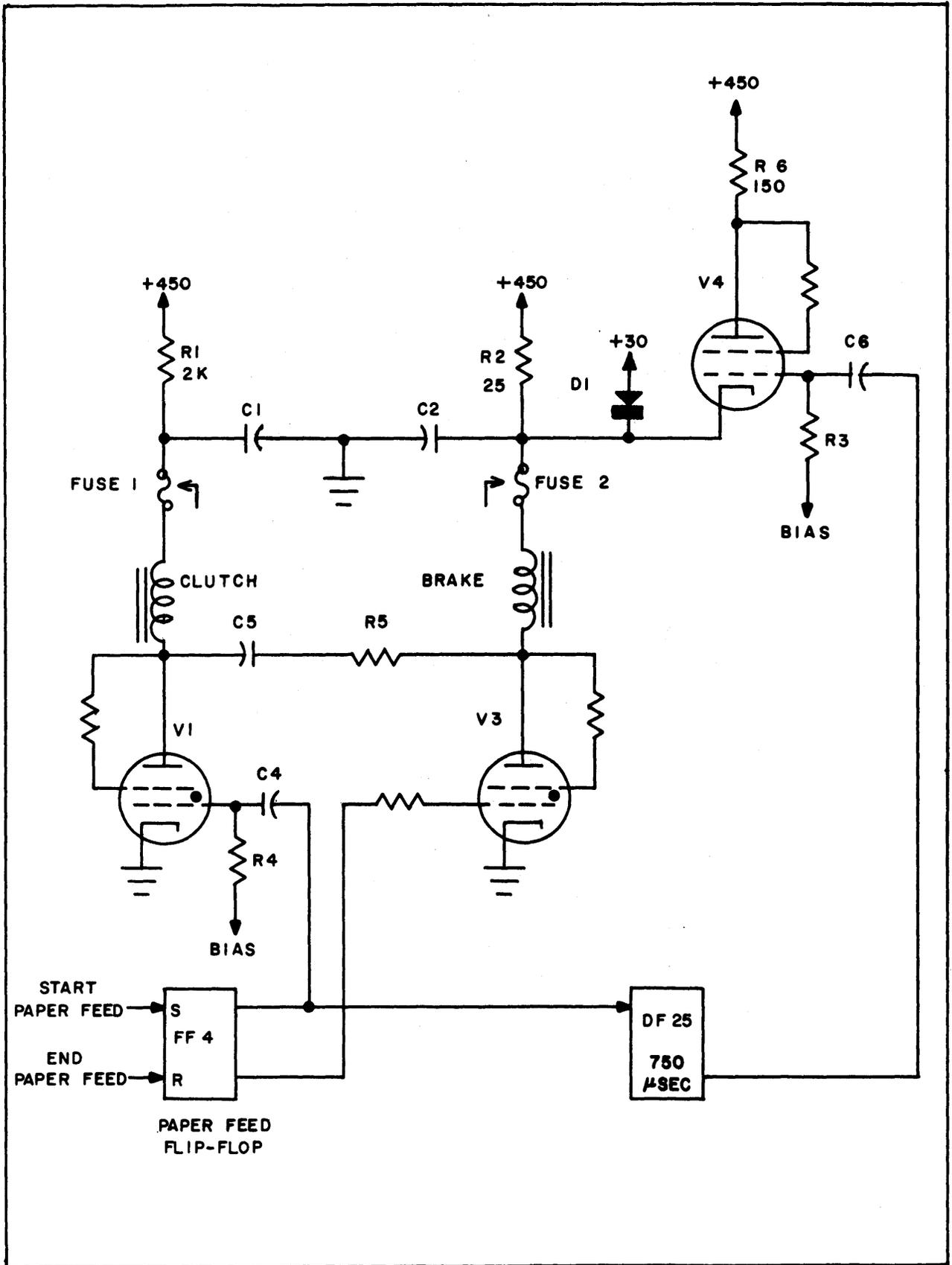


Figure 2-4. Clutch and Brake Energizing Circuit
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It is possible that an EPF pulse may pass gate G11 and trigger DF7 just prior to the occurrence of a Start Fast-Feed signal. In this case, the undelayed output of DF7 inhibits G64 for 10 milliseconds; the Start Fast Feed signal restores FF12 and inhibits G13 for the duration of the Fast-Feed. When DF7 recovers, the delayed output of DF7 cannot pass G13 because of the Fast-Feed inhibition, and FF12 cannot be set. Gate G13 thus prevents the initiation of a Print Cycle while paper is in motion during a Fast-Feed. The recovery of DF7 allows the Fast-Feed signal to pass G64, which develops a signal to start paper feed if the paper is not already in motion. Gate G64 insures that Start Fast-Feed signals cannot generate Start Paper Feed signals at intervals closer than 10 milliseconds. The End Fast-Feed signal removes the inhibition from G11, permitting the next EPF pulse to energize the Paper drive Brake and the Paper Stop Stabilizer; it also removes the inhibition from G13, allowing the delayed DF7 output to set FF12.

Due to the paper feeding at 22 inches per second, a failure of one of the normal paper-stop circuit components could result in the feeding of a considerable amount of paper before discovery of the fault and subsequent manual shutdown by the operator. The Paper Feed Error (PFE) Detector protects against such an occurrence by limiting the length of any one paper feeding to approximately 22 inches of paper. If an EPF signal does not occur within one second following the start of the paper feed, the Error Detector energizes the Paper Drive Brake to stop paper from feeding, inhibits the Print Gate to prevent a Print Cycle, and lights the P.F. CHECK indicator. The Paper Feed Error Detector is described in greater detail in this Section under "Error Detection Circuits."

c. INPUT CIRCUITS. - As each character stored on the tape moves past the Read Head, the eight tape levels (seven containing the binary code combination for the character and the eighth containing the sprocket pulse) are read simultaneously. Each character, in its binary form, leaves the Read Head as an electrical impulse, is amplified, clipped, and applied to the set inputs of the Align Input flip-flops. The sprocket signal level applied to the sprocket head amplifier is opposite in phase to the information signal, as the Read Head connection to the sprocket head amplifier is reversed.

The signal from each information level containing a "1" sets the associated Align Input flip-flop. Then the sprocket pulse, which lags the information signals by 180 degrees because of reversed polarity, passes gate G1 and restores (jam-clears) all Align Input flip-flops simultaneously. The restore side of each Align Input flip-flop is connected to the set input of the corresponding Input flip-flop. The Jam-Clear signal generates a set signal from each Align Input flip-flop where a "1" was stored, to the corresponding Input flip-flop. This transfers the character to the Input flip-flops. The restore outputs of the Input flip-flops are applied as first permissives (or enables) to the Memory input gates, thus placing at the entrance to these gates the complement of the information read from the tape. Only if a binary zero has been read from a particular tape level does an enable appear at that particular Memory input gate.

The sprocket pulse, in addition to generating the Jam-Clear signal, feeds into a delay line. After five microseconds, a delayed sprocket pulse (SP_1) emerges to set delay-flop DF9, applying for 29.9 microseconds a second enable

to the Memory gates. The gates which have both enables pass signals into the Memory to fire the Memory tubes selected by the Memory Address Function Table. The recovery of DF9 after 29.9 microseconds removes the second enable from the Memory input gates and generates a Clear Input flip-flop (CIF) pulse, which restores the Input flip-flops in preparation for the next code combination. The Memory Address Function Table is also advanced to the next Memory Address.

Successive characters are read from the tape into Memory until the Memory Address Function Table has selected all 120 Memory locations, and the Memory has been filled. Then an End Read Cycle signal stops the tape reader and starts the Print Cycle. The following paragraphs explain the function of various sections of the Input Circuit.

Normally, a SPROCKET SIGNAL is read from the tape every 80 microseconds. The period between Sprocket Signals may vary considerably, however, and may be as short as 40 microseconds without adversely affecting machine operation.

The Sprocket Signal is an alternating signal lagging the information signals by 180 degrees. Before it is applied as an enable to gate G1, the Sprocket Signal is amplified, and its negative portion is clipped. The HIGH GAIN/LOW GAIN switch controls the clip level and the bias voltage on G1. With the positive unclipped portion of the Sprocket Signal as an enable, gate G1 passes a signal to a squarer stage if no inhibition is present on the screen grid of G1. The squarer produces a jam-clear signal and an SP pulse (see following paragraphs). Inhibitions to G1 include Keyed B+, Not Reading, Rewind, Tape Load, and Bad Spot signals. These signals, in addition to inhibiting G1, generate a Jam-Clear signal, but not an SP pulse.

The JAM-CLEAR signal restores all Align Input flip-flops simultaneously, producing synchronized set signals to the Input flip-flops.

The SP PULSE is a basic timing pulse derived from the Sprocket Signal. It performs the following functions:

1. Triggers a delay line which produces two delayed pulses, SP₁ (delayed 5 microseconds) and SP₂ (delayed 7.5 microseconds).
2. Interrogates the end read circuitry; when the last Memory location has been filled, the SP pulse generates an End Read signal which stops the tape reader and starts the Print Cycle.
3. Interrogates the 120-error detector; if more or less than 120 characters have been received from the tape at the end of a Read Cycle, a 120-error signal is generated.
4. Starts a zero field if a Memory Address selected on the Start Zero Field plugboard has been reached.

The SP₁ PULSE is delayed five microseconds from the commencement of the SP pulse to permit time for the input flip-flops to stabilize after they are set by the Jam-Clear signal. SP₁ performs the following functions:

1. Triggers delay-flop DF9, placing a second enable on the Memory input gates for the 30-microsecond period of DF9.
2. Samples Function Table I; if a special function symbol is present, a Prevent Read-in signal is generated and the appropriate special function is initiated.
3. Interrogates the Odd-Even Error Detector, generating an Odd-Even Error if one is present.
4. Interrogates the Address Error Detector, generating an Address Error if one is present.
5. During a zero field, continues or stops the zero field, depending upon whether or not a zero has been read from the input tape.

The SP₂ PULSE is delayed 7.5 microseconds from the SP pulse. It performs the following functions:

1. Initiates a signal to the End Read circuitry when the last Memory location has been selected.
2. Ends a zero field if a Memory address selected on the End Zero Field plugboard has been reached.

A "1" read from an information level of the tape produces an alternating signal which leads the Sprocket Signal by 180 degrees. The signal is amplified and its negative portion clipped before it is applied to the set input of an ALIGN INPUT FLIP-FLOP (FF1A-1G). When the signal amplitude reaches the set level of the Align Input flip-flop, the flip-flop is set. The clip level is controlled by the HIGH GAIN/LOW GAIN switch. The switch, which has three positions (HIGH GAIN, NORMAL and LOW GAIN), adjusts the input circuits to compensate for the various signal amplitudes and noise levels encountered on different tapes. Most tapes will be read correctly with the switch set to NORMAL. A tape with low-amplitude signals may require a HIGH GAIN switch setting to insure that signals are not missed. A tape with a high noise level may require a LOW GAIN switch setting to prevent the reading of noise pulses as information.

Under normal conditions with a properly aligned Read Head and a satisfactorily recorded tape, all Align Input flip-flops in channels containing "ones" are set simultaneously at Time Zero. At T40 (Time +40 μ sec), the Jam-Clear signal restores all Align Input flip-flops. Those flip-flops which change state from "1" to "0" generate differentiated set signals to the corresponding Input flip-flops.

A set pulse to an INPUT FLIP-FLOP (FF2A-2G) is generated when the associated Align Input flip-flop is changed from set to restore by a Jam-Clear signal. Thus, at T40, all Input flip-flops, in channels where a "1" was read from the tape, are set simultaneously. About 35 microseconds later, a Clear Input Flip-flop (CIF) pulse, generated by the recovery of DF9, clears all Input flip-flops. During this 35 microsecond period, the Memory input gates of channels storing a "0" receive first enables, as they are connected to the restore sides of the

Input flip-flops. The pattern of first enables to the Memory input gates is therefore the complement of the character read-in from the tape.

The set sides of the Input flip-flops are connected to a network of QUARTER-ADDERS (Q1, 2, 3, 4, 5 and 6), which insures that the total number of binary "ones" is odd; if not, an Odd-Even Error signal is generated. The error detector is discussed in detail under paragraph 5.a. of this Section "Odd-Even Error."

Both sides of the Input flip-flops are connected to FUNCTION TABLE ONE, which checks each input character before it is stored in the Memory in order to determine if it is a Special Function symbol. When such a symbol is detected, Function Table One prevents read-in of the character to Memory, and activates the proper Special Function circuitry. Function Table One is discussed in detail in paragraph 2.i. of this Section.

The INPUT FLIP-FLOPS can be controlled manually by the INPUT FLIP FLOPS switches on the Test Control Panel. Raising a switch sets the associated flip-flop, and lowering the switch restores it. The INPUT FLIP FLOPS indicators light when their corresponding flip-flops are set.

Each MEMORY INPUT GATE (G2A-2G) requires two enables to produce an output signal. The first enable is present when the associated Input flip-flop is in the restored state. The second enable is received from gate G19. An SP₁ pulse sets delay-flop DF9. The undelayed output of DF9 passes gate G19, to apply a second enable to all Memory Input gates -- providing G19 is not inhibited by a Prevent Read-in signal from Function Table One, or by a Greater-than-120-error signal. Gate G19 remains enabled for 30 microseconds until DF9 recovers.

The output signal from each Memory Input gate is applied as a second enable to the 120 Memory tubes for the corresponding channel. The first enable for the Memory tubes is supplied by the Memory Address Function Table, which selects a Memory Address by applying a first enable to one Memory tube in each channel.

The recovery of DF9 removes the enable from G19 and generates a Clear Input Flip-flops (CIF) signal. The CIF signal clears the Input flip-flops and steps the Memory Address Counter to the next Memory Address. It also restores FF18 in Function Table One to remove the G19 Prevent Read-in inhibition present during a Special Symbol read-in, and sets FF23 in the Fast-Feed circuitry.

Under ideal conditions, with perfect alignment of the information recorded on the tape, with a perfectly aligned Read Head, and with identical input amplifiers, all information channels containing "1" would set their respective Align Input flip-flops simultaneously at T+0. With Sprocket signals spaced 80 microseconds apart, the Sprocket Pulse would occur exactly 40 microseconds later, at T+40.

Due to many variables, such ideal circumstances as mentioned rarely occur. Variation in head construction and in head alignment results in a condition known as tape skew, which produces a condition in which the binary digits of a given character are not read from the tape simultaneously, as should ideally occur.

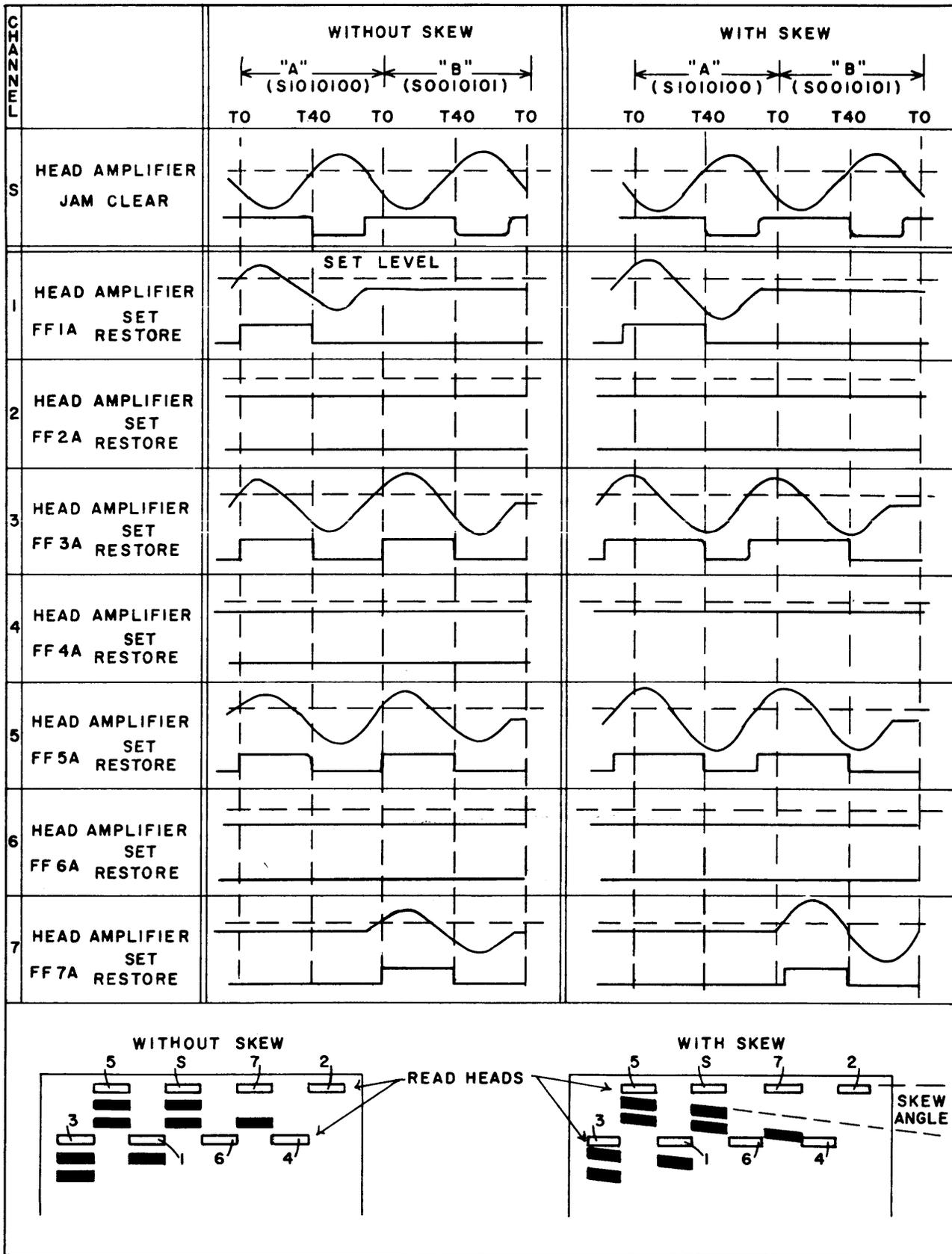


Figure 2-5. Effect of Tape Skew
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Figure 2-5 illustrates the effect of tape skew, by showing the consecutive read-in of two characters "A" and "B" from a normal tape, and from a "skewed" tape. With tape skew, the binary digits in a recorded character do not all pass over a respective Read Head simultaneously. Inasmuch as the sprocket channel is near the center of the tape, some of the skewed tape channels lead the sprocket channel, and some lag. With the Sprocket Pulse occurring at $T+40$, the Align Input flip-flops fire at various times before and after $T+0$. As the Sprocket Signal lags the information signals by 180 degrees, there is ample time for all Align Input flip-flops to be set before the Jam-Clear signal restores them simultaneously at $T+40$.

d. MEMORY CIRCUITS. - The MEMORY stores input information from the magnetic tape one blockette at a time. For each character of the blockette, there is a Memory location consisting of seven cold-cathode gas tubes. The Memory thus contains a total of 840 gas tubes for the 120 Memory locations. Each tube in a Memory location stores one of the seven binary digits comprising the coded combination for the character to be stored. Since every character that is stored must be printed-out during the subsequent Print Cycle, only printable characters are stored. The non-printable Special Symbols are prevented from entering the Memory during read-in by Function Table One. The correct Memory location for each successive character read from the tape is selected by the Memory address system. Prior to read-in, the Memory is cleared by the de-ionizing of all the Memory tubes. A blockette is then read into and stored in the Memory. When the blockette has been stored, the tape reader stops and the Print Cycle begins. The blockette remains stored in the Memory until the end of the Print Cycle; at this time, if no print errors have occurred, the Memory is cleared in preparation for the next Read Cycle. Figure 2-6 shows the Memory circuits of the Printer.

The MEMORY ADDRESS SYSTEM selects each of the 120 Memory locations in succession for storage purposes. The system consists of three major parts: the Memory Address Counter, Minor Address Function Table, and the Memory Address Function Table. The Memory Address Counter is a seven-stage binary counter which advances the Memory address line selection each time it is stepped. The Minor Address Function Table is driven by the Counter. The former contains two sections; an L section which selects one of eight L minor address lines, and an M section which selects one of fifteen M minor address lines.

The Memory Address Function Table is a diode matrix driven by the Minor Address Function Table. This matrix combines the eight L and fifteen M line outputs to produce an output on one of 120 Memory address lines. The Memory address lines, numbered from 0 through 119, apply enabling signals to Memory locations 1 through 120 respectively. Only one Memory location at a time receives an enabling signal from the address line associated with that particular Memory location.

The MEMORY ADDRESS COUNTER performs two main functions. Primarily, during the Read Cycle, a selection is made of successive address lines to the Memory as successive characters are read from the tape, and the Read Cycle is caused to end when 120 characters have been read-in and stored. Secondly, during the Print Cycle, the number of rows of typewheel characters which have passed the print hammers is computed and the Print Cycle is caused to end when one complete typewheel revolution (102 rows of typewheel characters) has been completed.

The Counter may be cleared by any one of the following signals: Initial Start, Manual Read Start, Read Start, General Clear, or Start Printing. The Counter is stepped by the restored output signal of DF9. During a Read Cycle, DF9 is set by an SP₁ pulse; during a Print Cycle, it is set by delayed PC (index) pulses. The Counter may be set manually to any desired count using the MAIN COUNTER switches on the Test Control Panel.

For Memory Address selections, the Counter outputs are applied to the Minor Address Function Table; the first three stages (2^0 , 2^1 , 2^2) go to the L section, the last four (2^3 , 2^4 , 2^5 , 2^6) to the M section. For the Print Cycle, gate G70 is enabled when the Counter reaches a count of 102.

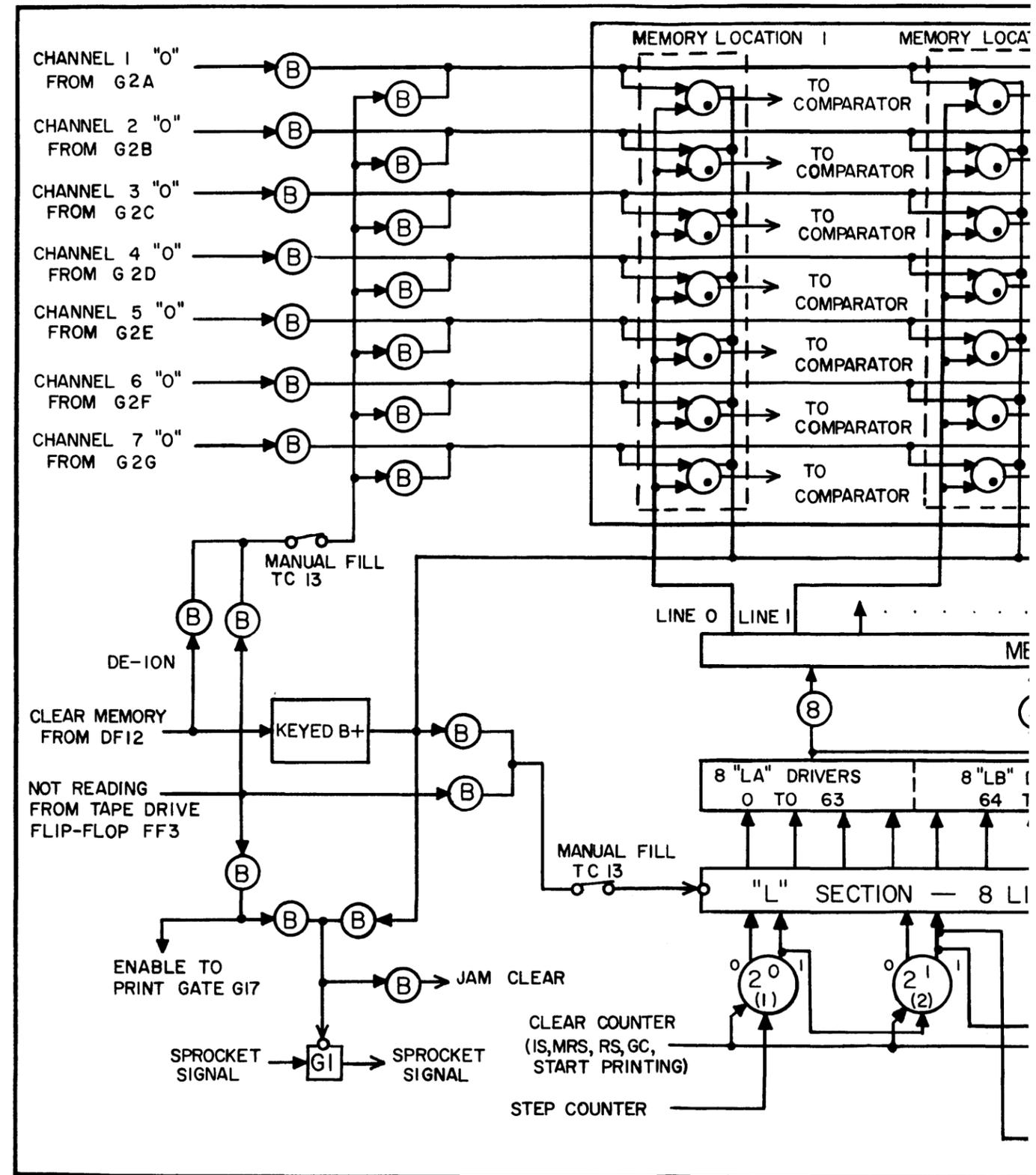
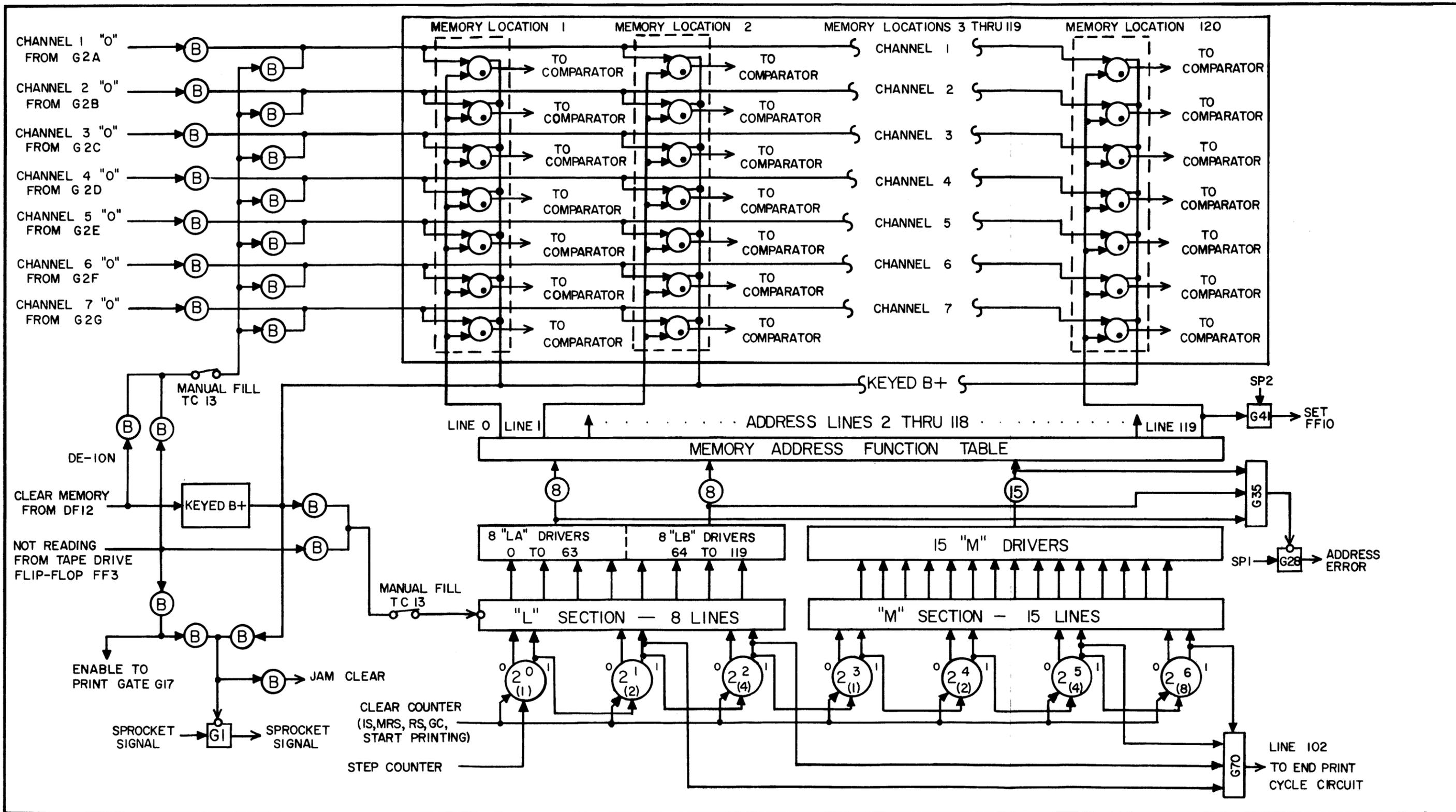


Figure 2-6.. HS Printer Memory Circuits
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The MINOR ADDRESS FUNCTION TABLE is divided into two sections -- the L section driven by the first three stages of the Main Counter, and the M section driven by the last four stages. The L section generates a signal on one of eight L section lines numbered L0 (L zero) through L7. The L line selected coincides with the count of the L section counter, which contains the first three Main Counter stages. The M section generates a signal on one of fifteen M section lines numbered M0 through M14. The M line that is selected coincides with the count of the M section counter, which contains the last four Main Counter stages. The M section advances once each time the L section recycles, since the M section counter is stepped by the carry from the L section counter. The L section counter must recycle fifteen times before the M section advances from line M0 through to line M14. At that time, 120 consecutive address lines have been selected by the Memory address function Table, and the Read Cycle has been completed.

Both the L section and M section outputs are applied to drivers which are coupled to the Memory Address Function Table. Because of the number of Memory Address Function Table circuits driven by each L section line, the L section drivers have been split into two parallel sections, labelled the LA and LB drivers. The LA drivers serve Memory address lines 0 through to 63; the LB drivers serve address lines 64 through 119. The M section drivers serve all address lines.

The Not Reading line inhibits the Minor Address Function Table whenever the tape is not in motion, thus preventing an address line from being selected.

An address line may be selected manually while the tape is at rest by setting the MANUAL FILL switch on the Test Control Panel. This action removes the Not Reading inhibition from the Minor Address Function Table, allowing the use of the MAIN COUNTER switches in the manual selection of an address line.

The address line selected is the same as the binary value set in the counter. For example, address line 109 is selected when the counter is set to a binary value of 1011011, (note that in this application, counting is accomplished left-to-right). The decimal equivalent of this binary number is 109. This may be determined by adding the binary values of the counter stages: $1 + 0 + 4 + 8 + 0 + 32 + 64 = 109$. To determine the L section and M section lines enabled when a given address line is selected, divide the counter setting by eight; the integer obtained in the dividend corresponds to the M line, the remainder to the L line. For example, if address line 109 has been selected:

$$\frac{109}{8} = 13 \text{ plus remainder of } 5$$

M line = M13

L line = L5

To simplify the determination of the L and M lines selected for a given address line, read the L section counter (the left three indicators) and the M section counter (the last four indicators) separately, and translate the binary equivalent value to decimal form. For example, with address line 109 selected, the counter reads 1011011 from left to right; the L section counter is set to

1 + 0 + 4 (or 5), the M section counter is set to 1 + 0 + 4 + 8 (or 13). Thus, L5 and M13 are selected.

The MEMORY ADDRESS FUNCTION TABLE is an 8 x 15 diode matrix driven by the Minor Address Function Table. The outputs from the eight L section lines and the fifteen M section lines are translated in the matrix to produce an output from one to 120 address lines. The address lines, numbered from 0 to 119, are connected as first enables to Memory locations 1 through 120 respectively.

Only one L section line and one M section line may be selected at any given time. Each L section line is applied to fifteen address line gates, one for each M section. The LA drivers service address lines 0 through 63, the LB drivers lines 64 through 119. When L section line 0 is selected, for example, the LOA (L zero A) and LOB drivers are energized. The LOA driver applies enables to address line gates 0, 8, 16, 24, 32, 40, 48, and 56; the LOB driver to address line gates 64, 72, 80, 88, 96, 104, and 112. In a similar manner, the other seven LA and LB drivers are connected to their respective address line gates. Each M driver applies an enable to eight address line gates, one for each L line. When M line 0 is selected for example, address line gates 0, 1, 2, 3, 4, 5, 6, and 7 receive M line permissives. Similarly, the fourteen remaining M line drivers are connected to their respective address line gates. With the counter set to 0, address line gate 0 receives both LOA and M0 enables, and address line 0 applies a first enable to the seven Memory tubes comprising Memory location 1. When Memory location 1 has been filled, DF9 recovers, clearing the input circuits and stepping the Counter to 1. When the Counter advances to 1, L1 is selected in place of L0, and the M0 selection remains. Address line gate 1 receives both L1A and M0 enables, causing address line 1 to apply a first enable to the seven channels in Memory location 2.

The process of selecting a Memory location, reading into it, and then selecting the next Memory location continues until the L7-M14 combination has appeared, selecting address line 119 and enabling Memory location 120. At that time, gate G41 receives an enable from address line 119. When the next SP₂ pulse probes G41, an output pulse occurs to set FF₁₀ and initiate a sequence which eventually stops the tape reader and ends the Read Cycle.

As previously mentioned, the 120-error circuit insures that no more, nor less than 120 characters have been read-in during the Read Cycle. If an error is detected, the 120 CHECK indicator lights, and the Printer stops before the Print Cycle begins. In addition, the Address Error Detector insures that an address line is selected each time a character is read from the tape. If at least one LA, one LB, and one M section line are not selected for each character read-in, gate G38 removes an inhibition from gate G28. The next SP₁ pulse then passes G28, triggering the Address Error circuit; but the Printer continues operation until the end of the Read Cycle, then stops with the ADDRESS CHECK neon lamp indicating an error.

The Memory is arranged in the form of a matrix with each address line feeding the seven Memory tubes in one Memory location. Each channel input line feeds one Memory tube in each of the 120 Memory locations. The Memory is initially cleared by a Clear Memory signal originating from the set side of delay-flop DF12. The Clear Memory signal lasts for 5.5 milliseconds which is the period of DF12. During this time, a de-ionizing signal is applied to the grid of each

Memory tube, and a reduced, keyed B+ voltage is applied to the anode of each Memory tube. As a result, all Memory tubes are cleared to a non-conducting state. The Clear Memory signal also applies an inhibition to the Minor Address Function Table, preventing the selection of an address line during the Clear Memory operation.

The Memory stores "0's" rather than "1's"; a conducting tube represents a "0", a non-conducting tube a "1". It may, therefore, be stated that the Memory actually stores the complement of the input character. A Memory location storing a legitimate, printable character always has either two, four, or six fired tubes. The storing of "0's" rather than "1's" improves the self-checking function of the Printer. All printable combinations of the Printer code contain at least two "0's", while some contain only a single "1". In storing "0's", therefore, any legitimate combination stored should cause at least two Memory tubes to fire. If one Memory tube fails to fire, the Memory location stores an unprintable combination, and the tube which does fire causes a Print Error to occur. If "1's" were stored rather than "0's", failure of a Memory tube to fire upon reading of a character containing only a single "1" would result in the occurrence of an undetected error, as there would be an empty Memory location rather than one containing an unprintable combination. Storing "0's", therefore, greatly reduces the occurrence of undetected errors.

Each channel input line to the associated Memory tubes is driven by a Memory input gate. To produce an output, a Memory input gate requires two enable inputs, a first enable from the "0" side of the input flip-flop, and a second enable from gate G19. A character is read-in from the tape, and is transferred to the input flip-flops at time SP. The channels containing "0's" clear the respective input flip-flops, applying first enables to the appropriate Memory input gates. At time SP₁, delay-flop DF9 is set, applying an enable to gate G19. If there are no inhibitions on G19, an output is the result, this output applying a second enable to the Memory input gates. The Memory input gates receiving both enables produce outputs which appear as enables on the appropriate groups of Memory tubes. These enables last for 30 microseconds, the delay period of DF9. In order to fire, a memory tube must receive two enables; one from the channel input line, the other from the Memory address line. In a given Memory location, all seven Memory tubes receive a first enable from the same Memory address line. Each one of the seven receives a separate second enable from the respective channel input line when a "0" has been read. During the 30-microsecond delay period of DF9, the tubes in the selected Memory location that are receiving enables from the associated channel input lines fire, thus storing the complement of the character read from the tape. The recovery of DF9 removes the second enable from the Memory input gates, clears the input flip-flops, and generates a Step Counter pulse to select the next Memory address. The process of reading a character, storing it, and selecting the next address continues until the Memory has been filled.

A typical Memory tube with its associated input circuitry is shown schematically in Figure 2-7a. The tube shown, V4, is that for Memory location #1, Channel 1. This tube fires when address line 0 has been selected, and a "0" has been read in to Channel 1.

Memory address line 0 is selected when minor addresses L0 and M0 are selected. Minor address line L0 drives tube V1, and line M0 drives V2.

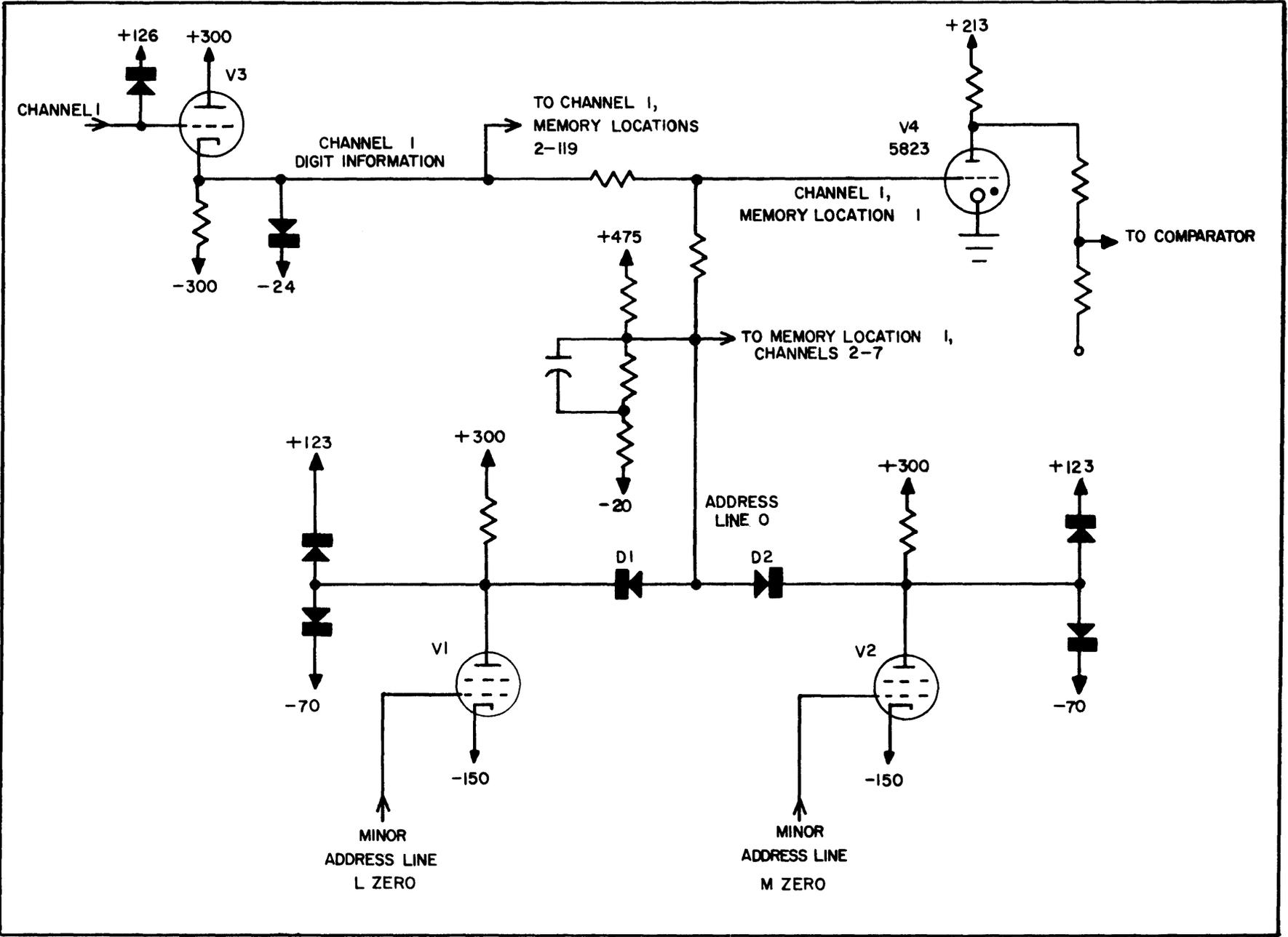
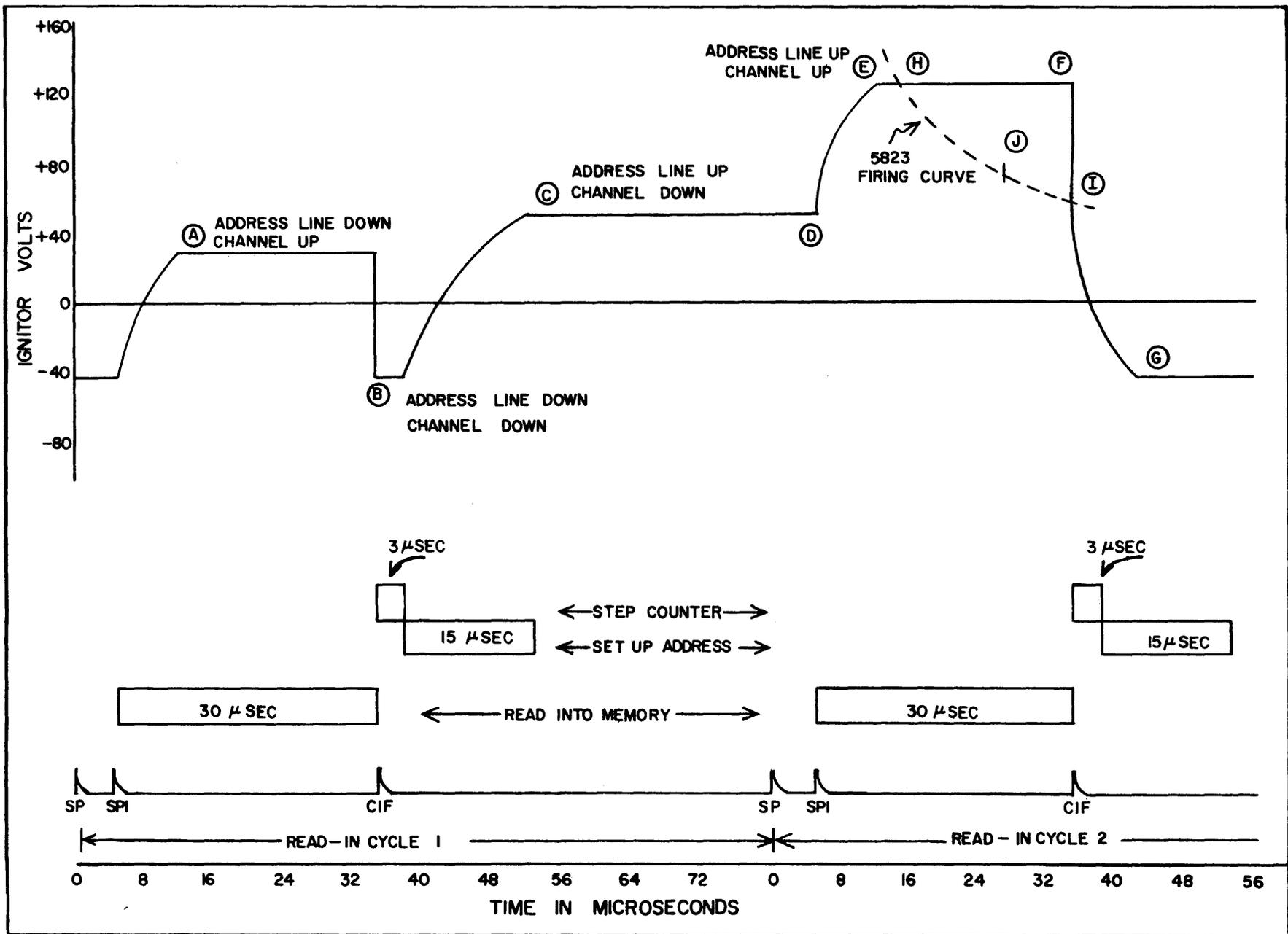


Figure 2-7a. Typical Memory Tube Circuit

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Figure 2-7b. Typical Memory Tube Curve
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When neither LO nor MO are selected, V1 and V2 both conduct, the plates being clamped to -70v. When both LO and MO are selected, V1 and V2 cut off, and both plate potentials rise to +123 volts. The Memory address line follows this voltage rise, applying a first enable to Memory tube V4 and the other six Memory tubes in Memory location 1. The Memory address line voltage cannot rise unless both the LO and MO lines are selected, since one unselected minor address line holds the Memory address line voltage to -70 volts.

Tube V3 is the digit driver for Memory tube V4. Unless a "0" has been read-in, V3 is cut off, and the output voltage of V3 to V4 and the other 119 Memory tubes in channel 1 is at a level of -24 volts. Upon read-in of a "0", the V3 grid voltage rises from cut-off to +126 volts for the 30-microsecond period of DF9. The V3 output voltage rises, applying a second enable to all Channel 1 Memory tubes. Memory tube V4 fires, since it is also receiving a first enable from address line 0.

Prior to the firing of Memory Tube V4, the latter's anode potential is held at +140 volts by the divider action of the Code Wheel inputs to the Comparator circuits. A clamping circuit in the Comparator prevents the anode potential from rising above +180 volts, as any potential above +200 volts fires the tube regardless of ignitor potential. Firing V4 drops the anode potential to +62 volts, at which point it remains until the Memory is cleared at the end of the Print Cycle.

The ignitor potential of a Memory tube varies with the signals applied to it by the respective Memory address line and channel input line. Figure 2-7b shows the variations in ignitor voltage occurring during the read-in of two successive zeros. The first "0" is read-in with the address line unselected, the second with the address line selected. At time T+0, an SP pulse commences the first Read-in Cycle. Both the address line and channel input line are at a negative level, and the ignitor potential is -41 volts. Five microseconds later, the SP1 pulse sets read-in timer DF9, applying an enable to the channel input gates through read-in gate G19. As a "0" has been read-in, the channel input line rises, bringing the ignitor voltage to +28 volts, the voltage indicated at point A. At T+35, DF9 recovers, generating a Step-Counter pulse and removing the enable from G19. The channel input line voltage drops, returning the ignitor voltage to the -41 volts shown at point B. The counter steps to the next address in three microseconds, selecting the address line. The address line voltage rises to a steady value within fifteen microseconds, producing an ignitor voltage of +48.5 volts at point C. The ignitor voltage remains at this level for the remainder of the 80-microsecond first Read-in Cycle, and through the first five microseconds of the next Read-in Cycle; until an SP1 pulse again sets DF9 (point D). The channel input line begins to rise, producing an ignitor potential of +124.5 volts at point E. The Memory tube firing curve intersects the ignitor potential curve at points H and I; the tube fires at some time between these points, probably before point J is reached. When DF9 recovers at point F, the channel input line voltage drops because the enable on G19 is removed, and the address line voltage drops because the counter steps to the next address. The ignitor voltage therefore returns to -41 volts, while the Memory tube remains fired.

e. CODE GENERATOR CIRCUIT. - The CODE GENERATOR continuously emits pulsed information respecting the type character appearing in line with the print hammers at the moment. This information is channeled to the various Code Generator circuits indicated in Figure 2-8, Code Generator Circuit. Mounted on the same revolving shaft as the 130 typewheels is a Code Wheel which combines an Index pulse wheel, Odd-Even wheel, and Clear wheel. Facets on the periphery of the three combined wheels rotate in synchronism with the typewheels on a common shaft.

The Index Pulse wheel contains 102 equally-spaced facets, (one for each character on each typewheel). Simultaneously with an apposition between a row of characters on the typewheel and the Print Hammers, one of the facets of the Index pulse wheel, by reflecting light to a photomultiplier tube, generates a Typewheel Index Pulse. The Odd-Even wheel has facets spaced in such a manner that one is present whenever a change is required in the check pulse for the character of the moment. The Clear Wheel contains but one facet which is located electrically in a position between the Index wheel facets for the characters "%" and "-". The Clear wheel primarily provides synchronization between the combined code wheels and associated electronic circuits.

Light rays from lamps, which pass through a lens and are reflected from the polished facets as narrow light pulses, are detected and amplified by the type 931A photomultiplier tube. Phasing between the three code wheels is accomplished by shifting the position of the aperture openings to the photomultiplier tube. A more precise synchronization is further accomplished by varying the angle of reflection of the optical system mirror. The pulses from the photomultiplier tube are passed to the Code Generator circuits which are located in the main Power Supply cabinet. The correct relationship of the code wheels to each other is shown in Figure 2-9, Relationship Between Index Typewheel and Code Wheels.

In addition to the code wheel, the Code Generator section contains a six-stage binary counter which advances with every second Index Pulse; also BC1, another binary counter stage which indicates accordingly as to whether or not the characters are odd or even. The Code Generator continuously emits pulsed information respecting the type character appearing in line with the Print Hammers at the moment. This information is channeled to the various Code Generator circuits indicated in Figure 2-8, Code Generator Circuit. G54, 55, and 56 are gates which automatically cause the binary counter to skip a count when a code combination representing special symbols on the typewheels is encountered. An Index Pulse Alternator, identified as BC2 interrupts the index pulses into alternate odd and even pulses and thereby supplies a step pulse to the six-stage counter every second index pulse. The Zero Cross Detector, ZCD2, detects pulses from the Index pulse wheel, the output of which sets DF16. DF16, the Probe Code Generator Timer develops the stepping pulses for BC2, the Pulse Alternator.

Following the binary representation of each type character in the Code Generator counters as they occur, this information is passed via gating circuits to the Comparator for further action. Refer closely to Figure 2-8 and Figure 2-9 for the detailed discussion that follows.

The logical sequence of operation of the Code Generator circuits is now discussed, with the initiation of this sequence being the Clear pulse. Figure 2-9 indicates the position of this facet with respect to the Odd-Even (O.E.) and Index facets, and the Code Wheel relationship to a portion of the typewheels. The binary count is also shown, but this, of course, does not appear on any wheel.

As previously mentioned, the Clear wheel has only one facet, thus producing one output pulse for every complete revolution. It will be observed that the Clear pulse occurs immediately following the even Index pulse representing the "percent" (%) symbol. The typewheel shaft turns at approximately 750 rpm when printing 600 lines per minute. The Index pulses therefore occur at intervals of 784 microseconds. The Clear pulse is phased to occur 484 μ sec following the Even Index pulse representing the % symbol, or conversely, 300 μ sec prior to the Index pulse representing the "hyphen" (-) symbol.

For the purposes of this explanation and as would be the case in fact, immediately prior to the arrival of the Clear pulse the Binary Counter contains the combination 11 1101, which represents the % symbol. BC1 is in the "0" state.

The Clear pulse now leaving the photomultiplier tube passes to BC1, BC2 and the six binary counter stages. BC1, being in the "0" state, remains as "0". BC2 however, is triggered to the "1" state, and all Code Generator binary counter stages (B, C, D, E, F, and G) are triggered by the pulse on the Clear pulse line. It will be noted by following this circuit that the counter will now contain 000001.

Following the Clear pulse, 300 μ sec later approximately, the Odd Index pulse representing the hyphen (-) symbol is detected by ZCD2, a Zero Cross Detector, with the output setting Delay flip-flop DF16. The set output of DF16 passes through a differentiating stage and appears as a pulse on BC2, stepping BC2 to the "0" state. The only output from BC2 which will step the Code Generator binary counter is a differentiated "zero" pulse. In this instance, this occurs now, and the "0" side of the "G" counter is stepped to "0", with a "carry" pulse being developed and passed on to counter "F". The count in the Code Generator binary counter will now be 000010. Referring to Figure 2-9 it will be observed that this is the count for the hyphen (-) symbol on the typewheels. The combined output from the Code Generator to gates G26A through G26G is passed to the Comparator. Should the circuitry of the Comparator indicate the presence of this combination in Memory, a cycle is initiated to produce a "print" action. This will be explained in detail in a later section.

It is possible for the Code Generator binary counter to count to decimal 64. There are 63 combinations on the High-Speed Printer, but only 51 characters may be printed. The counter therefore "skips" a count each time a code combination is presented which does not have an equivalent typewheel representation. Accomplishment of this occurs through the action of SKIP GATES G54, G55 and G56.

Following the release of the pulses to the Comparator as indicated in the preceding section, 784 μ sec later the Even Index pulse for the hyphen symbol passes ZCD2 and again sets DF16. The differentiated output of DF16 triggers

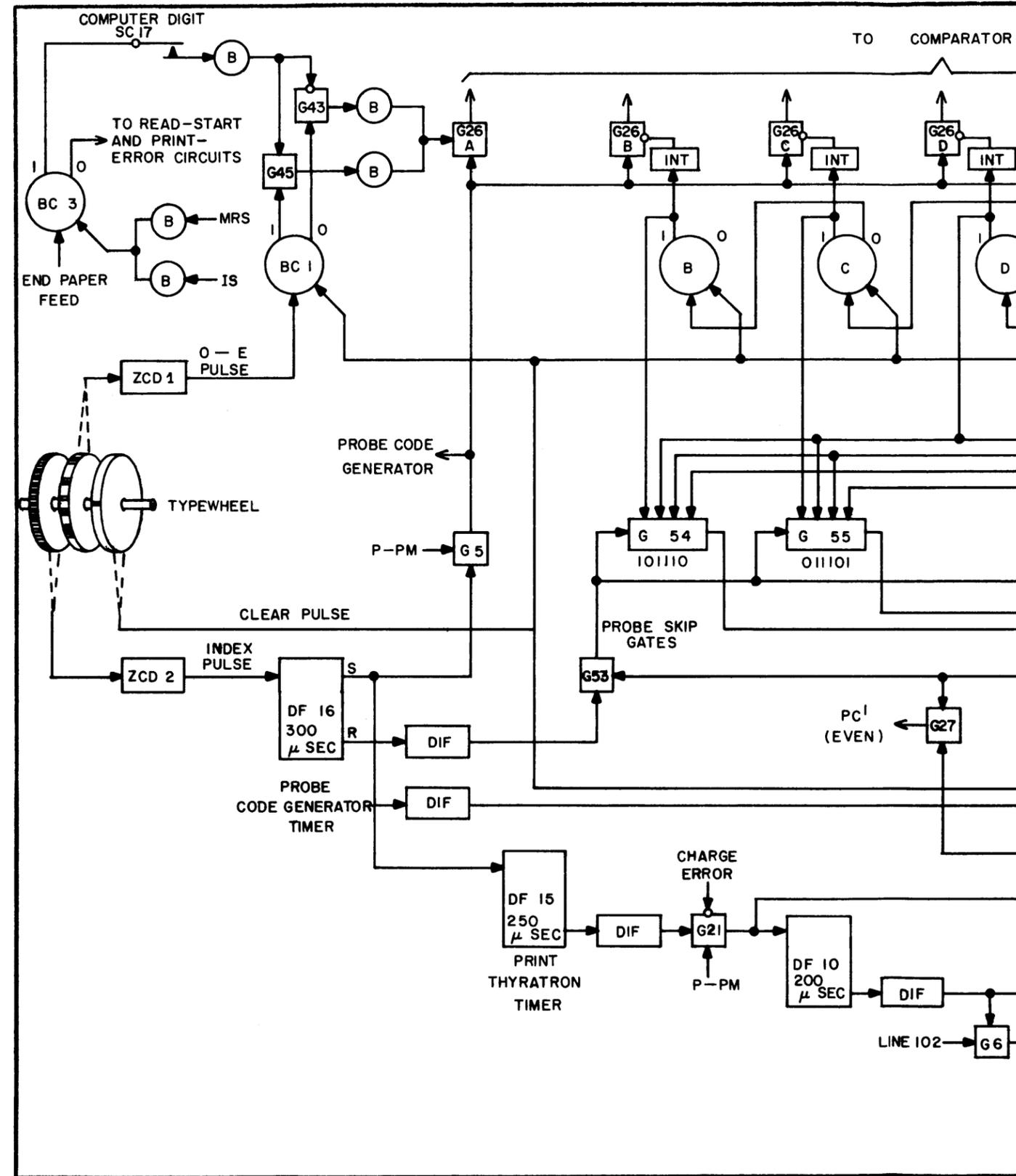
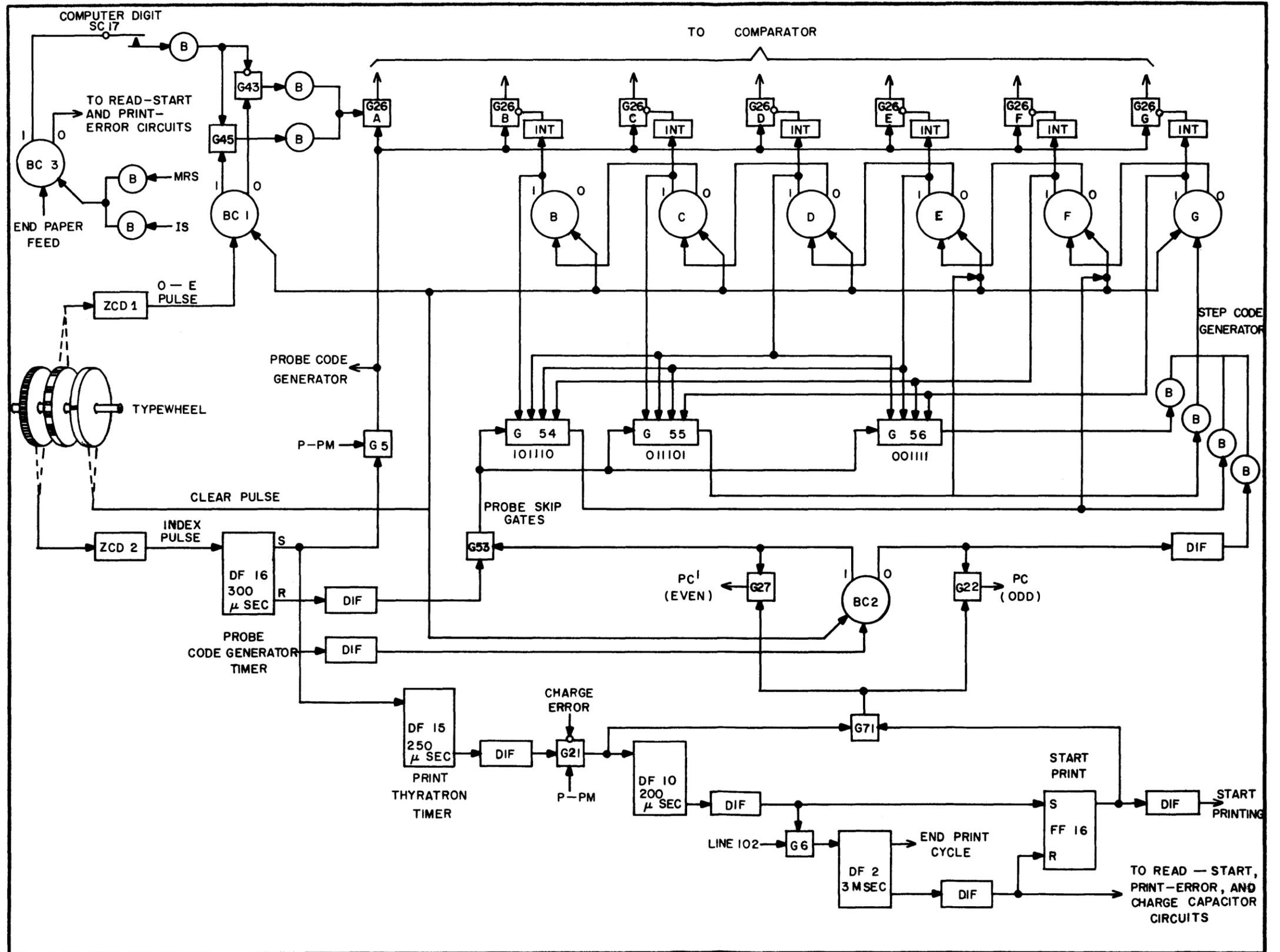


Figure 2-8. Code Generator Circuit
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1 11 1001	W
1 11 1010	X
0 11 1011	Y
1 11 1100	Z
0 11 1101	%
0 00 0010	-
1 00 0011	0
0 00 0100	1
1 00 0101	2
1 00 0110	3

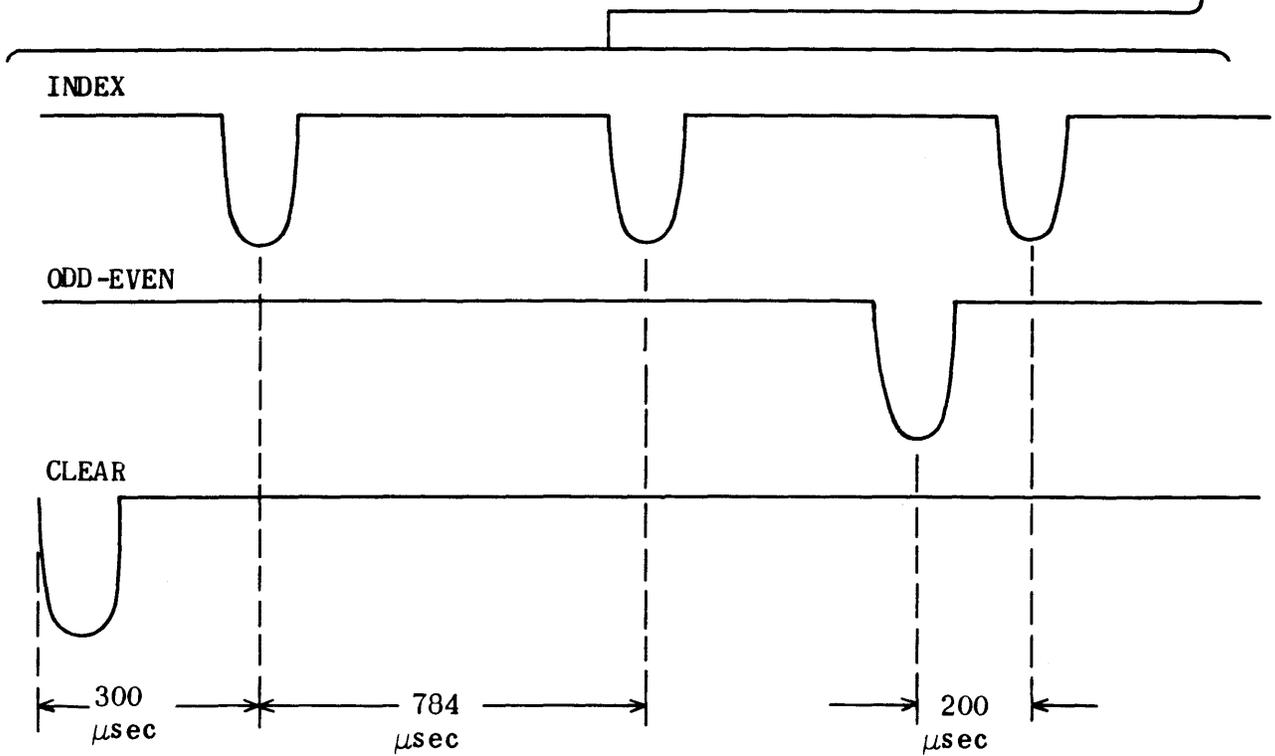
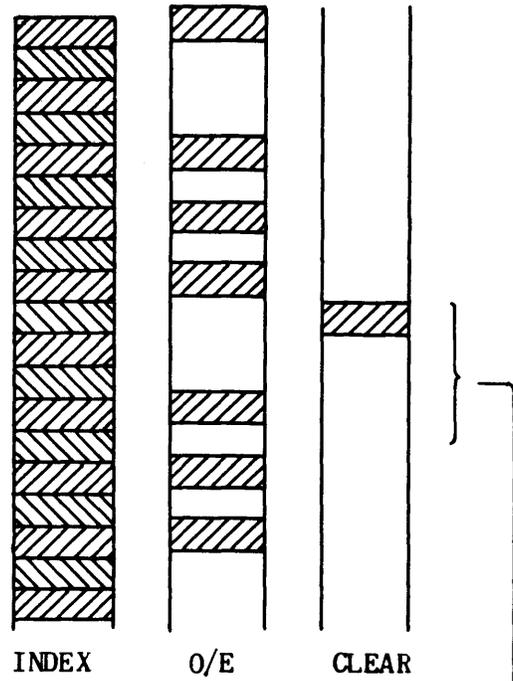


Figure 2-9. Relationship Between Index Typewheel and Code Wheel
PX 616

BC2 to the "1" state, and this in turn places an enable upon gate G53. Delay flip-flop DF16 recovers 300 μ sec later, the differentiated recovery output pulse passing through Gate G53 (enabled by BC2) and probing gates G54, G55, and G56 simultaneously. Should an enable be present on any or all of gates G54, G55 or G56, the pulse from the Skip gate will change the Code Generator binary counter reading to the code combination preceding the next character that is printable. The following Index pulse triggers BC2 to "0" and the binary counter is advanced. The counter reading will now correspond to the reading of a type character opposite the print hammers. In order to clarify the operation of this circuit, further examples of the sequence are given below.

Normally, following the passing of the hyphen symbols described previously, stepping of the binary counter continues until the odd Index pulse for the parenthesis "on" sign "(" sets DF16. The output pulse of DF16 triggers BC2 to the "0" state, and in turn the binary counter reaches 001111. As BC1 is on the "1" side, the combined gate output is 1 001111, which is the coded combination for (. At this point, the outputs from the D, E, F, and G gates are applied as enables to Skip gate G56, (and also G54 and G55). Delay flip-flop DF16 recovers 300 μ sec later, the restored output being differentiated and applied to G53. However, it is not possible for this output to pass G53, inasmuch as there is no enable from BC2 on G53 -- BC2 being in the "0" state. The even Index pulse for the (symbol passes through ZCD2, triggering DF16. This places BC2 in the "1" state via the differentiator, thus enabling G53. DF16 recovers following the delay of 300 μ sec, the restored output being differentiated and passing through G53, (the latter now being enabled). This pulse now probes G54, G55, and G56, (see Figure 2-10).

Gate G56, which received enables from counters D, E, F and G now passes the pulse received from G53 to step the Code Generator, which steps counter G to "0". The carry pulse from G is applied to F, triggering it to "0" also, with "1" carry, the additive process continuing until the counter reads 01 0000 -- the total combination at the output gates being 1 010000, a combination for which there is no printable type equivalent.

The odd Index pulse for the comma (,) symbol is passed through ZCD2, 484 μ sec later, thus setting DF16. The output of DF16, differentiated, triggers BC2 to "0" and thus the G counter to "1". The combination total is now 1 010001, which is the combination for the comma symbol. In the manner shown, the gating circuits and Skip gate G56 has prevented the application of an unprintable combination to the Comparator -- skipping the unprintable combination but accepting the next printable one. A Skip will be initiated by a coded combination immediately preceding the non-printable combination or combinations to be "skipped." Although the preceding has indicated Skip gate G56 as accomplishing the "skipping" action in this instance, it will be clear that other unprintable coded combinations will actuate the two remaining gates G54 and G55.

- * f. COMPARATOR CIRCUIT. - As previously described under 2 d., Memory Unit, all address lines in the Memory are transformer-coupled to the Check and Print thyratrons, with the coupling transformer being double-ended. The initiation of a "Print" signal permits the output of the Code Generator to probe the Comparator. Should equality be found in the Comparator with the code

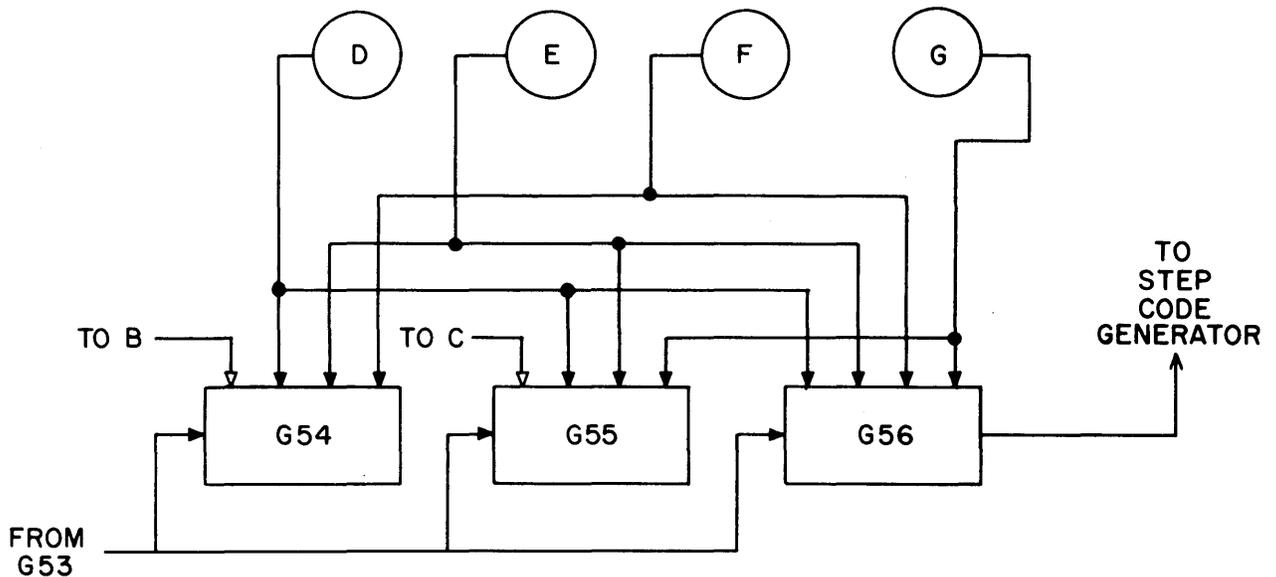


Figure 2-10. Pulse Path from G53 to Step Code Generator

combination being passed on from the Code Generator, a current will flow in one-half of the coupling transformer primary winding. This causes a voltage rise in the secondary of the transformer which is applied to the first grid of the Print thyratrons. Later action causes the Print thyatron to alert the hammer-actuator driving circuits with a consequent printing action.

Reference should again be made to Figure 2-8, Code Generator Circuit, in addition to Figure 2-11, Comparator Actuating Circuits, in order to follow the ensuing explanation.

In order that the output (G26) of the Code Generator may probe the Comparator, a final enable must reach the output gates (G26) from G5. This pulse is applied to all parts of G26 simultaneously. The release of this pulse through G5 is in turn dependent upon a final enable applied to G5 from Flip-Flop 20 (FF20). This enable from FF20 originates with the Start Print pulse which is applied to DF3 as the Leading Edge (LE) of the Start Print pulse.

DF3, which delays the pulse 300 μsec , originates a recovery (Print) pulse which passes G57 and sets FF20, the set output of which is applied to G5 (and G26).

The fact that G5 is only enabled during actual printing insures that the Comparator also is probed only during actual printing. In order that the comparison process may be fully reliable the complete 300 μsec output of DF16 must reach the Comparator.

The 300 μsec Probe Memory pulse also from DF3, passes G47 and samples all Memory locations to see if information is being stored. As any Memory location storing information will have an output at that time through the Comparator and plugboard to a Check tube, the Probe Memory pulse will act as a final set to these tubes. During the Print Cycle the output of the Comparator is channeled via the plugboard and single line relays to the Print and Check thyratrons, where it is applied to the control grid of these tubes. It should be noted at this point that the only Print and Check tubes receiving this output will be those connected to a Memory location which is actually storing information.

As the Print signal which reaches G5 may arrive at any time totally unrelated to the Code Generator action, the initial comparison, if released, could be unreliable. In order that a signal of less than 300 μsec will not be used by the Comparator the initial Index output of G21 is not used. As an example of the method in which this is accomplished the following is given.

Assume that the Code Generator binary counters contain 01 0111, which is the code combination for the character "D". In addition, it will be assumed that BC1 is in the "1" state, BC2 at "0", DF15, DF16 and FF16 restored, and G5 and G21 lacking enabling signals.

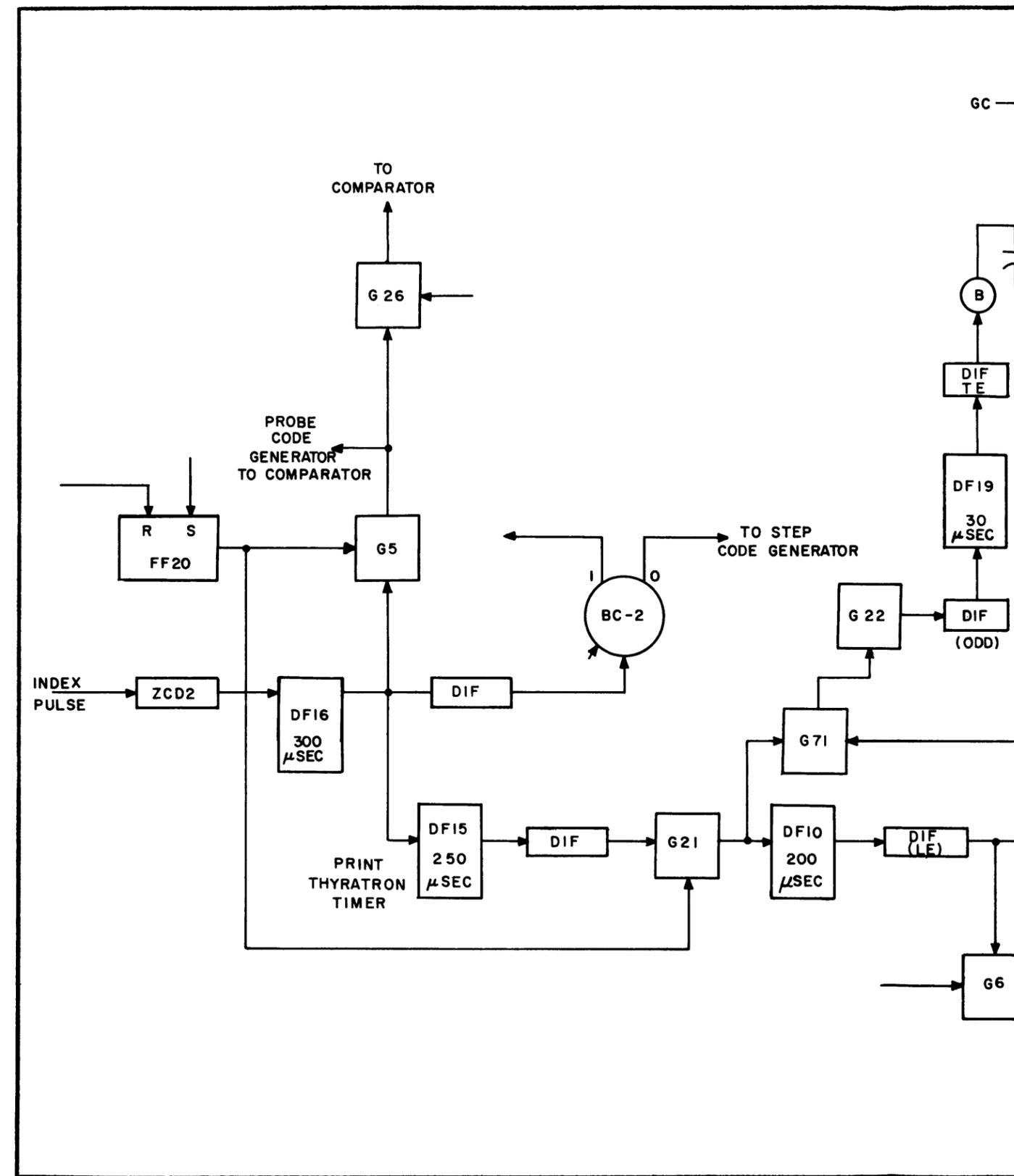
DF16 is set by the even Index pulse for the character D. The set output of DF16 is applied as a sampling pulse to G5, but inasmuch as G5 has not been enabled by FF20, no transfer occurs. Simultaneously, the output of DF16 is applied to BC2 through a differentiator, changing it to a "one" condition, (it being a bistable device); and to DF15, the Print Thyatron Timer. Following this action, 100 μsec later FF20 is set, passing a final enable to both G5 and G21. G5 in turn develops an output pulse which acts as a final enable to G26. The coded combination for "D" is therefore released from G26 and channeled to the Comparator for comparison with every Memory location.

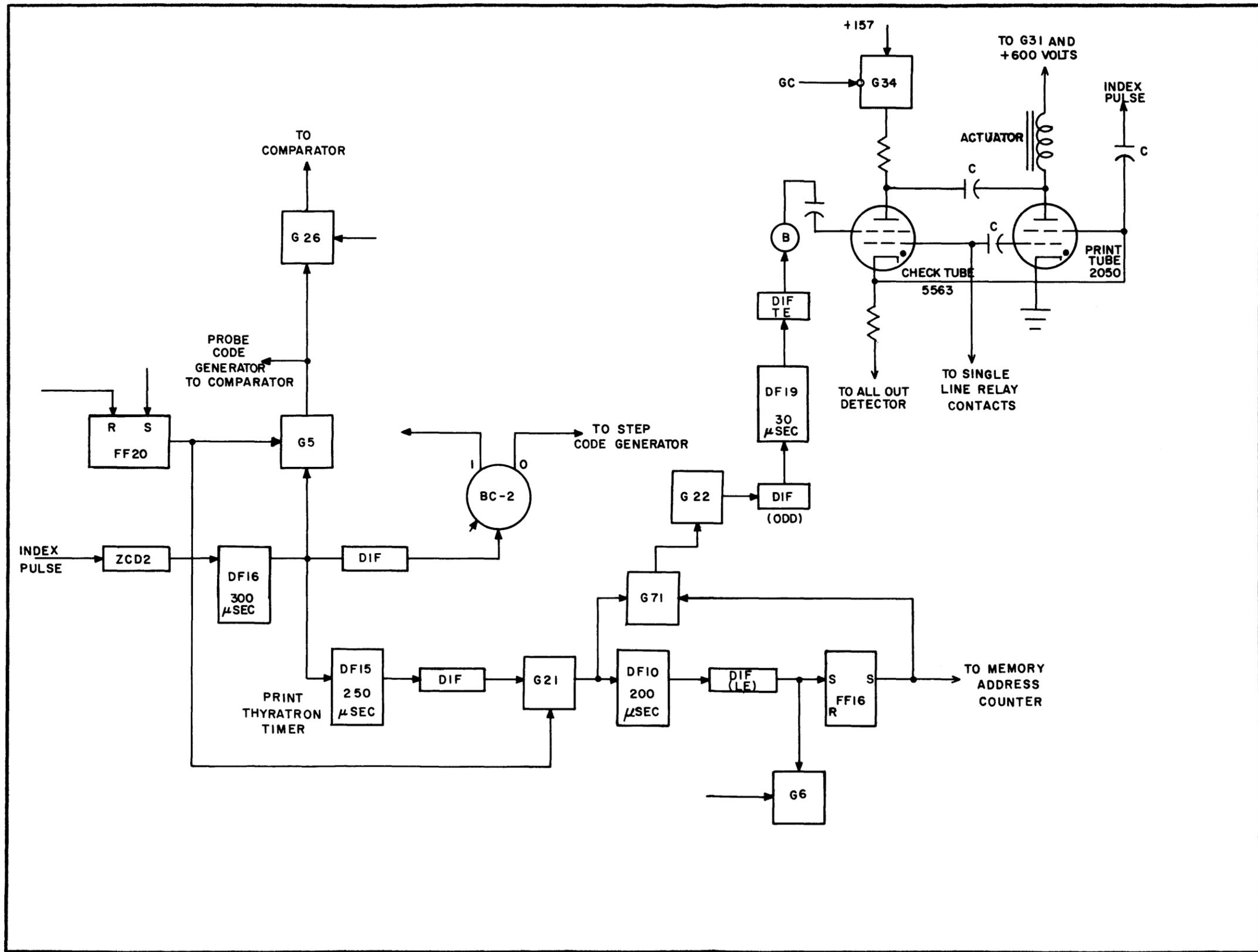
DF15 recovers 150 μsec later, with the restored output being differentiated and passed to G21, which is sampled. (Note that at this point the output to the Comparator has been in progress for only 150 μsec -- insufficient time for the Comparator circuits to stabilize and the enable to the Print locations to reach the required value). The output from G21 passes both a sampling pulse to G71 and a setting pulse to DF10. As G71 does not have a required enable from the output of FF16, the first Index pulse terminates at G71.

Thus far, it will be noted that the greater part of the Comparator action has been occurring in the so-called Code Generator circuits, and this is true for the most part. However, the effects of this action are directly related to Comparator action which may be shown by continuing the example given in the preceding paragraphs.

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Figure 2-11. Comparator Actuating Circuits
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Actuating Circuits

DF16 recovers 50 μ sec later, thus removing the Probe Code Generator signal and the enable that was on G26. DF10 recovers 150 μ sec following this action and the restoration pulse is differentiated and transferred to G6 (which is not fully enabled) as a sampling pulse, and as a set pulse to FF16. G71, therefore, receives a first enable from FF16, with the leading edge of the FF16 output pulse being routed to the Memory Address Counter to clear it to binary "0".

The odd Index pulse for the character E passes through ZCD2 334 μ sec later, thus setting DF16. The set output of DF16 in turn sets DF15, and enables G5, with the leading edge of the pulse from DF16 being differentiated and used as a set signal to BC2, which returns to a "0" state. This in turn, changes the binary code counter to a binary count of 01 1000. As G5 has enables from FF20 and DF16, G26 passes the coded combination to the Comparator, and as shown in Figure 2-11, the Probe Code Generator channel is also receiving an enable.

All Memory locations now storing the letter "E" will agree with the coded combination from the output gates, and an enable will be placed on the Comparators which are associated with these locations. The Probe Code Generator signal which is being received at the Comparator from G5, will pass through the Comparators which are enabled, and thus, will place an enable on the control grids of the Print and Check tubes which have previously been connected to the Comparators via the plugboard. The voltage on the control grids of the Print and Check tubes will have reached maximum amplitude 250 μ sec later, and DF15 will have recovered state. The recovery output pulse from DF15 is differentiated and passes through G21, G71 and G22, developing an odd Index pulse to DF19, which is thereby set. The pulse output of DF15, differentiated, may be considered a firing pulse to the screen grids of all odd Print thyratrons. However, the only thyratrons to fire will be those already enabled by the voltage from the Comparator appearing on the respective control grids, and which have associated Check tubes in a fired condition.

g. CHARGE CAPACITOR, AND PRINT AND CHECK CIRCUIT. - Reference is made to Figure A, the large overall logical diagram at the end of this manual, in the following description of these circuits.

Each print position, of which there are 130, consists of one type 2050 thyratron tube, identified as a Print thyratron, and which acts as an actuator driver; one electromechanical actuator and associated mechanical components which forces a hammer against the typewheel (paper and ribbon riding between the two); one 5663 thyratron tube, identified as a Check thyratron; and one actuator capacitor and an associated diode.

The capacitor in the plate circuit of each Print thyratron is charged through a diode to +600 volts during the Read-in Cycle. At the commencement of the Print Cycle, the Fast Charge circuit, through which the capacitor charges, is disconnected. This makes the actuator capacitors the sole source of energy for the type 2050 Print thyratron plates. In this manner, a particular print location can be fired but once for each Print Cycle. An inhibiting signal on Gate G31 from FF21 prevents the capacitor from charging during the Start Print Cycle. This inhibition is removed when the +600-volt enable is applied to G31.

The 600-volt potential reaches G31 via a contact on relay RE2. The solenoid of RE2 is actuated by a contact of RE1, which in turn is solenoid-controlled by gate G49. G49 supplies an enabling current to this solenoid except under three conditions, the occurrence of any one or more releasing RE1. These are: the typewheel drum carriage "out"; absence of correct grid-bias on the type 2050 (Print) thyratrons and also to gate G31; and the presence of a Charge Error (which is described under 5.f. of this Section).

When the contacts of relay RE2 close, a circuit is completed which supplies an enable through buffer stages to G31, G23 (the Ribbon Feed Control gate) and G30; and a differentiated output as a reset pulse to FF21, the Charge Capacitor flip-flop. It will thus be noted that the removal of a final inhibition from G49 will always produce a Charge Capacitor signal.

One example of the above situation would be in the case of a Charge Error being developed and GENERAL CLEAR being actuated with carriage moved "in." Another situation could be in the event of applying secondary power with the carriage "in", in which case the Grid-Bias Failure will be the final inhibition to be removed. However, should either of the above actions be attempted there is a possibility of a component failure.

The CC signal, when restoring FF21, removes the inhibition from G31 and the enable from G60, which permits the charge line to increase from zero potential to +600 volts. The +600 volts acts as an enable on G63 and as a voltage source for all actuator capacitors.

The plate voltage supply for the Check tubes arrives by way of gate G34. The Check tubes are normally de-ionized by the associated Print tubes, therefore G34 is only used as a closed gate in the event of an error. In this event the GC signal is applied as an inhibition to G34, thus removing the plate voltage from the Check tubes.

The Check tubes accomplish four main functions:

1. To alert the Print tube that the Memory location to which it is connected is storing information to be printed.
2. To alert the error-checking circuits that the Print location has failed to print information stored in the Memory location (incorrect or correct information).
3. To alert the error-checking circuits that the Print Location has printed information not stored in the Memory location.
4. To alert the error-checking circuits that no information stored in the Memory location which is connected to the Print location, has been correctly printed.

Conditions 2 and 3 are abnormal situations and will result in the machine coming to a stop at the end of a Print Cycle and with an Error being indicated.

Before the mechanical action of a Print Cycle occurs, each Memory location is sampled in order to determine whether or not information is being stored. As this Probe Memory operation occurs, the Memory locations that are storing information will channel an alerting pulse by way of the Comparator to the respective Print location. The alerting signal places one enable on the control grid of the Print and the Check tubes. A Probe Check Thyatron (PCT) pulse next samples the screen grids of all Check thyatrons simultaneously. The Check thyatrons sustaining an alert signal on the control grid will now conduct.

A Memory location which has one, or all seven tubes conducting will develop an alerting pulse during the Probe Memory operation. Note that a Print tube will be alerted for a print phase regardless of whether the information being stored is correct or incorrect.

As the Check tube conducts, the increase in cathode potential is coupled to the screen of the Print tube, thus acting in the manner of a partial enable, the increase being insufficient however, to cause the tube to ionize. When the Check tube is fired, it will remain in a conductive state until de-ionized by the firing of the associated Print tube.

At the time the coded combination from the Code Generator establishes a comparison with the coded combination in Memory, an alerting pulse is channeled from that particular Memory location to the Print location associated with it. This pulse will act as an enable on the control grids of both the Print and Check tubes for the respective location.

At exact firing time the Print tube receives a final enable from the Code Wheel circuits, this enable being applied to the screen grids of the Print and Check tubes. Note that the Print tube must be fired in advance of the alignment between the character to be printed and the Print Head, due to the hammer transit-time.

The Print tube will be fired by the combination of the three enables, thus discharging the associated capacitor through the actuator solenoid. The print hammer moves rapidly against the typewheel (the ribbon interposed), thus printing the character. The negative swing in the plate potential of the Print tube is coupled to the Check tube, causing the Check tube to cease conduction. The amplitude and duration of this negative pulse is such that the plate potential of the Check tube will be held below the ionization point for a time greater than 100 μ sec but not beyond 600 μ sec. By this means the Check tube is incapable of refiring prior to 100 μ sec following the firing of the Print tube.

Further amplification of the circuits discussed in the foregoing will be found in this Section under 3.d., Print Cycle.

h. RIBBON FEED CONTROL CIRCUIT. - (Refer to Figure 2-12, Ribbon Feed Control, in the following theoretical description.) Mechanical coupling to the typewheel shaft provides the means of driving the ribbon feed. This coupling is controlled by an actuator energized by the output of G29. One enable that is impressed on G29 is derived from the actuator power-supply circuit, and will not be present unless the carriage is in the "in" position. This, therefore, prohibits the ribbon from feeding unless the Printer is actually

involved in a printing operation. By restricting the feeding of ribbon in this manner, conservation of ribbon during maintenance is accomplished.

The other enable on gate G29 originates from RDF3, a 50 msec retriggerable delay-flop. RDF3 will be set at the time that FF20 is set, and will remain in this state until 50 msec following the resetting of FF20. In effect, therefore, the enable will be impressed on G29 for the entire Print Cycle plus 50 msec into the duration of the Read Cycle. In this operation (precluding the possibility of a long Bad Spot, or long Fast-Feed), the ribbon will move continuously during machine operation.

i. FUNCTION TABLE ONE CIRCUIT. - Function Table One, also known as the Decoding Function Table or Special Symbols Decoder, consists of thirteen gates, each receiving one enable from the outputs of various combinations which originate in the Input flip-flops. The Input flip-flops transfer a first enable to the gates, with but one exception -- the Zero Decoding gate, which receives both an enable and sampling pulse from the Input flip-flop source. The final enable in the case of the first twelve gates issues from Sprocket Pulse 1 (SP₁), which samples all gates at the same instant. The gate which has an enable from the Input flip-flops passes the pulse to the circuit for which it is intended (e.g., Breakpoint).

Figure 2-13, Function Table One Logic, indicates the logical circuits involved in the operation of this section of the Printer, and should be referred to in following the information in the next paragraph. Figure A (at end of Manual) should also be referred to in order to obtain information beyond the scope of the simplified diagram.

A signal from any of the Input flip-flops will appear at the Function Table One gates as an enable. The final enable will arrive from a delay circuit as Sprocket Pulse (SP₁) One. This permits a pulse to leave the gate concerned and proceed (a) to the Special Function circuitry; (b) to FF18, via a buffer. At the latter flip-flop the pulse will act as a set pulse for FF18, the Prevent Read-in flip-flop, which releases a pulse to gate G52.

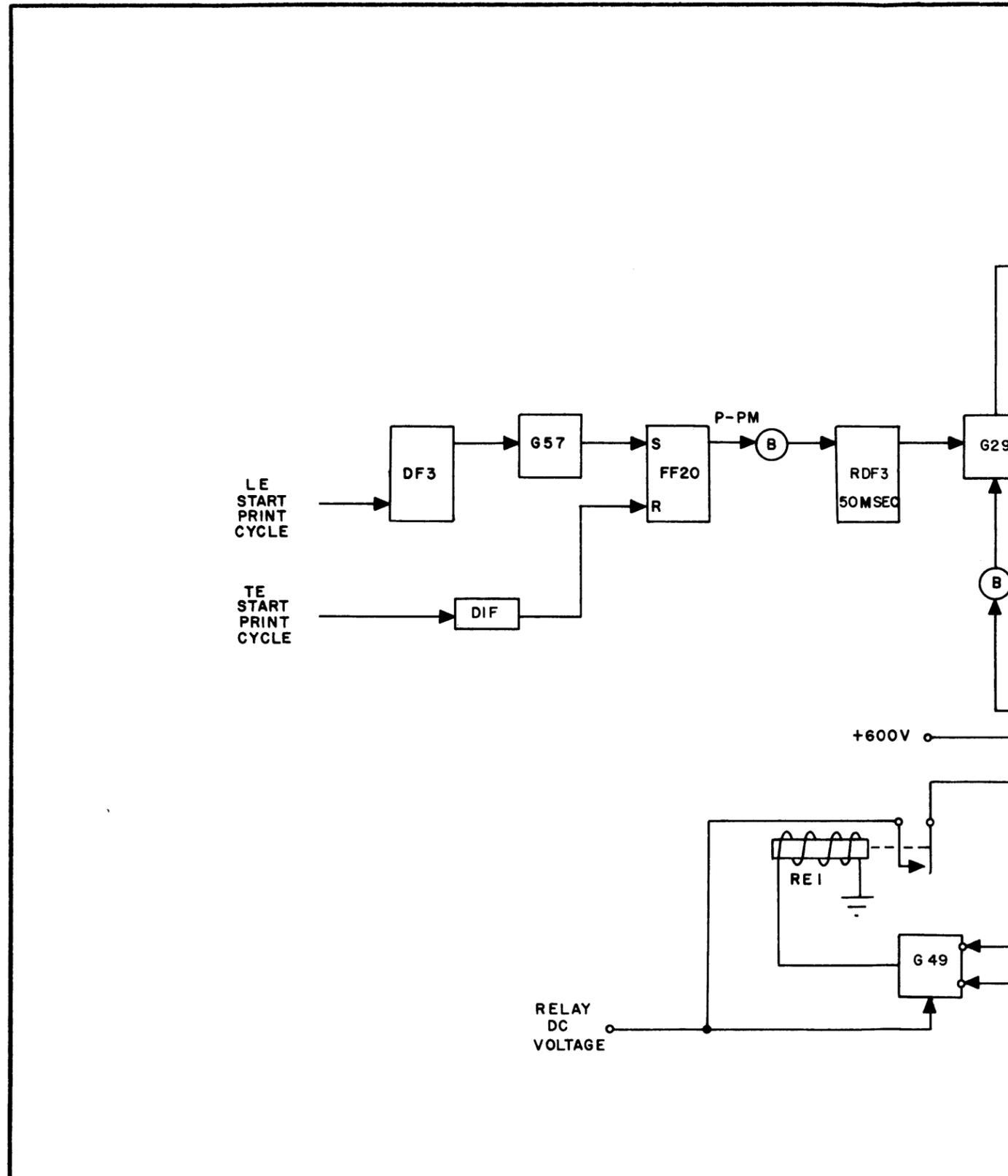
The output of gate G52 acts as an inhibitive signal on gate G19, the Prevent Read-In control gate. As may be seen, FF18 will be set simultaneously with DF9, and the inhibiting Prevent Read-in signal will arrive at G19 at the same instant that the output pulse of DF9 reaches it. Further study indicates that the inhibiting signal will be removed as DF9 recovers, inasmuch as the recovery pulse of DF9 restores FF18, with a consequent lack of pulse to G52.

Therefore, during a normal read-in of a special symbol, G19 is inhibited for the duration of the set pulse from DF9, and thus no special symbols are stored in Memory.

3. EQUIPMENT OPERATIONS

a. TAPE LOAD. - During NORMAL operation in order that a pre-determined amount (115 inches) of tape may pass the Read Head prior to information being read from the tape, and following the installation of a new roll on the machine, the Tape Load operation is required. If this were not observed, tape

Figure 2-12. Ribbon Feed Control
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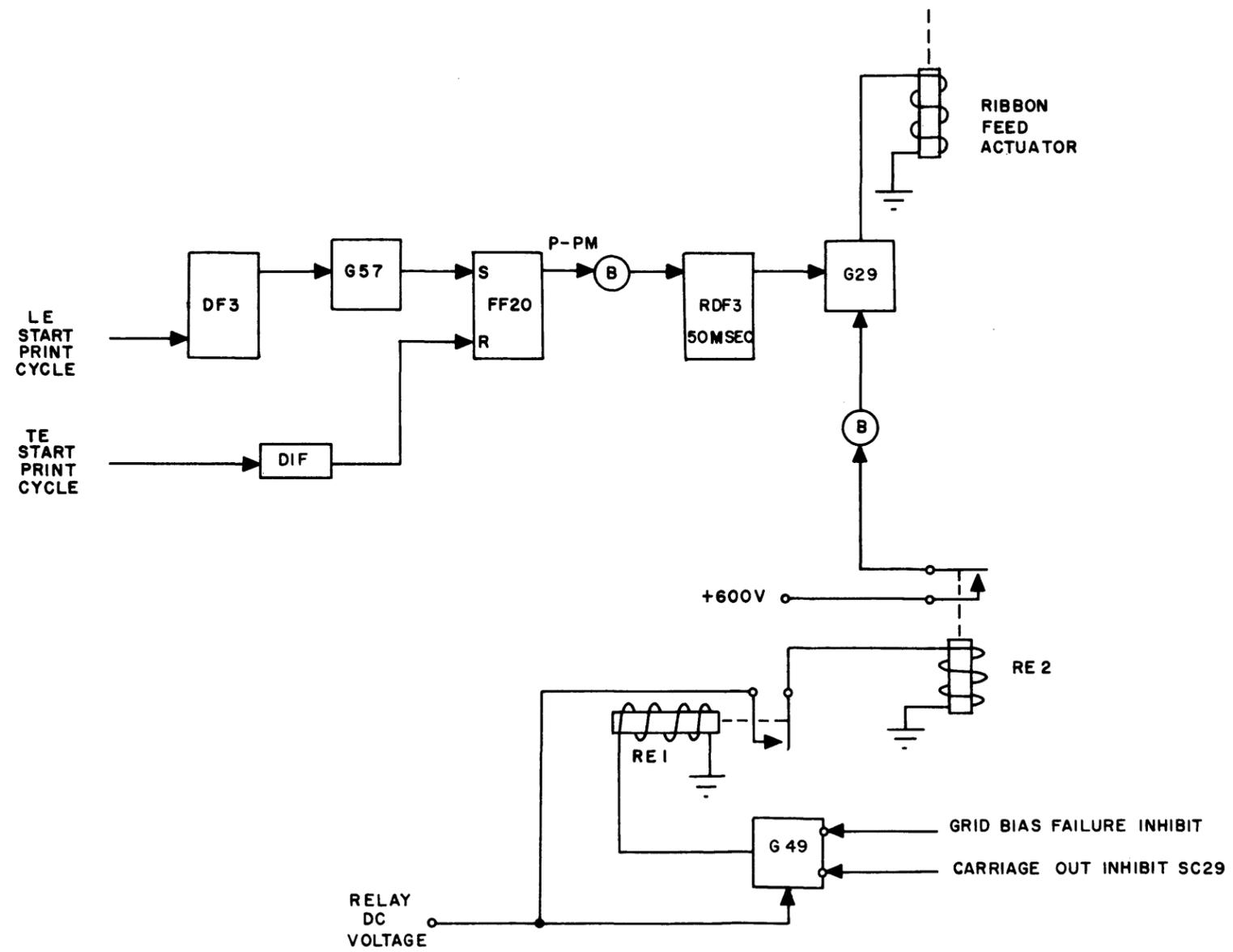
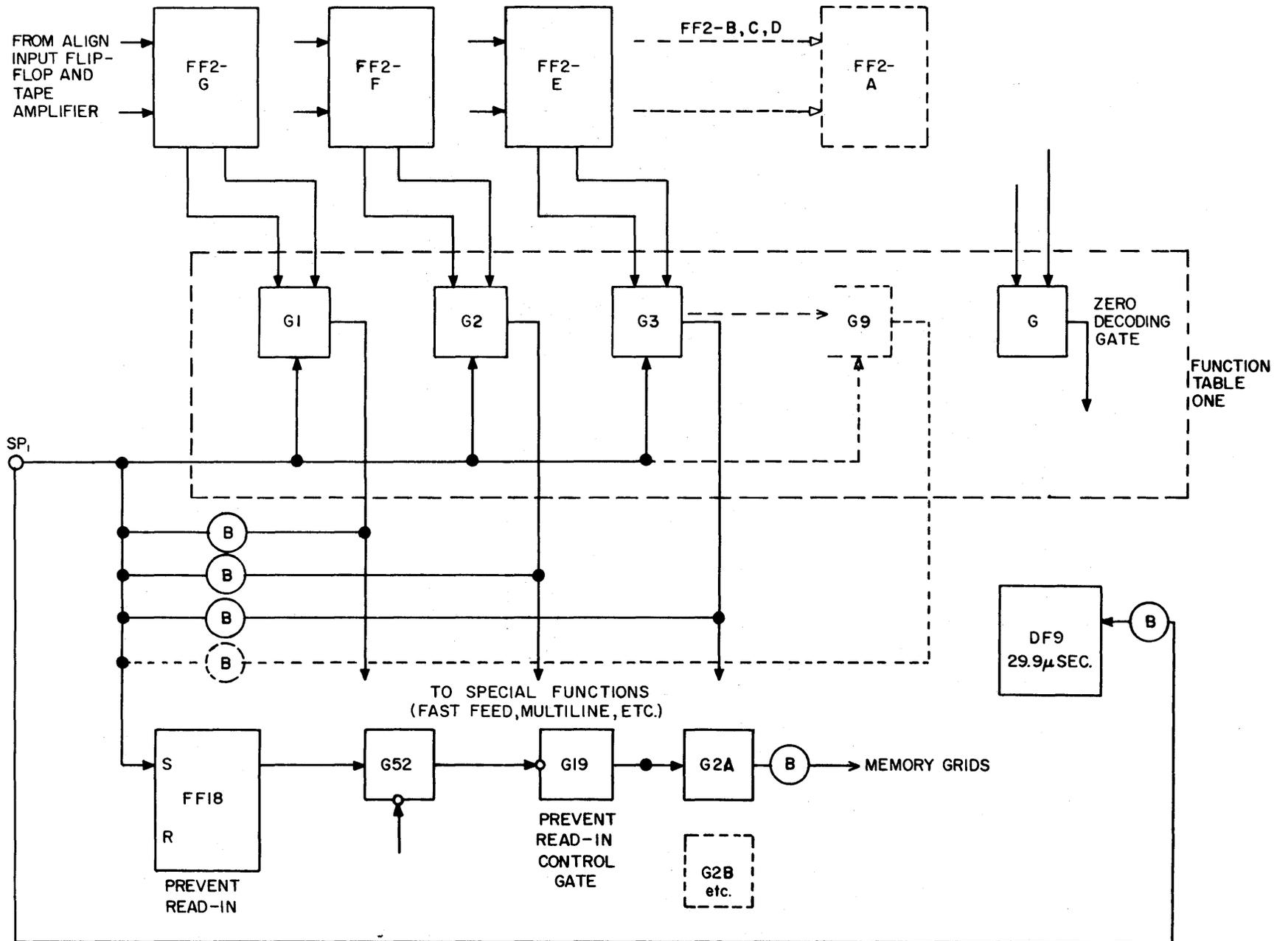


Figure 2-13. Function Table One Logic



noise and lack of completion of the Clear-Memory function would actuate the equipment in an unnecessary manner. Refer to the simplified drawing in Figure 2-14, Tape Load Operation, in the description that follows.

The Tape Load operation commences with the closing of SC12, the Tape Load switch. The switch is located on the Supervisory Control Panel shown in Figure 1-6, with a functional description in Table 2. The closing of the Tape Load switch will light the Tape Load indicator on the same panel (Figure 1-7), to indicate that a Tape Load operation is occurring. As the START and INITIAL START switches are electrically interlocked with the Tape Load switch, whenever the latter is actuated the former two are inoperative, thus insuring that the Start functions cannot occur while Tape Load is in progress. An output from the Tape Load switch SC12 when actuated, reaches the inhibit line of the tape inputs by way of a buffer, which effectively prevents spurious noise from entering the input channels during the Tape Load sequence.

The output from SC12 supplies an enable to G50 which is also differentiated and applied as a set pulse to DF6, the Tape Load Timer having a delay of 1.15 seconds. The setting of DF6 supplies an inhibitive pulse to G50, therefore preventing the enable from the Tape Load switch from passing the gate and producing an output signal. The output of DF6 is differentiated also, and, after passing through a buffer, passes G23, the Single Line control gate, this output pulse acting as a set pulse to DF1. Following a delay of 2.5 milliseconds, the restored output pulse of DF1, after being differentiated and passed through a buffer, sets FF3. The drive-clutch is then caused to engage by the restored output of FF3, and tape feeding commences. The tape is fed for a total of 115 inches, the time required being 1.15 seconds. DF6, which has a delay of 1.15 seconds, recovers at the end of this time, and this removes the inhibitive signal from G50. The enable from SC12, which was applied to G50 now passes through, is differentiated, and passes through a buffer stage to FF3, which it resets. Thus the center drive impulse is removed, which consequently disengages the clutch and stops the tape drive.

Recording tape occasionally contains faulty areas that are unsatisfactory for recording purposes due to high inherent noise, lack of magnetic material, poor splicing, etc. The areas affected may be small, such as a few inches or up to several feet in length.

The unsatisfactory areas are identified on the Univac tape by the punching of holes every two and one-half inches throughout the faulty portion of tape, with a punched hole always occurring immediately preceding and immediately following the affected area. The Central Computer, in writing a tape for the High-Speed Printer, is alerted to the faulty portion of tape by the punched holes, and does not record in that area. As the Central Computer will not complete a blockette of information should a faulty portion of tape be encountered, a "Bad Spot" as the area is termed, may appear during a blockette or between blockettes. It is a requirement of the High-Speed Printer circuits, that Bad Spots which appear between blockettes be spaced in a manner that will identify the Bad Spot prior to the read-in, not following it. Should the latter occur, a second blockette must also be read and an error will be registered on the Control Panel.

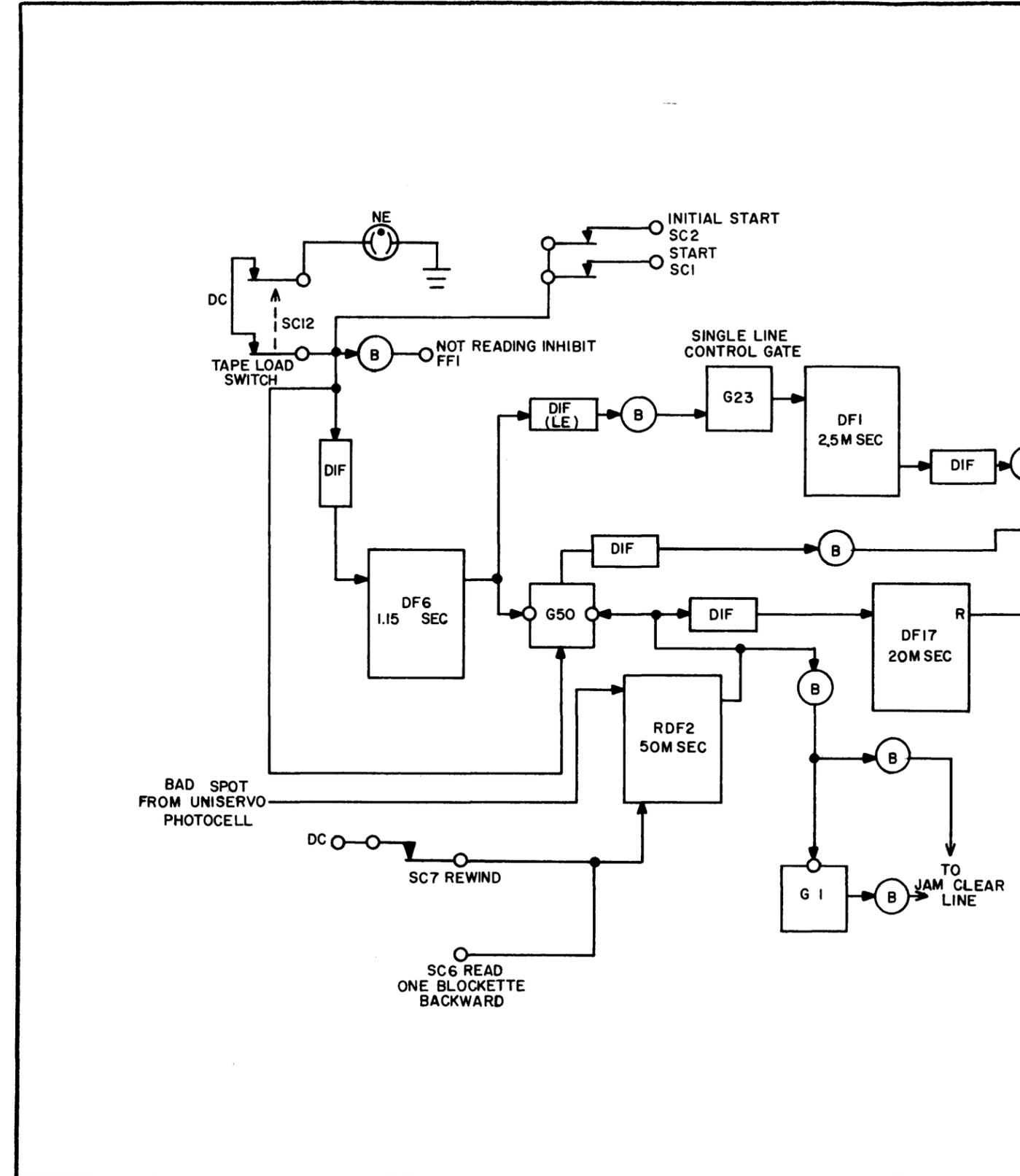
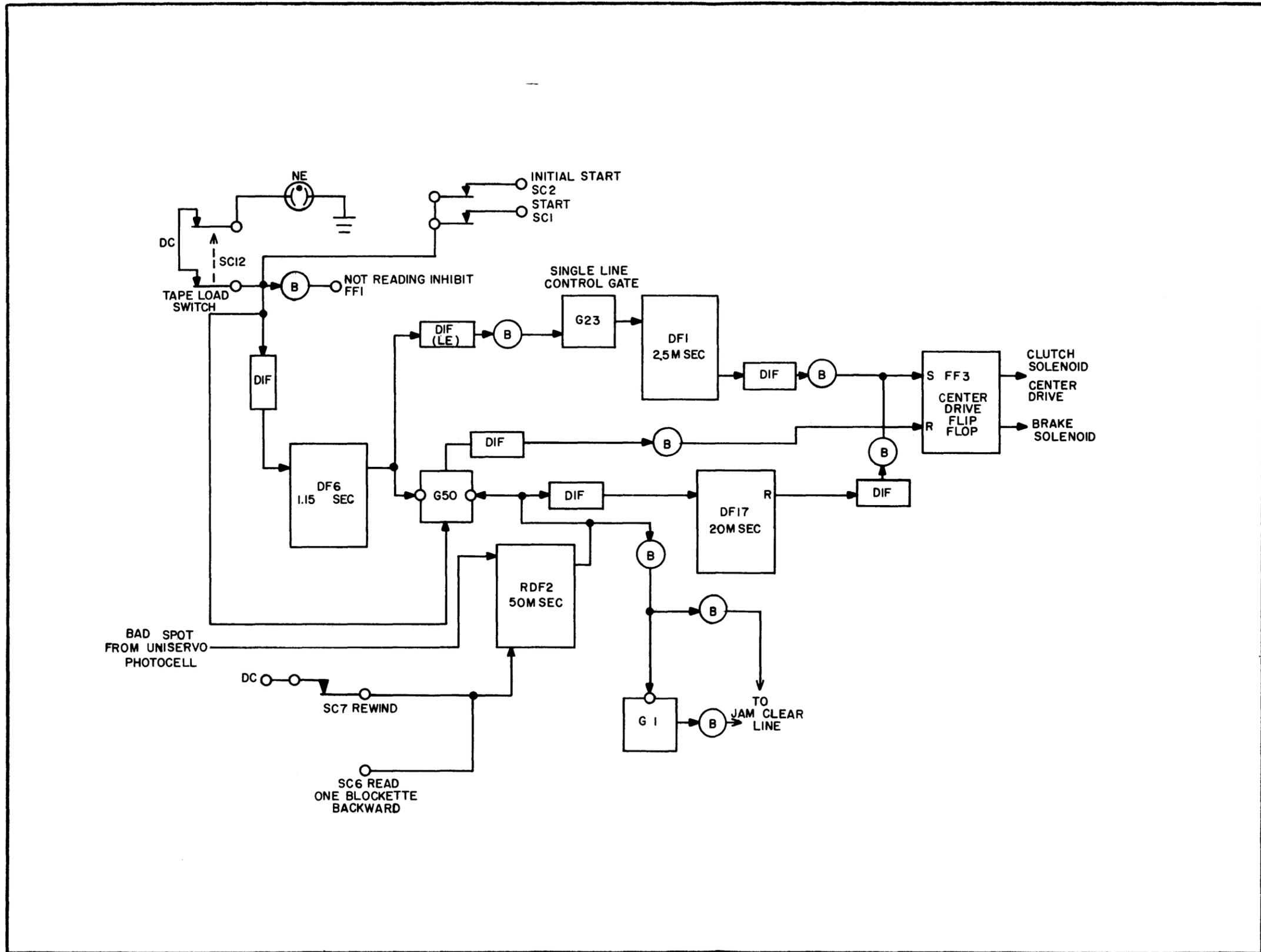


Figure 2-14. Tape Load Operation
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Essentially, operation of the Bad Spot Detector is as follows. Light, passing through a hole in the tape, strikes a photocell, thereby developing an output from this tube. This output triggers RDF2, a 50-millisecond re-triggerable delay flip-flop shown in Figure 2-14. As the faulty area of tape is punched every two and one-half inches as previously mentioned, and moves past the photocell assembly at 100 ips, an impulse will be received by the photocell every 25 milliseconds, subsequently re-triggering RDF2 every 25 milliseconds. This will occur for the entire duration of the passage of faulty tape. (Note: The total elapsed time in milliseconds that RDF2 will be triggered may be calculated by adding the quantity one to the number of holes punched in the faulty portion of tape, and multiplying the total figure by twenty-five (e.g., 13 holes + 1 = 14 x 25 = 350 msec). As RDF2 requires 50 msec to recover at any time, it will be seen that during a sequence of holes RDF2 will not recover until a delay of 50 msec following the transit of the last hole.

Referring again to Figure 2-14, during BAD SPOT operation, the triggered (or set) output of RDF2 is applied as an inhibition to G1 and as a "Jam-Clear" pulse to the Align Input flip-flops (also to G50, described later). This action effectively prevents any spurious pulses or noise from the faulty tape area from setting the Align Input flip-flops or from producing false Sprocket Pulses. Two signals which are applied on the same input line and that will prevent RDF2 from producing a set output are the "Rewind" signal SC7, and "Read (One-Blockette) Backward" signal SC6. The purpose of the signal from SC6 is to prevent areas of recorded tape from being missed on a "Read Backward" operation. For example, as shown in the drawing below, which is drawn for clarity rather than technical accuracy, when the tape is running forward, information is recorded to within two and one-half inches of the commencement of a Bad Spot. However, in this typical instance information has not been recorded on the tape prior to an elapsed movement of five inches of tape following the Bad Spot. If this should occur, RDF2 would recover (delay 50 msec) prior to the information following the Bad Spot passing under the reading head, which would not necessarily be adverse; however, on a Read-Backward operation, RDF2 would remain set for 25 msec after information appeared under the reading head. This would permit the Uniservo to ignore up to a maximum of two blockettes of information.

The purpose of the signal from SC7 is again to prevent RDF2 from becoming set, and consequently erroneously triggering the Input flip-flops. This would be caused otherwise by the translucent end-of-tape Mylar leader permitting a light-cell pulse to interfere with the normally-produced "end-of-rewind" signal to the tape control.

In the case of a Bad Spot being encountered during a Tape Load operation, the set output of RDF2 is also applied to G50 as a second inhibition, which insures that the tape will continue to move until the faulty portion has passed. Should the Bad Spot be sufficiently short that it has passed prior to the 1.15 sec recovery of DF6, no change in the Tape Load operation will occur. If the Bad Spot occurs immediately previous to the recovery of DF6, the length of the Bad Spot will be added to the amount of tape normally being advanced.

There is always the possibility that following a normal Tape Loading operation, a Bad Spot will appear under the detector just as the tape is being braked to a stop. In this event, the signal from the Bad Spot Detector will

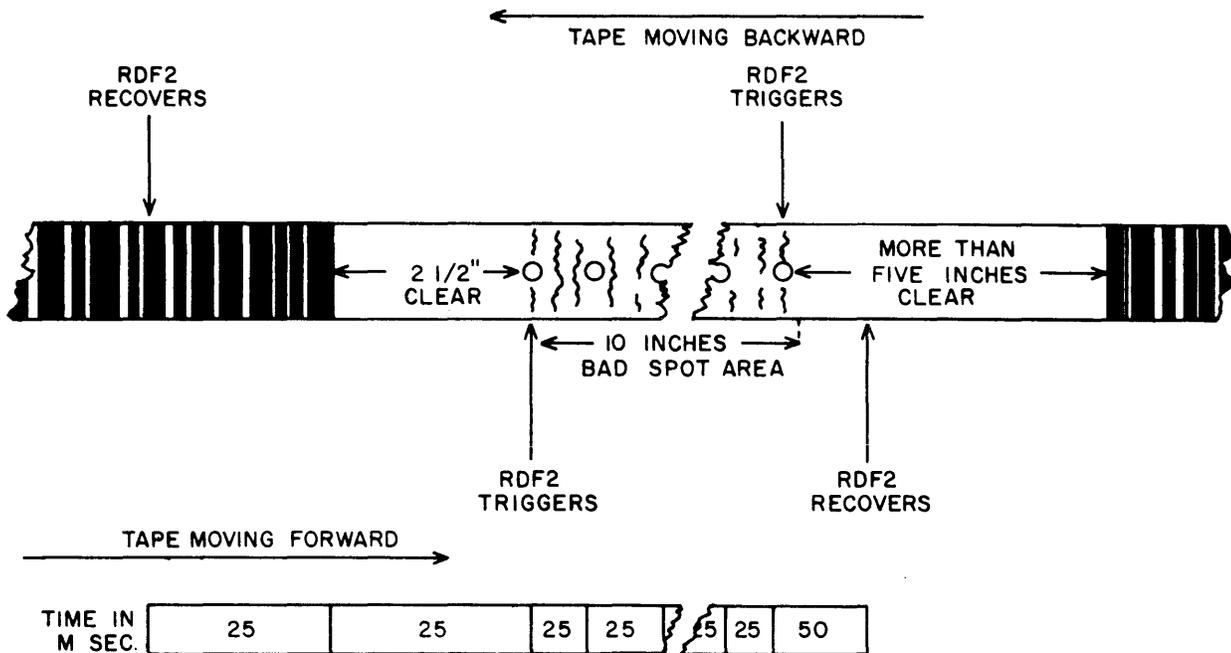


Figure 2-14a. Bad Spot Reading

set RDF2 in the usual manner, the output of RDF2 being applied as an inhibition to G50, and also as a differentiated pulse to DF17, a 20 msec delay flip-flop. The delay in this case is sufficient to permit the center drive circuits to have sufficient time to stabilize from previous tape movement, inasmuch as the restored output of DF17 after passing through a buffer, is applied as a set pulse to FF3. This, of course, places the center drive in motion again, as the clutch is engaged. The faulty portion of tape which has caused this action now moves on, past the Read Head.

A situation may also arise, in which the tape may stop with the perforation for a Bad Spot just beyond the photocell light, or in front of the light. In this case the tape should move another two and one-half inches to the next hole, which would normally require 25 msec. However, the tape, having stopped, may require up to 30 msec to reach the next hole, due to starting inertia. The delay

period of RDF2 (50 msec) minus the delay of DF17 (20 msec) permits a tape transport of 30 msec prior to recovery of RDF2. Once the tape has been placed in motion it will continue in that state until 50 msec following the last set pulse to RDF2. When RDF2 recovers, the inhibitive signal from G50 will be removed, which will permit the SC12 enable to G50 to pass through and restore the center drive.

Bad Spots located between blockettes of tape information must be in a position that will permit them to be detected at the commencement of a blockette. Should a Bad Spot be encountered after FF3 has recovered, following a normal Read operation, the restored output of DF17 will again set FF3, which causes a second blockette to be read in. This stops the Printer and registers a 120 CHECK indication, (as more than 120 characters have been read-in during the single Read operation). This type of error is further described under 5.b. of this Section.

In reviewing the preceding paragraphs, it will be noted that Bad Spot signals have an effect upon the Tape Control circuits only during a Tape Load operation. Should Bad Spot signals be encountered during normal reading operations, FF3 will be in a set condition, the restored output of DF17 having no effect.

b. INITIAL START. - In studying the Initial Start operation simplified logic drawing Figure 2-15, Initial Start and Read Operation, should be referred to during reading of the text. Overall logic drawing Figure A will also be of assistance in locating peripheral circuits which are mentioned.

The purpose of the Initial Start operation is to commence the operation of the machine and to create a Read-in Cycle and subsequent continuous running of the machine (barring faults). Before actuating the START switch the GENERAL CLEAR switch should have been operated, which insures that all error-checking circuits are reset and the Stop flip-flop circuit is in a restored state. Details as to operating procedure may be found in the Programmer's and Operator's Manual, and switch functions are detailed in Table 2.

The START switch is logically and schematically identified as SC2 and is of the momentary contact spring-return type. Certain signals are initiated when SC2 is actuated, some of these signals have been mentioned previously in describing other circuits. The signals are:

1. A Clear-to-Zero pulse to the Memory address counter.
2. A set pulse to DF7, Paper Stop Stabilizer Delay-Flop.
3. A Clear pulse to BC3, Computer Digit control counter.
4. An enabling pulse to G23, which in turn develops an output as a Clear Memory signal and a set pulse to DF1.

The set output of DF1 is differentiated and supplied as a reset pulse to FF10. The Clear Memory signal from G23 acts as a set pulse to DF12, the Clear Memory Timer. The output of DF12 in turn provides a De-ion signal to the Keyed B+ (sometimes referred to as Memory B+) as an enable. The Keyed B+ is a signal

which permits the plate voltage of the Memory tubes to be reduced to a point where they de-ionize. The Keyed B+ also provides a Not-Reading inhibition to the L-Section of the Minor Address. As the delay of DF12 is 5.5 msec, this will be the length of time during which the latter signal is provided. In addition, the output from the Keyed B+ passes to the Paper Feed control circuits.

When DF1 recovers 2.5 msec following the set pulse received from G23, the restored output is used as a Charge Capacitor (CC) signal via FF21 and G31, and also as a set pulse to FF3, center drive control flip-flop. The CC signal, channeled as mentioned, acts as final enable to the actuator power-supply, thus placing the charging current on the actuator capacitors.

c. READ CYCLE. - The Read Cycle commences with the setting of FF3, which starts the Tape Drive by engaging the clutch; this removes the enable from G17 and also the Not-Reading line. The time consumed from the setting of FF3 until the initial tape information appears is 5 msec between blockettes and 15 msec between blocks. Approximately 3 msec following the start of the center drive, DF12 recovers, which discontinues the Not-Reading signal at its output. This also removes the inhibition signals from the Memory channels. The inhibition from the L Section of the Minor Address is removed, thus selecting Line L_0 which together with Line M_0 , selects Address Line Zero and alerts Memory location One for a read-in. Simultaneously, the Not-Reading inhibition is removed from G1 and the Align Input flip-flops, which are prepared to receive the first character.

The SP pulses, in addition to being channeled to the tape-control circuits, are used as set pulses to RDF1, a 400 μ sec retriggerable delay-flop. This removes the enable from G16, the Read-in control gate, which was applied by RDF1.

As RDF1 receives a set pulse from SP every 80 μ sec, it remains set for the full duration of the read-in Cycle. A pulse from SP_2 samples G41 each time that a character is read-in. Following the read-in of 119 characters, DF9, which has been receiving SP_1 pulses, (and which requires 29.9 μ sec to recover), recovers for the 119th time and sets the Memory address counter to 119. This action then selects Address Line 119, and places an enable on Memory location 120 for read-in. The pulse on Address Line 119 is also sent to the tape control circuits and is used as a first enable on G41. The remaining and final enable for G41 is applied by the 120th SP_2 pulse produced by the 120th character read-in, with the output of G41 being applied as a set pulse to FF10. The subsequent set output of FF10 becomes a first enable to gates G15 and G16.

The retriggerable delay-flop RDF1 recovers 400 μ sec following the 120th SP pulse, and supplies a final enable, in so doing, to G16. The output of G16, differentiated, passes through a buffer stage and is applied to FF3, restoring the latter flip-flop. The restored output pulse acts as an enable on G17 as well as passing to the other circuits shown in Figure 2-15. Presuming that no errors have occurred during read-in, a Print Cycle will now occur.

The Print-Cycle will be described in detail in this Section under item 3.d. However, in order to complete the discussion of the Read-in Cycle, it will now be considered that a Print Cycle has ensued and has been completed. When this has occurred, FF12 is restored to its original state by the set

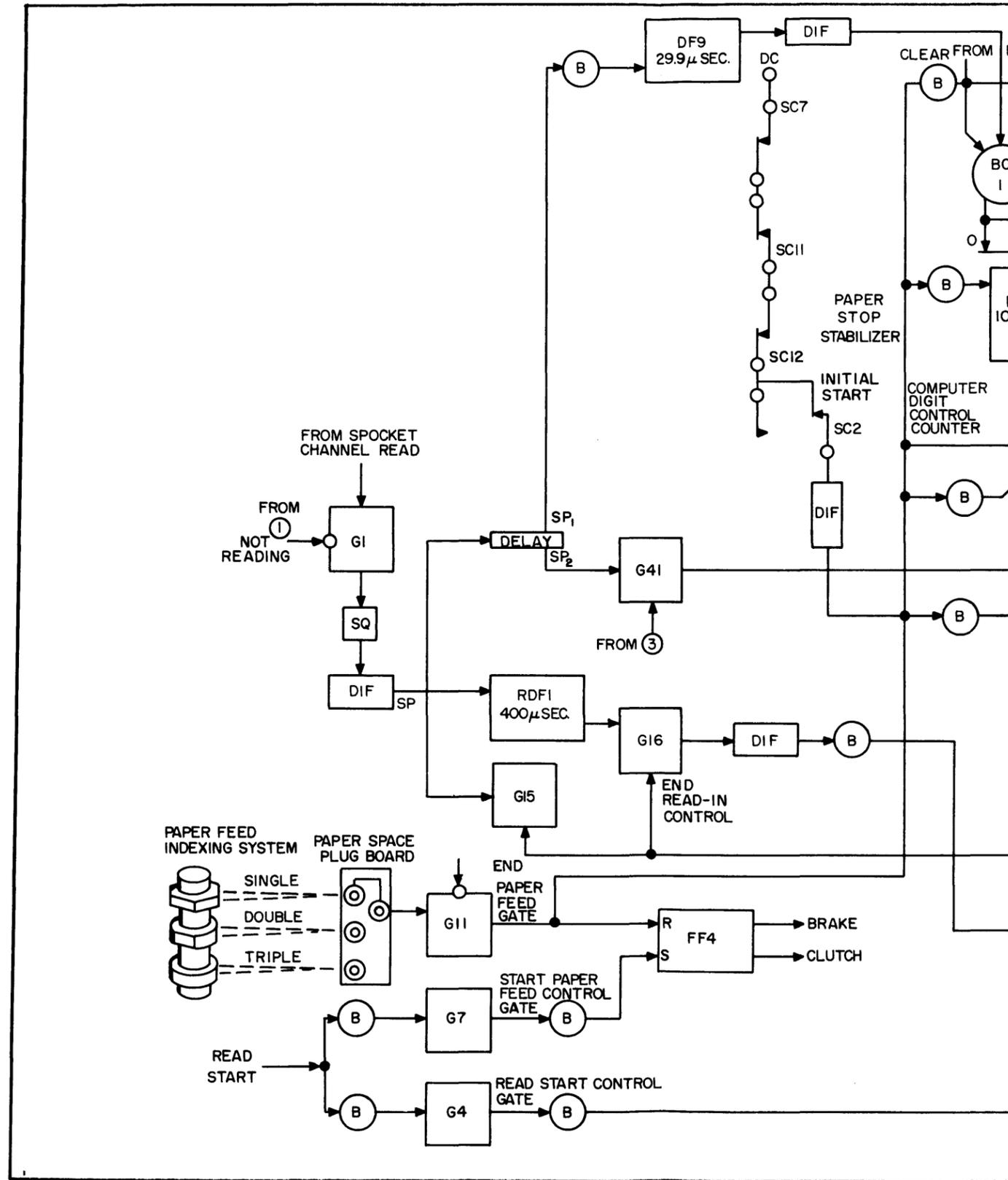
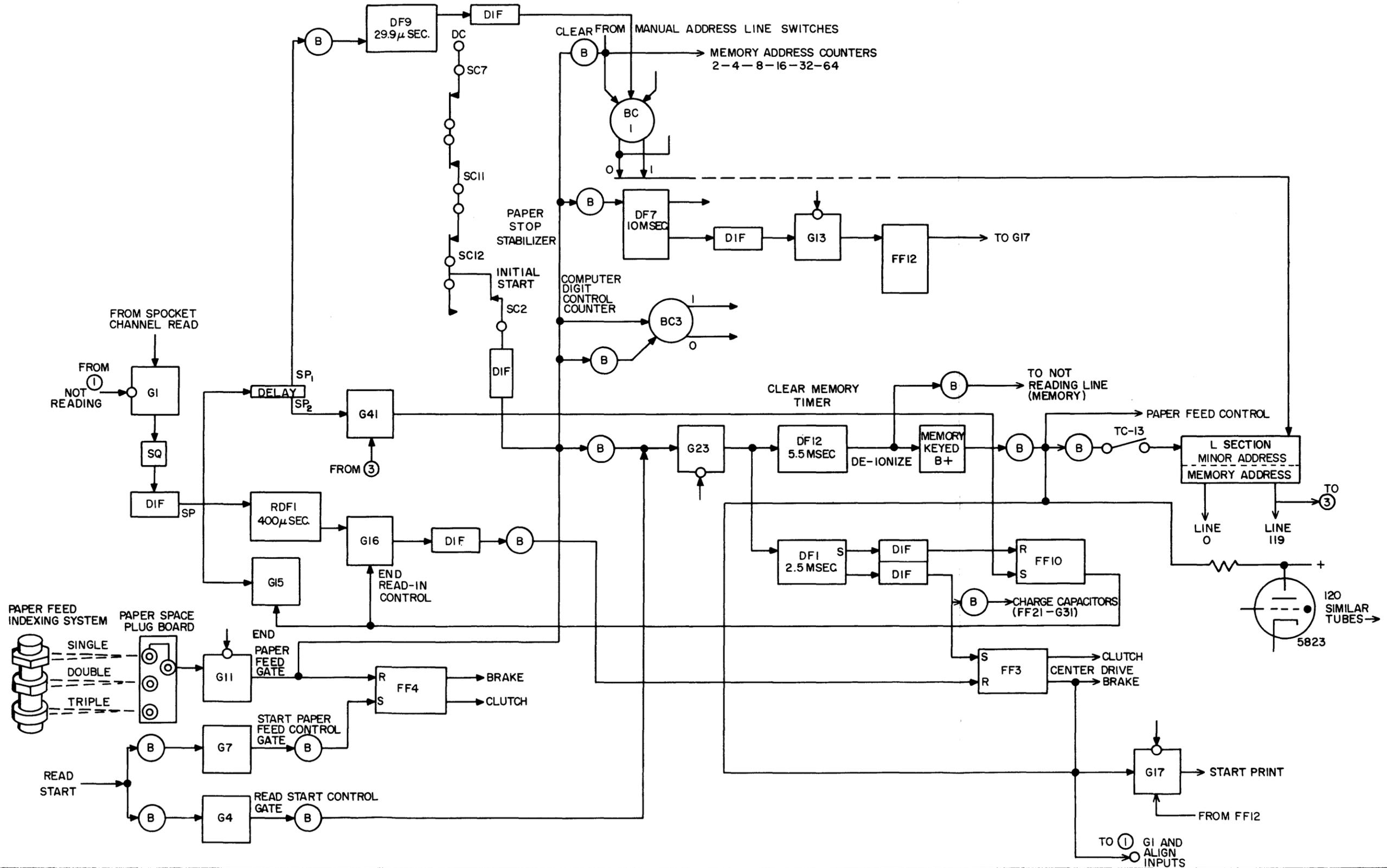


Figure 2-15. Initial Start and Read
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pulse "End Print", which will be discussed later. This removes one enable from G17. At this juncture, if no errors have occurred, a Read-Start signal is developed which is applied as an enable to G4, the Read-Start control gate, through a buffer stage. This signal is also applied to the Start Paper Feed control gate G7 and along the Clear Line of the Memory address counters. The output signal from G7 triggers FF4, the output of FF4 engaging the clutch for the Paper Feed drive assembly.

The output from G4 places an enable on the Single Line control gate G23, which in turn develops a Clear Memory pulse, and a set pulse to DF1. The first SP pulse sets RDF1 7.5 msec later, and 100 μ sec following this, an End Paper Feed (EPF) signal is produced by the Paper Feed indexing system (presuming that single line spacing is being used in this case).

The EPF signal samples G11 which it passes through (if not inhibited) and is applied as a reset pulse to FF4. The reset output of FF4 releases the Paper Feed clutch, and energizes the brake solenoid to stop the paper-feed action. The EPF signal additionally triggers BC3 to the "one" state and triggers DF7, the Paper Stop Stabilizer delay-flop.

RDF1 is set for the final time in the cycle 120 Sprocket Pulses later (or 9.6 msec). Following the delay period of RDF1, 400 μ sec, the recovery pulse produces an enable for G16, which stops the center drive by resetting FF3. DF7 recovers state 100 μ sec later, setting FF12, and G17 receives a final enable. Again, if no errors have occurred a Print Cycle commences.

The total elapsed time from "Read-Start" to the final enable on G17 is 17.6 msec. If double-spacing is selected, the time required for the completion of one Read Cycle is increased to 25.2 msec, and if triple-spacing is selected, 32.8 msec.

d. PRINT CYCLE. - As the Print Cycle circuitry is extensive, a simplified-logic diagram would duplicate or approach the complexity of Figure A. It is recommended therefore, that the latter drawing be referred to in reading the material that follows.

G17, the Start Print control gate, controlling the Start Print Cycle, is enabled by FF3 on a restored pulse. This insures that at no time will printing take place while the tape is in motion. Therefore, as long as the brake is actuated, G17 will be enabled, thus permitting a Print Cycle. G17 receives another enable from FF12, which insures that the paper has been "fed" and stabilized. It is possible for G17 to be inhibited by signals from Multiline Time Out (MTO) and the Prevent Print line. There are numerous sources which will produce an inhibitory pulse on the Prevent Print Line. These are as follows:

1. Paper Feed Error (PFE) restored output of RDF4
2. Print Error (PE) set output of FF13
3. Fast-Feed Error (FFE) set output of FF17
4. Greater-than-120 Error set output of FF9

5. Odd-Even (OE) Error set output of FF8
6. Address Error (AE) set output of FF19
7. Normal Stop set output of FF11

Certain of the above sources may be cancelled by intervening switches, if actuated.

FF11 in turn, may be set by the following sources:

1. HOME PAPER Switch SC1c. When this switch is actuated FF11 is locked in the set condition.
2. The output of gate G59. Should a Fast-Feed I symbol be encountered during a Manual Read operation, gate G59 is enabled thus setting FF11.
3. The Stop symbol being received from tape.
4. The output of gate G40. Should a Breakpoint symbol be encountered on the tape while the BREAKPOINT switch SC3 is closed, SC11 will receive a set signal.
5. The output of G58. Should a Manual Read operation be initiated, with no inhibiting signal being applied from the Read, No Print source, FF11 will receive a set signal, (SC9 Read, No Print normal).
6. The Feed Paper and Stop signal from G25, which is actuated by the generation of a Read Start signal with Single Line switch SC2 closed. The Feed Paper and Stop signal is also generated from SC26, Space Paper switch, which manually feeds paper.
7. The output of G18. The set output of DF8 with no inhibiting signal being placed on G18 from a Print Cycle, will set FF11.

DF8, a .3 sec delay-flop may be set by the following signals:

1. An Out-of-Ribbon signal actuated by the Out-of-Ribbon microswitch.
2. An Out-of-Tape signal, (simultaneously the d-c is removed from the Uniservo).
3. Manual Stop switch SC4.
4. The Out-of-Paper contactor when the carriage is "in". This signal will be channeled by way of gate G62 if the Printer is operating Fast-Feed, but will otherwise pass through SC30 (Control Loop).

Gate G18 is always inhibited during a Print Cycle, and therefore will prevent FF11 from receiving any of the preceding four signals during this Cycle. If this occurred the Printer would stop during a Print cycle.

All Error signals (excepting Charge Error) will alert the Prevent Print line. In this event, the machine will come to a stop upon completion of the following Read Cycle. With the exception of a Charge Error or Print Error, the Memory will contain a new blockette of information. If there is a Charge Error or Print Error the Memory will contain the information currently printed, and these two errors will initiate a Space Paper action.

With none of the foregoing possibilities presenting an inhibiting signal to G17, upon arrival of the final enable to G17 a Start Print Cycle ensues. This cycle follows several paths; one, as an inhibition to gate G18 as mentioned in the second paragraph above, and two, as an alerting signal to the All-Out Detector (through a buffer stage); three, the signal is differentiated to produce a Start Print Cycle Leading Edge (LE) signal; and four, a Start Print Cycle Trailing Edge signal.

The Start Print Cycle LE is channeled to the following sections:

1. G24, as a final enable during a Read, No Print operation.
2. DF3, as a set signal.
3. FF21, as a set signal.

The setting of FF21 places an inhibition on G31, at the same time as an enable is placed on G60. The charging voltage thereby is reduced from G63 for this period, following the setting of FF21.

When DF3, the Probe Memory Timer, develops a 300 microsecond Probe Memory signal which is channeled by way of G47 to the Comparator, the leading edge of the Probe Memory signal is differentiated and develops a set pulse to DF4 (Probe Check Thyatron Timer), and DF21 (Charge Line Stabilizer Delay-Flop).

The six millisecond output of DF21 passes as an inhibition to G63, which permits the charge line to reduce to zero potential in the time required. If the charge line has not reduced to zero within the six-millisecond period, or increased above zero during the remainder of the Print cycle, a Charge Error will develop.

The 300 microsecond Probe Memory signal to the Comparator samples all Memory locations to determine if information is being stored. In the event that any Memory location has one or more conducting tubes, a first enable will be placed on the associated Comparator. The Probe Memory signal will then act as a second and final enable to the Comparator.

The resultant output from the Comparator will pass by way of plugboard connections to the Print location, and will be applied as an enable or signal increase to the control grid of the Print and Check thyratron tubes. It should be noted that only those Memory locations which are storing information by virtue of having one or more conducting tubes, will have a first enable. Therefore, only the Print locations that are connected to a Memory location storing information will have a Probe Memory signal on the respective grid.

DF4 recovers 250 microseconds following the setting of DF3. The consequent restored output is differentiated and applied as a sampling pulse to the screen grids of all Check thyratron tubes. The Check thyratrons that have an enable on the control grid will now fire. It may be seen, therefore, that any Memory location storing information will have a conducting Check thyratron in an associated Print location. The Probe Check Thyratron pulse will also act as a set pulse to DF9, the restored output of which will set the Memory counter to a count of 121.

A delay will occur within the Comparators, and the set period of DF4 will compensate for this delay. Inasmuch as there is a capacitive-loading effect on the Comparator, the control-grid voltage increase required on the Print location thyratrons may require as much as 250 microseconds. When the Check thyratron ignites, the cathode potential of the Check thyratron will increase -- this increase being directly coupled to the screen grid of the associated Print tube as a partial enable.

The restored output of DF3 is differentiated, and acts as an enable on G57. The output of G57 passes as a set signal to FF20. The set output of FF20 develops an enable for G63, G5 and G21. When gates G5 and G21 are enabled, the output of the Code Generator is channeled to the Comparator and the Actuator circuits.

e. READ, NO PRINT. - It is frequently desirable to edit information contained on the tape without the necessity of printing the material. In order to retain all of the checking features of the Printer while performing such an operation, recirculation must be accomplished through gate G17. The retention of error checking is necessary in order that error detection may stop the Printer. In discussing the action of Read, No Print operation let it be assumed that the tape is to be read for checking purposes until the symbol for Breakpoint (β) is encountered. The machine has been "General Cleared" and the tape is loaded. To initiate the function, the BREAKPOINT switch on the control panel is closed. With the closing of the BREAKPOINT switch (SC3), a first enable is placed upon G40, the Breakpoint gate. Refer to Figure 2-16, Read, No Print Operation in the following discussion.

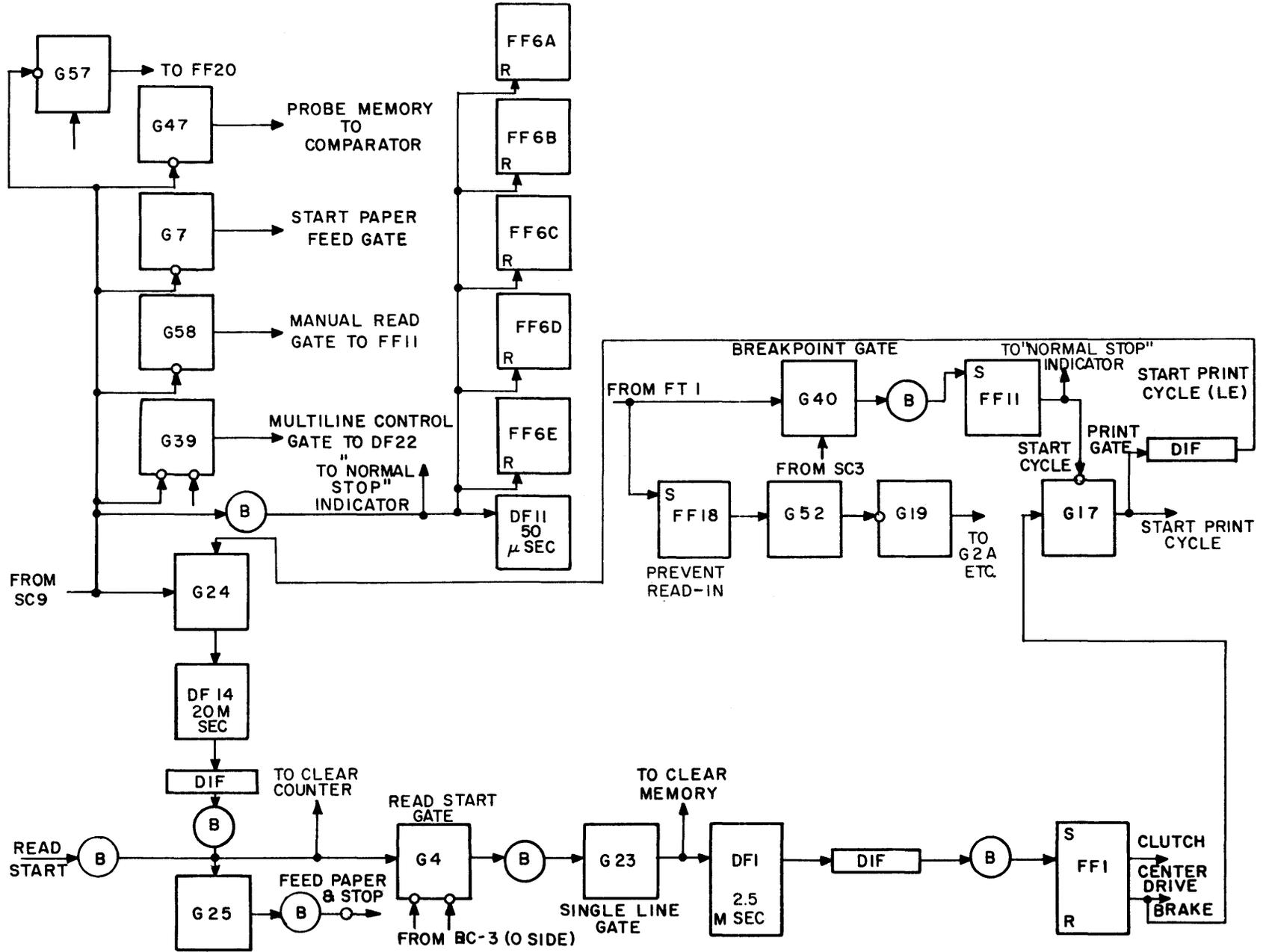
With the closing of the READ, NO PRINT switch SC9, the following signals are initiated:

1. An enable to G24, which provides a recirculation path for Start signals.
2. An inhibition to G39, the Multiline control gate. This insures that no Multiline signals are observed throughout the operation.
3. An inhibition to G7. This will prevent any paper from moving through the machine during the operation.
4. An inhibition to G58. This prevents the Manual Read switches from developing a set pulse to FF11.
5. An inhibition to gate G47. This inhibition insures that no Probe Memory operations occur during the Read, No Print operation.
6. An inhibition to G57 which determines that a Start Print signal does not develop during the operation.
7. A jam-restored signal (continuous signal level) is channeled to certain portions of the Fast-Feed circuitry, namely, FF6A, FF6B, FF6C, FF6E and DF11, thus insuring non-operation of the circuits during the Read, No Print operation.

From the foregoing it will be noted that during the Read, No Print operation, the circuits involving the Print operation are quite effectively prevented from operating, and the Paper Feed and Multiline circuits are also non-operative.

The next manual operation performed by the operator, that of closing the INITIAL switch SC2, initiates the read-in to Memory of a blockette of information. While the read-in is in progress, the Memory fills, and all error-checking circuits connected with this operation perform their functions. At the completion of the Read-in Cycle, FF2 recovers, and thereby supplies an enable to G17. The Leading Edge of the Start Print Cycle pulse from G17 is differentiated and transferred to G24, and as G24 is now fully enabled as a result of this pulse, develops a set pulse for DF14, a 20 msec delay flip-flop.

Figure 2-16. Read, No Print



The delay period of DF14 permits the center drive circuits to stabilize between set pulses to FF3. The Print circuits having been jammed, the other output from G17 has no effect at this moment.

The restored output of DF14 is differentiated to the Clear Address Line binary counters, and passes through a buffer stage to the Read Start line, Read Start gate G4, Single Line gate G23, and to the Memory line, clearing the Memory.

The latter pulse also passes to DF1, which it sets, and drive subsequently commences. In this manner another blockette of information is read-in, with this type of recirculation continuing until the blockette which contains the Breakpoint symbol is in the process of being read-in.

When this occurs, the Breakpoint symbol is decoded in Function Table One and develops a set pulse to FF18, the set output of which passes G52 and thence to G19 as an inhibition, preventing the symbol from being read into Memory. This pulse from Function Table One also samples G40, the output which then occurs setting FF11 by way of a buffer stage. The set output of FF11 passes by way of a buffer to the Prevent Print line, which places an inhibition signal on G17 and ignites the NORMAL STOP neon light on the Supervisory Control panel. As G17 is thus inhibited, the following recovery pulse of FF3 does not pass G17 to produce a Start Print Cycle Leading Edge. The Printer unit therefore stops, with the blockette which has contained the Breakpoint symbol in the Memory. (Note that the symbol itself has not entered Memory).

It will be observed that the Read, No Print operation cannot be integrated with a Computer Digit operation due to the inhibition of G4 from BC3, the Computer Digit Control counter, the inhibition occurring during Computer Digit operation. Should this be attempted, the recirculation path will thus be broken and the Printer will stop.

f. PRINT, NO READ. - Whereas a Read, No Print operation is used for editing and sometimes testing the operation of the Printer, the Print, No Read operation is used exclusively for test purposes. With this type of operation, information stored in Memory is printed-out -- continuously repeating the print-out -- until such time as a normal Stop is performed, or an error develops. No information is read into Memory once the Print, No Read operation is initiated. It is therefore necessary that the operation be preceded by, or commenced with, a Memory Fill or Read operation.

To commence Print, No Read, the operator depresses the GENERAL CLEAR switch and raises the PRINT, NO READ switch. The latter switch, SC8, places an inhibition on G4 (see Fig. 2-17 Print, No Read Operation). The operator then raises the INITIAL/CONT/SINGLE LINE (Initial Start SC2) switch, which causes a Read Cycle. (The switch being non-locking, will normally return to the CONT(inuous) position when released).

Following the completion of the Read Cycle, the restored output of FF3 initiates a Print Cycle by placing a final enable on G17. The Read Start signal, which is developed at the end of the Print Cycle, follows the Read Start line, and passes through G7 to FF4, which causes paper to feed when set. However, with G4 inhibited, the Read Cycle does not occur. Therefore, following completion of paper feed operation delay flip-flop DF7 is set,

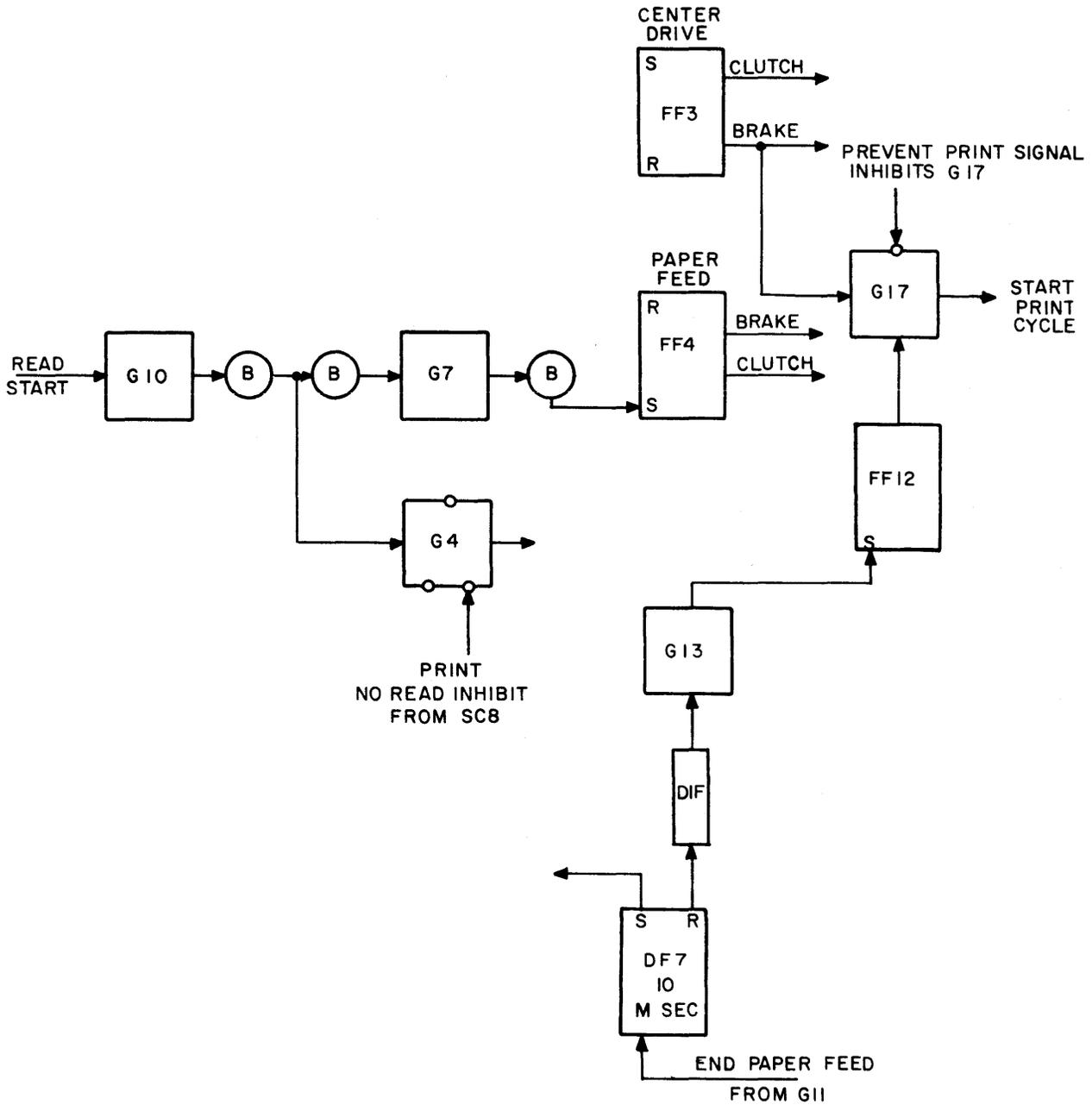


Figure 2-17. Print, No Read
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with the restored output consequently setting FF12, and thus providing a final enable to G17, again with a Print Cycle occurring. This orbit continues until a Normal Stop signal is developed or an Error signal is encountered, which will inhibit G17.

Computer Digit operation may be accomplished in conjunction with the Print, No Read operation. Computer Digit operation is discussed under 4.c of this Section.

g. SINGLE LINE. - Single Line or Normal Line printing is, as the name implies, an operation that permits one blockette of information to be printed on one line at a time, without a Read Cycle occurring. The usual purpose of this operation is to print the contents of Memory following a Normal Stop. It is also used for fault determination. Refer to Fig. 2-18, Single Line Operation, in following the explanation of this operation.

Commencing the sequence of operation with the machine stopped and the NORMAL STOP neon lamp illuminated, which indicates that FF11 is in the set state, the operator depresses the SINGLE LINE switch. This action results in an inhibition being placed on gate G23, the Single Line control gate. With this inhibition on G23, further signals in the direction of the center drive flip-flop FF3 are prevented from passing, and in addition, the Clear Memory line does not receive a signal. SINGLE LINE switch SC2 also places an enable upon G25.

The operator then raises the START/STOP switch, SC1, thus applying a reset pulse to FF11 by way of a differentiating circuit. The restored pulse of FF11 removes the inhibition from G17 (placed there, as mentioned, by the Normal Stop signal), and a Print Cycle occurs. Following the completion of the Print Cycle, a Read Start signal is developed, passing through G10 and reaching the Read Start line through a buffer stage. This signal clears the Memory counter and also passes through G7, which permits a Start Paper Feed signal. The signal from G10 also passes G23, developing a Feed Paper And Stop signal, which, after being reshaped in a buffer stage, is applied to the set side of FF11. It will be observed that the Read Start signal also passes G4, but is unable to pass through G23 due to the Single Line inhibition which is present on G23. Therefore, following paper feeding, the Printer comes to a stop.

Note that the information in Memory has not been cleared following this operation, and that the same sequence will again occur each time the START/STOP switch is set to START.

h. READ FORWARD, READ BACKWARD (MANUAL READ). - The necessary physical operations required in order to commence a Read Forward or a Read Backward operation are given in detail in Table 2. The operation in this mode permits the read-in to Memory of one blockette of information, following which the Printer will stop immediately prior to a Print Cycle. The information may be read-in either forward or backward, depending upon the actuation of the READ FORWARD/READ BACKWARD switch. The latter switch, although an integral mechanical assembly, is designated SC5 (forward) and SC6 (backward), the center position being neutral and non-designated.

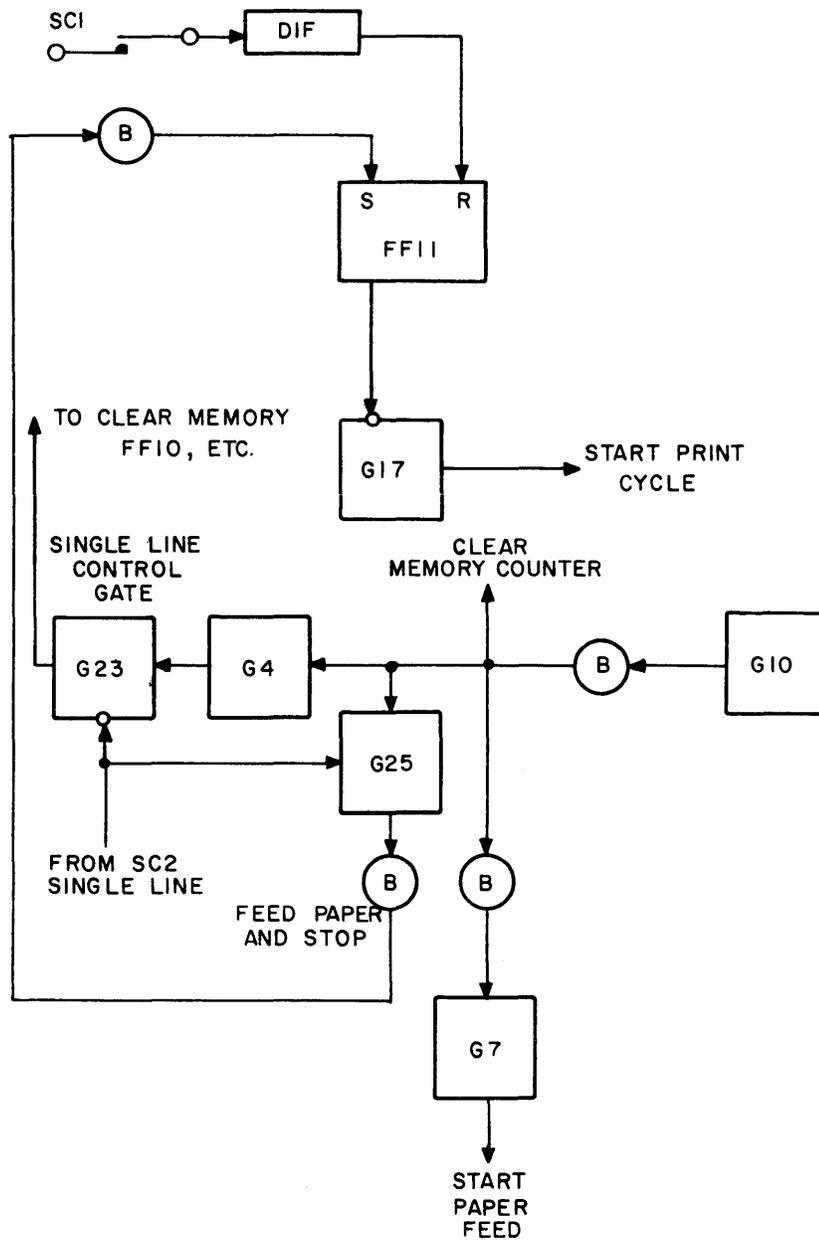


Figure 2-18. Single Line
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When placed in operation as either SC5 or SC6, (henceforth to be referred to separately), these switches may integrate various other functions of the machine while performing the reading operation. These functions have been detailed in Table 2. For instance, following the "Manual Read," as the R-F/R-B operation is frequently known, it is normally desirable to initiate a Print Cycle in order to determine what has been read from the tape. This is accomplished by raising the START switch, resulting in the information being printed and the machine stopping. Customarily, the RF/RB operation is used for editing and fault-finding purposes. Refer to Fig. 2-19, Read Forward/Backward Operation, in reading the following.

It may be assumed, for purposes of discussion, that the Printer has been prepared for an initial operation -- tape loaded, Tape Load operation performed, and the paper in position for receiving the first line of print. It may be assumed also, that a determination is to be made as to whether or not the blockette of information desired is the one ready to pass the Read Head. The operator raises the switch READ FORWARD, SC5, which develops the following signals:

1. A voltage-level holding signal (jamming) to the Fast-Feed circuits which prevents Flip-Flops 6A through 6E from setting.
2. An enable to G58, which, passing through a buffer stage, sets FF11.
3. An enable to G59, the Fast-Feed I editing gate (see 4.d).
4. A differentiated set pulse to DF5, an 800 msec delay flip-flop which, by delaying the Start Center Drive signal, permits the tape loops on the high-speed tape transport to stabilize when the operation is changed from either Read Forward, to Read Backward, or the opposite. The restored output of DF5, in order to accomplish the preceding action, after passing through a buffer stage passes along the Manual Read Start (MRS) line to G23, developing a Clear Memory and Start Center Drive pulse.

The MRS signal is channeled to the following circuits:

1. By way of a buffer stage to the Memory address binary counter, which it clears.
2. As a set pulse to DF7.
3. As a reset pulse to Error flip-flops FF8, FF9 and FF19.
4. A clear pulse to BC3.

When the foregoing has occurred, a normal Read Cycle occurs; the Memory filling with the information contained on the first blockette of tape. Following the completion of the Read Cycle, the Printer stops due to FF11 being set.

The operator now closes the SINGLE LINE switch by depressing it (SC2), and lowers switch SC5, READ FORWARD, to the middle position, thereby opening that circuit. The START switch is now operated, resulting in a single Print Cycle, followed by a normal Paper Space and the stopping of the machine.

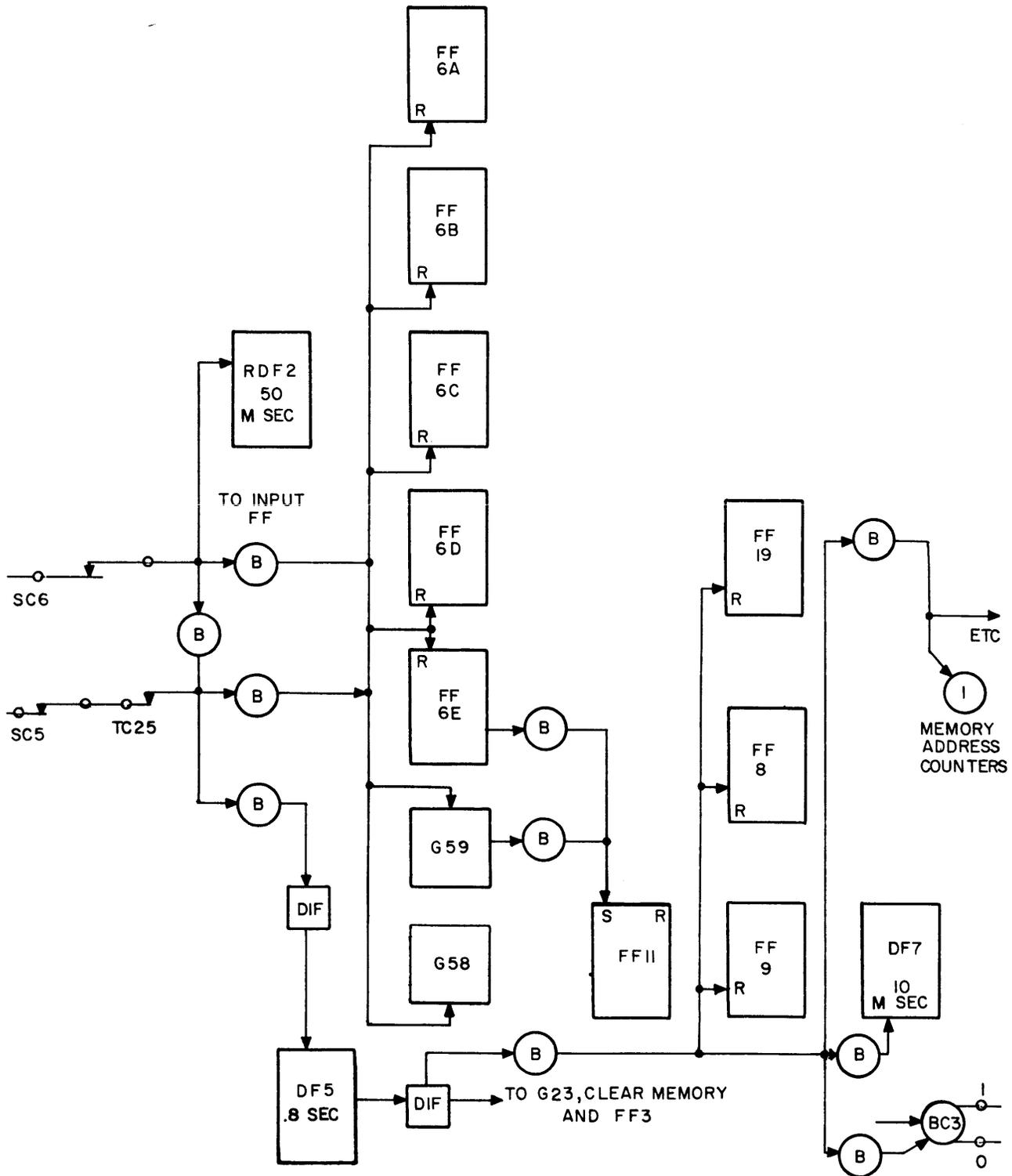


Figure 2-19. Read Forward/ Backward
PX 616

Read-One-Blockette-Forward has now been accomplished, and in order to read the information thus printed-out, the carriage is moved out to observe the line printed.

Read-One-Blockette-Backward is essentially similar in operation, switch SC6 being the actuating medium. However, in this case the information is read backward into Memory, with Bad Spots not being observed due to the voltage level applied to RDF2 as a jamming signal from SC6. Opening SC6 on a read-backward operation will cause the center drive to stop prior to the ending of the Read Cycle.

i. REWIND. - Raising the REWIND Switch key SC7 causes the Uniservo to rewind to the beginning of the tape. Manual operational details are given in Table 2. Figure 2-20 (Rewind Operation) indicates the circuits involved in the following description.

Upon actuating SC7, the following signals are developed:

1. A jamming signal to RDF2. This prevents Bad Spot signals from being accepted during Rewind.
2. An inhibiting signal to the Tape Signal Input circuits. This prevents noise signals or information from entering the input channels while the tape is in motion.
3. A set pulse to FF11 by way of the buffer stage. FF11 presents an inhibit to G17 and a signal to the Prevent Print line, thus preventing printing from occurring while the Rewind operation is in progress.

The Rewind signal is removed either by a Stop Rewind signal from the end of the tape, which is detected on the Uniservo (see Uniservo Handbook), or a Rewind Trailing Edge signal, which occurs as the Rewind switch is opened by returning it to center position. These signals restore FF3, releasing the center drive clutch, and actuating the brake.

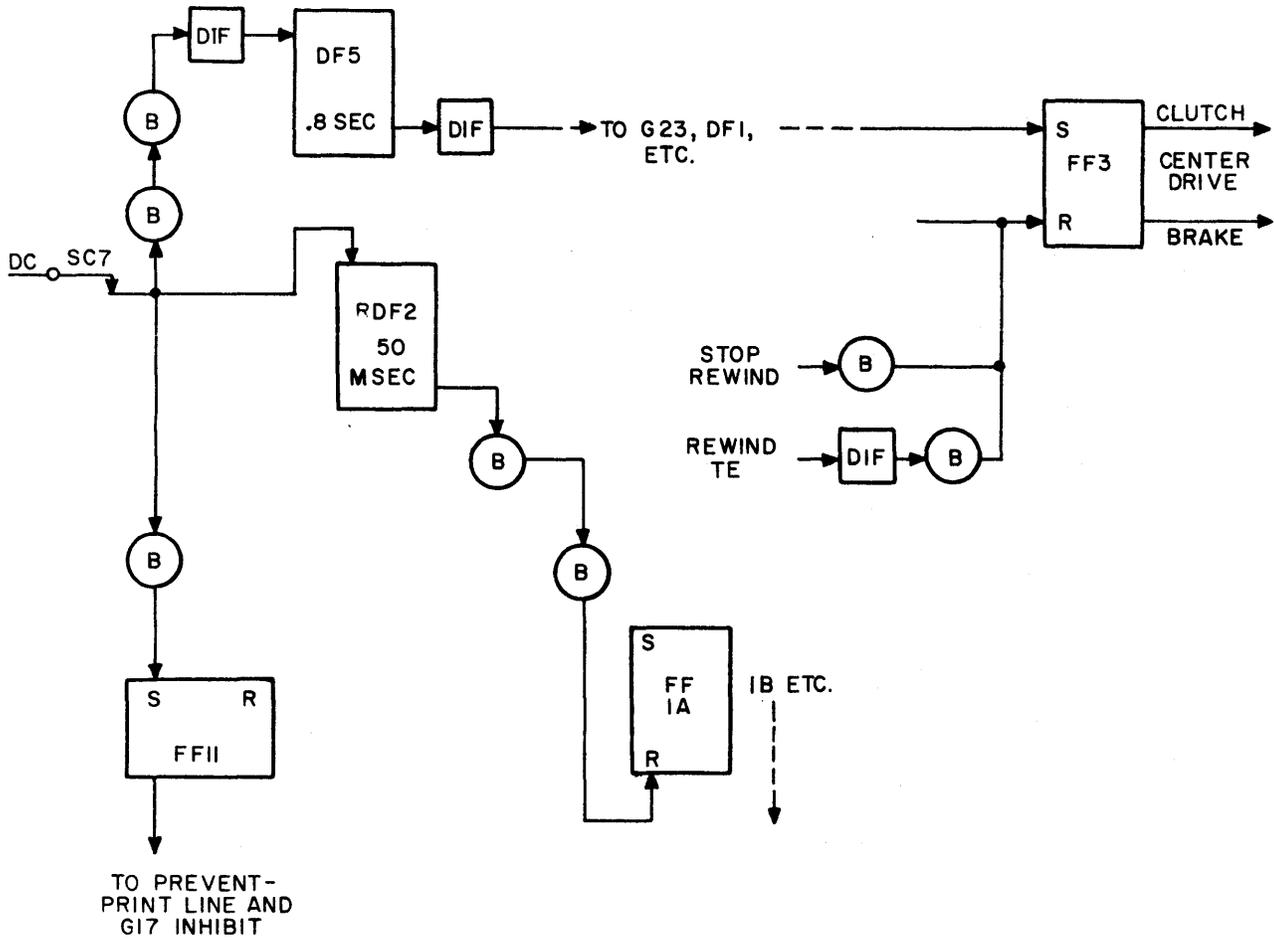


Figure 2-20. Rewind
PX 616

4. SPECIAL EQUIPMENT FUNCTIONS

In this portion of this Manual; for optimum clarity logical operation of the High-Speed Printer is explained largely by means of typical examples. Where a fault is given it does not necessarily follow that this type of fault is either common or normal to the equipment, but has been selected as possibly being the most suitable for explanation of the typical example presented.

a. ZERO SUPPRESSION. - The circuits of the Zero-Suppress portion of the Printer are used whenever it is required that zeros be suppressed to the left of the most significant digit in a numerical portion of a blockette. This action has been briefly described in Section 1, and the manual operations required are given in considerable detail in the "Programmer's and Operator's Manual for the High-Speed Printer," pages 26 and 27.

In order that a blockette recorded on tape be recognized by the Printer as such, the blockette must contain 120 characters. Should this not be so, the machine will stop; this fault being described under Error Detection Circuits. Therefore, it may be seen that each character position must be occupied by a symbol of some description. However, inserting ignores for the spaces, although not a particularly large problem for the Central Computer in the case of alphabetic characters, is a time-consuming and wasteful process in the case of numerics. This is due to the fact that blank areas between numerics are filled with zeros in the Central Computer, and it would normally be necessary to replace the non-significant zeros with ignores. Fortunately, by plugboard control (see Operator's Manual), non-significant zeros may be eliminated within the High-Speed Printer using the Zero Suppression circuits shown in Figure 2-21, Zero Suppression Function. The search for non-significant zeros is conducted in areas or zones (termed "fields") until the first non-zero digit arrives, or until the end of the field is reached, the field selected being accomplished through the use of a plugboard.

The information contained in one blockette may be sub-divided into a maximum of eighteen different fields, each one containing information desired for printing, or to control. For instance, pay check information could consist of separate fields for the Name, Clock Number, Gross Pay, Net Pay, etc. The number of characters occupying any one field will be determined by the maximum number of significant characters to occupy that field in any one blockette. For example, in the Name field, should the longest name to be encountered in a payroll contain seventeen characters, the Name field will at all times require seventeen characters (printed or suppressed), as:

(longest name) J.iN.iBORRMANISKI (17 characters)
(shortest name) iiiiiiiiiJ.iL.iWU (17 characters)

In the preceding example, the "i" symbols are for the ignore instruction, and would normally appear in the place of non-significant characters when the Name field is alphabetic, and hence not requiring arithmetical processing in the Central Computer.

In the case of figures appearing in a field, the situation is changed, as has been mentioned. When this occurs, the numerical quantities are processed by the arithmetical circuits of the Computer and the non-significant areas of

the tape are filled with zeros. For example, if the largest amount encountered was 115.87 and the smallest amount 0.52, the latter amount would appear on the tape as 000.52. As the first two zeros are non-significant, they must be deleted from read-in and subsequent printing. Assuming that the figures 115.87 occupy from the 23rd to the 28th character positions in a blockette, the non-significant zeros appearing in positions 23 and 24 (for the example given, 000.52) are therefore the zeros to be eliminated, in this instance.

There is always the possibility that a zero may occupy (again using the above character positions), the 24th character position as a significant digit -- for example, 105.32. In this case, the zero in this figure group is read-in and printed, inasmuch as a zero field, even though plugged, will cease upon the arrival of a significant figure. This is true, even in the event that the character arrives in the same position as the position for which plugboard connections have been made for the field to commence.

The control of the zero fields is determined by the zero suppression section of Plugboard II. This plugboard will consist of the following: One 120-jack (also known as "hubs") board with connections to the 120 Memory address lines. Two eighteen-jack boards one for START control and one for STOP control. The thirty-six hubs connect by way of thirty-six buffer stages to two boards each containing eighteen sets of jacks. The latter two boards also have jacks for Start and End Single Line, and jacks for START and END Multiline operations.

As shown in Figure 2-21 Zero Suppression Function, the output of the zero field plugboard START Single Line jack connects directly to gate G44, the Start Single Line Zero Suppress gate; with the output of the End Single Line jack being connected to G48, the End Single Line Zero Suppress gate. As the operation of the zero-suppress circuit is the same for either Single Line or Multiline, with the exception that different fields may be selected for each without interference to one another (discussed in a later paragraph), the present description will be limited to Single Line operation.

Using the example already mentioned, to suppress the non-significant zeros in character positions 23 and 24 will require that the plugboard be connected as shown in the drawing Figure 2-22, Plugboard Suppressing Zeros in Character Positions 23 and 24. This drawing shows Jack 23 of the Memory address lines being connected to Jack 1 of the eighteen-jack START Zero Suppression plugboard. Jack 1 is connected by way of a buffer to the two Jack 1 units on the eighteen-pair START Zero Fields board. This arrangement will require that the Programmer connect between the remaining open Jack 1 and the Start Single Line (START SL). This now completes a connection from Memory address line 22, (character position 23 - note carefully the following explanation) to G44 as a possible enable. The address lines are numbered 0 to 119, whereas the plugboard jacks are numbered from 1 to 120. It will therefore be seen that the number of the plugboard will always be one number greater than the number of the address line to which it connects. Address line 22 will be selected in this instance, during the read-in of the 23rd character.

Plugboard wiring is continued, in the present example, by plugging from the Memory address line jack 24 to jack 1 on the eighteen-jack End Zero Fields board. Jack 1 is already connected internally by way of a buffer to the

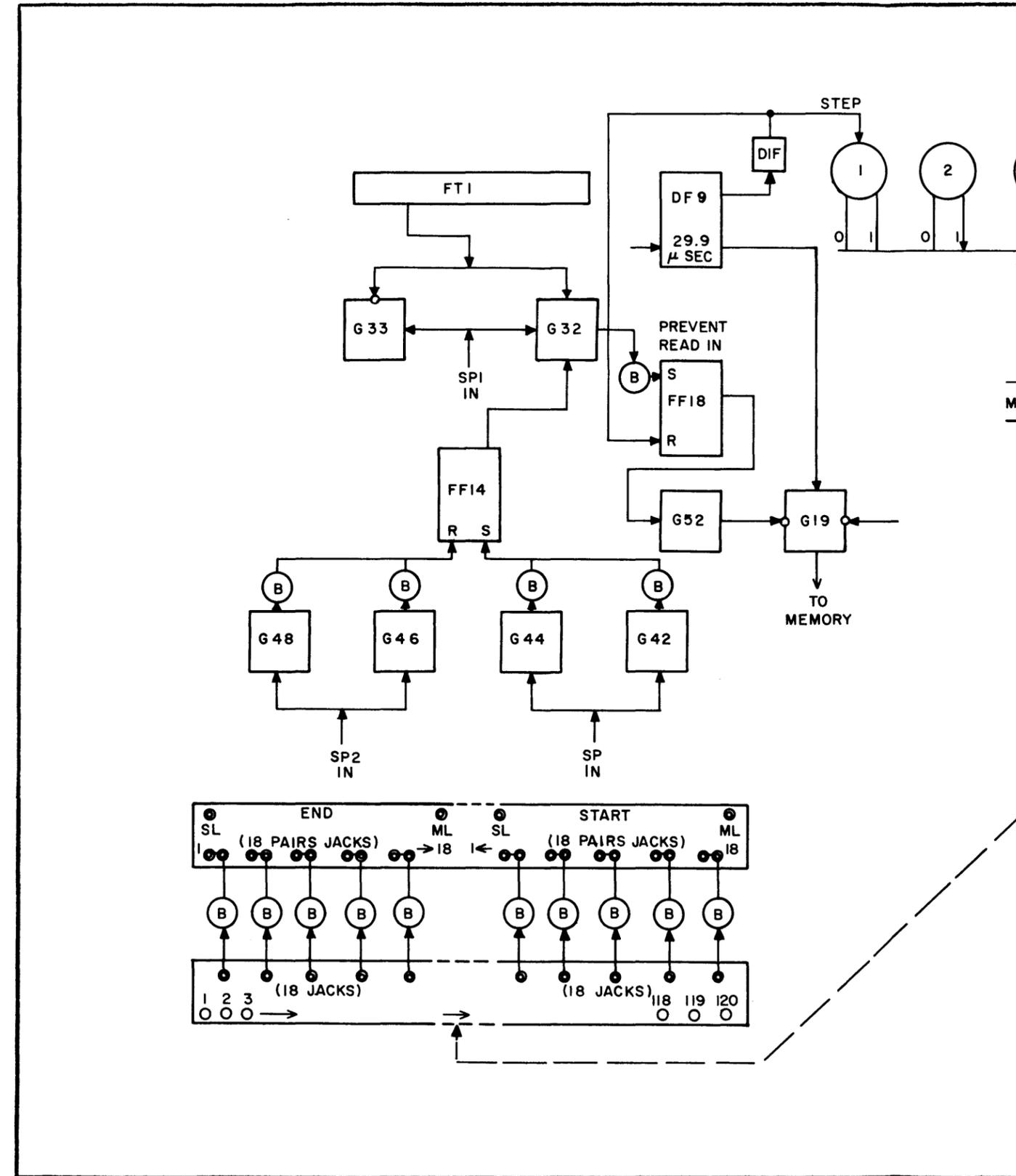
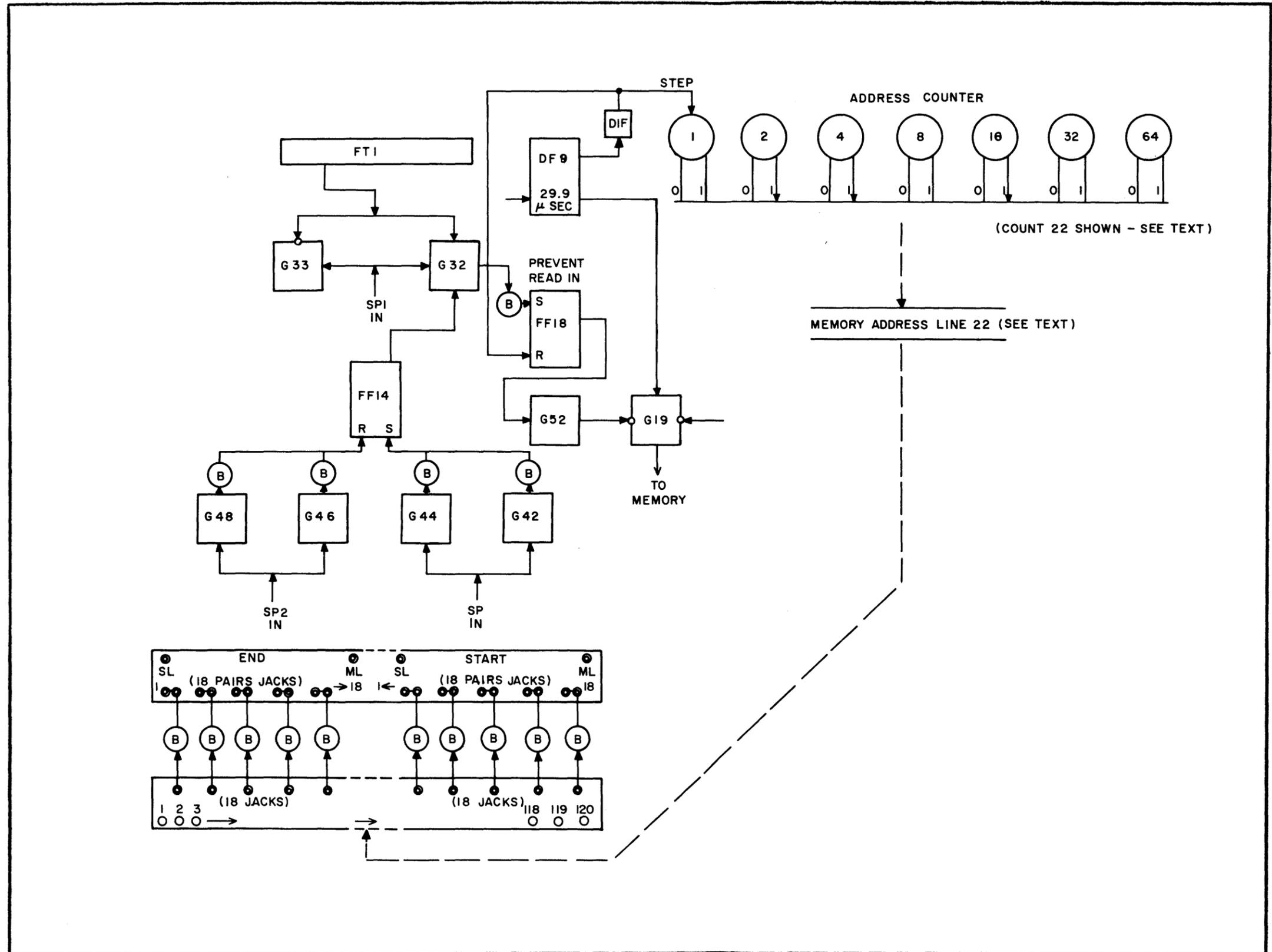


Figure 2-21. Zero Suppression Function
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ression Function

eighteen-pair jack 1 unit. The unused Jack 1 is connected using a jumper to the End Single Line (END SL) jack. Address line 23 has thus been connected to gate G48 (End Zero Field) as a possible enable.

Continuing the use of the previously-stated example, the blockette which contains the amount 000.52 in character positions 23 to 28 inclusive is read-in. Delay flip-flop DF9, acting upon the recovery pulse from the 22nd character, steps the Memory address counter to a count of 22, which selects address line 22. This proceeds as a first enable to gate G44 by way of the plugboard connections previously arranged. The 23rd character now follows into the Align Input flip-flops, and, at the time of the Sprocket Pulse (SP), is transferred to the Input flip-flops.

The SP for this 23rd character samples G44, which is enabled thus permitting the SP to pass through and develop a set pulse for FF14, the Zero Field flip-flop. The set output of FF14 is supplied as an enable to G32 simultaneously with the arrival of the zero enable from Function Table One. In addition, the output of the Zero Decoding gate in FF1 is supplied as an inhibition to G33. When the SP₁ for the 23rd character samples G32, the latter, which is fully enabled, passes the pulse as a set pulse to FF18 the Prevent Read-in flip-flop, by way of a buffer stage. G19, the Prevent Read-in gate, now being inhibited will thus prevent the zero which occupies the 23rd character position, from entering the Memory.

Delay-flop DF9 now recovers for the 23rd time, which resets FF18 and steps the Memory address counter to 23. In a similar manner as the 22nd count, address line 23 is now selected, and again via the pre-arranged plugboard, G48 in this instance receives a first enable.

The 24th character, which is also a zero, is now read-in to the Align flip-flops, and is transferred to the Input flip-flops, the output selecting the Zero Decoding gate in FT1. The zero output of FT1 now places a second enable on G32 as in the previous instance, and an inhibition on G33. As before, an SP₁ pulse is generated, this time for the 24th character, which samples G32 and passes through, developing a set pulse for FF18, again producing a Prevent Read-in inhibit to G19 via G52. The zero in character position 24 is thereupon also prevented from entering Memory.

The SP₂ pulse for the 24th character when it occurs, samples gate G48, which has previously received an enable, and accordingly passes through as a reset pulse to FF14. This ends the zero field selected in the example given.

When the read-in of the zero in character position 25 occurs, gate G32 will not have a first enable, FF14 having been restored as mentioned above. In this event the SP₁ pulse will not pass through G32 and develop a set pulse for FF18. This zero (the third in the group 000.52) will therefore not be suppressed, but will pass into Memory to appear in due course, as a printed character.

It may be noted from the foregoing that the length of a zero field is determined by the set period of FF14. Additionally, a zero which occupies the character position chosen to commence, or end a zero field will be suppressed,

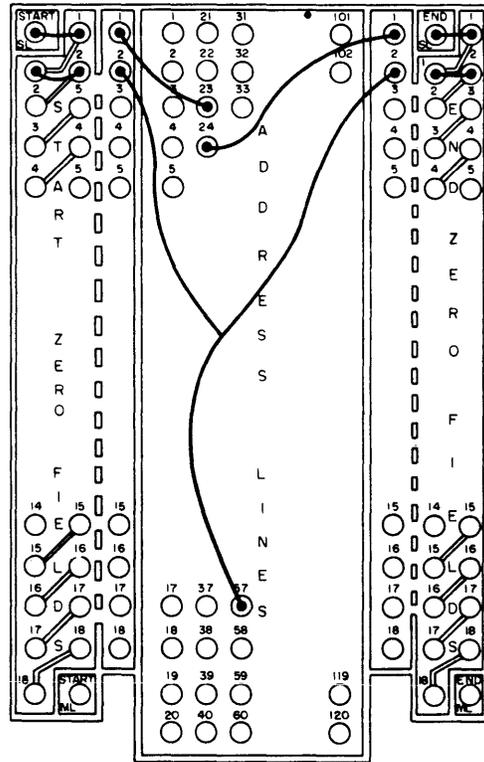


Figure 2-22. Plugboard Suppressing Zeros in Character Positions 23 and 24

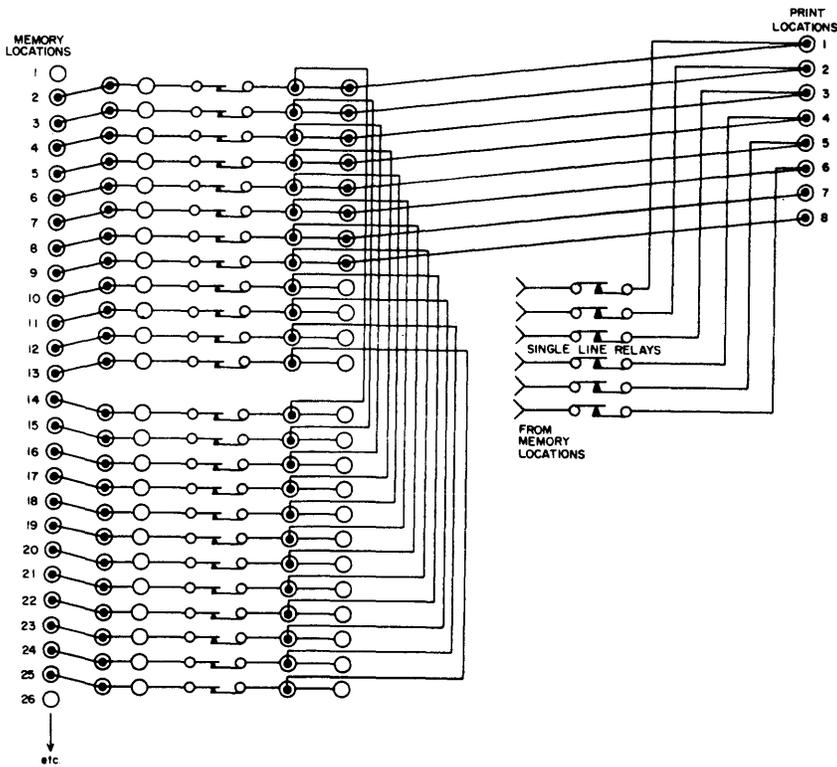


Figure 2-23. Multiline Relay Connections for Text Example PX 616

as well as any non-significant zeros occurring within that field. However, the arrival of any significant character within a zero field will end the zero field.

Gate G33 is sampled by each SP₁; accordingly any character read-in which is not a zero, will result in a reset pulse being developed for FF14, as explained in a preceding paragraph above. In this manner zeros, and only zeros, are suppressed by the zero-suppression circuits.

Determination of zero significance is made only by plugboard connections manually provided by operating personnel. Certain variable features may be accomplished by operating and programming personnel in the suppression of zeros. The techniques employed are fully explained in the Operator's Handbook. Inasmuch as a field may contain any number of character positions, the zero-suppression circuits may be arranged by plugboard to suppress from one to one hundred and twenty zeros. When it is necessary to suppress a single zero in a group containing zeros, the START, and END-Zero Field jacks are connected to the same address line jack using a Y connector. In this case, the zero field will commence and end on the same address line, suppressing the single zero.

When Multiline operation is in progress, the Multiline signal occurring simultaneously with the Multiline symbol (r) from the Multiline Decoding gate in FT1, switches the zero-suppression control from gates G44 and G48 to gates G42 and G46 (see next subject - Multiline). This will permit, if required, different fields to be suppressed during the read-in of a Multiline blockette. By placing the Multiline symbol in the last character position of a blockette, a Multiline blockette may be read-in using Single Line suppression control. In this way, transfer of control from the Single Line gates (G44 and G48) will not occur until the last character has been read-in. This facilitates the entire blockette being read-in, using Single Line Control.

b. MULTILINE. - Another Printer function which is accomplished through plugboard control is Multiline operation. This method of printing permits a blockette of information to be subdivided and printed on two, to a maximum of six lines. When Multiline operation is initiated with the symbol "r", the plugboard connections which normally control the Single Line output format are disconnected by the release of the Single Line relays, breaking the circuit. When this occurs, the information from Memory passes to the print locations by way of the Multiline relay contacts.

A typical example of a portion of a blockette read-in for Single Line would be:

J.iT.iREMRANDi16iWALNUTiST.iiiiPORTLANDiiiORE.iiii

(Note the insertion of the "ignore" symbol) which would appear on the printer as:

J. T. REMRAND 16 WALNUT ST. PORTLAND ORE.

If the above blockette had been influenced by Multiline symbols for three-line presentation, the printed copy would appear as:

J. T. REMRAND
16 WALNUT ST.
PORTLAND ORE.

In the above example, using Multiline, three Print Cycles would occur, but with each Print Cycle a different group of Multiline relays connect the Memory locations to the Print locations. The relay-selection change occurs between Print Cycles, simultaneously with paper movements. A new Read Cycle is initiated following the completion of the final Print Cycle; the third in this particular example.

The Multiline ring counter is the unit which controls the number of lines printed during the Multiline process. This counter is capable of counting up to a maximum of six only, with the number of counts being determined by manual plugboard control. Initially, this counter is in the zero state and the first Multiline pulse will step it to a count of one, with successive pulses increasing this count to the required plugboard amount before it is stepped back to zero, which in turn produces an End-of-Multiline signal.

When the ML ring counter is in the zero state the eleven twelve-pole Single Line relays are energized, with the first stage of the counter receiving a first enable. This occurs in a normal manner, and does not require plugboard connections to accomplish the enable. When the ring counter is stepped to "1", the Single Line relays are de-energized and the Multiline relays, which are connected by plugboard to the first stage of the counter, are energized. A first enable is simultaneously placed on the second stage of the counter, also by way of plugboard connections. At this point a Print Cycle occurs, which is followed by a Read Start Cycle. The Read Start signal moves the paper, and also produces a second Step-Multiline signal. This signal steps the ring counter to the second stage, releasing the first stage and energizing the second stage relays previously determined by plugboard connections. Again an enable is produced, this time to the third stage of the ring counter. This type of progress continues until an enable is placed on the zero stage (again by pre-determined plugboard connections, using the HOME jack). As the counter resets to the zero state, the Single Line relays are again energized, and an End-of-Multiline signal is also produced by the counter. The End-of-Multiline signal places the Multiline control circuits in a quiescent state, and also develops a Start Center Drive signal, commencing the read-in of another blockette from the tape.

The following is a typical example of a Multiline printing operation, with the circuits and units involved being normal except where the requirements of the example necessitate specific selection of components. Figure 2-24, Multiline Operation, indicates the component blocks used in Multiline in general, and in the example given.

The operator of the machine has, in this example, connected the plugboard sections so that:

ring counter 1 connects to ML relay coil 1

ring counter 2 connects to ML relay coils 2 and 3

ring counter 3 connects to ML relay coil 4

ring counter 4 connects to ML relay coil 5;

the plugboards used for this purpose being ML COUNTER and the "1-1" to "15-15" (otherwise unmarked) board.

The ML relay coils will, if actuated, close the contacts of correspondingly-numbered relays. These relay contacts have been selected to connect the Memory locations by way of the FROM COMPARATOR and TO ML RELAYS boards.

Relay 1 contacts connect to Memory locations 2 to 13 inclusive

Relay 2 contacts connect to Memory location 14 to 25 inclusive

Relay 3 contacts connect to Memory location 26 to 29 inclusive

Relay 4 contacts connect to Memory location 30 to 40 inclusive

Relay 5 contacts connect to Memory location 41 to 52 inclusive

The contacts of the Multiline relays used in the example are connected in parallel with the corresponding contacts of each other; that is, contact 1 of relay 1 is connected to contact 1 of relays 2, 4, and 5, (see Figure 2-23, "Multiline Relay Connections for Text Example"). The "ones" contacts are then connected by plugboard cords to print position 1, "twos" contacts of the relays to print position 2, etc. The contacts of Relay 3 are connected to Print positions 13 to 15 inclusive. The TO THYRATRONs and FROM ML RELAYS board portions are used in this plugboard operation.

The operator at this point would normally clear the machine by actuating the GENERAL CLEAR switch, continuing by raising the INITIAL/CONT/SINGLE LINE to INITIAL for an Initial Start. This then, in the example, will cause the following information to be read-in from the tape, which, it will be observed, has the ML symbol "r" in the first character position (pulse code 0 01 0000):

```
rJOHNiL.iDOEiMANAGINGiEDITORiDAILYiBUGLEiANYTOWNiUSAi
```

The ML symbol is decoded in FT1 and passes a set pulse to FF18 and an enabling signal to the ML Control Gate G39. The latter gate applies the subsequent output as a set pulse to DF22, the ML Time Out (MTO) delay-flop of 20 msec duration. The set output of DF22 is applied as an inhibition to gate G17, which prevents a Print Cycle for a period of 20 msec. Additionally, the output of DF22 is differentiated, passing through a buffer stage to produce a Step Multiline pulse to the ring counter; and a set signal for FF15, the Multiline-in-Process flip-flop. The set output of FF15 develops the ML-in-Process signal, which places an inhibit on gate G4, an enable on G35 and, as mentioned under sub-section 4.a. "Zero Suppression", transfers control on the Zero Suppression gates from G44 and G48 to G42 and G46. This is accomplished due to the ML-in-Process signal being applied as an enable to both G42 and G46, and as an inhibit to G44 and G48. The Step Multiline signal to the ring counter steps the counter to "1". When this occurs, ML relay 1 is actuated and the SL relays release -- the actuating voltage being removed from the SL relay solenoids.

Following the completion of the Read Cycle, the Center drive flip-flop FF3 recovers, with the restored output signal acting as a second enable on G17. Note, however, that G17 is at this time inhibited by the MTO signal from DF22 -- the 20 msec delay period permitting sufficient time for the mechanical operation of the relays, prior to the commencement of a Print Cycle.

During this particular Print Cycle the following information will print:

JOHN L. DOE

Following the completion of the Print Cycle, a Read Start signal is produced from G10, which, after passing through a buffer, enters the Read Start line. This signal is channeled to three destinations: By way of a buffer stage to G7 (which develops a Start Paper Feed signal), to the Clear line of the Memory address counter, and to G35 as an enable.

The signal from the output side of G35 develops a set pulse to DF23, the Recirculation Delay flip-flop. The set output of DF23 provides a 20 msec MTO signal which enters the inhibit line of G17, and a Step ML signal to the ring counter.

The signal to the ring counter steps it to the second stage, which, in the example given, actuates ML relays 2 and 3, releasing the first stage of the counter and placing an enable on the third stage. As G4 is inhibited by the set output of FF15, no Read Cycle occurs during this phase.

As DF7 recovers, following the set condition produced by the End Paper Feed signal, the recovery pulse sets FF12 via G13, the set output of FF12 producing a second enable for gate G17. As G17 is not inhibited at this time a second Print Cycle occurs, with the following being printed:

MANAGING EDITOR

This sequence of events continues as: Read Start - Paper Feed - Step Counter to 3 - Print: DAILY BUGLE

Read Start - Paper Feed - Step Counter to 4 - Print: ANYTOWN USA

Read Start - Paper Feed - Step Counter to 0.

When the ring counter is stepped to 0, it produces an End-of-Multiline signal which appears at G61, the Hold Multiline Control Gate, as an enable. The output of G61 produces a reset pulse to FF15, which terminates the Multiline operation. The restored output of G61 produces a Start Center Drive signal for G23, and this commences the read-in of a second blockette of information.

It will be apparent that the first character of this blockette will be read-in considerably in advance of the recovery of DF22. If a recirculation delay-flop (DF23) were not introduced at this point, an ML symbol in this blockette (or any blockette under similar circumstances), would pass and be ignored.

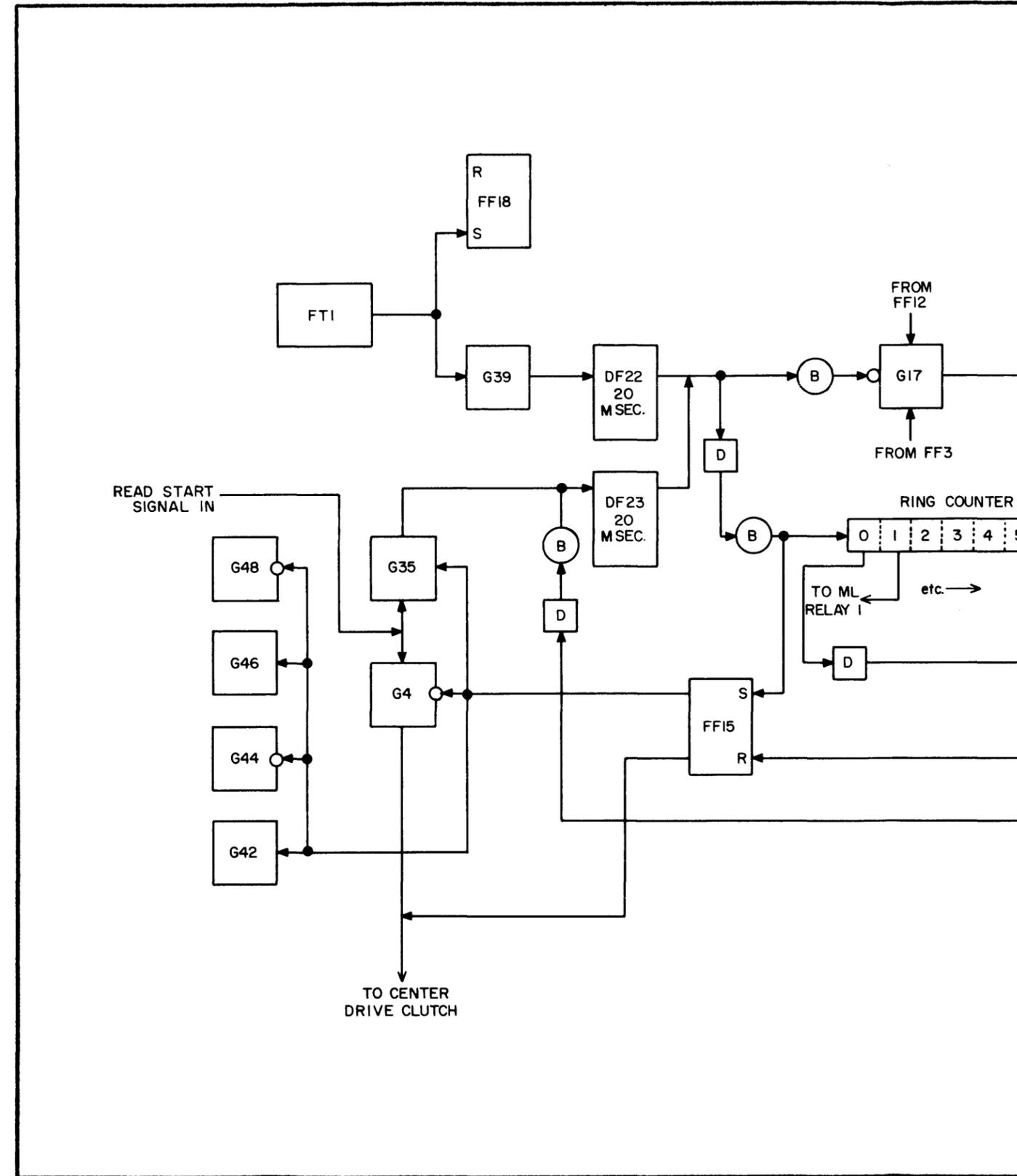
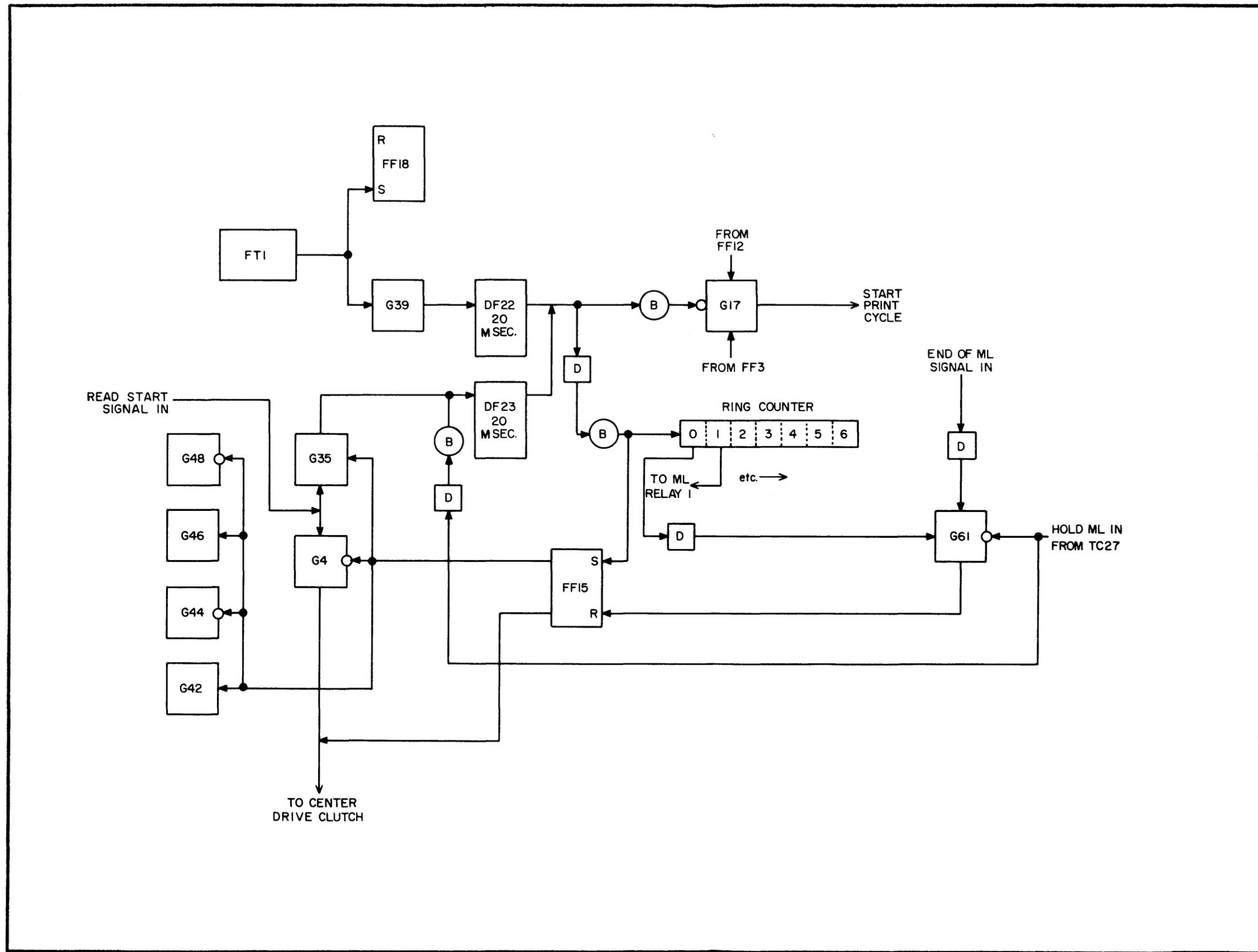


Figure 2-24. Multiline
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In order to amplify this explanation, consider an ML symbol occupying the first character position in the second blockette of information. DF22 will be set and the set pulse output differentiated and passed through a buffer to FF15, this pulse also being a step pulse to the ring counter. Due to the 20 msec delay of DF23 this delay-flop will not have recovered at this time.

If no ML symbol were encountered under the foregoing circumstances, or at any time prior to the recovery of DF23, the information read-in would be printed by way of the Single Line relay contacts.

The HOLD MULTILINE switch TC27, which is located on the Maintenance Panel, is used for testing and maintenance purposes. Should this type of operation be required the operator will cause the Memory to fill normally with the information that is required for printing. The HOLD MULTILINE switch is then operated, the impulse from this circuit inhibiting G61 and developing a set pulse to DF23. The output from DF23 subsequently is differentiated and passes through a buffer to step the ring counter to a count of "1", simultaneously with setting of FF15. With the actuating of TC27, the indicating lamp for MULTILINE is ignited on the Supervisory Control Panel.

It will now be necessary for the operator to actuate the START switch, as closing TC27 does not perform this function. A Print Cycle follows for the information in Memory.

Again referring to the example previously used, the information is printed out, first in Multiline then followed by a Single Line format, as:

JOHN L. DOE

MANAGING EDITOR

DAILY BUGLE

ANYTOWN USA

JOHN L. DOE MANAGING EDITOR DAILY BUGLE ANYTOWN USA

With this format sequence continuing indefinitely until the START/STOP switch is returned to STOP, or the HOLD MULTILINE switch is opened.

In the Hold Multiline operation the inhibiting of G61 prevents an End-of-Multiline signal from passing G61 and thereby resetting FF15. Inasmuch as the End of Multiline signal is developed by resetting the ring counter to zero, the SL relays will be actuated upon recovery of DF23 from the preceding Read Start signal. This line then will be printed by way of the Single Line relay contacts, following a normal ML print-out. Following the Print Cycle, the Read Start signal developed will set DF23, the output stepping the ring counter to the "1" state, and an ML cycle occurs. As the ring counter will step back to the zero state each time a fifth step occurs, a Print Cycle will occur by way of the SL relays. Note that the sequence of fifth step recurrence pertains only to the example given, with the plugboard connected for this example.

c. COMPUTER DIGIT. - For purposes of editing, fault location, and error information it is occasionally required that a normally non-printable symbol be printed, together with the printable characters in a blockette of information. Normally, non-printable symbols will not be stored in Memory, but in order to print these characters this storage action must occur.

In Computer Digit operation, which is controlled basically by the COMPUTER DIGIT switch on the Supervisory Control Panel, the read-in to Memory of normally non-printable characters is accomplished. The entry code of such symbols is modified in a manner that makes them recognizable as special symbols upon printing, the print-control circuits again changing them from special symbols, such as Δ , to 6.

If this printed information were all to occur on one line, the figure 6 as above, could be interpreted as being a "legitimate" 6 in the course of some group of figures or letter-figure combination. In order for such characters to be recognized as special symbols, the printing of the Memory contents under Computer Digit operation requires two individual Print Cycles. The first Cycle prints the normal line as it would appear under non-Computer Digit operation. The second Cycle prints the special symbols stored in Memory, printing these symbols in correct relative position to the preceding line. It may accordingly be seen that a complete Computer Digit cycle of operation will require one Read, and two Print Cycles.

All error-checking circuits function during Computer Digit operation, which materially assists fault location while using this mode of operation. Note however, that the check for print errors (PRINT CHECK) does not occur until the completion of printing of the second line.

All Check tubes connected to Memory locations are fired during the Probe Memory operation for the first Print Cycle, no Probe Memory operation occurring for the second Print Cycle. Computer Digit operation in no way inhibits the read-in of printable symbols, but as it is purposely intended that all characters be read-in to Memory during this type of operation, it is impossible for a Prevent Read-in signal to occur. In order that the special symbols will not actuate any of the circuits normally influenced, this function is prevented during Computer Digit operation. Zeros which are being suppressed upon read-in will be modified prior to entering Memory and print as "0" on the second printed line.

In order to explain the logical operation of the Computer Digit circuitry, one complete cycle of this type of operation will be described. It may be assumed that prior to the initiation of this cycle, certain manual and machine operations have been completed - GENERAL CLEAR has been operated, and a START ZERO FIELD has been connected to start on address line 5. Refer to Figure A, and Figures 2-25, and 2-26, Computer Digit - Read Cycle, and Computer Digit - Print Cycle, respectively, in conjunction with the following.

The portion of a blockette considered for description purposes consists of Fast-Feed I, Multiline, Ignore, Space, Zero, Zero (suppressed). (The symbols are presented here without consideration of any printing information with which they may be combined).

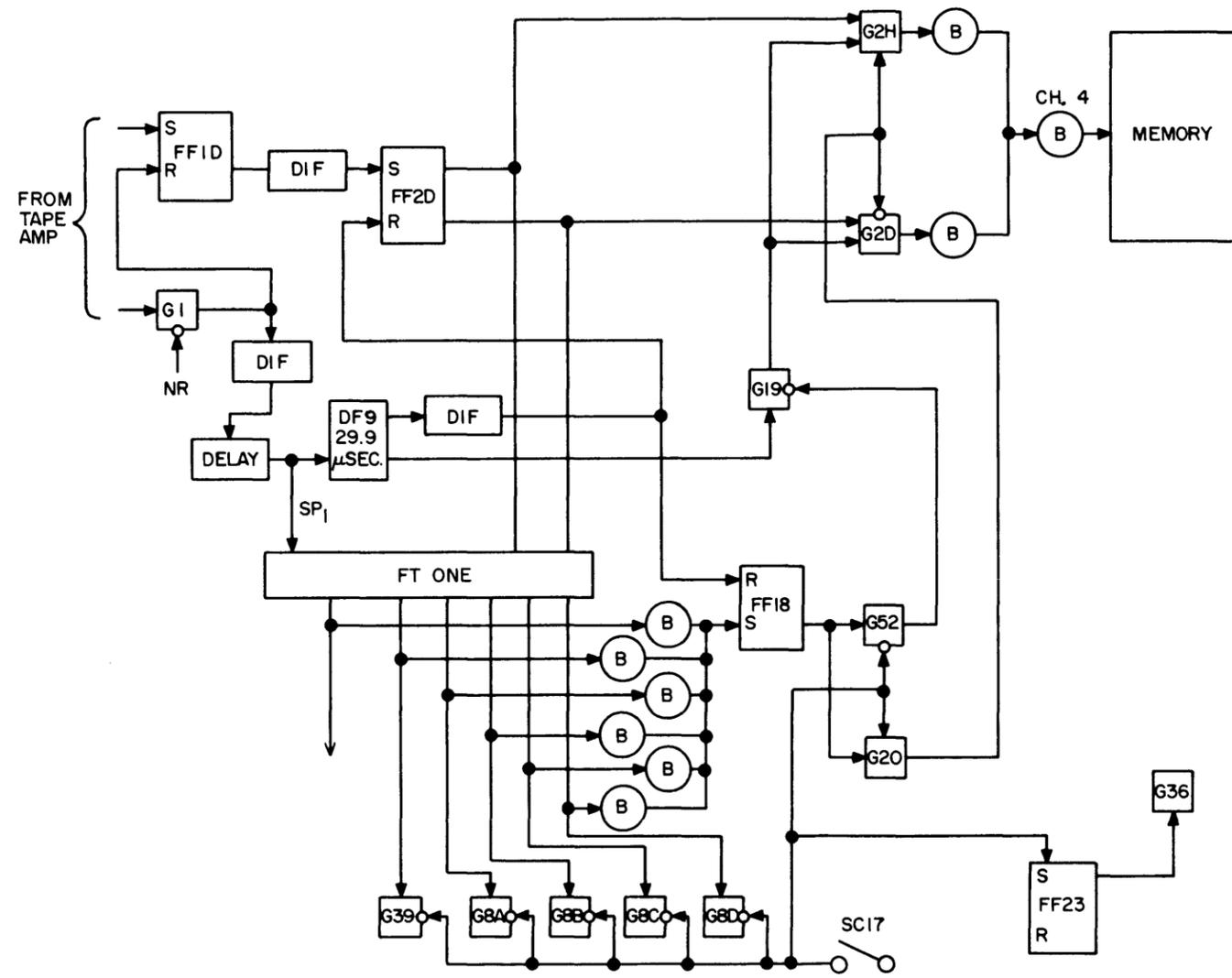
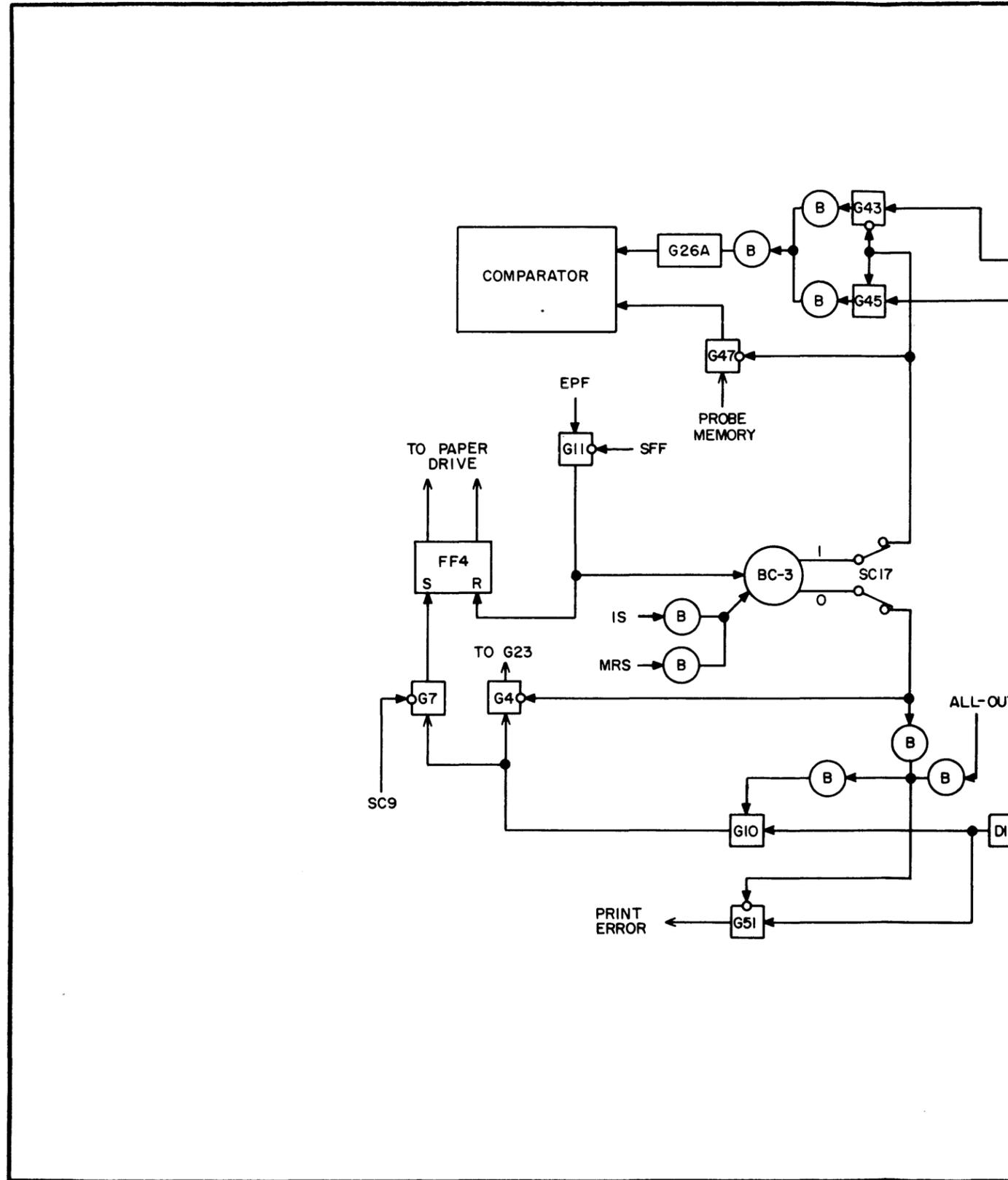
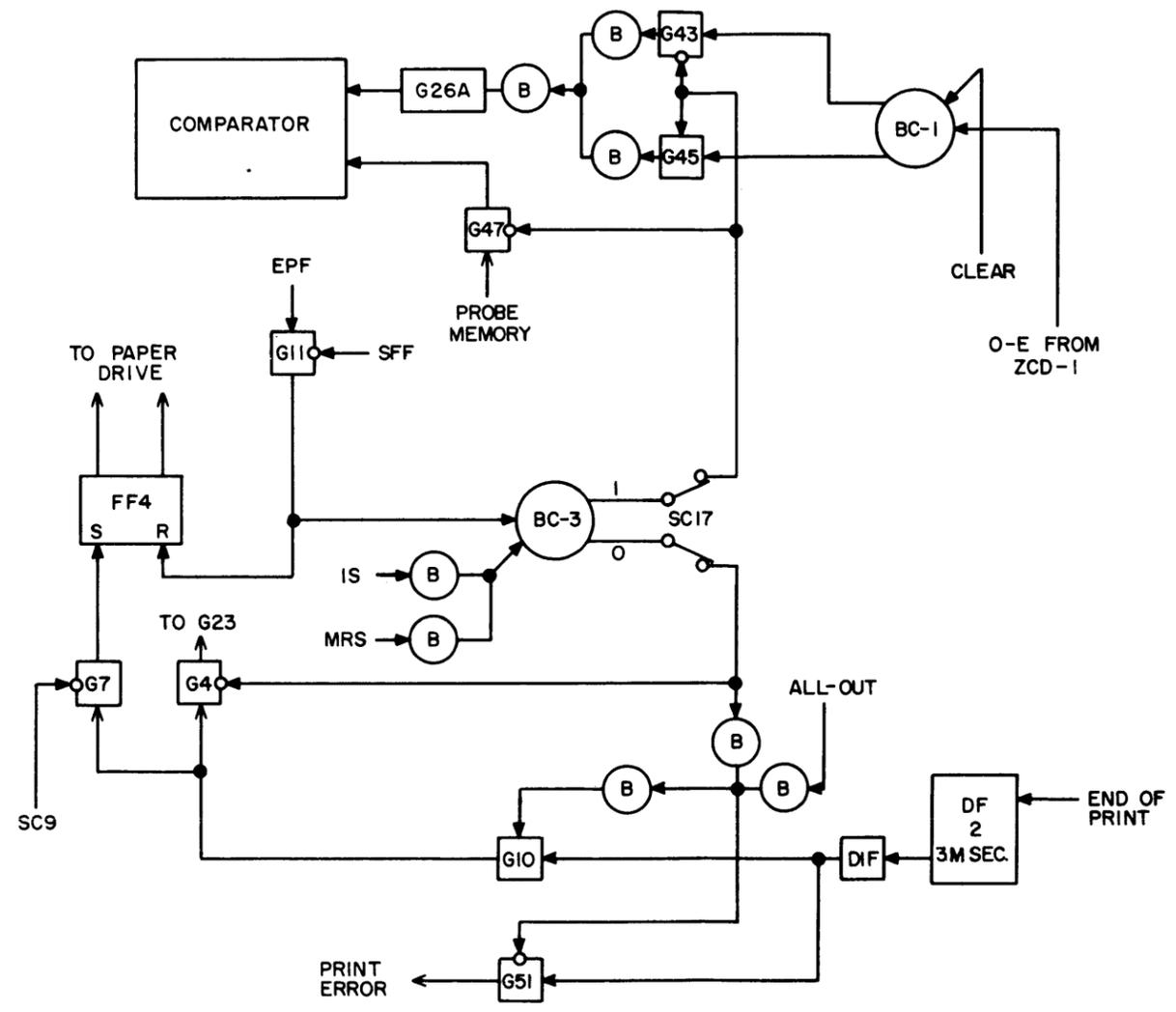


Figure 2-26. Computer Digit - Print Cycle
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Closing the COMPUTER DIGIT switch SC17 affects numerous circuits. An inhibition is placed on G39, the Multiline Control gate (described in the preceding sub-section under "Multiline"); an inhibition is placed on G52, and an enable on G20. As was mentioned in the referenced sub-section, the latter action will prevent ML symbols received during Computer Digit read-in from producing a set pulse for DF22. In addition, any set output from FF18 will produce a non-printing Symbols signal through G20, rather than a Prevent Read-in signal by way of G52. In this way a Prevent Read-In signal cannot occur during Computer Digit operation.

Further circuits included in the voltage level received from SC17 are an inhibition to gates 8A, 8B, 8C and 8D, which prevents Fast-Feed symbols from the tape from being acted upon during Computer Digit operation; and a set signal of continuing level to FF23, which permits a Fast-Feed V operation to be commenced prior to the read-in of the first character. SC17 also connects the output of BC3, the Computer Digit control counter (see Figure 2-26, Print Cycle) to the circuits indicated. In operation the "0" side of BC3 places an inhibition on G51 and G4, and an enable on G10. The "1" side of BC3, when set, places an inhibition on G43 and G47, and an enable on G45.

Following the closing of SC17, the INITIAL start switch (SC2) is closed, which commences a Read Cycle. As the blockette being considered here is as indicated in a preceding paragraph, the initial character read-in is the symbol for Fast Feed I (@, print-out D). This sets the Input flip-flops as in the following, with corresponding outputs as shown (pulse code 0 01 1111):

FF2A	Reset,	Output enable to G2A
FF2B	Reset,	Output enable to G2B
FF2C	Set,	Output 1 to Q2 (Quarter Adder)
FF2D	Set,	Output 1 to Q3
		Output enable to G2H
FF2E	Set,	Output 1 to Q3
FF2F	Set,	Output 1 to Q2
FF2G	Set,	Output 1 to Q1

It should be observed in the above table that there are an odd number of "0's" being directed to the Quarter Adders, and also an odd number of enables being supplied to the Input Gates.

The coded combination is passed to FT1, which alerts the FFI decoding gate. The SP₁ pulse for the character being read-in at the moment sets DF9 by way of a buffer stage (not shown in figure), which enables G19, and also is channeled through the FT1 decoding gate, thence through a buffer stage, to set FF18.

The set output of FF18 supplies a final enable to G20, the output of which develops a Non-printing Symbols signal (Computer Digit Symbols). This signal is transferred to input gates G2D and G2H as an inhibition and an enable respectively.

Three enables are now impressed on G2H as a result of the foregoing action -- one from the output of DF9 by way of G19, one from FF18 by way of G20, and one from the set output of FF2D. Therefore, in Memory location 1, channel grids 1, 2 and 4 receive enables and the three corresponding thyratrons fire.

Observe that the pulse code combination stored in the Input flip-flops is 0 01 1111 (FF1), but the combination in Memory location 1 is 0 01 0111. An explanation of Memory storage is thoroughly discussed in Section 1 under 3.c, "Memory Unit," It will be observed in that discourse that Memory stores "0's", rather than "1's". However, when non-printing symbols are read-in during Computer Digit operation, the fourth binary digit will be complemented during transfer to Memory, due to the action of the Non-printing Symbols signal on G2D and G2H. It will also be noted that in this instance, the coded combination stored in Memory is a character without representation, neither printable nor non-printable. Figure 2-27, Transfer Between Input and Memory, shows how digits impressed on the Input flip-flops are transformed in reaching Memory. As the second character is read-in, a Multiline symbol is transferred to Memory. As in the previous instance, a transposition occurs in transfer to Memory. The combination stored in the Input flip-flops is 0 01 0000 and the combination stored in Memory is 0 01 1000 -- note that the fourth binary digit is complemented during transfer.

The third character to be read-in is an Ignore symbol. In this case the Input flip-flops retain 1 00 0000, and the combination transferred to Memory is 1 00 1000.

The Space symbol (Δ , print 6) occurs as the fourth character to be read-in, with the Input flip-flop combination being 0 00 0001 and the Memory transfer-combination being 0 00 1001.

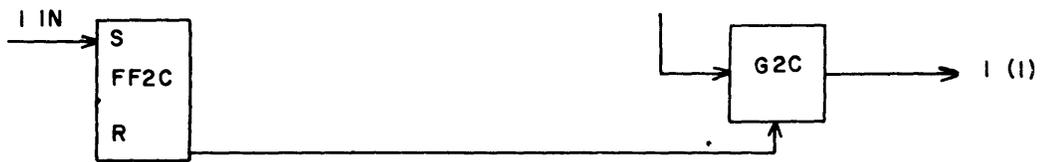
As the next character read-in is a "0" which does not occur during a Zero Field, FF18 is not set, a non-printing symbol signal is not produced, and the combination transferred to Memory is that which appears at the Input flip-flops, 1 00 0011, no transposition having occurred.

G44 receives an enable from Address line 5 following the end of the fifth Zero Field gate for Single Line. The SP pulse from the sixth character therefore passes G44, developing a set pulse for FF14. The set output of FF14 passes to G32 as an enable. As this occurs, the sixth character, a suppressed zero in this instance, is being transferred to the Input flip-flops. It is decoded in FT1 as a zero and appears as a second enable on G32 and as an inhibition on G33. The SP₁ samples G32, which is enabled and the pulse accordingly passes through to set FF18, via a buffer stage. FF18 develops a non-printing symbols signal via G20.

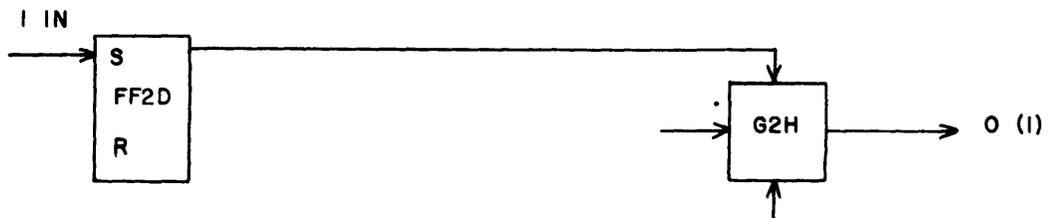
The zero is transferred to Memory with the fourth binary digit being complemented, and the combination being stored as 1 00 1011.



"0" signal restores FF2A, enabling gate G2A. Unit Memory changes normally stored "1" to "0".



"1" signal sets FF2C. No enable is placed on G2C. Unit Memory therefore retains normally stored "1".



"1" signal sets FF2D to "1", with output impressed on G2H, (note output from restored side of FF2D). Set signal samples G2H, which is enabled, thus changing normally stored "1" to "0".

Figure 2-27. Transfer Between Input and Memory
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From the foregoing, the combinations now stored in Memory locations 1 to 6 are as follows:

0	01	0111	(Fast Feed I)
0	01	1000	(Multiline)
1	00	1000	(Ignore)
0	00	1001	(Space)
1	00	0011	(Zero, not complemented)
1	00	1011	(Zero, complemented)

(The coded combinations above do not represent the Univac code combinations for the symbols shown, the fourth binary digit having been complemented.)

Observe in the table above, that all symbols read-in which are influenced by the non-printing symbols signal contain an even number of ones. Upon completion of the Read Cycle, G17 receives a final enable and a Print Cycle occurs. During the Probe Memory phase, all Check tubes connected to a Memory location by patch cord will be fired, as these locations will be retaining information.

As the Print Cycle occurs, all printable combinations stored in the Memory will be printed. The non-printable symbols stored will not be printed at this time, as no combination will appear at the Code Generator output gates which will compare with a combination having an even number of binary ones.

It follows, therefore, that at the completion of the Print Cycle mentioned, the Check tubes in the Print locations, which are connected to Memory locations storing a non-printing combination, will still be in a conductive state. As a result, following the completion of this Print Cycle, an All-Out signal will not be developed.

In order that a Read-Start signal may be developed under these circumstances following the end of the first Print Cycle, the "0" output of BC3 is placed on gates G10 and G51 as a substitute for the All-Out signal. This is accomplished through the action of a portion of the Computer Digit switch SC17.

When DF2 recovers, the output passes through a differentiator to G10, and is then channeled by way of a buffer to the Read-Start line. The signal on this line clears the Memory address counter and a Start Paper Feed signal is developed. However, due to the inhibiting signal on G4 from the "0" output of BC3, a Start Center Drive signal is not developed. Normal paper spacing occurs, nevertheless, following which the End Paper Feed signal steps BC3 to the "1" state.

When BC3 is stepped to the "1" state, all "0" signals are removed and the "1" signal is channeled to the following circuits:

1. An inhibition is placed on G47, the Probe Memory gate, which insures that no Check tube will be fired again pending the second Print Cycle. This probe-memory action is essential at this point, inasmuch as all Check tubes connected to Memory locations which are storing non-printing symbols, are still in a conducting state. As no printable combinations are to be printed during the Print Cycle at this time, the probe-memory action prevents the Check tubes, extinguished during the previous Print Cycle, from again firing at this time.
2. Gate G43 is inhibited, and gate G45 receives an enable which complements the output of BC1 for the second Print Cycle to occur.

When DF7 recovers following the paper-stabilizing period, the output of DF7 sets FF12, which initiates the second Print Cycle. In addition, DF3 and DF4 are set, but the same signal is unable to pass G47 as a probe-memory signal due to the BC3 inhibition. Consequently, when DF4 recovers in 250 μ sec and the output samples the Check tubes, no tubes are fired.

FF20 is set with the occurrence of the Print Cycle, and the Print signal also places an enable on the output gates of the Code Generator. Due to the output of BC1 being complemented, a combination appears at the Code Generator binary counter which requires a "1" for a check pulse, and the output of G26A will be a "0" representation. (For example, if the Index pulse for the Even minus (-) symbol sets DF16, BC2 is stepped to the "1" state. BC1 will be in the "0" state, therefore placing an enable on G43, but no enable on G45. The output of BC3 will place an inhibition on G43 and an enable on G45. The net result will be no output from G26A, as it will not be fully enabled.) Two hundred microseconds in advance of the odd Index pulse for the "0" character, a stepping pulse for BC1 passes ZCD1. This steps BC1 to the "1" state, which in turn places a second enable on G45. By way of a buffer this places a first enable on G26A.

As the Index pulse for the character "0" arrives, the pulse sets DF16, the output of which is differentiated and steps BC2 to the "0" state. This action then, steps the Code Generator binary counter to 00 0011. The set output of DF16 also passes gate G5, which develops a Probe Code Generator signal, and in so doing, a second enable to output gates G26A, G26B, G26C, G26D, and G26E. As gates G26F and G26G have an inhibition on them from the "1" side of their counters, no output will be obtained from these gates. The output from the Code Generator counter to the Comparator will be 0 00 0011. It will be observed that the output gates are enabled when the counter is on a count of "0" (output). When a "1" output occurs, an inhibition appears on the gate. It therefore follows that a "0" is read on the output side of the gates.

The code combination mentioned in the preceding paragraph will not compare with any of the combinations stored in Memory, using the example given. Under these circumstances, no alerting signals will be channeled to the Print locations, and equality will not occur between the "0" being stored in Memory location five and a Print location. Furthermore, no printable combinations stored in Memory can compare during the second Print Cycle (presently occurring in the example given), inasmuch as all combinations appearing at the output gates of the Code Generator will have an even quantity of "1's". However, at

this time the non-printing combinations stored in Memory (fourth binary digits complemented) will agree with certain combinations presented for comparison.

To illustrate, using the example quoted, the odd Index pulse for the character 5 (note that 5 is the Computer Digit print symbol for "Ignore") steps the Code Generator counter to 00 1000, BC1 being in the "0" state. As G43 will be inhibited, G26A produces no output (which is in effect, "1"), the total combination at the output gates being 1 00 1000. This code combination, when compared to the combination being stored in Memory location three, indicates equality. The "Ignore" symbol read-in under Computer Digit operation will therefore be printed as 5 on the paper.

Next, the Odd Index pulse for the character 6 steps the Code Generator counter to the combination of 00 1001. BC1 is in the zero state, permitting an output to appear from G26A with a total combination of 0 00 1001. This combination, upon comparison, agrees with the combination stored in Memory location four, and a printing of character 6 (Δ space) is effected.

Without further progressive details being given, the printing of the remaining non-printing symbols occurs, with the example being represented on the paper along with other information in the following typical manner:

2070 0529 BROWNSTONE

DE5 68 666

Spacing symbols to the right of the figure 8 (Zero Suppressed), were not given in the original example, but are indicated here as a typical print-out. It will be noted that the print-out is accomplished on two lines - the printable symbols being printed on the first line during the first Print Cycle, and the normally non-printing symbols on the second line during the second Print Cycle.

Upon completion of the second Print Cycle, all Check tubes will be extinguished (non-conducting), and at the time of recovery of DF2, G51 will be inhibited and G10 enabled, resulting in a Read Start signal, (see Figure 2-26 Print Cycle). The All-Out signal must be present at the end of a Print Cycle, otherwise G10 will not be enabled and G51 will not be inhibited, and a Print Error Stop will result.

The Read Start signal produces a Clear Counter, a Feed Paper, and a Start Center Drive signal, respectively. The Memory is cleared and a new blockette of information proceeds to be read-in. Following a Paper Feed action, BC3 is stepped to the "0" state, thus alerting the Print Cycle circuits to again print printable code combinations. This cycle of operation will continue as Read, Print printable codes, Print non-printing codes, Read, etc. The operation will stop upon a Normal Stop or Error Stop.

d. FAST-FEED. - A brief description of Fast-Feed operations and the techniques involved has been given in Section 1 under "Special Functions." It must be clearly understood that a Fast-Feed operation does not mean that the paper moves through the Printer at a greater rate than normally (22 ips); merely that the paper moves a greater number of line spaces in one general motion than that indicated by previous plugboard connection (single-, double-,

or triple-space). Between Fast-Feed (FF) Start and Stop, the paper will continue to space-out -- to the end of the paper roll if not stopped.

Certain operations under FF control which are mentioned in the "Programmer's and Operator's Handbook" are briefly reviewed here, prior to discussing the circuit-logics in detail.

An FF function may be actuated by tape control symbols (FF I, FF II, FF III and FF IV), or by Paper loop control (FF V and FF VI); however, all FF operations are ended by paper loop control.

The paper loop mentioned is thoroughly described in the "Operator's and Programmer's Handbook". This loop, which is mechanically ganged to the paper-drive roller, has seven channels, each of which contains a punched hole. Wire brushes, forming part of an electrical circuit, probe the channels on the paper loop, with the circuit being completed and a signal generated each time a hole is encountered by a brush.

An FF V symbol (also known as Automatic Start-Stop) from the paper loop may occur together with a tape-controlled Fast-Feed start, during a paper-feed period. The circuits involved determine that the FF symbol in the tape will override the paper loop instruction. Furthermore, any FF symbol must occupy the first character position of a blockette of information in order to be recognized as such by the paper-feed circuits. However, when the Printer is in continuous operation, the paper will be approximately at the end of its movement at the time the first character is read-in, and it is conceivable that an FF V signal (from loop) could be received prior to the FF V signal being received from the tape.

In order that the tape symbol will precede the loop signal, the latter is delayed until the completion of the first character read-in. Should this first character be an FF symbol, the FF V signal is cleared from the circuit, with the tape-controlled FF symbol signal replacing it. When an FF V Start symbol is received by the circuits involved during a normal paper space, and an FF symbol does not appear in the first character position of a blockette, the FF V start operation occurs following the read-in of the first character.

An FF V signal will be accepted by the FF circuits if the paper is in motion in a normal paper-spacing action, but not when the paper is already under an FF influence.

The following paragraph indicates the various FF operations, the signal required to start and stop each operation, and prerequisites where applicable:

<u>Operation</u>	<u>Start Signal</u>	<u>Stop Signal</u>	<u>Required Conditions</u>
FF I	FF I symbol	Paper Loop, CH 1	
FF II	FF II symbol	Paper Loop, CH 2	
FF III	FF III symbol	Paper Loop, CH 3	Tape-controlled start

FFIV	FF IV symbol	Paper Loop, CH 4	Must occupy first character position
FFV	Paper Loop, CH5	Paper Loop, CH 6	Feed paper flip-flop. FF4 must be in set state. No Fast-Feed in process. First character read-in.
Homepaper	SC11	Paper Loop, CH7	Control-loop switch closed.

The duration of an FF operation is controlled essentially by the set period of FF5, the Master Fast-Feed flip-flop. The setting of FF5 initiates an FF operation, with the set output of FF5 inhibiting End Paper Feed signals until the previously-arranged quantity of these signals has been prevented from influencing the machine.

The following example illustrates an application of the foregoing action. In this, and other examples to follow in the discussion of Fast-Feed operations, refer to Figure A, and the various simplified logic diagrams as mentioned progressively in the text.

In this example, paper spacing has been prepared by connecting the paper-spacing plugboard for single spacing. An FF operation occurs, arranged to move the paper eight spaces. When FF5 is set the paper is moving, and as the paper must be moved eight spaces, the set output of FF5 inhibits eight End Paper Feed signals. Following this inhibition, a hole which has previously been placed in the paper loop will produce a reset signal to FF5, which permits the next EPF signal to reset the Feed Paper flip-flop FF4, thus ending the paper feed.

In Fast-Feed operation the Master Fast-Feed signal initially sets FF5. An inhibition is placed on G11 from the set side of FF5, in addition to inhibitions to G11, G37 and G13. The same set signal passes to G64 as an enable. The inhibition which prevents an End Paper Feed, mentioned previously, is the one to G11, and the inhibition on G37 prevents a FF V Start signal from setting FF6E while a Fast-Feed operation is in progress.

The inhibition to G13 insures that FF12 will not receive a set pulse during a Fast-Feed. Note that it is possible for the EPF pulse from the normal paper space to have passed G11 before FF5 receives a set signal; when this occurs, the FF operation is delayed until DF7 recovers, inhibiting the restored output, and only then continuing the paper-feed. If the restored output of DF7 from a normal EPF pulse were permitted to set FF12, a Print Cycle would occur simultaneously with paper transport.

The enable to G64 develops a Start Paper Feed signal, should the paper drive not be in motion upon arrival of the FF symbol. Set pulses for FF5 are developed by the closing of SC11, the HOME PAPER switch, when used; and by the restored output of DF11 with Fast-Feed sequences. The latter action is determined by each FF symbol developing a reset pulse for FF6E, destined to precede an FF V command. Should FF6E be in a set state at the time of arrival of a

reset pulse, FF6E will develop a reset pulse for FF5. In order to accomplish this the set pulse is delayed 50 μ sec by DF11 before applying to FF5. Thus a set and a reset pulse will not arrive simultaneously at FF5. An example of this follows (refer to Figure 2-28, Fast Feed Operation - Delay).

Presume that FF6E is in the set state, with the first character to be read-in being a Fast-Feed II. The FF II signal passes through G8B, developing a set pulse for DF11, DF13, FF6B, and a reset pulse for FF6E. The resetting of FF6E produces an output from the reset side, which is differentiated and develops a reset pulse for FF5. As described in the foregoing paragraph, FF5, which is already in a reset state, is not influenced at this time by the pulse.

The delayed (100 μ sec) output of DF13 inhibits G37, thus insuring that FF6E does not receive another set signal during the period that DF11 is delayed. The recovery of DF11 produces a set pulse for FF5, commencing a Fast-Feed operation. It will be observed that the delay of DF11 has prevented a set and a reset pulse from reaching FF5 simultaneously. The action proceeds with G11 being inhibited for the number of EPF pulses required, until a Channel 2 hole is sensed, which restores FF6B. The restored output of FF6B resets FF5, which permits the next EPF pulse to pass G11 by removing the inhibition, thus ending the paper-feed.

The circuits of the Home Paper section of the Printer provide a means of synchronizing the paper loop with the format of the forms used for receiving the printed output of the machine. This synchronization is accomplished automatically by the Home Paper circuits if the paper loop is initially aligned with the form, and when the latter is accomplished, it is also indexed with the tape information.

Switch SC11, HOME PAPER, and CONTROL LOOP switch SC30, together initiate the accomplishment of the Home Paper function. CONTROL LOOP switch SC30 when actuated, connects the sensing brushes into circuit when a Fast-Feed operation is to be performed. Stop signals will not be generated on Fast-Feed operation unless switch SC30 is closed.

Referring to Figure 2-29, Fast Feed Operation Home Paper, a Home Paper operation functions as will be described in the following. With a paper loop on the paper-loop drum and all switches initially neutral, the CONTROL LOOP switch is raised, which performs the function described previously, and connects the HOME PAPER switch to the set input line of FF5. In addition, a circuit from the input side of G62, around G62 to DF8 is opened when CONTROL LOOP SC30 is actuated.

With the actuating of HOME PAPER SC11 a number of actions occur. The circuit is broken to the INITIAL (Start) SC2, and START (SC1) switches. Flip-flop FF11 receives a set jamming signal, thus preventing a Print action, and the Channel VII Fast-Feed brush is connected to the restored input side of FF5. The neon indicator on the Supervisory Control panel illuminates HOME PAPER, and a differentiated input signal is directed to the set side of FF5, via SC30.

Subsequently the set output of FF5 places an inhibition on G37, G11, and G13, and an enable on G64. The output of G64 is differentiated and passes by

way of a buffer to G7. The output of G7 is a Start Paper Feed signal to set FF4, engaging the paper-feed clutch for a mechanical paper-feed action.

As G11 is inhibited, all EPF pulses generated by the indexing system are disregarded, which causes the paper drive to remain in motion. Consequently the paper loop continues to move until the Channel 7 hole on the loop is encountered by the probing brush. When this occurs, the circuit between the metal drum and brush is completed, causing a signal level to be routed by way of switch SC11, through a differentiator and a buffer to the reset side of FF5.

As FF5 is restored, the inhibition is removed from G11, permitting the next EPF pulse to pass G11. The output of G11 restores FF4, subsequently causing a mechanical braking action of the paper-drive system and a stopping of paper movement.

Figure 2-30, Fast Feed Operation - Typical Example, represents a typical form similar to many that find use on the HS Printer. This form and the operations evolving from the program prepared for the use of the form will be explained in some detail in this discussion of Fast-Feed operation. The form as shown illustrates the results of a typical operation, with a paper loop being shown to the left of the invoice. Due to the short length of the invoice forms, one paper loop is used to accommodate two forms. The total length of one form is thirty-six lines; thus, a seventy-two line paper loop is used. The second-half of the paper loop is an exact replica of the first half. One complete revolution of the paper loop causes two complete forms to move past the print hammers.

Consider for example, a condition in which the paper loop has just been placed on the machine. The tractors do not contain paper, and the carriage is "out". At this time the CONTROL LOOP switch SC30 is closed, which brings the loop brushes in contact with the loop at, arbitrarily, line 65. The brushes bisect the space between line 65 and line 66. Closing the HOME PAPER switch, SC11, commences paper movement, the movement continuing until the Channel 7 brush senses the Channel 7 hole in line three. The Channel 7 brush develops an output which restores FF5, removing the inhibition from G11. The next light-pulse resets FF4, which brings the paper to rest with the loop brushes bisecting the space between line three and four. The foregoing is typical of the operations required prior to running the form.

The pre-printed forms are now placed in the tractors, the top of the pre-printed "UNIVAC HIGH-SPEED PRINTER" being aligned with the index line on the Print Head as shown in Figure 2-31, Index Line on Backplate. (Deviations of less than a sprocket distance may be compensated by the tractor-adjustment handle, which moves the complete tractor assembly vertically.) Following the completion of alignment with the index line on the Print Head, the carriage is moved in and the HOME PAPER switch is placed in the neutral position. The paper-drive system is now prepared to print.

The GENERAL CLEAR switch is raised, insuring that all circuits are in a neutral state. It is presumed here that tape has been loaded, and the Uniservo is prepared to read. The INITIAL switch is actuated, thus initiating a Read Cycle. The recovery of DF12 permits the selection of L Address lines, and Address line 0 is selected. Address line 0 is supplied as an enable to the Fast-Feed gates, G8A through to G8D. The blockette currently being read-in

Figure 2-28. Fast-Feed Operation - Delay
PX 616

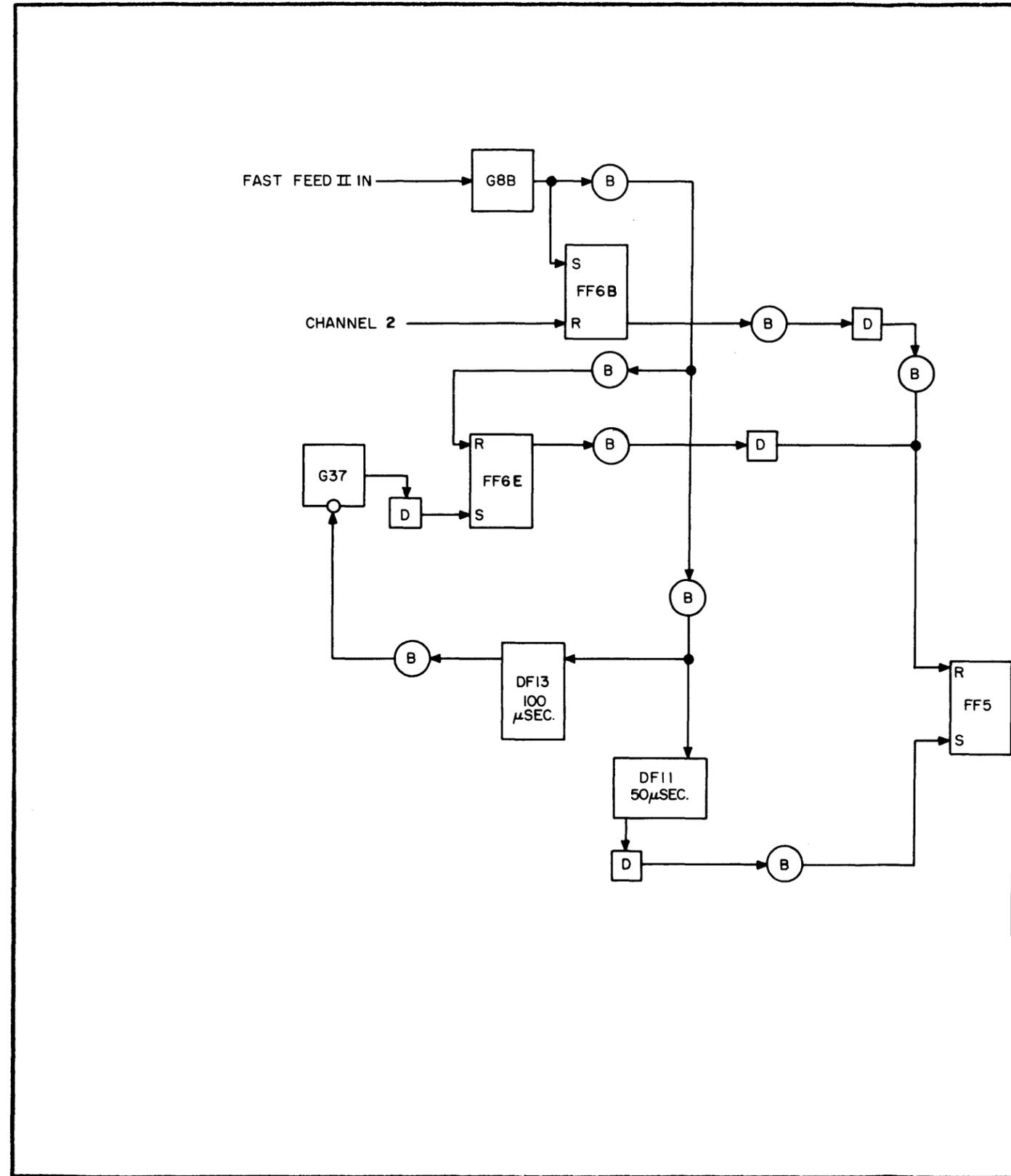
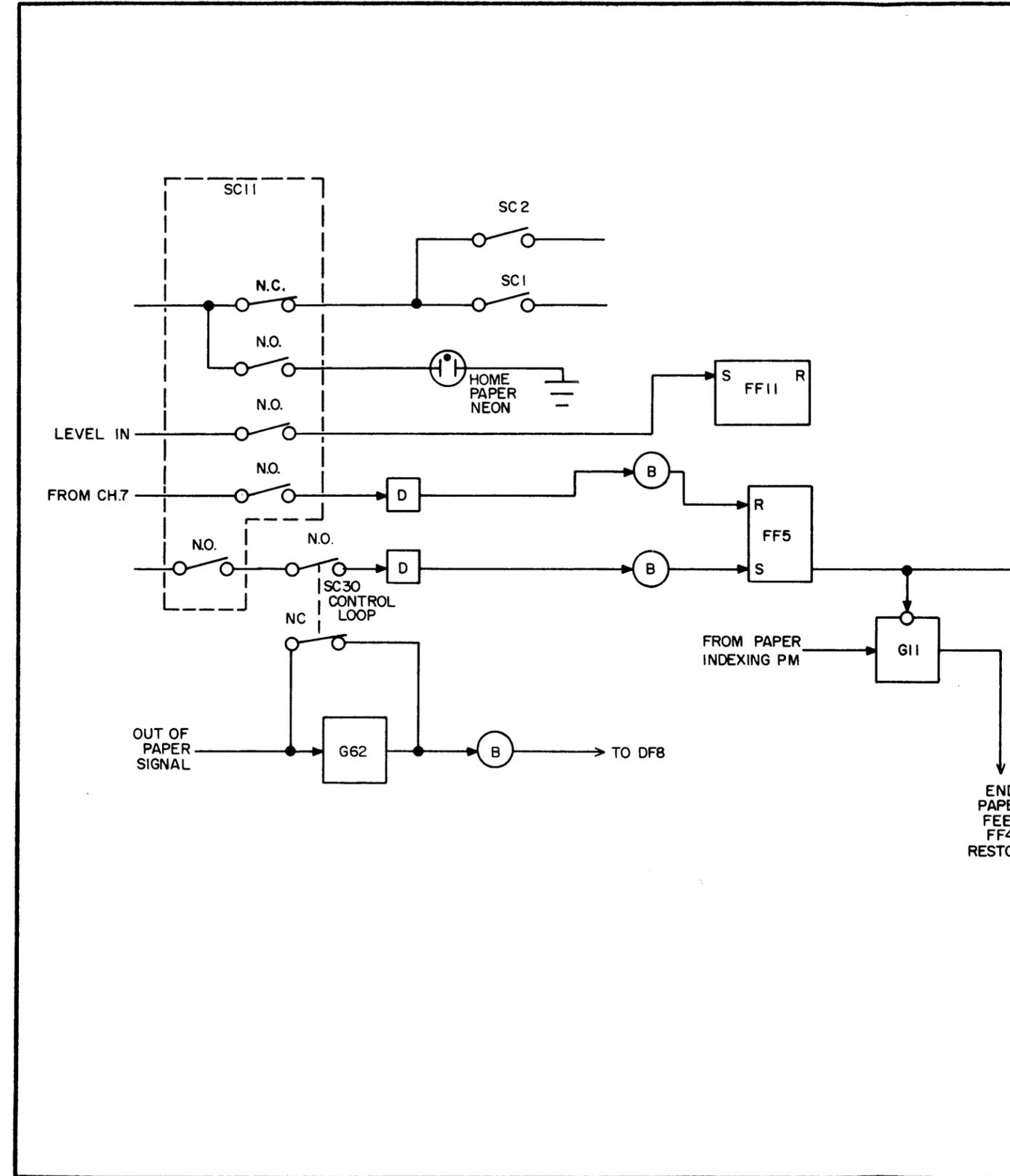
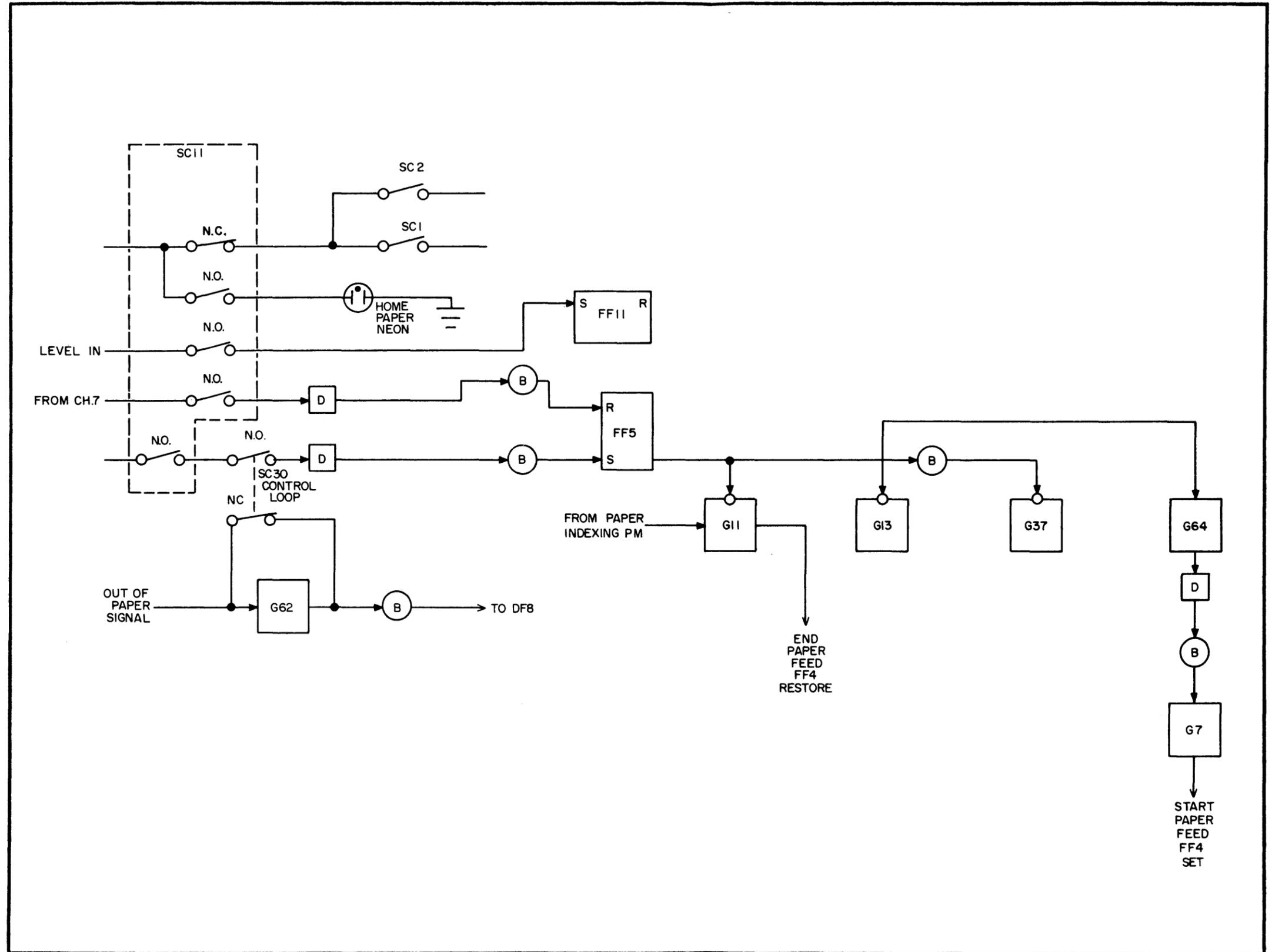
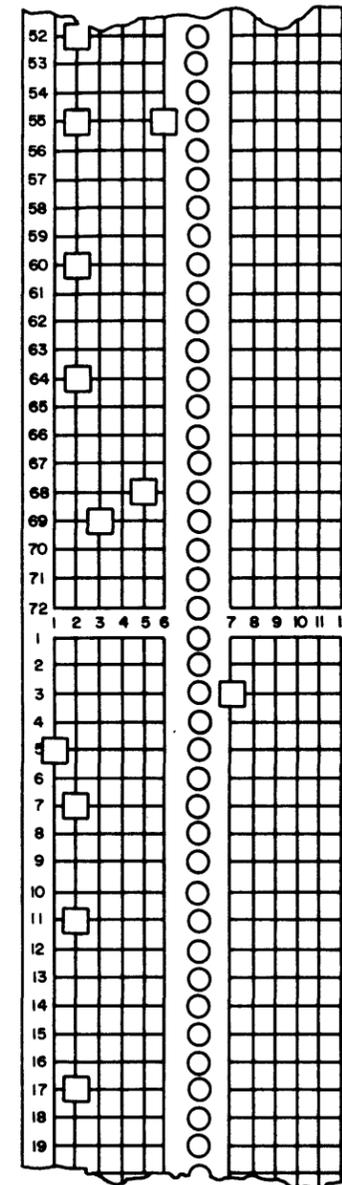


Figure 2-29. Fast-Feed Operation - Home Paper
PX 616







PREPAID EXP		TERMS	NET CASH
QUANTITY	CATALOG	DESCRIPTION	
100	31-901	PIPE FITTING, ELBOW, 2-INCH	
50	31-902	PIPE FITTING, TEE, 1 1/2-INCH	
30	31-904	PIPE FITTING, TRUE V, 2-INCH	
50	47-905	COUPLING, 1 1/2-INCH	
30	47-906	REDUCER, 2-INCH	
5	50-920	HUNDRED FEET SWP PIPING 2-INC	

CUSTOMER BILLING BY REMI
 PREPARED BY THE
UNIVAC® HIGH-SPEED

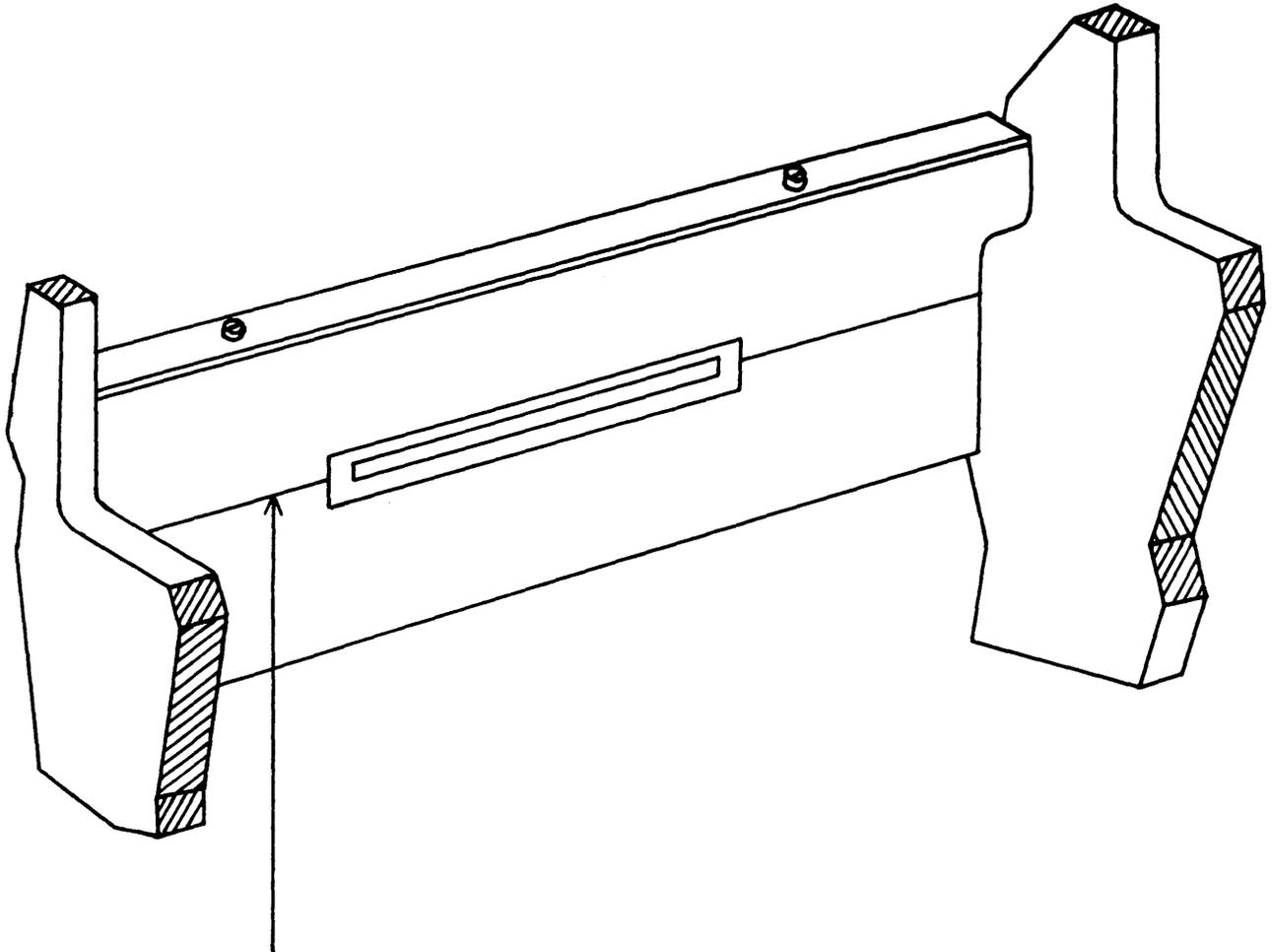
DATE JUNE 27, 195

SOLD TO ASSOCIATION OF AMERICAN RAILROADS
 ACCOUNTING DIVISION

SHP TO SAME
 HOTEL AMBASSADOR
 THE BOARDWALK
 ATLANTIC CITY, N. J.

PREPAID EXP		TERMS	NET CASH
QUANTITY	CATALOG	DESCRIPTION	
200	11-403	BEARING, ROLLER	

Figure 2-30. Fast-Feed Operation - Typical Example
 PX 616



INDEX LINE SCRIBED ON STAINLESS STEEL
COVER PLATE CENTERED IN RELATION TO HAMMERS



Figure 2-31. Index Line on Backplate
PX 616

contains a Fast-Feed I symbol in the first character position, and a Date and Invoice Number field. The FF I symbol is decoded in Function Table 1, and, at the time of the SP₁ pulse, supplies a set signal to FF18 and an enable to Gates G58 and G8A. Gate G58 lacks an enable, but as G8A is fully enabled by Address line 0, the signal passes through. The output of G8A channels a set pulse to DF11, DF13, and FF6A, and a reset pulse to FF6E.

The recovery of DF11, fifty μ sec later, produces a Master Fast-Feed signal, which acts as a reset pulse to FF7 and FF12 (note that FF12 up to this point would be in a set state resulting from the recovery of DF7, which was set by the Initial Start signal). The Master Fast-Feed also functions as a set pulse to FF5. When FF5 is set, a Start Fast-Feed signal is produced, which passes through G64 and G7, setting FF4 which subsequently causes the paper drive to commence. The form and the paper loop now move in synchronism for a distance of two line-spaces. The Channel 1 brush then detects the hole in line 5, resetting FF6A the reset output in turn resetting FF5, and removing the inhibition from G11. The next EPF pulse stops the paper drive on line 5, and is channeled as a set pulse to DF7. The recovery of DF7, 10 msec later, supplies a set pulse to FF12, the set output of which supplies the final enable to G17, and a Print Cycle ensues. The information read-in is now printed on line 5 of the form.

Following the completion of the Print Cycle, a Read-Start is developed, which clears the Memory and the Memory Address counter. The Read Start also starts the center drive and the paper drive. Approximately 7.5 msec later, the read-in of the first character occurs. The character is decoded in FT1 as an FF II, and is channeled from that point at SP₁ time as a sampling pulse to G8B. As Address line 0 is present, the FF II pulse passes through, setting FF6B, and passes via a buffer into the set line of DF11. The recovery of DF11 and the subsequent setting of FF5 occurs prior to the generation of the EPF pulse, to end the normal paper spacing (the EPF pulse occurs approximately 8.2 msec after Read Start two), thus the paper drive continues in motion an additional space, at the end of which the Channel 2 brush detects a hole. This occurrence causes FF6B to be reset, the output in turn resetting FF5, removing the inhibition from G11 and stopping the paper drive on line 1. A Print Cycle occurs, followed by another Read Cycle and a single paper space, again followed by a Print Cycle.

The next Read Cycle involves another Fast-Feed, which moves the paper to line 11. Reading and printing continues, with Fast-Feeds programmed to move the paper the desired number of spaces. Each time a form is completed (printing of the "Total" or last line), the following blockette of information will contain a Fast-Feed I symbol, which moves the paper to the date line on the following form. For purposes of editing, a Fast-Feed I will always be programmed for fast-feeding from one form to another. A further sub-example to the foregoing may clarify the reasoning behind such programming procedures.

Let it be assumed that the Printer is in operation, and a Print Cycle is in process on line 57. A Print Error occurs as a result of spurious noise erroneously firing a print location. The Printer now stops with the printing error registered and the paper on line 58.

The carriage is "run-out" for examination of the copy and it is determined that a printing has occurred in an incorrect column, thus nullifying the use of the form. The carriage is returned and the READ NO PRINT switch is closed, jamming the print circuits and the Special Functions circuits. GENERAL CLEAR is actuated and the READ (one blockette) BACKWARD switch, SC 6 is closed, which supplies a first enable to G59 and G58. Due to the inhibition from SC9, the signal cannot pass G58, thus FF11 remains in the reset state. The restored output of DF5, the Manual Read delay flip-flop supplies a set pulse to DF1, and an MRS signal which sets DF7. The recovery of DF1 sets FF3 and the center drive now commences to move in a backward direction.

The tape continues to move until the blockette containing the FF I symbol is read-in. As the blockette is being read-in in a backward direction, the FF I symbol will now occupy the 120th character position. As the information is read-in backwards, the FF I signal, in sampling G59 (which is enabled by SC5), passes through and sets FF11. The recovery of FF3 at the end of the Read Cycle finds G17 inhibited and the Printer stops. The READ (one blockette) BACKWARD switch is now placed in a neutral position, together with the READ NO PRINT switch, SC9.

The GENERAL CLEAR switch is now closed, followed by the raising of the INITIAL switch. The blockette containing the FF I is now read-in in a forward direction, thus the FF I symbol occupies the first character position. Consequently FF6A is set, and a Fast-Feed I operation occurs. The paper drive moves from line 58 on the form upon which the error occurred, to line 5 on a new form, at which point a Channel 1 hole is sensed and the paper drive ceases. The first blockette printed on the new form is the same information which was printed on the first line of the faulty form. Continuous operation now continues until a Normal Stop or Error is developed. By programming to form Fast-Feed operations as Fast Feed I operations, information may be edited one form at a time rather than one blockette at a time.

A Fast-Feed V, or automatic Start-Stop, receives a Start signal from the Channel 5 hole on the paper loop. However, the start is delayed due to the lack of an enable on gate G36 from FF23 (see Figure 2-32, Fast Feed Operation - FF V), until the completion of the read-in of the first character.

FF23 is set to produce the required enable for G36 by the initial Clear Input flip-flops (CIF) signal from the restored output of DF9, via a differentiating circuit and buffer stage, which occurs at the end of the first character read-in. In this manner, an FF V operation cannot occur until the initial character position in each blockette is searched for a Fast-Feed symbol FF I through to FF IV. When a Fast-Feed symbol occupies the first character position, FF6E is reset, with this symbol assuming precedence to an FF V demand. An example of this phase of operation follows:

Again refer to Figures 2-30 and 2-32, in addition to Figure 2-33, Fast-Feed Operation - Precedence. A line of printing has occurred on Line 67. Punching of the paper loop has been previously performed for a required format as indicated in the figure. Presume that a Read Start signal has just been generated.

The Read Start signal develops a Start Paper Feed signal, a Clear Counter signal, a set pulse for DF1 and a Clear Memory signal. As the Clear Memory signal sets DF12, a de-ion signal is produced which alerts the Keyed B+ circuitry. The output of the Keyed B+ passes through a buffer and is differentiated and passes to FF23 as a reset pulse, thus removing one enable from G36.

At a point approximately half-way in the normal paper-space transit (4.1 msec) the Channel 5 brush detects the hole on line 68 of the paper loop. Note that at this moment G37 is enabled, as no inhibitions are present, consequently FF6E receives a set signal caused by the Channel 5 probe brush. The set output of FF6E is a first enable to G36.

Three milliseconds later, the first character is transferred from the Align Input flip-flops to the Input flip-flops. Inasmuch as the blockette being read-in contains the "Total" for the invoice shown, the first character in the blockette will be a FF III symbol (pulse code 0 10 1111, symbol ?). The SP₁ gates the FF III symbol through Function Table I, which passes a set pulse to FF18 and an enable to G8C.

The output of G8C develops a set pulse to FF6C, DF11 (via a buffer stage), DF13, and also by way of another buffer to reset FF6E. When the latter action occurs, the first enable which is on G36 is removed, and the reset pulse, after passing through a buffer, differentiator and second buffer stage, resets FF5, the latter being up to that moment in a set state.

Delay-flop DF9 develops a CIF pulse 29.9 μ sec following the above action, which passes to FF23 as a set pulse and to G36 as an enable. Nevertheless, there will be no output from G36, the enable from the set side of FF6E being removed as described. Approximately 20 μ sec later, DF11 recovers, the recovery pulse passing through a differentiator and buffer to FF5, setting DF5 to produce a Fast-Feed III operation.

The paper-drive system transports paper until the probe brushes on the tape-loop roller sense the hole on line 69. When this occurs a reset pulse is channeled to FF6C, which in turn supplies a reset pulse to FF5 by way of the components previously mentioned. When FF5 is reset, the inhibition to G11 is removed, which permits the next EPF pulse to pass through G11 and reset FF4. FF4 then accomplishes a normal braking action function, stopping the paper drive. A printing action subsequently occurs and the "Total" indicated on the sample invoice in Figure 2-33 is printed-out on line 69. The function of a tape-controlled Fast-Feed action assuming precedence before a FF V operation has thus been accomplished in the example given.

The Fast-Feed V operation provides two important functions to Printer operation. One is to provide for automatic Start-Stops for double or triple spacing since the first character position in a blockette cannot be used for a Fast-Feed symbol, for instance when a Fast-Feed operation is required within a Multiline operation. In addition, the Fast-Feed V operation permits overflow conditions, which may arise on pre-printed forms, to be successfully accomplished. An example will be given to clarify this type of occurrence. Refer to Figure 2-35, Fast Feed Operation - Form Overflow, and to Figure 2-34, Fast Feed Operation - Overflow Logic.

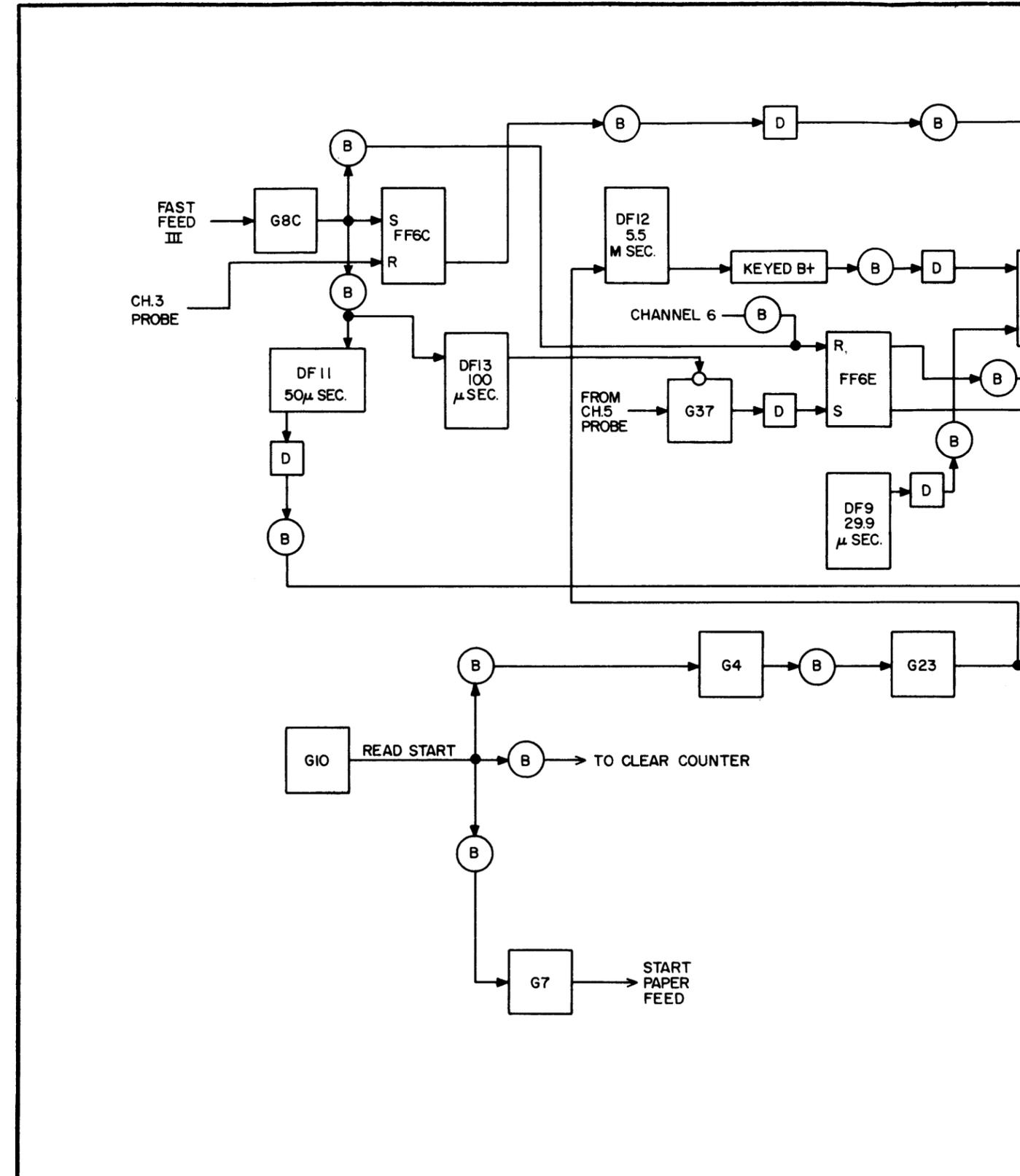
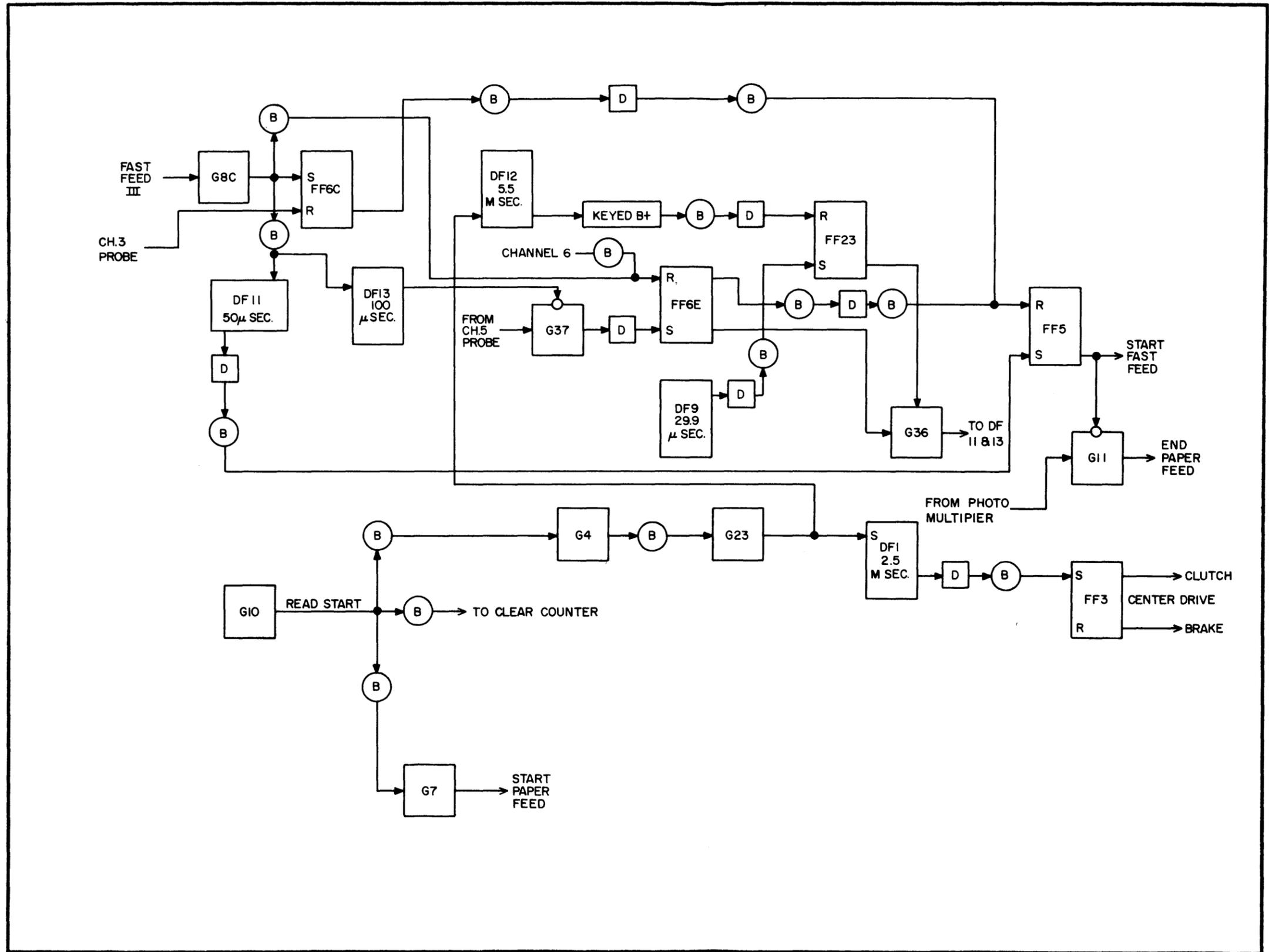


Figure 2-32. Fast-Feed Operation - FF V Example
PX 616



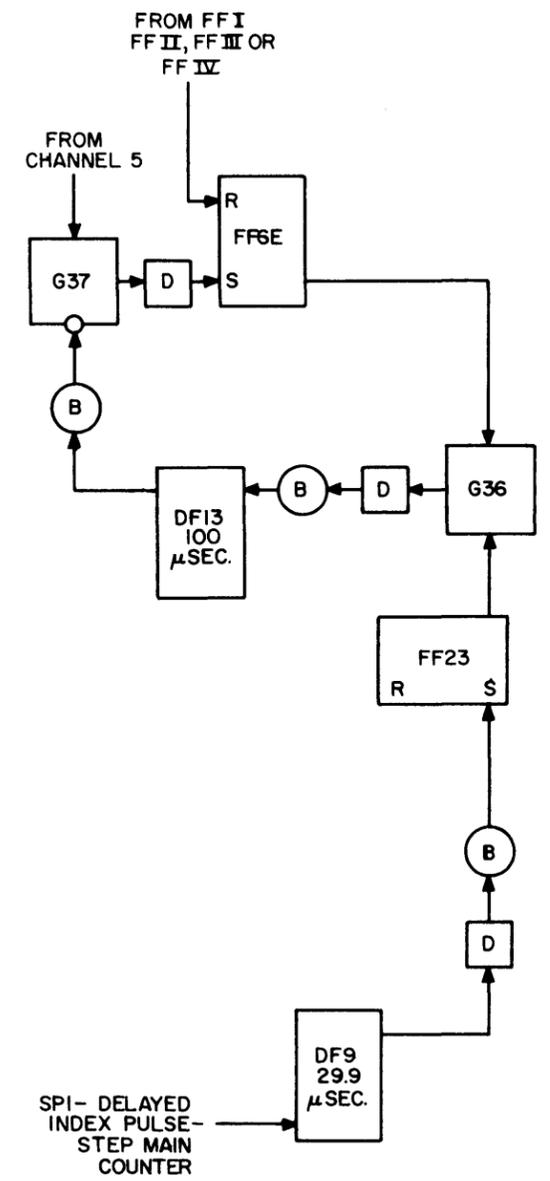
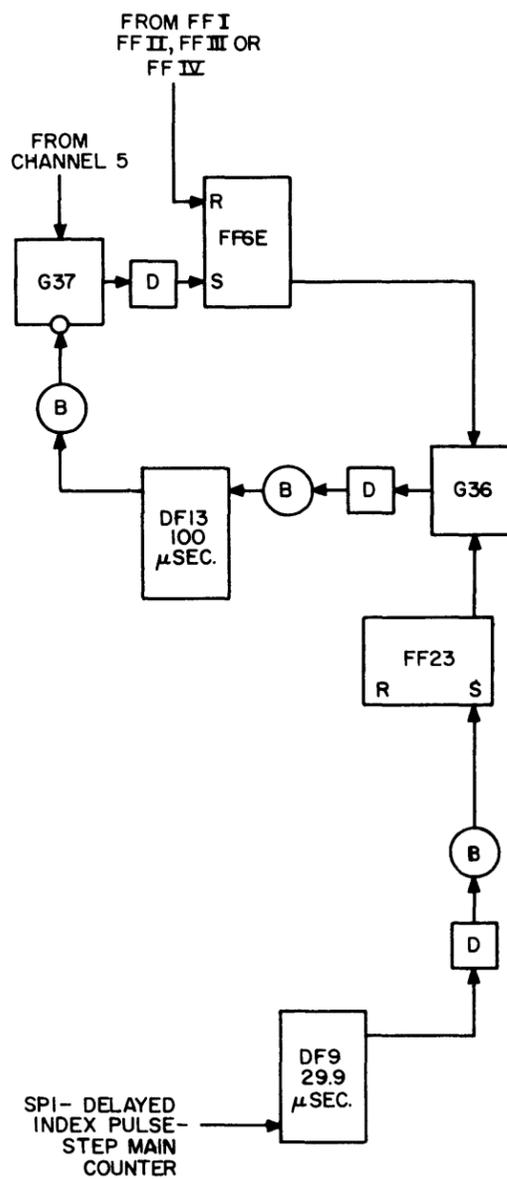


Figure 2-33. Fast-Feed Operation - Precedence
PX 616



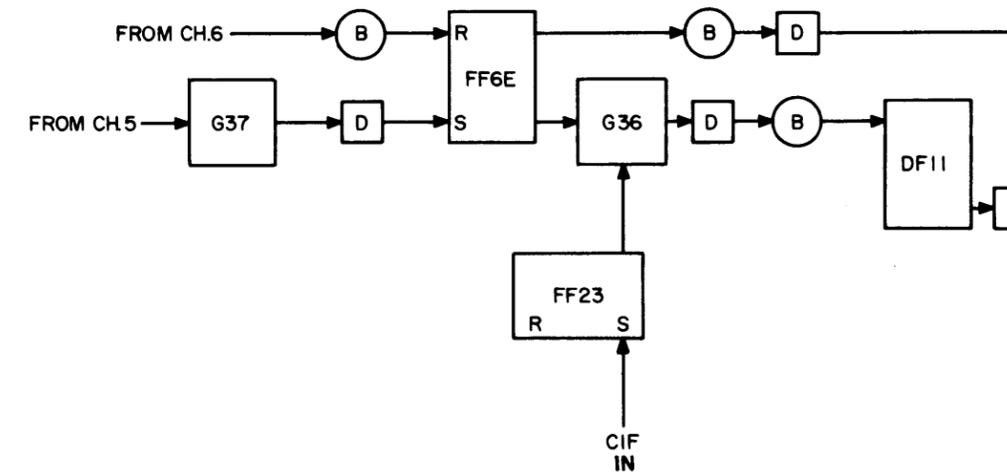


Figure 2-34. Fast-Feed Operation - Overflow Logic
PX 616

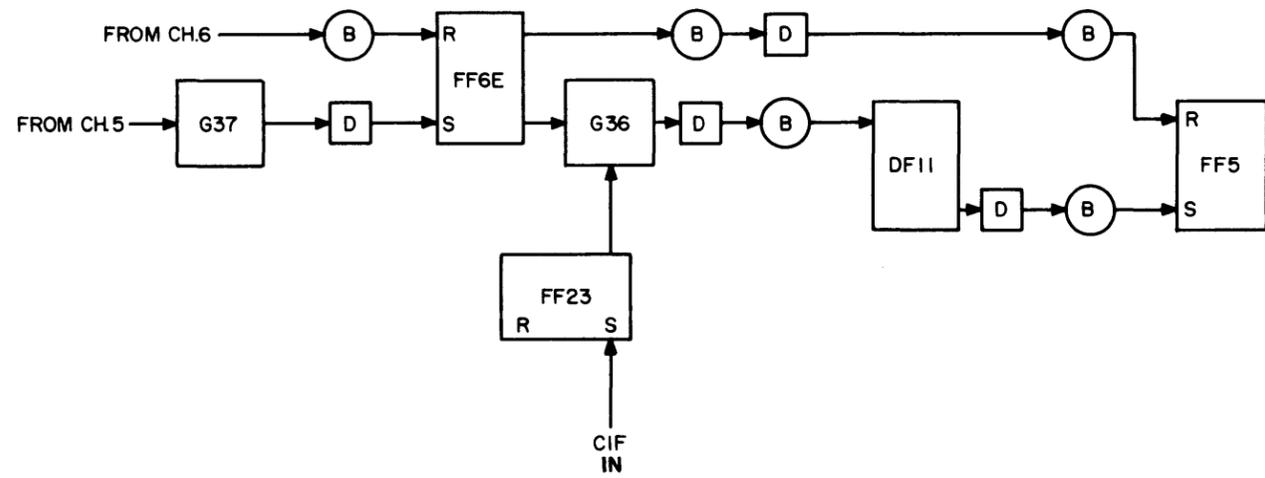
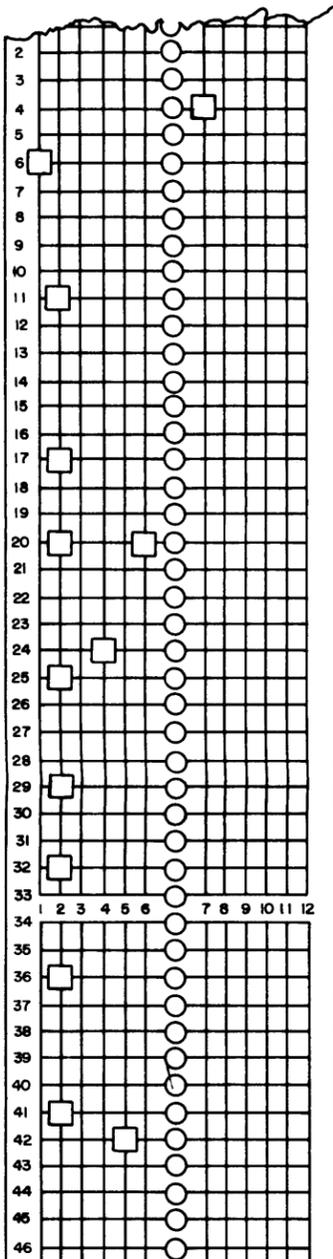


Figure 2-35. Fast-Feed Operation - Form Overflow
PX 616

131



CUSTOMER BILLING BY REMINGTON RAND
PREPARED BY THE
UNIVAC® HIGH-SPEED PRINTER

DATE JUNE 27, 1955

INVOICE NO.

SOLD TO ASSOCIATION OF AMERICAN RAILROADS
ACCOUNTING DIVISION

SHIP TO SAME
HOTEL AMBASSADOR
THE BOARDWALK
ATLANTIC CITY, N. J.

INVOICE

PREPAID EXP.

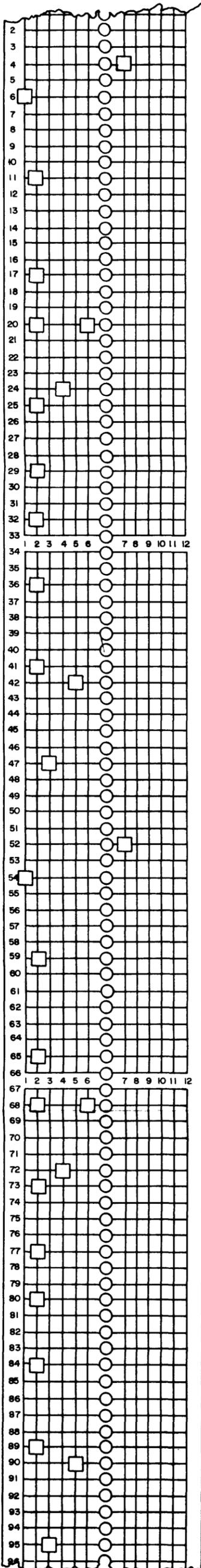
TERMS NET CASH

SALESMAN GS

YOUR ORDER NO.
09800

QUANTITY	CATALOG	DESCRIPTION	UNIT PRICE	AMOUNT
100	31-901	PIPE FITTING, ELBOW, 2-INCH	\$ 97	\$ 97.00
50	31-902	PIPE FITTING, TEE, 1/2-INCH	1 03	51.50
30	31-904	PIPE FITTING, TRUE V, 2-INCH	1 46	43.80
50	47-905	COUPLING, 1 1/2-INCH	56	28.00
30	47-906	REDUCER, 2-INCH	60	18.00
5	50-920	HUNDRED FEET SWP PIPING, 2-INCH ID	81 37	406.85
8	56-786	BUSHINGS, BRASS, 3-INCH	2 35	18.80
13	56-787	BUSHINGS, BRASS, 3 1/2-INCH	2 57	33.41
8	63-432	DRUMS, STEEL, 25-GAL CAP	14 28	114.24
10	63-433	DRUMS, STEEL, 35-GAL CAP	15 80	158.00
6	63-435	DRUMS, STEEL, 50-GAL CAP	17 43	104.58
2	81-211	CABINET, STEEL STORAGE	44 50	89.00

TOTAL THIS INVOICE



CUSTOMER BILLING BY REMINGTON RAND

PREPARED BY THE
UNIVAC® HIGH-SPEED PRINTER

DATE JUNE 27, 1955

INVOICE NO.

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8	56-786	BUSHINGS, BRASS, 3-INCH	2 35	18.80
13	56-787	BUSHINGS, BRASS, 3 1/2-INCH	2 57	33.41
8	63-432	DRUMS, STEEL, 25-GAL CAP	14 28	114.24
10	63-433	DRUMS, STEEL, 35-GAL CAP	15 80	158.00
6	63-435	DRUMS, STEEL, 50-GAL CAP	17 43	104.58
2	81-211	CABINET, STEEL STORAGE	44 50	89.00

TOTAL THIS INVOICE

CUSTOMER BILLING BY REMINGTON RAND

PREPARED BY THE
UNIVAC® HIGH-SPEED PRINTER

DATE

INVOICE NO.

SOLD TO

SHIP TO

INVOICE

TERMS

SALESMAN

YOUR ORDER NO.

QUANTITY	CATALOG	DESCRIPTION	UNIT PRICE	AMOUNT
9	91-549	STOCK, STEEL ROD 3/4-INCH	10 85	\$ 97.65
20	91-563	STOCK, STEEL ROD 1 1/2-INCH	21 00	420.00
12	92-422	STOCK, STEEL ANGLE 2-INCH	27 50	330.00
4	92-423	STOCK, STEEL ANGLE 2 1/2-INCH	28 70	114.80

TOTAL THIS INVOICE \$ 2125.63

It will be seen, by glancing at the invoice used for this example, that the format has limitations as to the quantity of items that may be entered. In this instance, the form is full and there remain four items to be included in addition to the "Total". It is therefore necessary to use a second form; but it would be superfluous to again enter the preamble on this copy of the invoice, not to mention the additional time required for tape programming and printing. In this event then, Fast-Feed is performed to advance the invoice to the next copy at the beginning of the description and quantity, in this manner passing the preamble.

In the example, consider the paper-drive system to have stopped at line 67, and the printing of a body item occurs. Following the Print Cycle, a Read-Start Cycle moves the paper-drive system to line 68, consequently the Channel 5 probe brush detects the Channel 5 hole in the paper loop. Flip-flop FF6E is thus set, and an enable is placed on G36. As there is further invoice information to be printed, there will not be a Fast-Feed symbol contained in the following blockette of information. Due to this, the CIF pulse to FF23 sets FF23, with the output acting as a second and final enable to G36. The output of G36 is differentiated, passes through a buffer stage, and after setting DF11 and again being differentiated sets DF5. The paper-drive mechanism now proceeds to move, continuing to do so past the invoice preamble area until the first line position in the second invoice body is reached. At this point, which is line 20 in this particular example, a hole in Channel 6 is probed by the probe brush on the paper-loop system, originating a reset pulse to FF6E, which in turn by means of the output pulse, resets FF5 stopping the paper drive on Line 20, the first line position in the body of the second invoice. A Print Cycle now occurs, with succeeding phases of operation printing the remaining invoice information. It will be observed that in this particular example a saving of eight blockettes of information and eight Print Cycles has been accomplished. (Following the completion of invoice information, the blockette read-in which contains the "Total" will also contain a Fast-Feed III symbol, this taking precedence before a Fast Feed V initiative.)

5. ERROR-DETECTION CIRCUITS

In the same manner that examples were frequently given in the previous sub-sections to illustrate various operational logics, this portion of the Manual will use examples to explain the functions of the Error-Detection circuits. In the majority of cases, more than one example will be given in order to indicate all possible operational conditions.

a. ODD-EVEN ERRORS. - Referring to Figure A, it may be seen that the Odd-Even Error circuit consists of six quarter-adder sections Q1, Q2, Q3, Q4, Q5, and Q6; gate G14, flip-flop FF8, and switch TC20.

The function of this circuit is to check each character while being read into the Input flip-flops and determine whether or not an odd number of binary "1's" are contained in the character.

EXAMPLE 1:

The Odd-Even circuits are operative in this example and a normal character "A" is being read-in during a normal Read Cycle. (Pulse code 1 01 0100.)

As SP time occurs during this process, the character is transferred from the Align Input flip-flops to the Input flip-flops by the action of the Jam Clear signal. This, then, places the Input flip-flops in the following status:

FF2A is set with a "1" to Q5
FF2B is reset with a "0" to Q1
(actually, with NOT a "1" to Q1, therefore a "0")
FF2C is set with a "1" to Q2
FF2D is reset with a "0" to Q3
FF2E is set with a "1" to Q3
FF2F is reset with a "0" to Q2
FF2G is reset with a "0" to Q1

The output from the Quarter Adders will be:

Q1 "0" to Q4, Q4 to "1" to Q6
Q2 "1" to Q4
Q3 "1" to Q5, Q5 to "0" to Q6, Q6 "1" to G14

Observe that a "1" signal output from Q6 will pass to G14 as a No Odd-Even Error signal thus placing an inhibition on G14. Conversely, a "0" signal output, or no output, from Q6 will not place this inhibition on G14. The inhibition, when it appears on G14, will appear for the duration of the read-in period, that is, the set period of DF9.

In this example, Q6 is passing a "1" to G14, hence an inhibition and the inability for the SP₁ pulse to pass through G14 due to this inhibition. As the SP₁ pulse does not pass G14, FF8 is not set and a Prevent Print signal is not developed.

If at any time during the course of a read-in, no output is developed from Q6, it will be seen that FF8 will duly become set and a Prevent Print signal will be developed.

A further example under slightly different conditions will now be considered.

EXAMPLE 2:

Again the Odd-Even circuits are operative and the character "A" is being read-in. However, in this instance, a noise pulse may be considered as erroneously setting flip-flop FF2G. The character thus created (1 01 0101) is transferred from the Align Input flip-flops to the Input flip-flops at SP time by the Jam Clear signal as in the preceding example, which places the Input flip-flops in the following status:

FF2A is set with a "1" to Q5
FF2B is reset with a "0" to Q1
FF2C is set with a "1" to Q2
FF2D is reset with a "0" to Q3
FF2E is set with a "1" to Q3
FF2F is reset with a "0" to Q2
FF2G is set with a "1" to Q1

The output from the Quarter Adders will then be as follows:

Q1 "1" to Q4, Q4 "0" to Q6
Q2 "1" to Q4,
Q3 "1" to Q5, Q5 "0" to Q6, Q6 "0" to G14

As explained previously, a "0" signal to G14 does not inhibit, thus the SP₁ pulse for the character read-in passes the gate and sets FF8. As this occurs the set output of FF8 passes by way of the DELETE O.E switch TC20 and buffer stages to the Prevent Print line. As the Prevent Print line is alerted, FF7 is reset and an inhibition is placed on G17. When G17 is alerted, the Printer will stop at the end of the Read Cycle. Inasmuch as any failure of any of the components or circuits involved in the Odd-Even Checker will produce a lack of inhibition on G14, the machine will stop operation should this occur.

The purpose of TC20 in this circuitry is to open the output line from FF8 to the Prevent Print line. This is primarily for the purposes of maintenance and fault-finding, for, by opening TC20, the Printer may be operated continuously even though Odd-Even errors may be occurring.

b. GREATER, OR LESS THAN, 120 ERRORS. - The greater, or less than 120 Error checking features of the machine, which is also known as the 120 Digit Check, insures that each blockette read from tape contains exactly 120 digits. The Less-Than-120 Error conditions are developed in the circuitry to a Greater-Than-120 Error, which permits the same general circuits to be used for both types of error. Examples follow which will detail this machine function.

EXAMPLE 1:

Consider the 120 circuits as operative and a blockette of 121 characters is read-in. Under normal conditions no change in operational state will occur if

exactly 120 characters are read-in. Assume then, at the point of this example, that DF9 is in the set state, having been thus set by the 119th Sprocket Pulse.

As DF9 recovers, the Manual Address binary counter is stepped to a count of 119, selecting Address line 119. This Address line alerts Memory location 120 and simultaneously places an enable on G41. The SP₂ from the 120th character, in sampling G41 finds it enabled, and passes through to set FF10.

The set output of FF10 is channeled to G16 as a first enable and to G15. G16 and G15 are the End Read and Greater-Than-120 gates, respectively. At this point the SP from the irregular 121st character arrives at G15, which, being enabled, produces an output signal that sets FF9, the Greater-Than-120 Error flip-flop. The output of FF9 passes to G19, the Prevent Read-in gate, as an inhibition. This will prevent the 121st character from being read into Memory. The latter statement may be amplified by considering the no Memory location will be alerted as an Address line is not selected, due to the fact that the character is being read-in with an Address line count of 120 - a non-existent address.

The DELETE 120 O.E. switch TC19 alerts the Prevent Print line via buffer stages and also illuminates the 120 CHECK neon indicator on the Supervisory Control panel. Under the conditions as indicated in this example, the machine will stop, with the lamp on. The Memory address counter will be at a count of 121 when this occurs, and, as an address that is non-existent was selected, the ADDRESS CHECK neon will also be indicating an error (see Address Line Errors, following sub-section).

EXAMPLE 2:

An example of a less-than-120 Error character occurring will now be given. In this case a blockette which contains 119 characters is read-in, and, as in the previous example it may be considered that DF9 is in the set state, having been set by the 119th SP₁.

DF9 recovers, which steps the Address line counter to a count of 119, which selects Address line 119. In this case however, no further Sprocket Pulses occur, so that after an elapse of five pulse times, RDF1, a 400 μ sec retrig-erable delay flop, recovers. The consequent recovery pulse samples G16, which is not enabled (FF10 still being in a reset condition).

The tape continues to move under the above conditions, but approximately ten milliseconds later the first character of the succeeding blockette is read into the Align Input flip-flops. The result of this is that the SP from this new first character triggers RDF1, which removes the sampling signal from G16. The occurrence of a blockette containing less than 120 characters will always result in the reading of a second blockette.

Note that at this point a similar action to the Greater-Than-120 Error begins to occur. The first character in the second blockette is read into Memory location 120. The SP₂ from this character samples G41, which is enabled, and FF10 is thus set by the output of G41. The set output of FF10 enables gates G15 and G16. The recovery of DF9 steps the binary counter to a count of 120 which selects line L zero, but as there is no M15 decoding gate in the M-Section of the Minor Address (see Section 1-c Memory Circuits), neither an M line, nor a consequent Address line is selected.

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The SP caused by the second character, when sampling G15, passes through and sets FF9, the error circuitry being alerted as previously shown. The Sprocket Pulses continue to trigger RDF1 until the entire blockette has passed the Read Head. Each time that DF9 is set, the counter is stepped, but no read-in to Memory occurs due to the inhibition appearing on G19. The recovery of RDF1, which enables G16 and restores FF3, ends the Read operation.

As a result of the preceding the CHECK and ADDRESS CHECK neon indicators will be on to indicate these errors. The Memory address counter will be at 111.

c. ADDRESS LINE ERROR. - The purpose of the Address Line Error circuits is to check that an Address line is selected for each character as it is read-in. Should an Address line not be selected for any reason, an SP₁ is passed to the AE (Address Error) flip-flop FF19, and the error is indicated by the lighting of the neon ADDRESS CHECK on the Supervisory Control Panel.

Each LA, LB and M line is channeled as an enable to G38 (refer to Figure A). During the Read Cycle, as each Address line is selected, the output lines from the Minor Address enable G38. Should an L or M line fail to select an address, one of the enables will not be present on G38, hence an output will not be present for the character read-in at the time.

As G38 has no output, the inhibition on G28 will be lacking and the SP₁ (resulting from the character destined to fill a Memory location connected to the faulty Address line) will pass through and set FF19. Through TC21, when closed, the error will be indicated on the neon lamp and the Prevent Print line alerted. By the same circuitry, the absence of an LA, LB, or M line will also result in an Address line error.

Two examples of typical Address line errors follow.

EXAMPLE 1:

For this example, it is assumed that a fault is occurring in Minor Address Decoding gate L1. For the purpose of fault-finding, or, in the normal course of operations, a normal blockette of information is read-in. At this point it will be considered that DF12, the Clear Memory Timer has recovered.

This recovery removes the alerting signal from the Keyed B+ section, with the Keyed B+ signal disappearing. This removes the inhibition from the L section of the Minor Address. L zero is then selected and the LOA line in conjunction with the MO line, selects Line 0, thus selecting Memory location 1.

LOA, LOB and MO lines are placed as enables on G38. As G38 is now completely enabled the output passes as an inhibition to G28. As the read-in of the initial character occurs, the SP₁ from the first character samples G28, but due to the inhibition is unable to pass. DF9, on the recovery pulse from the first character read-in, steps the binary Address counter to "1", thus alerting the L1 gate. As a fault is considered to be in existence for the example in this circuit, no L1A nor L1B signal is produced.

It will be apparent that G38 now lacks two enables, and therefore an Address line will not be selected. The SP₁ which occurs from the second character

samples G28, which is enabled, and passes through to set FF19. From FF19 by way of switch TC21 and buffer stages the Prevent Print line is alerted.

The character is transferred to Memory by way of the read-in circuits; however, as no Address line is present, the character is not stored and Memory location 2 does not receive a character. DF9 recovers from the read-in and steps the counter to a count of 2, which selects the L2 gate. The output of the L2 gate selects L2A and L2B, which act as enables on G38 together with the MO signal which is present. It may therefore be seen that during the third character read-in, G28 is once again inhibited; and further, that every time the L1 gate is alerted, an Address line will not be selected, and FF19 will receive a set pulse. Note that under these circumstances Memory locations 2, 10, 18, 26, etc. will not contain information.

Upon recovery of FF3 the machine will stop and the ADDRESS CHECK neon lamp will be on. The failure of an M gate will result in an Address Check error, and eight consecutive empty Memory locations. It is quite possible for an LA line to fail and the LB line will be selected; however, an error will nevertheless be registered.

It is also possible that due to component failure, an LA, LB or M line may be selected during the entire read-in period. In this event, an Address Error will not be developed, but Memory locations will receive multiple read-in information. A typical example of such a situation is given in the following.

In this instance, all L gates and lines are normal. M2 is selected throughout the entire read-in of a blockette. As the Keyed B+ is removed, the LO lines are selected, with MO being selected in a normal manner and M2 by error. As LO, MO and M2 are selected, Address Lines 0 and 16 are selected, which alerts Memory locations 1 and 17. Under these conditions, the first character in the blockette is read into both Memory locations. Upon completion of the read-in, the binary counter is stepped to "1", which selects L1. With L1, MO and M2 selected, Address lines 1 and 17 are selected, alerting Memory locations 2 and 18, resulting in the second count being read into both locations.

The net result of the preceding is that Memory locations 17 through 24 will each receive eight characters, and presumably one to all of the eight Memory locations will contain non-printable combinations. The indicated result of such a situation will not be an Address Check error, and an error will not be registered while the Read Cycle is occurring. However, as the Memory locations contain information that cannot be printed, a PRINT CHECK error will be shown during the printing of the line.

d. PAPER FEED ERROR. - As paper moves through the HS Printer at a rate of 22 inches per second, should the normal stop circuits fail a considerable amount of paper could conceivably be wasted in a very short time. For instance, in one minute during a Paper Feed indexing system failure, 100 feet of paper will pass the print Head. The purpose of the Paper Feed Error circuits is to prevent such a situation from occurring by limiting the amount of paper fed during any one paper feeding operation, to approximately 22 inches.

This limitation is accomplished by providing that in the event that FF4 remains set for a period greater than one second, a Paper Feed Error signal

will be developed through RDF4, a retriggerable delay-flop of one second delay. The signal thus developed will jam FF4 in the reset state and at the same time inhibit G17. The resetting of FF4 of course, completes the brake actuating circuits for the paper-feed system.

Two examples follow; one to indicate a normal operation, and, by comparison, the generation of a Paper Feed Error.

In the first example, assume that the plugboard is connected for a single-space operation and the paper-feed circuitry is operative. Operation begins with a Start Paper Feed signal from G7. (FF11 will be in a set state at this time.)

The Start Paper Feed signal sets FF4, releasing the paper brake and energizing the clutch. The set output of FF4 is supplied as a set signal to RDF4, the Feed Paper Timer, and DF25, the Fast-Charge Delay. Setting RDF4 removes the enable from G29 at the same instant the inhibition from the reset side of FF4 to G29 is removed. DF25 recovers 750 μ sec after receiving a set pulse, and alerts the Fast-Charge tube for the brake capacitors, which stabilizes the brake circuits. Eight milliseconds following a set pulse, FF4 recovers, thus setting the brake and releasing the clutch. The set output of FF4 is placed as an enable on G72, the output of which places an inhibition on G29. One second after receiving a set signal, RDF4 recovers. As G29 is inhibited by a signal from the reset side of FF4, no output will occur from the gate. During continuous operation, RDF4 does not reset, as set pulses will arrive every 100 milliseconds, far more rapidly than the delay period.

In the next example, the machine is about to commence operation. Assume that an inadvertent failure to insert the paper-space control plug has occurred. Operation is commenced by raising the SPACE PAPER switch, SC25. The Start Paper Feed signal from G7 sets FF4, starting the paper drive in motion and supplying a set signal to DF25 and RDF4. As the plugboard connection for the paper-feed indexing system has not been completed, the exciter lamps will not be on, so that the paper feed will be moving, but pulses are not generated by the indexing system. One second after receiving a set pulse, RDF4 recovers. In so doing, the recovery pulse samples G29, which is non-inhibited and passes through to develop a Paper Feed Error (PFE). The PFE signal is supplied as an inhibition to G72 by way of the START Switch, SC1; as an inhibition to G17 by way of the Prevent Print line, and as a jamming reset signal to FF4, thus stopping the paper drive and placing an enable on G72. The PFE signal will remain until the START Switch is actuated, which removes the inhibition from G72 and permits the signal from the reset side of FF4, via G72, to inhibit G29 and remove the Paper Feed Error signal. In order for a PFE to develop, RDF4 must recover prior to the resetting of FF4, or in other words, the paper drive must be in motion in excess of one second.

e. FAST-FEED ERROR. - A Fast-Feed Error will occur when a tape initiated Fast-Feed instruction fails to precede a Fast-Feed V instruction. Logically and mechanically, the Fast-Feed gates fail to reset FF6E.

For example, consider the situation where a Fast-Feed III instruction is being used to fast-feed paper from the body of an invoice to the "Total" line. The paper loop has been punched to assume control of an overflow condition, should one occur.

Following the completion of the Print Cycle for the last line in the body of the current invoice, DF2 recovers and the output of G10 develops a Read Start signal. The Read Start circuitry commences paper movement through DF1, and clears the Address binary counter and the Memory. The leading edge of the Keyed B+ signal restores FF23, thus removing the enable from G36. As the paper loop is in motion and G37 enabled, the Channel 5 probe brush will detect a hole in the loop and set FF6E. The set output of FF6E places an enable on G9 and G36.

As the read-in of the first character takes place, the character is decoded by FT1 and passes by way of the Fast-Feed III output to G8C. The consequent output of G8C develops a set pulse for FF6C together with set pulses for DF11 and DF13. The same signal as a reset pulse to FF6E may be considered, for purposes of the example, to have insufficient amplitude (a faulty buffer component could cause this) and fails to reset FF6E. Therefore, the set output of FF6C arrives at G9 as a second enable, and a Fast-Feed Error signal is the output from G9. This is applied as a set signal to FF16, the output of which passes by way of a buffer stage to the Prevent Print line.

Paper movement continues until the Channel 3 hole along the "Total" line is sensed, which resets FF6C. The reset output of FF6C sets FF5 thus ending the Fast-Feed operation. The Printer comes to a stop with the immediately preceding blockette stored in Memory. At this moment also, the FAST FEED CHECK neon indicator will be on to indicate the error, and FF6E will be in the set state.

Under the above circumstances it would be normal for the operator to move the carriage out for inspection of the copy to determine whether or not the paper has been fed to the correct area. Assuming that this is the case, the carriage is returned and the START switch engaged. The latter action will cause SC1, through the circuits shown in Figure A, to place a reset pulse on FF6E, in addition to a MRS, to reset FF17. The machine then resumes normal operation.

f. CHARGE ERROR. - The Charge Error circuits are designed to check for the presence of a high-voltage supply for the actuator capacitors immediately prior to or during a Print Cycle. Should this be present or appear during the Cycle, the supply source will be interrupted. If the charge source were not removed during a Print Cycle the actuator fuses would fail, possibly all of them.

The charge voltage will be present at any time that gate G31 is enabled by having the inhibition from FF21 removed. By way of explanation of the Charge Error circuits, assume that during a phase of operation FF21 is in a reset condition and the charging line is at charging potential. Assume also that G17 has received a final enable and a Print Cycle is about to commence.

The Start Print Cycle LE, after differentiation, supplies a set pulse, but in this instance, due to either a component failure or deficient signal levels, fails to set FF21. The set output of DF3 sets DF21, which places a six μ sec inhibition on G63. When DF3 recovers, the recovery pulse sets FF20, which produces a Print Minus Probe Memory signal, one purpose of which is to act as a second enable on G63. DF21, as it recovers, removes the inhibition from G63, which, now fully enabled, develops a set pulse for FF22, the Charge Error flip-flop.

The set output of FF22, as a Charge Error signal, inhibits G49, thus opening the circuits to both RE1 and RE2. When these relays are not actuated the open contacts of RE2 remove the +600 volts from G31.

The Charge Error signal from the set output of FF22, is, in addition to the application mentioned above, applied to G21 as an inhibition, effectively preventing further Index pulses from passing G21. The Charge Error signal, after being differentiated and passed through a buffer, is applied to G7 which produces a Start Paper Feed signal. Due to the fact that further Index pulses are not forthcoming, the Printer stops and the CHARGE CHECK neon indicator lights.

In order to restore FF22, if the GENERAL CLEAR is actuated with no other inhibitory signals on G49, relays RE1 and RE2 will again close, placing the +600-volt supply on G31, and a reset pulse to FF21. In this case print capacitors discharging will cause any associated actuator fuses to fail. In order that this may be prevented, the carriage is properly moved out prior to actuating GENERAL CLEAR, thus providing an inhibition to G49 from the Carriage-Out limit switch SC29.

g. PRINT ERROR. - A description of the Print Error elements and general mode of operation has been previously given in Section 1. The prime purpose of the High-Speed Printer being to visually record information, the majority of faults occurring in the machine will have a visual result. The explanation of the Print Error circuits will therefore be based on six typical examples of faults which will result in Print Error checks being registered.

The All-Out signal is channeled to G10 as an enable, and to G51 as an inhibition. Should an All-Out signal not be present at the end of a Print Cycle, G51 will not be inhibited, and the differentiated output of DF2 will pass through G51 to produce a Print Error signal, rather than passing through G10 as a Read Start signal.

Any Check tube which remains in a conducting state following the completion of a Print Cycle will result in a Print Error being registered. The Print Error signal is placed on G7 as an enable, thus causing a Paper Feed; and to FF13, the Print Error flip-flop. With switch TC18 (DELETE PRINT ERROR) the machine will not print, and stops with the PRINT CHECK neon lamp on (the A.O. DET CHECK neon will be off).

Example 1:

Presume that during a Read Cycle, a character "A" is stored in Memory location 1. A normal read-in occurs up to the point of actual firing of the Memory tubes. At this time the Channel 2 thyratron fails to fire, which causes a non-printable combination of 1 11 0100 to be stored in Memory. Inasmuch as the read-in was normal up to and past the input circuits, no error circuits are alerted during the Read Cycle. Memory location 1 is thus connected to Print Location 1.

During the succeeding Probe Memory operation, the set output of DF3, by way of G47, detects the stored information in Memory location 1, and is channeled by plugboard connection to the control grids of Print location 1.

The recovery of DF4 fires the check tube in Print location 1, which alerts the Print tube.

The recovery of DF3 commences a Print signal, and after elimination of the first Index pulse, the printing operation begins. As the information which is stored in Memory location 1 is a non-printable combination as noted previously, an equality in comparison cannot be accomplished during the following Probe Code Generator phase. Further enables are not received at the control grids of Print location 1, so that the Print tube will not be fired during the Cycle. At the end of the Print Cycle, the recovery of DF2 occurs, but the All-Out signal is not present, therefore the signal is channeled by way of G51 to the Print Error circuits. The machine stops with the PRINT CHECK neon light on, and moving the carriage outwards will show the vacant print location. By observing the associated Memory location the non-printable combination will be noted.

Example 2:

In this instance the Memory fills normally. However, the Probe Memory section of the Comparator connected with Memory location 1 fails to operate. Memory location 1 contains a Character "A", and is connected to Print location 1.

During the Probe Memory operation, Memory location 1 is sampled, and erroneously shows no output, resulting in a lack of an enable to the control grid of Print location 1, and consequently the Check tube does not fire. During the Print Cycle, the coded combination for the character senses an agreement with the coded combination stored in Memory location 1, and an output is therefore channeled by way of the plugboard connection to Print location 1. This places an enabling voltage level on the control grids of the Print tube. As the Check tube is in a non-conducting state, the Print tube is incapable of firing even with the comparison signal present on the control grid, thus the Index pulse for "A", when sampling the screen grid, is unable to cause the Print tube to fire. Thirty microseconds later, the delayed Index pulse from DF19 samples the screen grid of the Check tube which has an enable, and thus the Check tube is fired. During the comparison for even print locations, the grid level is again increased, but as an Index pulse is not available, the Print tube is unable to fire. As no further comparisons occur with the character in Memory location 1, the Print Cycle ends with the Print tube remaining not fired and the Check tube conducting, thus developing a Print Error.

This particular type of error is recognizable by initiating the following fault-determining procedure. The information may be left in Memory by actuating the SINGLE LINE switch and then the START switch. The ensuing print-out should terminate with no error being shown. Again actuating the START switch will result in a print-out, but this time followed by a Print Error. Each alternate line printed will develop a Print Error. The Check tube will be fired during the comparison on one cycle, and extinguished by the firing of the Print tube in the succeeding cycle.

Example 3:

In this example it is considered that the Memory fills normally and Memory location 1 contains the character "A" and is connected to Print

location 1. The Probe Memory circuit is operating normally, but during the Probe Memory phase of operation a transient noise pulse fires the Print tube.

When DF4 recovers, the Check tube in Print location 1 fires, which places a partial level on the screen of the Print tube. During the 50 μ sec period that the enable remains on the control grid of the Print tube, a noise pulse arrives at the screen grid of this tube, causing the tube to ignite and placing the Check tube in a non-conducting state. During the odd comparison for the character "A", the control grids of the Print tubes are again enabled, but due to the Print tube lacking plate voltage and an enable on the screen grid (Check tube off), it is unable to fire.

The delayed Index pulse samples the Check tube, which is enabled, thus causing the Check tube to again fire. However, as the Print tube is incapable of firing, the Print cycle ends. The Check tube remains conducting, and a Print error is developed.

Example 4:

In the following fault condition, the Memory fills in a normal manner. Memory location 1 is connected to Print location 1 and Memory location 2 is connected to Print location 2, with both Memory locations storing the character "A". The Probe Memory phase occurs and the Check tubes in both Print locations 1 and 2 ignite.

During the odd comparison for the character "A", the control grids of Print location 1 and Print location 2 are enabled. The recovery pulse from DF15 is channeled by way of G21, G71 and G22 to the screen grid of the Print tube in Print location 1, which fires in a normal manner. The negative swing in plate potential is coupled by the cross-over capacitor to the plate circuit of the Check tube. The resulting drop in the plate potential of the Check tube, negative with respect to the cathode, extinguishes the tube.

Presume now that a noise pulse which enters the even Index pulse channel, fires the Print tube in Print location 2 in error, with the companion Check tube being extinguished. Thirty microseconds later, DF19 recovers and the resultant pulse samples the screen grids of the odd Check tubes. It will be recalled that the Check tube in Print location 1 has an enable on the control grid; however, the plate of this tube is negative with respect to cathode, and there is no effect from the delayed Index pulse.

The even comparison for the character A occurs 500 μ sec later, which again increases the voltage level on the control grids of Print location 1 and Print location 2 beyond the cut-off point. The even Index pulse samples the Print tube in Print location 2, but the tube is now incapable of firing. The even delayed Index pulse samples the Check tube in Print location 2 thirty microseconds later, and, as the control grid is enabled and the plate potential having reached a firing level, the Check tube again is placed in a conductive state.

As the Print tube is incapable of firing, the Print Cycle ends with the Check tube in a conducting state, and a Print Error being developed by the

recovery of DF2. Figure 2-36, Check Thyatron Voltage Curve, illustrates the plate-voltage curve of the Check thyatron, which indicates the arrival of both the odd and even delayed Index pulses.

The printed output in this instance will indicate a character "A" in Print location 1, and a possible ink smudge in Print location 2.

Example 5:

The Memory fills in a normal manner in this fault example, and all Print locations are also in a normal state. The hypothetical fault in this instance is the failure of grid-bias supply to the output circuits during the Read Cycle. This causes an inhibition on G49, and relays RE1 and RE2 consequently lose actuating current. As the charging-voltage source to the actuator capacitors is removed prior to the capacitors receiving sufficient charge, the Print Cycle commences with the Print tubes lacking a supply voltage.

The Probe Memory phase occurs in a normal manner, but, inasmuch as the Print tubes lack plate voltage as mentioned, these tubes are not capable of firing, and the Print Cycle is completed with the major portion of the Check tubes conducting. A Print Error is consequently developed. The visual indication of this type of fault is the large quantity of conducting Check tubes together with a lack of printed information.

Example 6:

In the final example given here, the Memory and Print circuits are normal, but due to possible component failure, DF19 is not operating. Under these circumstances the Probe Memory operation will occur in a normal manner, but during the Print Cycle, DF9 will receive a set pulse from the even delayed Index pulses only. It will be observed that one revolution of the typewheel will place the Memory counter on a count of 51 only, causing the Print Cycle to continue for another revolution.

All Print tubes will fire normally during the initial typewheel revolution, and all Check tubes will be extinguished. As the second sweep of comparisons occur, the even delayed Index pulses re-ignite all Check tubes in the even Print locations, which receive an enable to the control grids. Upon completion of the second revolution of the typewheel, the counter will step to a binary count of 102, with the output of G6 setting DF2 and thus ending the Print Cycle by way of the circuitry involved. Due to the fact that all even Print locations have conducting Check tubes, an All-Out signal will not be present to inhibit G51, and the subsequent recovery pulse of DF2 will pass G51 to produce a Print Error signal.

The visual indication of this fault may be recognized by the fact that all odd or all even Check tubes will be ignited in addition to the PRINT CHECK neon (assuming that all Memory locations are storing information).

h. ALL-OUT DETECTOR ERROR. - The All-Out Detector check insures that the All-Out circuit is functioning correctly. Should this not be satisfactory, the Printer will stop and the A.O. DET CHECK neon lamp will indicate a fault. The failure of the All-Out Detector will produce a spurious All-Out Detector

signal, whether a Check tube is, or is not, conducting. In order that this type of fault may be recognized, certain circuits perform a check on the All-Out Detector during each Probe Memory operation. If the All-Out Detector is operating normally, the Trailing Edge of the Probe Memory pulse produces a Print signal. In the case where the All-Out Detector is not operating correctly, the Trailing Edge will not produce a Print signal, and the Printer will stop. This type of error will be recognizable by the indication of all error and stop lights being off with the exception of the A.O. DET CHECK indicator. The counter will indicate 121. (Normally the All-Out Check indicator will be on except during a Print check.)

The All-Out signal passes to G57 as an inhibition, and failure of the All-Out Detector will result in a steady-state inhibition to G57. Should the All-Out Detector fail, the first Probe Memory operation following this failure will result in the Printer stopping at the end of the Probe Memory operation, due to G57 preventing the set signal to FF20 from developing the Print signal through G21, etc.

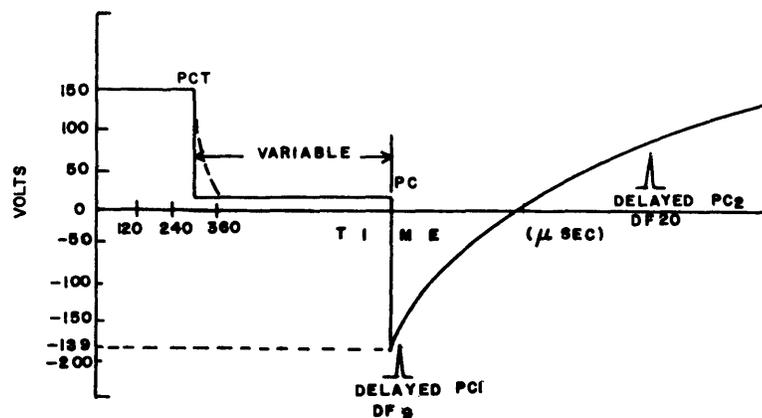


Figure 2-36. Check Thyatron Plate Voltage Curve

TABLE 1
UNIVAC® CODE FOR THE HIGH-SPEED PRINTER

CHARACTER	CODE			COMPUTER DIGIT	CHARACTER	CODE			COMPUTER DIGIT
	CHECK PULSE	ZONE	BODY			CHECK PULSE	ZONE	BODY	
i	1	00	0000	5	t	0	10	0000	N
Δ	0	00	0001	6	t	1	10	0001	O
-	0	00	0010		l	1	10	0010	P
0	1	00	0011)	0	10	0011	
1	0	00	0100		J	1	10	0100	
2	1	00	0101		K	0	10	0101	
3	1	00	0110		L	0	10	0110	
4	0	00	0111		M	1	10	0111	
5	0	00	1000		N	1	10	1000	
6	1	00	1001		O	0	10	1001	
7	1	00	1010		P	0	10	1010	
8	0	00	1011		Q	1	10	1011	
9	1	00	1100		R	0	10	1100	
,	0	00	1101		\$	1	10	1101	
&	0	00	1110		*	1	10	1110	
(1	00	1111		(FFIII)?	0	10	1111	M
ML r	0	01	0000	E	(STOP) Σ	1	11	0000	V
,	1	01	0001		(BP) β	0	11	0001	W
.	1	01	0010		:	0	11	0010	
;	0	01	0011		+	1	11	0011	
A	1	01	0100		/	0	11	0100	
B	0	01	0101		S	1	11	0101	
C	0	01	0110		T	1	11	0110	
D	1	01	0111		U	0	11	0111	
E	1	01	1000		V	0	11	1000	
F	0	01	1001		W	1	11	1001	
G	0	01	1010		X	1	11	1010	
H	1	01	1011		Y	0	11	1011	
I	0	01	1100		Z	1	11	1100	
#	1	01	1101		%	0	11	1101	
¢	1	01	1110	C	(FFIV) =	0	11	1110	T
(FF I) @	0	01	1111	D	(UNUSED)	1	11	1111	

NOTE: Non-printable symbols are indicated in the "character" column by a double block. The corresponding Computer Digit symbols are listed in the "Computer Digit" column.

**TABLE 2
SUPERVISORY CONTROL PANEL FUNCTIONS
HIGH-SPEED PRINTER**

CONTROL	POSITION	FUNCTION	CONDITION
WARNING BELL/OUT (SC32) REWIND (SC7)	WARNING BELL (non-locking)	Rings warning bell (Early warning thermostat also rings bell if temperature in Memory or power supply units exceeds pre-determined limit.)	
	OUT (locking)	Disconnects warning bell.	
	REWIND (Non-locking) NEUTRAL	Rewinds Uniservo to beginning of tape; prevents operation of START and INITIAL switches. Switch must be returned to neutral before Printer may be started again. Stops Uniservo if rewind is in progress. As the Uniservo generally stops the tape in the middle of a blockette, it is usually necessary to perform a Read (one-blockette) Forward or Read (one blockette) Backward operation for synchronization. Permits operation of START and INITIAL switches.	
HOME PAPER/TAPE LOAD (SC11/SC12)	HOME PAPER (locking)	Feeds paper until a hole is sensed in Channel 7 of the paper loop, locating the beginning of a form. Prevents operation of START (SC1) and INITIAL START (SC2) switches.	Machine must contain a paper loop punched in Channel 7; CONTROL LOOP switch must be raised.
	TAPE LOAD (locking)	Feeds 115 inches of tape leader past the Read Head, then stops tape feed. Prevents operation of START (SC1) and INITIAL START (SC2) switches.	
	Neutral	Permits operation of START (SC1) and INITIAL START (SC2) switches.	
INITIAL/SINGLE LINE (SC2)	INITIAL (Non-Locking)	Reads new blockette into Memory and commences printing operation.	Precede with GENERAL CLEAR signal REWIND (SC7), HOME PAPER (SC11), and TAPE LOAD (SC12) switches must be in neutral position.

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TABLE 2 CONTINUED

CONTROL	POSITION	FUNCTION	CONDITION
BREAKPOINT (SC3)	Neutral	Printer operates continuously when START switch is actuated. Printing starts with blockette currently in Memory. If Memory is initially empty, no output appears with the first Print Cycle, but the paper is spaced.	START switch engaged momentarily. Memory previously filled. START switch actuated momentarily.
	SINGLE LINE (locking)	Each time the START switch is actuated, the Printer prints the contents of the Memory and stops, without clearing the Memory. The sequence is repeated each time the switch is moved to START.	
	BREAKPOINT (locking)	Printer stops whenever a Breakpoint symbol (0 11 0001) is read from the tape.	
COMPUTER DIGIT (SC17)	Neutral	Ignores Breakpoint symbols on the tape.	
	COMPUTER DIGIT (locking)	With the INITIAL switch actuated, Printer prints two lines: the first contains only the normal characters; the second contains only the Computer Digit print-out symbols for all non-printable symbols in the blockette. (See Table 1 for list of print-out symbols). The Printer will not perform a Multiline or tape-initiated Fast-Feed.	
PRINT NO READ/READ NO PRINT (SC8/SC9)	Neutral	Non-printable combinations are not printed.	
	<p data-bbox="558 1195 810 1308">PRINT NO READ (locking)</p> <p data-bbox="558 1308 810 1547">READ NO PRINT (locking)</p>	<p data-bbox="810 1195 1440 1308">Prints contents of Memory repeatedly. Tape does not advance.</p> <p data-bbox="810 1308 1440 1547">Reads blockette into Memory, checks the blockette, then clears Memory. No printing occurs and paper does not move. Checking of tape blockette-by-blockette continues until:</p> <ol data-bbox="810 1438 1440 1547" style="list-style-type: none"> (1) Odd-Even or 120 Error occurs, (2) Stop or Breakpoint symbol encountered, (3) STOP switch is actuated. 	

TABLE 2 CONTINUED

CONTROL	POSITION	FUNCTION	CONDITION
START/STOP (SC1)	START (non-locking)	<p>(4) Tape is exhausted.</p> <p>In all cases, the Printer stops, with the Memory containing the last blockette entered. The Printer will not perform a Multiline or Fast-Feed operation.</p> <p>Printer operates as above except that in addition, operation stops also when a Fast-Feed I symbol is encountered. This operation is useful for repositioning tape to correspond to the beginning of a new paper form.</p> <p>Starts the Printer in whatever mode of operation has been selected.</p> <p>Starts continuous operation. Printing starts with blockette currently in Memory. If Memory is initially empty, nothing is printed in the first printing cycle, but the paper is spaced. Prints the contents of the Memory and stops, without clearing the Memory.</p> <p>Prints contents of Memory repeatedly. Tape does not advance.</p> <p>Reads blockette into Memory, checks blockette, then clears Memory; no printing occurs and paper does not move.</p> <p>Checking of tape blockette-by-blockette continues until:</p> <ol style="list-style-type: none"> (1) Odd-Even or 120 Error occurs, (2) Stop or Breakpoint symbol encountered, (3) STOP switch is actuated, (4) Tape is exhausted. <p>In all cases, the Printer stops with the Memory containing the last blockette entered. Printer will not perform a Multiline or Fast-Feed operation.</p>	<p>READ FORWARD/READ BACKWARD switch in either position, START/STOP switch in neutral position.</p> <p>INITIAL/SINGLE LINE switch in Neutral position.</p> <p>SINGLE LINE switch actuated.</p> <p>PRINT NO READ switch actuated, Memory previously filled.</p>

TABLE 2 CONTINUED

CONTROL	POSITION	FUNCTION	CONDITION
<p>READ FORWARD/READ BACKWARD (SC5/SC6)</p>	<p>STOP (non-locking)</p>	<p>Stops the Printer upon completion of the current or next reading process, retaining the information in the Memory.</p> <p>Stops the Printer upon completion of a print-out, retaining the information in the Memory.</p>	<p>PRINT NO READ/READ NO PRINT switch in READ NO PRINT or neutral position.</p> <p>PRINT NO READ switch actuated.</p>
	<p>READ FORWARD (locking)</p>	<p>After a pause of approximately one second, the tape moves forward, and one blockette is read into Memory in a forward direction. The process is also known as a "Manual Read" operation, and may be repeated by returning the switch to neutral, pausing momentarily, and again placing the switch in READ FORWARD. Fast-Feed symbols are ignored except for a Fast-Feed symbol occurring with the Test Control panel F.F. ON M.R. switch actuated.</p> <p>A Multiline symbol is not ignored; but prepares the Printer for a Multiline operation.</p> <p>Reads blockette into Memory, checks blockette, then clears Memory; no printing occurs and paper does not move.</p> <p>Checking of tape blockette-by-blockette continues until:</p> <ol style="list-style-type: none"> (1) Odd-Even or 120 Error occurs, (2) Stop, Breakpoint, or Fast-Feed I symbol appears, (3) STOP switch is actuated, (4) Tape is exhausted, <p>In all cases, the Printer stops with the Memory containing the last blockette entered. The Printer will not perform a Multiline operation.</p>	<p>PRINT NO READ/READ NO PRINT switch neutral or in PRINT NO READ position. (In these positions, switch has no effect on the Read Forward operation).</p> <p>READ NO PRINT switch actuated.</p>
	<p>READ BACKWARD (locking)</p>	<p>Operates the same as in the READ FORWARD position, except that the tape is read backward, and the Test Control panel F.F. ON M.R. switch has no effect.</p>	

TABLE 2 CONTINUED

CONTROL	POSITION	FUNCTION	CONDITION
HIGH GAIN/LOW GAIN (SC28)	Neutral	Adjusts the sensitivity of the input circuits to the normal value. Neutral is the normal position of the switch.	
	HIGH GAIN (locking)	Increases sensitivity of the input circuits. Operation in this position is attempted when tape-reading errors are occurring with the switch in the neutral position.	
	LOW GAIN (locking)	Decreases sensitivity of the input circuits. Operation in this position is attempted when tape-reading errors are occurring with the switch in the neutral position.	
CARRIAGE IN/CARRIAGE OUT (SC29)	CARRIAGE IN (locking)	Places the carriage in printing position. Limit switches open the power circuit to the motor when carriage has reached the end of travel (or when an obstruction impedes the motion of the carriage). Switch need not be returned to Neutral. The Printer will not operate if the carriage is not fully in; an attempt to print under this condition produces a Print Check error on the first line, stopping the Printer.	
	CARRIAGE OUT (locking)	Runs the carriage out from the Print Head. Limit switches open the motor circuit when the carriage has reached the end of travel (or when an obstruction impedes the motion of the carriage). The carriage is run-out to change paper, change ribbon, or to view the last few lines printed. All tape-reading operations may be performed with the carriage out.	
SPACE PAPER (SC26)	SPACE PAPER (non-locking)	Spaces paper one unit (single-, double-, or triple-space as selected on the plugboard). The contents of the Memory (if any) are retained.	

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TABLE 2 CONTINUED

CONTROL	POSITION	FUNCTION	CONDITION
GENERAL CLEAR (SC24)	GENERAL CLEAR (non-locking)	Restores all flip-flops except FF21, clears Memory, clears the Main Counter. A General Clear routine occurs automatically when DC ON is actuated.	PRINT NO READ/READ NO PRINT switch in Neutral position.

**TABLE 3
TEST CONTROL PANEL FUNCTIONS
HIGH-SPEED PRINTER**

CONTROL	POSITION	FUNCTION	CONDITION
INPUT FLIP FLOPS (TC15A, B, C, D, E, F, G)	Raised (Non-locking)	Sets the associated Input flip-flop. Lights the associated Test Control Panel INPUT FLIP FLOPS indicator.	
	Lowered (non-locking)	Restores the associated Input flip-flop. Extinguishes the associated Test Control Panel INPUT FLIP FLOPS indicator.	
	Neutral	No effect on associated Input flip-flop.	
MAIN COUNTER (TC16A, B, C, D, E, F, G)	Raised (Non-locking)	Sets the associated main counter stage. Lights the associated Test Control Panel and Supervisory Control Panel MAIN COUNTER indicators.	
	Lowered (Non-locking)	Restores the associated Main Counter stage. Extinguishes the associated Test Control Panel and Supervisory Control Panel MAIN COUNTER indicators.	
	Neutral	No effect on associated Main Counter stage.	
MOTORS TEST/MOTORS NORMAL (TC10)	MOTORS TEST	Connects the cooling motors to the primary power, the motor on-off function being then controlled by the AC ON switch.	
	MOTORS NORMAL	Connects the cooling motors to the secondary power, the on-off function being controlled by the DC ON switch.	
DELETE PRINT CHECK (TC18)	DELETE PRINT CHECK (locking)	Disables Print Error Detector.	
DELETE 120 CHECK (TC19)	DELETE 120 CHECK (locking)	Disables Greater-Than-120 or Less-Than-120 Error detector.	
DELETE O.E. CHECK (TC20)	DELETE O.E. CHECK (locking)	Disables Odd-Even Error detector.	
DELETE ADDRESS CHECK (TC21)	DELETE ADDRESS CHECK (locking)	Disables Address Line Error detector.	

TABLE 3 CONTINUED

CONTROL	POSITION	FUNCTION	CONDITION
HOLD MULTILINE (TC27)	HOLD MULTILINE (locking)	Initiates continuous repeating sequence of a Multiline operation followed by a Single Line operation. The contents of Memory remain unchanged, the same information being printed repeatedly. Printer stops.	Memory initially filled; Supervisory Control Panel START switch momentarily actuated. Supervisory Control Panel STOP switch actuated momentarily while Hold Multiline operation is in progress.
F.F. ON M.R. (TC25)	Neutral	Printer returns to mode of operation selected on Supervisory Control Panel.	Hold Multiline operation in progress.
	F.F. ON M.R. (locking)	Printer observes fast-feed symbols during a Read Forward operation.	Supervisory Control Panel READ FORWARD switch actuated.
	Neutral	Printer ignores fast-feed symbols during a Read Forward operation.	Supervisory Control Panel READ FORWARD switch actuated.
MANUAL FILL (TC13)	MANUAL FILL (locking)	Disables the Not-Reading circuits, allowing manual address selection and read-in to the Memory.	MANUAL FILL switch actuated.
STEP MAIN COUNTER (TC14)	STEP MAIN COUNTER (Non-locking)	Initiates one Manual Read-in Cycle; character sent into Input flip-flops is stored in the Memory location selected on the Main Counter.	Memory address selected by MAIN COUNTER switches, input character selected by INPUT FLIP FLOPS switches.
FAULT TEST/GENERAL CLEAR (TC31)	FAULT TEST (Non-Locking)	Indicates the type and location of a blown fuse.	
	GENERAL CLEAR (Non-Locking)	Generates a General Clear signal, restoring all flip-flops except FF21, clearing Memory, and clearing the Main Counter.	

TABLE 4
HIGH-SPEED PRINTER
DELAY FLIP-FLOPS

DF	Delay Period	Function
1	2.5 msec	Prevents center drive from moving prior to 2,5 msec following RS signal. Permits de-ionization to occur before leading edge of a blockette crosses Read Head. In addition, if brake is applied, 2.5 msec must elapse before clutch may again be engaged.
2	3.0 msec	Prevents CC signal from removing inhibition from G31 prior to de-ionization of Print thyatron tubes. If this delay was not introduced the Print thyatron plate circuit would be corrected to +600 volts upon removal of the inhibition, thus causing a severe overload.
3	300 μ sec	(Probe Memory Timer). Leading edge (P') of Start Print signal sets DF3. The 300 μ sec voltage level probes Memory by way of G47. Differentiated set output sets DF4 and differentiated restored output through G57 sets FF20, generating the P-PM signal.
4	250 μ sec	(Check Thyatron Timer). Set by set output of DF3. Following a 250 μ sec delay, check tubes are fired that are associated with Memory locations storing information. Delay permits Comparator transformer to reach optimum output.
5	0.8 sec	Triggered by SC5, SC6 and SC7. Set output produces Manual Read signal. Restored output produces MRS signal and RS signal. Provides time for servo-loops to balance when a reverse operation initiated, preventing breaking of tape.
6	1.15 sec	Triggered by SC12, set output supplies RS signal to center drive. Restored output restores center drive by removing inhibition from G50. Provides for indexing the first blockette of a new tape.

TABLE 4 (continued)

7	10 msec	(Paper Stop Stabilizer). Insures that paper is stopped and stabilized before print operation can commence. Triggered by an End Paper Feed from FF4, Initial Start or Start. Restore output sets FF12, which supplies one permissive to G17, Start Print Gate.
8	333 msec	Triggered by Manual Stop, Out of Paper, Out of Tape, or Out of Ribbon Signals. Enable is placed on G18 for duration of delay period. G18 inhibited during the Print Cycle to insure that machine cannot be stopped in the middle of Print Cycle. DF8 sustains Stop signals until G18 fully enabled at end of Print Cycle.
DF9	29.9 μ sec	Triggered by SP ₁ pulses from the delay line, PC, PC', or PCT pulses. Set output enables Input for duration of delay period. Restored output steps main counter, restores Input flip-flops, and FF18.
10	200 μ sec	Triggered by Index pulses from G21. Used in delaying setting of FF16, thus preventing first Index pulse from passing Gates 22 and 27. Insures that first set output from DF16 following P-PM is a 300 μ sec level. Following Print Cycle, restored output enables G6, and produces count 102 to set DF2.
11	50 μ sec	Prevents simultaneous attempt of restore and set to FF5 when Fast-Feed I through IV assumes precedence before Fast-Feed V.
12	5.5 msec	Switches plate supply for Memory tubes from +213 volts to +55 volts, thus permitting tubes to de-ionize. Also produces NR signal.
13	100 μ sec	Prevents a Channel 5 signal from setting FF6E until FF5 is set, at the commencement of Fast-Feed I through IV command during 50 μ sec delay.
14	20 msec	Provides time for center drive to stabilize between stopping and starting during a Read, No-Print operation.

TABLE 4 (continued)

15	250 μ sec	Permits output of Comparator to reach an optimum condition during P-PM prior to sampling of Print thyratrons by an Index pulse.
16	300 μ sec	Set output probes output gates of Code Wheel counter and Comparator for duration of delay, and steps BC2. Reset side enables the Skip Gates, G54, G55 and G56.
17	20 msec	If Bad Spot encountered at end of tape-load operation, Restored side of DF17 sets center drive flip-flop FF3. Center drive is restored at end of Bad Spot by removal of inhibition on G50.
19 20	30 μ sec	Delays the PC and PC [*] signals until plate voltage has dropped below ionization point during normal operation. If Print thyatron has been fired during Probe Memory, the restored outputs of these delay flip-flops will refire the Check tubes during P-PM, indicating the error.
21	5 msec	Inhibits G63 at start of Print Cycle to permit FF21 and G31 to stabilize, thus preventing false Charge Error signal.
22	20 msec	Multiline Time Out delay-flop. Output inhibits G17, preventing Print Cycle from occurring for 20 msec delay period. Differentiated output also produces Step Multiline pulse for ring counter, set signal for FF15.
23	20 msec	Recirculation Delay flip-flop. Provides same action as DF22 but is actuated by TC27 Hold Multiline switch or the output of G35. Prevents an ML symbol from being ignored during read-in.
24	50 msec	Step Line Counter delay-flop. Causes line counter to be actuated each time a Print Cycle occurs. Will not be set unless G30 fully enabled.
25	750 μ sec	Fast Charge delay flop, set by Start Paper Feed signal via FF4. Provides delay for complete de-energization of brake solenoid (paper brake) prior to triggering brake actuating fast-charge circuit.

TABLE 4 (continued)

RETRIGGERABLE DELAY FLIP-FLOPS		
1	400 μ sec	Insures that all information in blockette has passed Read Head prior to stopping of center drive, (in the event of a Greater-Than-120 error).
2	50 msec	Prevents information being read from faulty portion of tape by inhibiting G1.
3	50 msec	Ribbon Feed Control. Provides enable to G29, being set at the time FF20 is set and remaining so for entire Print Cycle plus 50 msec.
4	1 sec	In the event of failure of Paper Stop circuits during normal paper spacing, or during Fast-Feed, prevents feeding of more than 22 inches of paper at one time by resetting FF4.

TABLE 5
HIGH-SPEED PRINTER
CONTROL SWITCHES

(Note: SC-designated switches are located at the Supervisory Control panel, TC-switches are located at the Test Control panel unless otherwise designated).

SWITCH	SYMBOL	SECTION OR CHASSIS NO.
AC ON OFF	SC22 SC22	Power Control
DC ON OFF	SC23 SC23	Power Control Power Control
GENERAL CLEAR	SC24-D1-2	Power Control
F.F. ON M.R.	TC25-D1-2 TC25-D3-4 TC25-C1-2	P2G P3G P4H
SPACE PAPER	SC26-D1-2	P8G
HOLD MULTILINE	TC27-D1-2 TC27-D3-4	P9L P4H
HIGH GAIN LOW GAIN	SC28-D1-2 SC28-B1-2	P1H - P1G P1H - P1G
CARRIAGE IN CARRIAGE OUT	SC29-B1-2 SC29-D1-2	Power Control Power Control
CONTROL LOOP	SC30 SC30	Power Control
SET MAIN COUNTER	TC16A-D1-2 TC16A-B1-2 TC16B-D1-2 TC16B-B1-2 TC16C-D1-2 TC16C-B1-2 TC16D-D1-2 TC16D-B1-2 TC16E-D1-2 TC16E-B1-2 TC16F-D1-2 TC16F-B1-2 TC16G-D1-2 TC16G-B1-2	P1L P1L P1L P1L P1L P1L P1L P1L P1L P1L P1L P1L P1L P1L

SWITCH	SYMBOL	SECTION OR CHASSIS NO.
REWIND	SC7-C1-2 SC7-C3-4 SC7-C5-6 SC7-D1-2 SC7-D3-4 SC7-D5-6 SC7-D7-8 SC7- SC7-	P7G P4G P1G P5G P7G P8G P5G P4G
PRINT NO READ	SC8-D1-2	P7G
READ NO PRINT	SC9-A1-2 SC9-A3-4 SC9-A5-6 SC9-A7-8 SC9-B1-2 SC9-B3-4 SC9-B5-6 SC9-B7-8 SC9-B9-10	P4H P3G P2G P2G P2G P8G P9G P8G P7G
MOTORS ON OFF	TC10	Power Control
HOME PAPER	SC11-C1-2 SC11-C3-4 SC11-D1-2 SC11-D3-4 SC11 SC11	P3G P3G P8G P2G P2G P7G
START	SC1-D1-2 SC1-D3-4 SC1-D5-6	P7G P2G P7G
INITIAL CONT SINGLE LINE	SC-2-D1-2 SC2-B1-2 SC2-B3-4	P7G P5G P8G
BREAK POINT	SC3-D1-2	P4H
STOP	SC4-B1-2	P8G
READ FORWARD	SC5-C1-2 SC5-C3-4 SC5-D1-2 SC5-D3-4 SC5-	P4H P3G P2G P5G P8G

SWITCH	SYMBOL	SECTION OR CHASSIS NO.
TAPE LOAD	SC12-A1-2 SC12-A3-4 SC12-B1-2 SC12-B3-4 SC12-B5-6 SC12 SC12	P4G P5G P5G P5G P1G
MANUAL FILL	TC13-D1-2 TC13-D3-4	P4G P5G
STEP MAIN COUNTER	TC14-D1-2	P6G
SET INPUT FF	TC15A-D1-2 TC15A-B1-2 TC15B-D1-2 TC15B-B1-2 TC15C-D1-2 TC15C-B1-2 TC15D-D1-2 TC15D-B1-2 TC15E-D1-2 TC15E-B1-2 TC15F-D1-2 TC15F-B1-2 TC15G-D1-2 TC15G-B1-2	P2H P2H P2H P2H P2H P2H P2H P2H P2H P2H P2H P2H P2H P2H
COMPUTER DIGIT	SC17-C1-2 SC17-C3-4 SC17-C5-6-7 SC17-C8-9 SC17-C10-11 SC17-D1-2 SC17-D3-4 SC17-D5-6 SC17-D7-8 SC17-D9-10	P4H P3G P7G P7H P4H P2G P9L P4H P8G
DELETE PRINT CHECK	TC18-D1-2 TC18-D3-4	P6G P6G
DELETE 120 CHECK	TC19-D1-2 TC19-D3-4	P5G P5G
DELETE OE CHECK	TC20-D1-2	P3G
DELETE ADDRESS CHECK	TC21-D1-2	P9L

SWITCH	SYMBOL	SECTION OR CHASSIS NO.
READ BACKWARD	SC6-A1-2 SC6-A3-4 SC6-A5-6 SC6-B1-2 SC6-B3-4 SC6-B5-6 SC6 SC6	P1G P4H P4G P3G P2G P5G P4H P8G

TABLE 6
HIGH-SPEED PRINTER
RELAY FUNCTIONS

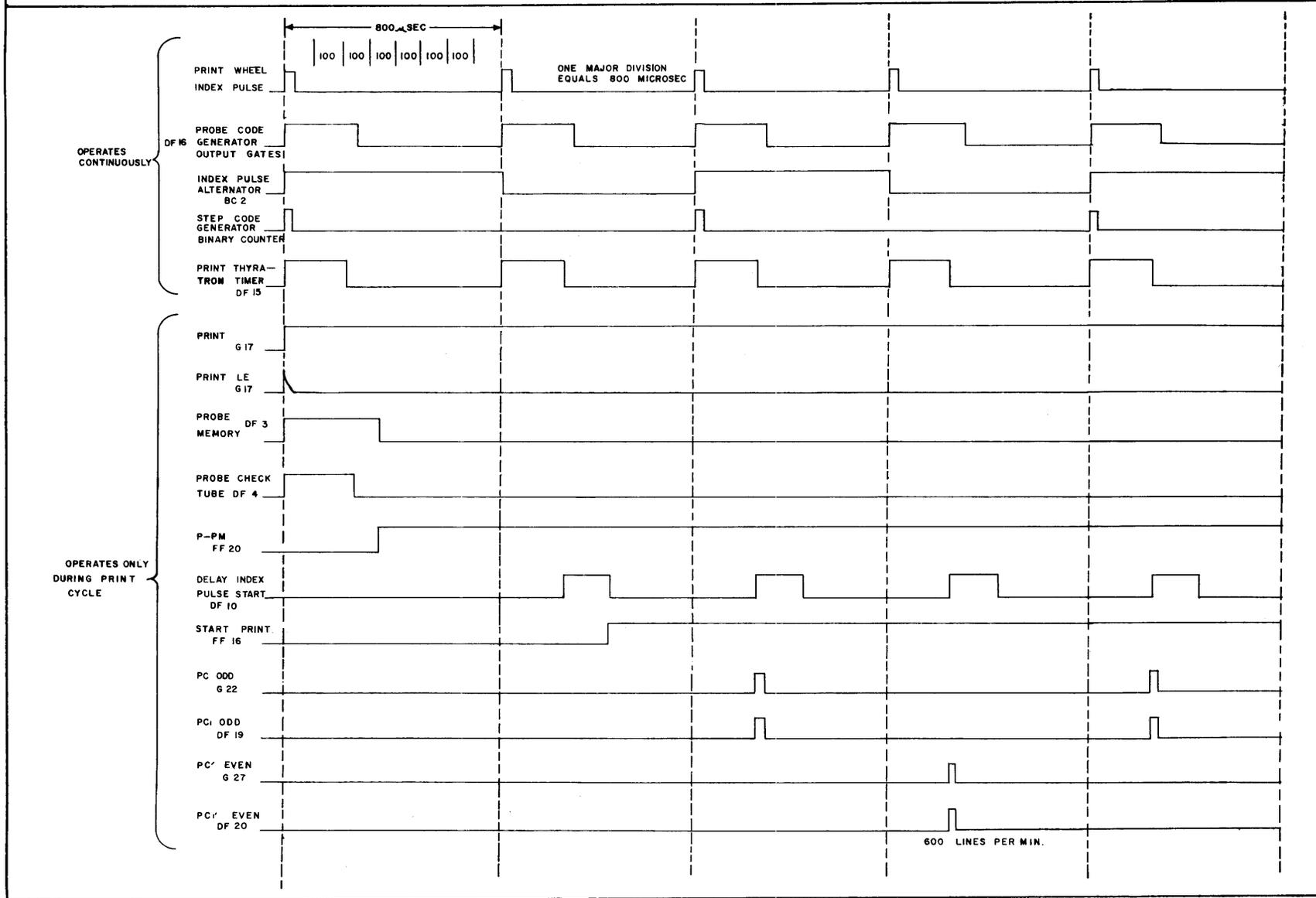
(Note: Relays may have the same designation in different units. It is therefore necessary that this Table be divided into Unit categories).

Relay	Name or Function
A. Printer Unit:	
RE1	When gate G49 enabled, energizes RE2
RE2	When energized by RE1, contacts will apply +600 volts to charge capacitors
RE3	When PF Error occurs, inhibits G17
RE4	Out-of-Paper relay, inhibits G17
B. Memory Cabinet:	
Hayden Timer 1	Thirty-second time delay energized by application of primary a-c. Applies a-c to Hayden Timer 2, and "Slow Heater relay," following delay period.
Hayden Timer 2	Thirty-second time delay energized by Hayden Timer 1. Following delay period, illuminates "DC Ready".
Slow Heater	Applies one-half filament voltage during delay period of Hayden Timer 1.
Gate 34	Removes B+ voltage from Check thyatron tubes.
Multiline (15 relays)	Connected by plugboard for printing in correct locations during ML operation
Single Line (11 relays)	Connected by plugboard for printing in correct locations during SL operation

Relay	Name or Function
C. Power Supply Cabinet: A-C Contactor D-C Contactor V4A PG RE1 RE2 RE3 RE4 RE5 RE6 RE7	 Holding relay for a-c Holding relay for d-c Steps line-counter General Clear line D-C alarm line A-C alarm line Advance A-C alarm Positive alarm Negative alarm
D. Miscellaneous: Early Warning Thermostats Overheat Thermostats Reverse Rewind	 Ring Alarm bell when cabinet temperature reaches 100F Open d-c circuits when cabinet temperature reaches 120F Reverses motor windings Repositions tape

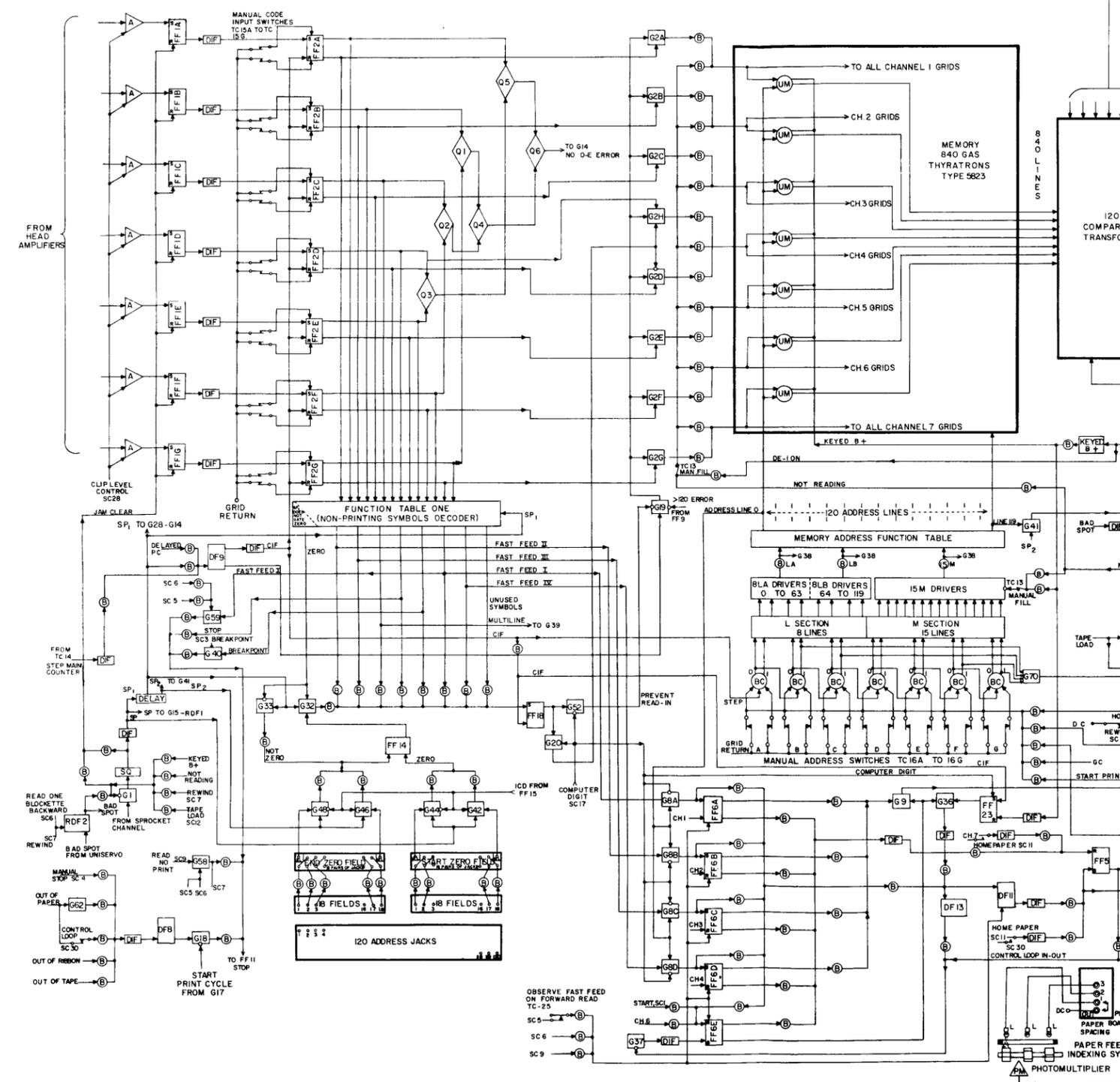
TABLE 7

PRINT CYCLE TIMING - HIGH-SPEED PRINTER

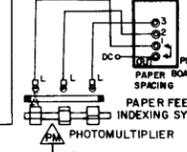


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NOTES
 GENERAL CLEAR RESTORES ALL FLIP-FLOPS EXCEPT FF21
 SC SWITCHES LOCATED ON SUPERVISORY CONTROL PANEL
 TC SWITCHES LOCATED ON TEST CONTROL PANEL
 ← DEMOTES EXTERNAL PLUG-TYPE CONNECTOR



OBSERVE FAST FEED ON FORWARD READ TC-25
 SC 5 →
 SC 6 →
 SC 9 →



NOTES:
 GENERAL CLEAR RESTORES ALL FLIP-FLOPS EXCEPT FF21
 SC SWITCHES LOCATED ON SUPERVISORY CONTROL PANEL
 TC SWITCHES LOCATED ON TEST CONTROL PANEL
 → DEMOTES EXTERNAL PLUG-TYPE CONNECTOR

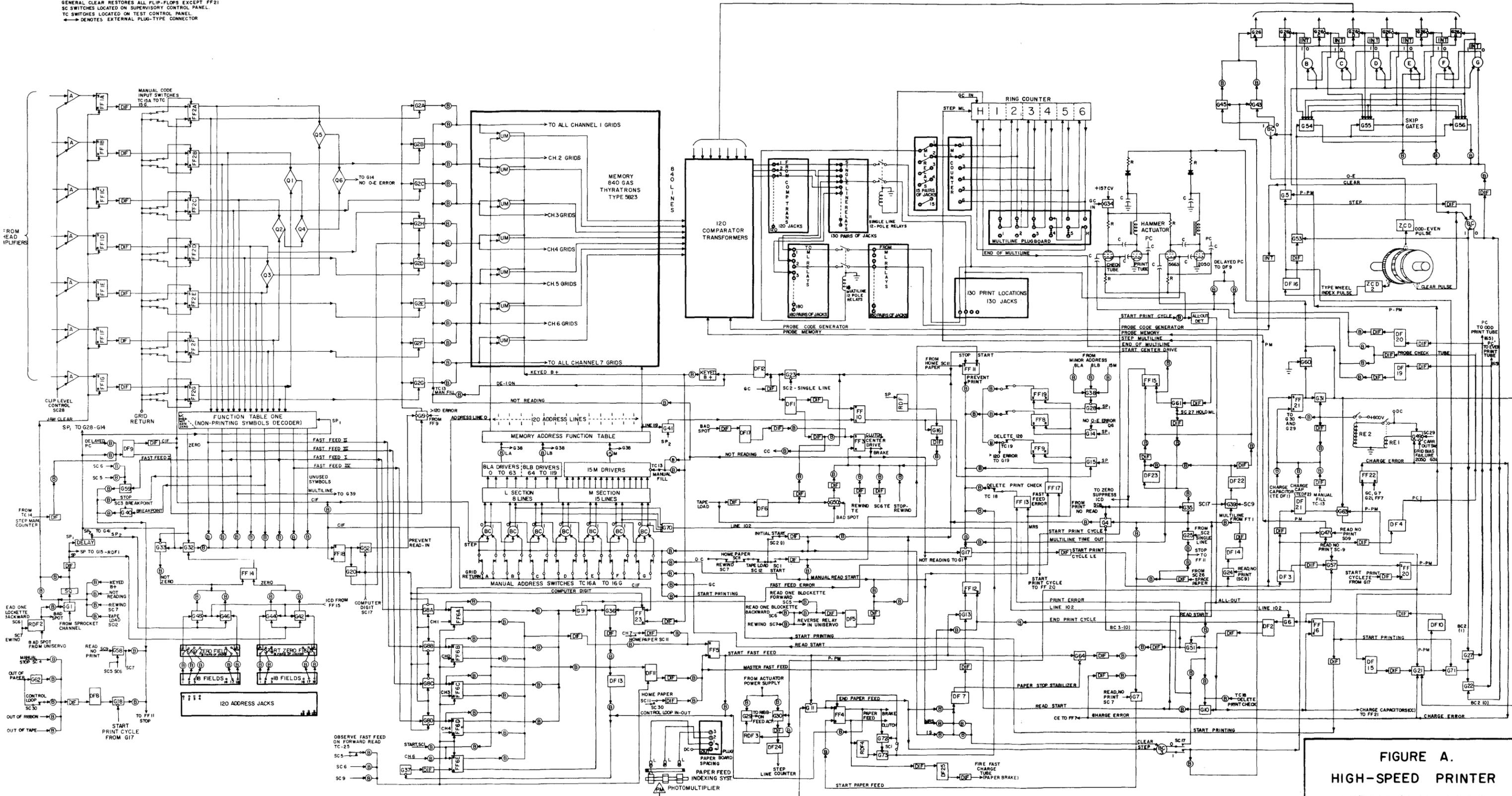


FIGURE A.
 HIGH-SPEED PRINTER
 OPERATIONAL LOGIC