SPERRY UNIVAC

V70 and 77 Series Cache Memory

Operation and Service

Mini-Computer Operations

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Mega Map Option

77-3301	F3026-00	0101938-001	Mega Map Option
		44P0785-000	Mega Map Assy
		44C0785	Mega Map Assy
		91C0569	Logic Diagram
		9809906-272	Mega Map Manual

CHANGE RECORD

Page Number	Issue Date	Change Description
Various	1/78	Deleted all references to Varian.

Change Procedure:

When changes occur to this manual, updated pages are issued to replace the obsolete pages. On each updated page, a vertical line is drawn in the margin to flag each change and a letter is added to the page number. When the manual is revised and completely reprinted, the vertical line and page-number letter are removed.

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SECTION 1
GENERAL DESCRIPTION

This SPERRY UNIVAC V70 Series 660 Nanosecond Semiconductor Memory Manual describes the 660 nanosecond random access memory and its interface with a V70 series computer processor.

The manual is divided into six sections:

- Introduction to the memory and its relation to the system
- Installation and interface information
- Operation
- Theory of Operation
- Maintenance
- Mnemonics list

Documents such as logic diagrams, schematics, and parts lists are supplied in a system documentation package. This package is assembled when the equipment is shipped, and reflects the configuration of a specific system.

The following list contains the part numbers of other manuals pertinent to the V70 series computers (the x at the end of each document number is the revision number and can be any digit 0 through 9:

Title	Document Number
V70 Architecture Manual	98A 9906 00x
Processor Manual	98A 9906 02x
Memory Map Manual	98A 9906 10x
V72/V76 Power Supply Manual	98A 9906 13x
V76 System Reference Manual	98A 9906 23x
Megamap Manual	98A 9906 27x
V77-600 System Reference Manual	98A 9906 40x
MAINTAIN III Manual	98A 9952 07x

The semiconductor memory is a dual-port, expandable, random-access, metal-oxide-semiconductor (MOS) memory that provides data storage for V70 series computers.

The basic memory module has a storage capacity of 16,384 (16K), 32,768 (32K) or 65,536 (64K) computer words of 16 bits each. An 18-bit version includes two parity bits per word (one parity bit per 8-bit byte). In some systems, each of the two 8-bit bytes of the standard 16-bit word can be manipulated independently. Since parity is an optional feature, subsequent references to the memory module in this manual will denote the basic version with the standard 16-bit word length unless otherwise indicated. When addressed with the memory map option, a semiconductor memory system using 64K modules is expandable to 262,144 (256K) words; with a megamap option, expansion to 1,048,576 (1000K) words is possible.

The dual-port access of the 660 nanosecond semiconductor memory module contains two independent sets of memory bus terminals for data entry and retrieval from two different sources, e.g.; main and peripheral processors. In this way, two different processors or one processor and a priority memory access (PMA) option, operating independently, can request access to the memory at virtually the same time. However, when this occurs during a read or write cycle, the processor connected to port B has priority over the port A processor. The processor accessing the memory through port A has no priority during normal read or write operations but can under special circumstances lock out the port B processor. It should be noted, that the previous discussion pertains only to port access priorities and not to memory cycle priorities.

Since the semiconductor memory is volatile and will loose data unless it is periodically refreshed (recharged), the memory refresh cycle has priority over both read and write cycles on either memory port. That is, data already stored in the memory must be refreshed on a precise time schedule before data can be entered or retrieved by any processor. This feature prevents data, already stored in memory, from being lost at any time during memory operation.

Being volatile, the semiconductor memory also loses data if input power is removed. To prevent data from being lost during an input power failure, a battery-powered data-save option can be installed. This data-save option provides the appropriate voltages to the memory refresh logic of up to four 64K memory modules in the system. Each additional four memory modules requires an additional data-save option.

With systems using standard software to address the memory locations of more than 32K words of the semiconductor memory, a memory map option is required for storing data. However, a memory map is not required for addressing memory locations of up to 64K-words with a writable control store option and non-standard software or for addressing memory locations of 32K words or less. When a 660 nanosecond semiconductor memory module contains a capacity below 64K words of addressable memory, the

memory module is said to be depopulated. When a single module is used with memory map, memory requests from the processor are received through the backplane wiring. When memory above 64K is used, memory requests are received through twisted pairs via the map board.

The memory is also designed to operate with an external error correction circuit (ECC) that eliminates data errors resulting from several possible sources. This ECC synchronizes the refresh cycle with the other memory cycles from the backplane or memory map board. When an ECC is used in the system, backplane request lines are bypassed and all memory requests are sent from the error correction board through twisted pairs to the memory. Acknowledgment from the memory is supplied by the error correction circuit and sent directly to the processor.

Table 1-1 lists the specifications of the 660 nanosecond semiconductor memory.

Table 1-1. 660 ns Semiconductor Memory Specifications

Parameter	Specification
Speed (without map)	Cycle time: 660 nanoseconds maximum Access time: 560 nanoseconds maximum
Logic levels (CPU bus)	True: -0.4V to +0.8V dc False: +2.4V to +5.0V dc
Address and control lines	Unidirectional
Data lines	Bidirectional
Word length	16-bit words containing two 8-bit bytes (without parity). Optional 18-bit version with one parity bit per byte.
Capacity	Up to 65,563 (64K) words per module.
Dimensions	Each memory module on a PC board is 15.6 by 19 by 0.587 inches (39.6 by 48.3 by 1.49 cm)
Interconnection	Over signal paths (bus lines) to the processor via one 132-pin connector and three 4-pin connectors

Table 1-1. 660 ns Semiconductor Memory Specifications (continued)

Parameter	Specification
Priority	Memory refresh has first priority over both port A and port B of the dual-port memory. Port B has priority over port A. Port A has no priority but can, under special conditions, lock out port B when required.
Input Power (maximum)	DC Volts / Amperes: Run, Standby, Data Save
	+12±.6/ +20±2: 1.3, 0.7, 0.5
	+5±.25: 0.5, 0.5, 0.0
	+5.2±.25 (memory): 1.6, 1.6, 0.13
Environment	0 to 50 degrees C; 0 to 90 percent relative humidity without condensation
Forced-air cooling (externally supplied)	A minimum of twenty cubic feet per minute of evenly distrubuted air applied crosswise above each memory module

SECTION 2
INSTALLATION

2.1 INSPECTION

The semiconductor memory has been packed and inspected to ensure its arrival in good working order. To prevent damage, take care during unpacking and handling. Check the shipping list to ensure that all equipment has been received. Immediately after unpacking, inspect the equipment for shipping damage. Ascertain that wires and cables are neither loose nor broken, and that hardware is secure. If damage exists:

a. Notify the transportation company.

b. Notify Sperry Univac.

c. Save all packing material.

2.2 PHYSICAL DESCRIPTION

The standard 660 nanosecond semiconductor memory module (figure 2-1) is a 15.6 by 19 by 0.587 inch (39.6 by 48.3 by 1.49 cm) printed circuit (PC) board with a mounted array of up to 256 random access memory (RAM) integrated-circuit (IC) chips and other memory system components. An 18-bit version (with parity) contains 288 IC RAM chips. Each RAM IC is contained in a 16-pin ceramic or plastic dual-in-line package. Figure 2-2 is the block diagram of a single 64K memory module. An expanded memory system block diagram is illustrated in figure 2-3.

2.3 MEMORY CONFIGURATION SWITCH SELECTION

The adaptation of a single 64K 660 nanosecond semiconductor memory module with different computer system configurations is determined by selecting the on/off positions of seven memory configuration switches as shown below:

SW1 ON = Memory acknowledge (YDNMx-) from memory (unless ECC board is used)
SW1 OFF = Memory acknowledge (YDNMx-) from an error correction board

SW2 ON - SW3 OFF = Memory request (MRQYA-) from backplane
SW2 OFF - SW3 ON = Memory request (MRQYA-) from J3 (map)

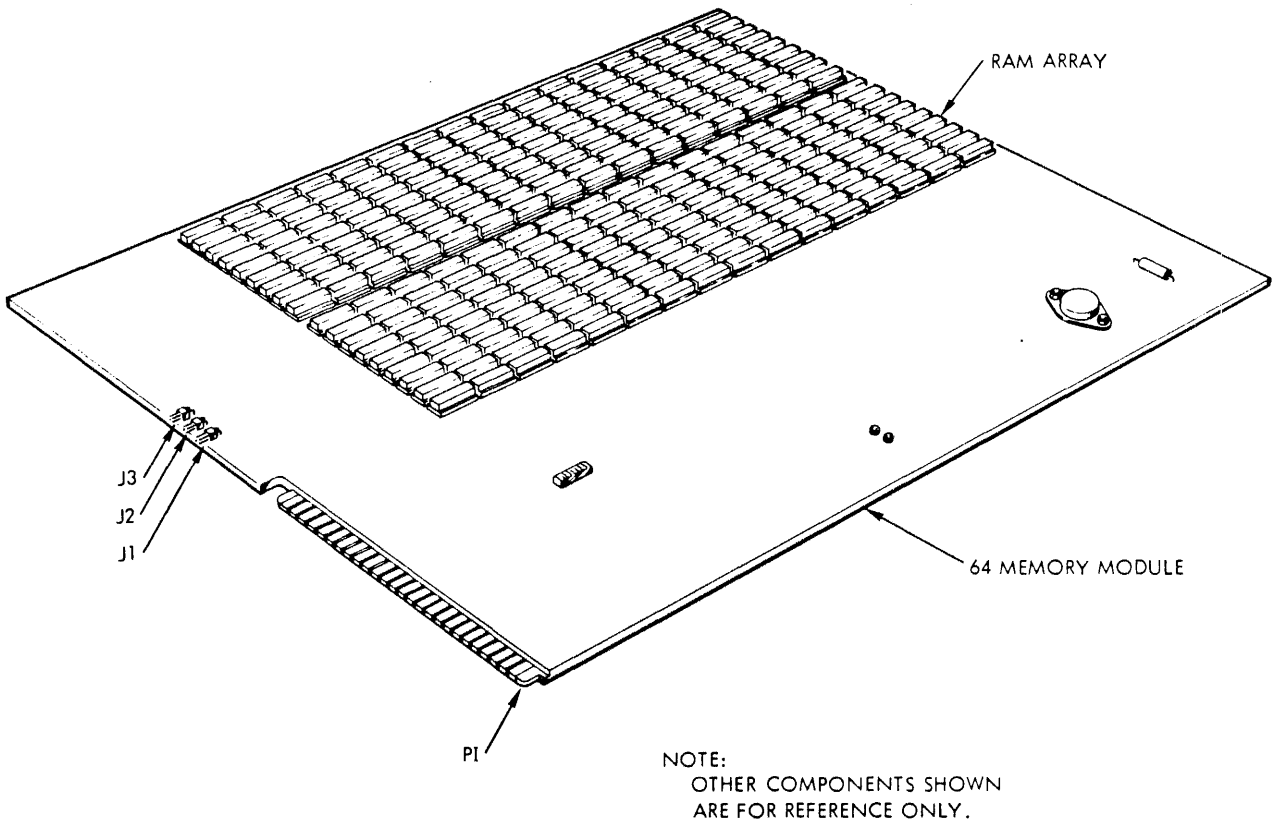

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Figure 2-1. 660 Nanosecond Semiconductor Memory

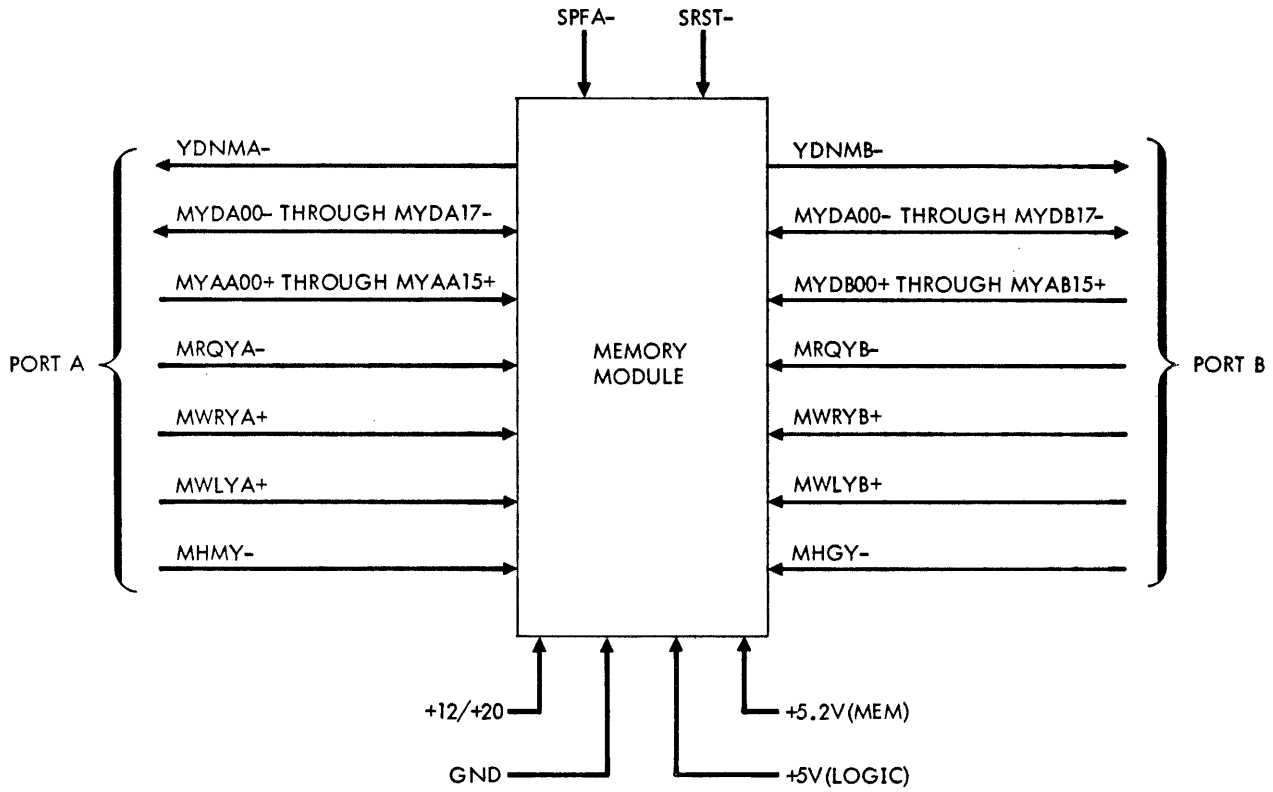

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Figure 2-2. Diagram of Single Memory Module

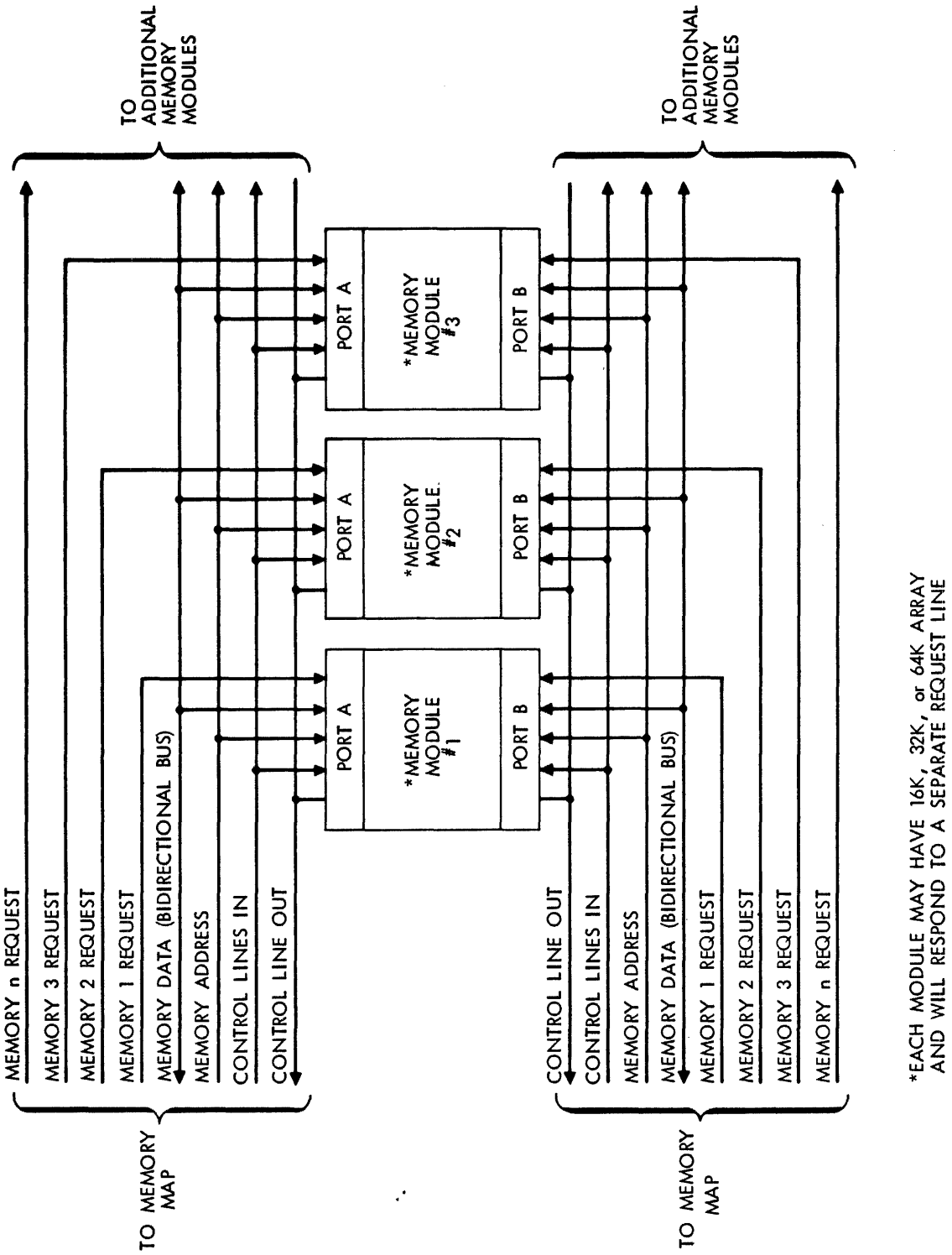

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Figure 2-3. Typical Expanded Memory System

SW4 ON - SW5 OFF = Internal refresh
SW4 OFF - SW5 ON = Refresh request (MRQYR-) from error correction PCB

SW6 ON - SW7 OFF = Refresh request (MRQYB-) from backplane
SW6 OFF - SW7 ON = Refresh request (MRQYB-) from J1 (map)

For systems utilizing both A and B ports of the semiconductor memory, without an error correction circuit (ECC), SW1, SW2, SW4, and SW6 are ON; SW3, SW5, and SW7 are OFF. If an ECC is used, SW5 is ON; SW1 and SW4 are OFF. If a memory map is required, SW1, SW3, SW4 and SW7 are ON; all other switches are OFF.

For systems utilizing only one port (A or B) with or without error correction, the corresponding switch settings provide the indicated connection to port A or B as shown below:

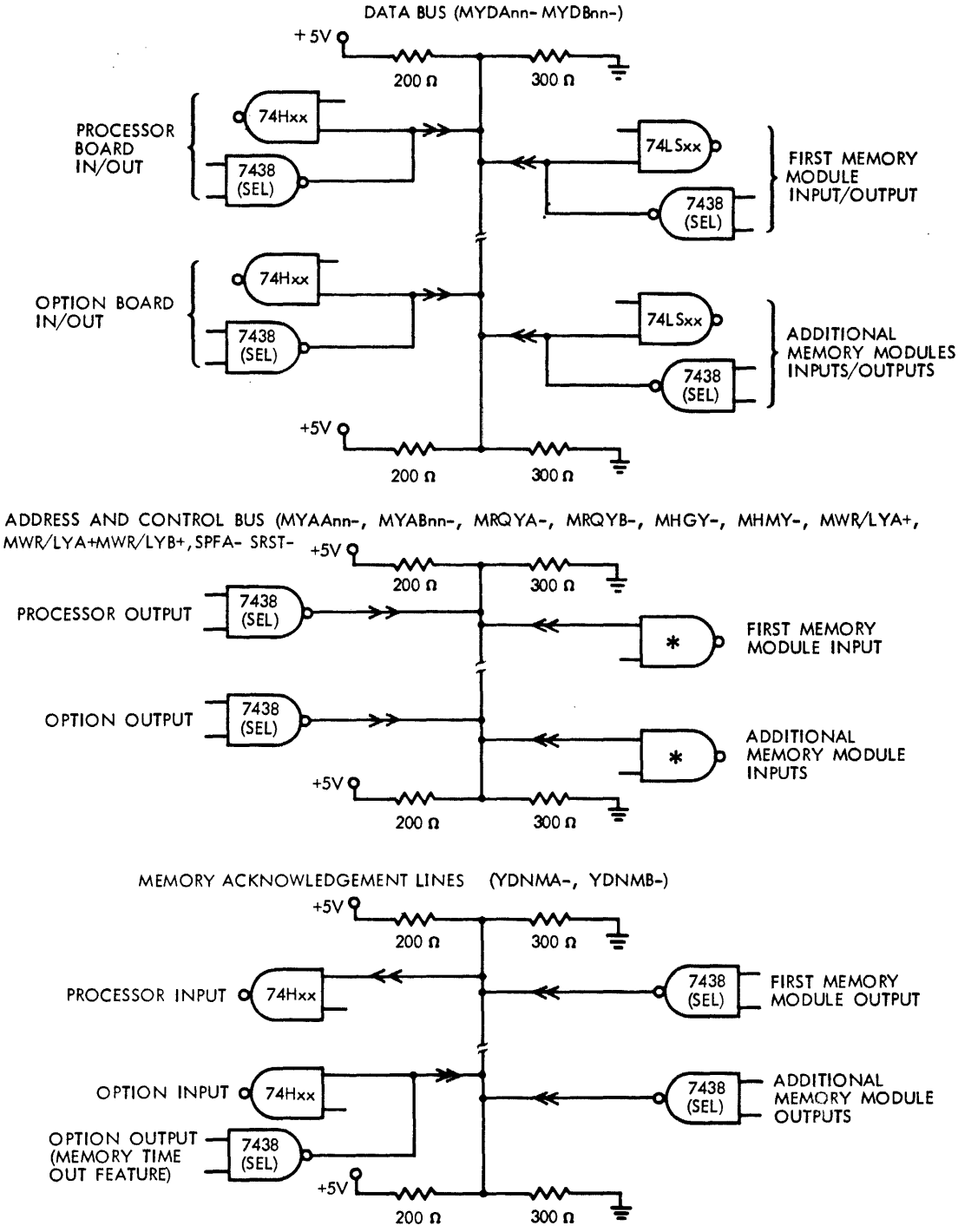
64K Increment	Port Utilized	WITHOUT Error Correction	WITH Error Correction
1st	A	1,2,4,7 ON; 3,5,6 OFF	3,5,7 ON; 1,2,4,6 OFF
	B	1,3,4,6 ON; 2,5,7 OFF	3,5,7 ON; 1,2,4,6 OFF
2nd and on	A	1,3,4,7 ON; 2,5,6 OFF	3,5,7 ON; 1,2,4,6 OFF
	B	1,3,4,7 ON; 2,5,6 OFF	3,5,7 ON; 1,2,4,6 OFF

2.4 INTERCONNECTION

The data, address, and control signals pass between memory and the processor over a multilayer PC backplane through PC edge connector (P1) and rear connectors J1 through J3. Power is supplied to the boards via the P1 connector. Up to sixteen 660 nanosecond semiconductor memory modules can interface the memory bus within a single system configuration.

The memory interface is transistor-transistor logic (TTL) compatible (figure 2-4). Address and control lines are unidirectional, and data lines are bidirectional. Each memory decodes 16 address lines, 4 of which select the MOS RAM elements (64K capacity) and 12 of which contain the address of the word within those elements. Only one module is active on a given port at one time. However, since the ports are independent, two modules can be active simultaneously, one on each port. No spurious signals are generated by nonactive memory modules.

The pin assignments for the connector on the semiconductor memory board are provided in logic diagram 91C0558 (system documentation package).



*FOR MYAAnn-, MYABnn-, MHGY-, MHMY-, MWR/LYA+ MWR/LYB+, SPFA-, AND SRST- TYPE 74LSxx INTEGRATED CIRCUITS ARE USED. (nn- is 00 THROUGH 11)

FOR MYAAnn- AND MYABnn-, TYPE 3404 ICS ARE USED (nn- is 12 THROUGH 15)

FOR MRQYA- AND MRQYB-, TYPE 74Sxx ICS ARE USED

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Figure 2-4. Memory Interface Schematic

SECTION 3
OPERATION

There are no operating controls or indicators on the 660 nanosecond semiconductor memory PC board.

SECTION 4
THEORY OF OPERATION

This section describes the circuit operation of a 660 nanosecond semiconductor memory-module. A functional block diagram, figure 4-1, and timing diagrams are included with the text; however, for a more in-depth analysis, the reader may wish to trace circuit paths of the logic diagram (91C0558) which is contained in the system documentation package. Memory mnemonics are described in section 6. For ease of reading, some mnemonics are written with the variable n replacing the actual numbers. For example, memory data mnemonics MYDB00- through MYDB17- are written MYDBnn-.

4.1 POWER ON

The operation of the 660 nanosecond semiconductor memory is initiated by +5-volt (+5L) and +12/+20-volt dc power supplied by the computer power supply. When the computer power switch is turned on, +5L is applied to a filtering network located on the memory board. This decoupling capacitor circuit removes electrical noise induced by processor circuits coupled to the memory through backplane wiring. At the same time, the +20 volts dc is applied to a voltage regulator circuit on the memory board. This regulator, a sub-circuit of the voltage control circuit (section 4.4), develops +12 volts which in turn develops -5 volts dc. Both of these voltages are used to power the IC RAM array.

Initially, the only filtered input voltages used to power other memory circuits are +5M (TP-1) and +5L (TP-9). The +5M voltage powers only those memory circuits that are continuously on during memory operation. The +5L voltage, supplied by the computer power supply, is used primarily to power the IC RAM output buffer and memory interface logic. Filtered voltages +5S and +5AD used to power other memory logic circuits are initiated and controlled by power control and voltage control circuits powered by the +5M voltage. The voltage and signal outputs from these two circuits initiate memory operations that are controlled by the processor.

4.2 POWER CONTROL LOGIC

When the +5M voltage is initially applied to the power control logic of the memory, both the system reset (SRST-) and system power failure alarm (SPFA-) input lines are at low levels (near zero voltage). The SRST- low applied to the input of a

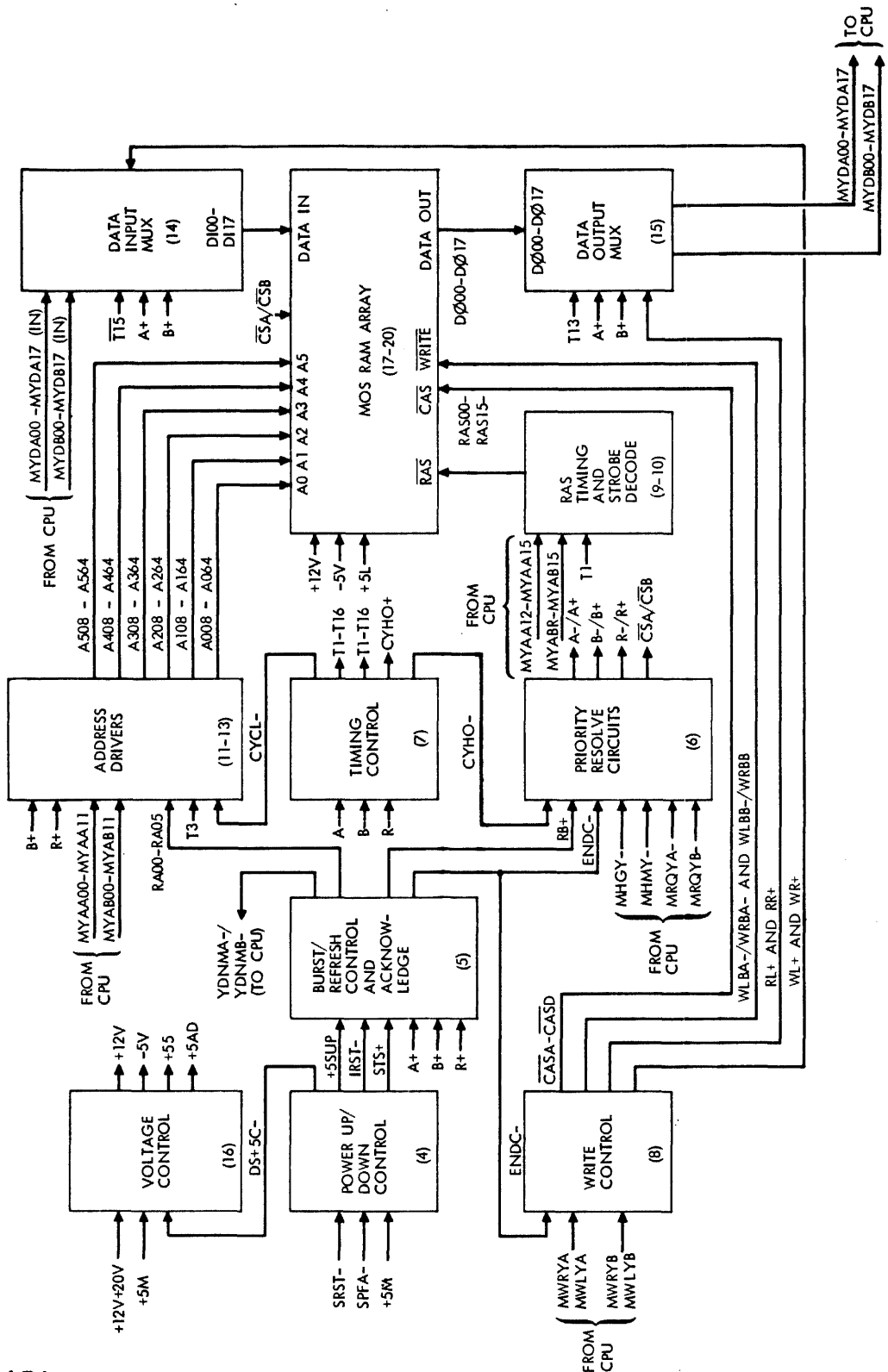

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Figure 4-1. Block Diagram

transistor switching circuit of the power control logic holds the gated output DS+5C- at a high level and prevents the voltage control circuit from supplying +5S and +5AD voltages to other memory logic circuits until SRST- goes high. During this initial period, the transistor switching circuit places the memory logic circuits in a ready state for on-line operation with the processor before the processor is completely operational. It should be noted, however, that this transistor switching circuit is primarily designed to operate in the same manner when a power failure occurs (section 4.11). When power is lost, the transistor switch places the memory logic circuits in a ready state for operation with a battery-powered data save option. The data-save option supplies the +5M voltage and the +12/+20 volts dc that are normally supplied by the computer power supply (section 4.12).

4.3 INTERNAL RESET

When the SRST- signal from the processor reaches a high level (figure 4-2), the gated clear input to a voltage control one-shot is driven low clearing the output and causing STS+ to go high. With a high level on the STS+ output, the DS+5C- gated output drops to a low level and causes a sub-circuit of the voltage control circuit to produce the +5S and +5AD voltages required to operate memory timing circuits and RAM drivers (section 4.4). At the same time, the DS+5C- low clocks a one-shot driving the inverted +5SUP output to a low level which presets the burst refresh flip-flop, clears memory logic circuits and causes an internal reset (IRST-) signal to be held high by a low RA6L-.

4.4 VOLTAGE CONTROL CIRCUIT

The voltage control circuit consists of two separate sub-circuits that control voltages required for both processor and data-save operation. Input voltages to both sub-circuits are supplied by either the computer power supply or the battery of the data-save option (section 4.12).

The first sub-circuit is an IC voltage pass regulator and IC pump converter. The pass regulator operates on a +20-volt dc input and supplies a filtered +12-volt dc output that is connected to the inputs of two pump converters. From the +12-volt dc input, each pump converter develops a negative voltage output that is regulated at -5 volts dc by a zener diode. One of these -5-volt circuits is a redundant circuit designed as a backup in the event that the other circuit fails. Each of the -5-volts clamped by each of the two zener diodes is applied to the base of one transistor of a two transistor exclusive OR

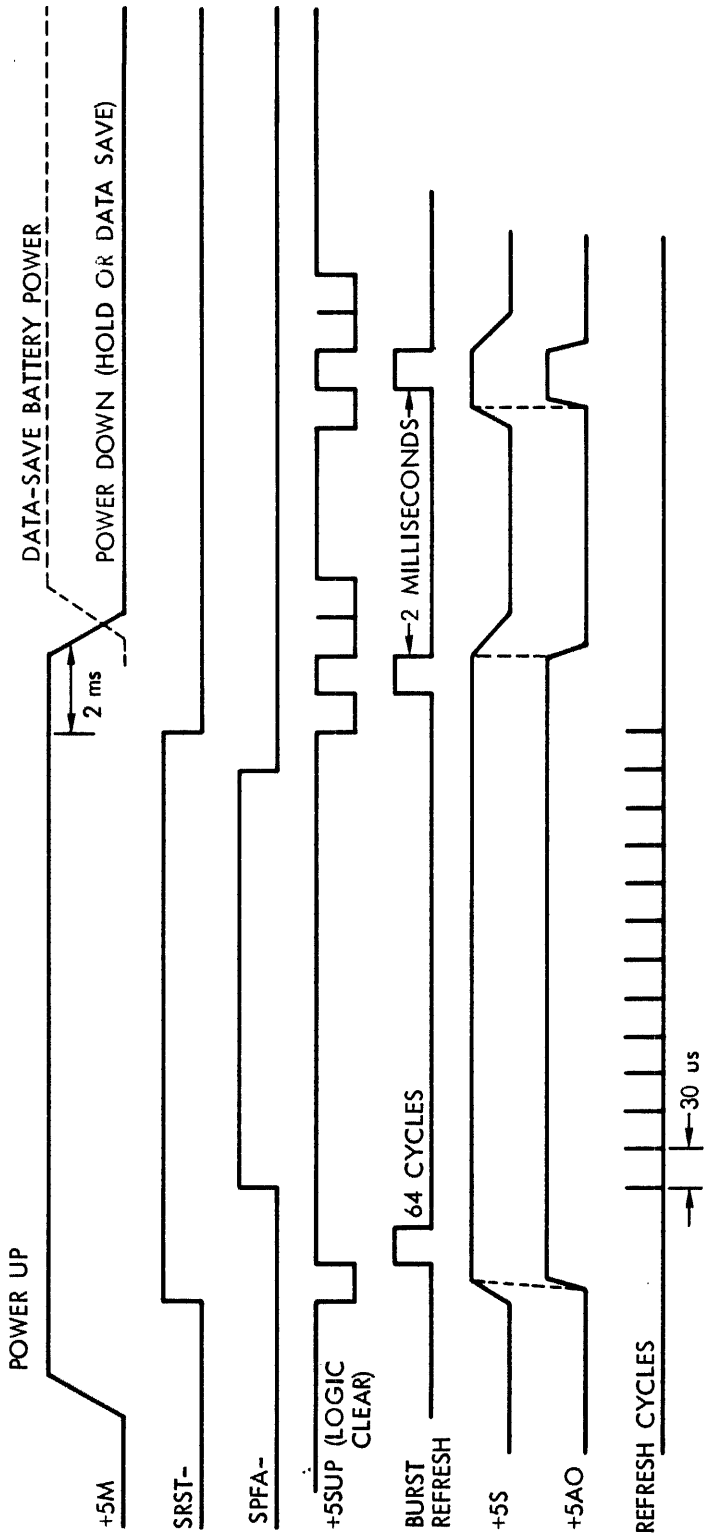

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Figure 4-2. Power Up and Refresh Timing Diagram

circuit. This circuit arrangement monitors both -5-volt dc inputs and if one fails, the exclusive OR collectors go low thereby ending RAS timing. Since both the +12 and -5-volt dc outputs are applied to the IC RAM array, this backup circuit prevents damage to IC RAM elements if a failure occurs.

The second sub-circuit is a transistor switch-amplifier circuit that operates on a filtered +5M voltage input and supplies +5S and +5AD voltages to the timing, address, and memory control logic. A low-level DS+5C- signal applied to the base of the first +5S transistor switch turns on the second +5S transistor switch placing the +5S output voltage at the collector. When this switching transistor reaches saturation, the +5AD transistor switching circuit is turned on placing the +5AD output voltage at the collector of the third +5AD transistor switch. Except when initial power is applied to the memory (section 4.3), the +5S and +5AD voltages are only continuously on when the memory is on-line with the processor. When the data-save option is utilized, +5S and +5AD are normally off but are turned on every two milliseconds for a burst refresh operation, (figure 4-2).

4.5 SYSTEM READY BURST REFRESH

After the system reset signal (SRST-) has reached a high level but before the system power failure alarm (SPFA-) goes high, a burst refresh of 64 normal refresh cycles (section 4.7) is initiated to refresh stored data in the memory array following a data-save operation. After the data-save option has been turned off by the high-going SRST- signal from the controlling computer processor but before the internal refresh seqeunce is initiated (section 4.7.1), the low +5SUP (section 4.3) initiates a burst refresh sequence which prevents data from being lost during the transition period from battery power to supply power. The detailed discussion is contained in subsequent paragraphs of this section.

When the +5SUP signal is clocked low by the low DS+5C- (section 4.3), the burst refresh flip-flop is preset and forces the RA6L- signal to a low level. At the same time CYHO- is held at a high level by +5SUP applied to one of four inputs to the CYHO- cycle timing gate. The low RA6L- sets the refresh request signal (RB+) high causing coincidence with the high CYHO- signal at dual inputs of a NAND gate which drives a two NAND gate refresh request flip-flop. When this coincidence occurs, the output of the first flip-flop gate is driven high and applied to one input of the second flip-flop gate. When +5SUP returns to a high level at the end of the +5SUP one-shot timing, it becomes coincident with the high STS+ and high IRST- signals (section 4.3) and causes the end of cycle signal (ENDC-) to go high.

The high ENDC- signal marks the beginning of the burst refresh sequence.

4.5.1 Burst Refresh Sequence

Now when the high ENDC- signal is applied to the second input of the second refresh request flip-flop gate it becomes coincident with the high output of the first flip-flop gate and drives the refresh cycle in progress signal (R-) low, the R+ (inverted R-) signal high, and the refresh address clocking signals (RA1- and RA2-) low. When the R- signal goes low, it locks out memory requests from the port A and B processors, enables the timing oscillator, and places cycle timing signals CYCL-, CYHO+, and CYHO- at their active (true) levels. It should be noted, however, that although CYHO- goes low when R- is low, the active change in the CYHO- level has no affect on the state of the refresh request flip-flop. When RA1- goes low, the refresh disable one-shot is clocked high and remains high throughout the burst refresh sequence. The significance of this action will become obvious later in the discussion. Now when the R- low enables the timing oscillator, the oscillator output clocks the four quad flip-flops of the delayed timing clock (section 4.7.2) which generates the timing pulses for each cycle. Near the end of the first of the 64 refresh cycles, a high T2 timing signal coincident with an already high T16 timing signal forces ENDC- low which changes the state of the refresh request flip-flop and causes RA1- to go high. On the high-going transition of RA1-, the 6-bit refresh address counter is clocked and produces a refresh address output with a binary count of one. Meanwhile, the R+ high permits the address multiplexor (section 4.8.2) to select the refresh address generated by the refresh address counter and the first refresh cycle address is applied to the 64K MOS RAM array. At the low going transition of the T5 timing signal, the first cycle ends. The low T5 forces CYHO- high which in turn clears the timing clock flip-flops and turns off the timing oscillator. With the timing clock cleared, ENDC- returns to a high level and the second refresh cycle begins. This cycle sequence is repeated through 64 cycles of the refresh address counter until all address bits are high (binary count of 64). At the end of cycle 64, the high-going transition of RA1- clocks the refresh address counter one more time producing a high RA6C+ signal. This high level RA6C+ signal clocks the burst refresh flip-flop forcing RA6L- high which becomes coincident with the high from the refresh disable one-shot (previously discussed) forcing RB+ low and ending the burst refresh seqeunce. It should be noted that neither the RA6C+ high nor the RA6L- high has an effect on the output levels of the STS+ or IRST- signals at this time because of the low clear input to the voltage control flip-flop produced by the high SRST- signal.

4.6 ON-LINE OPERATION

Within a period of not less than 110 microseconds after the high SRST- signal is generated by the processor, the system power failure alarm signal (SPFA-) from the main processor reaches a high level. When SPFA- becomes high, the memory is on-line with the main processor and ready to perform normal operating cycles. It should be noted that a low level SRST- generated by the front panel RESET switch will not effect normal memory operation once SPFA- reaches a high level (see figure 4-3).

4.7 OPERATING CYCLES

The 660 nanosecond semiconductor memory has two operating cycles, memory and refresh. The refresh cycle is initiated internally by a refresh request flip-flop (section 4.5) unless the memory is used with an error correction circuit (sections 1 and 2.3). Each memory cycle is initiated by the combination of a memory request signal (MYQRA- or MYQRB-) and a priority signal (MHGY- or MHMY-) from one of two possible processors (section 1) through associated terminals of port A or port B. However, before any of the operating cycles can begin, priority must be resolved.

4.7.1 Priority Resolve Circuits

Since the refresh cycle has priority over memory cycles, it is only reasonable that cycle priority is controlled by the refresh request signal (RB+). Prior to the beginning of each operating cycle, a gated high CYHO- signal from the cycle timing circuit samples the RB+ refresh request signal. The resulting signal produced by coincident gating of these two signals sets the refresh request flip-flop that establishes the priority for that cycle. If RB+ is high at the beginning of a cycle, the output of refresh request flip-flop which is also the refresh cycle in progress signal (R-) is set low and a refresh cycle is initiated. If, however, RB+ is low at the beginning of a cycle, R- is set high which permits memory cycle priority to be controlled by memory request and priority signals from the A or B processors. Cycle priority for either the A or B port is established during a memory cycle by the high and low level condition of both memory request signals (MRQYA- and MRQYB-) and memory priority signals (MHMY- and MHGY-) as shown in table 4-1.

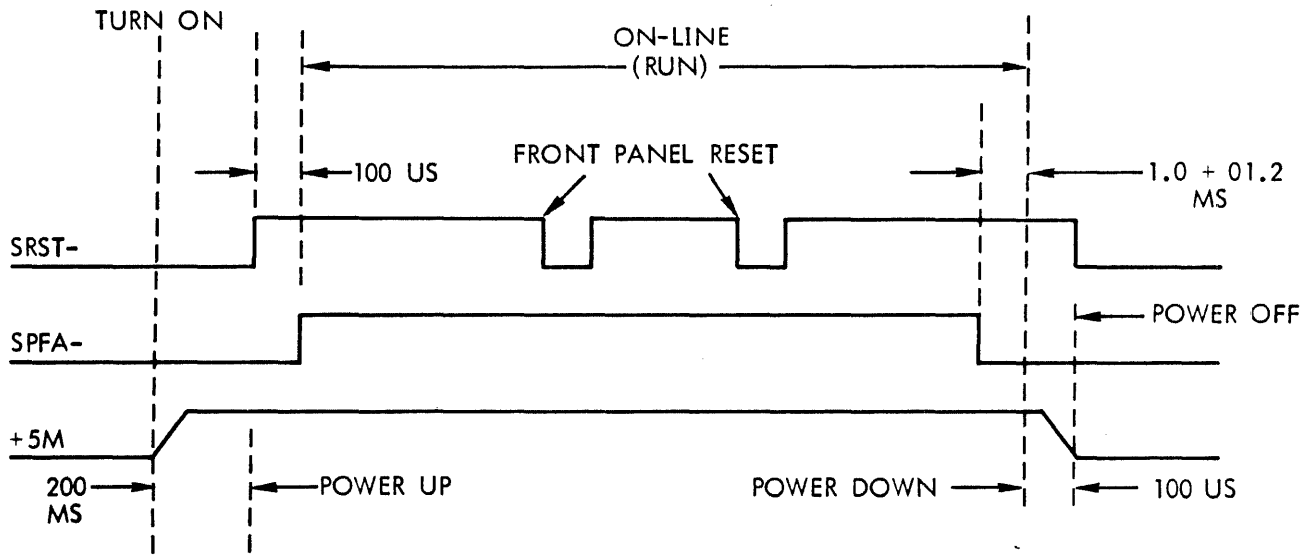

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Figure 4-3. Panel Reset

It should be noted, however, that cycle timing established by the refresh disable one-shot and the T5 timing signal (section 4.7.2) permits R- to initiate a refresh cycle approximately every 30 microseconds after the preceeding cycle is complete regardless of established port priority, (figure 4-2).

The timing for initiating a refresh cycle is established by the trailing edge of the high pulse output of the refresh disable one-shot. Near the end of each refresh cycle, a low-going refresh address clock (RA1-) triggers the refresh disable one-shot causing the output to go high for 30 microseconds. This high becomes coincident with the high level RA6L- signal (section 4.5) and forces the RB+ signal low. While RB+ is low, refresh is disabled and memory cycles can be initiated. At the end (trailing edge) of the 30 microsecond pulse, RB+ returns to a high level. When the preceeding cycle is complete, the T5 timing signal low (figure 4-4) forces cycle timing signal CYHO- high. As noted at the beginning of this section, each time this combination of a high RB+ and high CYHO- occurs, the refresh request flip-flop is set and the refresh cycle is repeated.

4.7.2 Timing Control Circuits

Cycle timing is initiated by one of the low level signals R-, B-, or A- applied to the inputs of a cycle-select NOR gate. The resulting output low triggers a 50 nanosecond (approximate output) oscillator that clocks a 20 MHz (approximate output) delayed timing circuit consisting of four D-type quad flip-flops. It should be noted however, that before the first clocking signal high is applied to these quad flip-flops that each flip-flop is cleared by a low level CYHO+ signal generated by the absence of a cycle-in-progress signal (R-, A-, or B-). As a result of this clear input, the T16- timing clock output goes high before the clock becomes active. This high is applied to the D-input of the first quad flip-flop through a feed back loop and places the first flip-flop of the clock in a ready state to receive the initial inverted clock pulse from the oscillator. When the initial inverted clock pluse goes high, the delayed timing sequence begins and stepped-timing pulses are generated at the flip-flop outputs (figure 4-4). A timing pulse is generated approximately every 25 nanoseconds as a result of the method of applying non-inverted and inverted oscillator output pulses to alternate quad flip-flop clock inputs.

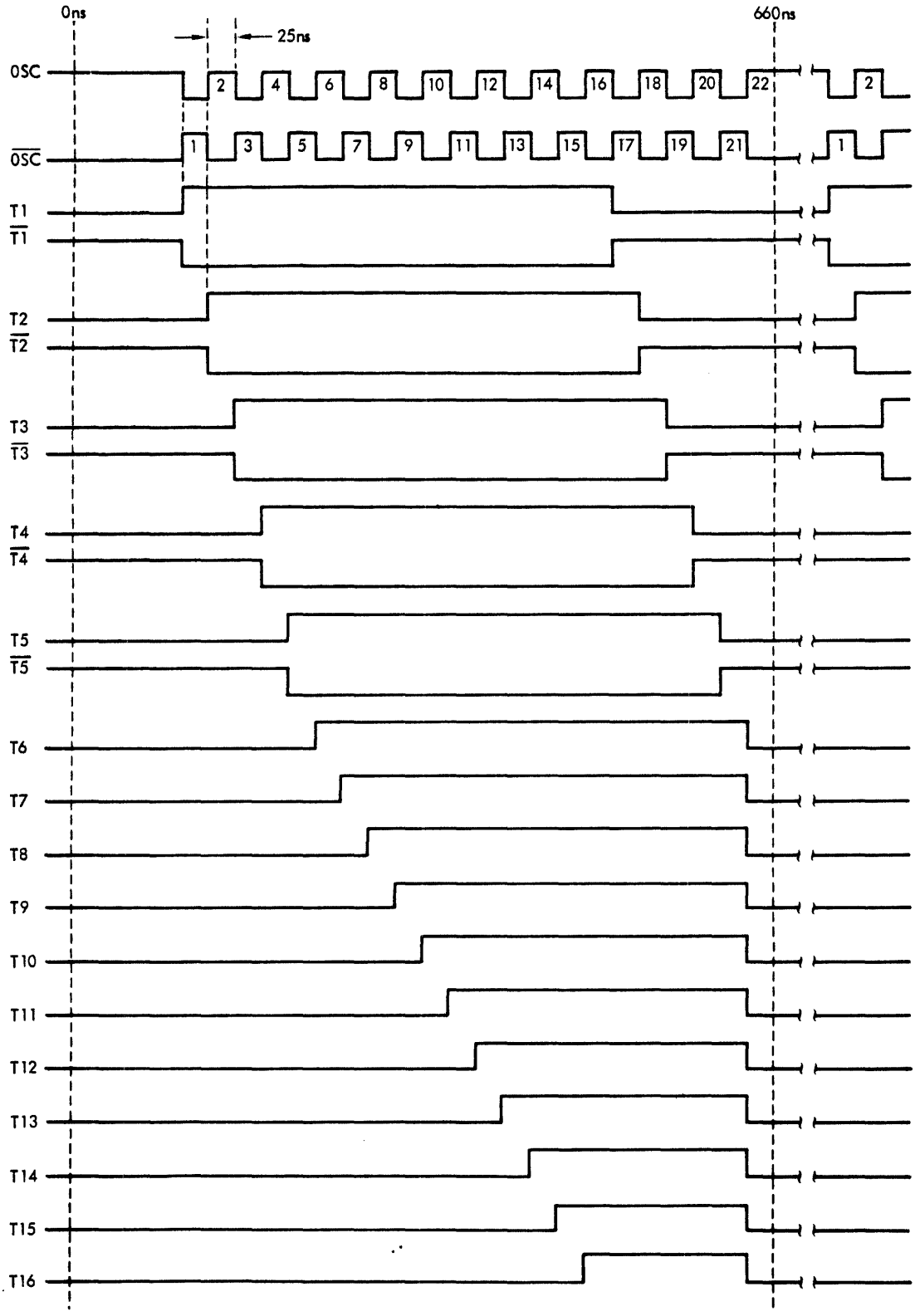
Table 4-1. Memory Cycle Priorities

MHMY-LEVEL	MRQYA-LEVEL	MHGY-LEVEL	MRQYB-LEVEL	CYCLE IN PROGRESS SIGNAL AND MEMORY STATUS	PORT PRIORITY
H	H	H	H	Memory cycle not requested; both A- and B - high	None
H	H	H	L	B-port cycle requested; A- high and B- low	B
H	H	L	H	B-port hogs memory without request; A- high and B- low	B (CI)*
H	H	L	L	B-port hogs memory; A- high and B- low	B (CA)*
H	L	H	H	A-port cycle requested; A- low and B- high	A
H	L	H	L	Both memory cycles requested; A- high and B- low	B
H	L	L	H	B-port hogs memory, locks out A-port request, and forces A- high and B- low	B (CI)*
H	L	L	L	B-port hogs memory with both cycles requested, locks out A-port request, and forces A- high and B- low	B (CA)*
L	H	H	H	A-port hogs memory without request; A- low and B- high	A (CI)*

Table 4-1. Memory Cycle Priorities (continued)

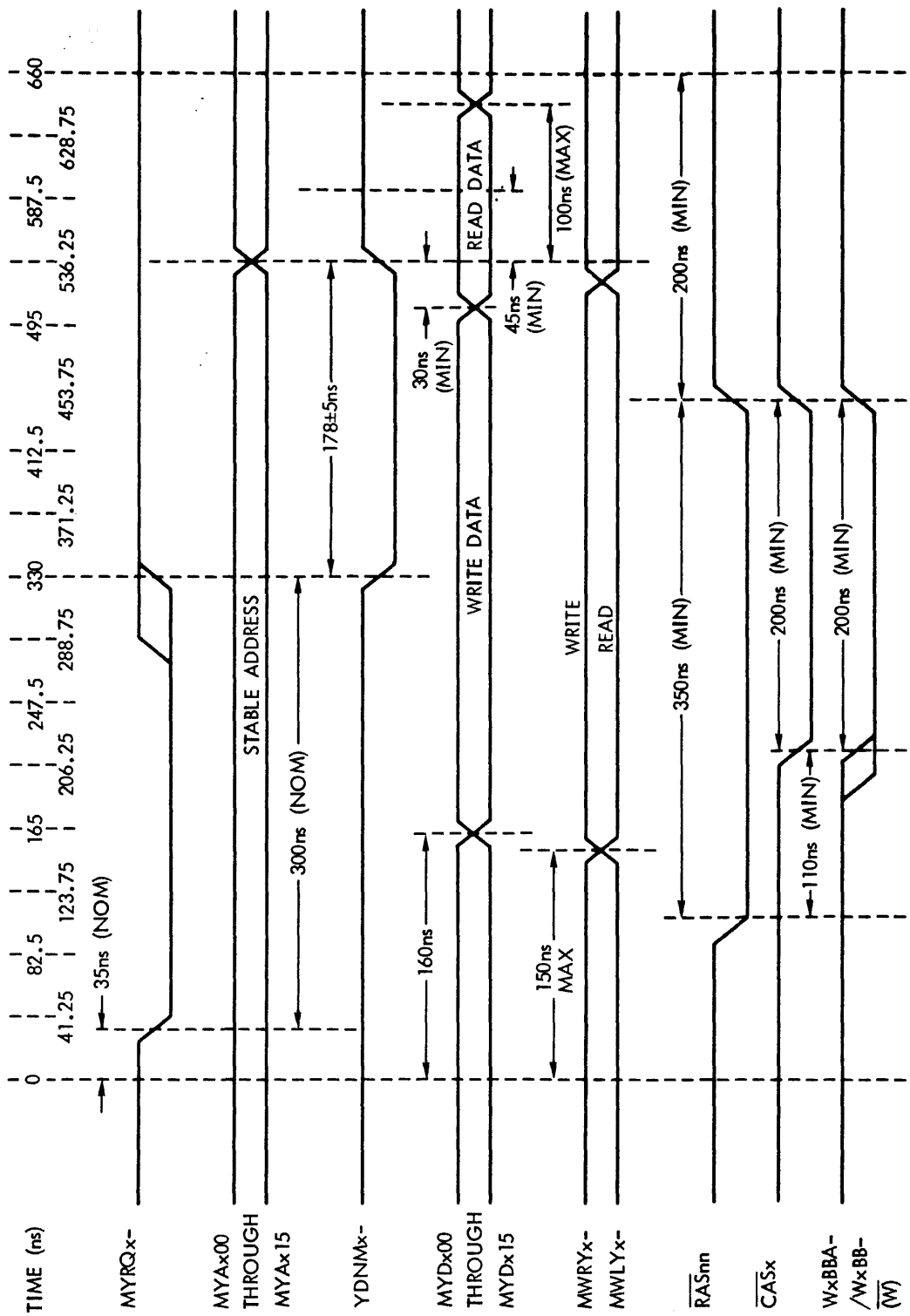
MHMY-LEVEL	MRQYA-LEVEL	MHGY-LEVEL	MRQYB-LEVEL	CYCLE IN PROGRESS SIGNAL AND MEMORY STATUS	PORT PRIORITY
L	H	H	L	A-port hogs memory, locks out B-port request, and foreces B-high and A- low	A (CI)*
L	H	L	H	Both hog lines cancel without memory request; both A- and B-high	None
L	H	L	L	Both hog lines cancel with B-port cycle requested; A-high and B- low	B
L	L	H	H	A-port hogs memory; A- low and B- high	A
L	L	H	L	A-port hogs memory with both cycles requested, locks out B-port request, and forces B-high and A- low	A (CA)*
L	L	L	H	Both hog lines cancel with A-port cycle requested; B-high and A- low	A
L	L	L	L	Both hog lines cancel with both memory cycles requested; A- high and B- low	B

* (CI) = Cycle Inactive; (CA) = Cycle Active



VTI2-475

Figure 4-4. Clock Timing



VTI1-3535

Figure 4-5. Memory Cycle Timing Diagram

These timing pulses are generated throughout one complete half cycle of the delayed clock and up through removal of the high level T5 timing pulse during the second half cycle. At that time, the low level T5 output completes the cycle time of the refresh or memory cycle in progress (660 nanoseconds) and permits the delayed timing clock to be cleared for the next operating cycle. The cycle timing sequence is repeated when the next cycle in progress signal (R-, B-, or A-) is applied to the cycle-select NOR gate.

4.7.3 Write Control Logic

Since a memory cycle is either a write or a read cycle, a data word is entered into memory or retrieved from memory during one cycle period (figure 4-5). In this memory, data words are written into memory or read from memory in half-word (byte) increments. The byte signal lines from the A and B processors (section 1) control the byte selections and the type of memory cycle. Byte control signals, MWRYA+ and MWLYA+, control the right and left bytes of each data word from the A processor while MWRYB+ and MWLYB+ control the right and left data bytes from the B processor.

When either of the right byte control signals (MWRYA+ or MWRYB+) is high, the complement memory cycle in progress signal (A+ or B+) permits that byte to be written into the addressed memory byte location. The same is true for the left byte control signals (MWLYA+ or MWLYB+). However, when any of the right or left byte control signals are low, the memory cycle in progress signal permits that byte to be read from the addressed memory byte location. The read/write functions are controlled by dual inverters that provide the appropriate byte signal outputs to the data input and output logic.

On a write memory cycle, the high level write data byte enable signals (WR+ and WL+) are produced by the inversion of the gated low outputs from two NAND gates. The high level read data byte enable signals (RR+ and RL+) are produced by the inversion of the inverted low WR+ and WL+ signals when the gated outputs are high during a read memory cycle. These signals enable the data input and output logic controlling data entry or retrieval (section 4.9.1 and 4.9.2).

In order for the right and left data bytes to be written into MOS RAM elements (section 4.10), write enable signals (WRBx- and WLBx-) are generated by coincident gating of WR+ or WL+ and timing signals T6 and T14. When WR+ is at a high level the resulting low level WRBA- and WRBB- write enable signals permit the right data byte to be written into right byte MOS RAM elements. When WL+ is high, write enable signals WLBA- and WLBB- are forced low which permit the left data byte to be written into left byte MOS RAMs.

4.8 ADDRESSING

Before the memory request signal (MRQYA- or MRQYB-) on either the A or B port can initiate a memory cycle, the corresponding memory address bits from the controlling processor or other device must be on-line and stable (figure 4-5). If the A processor is in control of the memory cycle, address bits MYAA00+ through MYAA15+ will be on-line and used to address the MOS RAM elements. If the B processor controls the memory cycle, address bits MYAB00+ through MYAB15+ will be on-line and used to address the MOS RAM elements. These address lines will remain stable until the positive going transition of the corresponding memory acknowledgment signal (YDNMA- or YDNMB-). If the operating cycle is a refresh cycle, refresh address bits (RA00 through RA05), generated by the refresh counter, are used to address the MOS RAM elements.

The logic circuits of this memory module have no provision for offset addressing or interleaving of groups of memory elements.

In those models with a storage capacity of less than 64K words, the computer program controls the addressing of available storage locations. Addressing beyond 32K words is controlled by the memory map logic (section 1).

4.8.1 Memory Cycle Address Logic

At the start of each operating cycle, 16 address bits from each of the A and B processors are present on each corresponding memory address bus (figure 4-5). Twelve of these address bits (MYAx00 through MYAx11) are applied to AND/NOR gate 2-to-1 address multiplexors of the memory address logic and four (MYAx12 through MYAx15) are applied to circuits of the row address strobe logic (section 4.8.3). When the high level of the inverted T3 timing signal from the timing control (section 4.7.2) enables the 2-to-1 multiplexors, the first six address bits from both processors are selected for row addressing of the MOS RAM elements (section 4.10) and applied as inputs to three 4-to-1 multiplexors.

If a memory cycle has priority (section 4.7.1) the level of the B+ priority signal applied to each 4-to-1 multiplexor will determine whether the A or B memory address bits are selected for driving the MOS RAM elements. If B+ is high, the six row address bits are selected from the controlling B processor bus; if B+ is low, they are selected from the controlling A processor bus. In either case, the resulting multiplexed inputs are enabled out of each 4-to-1 multiplexor by CYCL- signal pulses from the timing control (section 4.7.2).

Part way through the cycle, T3 goes low and the second six address bits are selected by the 2-to-1 and 4-to-1 multiplexors for column addressing of the MOS RAM elements. Here again the same level of B+ controls the address selection from either the A or B processor bus. The resulting multiplexed outputs are inverted and applied to the column address inputs of all MOS RAM elements in the memory array.

4.8.2 Refresh Cycle Address Logic

If a refresh cycle has priority, refresh address bits generated by the refresh counter (section 4.5) are applied to the inputs of the 4-to-1 multiplexors. The high level R+ priority signal generated by priority logic circuits (section 4.7.1) then enables the selection of the refresh address applied to both row and column address latches of all MOS RAM elements. The CYCL- signal enables the 4-to-1 multiplexor which permits the refresh address input to be multiplexed out, inverted, and applied to the input of both latches in each MOS RAM element.

4.8.3 Memory Address Strobe Logic

Before either the memory cycle address or the refresh cycle address can be latched into the row and column latches of a MOS RAM element, each MOS RAM latch must be clocked by a respective address strobe. The row address latch of each MOS RAM element is clocked by a corresponding row address strobe (RASnn-). Each MOS RAM column address latch is clocked by a corresponding column address strobe (CASx) (section 4.10).

Sixteen row address strobes (one for each 4K segment of memory) are generated by the last four memory address bits from the controlling processor address bus.

During a memory cycle, memory address bits MYAA12+ through MYAA15+ and MYAB12+ through MYAB15+ from each respective A and B processor address bus are applied to the input lines of two corresponding 4-bit latches of the row address and timing circuits. Both of these latches are enabled by the low-level of the T1 timing signal (section 4.7.2) which stores the address. Thereafter, on the high-going transition of the T1 low the complement output of the address from both latches are multiplexed by four AND/NOR gate 2-to-1 multiplexors. These multiplexors select the complementary address bits from the controlling processor and reject those from the non-controlling processor. This is accomplished by the coincident gating of each complement address bit with the high level of either the A+ or B+ priority signal generated by priority resolve circuits (section 4.7.1). The multiplexed outputs corresponding to address bits MYAx12+, MYAx13+,

and MYAx14+ are gated by a high level RA2- and then decoded to provide two groups of eight row address strobes, RAS00- through RAS07- and RAS08- through RAS15-. At the same time, the multiplexed output corresponding to the true or false term of MYAx15+ is applied in coincidence with required delayed timing to inputs of two RAS timing gates. The resultant RAS timing outputs, in turn, select one of the two groups of row address strobes thereby permitting only one of the sixteen address strobes to be applied to the RAM array during the memory cycle. This single row address strobe is then used to enable the row address latches of the sixteen (bits of one word) MOS RAM elements in the memory array. During a refresh cycle all sixteen row address strobes are applied to the RAM array.

During both memory and refresh cycles, four column address strobes (CASA- through CASD-) are initiated by the coincident gating of the T6 and the inverted T15 timing pulses (section 4.7.2). With inverted T15 at a high level after the initial clear applied to each of the timing clock quad flip-flops, the high-going transition of the T6 pulse forces the outputs of four NAND gates low and initiates the column address strobes. These low level column address strobes are then applied to all MOS RAM elements (one for each group of 64) in the memory array (section 4.10).

When a memory cycle has priority (section 4.7.1) two identical chip select (CSA- and CSB-) low level signals are initiated which enable the column address latch for all MOS RAM elements in the memory array. During a refresh cycle the chip select signals are at high levels and the column address latching function becomes inactive.

4.9 DATA CONTROL LOGIC

When the cycle in progress is a memory cycle, data entry (write) or data retrieval (read) is controlled by data input multiplexing or data output demultiplexing circuits of the data control logic (figure 4-1). Although these input multiplexors and output demultiplexors are connected directly to the bidirectional bus for each processor or device (port A and port B), only one processor or device is active at a time. This means that during the cycle, each 16-bit data word (18-bits with parity) is written into memory or read from memory through the active port.

If the cycle is a write cycle, the controlling processor or device places data on the memory data bus. When this data is stable on the bus from the leading edge of the memory request (MYQRx) signal (time 0 plus 160 nanoseconds) to the trailing edge of the memory acknowledgement (YDNMx) signal, the data is written into the memory (figure 4-5).

If the cycle is a read cycle, the memory places data on the memory data bus. When this data is valid and stable from 30 nanoseconds before the trailing edge of the memory acknowledgment (YDNMx) signal until 45 (minimum) to 100 (maximum) nanoseconds after, the data is read (accepted) by the processor (figure 4-5).

The memory (YDNMA- or YDNMB-) is initiated by the high-going transition of the T8 timing signal (section 4.7.2) which clocks a retriggerable one-shot. Enabled by a low-level R+ signal (section 4.7.1), the one-shot then generates a high level DUN+ pulse that is gated by a coincident high level A+ or B+ port priority signal. The resulting output is the memory acknowledgment signal.

4.9.1 Read Data Logic

If the memory cycle in progress is a read cycle, sixteen high and low level data bits stored in sixteen adjacent MOS RAM elements (section 4.10) are made available on the output lines of the memory array. As a single data word, these buffered data output signals (DO00- through DO15-) are inverted and applied to inputs of sixteen corresponding 1- to 2 demultiplexors. Note, if optional parity bits are also available, parity signals (DO16- and DO17-) are inverted and applied to two corresponding demultiplexors. The buffered data, with or without parity, is demultiplexed with one of two pair of high-going byte output enable signals (DOENAR+ and DOENAL+ or DOENBR+ and DOENBL+). Generated by the coincident gating of read byte enable (RR+ or RL+), port priority (A+ or B+), and the T13 timing signal, the byte output enable signals cause the demultiplexors to place the 16-bit data word and parity bits (if present) on the data bus terminals of the controlling processor. Thus read data bits, MYDA00- through MYDA17- or MYDB00- through MYDB17-, are available for processing by the controlling A or B processor.

4.9.2 Write Data Logic

If a write memory cycle is in progress, sixteen data bits and two parity bits (if used) from both A and B processors can be on-line at the same time. That is, write data bits, MYDA00- through MYDA17- or MYDB00- through MYDB17- can be present on both the A and B terminals of the data bus and available to the memory for storage. As a single data word, these data bits are multiplexed with one of two pair of high-going byte input enable signals (DIENAR+ and DIENAL+ or DIENBR+ and DIENBL+). Generated by the coincident gating of write byte enable (WR+ or WL+), port priority (A+ or B+), and the complement of the T15 timing signal, the byte input enable signals cause the 2- to -1 multiplexors to initiate a single output which is inverted and applied to the MOS RAM elements for storage. Thus, each of data bits, DI00- through DI17-, are written into one of sixteen corresponding MOS RAM elements.

4.10 MOS RAM ELEMENT LOGIC

The basic IC element of the semiconductor memory array is a dynamic 4096 (4K) by 1 bit RAM with a high density N-channel metal oxide semiconductor (MOS) substrate. The operation of this 4K MOS RAM is straight forward in that decoded serial data is entered into or retrieved from an internal 4096-bit (4K) storage matrix (figure 4-6).

When used in the 660 nanosecond semiconductor memory module, the internal storage array of each MOS RAM represents one bit of the 16-bit format (18-bits with parity) for 4096 computer words.

During one MOS RAM write or read cycle, twelve input address bits are used to access a single bit location of the MOS RAM array. The first six parallel address bits are applied to a six bit latch which is enabled by an internal timing pulse and permits row decoding (figure 4-7). The internal row timing generator is triggered by the row address strobe (RAS). The second six parallel address bits are applied to a 7-bit latch which is clocked by a column address strobe (CAS) signal and permits column decoding when chip select (CS) is low during a memory cycle. The latched row and column addresses are then clocked into their respective 1 to 64 decoders by the corresponding timing generators triggered by the low going row address strobe (RAS) and a low going column address strobe (CAS).

During one MOS RAM refresh cycle, CS is at a high level and both the row and column addresses are identical through the cycle but only six different address bits are used instead of the twelve required for read and write cycles. The second six (column address bits are ignored since the column address strobe is only used to disable the data output. With a high level at the chip select (CS) input both the data input and output latches are disabled and the address current refreshes the stored data locations.

4.11 POWER DOWN

When the computer power switch is turned off or a short-term system power failure occurs, the system power failure alarm signal (SPFA-) immediately drops to a low level (figures 4-2 and 4-3). Approximately one millisecond later SRST- goes low. It should be noted, however, that the +5M voltage is sustained by the power supply for 2 milliseconds after the SRST- low occurs. In the meantime, the low SRST- drives IRST- low clocking the +5SUP one-shot high and forcing +5SUP low. The low +5SUP presets the burst refresh flip-flop and clears the 6-bit refresh counter. When the burst refresh flip-flop is preset, RA6L- is set low and IRST- returns to a high level. Afterward +5SUP returns to a high level and becomes coincident with the high

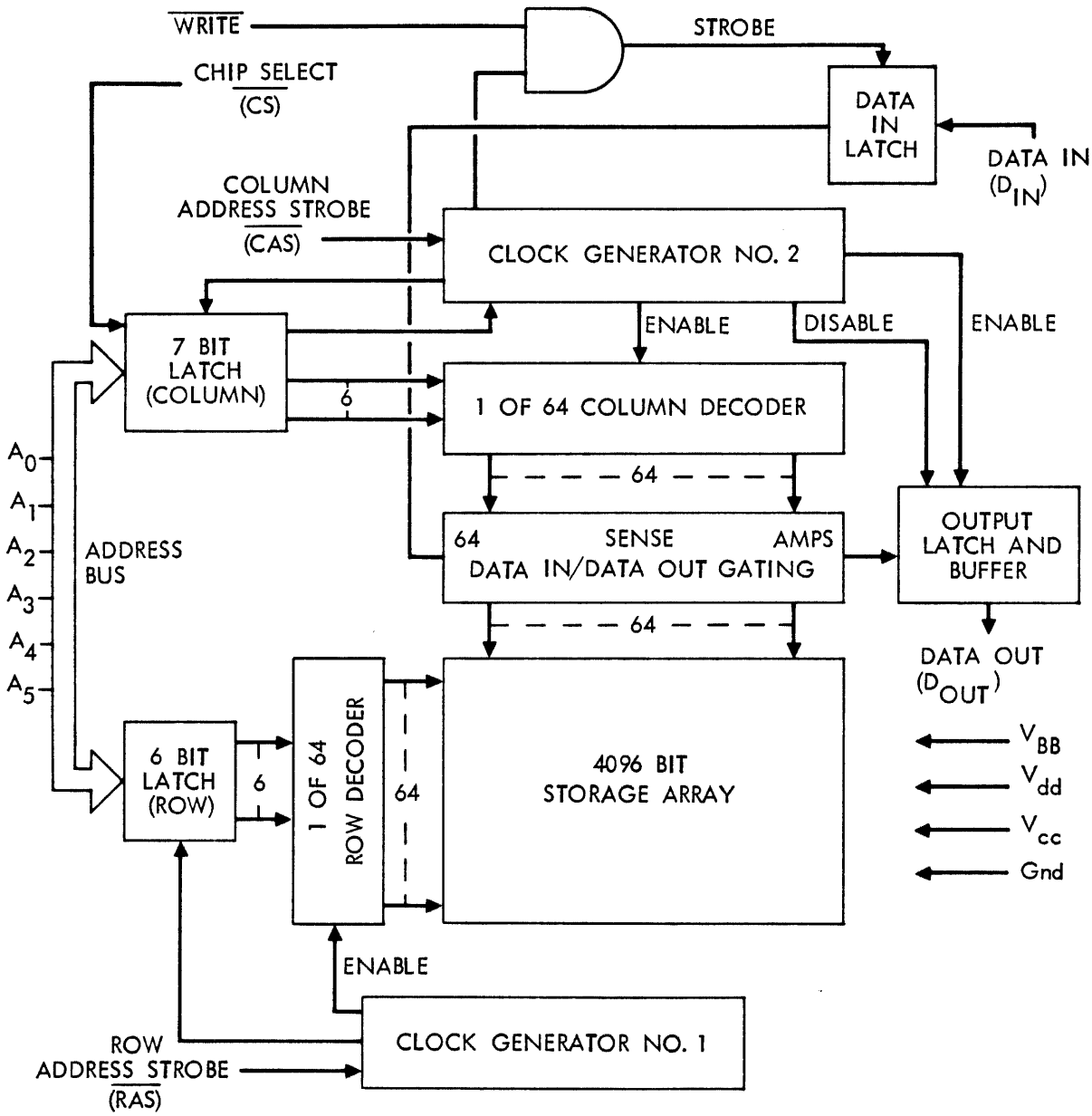


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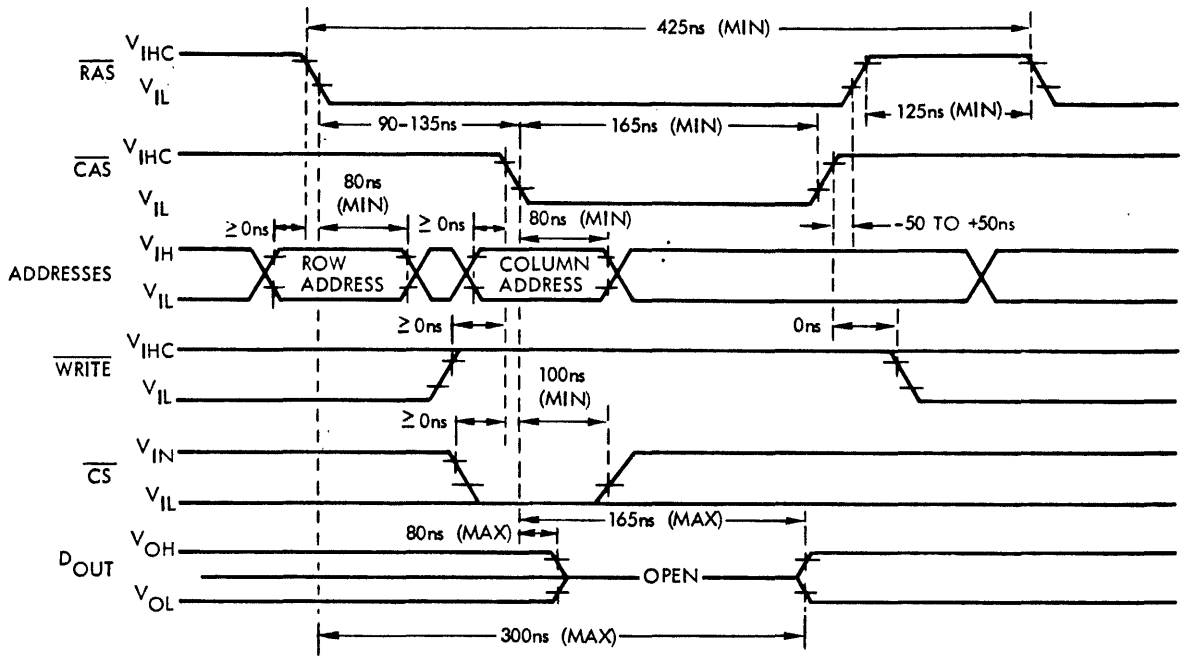
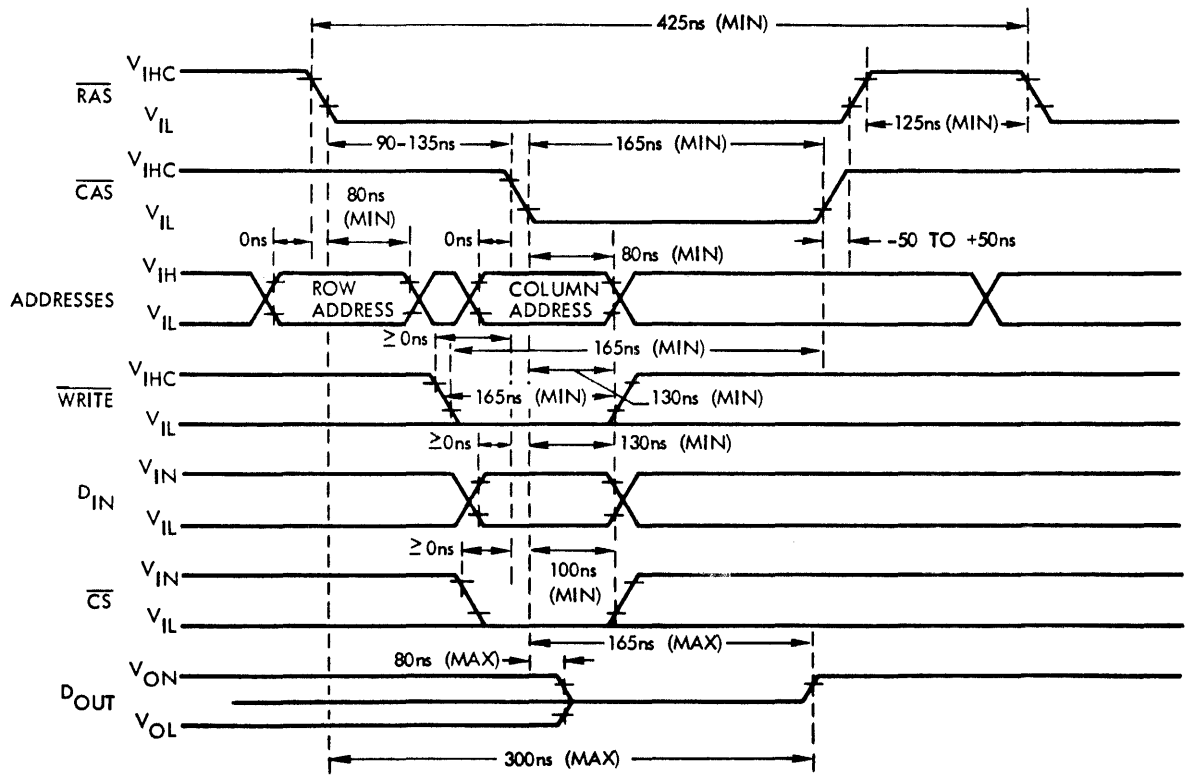
Figure 4-6. MOS RAM Element Block Diagram



READ CYCLE



WRITE CYCLE

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Figure 4-7. MOS RAM Timing

IRST- and STS+ signals to set ENDC- at a high level and initiate a burst refresh sequence (section 4.5.1). At the end of this 64-cycle burst refresh, the RA6C+ signal high generated by the refresh counter clocks the voltage control one-shot which drives the inverted STS+ low and DS+5C high. This action turns off the +5S and +5AD voltages and power down is complete. If the computer power supply is not equipped with the data-save option, the +5M voltage then drops to zero volts and power is off.

4.12 DATA-SAVE FUNCTIONS

If the computer power supply is equipped with a battery-powered data-save option, data already stored in the 4K MOS RAM array is sustained for up to 4 hours in a 660 nanosecond semiconductor memory with a capacity of 64K words. This is made possible by the data-save option which provides the +5M and +12/+20 volt dc operating voltages for the memory. In a data-save mode, two milliseconds after the power down burst refresh and every two milliseconds thereafter, the voltage control one-shot output high clocked by the RA6C+ inverted low, also goes low producing a STS+ high and enabling the burst refresh sequence (section 4.5.1) to be repeated.

SECTION 5
MAINTENANCE

Maintenance personnel should be familiar with the contents of this manual before attempting memory troubleshooting. The MAINTAIN III test program system (MAINTAIN III Manual) contains a memory test program used to isolate a malfunction to a particular 660 nanosecond memory module. Determine which memory board is at fault and move it to the top slot for troubleshooting. Further diagnosis can then be made by referring to this manual.

5.1 TEST EQUIPMENT

The following is a list of recommended test equipment for memory maintenance:

a. Oscilloscope, Tektronix type 547 with dual-trace plug-in unit, or equivalent.

b. Multimeter, Hewlett-Packard 3469B or equivalent.

5.2 CIRCUIT BOARD REPAIR

The memory module is contained on a standard 2-layer PC board. If it has been determined that circuit-board repair is required except for plug-in MOS RAM ICs, it is recommended that the Sperry Univac customer service department be contacted so that a new circuit board can be installed in the user's system and the faulty one returned to the factory for repairs. However, if the user decides to perform his own repairs, extreme caution should be used so that the circuit board is not permanently damaged. Approved repair procedures should be followed such as the ones described in document IPC-R-700A prepared by the Institute of Printed Circuits. However, if it has been determined that one of the MOS RAM ICs is faulty simply remove it from its associated socket and replace it with a new one.

5.3 MEMORY FAILURE SYMPTOMS

The repeated occurrence of the halt instruction or the completely random sequencing of instructions are indicative of a possible memory failure. If either of these symptoms or any other symptom which is indicative of a memory failure occurs during normal computer operation, perform the checks, adjustments, tests, and troubleshooting procedures listed in subsequent paragraphs, as required.

As an aid to troubleshooting, refer to the theory of operation (section 4) and the logic diagram in the system documentation package.

5.4 DC VOLTAGE CHECKS

The DC voltage checks provided herein are divided into two sections. The first section deals with mandatory procedures required for each memory module in the system when a memory failure occurs. The second section provides a convenient check of the dc voltages required for normal memory operation.

> CAUTION: Failure to perform the mandatory procedures as presented in the subsequent paragraph could result in extensive damage to the MOS RAM elements of the memory array.

5.4.1 Mandatory Procedures

If a malfunction of the computer occurs which is indicative of a memory failure, turn off the computer power switch and perform these mandatory procedures in the following explicit manner:

1. Remove all memory boards except one (top slot) from the mainframe chassis.

2. Place the multimeter probes across zener diode CR8 of the inserted board with the negative (-) probe on the anode and the positive (+) probe on the cathode.

3. Turn on the computer power switch, observe the voltage reading on the multimeter, and turn the computer power switch off.

4. If the multimeter registered -5 volts plus or minus 0.25 volt as observed in step 3, proceed to step 6.

5. If the multimeter did not register -5 volts plus or minus 0.25 volt as observed in step 3, correct the malfunction before proceeding with step 6. Note that there are two -5-volt dc circuits with an exclusive OR output to prevent memory operation when one circuit malfunctions.

6. Place the positive (+) probe of the multimeter in TP1 of the inserted board and the negative (-) probe in TP5.

7. Turn on the computer power switch, observe the voltage reading on the multimeter, and turn the computer power switch off.

8. If the multimeter registered +5.2 volts plus or minus 0.26 volt as observed in step 7, proceed to step 10.

9. If the multimeter did not register +5.2 volts plus or minus 0.26 volt as observed in step 7, correct the malfunction before proceeding with step 10.

10. Remove the inserted memory board, insert another of the memory boards removed in step 1, as applicable, and repeat steps 2 through 9 until all system memory modules have been checked for the indicated voltages; then proceed to step 11.

11. Replace all memory boards in the mainframe chassis and perform the checks, adjustments, tests, and trouble-shooting procedures given in subsequent paragraphs, as required.

5.4.2 Normal Procedures

Except as indicated, ensure that the dc voltages applied to the memory board are within 5 percent of their nominal values by measuring them at the following pins of connector P1:

+20 volts (±10 percent) at pin B1 with respect to ground

+5.2 volts (memory) at pin B5 with respect to ground

Ensure that the dc voltages generated internally by circuits of the memory are within 5 percent of their nominal values by measuring between the indicated test points:

+12 volts between TP4 and TP5 (gnd)

+5.2 volts (+5M) between TP1 and TP6 (gnd)

+5 volts (+5AD) between TP2 and TP7 (gnd)

+5 volts (+5S) between TP3 and TP8 (gnd)

+5 volts (+5L) between TP9 and TP5

-5 volts between TP10 and TP5

5.5 CYCLE TIME ADJUSTMENTS

To determine the precise cycle time of 660 nanoseconds required for proper memory operation, use the oscilloscope to monitor the CYCL- signal at pin 8 of IC67 and perform the following procedures:

1. Connect the oscilloscope trigger to a common jumper between TP13 and TP14.

2. Connect the oscilloscope ground to TP8.

3. With the memory test program in a dynamic loop for reading and writing data, the CYCL- signals should display timing between 640 and 660 nanoseconds from the negative going edge of one signal to the negative going edge of the next.

4. If CYCL- timing is out of tolerance, return the memory board to the factory for adjustment under warranty. Note that this adjustment is sealed and the warranty will be void if the seal is broken. If the memory board is out of warranty, adjust R27 until the timing is within the required limits.

5. If CYCL- timing is out of tolerance after attempting to adjust R27, turn R27 fully clockwise and adjust R26 until the negative going edges of the two CYCL- signals are approximately 800 nanoseconds apart then repeat step 4.

6. If there are no signals present refer to section 5.7.

5.6 MEMORY ACKNOWLEDGMENT ADJUSTMENT

To determine the proper width of 178 nanoseconds for each of the memory acknowledgment signals, use the oscilloscope to monitor YDNMA- at TP11 and YDNMB- at TP12 and perform the following procedures:

1. Connect the oscilloscope trigger to terminal E8.

2. Connect the oscilloscope ground to TP8.

3. With the memory test program in a dynamic loop for reading and writing data, the pulse width of YDNMA- and YDNMB- displayed on the oscilloscope should be 178 plus or minus 5 nanoseconds at the 1.5 volt level.

4. If the pulse width of YDNMA- and YDNMB- is out of tolerance, adjust R16 until the pulse width is within the required limits.

5.7 GENERAL EXERCISE TEST

With the memory test program in a dynamic loop for reading and writing data, check the following signals with the oscilloscope at the indicated test points:

Signal	Test Point	Scope Trigger	Scope Ground
A-	TP13	A1-12	TP8
B-	TP14	A1-9	TP8
R-	TP15	A1-4	TP8
CSA and CSB	IC74-6	TP13 and TP14 (jumper)	TP8
COLSEL+	IC60-12	IC60-4	TP8
ROWSEL+	IC60-10	IC60-3	TP8
DIENAR+	IC53-8	IC74-8	TP8
DIENBR+	IC54-8	IC74-8	TP8
DIENAL+	IC53-6	IC74-8	TP8
DIENBL+	IC54-6	IC74-8	TP8
DOENAR+	IC61-8	IC74-8	TP8
DOENBR+	IC62-8	IC74-8	TP8
DOENAL+	IC61-6	IC74-8	TP8
DOENBL	IC62-6	IC74-8	TP8
RAS15A	IC75-8	IC74-12	TP8
RAS15B	IC75-12	IC74-12	TP8
CASA	IC100-15	IC60-3	TP8
CASB	IC500-15	IC60-3	TP8
CASC	IC900-15	IC60-3	TP8
CASD	IC1300-15	IC60-3	TP8
RA6C+	IC44-12	IC50-6	TP8
DS+5C-	IC91-6	IC44-12	TP8

5.8 REFRESHER TEST (POWER LOSS)

To check the refresher logic, turn the power switch, on the control panel, to the hold position. Place the oscilloscope probe on IC44-12 (RA6C+) and observe that the signal goes high every 2 milliseconds. If the system has the data-save option, simulate a power failure (trip circuit breaker on computer power supply) and observe that the RA6C+ signal goes high every 2 milliseconds. If RA6C+ does not go high approximately every 2 milliseconds (maximum), check the +5SUP output at IC92-2 and the R- output at TP15. Also check to see if the +5M voltage is on continuously.

5.9 REFRESHER TEST (POWER ON)

To check the refresher logic with computer power on, place the oscilloscope probe on IC60-2 (R+) and observe that the signal goes high approximately every 30 microseconds (maximum). This occurs with or without memory requests on port A and port B. If the R+ signal occurs within a time period above the maximum 30 microseconds, check the timing of one-shot IC81.

5.10 TROUBLESHOOTING DATA ERRORS

The MOS RAM IC's of the memory array are arranged on the memory PC board in such a way that data errors can be isolated to the faulty MOS RAM with little effort. Figure 5-1 shows the MOS RAM layout of a 16-bit 64K memory array (16K and 32K not shown). Each row of MOS RAM's provides the storage locations for 4096 (4K) 16-bit words of memory data. From top to bottom, the MOS RAM rows comprise memory capacities of 4K through 64K in multiples of 4K-word increments. Each MOS RAM in a row contains 4096 1-bit memory cells. From column 1 to column 8 and from row 10 to row 17 of the array, the MOS RAM IC's comprise bit 0 through 15, respectively. Column 9 and row 18 represent associated parity bits. The IC designations conform to the number of rows of RAM IC's (from top to bottom) and the bit designation for each column. Thus the 16 bits for the first 4K-word increment are located in IC100 through IC115 of row 1, for the second 4K increment (8K) in IC200 through IC215 of row 2, etc. The two parity bits for each 4K increment are located in ICn16 and ICn17 where n represents the row number.

5.11 CIRCUIT-COMPONENT IDENTIFICATION

Each discrete component of the memory board is identified by a reference designator. This reference designator appears on both the PC board adjacent to the associated component and the logic diagrams within or adjacent to the component symbol. For integrated circuit (IC) components, the IC reference designator appears

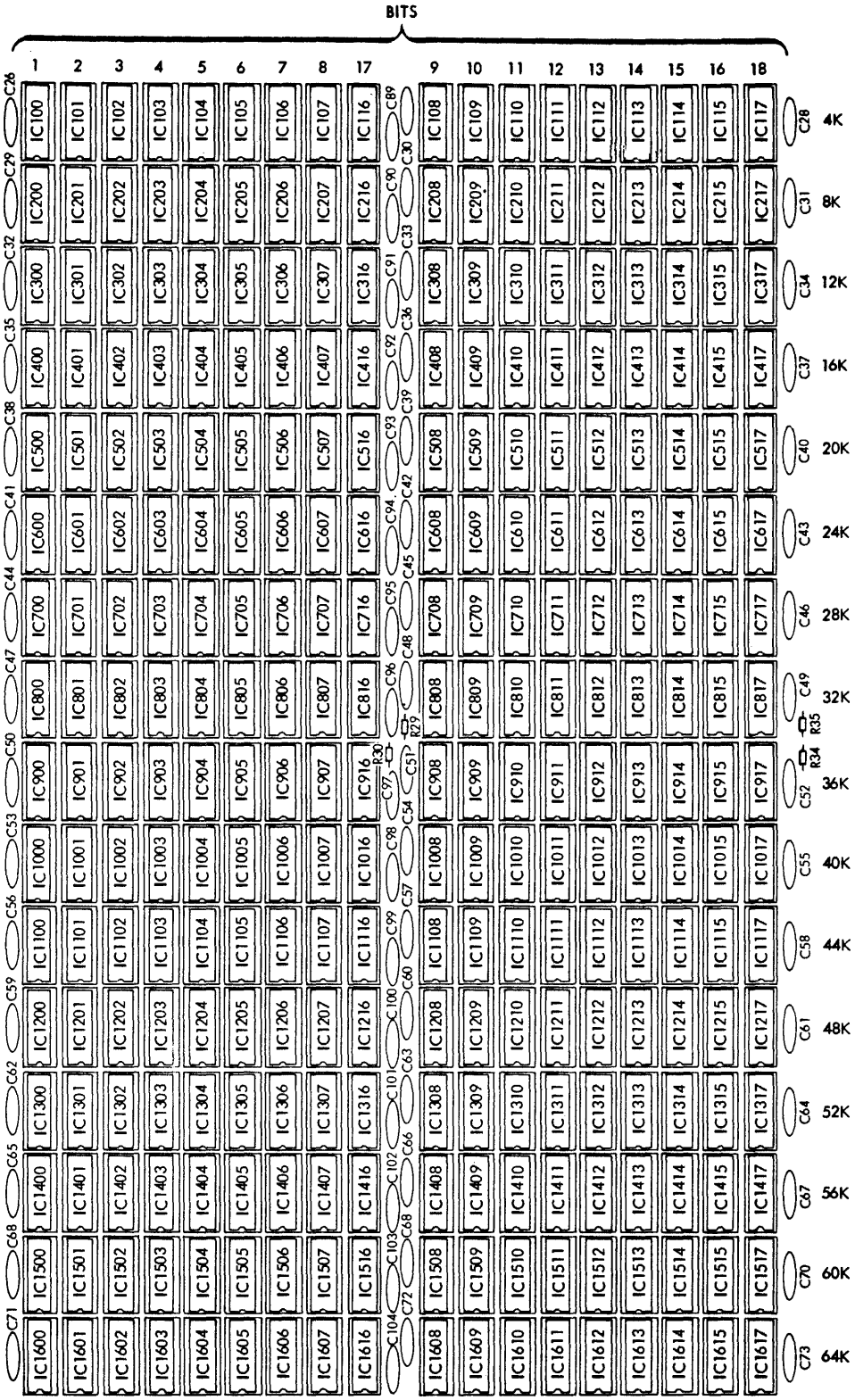

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Figure 5-1. MOS RAM Layout of 16-Bit 64K Memory Array

on the PC board next to the IC package and within each associated logic symbol on the logic diagrams. The individual logic circuits of a multi-circuit IC can be identified on the logic diagrams and located on the PC board by the IC pin numbers. The numeral 1 appears on the PC board adjacent to pin 1 of each IC package.

SECTION 6
MNEMONICS

Mnemonic	Description
A+	Complement memory cycle in progress from port A
A-	Memory cycle in progress from port A
A008 A016 A024 A032 A040 A048 A056 A064 A108 A116 A124 A132 A140 A148 A156 A164 A208 A216 A224 A232 A240 A248 A256 A264 A308 A316 A324 A332 A340 A348 A356 A364 A408 A416 A424 A432 A440 A448 A456 A464 A508	Row and column address drivers for routing address information from ports A or B or from refresh counter to MOS RAM elements

Mnemonic	Description
A516 A524 A532 A540 A548 A556 A564	
B+	Complement memory cycle in progress from port B
B-	Memory cycle in progress from port B
CASA- CASB- CASC- CASD-	Strobe signals for enabling column address information to be accepted by MOS RAM elements
COLSEL+	Timing signal for selecting MOS RAM column address
CSA- CSB-	Chip-selection signal for selecting row and column addressing of MOS RAM elements during refresh cycles and row addressing only during memory cycles
CYCL-	Enables address driver selection for all operating cycles
CYHO+	Enables delayed timing for row address strobe selection
CYHO-	Samples refresh burst request (RB+) for active or inactive state of refresh cycle priority logic
DI00 through DI07	Input data bits of right input byte of 16-bit input data word selected from either A or B port
DI08 through DI15	Input data bits of left input byte of 16-bit input data word selected from either A or B port
DI16	Parity bit for right input byte selected from A or B port
DI17	Parity bit for left input byte selected from A or B port

Mnemonic	Description
DIENAL+	Enables left data input byte selection from port A
DIENAR+	Enables right data input byte selection from port A
DIENBL+	Enables left data input byte selection from port B
DIENBR+	Enables right data input byte selection from port B
DO00 through DO07	Output data bits of right output byte of 16-bit output data word selected from either A or B port
DO08 through DO15	Output data bits of left output byte of 16-bit output data word selected from either A or B port
DO16	Parity bit for right output byte selected from A or B port
DO17	Parity bit for left output byte selected from A or B port
DOENAL+	Enables left data output byte selection from port A
DOENAR+	Enables right data output byte selection from port A
DOENBL+	Enables left data output byte selection from port B
DOENBR+	Enables right data output byte selection from port B
DS+5C-	Enabling and disabling signal for +5S and +5AD voltage control
DUN+	Trigger for generating port A or B memory acknowledgment signal
ENDC-	End of cycle
ENDT-	End of cycle timing
IRST-	Internal reset

Mnemonic	Description
MA00 through MA05	Multiplexed address bits selected from ports A or B or from refresh counter
MA12+	Memory address bit selected from port A or B for row addressing of MOS RAM elements
MA12-	Complement memory address bit selected from port A or B for row addressing of MOS RAM elements
MA13+	Memory address bit selected from port A or B for row addressing of MOS RAM elements
MA13-	Complement memory address bit selected from port A or B for row addressing of MOS RAM elements
MA14+	Memory address bit selected from port A or B for row addressing of MOS RAM elements
MA14-	Complement memory address bit selected from port A or B for row addressing of MOS RAM elements
MA15+	Memory address bit selected from port A or B for enabling row addressing of MOS RAM elements
MA15-	Complement memory address bit selected from port A or B for enabling row addressing of MOS RAM elements
MHGY-	Port B priority modifier (inhibits port A)
MHMY-	Port A priority modifier (inhibits port B)
MRQYA-	Memory start request for starting port A memory cycle
MRQYB-	Memory start request for starting port B memory cycle
MRQYR-	Auxillary memory start request from error correction circuit for starting refresh cycle
MWLYA+	Read/write control for left data byte of port A

Mnemonic	Description
MWLYB+	Read/write control for left data byte of port B
MWRYA+	Read/write control for right data byte of port A
MWRYB+	Read/write control for right data byte of port B
MYAA00+ through MYAA15+	Memory address bits for port A
MYAB00+ through MYAB15+	Memory address bits for port B
MYDA00- through MYDA15-	Memory input/output data bits for port A
MYDA16-	Parity bit for first input/output data byte of port A
MYDA17-	Parity bit for second input/output data byte of port A
MYDB00- through MYDB15-	Memory input/output data bits for port B
MYDB16-	Parity bit for first input/output data byte of port B
MYDB17-	Parity bit for second input/output data byte of port B
R+	Complement refresh cycle in progress
R-	Refresh cycle in progress
RA1- RA2-	Refresh timing for enabling refresh cycle logic
RA00 through RA05	Refresh address bits from refresh counter

Mnemonic	Description
RA6C+	Trigger for generating two millisecond time for power down
RA6L-	Enabling signal for refresh burst request and refresh cycle priority
RAS00- through RAS15-	Strobe signals for enabling row address information to be accepted by MOS RAM elements
RAS15A RAS15B	Enabling signals for row address strobes
RB+	Refresh burst request
RL+	Read output enabling signal for left data byte
ROWSEL+	Timing signal for selecting MOS RAM row address drivers
RR+	Read output enabling signal for right data byte
SPFA-	System power failure alarm signal for initiating normal memory operation
SRST-	System reset signal for initiating normal memory power
STS+	Enables power for initiating both memory and refresh cycles
T1+ through T16+	Internal timing signals for sequential memory cycle operation
T1- through T16-	Complementry internal timing signals for sequential memory cycle operation
WL+	Write input enabling signal for left data byte selection
WLBA- WLBB-	Write enabling signal for left data byte input to MOS RAM elements