SPERRY UNIVAC

MAINTAIN III Communications Equipment and Controllers Test Programs

User Guide

Mini-Computer Operations

2722 Michelson Drive
P.O. Box C-19504
Irvine, California 92713

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SPERRY UNIVAC®

MAINTAIN III

Communications Equipment and Controllers Test Programs

User Guide

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Part 1
Introduction

Part 1 of the MAINTAIN III Communications Equipment and Controllers Test Program User Guide contains an introduction and information on the SPERRY UNIVAC MAINTAIN III Test System.

This part of the user guide consists of:

Section 1 - INTRODUCTION. Contains the scope of the manual, description of MAINTAIN III, conventions used, tape loading procedures, SENSE switch description, and related documentation.

Section 2 - EXECUTIVE PROGRAM. Contains a description of the MAINTAIN III executive, operating procedures, error messages, and test examples.

Section 1
Introduction

1.1 GENERAL

This manual describes those parts of the SPERRY UNIVAC MAINTAIN III Test Program System that are used in SPERRY UNIVAC communications equipment and controllers. The system is used for verifying correct operation and the detection and isolation of malfunctions.

The user who executes these tests must be familiar with:

- the instruction set of the equipment on which these programs are used,
- assembly-language programming,
- operating procedures for the computer control panel or virtual console,
- and operating procedures for the peripheral devices on the system under test.

Control panel operating procedures are described in the appropriate system manuals.

1.2 SCOPE

The organization of this manual is based on the MAINTAIN III Program System. The first section presents an overview of the test system. The sections that follow the overview describe the components (test) of the test system. Except for Sections 1 and 2, each section comprises a test for a related equipment, e.g., terminal, data communications, or controller.

In the presentation for any given test, the user finds:

- A test design description.
- A test structure.
- Preliminary procedures; such as loading the media and setting sense switches.
- Execution procedures.
- Error indications that can occur during program execution or cause termination of the test.

- Examples of loaded parameters and program output.

As new systems are developed, the existing test system is expanded to include the new system. In those cases where tests are applicable to more than one system, reference is made to those systems.

1.3 DESCRIPTION OF MAINTAIN III

MAINTAIN III is a systematic approach to testing and maintaining SPERRY UNIVAC V70-series computers and related equipment. The tests provide an interface between the equipment under test, the computer, and the user.

Test programs in this manual cover only the communications equipment and associated controllers. The programs are to be used in conjunction with appropriate servicing manuals which include theory of operation, installation, and maintenance information.

MAINTAIN III test programs are designed to verify correct system operation. Malfunctions can be detected and isolated to a specific area of the system.

A MAINTAIN III test programs object file directory is contained in the current edition of the MAINTAIN III Test System Software Release Description, part number 92W0106-013xx.

1.3.1 STRUCTURE

The MAINTAIN III system consists of the components illustrated in Figure 1-1.

The executive program includes a preliminary instruction test, preliminary memory test, binary object loader, and executive. The program:

- Loads test programs.
- Accepts control directives and parameters from the user.
- Executes test programs.
- Contains a utility package comprising aids for debugging, for program maintenance, and for hardware troubleshooting.
- Includes standard test program subroutines, i.e., teletypewriter (TTY) input/out (I/O), time delay, memory size determination, SENSE switch option, etc.

The preliminary instructions test portion of the executive program validates basic CPU operation. The preliminary memory test checks basic functions of the first 8K memory module. The binary loader reads binary data and stores it in memory.

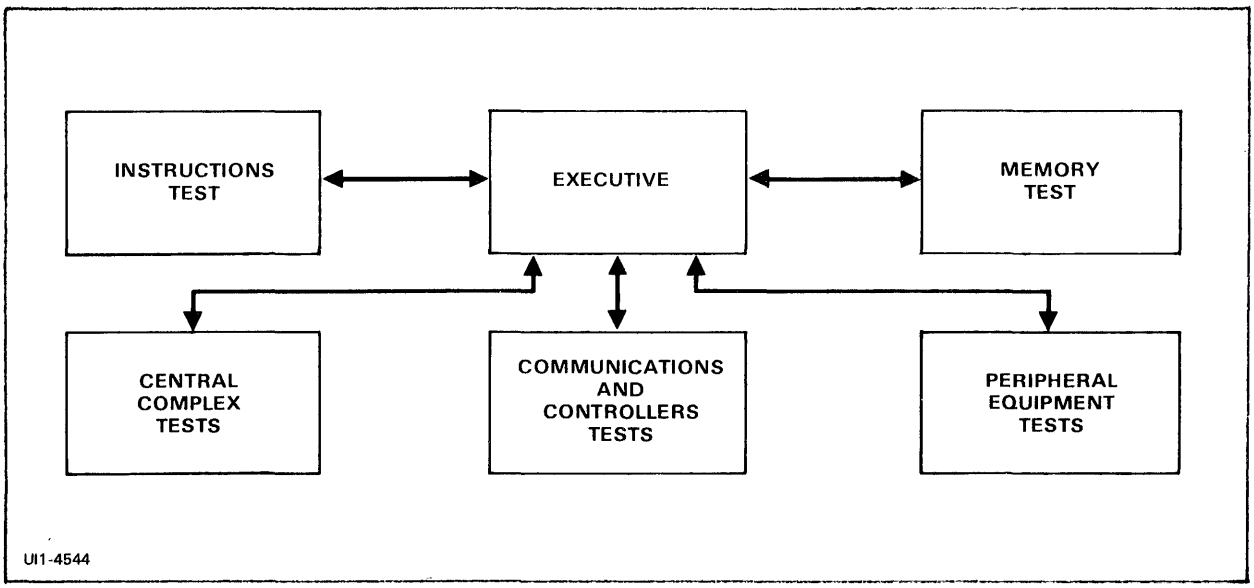

Figure 1-1. MAINTAIN III System Block Diagram

Test programs are available for the V77 central complex, communications equipment and controllers, and peripheral equipment. Refer to section 1.7 for related information.

Central complex test programs test the central processor (instruction test), main memory, and computer options.

Communications and controllers test programs verify correct operation of communications devices such as terminals, data communications multiplexers, and line adapters. Controllers that are not associated with specific peripheral equipment are also tested.

Peripheral equipment test programs verify correct operation of system peripherals such as line printers, disks, and paper tape systems. Associated controllers are tested with the peripherals.

1.3.2 MAINTENANCE CONCEPTS

MAINTAIN III minimizes system maintenance time for the V70-series computers. Test programs are executed when the computer is offline and not transferring data or performing control functions. Test programs are normally furnished on punched paper tape; however, other media such as object card decks, magnetic tape, or disk are also available.

The programs exercise the central complex, communications equipment, peripheral equipment, and associated controllers with sequences of instructions. If an instruction is improperly executed, the sequence is halted and an error message is produced to indicate the failing instruction or operation. The user can then repeat, continue, or halt the program until the fault is isolated or corrected. The recommended procedure for correcting hardware malfunctions is:

1. Isolate the fault to a functional area, such as memory, control, arithmetic/logic, operations register, I/O, communications device or peripheral equipment.

2. Execute, repeat, or modify the applicable test program for the area of the suspected fault.

3. Correct the fault by replacing the faulty component or printed-circuit board and restore the system to normal operation.

4. Verify system operation by rerunning the test program.

Servicing manuals appropriate to the user's system contain a description of the major components of the computer's central complex, communications devices, and peripheral equipment.

Specific operating procedures for applicable MAINTAIN III test programs are given in this manual. The procedures also include descriptions of error conditions and error messages. While operating the test program, all input and output messages are via the virtual console. A virtual console is defined as a teletypewriter or keyboard-display terminal which is used as an interface between the computer and the operator.

1.4 CONVENTIONS USED

In the operational procedures, a required operator response is designated by an underscored R (R). The R indicates that a program pause is encountered and that a response is to be made before the program continues. Responses or messages generated by the computer program are not underscored.

Unless a specific computer model is called out, the term V70 refers to V72, V73, V75, V76, and V77 series. The term V77 refers to all V77 series computers such as V77-200, V77-400, V77-600, and V77-800.

1.5 TEST PROGRAM LOADING

For paper tape systems, the procedure for loading the test program is as follows:

1. Place the test program tape in the paper tape reader.

2. Position the tape within the leader area between the test part number and the start of the program.

3. Enter an L. on the virtual console.

Magnetic tape systems require the use of file numbers. The procedure for loading the test program is as follows:

1. Consult the MAINTAIN III Software Release Description for the file number of the test program to be used.

2. Position the tape reel on transport.

3. Position the tape to the required test program file number by using MAINTAIN III tape commands (paragraph 2.4.2.1).

4. Load the test program by using magnetic tape commands.

1.6 SENSE SWITCH SETTINGS

Unless otherwise indicated, SENSE switch settings can alter the test program operation as follows:

SENSE Switch	Set Position	Reset Position
1	Suppress error printout. If no TTY, suppress error halt.	Print error messages. If no TTY, halt.
2*	Halt on error. (Continue testing.)	Do not halt on error. (Loop on error.)
3	Terminate test and return to start of test.	Continue testing.

* Following an error halt, SENSE switch 2 can be used to continue the test or to loop on the error:

  . To continue testing, leave the SENSE switch set and depress R on the virtual console or the START switch on the computer control panel.

  . To loop on an error, reset the SENSE switch and depress R on the virtual console or the START switch on the computer control panel. Looping continues until the switch is set, the program then continues in the "halt on error" mode until the next error halt.

1.7 RELATED DOCUMENTATION

Documentation containing information associated with the operation of MAINTAIN III tests are listed in Table 1-1.

Table 1-1. Reference Documents

Document and Part Number	Document Title	Use
UP-8634 98A 9906 00x	V70 Series Architecture Reference Manual	Contains description of the V70 series instruction set, data and instruction formats, and addressing modes.
UP-8651 98A 9906 40x	V77-600 Computer System Description Manual	Contains program loading procedures as well as operating procedures for the computer control panel.
UP-8652 98A 9906 41x	V77-400 Computer System Description Manual	Contains program loading procedures as well as operating procedures for the computer control panel.
UP-8653 98A 9906 42x	V77-200 Computer System Description Manual	Contains program loading procedures as well as operating procedures for the computer control panel.
UP-8672 98A 9952 07x	MAINTAIN III Test Programs User Manual	Contains procedures for use of V77 central complex test programs.
UP-8877 98A 9952 95x	MAINTAIN III Peripheral Equipment Test Programs User Guide	Contains procedures for use of test programs for V77 peripheral equipment and controllers.
UP-9028 98A 9906 70x	V77-800 Operations Manual	Contains program loading procedures as well as operating procedures for the computer control panel and virtual console.

The x that appears at the end of each document number is the revision number and can be any of the digits 0 through 9.

Section 2
Executive Program

2.1 GENERAL

The Executive Program is the program that controls the execution of other programs in the MAINTAIN III test program system. In addition to loading, executing, and monitoring the other MAINTAIN III test programs, the executive program:

- Provides utility aids for debugging, program maintenance, and hardware troubleshooting.
- Includes standard subroutines for use by associated test programs, i.e., teletypewriter (TTY) input/output (I/O), time delay/time out, memory size determination, power failure/restart protection, SENSE switch options, etc.

2.2 HARDWARE REQUIREMENTS

The executive program minimum hardware configuration is as follows:

- V70 series computer with 8K of memory.
- A CPU control panel or a virtual console (teletypewriter or keyboard-display terminal).
- A program loading device for the object test media.

2.3 DESCRIPTION OF TEST COMPONENTS

The executive program consists of:

- Preliminary instructions test
- Preliminary memory test
- Binary loader
- Executive

Figure 2-1 illustrates the operation of the executive.

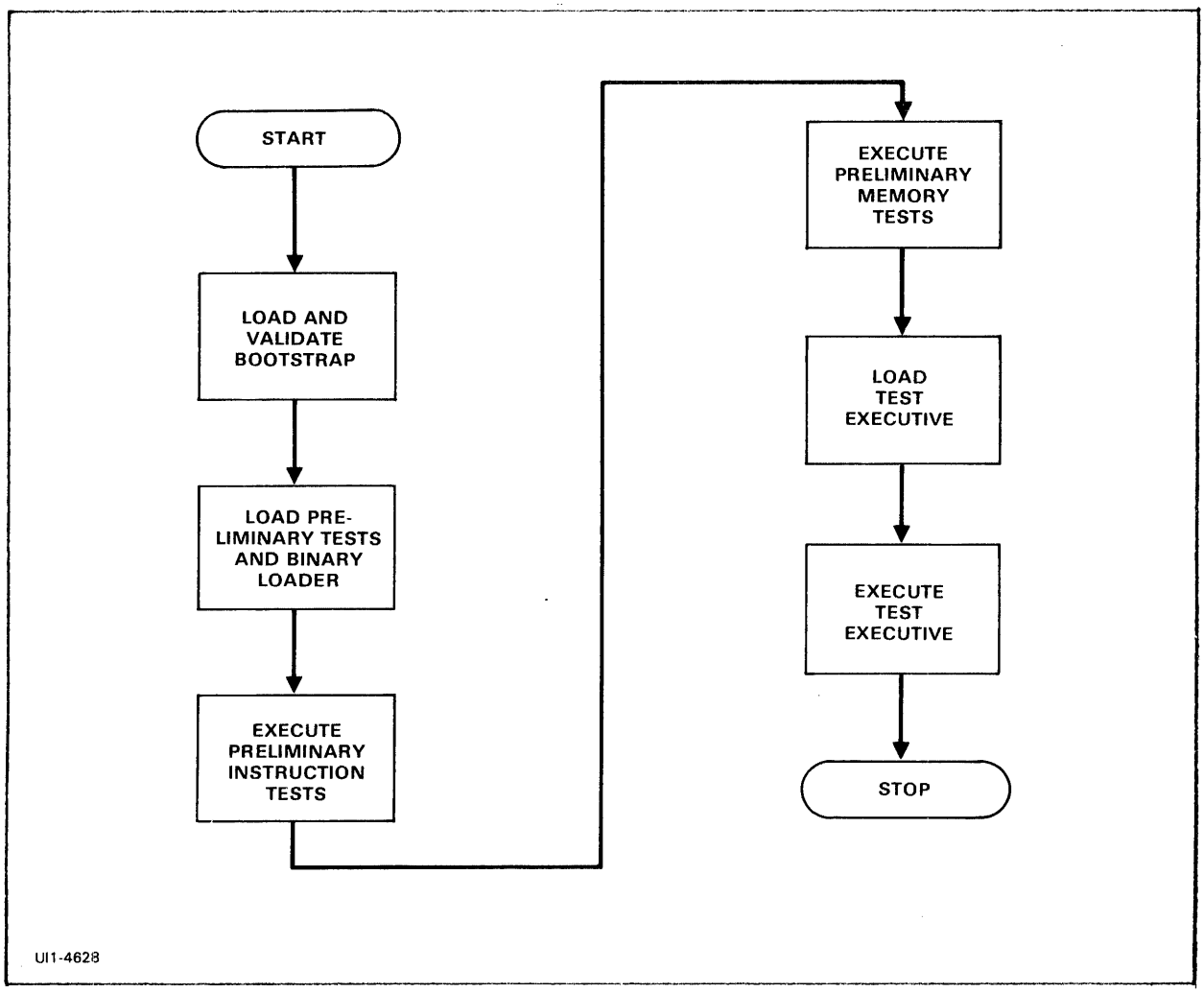

Figure 2-1. Executive Block Diagram

2.3.1 BINARY LOADER

The binary loader loads formatted object data into computer memory, computes the checksum, and transfers program control as directed.

2.3.2 PRELIMINARY INSTRUCTIONS TEST

The preliminary instructions test validates central processing unit (CPU) operation by testing the machine instructions listed in Table 2-1. Successful execution of this test indicates that MAINTAIN III test programs can be loaded correctly if loading procedures are followed.

Table 2-1. Preliminary Instructions Test Summary

Mnemonic	Description
ADD	Add memory to A register
ADDI	Add immediate
ANAI	AND immediate
DAR	Decrement A register
DBR	Decrement B register
DECR 02	Set B register to -1
DXR	Decrement X register
ERA	Exclusive-OR memory and A register
ERAI	Exclusive-OR immediate
IAR	Increment A register
IBR	Increment B register
INCR 03	Set A and B registers to +1
IXR	Increment X register
JAN	Jump if A register negative
JAP	Jump if A register positive
JAZ	Jump if A register zero
JBZ	Jump if B register zero
JIF 011	Jump if A register = 0 and OVFL is set
JMP	Jump (unconditional)
JMPM	Jump and mark (unconditional)
JMP*	Jump indirect
JOF	Jump if overflow indicator set
JXZ	Jump if X register zero
LDA	Load A register
LDAI	Load A register immediate
LDB	Load B register
LDBI	Load B register immediate
LDX	Load X register
LDXI	Load X register immediate
LLRL	Long logical rotation left
LLSR	Long logical rotation right
LRLA	Logical rotation left A register
LSRA	Logical shift right A register
MERG 032	Transfer ORed A and B registers to B register
NOP	No operation
ORAI	Inclusive-OR immediate
ROF	Reset overflow indicator
STA	Store A register
STAI	Store A register immediate
STB	Store B register
STX	Store X register
SUB	Subtract memory from A register
TBA	Transfer B register to A register
TBX	Transfer B register to X register
TXA	Transfer X register to A register

Table 2-1. Preliminary Instructions Test Summary (Continued)

Mnemonic	Description
TZA	Transfer zero to A register
TZB	Transfer zero to B register
TZX	Transfer zero to X register
XAZ	Execute if A register zero
XBZ	Execute if B register zero
XIF 022	Execute if B register = 0 and A register ≥ 0

2.3.3 PRELIMINARY MEMORY TEST

The preliminary memory test verifies correct operation of the first 8K of memory. Memory addresses 000044 through 017777 (8K) are tested in two passes. The first pass checks each address with a pattern of 052525_8; the second pass, 012525_28. The original contents of memory are saved and restored by the program.

2.3.4 EXECUTIVE

The executive is an integral part of the MAINTAIN III test program system. In addition to providing test control and user interface, it contains standard subroutines commonly required by the associated test programs, i.e., TTY, I/O routines SENSE switch routines, etc.

The executive program utility package consists of aids for debugging, program maintenance, and hardware troubleshooting. The capabilities are:

- CPU registers and memory can be displayed or altered.
- The user can specify memory data pattern searches.
- Areas of memory can be set to specified data patterns.
- Object code can be punched or written.
- During execution, test programs can be trapped.

Utility routines are summarized in Table 2-2; standard executive data items, in Table 2-3; and standard I/O routines, in Table 2-4. Refer to the listing supplied with the program for the entry addresses of these routines.

Table 2-2. Executive Utility Routines

Mnemonic	Description
EARG	Print/change the contents of the pseudo-A register
EBPN	Punch a tape on the TTY (binary)
EBRG	Print/change the contents of the pseudo-B register
ECNG	Print/change the contents of memory
EDUM	Dump (print) the contents of memory on the TTY
EGOT	Transfer to the specified address
EPUN	Punch a tape on the TTY (object)
ESRC	Search memory
ETRP	Trap to the specified address
EXRG	Print/change the contents of the pseudo-X register
INIT	Initialize memory

Table 2-3. Executive Data Items

Mnemonic	Description
$CON	Value of 1
$DCT	Digit counter for I/O routine INPG
$FLG	Loop on error flag
$LWE	Lowest address used by executive
$MEM	Highest available memory address
MSG3	Memory size message
$TTY	TTY device address

Table 2-4. Executive I/O Routines

Mnemonic	Description
ESZC	Determine memory size
INPA	Input one character
INPB	Input and print one character
INPC	Input one edited character
INPD	Input one alphabetic character
INPE	Input two alphabetic characters
INPF	input terminating control character
INPG	Input octal number
INPH	SENSE TTY buffer ready
INPI	Initialize TTY (clear input buffer)

Table 2-4. Executive I/O Routines (Continued)

Mnemonic	Description
OUTA	Output one character
OUTB	Output two characters
OUTC	Output carriage return and line feed
OUTD	Output message
OUTE	Output octal word
OUTF	Output octal address
OUTG	Output typing error message
OUTH	Output control character
SSWT	Standard SENSE switch routine
TDLY	Time delay
TOUT	Time out

2.4 OPERATING PROCEDURES

A variety of program loading devices are available for use with Sperry Univac computers. When using the folowing general procedures, the operator must determine what equipment is in use and then follow the detailed procedures described in the appropriate manual.

Operating procedures for the V77 series control panels and virtual consoles are contained in the applicable V77 series operations or system description manuals (Table 1-1).

2.4.1 PRELIMINARY PROCEDURES

After bringing up computer system power:

1. Enter step mode.

2. Reset SENSE switches 1, 2, and 3.

3. Initialize the computer control circuits by activating RESET. If using a virtual console, enter an A to reset the system.

4. Load the object program. Use the applicable following procedure:

   If using the high-speed paper tape (HSPT) reader, set the LOAD/RUN switch to LOAD. Position the tape in the reader with the first nonblank binary frame at the read station. Set the LOAD/RUN switch to RUN. Skip to step 5.

When using the high-speed paper tape reader punch, open the cover of the read head and insert tape. Position the tape in the reader with the first nonblank binary frame at the read station. Close the cover of the read head. Skip to step 5.

NOTE

The Sperry Univac part number is punched in the leader portion the object tape, e.g., 92U0106-013x in the executive tape, where x indicates the revision level.

If the TTY is used, initialize the TTY by setting control to LOCAL (off-line). Type CONTROL, D, T, and Q. Return control to LINE (on-line). Position test program tape in the reader with the first nonblank binary frame at the reading station. Set the reader control switch to STOP. Skip to step 5.

If the computer is equipped with TTY or HSPT automatic bootstrap loader (ABL), initiate RESET. Place the computer in run mode and press BOOT. Skip to step 5.

To use a card reader, place the executive object card deck in the card reader hopper. Place the card reader in the ready status. Skip to step 5.

If using magnetic tape, place the MAINTAIN III test object tape on the appropriate tape drive unit at proper density. Then:

a. Manually load the magnetic tape bootstrap routine listed in Table 2-5 or 2-6. Refer to the appropriate equipment operations manual for loading procedures.

b. Place the MAINTAIN III magnetic tape on the tape unit and position the tape to the load point.

c. Enter 000212 into the P register, 07000 into the X register (register R2 on the virtual console), and zero in the A and B registers (R0 and R1 on the virtual console).

d. Set STEP/RUN to RUN on control panel or press key R on the virtual console to enter the executive into memory.

5. If a magnetic tape unit is not used, enter the test executive program into memory by using one of the following procedures.

   To enter the executive program via the computer control panel, momentarily place the load switch to the LOAD position. The high-speed tape reader (reader-punch) is selected when the load switch is activated.

   If the virtual console is used:

   a. Select the desired program loader routine from the following listing. Reference tables are listed in the event that the routine must be loaded manually.

Program Loader Routine	Loader Code	Reference Table
Teletypewriter paper tape reader	000 000	2-7
High-speed paper tape reader	000 001	2-8
F3094-0x or F3096-0x disk memory	000 002	2-9, 2-10
Type 2842-0x or 2826-0x disk memory	000 003	

   b. Enter the program loader code into register R0 by pressing key 0 on the virtual console and typing the desired code. Press key 0 again to verify the contents of register R0.

   c. Press key B on the virtual console to load the program loader and object program. When the tape stops, press R on the virtual console or set the STEP/RUN switch to RUN on the control console.

   When using a card reader, the program loader routine must be manually loaded. Use the listing in Table 2-11 and the procedures outlined for the magnetic tape unit.

   If the TTY is used, set the reader control switch to START/RUN.

Ater the preliminary tests and binary loader are read into memory, the bootstrap routine jumps to address 007000. The paper-tape reader is turned off. The preliminary instructions test, starting at address 007002, is automatically executed. Following successful execution of the instructions

test, the program automatically executes the preliminary memory test. The program then jumps to the binary loader, which loads the executive. Setting SENSE switch 3 during execution causes the program to loop on the combined preliminary instructions and memory tests.

Preliminary test error conditions are described in paragraph 2.5.

Table 2-5. Magnetic-Tape Bootstrap Routine

Instruction Address	Code	Symbolic Coding
		1 * MAGNETIC TAPE BOOTSTRAP
		2 *
	0000ZZ	3 MT SET ZZ
	00000Y	4 TU SET Y
000200		5 ORG 0200
000200	1012XX	6 MTS SEN 0200+MT,07002 SENSE IF DONE
000201	007002	
000202	1011ZZ	7 SEN 0100+MT,MTST SENSE IF DATA IN
000203	000206	
000204	001000	8 JMP MTS SENSE DATA IN
000205	000200	
000206	1025ZZ	9 MTST CIA MT GET WORD
000207	055000	10 STA 0,1 STORE WORD
000210	001000	11 JMP MTSA
000211	000214	
		12 *
		13 * START HERE WITH X=07000
		14 *
000212	104YZZ	15 ENTR EXC2 (TU*64)+MT SELECT UNIT
000213	1000ZZ	16 EXC MT READ ONE RECORD BINARY
000214	005144	17 MTSA IXR STEP INDEX
000215	001000	18 JMP MTS LOOP
000216	000200	

where:
Y = Drive number 1, 2, 3, or 4
Z = Device address, (normally 010)

Table 2-6. Magnetic Tape Bootstrap Routine (F3093-0x, F3062-00, Type 0870-99, and Type 0870-35 Tape Units)

Instruction Address	Code	Symbolic Coding			
000200	1031WW	BOOT	OAR	BIC	SET INITIAL ADDRESS
000201	005301		DECR	1	A=0177777 FOR LAST ADDRESS
000202	1031XX		OAR	BIC+1	SET FINAL ADDRESS
000203	1000WW		EXC	BIC	ACTIVATE BIC
000204	1000ZZ		EXC	MT	READ ONE RECORD FROM MAG TAPE
000205	1012ZZ	WAIT	SEN	0200+MT,07002	TO START IF MAG TAPE READY
000206	007002				
000207	005000		NOP		
000210	001000		JMP	WAIT	LOOP UNTIL READY
000211	000205				
		.		START AT 0212	WITH X=07000
		.			
		.			
000212	1000XX	START	EXC	BIC+1	INITIALIZE BIC
000213	104YZZ		EXC2	(TU*0100)+MT	SELECT MAG TAPE UNIT
000214	005141		INCR	041	SET A+07001 (START ADDRESS)
000215	001000		JMP	BOOT	START BIC
000216	000200				

where:

WW=Even BIC device address
XX=Odd BIC device address
Y =Drive number 1, 2, 3, or 4
ZZ=MT device address

Table 2-7. Teletypewriter Paper-Tape Bootstrap Routine

Instruction Address	Instruction Code	Symbolic Coding
		1 * TELETYPEWRITER PAPER TAPE BOOTSTRAP
		2 *
	0000ZZ	3 TY SET ZZ
000200		4 ORG 0200
000200	1026ZZ	5 READ CIB TY 8 BITS TO B
000201	004011	6 ASLB 9 SAVE LS6
000202	004041	7 LRLB 1
000203	004446	8 LLRL 6 MERGE INTO A
000204	001020	9 JBZ SEL MORE IF B ZERO
000205	000214	
000206	055000	10 STA 0,1
000207	001010	11 JAZ 07000 EXIT IF ZERO
000210	007000	
000211	005144	12 IXR STEP INDEX
		13 *
		14 * START HERE WITH X=07000
		15 *
000212	005101	16 ENTR INCR 1 SET A BIT 0
000213	1026ZZ	17 SEL CIB TY CLEAR TTY BUFFER
000214	1012ZZ	18 SEN 0200+TY,READ SENSE READ READY
000215	000200	
000216	001000	19 JMP *-2 LOOP
000217	000214	

where: Z = Device address, (normally 01)

Table 2-8. High-Speed Paper-Tape Bootstrap Routine

Instruction Address	Instruction Code	Symbolic Coding			
		1 *	HIGH-SPEED PAPER TAPE BOOTSTRAP		
		2 *			
	0000ZZ	3 PT	SET	ZZ	
000200		4	ORG	0200	
000200	1026ZZ	5 READ	CIB	PT	8 BITS TO B
000201	004011	6	ASLB	9	SAVE LS6
000202	004041	7	LRLB	1	
000203	004446	8	LLRL	6	MERGE INTO A
000204	001020	9	LBZ	SEL	MORE IF ZERO
000205	000214				
000206	055000	10	STA	0,1	STORE WORD
000207	001010	11	JAZ	07000	EXIT IF ZERO
000210	007000				
000211	005144	12	IXR		STEP INDEX
		13 *			
		14 *	START HERE WITH X=07000		
		15 *			
000212	005101	16 ENTR	INCR	1	SET A BIT 0
000213	1005ZZ	17 SEL	EXC	0500+PT	READ A FRAME
000214	1015ZZ	18	SEN	0500+PT,READ	SENSE READ READY
000215	000200				
000216	001000	19	JMP	*-2	LOOP
000217	000214				

where: Z = Device address, (normally 037)

Table 2-9. Disk Bootstrap Routine
(F3094-0x and F3096-0x RMD)

Instruction Address	Code	Symbolic Coding			
001130	1004ZZ	START	EXC	0400+DISK	INITIALIZE DISK
001131	011167		LDA	DBUNT	POSITION TO CYLINDER
001132	1002ZZ		EXC	0200+DISK	
001133	1031ZZ		OAR	DISK	
001134	101XZZ	SLP	SEN	(UNIT*01000) +DISK,GO	GO SEEK COMPLETE?
001135	001140				
001136	001000		JMP	SLP	NO. LOOP
001137	001134				
001140	1025ZZ	GO	CIA	DISK	CHECK STATUS
001141	151166		ANA	DBSTS	
001142	001010		JAZ	GOOD	I.O ERROR
001143	001145				
001144	000000		HLT		
001145	011167	GOOD	LDA	DBUNT	POSITION TO SECTOR
001146	1003ZZ		EXC	0300+DISK	
001147	1031ZZ		OAR	DISK	
001150	1000WW		EXC	BIC+1	INITIALIZE BIC
001151	011170		LDA	DBSRT	SET START
001152	1031VV		OAR	BIC	
001153	011171		LDA	DBEND	SET END
001154	1031WW		OAR	BIC+1	
001155	1000VV		EXC	BIC	ACTIVATE BIC
001156	1000ZZ		EXC	DISK	READ FROM DISK
001157	1014ZZ	BLP	SEN	0400+DISK,BLP	BUSY?
001160	001157				
001161	1025ZZ		CIA	DISK	CHECK STATUS
001162	151166		ANA	DBSTS	
001163	001010		JAZ	0600	START PROGRAM
001164	000600				
001165	000000		HLT		
001166	005760	DBSTS	DATA	05760	STATUS BITS
001167	0Y0000	DBUNT	DATA	(UNIT*020000)	
001170	000000	DBSRT	DATA	0	START LOAD
001171	001130	DBEND	DATA	01130	END LOAD

where:

VV = Even BIC device address
WW = Odd BIC device address
X = Unit number 0, 1, 2, or 3
Y = Unit number times 2
ZZ = Disk device address

Table 2-10. Disk Bootstrap Routine
(Model 70-7607, F3094-0x, F3096-0x,
and F3310-xx RMD)

Instruction Address	Code	Symbolic Coding			
001130	1004ZZ	START	EXC	0400+DISK	INITIALIZE DISK
001131	011167		LDA	DBUNT	POSITION TO CYLINDER
001132	1031ZZ		OAR	DISK	
001133	1002ZZ		EXC	0200+DISK	
001134	101XZZ	SLP	SEN	((UNIT/2)*100) +DISK.	GO SEEK COMPLETE?
001135	001140				
001136	001000		JMP	SLP	NO, LOOP
001137	001134				
001140	1025ZZ	GO	CIA	DISK	CHECK STATUS
001141	151166		ANA	DBSTS	
001142	001010		JAZ	GOOD	NO ERROR
001143	001145				
001144	000000		HLT		
001145	011167	GOOD	LDA	DBUNT	POSITION TO SECTOR
001146	1031ZZ		OAR	DISK	
001147	1003ZZ		EXC	0300+DISK	
001150	1000WW		EXC	BIC+1	INITIALIZE BIC
001151	011170		LDA	DBSRT	SET START
001152	1031VV		OAR	BIC	
001153	011171		LDA	DBEND	SET END
001154	1031WW		OAR	BIC+1	
001155	1000VV		EXC	BIC	ACTIVATE BIC
001156	1000ZZ		EXC	DISK	READ FROM DISK
001157	1014ZZ	BLP	SEN	0400+DISK,BLP	BUSY?
001160	001157				
001161	1025ZZ		CIA	DISK	CHECK STATUS
001162	151166		ANA	DBSTS	
001163	001010		JAZ	0600	START PROGRAM
001164	000600				
001165	000000		HLT		
001166	173760	DBSTS	DATA	0173760	STATUS BITS
001167	0Y0000	DBUNT	DATA	UNIT*020000	SETUP WORD
001170	000000	DBSRT	DATA	0	START LOAD
001171	001130	DBEND	DATA	01130	END LOAD

where:

VV = Even BIC device address
WW = Odd BIC device address
X = Integer of Unit/2
Y = Unit number times 2
ZZ = Disk device number

Table 2-11. Card Bootstrap Routine

Instruction Address	Code					Symbolic Coding
		1	*	CARD	BOOTSTRAP	
		2	*		ZZ	
	0000ZZ	3	CR	SET		
000200		4		ORG	0200	
000200	1025ZZ	5	BOOR	CIA	CR	INPUT ODD COLUMN
000201	004250	6		LRLA	8	MOVE TO HIGH ORDER
000202	1011ZZ	7		SEN	0100+CR,BOOS	SENSE CHARACTER READY
000203	000221					
000204	001000	8		JMP	*-2	LOOP
000205	000202					
000206	001010	9	BOOT	JAZ	07000	END OF PRELIM
000207	007000					
000210	001000	10		JMP	ENTR	
000211	000212					
		11	*			
		12	*		START HERE WITH X=07000	
		13	*			
000212	1002ZZ	14	ENTR	EXC	0200+CR	READ A CARD
000213	1011ZZ	15	BOOU	SEN	0100+CR,BOOR	SENSE CHARACTER READY
000214	000200					
000215	1016ZZ	16		SEN	0600+CR,BOOT	SENSE END OF CARD
000216	000206					
000217	001000	17		JMP	*-4	LOOP
000220	000213					
000221	1021ZZ	18	BOOS	INA	CR	MERGE EVEN COLUMN INTO A
000222	055000	19		STA	0,1	STORE WORD
000223	005144	20		IXR		STEP INDEX
000224	001000	21		JMP	BOOU	MORE ON CARD
000225	000213					

where: Z = Device address, (normally 030)

2.4.2 OPERATING THE EXECUTIVE

This program can be executed using the system virtual console.

When the executive program is loaded and halts with 000000 in the instruction register, check the device address. This procedure assumes that the desired device address is 01; if it is not, load the virtual console device address in the A register. Press START or RUN to start the program.

To start the executive program manually:

1. Clear the instruction register to zero.
2. Load 014000 in the P register.
3. Press RESET, and while in run mode, press START or RUN.
4. Load the desired device address (if the console address is other than 01) in the A register, and press START or RUN

The program begins execution by displaying the identification message:

```
THIS IS THE V70/620 EXECUTIVE
MEMORY SIZE IS nK
```

For a V75/V77 computer system the identification message is:

```
THIS IS THE V75 EXECUTIVE
MEMORY SIZE IS nK
```

where:

n
: Indicates memory size in multiples of 4 (for example, 8, 12, etc.) up to a maximum of 32.

This message is for information only and requires no operator action. At this time, cache memory (if included in the system) is disabled. The executive program then waits for a command input (Table 2-12).

The executive can be restarted at any time by initializing the computer and entering RUN from location 0 or by pressing the console interrupt (INT) switch.

Table 2-12. Executive Utility Routine Commands

Command	Description
A	Print/change the contents of the pseudo-A register.*
B	Print/change the contents of the pseudo-B register.*
Cx.	Print/change the contents of memory address x.
Dx.	Dump (list) memory on the TTY printer beginning at memory address x.
Gz.	Load the contents of the pseudo-registers into the respective A, B, and X registers, and transfer to memory address z.
Ix,y,z.	Initialize memory addresses x through y with the value of z.
L.	Load a test program (object) and transfer control to the loaded program.
Px,y,z.	Generate an object format on associated peripherals: x is the address of the first word; y is the address of the last word; and z is the execution address. For noncontiguous areas of memory, set z at minus one except for the final area to be copied.
Rn	Print/change the contents of the pseudo-n register* (n is any number 0 through 7).
Sx,y,z,m.	Search memory addresses x through y for the z value, use search mask m for comparison.
Ty,x	Trap to memory addresss y, starting at address x.
X	Print/change the contents of the pseudo-X register.*
\	Terminate the control statement and return to the beginning of the executive supervisor routine. Must be typed prior to entering the period of the control statement.

Table 2-12. Executive Utility Routine Commands (Continued)

Command	Description
←	Delete the last octal digit and substitute the digit following the backarrow.
CR (Return)	Output a carriage return on the TTY printer.
LF (Line Feed)	Output a line feed on the TTY printer.
. (period)	Execute the control statement.
, (comma)	Print/change sequential memory addresses.

* The pseudo-registers are memory cells used for storing and saving the contents of the respective operations registers.

2.4.2.1 Magnetic Tape Commands

If the magnetic-tape version of the executive is used, the following additional commands can be used:

Edc.	Write end-of-file (EOF) on drive d, controller c.
Fn,dc.	Skip to file n on drive d, controller c.
Ldc(,bic).	Load and execute program on drive d, controller c (use bic-number BIC).
Px,y,z,dc(,bic).	See P control command for description. Execute on drive d, controller c (use bic-number BIC).

NOTE

d = 0 for master drive
d = 1 for first slave, etc.
c = 0 for magnetic-tape unit device address 010
c = 1 for magnetic-tape unit device address 011, etc.

A feature that appears in the magnetic tape version only is a directory of available programs. The directory can be called up after the executive identification message is displayed. Do not position the tape prior to loading the directory. Type:

```
Ldc(,bic).
```

Position the tape.

2.4.2.2 Disk Commands

If the disk version is being used, the following additional commands can be used:

Fn. Position to file n.

Ln. Load to file n
If the terminator is a period, the program is loaded and the start address is displayed, control is then returned to MAINTAIN III.

or

Ln, If the terminator is a comma, then the program is loaded and executed.

2.4.2.3 Writing Disk Files

When writing a file from memory to disk:

1. Ensure the disk drive is write-enabled.
2. Select an output file by using F command
3. Write the object modules by using the P command.
4. Close the file after all the object modules are written. Use the E command to close the file.

The current output file is closed when either an L or a second F command is entered. If the selected file is a system file, the following message is displayed:

```
SYSTEM FILE OK?
```

Enter a Y if the request was intentional or enter an N if unintentional.

All MAINTAIN III system files are two cylinders long and all non-system (scratch) files are four cylinders long. Capacity is approximately 4K words per cylinder. Programs over 16K words will use at least two scratch files.

2.4.2.4 Test Programs

Detailed descriptions of loading and execution procedures of other MAINTAIN III test programs under executive control are contained in the applicable test section.

Briefly, to load a test program:

1. Select the desired test program.
2. Position the program for loading.
3. Type L. on the virtual console keyboard.
4. The program is loaded and a test identifier message is displayed on the virtual console.

Return to the beginning of a test program is normally controlled by a SENSE switch option, or after the execution of a specified number of cycles.

To return to the executive from a test program, follow the restarting procedure described in Section 2.4.2. Pressing the INT switch on the computer also returns control to the executive; however, since some programs dynamically alter memory, refer to the applicable test section of this manual regarding restrictions on interrupting a test in progress.

In general if a test is operating under interrupt control, the program should be terminated via SENSE switch 3, then use the INT switch. This precludes leaving an interrupt in progress that can cause subsequent problems.

To return to a just-executed test program from the executive, type:

```
Gx.
```

where:

x
: Is the starting address of the test program.

Refer to the program listing supplied with the software and to the test section for starting addresses.

2.5 ERROR MESSAGES

AFter the preliminary tests and binary loader are loaded, the preliminary instructions test is automatically executed beginning at address 007002. If an error is detected, the program halts with the error code (Table 2-13) in the instruction register.

Table 2-13. Preliminary Instructions Test Error Codes

Error Code	Instruction Subtest
000001	TZA/DAR/JAZ/JAN
000002	LDA/IAR/STA
000003	LDB/JBZ/TZB
000004	IBR/DBR
000005	LDX/JXZ/TZX
000006	IXR/DXR
000007	LDAI/JAN
000010	LDAI/ERA/JAN
000011	ERAI/JAP
000012	LDBI/TBA
000013	LDXI/TXA
000014	LDB/TBX
000015	LDA/ERA
000016	LDA/STA
000017	LDB/STB
000020	LDX/STX
000021	XAZ
000022	XBZ
000023	ROF/SOF/JOF
000024	ROF/JOF/JMP
000025	JMPM/(JMP)
000027	LRLA
000030	LLSR
000031	LLSR
000032	LLRL
000033	LLRL
000034	ADD
000035	ADDI/ORAI
000036	SUB
000037	NOP
000040	INCR 03 (005103)
000041	DECR 02 (005302)
000042	MERG 032 (005032)
000043	LSRA
000044	LDA
000045	STA
000046	ANAI
000047	STAI
000050	XIF 022 (003022)
000051	JIF 011 (001011)

Refer to the program listing for the significance of the A, B, and X registers after an error halt. The applicable maintenance manual contains correction procedures.

If an error is detected in the preliminary memory test, the program halts with 000077 in the instruction register, the address of the faulty cell in the X register, and the bits in error in the A register.

To continue program execution after an error halt, press START or RUN. To loop on the subtest in error:

1. Set SENSE switch to 2.

2. Refer to the program listing for the jump address specified by the preceding JSS2 instruction, and set the P register to that address.

3. Press START or RUN.

The binary loader computes the checksum of each record of a test program (object) as it is loaded. The result is compared with the expected value in the checksum frames at the end of each record.

If a checksum error is detected during program loading the program stops. The executive produces the message:

```
CHECKSUM ERROR X = xxxxxx
```

where:

xxxxxx
Is the error address in the X register.

To restart the program after a checksum error halt:

1. Position the program tape in the reader at the previous record mark (three all-holes frames).

2. Press START or RUN.

If the record does not cause a halt on restarting, an intermittent fault probably exists in the reader. If a halt again occurs, visually examine the tape. Compare the tape to the illustration of object tape format in the programming section of the applicable system reference manual. If the tape is correct and the reader is operating correctly, refer to the program listing for the address of CKSM. Display the address on the control panel. Analyzing the ones in the checksum can indicate the location of the fault.

If the executive does not display the executive identification message, the virtual console or its controller is not operating properly. The program halts with 000077 in the instruction register. The output routine then goes into a time-out mode.

Refer to the applicable maintenance manual for troubleshooting and correction procedures.

If an illegal control statement is input, the executive displays the message:

```
INVALID
```

Enter the correct control statement.

During virtual console input activity or while the virtual console is waiting for input, SENSE switch 3 can be set to terminate the input. This internal executive routine also applies to test programs calling the executive I/O routines.

The computer system can include a power failure/restart (PF/R) option. The executive PF/R routine permits automatic recovery of operating conditions after a prime power failure and recovery.

2.6 EXECUTIVE EXAMPLES

This section contains examples of the executive messages and operator actions.

2.6.1 TEST EXAMPLE

The identification message for the V70/620 system is:

```
THIS IS THE V70/620 EXECUTIVE
MEMORY SIZE IS 16K
```

The identification message for the V75/V77 system is:

```
THIS IS THE V75 EXECUTIVE
MEMORY SIZE IS 16K
```

2.6.2 OPERATOR ACTIONS

In the following examples, operator entries are represented in bold font. Other entries are program responses output to the virtual console. Operator entry definitions are contained in Table 2-12.

Display the contents of a pseudoregister:

```
A    142340.
B    001000.
X    006003.
```

Display the contents of a pseudoregister on a V77 system:

```
R0   143240.
R1   001000.
R2   013421.
R3   000000.
R4   000000.
R5   000000.
R6   000000.
R7   000000.
```

Display and change the contents of a pseudoregister and return to the executive:

```
A    010454    10406.
B    006016    10406.
X    007413    10406.
```

Display and change the contents of a pseudoregister on a V77 system:

```
R0   010454    10406.
R1   006016    10406.
R2   007413    10406.
R3   006234    10406.
R4   013457    10406.
R5   013341    10406.
R6   000000    10406.
R7   000000    10406.
```

Display the contents of memory address 002050 and return to the executive:

```
C02050. = 102401.
```

Display and change the contents of memory address 002050, then display the next two addresses:

```
C02050. = 102401  103402,
( 002051 ) = 000067,
( 002052 ) = 177777.
```

Dump (display) memory starting at address 006000:

```
D6000.
( 006000 )     010454     002000 . . .
( 006010 )     005145     004543 . . .
( 006020 )     005041     001000 . . .
( 006030 )     006217     001000 . . .
```

Eight columns of data (representing the contents of eight memory addresses) follow the base memory dump address in the parenthesis. Space limitations prohibit a full representation of the eight memory contents.

Terminate the dump by pressing RUBOUT or set SENSE switch 3. The program then completes the current print line before the operation is terminated. Initialize memory addresses 000200 through 000210 to 177777 and return to the executive:

```
1200,210,177777.
```

Search memory addresses 000200 through 000240 for the contents of 106213 use search mask 177777. Display addresses that compare and return to the text executive:

```
S200,240,106213,177777.
( 000220 ) = 106213
( 000235 ) = 106213
```

Trap to memory address 000204 starting at address 000100. Display the trap address, contents of the overflow indicator, and contents of the A, B, and X register.

```
T204,100.
( 000204 )   142340   002000   010405   1
```

For a V75 system the trap command maintains the same format; however, eight registers (R0 through R7) will be displayed along with the overflow indicator.

Load and execute a test program:

```
L.
(TEST IDENTIFIER)
```

Transfer to and execute a test program located at address 000500:

```
G500.
(TEST IDENTIFIER)
```

Punch or write in object format beginning at address 000001 through 000006, after initializing the addresses to the desired values:

```
I0,7,0.
I1,6,1.
I2,5,2.
I3,4,3.
P1,6,7.
```

In the preceding example the initialize memory control statement has been used to establish a specified pattern in memory. The pattern is used to validate the format of the resultant operation.

Terminate an erroneous control statement:

```
P1,6/
```

Cancel digit and replace with another digit:

```
I0,6←7.
```

The following examples illustrate correct operator inputs, cancelling an operator input, and the results of invalid operator inputs. Refer to Table 2-12 for descriptions of the control commands.

Example of a correct control statement A input:

```
A 000000 2.
A 000002 1,
A 000001 .
A 000001 ,
```

Example of cancelling a control statement A input:

```
A 000001\
A 000001 2\
A 000001 .
```

Example of an invalid control statement A input:

```
A 000001 X  INVALID
A 000001 2X  INVALID
A 000001 .
```

Example of a correct control statement B input:

```
B 000000 2.
B 000002 1,
B 000001 .
B 000001 ,
```

Example of cancelling a control statement B input:

```
B 000001 \
B 000001 2\
```

Example of an invalid control statement B input:

```
B 000001 X  INVALID
B 000001 2X  INVALID
B 000001 .
```

Example of a correct control statement C input:

```
C10.=000000 1.
C10.=000001 .
C10,=000001 2.
C10,=000002 .

C10.=000002 1,
( 000011 ) =000000 2.
C10.=000001 ,
( 000011 ) =000002 .
C10.=000001 ,
( 000011 ) =000002 ,
( 000012 ) =000000 3.
C10.=000001 ,
( 000011 ) =000002 ,
( 000012 ) =000003 .
```

Example of cancelling a control statement C input:

```
C10.=000002 \
C10.=000002 3\
C10,=000002 \
C10,=000002 3 \
C10.=000002 .
```

```
C10,=000001 ,
( 000011 ) =000002\
C10,=000001 ,
( 000011 ) =000002 3\
C10,=000001 ,
( 000011 ) =000002 ,
( 000012 ) =000003 4\

C10.=000001 ,
( 000011 ) =000002\
C10.=000001 ,
( 000011 ) =000002 3\
C10.=000001 ,
( 000011 ) =000002 ,
( 000012 ) =000003 4\
C12.=000003 .
```

Example of an invalid control statement C input:

```
C10.=000002 3X  INVALID
C10,=000002 3X  INVALID
C10.=000002 .
C1X  INVALID
C10,=000001 ,
( 000011 ) =000002 X  INVALID
C10,=000001 ,
( 000011 ) =000002 3X  INVALID
C10,=000001 ,
( 000011 ) =000002 ,
( 000012 ) =000003 X  INVALID
C12.=000003 .
```

Example of a correct control statement D input:

```
D0.
(000000) 000000 000001 000002 000003 000004 000005 000006 000007
(000010) 000010 000011 000012 000013 000014 000015 000016 000017
(000020)

D0,
(000000) 000000 000001 000002 000003 000004 000005 000006 000007
(000010) 000010 000011 000012 000013 000014 000015 000016 000017

D4.
(000004) 000004 000005 000006 000007
(000010) 000010 000011 000012 000013 000014 000015 000016 000017
```

```
D4,
(000004) 000004 000005 000006 000007
(000010) 000010 000011 000012 000013 000014 000015 000016 000017
```

Example of cancelling a control statement D input:

```
    D\
    D44\
```

Example of an invalid control statement D input:

```
    DX  INVALID
    D4X  INVALID
```

Example of a correct control statement E input:

```
    I0,7,0.
    I1,6,1.
    I2,5,2.
    I3,4,3.
```

Example of a correct control statement I input:

```
I0,7,0.
I1,6,1.
I2,5,2.
I3,4,3.
D0.
(000000) 000000 000001 000002 000003 000003 000002 000001 000000
```

Example of cancelling a control statement I input:

```
    I\
    I0\
    I0,\
    I0,7\
    I0,7,\
    I0,7,0\
    I,\
    I,7\
    I,7,\
    I,7,0\
    I,,\
    I,,0\
```

Example of an invalid control statement I input:

```
IX  INVALID
I0x  INVALID
I0,X  INVALID
I0,7X  INVALID
I0,7,X  INVALID
I0,7,0X  INVALID
I7,0,0.  INVALID
```

Example of a correct control statement L input:

```
L.
```

Example of cancelling a control statement L input:

```
L\
```

Example of an invalid control statement L input:

```
LX  INVALID
L0  INVALID
```

Example of a control statement L input with a forced checksum error:

```
I0,7,0.
L.CHECKSUM ERROR  X = 000001
D0.
(000000) 000000 000001 000002 000003 000003 000006 000001 000000
```

Example of a correct control statement P input:

```
I0,7,0.
I1,6,1.
I2,5,2.
I3,4,3.
P1,6,7.@@F@@A@@A@@B@@C@@C@@B@@A@@G@@@@@@G@@G

P1,6,777777.@@F@@A@@A@@B@@C@@C@@B@@A@@B@@A@@G
```

Example of cancelling a control statement P input:

```
P\
P1\
P1,\
P1,6\
P1,6,\
P1,6,0\
P,\
P,6\
P,6,\
P,6,0\
P,,\
P,,0\
```

Example of an invalid control statement P input:

```
PX  INVALID
P1X  INVALID
P1,X  INVALID
P1,6X  INVALID
P1,6,X  INVALID
P1,6,0X  INVALID
```

Example of a correct control statement R input:

```
R0   000000 2.
R1   000000 1.
R2   000000.
R3   000000.
R4   000000.
R5   000000 4.
R6   000000.
R7   000000.
```

Example of cancelling a control statement R input:

```
R0   000001\
R1   000000\
R2   000300 2\
R3   010000 3\
R4   000000 4\
R5   000003 5\
R6   040000 6\
R7   050000 7\
```

Example of an invalid control statement R input:

```
R0    000001    X     INVALID
R1    000001    2X    INVALID
R2    000001    2X    INVALID
R3    000001    X     INVALID
R4    000001    X     INVALID
R5    000001    X     INVALID
R6    000001    A     INVALID
R7    000001    B     INVALID
```

Example of a correct control statement S input:

```
DO,
(000000) 000000 000001 000002 000003 000004 000005 000006 000007

SO,6,0,7777.
( 000000 ) =000000

S1,7,7,7777.
( 000007 ) =000007

S1,6,0,7777.
S1,6,7,7777.

SO,7,35,7.
( 000005 ) =000005
S1,5,1,1.
( 000001 ) =000001
( 000003 ) =000003
( 000005 ) =000005
S1,2,77,0.
( 000001 ) =000001
( 000002 ) =000002
```

Example of cancelling a control statement S input:

```
S\
SO\
SO,\
SO,7\
SO,7,\
SO,7,5\
SO,7,5,\
SO,7,5,7\
```

```
S,\
S,7\
S,7,\
S,7,5\
S,7,5,\
S,7,5,7\
S,,\
S,,5\
S,,5,\
S,,5,7\
S,,,\
S,,,7\
```

Example of an invalid control statement S input:

```
SX  INVALID
S0X  INVALID
S0,X  INVALID
S0,7X  INVALID
S0,7,X  INVALID
S0,7,5X  INVALID
S0,7,5,X  INVALID
S0,7,5,7X  INVALID
```

Example of a correct control statement X input;

```
X 000000 2.
X 000002 1,
X 000001 .
X 000001 ,
```

Example of cancelling a control statement X input:

```
X 000001\
X 000001 2\
```

Example of an invalid control statement X input:

```
X 000001 X  INVALID
X 000001 2X  INVALID
X 000001 .
```

Part 2
Terminals

Part 2 of the MAINTAIN III Communications Equipment and Controllers Test Programs User Guide contains the test programs that are used in testing SPERRY UNIVAC V77 terminals.

This part of the guide consists of:

Section 1 - ASYNCHRONOUS-BUFFERED TERMINAL TEST. Contains a test description and test operating procedures used in testing the buffered terminals (Type 2840-00 and 2840-03).

Section 2 - BINARY-SYNCHRONOUS TERMINAL TEST. Contains a test description and test operating procedures used in testing the binary-synchronous terminal (Type 2846).

Section 1
ASYNCHRONOUS-BUFFERED TERMINAL TEST

1.1 GENERAL

The Asynchronous-Buffered Terminal test program tests the asynchronous-buffered terminals (Type 2840-00 and -03).

The test program is designed to operate with the MAINTAIN III executive. The test uses the virtual console interface, SENSE switch routines, I/O, timing routines, and system constants contained in the executive.

Testing of the terminal is via a data communications multiplexer (DCM) with an asynchronous line adapater. The test program consists of a parameter set-up and a specific test selection component. The parameter set-up component requests and accepts various values to configure the software to the hardware. There are several specialized tests that can be requested by the operator of the test program. Each test is designed to check the operation of certain portions of the terminal which assists in fault isolation. Depending on the operator setting of the SENSE switches, errors or malfunctions are optionally reported to the operator. Error reporting comprises error or malfunction messages, error loops, and halts.

Available documentation is as follows:

Document Number	Title
92( )0106-030	Buffered Editing Terminal Test

1.2 HARDWARE REQUIREMENTS

The minimum hardware requirements are as follows:

- One V70 series computer with 12K words of memory.
- One DCM with an asynchronous line adapter installed.
- One asynchronous-buffered terminal.

1.3 DESCRIPTION OF TEST COMPONENTS

The two major components of the test program are the parameter set-up and the specific test selection. The general program block diagram is illustrated in Figure 1-1.

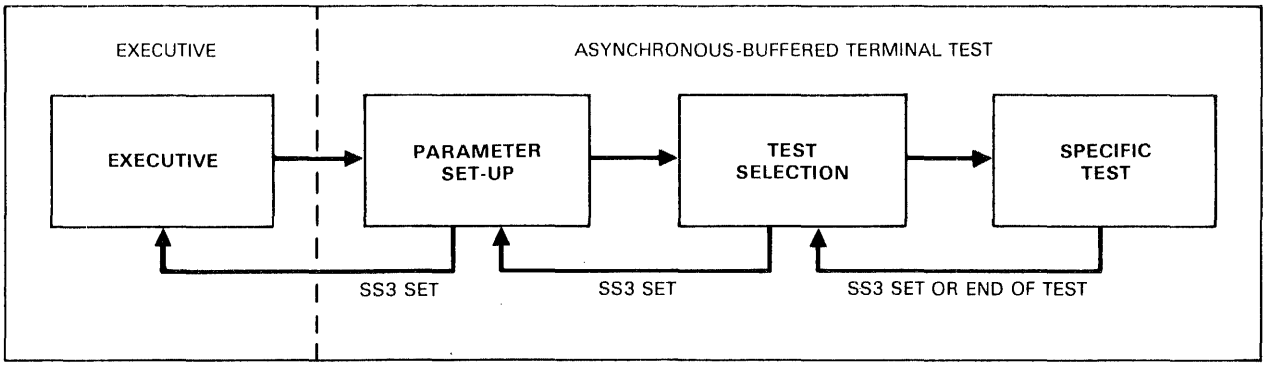

Figure 1-1. General Asynchronous-Buffered Terminal Test Block Diagram

1.3.1 PARAMETER SET-UP

The parameter set-up routine clears various constants and tables to initialize the test program. This routine is executed each time the program is started from address 1000_8 or when SENSE switch 3 (SS3) is set during the test selection phase.

During this phase:

- the program identification message is displayed;
- the user enters the line control block (LCB), DCM, and interrupt origin addresses;
- the user determines the active line to be used; and
- the user determines the number of times the selected test is to be performed.

Setting SS3 at any time during the parameter set-up routine causes the test program to transfer control to the executive.

1.3.2 TEST SELECTION

During this phase, the user determines which test is to be conducted on the terminal. Descriptions of the selectable tests are contained in the following paragraphs. Any errors or malfunctions are reported to the user if SS1 is reset. Setting SS3 while a test is in progress terminates the test

and control is returned to the test selection routine. Setting SS3 while in the test selection routine returns control to the parameter set-up routine. After a test is completed, the number of passes through the test is displayed.

1.3.2.1 Test 0 Continuous Output

A spiral data pattern is transmitted to the terminal. Writing is continuous until SS3 is set or RUBOUT is depressed on the console keyboard.

1.3.2.2 Test 1 Terminal Edit

An easily recognizable text with one or more character errors is transmitted to the terminal. The terminal operator corrects the text by using the terminal editing features. The corrected text is then transmitted to the computer for validation.

1.3.2.3 Test 4 Character Test

The terminal displays every printable character in every printable position.

1.3.2.4 Test 5 Cursor Position Test

The terminal has the cursor moved to every display position.

1.3.2.5 Test 6 Printer Format Test

All the vertical formats are transmitted to the terminal.

1.3.2.6 Test 10 Programmed Attention Test

A request to depress a particular attention key is displayed on the terminal. When the operator depresses the attention key, a new request is displayed.

1.3.2.7 Test 11 Field Attribute Test

A spiral data pattern is transmitted to the terminal. The text is grouped into four lines. The first two lines appear normal, the third line is intensified, and the fourth line is not displayed.

1.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the asynchronous-buffered terminal test program can be loaded. Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4.

Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Partl, Section 1, paragraph 1.6) are used.

1.4.1 PARAMETER SET-UP

After loading of the test program is completed, the following identification message is displayed:

BUFFERED EDITING TERMINAL TEST

The message is for information only and does not require any operator response.

The next message is:

LCB ADDRESS = R.

Enter the octal address of the line control block for the DCM. Tests are made on this value to ensure that the LCB does not overlay any program area. If the LCB overlays the program, the address is rejected. The error message "INVALID" is displayed and the LCB address is again requested.

After the LCB address has been validated, the following message is displayed:

DCM ADDRESS = R.

Enter the octal device address of the DCM. The address range is 0 through 077. Tests are made to ensure that the entered value falls within this range.

The next message to be displayed is:

INTERRUPT ORIGIN = R.

Enter the octal address of the first interrupt of the DCM interrupt block. Tests are made to ensure that the entry is modulo 16 and in the range of 0 through 0760.

The number of the DCM line to be used during the test is entered after the following message is displayed:

```
ACTIVE LINE = R.
```

Enter an octal number that corresponds to the DCM line that is to be used during the test.

The number of test cycles is specified next. The following message is displayed:

```
TERMINATE TEST = R.
```

Enter a 0 for continuous testing or a 1 to terminate the test after one pass.

1.4.2 TEST SELECTION

The test to be conducted on the asynchronous-buffered terminal is selected after the following message is displayed:

```
TEST = R.
```

A brief description of each valid test is contained in Part 2, Section 1, paragraph 1.3.2. Enter a single test number. The valid entries are:

Entry	Description (Test)
0	Continuous output
1	Terminal edit
3	Character
4	Cursor position
5	Printer format
11	Programmed attention
12	Field attribute

1.4.3 TEST PROGRAM MESSAGES

Messages encountered prior to performing the test program are:

```
INFORMATION DISPLAY SUBSYSTEM TEST
LCB ADDRESS =
DCM ADDRESS =
INTERRUPT ORIGIN =
ACTIVE LINE =
TERMINATE TEST =
TEST =
```

Normal termination of the test causes the number of completed test passes to be displayed. The message is:

```
PASSES nnnnnn
```

where

n
: Is the octal number of places.

1.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages are:

```
TIME OUT ON LINE ll
INVALID USE OF LINE ll
e ERROR LINE ll
SC INTERRUPT sss
EXP        RX        ERROR
vvvvvv     iiiiii    *
```

where:

e
: Is type of error; B = BCC, F = format, O = overflow, and T = timeout.

iiiiii
: Is valid data.

ll
: Is line number

sss
: Is octal status.

vvvvvv
: Is expected data.

*
: Is error identification

Section 2
Binary-Synchronous Terminal Test

2.1 GENERAL

The Binary-Synchronous Terminal test program tests the binary-synchronous terminal (Type 2846).

The test program is designed to operate with the MAINTAIN III executive. The test uses the virtual console interface, SENSE switch routines I/O, timing routines, and system constants contained in the executive.

Testing of the terminal is via a data communications multiplexer (DCM) with a binary-synchronous control (BSC) line adapter (LAD). One or more terminals can be tested simultaneously. The test program comprises a parameter set-up and a specific test selection component. The parameter set-up component requests and accepts various values to configure the software to the hardware. There are several specialized tests that can be requested by the operator of the test program. Each test is designed to check the operation of certain portions of the terminal which assists in fault isolation. Depending on the operator setting of the SENSE switches, errors or malfunctions are optionally reported to the operator. Error reporting comprises error or malfunction messages, error loops, and halts.

Available documentation is as follows:

Document Number	Title
92( )0106-026	Information Display Subsystem Test

2.2 HARDWARE REQUIREMENTS

The minimum hardware requirements are as follows:

- One V70 series computer with 32K words of memory.
- One DCM with a BSC LAD installed.
- One modem or modem eliminator.
- One terminal controller (Type 2845).
- One binary-synchronous terminal.

2.3 DESCRIPTION OF TEST COMPONENTS

The two major components of the test program are the parameter set-up and the specific test selection. The general program block diagram is illustrated in Figure 2-1.

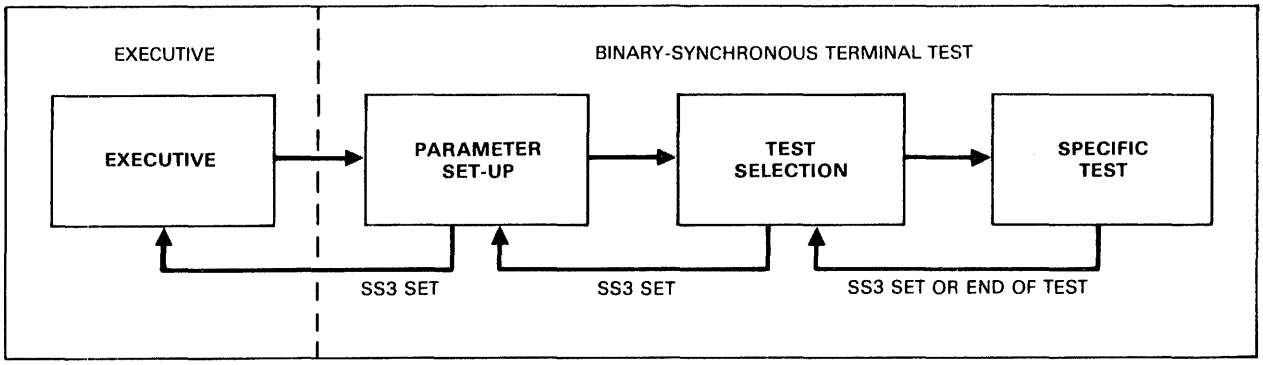

Figure 2-1. General Binary-Synchronous Terminal Test Block Diagram

2.3.1 PARAMETER SET-UP

The parameter set-up routine clears various constants and tables to initialize the test program. This routine is executed each time the program is started from address 1000_8 or when SENSE switch 3 (SS3) is set during the test selection phase.

During the phase:

- the program identification message is displayed;
- the user enters the line control block (LCB), DCM, interrupt origin, and terminal addresses;
- the user determines the active line and controller numbers; and
- the user determines the number of times the selected test is to be performed.

Setting SS3 at any time during the parameter set-up routine causes the test program to transfer control to the executive.

2.3.2 TEST SELECTION

During this phase, the user determines which test is to be conducted on the terminal. Descriptions of the selectable tests are contained in the following paragraphs. Any errors or malfunctions are reported to the user if SS1 is reset. Setting SS3 while a test is in progress terminates the test and control is returned to the test selection routine. Setting SS3 while in the test selection routine returns control to the parameter set-up routine. After a test is completed, the number of passes through the test is displayed.

2.3.2.1 Test 0 Continuous Output

A spiral data pattern is transmitted to each active terminal. Writing is continuous until SS3 is set or RUBOUT is depressed on the console keyboard.

2.3.2.2 Test 1 Terminal Edit

An easily recognizable text with one or more character errors is transmitted to each active terminal. The terminal operator corrects the text by using the terminal editing features. The corrected text is then transmitted to the computer for validation.

2.3.2.3 Test 2 Hot Keyboard

Each active terminal is placed in the receive mode. The operator displays a routing code and text on one terminal, then transmits the code and text to the computer. The computer uses the routing code to transmit the text to the requested terminal.

2.3.2.4 Test 3 Character Test

Active terminals display every printable character in every printable position.

2.3.2.5 Test 4 Cursor Position Test

Active terminals have the cursor moved to every display position.

2.3.2.6 Test 5 Printer Format Test

All the vertical formats are transmitted to each active terminal.

2.3.2.7 Test 6 Read Modified Function Test

An easily recognizable text having character errors is transmitted to each active terminal. The terminal operator corrects the text by using the terminal editing features. The corrected text is then transmitted to the computer for validation.

2.3.2.8 Test 7 Unique Terminal Test

Each active terminal receives an identification message with the terminal address displayed.

2.3.2.9 Test 8 Copy Terminal to Terminal

Data from the lowest-numbered active terminal is copied onto the next higher-numbered active terminal. The data is then copied on the next higher-numbered active terminal. Copying continues until all active terminals have the same data displayed as the lowest-numbered active terminal.

2.3.2.10 Test 9 Programmed Attention Test

A request to depress a particular attention key is displayed on the terminal. When the operator depresses the attention key, a new request is displayed.

2.3.2.11 Test 10 Field Attribute Test

A spiral data pattern is transmitted to the active terminals. The text is grouped into four lines. The first two lines appear normal, the third line is intensified, and the fourth line is not displayed.

2.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the binary-synchronous terminal test can be loaded.

Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4.

Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, Section 1, paragraph 1.6) are used.

2.4.1 PARAMETER SET-UP

After loading of the test program is completed, the following identification message is displayed:

INFORMATION DISPLAY SUBSYSTEM TEST

The message is for information only and does not require any operator response.

The next message is:

LCB ADDRESS = R.

Enter the octal address of the line control block for the DCM. Tests are made on this value to ensure that the LCB does not overlay any program area. If the LCB overlays the program, the address is rejected. The error message "INVALID" is displayed and the LCB address is again requested.

After the LCB address has been validated, the folowing message is displayed:

DCM ADDRESS = R.

Enter the octal device address of the DCM. The address range is 0 through 077. Tests are made to ensure that the entered value falls within this range.

The next message to be displayed is:

INTERRUPT ORIGIN = R.

Enter the octal address of the first interrupt of the DCM interrupt block. Tests are made to ensure that the entry is modulo 16 and in the range of 0 through 0760.

The number of the DCM line to be used during the test is entered after the following message is displayed:

ACTIVE LINE = R.

Enter an octal number that corresponds to the DCM line that is to be used during the test.

The controller number is entered after the folowing message is displayed:

CONTROLLER NUMBER = R.

Enter an octal number that represents the number of the controller to be used during the test.

The terminals to be used during the test are specified after the following message is displayed:

ACTIVE TERMINALS = R1,R2,...Rn.

Enter an octal number in the range of 0 through 037 that corresponds to the address of each terminal to be used during the test. When addressed, the terminals become active for the duration of the test.

The number of test cycles is specified next. The following message is displayed:

TERMINATE TEST = R.

Enter a 0 for continuous testing or a 1 to terminate the test after one pass.

2.4.2 TEST SELECTION

The test to be conducted on the binary-synchronous terminal is selected after the following message is displayed:

TEST = R.

A brief description of each valid test is contained in paragraph 2.3.2. Enter a single test number. The valid entries are:

Entry	Description (Test)
0	Continuous output
1	Terminal edit
2	Hot keyboard
3	Character test
4	Cursor position
5	Printer format
6	Read modified function
7	Unique terminal
8	Copy terminal to terminal
9	Programmed attention
10	Field attribute

2.4.3 TEST PROGRAM MESSAGES

Messages encountered prior to performing the test programs are:

```
INFORMATION DISPLAY SUBSYSTEM TEST
LCB ADDRESS =
DCM ADDRESS =
INTERRUPT ORIGIN =
ACTIVE LINE =
CONTROLLER NUMBER =
ACTIVE TERMINALS =
TERMINATE TEST =
TEST =
```

Normal termination of the test causes the number of completed test passes to be displayed. The message is:

```
PASSES nnnnnn
```

where:

nnnnnn
: Is the octal number of passes.

2.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages are:

```
TIME OUT ON LINE 11
INVALID USE OF LINE 11
e ERROR LINE 11
SC INTERRUPT sss
INVALID RESPONSE TERMINAL tt
NO RESPONSE TERMINAL tt
REVERSE INTERRUPT TERMINAL tt STATUS sss
EXP       RX        ERROR
vvvvvv    iiiiii    *
```

where:

e
: Is type if error; B = BCC, F = format, O = overflow, and T = timeout..

iiiiii
: Is valid data.

ll
: Is line number.

sss
: Is octal status.

tt
: Is terminal number.

vvvvvv
: Is expected data.

*
: Is error identification.

Part 3
Data Communications Equipment

Part 3 of the MAINTAIN III Communications Equipment and Controllers Test Programs User Guide contains test programs that are used in testing SPERRY UNIVAC V77 data communications equipment.

This part of the guide consists of:

Section 1 - DATA COMMUNICATIONS MULTIPLEXER (DCM) TEST. Contains a test description and test operating procedures used in testing the DCM (F3000) and line adapters (LAD, F3001-00 through -04, -06, and -07).

Section 2 - MAPPED DATA COMMUNICATIONS MULTIPLEXER (DCM) TEST. Contains a test description and test operating procedures used in testing the mapped DCM (F3000) and line adapters (LAD, F3001-00 through -04, -06, and -07).

Section 3 - BINARY SYNCHRONOUS CONTROL (BSC) LINE ADAPTER (LAD) TEST. Contains a test description and test operating procedures used in testing the BSC LAD (F3001-05).

Section 4 - UNIVERSAL DATA LINK CONTROL (UDLC) LINE ADAPTER (LAD) TEST. Contains a test description and test operating procedures used in testing the UDLC LAD (F3060-00).

Section 1
Data Communications Multiplexer Test

1.1 GENERAL

The Data Communications Multiplexer (DCM) test program tests the DCM (F3000) and certain line adapters (LAD, F3001-00 through -04, -06, and -07).

The test program is designed to operate with the MAINTAIN III executive. The test uses the virtual console interface, SENSE switch routines, I/O, timing routines, and system constants contained in the test executive.

The test program consists of a parameter set-up and a specific test selection component. The parameter set-up component requests and accepts various values to configure the software to the hardware. There are several specialized tests that can be requested by the operator of the test program. Each test is designed to check the operation of certain portions of the DCM. The specific test is performed, as requested by the user, with errors and malfunctions optionally reported to the user. Depending on the setting of the SENSE switches, the program provides for the logging of error or malfunction messages, error loops and halts.

Modularizing of the test program allows testing of specific DCM components and the addition of new tests.

Available documentation is as follows:

Document Number	Title
92( )0106-014D	DCM Test Program
UP-8629	DCM Operation and Service Manual

1.2 HARDWARE REQUIREMENTS

The DCM test program requires a V77 computer with at least 12K words of memory and at least one or more of the following line adapters:

Feature Number	Line Adapter (LAD) Name
F3001-00	Asynchronous RS232 Modem LAD
F3001-01	Direct Connection RS232/DT-TTL LAD
F3001-02	Direct Connection Current Loop LAD
F3001-03	Direct Connection Relay Current Loop LAD
F3001-04	Synchronous RS232 Modem LAD
F3001-06	Automatic Call Unit (ACU) LAD
F3001-07	Programmable Asynchronous RS232 Modem LAD

1.3 DESCRIPTION OF TEST COMPONENTS

The two major components of the test program are the parameter set-up and the specific test selection. The general program block diagram is illustrated in Figure 1-1.

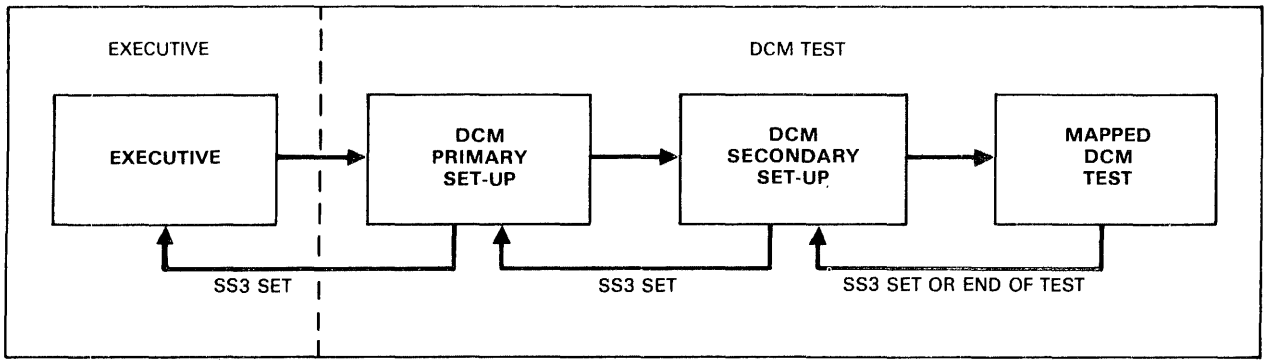

Figure 1-1. General DCM Test Block Diagram

1.3.1 PARAMETER SET-UP

The parameter set-up component consists of two routines: primary set-up and secondary set-up.

The primary set-up routine clears various constants and tables to initialize the test program. This routine is performed each time the program is started from address 1000_8 or when SENSE switch 3 (SS3) is set during the secondary set-up routine. During the routine, the test executive indicator $CON is tested to determine if a teletypewriter or CRT is available.

During this phase:

- the program identification message is displayed and
- the user enters the line control block (LCB), DCM, and interrupt origin addresses.

Setting SS3 at any time during the primary set-up routine causes the test program to transfer control to the test executive.

The secondary set-up routine initializes variables that pertain to the line adapter under test. This routine also provides the software procedures for the orderly shutdown of the program in the event of an operator initiated test termination. When any test has been completed, this routine causes a display of the number of passes through the test.

Variable entries which must be made during this phase are:

- Line adapter type
- Test duration
- Data pattern to be used
- Active lines to be tested
- Line adapter bit length
- Parity selection
- Stop bit value
- Speed selection
- Desired test
- Mirror image selection.

Setting SS3 at any time during the secondary set-up routine causes the test program to transfer control to the primary set-up routine.

Valid entries for all variables are contained in the operating procedures.

1.3.2 TEST SELECTION

Descriptions of the selectable tests are contained in the following paragraphs. Each selected line is tested. Any errors or malfunctions are reported to the user if SS1 is reset. Setting SS3 terminates the test.

1.3.2.1 Test 0 Transmit Only

Active lines are placed in the transmit mode and allowed to run continuously while using the selected data pattern.

1.3.2.2 Test 1 Loop

Active lines are placed in full-duplex mode and allowed to run continuously while using the selected data pattern. During Test 77 (Burn-in) on the programmable asynchronous RS232 modem LAD, all possible combinations of word lengths, parity selection, stop bit selections, and speeds are automatically tested.

1.3.2.3 Test 2 Control Character

Active lines are placed in full-duplex mode. Each line is separately tested while using the binary data pattern. A total of 255 control characters are checked (0 is not checked) one at a time. When the test is completed on one line, the next active line is tested. The test runs continuously until terminated by the operator. If a control character is not detected, an error is reported.

1.3.2.4 Test 3 Speed Selection

Active lines are placed in full-duplex mode and allowed to run continuously while using the selected data pattern. As each line completes a block, the line speed is changed.

1.3.2.5 Test 4 Break Transmission

Active lines are placed in the full-duplex mode and allowed to run continuously while using the selected data pattern. Each line is selectively forced to transmit a break. The receiver detects the break and reports to the test program. If a break is not detected, an error is reported.

1.3.2.6 Test 5 Interrupt Response

Active lines are tested for correct interrupt response: control line in, control line out, output buffer empty, output register empty, and ring indicator. The test runs continuously until terminated by the operator. If an interrupt is not detected, an error is reported.

1.3.2.7 Test 6 Status Flag

Active lines are tested for the correct status flag setting. The three modem status lines (interlock, carrier-on, and clear-to-send) are tested. The test runs continuously until terminated by the operator.

1.3.2.8 Test 7 Large Block Transfer

Active lines are placed in the full-duplex mode and allowed to transmit a large block (4096 bytes) of random data. The receiver circuit receives small blocks (256 bytes) of data and tests the first word for correct data. Errors in data are reported. The test runs continuously until terminated by the operator.

1.3.2.9 Test 10 Echo Mode

Active lines are placed in the full-duplex mode and then into the echo mode. The test verifies that each line will automatically echo all received data when required to do so. Failure to echo data results in an error.

1.3.2.10 Test 11 Synchronization (Sync)

Active lines are placed in the full-duplex mode. Each line is allowed to run while using a fixed set of sync characters. The test sequentially transmits the group of sync characters that test all bits. This test does not test a line that is set for five-bit data with odd parity.

1.3.2.11 Test 12 Resynchronization

Active lines are placed in the full-duplex mode. Each line is tested to see if that line can be resynchronized in the middle of a message. Testing is accomplished by loading the line receive-sync-character register with a new sync character. This forces the line into an overrun condition.

1.3.2.12 Test 13 Transmit Synchronization

Active lines are placed in the full-duplex mode and set to transmit a receive sync character. The receiver is set to receive one character which should be the transmitted character. All combinations of transmit sync characters are used.

1.3.2.13 Test 14 Automatic Parity

Active lines are placed in the full-duplex mode with parity selected. The most significant bit (MSB) contains the transmitted parity. The parity bit is truncated by the receiver, then the received byte is checked to see if the MSB is received. Receipt of the MSB results in an error.

1.3.2.14 Test 15 Inhibit Output Data Requests

Active lines are placed in the full-duplex mode with the accept-ring (AR) bit in the line control bit set. Under this condition, no data in memory can be accessed. When the receive mode is completed, the transmit word pointer is tested to verify that it has not moved. A movement of the word pointer is reported as an error.

1.3.2.15 Test 16 One Synchronization Character

Active lines are placed in the full-duplex mode and a character block of data with only one sync character is transmitted. When the transmission is complete, the receive word pointer is tested to verify that it has not moved.

1.3.2.16 Test 17 VDM ASCII

Active lines are placed in the full-duplex mode with VDM ASCII selected. The MSB of the received byte is tested to verify that the bit is set.

1.3.2.17 Test 20 ACU Data Integrity

The ACU LAD is tested in the back-to-back mode through the use of the ACU LAD test shoe. The test transmits, to each line, various data patterns whose inverted images are read back as status condition. The four received status bits reflect the transmitted number as follows:

- B = NB8
- A = NB4
- U = NB2
- I = NB1

The data verifies that data patterns which cause a status change interrupt do produce this condition. When either an invalid timeout or a status comparison failure occurs, an error message is generated.

1.3.2.18 Test 21 ACU Data Request

The ACU LAD is tested in the back-to-back mode through the use of the ACU LAD test shoe. The ACU LAD is placed in the transmit mode and the dial-digit data is fetched from the output buffer. The test then checks the transfer sequence to see that it is correct.

1.3.2.19 Test 22 Character Mode

Active lines are sequentially placed in the full-duplex mode. The character mode (CM) bit of the mode byte is set to cause a line error interrupt for each byte transmitted. The line control table is set to transfer 200 characters. A data line error interrupt is expected for each received character. This is verified by comparing bits 8-15 of the received data and the transmitted data. Discrepancies are reported as an error.

During Burn-in testing, all possible combinations of word lengths, parity selections and speeds are automatically tried and tested.

1.3.2.20 Test 77 Burn-in

All applicable tests (except for tests 0, 7, and 8) are performed on all active lines.

1.3.2.21 Test 100 Terminal Echo

Active lines are placed in the receive mode. As each character is received, the interrupt processor transmits the received character back over the same line.

1.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the DCM test program can be loaded. Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4.

Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, Section 1, paragraph 1.6) are used.

1.4.1 PRIMARY SET-UP

After loading of the test program is completed, the following identification message is displayed:

```
DCM TEST
```

The message is for information only and does not require any user response.

The next message is:

```
LCB ADDRESS = R.
```

Enter the octal address of the line control block. Tests are made on this value to ensure that the LCB does not overlay any program area. If the LCB overlays the program, the address is rejected. The error message "INVALID" is displayed and the LCB address is again requested.

After the LCB address has been validated, the following message is displayed:

```
DCM ADDRESS = R.
```

Enter the octal device address of the DCM . The address range is 0 through 077_8. Tests are made to ensure that the entered value falls within this range.

The next message to be displayed is:

```
INTERRUPT ORIGIN = R.
```

Enter the octal address of the first interrupt of the DCM interrupt block. Tests are made to ensure that the entry is modulo 16 and in the range of 0 through 0760.

1.4.2 SECONDARY SET-UP

The line adapter request is:

```
LINE ADAPTER TYPE = R.
```

Enter a single digit to represent the type of line adapter under test. The valid entries are:

Entry	Description
1	Asynchronous LAD (F3001-00)
2	Direct connection LAD (F3001-01 through -03)
4	Synchronous LAD (F3001-04)
10	ACU LAD (F3001-06)
20	Programmable asynchronous LAD (F3001-07)

The number of test cycles to be performed is specified next. THe following message is displayed:

```
TERMINATE TEST = R.
```

Enter a period (.) for continuous testing (terminate by setting SS3) or a 1. to terminate the test after one pass.

The test data pattern is requested when the following message is displayed:

```
DATA PATTERN = R.
```

Enter an octal value that corresponds to the desired test data pattern. The valid entries are:

Entry	Description
0	All zeros
1	All ones
2	Ascending binary
3	Alternating ones and zeros
4	User pattern

The user data pattern is an octal word that defines the left and right byte of the data pattern. THe user can enter any data pattern that is to be used by the test. The data pattern is entered after the 4. entry and is itself terminated with a period. For example:

```
DATA PATTERN = 4.1234.
```

The number of lines to be tested is entered after the following message is displayed:

```
ACTIVE LINES = R,R.
```

Enter two octal numbers, separated with a comma and terminated with a period, that correspond to the first and last line (inclusive) to be used during the test.

The bit length of the line adapter under test is entered after the following message is displayed:

BIT LENGTH = R.

Valid octal entries are 5, 6, 7, or 10.

The following three messages are applicable if the selected line adapter type is 20.

Parity to be used during the test is selected after the following message is displayed:

PARITY SELECT = R.

Enter an octal value that corresponds to the desired parity. The response is entered into bits 10 (PS) and 11 (PI) of control byte number 2. The valid entries are:

Entry	Description	
0	No parity:	PI=0, PS=0
1	No parity:	PI=0, PS=1
2	Even parity:	PI=1, PS=0
3	Odd parity:	PI=1, PS=1

The stop bit for the line adapter under test is placed in bit 12 (SB) of control byte number 2. A stop bit is entered after the following message is displayed:

STOP BIT = R.

Valid entries are:

Entry	Description
0	Two stop bits (SB=0)
1	One stop bit (SB=1)

The speed to be used on the line adapter under test is selected for the programmable asynchronous LAD (F3001-07) only. The asynchronous LAD (F3001-00) has both available speeds tested. Selection is made after the following message is displayed:

SPEED SELECT = R,R.

The operator response is entered into bits 8-13 of control byte number 3. The transmit and receive values should be equal for correct data transfer; however, these values can be set unequal in order to isolate errors. The valid entries are:

Transmit Entry	Receive Entry	Description (Speed)
0	0	One
1	1	Two
2	2	Three
3	3	Four
4	4	Five
5	5	Six

The following messages are applicable to all line adapter types.

The test to be conducted on the line adapter is selected after the following message is displayed:

TEST = R.

A brief description of each valid test is contained in paragraph 1.3.2. Only test 77 (burn-in) can be used on all line adapters. Since the specific tests are designed to test certain functions, the tests are restricted to use on certain line adapters. The following list, which contains the valid test number entries, also lists the line adapter types that the test can be used on. A description of the line adapter types can be found following the LINE ADAPTER TYPE entry (paragraph 1.4.2).

Entry	Description	Line Adapter Applicability
0	Transmit only	1, 2, 4, and 20
1	Loop	1, 2, 4, and 20
2	Control character	1, 2, 4, and 20
3	Speed selection	1 and 2
4	Break transmission	1, 2, and 20
5	Interrupt response	1, 2, 4, and 20
6	Status flag	1, 4, and 20
7	Large block transfer	1, 2, and 20
10	Echo mode	1, 2, and 20
11	Synchronization	4
12	Resynchronization	4
13	Transmit synchronization	4
14	Automatic parity	4
15	Inhibit output data requests	4

Entry	Description	Line Adapter Applicability
16	One synchronization character	4
17	VDM ASCII	1, 2, 4, and 20
20	ACU data integrity	10
21	ACU data request	10
22	Character mode	20
77	Burn-in	All adapters
100	Terminal echo	1, 2, and 20

Test 77 cycles through all applicable tests except for tests 0, 2, 7, 10, and 100.

If the selected bit length is seven bits or less, the following message is displayed:

```
MIRROR IMAGE = R.
```

The valid entries are 0 for no or 1 for yes. When mirror image is selected, the data is left justified; otherwise, the data is right justified.

1.4.3 TEST PROGRAM MESSAGES

Messages that are encountered prior to performing the test program are:

```
DCM TEST
LCB ADDRESS=
DCM ADDRESS=
INTERRUPT ORIGIN=
LINE ADAPTER TYPE=
DATA PATTERN=
ACTIVE LINES=
TERMINATE TEST=
BIT LENGTH=
TEST=
MIRROR IMAGE=
```

Normal termination of the test causes the number of completed test passes to be displayed:

```
n PASSES
```

where:

n
: Is the octal number of passes.

1.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages and the applicable tests are:

Test	Error Message
ALL	TIMEOUT ON LINE 11
ALL	INVALID USE OF LINE 11
ALL	NOT A VALID TEST FOR THIS LINE ADAPTER
0	IBCZ INTERRUPT FROM LINE 11
ALL	eERROR ON LINE 11
ALL	SC INTERRUPT FROM LINE 11 ss
5	LINE ERROR INTERRUPT FROM LINE 11
ALL	MEMORY FULL, CAN'T START kk LINES
1,22	CMP ERR LINE 11 SHBE vvvvvv WAS iiiiii
2	CC ERR LINE 11 CC cccccc

Test	Error Message
4	BREAK TIMEOUT ON LINE 11
5,22	tTIMEOUT, LINE 11
6	CO&I NOT ON AFTER DTR, LINE 11
6	CTS NOT AFTER T, LINE 11
10	ECHO ERROR, LINE 11
11	UNABLE TO SYNC-UP LINE 11 WITH pppp
12	RE-SYNC FAILURE, LINE 11
13	TRANSMIT SYNC FAILURE, LINE 11 CHAR. pppp
14	PARITY BIT ERROR, LINE 11
15	AR FAILURE, LINE 11
16	LINE 11 SYNCS UP AFTER ONE SYNC CHARACTER
17	ASCII ERROR, LINE 11
20	LINE: 11 STATUS: xxx EXPECTED: yyy
20	LINE: LL TIME OUT ERROR
21	STATUS CHANGE INTERRUPT. LINE, CONTROL, DATA COUNT 11,nnn,ddd
21	TIMEOUT ERROR. LINE, CONTROL, DATA COUNT 11, nnn, ddd

where:

cccccc
: Is control character (may be left or right byte).

ddd
: Is data count.

e
: Is type of error where F = framing, P = parity, O = overflow, PO = parity and overflow, or D = data.

iiiiii
: Is invalid data.

kk
: Is number of lines.

ll
: Is line number.

nnn
: Is line control byte.

pppp
: Is sync character.

ss
: Is octal status.

t
: Is type of interrupt expected, O = overflow, C = control line, R = ring, D = data line error.

vvvvvv
: Is valid data.

xxx
: Is observed status.

yyy
: Is expected status.

1.6 PROGRAM EXAMPLE

The following messages are examples of typical test program messages that are displayed when various tests are performed.

```
DCM TEST

LCB ADDRESS=5L  INVALID
LCB ADDRESS=75000.
DCM ADDRESS-76.
INTERRUPT ORIGIN= 260.
LINE ADAPTER TYPE=1.
DATA PATTERN=2.
ACTIVE LINES- 1,2.
TERMINATE TEST= 1.
BIT LENGTH= 10.
TEST= 1.
TIME-OUT ON LINE  02
TIME-OUT ON LINE  02
F  ERROR LINE 01
F  ERROR LINE 01
F  ERROR LINE 01
F  ERROR LINE 01
F  ERROR LINE 01
F  ERROR LINE 01
F  ERROR LINE 01
F  ERROR LINE 01
F  ERROR LINE 01
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES= 1,1.
TERMINATE TEST= 1.
BIT LENGTH= 10.
TEST= 2.
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES= 2,2.
TERMINATE TEST= 1.
BIT LENGTH= 10.
TEST= 1.
TIME-OUT ON LINE  02
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES= 1,1/  INVALID
ACTIVE LINES= 2,2/  INVALID
ACTIVE LINES= 2,2.
TERMINATE TEST= 1.
BIT LENGTH= 10.
```

```
TEST= 2.
TIME-OUT ON LINE  02
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES = 1,1.
TERMINATE TEST= 1.
BIT LENGTH= 10.
TEST= 3.
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES= 1,1.
TERMINATE TEST= 1.
BIT LENGTH= 10.
TEST= 4.
000001 PASSES
LINE ADAPTER TYPE=1.
DATA PATTERN= 2
ACTIVE LINES= 1,1.
TERMINATE TEST= 1.
BIT LENTH= 10.
TEST= 5.
000001 PASSES
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES= 1,1.
TERMINATE TEST= 1.
BIT LENGTH= 10.
TEST= 6.
000001 PASSES
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES= 1,1.
TERMINATE TEST= 1.
BIT LENGTH= 10.
TEST=  7.
000001 PASSES
```

Section 2
Mapped Data Communications Multiplexer Test

2.1 GENERAL

The Mapped Data Communications Multiplexer (DCM) test program tests the DCM (F3000) and certain line adapters (LAD, F3001-00 through -04, -06, and -07) in a mapped environment.

The test program is designed to operate with the MAINTAIN III executive on systems with mapped memories. The test uses the virtual console interface, SENSE switch routines, I/O, timing routines, and system constants contained in the executive. This program has no console mode.

This test program is used in conjunction with the DCM test program that tests normal DCM functions. The mapped DCM test program tests only the mapped functions of the DCM. Unless the user is absolutely certain that malfunctions exist only in mapped functions, the DCM test program should be executed first.

The test program comprises a parameter set-up and a test component. The parameter set-up component requests and accepts various values to configure the software to the hardware. The test component is a single specialized test that tests DCM map functions. Any detected errors and malfunctions are optionally reported to the operator. Depending on the setting of the SENSE switches, the program provides for the logging of error or malfunction messages, error loops and halts.

Available documentation is as folows:

Document Number	Title
92( )0105-13	DCM Mapped Test (V77-600)
92( )0109-011	DCA Mapped Test (V77-400)
92( )0115-003	DCA Mapped Test (V77-800)
UP-8629	DCM Operation and Service Manual

2.2 HARDWARE REQUIREMENTS

The mapped DCM test program has the same hardware requirements as the DCM test program (paragraph 1.2). An additional requirement is the memory map feature.

2.3 DESCRIPTION OF TEST COMPONENTS

The two major components of the test program are the parameter set-up and the test. The general block diagram is illustrated in Figure 2-1.

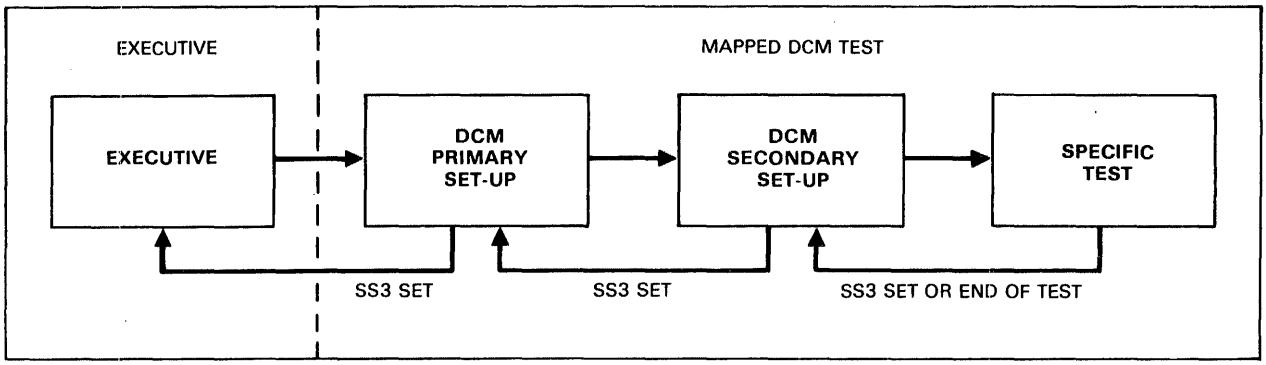

Figure 2-1. General Mapped DCM Test Block Diagram

2.3.1 PARAMETER SET-UP

The parameter set-up component, like the DCM test (paragraph 1.3), consists of two routines: primary set-up and secondary set-up. Operation and description is the same. The program is started from address 2000_8 or when SENSE switch 3 (SS3) is set during the secondary set-up routine.

During the primary set-up, the user enters the addresses for the line control block (LCB), DCM, interrupt origin, and map. Setting SS3 at any time during the primary set-up routine causes the test program to transfer control to the executive.

Operator entries for the seconday set-up are: line adapter type, data pattern, number of active lines, test duration, bit length and mirror image to be used during the test.

Valid entries for all variables are contained in the operating procedures.

2.3.2 MAPPED TEST

The memory locations that are used as transmit and receive buffers in all memory banks are mapped into memory bank 0. Each of the active lines is placed in the full-duplex mode and allowed to run continuously while using the selected data pattern. Any detected errors or malfunctions are optionally reported to the user. If so configured, the test continues after an error is detected.

2.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the mapped DCM test program can be loaded. Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4. Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, Section 1, paragraph 1.6) are used.

Since many of the entries are similar to the DCM test program which is run prior to this test, only those entries that are different are explained in this section.

2.4.1 PRIMARY SET-UP

After loading of the test program is completed, the following identification message is displayed:

```
DCM MAPPED TEST
```

The message is for information only and does not require any user response.

Setting SENSE switch 3 at any time during the remainder of the primary set-up routine causes control to be transferred to the executive.

The following messages are then sequentially displayed after the proper user response:

```
LCB ADDRESS = R.
DCM ADDRESS = R.
INTERRUPT ORIGIN = R.
```

Valid entries are the same as those used in the DCM test program (paragraph 1.4.1); however, the LCB address must not be higher than 013700_8.

After the proper addresses are entered, the following message is displayed:

```
MAP DA = R.
```

Enter the octal device address of the map.

2.4.2 SECONDARY SET-UP

Setting SENSE switch 3 at any time during the secondary set-up routine causes the program to transfer control to the primary set-up routine.

The first message that is displayed is:

```
LINE ADAPTER TYPE = R.
```

Enter a single digit to represent the type of line adapter under test. The valid entries are:

Entry	Description
1	A synchronous LAD (F3001-00)
2	Direct connection LAD (F3001-01 through -03)
4	Synchronous LAD (F3001-04)

Once the line adapter type is selected, the following messages are sequentially displayed after the proper user response:

```
DATA PATTERN = R.
ACTIVE LINES = R.
TERMINATE TEST = R.
BIT LENGTH = R.
```

The valid entries are the same as those used in the DCM test program (paragraph 1.4.2) mirror image is requested only if the bit length under test is seven bits or less. The message is:

```
MIRROR IMAGE = R.
```

Valid entries for the preceding message requests are the same as those used in the DCM test program.

2.4.3 TEST PROGRAM MESSAGES

Messages encountered prior to performing the test program are:

```
DCM MAPPED TEST
LCB ADDRESS =
DCM ADDRESS =
INTERRUPT ORIGIN =
MAP DA =
LINE ADAPTER TYPE =
DATA PATTERN =
ACTIVE LINES =
TERMINATE TEST =
BIT LENGTH =
MIRROR IMAGE =
```

Normal termination of the test causes the number of completed test passes to be displayed:

```
n PASSES
```

where:

n
: Is the octal number of passes.

2.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages are:

```
TIMEOUT ON LINE 11 MAP mm
INVALID USE OF LINE 11
eERROR ON LINE 11
SC INTERRUPT FROM LINE 11 ss
MEMORY FULL, CAN'T START kk LINES
CMP ERR LINE 11 SHBE vvvvvv WAS iiiiii MAP mm
MAP TIMEOUT
```

where:

e
: Is type of error where F = framing, P = parity, O = overflow, PO = parity and overflow.

iiiiii
: Is invalid data.

kk
: Is number of lines.

11
: Is line number.

mm
: Is map.

ss
: Is octal status.

vvvvvv
: Is valid data.

2.6 PROGRAM EXAMPLE

The following messages are examples of typical test program messages that are displayed when various tests are performed.

```
DCM MAPPED TEST

LCB ADDRESS=75000.
DCM ADDRESS=76.
INTERRUPT ORIGIN= 260.
MAP DA= 46.
LINE ADAPTER TYPE=1.
DATA PATTERN= 2.
ACTIVE LINES= 0,3.
TERMINATE TEST= 1.
BIT LENGTH= 10.
LINE ADAPTER TYPE=

(The remainder of this
test is the same as
the DCM test in part
3, Section 1.6).
```

Section 3
Binary Synchronous Control Line Adapter Test

3.1 GENERAL

The Binary Synchronous Control (BSC) Line Adapter (LAD) test program tests the BSC LAD (F3000-05) when the line adapter is installed as part of the data communications multiplexer (DCM, F3000).

The program is designed to operate with the MAINTAIN III executive on DCM systems. The test uses the virtual console interface, SENSE switch routines, I/O, timing routines, and system constants contained in the executive.

This test program is used in conjunction with the DCM test program that tests normal DCM multiplexer functions. The BSC test program tests only the BSC functions of the DCM. The program comprises several specialized tests that are requested by the user. Each test is designed to check the operation of a specific part of the BSC LAD. Modularizing of the test program facilitates testing during fault isolation. Any detected errors and malfunctions are optionally reported to the operator. Depending on the setting of the SENSE switches, the program provides for the logging of error or malfunction messages, error loops and halts.

Available documentation is as follows:

Document Number	Title
92( )0106-017G	Binary Synchronous Control Line Adapter Test
UP-8629	Data Operation and Service Manual Data Communications Multiplexer

3.2 HARDWARE REQUIREMENTS

The BSC test program requires a V70 computer with at least 12K words of memory, a DCM, and at least one BSC LAD.

The BSC LAD under test must have a test connector wired as shown in the DCM Operation and Service Manual.

3.3 DESCRIPTION OF TEST COMPONENTS

The two major components of the test program are the parameter set-up and the test. The general block diagram is illustrated in Figure 3-1.

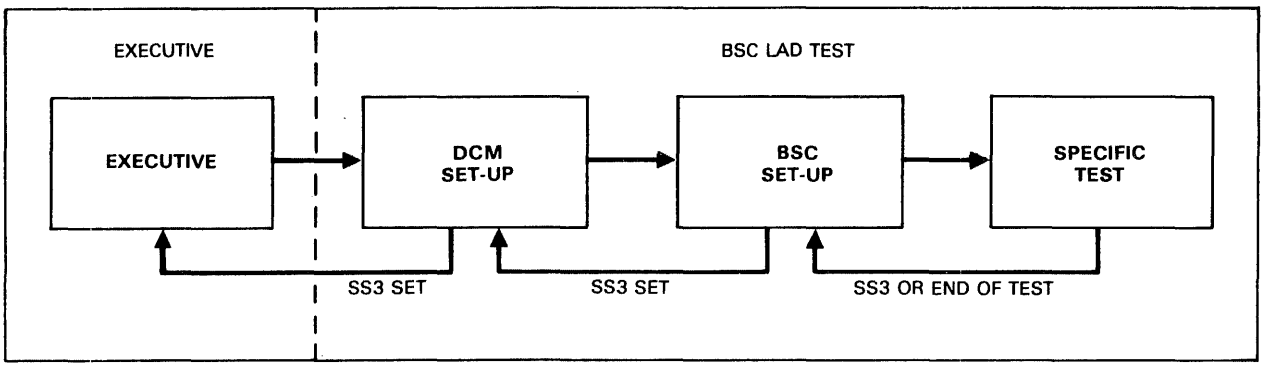

Figure 3-1. General BSC LAD Test Flow Diagram

3.3.1 PARAMETER SET-UP

The parameter set-up component consists of two routines: DCM set-up and BSC set-up.

The DCM set-up routine clears various constants and tables to initialize the test program. This routine is executed each time the program is started from address 1000_8 or when SENSE switch 3 (SS3) is set during the BSC set-up routine. During the routine, the executive indicator $CON is tested to determine if a teletypewriter or console is available.

During this phase:

- The program identification message is displayed and
- The operator enters the line control block (LCB), DCM, and interrupt origin addresses.

Setting SS3 at any time during the primary set-up routine causes the test program to transfer control to the executive.

The BSC set-up routine initializes variables that pertain to the BSC LAD under test. This routine also provides the software procedures for the orderly shutdown of the program in the event of an operator initiated test termination. When any test has been completed, this routine causes a display of the number of passes through the test.

Operator entries which must be made during this phase are:

- Parameter changes if required
- Data pattern required for the test
- Data mode to be used
- Wide-band interface requirement
- Lines to be tested
- Number of test passes
- Test to be executed

Entries are checked for proper values. If the entry is not within the proper range, the parameter is re-requested.

Setting SS3 at any time during the BSC set-up routine causes the test program to transfer control to the DCM set-up routine.

Valid entries for all variables are contained in the operating procedures.

3.3.2 TEST SELECTION

Descriptions of the selectable tests are contained in the following paragraphs. Each selected line is tested. Any errors or malfunctions are reported to the user if SS1 is reset. Setting SS3 terminates the test.

3.3.2.1 Test 0 Transmit Only

This test is designed to test each active line in the transmit mode only. Active lines are placed in the transmit mode and allowed to run continuously while using the selected data pattern. The test is terminated by setting SS3. No count of the number of test passes is maintained. Data pattern 2 is not allowed and this test is excluded from burn-in (test 77).

3.3.2.2 Test 1 Output and Display

This test is designed to verify the correct functioning of the transmit logic in transferring data and formulating and transferring a block check character (BCC).

Each active line is tested sequentially for its ability to transfer data. The line is placed in the transmit and test receive mode to allow all output data characters to be transferred, without hardware control character stripping, to the processor. The first 20 characters in the input data buffer are transferred to the TTY and the appended BCC is verified for data patterns 0 and 3. Error reports are to be expected with slow data transfer rates because the BSC LAD injects SYN characters at one-second intervals. The injected SYN character causes the input buffer to increase in size and consequently the BCC character position is moved. The movement is transparent to the program. An error will result in a display of the error message: BCC ERR SHBE vvvvvv WAS 111111 (paragraph 3.5). Data pattern 2 is not allowed in this test. If data pattern 4 is selected, the received BCC is not tested.

3.3.2.3 Test 2 Input/Output (I/O)

This test is designed to test each active line in the full duplex mode. The program appends the correct starting and ending control character sequences to the selected data pattern. Data patterns 2 and 4 are not allowed. The receiver strips all control characters and then strips and checks the BCC. The received data is compared to the output data and any detected data errors result in a display of the error messages (paragraph 3.5):

- CMP ERR LINE 11
- SHBE vvvvvv WAS 111111

3.3.2.4 Test 3 Loop Back

The test is designed to verify the internal cycling of data when the loop back (LB) bit is set and the test connector is removed.

After the test connector has been removed by the user, the program sets the LB bit and places each active line in the full duplex mode. The I/O test (test 2) is then executed. This test is not included as part of the burn-in (test 77) sequence since the test connector must be removed for loop back verification.

3.3.2.5 Test 4 BSC Output Control Characters

This test is designed to verify BSC-control-character-transmission detection. Active lines are placed in the transmit and test receive mode. A total of 14 EBCDIC and 12 ASCII messages are transmitted in the EBCDIC, UWT and UNT data modes. Both normal and transparent control characters are attached to and imbedded in the prepared messages. The receiver transfers the formulated messages to the processor without stripping the control characters. The

program verifies the reception of an output complete status change interrupt and the reception of the correct message for each message sequence transmitted. The transmission of the correct BCC (CRC-16) is checked when the BSC LAD is in the EBCDIC and UWT data modes. The transmission of the correct BCC (CR-8) is also checked when the BSC LAD is in the UNT data mode. Any errors or malfunctions are optionally reported to the user.

3.3.2.6 Test 5 BSC Input Control Characters

This test is designed to verify BSC-control-character-receive detection by using portions of the test 4 program.

Active lines are placed in the test transmit and receive mode. The receiver strips all control characters prior to transferring the formulated messages to the processor. The program then verifies the reception of a control character detect status change interrupt for each message sequence received. The rest of the test description remains the same as for test 4.

3.3.2.7 Test 6 Intermediate Transmission Block (ITB) Output

This test is designed to verify the ability of the no-block-check (NBC) bit in the control byte to control BCC accumulation when ITB data streams are encountered. Portions of test 4 and 7 are used.

Active lines are placed in the transmit and test receive mode. EBCDIC and ASCII messages from test 4 are transmitted and received. Both normal and transparent ITB characters are imbedded and appended to the fixed data messages. The NBC bit is tested for BCC accumulation control when ITB characters are present or absent. When the NBC bit is reset, the ITB character causes a control-character-detect-status-change interrupt for each message received. When the NBC bit is set, the ITB character is treated as data. Any errors or malfunctions are optionally reported to the user.

3.3.2.8 Test 7 Intermediate Transmission Block (ITB) Input

This test is designed to verify the ability of the no-block-check (NBC) and input-ITB (IIB) bits in the control byte to detect ITB data messages.

Active lines are placed in the receive and test transmit mode. Both normal and transparent ITB characters are imbedded and appended to fixed data messages from test 6. The NBC and IIB bits are tested for BCC accumulation and ITB transfer to the processor. The ability to treat the ITB character as control and to strip the same character from the data message is verified by resetting both the NBC and IIB bits. Any errors or malfunctions are optionally reported to the user.

3.3.2.9 Test 10 DCM Control Character Detection

This test is designed to test and exercise the control character detection logic of the DCM.

Active lines are sequentially placed in the full-duplex mode while using the ascending binary data pattern (data pattern 2). Regardless of what pattern is chosen by the user, the program forces data pattern 2 into the test stream. Each line is tested for the recognition of control characters. A total of 252 out of 254 (0 and 32 are not used) possible control characters are tested. After a line has been tested, the next active line is tested. Any error or malfunction is optionally reported to the user with the error message (paragraph 3.5):

CCOERR LINE 11 CC cccccc

3.3.2.10 Test 11 Line Error, Ring, and Underflow Interrupts

This test is designed to test the DCM interrupts while using data patterns 1 through 3. Data pattern 4 is not allowed.

Active lines are tested for a correct response when an interrupt is detected. The interrupts comprise:

- Line error format
- Line error BCC
- Line error timeout
- Line error overflow
- Status change ring
- Status change underflow

The ring interrupt for a direct-connection line adapter is not tested. Any errors or malfunctions are reported to the operator.

3.3.2.11 Test 12 Status Check

This test is designed to test each active line for correct status responses.

The correct test connector (DCM Operation and Service Manual) must be utilized for the LAD under test. The response of the RS232 interface is tested when activated by the data-terminal-ready (DTR), transmit (T), and control-line-1 (C1) bits of the control byte. The wideband interface is tested by activating the T and C1 bits of the control byte. Any errors or malfunctions are optionally reported to the user.

3.3.2.12 Test 13 Large Block Transfer

This test is designed to test for large byte count.

Active lines are placed in the full-duplex mode and are allowed to transmit a large block (4096 bytes) of random data. The large block is received as small blocks (256 bytes) and the next-to-last-word is tested.

3.3.2.13 Test 14 High Speed Poll

This test is designeed to test rapid time turn around (transmit-to-receive). The program software turns the receiver on without waiting for a user command.

3.3.2.14 Test 77 Burn-In

This test is designed to test all functions of the BSC LAD during burn-in.

This test cycles continuously through all BSC LAD tests except for test 0, 3, and 14. The alternating ones and zeros data pattern is used for tests 1 and 2. Tests 4 through 7, 11, and 12 use preselected data patterns. Test 10 uses the ascending binary data pattern and test 13 uses random data.

3.4 OPERATING PROCEDURES

The MAINTAIN II executive must be loaded and operational before the BSC LAD test program can be loaded. Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4.

Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, Section 1, paragraph 1.6) are used.

Two parameter entry modes are available: teletypewriter and console.

3.4.1 TELETYPEWRITER MODE

In this mode, all entries and responses are made via a teletypewriter.

3.4.1.1 DCM Set-up

After loading of the test program is completed, the following identification message is displayed:

```
BSC TEST
```

The message is for information only and does not require any user response.

Setting SENSE switch 3 (SS3) at any time during the remainder of the primary set-up routine causes the program to transfer control to the executive.

The following messages are then sequentially displayed after the proper user response:

```
LCB ADDRESS = R.
DCM ADDRESS = R.
INTERRUPT ORIGIN = R.
```

Valid entries are the same as those used in the DCM test program (Part 3, Section 1.4.1). The LCB address can go as high as 076000.

3.4.1.2 BSC Set-up

Setting SS3 at any time during the BSC set-up routine causes the program to transfer control to the primary set-up routine.

The first message that is displayed on a second and subsequent test is:

```
PARAMETER CHANGES = R.
```

Valid responses are:

Entry	Description
0	No. Bypass the BSC set-up routine, utilize previous parameter values.
1	Yes. Start BSC set-up routine, all new values are to be used.

The entry is not required for the initial test since there are no test parameters in memory from which to work from.

On the initial test, the following message is the first message displayed.

```
DATA PATTERN = R.
```

Enter an octal value that corresponds to the desired test data pattern. The valid entries are:

Entry	Description
0	All zeros
1	All ones
2	Ascending binary
3	Alternating ones and zeros
4	User pattern

Responses of 0 through 3 cause a 128-word data buffer to be formed. A start-of-text (STX) and end-of-text (ETX) control character replace the first and last characters in the buffer. Data pattern 2 can only be used in test 10.

A response of 4 builds a data buffer whose length is a function of the operator input message. The pattern can only be use tests 0 and 1. The program does not append control characters to the data buffer formed from the operator input. The user can enter any data pattern that is to be used by the test. The data pattern is entered after the 4. entry and is itself terminated with a period. For example:

DATA PATTERN = 4.1,2,',4.

The test data mode is entered after the following message is displayed:

DATA MODE = R.

Enter a single digit that represents the mode. Valid entries are:

Entry	Description
0	EBCDIC with transparent text capability. The UNT and UWT bits of the mode selection byte are reset.
1	ASCII without transparent text capability. The UNT bit is set and the UWT bit is reset.
2	ASCII with transparent text capability. The UNT bit is reset and the UWT bit is set.

The interface to be used during the test is specified after the following message is displayed:

WIDE BAND INTERFACE = R.

Enter a single digit that designates the type of interface to be tested. Valid entries are:

Entry	Description
0	No. An RS232 interface test connector is installed with signal DTR connected to signals DSR and CO.
1	Yes. A wide-band interface test connector is installed with signal C1 connected to signals DSR and S.

The number of lines to be tested is entered after the following message is displayed:

ACTIVE LINES = R,R.

Enter two line numbers, separated with a comma and terminated with a period, that correspond to the first and last line (inclusive) to be used during the test.

The number of test cycles to be performed is specified next. The following message is displayed:

TERMINATE TEST = R.

Enter a 0. for continuous testing or a 1. to terminate the test after one pass. To terminate a continuous test, set SENSE switch 3.

The test to be conducted on the line adapter is selected after the following message is displayed:

TEST = R.

The valid entries are:

Entry	Description
0	Transmit only
1	Output and display
2	Input and output
3	Loop back
4	BSC output control characters
5	BSC input control characters
6	Intermediate transmission block output
7	Intermediate transmission block input
10	DCM control character detection
11	Line error, ring, and underflow interrupts
12	Status check
13	Large block transfer
14	High speed poll
77	Burn-in

3.4.2 CONSOLE MODE

In this mode, all entries and responses are made via a CRT terminal. Routine halts are made at various points in the parameter set-up to allow the user to enter parameters into registers. Valid entries are the same as those given for the teletypewriter mode (paragraph 3.4.1).

Primary set-up entry points are:

Program Halt	Description	Entry Register
01	LCB ADDRESS =	A
	DCM ADDRESS =	B
	INTERRUPT ORIGIN =	X

Secondary set-up entry points are:

Program Halt	Description	Entry Register
02	DATA PATTERN TYPE =	A
	DATA MODE =	B
03	INTERFACE TYPE =	B
	FIRST ACTIVE LINE =	X
	LAST ACTIVE LINE =	A
04	TERMINATE TEST =	A
	TEST NUMBER =	B

3.4.3 TEST PROGRAM MESSAGES

Messages encountered prior to performing the test program are:

```
BSC TEST
LCB ADDRESS =
DCM ADDRESS =
INTERRUPT ORIGIN =
PARAMETER CHANGES = (encountered on second and
                     subsequent tests
DATA PATTERN =
DATA MODE =
WIDE-BAND INTERFACE =
ACTIVE LINES =
TERMINATE TEST =
TEST =
```

Normal termination of the test causes the number of completed test passes to be displayed:

```
n PASSES
```

where:

n
: Is the octal number of passes.

3.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages and the applicable tests are:

Test	Error Message
ALL	TIMEOUT ON LINE 11
ALL	INVALID USE OF LINE 11
4,6,7	CMP ERR LINE LL SHBE vvvvvv WAS MSGE-cc
0	IBCZ INTERRUPT FROM LINE 11
0	DATA PATTERN n NOT VALID FOR THIS TEST
ALL	eERROR ON LINE 11
ALL	SC INTERRUPT sss
1	BCC ERR SHBE vvvvvv WAS iiiiii
2,3	CMP ERR LINE 11 SHBE vvvvvv WAS iiiiii
4,5,6,7	NO si SCI WITH dddddd MSGE-cc LINE 11
10	CC ERR LINE 11 CC cccccc
11	LINE ERROR INTERRUPT FROM LINE 11
ALL	MEMORY FULL, CAN'T START kk LINES
11	t TIMEOUT, LINE 11
12	CO&I NOT ON AFTER DTR, LINE 11
12	CTS NOT AFTER T, LINE 11
12	s NOT ON AFTER Cl, LINE 11
12	CP, I&S NOT ON AFTER Cl, LINE 11
13	LARGE BLOCK DATA ERROR, LINE 11

where:

cc
: Is message type:

01=EBCDIC	STX, ETX CRC-16
02=EBCDIC	SOH, ETX CRC-16
03=EBCDIC	STX, ETB CRC-16
04=EBCDIC	SOH, ETB CRC-16
05-EBCDIC	STX, EOT CRC-16
06=EBCDIC	0, EOT CRC-16
07=EBCDIC	STX, ENQ CRC-16
10=EBCDIC	0, ENQ CRC-16
11=EBCDIC	0, ACKO CRC-16

```
12=EBCDIC  0, NAK                                          CRC-16
13=EBCDIC  DLE, STX, 0, ETX                                CRC-16
14=EBCDIC  DLE, STX, 0, ETB                                CRC-16
15=EBCDIC  DLE, STX, 0, ENQ                                CRC-16
16=EBCDIC  DLE, STX, DLE, ETX                              CRC-16
17=ASCII   STX, ETB                                        CRC-16
20-ASCII   SOH, ETB                                        CRC-16
21=ASCII   STX, EOT                                        CRC-16
22=ASCII   0, EOT                                          CRC-16
23=ASCII   STX, ENQ                                        CRC-16
24=ASCII   0, ENQ                                          CRC-16
25=ASCII   0, ACKO                                         CRC-16
26=ASCII   0, NAK                                          CRC-16
27=ASCII   DLE, STX, 0, ETB                                CRC-16
30=ASCII   DLE, STX, 0, ENQ                                CRC-16
31=ASCII   STX, ETB                                        CRC-8
32=ASCII   0, EOT                                          CRC-8
40=EBCDIC  STX, ITB, STX, ETX NBC Reset                    CRC-16
41=EBCDIC  STX, ITB, STX, ETX NBC Set                      CRC-16
42=ASCII   STX, ITB, STX, ETX NBC Reset                    CRC-16
43=ASCII   STX, ITB, STX, ETX NBC Set                      CRC-16
50=EBCDIC  STX, ITB, STX, ETX NBC Reset 11B Set            CRC-16
51=EBCDIC  STX, ITB, STX, ETX NBC Set   11B Set            CRC-16
52=ASCII   STX, ITB, STX, ETX NBC Reset 11B Reset          CRC-16
53=ASCII   STX, ITB, STX, ETX NBC Set   11B Set            CRC-16
54=EBCDIC  STX, ITB, STX, ETX NBC Reset 11B Reset          CRC-16
```

cccccc
: Is control character (may be left or right byte).

dddddd
: Is type of code structure, EBCDIC and ASCII.

e
: Is type of error, B = BCC, F = format, O = overflow, and T = timeout.

kk
: Is number of lines.

iiiiii
: Is invalid data.

ll
: Is line number.

n
: Is data pattern number.

t

Is type of interrupt expected where: B = BCC line error, F = format line error, O = overflow status change interrupt, T = timeout line error, and U = underflow status change interrupt.

si

Is type of status change interrupt expected, OC = output complete and CD = control character detected.

sss

Is octal status.

vvvvvv

Is valid data.

3.6 PROGRAM EXAMPLE

The following messages are examples of typical test program messages that are displayed when various tests are performed.

```
BSC TEST

LCB ADDRESS=17000.
DCM ADDRESS=70.
INTERRUPT ORIGIN= 60.
DATA PATTERN= 0.
DATA MODE=0.
WIDE-BAND INTERFACE=0.
ACTIVE LINES= 1.1.
TERMINATE TEST= 1.
TEST= 1.
LINE  01
031062 001000 000000 000000 000000 000000 000000 000000 000000 000000
000001 PASSES
PARAMETER CHANGES=0.
TERMINATE TEST= 1.
TEST= 2.
000001 PASSES
PARAMETER CHANGES=0.
TERMINATE TEST= 1.
TEST= 4.
000001 PASSES
PARAMETER CHANGES=0.
TERMINATE TEST= 1.
TEST= 5.
000001 PASSES
```

Section 4
Universal Data Link Control Line Adapter Test

4.1 GENERAL

The Universal Data Link Control (UDLC) Line Adapter (LAD) test program tests the UDLC LAD (F3060-00) when the line adapter is installed as part of the data communications multiplexer (DCM, F3000).

The program is designed to operate with the MAINTAIN III executive on DCM systems. The test uses the virtual console interface, SENSE switch routines, system constants, I/O, and timing routines contained in the executive.

The test program is designed to interface with the DCM. Although the UDLC LAD is designed to be used in various bit-protocol environments such as SDLC and UDLC, the test program does not use these protocols. The program comprises a primary parameter set-up, a secondary parameter set-up, and a test selection component. The primary and secondary set-up components initialize the test program, then requests and accepts various values to configure the software to the hardware. Operator entries are tested to ensure that the entries are within certain specified ranges. The test selection component allows the operator to select one of several specialized tests that is to be used to exercise the UDLC LAD. Each test is designed to test the operation of certain portions of the UDLC LAD which assists in fault isolation. Depending on the setting of the SENSE switches, errors or malfunctions are optionally reported to the operator. Error reporting comprises error or malfunction messages, error loops, and halts.

Available documentation is as follows:

Document Number	Title
92( )0109-013	Bit Oriented Protocol LAD Test Program
UP-8629	Data Communications Multiplexer Operation and Service Manual

4.2 HARDWARE REQUIREMENTS

The minimum hardware requirements are as follows:

- One V77 series computer with 12K words of memory
- One DCM with a UDLC LAD installed

- One test connector wired as shown in the DCM Operation and Service Manual
- One virtual console

The test connector must be connected to the line adapter under test. The connector provides a test clock for back-to-back testing. For test purposes, this clock must be 4800 Hz.

4.3 DESCRIPTION OF TEST COMPONENTS

The two major components of the test program are the parameter set-up and the specific test selection. The general program flow chart is illustrated in Figure 4-1.

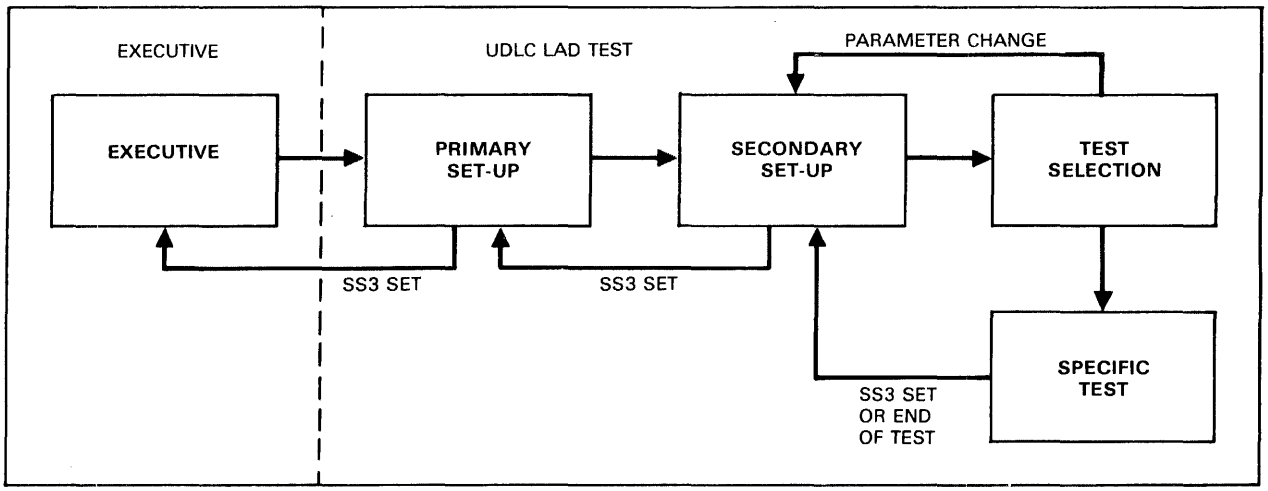

Figure 4-1. General UDLC LAD Test Block Diagram

4.3.1 PARAMETER SET-UP

The parameter set-up component consists of two routines: primary set-up and secondary set-up.

The primary set-up routine clears various constants and tables to initialize the test program. This routine is executed each time the program is started from address 1000_8 or when SENSE switch 3 (SS3) is set during the secondary set-up.

During this phase:

- the program identification message is displayed and
- the operator enters the line control block (LCB), DCM, and interrupt origin addresses.

Setting SS3 at any time during the primary set-up routine causes the test program to transfer control to the executive.

The secondary set-up routine initializes variables that pertain to the line adapter under test. This routine also provides the software procedures for the orderly shutdown of the program in the event of an operator initiated test termination. When any test has been completed, this routine causes a display of the number of passes through the test.

Variable entries which must be made during this phase are:

- Parameter changes if required
- Data pattern to be used
- User pattern if required
- Character length to be used
- Active lines to be tested
- Single or multiple test cycles to be conducted.

Setting SS3 at any time during the secondary set-up routine causes the test program to transfer control to the primary set-up routine.

Valid entries for all variables are contained in the operating procedures.

4.3.2 TEST SELECTION

Descriptions of the selectable tests are contained in the following paragraphs. Any errors or malfunctions are reported to the user if SS1 is reset. The operator can terminate a test by setting SS3.

Test considerations:

- At 4800 Hz, a maximum of four lines can operate simultaneously in the full-duplex mode.
- Test 0 runs the active lines simultaneously in the transmit-only mode.

- Tests 1, 10, and 11 run active lines simultaneously in the full-duplex mode.
- All other tests sequentially exercise the active lines.

4.3.2.1 Test 0 Transmit Only

Each active line is placed in the transmit mode with receiver disabled and allowed to run continuously. The selected character length and data pattern are used. Transmit complete status is checked during the test. This test is not run during test 77 (burn-in).

4.3.2.2 Test 1 Transmit and Receive

Each active line is placed in the full-duplex mode and allowed to run continuously while using the selected data pattern and character length. Each line transmits 256 bytes. The transmit status, receive status, and data are checked for errors. If there is not enough memory to start another line, an error message is displayed. If the maintenance mode flag (MMFLG) is set, the routine is modified to set the appropriate control bits.

4.3.2.3 Test 2 Control Character

The ability of the DCM to detect control characters is tested. Each active line is placed in the full-duplex mode and each active line is checked for correct recognition of all 256 possible control characters. Each character is separately checked in both the high and low byte positions. If a control character is not detected, an error message is displayed. This test is not run during test 77 (burn-in).

4.3.2.4 Test 3 Transmit Residual Bits

Active lines are tested for the ability to handle all possible character lengths with all possible residual bits. Each active line is placed in the full-duplex mode. On each active line the transmitter and receiver character lengths are set to maximum (eight bits) and the residual bit length is set to seven bits (one bit less than the character length). Four bytes are transmitted and received. The transmit residual number is compared to the assembled bit count for the save value. If there is no error, the residual number is decremented by one, data is transmitted, received, and compared. Decrementing and testing continues until after the residual number of one is tested. At this time, the character length is decremented to seven and the residual number is set to six (one bit less than the character length). Testing and decrementing continues until all possible combinations of character lengths and residual numbers are tested.

4.3.2.5 Test 4 Abort Message

Active lines are tested for the ability to properly abort a transmission. Each active line is placed in the full-duplex mode. A normal transmit and receive sequence is initiated with a random delay. At the end of the delay, the message is aborted. The transmit and receive status are tested for correct status.

4.3.2.6 Test 5 Ring Indicator

Active lines are tested for the correct interrupt response to the accept ring (AR) control bit. A data terminal ready (DTR) signal is transmitted and received on the ring indicator via the test connector. With the AR bit set, the line responds with a status change interrupt.

4.3.2.7 Test 6 Idle

Active lines are tested for the correct interrupt response to a control read. Each active line is placed in the idle mode. A control read is issued to the idle line and the status is tested.

4.3.2.8 Test 7 Large Block Transfer

Active lines are tested for the ability to handle a large block length of 4095 bytes. A search is made for an unused 4K block of memory. If a block is not found, an error message is displayed and the test is aborted. When a 4K memory block is found, the block is designated as an input and output buffer for the 4095 byte-block transfer (on the last word received, only the left byte is valid). The lower half of the buffer is filled with random data. Each active line is placed in the full-duplex mode and a transmit sequence is initiated. When the sequence is complete, the status of the line and the data are tested.

4.3.2.9 Test 10 Maintenance Mode

Active lines are tested for the maintenance mode condition. The maintenance mode bit is set and then each of the active lines is placed in the full-duplex mode. The transmit data is internally connected to the receiver by the UDLC LAD. Test 1 is then used as a test.

4.3.2.10 Test 11 Transmit Flags

Active lines are tested for the ability to distinguish a flag character (01111110) and a data character. Each of the active lines is placed in the full-duplex mode, the data pattern is set equal to the flag character, and

the character length is set to 8 bits. Test 1 is called in order to perform the data transfer. The receive data is checked for the proper content.

4.3.2.11 Test 12 Secondary Station

Active lines are tested for the ability to properly receive or ignore messages when the line is in the secondary station mode. Each of the active lines is placed in the full-duplex mode and set to be a secondary station. A table of 16 different addresses is used as the station or message address. As messages with various addresses are transmitted, the addresses are compared to secondary station address. When the addresses are the same, the line receives the message. All other messages are rejected.

4.3.2.12 Test 13 All Parties Address

Active lines are tested for the ability to respond to the all parties address command. Each active line is placed in the full-duplex mode and set to be a secondary station with the all parties address (APA) bit set. Various combinations of addresses are set into the secondary station address register while the transmitted message address is set to all ones. The line's ability to receive the message is verified.

4.3.2.13 Test 14 Transmit One Byte

Active lines are tested for reaction to an illegal transmission of one byte (minimum length is two bytes). Each active line is placed in the full-duplex mode. The transmit byte count is set to one and a transmit sequence is initiated. When the transmission is completed, the transmit status is checked for an idle condition that indicates the receiver did not respond to the invalid message.

4.3.2.14 Test 15 Receive One Byte

Active lines are tested for a receiver overrun error. Each active line is placed in the full-duplex mode. The receive byte count is set to one and a 256-byte message is initiated. At the completion of the message, a normal transmit complete status and a receive status of receiver overrun (ROR) is detected.

4.3.2.15 Test 16 Transmitter Error

Active lines are tested for a transmitter error. Each active line is placed in the transmit mode and a 256-byte transfer is initiated. After a software delay, interrupts are disabled and a control write is requested. The request causes the DCM to stop scanning while the DCM tries to service the interrupt.

In addition, DMA activity is inhibited and the DCM transmitter error (TERR) bit is set. After another delay, the interrupts are enabled and the next line is tested.

4.3.2.16 Test 17 Transmit Only (Debug)

This test allows changes in buffer length when debugging a board. The user selects a buffer length that is smaller than the standard 256 bytes and test 0 is executed. This test should only be used during the debug phase when smaller buffer lengths allow for easier troubleshooting.

4.3.2.17 Test 20 Transmit and Receive (Debug)

The description for this test is the same as for test 17 except that test 1 is called instead of test 0.

4.3.2.18 Test 77 Burn-in

This test is designed to test all functions of the UDLC LAD during burn-in. This test cycles through all the previously described tests except for tests 0, 2, 17 and 20. Each test reports errors to the operator.

4.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the UDLC LAD test program can be loaded. Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4.

Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, Section 1, paragraph 1.6) are used.

4.4.1 PARAMETER SET-UP

The parameter set-up component consists of two routines: primary set-up and secondary set-up.

4.4.1.1 Primary Set-up

After loading of the test program is completed, the following identification message is displayed:

THIS IS THE BOP LAD DIAGNOSTIC PROGRAM

The message is for information only and does not require any user response.

Setting SENSE switch 3 (SS3) at any time during the remainder of the primary set-up routine causes the program to transfer control to the executive.

The following messages are then sequentially displayed after the proper user response:

LCB ADDRESS = R.
DCM ADDRESS = R.
INTERRUPT ORIGIN = R.

Valid entries are the same as those used in the DCM test program (paragraph 1.4.1).

4.4.1.2 Secondary Set-up

The secondary set-up obtains secondary parameters and provides the routines for the orderly shutdown of the test in the event of an operator initiated termination. The routine is entered when SS3 is set while a test is in progress, or when a test terminates.

Setting SS3 u i th s a y set-up routine causes the program to transfer control to the primary set-up routine.

The first message that is displayed on a second and subsequent test is:

PARAMETER CHANGE = R.

Valid responses are:

Entry	Description
0	No. Bypass the secondary set-up routine, utilize previous parameter values.
1	Yes. Start secondary set-up routine, all new values are to be used.

The test data pattern is requested when the following message is displayed:

DATA PATTERN = R.

Enter an actual value that corresponds to the desired test data pattern. The valid entries are the same as those used in the DCM test program (paragraph 1.4.2).

If a data pattern of 4 is selected, the program responds with the message:

USER PATTERN = R.

Enter the desired octal data pattern.

The character length to be used is selected after the following message is displayed:

CHARACTER LENGTH = R.

Enter a character length within the range of 01 through 010. All other entries are rejected and the request is repeated.

The number of lines to be tested is entered after the folowing message is displayed:

ACTIVE LINES = R1,R1,...R8.

Enter the line numbers of the lines that are to be tested. The program accepts up to eight line numbers. Separate line numbers with a comma and terminate the last line number with a period. The line numbers must be in the range of 0 through 77_8.

The number of test cycles to be performed is specified next. The following message is displayed:

TERMINATE TEST = R.

Enter a 0 for continuous testing (terminate by setting SS3) or a 1 to terminate the test after one pass.

4.4.2 TEST SELECTION

The test to be conducted on the active lines is selected after the following message is displayed:

TEST = R.

A brief description of each valid test is contained in paragraph 4.3.2. Enter the number of the test to be performed. Valid entries are:

Entry	Description
0	Transmit only
1	Transmit and receive
2	Control character
3	Transmit residual bits
4	Abort message
5	Ring indicator
6	Idle
7	Large block transfer
10	Maintenance mode
11	Transmit flags
12	Secondary station
13	All parties address
14	Transmit one byte
15	Receive one byte
16	Transmitter error
17	Transmit only (Debug)
20	Transmit and receive (Debug)
77	Burn-in

4.4.3 TEST PROGRAM MESSAGES

Messages that are encountered prior to performing the test program are:

```
THIS IS THE BOP LAD DIAGNOSTIC PROGRAM
LCB ADDRESS =
DCM ADDRESS =
INTERRUPT ORIGIN =
PARAMETER CHANGE =
DATA PATTERN =
USER PATTERN =
CHARACTER LENGTH =
ACTIVE LINES =
TERMINATE TEST =
TEST =
```

Normal termination of the test causes the number of completed test passes to be displayed:

```
nnnnnn PASSES
```

where:

n
: Is the octal number of passes.

4.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages and the applicable tests are:

Test	Error Message
ALL	TIME-OUT ON LINE 11
ALL	TRANSMIT STATUS ERROR LINE 11 SHBE ssss WAS ssss
ALL	RECEIVE STATUS ERROR LINE 11 SHBE ssss WAS ssss
ALL	NO TRANSMIT COMPLETE INTR. LINE DD
ALL	NO RECEIVE COMPLETE INTR. LINE DD
1,3,7,11	DATA COMPARE ERROR LINE 11 SHBE dddddd WAS dddddd
ALL	MEMORY FULL, CANNOT START 11 LINES
2	CTRL CHAR ERR LINE 11 CTRL CHAR cccccc
12,13	RECEIVED WRONG MSG LINE LL STA = aaaa MSG = aaaa
12,123	DID NOT RECEIVE MSG LINE 11 STA = aaaa MSG = aaaa
7	NOT ENOUGH MEMORY TO RUN TEST
17,20	BUFFER LENGTH =

where:

aaaa
: Is the station or message address.

cccccc
: Is the control character.

dddddd
: Is the data.

11
: Is the line number.

ssss
: Is the status byte.

Part 4
Controllers

Part 4 of the MAINTAIN III Communications Equipment and Controllers Test Programs User Guide contains test programs that are used in testing SPERRY UNIVAC V77 controllers.

This part of the guide consists of:

Section 1 - UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLER (UASC) TEST. Contains a test description and test operating procedures used in testing the UASC (F3004).

Section 2 - PRIORITY MEMORY ACCESS (PMA) BLOCK TRANSFER CONTROLLER (BTC) TEST. Contains a test description and test operating procedures used in testing the PMA BTC (F3024).

Section 3 - DATA ACQUISITION CONTROLLER (DAC) TEST. Contains a test description and test operating procedures used in testing the DAC (F2963).

Section 1
Universal Asynchronous Serial Controller Test

1.1 GENERAL

The Universal Asynchronous Serial Controller (UASC) test program tests the operational status of the UASC (F3004).

The program is designed to operate with the MAINTAIN III executive. The test uses the virtual console interface, SENSE switch routines, system constants, I/O, and timing routines contained in the executive.

The UASC is a character buffered serial controller that can operate in both half- or full-duplex mode. Four interfaces are available to the user: RS232, current loop, relay and DTL/TTL. The controller is not a data set controller but is designed for use on direct connection interfaces. Operating capabilities are: one start bit and one or two stop bits; 5, 6, 7, or 8 bits of data; parity or no parity bit; odd or even parity; and an operating frequency of 45 through 9600 baud.

The test program consists of a parameter set-up and a test component. The parameter set-up component requests and accepts various values to configure the software to the hardware. The test component is a single specialized test that checks the UASC in either a sense mode, priority interrupt module (PIM), or buffered interlace controller (BIC) mode. The test is designed to check the operation of certain portions of the UASC which assists in fault isolation. Depending on the operator setting of the SENSE switches, errors or malfunctions are optionally reported to the operator. Error reporting comprises error or malfunction messages, error loops, and halts.

Available documentation is as follows:

Document Number	Title
92( )0107-031	Universal Asynchronous Serial Controller Test
98A0767	Engineering Description Universal Asynchronous Serial Controller

1.2 HARDWARE REQUIREMENTS

The minimum hardware requirements are as follows:

- One V77 series computer with 4K words of memory

- One test connector wired as shown in the Engineering Description
- One UASC
- One virtual console
- One program loading device

The test connector must be connected to the UASC under test.

1.3 DESCRIPTION OF TEST COMPONENTS

The major components of the test program are illustrated in Figure 1-1.

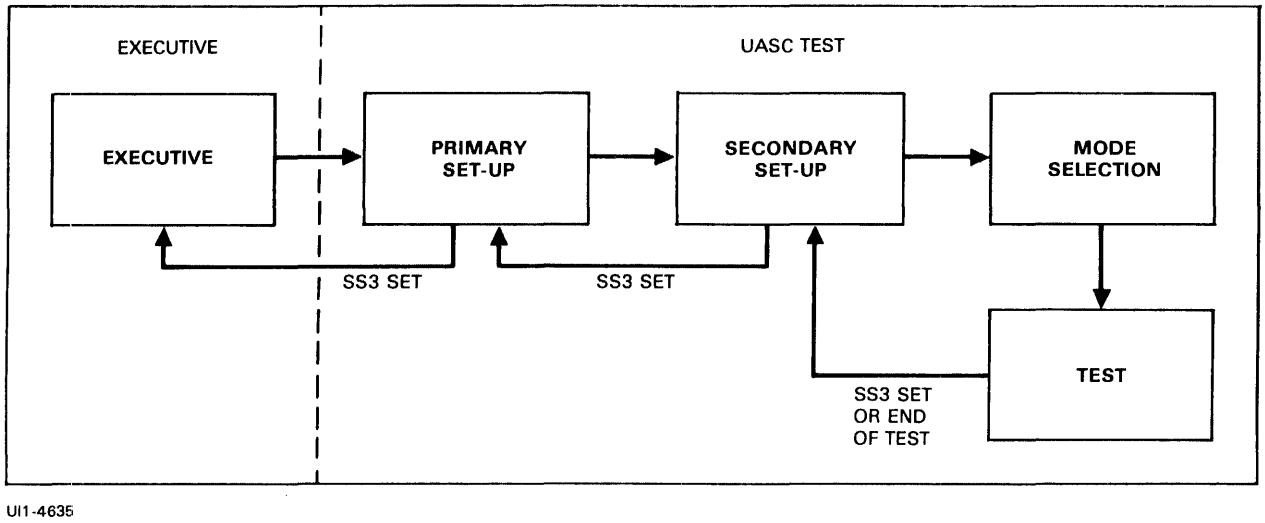

Figure 1-1. General UASC Test Block Diagram

The primary set-up allows the operator to enter the device address and data length to be used during the test. The routine is performed each time the program is started from address 500_8 or when SENSE switch 3 (SS3) is set during the secondary set-up routine.

The secondary set-up allows the operator to enter a data pattern that is to be used during the test. The set-up also allows the operator to enter the PIM address mask and interrupt address on the initial UASC test. On subsequent retests, the operator can elect to change pattern and mode entries or retain the previous information and perform the test again.

Mode selection allows the oprator to select between sense mode and BIC mode as a test environment.

In the sense mode (no PIM or BIC selected), the UASC is tested to determine if the data length is correct and to see if the sense option is functioning. The message FUNCTIONING SENSE OPTION is displayed to indicate proper functioning. A total of 512 words are generated from the selected data pattern, transmitted and received under sense mode, and compared. The test cycles continuously until SENSE switch 3 (SS3) is set by the operator. The program then displays the number of test cycles (passes) completed and returns control to the data pattern selection routine.

The PIM mode provides a test in a program interrupt mode with or without a BIC. Testing is the same as that described for the sense mode.

Testing in the BIC mode is accomplished by selecting the BIC direction. The two options are: sense mode write with BIC mode read (receive) or sense mode read with BIC mode write (transmit). The test method is the same as that described for the sense mode.

1.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the UASC test program can be loaded. Loading procedures for the executive are outlined in Part 1, paragraph 2.4.

Test program loading procedures are contained in Part 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, paragraph 1.6) are used.

Two modes of operation are available: teletypewriter and console.

Registers R9 and R12 on UASC part number 44P0677-001 must be shorted out for test purposes. Ensure that the jumpers are removed on completion of this test.

1.4.1 TELETYPEWRITER MODE

In the teletypewriter mode, the teletypewriter printer is used to display (type) the computer messages. The keyboard is used by the operator to enter responses or commands to the computer.

1.4.1.1 Primary Set-up

While the program is in the primary set-up routine, if SS3 is set, the program transfers control to the executive.

After loading of the test program is completed, the following identification message is displayed:

UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLER TEST

The message is for information only and does not require any user response.

The device address is entered after the following message is displayed:

UASC DA R.

Enter a two-digit octal number for the UASC device address. Valid entries are in the range of 02_8 through 77_8.

The number of data bits that are to be used during testing is specified after the following message is displayed:

DATA LENGTH R.

Enter a single digit number for the data word length. Valid entries are 5, 6, 7, or 8.

1.4.1.2 Secondary Set-up

The secondary set-up allows the operator to specify a test data pattern and PIM parameters. On subsequent retests, the program enters at this point.

The first message is:

PATTERN R.

Enter a single alphabetic character followed by a three-digit octal number to be used as the pattern. Valid alphabetic entries are:

Entry	Description
A	Alternating test pattern
F	Fixed test pattern
I	Incrementing test pattern
C	Continue test, use previous test data

An entry of C causes the program to initiate a retest of the UASC with no change in the parameters from the previous test. This entry is used on a second or subsequent test.

Setting SS3 prior to making a pattern selection causes the program to transfer control to the UASC DA message. After entry of a pattern, if SS3 is set, control is returned to the PATTERN message.

After a test pattern has been specified, the PIM parameters are entered. The first PIM message is:

PIM REQUIRED R.

Enter a single alphabetic character: Y for yes, N for no.

If the response to PIM REQUIRED is N, the program transfers control to the mode selection routine. In this case, the subsequent messages in this routine are not used.

When the response to PIM REQUIRED is Y, then PIM parameters are required. The PIM device address is entered after the following message is displayed:

PIM DA R.

Enter a two-digit octal number that represents the PIM device address. Valid entries are in the range of 40_8 through 43_8. Once the PIM address has been specified, this message does not reappear on subsequent retests unless a restart is made from the primary set-up.

The transmit interrupt, receive interrupt, and error interrupt addresses are then requested. The following messages are then sequentially displayed after the proper user response:

TX INT LOC R.
RX INT LOC R.
ER INT LOC R.

Enter a 1- through 6-digit octal number that represents the interrupt address.

A PIM mask is required and is specified after the folowing message is displayed:

MASK R.

Enter a 3-digit octal code that represents the test mask.

1.4.1.3 Mode Selection

The test mode is selected in this routine. If SS3 is set during this routine, control is returned to the PATTERN message. The test mode is specified after the following message is displayed:

MODE R.

Enter SE for sense mode or BI for BIC mode. If SE is selected, no further set-up is necessary and the test is initiated. The BIC mode requires that BIC parameters be entered.

The first BIC parameter is the address which is entered after the following message is displayed:

BIC DA R.

Enter a two-digit octal number that represents the BIC device address. Valid entries are in the range of 20_8 through 27_8. Once the BIC address has been specified, this message does not reappear on subsequent retests unless a restart is made from the primary set-up.

The direction in which data is transferred during the test is specified after the following message is displayed:

BIC DIRECTION R.

Enter an R for sense mode write and BIC mode read or a T for sense mode read and BIC mode write.

A quick test of the UASC is made to determine if the data length is correct and the sense option functional. The following messge is displayed:

FUNCTIONING SENSE OPTION

1.4.2 CONSOLE MODE

In the console mode of operation, the cathode ray tube (CRT) is used to display the computer messages. The keyboard is used by the operator to enter responses or commands to the computer.

The test is started at address 500_8. The program halts at certain points in the test that correspond to program requests for operator parameter entries. Program halts are displayed in the I-register and data entries are made to the A, B, and X-registers via the console. Depress RUN on the computer control panel to continue the parameter entry to the next program halt.

The program halts, registers used, and register or data entries are explained in the following list.

Halt	Register	Meaning and Data Entry
01	A	UASC device address
	B	Data length 037 = 5 bits 077 = 6 bits 0177 = 7 bits 0377 = 8 bits
02	A	Pattern 1 = Alternating 6 = Fixed 011 = Incrementing
	B	Initial pattern configuration
03	A	PIM device address 0 = No PIM required
	B	PIM mask
04		Optional halt. If PIM address entered, program halts.
	A	Transmit interrupt address
	B	Receive interrupt address
	X	Error interrupt address
05	A	Mode 0 = Mode 1 = BIC
	B	BIC device address
	X	BIC direction 0 = Receive 1 = Transmit
0704	A	Sense option status A < 0 = Functioning sense option A > 0 = Non-functioning sense option

1.4.3 TEST PROGRAM MESSAGES

Messages encountered prior to performing the test program in the teletypewriter mode are:

```
Universal Asynchronous Serial Controller Test
UASC DA
DATA LENGTH
PATTERN
PIM REQUIRED
PIM DA
XMIT INT LOC
RCVE INT LOC
ERR INT LOC
MASK
MODE
BIC DA
BIC DIRECTION
```

No messages are displayed in the console mode.

Normal termination of the test causes the number of completed test passes to be displayed:

```
nnnnnn PASSES
```

where:

n
: Is the octal number of completed tests.

1.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages, applicable test modes, and program halts are:

Program Halt	Test Mode	Message and Description
040	BIC, Sense	CONTROLLER NOT READY. A timeout has occurred while waiting for a response from the UASC.
041	BIC	BUFFER SIZE ERROR. The size of either the input or output buffer is not 512 words.
042	BIC	BIC NOT READY. A timeout has occurred while waiting for a response from the BIC.
043	BIC	BIC ABNORMAL. The BIC has reported an abnormal condition.

Program Halt	Test Mode	Message and Description
0102	BIC, Sense	ERROR aa WORD bb TX cc RX dd. The read error status aa of word bb is set. Where aa is: 1 = Input overflow error. 2 = Input parity error. 3 = Input overflow error and parity error. 4 = Frame error or break. 5 = Input overflow, error, and frame error or break. 6 = Input parity error and frame error or break. 7 = Input overflow error, input parity error, and e err r r reak. The transmitted word is cc and the received word is dd. In the console mode: register A = buffer word bb, register B = transmitted word, and register X = received word with error flags in the most significant bits.
0103	BIC, Sense	CMP ERR WORD aa TX bb RX cc dd. A compare error word at aa has occurred between the transmitted character bb and the received character cc with dd being the Exclusive OR of the two characters. In the console mode: register A = buffer word, register B = transmitted word, and register X = received word.
0700	BIC, Sense	TRANSMIT NOT READY. After initialization of the controller, the output section was not immediately ready.
0701	BIC, Sense	RECEIVE SHOULD NOT BE READY. After initialization of the controller, the input section was immediately ready.
0702	BIC, Sense	LENGTH ERROR. The length selected by the operator does not match that of the controller.
0704	BIC, Sense	FUNCTIONING SENSE OPTION. Register A < 0. The sense option is installed and functioning (no error).
0704	BIC, Sense	NON-FUNCTIONING SENSE OPTION. Register A > 0. Either the sense option is not installed or the sense option is malfunctioning.

1.6 PROGRAM EXAMPLE

The following messages are examples of typical test program messages that are displayed when various tests are performed.

```
UNIVERSAL ASYNCHRONOUS SERIAL CONTROLLER TEST

UASC DA              2.
DATA LENGTH          8
PATTERN              F377.
PIM REQUIRED         N
MODE                 SE
FUNCTIONING SENSE OPTION

000025 PASSES
PATTERN              A252.
PIM REQUIRED         Y
PIM DA               40.
TX INT LOC           100.

RX INT LOC           102.
ER INT LOC           104.
MASK                 370.
MODE                 SE
FUNCTIONING SENSE OPTION

000013 PASSES
PATTERN              10.
PIM REQUIRED         Y
MODE                 BI
BIC DA               20.
BIC DIRECTION        T
FUNCTIONING SENSE OPTION

000027 PASSES
PATTERN              C
000016 PASSES
PATTERN              FO.
PIM REQUIRED         N
MODE                 BI
BIC DIRECTION        R
FUNCTIONING SENSE OPTION

000022 PASSES

PATTERN

UASC DA
```

Section 2
Priority Memory Access Block Transfer Controller Test

2.1 GENERAL

The Priority Memory Access (PMA) Block Transfer Controller (BTC) test program tests the operational status of the priority memory access (PMA) option, the PMA bus, and the block transfer controller (BTC, F3024).

The program is designed to operate with the MAINTAIN III executive. The test uses the virtual console interface, SENSE switch routines, system constants, I/O, and timing routines contained in the executive.

The PMA BTC interfaces the V70 series computer PMA port to a peripheral controller that requires fast access, high-speed transfer of data in or out of main memory. The BTC provides memory address control when the transferred data is organized into blocks of 16-bit words.

The test program comprises a parameter set-up and a test component. The parameter set-up component requests and accepts various values to configure the software to the hardware. The test component comprises three selectable tests that check the BTC registers, the PMA read function, and the PMA write function. Depending on the operator setting of the SENSE switches, errors or malfunctions are optionally reported to the operator. Error reporting comprises error or malfunction messages, error loops, and halts.

Available documentation is as follows:

Document Number	Title
92( )0105-014	V70/620F PMA/BTC Test
98A 9908 420	Priority Memory Access Manual
98A 0783	Block Transfer Controller Engineering Description

2.2 HARDWARE REQUIREMENTS

The minimum hardware requirements are as follows:

- One V70 series computer with 8K words of memory
- One priority memory access option
- One block transfer controller
- One virtual console

2.3 DESCRIPTION OF TEST COMPONENTS

The major components of the test program are illustrated in Figure 2-1.

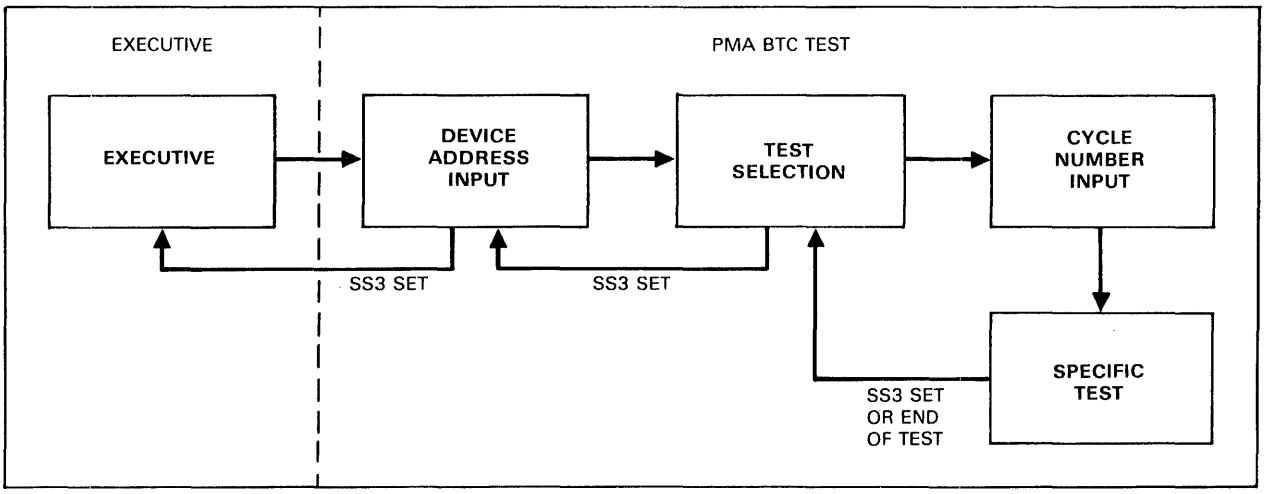

Figure 2-1. General PMA BTC Test Block Diagram

2.3.1 PARAMETER SET-UP

The parameter set-up allows the operator to enter the device address, the test to be performed, and the number of times the test is to be performed. The routine is performed each time the program is started from address 2020_8.

2.3.2 TEST SELECTION

Three tests are available for selection by the operator. They are:

- Register
- PMA read
- PMA write

2.3.2.1 Register Test

The initial and final registers are loaded with test data. The registers are read and the data verified. The test data is verified through 2^{15} bit combinations. The E-bus bit 15 is not used.

2.3.2.2 PMA Read Test

This test verifies that data can be correctly read from each memory location of a memory block that is defined by the user. The test uses the test data transfer command to read the contents of the PMA read data buffer which is loaded from the PMA bus. A test cycle read command is used to initiate the PMA cycle. The test verifies that 2^{16} bit combinations can be read from each memory location under test.

2.3.2.3 PMA Write Test

This test verifies that data can be correctly written into each memory location of a memory block taht is defined by the user. The user uses the test data transfer command to load the PMA write data buffer with the test data. A test cycle write command is used to transfer the data to memory over the PMA bus. The test verifies that 2^{16} bit combinations can be written into each memory location under test.

2.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the PMA BTC test program can be loaded. Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4.

Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, Section 1, paragraph 1.6) are used.

After loading of the test program is completed, the following identification message is displayed:

PMA/BTC TEST

The message is for information only and does not require any user response.

The device address is entered after the following message is displayed:

BTC DEVICE ADDRESS R.

Enter a two-digit octal number for the BTC device address.

The specific test to be conducted is selected after the following message is displayed:

```
TEST NUMBER R.
```

A brief description of each valid test is contained in paragraph 2.3.2. Enter the number of the test to be performed. Valid entries are:

Entry	Description
1	Register test
2	PMA read test
3	PMA write test

The PMA read and PMA write tests save the contents of the memory word currently being tested and restores those contents when the test is done. Therefore, these tests should only be terminated by setting SS3 at the end of the test cycle.

The number of test cycles to be performed is specified next. The following message is displayed:

```
CYCLE COUNT = R.
```

Enter a 0 for continuous testing or an octal number in the range of 1 through 77777.

If the PMA read or PMA write test has been selected, the program requests a starting and ending address that defines the block of memory to be tested. The addresses are entered after the following messages are displayed:

```
STARTING ADDRESS = R.
ENDING ADDRESS = R.
```

Should the specified block overlay the program, the program either modifies the entered addresses or requests a new set of addresses.

Messages that are encountered prior to performing the test program are:

```
PMA/BTC TEST
BTC DEVICE ADDRESS
TEST NUMBER
CYCLE COUNT =
STARTING ADDRESS =
ENDING ADDRESS =
```

2.5 ERROR MESSAGES

After an error has been detected, a message that briefly describes the error is displayed. The messages and the applicable tests are:

Test	Error Message
2,3	aa bb cc. Error has occurred. aa = Memory address where failure occurred bb = Pattern in memory or data buffer (was) cc = Pattern written to or read from memory
2,3	BTC ABNORMAL STOP. An abnormal stop condition was detected on the BTC at the completion of a test PMA read or write cycle.
2,3	BTC BUSY. The BTC was detected as being busy after completion of a test PMA read or write cycle.
2,3	BTC NOT BUSY. The BTC was detected as being not busy after it was activated.
2,3	END OF BLOCK. A spurious end of block condition was detected when the initial and final address registers were equal.
0	FINAL REGISTER aa bb. Final register pattern did not match test pattern. aa = Pattern that was read from final address register bb = Pattern that should have been read from final address register
0	INITIAL REGISTER aa bb. Initial register pattern did not match test pattern. aa = Pattern that was read from initial address register bb = Pattern that should have been read from final address register
2,3	NO END OF BLOCK. The end of block condition was not detected at the completion of a data transfer when the initial and final address registers were equal.

2.6 PROGRAM EXAMPLE

The following messages are examples of typical test program messages that are displayed when various tests are performed.

```
PMA/BTC TEST

BTC DEVICE ADDRESS 20.

TEST NUMBER 1.
CYCLE COUNT = 1.

TEST NUMBER 2.
CYCLE COUNT = 1.

STARTING ADDRESS = 124.
ENDING ADDRESS = 137.

TEST NUMBER 3.
CYCLE COUNT = 1.

STARTING ADDRESS = 10127.
ENDING ADDRESS = 10400.

TEST NUMBER
```

Section 3
Data Acquisition Controller Test

3.1 GENERAL

The Data Acquisition Controller (DAC) test program verifies the operational status of the DAC option (F2663-0x) and the data acquisition system.

The diagnostic is designed so that the user can:

- test the DAC through use of a test connector, or
- test the data acquisition system through use of a self-test board (STB).

The DAC interfaces SPERRY UNIVAC V70 series computers with a data acquisition and distribution system.

The V70 series computers utilize the DAC as an option. The test program assures that the diagnosis of a malfunctioning system can be accomplished in a manufacturing or field environment. The test program comprises various tests which provide a means for validating the various functions of the analog to digital and digital to analog conversion in a MAINTAIN III environment.

The test is designed to operate with the MAINTAIN III executive. The test uses the console interface, SENSE switch routines, system constants, I/O, and timing routines contained in the executive.

The diagnostic is divided into various subroutines and tests. Each subroutine is used for either:

- requesting and receiving input parameters from the user,
- performing program updates,
- testing functions, or
- generating and displaying test messages.

Parameters are entered via the operator console by the test user. Test messages are displayed in English text on the operator console.

An initialization dialog routine allows the user to enter certain hardware dependent parameters prior to testing the system. The parameters describe the system to be tested.

Input parameters are then used to modify the program to the system configuration. Parameters, to be entered by the user, are listed in the System Memo.

After generating a program identification message, the user must specify whether the DAC or STB is to be tested. The following parameters are then requested:

1. DAC device address
2. BIC device address
3. PIM parameters
   - PIM device address
   - Interrupt address
   - PIM mask

The program is then ready to execute any operator specified test.

Sequence of testing is not critical. The user can select tests as required.

Selection of tests consists of entering appropriate decimal test numbers via the operator console. Setting SENSE switch 3 (SS3) at any time during execution causes a test abort.

The SS3 routine does not allow the user to continue testing until SS3 is reset.

Test routines are divided into two routines:

- controller diagnostic (DAC)routines and
- analogic unit self test (STB) diagnostic routines.

Available documentation is as follows:

Document Number	Title
92( )0109-014	Analogic Test
UP-9057	Data Acquisition Controller Assembly Functional Analysis and Servicing Manual

3.2 HARDWARE REQUIREMENTS

The minimum hardware requirements are as follows:

- Any processor capable of executing the V75 instruction set
- 32K words of memory
- Data Acquisition Controller (DAC, F2964-10)
- DAC test connector
- Analogic 5400 series unit
- Analogic STB (Analogic AC3000)
- Operator console
- Program input device

3.3 DESCRIPTION OF TEST COMPONENTS

This section contains a brief discription of the tests that make up the diagnostic.

3.3.1 CONTROLLER DIAGNOSTIC

The controller diagnostic utilizes the following tests:

Test Number	Description
0	Return to MAINTAIN III executive
1	Data transfer without BIC
2	DMA trap out
3	DMA trap in
4	Analogic clear test
5	Controller device address selection
6	Controller data path validation

These tests are made with the assumption that the following hardware is functioning properly:

- Processor
- Memory

- Operator console
- Program input device

After a test has been selected, a test identification (ID) message is displayed. The message is in the general format:

```
TEST X TEST DESCRIPTION
```

where:

X
: Is the test number selected.

Following the ID message, the following message is displayed:

```
ENTER CYCLE COUNT = R.
```

Enter an octal number (cycle count) that specifies the number of times that the selected test is to be performed. After the test has successfully completed the specified number of cycles, the following messages are displayed:

```
TEST COMPLETE CYCLES = XXXX

ENTER TEST NUMBER = R.
```

where:

XXXX
: Is the number of time the test was performed before terminating.

The user can then repeat the test or select another test.

A cycle count is used to specify the number of times the test is to be performed. The count is entered when the following message is displayed:

```
ENTER CYCLE COUNT = R.
```

After the test has completed the specified number of cycles, the following messages are displayed:

```
TEST COMPLETE CYCLES = XXXX

ENTER TEST NUMBER = R.
```

The cycle count format is:

Format	Description
XXXX,	Print the cumulative number of cycles performed at the end of each test cycle. Print CYCLE = YYYY after each test cycle until YYYY = XXXX. Terminate testing with the message: TEST COMPLETE CYCLES = XXXX.
XXXX.	Suppress CYCLE = XXXX message at the end of each test cycle. Terminate test after XXXX cycles with the message: TEST COMPLETE CYCLES = XXXX.
0,	Continuous testing until SS3 set. Print the cumulative number of cycles performed at the end of each test cycle.
0.	Continuous testing until SS3 set. Suppress cycle count message at the end of each test cycle. Print cycle count when test terminated.

3.3.1.1 Test 0. Return To MAINTAIN III Executive

This test transfers program control to the MAINTAIN III executive. The executive allows the user several options in which the program can be modified for customized testing. Refer to UP-8672. Otherwise, the user can return to the Analogic System Diagnostic program by entering G500.

There are no user or error messages associated with this test.

3.3.1.2 Test 1. Data Transfer Without BIC

This test performs three data pattern tests and verifies that the data transfer without BIC is functioning properly.

The first data pattern test is a zero fill test. During this test, an all ones pattern is sent to the controller. The pattern is read back and compared. The next pass right-shifts a zero into the pattern. The pattern is sent to the controller, read back, and compared. This process continues until all bits are zero.

The second data pattern test is a ones fill test. During this test, an all zero pattern is sent to the controller. Test processing is the same as the zero fill test except that each pass left-shifts a one into the pattern until all bits are one.

The third data pattern test is an alternating ones and zero pattern. During this test, the alternating pattern is sent to the controller. Test processing is the same as the two previous tests. Each pass shifts the pattern one bit until sixteen passes are completed.

User messages are:

TEST #1 DATA TRANSFER TEST W/O BIC

ENTER CYCLE COUNT = R.

The user enters an octal number (cycle count) that specifies the number of times that this test is to be performed.

If a data transfer error is detected, the following message is displayed:

DATA TRANSFER ERROR IS XXXX S/B YYYY

where:

XXXX
Is the erroneous data.

YYYY
Is the correct data.

3.3.1.3 Test 2. DMA Trap-Out

This test verifies that the BIC trap-out capabilities of the DAC are functioning properly.

A block of memory is allocated for data transfer. The beginning and ending addresses are loaded into the BIC initial and final registers. A known data pattern is stored at the end of the memory block. The BIC is activated. After a BIC COMPLETE signal is detected (either by sense or interrupt), the data pattern is compared. The pattern stored in the controller input buffer should be the same as the known data pattern in memory.

The controller ABS latch is tested by aborting the DMA transfer (disconnect the controller test connector). The program will then generate a controller ABS latch reset command and then sense for the ABS latch to reset.

If a PIM is used, then a BIC COMPLETE interrupt must be received.

If a 0. has been entered for the BIC device address, the following messages are displayed:

NO BIC DETECTED

ENTER TEST NUMBER = R.

User messages are:

BIC TRANSFER TRAP OUT

ENTER CYCLE COUNT = R.

The user enters an octal number (cycle count) that specifies the number of times that this test is to be performed.

To test the ABS latch, enter a period (.) for cycle count and then disconnect the test connector. If the latch is operating properly, the following messages are displayed:

DATA TRANSFER ERROR IS XXXX S/B YYYY
BIC ABNORMAL STOP
CONTROLLER ABNORMAL STOP
BIC ABNORMAL STOP

This series of messages is repeated until the test connector is re-installed. Any other message sequence constitutes an error.

If a data transfer error is detected, the following message is displayed:

DATA TRANSFER ERROR IS XXXX S/B YYYY

where:

XXXX
Is the erroneous data.

YYYY
Is the correct data.

3.3.1.4 Test 3. DMA Trap-In

This test verifies that the BIC trap-in capabilities of the DAC are functioning properly.

A block of memory is allocated for data transfer. The beginning and ending addresses are loaded into the BIC initial and final registers. A known data pattern is stored in the controller input buffer. The BIC is activated. After a BIC COMPLETE signal is detected (either by sense or interrupt), the data pattern is compared. The pattern stored in the block of memory should be the same as the known data pattern in the controller input buffer.

If a PIM is used, then a BIC COMPLETE interrupt must be received.

If a 0. has been entered for the BIC device address, the following messages are displayed:

NO BIC DETECTED

ENTER TEST NUMBER = R.

User messages are:

BIC TRANSFER TRAP IN

ENTER CYCLE COUNT = R.

The user enters an octal number (cycle count) that specifies the number of times that this test is to be performed.

If a data transfer error is detected, the following message is displayed:

DATA TRANSFER ERROR IS XXXX S/B YYYY

where:

XXXX
Is the erroneous data.

YYYY
Is the correct data.

3.3.1.5 Test 4. Analogic Clear Test

This test verifies that an octal 170000 is placed on the data output lines when an analogic clear command is issued.

A 170000 code performs a system reset on the analogic chassis. The controller has the capability to issue this code when commanded by an EXC command.

This test issues an analogic clear command to the controller. The controller input register is then checked for a 17000 code.

User messages are:

ANALOGIC CLEAR INSTRUCTION TEST

ENTER CYCLE COUNT = R.

The user enters an octal number (cycle count) that specifies the number of times that this test is to be performed.

The program then generates an initialize-analogic-master-chassis command (EXC1). If SS1 is reset, the following message is displayed:

ANALOGIC CLEAR CODE = 170000

Any code other than 170000 constitutes an error.

3.3.1.6 Test 5. Controller Device Address Selection

This test verifies that the controller address selection switches are functioning properly.

A controller device address is specified. A test is selected to validate that the new address has been accepted.

User messages are:

INPUT CONTROLLER DEVICE ADDRESS (50-57).

Enter an octal number from 50 through 57. Terminate the entry with a period. Any octal number outside this range constitutes an error and the user is prompted again for the controller device address.

To validate the new address, a test must be performed. The following message is displayed:

ENTER TEST NUMBER = R.

Enter the test number (1 through 4) of one of the previously defined tests. Results of the selected test are described in the applicable test description.

3.3.1.7 Test 6. Controller Data Path Validation

This test allows the user to troubleshoot the controller data path.

An octal data pattern is entered. The program will continuously output and input the specified data pattern until SS3 is set. If there is a data path error, the user can trace the pattern through the data path. The defective component can then be isolated.

User messages are:

CONTROLLER DATA PATH VALIDATION

INPUT OCTAL NUMBER FOR DATA PATTERN = R.

Enter an octal data pattern.

When SS3 is set, the following message is displayed:

RESET SENSE SWITCH THREE (3)

Reset SS3 to continue testing.

3.3.2 SELF-TEST BOARD DIAGNOSTIC TESTS

The self-test board (STB) tests use the Analogic Self-Test Board to test the analogic unit.

The available tests are:

Test Number	Test
0.	Return to MAINTAIN III Executive
1.	Digital Bus Read/Write
2.	Sample and Hold
3.	A/D Offset
4.	A/D Range
5.	Power Supply Voltages
6.	Peak-to-Peak Noise
7.	Slew Error
8.	Common Mode Rejection Ratio
9.	Signal Processor Gains
10.	Missing Codes
11.	A/D Linearity
12.	Code Centers
13.	Pass/Fail Lights
14.	External Digital Output
15.	External Digital Input
16.	External Analog Inputs
17.	Re-enter Analogic Parameters

3.3.2.1 Test 0. Return To MAINTAIN III Executive

This test transfers program control to the MAINTAIN III executive. The executive allows the user several options in which the program can be modified for customized testing. Refer to UP-8672. Otherwise, the user can return to this diagnostic program by entering G500.

There are no user or error messages.

3.3.2.2 Test 1. Digital Bus Read/Write

This test verifies that the digital bus is functioning properly.

During this test, the STB is used as both an output card and as an input card. Data is transmitted (write) to the card and then received (read) from the card. To prevent a test on a missing card, due to capacitive storage of data on the data bus, the STB performs a shift and loop on the data it receives. Thus, the data read back from the STB is the same as that data written to the card, shifted one bit to the left. All 65K bit combinations are checked. All errors are accumulated and listed.

The test identification message is:

TEST 1 DIGITAL BUS READ/WRITE TEST

After the test is completed, the following messages are displayed:

XXXX ERRORS

ENTER TEST NUMBER = R.

where:

XXXX
Is the number of errors encountered.

The user can then repeat the test or select another test.

3.3.2.3 Test 2. Sample And Hold

This test verifies that sample and hold cards are functioning properly.

During this test, the data acquisition system is sent a series of digital output commands (4000, 4001, 4002, and 4003). These commands create defined responses in simultaneous sample and hold cards. The STB contains the same logic circuitry that is on a sample and hold card. After each command is generated, the STB is interrogated and checked. A message is displayed to indicate the result of each command.

User messages are:

TEST 2 SAMPLE & HOLD TEST

PART 1: ODD-SAMPLE, EVEN-SAMPLE

PASS!!!

PART 2: ODD-HOLD, EVEN-SAMPLE

PASS!!!

PART 3: ODD-SAMPLE, EVEN HOLD

PASS!!!

PART 4: OFF-HOLD, EVEN HOLD

PASS!!!

Errors are indicated by the following messages:

PART 1: ODD-SAMPLE, EVEN-SAMPLE

ERROR! ODD HOLD

ERROR! EVEN HOLD

PART 2: ODD-HOLD, EVEN-SAMPLE

ERROR! ODD SAMPLE

ERROR! EVEN HOLD

PART 3: ODD-SAMPLE, EVEN-HOLD

ERROR! ODD HOLD

ERROR! EVEN SAMPLE

PART 4: ODD-HOLD, EVEN-HOLD

ERROR! ODD SAMPLE

ERROR! EVEN SAMPLE

3.3.2.4 Test 3. Analog/Digital Offset

This test measures the offset in the analog to digital converter. During this test, the STB is programmer to short the off and even analog buses together. Shorting is accomplished via field effect transistor (FET) switches. A differential measurement is then made by using the signal processor and the A/D converter. The resulting data is converted into an equivalent voltage based on the type of converter being used. A message is displayed to indicate the results.

User messages are:

TEST 3 A/D OFFSET
MEASUREMENT OF OFFSET IN A/D SYSTEM WITH SHORTED INPUTS = XXXX

where:

XXXX
Is the measured offset.

If a measurement results in the lowest possible code from the converter, the following message is displayed:

OFF SCALE LOW

3.3.2.5 Test 4. Analog/Digital Range

This test is used to measure the analog to digital converter range accuracy.

System offsets are automatically removed before the range test is performed. A precise reference voltage on the STB is measured by the converter. The measured voltage is always 90% of full scale for the converter used in the system. The results of the measurement are then displayed.

The voltage measured in this test is quantized by the converter. Movement is in one LSB increments as the range is adjusted. The adjustment process attempts to reach that quantized voltage that is closest to 90% of full scale.

During the measurement process, certain corrections are performed by the software. These corrections remove amplifier offset errors on the STB and signal processor. Errors are normally caused by component aging and temperature drift. The offset measurements are subtracted from the range reading before the result is displayed.

Offset measurements take place near zero volts. It is possible that systems with unipolar converters will yield offset readings of OFF SCALE LOW during this portion of the test. If this happens, the software utilizes several techniques, including polarity reversal, to make meaningful offset measurements.

The user message is:

TEST 4 MEASUREMENT OF A/D CONVERTER RANGE ACCURACY = XXXX VOLTS

where:

XXXX
Is the accuracy.

If all measurement techniques fail to produce meaningful results, the following message is displayed:

OFFSCALE LOW

Normally, a retest will result in a successful measurement. If not, the offset can be adjusted in a positive direction during the A/D offset test before running the range test. The range results are not adversely affected by the artifically induced offset.

3.3.2.6 Test 5. Power Supply Voltages

This test measures the three voltages (+5Vdc, +15Vdc, and -15Vdc) supplied to the STB.

In this test, the STB uses the three power supply voltages to produce three voltages that are 90% of full scale. The voltages are used by the A/D converter. When read by the software, these voltages values are rescaled to represent the power supply levels.

This test is affected by the quantizing levels of the converter. However, the levels are scales and do not directly correspond to an LSB value.

Power supplies shall be set to within ±5% of nominal voltage.

The +5 Vdc is produced by a switching power supply and has approximately 70 mv of ripple. Successive repetitions of this test will show small variations in the +5 Vdc value.

This test will run successfully on unipolar systems. The STB inverts the polarity of the -15 Vdc signal for measurement by unipolar converters.

User messages are:

TEST 5 POWER SUPPLIES

+5 VOLT POWER SUPPLY = X.XXX

+15 VOLT POWER SUPPLY = XX.XXX

-15 VOLT POWER SUPPLY = XX.XXX

where:

XX.XXX
Is the power supply voltage.

3.3.2.7 Test 6. Peak-To-Peak Noise

This test measures the peak-to-peak noise level of the system.

During this test, the STB produces a stable voltage that is 1/16 of full scale. The software makes 1000 measurements of this value. The difference, with respect to the A/D input, between the highest and lowest measured values, divided by two, is displayed. The number of measurements are taken over a time frame that includes a 60 Hz line frequency cycle. Thus, AC power coupling is included as a noise source.

In programmable gain systems, the software allows the user to choose gain codes of 1 through 13. Otherwise, a default value of 10 is used.

The measured noise is always referenced to the A/D input.

Noise can be measured at signal processor gains greater than unity. The equivalent system input noise is found by dividing the printed result by the signal processor gain.

User messages are:

```
TEST 6 PEAK-TO-PEAK NOISE TEST

ENTER GAIN CODE (10-13)
```

The gain code is requested on programmable gain systems only. Enter a code of 10, 11, 12, or 13.

At the end of the test, the following message is displayed:

```
PEAK-PEAK NOISE GAIN CODE XX = +/- X.XXX V
     (REF. TO A/D INPUT)
```

3.3.2.8 Test 7. Slew Error

This test checks the ability of the system to accurately follow a fast-moving waveform.

Two checks are performed: one for a positive step input and one for a negative step input. For a bipolar converter, the two voltage levels are located at +90% of full scale (high ref) and -90% of full scale (minus ref). In a unipolar converter, the two levels are set at +90% of full scale (high ref) and 1/16 of full scale (low ref).

In each case the process is identical. The software addresses the channel to be measured, waits a long time (approximately 50 msec), measures and saves the result. The program then addresses the channel to be slewed from and waits a long time. Finally, the original channel is readdressed and measured within the settling time constraints of the system (normally 5 usec). This value is compared to the previosuly saved value. The number of difference counts is then displayed.

Essentially, the test compares a reading obtained after a long settling time with a reading obtained after the minimum settling time. The minimum settling time varies from 5 to 20 usec. It is determined by the adjustable delay built into the signal processor. In special systems, the adjustable delay can be greater.

The count is directly equivalent to the number of LSBs of error. The polarity of the count is an indication of undershoot or overshoot.

An equivalent voltage error is obtained by multiplying the number of error counts by the voltage value of an LSB in the system under test.

User messages for a bipolar converters:

TEST 7 SLEW RATE TEST

RESULT OF SLEW FROM MINUS REF TO HIGH REF = XXXX COUNTS

RESULT OF SLEW FROM HIGH REF TO MINUS REF = XXXX COUNTS

where:

XXXX
: Is the number of counts.

User messages for a unipolar converter:

TEST 7 SLEW RATE TEST

RESULT OF SLEW FROM LOW REF TO HIGH REF = XXXX COUNTS

RESULT OF SLEW FROM HIGH REF TO LOW REF = XXXX COUNTS

where:

XXXX
Is the number of counts.

3.3.2.9 Test 8. Common Mode Rejection Ratio

This test simulates a common-mode voltage applied to shorted inputs.

During this test, the two analog bus lines (even bus and odd bus) are connected together under program control. The two lines are connected to +90% of full scale and then to -90% of full scale. Connection of the lines simulates a common-mode voltage applied to shorted inputs. The resulting differential readings are translated into voltages.

User messages are:

TEST 8 COMMON MODE REJECTION

CMV = +90% OF FULL SCALE, A/D READING = X.XXX VOLTS

CMV = -90% OF FULL SCALE, A/D READING = X.XXX VOLTS

where:

X.XXX
Is the voltage.

To calculate the common-mode rejection ration, use the formula:

CMRR=20 LOG(10) ((+90% RDNG)-(-90% RDNG))/(2(90% OF FULL SCALE))

An error can result in the following messages:

CMV = +90% OF FULL SCALE, A/D READING = OFF SCALE LOW

CMV = -90% OF FULL SCALE, A/D READING = OFF SCALE LOW

3.3.2.10 Test 9. Signal Processor Gains

This test checks the four differential programmable gain codes for offset and gain accuracy.

During this test, gain codes 10, 11, 12, and 13 are successively applied. If the system does not have a programmable gain capability, a gain code of 10 is used. A fixed reference voltage of 1/16 full scale is used on all gain codes.

All voltages are given in reference to the A/D converter input. Thus, signal processor gains are equal to the converter reading divided by the input voltage.

User messages for programmable gain systems are:

```
TEST 9 MEASUREMENT OF SIGNAL PROCESSOR GAINS

OFFSET WITH GAIN CODE 10 = X.XXXXXXX VOLTS
  (REFERENCED TO A/D INPUT)
OFFSET WITH GAIN CODE 11 = X.XXXXXXX VOLTS
  (REFERENCED TO A/D INPUT)
OFFSET WITH GAIN CODE 12 = X.XXXXXXX VOLTS
  (REFERENCED TO A/D INPUT)
OFFSET WITH GAIN CODE 13 = X.XXXXXXX VOLTS
  (REFERENCED TO A/D INPUT)
INPUT VOLTAGE = 0.6250000 VDC
MEASUREMENT WITH GAIN CODE 10 = X.XXXXXXX V
  (REFERENCED TO A/D INPUT)
MEASUREMENT WITH GAIN CODE 11 = X.XXXXXXX V
  (REFERENCED TO A/D INPUT)
MEASUREMENT WITH GAIN CODE 12 = X.XXXXXXX V
  (REFERENCED TO A/D INPUT)
MEASUREMENT WITH GAIN CODE 13 = X.XXXXXXX V
  (REFERENCED TO A/D INPUT)
```

where:

X.XXXX
: Is the voltage.

User messages for nonprogrammable gain systems are:

```
OFFSET WITH GAIN CODE 10 = X.XXXXXXX VOLTS
     (REFERENCED TO A/D INPUT)
INPUT VOLTAGE = 0.6250000 VDC
MEASUREMENT WITH GAIN CODE 10 = X.XXXXXXX V
     (REFERENCED TO A/D INPUT)
```

Errors will cause the following message:

```
OFF SCALE LOW
```

to be displayed.

Unipolar systems can display OFF SCALE LOW messages because:

- The offset readings are near zero.
- Automatic offset correction is used to remove STB offsets during the gain portion of this test.

If this occurs, an artifically induced offset can be adjusted into the signal processor by using test 3 before executing this test. The induced offset will show up in the offset portion of this test but will not adversely affect the gain readings.

3.3.2.11 Test 10. Missing Codes

This test validates that the integrator on the STB is functioning properly.

This is a fully automated test. The integrator, whose direction and speed is under software control, is used to cover the entire input voltage range of the system. At the same time, a search for each possible bit combination is made at the output of the A/D converter.

User messages are:

TEST 10 MISSING CODES TEST

XXXX CODES FOUND

XXXX CODES MISSING

where:

XXXX
Is the number of codes.

The maximum possible number of codes is 2^n, where n is the number of A/D converter bits.

Some high resolution converters (14, 15, and 16 bits) can have missing codes and still meet differential linearity specifications. In this case, the data sheet for the A/D converter, must be checked.

3.3.2.12 Test 11. Analog/Digital Linearity

This test validates that the A/D converter is functioning properly.

This test is a check of converter characteristics such as differential linearity, wide codes, narrow codes, and missing codes. Any binary converter can be tested, regardless of coding, voltage range, or number of bits.

During the test, a linear, slow-moving ramp is applied to the system input. Range is from minus full scale to plus full scale. Ramp speed is so slow that movement is less than one LSB during an A/D conversion. While the ramp is moving up, continous A/D conversions are made at a constant rate. Each time

that a code is found, a related counter in memory is incremented. Data is stored in 4K of memory. When the test is complete, a software analysis is performed on the data. A summary of the results is then displayed. Such a result is referred to as a histogram.

By analyzing the results, the user can determine the degree of code width variation over the entire range of conversion. Resolution is at least 1/60 of an LSB for a 12-bit converter.

User messages are:

```
TEST 11 A/D LINEARITY TEST

# TIMES        # CODES
 FOUND

 XXXX          XXXX      WIDEST CODE
 XXXX          XXXX
  -             -
  -             -
  -             -
 XXXX          XXXX
 XXXX          XXXX      NARROWEST CODE
 XXXX          XXXX      MISSING CODE
               ----
               XXXX      TOTAL NUMBER OF CODES

RECAP OF RESULTS:

# TIMES        # CODES
 FOUND

 XXX             X      WIDEST CODE
 XXX             X      NARROWEST CODE
 XXX            XXX     HIGHEST # OF CODES
```

where:

XXXX
Is the decimal number for each category.

3.3.2.13 Test 12. Code Centers

This test is used to produce a voltage that corresponds to the center of a requested code.

In this test, the user requests any octal code that the A/D converter is capable of producing. Software manipulates the integrator on the STB. A voltage that corresponds to the center of the requested code is produced. The voltage can be displayed on a digital voltmeter (DVM). A comparison to an ideal voltage can then be made.

The DVM is connected between pin N (analog ground) and pin M (integrator output) at the rear of the STB.

This test creates an active feedback loop. Changes in the offset and range controls can be made while the program is running. Results are continuously displayed on the DVM.

Setting SS3 terminates this test.

User messages are:

```
TEST 12 CODE CENTER TEST

ENTER OCTAL VALUE FOR CODE CENTER XXXX

DESIRED VOLTAGE = YYYY VOLTS
```

where:

XXXX
: Is the code center six digit octal number, left justified and terminated with a period.

YYYY
: Is resultant voltage.

The user cannot specify the absolute bottom or top converter codes. These entries will result in the following messages:

```
ERROR!  ENTERED VALUE EQUALS MINIMUM LIMIT

  RE-ENTER CODE CENTER VALUE

ERROR!  ENTERED VALUE EQUAL MAXIMUM LIMIT

  RE-ENTER CODE CENTER VALUE
```

If the specified code center is too large, the following message is displayed:

```
ERROR!  ENTERED VALUE TOO LARGE

  RE-ENTER CODE CENTER VALUE
```

3.3.2.14 Test 13. Pass/Fail Lights

This test verifies that green and red lights mounted at the rear of the STB are functioning properly.

This is a visual test of the lights. Each light is tested. The cycle of testing is:

1. Green light on.
2. Red light on.
3. Both lights on.
4. Both lights off.

Each step is approximately five seconds long. The test is automatic and requires no operator intervention.

User messages are:

```
TEST 13 PASS/FAIL LIGHTS

     THE GREEN/RED LEDS ON THE SELF TEST BOARD

     WILL CYCLE ON/OFF IN THE FOLLOWING SEQUENCE:

                    GREEN ON

                    RED ON

                    GREEN & RED ON

                    GREEN & RED OFF

     EACH PHASE IS APPROXIMATELY 5 SECONDS LONG.
```

3.3.2.15 Test 14. External Digit Output Test

This test allows the user to program the state of the eight external digital outputs on the STB. The output lines can then be checked through the use of a logic probe, oscilloscope, or DVM.

User messages are:

TEST 14 EXTERNAL DIGITAL OUTPUT TEST

D0 = X
D1 = X
D2 = X
D3 = X
D4 = X
D5 = X
D6 = X
D7 = X

CODE TRANSMITTED

where:

X
Is a user entry of either 0 or 1.

The relationship of program input to digital output pins is:

Program Input	STB Pin	Mnemonic	Program Input	STB Pin	Mnemonic
D0	14	DY0	D4	18	DY4
D1	15	DY1	D5	19	DY5
D2	16	DY2	D6	20	DY6
D3	17	DY3	D7	21	DY7

3.3.2.16 Test 15. External Digital Input

This test allows the user to read the state of the eight external digital inputs on the STB. The state of each input is listed as either a 0 or 1. If no signal is connected to the input, a 1 is displayed.

User messages are:

TEST 15 EXTERNAL DIGITAL INPUT TEST

D0 = X
D1 = X
D2 = X
D3 = X
D4 = X
D5 = X
D6 = X
D7 = X

where:

X
: Is either 0 or 1.

The relationship of program display to digital input pins is:

Program Input	STB Pin	Mnemonic	Program Input	STB Pin	Mnemonic
D0	R	DX0	D4	V	DX4
D1	S	DX1	D5	W	DX5
D2	T	DX2	D6	X	DX6
D3	U	DX3	D7	Y	DX7

3.3.2.17 Test 16. External Analog Inputs

This test verifies that the A/D converter and signal processor are reading the analog input channels on the STB.

In this test, the A/D converter and signal processor are used to read the eight external differential analog input channels. On gain programmable systems, the user can request a gain code of 10 through 13. The A/D value is checked to see if it is at minimum or maximum and if so, a message is generated to reflect the condition. Otherwise, the voltage is displayed.

User messages are:

```
TEST 16 EXTERNAL ANALOG INPUTS

ENTER GAIN CODE YY
```

where:

YY
: Is the user entered gain code (10 through 13) programmable gain systems.

After the gain code is entered, the following messages are displayed:

```
CH 0  = X.XXXXXXX V (REFERENCED TO A/D INPUT)
CH 2  = X.XXXXXXX V (REFERENCED TO A/D INPUT)
CH 4  = X.XXXXXXX V (REFERENCED TO A/D INPUT)
CH 6  = X.XXXXXXX V (REFERENCED TO A/D INPUT)
CH 10 = X.XXXXXXX V (REFERENCED TO A/D INPUT)
CH 12 = X.XXXXXXX V (REFERENCED TO A/D INPUT)
CH 14 = X.XXXXXXX V (REFERENCED TO A/D INPUT)
CH 16 = X.XXXXXXX V (REFERENCED TO A/D INPUT)
```

where:

CH
: Is the abbreviation for channel.

X.XXX
: Is the A/D code to voltage conversion.

In the message, CH 0 corresponds to CH 0 on the STB. This is denoted by signal AN 0 on pin C (HI side) and AI 0 on pin 3 (LO side).

Two possible error messages are:

CH X = OFF SCALE LOW

CH X = OFF SCALE HIGH

where:

X
: Is the channel that is in error.

3.3.2.18 Test 17. Re-Enter Analog Parameters

This test verifies that analog system parameters can be changed.

During this test, parameters that are used to initialize the system are re-entered.

User messages are:

INPUT ANALOGIC BOX # (1-8) = X

INPUT CARD SLOT # (1-16) = X

INPUT A/D TYPE (A-J) = X

PROGRAMMABLE GAIN (Y/N) = X

where:

X
: Is the appropriate user entry.

Any entry outside the specified range in parenthesis constitutes an error. The user is prompted again for the entry.

After all entries are made, the following message is displayed:

ENTER TEST NUMBER = R.

Enter any of the previously described tests to validate that the new entries are functioning properly.

3.4 OPERATING PROCEDURES

The MAINTAIN III executive must be loaded and operational before the DAC test program can be loaded. Loading procedures for the executive are outlined in Part 1, Section 2, paragraph 2.4.

Test program loading procedures are contained in Part 1, Section 1, paragraph 1.5. When loading of the test program is complete, a program identification message is displayed and automatic transfer to the start of the program takes place.

Standard SENSE switch settings (Part 1, Section 1, paragraph 1.6) are used.

3.4.1 PROGRAM LOADING

For paper tape systems, the procedure for loading the test program is as follows:

1. Place the test program tape in the paper tape reader.
2. Position the tape within the leader area between the test part number and the start of the program.
3. Enter an L. on the virtual console.

Magnetic tape systems require the use of file numbers. The procedure for loading the test program is as follows:

1. Consult the MAINTAIN III Software Release Description for the file number of the test program to be used.
2. Position the tape reel on transport.
3. Position the tape to the required test program file number by using MAINTAIN III tape commands (Part 1, Section 2, paragraph 2.4.2.1).
4. Load the test program by using magnetic tape commands.

3.4.2 EXECUTION

Device addresses are system dependent. In order to enter the correct addresses, reference must be made to the System memo.

The setting of the computer operator panel SENSE switches determines the execution modes of the diagnostic program. Switch settings can alter program operation as follows:

SENSE Switch	Set Position	Reset Position
1	Suppress error printout. If no TTY, suppress error halt.	Print error messages. If no TTY, halt.
2*	Halt on error. (Continue testing.)	Do not halt on error. (Loop on error.)
3	Terminate test and return to start of test.	Continue testing.

* Following an error halt, SENSE switch 2 can be used to continue the test or to loop on the error:

  - To continue testing, leave the SENSE switch set and depress R on the virtual console.

  - To loop on an error, reset the SENSE switch and depress R on the virtual console. Looping continues until the switch is set, the program then continues in the "halt on error" mode until the next error halt. If the error condition clears, looping continues until SENSE switch is set.

3.4.3 PROGRAM IDENTIFICATION

When the diagnostic program is loaded, execution begins. The following message is displayed:

ANALOGIC DIAGNOSTIC TEST PROGRAM 92( )0109-014B

The message serves to identify the diagnostic program and requires no response from the user.

3.4.4 DIAGNOSTIC SELECTION

Selection of a diagnostic routine is made when the following two messages are displayed:

```
INPUT C FOR CONTROLLER TEST

INPUT S FOR SELF TEST BOARD

R
```

Enter a C if the DAC is to be tested or S if the STB is to be tested.

If the response is C, the subtests are described in Section 3.4.4.

If the response is S, the subtests are described in Section 3.4.5.

3.4.5 DATA ACQUISITION CONTROLLER TESTS

After the user enters C, the following message is displayed:

```
INPUT CONTROLLER DEVICE ADDRESS (50-57). R.
```

Enter an octal number from 50 through 57. Terminate the entry with a period. Any octal number outside this range constitutes an error and the user is prompted again for the controller device address.

The BIC device address is requested when the following message is displayed:

```
INPUT BIC DEVICE EVEN ADDRESS (20-26). R.
```

Enter an even octal number from 20 through 26. Terminate the entry with a period. If no BIC is to be used, enter a 0. Any octal number outside the specified range constitutes an error. An error causes the request for a BIC device address to be repeated.

After successful entry of the BIC device address, the PIM parameters are requested when the following message is displayed:

```
INPUT PIM PARAMETERS

PIM DA, INTERRUPT CELL, MASK. R, R, R.
```

Enter the required parameters separated by a comma and terminated with a period. Enter an octal number between 40 and 47 for the PIM DA. If no PIM is used, enter a 0. The INTERRUPT CELL is an octal number between 100 and 236. The MASK is a number between 0 and 377. Enter a MASK number, taken from the following list, that corresponds to the INTERRUPT CELL.

INTERRUPT CELL	MASK Number	INTERRUPT CELL	MASK Number
100	376	120	376
102	375	122	375
104	373	124	373
106	367	126	367
110	357	130	357
112	337	132	337
114	277	134	277
116	177	136	177

Any input parameter that is outside the specified range constitutes an error. An error causes the request for PIM parameters to be repeated.

After the system parameters are entered, the software checks for the presence of a test connector. If the test connector is not installed, the following message is displayed:

CONNECT TEST SHOE

The program loops until the test connector is installed.

When the test connector is connected, the following message is displayed:

ENTER TEST NUMBER = R.

Enter a test number (0 through 6) terminated with a period. The available tests are:

Test Number	Description
0	Return to MAINTAIN III executive
1	Data transfer without BIC
2	DMA trap-out
3	DMA trap-in
4	Analogic clear test
5	Controller device address selection
6	Controller data path validation

3.4.5.1 Test 0. Return to MAINTAIN III Executive

By entering a 0, the user transfers program control to the MAINTAIN III executive.

3.4.5.2 Test 1. Data Transfer Without BIC

When a 1. is entered, the following message is displayed:

TEST #1 DATA TRANSFER TEST W/O BIC

ENTER CYCLE COUNT = R.

Enter the cycle count.

3.4.5.3 Test 2. DMA Trap-out

When a 2. is entered, the following messages are displayed:

BIC TRANSFER TRAP OUT

ENTER CYCLE COUNT = R.

Enter the cycle count.

3.4.5.4 Test 3. DMA Trap-in

When a 3. is entered, the following messages are displayed:

BIC TRANSFER TRAP IN

ENTER CYCLE COUNT = R.

Enter the cycle.

If the user has entered a 0. for the BIC device address and this test is selected, the following messages are displayed:

NO BIC DETECTED

ENTER TEST NUMBER = R.

3.4.5.5 Test 4. Analogic Clear Test

When a 4. is entered, the following messages are displayed:

ANALOGIC CLEAR INSTRUCTION TEST

ENTER CYCLE COUNT = R.

Enter the cycle count.

The following message is then displayed:

ANALOGIC CLEAR CODE = 170000

Any other code constitutes an error.

3.4.5.6 Test 5. Controller Device Address Selection

When a 5. is entered, the following message is displayed:

INPUT CONTROLLER DEVICE ADDRESS (50-57). R.

Enter an octal number from 50 through 57 terminated with a period. Any octal number outside this range constitutes an error and the user is prompted again for the controller device address.

When the new device address is accepted, the following message is displayed:

ENTER TEST NUMBER = R.

Enter any of the previous tests (1 through 4). Successful completion of the selected test validates that the controller address selection switches are performing properly.

3.4.5.7 Test 6. Controller Data Path Validation

When a 6. is entered, the following messages are displayed:

CONTROLLER DATA PATH VALIDATION

INPUT OCTAL NUMBER FOR DATA PATTERN = R.

Enter an octal data pattern. The program will loop continuously until terminated by setting SS3. This allows the user to follow the known data pattern along the data path until a defective component is located.

3.4.6 SELF-TEST BOARD TESTS

The self-test board (STB) tests use the Analogic Self-Test Board to test the analogic unit.

After the user enters S, analogic system parameters are entered before a test is selected.

The following message is displayed:

INPUT CONTROLLER DEVICE ADDRESS (50-57). R.

Enter an octal number from 50 through 57. Terminate the entry with a period. Any octal number outside this range constitutes an error and the user is prompted again for the controller device address.

If the analogic unit is not in remote, the following message is displayed:

PUT ANALOGIC CHASSIS INTO REMOTE

The input analogic chassis number is requested when the following message is displayed:

INPUT ANALOGIC BOX # (1-8) = R.

Enter the analogic chassis number in which the STB is installed.

Terminate the entry with a period.

If a number outside the specified range is entered, the following message is displayed:

RE-ENTER NUMBER R.

After successfully entering the chassis number, the STB slot number is requested. The following message is displayed:

INPUT CARD SLOT # (1-16) = R.

Enter the analogic chassis number in which the STB is installed.

If a number outside the specified range is entered, the following message is displayed:

RE-ENTER NUMBER

After successfully entering the slot number, the analog-to-digital type is requested. The following message is displayed:

INPUT A/D TYPE (A-J) = R.

Enter a single letter (type) chosen from the following list:

Type	Voltage Range
A	0 to 1
B	0 to 5
C	0 to 5.12
D	0 to 10
E	0 to 10.24
F	± 1
G	± 5
H	± 5.12
I	± 10
J	± 10.24

Any letter other than those listed, constitutes an error. The user will be prompted again for the A/D type.

After successfully entering the A/D type, the programmable gain is specified. The following message is requested:

PROGRAMMABLE GAIN (Y/N) = R.

Enter a Y (YES) for programmable gain or N (NO) for no programmable gain. A wrong entry will cause the prompt to be repeated.

After the system parameters are entered, a test number is specified. The following message is displayed:

ENTER TEST NUMBER = R.

Enter a test number (0 through 17) terminated with a period. The available tests are:

Test Number	Test Identification Message
0	Return to MAINTAIN III Executive
1	Test 1. Digital bus read/write test
2	Test 2. Sample and hold test
3	Test 3. A/D offset
4	Test 4. Measurement of A/D converter range accuracy =
5	Test 5. Power supplies
6	Test 6. Peak-to-peak noise test
7	Test 7. Slew rate test
8	Test 8. Common mode rejection
9	Test 9. Measurement of signal processor gains
10	Test 10. Missing codes test
11	Test 11. A/D linearity test
12	Test 12. Code center test
13	Test 13. Pass/fail lights

Test Number	Test Identification Message
14	Test 14. External digital output test
15	Test 15. External digital input test
16	Test 16. External analog inputs
17	Test 17. Input analogic box # (1-8) =

Test descriptions are contained in Section 3.3.2.

Except for those tests explained below, most tests do not require any operator intervention. The tests generate a test identification message and then cycle through programmed parameters. When the specified test is completed, a new test number is requested. The following message is displayed:

ENTER TEST NUMBER = R.

The user can then repeat the test or select any other test.

When test 6 or 16 is selected, the following message is displayed on programmable gain systems only.

ENTER GAIN CODE = R.

Enter a gain code of 10 through 13. Otherwise, a gain code of 10 is used on non-programmable systems.

In test 12, the following message is displayed:

ENTER VALUE FOR CODE CENTER R.

Enter a six digit octal number, left justified, and terminated with a period. Do not use the absolute top or bottom converter codes since these codes have only one edge and the center cannot be determined. Setting SS3 will abort this test.

In test 14, the following message is displayed:

D0 = R.
D1 = R.
D2 = R.
D3 = R.
D4 = R.
D5 = R.
D6 = R.
D7 = R.

The entries represent the eight digital outputs at the rear of the STB. Enter either a 1 or 0 for each signal (D0 through D8).

In test 17, the system parameters are re-entered.

3.5 PROGRAM EXAMPLES

This is a print-out example of an analogic system containing the following:

- 14-bit A/D wired for 10 volts full scale
- Programmable gain signal processor

```
ANALOGIC DIAGNOSTIC TEST PROGRAM    92( )0109-014B

INPUT  C  FOR CONTROLLER TEST
INPUT  S  FOR SELF TEST BOARD
S

INPUT CONTROLLER DEVICE ADDRESS (50-57).  50.

INPUT ANALOGIC BOX # (1-8) = 1.

INPUT CARD SLOT # (1-16) = 5.

INPUT A/D TYPE (A-J) = I.

PROGRAMMABLE GAIN (Y/N) = Y.

ENTER TEST NUMBER 1.

     0 ERRORS

ENTER TEST NUMBER 2.

TEST 2  SAMPLE & HOLD TEST

PART 1:  ODD-SAMPLE, EVEN SAMPLE

    PASS!!!

PART 2:  ODD HOLD, EVEN SAMPLE

    PASS!!!
```

```
PART 3:  ODD SAMPLE, EVEN HOLD

    PASS!!!

PART 4:  ODD HOLD, EVEN HOLD

    PASS!!!

ENTER TEST NUMBER 3.

TEST 3  A/D OFFSET

MEASUREMENT OF OFFSET IN A/D SYSTEM WITH SHORTED INPUTS = +0.00244140

ENTER TEST NUMBER 4.

TEST 4 MEASUREMENT OF A/D CONVERTER RANGE ACCURACY = 9.00146484 VOLTS

ENTER TEST NUMBER 5.

TEST 5  POWER SUPPLIES

+5 VOLT POWER SUPPLY =    +5.04624938

+15 VOLT POWER SUPPLY =  +15.09805679

-15 VOLT POWER SUPPLY =  -15.12857436

ENTER TEST NUMBER 6.

ENTER GAIN CODE (10 - 13) 10.

PEAK-PEAK NOISE WITH GAIN CODE 10 = +/-0.00061035 V (REF. TO A/D INPUT)

ENTER TEST NUMBER 7.

RESULT OF SLEW FROM MINUS REF. TO HIGH REF. =      0 COUNTS

RESULT OF SLEW FROM HIGH REF. TO MINUS REF. =     -1 COUNTS

ENTER TEST NUMBER 8.

CMV = +90% OF FULL SCALE, A/D READING = -0.00244140 VOLTS

CMV = -90% OF FULL SCALE, A/D READING = +0.00000000 VOLTS
```

```
ENTER TEST NUMBER 9.

TEST 9  MEASUREMENT OF SIGNAL PROCESSOR GAINS

OFFSET WITH GAIN CODE 10 = -0.00122070 V (REFERENCED TO A/D INPUT)

OFFSET WITH GAIN CODE 11 = -0.00122070 V (REFERENCED TO A/D INPUT)

OFFSET WITH GAIN CODE 12 = -0.00122070 V (REFERENCED TO A/D INPUT)

OFFSET WITH GAIN CODE 13 = +0.00000000 V (REFERENCED TO A/D INPUT)

INPUT VOLTAGE = +0.62500000 VDC

MEASUREMENT WITH GAIN CODE 10 = +0.62500000 (REFERENCED TO A/D INPUT)

MEASUREMENT WITH GAIN CODE 11 = +1.25000000 (REFERENCED TO A/D INPUT)

MEASUREMENT WITH GAIN CODE 12 = +2.49877929 (REFERENCED TO A/D INPUT)

MEASUREMENT WITH GAIN CODE 13 = +5.00000000 (REFERENCED TO A/D INPUT)

ENTER TEST NUMBER 10.

TEST 10  MISSING CODES TEST

 16384 CODES FOUND

     0 CODES MISSING

ENTER TEST NUMBER 11.

# TIMES          # CODES
 FOUND

  245                1     WIDEST CODE
   .                 .
   .                 .
   .                 .
  154                1     NARROWEST CODE
   0                 0     MISSING CODE
                   -------
                    4096     TOTAL NUMBER OF CODES
```

```
RECAP OF RESULTS:

# TIMES              CODES
 FOUND

  245                  1      WIDEST CODE
  154                  1      NARROWEST CODE

  196                327      HIGHEST # OF CODES

ENTER TEST NUMBER 12.

TEST 12 CODE CENTER TEST

ENTER OCTAL VALUE FOR CODE CENTER 100004.

   DESIRED VOLTAGE = -9.99877929 VOLTS

                  (SET SS3  -  RESET SS3)

ENTER TEST NUMBER 12.

TEST 12 CODE CENTER TEST

ENTER OCTAL VALUE FOR CODE CENTER 0.

   DESIRED VOLTAGE = +0.00000000 VOLTS

                  (SET SS3  -  RESET SS3)

ENTER TEST NUMBER 12.

TEST 12 CODE CENTER TEST

ENTER OCTAL VALUE FOR CODE CENTER 77770.

   DESIRED VOLTAGE = +9.99755859 VOLTS

                  (SET SS3  -  RESET SS3)

ENTER TEST NUMBER 13.

TEST 13  PASS/FAIL LIGHTS

    THE GREEN/RED LEDS ON THE SELF TEST BOARD
    WILL CYCLE ON/OFF IN THE FOLLOWING SEQUENCE:

                  GREEN ON
                  RED ON
                  GREEN & RED ON
                  GREEN & RED OFF
```

EACH PHASE IS APPROXIMATELY 5 SECONDS LONG.

ENTER TEST NUMBER 14.

TEST 14 EXTERNAL DIGITAL OUTPUT TEST

D0 = 1

D1 = 0

D2 = 1

D3 = 0

D4 = 1

D5 = 0

D6 = 1

D7 = 0

CODE TRANSMITTED

ENTER TEST NUMBER 15.

D0 = 1

D1 = 1

D2 = 1

D3 = 1

D4 = 1

D5 = 1

D6 = 1

D7 = 1

ENTER TEST NUMBER 16.

TEST 16 EXTERNAL ANALOG INPUTS (USING A 5 VOLT PRECISION P.S.)

ENTER GAIN CODE 10.

CH 0 = +5.00244140 V (REFERENCED TO A/D INPUT)

CH 2 = +5.00488281 V (REFERENCED TO A/D INPUT)

CH 4 = +5.00488281 V (REFERENCED TO A/D INPUT)

CH 6 = +5.00366210 V (REFERENCED TO A/D INPUT)

CH 10 = +5.00244140 V (REFERENCED TO A/D INPUT)

CH 12 = +5.00366210 V (REFERENCED TO A/D INPUT)

CH 14 = +5.00244140 V (REFERENCED TO A/D INPUT)

CH 16 = +5.00366210 V (REFERENCED TO A/D INPUT)

3.6 ERRORS

When an error condition is detected by the program, an error message is displayed. Error message descriptions are contained in Section 3.3.