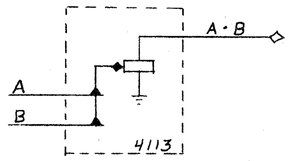
LOGIC DRAWINGS

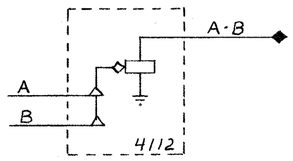
The symbology used in the LINC logic drawings is very similar to that used by Digital Equipment Corporation (DEC) of Maynard, Massachusetts. For a general explanation of this symbology, see DEC manual C-100. This manual also contains a description of each of the DEC logic packages used in the LINC. Other logic packages used in the LINC are described in volume 2 of the LINC Manufacturing Description.

DEC packages are identified by type numbers such as 4113, 4204, 4141, etc. Some of these packages can be jumpered internally to satisfy different loading conditions or to perform different logic functions. Packages used in the LINC indicate their jumpering configuration through suffixes appended to their type number. The package 4204, for example, appears as a plain 4204, a jumpered 4204A, and a jumpered 4204AC. The jumpering configuration specified by a suffix can be looked up in volume 2 of the LINC Manufacturing Description.

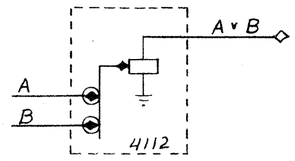
A broken line encloses each logic package or piece thereof that appears on a LINC logic drawing. The package type is written just inside the broken line, the packages frame location is written just outside. Minor variation from DEC symbology can always be resolved by looking up a particular package in the DEC manual and checking out the pins in questions. Grosser departures from DEC symbology are explained to the right.



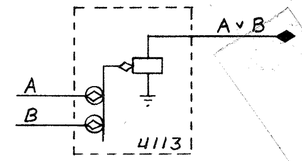
NEG. "AND"



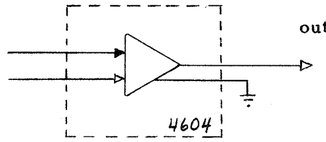
GND. "AND"



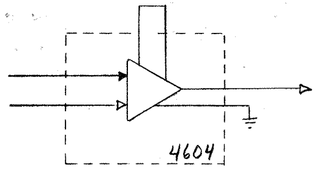
NEG. "OR"



GND. "OR"

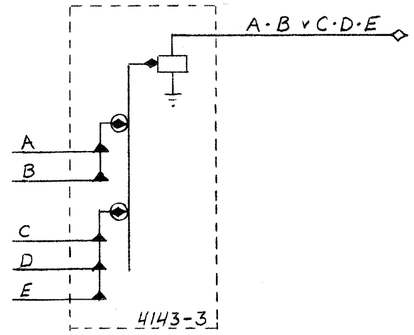


output is a 0.4 usec pulse.



jumper makes output a 1.0 usec pulse.

PULSE AMPLIFIERS



NEG. "AND-OR"

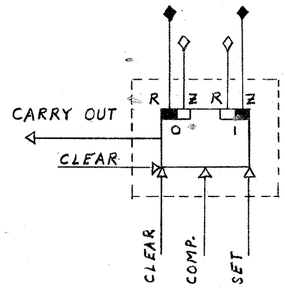
TIMING DIAGRAMS

Timing diagrams are used to show that occurence and relationship of the various operations involved in the execution of an instruction. In this notation, each of the principal flip-flop registers is represented by a horizontal line. Time is measured along the line from left to right, and operations involving the register are marked at their proper time of occurence. The registers R, L, and Z are shown only in those instructions that involve them. Registers B, C, P, S, and A are always shown. The operation of memory is indicated by a line marked "M." When this line is displaced upward, memory is in its read phase: when it's displaced downward, memory is in its write phase. A conditional operation of memory is indicated by a broken line.

Most operations occur at one of the standard event times marked along the top of the diagram by the numbers 0, 1, 2, and 3 (representing time pulses t_0, t_1, t_2, and t_3). Some operations, however, occur at other times. The clearing of S, for example, occurs at the end of the memory write gate if memory is operated. Otherwise it occurs at time t_2.

A vertical arrow indicates the modification of the contents of one register by the contents of another. The type of modification involved is specified to the right of the arrow head. All other operations are indicated by small vertical slash marks. If a slash mark indicates the clearing of a register, the register line will end at the slash mark. If the slash mark indicates anything else, the name of the operation is specified to its right.

Parentheses around the name of an operation indicate it as being conditional. Notes to one side of the diagram will specify the condition. Parentheses around the head of an arrow or around a slash mark indicate that more than one kind of operation can occur. Notes to the side of the diagram will call out the different operations possible and will specify the conditions under which they occur.



FLIP-FLOP

Outputs: 1. Output pins are shown twice, once for each side of the flip-flop. In this example, the output pins are R and Z. The example indicates that:

when the flip-flop is a "zero," pin R is negative and pin Z is gnd.
when the flip-flop is a "one," pin Z is negative and pin R is gnd.

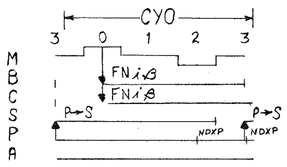
Inputs: 1. AC coupled inputs are always drawn as though connected to a pulse source, even when the input signal is not a pulse.

2. "Clear" inputs may be drawn in either of the two ways shown.

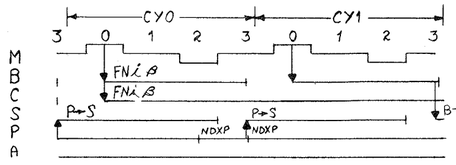
CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC	SYMBOLOGY AND NOTATION	
ENG.		
DATE	1000 –	CH.

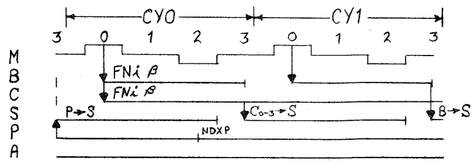
INDEX CLASS AND HALF WORD CLASS SET-UP CYCLES.



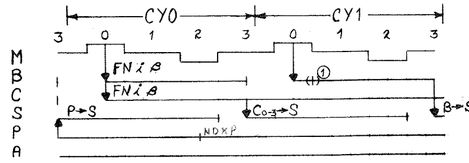
i1B0



i0B0



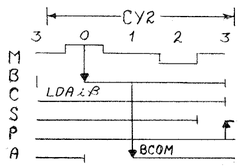
i0B0

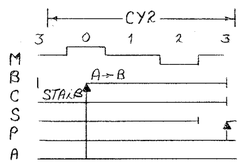


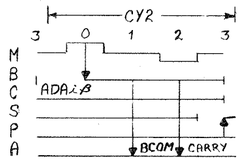
i1B0

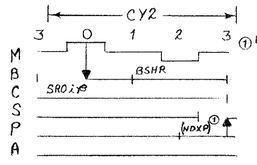
① NDXB IFF $\overline{(LDH \vee STH \vee SHD)}$
HALFNDXB IFF (LDH ∨ STH ∨ SHD)

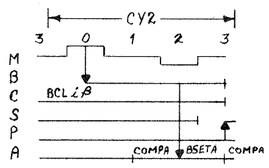
INDEX CLASS EXECUTION CYCLES.

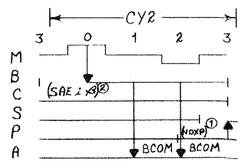


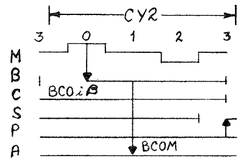


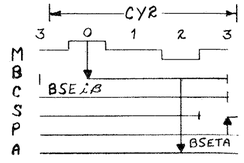


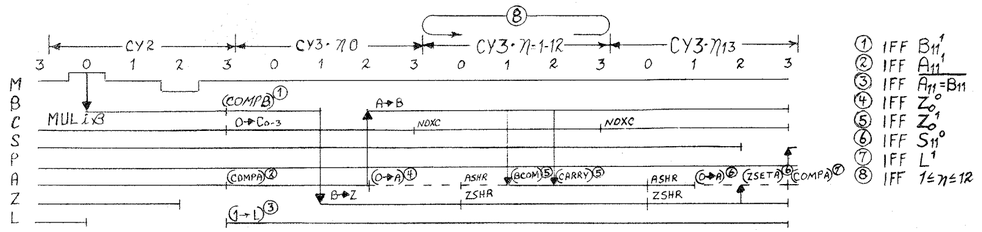


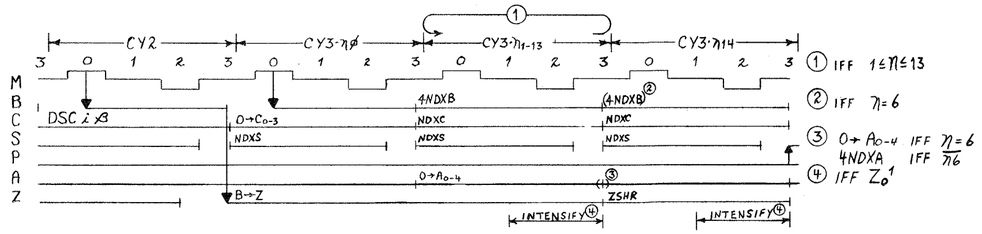


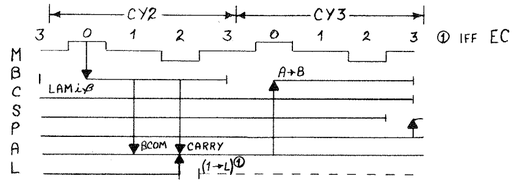


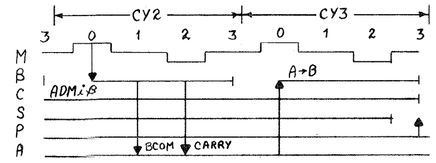




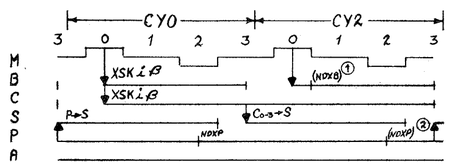




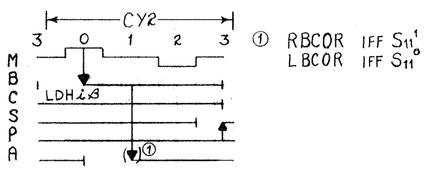




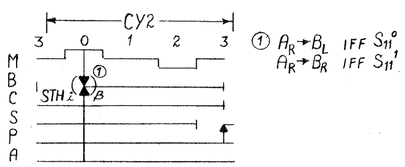
HALF WORD EXECUTION CYCLES.



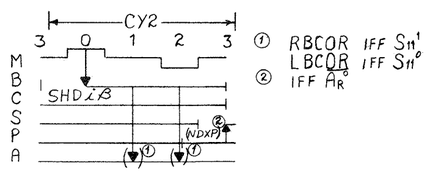
① IFF i=1
② IFF B_{0-7}^{1FFF}



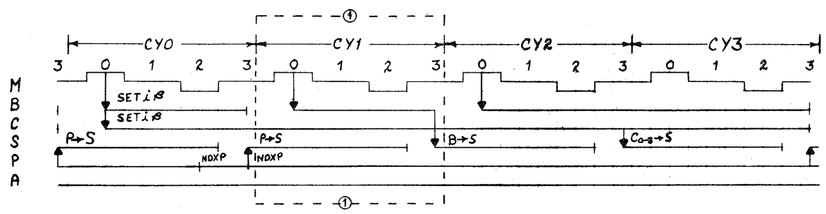
① RBCOR IFF S_{11}^{1}
LBCOR IFF S_{11}^{0}



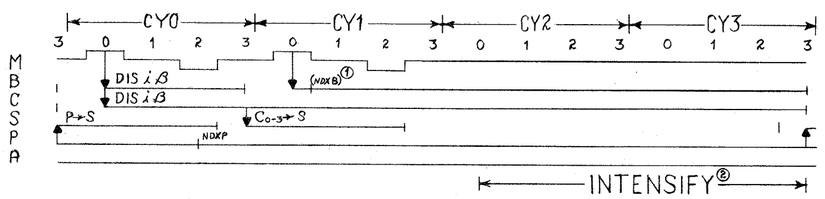
① $A_R \rightarrow B_L$ IFF S_{11}^{0}
$A_R \rightarrow B_R$ IFF S_{11}^{1}



① RBCOR IFF S_{11}^{1}
LBCOR IFF S_{11}^{0}
② IFF A_R^{0}



① CY1 IFF i=0



① IFF i=1
② THE SCOPE INTENSIFIES ON RECEIPT OF AN ON INTENSIFY PULSE (ONINTP) AND TERMINATES ON RECEIPT OF AN OFF INTENSIFY PULSE (OFFINTP)

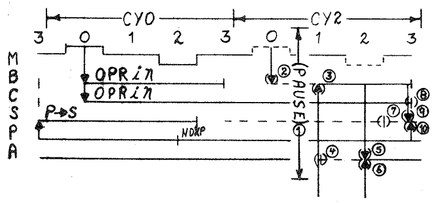
CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC — INSTRUCTION TIMING SHEET #1

ENG.

DATE 1001 CH.

OPERATE CLASS INSTRUCTIONS.

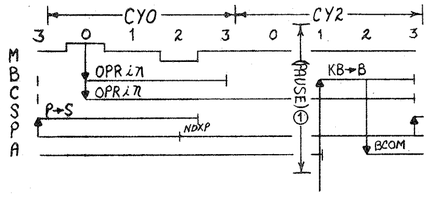


① IFF i=1 AND $\overline{\text{XCMET}}$
RESUME WHEN (XCMET OR QKRESTART)
② IFF MOUT
③ UN→B IFF UNEL
VN→B IFF VNEL
KB→B IFF n15
RS→B IFF n16
LS→B IFF n17
④ O→A IFF (n15∨n16∨n17∨CLEL ∨SNEL∨TNEL)·$\overline{\text{BEGT}}$

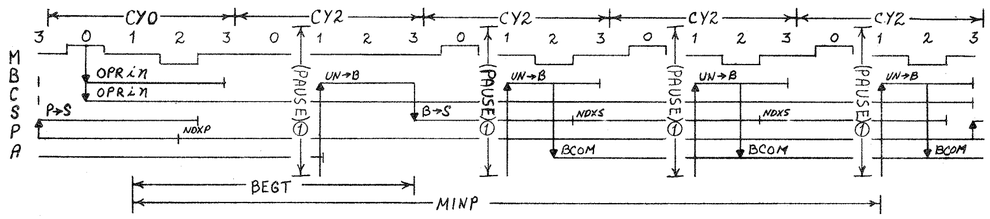
⑤ BCOM IFF $\overline{\text{BEGT}}$ · DOINTFF
⑥ SN→A IFF SNEL
TN→A IFF TNEL
⑦ ~~O→A IFF GULP~~
NDXS IFF GULP·BEGT
⑧ O→C IFF GNIL
⑨ B→S IFF BEGT
⑩ P→S IFF GNIL

EXAMPLES OF OPERATE USAGE

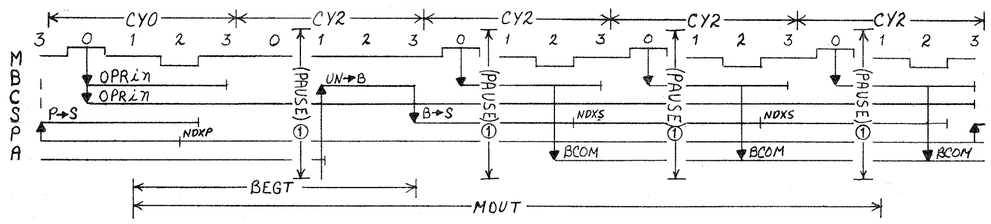
A. OPR i n15 (KBD)



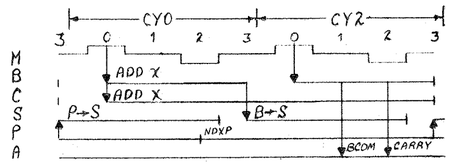
B. OPR · GULP (3 WORD TRANSFER INTO MEMORY)

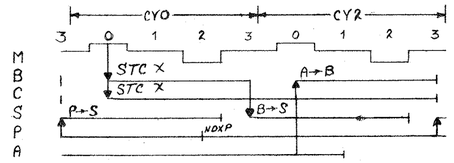


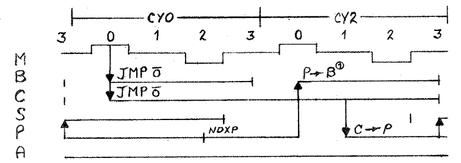
C. OPR · GULP (3 WORD TRANSFER OUT OF MEMORY)



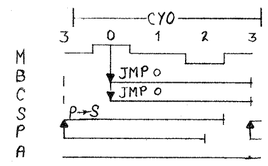
FULL ADDRESS INSTRUCTIONS.



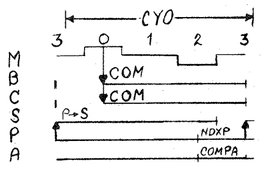


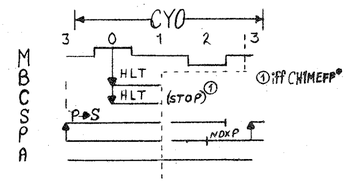


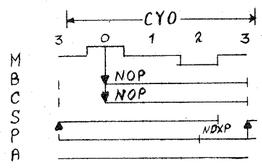
① $1 \rightarrow (B_{11} \cdot B_{10})$ IFF P→B

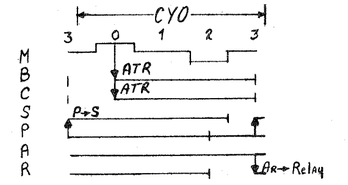


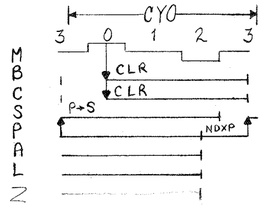
MISCELLANEOUS CLASS INSTRUCTIONS

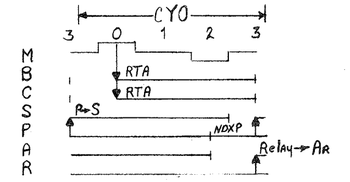




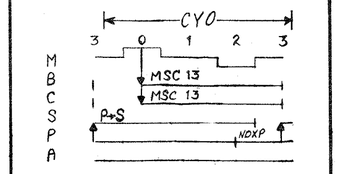


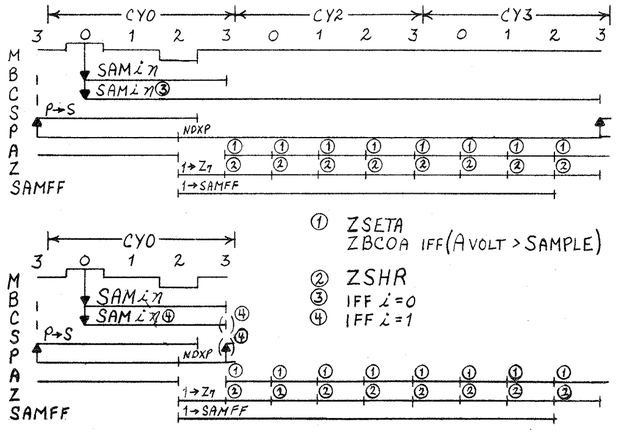






to be used with MARK program only

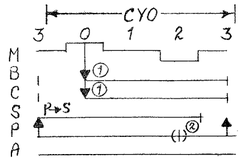




① ZSETA
ZBCOA IFF (AVOLT > SAMPLE)
② ZSHR
③ IFF i=0
④ IFF i=1

SKIP CLASS INSTRUCTIONS

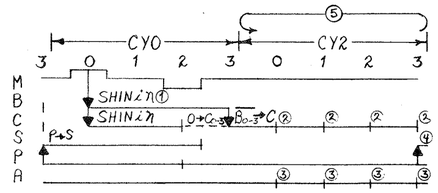
SKP i n_{0-5} = SNS i n_{0-5}
n_{10} = AZE i
n_{11} = APO i
n_{12} = IZE i
n_{13} = IBZ i
SXL i n_{0-14} = SXL i n_{0-14}
n_{15} = KST i



① SKP i n ∨ SXL i n
② NDXP IFF CMET
ZNDXP IFF CMET

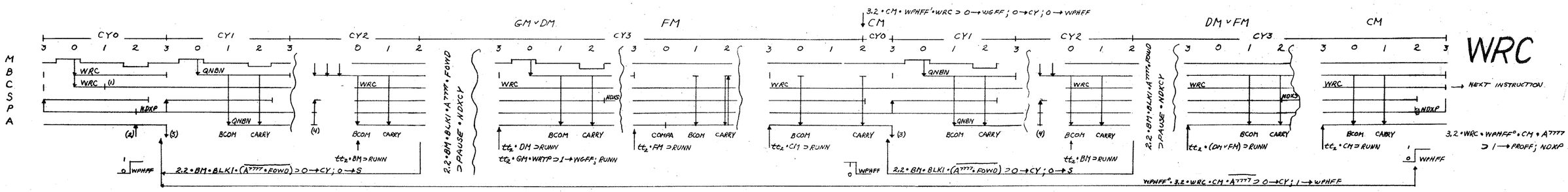
NOTE:
i_{0_3} *Skip if condition met.*
i_{1_3} *Skip if condition not met.*

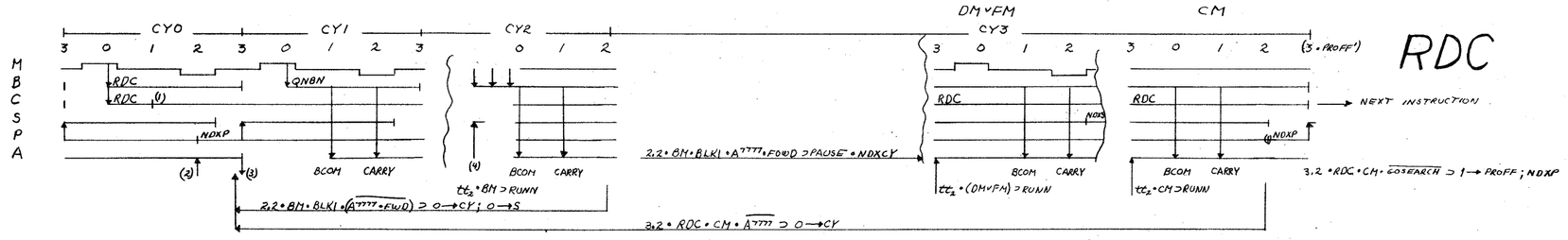
ROTATE CLASS INSTRUCTIONS

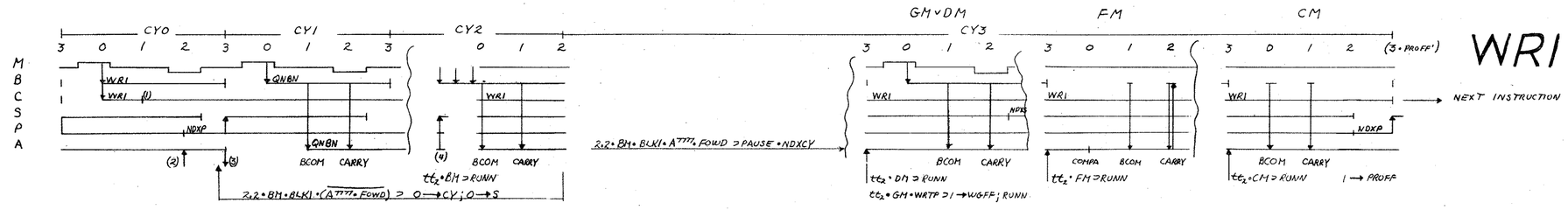


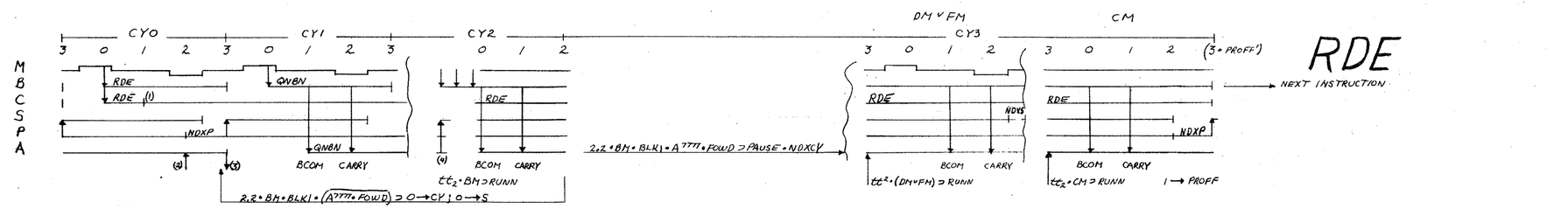
① SHIN = ROL∨ROR∨SCR
② NDXC IFF n=17
③ ASHR IFF ROR∨SCR
ASHL IFF ROL
④ P→S IFF n=17
⑤ IFF $\overline{n17}$

CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			INSTRUCTION TIMING SHEET #2
ENG.			
DATE	1002		CH.









NOTES

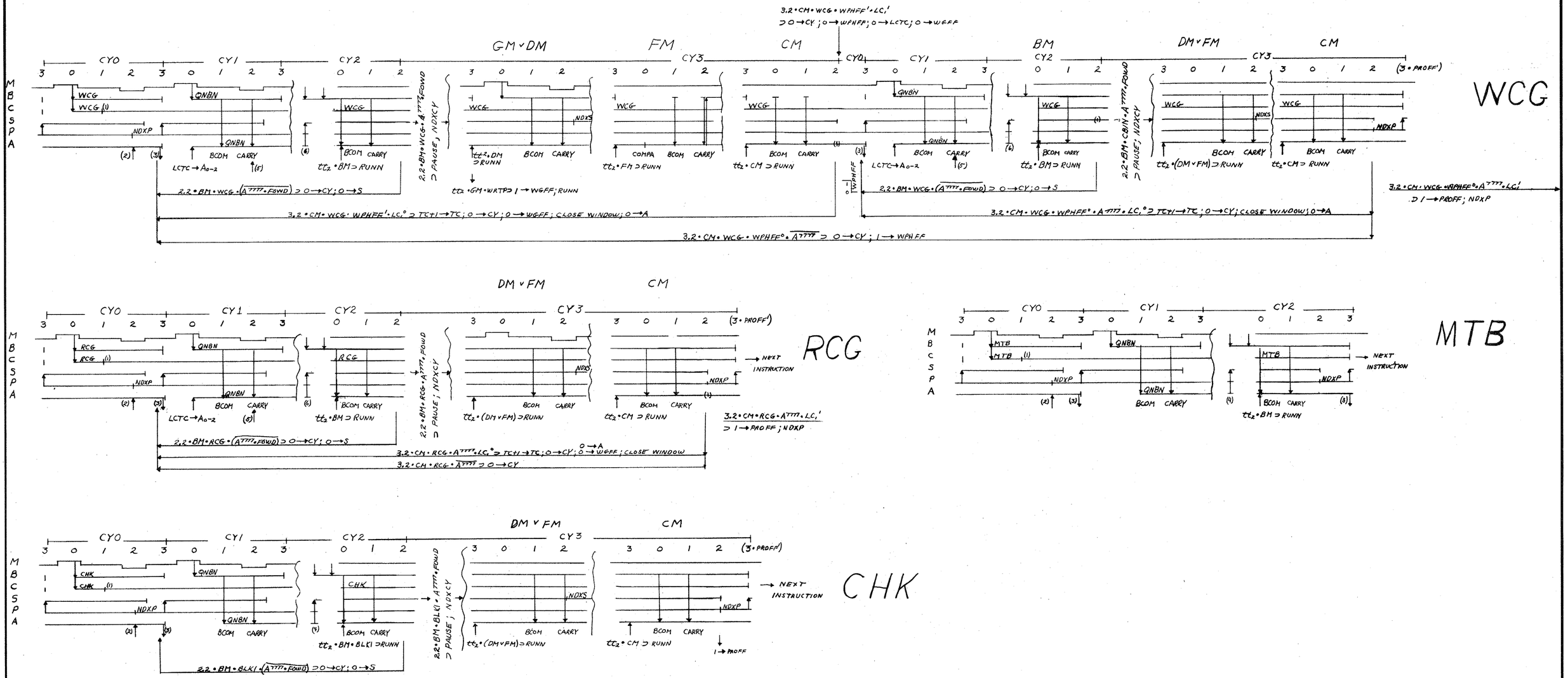
(1) SET UNIT

(2) MOTN$_n$ → A$_n$; 0 → LCTC ; 1 → WPHFF ; 0 → PROFF

(3) SET MOTION

(4) FIXQL(0 → A$_{q-11}$) ; A$_{q-11}$ → S$_{8-10}$

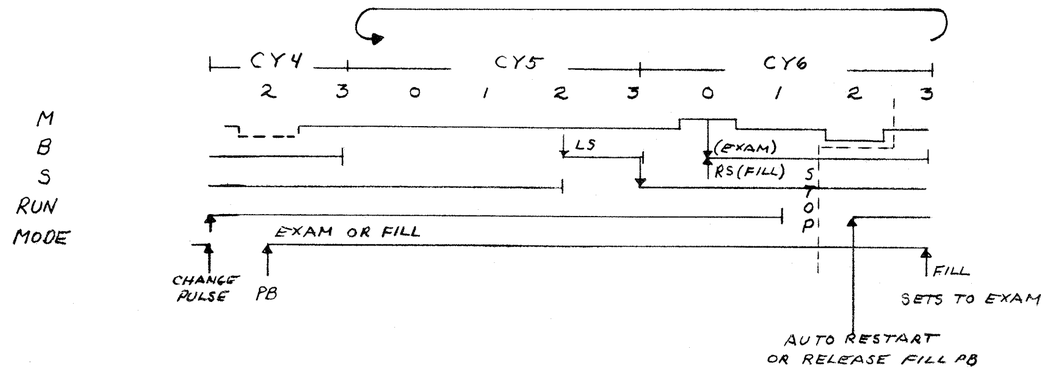
CHANGE LIMITS	APP'D BY	DATE	CHANGES
LINC			INSTRUCTION TIMING SHEET 3
ENG.			
DATE	1003		CH.

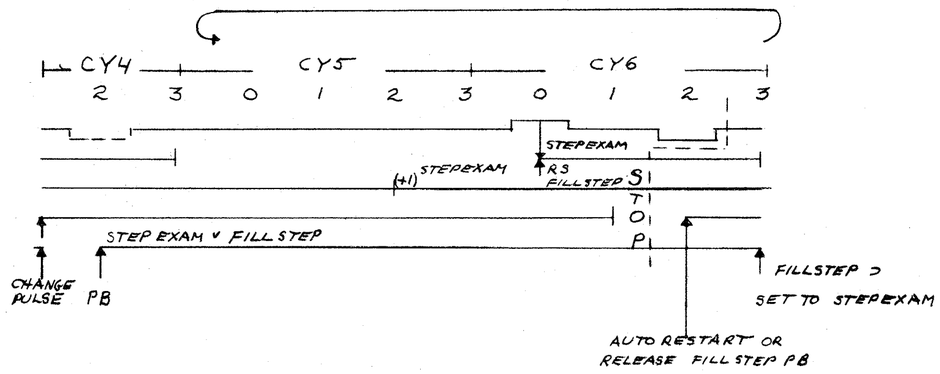


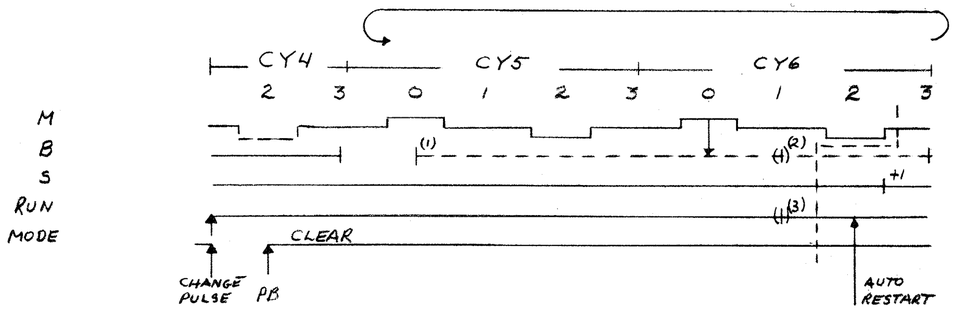
NOTES:

1. SET UNIT
2. MOTN$_0$ → A$_{11}$; 0 → LCTC; 1 → WPHFF; 0 → PROFF
3. SET MOTION
4. FIXQ (0 → A$_{5-11}$); A$_{5-11}$ → S$_{8-10}$
5. B$_{9-11}$ ≡ LCTC$_{0-2}$ ⊃ 1 → LC$_1$
6. FIXQR(0 → A$_{5-11}$); A$_{0-2}$ → S$_{8-10}$

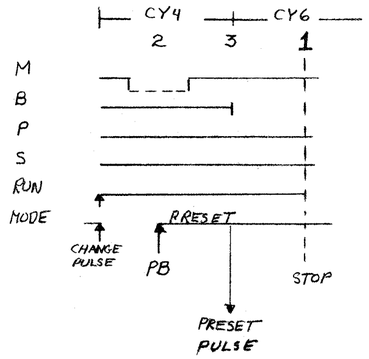
CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			INSTRUCTION TIMING
ENG.			SHEET 4
DATE	1004		CH.

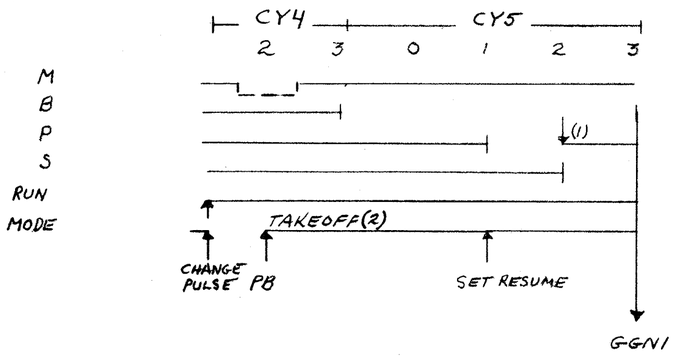






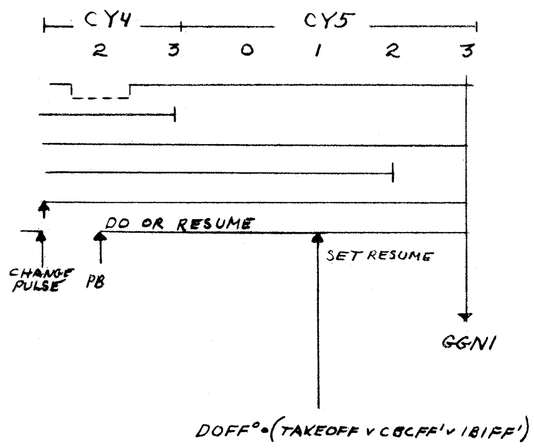
(1) $S_{11}' \supset$ SET B
(2) $S_{11}' \cdot \overline{B^0} \supset$ COMPB
(3) $\overline{B^0} \cdot (S_{10} \vee MEM1) \supset$ STOP





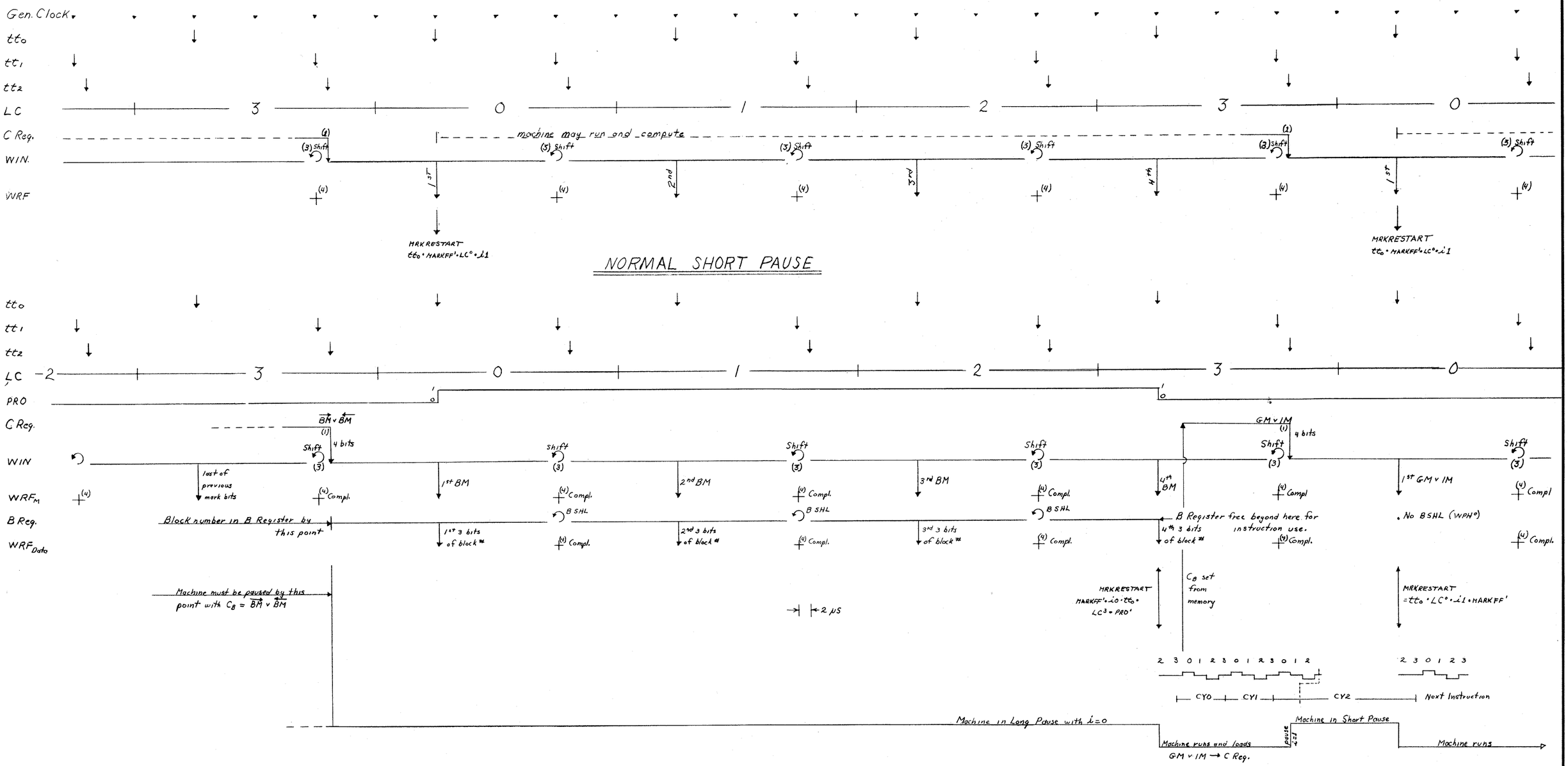
(1) START 20 ⊃ 20 → P
" 400 ⊃ 400 → P
" RS ⊃ RS → P
MARK ⊃ 40 → P

(2) TAKEOFF = ST20FF' v ST400FF' v STRSFF' v MARKFF'



DOFF° · (TAKEOFF v C8CFF' v 181FF')

CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			CONSOLE FUNCTION TIMING DIAGRAM
ENG.			
DATE	1005		CH. E



Notes:

(1) Machine must be paused by this time with next mark in $C_B \cdot tt_2 \cdot LC^3$ jams $C_B \rightarrow WIN$.

(3) Shift next bit for mark track into leftmost bit of WIN (WIN_3). Shift in zeros from right so cleared before load from C_B.

(4) Complement WRF_M at tt_1 time; tt_0's load it from WIN_3.

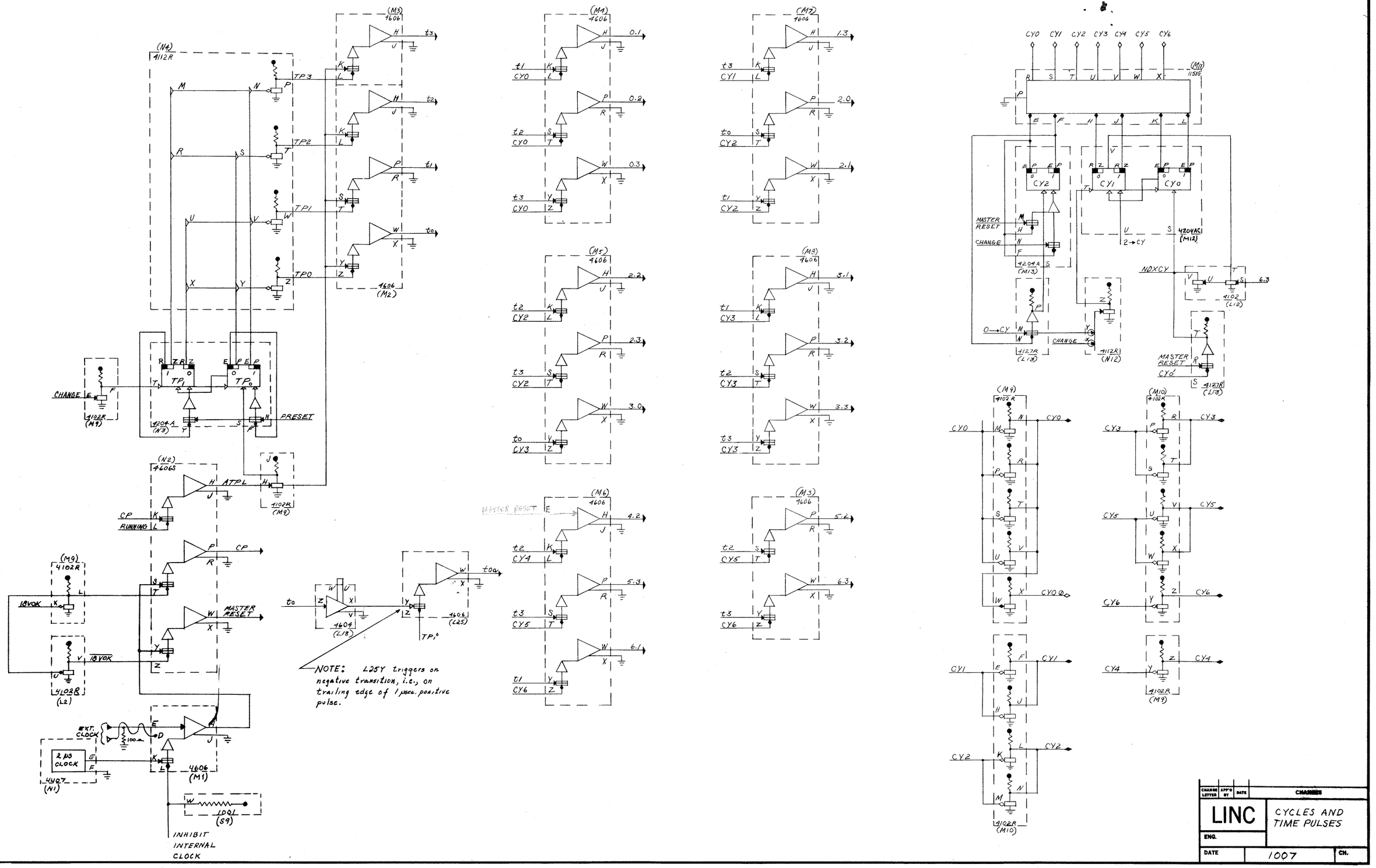
CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC — TAPE MARKING TIMING DIAGRAM

ENG.

DATE 1006 CH.

1008	0 → CY
1008	2 → CY
EXT.	18VOK ◇
1008	CHANGE
EXT.	EXT. CLOCK
EXT.	INHIBIT INT. CLOCK
1008	NDXCY
1018	PRESET
1009	RUNNING

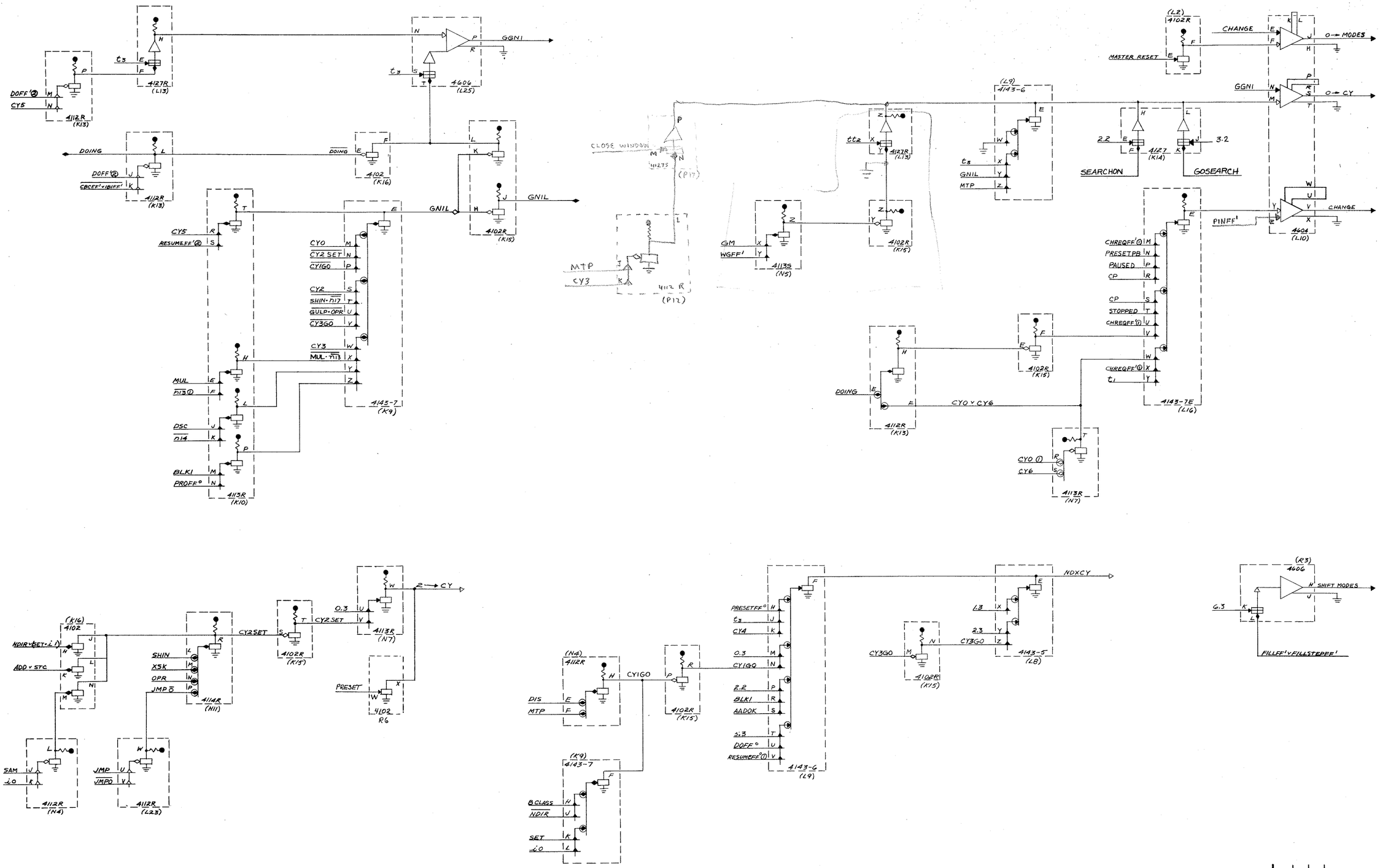


CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			CYCLES AND TIME PULSES
ENG.			
DATE	1007		CH.

1007	0.0 = 4.3
1026	AADOK
1020	ADD + STC
1020	BCLASS'
1026	BLK1
1018	CBCFF' v IBIFF'
1018	CHREQFF
1024	CP — CLOSE WINDOW
1007	CP
1020	CY3GO
1007	CY0 - CY6
1018	DOFF
1018	FILLFF' v FILLSTEPFF'

1024	GM
1026	GOSEARCH
1020	GULP · OPR
1012	INSTRUCTIONS ϕ
1020	INSTRUCTIONS ϕ
1012	i0 - i1
1017	JMPO
1007	MASTER RESET
1012	NO - N17
1020	NDIR
1020	NDIR v (SET · i1)
1009	PAUSED
1026	PINFF

1018	PRESET
1018	PRESETFF
1018	PRESETPB ϕ — PROFF (1026)
1018	RESUMEFF
1026	SEARCHON
1020	SHIN
1020	SHIN · N17
1009	STOPPED
1007	$t_0 - t_3$
1023	$tt_0 - tt_2$
1024	WGFF



CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC

MODE AND CYCLE CONTROL LOGIC

ENG.

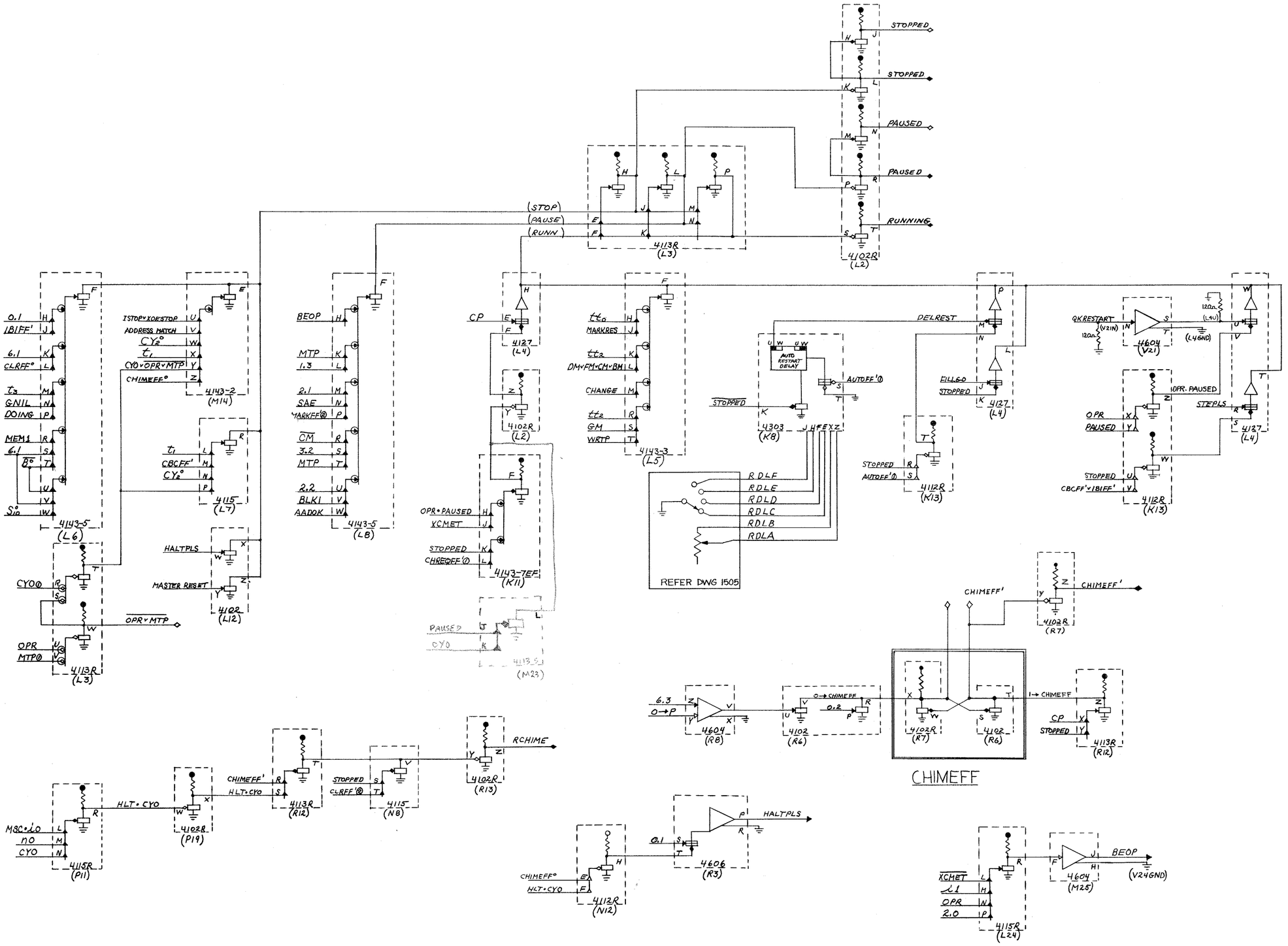
DATE 1008 CH.

1007	0.0 – 6.3
1017	0 → P
1026	AADOK
1021	ADDRESS MATCH
1018	AUTOFF
1016	B°
1026	BLK1
1018	CBCFF
1018	CBCFF' ∨ 1BIFF'
1008	CHANGE
1018	CHREQFF
1018	CLRFF

1026	CM ◇
1007	CP
1007	$CY_0 - CY_2$
1007	CY0 - CY6
1026	DM ∨ FM ∨ CM ∨ BM
1008	DOING
1018	FILLGO
1024	GM
1008	GNIL
1018	1BIFF
1012	INSTRUCTIONS ◇
1020	INSTRUCTIONS ◆

1018	ISTOP ∨ XOESTOP
1018	MARKFF
1026	MARKRES
1007	MASTER RESET
1030	MEM 1
1020	MSC - iO
EXT.	QKRESTART
EXT.	RDLA – RDLF
1013	$S_0 - S_{11}$
1018	STEPLS
1007	$t_0 - t_3$
1023	$tt_0 - tt_2$

1021	XCMET



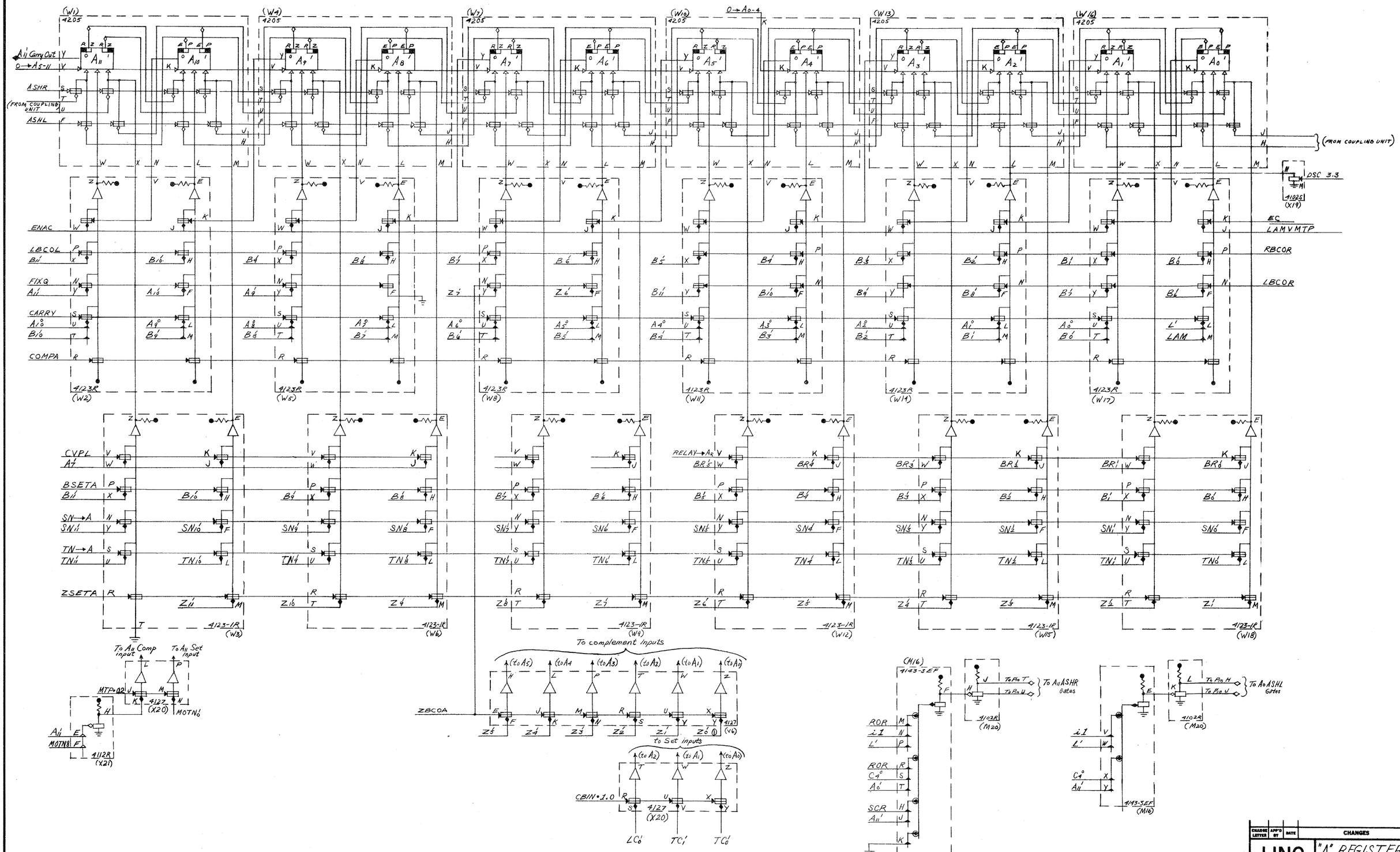
CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC	RUN – PAUSE – STOP LOGIC	
ENG.		
DATE	1009	CH.

1015	$0 \rightarrow A_{0-4}$
1015	$0 \rightarrow A_{5-11}$
1015	ASHL
1015	ASHR
1011	$B_0 - B_{11}$
1022	$BR_0 - BR_5$
1015	BSETA
1012	$C_0 - C_{11}$
1015	CARRY
1026	CBIN · 1.0
1015	COMPA
1027	CVPL

1020	DSC · 3.3
1014	EC
1015	ENAC
1015	FIXQ
1012	$i0 - i1$
1020	INSTRUCTIONS
1014	L
1020	LAM · MTP
1015	LBCOL
1015	LBCOR
1023	$LC_0 - LC_1$
1025	$MQTN_0 - MQTN_1$

1015	RBCOR
1015	RELAY $\rightarrow AR$
1015	$SN \rightarrow A$
EXT.	$SN_0 - SN_{11}$
1023	$TC_0 - TC_1$
1015	$TN \rightarrow A$
EXT.	$TN_0 - TN_{11}$
1014	$Z_0 - Z_{11}$
1027	ZBCOA
1015	ZSETA



COUPLING UNIT

CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC — "A" REGISTER

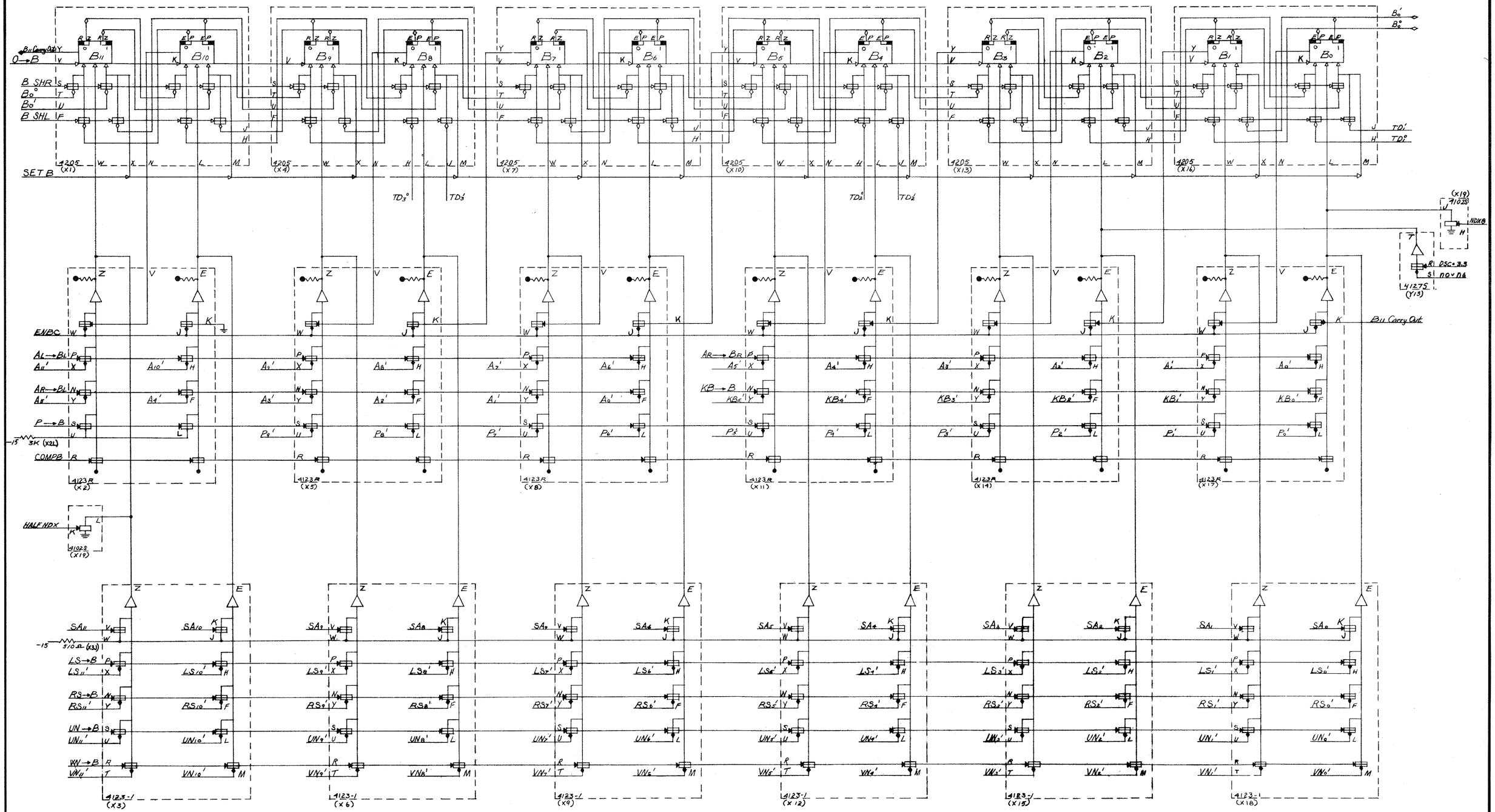
ENG.

DATE 1010 CH.

1016	0 → B
1010	$A_0 - A_{11}$
1016	$A_L \rightarrow B_L$
1016	$A_R \rightarrow B_L$
1016	BSHL
1016	BSHR
1016	COMPB
1020	DSC·3.3
1016	ENBC
1016	HALFNDX
1016	LS → B
EXT.	$LS_0 - LS_{11}$

1015	n0 ∨ n6
1016	NDXB
1016	P → B
1013	$P_0 - P_9$
1016	RS → B
EXT.	$RS_0 - RS_{11}$
1028	$SA_0 - SA_{11}$
1016	SETB
1024	$TD_1 - TD_3$
1016	UN → B
EXT.	$UN_0 - UN_{11}$
1016	VN → B

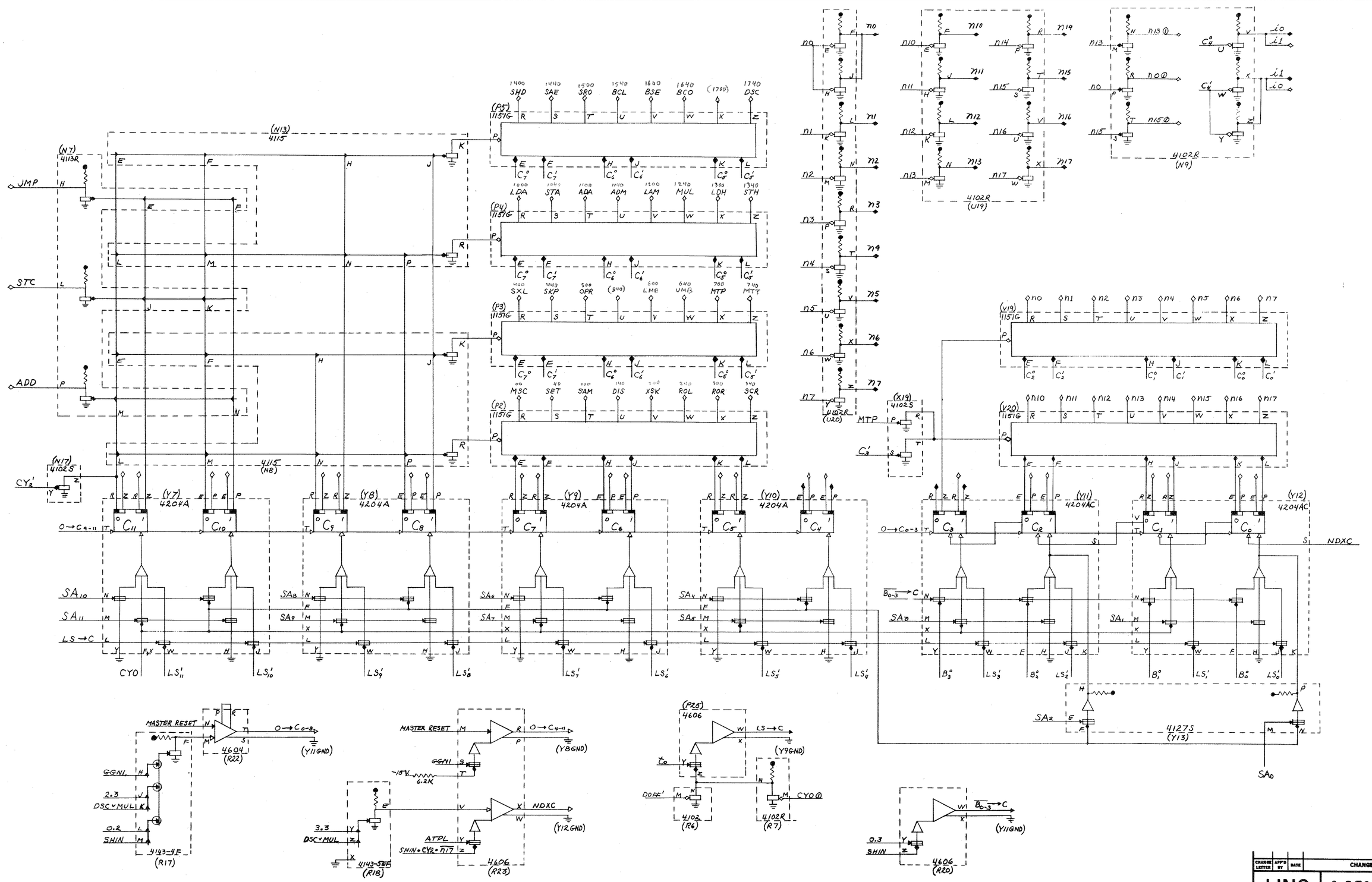
EXT. | $VN_0 - VN_{11}$



CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			B REGISTER
ENG.			
DATE	1011		CH.

1007	0.0 – 6.3
1007	ATPL
1007	$CY_0 - CY_2$
1007	CY0 – CY6
1018	DOFF
1020	DSC v MUL
1008	GGN1
1020	INSTRUCTIONS ↑
EXT.	$LS_0 - LS_{11}$
1007	MASTER RESET
1028	$SA_6 - SA_{11}$
1020	SHIN

1015 | SHIN · CY2 · $\overline{n17}$



CHANGE LETTER	APP'D BY	DATE	CHANGES

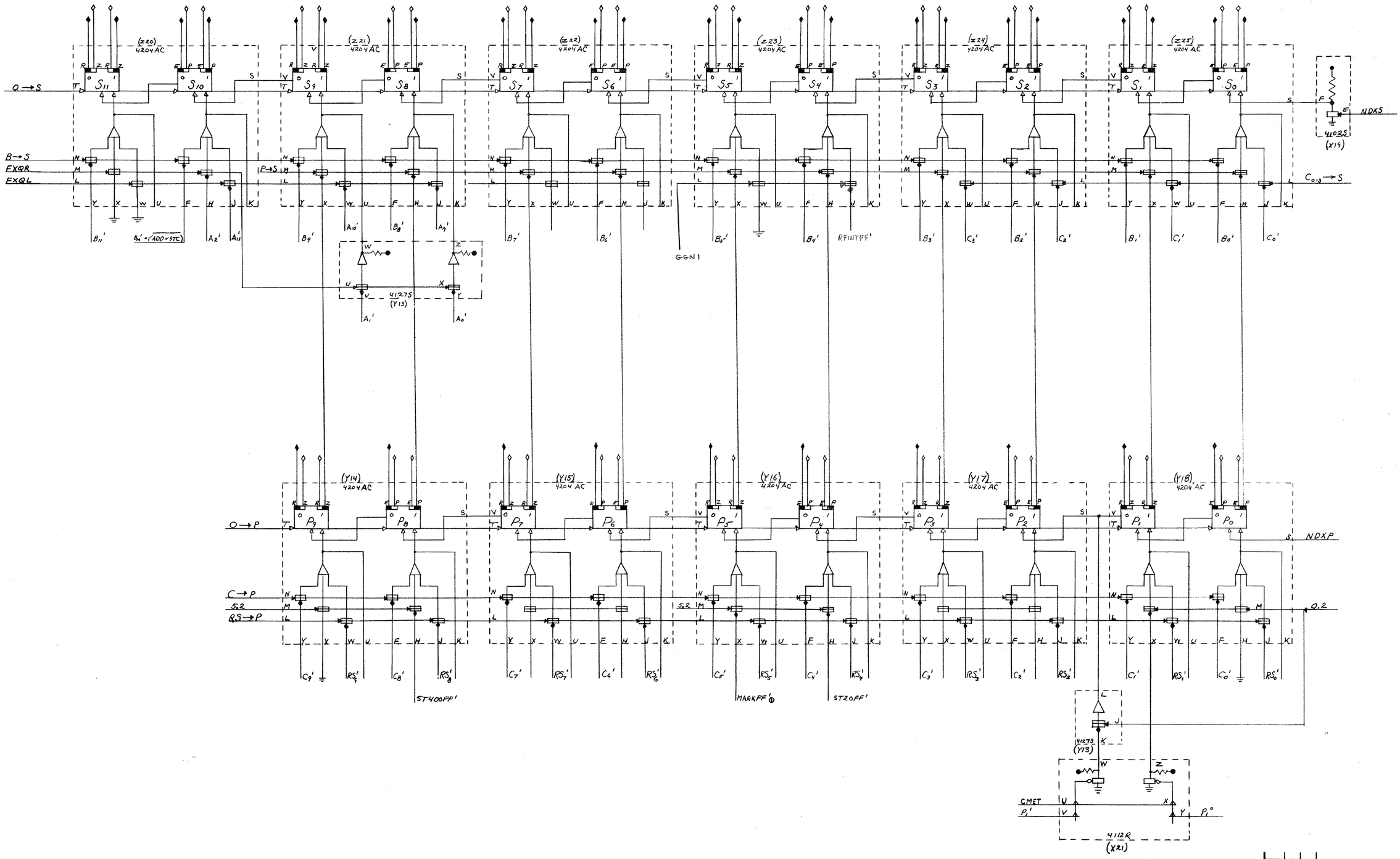
LINC — C REGISTER

ENG.

DATE 1012 CH.

1007	0.0 – 6.3
1017	O → P
1017	O → S
1010	$A_0 - A_{11}$
1017	B → S
1011	$B_0 - B_{11}$
1020	$B_{10}' \cdot (\overline{ADD \vee STC})$
1017	C → P
1017	$C_{0-3} \rightarrow S$
1012	$C_0 - C_{11}$
1017	CMET
1017	FXQL

1008	1017	FXQR
	1018	MARKFF
	1017	NDXP
	1017	NDXS
1036	1017	P → S
	1017	RS → P
	EXT.	$RS_0 - RS_{11}$
	1018	ST20FF
	1018	ST400FF

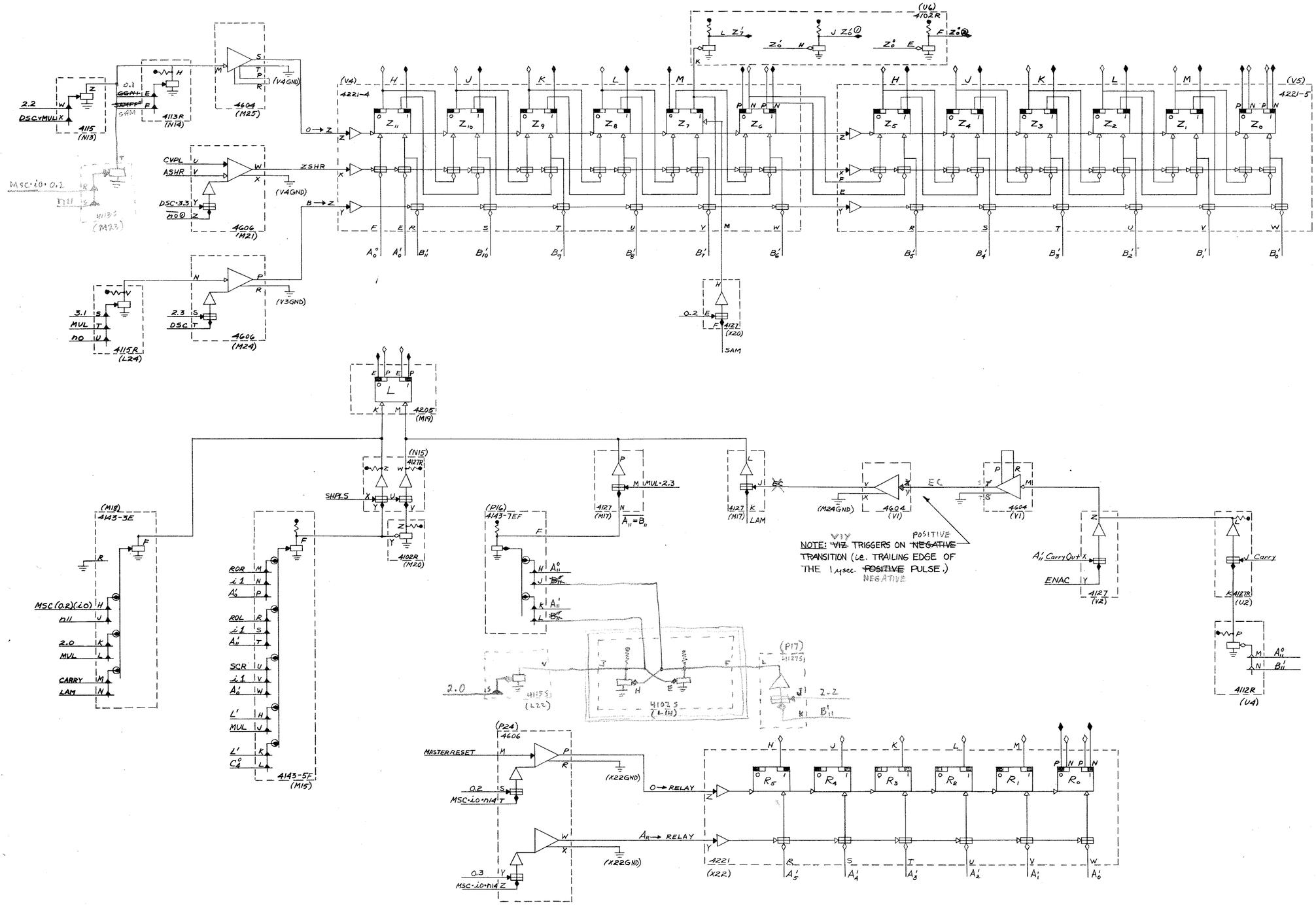


CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC	P & S REGISTERS	
ENG.		
DATE	1013	CH.

1007	0.0 – 6.3
1010	$A_0 - A_{11}$
1015	ASHR
1011	$B_0 - B_{11}$
1012	$C_0 - C_{11}$
1015	CARRY
1027	CVPL
1020	DSC · 3.3
1020	DSC v MUL
1015	ENAC
1008	GGNI
1012	i0 – i1

1020	INSTRUCTIONS
1007	MASTER RESET
1020	MSC · i0 · n14
1020	MSC · i0 · 0.2
1020	MUL · 2.3
1012	n0 – n17
1027	SAMFF
1015	SHPLS



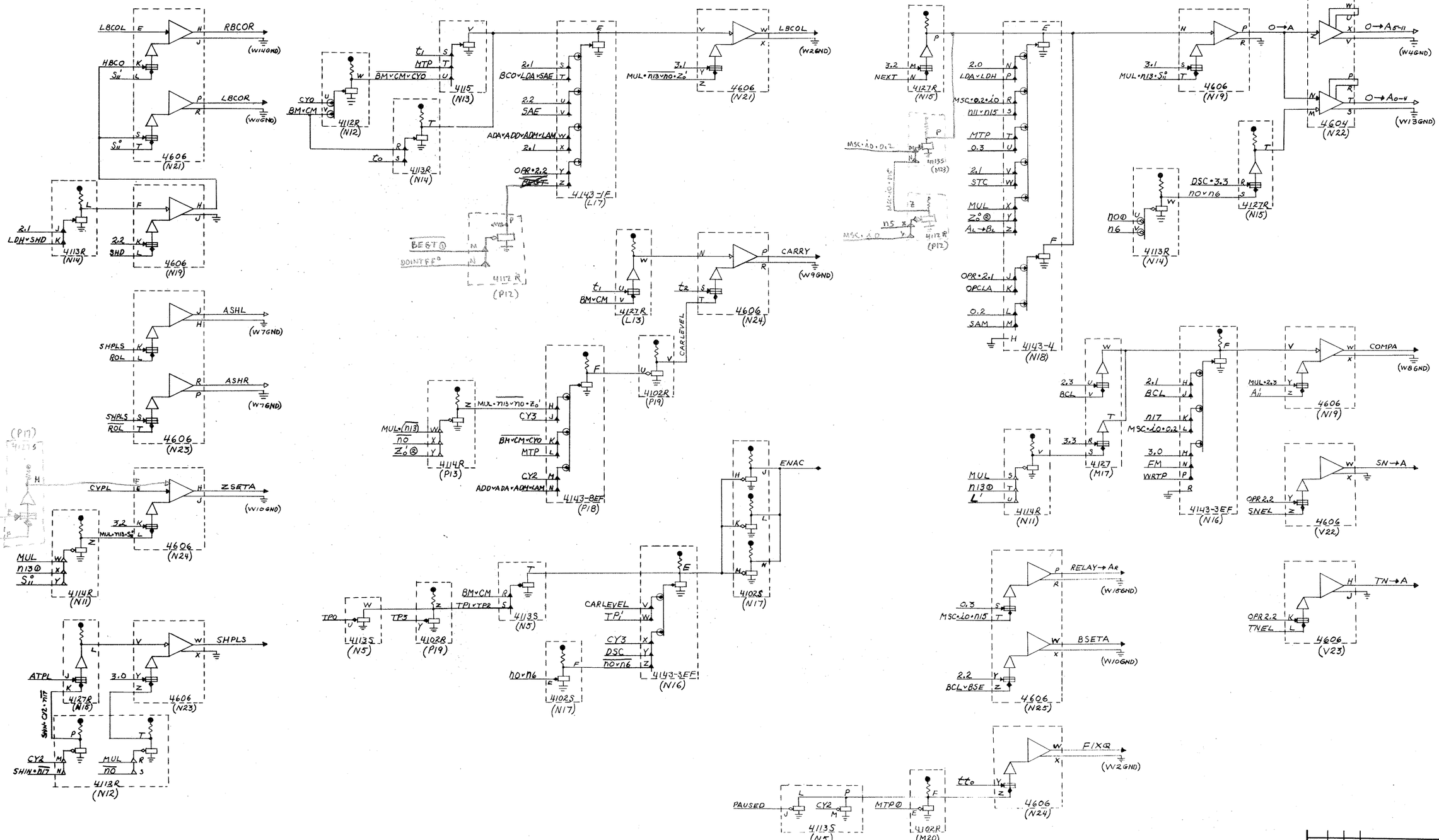
CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			L, Z + R REGISTERS
ENG.			
DATE	1014		CH.

1007	0.0 – 6.3
1010	$A_0 - A_{11}$
1016	$A_L \rightarrow B_L$
1020	ADD ∨ ADA ∨ ADM ∨ LAM
1007	ATPL
1020	BCL ∨ BSE
1020	BCO ∨ LDA ∨ SAE
1020	BEGT ◇
1026	BM ∨ CM
1027	CVPL
1007	CY0 – CY6
1020	DSC · 3.3

1024	FM
1012	INSTRUCTIONS ◇
1020	INSTRUCTIONS ◆
1014	L
1020	LDA ∨ LDH
1020	LDH ∨ SHD
1020	MSC · i0 · n15
1020	MSC · i0 · 0.2
1020	MUL · 2.3
1008	MUL · $\overline{n13}$
1015	MUL · n13 · S_{11}^{0}
1012	n0 – n17

1020	n11 ∨ n15
1026	NEXT
1020	OPCLA
1020	OPR · 2.1
1020	OPR · 2.2
1009	PAUSED
1013	$S_0 - S_{11}$
1020	SHIN · $\overline{n17}$
EXT.	SNEL
1007	$t_0 - t_3$
1023	$tt_0 - tt_2$
EXT.	TNEL

1007	$TP_0 - TP_1$
1007	TP0 – TP3
1026	WPTP
1014	$Z_0 - Z_{11}$



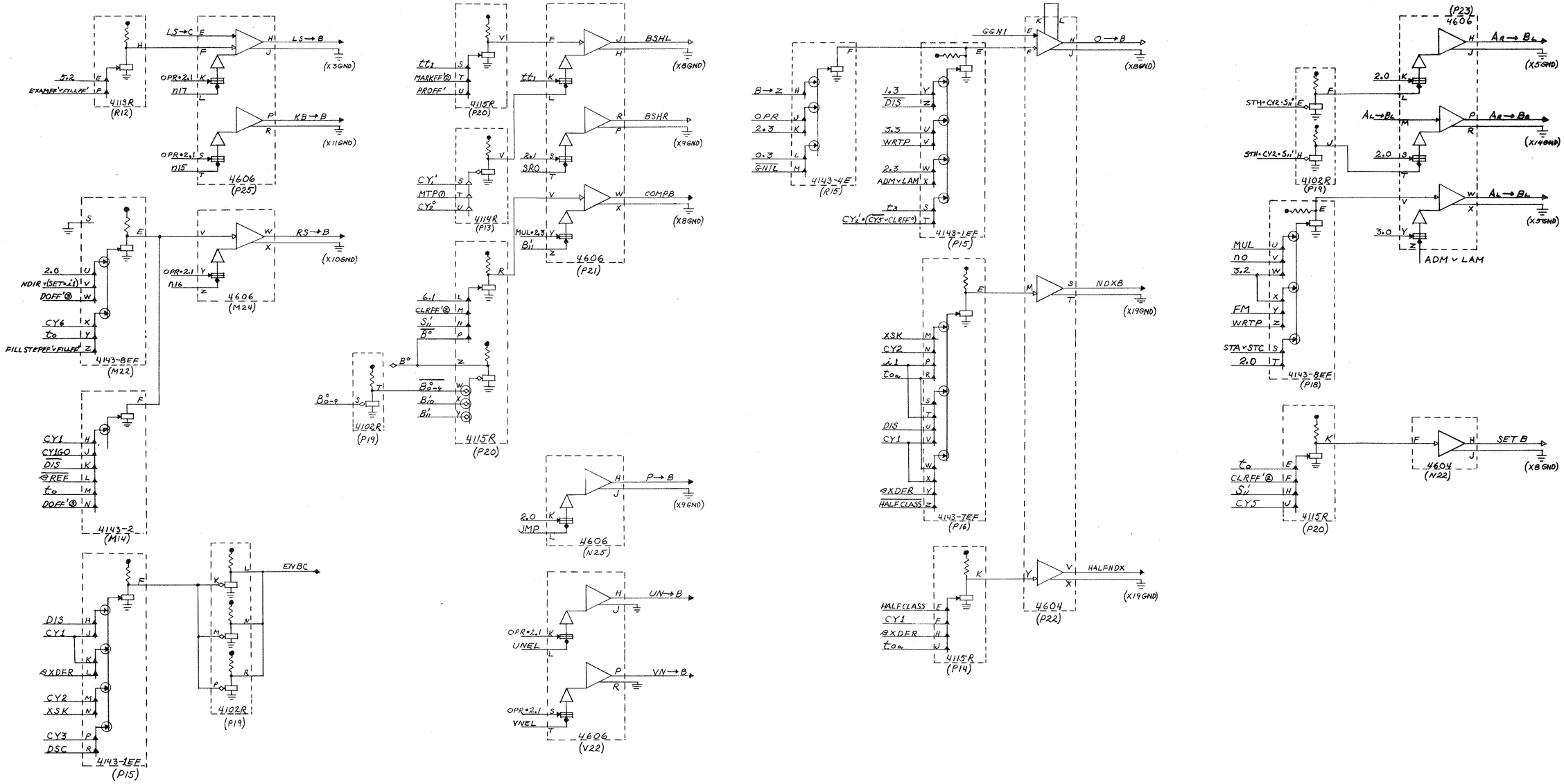
CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			A REGISTER CONTROL LOGIC
ENG.			
DATE	1015		CH.

1007	0.0 — 6.3
1020	ADM ∨ LAM
1014	B → Z
1021	B°_{0-9}
1011	$B_0 - B_{11}$
1020	BREF
1020	BXDFR
1018	CLRFF
1007	$CY_0 - CY_2$
1020	$CY_2' \cdot (\overline{CY5} \vee CLRFF^{\circ})$
1007	CY0 — CY6
1008	CY1GO

1018	DOFF
1018	EXAMFF' ∨ FILLFF'
1018	FILLSTEPFF' ∨ FILLFF'
1024	FM
1008	GGNI
1008	GNIL
1020	HALFCLASS
1012	i0 — i1
1012	INSTRUCTIONS ◇
1020	INSTRUCTIONS ◆
1012	LS → C
1018	MARKFF

1020	MUL · 2.3
1012	n0 — n17
1020	NDIR ∨ (SET · i1)
1020	OPR · 2.1
1018	PROFF
1013	$S_0 - S_{11}$
1020	STA ∨ STC
1020	STH · CY2 · S_{11}'
1020	STH · CY2 · S_{11}
1007	$t_0 - t_3$
1007	t_{0a}
1023	$tt_0 - tt_2$

1026	WRTP



CHANGE LETTER	APP'D BY	DATE	CHANGES

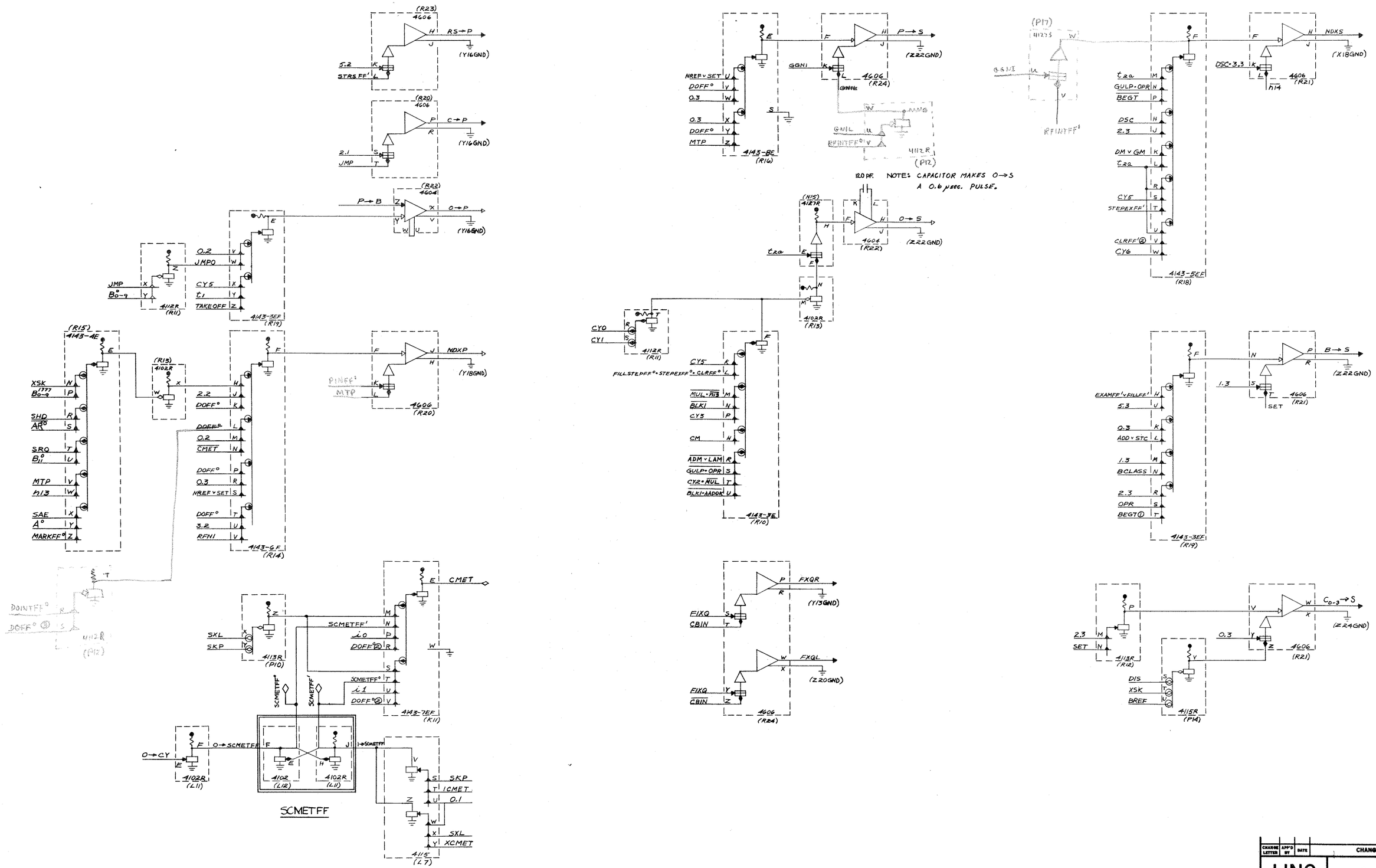
LINC	B REGISTER CONTROL LOGIC	
ENG.		
DATE	1016	CH.

1007	0.0 — 6.3
1008	0 → CY
1021	A^0
1020	ADD ∨ STC
1020	ADM ∨ LAM
1021	AR^0
1011	B_0 — B_{11}
1021	B^{0}_{0-9}
1021	B^{1777}_{0-9}
1020	BCLASS
1020	BEGT ◇
EXT.	BEGT ◆

1026	BLK1
1026	BLK1 · AADOK
1020	BREF
1026	CBIN
1018	CLRFF
1024	CM ◆
1007	CY0 — CY6
1020	CY2 · MUL
1026	DM ∨ GM
1036 DOINTFF	
1018	DOFF
1020	DSC · 3.3
1018	EXAMFF' ∨ FILLFF'

1018	FILLSTEPFF° · STEPEXFF° · CLRFF°
1015	FIXQ
1008	GGN1
1008	GN1L
1020	GULP · OPR
1012	i0 — i1
1021	ICMET
1012	INSTRUCTIONS ◇
1020	INSTRUCTIONS ◆
1018	MARKFF
1008	MUL · n13
1012	n0 — n17

1036 1020	NREF ∨ SET PINFF
1036 1016	P → B RFINTFF
1026	RFN1
1018	STEPEXFF
1018	STRSFF
1007	t_0 — t_3
1019	t_{2a}
1018	TAKEOFF
1021	XCMET



CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC

P AND S CONTROL LOGIC

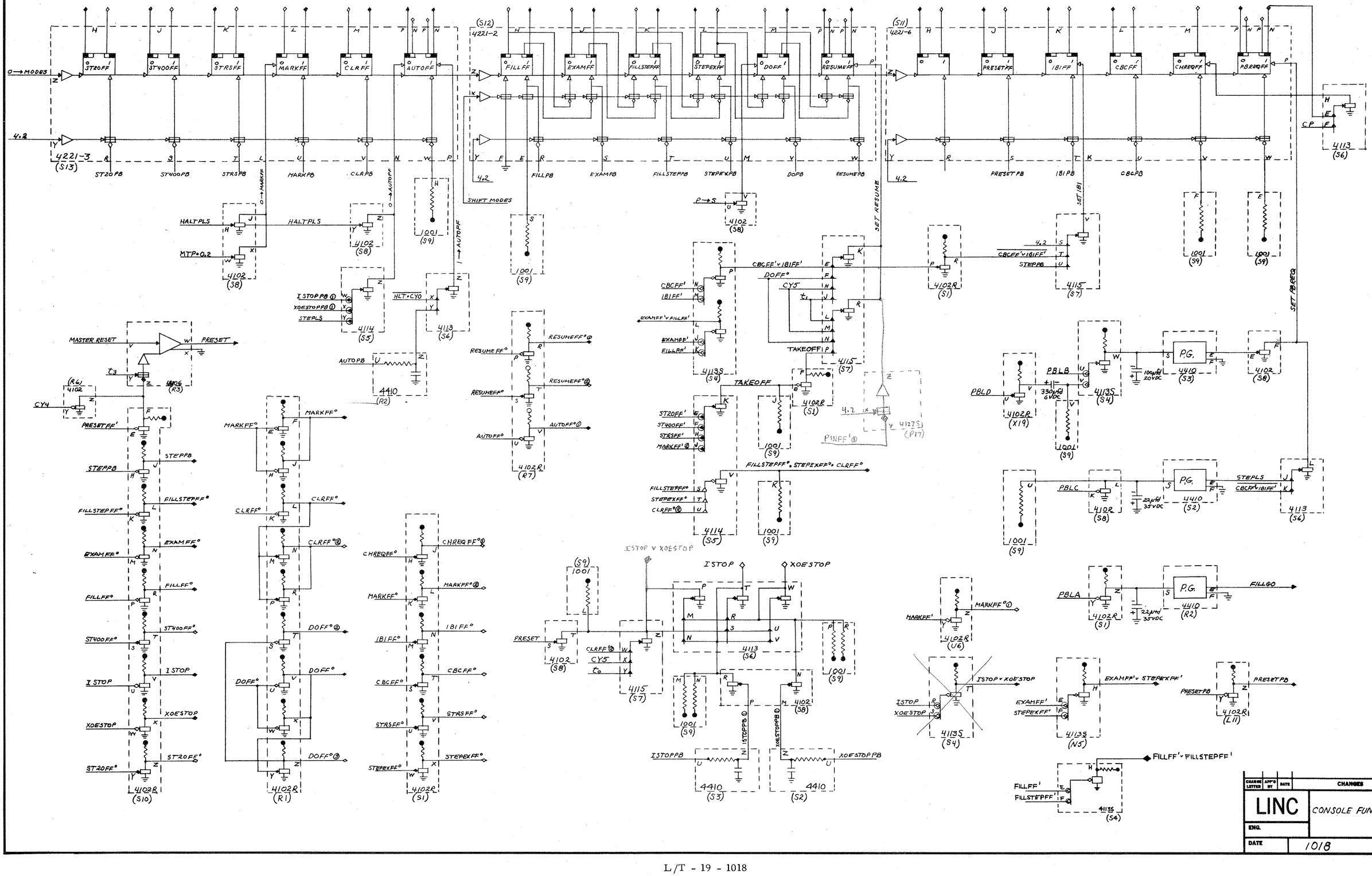
ENG.

DATE 1017 CH.

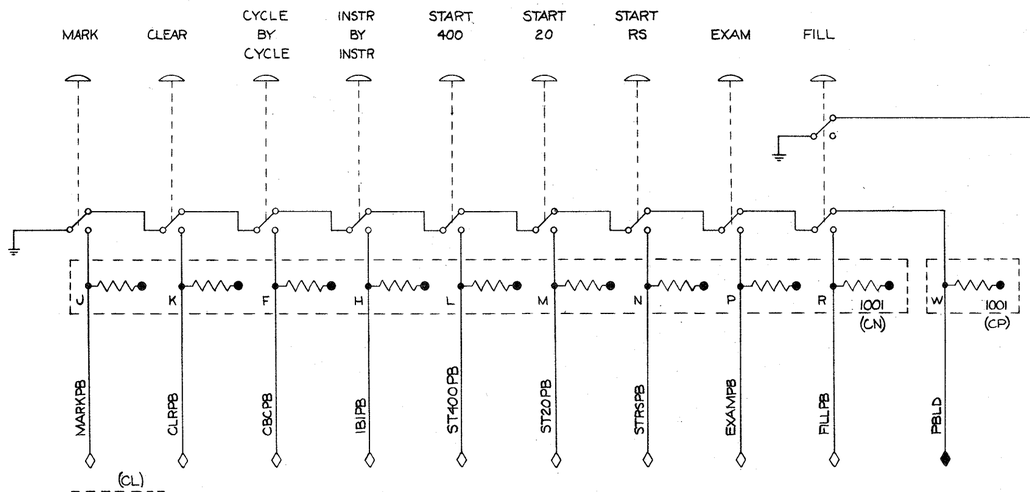
1007	0.0 – 6.3
1008	0 → MODES
EXT.	AUTOPB
EXT.	CBCPB
EXT.	CLRPB
1007	CP
1007	CY0 – CY6
EXT.	DOPB
EXT.	EXAMPB
EXT.	FILLPB
EXT.	FILLSTEPPB
1009	HALTPLS

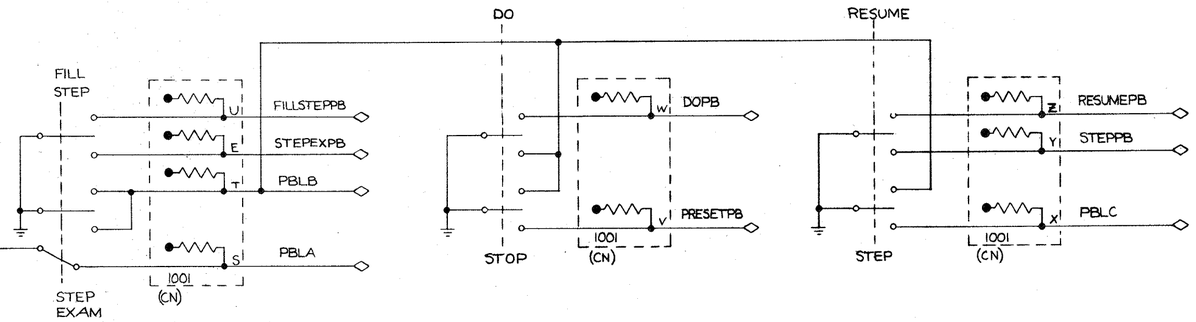
1009	HALT · CY0
EXT.	IBIPB
EXT.	ISTOPPB
EXT.	MARKPB
1007	MASTER RESET
1026	MTP · 0.2
1017	P → S PINFF
EXT.	PRESETPB ◇
EXT.	PBLA – PBLD
EXT.	RESUMEPB
1008	SHIFT MODES
EXT.	ST20PB

EXT.	ST400PB
EXT.	STEPPB ◇
EXT.	STEPEXPB
EXT.	STRSPB
1007	$t_0 - t_3$
EXT.	XOESTOPPB



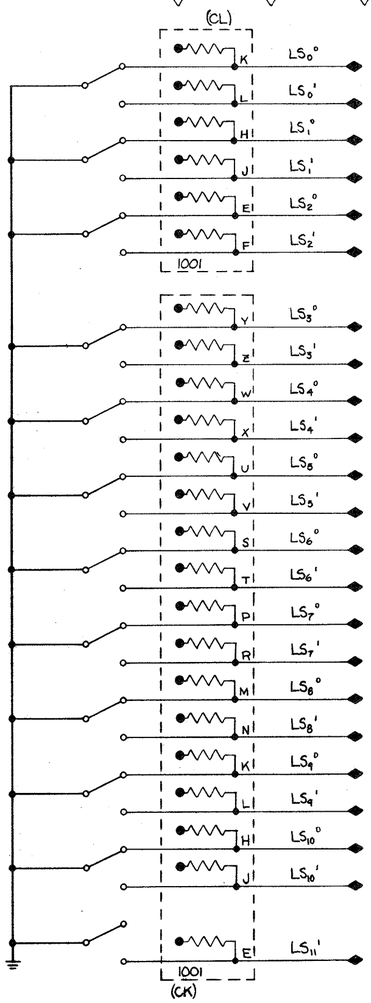
CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			CONSOLE FUNCTIONS
ENG.			
DATE	1018		CH.

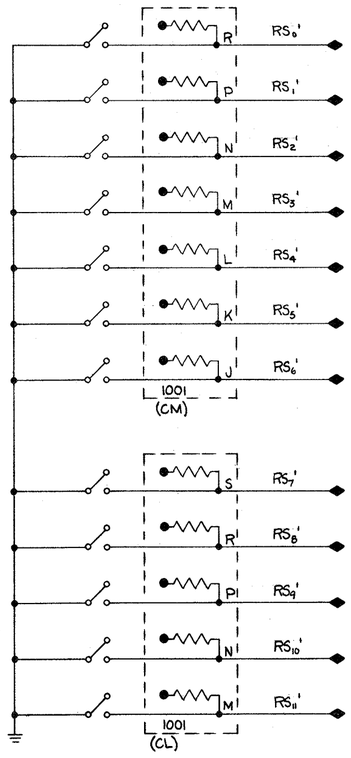


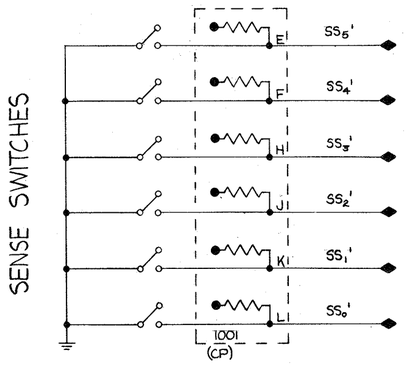


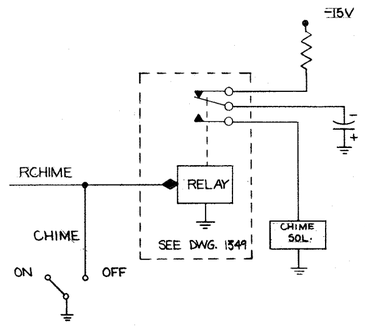
NOTE:

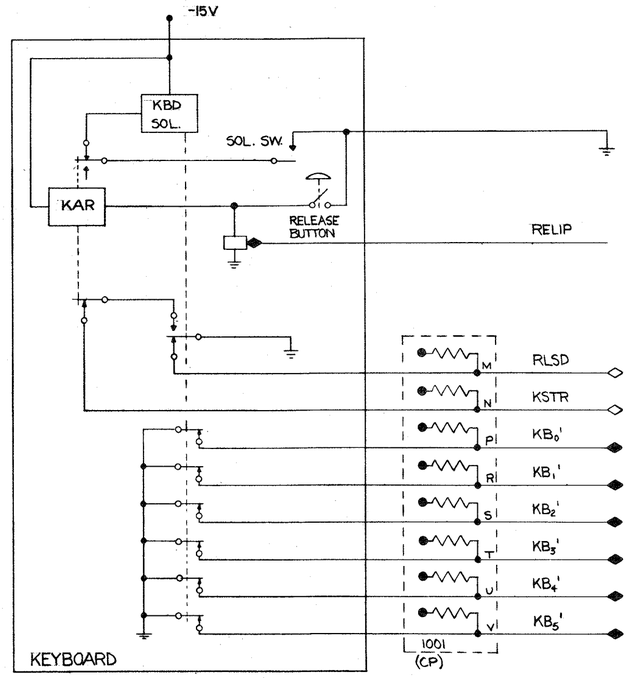
IN THE ABOVE LEVER SWITCHES, THE CONTACT SPRINGS ARE ARRANGED SO THAT THE PBLB LEVEL OCCURS AFTER STEPEXPB, FILLSTEPPB, PRESETPB, DOPB, RESUMEPB; AND PBLC OCCURS AFTER STEPPB. PBLA GOES TO GND ONLY ON RELEASE OF FILLSTEP OR FILL.











KEYBOARD SEQUENCE:

1. WHEN KEY IS STRUCK, 6 BIT CODE APPEARS ON $KB_0 \cdots KB_5$
2. KSTR LINE GOES TO GND.
3. KB → B PULSE READS 6 BIT CODE INTO B AND TURNS ON RELIPFF.
4. RELIP OPERATES KAR, RELEASING KBD SOL.
5. RLSD CLEARS RELIPFF.

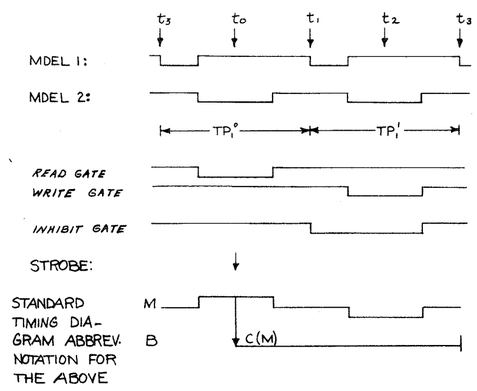
CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC	KEYBOARD AND CONSOLE SWITCH SIGNALS	
ENG.		
DATE	1018A	CH.

1007	0.0 – 6.3
1020	ADM ∨ LAM
1017	B → S
1026	BLK1
1026	BLK1 · C_2^0
1026	(BLK1 · C_2^0) ∨ WRTP
1017	C_{0-3} → S
1012	$C_0 - C_{11}$
1018	CLRFF
1007	CY0 – CY6
1024	DM
1018	DOFF

1018	FILLFF' ∨ FILLSTEPFF'
1024	GM GSNI
1020	INSTRUCTIONS ◆
1008	JMP $\bar{0}$
1020	MOUT ◇
1012	n0 – n17
1017	NDXS
1020	OPR · GULP
1017	P → S
1018	PRESET RFNI
1020	STA ∨ STC
1020	STH · CY2 · S_{11}^0

1020	STH · CY2 · S_{11}'
1009	STOPPED
1007	$t_0 - t_3$
1007	$TP_0 - TP_1$



TYPICAL VALUES

MDEL 1: 0.9 μsec

MDEL 2: 1.8 μsec

CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC

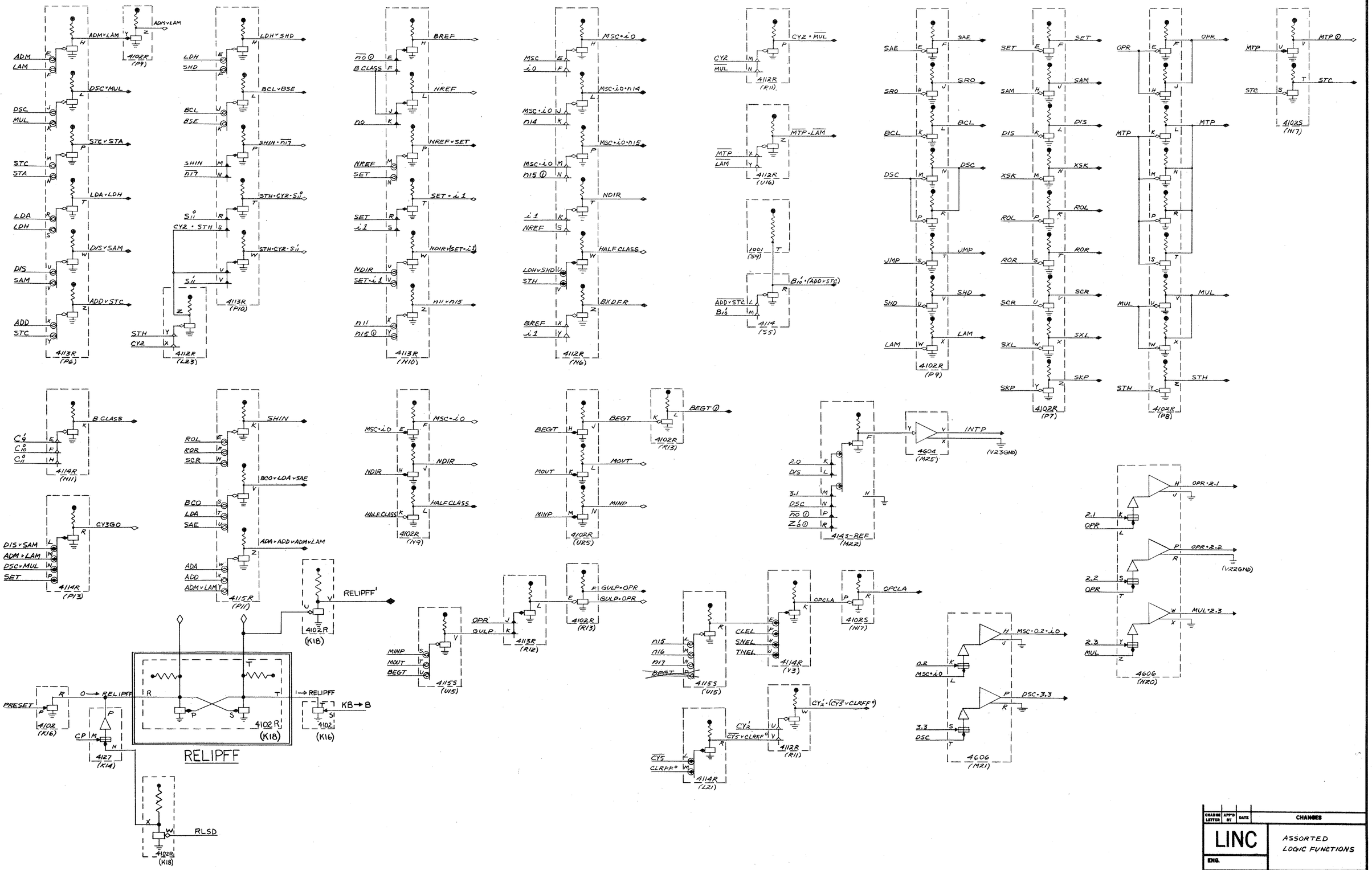
ENG.

DATE 1019 CH.

MEMORY CONTROL LOGIC

1007	0.0 – 6.3
EXT.	BEGT ◆
1012	$C_0 - C_{11}$
EXT.	CLEL ◆
1007	CP
1007	$CY_0 - CY_2$
1007	CY0 – CY6
1012	i0 – i1
1012	INSTRUCTIONS ☆
1016	KB → B
EXT.	MINP ◆
EXT.	MOUT ◆

1012	n0 – n17
1018	PRESET
EXT.	RLSD ☆
1013	$S_0 - S_{11}$
EXT.	SNEL ◆
EXT.	TNEL ◆
1014	$Z_0 - Z_{11}$



CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC

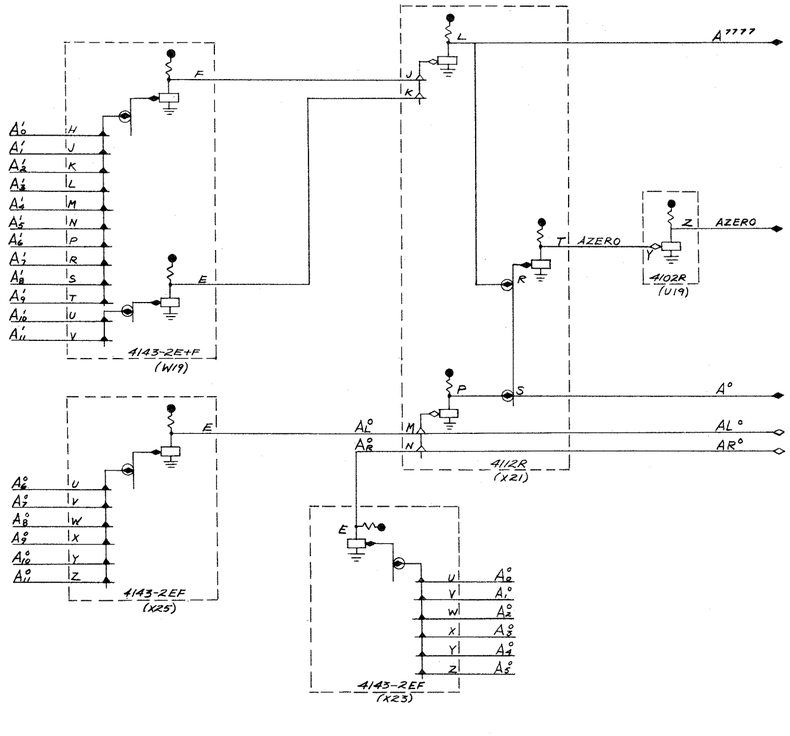
ENG.

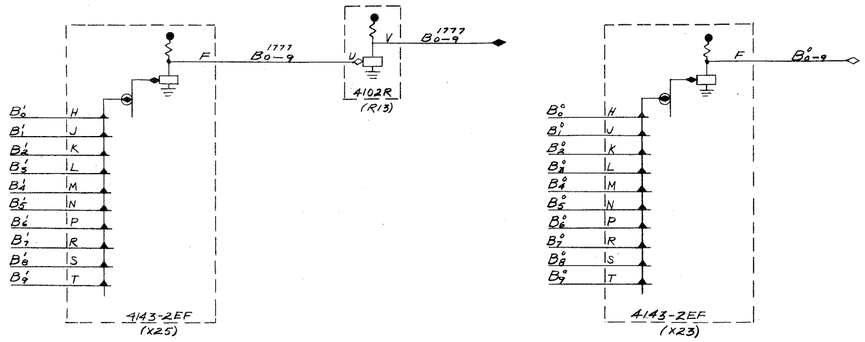
ASSORTED LOGIC FUNCTIONS

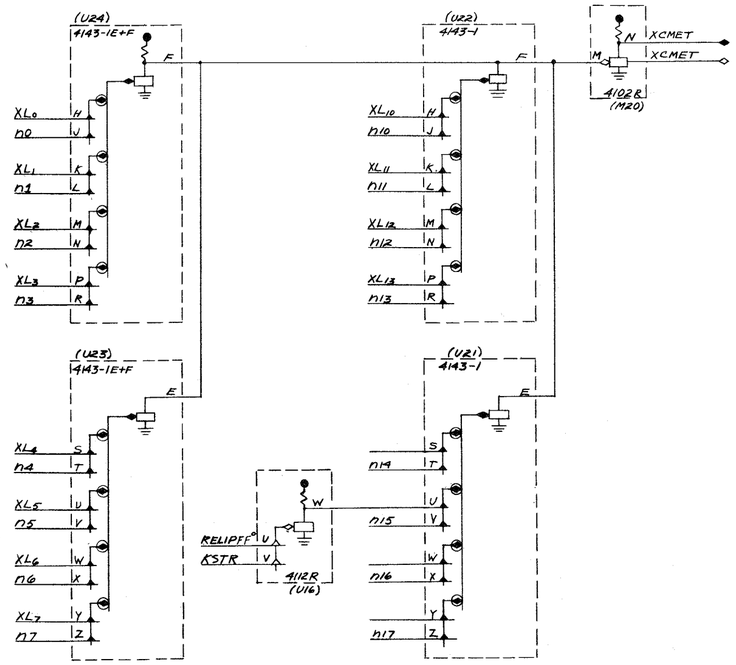
DATE 1020 CH.

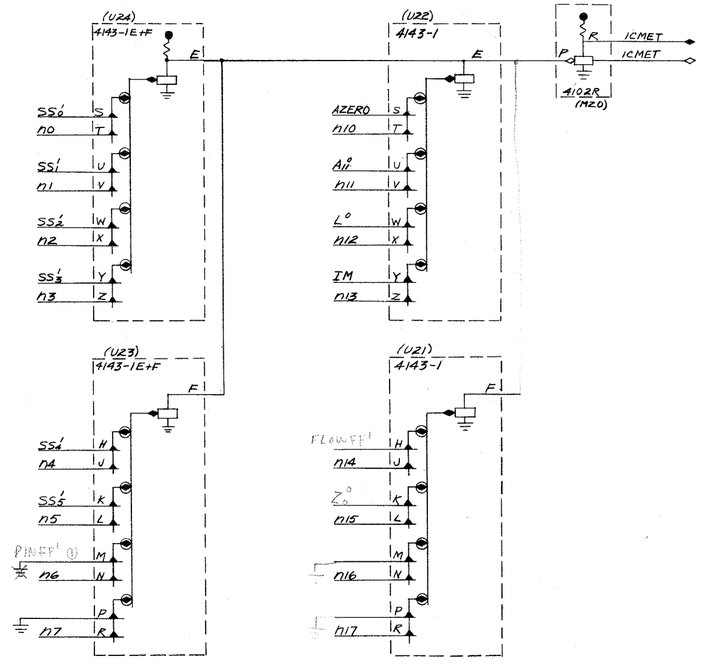
1010	$A_0 - A_{11}$
1011	$B_0 - B_{11}$
1007	$CY0 - CY6$
1036	FLOFF
1024	IM
1018	ISTOP
EXT.	KSTR Φ
1014	L
EXT.	$LS_0 - LS_{11}$
1012	$n0 - n17$
1036	PINFF
1020	RELIPFF
1013	$S_0 - S_{11}$
EXT.	$SS_0 - SS_5$

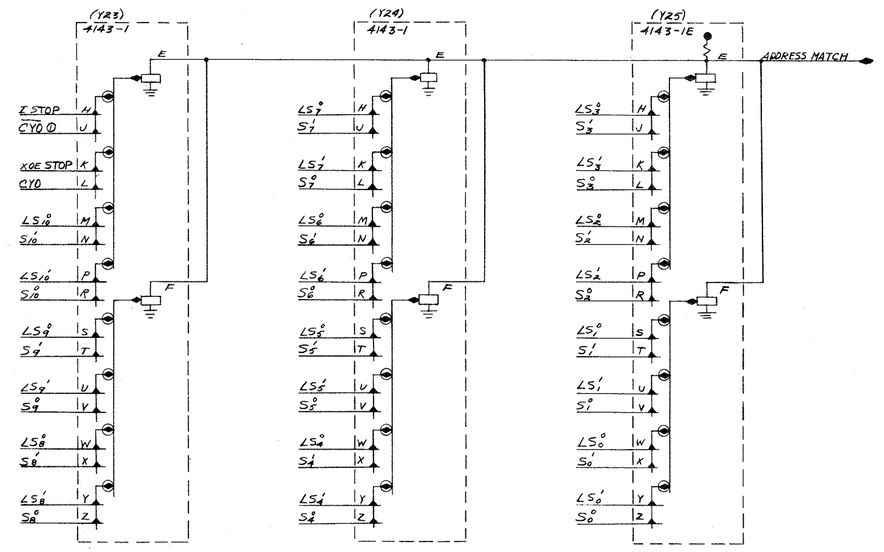
EXT.	$XL_0 - XL_{13}$
1018	XOESTOP
1014	Z_0









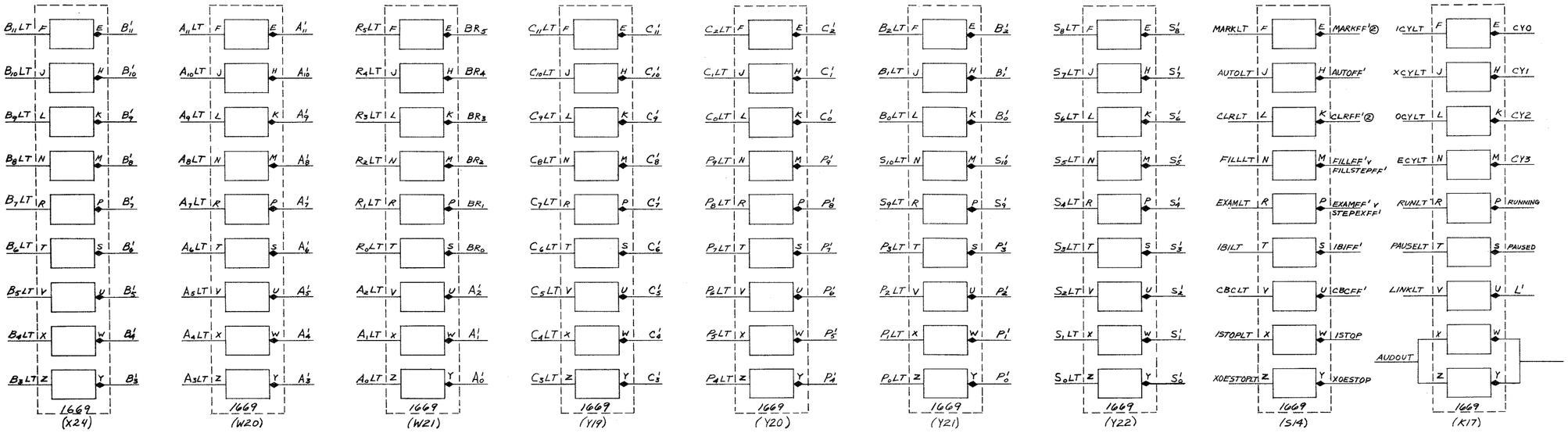


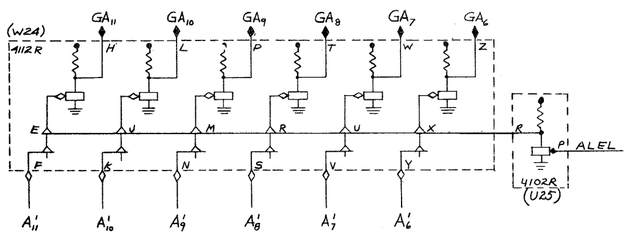
CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			SENSE NETS
ENG.			
DATE	1021		CH.

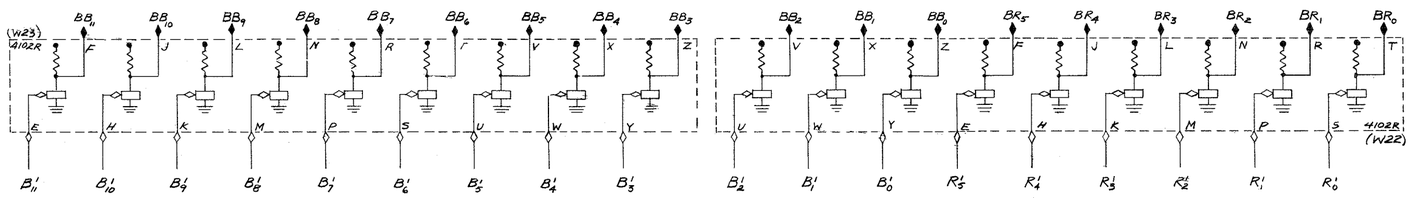
1007	0.0 – 6.3
1010	$A_0 - A_{11}$
EXT.	ALEL ◆
EXT.	AREL ◆
1007	ATPL
1018	AUTOFF
1011	$B_0 - B_{11}$
1009	BEOP
1012	$C_0 - C_{11}$
1018	CBCFF
1018	CLRFF
1007	CP

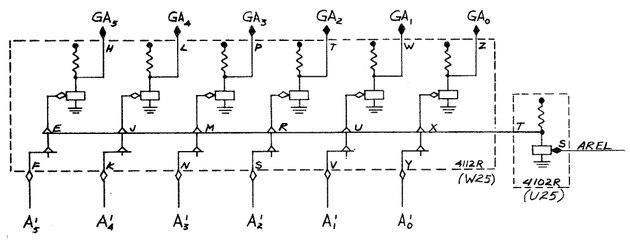
1007	CY0 – CY6 DOINTFF
1018	EXAMFF' v STEPEXFF'
1018	FILLFF' v FILLSTEPFF'
1008	GGNI
1018	IBIFF
1020	INSTRUCTIONS ◆
1020	INTP
1018	ISTOP
1014	L
1018	MARKFF
1025	$MOTN_0 - MOTN_1$
1012	n0 – n17

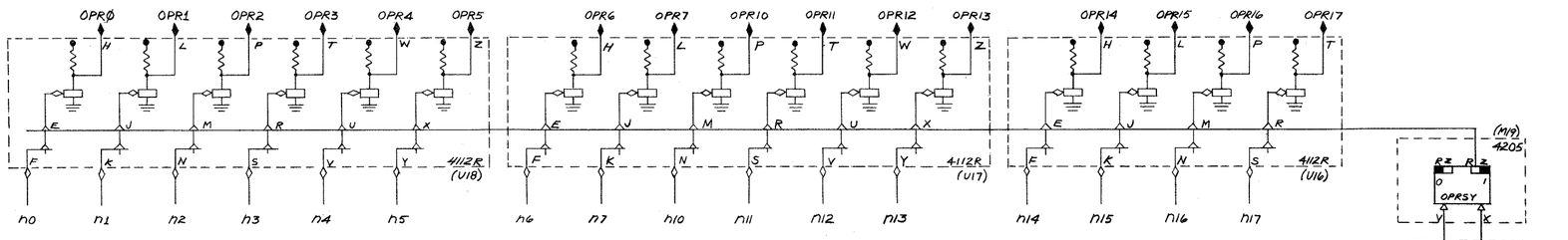
1020	OPR · 2.1
1020	OPR · 2.2
1013	$P_0 - P_7$
1009	PAUSED
1018	PRESET
1014	$R_0 - R_5$
1009	RUNNING
1013	$S_0 - S_{11}$
1025	U
1018	XOESTOP

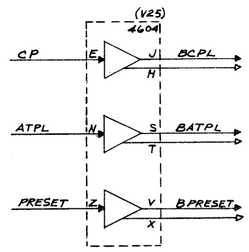


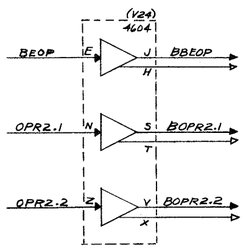


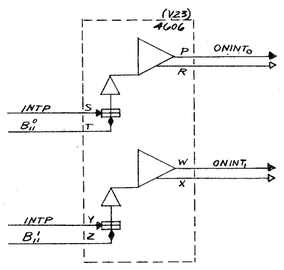


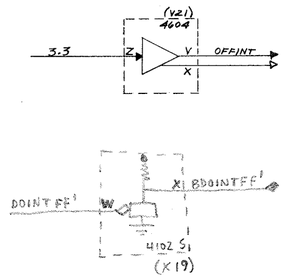


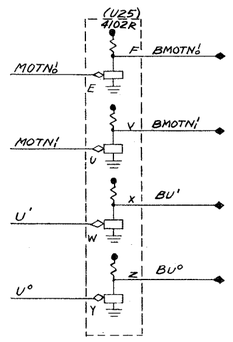


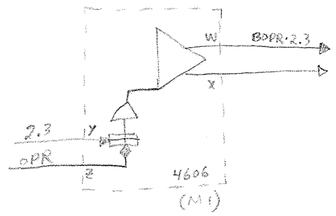






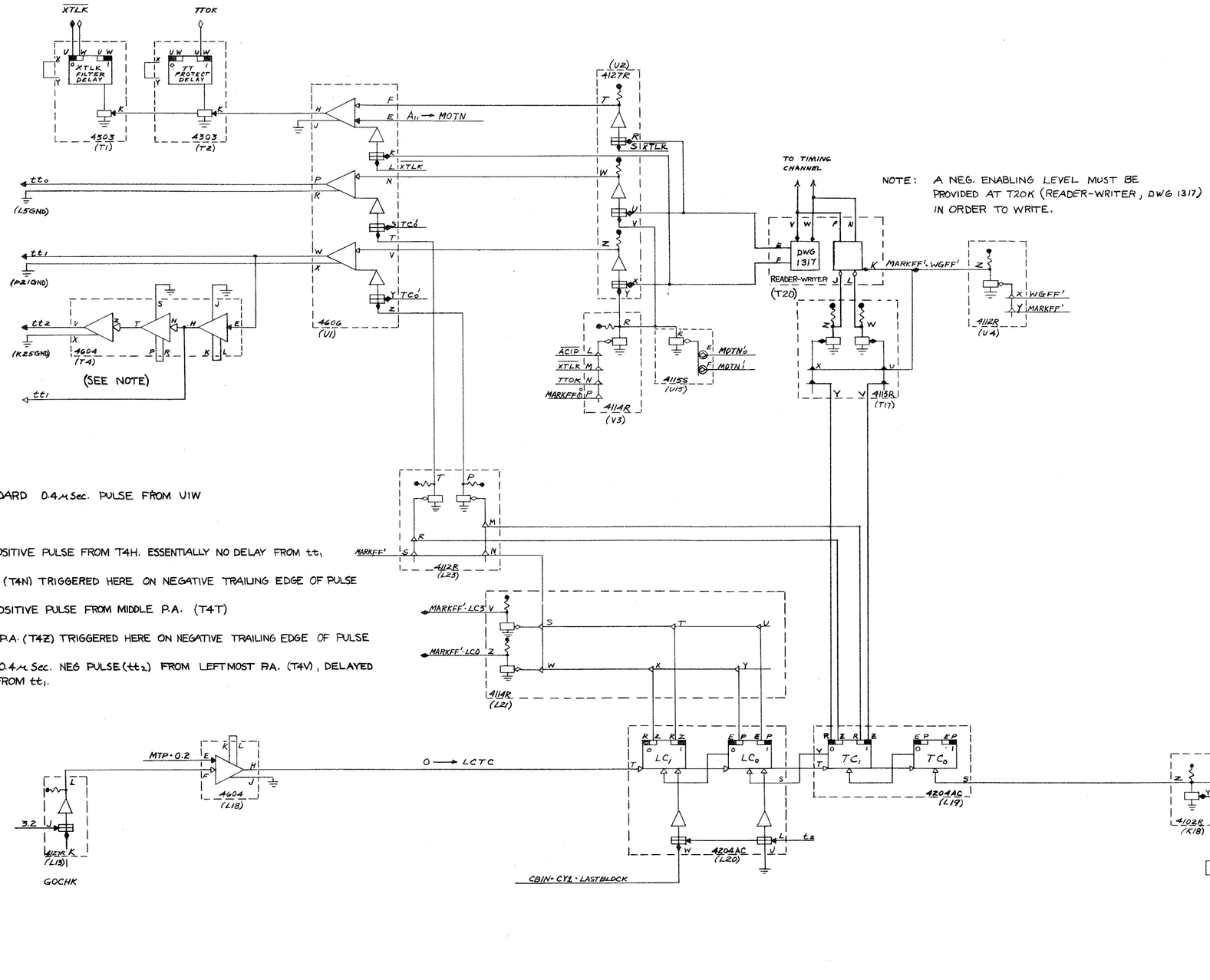






CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			OUTPUT DRIVERS AND BUFFERS
ENG.			
DATE	1022		CH.

1007	0.0 – 6.3
1025	$A_{11} \rightarrow$ MOTN
1025	ACIP
1026	CBIN · CY1 · LAST BLOCK
1018	MARKFF
1026	MARKUP
1025	$MOTN_0 - MOTN_1$
1026	MTP · 0.2
1007	$t_0 - t_3$
1024	WGFF
1026	NEXT
1026	GOCHK



CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC

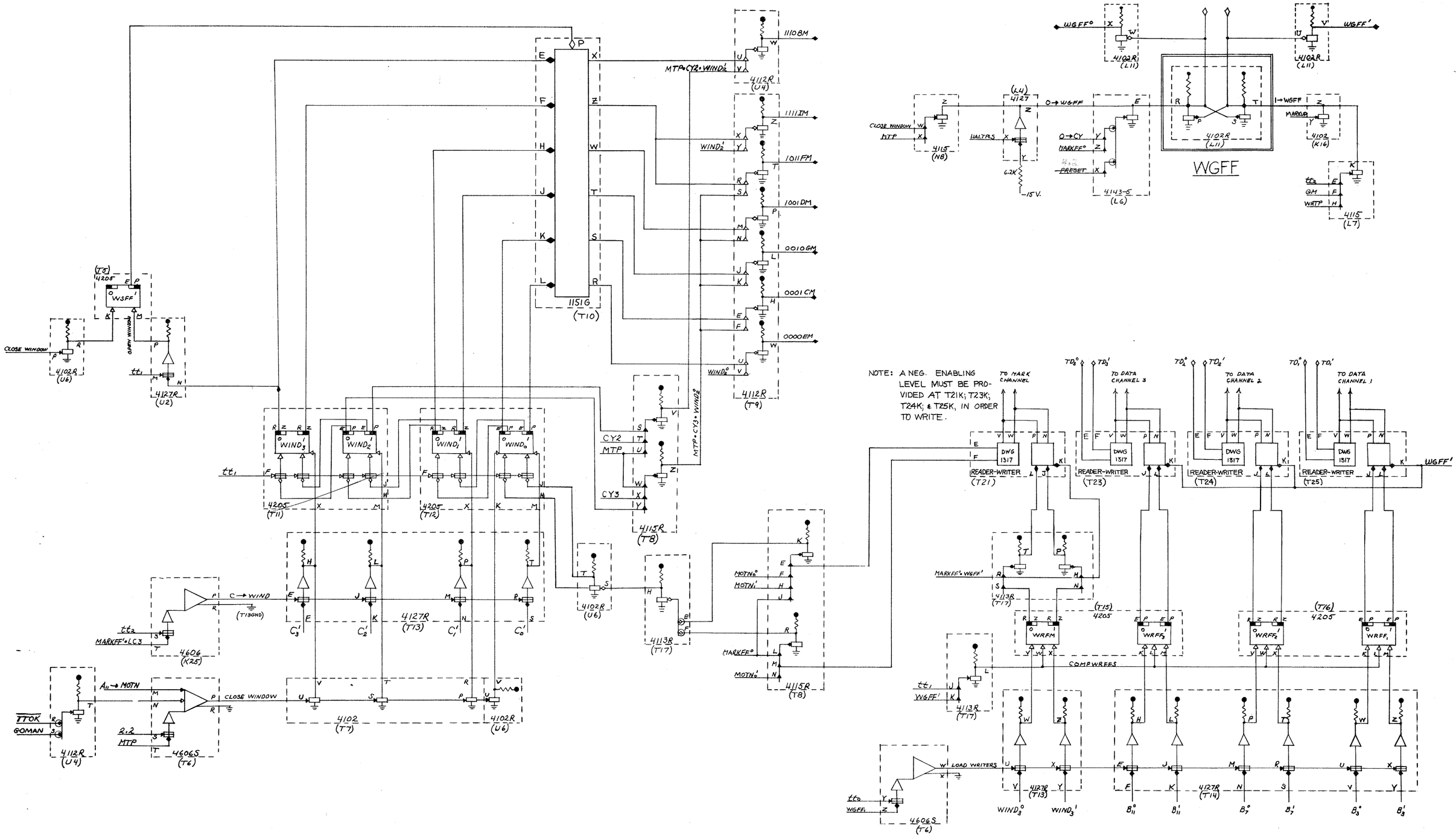
TAPE TIMING CHANNEL LOGIC

ENG.

DATE 1023 CH.

1007	0.0 – 6.3
1008	0 → CT
1025	A_{11} → MOTN
1011	$B_0 - B_{11}$
1012	$C_0 - C_{11}$
1025	GOMAN
1009	HALTPLS
1020	INSTRUCTIONS ♦
1018	MARKFF
1023	MARKFF'·LC3
1023	MARKFF'·WGFF'
1026	MARKUP

1025	$MOTN_0 - MOTN_1$
1018	PRESET
1023	$tt_0 - tt_2$
1023	TTOK
1026	WRTP



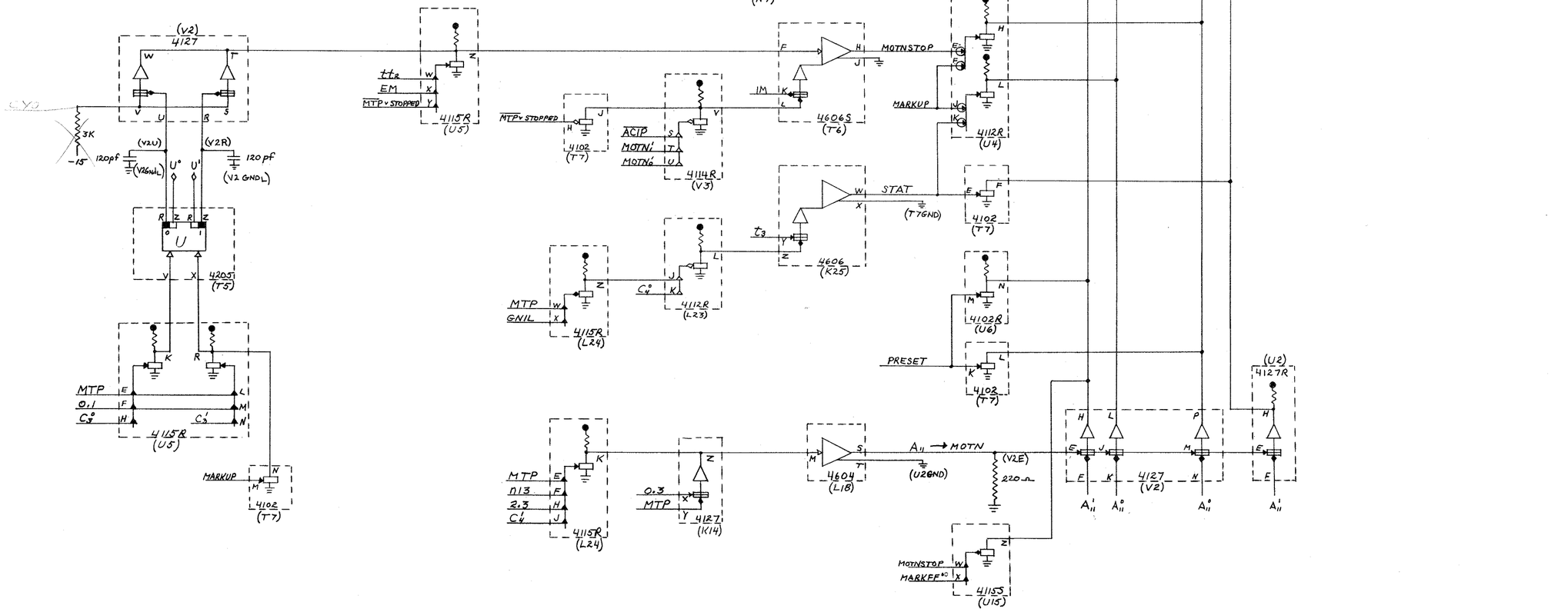
CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC	TAPE LOGIC, MARK & DATA CHANNELS	
ENG.		
DATE	1024	CH.

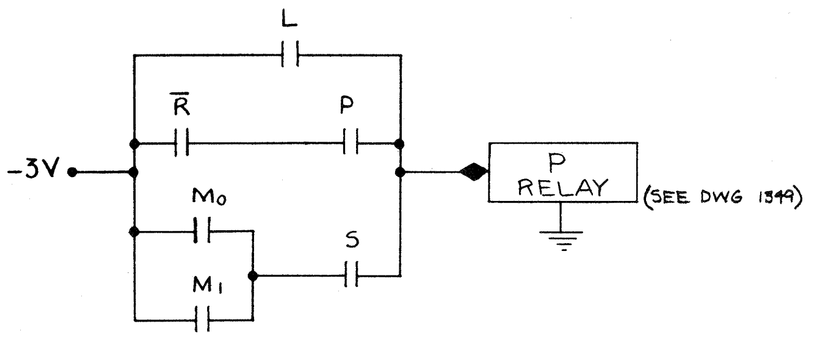
1007	0.0 – 6.3
1010	$A_0 - A_{11}$
1012	$C_0 - C_{11}$
1024	EM
1008	GNIL
1024	IM
1020	INSTRUCTIONS ◆
1018	MARKFF
1026	MARKUP
1012	m0 – m17
1018	PRESET
1009	STOPPED

1007	$t_0 - t_3$
1023	$tt_0 - tt_2$

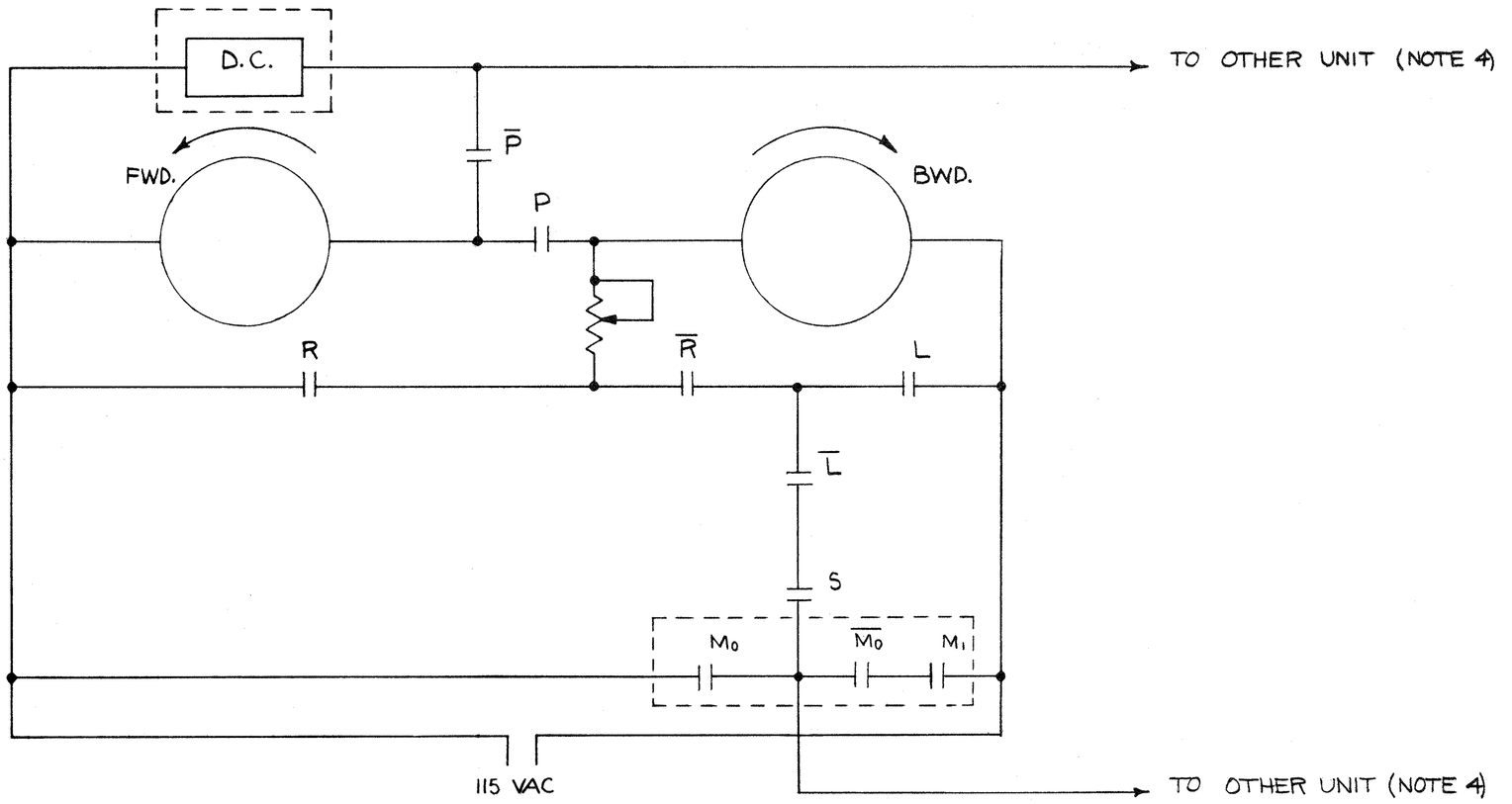
00 STOP
01 BAWD
10 FOWD
11 TURN ARND



CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			TAPE MOTION CONTROL LOGIC
ENG.			
DATE	1025		CH.



POWER RELAY (P) LATCHING CONTROL (NOTE 1)



1. POWER RELAY (P) WHENEVER A CLOSED PATH CONNECTS -3 VOLTS TO THE P RELAY CONTROL, THE P CONTACTS CLOSE. ONCE CLOSED, THEY CAN BE OPENED AGAIN ONLY BY OPENING THE $\overline{R}$ CONTACT, i.e. BY PRESSING THE R BUTTON.
2. CONTACT NOTATION: $\dashv\vdash^{X}$ A CONTACT WHICH IS CLOSED WHEN CONDITION "X" EXISTS.
   $\dashv\vdash^{\overline{X}}$ A CONTACT WHICH IS OPEN WHEN CONDITION "X" EXISTS.
3. "L" = LEFT BUTTON
   "R" = RIGHT BUTTON
4. ONLY ONE OF THE TWO UNITS IS SHOWN, AS THEY ARE ESSENTIALLY IDENTICAL. DOTTED LINES INDICATE SECTIONS SHARED BY THE TWO UNITS, i.e. THERE IS BUT ONE D.C. SUPPLY AND ONE PAIR OF MOTION RELAYS. IN ADDITION TO THE 115 VOLT LINE, THE TWO INDICATED LINES ARE CONNECTED TO THE OTHER UNIT. UNITS OPERATE INDEPENDENTLY SO FAR AS PUSH BUTTONS ARE CONCERNED. EACH UNIT HAS A SELECTION RELAY (S), WHICH, WHEN ACTIVATED, CONNECTS CONTROL TO THE M_0 AND M_1 RELAYS. THESE MOTION RELAYS ARE CONTROLLED BY BMOTN$_0$ ◆ AND BMOTN$_1$ ◆ LEVELS DERIVED FROM THE MOTN$_0$ AND MOTN$_1$ FLIP-FLOPS IN THE CABINET. (SEE DWG. 1025) NOTE THAT THE SUBSCRIPTS DO NOT REFER TO THE UNIT, i.e. BOTH FLIP-FLOPS ARE REQUIRED TO CONTROL THE MOTION OF EITHER UNIT SELECTED. ONLY ONE UNIT WILL HAVE ITS SELECTION RELAY ACTIVATED AT ANY ONE TIME.
   THE VARIOUS STATES ARE:

MOTN$_1$	MOTN$_0$	LEFT MOTOR	RIGHT MOTOR	RESULTANT MOTION
0	0	HALF VOLTAGE	HALF VOLTAGE	STOP
0	1	SHUNTED	FULL VOLTAGE	BACKWARD
1	0	FULL VOLTAGE	SHUNTED	FORWARD
1	1	SHUNTED	FULL VOLTAGE	BACKWARD

5. THE VARIABLE RESISTOR ACTS AS A VOLTAGE DIVIDER SO THAT RATHER THAN COMPLETELY SHUNTING ONE MOTOR, AND APPLYING FULL VOLTAGE TO THE OTHER, A SMALL PART OF THE VOLTAGE MAY BE APPLIED TO THE TRAILING MOTOR. THIS PERMITS PROPER ADJUSTMENT OF TAPE TENSION.

L/T - 28 - 1025A

LINC

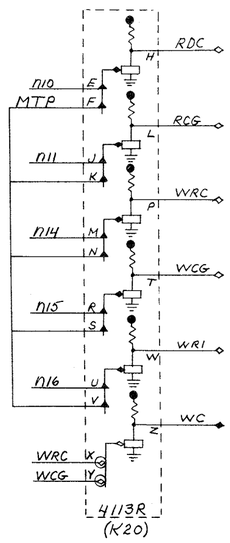
TAPE UNITS
MOTOR POWER
CONTROL NETWORK

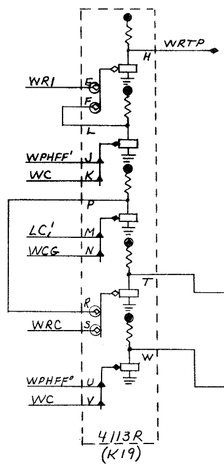
DWG. 1025A

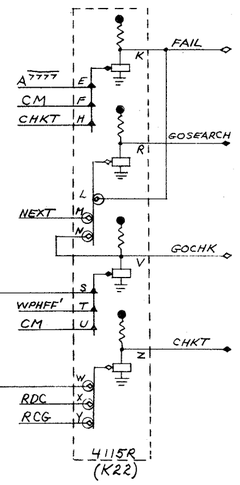
DATE | CHANGES | CHANGE LETTER | APP'D BY | DATE | CH.

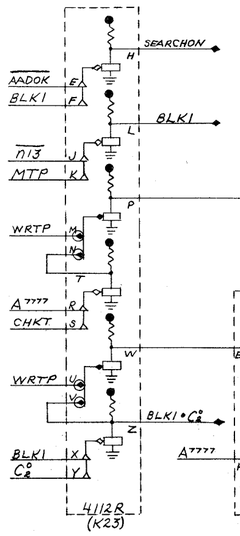
1007	0.0 - 6.3
1008	0 → CY
1021	A^{7777} ◆
1024	BM ◆
1012	$C_0 - C_{11}$
1024	CM ◆
1007	CY0 - CY6
1024	DM
1024	FM
1012	INSTRUCTIONS ◆
1023	$LC_0 - LC_1$
1025	$MOTN_0 - MOTN_1$

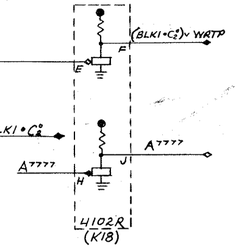
1012	n0 - n17
1018	PRESET
1007	$t_0 - t_3$
1023	$tt_0 - tt_2$

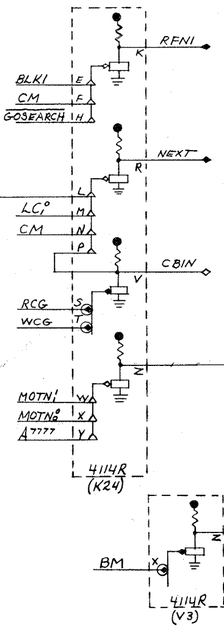


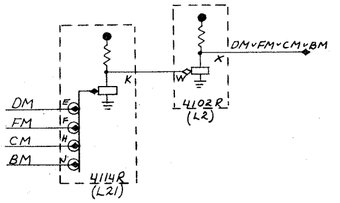


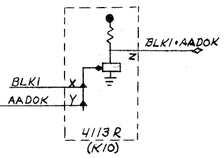


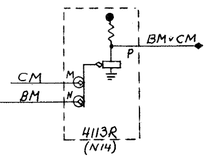


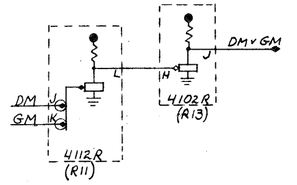


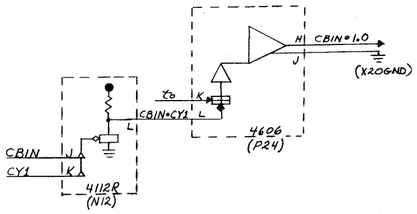


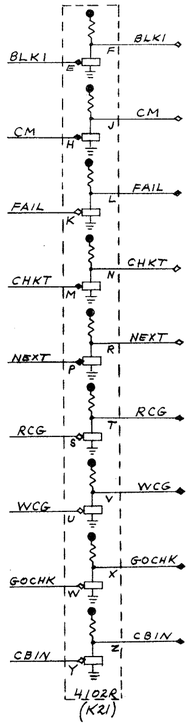


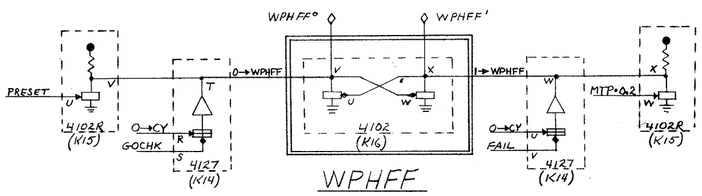


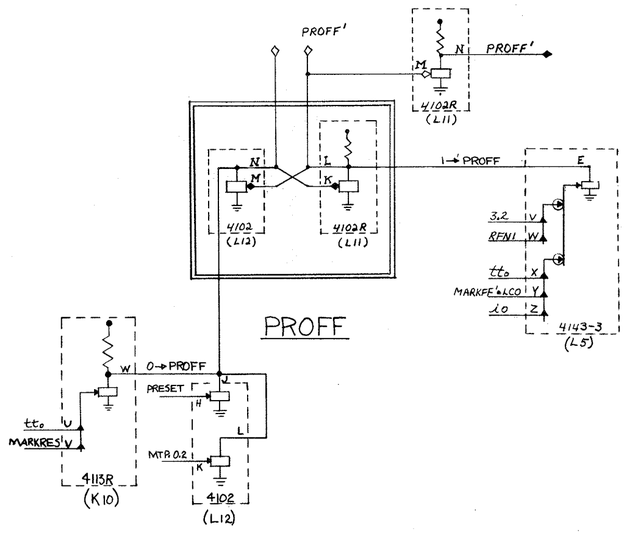


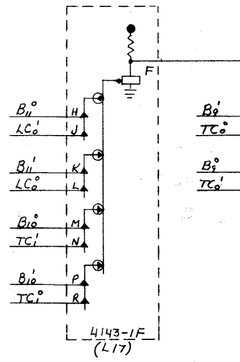


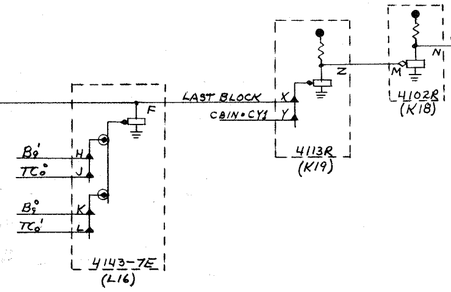


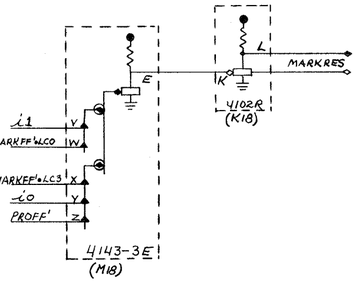


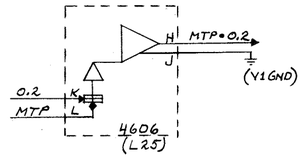


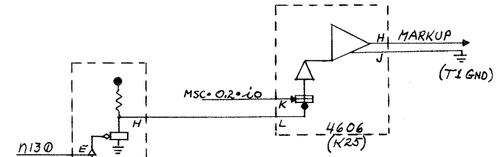








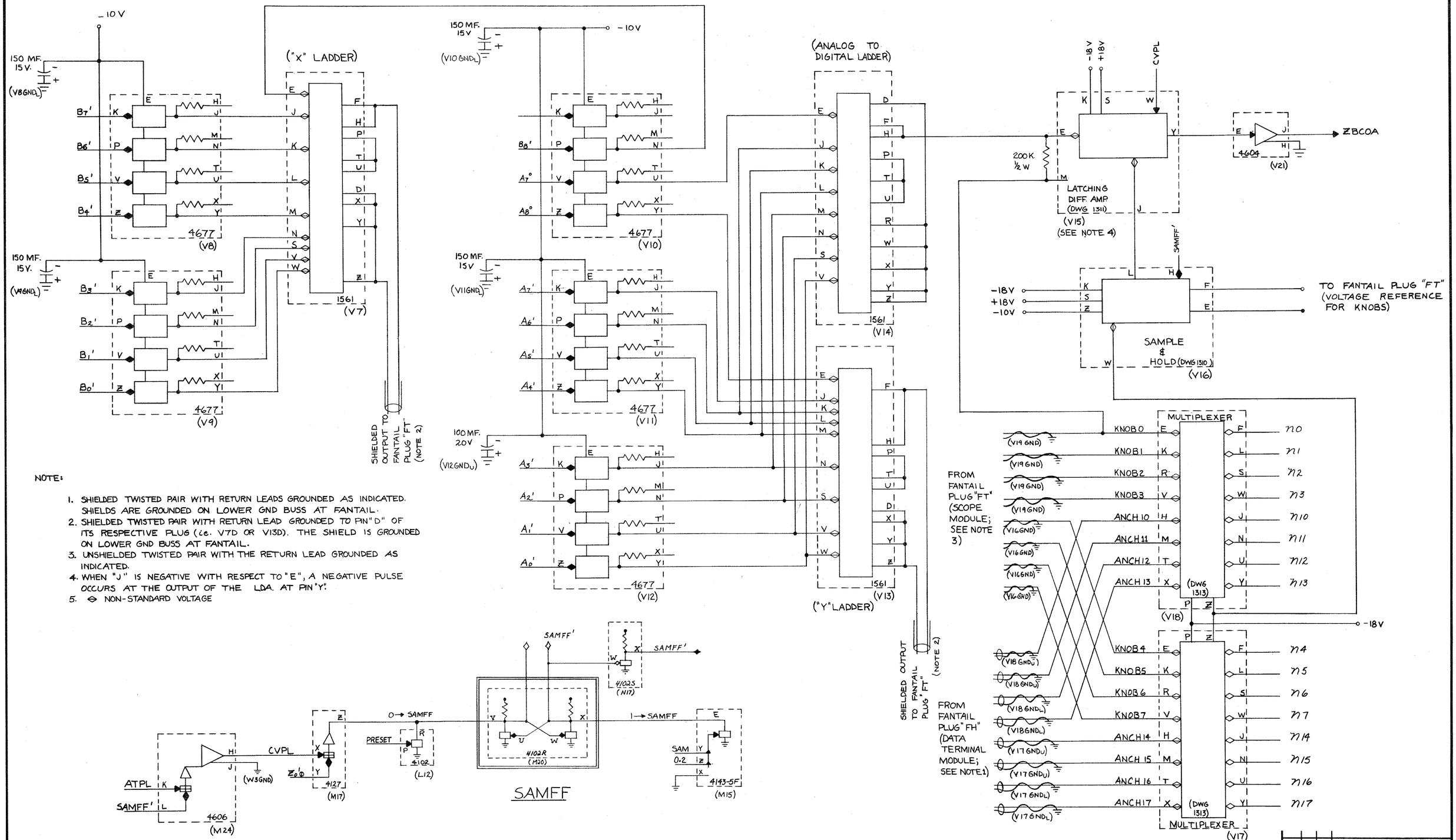




CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC	ASSORTED MAG TAPE LOGIC FUNCTIONS	
ENG.		
DATE	1026	CH.

1007	0.0 - 6.3
1010	$A_0 - A_{11}$
EXT.	ANCH 10 - ANCH 17
1007	ATPL
1011	$B_0 - B_{11}$
1020	INSTRUCTIONS ◆
EXT.	KNOB 0 — KNOB 7
1012	M0 - M17
1018	PRESET
1014	$Z_0 - Z_{11}$



NOTE:

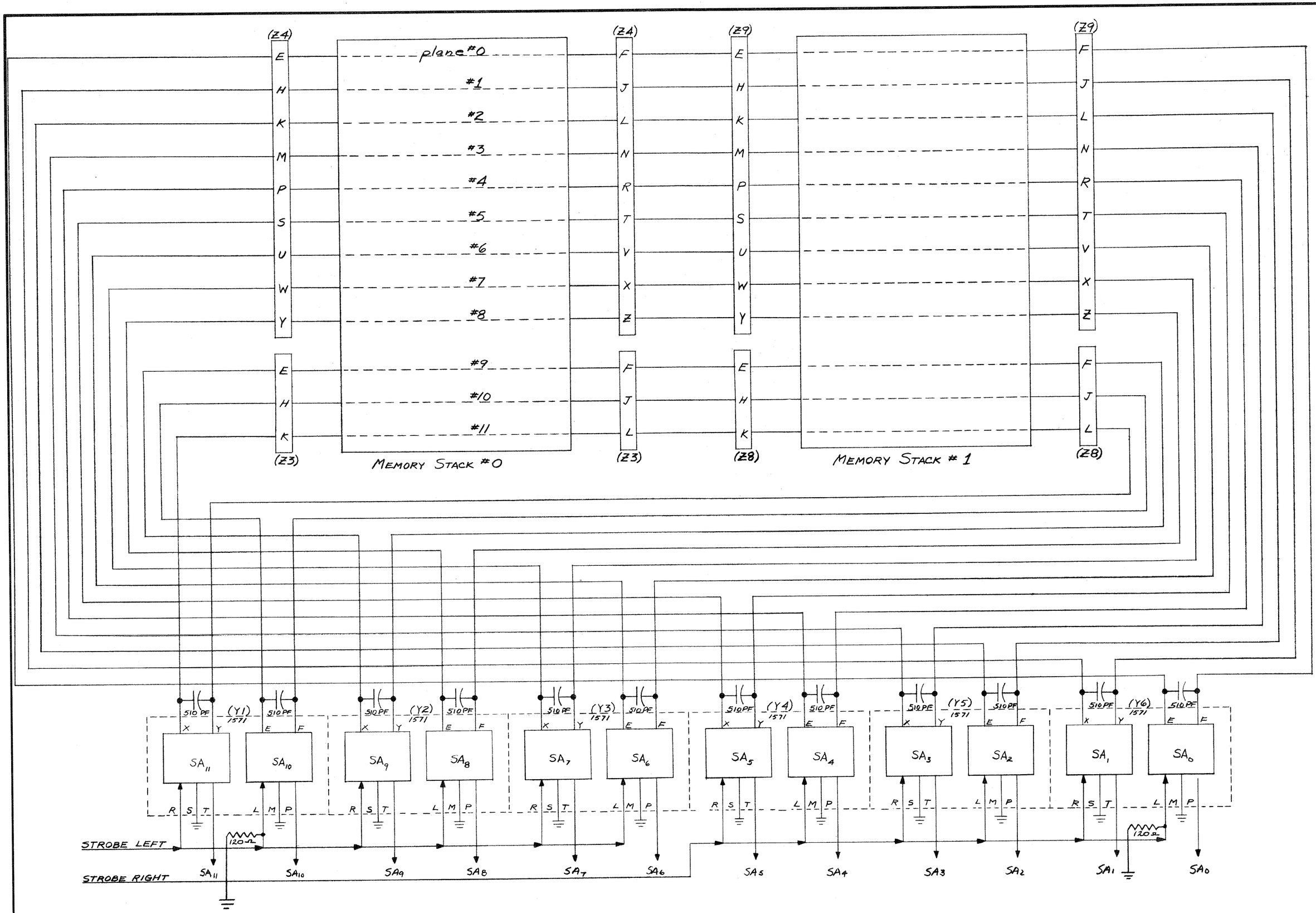
1. SHIELDED TWISTED PAIR WITH RETURN LEADS GROUNDED AS INDICATED. SHIELDS ARE GROUNDED ON LOWER GND BUSS AT FANTAIL.
2. SHIELDED TWISTED PAIR WITH RETURN LEAD GROUNDED TO PIN "D" OF ITS RESPECTIVE PLUG (i.e. V7D OR V13D). THE SHIELD IS GROUNDED ON LOWER GND BUSS AT FANTAIL.
3. UNSHIELDED TWISTED PAIR WITH THE RETURN LEAD GROUNDED AS INDICATED.
4. WHEN "J" IS NEGATIVE WITH RESPECT TO "E", A NEGATIVE PULSE OCCURS AT THE OUTPUT OF THE LDA. AT PIN "Y".
5. ◇ NON-STANDARD VOLTAGE

CHANGE LETTER	APP'D BY	DATE	CHANGES

LINC — ANALOG DIGITAL SYSTEM

ENG.

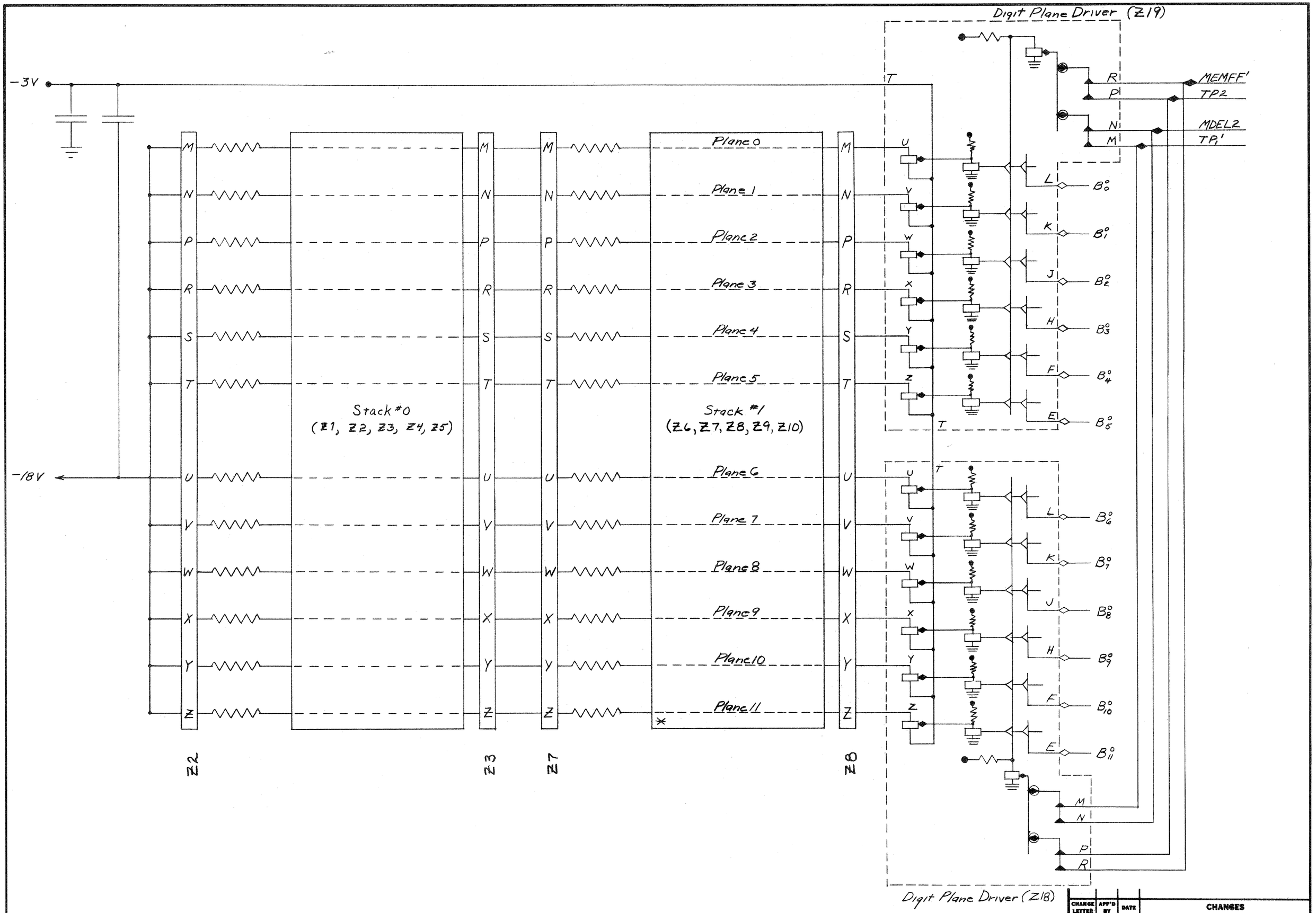
DATE — 1027 — CH.



NOTE:

1. A BY PASS CAPACITOR, (100 MFD, 20 V, 20%, SPRAGUE # 150D) IS ATTACHED BETWEEN Y2C (-15 VOLTS) AND Y4GNDU.
2. SLICE LEVELS ARE AVAILABLE ON SENSE AMPLIFIER PINS "U" AND "K" (FOR UPPER AND LOWER AMPS.)
3. EACH SENSE AMPLIFIER INPUT, (PINS X, Y, E, F) HAS A 120Ω RESISTOR TO GROUND.

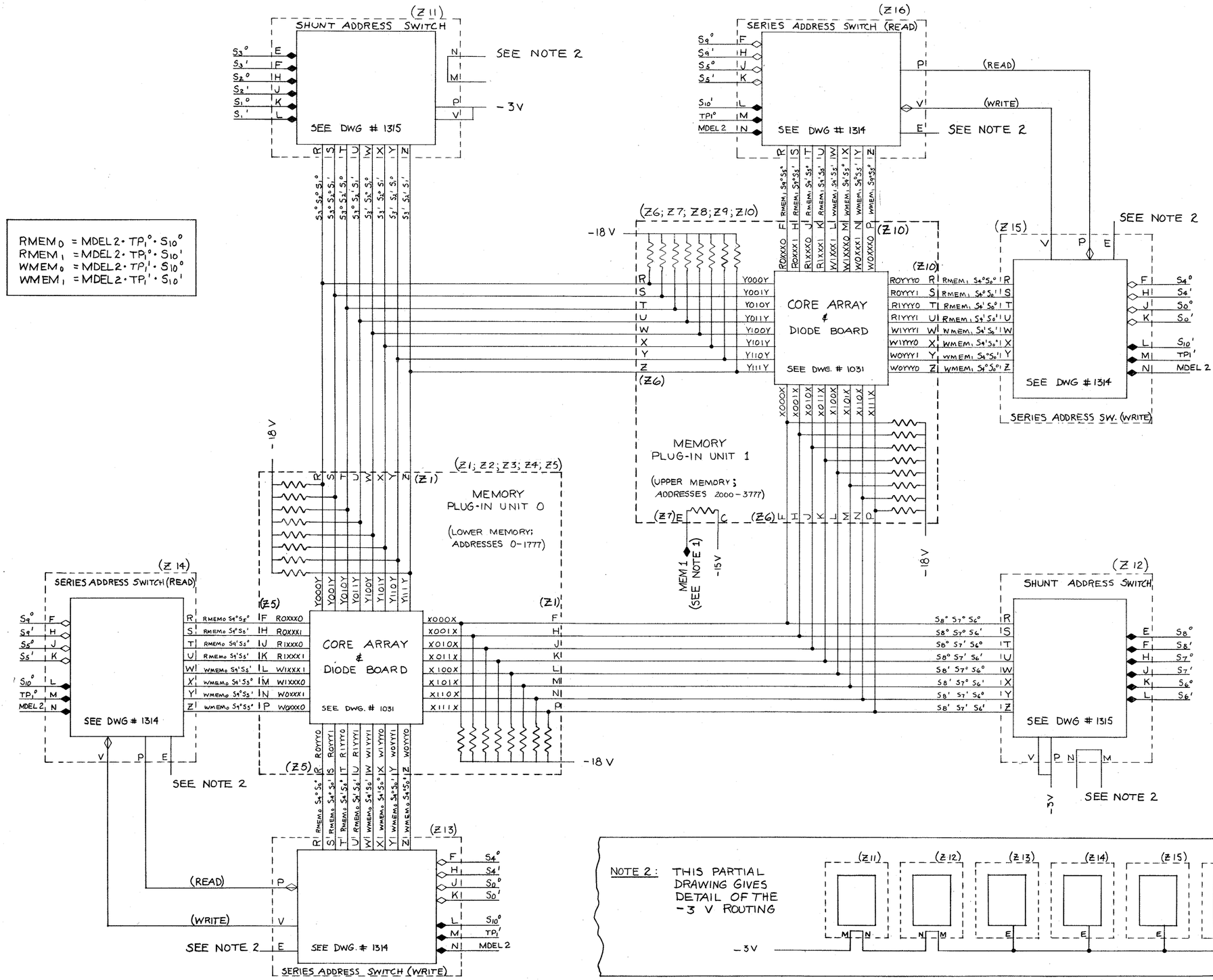
CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			MEMORY SENSE LOGIC
ENG.			
DATE	1028		CH.



CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			MEMORY DIGIT PLANE CONNECTIONS
ENG.			
DATE	1029		CH.

1019	MDEL 2
1013	$S_0 - S_{11}$
1007	$TP_0 - TP_1$

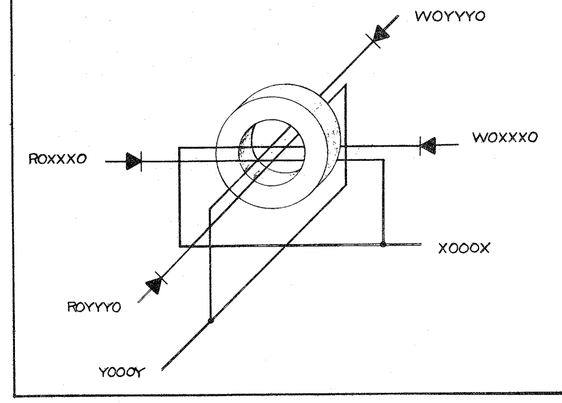
$RMEM_0 = MDEL2 \cdot TP_1^0 \cdot S_{10}^0$
$RMEM_1 = MDEL2 \cdot TP_1^0 \cdot S_{10}^1$
$WMEM_0 = MDEL2 \cdot TP_1^1 \cdot S_{10}^0$
$WMEM_1 = MDEL2 \cdot TP_1^1 \cdot S_{10}^1$

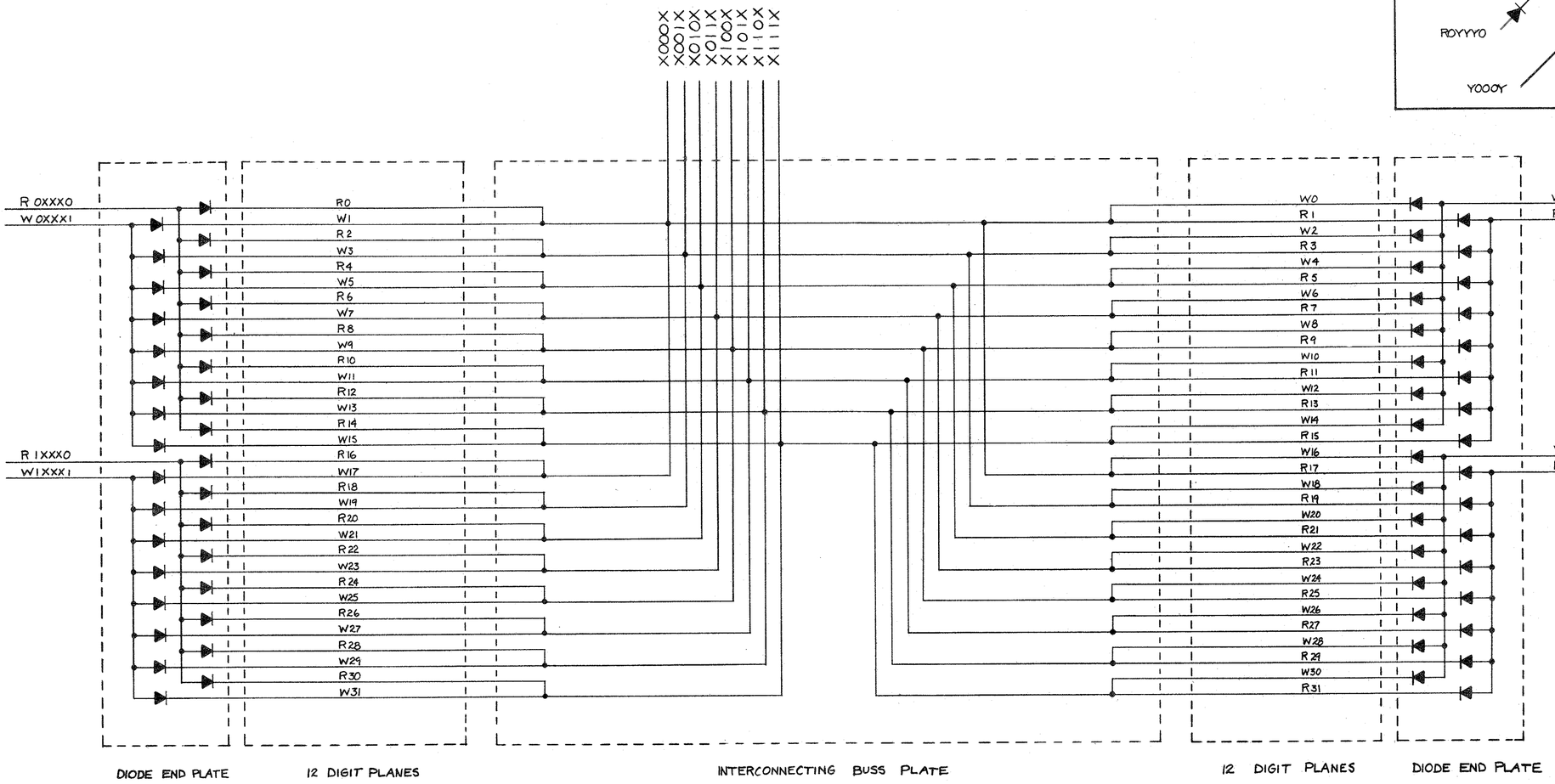


NOTE 1: WHEN A DUMMY STACK PLUG-IN UNIT IS INSERTED, PIN E OF Z7 IS INTERNALLY CONNECTED TO GND.

WHEN MEMORY PLUG-IN UNIT 1 IS INSERTED, PIN E OF Z7 IS INTERNALLY CONNECTED TO -15 V THROUGH A 10KΩ RESISTOR.

CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			MEMORY ADDRESS SELECTION SYSTEM
ENG.			
DATE	1030		CH.





NOTE 1: EACH CORE HAS TWO X SELECTION AND TWO Y SELECTION LINES RUNNING THROUGH IT. (SEE PICTORIAL ABOVE) THE DIGIT PLANES ARE DRAWN TWICE SCHEMATICALLY SO THIS MAY BE MORE EASILY SEEN.

NOTE 2: THE "Y" MEMORY STACK ADDRESS IS WIRED FROM A SIMILAR SCHEMATIC.

CHANGE LETTER	APP'D BY	DATE	CHANGES
LINC			"X" MEMORY STACK ADDRESS WIRING
ENG.			
DATE	1031		CH.

FU (MAG TAPES)

NAME		PIN	FRAME LOC
CHASSIS GND		1	
SOLENOID GND		17	
$TCHAN^0$	♦	2	T20V
$TCHAN^1$	♦	18	T20W
$MCHAN^0$	♦	3	T21V
$MCHAN^1$	♦	19	T21W
TM RETURN		4	$T21gnd_L$
D RETURN		20	$T24gnd_L$
$DCHAN^0_1$	♦	5	T25V
$DCHAN^1_1$	♦	21	T25W
$DCHAN^0_2$	♦	6	T24V
$DCHAN^1_2$	♦	22	T24W
$DCHAN^0_3$	♦	7	T23V
$DCHAN^1_3$	♦	23	T23W
$BMOTN^1_0$	♦	8	U25F
$BMOTN^1_1$	♦	24	U25V
BU^0	♦	9	U25Z
BU^1	♦	25	U25X
		10	
		26	
		11	
		27	
		12	
		28	
		13	
		29	
		14	
		30	
OV		15	
−18V		31	
−15V		16	
−15 SOLENOID		32	

MAGNETIC TAPE CONNECTOR

FC (DA)

NAME		PIN	FRAME LOC
TN_0	♦	1	W18L
TN_1	♦	17	W18U
TN_2	♦	2	W15L
TN_3	♦	18	W15U
TN_4	♦	3	W12L
TN_5	♦	19	W12U
TN_6	♦	4	W9L
TN_7	♦	20	W9U
TN_8	♦	5	W6L
TN_9	♦	21	W6U
TN_{10}	♦	6	W3L
TN_{11}	♦	22	W3U
TNEL	♦	7	V23L
OPR10	♦	23	U17P
OPR11	♦	8	U17T
OPR12	♦	24	U17W
OPR13	♦	9	U17Z
OPR14	♦	25	U16H
OPR15	♦	10	U16L
OPR16	♦	26	U16P
OPR17	♦	11	U16T
XL7	♦	27	U23Y
XL10	♦	12	U22H
XL11	♦	28	U22K
XL12	♦	13	U22M
XL13	♦	29	U22P
INTERNAL CLOCK INHIBIT	◇	14	S9W
[illegible]	♦	30	L'd
BEGINTEF	♦	15	X'd X

TN & JN = A, in

FD (DB)

NAME		PIN	FRAME LOC
UN_0	♦	1	X18L
UN_1	♦	17	X18U
UN_2	♦	2	X15L
UN_3	♦	18	X15U
UN_4	♦	3	X12L
UN_5	♦	19	X12U
UN_6	♦	4	X9L
UN_7	♦	20	X9U
UN_8	♦	5	X6L
UN_9	♦	21	X6U
UN_{10}	♦	6	X3L
UN_{11}	♦	22	X3U
UNEL	♦	7	V22L
CLEL CLEAR A	♦	23	V3F
BEGT	♦	8	U25H
MINP	♦	24	U25M
MOUT	♦	9	U25K
OPR0	♦	25	U18H
OPR1	♦	10	U18L
OPR2	♦	26	U18P
OPR3	♦	11	U18T
OPR4	♦	27	U18W
OPR5	♦	12	U18Z
OPR6	♦	28	U17H
OPR7	♦	13	U17L
XL0	♦	29	U24H
XL1	♦	14	U24K
XL2	♦	30	U24M
XL3	♦	15	U24P
XL4	♦	31	U23S
XL5	♦	16	U23U
XL6	♦	32	U23W

UN & VN = B, in

FE (DC)

NAME		PIN	FRAME LOC
GA_0	♦	1	W25Z
GA_1	♦	17	W25W
GA_2	♦	2	W25T
GA_3	♦	18	W25P
GA_4	♦	3	W25L
GA_5	♦	19	W25H
GA_6	♦	4	W24Z
GA_7	♦	20	W24W
GA_8	♦	5	W24T
GA_9	♦	21	W24P
GA_{10}	♦	6	W24L
GA_{11}	♦	22	W24H
ALEL	♦	7	U25P
AREL	♦	23	U25S
SN_0	♦	8	W18F
SN_1	♦	24	W18Y
SN_2	♦	9	W15F
SN_3	♦	25	W15Y
SN_4	♦	10	W12F
SN_5	♦	26	W12Y
SN_6	♦	11	W9F
SN_7	♦	27	W9Y
SN_8	♦	12	W6F
SN_9	♦	28	W6Y
SN_{10}	♦	13	W3F
SN_{11}	♦	29	W3Y
SNEL	♦	14	V22Z

GA = gated A, out

BB = Buffered B, out

FF (DD)

NAME		PIN	FRAME LOC
BB_0	♦	1	W22Z
BB_1	♦	17	W22X
BB_2	♦	2	W22V
BB_3	♦	18	W23Z
BB_4	♦	3	W23X
BB_5	♦	19	W23V
BB_6	♦	4	W23T
BB_7	♦	20	W23R
BB_8	♦	5	W23N
BB_9	♦	21	W23L
BB_{10}	♦	6	W23J
BB_{11}	♦	22	W23F
VN_0	♦	7	X18M
VN_1	♦	23	X18T
VN_2	♦	8	X15M
VN_3	♦	24	X15T
VN_4	♦	9	X12M
VN_5	♦	25	X12T
VN_6	♦	10	X9M
VN_7	♦	26	X9T
VN_8	♦	11	X6M
VN_9	♦	27	X6T
VN_{10}	♦	12	X3M
VN_{11}	♦	28	X3T
VNEL	♦	13	V22T
BR_0	♦	29	W22T
BR_1	♦	14	W22R
BR_2	♦	30	W22N
BR_3	♦	15	W22L
BR_4	♦	31	W22J
BR_5	♦	16	W22F

FH (DE)

NAME		PIN	FRAME LOC
CHASSIS		1	
OV		17	
ANCH17	⧫	2	V17X
ANCH17	◇	18	$V17gnd_L$
		3	
		19	
		4	
OV±18 Return		20	V15SO
+18V		5	V17SO
−18V		21	V19SO
ANCH10	⧫	6	V18H
ANCH10	◇	22	$V18gnd_U$
ANCH11	⧫	7	V18M
ANCH11	◇	23	$V18gnd_U$
ANCH12	⧫	8	V18T
ANCH12	◇	24	$V18gnd_L$
ANCH13	⧫	9	V18X
ANCH13	◇	25	$V18gnd_L$
ANCH14	⧫	10	V17H
ANCH14	◇	26	$V17gnd_U$
ANCH15	⧫	11	V17M
ANCH15	◇	27	$V17gnd_U$
ANCH16	⧫	12	V17T
ANCH16	◇	28	$V17gnd_L$
		13	
		29	
		14	
		30	
		15	
		31	
−15V		16	
		32	

ANCH = analog channel

FJ (DF)

NAME		PIN	FRAME LOC
CHASSIS		1	
OV		17	
BOPR 2.3	▷	2	M1W
BOPR 2.3	▷	18	M1X
		3	
		19	
		4	
		20	
		5	
		21	
QKRESTART	►	6	V21N
QKRESTART	▷	22	V21D
BCPL	►	7	V25J
BCPL	▷	23	V25H
BATPL	►	8	V25S
BATPL	▷	24	V25T
BPRESET	►	9	V25V
BPRESET	▷	25	V25X
BBEOP	►	10	V24J
BBEOP	▷	26	V24H
BOPR·2.1	►	11	V24S
BOPR·2.1	▷	27	V24T
BOPR·2.2	►	12	V24V
BOPR·2.2	▷	28	V24X
EXT CLOCK	►	13	M1E
EXT CLOCK	▷	29	M1D
+10V		14	
+10V		30	
		15	
		31	
−15V		16	
OV		32	

TERMINAL FRAME CONNECTORS

DATE		CHANGE LETTER	CHANGES
ENG.	LINC	APP'D BY	
		DATE	
1032	FANTAIL PIN ASSIGNMENTS SHEET #1		
CH.			

FT (SCOPES)			
NAME		PIN	FRAME LOC
CHASSIS		1	GD AT F.T.
		17	
YDEFLECTION		2	V13F
YRETURN		18	V13D
XDEFLECTION		3	V7F
XRETURN		19	V7D
		4	
		20	
OFFINT	►	5	V21V
OFFINT	▷	21	V21X
KNOB^0		6	V18E
KRTN^0		22	V19gnd
KNOB2		7	V18R
KRTN2		23	V19gnd
KNOB4		8	V17E
KRTN4		24	V16gnd
KNOB6		9	V17R
KRTN6		25	V16gnd
+6 VOLTS		10	V16F
−6 VOLTS		26	V16E
ONINT$_0$	►	11	V23P
ONINT$_0$	▷	27	V23R
ONINT$_1$	►	12	V23W
ONINT$_1$	▷	28	V23X
KNOB1		13	V18K
KRTN1		29	V19gnd
KNOB3		14	V18V
KRTN3		30	V19gnd
KNOB5		15	V17K
KRTN5		31	V16gnd
KNOB7		16	V17V
KRTN7		32	V16gnd

SCOPE CONNECTOR

FL (CA)			
NAME		PIN	FRAME LOC
OV		1	
OV		17	
RS$^1_8$	♦	2	Y14J
LS$^0_5$	♦	18	Y24S
RS$^1_9$	♦	3	Y14W
LS$^1_5$	♦	19	Y24U
RS$^1_{10}$	♦	4	X3F
LS$^0_6$	♦	20	Y24M
RS$^1_{11}$	♦	5	X3Y
LS$^1_6$	♦	21	Y24P
LS$^0_0$	♦	6	Y25W
LS$^0_7$	♦	22	Y24H
LS$^1_0$	♦	7	Y25Y
LS$^1_7$	♦	23	Y24K
LS$^0_1$	♦	8	Y25S
LS$^0_8$	♦	24	Y23W
LS$^1_1$	♦	9	Y25U
LS$^1_8$	♦	25	Y23Y
LS$^0_2$	♦	10	Y25M
LS$^0_9$	♦	26	Y23S
LS$^1_2$	♦	11	Y25P
LS$^1_9$	♦	27	Y23U
LS$^0_3$	♦	12	Y25H
LS$^0_{10}$	♦	28	Y23M
LS$^1_3$	♦	13	Y25K
LS$^1_{10}$	♦	29	Y23P
LS$^0_4$	♦	14	Y24W
RS$^1_7$	♦	30	Y15W
LS$^1_4$	♦	15	Y24Y
LS$^1_{11}$	♦	31	Y7W
−15V		16	
−15V		32	

FM (CB)			
NAME		PIN	FRAME LOC
OV		1	
OV		17	
XOESTOPPB	♦	2	S2U
ST400PB	◇	18	S13S
ISTOPPB	♦	3	S3U
ST20PB	◇	19	S13R
RESUMEPB	◇	4	S12W
STRSPB	◇	20	S13T
STEPPB	◇	5	S10H
IBIPB	◇	21	S11T
PBLC	◇	6	S8K
CBCPB	◇	22	S11U
DOPB	◇	7	S12V
PBLB	◇	23	S4U
PRESETPB	◇	8	S11S
RS$^1_0$	♦	24	Y18J
FILLSTEPPB	◇	9	S12T
RS$^1_1$	♦	25	Y18W
STEPEXPB	◇	10	S12U
RS$^1_2$	♦	26	Y17J
PBLA	◇	11	S1Y
RS$^1_3$	♦	27	Y17W
FILLPB	◇	12	S12R
RS$^1_4$	♦	28	Y16J
EXAMPB	◇	13	S12S
RS$^1_5$	♦	29	Y16W
MARKPB	◇	14	S13U
RS$^1_6$	♦	30	Y15J
CLRPB	◇	15	S13V
AUTOPB	♦	31	R2U
−15V		16	
−15V		32	

FP (CC)			
NAME		PIN	FRAME LOC
OV		1	
OV		17	
		2	
SS$^1_5$	♦	18	U23K
RLSD	◇	3	K18W
		19	
KSTR	◇	4	U16V
		20	
KB$^1_0$	♦	5	X17F
		21	
KB$^1_1$	♦	6	X17Y
		22	
KB$^1_2$	♦	7	X14F
		23	
KB$^1_3$	♦	8	X14Y
		24	
KB$^1_4$	♦	9	X11F
PBLD	♦	25	X19U
KB$^1_5$	♦	10	X11Y
RDLF	◇	26	K8J
SS$^1_0$	♦	11	U24S
RDLE	◇	27	K8H
SS$^1_1$	♦	12	U24U
RDLD	◇	28	K8F
SS$^1_2$	♦	13	U24W
RDLC	◇	29	K8E
SS$^1_3$	♦	14	U24Y
RDLB	◇	30	K8X
SS$^1_4$	♦	15	U23H
RDLA	◇	31	K8Z
−15V		16	
−15V		32	

FN (CD)			
NAME		PIN	FRAME LOC
OV		1	
OV		17	
S_0LT		2	Y22Z
P_3LT		18	Y21T
S_1LT		3	Y22X
P_4LT		19	Y20Z
S_2LT		4	Y22V
P_5LT		20	Y20X
S_3LT		5	Y22T
P_6LT		21	Y20V
S_4LT		6	Y22R
P_7LT		22	Y20T
S_5LT		7	Y22N
P_8LT		23	Y20R
S_6LT		8	Y22L
P_9LT		24	Y20N
S_7LT		9	Y22J
C_6LT		25	Y19T
S_8LT		10	Y22F
C_7LT		26	Y19R
S_9LT		11	Y21R
C_8LT		27	Y19N
S_{10}LT		12	Y21N
C_9LT		28	Y19L
P_0LT		13	Y21Z
C_{10}LT		29	Y19J
P_1LT		14	Y21X
C_{11}LT		30	Y19F
P_2LT		15	Y21V
AUDOUT		31	K17X
−15V		16	
−15V		32	

FR (CE)			
NAME		PIN	FRAME LOC
OV		1	
OV		17	
R_0LT		2	W21T
EXAMLT		18	S14R
R_1LT		3	W21R
MARKLT		19	S14F
R_2LT		4	W21N
CLRLT		20	S14L
R_3LT		5	W21L
XOESTOPLT		21	S14Z
R_4LT		6	W21J
ISTOPLT		22	S14X
R_5LT		7	W21F
AUTOLT		23	S14J
ECYLT		8	K17N
IBILT		24	S14T
OCYLT		9	K17L
CBCLT		25	S14V
XCYLT		10	K17J
C_0LT		26	Y20L
ICYLT		11	K17F
C_1LT		27	Y20J
PAUSELT		12	K17T
C_2LT		28	Y20F
RUNLT		13	K17R
C_3LT		29	Y19Z
		14	
C_4LT		30	Y19X
FILLLT		15	S14N
C_5LT		31	Y19V
−15V		16	
−15V		32	

FS (CF)			
NAME		PIN	FRAME LOC
SOLGND		1	
SOLGND		17	
CHASSIS		2	
A_1LT		18	W21X
B_0LT		3	Y21L
A_2LT		19	W21V
B_1LT		4	Y21J
A_3LT		20	W20Z
B_2LT		5	Y21F
A_4LT		21	W20X
B_3LT		6	X24Z
A_5LT		22	W20V
B_4LT		7	X24X
A_6LT		23	W20T
B_5LT		8	X24V
A_7LT		24	W20R
B_6LT		9	X24T
A_8LT		25	W20N
B_7LT		10	X24R
A_9LT		26	W20L
B_8LT		11	X24N
A_{10}LT		27	W20J
B_9LT		12	X24L
A_{11}LT		28	W20F
B_{10}LT		13	X24J
LINKLT		29	K17V
B_{11}LT		14	X24F
RCHIME	♦	30	R13Z
A_0LT		15	W21Z
RELIP^0	◇	31	U16U
−15VSOL		16	
−15VSOL		32	

CONSOLE CONNECTORS

CHANGES	CHANGE LETTER	APP'D BY	DATE

DATE

ENG.

LINC

FANTAIL
PIN ASSIGNMENTS
SHEET #2

1033

CH.

BOX K

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER								1009	1008	1 1008 2 1008 3 1008 4 1008 5 1026 6 1026	E 1017 F 1009	1023	1 1008 2 1008 3 1008 4 1009 5 1009 6 1009	1 1008 2 1008 3 1020 4 1026 5 1026 6 1025	1 1008 2 1008 3 1008 4 1008 5 1008 6 1008 7 1026 8 1026 9 1008	1 1008 2 1008 3 1008 4 1008 5 1020 6 1020 7 1026 8 1026 9 1029	1022	1 1026 2 1026 3 1026 4 1026 5 1020 6 1020 7 1020 8 1020 9 1023	1026	1026	1026	1026	1026	1026	1026	1026 1029 1025
P.I.U. TYPE								4303	4193-7	4113-R	4143-7EF	4303	4112 R	4127	4102 R	4102	1669	4102 R	4113 R	4113 R	4102 R	4115 R	4112 R	4119 R	4606

BOX L

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1 1036 * 2 1036 * 3 1036 4 1036	1 1008 2 1003 * 3 1003 4 1003 5 1003 6 1003 7 1007 8 1026 9 1009	1 1003 2 1003 3 1003 4 1003 5 1003 6 1019	1 1003 2 1003 3 1003 4 1003 5 1003 6 1029	E 1026 F 1003	E 1029 F 1009	1 1029 2 1009 3 1017 4 1017	E 1008 F 1008	1008	1008	1 1017 2 1017 3 1026 4 1026 5 1024 6 1026 7 1028 8 1024 9 1018	1 1017 2 1026 3 1026 4 1026 5 1027 6 1007 7 1007 8 1009 9 1003	1 1008 2 1023 3 1007 4 1007 5 1015 6 1008	1 1014 * 2 1014 * 3 1036 * 4 1036 * 5 1036 * 6 1036 7 1026 * 8 1026 * 9 1054 *	1036	E 1008 F 1026	E 1015 F 1026	1 1023 2 1025 3 1007	1023	1023	1 1026 2 1020 3 1023 4 1023	1 1036 2 1036 * 3 1014 4 1036	1 1026 2 1025 3 1023 4 1023 5 1009 6 1020	1 1025 2 1003 3 1019 4 1025	1 1026 2 1008 3 1007
P.I.U. TYPE	4115 S	4102 R	4113 R	4127	4193-3	4193-5	4115	4193-5	4193-6	4604	4102 R	4102	4127 R	4102 S	4221-6	4193-7E	4193-1F	4604	4204AC	4204AC	4114 R	4115 S	4112 R	4115 R	4606

BOX M

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1 1007 2 1036 3 1027	1007	1007	1007	1007	1007	1007	1007	1007	1007	1007	1007	1007 1036	E 1009 F 1016	E 1027 E 1014	1010	1 1023 2 1014 3 1014 4 1015 5 1015 6 1027	E 1026 F 1014	E 1014 Z 1022	1 1015 2 1010 3 1010 4 1021 5 1021 6 1022 7 1027 8 1027 9 1014	1 1020 2 1020 3 1014	E 1016 F 1020	1 1036 2 1009 3 1015 4 1014 5 1036 6 1036 *	1 1027 2 1014 3 1016	1 1009 2 1014 3 1020
P.I.U. TYPE	4606	4606	4606	4606	4606	4606	4606	4606	4102R	4102R	1151G	4204AC	4204A	4143-2	4143-5F	4143-3EF	4127	4143-3E	4205	4102R	4606	4143-8EF	4113S	4606	4604

BOX N

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1007	1007	1007	1 1008 2 1008 3 1007 4 1007 5 1007 6 1007	1 1018 * 2 1015 * 3 1015 * 4 1015 * 5 1015 * 6 1008 *	1020	1 1012 2 1012 3 1012 4 1008 5 1008 6 1025	1 1012 2 1012 3 1009 4 1024	1 1020 2 1020 3 1020 4 1012 5 1012 6 1012 7 1012 8 1012 9 1012	1020	1 1020 2 1008 3 1012 4 1010	1 1009 2 1026 3 1015 4 1015 5 1015 6 1007	1 1012 2 1012 3 1015 4 1014	1 1014 2 1015 3 1026 4 1015 5 1015 6 1022	1 1017 2 1015 3 1016 4 1016 5 1014 6 1014	1015	1 1015 * 2 1015 * 3 1015 * 4 1015 * 5 1020 * 6 1020 * 7 1020 * 8 1027 * 9 1012	1015	1015	1020	1015	1 1016 2 1015 3 1015	1015	1015	1 1016 2 1015 3 1015
P.I.U. TYPE	4407	46065	4204AC	4112R	4113S	4112R	4113R	4115	4102R	4113R	4114R	4112R	4115	4113R	4127R	4143-3EA	4102S	4143-4	4606	4606	4606	4604	4606	4606	4606

BOX P

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER		1012	1012	1012	1012	1020	1020	1020	1020	1 1020 2 1020 3 1020 4 1020 5 1020 6 1017	1 1020 2 1009 3 1020 4 1020	1 1036 2 1008 3 1015 4 1017 5 1017 6 1015	1 1019 2 1020 3 1016 4 1015	1 1016 2 1019 3 1017 4 1019	1016	E 1016 F 1014	1 1015 * 2 1014 3 1009 4 1019 5 1017 6 1018	E 1016 F 1015	1 1016 2 1016 3 1015 4 1016 5 1016 6 1016 7 1015 8 1009 9 1015	1016	1016	1016	1016	1016	1 1026 2 1014 3 1014	1 1016 2 1016 3 1012
P.I.U. TYPE		1151G	1151G	1151G	1151G	4113R	4102R	4102R	4102R	4113R	4115R	4112 R	4114R	4115R	4143-1EF	4143-7EF	4127 S	4143-8EF	4102R	4115R	4606	4604	4606	4606	4606

BOX R

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1018	1018	1 1008 2 1009 3 1018	1019	1019	1 1019 2 1019 3 1019 4 1012 5 1009 6 1009 7 1009 8 1008 9 1018	1 1019 2 1019 3 1019 4 1012 5 1018 6 1018 7 1018 8 1009 9 1009	1 1019 2 1019 3 1009	1019	E 1019 F 1017	1 1019 2 1026 3 1020 4 1017 5 1020 6 1017	1 1016 2 1020 3 1017 4 1009 5 1019 6 1009	1 1020 2 1026 3 1020 4 1017 5 1019 6 1019 7 1021 8 1017 9 1009	E 1019 F 1017	E 1017 F 1016	E 1017 F 1019	E 1019 F 1012	E 1012 F 1017	1017	1 1017 2 1017 3 1012	1017	1 1017 2 1012 3 1017	1 1017 3 1018 3 1012	1017	1019
P.I.U. TYPE	4102R	4410	4606	1304	1304	4102	4102R	4604	4143-4	4143-3E	4112 R	4113R	4102 R	4143-6F	4143-4E	4143-8E	4143-4F	4143-5EF	4143-3EF	4606	4606	4604	4606	4606	1607

BOX S

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1018	1018	1018	1 1008 * 2 1018 * 3 1018 * 4 1018 * 5 1018 * 6 1019 7 1036 *	1 1018 * 2 1020 * 3 1018 * 4 1018 *	1018	1018	1018	1-1143-W 1018 12 1020 16-18 1036 15 1007	1018	1018	1018	1018	1022												
P.I.U. TYPE	4102R	4410	4410	4113S	4114	4113	4115	4102	1001	4102R	4221-6	4221-2	4221-3	1669											

* DENOTES LOAD RESISTOR CONNECTED.

1001

1. E	10. R
2. F	11. S
3. H	12. T
4. J	13. U
5. K	14. V
6. L	15. W
7. M	16. X
8. N	17. Y
9. P	18. Z

4102

1.	E, F
2.	H, J
3.	K, L
4.	M, N
5.	P, R
6.	S, T
7.	U, V
8.	W, X
9.	Y, Z

4112 & 4113

1.	E, F, H
2.	J, K, L
3.	M, N, P
4.	R, S, T
5.	U, V, W
6.	X, Y, Z

4114 & 4115

1.	E, F, H, J, K
2.	L, M, N, P, R
3.	S, T, U, V
4.	W, X, Y, Z

4127

1.	E, F, H
2.	J, K, L
3.	M, N, P
4.	R, S, T
5.	U, V, W
6.	X, Y, Z

4205

1.	E, F, H, J, K, L, M, N, P
2.	R, S, T, U, V, W, X, Y, Z

4604 & 4606

1.	E, F, H, J, K, L
2.	M, N, P, R, S, T
3.	U, V, W, X, Y, Z

DATE	ENG.	LINC	CHANGES	CONTRACT NO.	APP'D DATE
1034	CH.	P.I.U. DRAWING NUMBER REFERENCE (CONTROL SIDE)			

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
DWG. NUMBER	1023	1023	1025	1023	E 1024 F 1025	1 1025 2 1024 3 1024	1 1025 2 1025 3 1025 4 1025 5 1024 6 1024 7 1024 8 9	1024	1024	1024	1024	1024	1024	1024	1024	1024	1 1024 2 1024 3 1024 4 1024 5 1023 6 1023			1023	1024		1024	1024	1024
BOX T																									
P.I.U. TYPE	4303	4303	4303	4604	4205	4606S	4102	4115R	4112R	1151G	4205	4205	4127R	4127R	4205	4205	4113R			EP107	EP107		EP107	EP107	EP107
DWG. NUMBER	1023	1 1025 2 1014 3 1024 4 1023 5 1023 6 1023	1025	1 1025 2 1025 3 1014 4 1024 5 1024 6 1023	1025	1 1014 2 1014 3 1014 4 1025 5 1024 6 1024 7 1024 8 1025 9 1018									1 1023 2 1020* 3 1020* 4 1025	1 1022 2 1022 3 1022 4 1022 5 1021 6 1020	1022	1022	1 1012 2 1012 3 1012 4 1012 5 1012 6 1012 7 1012 8 1012 9 1021	1012	1021	1021	1021	1021	1 1022 2 1020 3 1020 4 1020 5 1022 6 1022 7 1022 8 1022 9 1022
BOX U																									
P.I.U. TYPE	4606	4127R	4205	4112R	4115R	4102R									4115S	4112R	4112R	4112R	4102R	4102R	4143-1	4143-1	4143-1EF	4143-1EF	4102R
DWG. NUMBER	1 1025 2 1014 3 1014	1 1025 2 1025 3 1025 4 1025 5 1025 6 1014	1 1020 2 1023 3 1025 4 1026	1014	1014	1010	1027	1027	1027	1027	1027	1027	1027	1027	1027	1027	1027	1027	1012	1012	1 1027 2 1009 3 1022	1 1016 2 1016 3 1015	1 1015 2 1022 3 1022	1022	1022
BOX V																									
P.I.U. TYPE	4604	4127	4114R	4221-4	4221-5	4127	1561	4677	4677	4677	4677	4677	1561	1561	EP108	EP103	EP104	EP104	1151G	1151G	4604	4606	4606	4604	4604
DWG. NUMBER	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1010	1021	1022	1022	1022	1022	1022	1022
BOX W																									
P.I.U. TYPE	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4205	4123R	4123-1R	4143-2EF	1669	1669	4102R	4102R	4112R	4112R
DWG. NUMBER	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1011	1 1013 * 2 1011 3 1011 4 1010 5 1013 6 1012 7 1018* 8 1022* 9	1 1014 2 1010 3 1010 4 1010 5 1010 6 1010	1 1010 2 1021 3 1021 4 1021 5 1013 6 1013	1014	1021	1022	1021
BOX X																									
P.I.U. TYPE	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4205	4123R	4123-1	4102S	4127	4112R	422/-6	4143-2EF	1669	4143-2EF
DWG. NUMBER	1028	1028	1028	1028	1028	1028	1012	1012	1012	1012	1012	1012	1 1012 * 2 1013 3 1012 * 4 1011 5 1013 * 6 1013 *	1013	1013	1013	1013	1013	1022	1022	1022	1022	1021	1021	1021
BOX Y																									
P.I.U. TYPE	1571	1571	1571	1571	1571	1571	4204A	4204A	4204A	4204A	4204AC	4204AC	4127S	4204AC	4204AC	4204AC	4204AC	4204AC	1669	1669	1669	1669	4143-1	4143-1	4143-1E
DWG. NUMBER											1030	1030	1030	1030	1030	1030		1029	1029	1013	1013	1013	1013	1013	1013
BOX Z						MEMORY																			
P.I.U. TYPE											EP102	EP102	EP105	EP105	EP105	EP105		EP101	EP101	4204AC	4204AC	4204AC	4204AC	4204AC	4204AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25

* DENOTES LOAD RESISTOR CONNECTED.

1001

1. E	10. R
2. F	11. S
3. H	12. T
4. J	13. U
5. K	14. V
6. L	15. W
7. M	16. X
8. N	17. Y
9. P	18. Z

4102

1.	E, F
2.	H, J
3.	K, L
4.	M, N
5.	P, R
6.	S, T
7.	U, V
8.	W, X
9.	Y, Z

4112 + 4113

1.	E, F, H
2.	J, K, L
3.	M, N, P
4.	R, S, T
5.	U, V, W
6.	X, Y, Z

4114 + 4115

1.	E, F, H, J, K
2.	L, M, N, P, R
3	S, T, U, V
4.	W, X, Y, Z

4127

1.	E, F, H
2.	J, K, L
3.	M, N, P
4.	R, S, T
5.	U, V, W
6.	X, Y, Z

4205

1.	E, F, H, J, K, L, M, N, P
2.	R, S, T, U, V, W, X, Y, Z

4604 + 4606

1.	E, F, H, J, K, L
2.	M, N, P, R, S, T
3.	U, V, W, X, Y, Z

LINC

P.I.U. DRAWING NUMBER REFERENCE (REGISTER SIDE)

DATE | ENG. | CHECKED | APP'D | DATE | CHANGES | CH.

1035

L/T - 38 - 1035

PRINTED IN U.S.A.