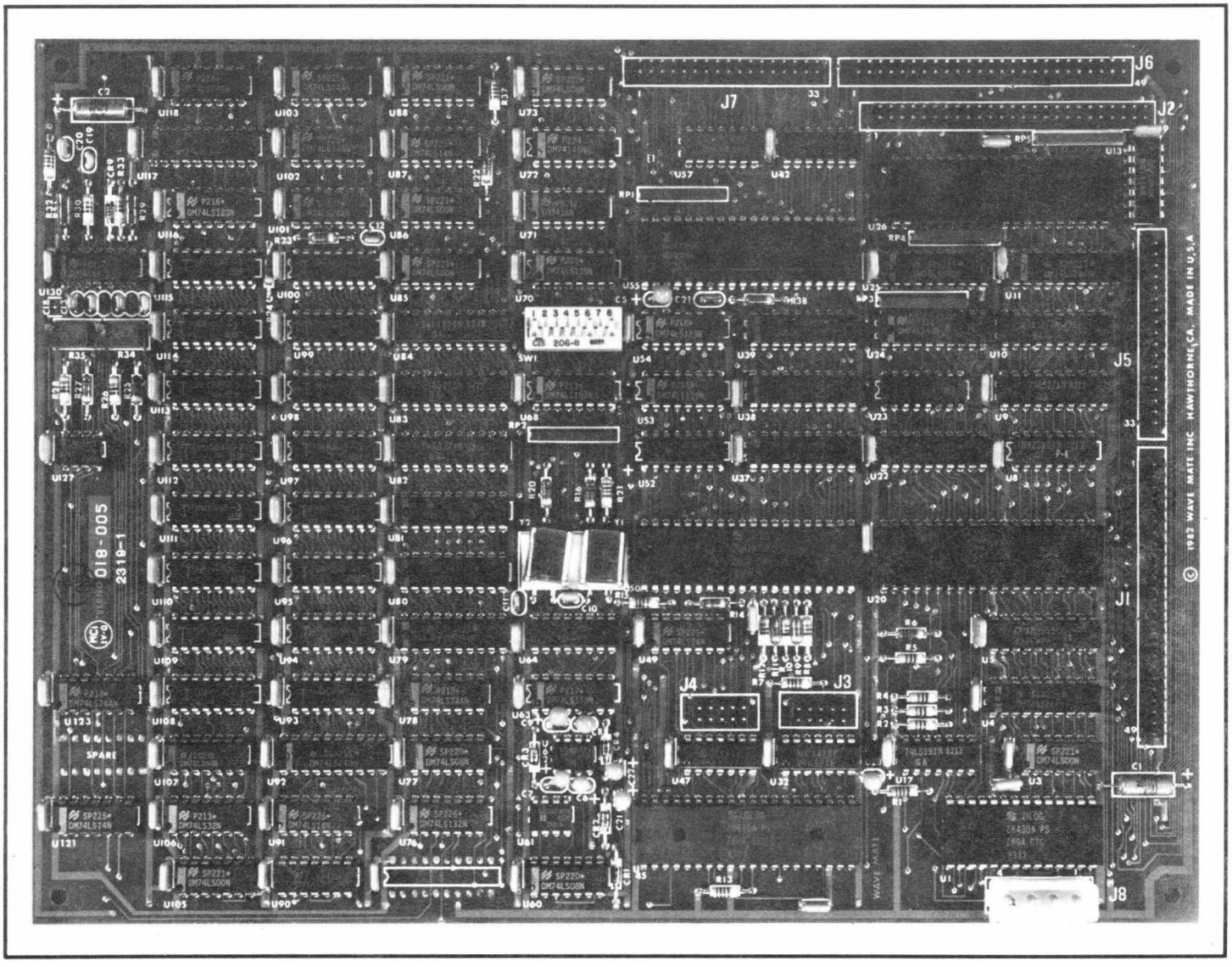

SINGLE-BOARD COMPUTER

WAVE MATE Z-80

BULLET MANUAL

Revised 6-3-83 for board etch revision E

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WAVE MATE Z-80
BULLET MANUAL

I INTRODUCTION

The WAVE MATE BULLET is a fast, compact and very powerful single board computer (SBC). This 4 MHz Z-80A with a powerful DMA (direct memory access) for data transfers uses 128K of RAM (random access memory), two RS-232-C serial ports, a Centronics printer interface, a floppy interface (for up to four mini's and four 8" drives), intelligent Winchester controller interface. The BULLET with its greatly enhanced C-BIOS will run CP/M at previously unheard of speeds. Video communication is provided through one of the RS-232-C ports to which any of several different serial terminals may be attached. Future expansion is provided through a special high speed bus link. Because the BULLET contains two serial ports and two memory banks of 64k bytes each, a two-user MP/M system may be realized.

II DESIGN PHILOSOPHY

The WAVE MATE BULLET has been designed to be the heart of an extremely low cost, high performance microcomputer system. The BULLET is ideally suited for single-user CP/M and two-user MP/M small business applications as well as providing intelligent terminal, distributed processing, and high speed local networking capabilities. Special BULLET hardware features and a greatly enhanced C-BIOS have been implemented in order to overcome several serious limitations of the CP/M operating system as related to most existing hardware configurations.

Since most small microcomputer systems are I/O bound (rather than computer bound), the BULLET design has addressed this fact by incorporating into its architecture a flexible DMA facility, fully interrupt driven I/O, and a high speed floppy disk controller. The 8 bit 4 MHz Z-80A CPU was chosen with the full complement of Zilog compatible peripheral chips.

This insures a cost effective, simple design, yet unlike most other implementations, the design results in full use of the microprocessor's capabilities. The BULLET has been designed with the OEM/systems integrator in mind. Its compact size, low power requirement, and single supply voltage, make it easy to incorporate into both existing and new equipment.

III HARDWARE DESCRIPTION

A. Physical Considerations

The BULLET is packaged on a double sided printed circuit board measuring 8" by 10 3/4". Mounting holes .156 inches in diameter are provided .250 inches from the corners. The maximum height of the board, considering pin lead protrusion through the board on the underside as well as component height, is .625 inches. Additional height must be provided for the header connectors for the I/O. However, all connectors have been placed on the component side of the board. Component and connector identifiers are silk screened on the board.

B. Electrical Considerations

The BULLET requires only one regulated 5 volt power supply, which under normal room temperatures need supply only 1.5 amps. The plus and minus voltages, required for the RS-232-C operation, are generated on the BULLET board itself.

For power, Amp connector part # 350211-1 has been mounted on the BULLET; therefore the mating connector, supplied by the user, must be Amp housing part # 1-480424-0 with AMP contacts # 60617-4 or equivalent.

If a switching power supply is used the board and ALL disk drives MUST be shielded from noise.

C. Functional Units

1. Z-80A Central Processing Unit (CPU)

This CPU device operates at the maximum 4 MHz clock rate with no wait states. All peripheral devices are connected to the standard Zilog interrupt priority daisy chain. The priority interrupt logic is provided with look ahead which terminates on the external bus connector. Thus any devices added to the external bus may use the priority interrupt daisy chain.

2. 128K Random Access Memory (RAM)

Memory mapping of the address space from 0 to BFFF HEX is provided at I/O port 1A HEX. Although the DMA device can move data from/to any address within the 128K bytes of RAM on the BULLET, the Z-80 can only address 64K bytes. To provide

greater versatility, the address space between 0 and BFFF HEX may be exchanged between the main memory space and the buffer memory space. This scheme still leaves 16K bytes of memory space which can only be accessed by the DMA device. This memory space is used for track buffering to enhance system performance. Thus the memory from C000 to FFFF HEX in the buffer memory is dedicated to buffer only operations.

The remainder of the buffer memory may be mapped into the Z-80 space by writing a binary 1 to the port at 1A HEX. Main memory may be mapped in by writing a binary 0 to the same write only port. Note that the state of the memory map does not affect the DMA operations; that is, the memory map is constant for the DMA device.

For example, assume each address space contains a program and the currently executing program requested the operating system to read a sector. If the sector was already resident in the buffer space the operating system could initiate a DMA operation to transfer the data from the buffer space to the user space. The operating system could then switch the address space and start the second program executing while the DMA operation was being performed without affecting the transfer of data to the first program.

A read only hardware status port at address 19 HEX is provided to check the state of the following functions:

BIT	FUNCTION READ.
0	Bit 7 of port 18H.
1	DIP switch 2.
2	DIP switch 3.
3	DIP switch 4.
4	Floppy disk head load status.
5	*Floppy disk exchange (8 inch only).
6	FDC interrupt request line.
7	FDC data request line.

Since the revision E board reads the state of bit 7 of I/O port 18 HEX instead of the DIP switch, software may write to port 18 HEX and test port 19 HEX to determine if bit 7 changes state. Thus the software can determine if it is executing on a revision E board or an earlier revision board.

3. Parallel Input/Output Controller (PIO)

This device provides two 8 bit parallel I/O ports. On the BULLET it is used to implement the SCSI bus control interface and the Centronics port status interface. To provide these functions, both ports must be programmed in bit mode. Port A provides the SCSI bus interface and port B provides the Centronics port interface. The control signal assignments presented here are further described under the applicable I/O device.

PIO Port A. SCSI bus.

BIT 0:	*ATN	output
BIT 1:	*RST	output
BIT 2:	*SEL	output
BIT 3:	*BUSY	input
BIT 4:	*MSG	input
BIT 5:	*C/D	input
BIT 6:	*REQ	input
BIT 7:	*I/O	input

PIO Port B. Centronics. (all inputs)

BIT 0:	Centronics ACK
BIT 1:	Centronics BUSY
BIT 2:	Centronics FAULT
BIT 3:	No connection
BIT 4:	No connection
BIT 5:	No connection
BIT 6:	No connection
BIT 7:	No connection

Note that program control allows these devices to operate in either interrupt driven or polled mode. The PIO device is the third device on the priority interrupt daisy chain.

The PIO registers are at the following I/O port addresses:

4 HEX	Port A data.
5 HEX	Port B data.
6 HEX	Port A control.
7 HEX	Port B control.

4. Direct Memory Access Controller (DMA)

This device provides for data transfer from/to any memory location or I/O device. External logic is provided which allows transfers from/to either memory bank. The device port address is 14 HEX.

External device multiplexing allows several devices to use the DMA channel and controls transfers between the memory banks. The multiplexor port is a write only register which has a port address of 17 HEX. Device selection is according to the following table:

BITS 2,1,0	DEVICE
000	FDC floppy disk controller.
001	DART serial channel A.
010	DART serial channel B.
011	SASI bi-directional bus.
100	External device 1.
101	External device 2.
110	Unused.
111	Unused.

Memory control of DMA operations is according to the following table:

BITS 4,3	FUNCTION
00	Transfer from main memory to main memory.
01	Transfer from buffer memory to buffer memory.
10	Transfer from main memory to buffer memory.
11	Transfer from buffer memory to main memory.

The remaining bits in this register are unused. Note that when a transfer is between an I/O port and memory, the memory control must be either main/main or buffer/buffer depending upon which memory bank is the memory target.

5. Floppy Disk Controller/Formatter (FDC)

This device is a Fujitsu MB8877. It is upward compatible with the Western Digital FD1793 controller. The following I/O port addresses are assigned to this device:

10 HEX	Command/Status register.
11 HEX	Track register.
12 HEX	Sector register.
13 HEX	Data register.

Since this is not a Zilog device and not capable of generating or responding to the Zilog priority daisy chain interrupt scheme, it is connected to the DART's channel A "DCD" input to provide an interrupt vector. External logic provides for control of four 8 inch floppy disk drives and four 5 inch floppy disk drives. The external logic also provides for software control of the spindle motors (5 inch drive only), side select, and enabling of write precompensation. These functions are controlled by a write only register at I/O port address 16 HEX. The following table gives the bit definitions:

BIT 0	Bits 0 and 1 form a binary unit select number.
BIT 2	Select 8 inch floppy drives.
BIT 3	Select software control of port.
BIT 4	Select side 2.
BIT 5	Disable 5 inch floppy spindle motors.
BIT 6	Lock doors.
BIT 7	Enable write precompensation.

The device is capable of formatting and reading a wide variety of soft sectored diskettes. With 8 inch drives it is compatible with the IBM 3740 format and FM recording and the IBM System-34 format and MFM recording. With 5 inch drives it is compatible with both single density and double density soft sector formats. Data separation for all modes is provided by a digital phase lock loop circuit.

Mode selection is provided by programmable external control at I/O port 18 HEX. This write only register controls the following parameters:

BIT 0	PLO: Phase Lock Oscilator.
BIT 1	RCD: Read Clock Frequency.
BIT 2	EXC: MB8877 clock frequency.
BIT 3	*DEN: MB8877 density select.
BIT 4	Enable software control of mode.
BIT 5	UNUSED
BIT 6	UNUSED
BIT 7	UNUSED

The following table gives the value to be written to this port for the four modes of operation:

8 inch single density:	19 HEX
8 inch double density:	10 HEX
5 inch single density:	1F HEX
5 inch double density:	15 HEX

6. Dual Asynchronous Receiver/Transmitter (DART)

This device provides two independent asynchronous serial data channels. Each channel has an independent baud rate which is derived from the first two channels of the counter timer device (described later). These baud rates are determined by the CTC and DART programming and can range from 110 baud to 76.8 kilobaud.

In addition, the transmit/receive word parameters are fully programmable within the DART. Channel A of the DART is used for the system console. It is normally operated in full duplex and the only input from the RS-232-C line is the received data. Channel B of the DART provides a full implementation of the RS-232-C interface type E with the exception that there is no circuit CE (ring indicator).

The channel A "DCD" input is used by the floppy disk controller to request an interrupt vector on the Zilog daisy chain interrupt system. The DART is the second device on the daisy chain following the DMA device.

The DART registers are at the following port addresses:

0 HEX	Channel A data.
1 HEX	Channel A status/control.
2 HEX	Channel B data.
3 HEX	Channel B status/control.

7. Centronics Printer Port

On the revision E board the Centronics Data out port is located at 15 HEX. This is the same port that disables the boot PROM. Note that the boot PROM can never be accessed once it is disabled except by a full system reset. Thus the Centronics Data out port may be shared. An out instruction to this port address loads the Centronics data latch. To

strobe the Centronics parallel interface an out instruction to port 1B HEX fires a one shot to create the Centronics strobe pulse. The Centronics interface signals BUSY, ACK, and *FAULT may be read in the PIO Port B to determine when the Centronics interface is ready for data, or to generate an interrupt when they change state. Thus to send data out over the Centronics interface the program must determine that the interface is not BUSY through the PIO Port B, load the data latch through port 15 HEX, and issue a strobe by accessing port 1B HEX with an in or out instruction.

8. SCSI Interface

A Small Computer System Interface (SCSI) has been provided on the revision E BULLET board. This interface is capable of controlling a variety of SCSI compatible devices; however, it is most commonly utilized to communicate with a Winchester disk controller.

The SCSI is implemented by a bi-directional data port which is addressed at the multiple port address of C, D, E, or F HEX. Note that there is only one 8 bit data port but since it is not fully decoded the same data port appears at those four port addresses. To simplify references to this port it will normally be referred to as port C. Status and control of the SCSI is implemented with the PIO Port A, and through hardware handshake. A read from port C HEX accesses the data on the SCSI bus. A write to port C HEX latches the data which will then be read by the external device when it reads the SCSI data bus. Note that a read or write to port C HEX causes the hardware to assert the SCSI bus signal *ACK.

Users wishing to program the SCSI bus should be familiar with the operation of the SCSI as described in ANSI X3T9.2/82-2.

9. Priority Interrupt Structure

The BULLET uses the standard Zilog priority interrupt level structure. The priorities are shown in the table below from the highest priority to the lowest.

1. DMA
2. Floppy Disk Controller and DART on the same level
3. Centronics and SCSI on the same level
4. Clock Timer Circuit
5. External Devices

10. General Purpose External DMA Bus (GPED)

The GPED bus has been provided to permit the addition of a variety of I/O devices to the system. The devices interfaced through the GPED bus can operate either with or without DMA and have the lowest priority level in the interrupt structure.

The user of the GPED bus should be familiar with both the Z-80A CPU and the DMA controller chips. Reference should be made to the Zilog Z-80 technical manual and application notes.

11. Clock Timer Circuit (CTC)

This device provides four independently programmable counter/timer channels. Channel 0 is used to provide the baud clock for the DART channel A. Channel 1 is used to provide the baud clock for the DART channel B. Both baud clocks are available on the external bus. Channels 2 and 3 are used together to provide a real time clock capability and clock interrupts. This is achieved by using channel 2 as a timer and channel 3 as a counter. Channels 0, 1, and 2 have their inputs connected to a crystal controlled clock which provides a 1.2288 MHz frequency. The CTC device is the fourth device on the priority daisy chain.

The CTC registers are at the following I/O port addresses:

Channel 0	8 HEX
Channel 1	9 HEX
Channel 2	A HEX
Channel 3	B HEX

12. Read Only Memory (ROM)

Initial program loading (the boot process) is done by a 32 byte program in a PROM. Upon power up reset the PROM is mapped into a starting address of zero which is the Z-80 starting address after power up reset. The PROM locations are read only which means that a write to its address space will be placed into RAM. In addition reset enables switch selection of the floppy disk boot parameters. The boot device and mode are determined by the settings of the 8 position DIP switch on the BULLET.

The following table summarizes their function:

Switch Position				
5	6	7	8	
off	off	off	off	5 inch single density.
off	on	off	on	5 inch double density.
off	on	on	off	8 inch single density.
on	on	on	on	8 inch double density.

Note that the physical unit number is always unit zero regardless of whether it is a 5 or 8 inch drive. At any time after a reset an input or output to the port address 15 HEX will disable the PROM and it will no longer be accessible until another reset occurs.

D. I/O Connections

1. J1—50 pin General Purpose External DMA Bus connector

A 50 pin male header is used to permit the Z-80A CPU bus and the DMA bus to be used externally from the BULLET. The pin-out of this header is shown below.

PIN#	Signal	I/O	Description
1	D0	IO	Data Bit 0
2	D1	IO	Data Bit 1
3	D2	IO	Data Bit 2
4	D3	IO	Data Bit 3
5	D4	IO	Data Bit 4
6	D5	IO	Data Bit 5
7	D6	IO	Data Bit 6
8	D7	IO	Data Bit 7
9	CLOCK	O	CPU Clock
10	GND	O	Ground
11	A0	IO	Address Bit 0
12	A1	IO	Address Bit 1
13	A2	IO	Address Bit 2
14	A3	IO	Address Bit 3
15	A4	IO	Address Bit 4
16	A5	IO	Address Bit 5
17	A6	IO	Address Bit 6
18	A7	IO	Address Bit 7
19	A8	IO	Address Bit 8
20	A9	IO	Address Bit 9
21	A10	IO	Address Bit 10
22	A11	IO	Address Bit 11
23	A12	IO	Address Bit 12
24	A13	IO	Address Bit 13
25	A14	IO	Address Bit 14
26	A15	IO	Address Bit 15
27	GND	O	Ground
28	*BAO	O	Bus Acknowledge Out (DMA)
29	*EXRDY1	I	External Device 1 Ready
30	*EXRDY2	I	External Device 2 Ready
31	*ZC0	O	Baud Clock A
32	*RESET	O	Reset
33	*INT	I	Interrupt (CPU)
34	MEM	O	Memory Bank 0 Selected
35	*BSREQ	IO	Bus Request (DMA)
36	*BSACK	O	Bus Acknowledge (CPU)
37	*IORQ	O	I/O Request (CPU)
38	*MREQ	O	Memory Request (CPU)
39	*RD	O	Read (CPU)
40	*WR	O	Write (CPU)
41	*MI	O	Machine Cycle One
42	*RFSH	O	Memory Refresh (CPU)
43	*NMI	I	Non Maskable Interrupt (CPU)
44	*WAIT	I	Wait (CPU)
45	*HALT	O	Halt (CPU)
46	*DMEM	I	Disable ALL on board memory
47	*CTCIEO	O	External Interrupt Priority
48	*SELEX	O	External I/O Select (1C HEX)
49	ZC1	O	Baud Clock B
50	VCC	O	Plus 5 volts

The female mating connector to J1 is 3M part number 3425-6000 or equivalent. The output lines are capable of driving a maximum of 4 CMOS loads or 1 TTL load. The maximum cable length to be attached to J1 shall not exceed 36 inches.

2. J2—50 pin Small Computer System Interface connector.

A 50 pin male header is used to connect the BULLET to the SCSI. The pin-out of the header is shown below.

PIN#	Signal	I/O	Description
2	*DATA0	IO	Data bit 0
4	*DATA1	IO	Data bit 1
6	*DATA2	IO	Data bit 2
8	*DATA3	IO	Data bit 3
10	*DATA4	IO	Data bit 4
12	*DATA5	IO	Data bit 5
14	*DATA6	IO	Data bit 6
16	*DATA7	IO	Data bit 7
18	No connection		
20	No connection		
22	No connection		
24	No connection		
26	No connection		
28	No connection		
30	No connection		
32	*ATN	O	Attention
34	No connection		
36	*BUSY	I	Busy
38	*ACK	O	Acknowledge
40	*RST	O	Reset
42	*MSG	I	Message
44	*SEL	O	Select
46	*C/D	I	Command/Data
48	*REQ	I	Request
50	*I/O	I	Input/Output

All odd numbered pins are signal grounds.

The female mating connector to J2 is 3M part number 3425-6000 or equivalent. The maximum cable length to be attached to J2 shall not exceed 6 meters.

3. J3—10 pin serial port connector

A ten pin male header is used to attach the first RS-232-C serial terminal to the BULLET. When using the WAVE MATE provided C-BIOS and CP/M, this port is used as the system console. The pin-out of the header is shown below.

PIN#	Signal	I/O	Description
1	*TXDA	O	Transmit Data
2	*RXDA	I	Receive Data
3	*DTRA	O	Data Terminal Ready
4	*RTSA	O	Request to Send
5			No connection
6			No connection
7	RLSDA	O	Receive Line Signal Detect
8	GND	O	Ground
9	*CRESET	I	Computer Reset
10	GND	O	Ground

The female mating connector to J3 is 3M part number 3473-6000 or equivalent.

NOTE: The above signals correspond to the Zilog DART definitions. See the cable section for recommended RS-232-C usage.

4. J4—10 pin serial port connector

A ten pin male header is used to attach a second RS-232-C serial terminal to the BULLET.

PIN#	Signal	I/O	Description
1	*TXDB	O	Transmit Data
2	*RXDB	I	Receive Data
3	*DTRB	O	Data Terminal Ready
4	*RTSB	O	Request To Send
5	*CTSB	I	Clear To Send
6	*DCDB	I	Data Carrrier Detect
7	RLSDB	O	Receive Line Signal Detect
8	GND	O	Ground
9			No connection
10			No connection

The female mating connector to J4 is 3M part number 3473-6000 or equivalent.

NOTE: The above signals correspond to the Zilog DART definitions. See the cable section for recommended RS-232-C usage.

5. J5—34 pin Centronics Printer port connector

A 34 pin male header is used to attach a Centronics type printer to the BULLET. The pin-out of this header is shown below.

PIN#	Signal	I/O	Description
1	*CSTRB	O	STROBE
3	CDTA1	O	DATA BIT 1
5	CDTA2	O	DATA BIT 2
7	CDTA3	O	DATA BIT 3
9	CDTA4	O	DATA BIT 4
11	CDTA5	O	DATA BIT 5
13	CDTA6	O	DATA BIT 6
15	CDTA7	O	DATA BIT 7
17	CDTA8	O	DATA BIT 8
19	*CACK	I	ACKNOWLEDGE
21	CBUSY	I	BUSY
23	CPE	I	PAPER END
28	*CFAULT	I	PRINTER FAULT

Even pins 2 through 24 and 27, 30, and 31 are all connected to ground.

The female mating connector to J5 is 3M part number 3414-6000 or equivalent. The maximum cable length to be attached to J5 should not exceed 8 feet.

6. J6—50 pin 8" floppy disk drive connector

A 50 pin male header is used to attach from one to four 8" Shugart 800 compatible disk drives to the BULLET. The pin-out of this header is shown below.

PIN#	Signal	I/O	Description
2	*XTG43	I	Track greater than 43
12	*XDCG	I	Disk has been changed. (door opened & closed)
14	*XSIDE	O	Side Select
16	*DLOCK	O	Door Lock
18	*XHLD	O	Head Load
20	*INDEX	I	Index Pulse
22	*READY	I	Ready
26	*SEL1	O	Select Drive #1
28	*SEL2	O	Select Drive #2
30	*SEL3	O	Select Drive #3
32	*SEL4	O	Select Drive #4
34	*XDIR	O	Direction
36	*XSTEP	O	Step
38	*XWDAT	O	Write Data
40	*XWGAT	O	Write Gate
42	*TR00	I	Track Zero Sensor
44	*WPROT	I	Write Protect Sensor
46	*RDATA	I	Read Data

All odd numbered pins are connected to ground. The female mating connector to J6 is 3M part number 3425-6000 or equivalent. The maximum cable length to be attached to J6 is 8 feet.

7. J7—34 pin 5 1/4 inch mini floppy disk drive connector

A 34 pin male header is used to attach from one to four 5 1/4 inch Shugart 400 compatible disk drives to the BULLET. The pin-out of this header is shown below.

PIN#	Signal	I/O	Description
2	*DLOC	O	Door Lock
4	*MHLD	O	Head Load
6	*MSEL4	O	Select Drive #4
8	*INDEX	I	Index Pulse
10	*MSEL1	O	Select Drive #1
12	*MSEL2	O	Select Drive #2
14	*MSEL3	O	Select Drive #3
16	*MMTR	O	Motor On
18	*MDIR	O	Direction
20	*MSTEP	O	Step
22	*MWDAT	O	Write Data
24	*MWGAT	O	Write Gate
26	*TR00	I	Track Zero Sensor
28	*WPROT	I	Write Protect Sensor
30	*RDATA	I	Read Data
32	*MSIDE	O	Side Select

All odd numbered pins are connected to ground.

NOTE: To enable *MHLD the jumper E1 next to U53 must be installed. Most mini-floppy drives do not need this option and it is called IN USE on those drives.

The female mating connector to J7 is 3M part number 3414-6000 or equivalent. The maximum length of cable to be attached to J7 is 8 feet.

8. J8—4 pin power connector.

PIN#	Description
1	Not Connected
2	Not Connected
3	Ground (+5V Return)
4	+5V plus or minus 0.25V at 1.5A

The female mating connector is AMP P/N 1-480424-0.

E. Switches and Adjustments

1. Switches

An 8 position DIP switch designated as SW1 is located approximately in the center of the BULLET. SW1-2 thru SW1-3 are unassigned. SW1-1 controls the 5 volt supply to the SCSI bus termination resistors. When the switch is ON, the bus is terminated by the BULLET board. When the switch is OFF, there is no 5 volt power supplied to the terminators. If the board is not connected to a SCSI bus, this switch may be left in the OFF position with a power savings of approximately 150 milliamperes. If the board is connected to a SCSI bus this switch MUST be ON. Switches SW1-5 through SW1-8 are used to initialize the floppy disk controller to be compatible with the type of drive being used in the boot strapping of the system.

The types of drives and the appropriate switch setting are shown in the table below:

FLOPPY TYPE	SW1-5	SW1-6	SW1-7	SW1-8
Single density mini	off	off	off	off
Double density mini	off	on	off	on
Single density 8"	off	on	on	off
Double density 8"	on	on	on	on

2. Floppy Disk Controller Data Separator Adjustments for 5 inch drives.

The floppy disk controller uses a phase locked loop (PLL) data separator circuit. The PLL contains 2 variable resistors designated R34 and R35.

a. Data Separator Clock

R34 is adjusted to obtain a pulse every one (1) microscecond at U116 pin 12 with the floppy cable removed.

b. Data Separator Data

R35 is adjusted to obtain a 1 microsecond negative pulse at U116 pin 4 while accessing the floppy.

NOTE: For 8 inch drives these times are one half the above values.

F. System Set-up.

Prior to a cold start boot strap operation, the system serial video console and floppy disk drive must be connected to the BULLET.

1. System serial video console. A serial terminal must be connected to J3 on the BULLET. Reference should be made to section D4 of this manual for the appropriate connector pin-outs.

2. System floppy disk drive. The system can be booted from either a 5 1/4" mini floppy or an 8" floppy drive, either of them operating in single or double density recording. The disk drive selected for the boot strap operation must be wired as drive 0 and its characteristics must be reflected by the setting of switches SW1-5 through SW1-8 located on the BULLET.

3. System printer. The system printer may be either a Centronics parallel or an RS-232-C serial model. If a Centronics printer is selected, the second serial port is free for use in other ways, i.e., communications port, second printer, etc.

G. Bullet I/O Port Assignments

The following chart summarizes the I/O port assignments. Note that the port number is in hexadecimal.

PORT	DEVICE
0	DART CHANNEL A DATA
1	DART CHANNEL A STATUS/CONTROL
2	DART CHANNEL B DATA
3	DART CHANNEL B STATUS/CONTROL
4	PIO PORT A DATA
5	PIO PORT B DATA
6	PIO PORT A CONTROL
7	PIO PORT B CONTROL
8	CTC CHANNEL 0
9	CTC CHANNEL 1
A	CTC CHANNEL 2
B	CTC CHANNEL 3
C,D,E,F	SCSI DATA PORT
10	FDC COMMAND/STATUS PORT
11	FDC TRACK REGISTER
12	FDC SECTOR REGISTER
13	FDC DATA PORT
14	DMA CONTROLLER PORT
15	BOOT ROM DISABLE PORT/CENTRONICS DATA LATCH
16	EXTERNAL DISK REGISTER (HARDWARE CONTROL)
17	EXTERNAL DMA MUX (CHANNEL SELECT)
18	DATA SEPARATOR HARDWARE CONTROL
19	HARDWARE STATUS PORT
1A	MEMORY BANK SELECT PORT
1B	CENTRONICS STROBE

H. Serial Cable Information

The following cable chart is presented to aid in connection of the serial I/O devices to standard RS-232-C terminals. It should be noted that the RS-232-C circuit names define the direction of the signal between Data Communication Equipment (DCE) and Data Terminal Equipment (DTE). These signal names should not be confused with the signal names assigned by Zilog to the DART. The Zilog names closely follow the usage of the DART as part of a DTE. In the BULLET, the DART will generally be used as a part of a DCE circuit.

RS-232-C Circuit Name	DB25S Pin	Signal Direction	10 pin Header	DART Name
BA-Transmitted Data	2	→	2	RxD
BB-Received Data	3	←	1	TxD
CA-Request to Send	4	→	5	CTS
CB-Clear to Send	5	←	4	RTS
CC-Data Set Ready	6	←	3	DTR
AB-Signal Ground	7	↔	8	GND
CF-Rec Line Sig Detect	8	←	7	RLSD
CD-Data Terminal Ready	20	→	6	DCD

I. Connecting Floppy Disk Drives

The following disk drive configuration tables are presented to aid in connection of eight inch and five inch floppy disk drives to the BULLET. It should be noted that there are few options on the five inch drives and configuration is usually simple. The eight inch drives sometimes present difficulties due to the number of options and differences in names of the option strapping between drive manufacturers. When optioning eight inch drives the following points should be kept in mind: The stepper motor which positions the heads must be enabled with drive select, not head load. This is the most common cause of difficulty. If not set up in this manner the drive will not move the heads when a restore command without head load is issued.

SHUGART SA800/850 JUMPER OPTIONS

NAME	OPEN/SHORT
T3,T4,T5,T6	short
T1	short
T2	short
DS1	short for unit 1, otherwise open
DS2	short for unit 2, otherwise open
DS3	short for unit 3, otherwise open
DS4	short for unit 4, otherwise open
RR	short
RI	short
R,I,S	short
HL	open
DS	short
WP	short
NP	open
D	open
A,B	short
X	open
C	short
Z	short
Y	open
DC	short

SHUGART SA400/450/410/460 JUMPER OPTIONS

NAME	OPEN/SHORT
MX	open
DS0	short for unit 0, otherwise open
DS1	short for unit 1, otherwise open
DS2	short for unit 2, otherwise open
DS3	short for unit 3, otherwise open
MS	short
MM	open

NOTE: For five inch drives having an option to load the head on drive select or motor on it is recommended that they be optioned to load the head on select.