Western Digital

WD1007A-WAH/2

Application Notes
OEM Manual

Engineering Specification
February 1988
Preliminary

WESTERN DIGITAL
CORPORATION

PRELIMINARY
User's Guide

WD1007A–WAH/2

February 17, 1988

USER'S GUIDE

WD1007A-WAH/WA2 WINCHESTER/FLOPPY DISK CONTROLLER

1.0 DESCRIPTION AND DOCUMENT SCOPE

The WD1007A-WA2 and the WD1007A-WAH are single board Winchester Disk Controllers designed to interface two ESDI compatible disk drives to the IBM PC/AT or compatible host computer. The WD1007A-WA2 supports two 5-1/4 inch floppy disk drives; the WD1007A-WAH is a hard disk only version of the controller.

The ESDI drives used with this controller generally have two modes of operation, soft sector and hard sector. At this time, the WD1007A-WA2 offers only the hard sector mode of operation.

When integrating a hard disk drive into the AT environment, a drive type table must be selected that represents the physical characteristics of the drive being used. This information consists of the number of cylinders, heads and sectors per track. It is often difficult to match the drive and the table exactly. Most system BIOS'and/or Operating Systems support only the older MFM/ST-506 drives that used 17 sectors per track. The ESDI disk drive typically has 34 sectors per track when operating in the hard sector mode.

The WD1007A controllers have an optional BIOS ROM that provides drive parameter tables, low-level formatting routines, and surface analysis routines. While low-level formatting of the drive can be accomplished by several means, Western Digital recommends that you use the low-level format routine present in the WD1007A BIOS. If your controller does not have the BIOS option, obtain Western Digital's WDFMT 2.10 formatting utility.

This document describes installation in the IBM Personal Computer AT. If you have an AT compatible, you should refer to your system manuals or contact your dealer for information concerning installation of the WD1007A-WA2. The user should refer to the 1007A Application Notes and Data Sheet for a more thorough explanation of the board functions.

2.0 HARDWARE INSTALLATION INSTRUCTIONS

This section briefly describes installation of the WD1007A-WA2. If you wish to install the disk drive internally, it is best to locate the controller in the closest available expansion slot relative to the drive.

CAUTION

Handle the controller board by the ends of the board. Some of the chips are static sensitive and damage may occur if the board is incorrectly handled.

1. Verify the controller jumper settings. Modification of the standard factor settings on the controller is rarely necessary. Modify the jumpers only under the direction of a qualified individual; i.e., your dealer. Figure 1 illustrates the jumper locations. Table 1 lists the jumper default settings for the WD1007A-WA2 and the WD1007A-WAH. Table 2 provides the various address select ranges and corresponding jumper settings. Refer to WD1007A-WA2/WAH Data Sheet and Application Notes for a more complete description of the jumper functions and options. The WD1007A-WAH can be used as a field replacement board for existing WD1005-WAH boards without reformatting the hard disk drive. The WD1005-WAH firmware does not recognize the Set Unformatted Bytes Per Second command, and the user must set jumper/switches on the drive to the desired sectors per track. Substituting the WD1007A-WAH board and installing a jumper at W8 precludes the use of "Set Unformatted Bytes/Sector" command. When in the WD1007A-WA2 mode (no jumper on W8), the ESDI drive is forced to 35 sectors per track by the Set Unformatted Bytes Per Sector command. The interleave ratio is 1:1.

2. Remove or disable any other floppy controller in your system, if you are installing the WD1007A-WA2.

3. Verify termination of the last hard disk drive. Verify proper setting of drive select switches on the drive, if necessary. Do NOT use the drive's radial select option. Refer to the drive owner's manual for information about proper drive termination and select switches.

4. Remove the blank expansion slot bracket. Put the bracket away and save it for possible future use. The bracket screw will be used to hold the controller board in place.

5. Connect the 34-pin control cable to J1 connector. Keyed connectors prevent reversal of the cables.

6. Connect the control cable to the hard disk drive(s).

7. Attach a 20-pin data cable to J2 connector (for Drive 0).

8. Attach a 20-pin data cable to J3 connector (for Drive 1).

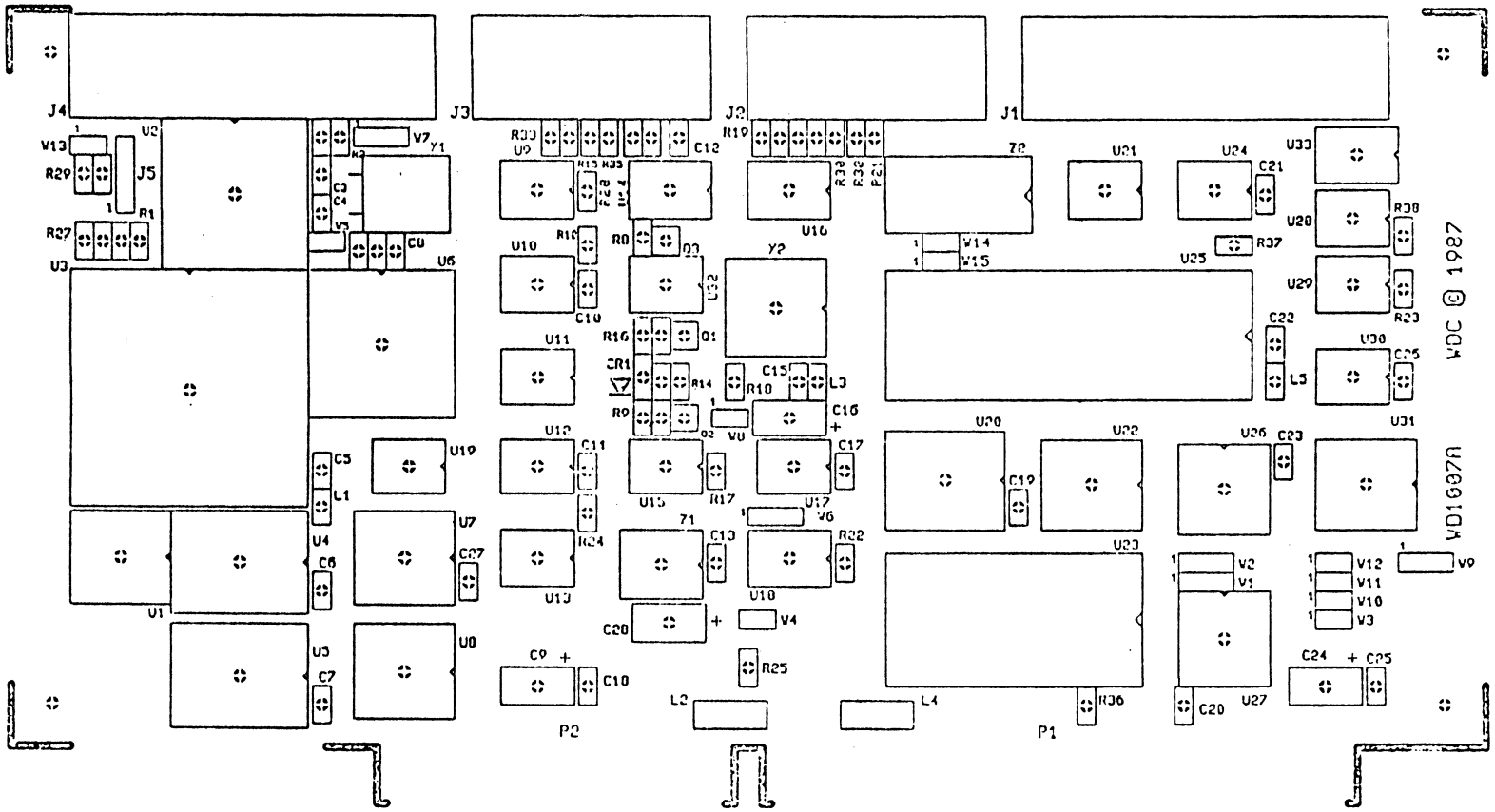
9. Connect the cable(s) to the proper hard disk drive(s).

10. Attach the 34-pin daisy-chain cable to J4 connector.

11. Connect the cable to the floppy drive(s).

12. Attach Winchester activity LED connector to J5.

13. Install the controller board into the expansion slot. Insure that the board is seated properly by pressing down on both ends of the board. Secure the board with the bracket screw.



WD1007A-WA 24-Aug-87 RMPLOT

GSCF BPL=1 SEG==

FIG. 1

WD1007A-WA2 JUMPERS CONFIGURATION TABLES

WD1007A-WA2 DEFAULT SETTING		WD1007A-WAH DEFAULT SETTING	
W1	2 - 3	W1	2 - 3
W2	2 - 3	W2	2 - 3
W3	JUMPED	W3	JUMPED
W4	NON JUMPED		
W5	NON JUMPED		
W6	2 - 3		
W7	1 - 2		
W8	NON JUMPED	W8	NON JUMPED
W9	NON JUMPED	W9	NON JUMPED
W10	NON JUMPED	W10	NON JUMPED
W11	JUMPED	W11	NON JUMPED
W12	NON JUMPED	W12	NON JUMPED
W13	UNCUT		
W14	NON JUMPED	W14	NON JUMPED
W15	NON JUMPED	W15	NON JUMPED

TABLE I

BIOS ADDRESS RANGES	JUMPER SETTINGS		
	W1	W2	W3
C0000 - C3FFF	2 - 3	2 - 3	JUMPED
C4000 - C7FFF	2 - 3	1 - 2	JUMPED
C8000 - CBFFF	1 - 2	2 - 3	JUMPED
CC000 - CFFFF	1 - 2	1 - 2	JUMPED
DISABLE			NON JUMPED

TABLE II

FLOPPY CONTROLLER	W4	W13 IN ETCH
ENABLE	NON JUMPED	UNCUT
DISABLE	JUMPED	CUT

TABLE III

DRIVE TYPE INPUT	W5
2 SPEEDS SPINDLE MOTOR	JUMPED
SINGLE SPEED	NON JUMPED

TABLE IV

FLOPPY ADDRESS RANGES	W6
37X	1 - 2
3FX	2 - 3

TABLE V

HIGH DENSITY SELECTION	W7
5.25", 1.2M	1 - 2
3.5", 1.44M	1 - 2

TABLE VI

WD1005 MODE	W8	JUMPED
WD1007 MODE		NON JUMPED

TABLE VII

CHASSIS GROUND & DIGITAL GROUND	W9
CONNECTED	2 - 3
UNCONNECTED	1 - 2

TABLE VIII

DIGITAL INPUT REG MODE	W10
LATCHED	JUMPED
NON LATCHED	NON JUMPED

TABLE IX

DISKCHANGE INPUT	W11
WITH FDC OPTION	JUMPED
WITHOUT FDC OPTION	NON JUMPED

TABLE X

PRIMARY/SECONDARY HARD DISK ADDRESSES	W12
1FX	NON JUMPED
17X	JUMPED

TABLE XI

SECTOR TRANSLATION	W14
ENABLE	NON JUMPED
DISABLE	JUMPED

TABLE XII

ECC SELECTION	W15
7 BYTES	JUMPED
4 BYTES	NON JUMPED

*WD1005 Mode - The controller sends 'Unformatted bytes/sector' from drive
WD1007 Mode - The controller sends 'Set Unformatted bytes/sector' command to the drive.

3.0 OPERATION

The WD1007A controller can be installed into any 16 bit slot in the IBM PC/AT or compatible host computer. By referring to the jumper option, the controller can be configured for the desired mode of operation. Be sure that the drive configuration is set properly to support the hard sector mode. Connecting cables for the ESDI hard disk are the same as those used on the ST506 interface disks. Also, device ID jumpers are implemented on the ESDI device just as with ST506 drives. In order to use an ESDI drive in a given system, a three step process has to be followed:

1) Low level format: done through WDFMT, third party software, or 1007A BIOS;

2) Active drive partitioning: done using MSDOS 3.3 (using FDISK) or other operating systems that allow partitioning (such as SCO XENIX).

3) High level format: done through the operating system using the normal 'Format C: (or D:)/S' command.

There are two different BIOS' that can play a role in the use of the WD1007A with the ESDI drive: the system BIOS and the 1007A BIOS. If one wishes to avoid using the 1007A BIOS (and just use the system BIOS), the exact physical drive parameters for the drive in question must be present in the system BIOS tables.

In terms of maximum flexibility and adaptability with different drives, Western Digital recommends the use of the WD1007A BIOS.

4.0 USING YOUR SYSTEM BIOS TO CONFIGURE YOUR DRIVE

The system BIOS refers to the BIOS that is controlling the computer (e.g. Phoenix, IBM-AT, Faraday). If the appropriate drive parameter tables are present, the system BIOS can be used, along with the operating system (MSDOS, SCO Xenix) to partition and high level format a given drive.

1. To determine if a system BIOS has the physical drive parameters required for your ESDI drive, use the appropriate set-up diskette for your system to see if the appropriate number of heads, number of cylinders and number of sectors/track are listed. If they are not listed, the system BIOS probably does not have the required parameter tables and one needs to use other means (such as WDFMT or the WD1007A BIOS) to low level format.

2. Another way of examining the system parameter tables to determine if the drive is listed in the BIOS is through the DOS Debug Utility:

a. Although some systems locate drive parameters in other locations, the standard location in the AT BIOS is F000:E401. The proper command at the DEBUG prompt (-) is as follows:

```
df000:e401 <CR>
```

This corresponds to drive type 1 and will display 8 lines of data from the BIOS ROM. By entering another "d" at the DEBUG prompt, another 8 lines of data will be displayed, corresponding to drive type 2, etc. This procedure is continued until all drive parameter information for all drive types is displayed. If the particular drive parameters are encountered in this process, it means the drive is recognized by the system BIOS.

Each parameter table has 16 bytes of data. Data from the BIOS ROM is displayed in hex, least signifcant byte first. This data breaks down as follows:

Bytes 1&2	Number of cylinders
Byte 3	Number of heads
Bytes 4&5	Not Used
Bytes 6&7	Write Pre-Compensation cylinder
Byte 8	Not Used
Byte 9	Control Byte (= 08H for > 8 heads)
Byte 10-12	Not Used
Bytes 13&14	Landing Zone3
Byte 15	Sectors Per Track
Byte 16	Not Used

3. There is also a way of using the DOS DEBUG utility to confirm the parameters for the current drive selected. This is done through the INT 41 (located at d0:104) and the INT 46 (located at d0:118) handlers. INT 41 corresponds to the address of the current selected parameters for drive) and INT 46 corresponds to the address of the current selected parameters for drive 1.

a. If you desire to see the current selected parameters for drive 0, the proper command at the DEBUG prompt (-) is:

d0:104

The first four bytes displayed correspond to the offset (2 bytes) and segment 6 (2 bytes) of the location where the selected parameters are, e.g., if after the above d0:104 the result is:

```
30   IF
00   C8    AB   73   . . . <=> Location C800:1F30
     [     ]    [     ]
     Offset     Segment
```

The current selected parameters are located at address C800:1F30. By typing DC800:1F30 at the DEBUG prompt, 16 bytes will be displayed (as explained above) describing the selected drive parameters.

Please see Figure 2 for the illustration of the above.

```
C:\>debug
-d0:104
0000:0100                       30 1F 00 C8-65 F0 00 F0 00 28 00 C0      0...e....(..
0000:0110  84 60 00 F0 84 60 00 F0-01 E4 00 F0 84 60 00 F0  .`...`.......`..
0000:0120  84 60 00 F0 84 60 00 F0-84 60 00 F0 84 60 00 F0  .`...`...`...`..
0000:0130  84 60 00 F0 84 60 00 F0-84 60 00 F0 84 60 00 F0  .`...`...`...`..
0000:0140  84 60 00 F0 84 60 00 F0-84 60 00 F0 84 60 00 F0  .`...`...`...`..
0000:0150  84 60 00 F0 84 60 00 F0-84 60 00 F0 84 60 00 F0  .`...`...`...`..
0000:0160  84 60 00 F0 84 60 00 F0-84 60 00 F0 84 60 00 F0  .`...`...`...`..
0000:0170  84 60 00 F0 84 60 00 F0-84 60 00 F0 84 60 00 F0  .`...`...`...`..
0000:0180  00 00 00 00                                      ....
-dc800:1f00
C800:1F00  57 45 53 54 45 52 4E 20-44 49 47 49 54 41 4C 24  WESTERN DIGITAL$
C800:1F10  01 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1F20  C8 03 09 00 00 FF FF 00-C0 00 00 00 00 00 23 00  ..............#.
C800:1F30  C8 03 09 00 00 FF FF 00-08 00 00 00 C8 03 22 00  ..............".
C800:1F40  C8 03 10 00 00 FF FF 00-08 00 00 00 C8 03 11 00  ................
C800:1F50  25 01 10 00 00 FF FF 00-08 00 00 00 25 01 3F 00  %...........%.?.
C800:1F60  37 36 39 00 00 00 00 00-00 00 00 00 00 00 00 00  769.............
C800:1F70  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-
-d
C800:1F80  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1F90  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1FA0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1FB0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1FC0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1FD0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1FE0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00  ................
C800:1FF0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 9E  ................
```

FIG. 2

4. If, in using the above methods you verify that the system BIOS does contain the physical parameter tables for your drives, you need to use WDFMT to low level format the drive, FDISK (MSDOS 3.3) to partition it and finally the 'FORMAT C:(D:)/S' to high level format.

SEE FIGURE 2 FOR AN ILLUSTRATION OF THE ABOVE METHODS OF DETERMINING IF THE PHYSICAL DRIVE PARAMETERS ARE LOCATED IN THE SYSTEM BIOS.

5.0 USING THE 1007A BIOS

1. Before using the BIOS, make sure the proper address range is selected on W1 and W2. Confirm that the BIOS is enabled (jumper on W3).

2. Enter the BIOS routine through the DOS DEBUG utility. Execute the DEBUG utility and at the program prompt "-", type:

G=C800:5 <CR>

Depending upon the settings of W1 and W2, this causes the system to execute program code stored at location 5 in ROM. The BIOS then tries to read the parameter tables from the drive and store them in the shadow RAM. If the drive has not been formatted the BIOS will return a message of "drive not initialized". The user will see the following on the screen:

```
*** Western Digital 1007A-WA2 Initialization Utilities, Rev. 1.0***
   PRESENT DRIVE SETUP ... + or - to change, <ENTER> for selection

DRIVE 0 CYLINDERS XXX HEADS XX PRECOMP CYLINDER XXX SPT XX
DRIVE 1 CYLINDERS XXX HEADS XX PRECOMP CYLINDER XXX SPT XX

Change Drive Types     ---> 1
Low Level Format       ---> 2
Surface Analysis       ---> 3
Verify Drive           ---> 4
Enter Defect List      ---> 5
Exit and Reboot        ---> 6

Enter Choice (1-6) -->
```

3. All functions can be executed by simply entering the number for the desired routine. The BIOS will execute that routine and then prompt the user to press a key to return to the main menu. Note that all changes made while in the BIOS will only be finalized after a proper exit through function 6 - otherwise some features might not be valid including drive type selected.

A. Drive type routine

The drive types can be changed by using the "+" and "-" keys. Assuming that all the ESDI drives in question are specified at 34 SPT, there are four possible choices that can be implemented for a drive:

A.1 No drive present. The BIOS will automatically select a drive type 0 if there is no drive present. The user will get the message "*** NONE SELECTED OR NO DRIVE PRESENT ! ***" next to the drive number.

A.2 A selection with 17 SPT. This feature should be used when the drive is being used in a system that does not recognize drives with SPT values other than 17 SPT. Although the low level format will still be at 35 SPT, logical parameter tables will be created reflecting 17 SPT (with translation enabled). See section on Translations for more details.

A.3 A selection with 34 SPT. This feature should be used, if the system being used recognizes the standard 34 SPT drive.

A.4 A selection with 63 SPT. This feature should be implemented only when the drive in question is specified as having greater than 1024 cylinders. Translation should always be enabled when such a condition exists. What this feature does is to allow full use of all the cylinders of the drive (even though most AT BIOS' only recognize 1024 cylinders as a maximum) through a translation scheme that uses 63 SPT.

B. Low Level Format Routine

Formatting routines are present to do the low-level initialization of the disk surface. The drive is formatted at 35 sectors/track (SPT). Transparent to the user, the format routine formats with a sector skew and also formats a spare sector on each track. This sector is used by the surface analysis routines to provide the ability to reallocate a bad sector on a track. It is also used to store the parameter information generated by the BIOS. This information is written to the spare sector on cylinder 0, head 0. The sector skew, which is fixed at two, allows the controller to maintain a one to one interleave across all head boundaries. Sector Skewing is a method of formatting in which the sector numbers are rotated in the interleave table for each track.

C. Enter defect list routine

This routine allows the user to enter the list of 'bad tracks' as listed by the drive manufacterer on the drive.

D. Surface analysis routine

A surface analysis routine is available that identifies bad tracks on the drive and in the event that there is only one sector bad on the track (and it is NOT sector zero), assigns the alternate sector (sector 35) in the place of the bad one. This 'saves' the track from being marked bad by the controller.

If one had entered a list of the 'bad tracks' at the begining of this routine, after the surface analysis, all the tracks marked bad will now be error free (within the constrictions of the above paragraph).

E. Verify drive routine.

The verify routine will identify all the 'bad tracks' on the drive and list them by head and cylinder number. Use the FDISK and FORMAT utilities to prepare

4. 1005 mode as opposed to the 1007 mode: If it is desired to format a drive at a value other than 35 SPT the board should be configured to be in the 1005-WAH mode (Jumper W8). In this mode the the controller will format the drive at this value as long as the drive is configured to reflect this SPT value. The WD1007A BIOS will read the drive parameters off the drive in this mode and will allow a low level format at the read values with no skew, no alternate sector, and a 1:1 interleave. The only exception to this is if the drive is configured to be at 36 SPT; for this mode, a 2:1 interleave has to be used.

5. If one is using a 5 MB/S ESDI drive the 1007A translation feature should be disabled (jumper W14). This type of ESDI drive is always configured at 17 SPT.

SEE FIGURES 3-7 FOR AN ILLUSTRATION OF THE VARIOUS BIOS FUNCTIONS.

6.0 WDFMT

Western Digital provides a low-level format utility that will allow the user to prepare the drive for use by the system. The program includes routines for low-level formatting, disk verify, surface analysis and bad track entry. When using the 1007A board one should use an interleave of 1, a skew on 2 and format at 35 SPT with an alternate sector. See the explanations for these features provided below. WDFMT 2.10 presents the following display:

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE, <ENTER> for SELECTION

DRIVE 0  CYLINDERS 968   HEADS 9   SPT 35   *** Drive NOT initialized ! ***
DRIVE 1  *** NONE SELECTED or NO DRIVE PRESENT ! ***

 Change Drive Types  ---> 1
 Low Level Format  ------> 2
 Surface Analysis  ------> 3
 Verify Drive  ----------> 4
 Enter Defect List  ----> 5
 Exit and Reboot  -------> 6

 Enter Choice (1-6) ----> 2 ... FORMAT
   Files will be LOST ... are you sure ? (Y/N) y
   Enter drive (0/1) 0
   FORMATTING ... head 8   cylinder 967
   FORMAT SUCCESSFUL ... Use DOS "FDISK" AND "FORMAT".

   Hit any key to return to Menu ...
```

ABOVE ARE THE PHYSICAL PARAMETERS OF A CDC WREN III.
WE HAVE JUST PERFORMED A LOW LEVEL FORMAT WITH 1:1 INTERLEAVE,
SKEW OF 2 SECTORS PER TRACK AND WITH ALTERNATE SECTOR.

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE, <ENTER> for SELECTION

DRIVE 0  *** NONE SELECTED or NO DRIVE PRESENT ! ***
```

TYPE + AS MANY TIMES AS YOU LIKE, UNTIL YOU HAVE THE LOGICAL
TABLE YOU WANT, THEN TYPE ENTER.

FIG. 3

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE, <ENTER> for SELECTION

DRIVE 0  CYLINDERS 748   HEADS 16  SPT 17


      ABOVE IS THE 17 SECTOR TABLE TO BE USED WITH EARLIER OPERATING
      SYSTEMS THAT ALWAYS EXPECT 17 SECTORS PER TRACK.
```

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE, <ENTER> for SELECTION

DRIVE 0  CYLINDERS 293   HEADS 16  SPT 63


      ABOVE IS THE 63 SECTOR TABLE TO BE USED IF YOUR DRIVE HAS MORE
      THAN 1024 CYLINDERS AND YOUR SYSTEM BIOS CANNOT HANDLE THAT MANY
      CYLINDERS.
```

FIG. 4

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE. <ENTER> for SELECTION

DRIVE 0  CYLINDERS 968   HEADS 9   SPT 34
```

ABOVE IS THE 34 SECTOR TABLE WHICH PROVIDES AN ALTERNATE SECTOR PER TRACK, WHICH IS USED BY THIS UTILITY IN THE EVENT OF A BAD SECTOR.

WE WILL USE THIS ONE ... TYPE ENTER.

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE, <ENTER> for SELECTION

DRIVE 0  CYLINDERS 968   HEADS 9   SPT 34
DRIVE 1  *** NONE SELECTED or NO DRIVE PRESENT ! ***

 Change Drive Types  ---> 1
 Low Level Format  ----> 2
 Surface Analysis  -----> 3
 Verify Drive  ---------> 4
 Enter Defect List  ----> 5
 Exit and Reboot  ------> 6

 Enter Choice (1-6) ----->
```

AT THE MENU NOW, LET'S DO A VERIFY ... TYPE 4.

FIG. 5

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE, <ENTER> for SELECTION

DRIVE 0  CYLINDERS 940   HEADS 9   SPT 34
DRIVE 1  *** NONE SELECTED or NO DRIVE PRESENT ! ***

 Change Drive Types  ---> 1
 Low Level Format  ------> 2
 Surface Analysis  -----> 3
 Verify Drive  ----------> 4
 Enter Defect List  ----> 5
 Exit and Reboot  ------> 6

 Enter Choice (1-6) -----> 4 ... VERIFY
   Enter drive (0/1) 0
   TESTING .....  head 8   cylinder 37   BAD TRACK
   TESTING .....  head 1   cylinder 43   BAD TRACK
   TESTING .....  head 2   cylinder 380   BAD TRACK
   TESTING .....  head 8   cylinder 967

   Hit any key to return to Menu ...
```

YOU WILL NOTICE THAT WE FOUND 3 BAD SECTORS.

WE WILL NOW DO A SURFACE ANALYSIS ... TYPE 3 AT THE MENU.

FIG. 6

```
* * *  Western Digital WD1007A-WA2 Initialization Utilities, Rev. 1.0  * *

   PRESENT DRIVE SETUP ... + or - to CHANGE, <ENTER> for SELECTION

DRIVE 0  CYLINDERS 968   HEADS 9   SPT 34
DRIVE 1  *** NONE SELECTED or NO DRIVE PRESENT ! ***

 Change Drive Types  ---> 1
 Low Level Format  -----> 2
 Surface Analysis  -----> 3
 Verify Drive  ----------> 4
 Enter Defect List  ----> 5
 Exit and Reboot  ------> 6

 Enter Choice (1-6) ----> 3 ... SURFACE ANALYSIS
   Files will be LOST ... are you sure ? (Y/N) y
   Enter drive (0/1) 0
   Enter manufacturer's DEFECT list . ( <ENTER> to end )
   CYLINDER 37     HEAD 8    BYTE COUNT AFTER INDEX 8054   ALTERNATE ASSIGNE
   CYLINDER 43     HEAD 1    BYTE COUNT AFTER INDEX 18245   ALTERNATE ASSIG

   CYLINDER 380    HEAD 2    BYTE COUNT AFTER INDEX 9293   ALTERNATE ASSIGNE
   CYLINDER        HEAD      BYTE COUNT AFTER INDEX
   TESTING .....   head 8    cylinder 136   ALTERNATE ASSIGNED
   TESTING .....   head 4    cylinder 315
```

WE ENTERED THE 3 BAD SPOTS LISTED ON THE DRIVE AND THE SURFACE ANALYSIS FOUND ONE MORE AND ASSIGNED AN ALTERNATE. IF WE DID A VERIFY NOW, WE WOULD HAVE AN ERROR FREE DRIVE.

FIG. 7

```
*** Western Digital Corporation ***
      AT Disk Format Utility
            Rev. 2.10
   Current drive parameters are:
       Drive (0/1)  :      0
       Cylinders    :    615
       Heads        :      4
       Sectors      :     17
       Interleave   :      3
       Precomp      :    306
       Skew         :      0
       Alt Sector   :     No

       ENTER MENU CHOICE

Format disk    CAUTION this will destroy all data on drive!
Verify disk
Bad sector entry
Surface test   CAUTION this will destroy all data on drive!
Quit
```

A. Sector Skewing

Sector Skewing is a method of formatting a drive in which sector numbers are rotated in the interleave table each time a new head on a cylinder is formatted. For example, using a 2 sector skew, the first sector after index on head 0 will be identified as sector 1. The sector identified as sector 1 on head 1 will be the third physical sector from index.

Sector Skew formatting is available with version 2.10 of WDFMT.

Example: Ten sectors per track with a skew of 2 and interleave of 1

Head #	Sector #'s
0	1 2 3 4 5 6 7 8 9 10
1	9 10 1 2 3 4 5 6 7 8
2	7 8 9 10 1 2 3 4 5 6

This formatting procedure allows the controller to maintain the 1:1 interleave when reading across the head boundary. This becomes critical when the number of sectors per track increases and the time allowed for overhead functions to be completed decreases as with ESDI applications. Because of controller firmware overhead, the controller will not be able to read the ID Field of the first sector on the next head. By changing the sector numbers, the controller can do the needed tasks and be ready to

read the sector marked as number 1. The minimum sector skew factor for proper performance of the WD1007A has been determined to be 2. Different skew factors may be needed to optimize performance for different applications.

B. Sector Spare

Another option available in WDFMT Version 2.10 is the ability to format a spare sector on the track. This spare sector is given the ID of zero, making it invisible to the AT compatible System BIOS, which expects sector numbers starting at 1. This sector is always formatted as the last physical sector on the track.

The surface analysis portion of WDFMT will use that spare sector if an error is encountered with any sector on the given track. The program will reformat the track, numbering the bad sector as zero and shifting the following sectors one to the right. If more than one sector is found to be bad on the track, the entire track is marked as bad when reformatted.

This feature is useful since many system BIOS ROMS that support ESDI drives have a sector per track parameter of 34. By using the spare sector option, the drive will look like it has only 34 sectors. The spare sector can be used for the above mentioned bad sector reassignment, or it can be used to store custom data by providing software drivers to use the hidden sector.

WESTERN DIGITAL
CORPORATION

PRELIMINARY
Data Sheet

WD1007A—WAH/2

February 17, 1988

WD1007A-WAH/WA2 WINCHESTER/FLOPPY DISK CONTROLLER

FEATURES

- PC-AT compatible Winchester and floppy disk controller
- ESDI Drive Interface
- Utilizes maximum storage capacity of ESDI drives
- Controls up to two fixed disk drives and two floppy disk drives (5.25 or 3.5 inch)
- 84-pin Buffer Management and Control (AMAC) gate array
- Optional BIOS ROM
- Supports 1:1 interleave
- Data transfer rate of 10 Mbits per second
- Supports NRZ disk data format
- Two 8192 x 8 RAMs for look-ahead read caching to reduce disk access time and increase data throughput
- Software selectable 56-bit ECC
- Multiple sector read/write commands

DESCRIPTION

The WD1007A-WA2 Winchester/Floppy Disk Controller (WFDC) module interfaces two ESDI-compatible fixed disk drives and two 5-1/4 inch floppy disk drives to the PC-AT computer I/O Channel bus structure. An optional BIOS ROM provides parameter tables, low-level formatting and surface analysis routines to fully integrate ESDI drive capabilities into the system.

The fixed disk section of the module includes the WD50C12 Winchester Disk Controller, the WD1018 Buffer Manager/Control Processor, sector buffer RAM and associated control logic. The WD37C65 Floppy Disk Controller (FDC) implements the optional floppy disk control section. The WD12C00A (AMAC) gate array also provides buffering and control. The AMAC reduces module logic and supports a 1:1 interleave format.

BLOCK DIAGRAM

A description of the functional blocks of the WD1007A-WA2 Winchester/Floppy Disk Controller (WFDC) appears below. Refer to the block diagram in Figure 1.

WD50C12 Winchester Disk Controller

The WD50C12 Winchester Disk Controller (WDC) is an advanced VLSI device that controls and coordinates the activity of the hard disk drive. The WDC supports 1:1 interleave and data transfer rates up to 10 Mbits per second. It utilizes the maximum storage capacity of ESDI drives by translating physical parameters into logical parameters for those operating systems which do not

recognize more than 17 sectors per track or more than 1048 cylinders per drive. (See Translation in the Appendix for an explanation of this feature). The WDC offers software selectable 56-bit ECC and supports the NRZ data format.

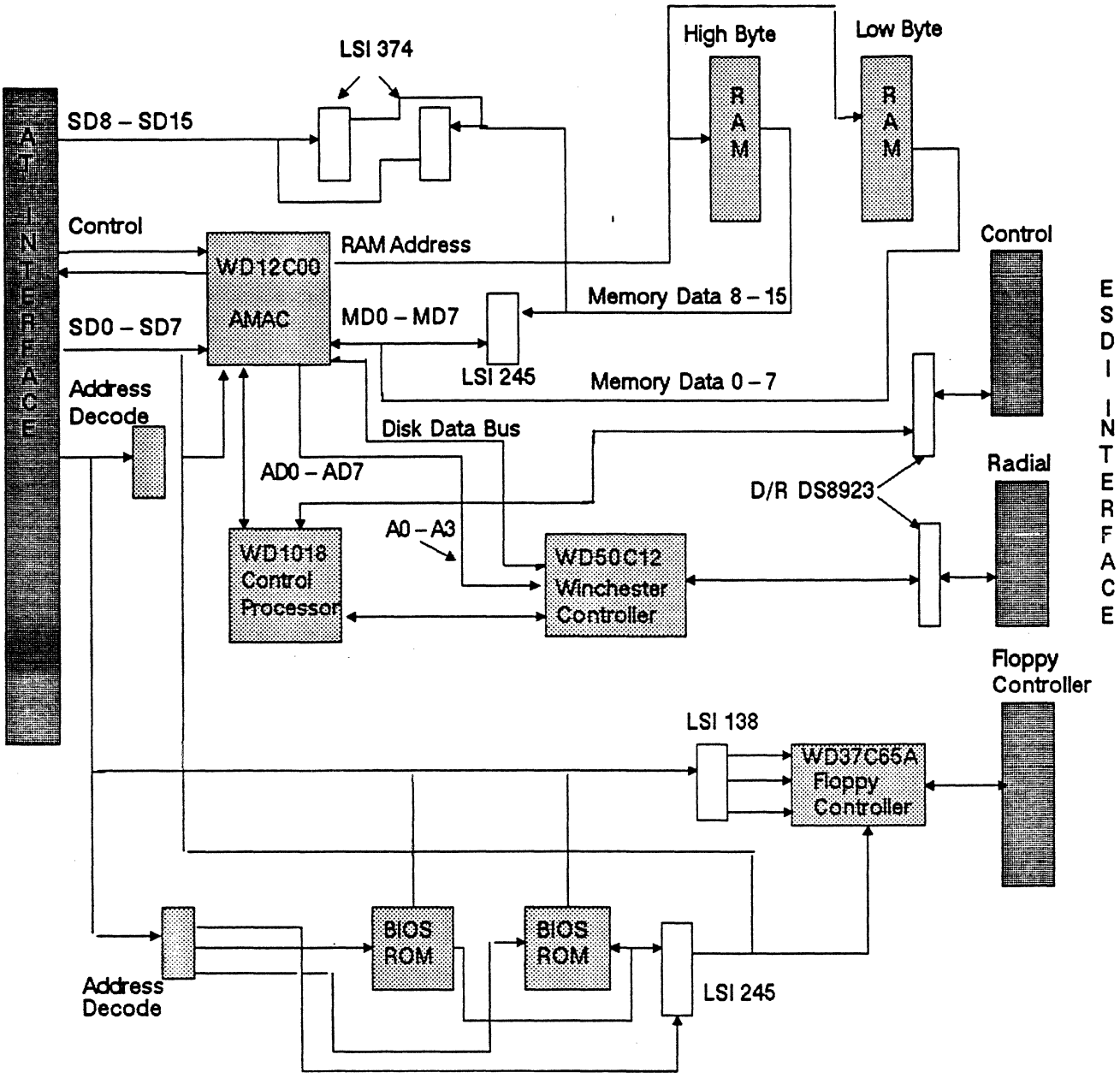


FIGURE 1. WD1007A-WA2 BLOCK DIAGRAM

WD1018 Buffer Manager/Control Processor

The WD1018 Buffer Manager/Control Processor is an eight-bit microcontroller that operates with the WD50C12 and the AMAC logic array to facilitate processing of disk commands. It provides sector data buffer management, helps in error recovery procedures and performs module diagnostics. The processor chip includes internal RAM and ROM memory.

WD12C00A-JU22 Logic Array (AMAC)

The primary function of the AMAC logic is to provide host address and command decoding, task file control and data buffering. The VLSI logic array replaces the standard WD1014 support device and several SSI/MSI components. This simplifies the logic and lowers power consumption. The AMAC logic includes the data and address registers, memory read/write control, and WD50C12 task file image registers. It interfaces to both the system and module (local) bus structures. (See Figure 2. AMAC Block Diagram)

RAM Data Buffer

Two 8192 x 8 static RAM memories buffer the sector data between the drive(s) and the PC-AT system bus. They also buffer Error Correction Code (ECC) information between the WD50C12 disk controller and the WD1018 control processor. The sector buffers and the above control components provide a 1:1 sector interleave format for optimal system performance.

WD37C65 Floppy Disk Controller (FDC)

The optional WD37C65 Floppy Disk Controller (FDC) is a standard VLSI device that supports both single and double density diskette formats and provides data and control interfaces for the host and the floppy drive. The units major features include:

- Multiple sector and track read/write commands
- Host DMA and programmed I/O data transfers
- High performance digital data separation

BIOS (P)ROM/RAM Option

Controller circuitry accommodates a programmed BIOS device for special applications. One unique feature of this BIOS option is its shadow RAM. The static RAM (which shares with the BIOS (P)ROM the last 256 upper address bytes of BIOS's 8 Kbyte address range) contains the Winchester drive's parameters. This shadow-RAM feature allows the WFDC to interface with all types of ESDI drives without modifying the system BIOS. Option jumpers

allow the device to be mapped at 1 of 4 address ranges. For more information, refer to the jumper configuration tables on page 13 and to the Appendix.

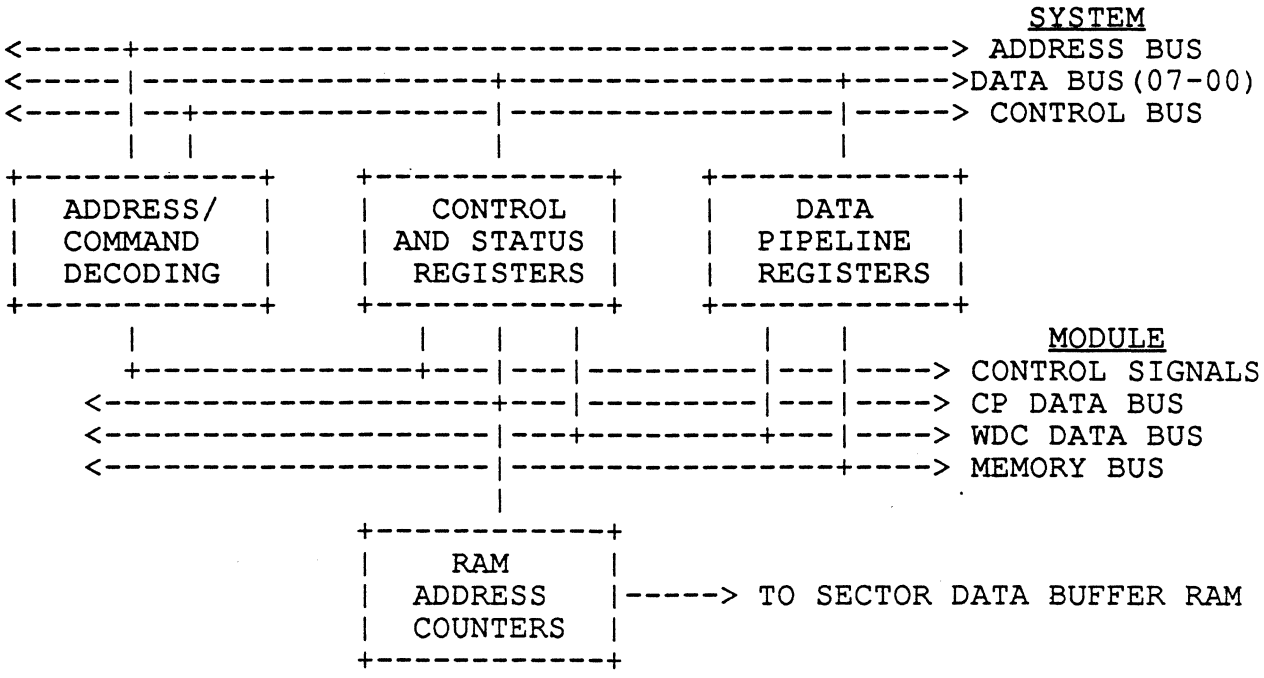


FIGURE 2. AMAC BLOCK DIAGRAM

INTERFACE DESCRIPTION - HARDWARE

System Bus Interface

The WFDC interfaces with the system bus address to transmit data and I/O control signals. All fixed disk read/write data transfers are 16-bits wide and utilize the host I/O transfer protocol. Floppy disk data, fixed disk control, floppy disk control, and status transfers are 8 bits wide and use the lower data byte (SD07-00) only. The register address map of the WFDC module is fixed (at a primary or secondary range) as are the bus interrupt requests and the Floppy DMA channel assignment.

Tables 1 and 2 below provides the pin descriptions for the P1 and P2 system bus connectors.

TABLE 1. SYSTEM INTERFACE CONNECTORS (P1) - PIN DESCRIPTION

Pin	Signal	Description
A02-A09	SD07-SD00	System Data Bus. Transfers 16-bit fixed disk data, 8-bit floppy data and 8-bit module control and status information.
A11	AEN	Address Enable. Indicates a valid I/O address is on the system bus. The AMAC decode logic uses this term to qualify the I/O address decoding.
A12-A31	SA19-SA00	System Address Bus. Selects the WFDC I/O addresses and BIOS ROM addresses.
B01,B10, B31	GND	Ground
B02	RST	Reset
B03,B29	VCC	
B06	DRQ2	DMA Request Level 2. When a data byte is ready for transfer to or from the host memory, the WD37C65 floppy controller generates this signal.
B09	VDC	+12 Volts
B11	-SMEMW	System Memory Write. Input strobe used to write drive parameters in the Shadow RAM.
B12	-SMEMR	System Memory Read. Enables BIOS ROM and shadow RAM.

B13	-IOW	I/O Write. Asserted by the system processor during bus 'write' cycles. The WFDC uses this strobe and the decoded bus address to input both data and command information.
B14	-IOR	I/O Read. Asserted by the system processor during bus 'read' cycles. The WFDC uses the signal (along with the system address bus decoding or DMA ACK signal) to enable system I/O reads of both data and command information.
B22	IRQ6	Interrupt Request Level 6. Floppy controller interrupt request to the system processor indicating that the WD37C65 has completed the execution phase of a command or that the selected 'drive ready' line has changed state. Reading the result phase status or issuing a 'Sense Interrupt Status' command will clear the IRQ6.
B26	-DACK2	DMA Acknowledge Level 2. Indicates the completion of a data byte transfer. The DMA controller provides bus control and system memory address.
B27	T/C	DMA Terminal Count. The WD37C65 terminates the data transfer sequence for read, write or scan commands when the DMA controller issues this signal.
B28	BALE	Bus Address Latch Enable. Input control signal used to initiate a data transfer on the system bus. The WFDC uses this input to generate the I/O transfer control signal and to enable control signals for high-order data bytes.

TABLE 2. SYSTEM INTERFACE CONNECTORS (P2) - PIN DESCRIPTION

Pin	Signal	Description
C18-C11	SD15-SD08	System Data Bus. Transfers 16-bit fixed disk data, 8-bit floppy data and 8-bit module control and status information.

D02	-I/OCS16	I/O Control Signal 16. Indicates 16-bit data transfer mode. The WFDC asserts this signal for all hard disk data transfers.
D07	IRQ14	Interrupt Request Level 14. Output to the processor from the fixed disk control requesting a data block transfer or indicating command completion. The level clears on a subsequent fixed disk command to the WFDC or a system reset.
D16	VCC	
D18	GND	Ground

Winchester Drive Interface

The WFDC module interfaces to the fixed disk drives via one 34-pin control cable (J1) and two 20-pin data cables (J2,J3) in conformance with ESDI signal definitions. The WFDC module does not furnish drive power. Signal descriptions appear in Tables 3 and 4.

TABLE 3. FIXED DISK DRIVE CONTROL CONNECTOR (J1)

Pin	Signal	Description
1,3,5,7, 9,11,13,15, 17,19,21,23, 25,27,29,31,33	GND	Ground - Pin 15 keys the connector.
2,4, 18,14	HS3-/0-	Head Select. Binary-coded select signals allows selection of drives with up to 16 read/write heads.
6	WRG-	Write Gate. Enables the selected drive to accept write data. A write fault condition or a module reset will clear this signal.
8	CSD-	Configuration/Status Data. Data from the selected drive in response to controller command.
10	TXACK-	Transfer Acknowledge. Handshake response from selected drive acknowledging the controller's transfer request. The drive then

		accepts command/data or returns configuration/status information.
12	ATN-	Attention. Control signal from the selected drive that indicates the drive has a faulty condition or a change of status. This signal is active also during drive power-up sequence.
16	SCT-	Sector Pulse (or Address Mark Found). Sector clock from the selected drive. Used for hard sectored format to mark the beginning of each sector. Used for soft sectored format to flag detection of an address mark.
20	INDEX-	Index. Positioning signal from the drive that occurs once per drive revolution. Used by the WDC for track formatting and command timeout.
22	DRDY-	Drive Ready. Control signal from the drive indicating the drive's motor is up to speed and that the I/O control signals are valid.
24	TXREQ-	Transfer Request. This control signal sets for command/data information transfers to the drive or for configuration/status information transfers from the drive.
26 28	DS0- DS1-	Drive Select. WFDC selects only Drive 0 or 1.
32	RG-	Read gate. Enables the selected drive to send read data. Controls the drive VCO and data recovery circuit.
34	CMDDAT-	Command Data. Sixteen-bit serial data plus parity sent to the selected drive. Data contains instructions for drive execution, i.e., recalibrate, seek, request status.

TABLE 4. FIXED DISK DATA CONNECTORS (J2, J3)

Pin	Signal	Description
1	DSLTD 0,1-	Drive Selected. Status signal from the drive informing the controller of the selection status after it has asserted a drive selection signal.
3	CMDCPLT 0,1-	Command Completed. Status signal from each drive indicating completion of any command.
4	AME 0,1-	Address Mark Enable. Control output to each drive used to write address mark onto the disk or search for address mark.
5,6,15,16,19	GND	Ground
7 8	WCLOCK 0,1+ WCLOCK 0,1-	Write Data Clock. Differential signal for synchronizing write data operations. Derived from reference clock.
10 11	RCLK 0,1+ RCLK 0,1-	Read/reference clock. Differential signal from the drive used to determine data transfer rate. The drive's data recovery circuits supply the read clock during read data transfers. At all other times the drive furnishes the reference clock.
13 14	WDATA 0,1+ WDATA 0,1-	Differential write data to be written to each drive.
17 18	RDATA 0,1+ RDATA 0,1-	Differential read data input from each drive.

Floppy Drive Interface

The controller interfaces to the floppy drives via one 34-pin data and control cable (J4) per the 5 1/4" PC-AT standard. Table 5 below provides the pin descriptions.

TABLE 5. FLOPPY DISK DRIVE INTERFACE (J4)

Pin	Signal	Description
1,3,5,7,9,11,13, 15,17,19,21,23, 25,27,29,31,33	GND	Ground - Pin 5 keys the connector.
2	DRATESLCT	Dual Rate Select. Selects either 360 rpm or 300 rpm for dual-speed drives.
8	IDX-	Floppy Index Pulse. Positioning signal used by the FDC to indicate the beginning of a disk track.
10 16	MO1- MO2-	Floppy drive motor enable.
12 14	FDS2- FDS1-	Floppy Drive Select 1 and 2. Select signals from the FDC operations register. A system master reset or a software reset will inactivate these signals.
18	DIRC-	Direction Control. Determines the head 'step' direction of a selected drive during controller seek operations. When asserted (low), the step direction is toward the inner tracks.
20	STEP-	Step. Step pulses to the selected drive from the FDC. FDC's Specify command controls the rate.
22	FWD-	Floppy write (MFM or FM). Data input to selected drive.
24	FWE-	Floppy Write Enable. Enable signal from FDC to selected head.
26	TRK0-	Floppy Track 0. During seek operations, the selected drive issues a positioning flag to indicate head position over the outermost track.

28	FWP-	Floppy Write Protect. Write protect status from selected drive.
30	FRDD-	Floppy read data. Output from selected drive.
32	FHS-	Floppy Head Select. Head select signal to the active drive. A low signal selects Head 1.
34	DCHG-	Diskette change status. Used for host control of diagnostic information.

FIGURE 3. CONTROLLER MODULE LAYOUT

Figure 3 illustrates the general module jumper placement and approximate connector locations. The module dimensions are 13.12 by 4.2 inches and a mounting bracket is included. Jumper configurations for the WFDC module appear in Table 6.

WFDC Configuration

Table 6 below lists the default settings for the WD1007A-WA2 which supports two 5-1/4 inch drives. The WD1007A-WAH is a hard disk only version of the controller.

TABLE 6. JUMPER DEFAULT SETTINGS

Jumper Function	WD1007A-WA2		WD1007A-WAH	
BIOS Address Select	W1	2-3	W1	2-3
BIOS Address Select	W2	2-3	W2	2-3
BIOS Shadow RAM Enable	W3	Jumper	W3	Jumper
Floppy Enable	W4	No Jumper		
Dual Spindle Speed Enable	W5	No Jumper		
Floppy Address Select	W6	2-3		
Floppy Drive Type	W7	1-2		
5WAH Mode Select	W8	No Jumper	W8	No Jumper
Chassis ground	W9	No Jumper	W9	No Jumper
Digital Input Register	W10	No Jumper	W10	No Jumper
Diskette Change Enable	W11	Jumper	W11	No Jumper
Secondary Address Select	W12	No Jumper	W12	No Jumper
In Etch	W13	Uncut		
Translate Override	W14	No Jumper	W14	No Jumper
ECC Length	W15	No Jumper	W15	No Jumper

Address Select Jumpers

Jumper connections W1-W2 select the BIOS ROM/RAM memory addresses. The default address range (C8000 - C9FFF) is factory set. Jumper connection W3 enables the ROM/RAM BIOS when it is jumpered.

Jumper connecton W6 selects the floppy drive's address ranges. The default range is 3FX.

The module's primary hard disk address range is (1F0-1F7 and 3F6-3F7). To select the secondary hard disk address range (170-177 and 376-377), jumper the W12 connector.

TABLE 7. ADDRESS SELECT JUMPERS

BIOS ADDRESS RANGES	JUMPER SETTINGS W1	W2	W3
C8000 - 09FFF	2 - 3	2 - 3	Jumper
CA000 - CBFFF	2 - 3	1 - 2	Jumper
CC000 - CDFFF	1 - 2	2 - 3	Jumper
CE000 - CFFFF	1 - 2	1 - 2	Jumper
FLOPPY ADDRESS RANGES	W6		
37X	1 - 2		
3FX	2 - 3		
PRIMARY/SECONDARY HARD DISK ADDRESSES	W12		
1FX	No Jumper		
17X	Jumper		

Diagnostic Register Latch Control

When installed, jumper connection W10 enables the diagnostic Digital Input Register for operation in the latched mode; i.e., the register outputs latch when the register is accessed. The jumper is normally not used.

WD1018 Mode Control

Jumper connections W8, W14, W15 provide three external mode selects to the control processor.

W8

No Jumper - This is the normal WD1007A-WAH/WA2 mode. The firmware forces a 10 Mhz ESDI drive to 35 sectors per track when using the Set Unformatted Bytes per Sector command. This mode supports a 1:1 interleave.

Jumper - This is the WD1005-WAH mode. It allows the 1007A-WAH to be used as a replacement board for existing WD1005-WAH boards without reformatting the drive. It provides 36 sectors per track, a 2:1 interleave, and use of the Set Unformatted Bytes per Second command. This eliminates the need to set the drive's jumpers and switches for the desired number of sectors per track.

W14

Because some of the older operating systems can only recognize 17 sectors per track or a maximum of 1048 cylinders per drive, the

WD1007A-WA2 provides a translation scheme so that ESDI hard disk drives can be fully utilized in the PC/AT environment.

No Jumper - The translation mode provides two types of physical to logical translation. See Translation, page 39 for explanation.

Jumper - Physical to logical translation by the firmware is disabled.

W15

The purpose of this jumper is to support either four or seven bytes of syndrome during Read or Write Long commands. Four bytes of ECC is the default mode. Installing the jumper provides seven bytes of ECC.

Floppy Drive and Data Rate Selection Control

Jumper connection W5 selects either single speed or dual speed drive type. A jumper is not normally installed causing selection to default to a single speed drive and 125 nanoseconds precompensation.

The WD1007A-WA2 supports 5 1/4 inch, 1.2 Megabyte or 360 Kbyte floppy disk drives. W7 (1 - 2) must be jumpered to select the 1.2 Megabyte drive option.

Jumper connectors W4 and W13 enable the floppy drive controller.

FLOPPY CONTROLLER	W4	W13 IN ETCH
ENABLE	No Jumper	Uncut
DISABLE	Jumper	Cut

Jumper W11 is the disk change input signal, and must be jumpered if floppy drives are installed.

Mounting Bracket Jumper

Jumper connection W9 allows grounding of the module mounting bracket to chassis or logic ground. The jumper is not normally used.

	W9
Chassis ground connected	2 - 3
Digital ground disconnected	1 - 2

INTERFACE DESCRIPTION - SOFTWARE

Register Address Map

Table 8 summarizes the WFDC I/O Register Address Map and includes the WD50C12 task file area, the WD37C65 registers and the module auxiliary support registers. It lists the primary address first with the secondary address shown within parentheses.

TABLE 8. REGISTER ADDRESS MAP

ADDRESS (HEX)	REGISTER	FUNCTION
1F0 (170) RW	HDDTR	Hard Disk Data Register (16 bits)
1F1 (171) WO	HDPLO	Gap, ID PLO and Data PLO Lengths
1F1 (171) RO	HDERR	Error Register
1F2 (172) RW	HDSCT	Sector Count
1F3 (173) RW	HDSSN	Starting Sector Number
1F4 (174) RW	HDCLL	Cylinder Number - Low Byte
1F5 (175) RW	HDCLH	Cylinder Number - High Byte
1F6 (176) RW	HDSDH	Sector Size, Drive/Head Select
1F7 (177) WO	HDCMD	Command Register
1F7 (177) RO	HDSTT	Status Register
3F2 (372) WO	FDDOR	Floppy Digital Operations Register
3F4 (374) RO	FDMSR	Floppy Main Status Reg (WD37C65)
3F5 (375) RW	FDDTR	Floppy Data Registers (WD37C65)
3F6 (376) WO	HDFDR	Fixed Disk (Control) Register
3F6 (376) RO	HDASR	Alternate Status Register
3F7 (377) WO	FDFCR	Floppy Control Register
3F7 (377) RO	HDDIR	Digital Input Register

Task File Registers

Table 9 summarizes the fixed disk Task File Registers (addresses 1F1/171 through 1F7/177) and their bit assignments with respect to the system processor's lower-byte bus terms (SD07-00).

Host access to these registers is always via the register image contained within the AMAC. The WD1018 control processor has access to both the AMAC and WD50C12 register set.

TABLE 9. TASK FILE REGISTERS

REGISTER	7	6	5	4	3	2	1	0
HDPLO	GAP, ID PLO AND DATA PLO LENGTHS							
HDERR	BBD	ECC	0	INF	0	ACD	TK0	DNF
HDSCT	NUMBER OF SECTORS							
HDSSN	STARTING SECTOR NUMBER							
HDCLL	CYLINDER NUMBER LSB							
HDCLH	0	0	0	0	0	CYL NUMBER MSB		
HDSDH	1	SECTOR		DN	HS3	HS2	HS1	HS0
HDCMD	COMMAND							
HDSTT	BSY	RDY	WFT	SKC	DRQ	CRD	CIP	ERR

WFDC Control and Status Registers

Hard Disk Alternate Status Register (HDASR) 3F6/376 (RO)

This register lies within the AMAC array and provides fixed disk status to the system processor. The register contains a 'real time' section (bits 7, 6, 3 and 1) and a 'register' section set by the control processor at sector transfer time (bits 5, 4, 2 and 0).

TABLE 10. ALTERNATE STATUS REGISTER

7	6	5	4	3	2	1	0
BSY	RDY	WFT	SKC	DRQ	CRD	IDX	ERR

where:
BSY = Controller Busy Flag
RDY = Ready from selected drive
WFT = Write Fault Flag from WD1018
SKC = Seek Complete Flag from WD1018
DRQ = Data Transfer Request Flag
CRD = Corrected Data Flag from WD1018
IDX = Index Pulse from selected drive
ERR = Error Flag from WD1018

The Alternate Status Register reflects the same status as the WD50C12 Status Register, except for bit position 1 which holds the drive index signal instead of the Command in Progress (CIP) flag. The index bit does not latch and thus follows the drive control signal (approximately a 200 microsecond pulse every 16.7 milliseconds).

The Write Fault bit sets for all the ESDI error conditions. The host processor detects a drive's error by issuing the Initiate ESDI command to read the drive's status.

The host processor can interrogate the register at any time without interfering with other control functions. The host status input at this address will not clear the fixed disk interrupt.

Hard Disk Diagnostic Input Register (HDDIR) 3F7/377 (RO)

The fixed disk Diagnostic Input Register reflects the current state of the floppy diskette change flag and the fixed disk Drive Select, Head Select and Drive Write gate signals (complimented form). When the floppy disk option is not installed, bit 7 remains tri-state.

TABLE 11. WFDC DIAGNOSTIC INPUT REGISTER

7	6	5	4	3	2	1	0
DCG	WTG-	HS3-	HS2-	HS1-	HS0-	DS2-	DS1-

where: DCG = Diskette Change flag
WTG- = Write Gate on
HS3-/0- = Drive Head Select (binary)
DS2-/1- = Drive Select

The WD1018 generates the head select signals which are not transparent as in previous Western Digital Winchester disk controllers. Before the HDASR can be read correctly, the WD1018 requires a "wake-up" in order to update the head select signals.

Hard Disk Auxiliary Control Register (HDFDR) 3F6/376 (WO)

AMAC's Hard Disk Auxiliary Control Register provides programmable controller reset. It also provides enable/disable control of the fixed disk priority interrupt.

TABLE 12. AUXILIARY CONTROL REGISTER

7	6	5	4	3	2	1	0
0	0	0	0	0	RST	IDS	0

where: RST = Program controlled (master) reset
IDS = Data Transfer Interrupt Disable

NOTE: The software controlled reset bit (RST) will reset the fixed disk logic for as long as the bit is 'on'. RST must be turned on (for a minimum of 10.0 microseconds), then off, to complete the reset function.

The Interrupt Disable control bit does not clear the interrupt level of the disabled state. A pending interrupt will occur when it is re-enabled. A system Master Reset will disable the interrupt.

Fixed Disk Data Registers

The controller reserves the system's I/O address 1F0/170(H) for programmed transfers of input/output data for the fixed disk. All data transactions on the system bus between the controller and the system processor use a 16-bit word. The controller and AMAC array provide read and write data 'pipeline' registers in order for the sector data memory to function as a dual-port memory. These registers (along with the host's upper byte

equivalent) allow the WFDC module to perform concurrent host and WDC memory accesses necessary for multi-sector 1:1 interleaving. The AMAC arbitrates simultaneous host and WDC requests and gates the appropriate address counter to external memory.

Table 13 below illustrates the fixed disk data format.

TABLE 13. FIXED DISK (WORD) DATA FORMAT

ID FIELDS	WORD 000 LSB	WORD 000 MSB		WORD 255 LSB	WORD 255 MSB	CHECK FIELDS

WD37C65 Floppy Disk Controller Status/Data Registers

Table 14 summarizes FDC's status and data read/write registers and bit assignments with respect to the system's lower-byte data bus. The main status register (FDMSR) contains the controller's primary status and may be accessed at any time. It indicates drive busy status and facilitates host/controller data transfers. The data register (FDDTR) is actually a register stack that is written during the WD37C65 command phase and read during the result phase.

TABLE 14. WD37C65 STATUS AND DATA REGISTERS

REGISTER	7	6	5	4	3	2	1	0
FDMSR	RQM	DIO	EXM	CB	0	0	D1B	D0B
FDDTR	READ/ WRITE DATA							

where:
- RQM = Transfer Request To/From Host
- DIO = Transfer Direction, '1' is from WD37C65 to Host
- EXM = Not DMA Transfer Mode during command execution phase
- CB = Read or Write Command in Progress (Busy)
- D1B = Drive B in Seek Mode (Busy)
- D0B = Drive A in Seek Mode (Busy)

Data Read/Write Register Stack

Tables 15 and 16 illustrate the write stack registers and the read stack registers, respectively.

The stack is accessed at the FDDTR register address 3F5 (375).

TABLE 15. WD37C65 WRITE STACK REGISTER

WD37C65 REGISTER MNEMONIC	BIT ASSIGNMENT							
	7	6	5	4	3	2	1	0
CMD	MT	MF	SK	CMD CODE				
SEL	0	0	0	0	0	HS	0	US0
C	0	CYLINDER NUMBER						
H	0	0	0	0	0	0	0	HA
R	0	0	0	0	SECTOR NUMBER			
N	0	0	0	0	0	0	1	0
EOT	0	0	0	0	TRACK FINAL SECTOR #			
GPL	FORMAT GAP LENGTH							
DTL	1	1	1	1	1	1	1	1
SC	0	0	0	0	SECTORS PER CYLINDER			
D	(FORMAT) DATA FILLER BYTE							
STP	0	0	0	0	0	0	STP	STP
SHT	STEP RATE TIME (SRT)				HEAD UNLOAD TIME (HUT)			
HLD	HEAD LOAD TIME (HLT)							ND
NCN	0	NEW CYLINDER NUMBER						

MT = Multi-track Mode
MF = MFM Data Mode
SK = Skip Deleted Address Mark
US0 = Unit (Drive) Select B
HS = Head Select 1
HA = Head Address 1
STP = 1 = Scan Compare Contiguous Sectors
= 2 = Scan Compare Alternate Sectors
ND = Non-DMA Transfer Mode

Note: The MT, MF and SK command bits set to zero for those commands which do not define them. The FDC digital operations register (FDDOR) selects the drive. The unit select bit (US0) is shown for reference only. The HD bit selects the head. The head address bit (HA) identifies the sector.

TABLE 16. WD37C65 READ STACK REGISTER

WD37C65 REGISTER MNEMONIC	BIT POSITION 7	6	5	4	3	2	1	0
ST0	IC		SE	EC	NR	HS	0	US0
ST1	EN	0	DE	OR	0	ND	NW	MA
ST2	0	CM	DD	WC	SH	SN	BC	MD
ST3	FT(0)	WP	RY(1)	T0	WP	HS	US1	US0
C	0	CYLINDER NUMBER						
H	0	0	0	0	0	0	0	HA
R	0	0	0	0	SECTOR NUMBER			
N	0	0	0	0	0	0	BYTES	
PCN	0	PRESENT CYLINDER NUMBER						

where:

IC = Interrupt Code = 0 = Normal Command Termination
= 1 = Abnormal (Error) Command Termination
= 2 = Invalid Command
= 3 = Abnormal (Drive Ready Change) Termination

SE = Seek End
EC = Equipment Check
NR = Drive Not Ready
HS = Current Head Adr
US0 = Unit Select B
EN = End of Cylinder
DE = Data Error
OR = Overrun Error
ND = No Data Transferred
NW = No Write
MA = Missing Addr Mark
CM = Control Mark Found
DD = Data Field Error
WC = Wrong Cylinder
SH = Scan Equal Hit
SN = Scan Not Hit
BC = Bad Cylinder
MD = Missing Data Mark
FT = Drive Fault
WP = Drive Wrt Protect
RY= Drive Ready
T0 = Track 0 Flag
TS = Drive Two Sided
HD = Drive Head Address

US1/0 = Drive Select Code = 0 Drive A, = 1 = Drive B

Status Register 3 (ST3) contains the status of the selected drive while status registers 0, 1 and 2 contain information on the controller status and command execution. Registers C, H, R and N contain sector identification information following command execution. Register PCN indicates the current cylinder number (head position) following the Sense Interrupt Status command.

Floppy Auxiliary Control Registers

Operations Register (FDDOR) 3F2/372 (WO)

The Operations Register selects the floppy drive, provides drive motor control, enables or disables the floppy interrupt and DMA functions, and provides a WD37C65 software reset command.

TABLE 17. FLOPPY CONTROL REGISTER

7	6	5	4	3	2	1	0
RSV	RSV	MBE	MAE	IDE	RST	RSV	DSB

where:
RSV = Reserved
MBE = Drive B Motor Enable
MAE = Drive A Motor Enable
IDE = Interrupt and DMA Enable
RST = Floppy Section Reset
DSB = Drive B Select

To enable the floppy section operation, RST and IDE must be set.

Floppy Control Register (FDFCR) 3F7/377 (WO)

The Floppy Control Register selects one of four standard read/write data rates as shown in Table 18. The 250 Kbps rate is the default state following any reset.

TABLE 18. FLOPPY DATA RATE REGISTER

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FR1	FR0

where: FR1/FR0 = 00 = 500 Kbps (MFM)
= 01 = 300 Kbps (MFM)
= 10 = 250 Kbps (MFM)
= 11 = 125 Kbps (FM)

SPECIFICATIONS

Power Requirements

+5 VDC	+/- 5.0% < 1.200 amps

Environmental

Temperature	
Operating	10 to 50 degrees Celsius
Non-operating	-40 to 60 degrees Celsius
Humidity	
Operating	8% to 85% non-condensing
Non-operating	5% to 95% non-condensing
Shock and Vibration	
Shock	35G/20MS square wave maximum
Vibration	1G/0-600Hz, dwell not to exceed 30 seconds at (any) resonance
Altitude	
Operating	0 to 3000 meters maximum
Non-operating	0 to 5000 meters maximum

Fixed Disk Specifications

Data Transfer Format	NRZ
Data Rate	10 MBits per Second
Sector format	512 bytes/sector, 35 sectors/track hard sectored format
Drives supported	2 maximum
Heads supported	16 maximum
Cylinders supported	2048 maximum

Error Correction Specifications:

Method	Polynomial division
Degree	56

Forward polynomial	$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^{8} + 1$
Reciprocal polynomial	$X^{56} + X^{48} + X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{06} + X^{04} + 1$
Record length (r)	519 X 8 bits maximum
Correction span (b)	11 bits
Single burst detection span With b = 11	r = 519 X 8 32 bits
Double burst detection span With b = 11	r = 519 X 8 11 bits
Non-detection probability	1.39(E-17), r = 519 X 8, b = 11
Miscorrection probability	5.84(E-11), r = 519 X 8, b = 11

Floppy Disk Recording Specifications

Data Rates (Standard)	500 Kbps (MFM), 250 Kbps (MFM) 125 Kbps (FM)
Data Rates (Non-standard)	300 Kbps (MFM)
WD37C65 Clocking Rate	500 Kbps (16.0 MHz) 250 Kbps (16.0 MHz) 125 Kbps (16.0 MHz) 300 Kbps (9.6 MHz)
Write Precompensation	125 nsec. early/late standard
Sector Format	512 bytes/sector, 15 sectors/track maximum - soft sectored format
Drives supported	2 maximum
Heads supported	2 maximum
Tracks supported	160 maximum
Hard Error Rate	less than 1 per 10(E12) bits read

Soft Error Rate	less than 1 per 10(E09) bits read
Seek Error Rate	less than 1 per 10(E06) seeks

Error Detection/Correction Specifications:

ID Field CRC	$X^{16} + X^{12} + X^5 + 1$
Data Field CRC	$X^{16} + X^{12} + X^5 + 1$

Floppy Disk Data Separator Specifications:

Bit Jitter Tolerance	60% (minimum) of window
Capture Range	+/- 8% (minimum)

System Bus Timing Specifications

TABLE 19. SYSTEM BUS TIMING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
	-IOCS16 from SA09-01		79	nsec
	-IOCS16 from SA00		38	nsec
	+IOCS16 from +IOR/+IOW		71	nsec
	SD15-08 from -IOR		35	nsec
	SD07-00 from -IOR, Fixed Disk		70	nsec
	SD07-00 from -IOR, Floppy Disk		90	nsec
	SD15-08 HIZ from +IOR		43	nsec
	SD07-00 HIZ from +IOR,Fixed Disk		75	nsec
	SD07-00 HIZ from +IOR, Floppy		65	nsec
	SD15-08 setup to +IOW	00		nsec
	SD07-00 setup to +IOW,Fixed Disk	20		nsec
	SD07-00 setup to +IOW, Floppy	80		nsec
	+IOW to SD15-08 HIZ (hold time)	20		nsec
	+IOW to SD07-00 HIZ (hold time)	20		nsec
Note 1	-IOR/-IOW pulse width(16 bit I/O)	70		nsec
Note 1	-IOR/-IOW pulse width (8 bit I/O)	70		nsec
Note 2	+IOR/+IOW to -IOR/-IOW(16 bit I/O	375		nsec
	-DACK2 to -DRQ2	140		nsec
	DRQ2 period	3.2		usec
	TC pulse width	60		nsec

Notes: 1. Does not include host read data setup time
2. 10 MHZ clock input

The I/O address lines (SA09-00) and the address control signal (AEN) connect to the address decode PAL for module selection. Lines SA9 and SA2-0 connect to the AMAC for individual register addressing. The low order data byte (SD07-00) connects directly to the AMAC, and the device provides the necessary bus drive current. Figure 4 illustrates the I/O read and write signal relationship.

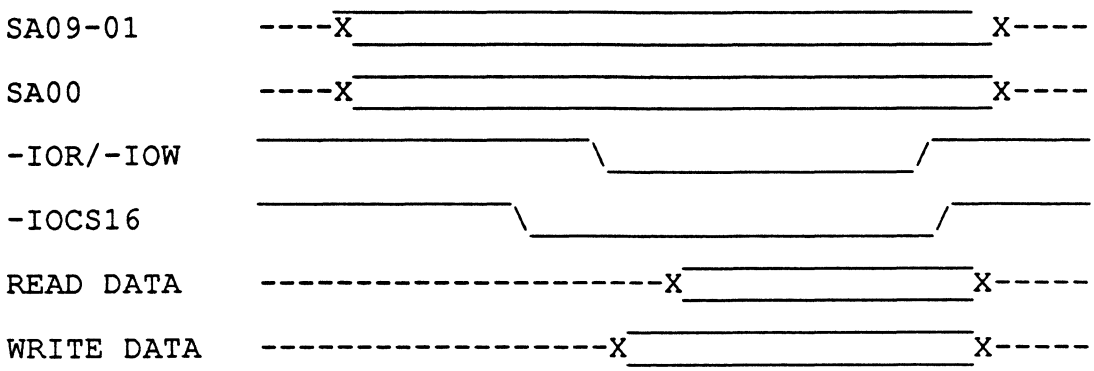


FIGURE 4. SYSTEM BUS SIGNALS
PROGRAMMED I/O CONTROL

AMAC's data pipeline registers allow the WFDC module to perform concurrent host and WDC memory accesses necessary for multi-sector 1:1 interleaving. A clocked sequencer controls the timing of the two AMAC generated strobes to resolve priority (in favor of the host request) and generate the external memory (and byte transfer gate) control signals.

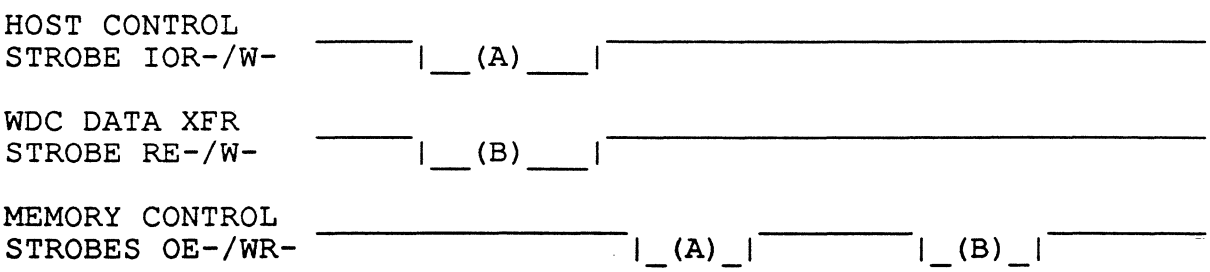


FIGURE 5. AMAC TIMING

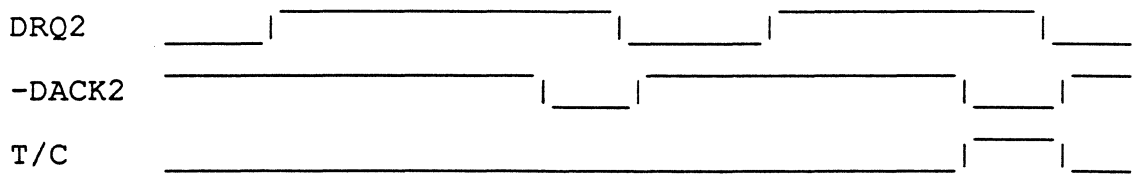


FIGURE 6. FLOPPY DISK CONTROLLER

COMMAND SUMMARY

Software Overview

All control and data transfers between the system processor and the WFDC fixed disk control section use system programmed I/O. Direct memory accesses (DMA) are used in the floppy disk section for data transfers only. All floppy control and status transactions use system programmed I/O. The module address range is fixed (at either of two ranges) as are the controller priority interrupt levels and the DMA channel assignment.

WD50C12 Winchester Disk Controller

Command Descriptions

The Task File Command Register (HDCMD) accepts the commands and command attributes as shown in Table 20. It does not accept commands when the WFDC is 'busy'. Commands terminate without execution if the Drive Ready signal is false, if a write fault condition exists at the drive, or if the command is undefined.

TABLE 20. WD50C12 COMMAND SUMMARY

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	X	X	X	X
SEEK	0	1	1	1	X	X	X	X
RD SECTOR	0	0	1	0	0	0	LNG	RTY
WRT SECTOR	0	0	1	1	0	0	LNG	RTY
FMAT TRACK	0	1	0	1	0	0	0	0
RD VERIFY	0	1	0	0	0	0	0	RTY
DIAGNOSE	1	0	0	1	0	0	0	0
SET PARAM	1	0	0	1	0	0	0	1
INIT ESDI	1	1	1	0	0	0	0	0
WT STACK	1	1	1	0	1	0	0	0
RD STACK	1	1	1	0	0	1	0	0
READ PARAM	1	1	1	0	1	1	0	0
CACHE CNTL	1	1	1	0	1	1	1	1

Where: X = Drive stepping rate. (Unused in ESDI drive)
LNG = 0 = Normal mode, WD50C12 performs normal ECC functions.
LNG = 1 = Long mode, the WD50C12 is unable to generate or check the ECC bytes. The WD50C12 appends the additional bytes supplied by the drive (read) or host processor (write) to the normal data field.

RTY = 0 = Error retries and ECC correction are enabled
RTY = 1 = Retries and ECC correction are disabled.

Standard Commands

The WD50C12 executes the following standard commands: Restore, Seek, Read Sector, Write Sector, Scan ID, Write Format, and Compute (ECC) Correction.

Of these, the Scan ID and Compute (ECC) Correction commands are not directly available to the system processor (although they may be executed by the WD1018 transparently to the host processor).

Restore - The selected ESDI drive receives a Seek-to-Cylinder 0 command via the serial command interface (WD1018 port 1.5). The drive heads seek to cylinder 0 and any track offsets are clear. The command aborts when the ERR bit sets in the status register. The Aborted Command (ACD) bit sets in the error register if the WD1018 receives an Attention interrupt from the drive indicating a transfer protocol or transfer parity error.

Seek - The Seek command positions the drive heads over the cylinder specified in the Task File registers (HDCLH/L) and clears any track offsets. The command aborts under the conditions noted for the Restore command above. Bit SKC of the HDSTT register sets true upon the completion of a Seek command. The fixed disk priority interrupt (IRQ14) issues after a successful ESDI Seek command transfer. The host can check for completion of the seek operation by checking bit SKC of HDSTT register.

Read Sector - A number of sectors (1-256) are read from the selected disk. If the drive is not positioned at the specified cylinder an implied 'seek' will occur. Drive furnished ECC check bits will be used if the Read Long mode is specified. Single burst data errors (up to 11 bits) will be corrected if retries are enabled and the long mode is not selected.

Uncorrectable errors do not inhibit the (error sector) data transfer, however, multi-sector transfers will terminate. The WFDC interrupt occurs as each sector is ready for system input. The WFDC also caches the remaining sectors until the buffer RAMs are full upon completion of a successful Read Command. When the next Read Command occurs, and if the desired sectors are the same

as the cached sectors, the data transfer occurs immediately. Caching therefore improves the data throughput by reducing the disk access time. IRQ14, BSY and DRQ bits of HDSTT register operate in the same fashion as in non-cache operations.

Write Sector - A number of sectors (1-256) are written to the selected disk with an implied seek occurring, if required. Multiple sector write (and read) operations may cross track and cylinder boundaries. The Write Long mode appends the ECC bytes to the data supplied by the system processor. The data request bit (On) along with the command cause the system processor to output the contents of the first data buffer. An interrupt occurs as the data for each subsequent sector is required.

Format Track - The Task File specifies the track to be formatted with identification, data, and check fields in accordance with the interleave table transferred to the sector buffer. The interleave table is composed of two bytes per sector, with the first byte set to "00" for a good sector or "80h" for a bad sector. The second byte designates the logical sector number. The Task File (HDSCT and HDSDH) specifies sectors per track and sector size. Command completion initializes the data field to 'zeros' and appends four ECC bytes after the data field. The Completion Interrupt occurs as each track is formatted. The WD1007A-WA2 controller forces 512 bytes/sector, 35 sectors/track, and the hard sectored drive format.

Non-standard Commands

The WD1018 intercepts fixed disk commands to the WFDC with the aid of the AMAC logic in order to define commands not specified in the WD50C12 command list.

Set (Drive) Parameters - This command communicates drive parameters to the controller. It selects the head, cylinder, and sector for each drive. The WD1018 uses the drive parameters in the execution of multi-sector commands and in evaluating legal controller commands.

Read Verify - This command verifies that a previous write command is correct by checking ECC bytes. The host processor does not input read data. The command may be used with multi-sector operations. An error condition will abort a multi-sector verify operation. The retry command may be used with this command.

Diagnose - The diagnostic command causes the WD1018 to execute an on-board diagnostic program and to report the test results to the WD50C12 Error Register. See Appendix for WFDC self tests.

Write Stack - This diagnostic command allows the host to write data to the sector buffer without executing an actual disk write command. This command does not generate an interrupt upon completion.

Read Stack - This diagnostic command allows the host to read the sector buffer without executing a disk read operation. This command does not generate an interrupt upon completion.

Initiate ESDI - This command allows the system processor to send instructions directly to the selected drive by loading the AMAC's cylinder register and executing the Initiate command. The host must load AMAC's cylinder registers (high and low data bytes) with the command it wants the drive to execute prior to issuing the Initiate ESDI command. The controller serializes the data, adds the required parity bit and transmits the instruction to the drive. The drive completes the instruction and transmits completion status to the controller. The drive's completion status data is then stored back into AMAC's cylinder registers for host access.

The following examples show how the Initiate ESDI command is used:

Using ARM(Western Digital Test Software)
When * appears, type 'MAKE' and Enter
Monitor will display:

```
Enter Task File Parameters.  All Entries are in hex
Enter Command =
Enter Cylinder # =
Enter Head # =
Enter Sector =
```

Enter 'E0' for the command.
Enter '20' (Request Standard Status) for the cylinder number.

The high byte (bits 15 - 8) of the ESDI command will go to Cylinder High Register, and the low byte (bits 7 - 0), if applicable, will go to Cylinder Low Register. Refer to ANSI ESDI Specification, Document No. X3T9.3/8X, for all ESDI commands.

The host can now access the drive's status by reading the cylinder register's addresses (AF4 - AF5). The high order status byte is stored in the Cylinder High Register: the low order status byte is stored in Cylinder Low Register.

Using DEBUG
Enter:

```
O1F4 00
O1F5 20    ;Output Read Status Command
O1F7 E0    ;Initiate ESDI Command

I1F4
I1F5       ;Read Drive Status
```

Read Parameters - This command causes the MC8753 to store 49 words of drive and controller parameters into the sector buffer for host access. The data is stored in the following format:

OFFSET	MODIFIER Bits 8 - 11	ESDI CONFIGURATION INFORMATION
0	0	General Configuration
1	1	# Fixed Cylinders
2	2	# removable cylinders
3	3	# heads
4	4	# unformatted bytes/track
5	5	# unformatted bytes/sector
6	6	# sectors/track
7	7	# min. bytes in ISG
8	8	# min. bytes in PLO
9	9	# words of vendor status

OFFSET	CONTROLLER PARAMETERS
10 - 19	Serial # (20 ASCII characters - 0)= not specified)
20	Controller type 0= not specified 1= single port, single sector buffer 2= dual port, multi-sector buffer 3= dual port, multi-sector buffer, cache
21	Controller buffer size in 512 byte increments (32 sectors)
22	# of ECC butes transferred on long operations (4 ECC bytes)
23 - 26	Controller firmware revision (8 ASCII characters)
27 - 46	Controller model # (40 ASCII characters)
47	# sectors transferred per INT on read commands (1 sector/interrupt)
48	Double word capability 0= not capable 1= capable

Cache Control - This command (EF) allows the user to enable or disable caching. By writing AA (enable) or 55 (disable) into the Write Precomp Register (1F1), then issuing the Cache Control command, caching will be turned on or off accordingly. The command will abort if any another code is written into 1F1, and caching stays unchanged. Caching is enabled in default.

Multi-sector Commands

The WFDC provides multiple sector read, write and verify commands of up to 256 sectors without restriction on track or cylinder boundaries. Unrecoverable control errors (Drive Not Ready, Write Fault, etc.) or uncorrectable read data errors will terminate a

multi-sector command, and the controller expects a new command to continue operation. Corrected read data errors do not terminate the command, and the controller expects a normal data transfer restart and continuation. WFDC can execute 'long mode' ECC diagnostic commands, however, the throughput is reduced.

Diagnostic Commands

The controller on-board diagnostic verifies the WD1018 local storage, the sector data buffer storage and the data paths for WD1018, WD50C12 and AMAC. The encoded results are available to the system processor via the controller error register.

WD37C65 Floppy Disk Controller

Standard Commands

The WD37C65 executes the following standard commands: Read Data, Read Deleted Data, Write Data, Write Deleted Data, Read Track, Read ID, Format Track, Scan (Data) Equal, Scan Low or Equal, Scan High or Equal, Recalibrate, Sense Interrupt Status, Specify, Sense Drive Status and Seek.

The WD37C65 has a specific command, execution and result phase protocol for each command. The floppy disk section commands are listed below along with their respective command codes, command phase (write) register stack and result phase (read) register stack.

Read Data - The host outputs the nine command phase bytes and the FDC selects the drive, loads the drive heads (if previously unloaded) and begins reading ID address marks and ID data fields to locate the selected sector. When the sector is found the FDC transfers data (via DMA) to host memory. Multi-sector and multi-track operations are allowed. Completion of the command updates the result phase registers, interrupts the system processor (if interrupt enabled) and unloads the heads following the head unload interval.

The **Read Deleted Data** command and **Read a Track** command have the same command and result phase register requirements except for the command opcode. The Read Deleted Data command transfers sectors which have the deleted data address mark. The Read Track command transfers all sectors from the index mark through the 'end of track' sector.

A **Read Identification Field** command transfers the first correct ID field data to the sector identification result registers and interrupts the host. Sector data does not transfer to system memory. The result register stack is the same as for a normal read command but the command phase requires only the command and

select register information.

Write Data - The host outputs the nine command phase bytes and the FDC selects the drive, loads the heads and searches the sector ID fields. When the C, H, R and N sector fields match the command register data the FDC transfers byte data via DMA to the drive. Command completion updates the result registers and interrupts the host processor.

The **Write Deleted Data** command is the same as Write Data except that a deleted data address mark appears at the beginning of the data field in place of a normal data address mark.

Format a Track - The FDC formats the selected track from index through the last track sector with address marks, ID fields, data fields and field gaps for either the single or double density format. The host furnishes the ID field data (four bytes) for each sector. The data field is filled with the data defined in the Command Stack Register D.

Scan Equal - The FDC compares the drive information and the host data for a selected sector on a byte basis. If the scan condition is satisfied, the SH (scan equal hit) bit sets in Status Register 2.

The **Scan Low or Equal** and **Scan High or Equal** commands are similar except for the logical compare condition. If the scan condition is not satisfied, the SN (scan not hit) bit sets in Result Register ST2.

Recalibrate - The heads of the selected drive retract to track position 0. The track 0 position flag is available as a separate signal from the selected drive and in the ST3 status byte.

Seek - The selected drive steps to the new cylinder position.

Specify - The Specify command sets the drive head's load and unload rates, the drive's step rate, and the DMA data transfer mode.

Sense Interrupt Status - Controller status register 0 and the current cylinder are available in the result registers following this command. This command clears the floppy section's interrupt level.

Sense Drive Status - This command returns selected drive status (ST3) during the result phase.

Non-standard Commands

The WD37C65 has two registers in addition to the industry standard UPD765 registers. They are: the Operations Register which

controls the floppy drive select, drive motor enables, controller reset, DMA request, and interrupt enable; and the Control Register which selects the floppy data rate.

WD1018 COMMANDS

The WD1018 communicates with the AMAC support logic via a set of read/write commands at preset addresses. The commands are available to the controller only and not to the system processor.

TABLE 20. CENTRAL PROCESSOR SUPPORT COMMANDS

ADDRESS	R/W	COMMAND
20	R/W	Host memory address block counter
21	R/W	WDC memory address block counter
22	W	Clear host memory address counter
22	R	Set sleep mode (clear busy)
23	W	Clear WDC memory address counter
23	R	Set 7 byte ECC mode
24	W	Set data request latch
24	R	Set interrupt
25	W	Set read mode
25	R	Set memory prefetch
26	W	Set multiple sector mode
26	R	Clear multiple sector mode
27	W	Set sector block counter
27	R	Set idle mode

Addresses 00-07(H) and 10-17(H) are reserved for CP communication with the AMAC and WD50C12 Task File registers respectively. Address range 30-3F(H) is reserved for special IDE and command control.

NOTE: The two high order address bits are not used in the AMAC address decode of the WD1018 support commands.

APPENDIX

WFDC SELF TESTS

The encoded result descriptors for each controller self test are shown in Table A-1. The WFDC error register HDERR (hex address 1F1/171) reports the test result. Issuing a Diagnose command or a reset will execute the tests.

The tests verify the WD1018 firmware checksum, the WD1018 RAM memory, the sector buffer RAM memory and the WD50C12 and AMAC data paths. System bus or host interactive tests are not included.

TABLE A-1. SELF TEST ERROR CODES

RESULT	DESCRIPTION
01	No Errors
02	Controller Error
03	Sector Buffer Error
04	AMAC Device Error
05	Control Processor Error
06-FF	Undefined

where: 02 = WD1018/WD50C12 register access error

03 = Sector buffer data error

04 = WD1018/AMAC register access error
= AMAC Byte 0 Pipeline register error

05 = WD1018 ROM checksum error
= WD1018 RAM data error

1007A-WA2 OPTIONAL BIOS

GENERAL

The WD1007A controllers have an optional BIOS ROM that enables the user to integrate a controller having an ESDI drive with an IBM PC/AT or compatible. The BIOS provides drive parameter tables, low-level formatting routines, and surface analysis routines. The parameter tables support the drive and controller in systems that do not provide ESDI parameters. Low-level formatting and verification routines prepare the drive for use by the operating system. Part of the optional BIOS is a "shadow RAM". This is a static memory device that resides in the upper 256 bytes of the BIOS address space. This memory stores the parameter information generated by the BIOS in an area outside system memory. The BIOS resides in the external I/O BIOS address

space. There are four address ranges available, which are selected by configuring the jumpers at W1-W2. (Refer to the Jumper Configuration Tables, page 13.)

PARAMETER TABLES

Most system BIOS ROMS support only the older MFM/ST-506 drives that used 17 sectors per track. The ESDI disk drive typically has 34 sectors per track when operating in the hard sector mode. The BIOS generates the needed information by using the ability of the ESDI drive to present the actual drive characteristics to the controller. The BIOS reads the ESDI information and generates the appropriate parameter tables. Parameter tables are also constructed for the translation features of the controller.

FORMAT AND SURFACE ANALYSIS

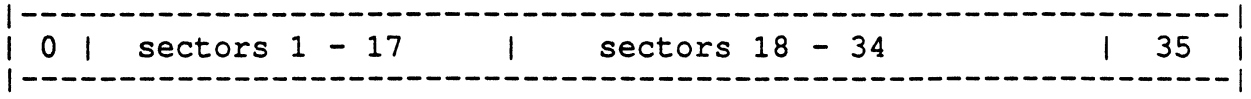
Formatting routines perform the low-level initialization of the disk surface. The drive is formatted with the physical characteristics read from the drive. Formatting is done at a 1:1 interleave ratio and is not changeable. The format routine formats with a sector skew and also formats a spare sector on each track. This sector is used by the surface analysis routines to provide the ability to reallocate a bad sector on a track. It also stores the parameter information generated by the BIOS. This information appears on the spare sector on cylinder 0, head 0. The sector skew which is fixed at two, allows the controller to maintain a 1:1 interleave across all head boundaries. Sector skewing is a method of formatting in which the sector numbers are rotated in the interleave table for each track.

TRANSLATION

MS-DOS assumes that a hard disk has 17 sectors per track (SPT). This reflects the ST-506 type drives. However, the ESDI drives support 34 to 36 sectors per track with 512 bytes per track. In order to utilize the maximum storage capacity of the ESDI drives, the WD1007A-WA2 controller provides two methods of translation:

1. Translation of 17 sectors per track mode - For those operating systems that recognize only 17 sectors per track, it is necessary to translate physical sectors per track into logical sectors per track. This is accomplished by setting the number of logical heads requested in the SDH register to twice the number of physical heads (for a maximum of 16 heads). This mode is invoked when the host issues a Set Parameters command with 17 in the Sector Count Register.

The WD1007A-WA2 utilizes the physical track in the following manner:



Sector 0 and 35 are optional alternate sectors which are not accessed by DOS. Sectors 1 through 17 represent a logical track, i.e. logical head 0, and sectors 18 - 34 represent another logical track, i.e logical head 1.

PHYSICAL PARAMETERS	LOGICAL PARAMETERS
1024 Cylinders	1024 Cylinders
8 Heads	16 Heads
34 Sectors/Track	17 Sectors/Track

Low-level formating of ESDI drives must be accomplished with physical parameters of 34 to 35 sectors per track. If a format for 17 sectors per track is attempted, only the data fields will be initialized.

2. General translation mode - This mode is invoked when the physical number of cylinders exceeds 1024. By increasing the logical sectors per track to 63 and increasing the logical heads to 16, the number of logical cylinders will decrease accordingly.

For this type of drive, the following algorithm for disk address translation is used:

ABS_SEC = (((LOG_CYL * LOG_HDS) + LOG_HD) * LOG_SPT) + LOG_SEC -1

ABS_HEAD = ABS_SEC DIV PHY_SPT

PHY_SEC = ABS_SEC MOD PHY_SPT + 1

PHY_HEAD = ABS_HEAD MOD PHY_HEADS

PHY_CYL = ABS_SEC DIV PHY_HEADS

Where :

ABS_SEC is the absolute logical sector number with range 1 through 1,032,192.
LOG_HDS is the maximum number of logical heads 1 - 16
LOG_SPT is the logical sector/track 1 - 63
LOG_SEC is the logical sector address 1 - 63
LOG_HD is the logical head address 0 - 15
LOG_CYL is the logical cylinder address 0 - 1023
PHY_HEADS is the maximum number of physical heads
PHY_SPT is the disk sector/track = 34
PHY_SEC is the disk physical sector 1 - 34

PHY_HEAD is the disk physical head 0 - 15

ABS_HEAD is the calculated absolute head address
0 - 19114
PHY_CYL is the disk physical cylinder address

This algorithm is based on the fact that a physical cylinder contains 510 (34 * 15) physical user sectors. Using half the number of physical cylinders as the logical cylinder gives a sector count of 1020 per logical cylinder. Dividing by 16 logical heads yields 63.75 sectors per track.

PHYSICAL TO LOGICAL FORMULAS

```
ABS_SEC = (((PHY-CYL * PHY_HEADS)+PHY_HEAD)*PHY_SPT)+PHY_SEC
LOG_SEC = ABS_SEC MOD LOG_SPT
ABS_HEAD = ABS_SEC DIV LOG_SPT
LOG_HEAD = ABS_HEAD MOD LOG_HEADS
LOG_CYL = ABS_HEAD DIV LOG_HEADS
```

Translation Algorithm Example

The following translation example uses an HP 9753XEA ESDI.

HP 9753XEA physical parameters:

```
PHY_CYLS = 1600 Cylinders
PHY_HEADS = 12 Heads
PHY_SPT = 32 sectors per track (actually 64,256 byte sectors)
```

By transposing these values into the following formula, this drive can offer 614,400 sectors:

```
ABS_SECS = PHY_CYLS * PHY_HEADS * PHY_SPT
ABS_SECS = 1600 * 12 * 32 = 614,400
```

The following formula determines the logical parameters:

```
ABS_SECS = LOG_CYLS * LOG_HEADS * LOG_SPT
```

If the logical sectors per track (LOG_SPT) is 63 and the logical number of heads (LOG_HEADS) is 16, then to determine the logical number of cylinders (LOG_CYLS):

```
LOG_CYLS = ABS_SECS / (LOG_HEADS * LOG_SPT)
LOG_CYLS = 614,400 / (16 * 63) = 609
```

The resulting logical parameter table for the HP 9753XEA would be:

```
LOG_CYCLS = 609 cylinders
LOG_HEADS =  16 heads
```

Log_SPT = 63 sectors per track (512 byte sector)

This yields a 314.3 Mbyte drive. The drive would actually have a capacity of 314.5 Mbytes if it could be accessed physically. Only read and write data operations use these logical parameters. Low level initialization and alternate sector utilization must be accomplished physically. When using diagnostics, such as IBM ADVANCED DIAGNOSTICS, and a format track command issues with a sector count not equal to the physical sectors per track, determine the starting physical sector and write a pattern of zeros in the data field of all sectors on that logical track.

preliminary

Application Note

WD1007A–WAH/2

February 17, 1988

Dated Material/Subject to Change

WESTERN DIGITAL

TABLE OF CONTENTS

1.0 INTRODUCTION

1.1 Document Scope

This document provides the user with the necessary information to integrate the WD1007A-WAH/WA2 into the IBM PC/AT or compatible environment. This document, accompanied by a WD1007A support diskette and a data sheet forms a complete 1007A support package.

1.2 Product Description

The WD1007A-WAH and the WD1007A-WA2 are single board Winchester Disk Controllers designed to interface two ESDI compatible disk drives to the IBM PC/AT or compatible host computer. The WD1007A-WA2 supports two floppy disk drives in the AT environment. The WD1007A-WAH is a hard disk only version of the controller. The two boards use the same artwork, with the WD1007A-WAH being depopulated with the floppy controller device and support circuitry. The controller is based on the WD50C12 disk controller device and the WD12C00 host interface and buffer manager device. Overall controller operation is handled by an Intel 8053 microcontroller (WD1018). Floppy support is handled by the WD37C65 integrated floppy controller device.

1.3 Features

- Controls two ESDI hard disk drives;
- Controls two floppy disk drives (WD1007A-WA2 only);
- Supports drives with up to 2048 cylinders and 16 heads;
- Device interface transfer rates to 10MHz;
- Supports 1:1 interleave;
- 16KB (8K word) ring buffer;
- Default cacheing operation;
- Expanded command support;
- Totally AT compatible.

2.0 DESCRIPTION

2.1 Overview

This section will present some information on two areas of concern when integrating the WD1007A controllers into an IBM PC/AT environment. First, some basic information on the ESDI interface and options at the device level that affect operation of the controller. Second, information about the system parameter information required to bring the hard disk on-line.

2.1.1 ESDI Interface

ESDI is an interface standard that allows the support of storage devices of different types on the same physical interface. These devices are hard disk, tape, and optical storage. The interface is intelligent, having command and status structures for each device, and a communications protocol for controller to device information transfer. Configuration data is available from the device containing information about the physical makeup of the drive and its current configuration. The attached controller has the option to read this data for use in configuring itself to the drive. See appendix for more ESDI information.

2.1.2 Sector Modes

The ESDI specification allows for two sectoring modes to be supported; hard or soft. This section will cover only the hard sector mode, as it is the only mode supported by the WD1007A controllers. In the hard sector mode, the drive will generate a sector pulse for every sector on the drive. The number of sectors per track can be specified in one of two ways:

A. Set Unformatted Bytes/Sector Mode

This mode allows the controller to send the ESDI command SET UNFORMATTED BYTES PER SECTOR to the ESDI device. Normal operation of the WD1007-WAH/WA2 (when the W8 is not jumpered). Not allowed using the WD1005-WAH board. Note that the WD1007-WAH assumes the drive will override any jumper settings on the drive (that might dictate other values) when this command is issued. If this assumption is not valid (as in the NEC 8652 ESDI drive), the drive jumper settings will have to be set to make it accept this command.

The byte per sector value is the total number of unformatted bytes per sector, including ID fields, PLO fields, and DATA fields. The device uses this value to divide a track into a given number of sectors and generate a pulse for each. This is the mode the WD1007A controllers default to when no jumper is installed on W8. When in this mode, the WD1007A will configure the drive for 35 sectors per track unless the physical drive parameter differs from 35 SPT. See section on the 1007A BIOS for details.

B. Read Configuration Switches Mode

Normal operation of the WD1005-WAH can be invoked on the WD1007A by putting a jumper on W8. The controller reads a jumper array from the drive representing the equivalent of the bytes/sector to be used. In this mode, the WD1007A controller is completely equivalent to the WD1005-WAH.

2.1.3 Parameter Information

When integrating a hard disk into the AT environment, it is essential to be able to select the proper drive type (conforming to the physical drive parameters) from the system BIOS parameter tables. The drive type information contains the number of cylinders, heads, and sectors/track. This parameter information is used to properly communicate with the drive. Matching the physical drive parameters is essential because it maximizes the use of the storage space on the drive. If, for example, a drive is specified by the drive manufacturer to have a capacity of 300MB at 35 sectors/track, but the system BIOS is only capable of recognizing 17 sectors/track, only half of the drive's storage capacity can be utilized. There are three possible ways of assuring compatibility:

1) Use the drive in a system that has a BIOS parameter table matching the drive's;

2) Use the optional WD1007A BIOS (see section 2.2 on the WD1007A-BIOS);

3) Use third party software of vendors that have developed products allowing customization of parameter information.

Of these options, the WD1007A BIOS option is the easiest to implement in terms of flexibility, availability and adaptibility to different drive types.

2.1.4 Translation

When integrating an ESDI drive into the AT environment, certain physical parameters may exceed limitations of the system BIOS or operating system. The sectors per track parameter and the number of total cylinders are the most likely to exceed these limitations.

Some older versions of MSDOS and DOS versions distributed by OEMs, as well as Zenix and Novell software, assumed that the drive would be divided into 17 sectors on each track. This was also reflected in the parameter tables available in the system BIOS.

MS-DOS assumes that a hard disk has 17 sectors per track (SPT). This reflects the ST-506 type drives. However, the ESDI drives support 34 to 36 sectors per track with 512 bytes per track. In order to utilize the maximum storage capacity of the ESDI drives, the WD1007A-WA2 controller provides two methods of translation:

1. Translation of 17 sectors per track mode - For those operating systems that recognize only 17 sectors per track, it is necessary to translate physical sectors per track into logical sectors per track. This is accomplished by setting the number of logical heads requested in the SDH register to twice the number of physical heads (for a

maximum of 16 heads). This mode is invoked when the host issues a Set Parameters command with 17 in the Sector Count Register. The WD1007A-WA2 utilized the physical track in the following manner:

```
-------------------------------------------------------------------
  0  /   sectors 1 - 17      /   sectors 18 - 34              /   35
-------------------------------------------------------------------
```

Sector 0 and 35 are optional alternate sectors which are not accessed by DOS. Sectors 1 through 17 represent a logical track, i.e. logical head 0, and sectors 18 - 34 represent another logical track, i.e. logical head 1.

PHYSICAL PARAMETERS	LOGICAL PARAMETERS
1024 Cylinders	1024 Cylinders
8 Heads	16 Heads
34 Sectors/Track	17 Sectors/Track

Low-level formatting of ESDI drives must be accomplished with physical parameters of 34 to 35 sectors per track. If a format for 17 sectors per track is attempted, only the data fields will be initialized.

2. General translation mode - This mode is invoked when the physical number of cylinders exceeds 1024. By increasing the logical sectors per track to 63 and increasing the logical heads to 16, the number of logical cylinders will decrease accordingly.

For this type of drive, the following algorithm for disk address translation is used:

```
ABS_SEC = ((LOG_CYL * LOG_HDS) + LOG_HD) * LOG_SPT) + LOG_SEC -1

ABS_HEAD = ABS_SEC DIV PHY_SPT

PHY_SEC = ABS_SEC MOD PHY_SPT + 1

PHY_HEAD = ABS_HEAD MOD PHY_HEADS

PHY_CYL = ABS_SEC DIV PHY_HEADS
```

Where :

ABS_SEC is the absolute logical sector number with range 1 through 1,032,192;
LOG_HDS is the maximum number of logical heads 1 - 16;
LOG_SPT is the logical sector/track 1 - 63;
LOG_SEC is the logical sector address 1 - 63;
LOG_HD is the logical head address 0 - 15;
LOG_CYL is the logical cylinder address 0 - 1023;
PHY_HEADS is the maximum number of physical heads;

PHY_SPT is the disk sector/track = 34
PHY_SEC is the disk physical sector 1 - 34;
PHY_HEAD is the disk physical head 0 - 15;
ABS_HEAD is the calculated absolute head address 0 - 19114;
PHY_CYL is the disk physical cylinder address.

This algorithm is based on the fact that a physical cylinder contrains 510 (34 * 15) physical user sectors. Using half the number of physical cylinders as the logical cylinder gives a sector count of 1020 per logical cylinder. Dividing by 16 logical heads yields 63.75 sectors per track.

Physical to Logical Formulas

ABS_SEC = (((PHY-CYL * PHY HEADS) + PHY_HEAD)*PHY_SPT)+PHY_SEC
LOG_SEC = ABS_SEC MOD LOG_SPT
ABS_HEAD = ABS_SEC DIV LOG_SPT
LOG_HEAD = ABS_HEAD MOD LOG_HEADS
LOG_CYL = ABS_HEAD DIV LOG_HEADS

Translation Algorithm Example

The following translation example uses an HP 9753XEA ESDI:

HP 9753XEA physical parameters:

PHY_CYLS = 1600 Cylinders
PHY_HEADS = 12 heads
PHY_SPT = 32 sectors per track (actually 64,256 byte sectors)

By transposing these values into the following formula, this drive can offer 614,400 sectors:

ABS_SECS = PHY_HEADS * PHY_SPT
ABS_SECS = 1600 * 12 * 32 = 614,400

The following formula determines the logical parameters:

ABS_SECS = LOG_CYLS * LOG_HEADS * LOG_SPT

If the logical sectors per track (LOG_SPT) is 63 and the logical number of heads (LOG_HEADS) is 16, then to determine the logical number of cylinders (LOG_CYLS):

LOG_CYLS = ABS_SECS / (LOG_HEADS * LOG_SPT)
LOG_CYLS = 614,400 / (16 * 63) = 609

The resulting logical parameter table for the HP 9753XEA would be:

LOG_CYCLS = 609 cylinders
LOG_HEADS = 16 heads
LOG_SPT = 63 sectors per track (512 byte sector)

This yields a 314.3 Mbyte drive. The drive would actually have a capacity of 314.5 Mbytes if it could be accessed physically. Only read and write data operations use these logical parameters. Low level initialization and alternate sector utilization must be accomplished physically. When using diagnostics, such as IBM ADVANCED DIAGNOSTICS, and a format track command is issued with a sector count not equal to the physical sectors per track, determine the starting physical sector and write a pattern of zeros in the data field of all sectors on that logical track.

Translation can be disabled by using the translation override jumper, W14. This requires that the parameters passed from the system must be the same as the parameters of the drive.

2.1.5 Floppy Support

Floppy disk drive support is provided by the WD37C65 integrated floppy disk controller chip. The device is fully compatible with the NEC 765 floppy controller chip, thus maintaining full AT BIOS compatibility. The controller will support combinations of 5.25" and 3.5" drives within the following key guidelines:

a. Only two floppies can be installed at any one time.

b. If using 3.5" drives it must be verified that the system BIOS supports the given version (either 720 Kb or 1.44 Mb) of the drive. Appropriate steps, including 'Setup' and the use of 'Driver.Sys' type device drivers, might have to be taken to assure that the system BIOS recognizes the drive.

c. When using 1.44 Mb drives one MUST make sure that the drive is of the type referred to hereon as the 'ANSI' type. This means that drive must be AT compatible and have a 'no care' condition on pin 2 at the floppy interface.

2.1.6 Track Cacheing

The WD1007A incorporates a track cacheing function to improve disk subsystem performance. This feature can be more clearly defined as a look-ahead read. When the host issues a read command to the controller, single or multi-sector, the controller will perform the read of the sector or sectors. While the host is offloading this data, the controller firmware will initiate the look-ahead read function. The controller will continue to read sectors from the track where the read command was started. The controller will

continue to read sectors until the buffer is full or the end of the track is reached. This cacheing routine is done in anticipation of a read of another sector or sectors on that track by the operating system. The cacheing read will be halted if a command is issued to the controller that is not a read command of the track that initiated the cacheing read. The cacheing feature can be disabled for those applications that may not gain performance from this feature. The WD1007A control firmware supports a non-standard command called "Cache Control". This command is used to enable or disable the cache feature. By writing a value to the Write Precomp Register and issuing the command to the Command Register, cacheing can be controlled by the host. To enable cacheing, an AAH is written to the precomp register, and a 55H will disable the feature. Writing any other value to this register aborts the command and the state of cacheing remains the same. The WD1007A default is cacheing enabled.

2.2 BIOS Notes

There are two different BIOS' that play a role in the use of the WD1007A with ESDI drive: the System BIOS and the 1007A BIOS.

A. The System BIOS.

1. The system BIOS refers to the BIOS that is controlling the computer (e.g. Phoenix, IBM-AT, Faraday). If the appropriate drive parameter tables are present, the system BIOS can be used, along with the operating system (MSDOS, SCO Xenix) to partition and high level format a given drive.

The easiest way to determine if a system BIOS has the physical drive parameters required for the ESDI drive is to use the appropriate set-up diskette and see if the appropriate heads, number of cylinders and number of sectors/track are listed. If they are not listed, the BIOS probably does not have the required parameter tables and one needs to use other means (such as WDFMT or the WD1007A BIOS) to low level format.

Another way of examining the system parameter tables to determine the drive type number for the given ESDI drive, is through the DOS Debug Utility.

Although some systems locate drive parameters in other locations, the standard location in the AT BIOS is F000:E401. The proper command at the DEBUG prompt (-) is as follows:

```
df000:e401 <CR>
```

This corresponds to drive type 1 and will display 8 lines of data from the BIOS ROM. By entering another "d" at the DEBUG prompt, another 8 lines of data will be displayed, corresponding to drive

type 2, etc. This procedure is continued until all drive parameter information is displayed. Each parameter table has 16 bytes of data. Data from the BIOS ROM is displayed in hex, least signifcant byte first. This data breaks down as follows:

Bytes 1&2	Number of cylinders
Byte 3	Number of heads
Bytes 4&5	Not Used
Bytes 6&7	Write Pre-Compensation cylinder
Byte 8	Not Used
Byte 9	Control Byte (= 08H for > 8 heads)
Byte 10-12	Not Used
Bytes 13&14	Landing Zone3
Byte 15	Sectors Per Track
Byte 16	Not Used

Another feature of the DOS DEBUG utility is in the user's ability to confirm the parameters for the current drive selected. This is done through the INT 41 (located at d0:104) and the INT 46 (located at d0:118) handlers. INT 41 corresponds to the address of the current selected parameters for drive) and INT 46 corresponds to the address of the current selected parameters for drive 1. For example, if one desires to see the current selected parameters for drive 0, the proper command at the DEBUG prompt (-) is:

```
d0:104
```

The first four bytes displayed correspond to the offset (2 bytes) and segment 6 (2 bytes) of the location where the selected parameters are, e.g., if after the above d0:104 the result is:

```
30   IF     00   C8    AB   73  . . . <=> Location DC800:1F30
[     ]     [     ]
Offset     Segment
```

The current selected parameters are located at address C800:1F30. By typing this at the DEBUG prompt, 16 bytes will be displayed (as explained above) describing the selected drive parameters.

B. 1007A BIOS

1.0 General Notes

The WD1007A controllers have an optional BIOS rom that provides functions to help the user integrate the controller with an ESDI drive into an IBM PC/AT or compatible. The BIOS provides drive parameter tables, low-level formatting routines, and surface analysis routines. The parameter information is needed to support the drive and controller in systems that do not support the parameters needed for this combination in their system BIOS. Low-level formatting and verification routines are used to prepare the drive for use by the operating system. Part of the optional BIOS is a "Shadow Ram". This

is a static memory device that resides in the upper 256 bytes of the BIOS address space. This memory is used to store the parameter information generated by the BIOS in an area outside system memory. The BIOS resides in the external I/O BIOS address space. There are four address ranges available, selected by configuring the jumpers at W1-W2. See Figures 1-5 for a complete flowchart description of the 1007A BIOS and Figure 6 for the addressing scheme implemented for the shadow RAM.

2. Parameter Tables

When integrating a hard disk into the AT environment, a drive type table must be selected that represents the physical characteristics of the drive being used. This information consist of the number of cylinders, heads, and sectors per track. It is often difficult to match the drive and the table exactly. When integrating an ESDI hard disk, the number of sectors per track becomes the most important parameter to match. Most system BIOS roms support only the older MFM/ST506 drives that used 17 sectors per track. The ESDI disk drive will have typically 34 sectors per track when operating in the hard sector mode (required by the 1007A controllers). The BIOS generates the needed information by using the ability of the ESDI drive to present the actual drive characteristics to the controller. The BIOS reads the ESDI information and generates the appropriate logical parameter tables. Since all low level formatting is done at 35 SPT (in order to accomodate the extra 'Alternate' sector feature) the parameter tables generated will make all their calculations based on this 35 SPT value. Parameter tables are constructed for all the translation features of the controller.

3. Options.

The 1007A BIOS offers the following features to the user:

A. Drive type routine

The drive types can be changed by using the "+" and "-" keys. Assuming that all the ESDI drives in question are specified at 34 SPT, there are four possible choices that can be implemented for a drive:

1. No drive present - the BIOS will automatically select a drive type 0 if there is no drive present. The user will get the message "*** NONE SELECTED OR NO DRIVE PRESENT ! ***" next to the drive number.

2. A selection with 17 SPT. This feature should be used when the drive is being used in a system that does not recognize drives with SPT values other than 17 SPT. Although the low level format will still be at 35 SPT, logical parameter tables will be created reflecting 17 SPT (with translation enabled). See section on Translations for more details.

3. A selection with 34 SPT. This feature should be used if the system being used recognizes the standard 34 SPT drive.

4. A selection with 63 SPT. This feature should be implemented only when the drive in question is specified as having greater than 1024 cylinders. Translation should always be enabled when such a condition exists. What this feature does is to allow full use of the all the cylinders of the drive (even though most AT BIOS' only recognize 1024 cylinders as a maximum) through a translation scheme that uses 63 SPT. See section on Translations for more details.

B. Low level Format Routine

Formatting routines are present to do the low-level initialization of the disk surface. The drive is formatted at 35 sectors/track (SPT). Transparent to the user, the format routine formats with a sector skew and also formats a spare sector on each track. This sector is used by the surface analysis routines to provide the ability to reallocate a bad sector on a track. It is also used to store the parameter information generated by the BIOS. This information is written to the spare sector on cylinder 0, head 0. The sector skew, which is fixed at two, allows the controller to maintain a one to one interleave accross all head boundaries. Sector Skewing is a method of formatting in which the sector numbers are rotated in the interleave table for each track (see Appendix 7.0).

C. Enter Defect List Routine

This routine allows the user to enter the list of 'bad tracks' as listed by the drive manufacterer on the drive.

D. Surface Analysis Routine

A surface analysis routine is available that identifies bad tracks on the drive and in the event that there is only one sector bad on the track (and it is NOT sector zero), assigns the alternate sector (sector 35) in the place of the bad one. This 'saves' the track from being marked bad by the controller.

If one had entered a list of the 'bad tracks' at the begining of this routine, after the surface analysis all the tracks marked bad will now be error free (within the constrictions of the above paragraph).

E. Verify Drive Routine.

The verify routine will identify all the 'bad tracks' on the drive and list them by head and cylinder number.

4. User Interface

The user gains access to the BIOS from the DOS DEBUG utility by giving the command "G=C800:5". This causes instructions in the BIOS rom to be executed starting at location 5 of the segment address. Note that the segment address may change depending on the BIOS address jumpers W1 and W2. When execution is started the user is presented with the following simple menu screen:

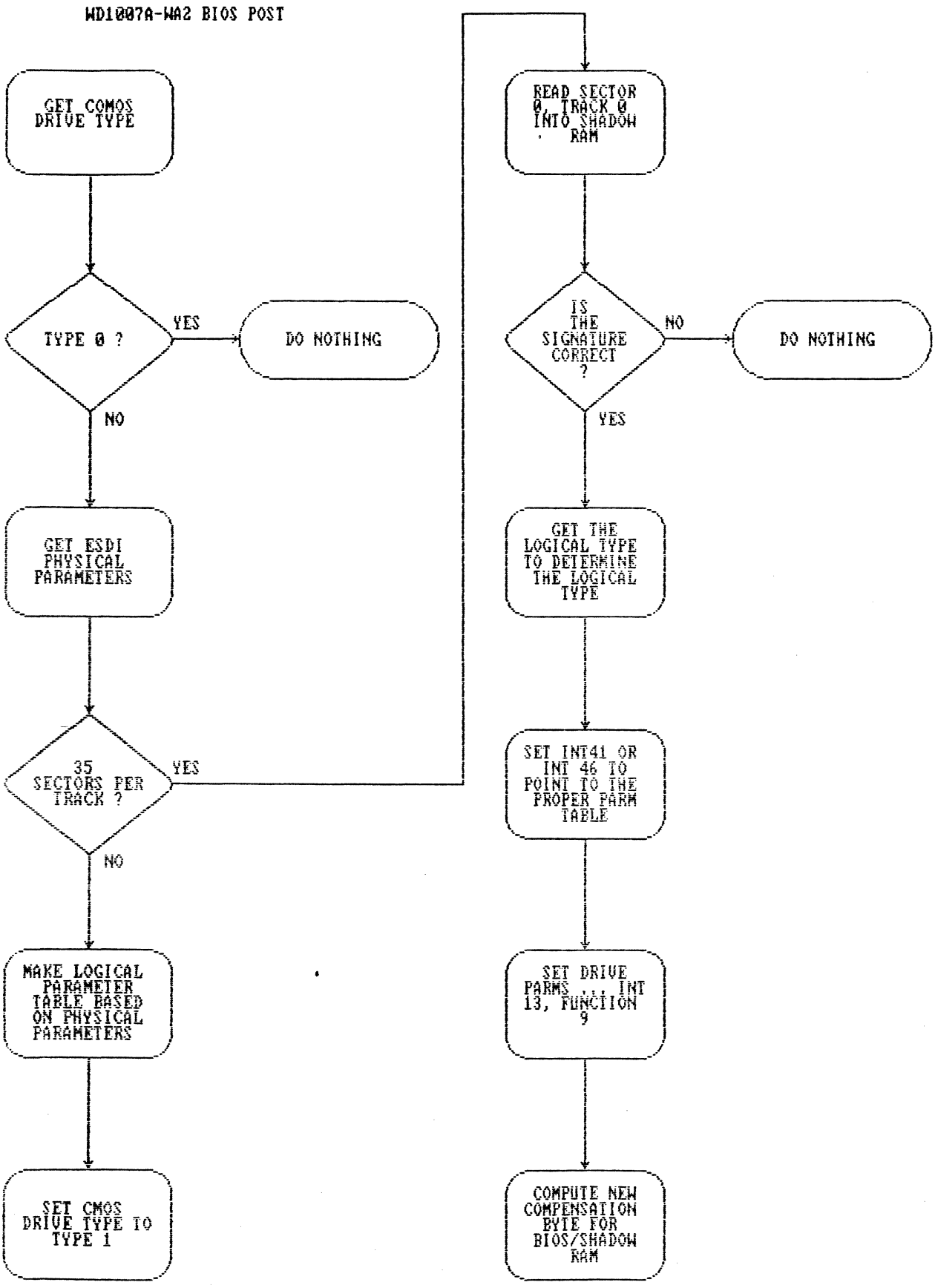
```
*** Western Digital 1007A-WA2 Initialization Utilities, Rev. 1.0***

PRESENT DRIVE SETUP ... + or - to change, <ENTER> for selection

DRIVE 0 CYLINDERS XXX HEADS XX PRECOMP CYLINDER XXX SPT XX
DRIVE 1 CYLINDERS XXX HEADS XX PRECOMP CYLINDER XXX SPT XX


Change Drive Types     ---> 1
Low Level Format       ---> 2
Surface Analysis       ---> 3
Verify Drive           ---> 4
Enter Defect List      ---> 5
Exit and Reboot        ---> 6


Enter Choice (1-6) -->
```

All functions can be executed by simply entering the number for the desired routine. The BIOS will execute that routine and then prompt the user to press a key to return to the main menu. Note that all changes made while in the BIOS will only be finalized after a proper exit through function 6 - otherwise some features might not be valid including drive type selected.

If the drive physical parameters are specified at a value other than 34 SPT, the 1007A BIOS will allow the board to function. The BIOS will read the drive parameters off the drive and if it recognizes the SPT value as being different from 34 it will allow a low level format at the read values with no skew and no alternate sector and at 1:1 interleave.

5. 1005 (1005-WAH) Mode As Opposed To The 1007 (1007A) Mode.

If a drive has been formatted with the WD1005-WAH it has been formatted at 34, 35 or 36 SPT. In the 1005 (1005-WAH) mode, the number of SPT were read from the drive (as opposed to the 1007 mode where the controller specifies the SPT through the 'set the unformatted bytes/sector' command). If one desires to use the 1007A in the 1005 mode, the following two facts should be true:



NOTE: This procedure is performed for both drives 0 and 1.

FIG. 1

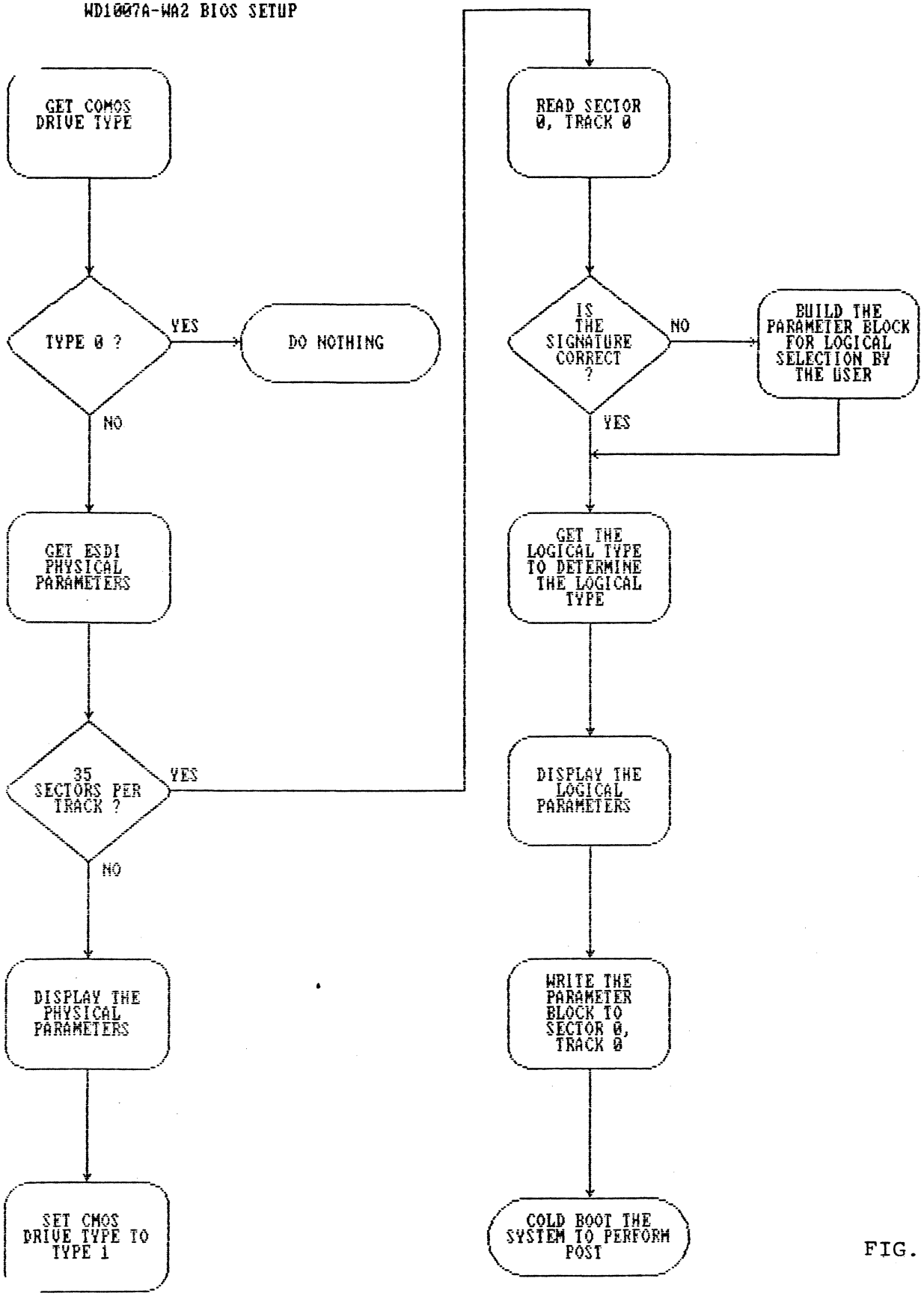


FIG. 2

NOTE: Except for the cold boot, the same procedure is performed for bot drives 0 and 1.

WD1007A-WA2 BIOS FORMAT

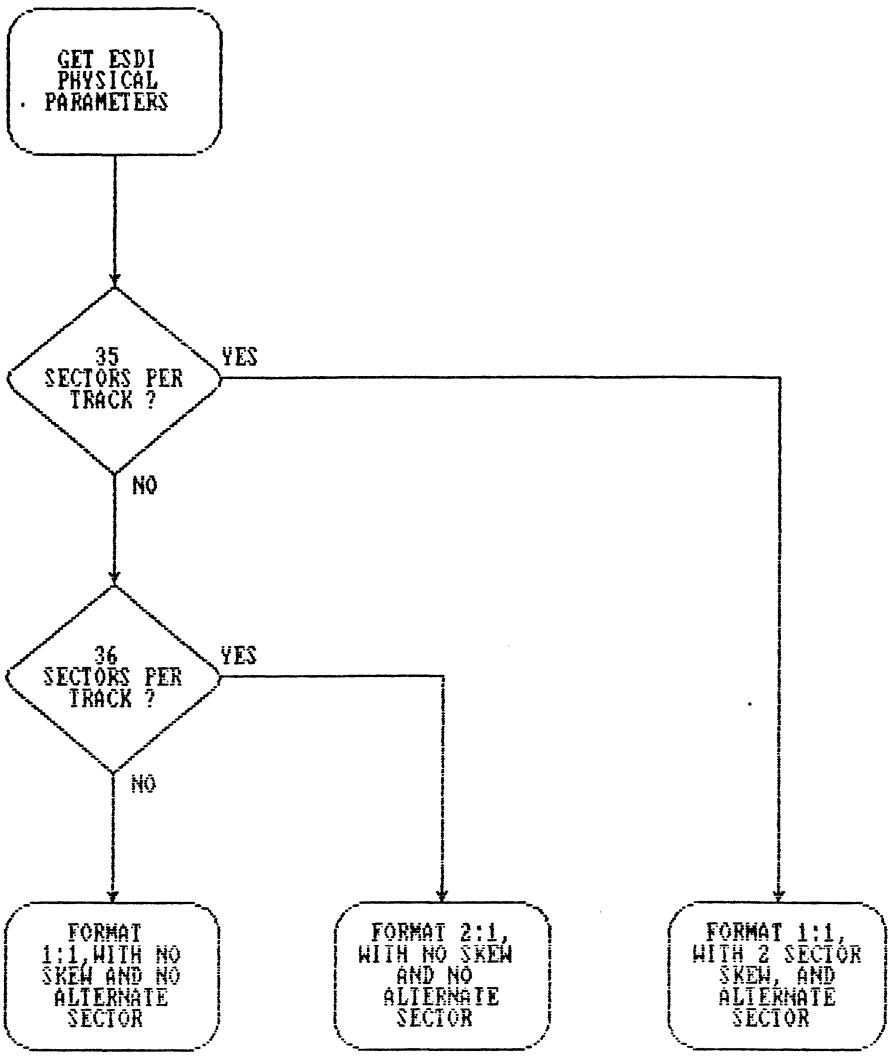


FIG. 3

NOTE: The skew factor of 2 allows for head switch time ... there is no compensation for a cylinder change. The alternate sector is represented with an ID of 0, thereby providing sectors 1-34 for system use.

WD1007A-WA2 BIOS SURFACE TEST

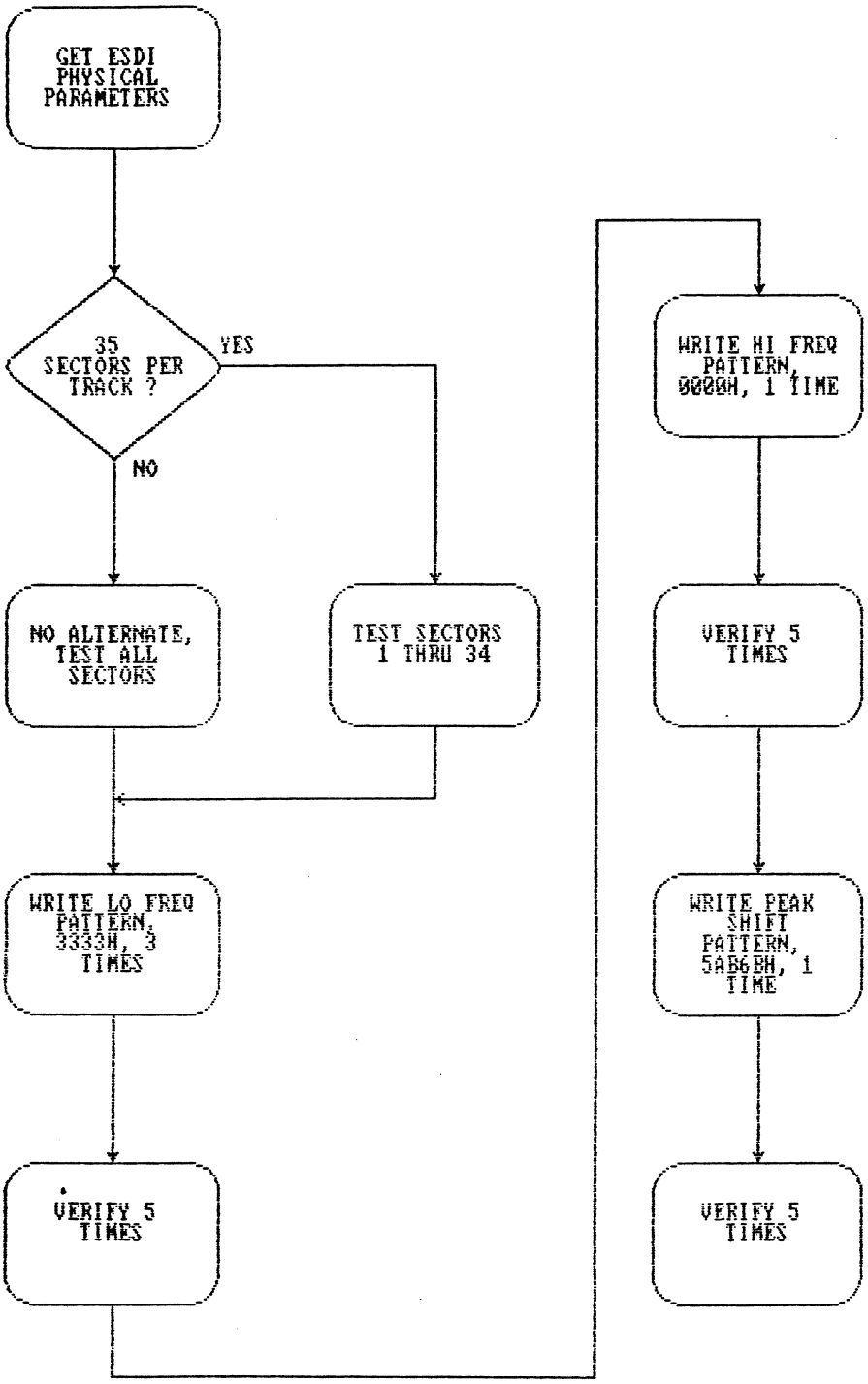
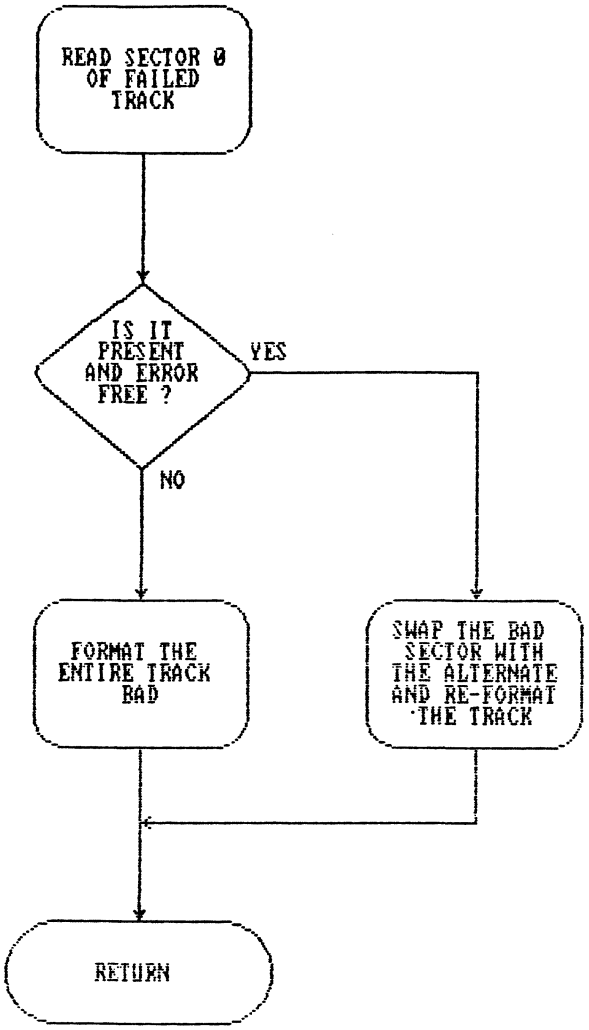


FIG. 4

NOTE: All operations are performed on a track ... if, at any time, there is an error, an alternate is assigned, or format bad track, and the test is resumed from the start of the failed test.

WD1007A-WA2 BIOS ALTERNATE ASSIGNMENT



NOTE: When the alternate is swapped with the bad sector, it is re-assigned the ID of 0FFH. The skew factor is accounted for during the re-assignment.

FIG. 5

WD1007A-WA2 BIOS ARCHITECTURE

ADDRESS	BIOS ROM ... 2764 EPROM	SHADOW RAM ... 256 BYTES
	55h, 0AAh - BIOS signature	
	10h - length, # of 512 byte blocks (8k)	
	JMP INIT - entry point to POST routine	
	JMP SETUP - entry point to SETUP routine	
F00		DRIVE 0 SIGNATURE
F10		DRIVE 0 TYPE (INDEX TO LOGICAL)
F20		DRIVE 0 PHYSICAL TABLE
F30		DRIVE 0 LOGICAL TABLE ... 34 SP
F40		DRIVE 0 LOGICAL TABLE ... 17 SP
F50		DRIVE 0 LOGICAL TABLE ... 63 SP
F80		DRIVE 1 SIGNATURE
F90		DRIVE 1 TYPE (INDEX TO LOGICAL)
FA0		DRIVE 1 PHYSICAL TABLE
FB0		DRIVE 1 LOGICAL TABLE ... 34 SP
FC0		DRIVE 1 LOGICAL TABLE ... 17 SP
FD0		DRIVE 1 LOGICAL TABLE ... 63 SP
FFF	COMP BYTE - required to insure that modulo hex 100 checksum equals 0	COMP BYTE

OTE:
At system RESET, the shadow ram is disabled, and the entire 8k of ram is enable
A dummy write to the shadow ram enables it and disables that portion of the ro
Of course, the compensation byte will be different, therfore, must be calculate

FIG. 6

a. The configuration switches on the drive should be set to the appropriate SPT value.

b. Jumper W8 should be present.

This allows one to make the 1007A fully equivalant to the 1005-WAH for all operations. As such all drives that have been formatted using the 1005-WAH can be read/written to using the 1007A.

6. Drives With Physical Parameters That Are Greater Than 34 SPT.

There are some ESDI drives in the market that are specified at greater than 34 SPT. This usually implies that the drive functions at 15 MB/s data rate. The 50C12, which is the 1007A hard disk controller, is specified to function at up to 10 MB/s. As such it is recommended that the 1007A NOT be used with drives that require greater than 10 MB/s data rates.

If the above drive (with the greater than 36 SPT specification) functions at 10 MB/s, the 1007A can successfully be used, if the system the drive is being used in recognizes the physical drive parameters explicitly.

2.3 Operation

The WD1007A controller can be installed into any 16 bit slot in the IBM PC/AT or compatible host computer. By referring to the jumper option, the controller can be configured for the desired mode of operation. Be sure that the drive configuration is set properly to support the hard sector mode. Connecting cables for the ESDI hard disk are the same as those used on the ST506 interface disks. Also, device ID jumpers are implemented on the ESDI device just as with ST506 drives. In order to use an ESDI drive in a given system, a three step process has to be followed:

1) Low level format;
2) Active drive partitioning through operating system;
3) High level format.

See the 1007A Users Guide for a more detailed explanation on the mechanics of installing and running and ESDI disk controller using the 1007A board.

A. Low Level Format

After the proper parameter information has been selected (see 2.1.3), the hard drive must be initialized through a low level format.

a) If the WD1007A controller does not have a BIOS, it is recommended that the user use routines available in third party software or use WDFMT (a formatting utility available on diskette from Western Digital as part of the support package for the 1007A).

b) If the WD1007A has a BIOS, low level formatting can be done through the BIOS (see section 2.2).

B. Active Drive Partitioning Through the Operating System

When the disk drive has been low-level formatted, it is now ready to be prepared for use by the operating system. Some operating systems handle disk usage differently so their methods of preparing the disk are different. We will cover the two main operating systems used today, MSDOS and SCO Xenix.

1. MSDOS (FDISK and FORMAT)
These two utilities are used to prepare the disk for use by the MSDOS operating system. In order to use the typical large capacity ESDI drives under MSDOS, the user must use version 3.3 or a compatible version that supports the division of a large physical drive into smaller logical volumes. It must be noted that the MSDOS operating system has a limit of 33.3 Megabytes per volume. If the version of MSDOS does not support the creation of multiple logical drives, disk enhancement software drivers must be used to obtain full usage of the high capacity drives.

2. SCO Xenix
The Xenix operating system does not limit the size of the disk volume. During the installation of the Xenix operating system, the user is prompted for information on how the disk is to be used. The entire disk may be used or a partition for Xenix and one for DOS may be created. The Xenix installation will perform all tasks comparable to the DOS FDISK and FORMAT utilities. A unique feature of SCO Xenix version 2.1 is the ability to create a parameter table for the drive outside of the system BIOS. The user is prompted at installation time as to what parameters are to be used and allows them to be customized for application requirements. Previous versions of the operating system assumed 17 sectors per track on the drive regardless of the parameter table information presented. These versions require the 17 sector translation operation mentioned above.

C. High Level Format

The drive can now be high level formatted with the given operating system through the 'Format C: (or D:)/S' command.

APPENDIX

1. Commands

A. Standard AT Commands

Command	Op Code
Read sector	20H
Write Sector	30H
Restore (Recal)	1XH
Set Parameters	91H
Format Track	50H
Diagnostics	90H
Seek	7XH
Read Verify	40H

Read Sector - A number of sectors (1-256) are read from the selected disk. If the drive is not positioned at the specified cylinder, an implied 'seek' will occur. Drive furnished ECC check bits will be used if the Read Long mode is specified. Single burst data errors (up to 11 bits) will be corrected if retries are enabled and the long mode is not selected. Uncorrectable errors do not inhibit the (error sector) data transfer, however multi-sector transfers will terminate. The WFDC interrupt occurs as each sector is ready for system input. The WFDC also caches the remaining sectors until the buffer RAMs are full upon completion of a successful Read Command. When the next Read Command occurs, and if the desired sectors are the same as the cached sectors, the data transfer occurs immediately. cacheing therefore improves the data throughput by reducing the disk access time. IRQ14, BSY and DRQ bits of HDSTT register operate in the same fashion as in non-cache operations.

Write Sector - A number of sectors (1-256) are written to the selected disk with an implied seek occurring, if required. Multiple sector write (and read) operations may cross track and cylinder boundaries. The Write Long mode appends the ECC bytes to the data supplied by the system processor. The data request bit (On) along with the command cause the system processor to output the contents of the first data buffer. An interrupt occurs as the data for each subsequent sector is required.

Read Verify - This command verifies that a previous write command is correct by checking ECC bytes. The host processor does not input read data. The command may be used with multi-sector operations. An error condition will abort a multi-sector verify operation. The retry command may be used with this command.

Seek - The Seek command positions the drive heads over the cylinder specified in the Task File registers (HDCLH/L) and clears any track offsets. The command aborts under the conditions noted for the Restore command above. Bit SKC of the HDSTT register sets true upon the completion of a Seek command. The fixed disk priority interrupt (IRQ14) issues after a successful ESDI Seek command transfer. The host can check for completion of the seek operation by checking bit SKC of HDSTT register.

Restore - The selected ESDI drive received a Seek-to-Cylinder 0 command via the serial command interface (WD1018 port 1.5). The drive heads seek to cylinder 0 and any track offsets are clear. The command aborts when the ERR bit sets in the status register. The Aborted Command (ACD) bit sets in the error register if the WD1018 receives an Attention interrupt from the drive indicating a transfer protocol or transfer parity error.

Diagnostics - The diagnostics command causes the WD1018 to execute an on-board diagnostic program and to report the test results to the WD50C12 Error Register. See Appendix for WFDC self tests.

Set (Drive) Parameters - This command communicates drive parameters to the controller. It selects the had, cylinder, and sector for each drive. The WD1018 uses the drive parameters in the execution of multi-sector commands and in evaluating legal controller commands.

Format Track - The Task File specifies the track to be formatted with identification, data, and check fields in accordance with the interleave table transferred to the sector buffer. The interleave table is composed of two bytes per sector, with the first byte set to "00", for a good sector or "80h" for a bad sector. The second byte designates the logical sector number. The Task File (HDSCT and HDSDH) specifies sectors per track and sector size. Command completion initializes the data field to 'zeros' and appends four ECC bytes after the data field. The Completion Interrupt occurs as each track is formatted. The WD1007A-WA2 controller forces 512 bytes/sector, 35 sectors/track, and the hard sectored drive format.

B. Non-Standard AT Commands

Command	Op Code
Write Data Stack	E8H
Cache Control	EFH
Read Parameters	ECH
Read Data Stack	E4H
Initiate ESDI	E0H

Read Data Stack - This diagnostic command allows the host to read the sector buffer without executing a disk read operation. This command does not generate an interrupt upon completion.

Write Data Stack - This diagnostic command allows the host to write data to the sector buffer without executing an actual disk write command. This command does not generate an interrupt upon completion.

Initiate ESDI - This command allows the system processor to send instructions directly to the selected drive by loading the AMAC's cylinder register and executing the Initiate command. The host must load AMAC's cylinder registers (high and low data bytes) with the command it wants the drive to execute prior to issuing the Initiate ESDI command. The controller serializes the data, adds the required parity bit and transmits the instruction to the drive. The drive completes the instruction and transmits completion status to the controller. The drive's completion status data is then stored back into AMAC's cylinder registers for host access.

The following examples show how the Initiate ESDI command is used:
Using ARM (Western Digital Test Software) when * appears, type 'MAKE' and 'ENTER'.
Monitor will display:

```
Enter Task File Parameters: All entries are in hex
Enter Command =
Enter Cylinder # =
Enter Head # =
Enter Sector =
Enter 'E0' for the command.
Enter '20' (Request Standard Status) for the Cylinder number.
```

The high byte (bits 15 - 8) of the ESDI command will go to Cylinder High REgister, and the low byte (bits 7 - 0), if applicable, will go to Cylinder Low Register. Refer to ANSI ESDI Specification, Document No. X3T9.3/8X, for all ESDI commands.

The host can now access the drive's status by reading the cylinder register's addresses (AF4 - AF5). The high order status byte is stored in the Cylinder High Register: the low order status byte is stored in Cylinder Low Register.

Using DEBUG enter:

```
01F4 00
01F5 20    ;Output Read Status Command
01F7 E0    ;Initiate ESDI Command
11F4
11F5     ;Read Drive Status
```

Cache Control - This command (EF) allows the user to enable or disable cacheing. By writing AA (enable) or 55 (disable) into the Write Precomp Register (1F1), then issuing the Cache Control command, cacheing will be turned on or off accordingly. The command will abort if any other code is written into 1F1, and cacheing stays unchanged. cacheing is enabled in default.

Read Parameters - This command causes the MC8753 to store 49 words of drive and controller parameters into the sector buffer for host access.

A. ESDI Config Information

General configuration

fixed cylinders
removable cylinders
heads
unformatted bytes/track
unformatted bytes/sector
sectors/track
minimum bytes in ISG
minimum bytes in PLO
words of vendor unique status

B. Controller Information

serial # (20 ASCII characters...0 = not specified)
controller type...0 = not specified
1 = single ported, multi sector buffer
2 = dual ported, multi sector buffer
3 = dual ported, multi sector buffer, cache

controller buffer size in 512 byte increments
# of ECC bytes xferred on long operations
controller firmware revision (8 ASCII characters)
# of sectors xferred per interrupt on read commands
double word capability (0 = not capable, 1 = capable)

ESDI Commands

Function			CMD Function Definition	CMD Modifier Applicable Bits 11-8	CMD Parameter Applicable Bits 11-0	Status/conf returned to controller
14	13	12				
0	0	0	Seek	No	Yes	No
0	0	1	Recalibrate	No	No	No
0	1	0	Request Status	Yes	No	Yes
0	1	1	Request Configuration	Yes	No	Yes
1	0	0	Select Head Group*	No	Yes	No
1	0	1	Control	Yes	No	No
1	1	0	Data Strobe Offset*	Yes	No	No
1	1	1	Track Offset*	Yes	No	No
0	0	0	Initiate Diagnostics*	No	Yes	No
0	0	1	Set Bytes per Sector*	No	Yes	No
0	1	0	Reserved	-	-	-
0	1	1	Reserved	-	-	-
1	0	0	Reserved	-	-	-
1	0	1	Reserved	-	-	-
1	1	0	Set Configuration*	No	Yes	No
1	1	1	Reserved	-	-	-

Optional commands

3.0 ESDI Request Configuration Data

Command Modifier Bits				Function
11	10	9	8	
0	0	0	0	General Configuration Response bits
0	0	0	1	Number of Cylinders-Fixed
0	0	1	0	Number of Cylinders-Removable
0	0	1	1	Number of Heads
0	1	0	0	Unformatted Bytes per Track
0	1	0	1	Unformatted Bytes per Sector(Hard Sector mode)
0	1	1	0	Number of Sectors per Track(Hard Sector mode)
0	1	1	1	Bytes in ISG Fieldc
1	0	0	0	Bytes per PLO Sync Field
1	0	0	1	Number of Vendor Unique Status Words Availble
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Vendor Identification

5.0 ESDI Status Response Bits

Bit	
15	Reserved
14	1=Removable Media Not presetn 0=If Not Removable
13	1=Write Protected-Removable Media 0=If Not Removable
12	1=Write Protected-Fixed Media
11	Reserved
10	Reserved
9	1=Spindle Motor Stopped by Stop command 1=Spindle Motor Stopped for Other(e.g. reset)
8	1=Power On Reset Conditions Exist(reconfiguration or Spindle Motor command may be required)
7	1=Command Data Parity Fault
6	1=Interface Fault
5	1=Invalid or Unimplemented command Fault
4	1=Seek Fault
3	1=Write Gate with Track Offset Fault
2	Vendor Unique Status Available
1	1=Write Fault
0	1=Removable Media Changed since last request

6.0 Executing ESDI Commands

As mentioned above, the host can send any of the ESDI commands to the device and receive data and status upon completion.

Below are some sample routines to send command and receive data from the drive.

EXAMPLE 1
REQUEST CONFIGURATION BYTE
(NUMBER OF HEADS)

```
mov   ah,cyllow          ;cylinder low address-1F4
mov   al,00              ;low byte of ESDI command
out   dx,al              ;output to port
mov   dx,cylhigh         ;cylinder low address-1F5
mov   al,33              ;request configuration command
                         ;with modifier for head byte
out   dx,al              ;output to port
mov   dx,cmdreg          ;command register address-1F7
mov   al,initesdi        ;initiate ESDI command-E0
out   dx,al              ;output to port
```

This routine loads the 16 bit ESDI command into the cylinder high and low registers, 1F5 and 1F4, and then loads the initiate ESDI command into the command register, 1F7. The Host should check for the controller to go not busy, then read the data returned by the drive, from the cylinder high and low registers. The controller Status register will reflect any error condition and the Host can request Status from the drive to determine if any device level error occurred.

A 1007A support diskette is available from Western Digital that encorporates these extended command features into three demo programs. These programs are explained in Appendix F.

The above command information is intended to give the user a general overview. Specific information can be obtained from the 1007A engineering specification available from Western Digital, and the ANSI Specification on the ESDI interface, available from the ANSI committee in Washington D.C.

7.0 WDFMT

Western Digital provides a low-level format utility that will allow the user to prepare the drive for use by the system. The program includes routines for low-level formatting, disk verify, surface analysis and bad track entry. When using the 1007A board one should use an interleave of 1, a skew on 2 and format at 35 SPT with an alternate sector. See the explanations for these features provided below.

A. Sector Skewing

Sector Skewing is a method of formatting a drive in which sector numbers are rotated in the interleave table each time a new head on a cylinder is formatted. For example, using a 2 sector skew, the first sector after index on head 0 will be identified as sector 1. The sector identified as sector 1 on head 1 will be the third physical sector from index.

Sector Skew formatting is available with version 2.10 of WDFMT.

Example: Ten sectors per track with a skew of 2 and interleave of 1

Head #	Sector #'s									
0	1	2	3	4	5	6	7	8	9	10
1	9	10	1	2	3	4	5	6	7	8
2	7	8	9	10	1	2	3	4	5	6

This formatting procedure allows the controller to maintain the 1:1 interleave when reading across the head boundary. This becomes critical when the number of sectors per track increases and the time allowed for overhead functions to be completed decreases as with ESDI applications. Because of controller firmware overhead, the controller will not be able to read the ID Field of the first sector on the next head. By changing the sector numbers, the controller can do the needed tasks and be ready to read the sector marked as number 1. The minimum sector skew factor for proper performance of the WD1007A has been determined to be 2. Different skew factors may be needed to optimize performance for different applications.

B. Sector Spare

Another option available in WDFMT Version 2.10 is the ability to format a spare sector on the track. This spare sector is given the ID of zero, making it invisible to the AT compatible System BIOS, which

expects sector numbers starting at 1. This sector is always formatted as the last physical sector on the track.

The surface analysis portion of WDFMT will use that spare sector if an error is encountered with any sector on the given track. The program will reformat the track, numbering the bad sector as zero and shifting the following sectors one to the right. If more than one sector is found to be bad on the track, the entire track is marked as bad when reformatted.

This feature is useful since many system BIOS ROMS that support ESDI drives have a sector per track parameter of 34. By using the spare sector option, the drive will look like it has only 34 sectors. The spare sector can be used for the above mentioned bad sector reassignment, or it can be used to store custom data by providing software drivers to use the hidden sector.

WD1007A-WA2 JUMPERS CONFIGURATION TABLES

TABLE I

BIOS ADDRESS RANGES	JUMPER SETTINGS		
	W1	W2	W3
C8000 - C8FFF	2 - 3	2 - 3	JUMPED
CA000 - CBFFF	2 - 3	1 - 2	JUMPED
CC000 - CDFFF	1 - 2	2 - 3	JUMPED
CE000 - CFFFF	1 - 2	1 - 2	JUMPED
DISABLE			NON JUMPED

TABLE II

FLOPPY CONTROLLER	W4	W13 IN ETCH
ENABLE	NON JUMPED	UNCUT
DISABLE	JUMPED	CUT

TABLE III

DRIVE TYPE INPUT	W5
2 SPEEDS SPINDLE MOTOR	JUMPED
SINGLE SPEED	NON JUMPED

TABLE IV

FLOPPY ADDRESS RANGES	W6
37X	1 - 2
3FX	2 - 3

TABLE V

HIGH DENSITY SELECTION	W7
5.25", 1.2M	1 - 2
3.5", 1.44M	1 - 2

TABLE VI

WD1005 MODE	W8	JUMPED
WD1007 MODE		NON JUMPED

TABLE VII

CHASSIS GROUND & DIGITAL GROUND	W9
CONNECTED	2 - 3
UNCONNECTED	1 - 2

WD1007A-WA2 DEFAULT SETTING		WD1007A-WAH DEFAULT SETTING	
W1	2 - 3	W1	2 - 3
W2	2 - 3	W2	2 - 3
W3	JUMPED	W3	JUMPED
W4	NON JUMPED		
W5	NON JUMPED		
W6	2 - 3		
W7	1 - 2		
W8	NON JUMPED	W8	NON JUMPED
W9	NON JUMPED	W9	NON JUMPED
W10	NON JUMPED	W10	NON JUMPED
W11	JUMPED	W11	NON JUMPED
W12	NON JUMPED	W12	NON JUMPED
W13	UNCUT		
W14	NON JUMPED	W14	NON JUMPED
W15	NON JUMPED	W15	NON JUMPED

TABLE VIII

DIGITAL INPUT REG MODE	W10
LATCHED	JUMPED
NON LATCHED	NON JUMPED

TABLE IX

DISKCHANGE INPUT	W11
WITH FDC OPTION	JUMPED
WITHOUT FDC OPTION	NON JUMPED

TABLE X

PRIMARY/SECONDARY HARD DISK ADDRESSES	W12
1FX	NON JUMPED
17X	JUMPED

TABLE XI

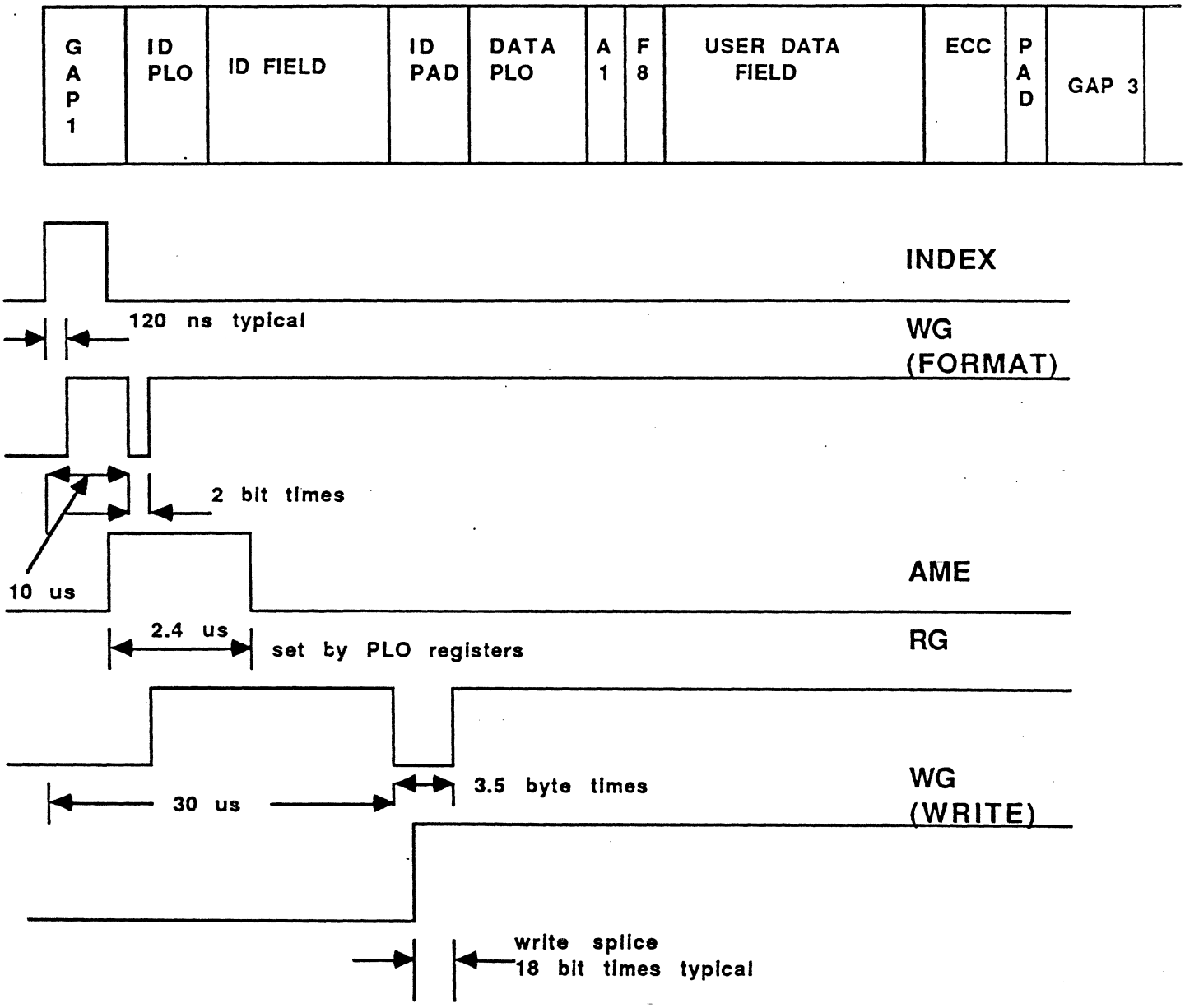
SECTOR TRANSLATION	W14
ENABLE	NON JUMPED
DISABLE	JUMPED

TABLE XII

ECC SELECTION	W15
7 BYTES	JUMPED
4 BYTES	NON JUMPED

* WD1005 Mode - The controller reads 'Unformatted bytes/sector' from drive
WD1007 Mode - The controller reads 'Set Unformatted bytes/sector' command to the drive.

WD1007A TRACK FORMAT AND TIMING



PRELIMINARY

ENGINEERING SPECIFICATION

WINCHESTER DISK/FLOPPY DISKETTE CONTROLLER MODULE

WD1007A-WA2
SPECIFICATION NO. 96-000697

OCTOBER 2 , 1987

ENGINEERING SPECIFICATION

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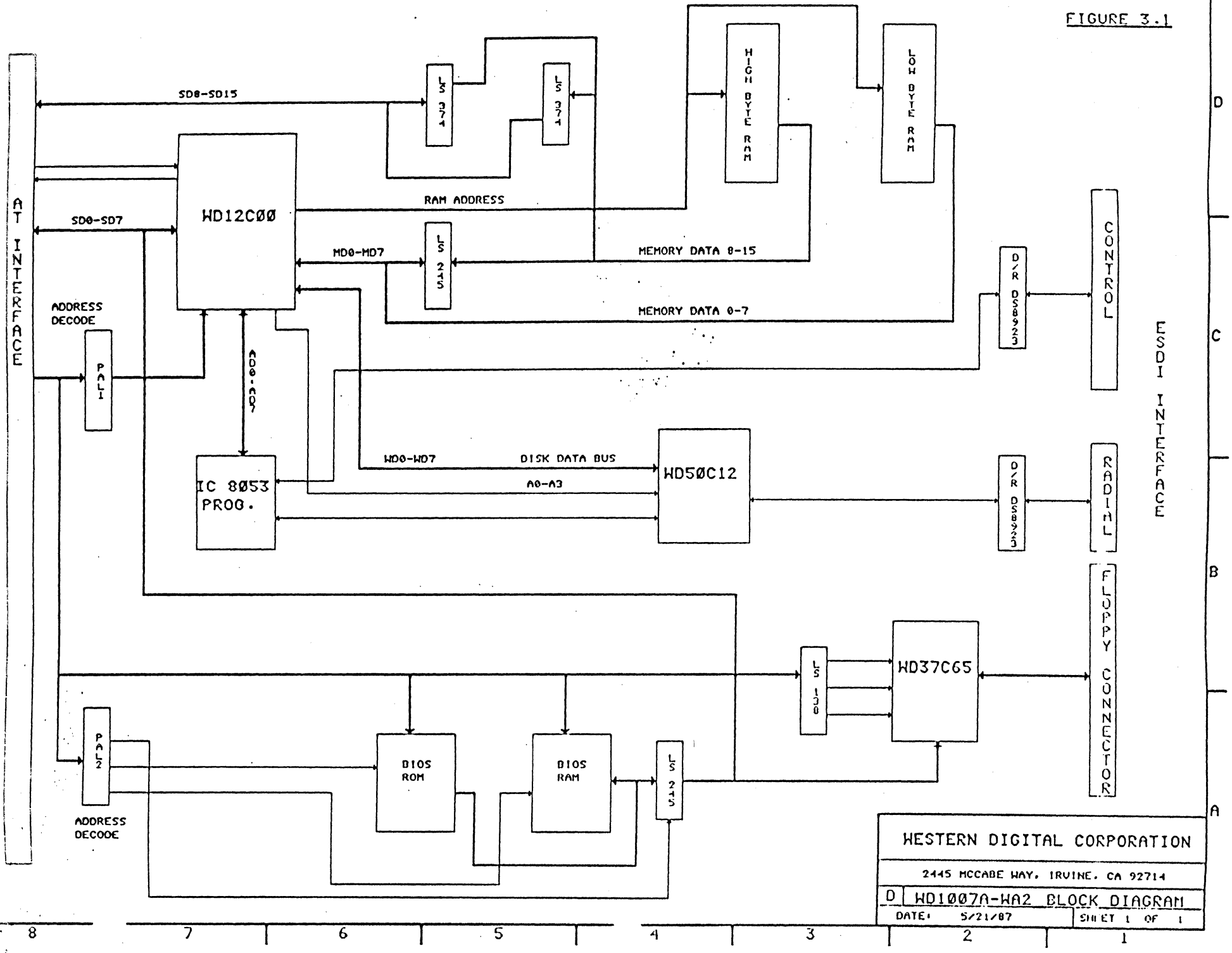
FIGURE 3.1



WESTERN DIGITAL CORPORATION	
2445 MCCABE WAY, IRVINE, CA 92714	
D	WD1007A-WA2 BLOCK DIAGRAM
DATE: 5/21/87	SHEET 1 OF 1

1.0 SCOPE

This document describes the functional, electrical and logical design characteristics of the WD1007A-WA2 Winchester/Floppy Disk Controller (WFDC) module. The board is used to interface two ESDI compatible fixed disk drives and two 5 1/4" floppy disk drives to the PC-AT computer I/O Channel bus structure.

The fixed disk section includes the WD5012 Winchester Disk Controller, the IC 8753 Prog. Buffer Manager Control Processor, RAM sector buffer memory and associated control logic. The floppy control section is implemented with the WD37C65 Floppy Disk Controller. The design features a Buffer Manager and Control (AMAC) gate array for module logic reduction and for 1:1 interleave format support.

Portions of the IC 8753 Prog. control processor protocol specification (firmware) are included as a part of this document as is a description of the module self-test operation. Software which resides in the PC processor (either test or operational) or is installed in the optional BIOS ROM is not included as a part of this document.

2.0 APPLICABLE DOCUMENTS

2.1 WD1007A-WA2 BOARD DOCUMENTS

61-600079	P/L & Assembly
60-600079	PWB Fabrication
65-600079	Artwork, PCB
96-000XXX	Test Specification
68-600079	Schematic Diagram

2.2 COMPONENT DOCUMENTS

	WD50C12 Winchester Disk Controller
	WD37C65 Floppy Disk Controller
62-002062-801	IC 8753 Prog. Control Processor
96-000034	WD12C00A-JU22 (AMAC) Specification
68-000147	AMAC TTL Schematic Diagram (Reference only)
62-601011	PAL Specification, Address Decoder, Fixed Disk Section
62-601012	PAL Specification, Address Decoder, BIOS ROM
	IC 8053 Prog. Firmware Listing
	WD1007A-WA2 BIOS Firmware Listing

3.1 HARDWARE OVERVIEW

The WD1007A-WA2 Winchester/Floppy Disk Controller is a PC-AT bus compatible surface mount technology printed-circuit module that interfaces up to two ESDI type fixed disk drives and two 5 1/4" floppy disk drives to the system processor. The module fixed disk control section includes the WD5012 and IC 8753 Prog. Winchester disk control components and two 8192x8 RAM's for sector data buffering. The (optional) floppy disk section includes the standard WD37C65 Floppy Disk Controller and an associated address decode TTL logic.

A primary feature of the module is an 84-pin Buffer Management and Control (AMAC) gate array used to minimize the module circuitry and provide 1:1 sector interleave support. Figure 3-1 is a simplified block diagram of the module fixed disk control section and the available options - each major block is briefly described below. The module logic is fully described in the referenced documents or in subsequent sections of this specification.

3.1.1 WD50C12 WINCHESTER DISK CONTROLLER

The WD50C12 Winchester Disk Controller (WDC) is an advanced design VLSI device that provides the data handling and control for an intelligent Winchester disk controller. The major features of the device include:

- *Support 1:1 interleave and data transfer rate up to 15 Mb/s*
- *Support NRZ disk data format*
- *Support Hard Sector mode (Soft Sector mode - future option)*
- *Software selectable 56 bit ECC, 32 bit ECC, or 16 bit CRC*
- *Software selectable 11 or 22 bit error correction span when 56 bit ECC is selected*
- *Multiple sector read/write commands*
- *Low power CMOS design*

3.1.2 IC 8753 Prog. BUFFER MANAGER CONTROL PROCESSOR

The IC 8753 Prog. Control Processor (CP) is an eight-bit microprocessor (type
8053) that operates with the WD50C12 and the AMAC logic array to aid in processing the disk commands, to provide sector data buffer management, to help in error recovery procedures and to perform module diagnostics. The processor chip includes internal RAM and ROM memory.

3.1.4 WD12C00A-JU22 AMAC LOGIC ARRAY

Module logic simplification and power reduction is provided by a VLSI logic array that replaces the standard WD1014 support device and several SSI/MSI components. The internal device logic includes the data buffer address registers and memory read/write control, WD50C12 task file image registers, data buffer registers and interfaces to both the system and module (local) bus structures.

Two 8192x8 static RAM memories buffer the sector data between the drive(s) and the PC-AT system bus and ECC correction information between the WD50C12 disk controller and the IC 8753 Prog. control processor. The sector buffers and the above control components allow a 1:1 sector interleave format for optimized system performance..

3.1.6 SYSTEM BUS INTERFACE

The WFDC interfaces to the system bus address, data and I/O control signals. All fixed disk read/write data transfers are 16 bits wide and utilize the host fast programmed I/O transfer protocol. Floppy disk data and both fixed and floppy control and status transfers are 8 bits wide and use the lower data byte (SD07-00) only. The WFDC module register address map is fixed (at a primary or secondary range) as are the bus interrupt requests and the Floppy DMA channel assignment.

3.1.7 WINCHESTER DRIVE INTERFACE

The WFDC interfaces to the fixed disk drives via one 34-pin control cable and two 20-pin data cables in conformance with ESDI signal definitions. Drive power is not furnished via the WFDC module.

3.1.8 WD37C65 FLOPPY DISK CONTROLLER OPTION

The optional WD37C65 Floppy Disk Controller (FDC) is a standard VLSI device that supports both single and double density diskette formats and includes both host and drive data and control interfaces. The units major features include:

* *Multiple sector and track read/write commands*
* *Host DMA and programmed I/O data transfers*
* *High performance digital data separation*

3.1.9 FLOPPY DRIVE INTERFACE

The controller interfaces to the floppy drives via one 34-pin data and control cable per the 5 1/4" PC-AT standard.

3.1.10 BIOS (P)ROM/RAM OPTION

Circuitry is included on the controller to permit a programmed BIOS device to be supplied for special applications. One unique feature of this BIOS option is its shadow ram. The static ram, sharing with the BIOS (p)rom the last 256 upper bytes address of the 8K BIOS's address range, is used to contain the Winchester drive's parameters. This shadow-ram's feature allows the WD1007A-WA2 to interface with all types of ESDI drives without to have to modify the system BIOS. Also option jumpers on board allow the device to be mapped at 1 of 4 address ranges.

3.2.1.2 STANDARD COMMANDS

The WD50C12 allows execution of the standard commands described in the WD50C12 specification and listed below - refer to Section 5.0 for the WD1007A-WA2 command descriptions.

> Restore, Seek, Read Sector, Write Sector, Scan ID, Write Format, Compute (ECC) Correction and Set (Head and ECC) Parameters.

Of these, the Scan ID, Compute Correction and Set (Head and ECC) Parameter commands are not directly available to the system processor (although they may be executed by the IC 8753 Prog. transparently to the host processor).

3.2.1.3 NON-STANDARD COMMANDS

Fixed disk commands to the WFDC are intercepted by the IC 8753 Prog. (with the aid of the AMAC logic) and thus commands not specified in the WD50C12 command list may be defined.

* *Set (Drive) Parameters - Non-standard command used to communicate drive parameters to the controller. The head, cylinder and sector definition for each drive is set by this command. The IC 8753 Prog. uses the drive parameters in the execution of multi-sector commands and in evaluating legal controller commands.*

* *Read Verify - Command used to verify that a previous write command was correct. Read data is not input by the host processor. The command may be used with multi-sector operations. An error condition will abort a multi-sector verify on the error sector. The retry command operand may be used with this command.*

* *Diagnostic Command - The diagnostic command causing the IC 8753 Prog. to execute an on-board diagnostic program and to report the test results (at the WD50C12 Error Register Address).*

* *Write Data Stack - Diagnostic command used to allow the host to write data to the sector buffer without executing a actual disk write command.*

* *Read Data Stack - Diagnostic command used with the above write data stack command allowing the host to read the sector buffer without executing a disk read operation. Neither the read or write data stack command generate an interrupt on command completion.*

* *Initiate ESDI Command - Command (E0) used to allow the system processor to directly send instructions to the selected drive by loading the AMAC's cylinder register and executing the initiate command. The controller serializes the data, adds the required parity bit and transmits the instruction to the drive. The drive completes the instruction and transmits completion status to the controller. The host is interrupted and may read the AMAC's cylinder register to complete the command. See referenced ESDI documents for drive instructions and completion status reponses.*

* *Cache Control - Command (EF) allows the user to enable/disable caching. By writing AA or 55 into Write precomp Register (1F1), then issuing the Cache Control command, caching will be turn on/off accordingly. The command will be aborted if any another code is written into 1F1, and caching stays unchange. Caching is enable in default.*

3.2.1.4 MULTI-SECTOR COMMANDS

Multiple sector read, write and verify commands of up to 256 sectors are allowed without restriction on track or cylinder boundaries. Non-recoverable control errors (drive not ready, write fault, etc.) or non-correctable read data errors will terminate a multi-sector command and the controller expects a 'new command' to continue operation. Corrected read data errors do not terminate the commmand and the controller expects a normal data transfer restart and continuation. The 'long mode' ECC diagnostic commands can be executed; however, the throughput will be reduced. The drive parameters are checked during the execution of this command.

3.2.1.5 DIAGNOSTIC COMMANDS

The controller on-board diagnostic is executed on command and verifies the IC 8753 Prog. local storage, the sector data buffer storage and the IC 8753 Prog., WD50C12 and AMAC data paths (the floppy control section is not checked by this command). Results are encoded and are available to the system processor via the controller error register - refer to Section 8.0.

3.2.1.6 EXTENDED MODE OPTIONS

The AMAC control logic permits multiple sectors to be transferred to the controller as a single data block thus reducing the individual sector transfer overhead. This mode requires a special control processor firmware version and is not normally supplied.

3.2.1.7 BIOS PROGRAMS

The board logic also includes a BIOS (P)ROM option for special programming requirements. The BIOS logic is provided on the board for convienience only. The program requirements are contained in separate documentation if the option is installed.

3.2.2 FLOPPY DISK SECTION

3.2.2.1 COMMAND CONTROL FLOW

The floppy disk control section consists of a WD37C65 floppy controller (which includes the floppy disk control and data interface, an operations control register, a floppy rate control register and a host DMA data transfer controller). A typical command sequence is illustrated below.

* *In the reset or idle state, the WD37C65 control signals are off, the controller and floppy drive status indicate ready, the floppy motor control signals are off, the DMA control terms are disabled and the floppy interrupt is disabled.*

* *The system processor initializes the external DMA controller (for read/write operations), clears the floppy controller reset, enables the DMA and interrupt circuits, sets the operations control and rate registers and outputs the required WD37C65 commmand phase register data sequence.*

* *The WD37C65 executes the command, provides the drive select and control signals, initiates any required DMA transfer requests and updates the result phase data registers.*

and completes the command.

3.2.2.2 STANDARD COMMANDS

The standard WD37C65 commands are listed below for information only - the commands are covered in detail in the referenced WD37C65 specification.

This document does not include hardware or software reference to the system DMA controller.

> **Read Data, Read Deleted Data, Write Data, Write Deleted Data, Read Track, Read ID, Format Track, Scan (Data) Equal, Scan Low or Equal, Scan High or Equal, Recalibrate, Sense Interrupt Status, Specify, Sense Drive Status and Seek**

It is important to remember that the WD37C65 has a specific command, execution and result phase protocol for each command.

3.2.2.3 NON-STANDARD COMMANDS

The WD37C65 includes two registers (in addition to the industry standard UPD765 registers). They are the Operations Register used to control the floppy drive select, drive motor enables, controller reset and DMA request and interrupt enable and the Control Register used to select the floppy data rate. The register addressing and bit assignments are given in Section 5.0 as well as in the referenced specification.

4.0 HARDWARE INTERFACE

This section provides detailed hardware interface information for the WFDC and includes a signal definition of the external signals used by the module. The signals are also listed in the Appendix along with their connector pin assignments. Further information on each signal is provided in the referenced literature.

4.1 SYSTEM BUS INTERFACE

The PC-AT I/O channel signals used by the WFDC are noted below and require both the P1 and P2 system bus connectors.

SA19-SA00
System Address bus - Inputs used to select the WFDC module bus I/O addresses and the BIOS ROM address. The module decodes the lower address input terms (SA09-00) to select the AMAC task file and data registers, the floppy controller and module support registers. The upper bits are used to select the BIOS ROM option system memory base and data address.

SD15-SD00
System Data bus - Bi-directional signals used to transfer 16-bit fixed disk data, 8-bit floppy data and 8-bit module control and status information.

AEN
Address Enable - Input control signal that indicates a valid I/O

System Memory Read - Input strobe used to enable the BIOS ROM and its SHADOW RAM.

-SMEMW
System Memory Write - Input strobe used to write drive parameters into SHADOW RAM.

RESET
Reset - Input module reset used to initialize the WD50C12, IC 8753 Prog. and WD37C65, clear the interrupt levels and to deselect the hard disk drives. When reset clears, the IC 8753 Prog. will automatically execute on-board diagnostic tests and load the test result status in the fixed disk error register.

4.2 FIXED DISK DRIVE INTERFACE

The Winchester drive control and data (ESDI) interface is well documented in the referenced literature and is included here for document completeness only.

4.2.1 CONTROL CABLE

DS1-/2-
Drive Select - Primary output control signal used to connect a drive interface to the control signals. The WFDC is limited to drive 0 or 1. The signals are negated by a system master or programmed reset and are controllable by the IC 8753 Prog.. Both 'latched' and 'non-latched' modes are available by module jumper selection.

HS3-/0-
Head Select - Binary-coded output head select signals allowing drives with up to sixteen R/W heads to be attached to the controller.

WG-
Write Gate - Write enable output control level to the selected drive. The signal is negated by a write fault condition or module reset.

RG-
Read gate - Read enable output control level to the selected drive. This signal is used to control the drive VCO and data recovery circuit.

CMDDAT-
Command Data - Sixteen bit serial data (plus parity) to the selected drive. Data contains instructions for drive internal execution (Recalibrate, Seek, Request Status, etc.). Data is transferred using a drive/controller hand shake protocol (TXREQ- and TXACK-).

TXREQ-
Transfer Request - Control signal to the selected drive asserted when each bit of the command data information is to be transferred to the drive or when the configuration/status data is to be returned from the drive. The signal clears when the selected drive asserts transfer acknowledge (XACK-) to the

TXACK-
Transfer Acknowledge - The selected drive's handshake response to the controller transfer request. The drive either accepts command data or returns configuration/status information.

CSD-
Configuration/Status Data - Response data from the selected drive initiated by the controller command or instruction. The response is 16 bit plus parity and indicates the completion status from the command or drive configuration data. The information is transferred using the transfer request/acknowledge protocol.

INDEX-
Index - Positioning signal from the drive that occurs once per drive revolution. Used by the WDC for track formatting and command timeout.

DRDY-
Drive Ready - Control signal from the drive indicating the drive's motor is up to speed and that the I/O control signals are valid.

ATN-
Attention - Control signal from the selected drive that indicates the drive has a faulty condition or a change of status. This signal is also asserted during drive power-on when the power up sequence is completed.

SCT-
Sector Pulse (or Address Mark Found) - Sector clock from the selected drive. The signal is used in hard sectored format to signal the beginning of each sector and in soft sectored formats to flag detection of an address mark. A non-gated sector clock signal is alsoavailable on the drive radial cable but is currently not used by the controller.

4.2.2 DATA (Radial) CABLES

RDATA0/1(+,-)
NRZ Read DATA - Differential read data input from each drive. The data received from each drive is gated by the drive select signal and is clocked into the WD50C12.

WDATA0/1(+,-)
NRZ Write DATA - Differential signal to each drive that defines the data to be written on each track. The write data is clocked by the pre-synchronized Write Clock generated by the WD50C12.

RCLK0/1(+,-)
Read/Reference Clock - Differential signal from the drive used to determine the data transfer rate. The read clock is derived from the drive data recovery circuits and is supplied during the read data transfer. The drive reference clock is furnished at all other times.

WCLOCK0/1(+,-)

Write Data Clock - Differential output to the selected drive and used to synchronize the write data transitions. This clock is derived from the reference clock signal.

DSLTD0/1-
Drive Selected - Statusl signal from (each) drive informing the controller of the selection status of the drive. This signal is asserted only when the drive has received the drive select signal asserted by the controller.

CMDCPLT0/1-
Command Completed - Status signal from each drive that is asserted when the drive completes any command. This signal will go false upon receiving the first Command Data bit and during power up sequence.

AME0/1-
Address Mark Enable - Control output to each drive used to write address mark onto the disk (WG- asserted) or search for address mark.

4.3 FLOPPY DISK DRIVE INTERFACE

The floppy data and control interface is provided by a single connector and conforms to 5 1/4" drive standards.

FDS1-/2-
Floppy drive 1 and 2 select signals from the FDC operations register. The drive select to both drives is negated by a system master reset or floppy section software reset.

DRATESLCT
Floppy Data rate control - Control signal to the selected drive.

Used to select either 360 rpm or 300 rpm on dual-speed drives.

IDX-
Floppy Index Pulse - Floppy index positioning signal used by the WD37C65 to indicate the beginning of a disk track.

MO1-/2-
Floppy motor enable signal from the digital output register to either drive. The signal is negated by the either system master reset or by the floppy area software reset.

DIRC-
Direction Control signal to the drive to determine the head 'step' direction during controller seek operations. When asserted (low) the step direction is toward the inner tracks.

STEP-
Step pulses to the selected drive from the WD37C65. The step direction is selected by DIRC- above and the step rate is controlled by the WD37C65 controller 'specify' command.

TRK0-
Floppy Track 0 - Positioning flag from the selected drive used during seek operations to indicate head positioning over the

outermost track.

FHS-
Head Select signal to the active drive. Head 1 is selected when the signal is asserted (low).

FWP-
Floppy Write Protect status signal from the selected drive.

FWE-
Floppy Write Enable - Control signal from the WD37C65 to the selected drive. The drive enables write current to the selected head when the signal is active. The signal is negated by system master reset external to the WD37C65 and controlled by several conditions internal to the device.

DCHG-
Diskette Change status signal from the selected drive at the Digital Input Register address (bit position 07) and used for host control or diagnostic information. The signal is not used by the WD37C65.

FWD-
Floppy write (MFM or FM) data to the selected drive. The data rate is controlled by the floppy control register. Write precompensation is automatically provided by the WD37C65 controller.

FRDD-
Floppy read data input from the selected drive. The data is input to the WD37C65 controller (directly) for digital data/clock separation.

4.4 INDICATORS

ACTIVE+/-
LED Indicator(s) - External indicator signals used to provide visual indication of WFDC fixed disk activity.

5.0 SOFTWARE INTERFACE

5.1 REGISTER ADDRESS MAP

The WFDC system I/O port address map is summarized in Figure 5-1 and includes the WD50C12 task file area, the WD37C65 registers and the module auxiliary support registers. The primary address is listed first with the secondary address shown within parenthesis (see Section 7.0 for address selection jumper installation).

ADDRESS (HEX)	REGISTER	FUNCTION
1F0 (170) RW	HDDTR	Hard Disk Data Register (16 bits)
1F1 (171) WO	HDWPC	Write Pre-compensation Cylinder
1F1 (171) RO	HDERR	Error Register
1F2 (172) RW	HDSCT	Sector Count
1F3 (173) RW	HDSSN	Starting Sector Number
1F4 (174) RW	HDCLL	Cylinder Number - Low Byte
1F5 (175) RW	HDCLH	Cylinder Number - High Byte
1F6 (176) RW	HDSDH	Sector Size, Drive/Head Select
1F7 (177) WO	HDCMD	Command Register
1F7 (177) RO	HDSTT	Status Register
3F2 (372) WO	FDDOR	Floppy Digital Operations Register
3F4 (374) RO	FDMSR	Floppy Main Status Reg (WD37C65)
3F5 (375) RW	FDDTR	Floppy Data Registers (WD37C65)
3F6 (376) WO	HDFDR	Fixed Disk (Control) Register
3F6 (376) RO	HDASR	Alternate Status Register
3F7 (377) WO	FDFCR	Floppy Control Register
3F7 (377) RO	HDDIR	Digital Input Register

FIGURE 5-1
REGISTER ADDRESS MAP

2.2 COMMAND DESCRIPTION

The task file command register (HDCMD) accepts the commands and command attributes as shown in Figure 5-3. Commands will not be accepted when the WFDC is 'busy' and will terminate without execution if the drive ready signals is false, if a write fault condition exists at the drive or the command is undefined.

COMMAND	7	6	5	4	3	2	1	0
RESTORE	0	0	0	1	X	X	X	X
SEEK	0	1	1	1	X	X	X	X
RD SECTOR	0	0	1	0	0	0	LNG	RTY
WRT SECTOR	0	0	1	1	0	0	LNG	RTY
FMAT TRACK	0	1	0	1	0	0	0	0
RD VERIFY	0	1	0	0	0	0	0	RTY
DIAGNOSE	1	0	0	1	0	0	0	0
SET PARAM	1	0	0	1	0	0	0	1
INIT ESDI	1	1	1	0	0	0	0	0
WT STACK	1	1	1	0	1	0	0	0
RD STACK	1	1	1	0	0	1	0	0
READ PARAM	1	1	1	0	1	1	0	0
CACHE CNTL	1	1	1	0	1	1	1	1

FIGURE 5-3
WD50C12 COMMAND SUMMARY

Where: X = Drive stepping rate .Unused in ESDI drive
LNG = 0 = Normal mode, normal ECC functions are performed .
= 1 = Long mode, the WD50C12 is inhibited from generating or checking the ECC bytes. The WD50C12 will append the additional bytes supplied by the drive (read) or host processor (write) to the normal data field

RTY = 0 = Error retries and ECC correction are enabled
= 1 = Retries and ECC correction are disabled.

This reflects the [illegible] support 34 to 36 SPT for 512 bytes per track. In order to utilize the maximum storage capacity of the ESDI drives, the WD1007A-WA2 controller translates a Physical track into 2 Logical tracks.

The WD1007A-WAH2 utilizes the Physical track in the following manner:

0	sectors 1 - 17	sectors 18 - 34	35

Sector 0 and 35 are optional alternate sectors which are not accessed by DOS. Sectors 1 - 17 represent a logical track, i.e. logical head 0, and sectors 18 - 34 represent another logical track, i.e logical head

1. PHYSICAL PARAMETERS

   1024 Cylinders

   8 Heads
   34 SpT

   LOGICAL PARAMETERS

   1024 Cylinders

   16 Heads
   17 SpT

It is important to note that low-level formats must be accomplished with PHYSICAL parameters, 34-35 SpT. If a format for 17 SpT is attempted, only the data fields will be initialized.

The WD1007A-WA2 also supports support high capacity ESDI drives, which have more than 1024 cylinders,15 heads, and at least 35 physical sectors per track (34 user, 1 spare).

For this type of drives, the following algorithm for disk address translation is used:

$$x = 63 * (LH \bmod 8) + LS - 1$$

$$PS = x \bmod 34 + 1$$
$$PH = x \operatorname{div} 34$$
$$PC = LC * 2 + (LH \operatorname{div} 8)$$

where:

PX is Physical (sector, head, cylinder)
LX is Logical (sector, head, cylinder)

This algorithm is based on the fact that a physical cylinder contains 510 (34 * 15) physical user sectors. Using half the number of physical cylinders as the logical cylinder gives a sector count of 1020 per logical cylinder. Dividing by 16 logical heads yields 63.75 sectors per track.

In the translate mode, the spare sector(s) will not be accessible by the host and will require the firmware to check the requested cylinder, head, and sector values before doing the translation.

The translated mode is invoked by issuing a Set Parameters command (91hex) at 17 or 34, which is performed by the DOS Bios

at "boot" time. This option may be disabled if jumper W14 is installed. W8 if jumped, and W14 opened will select WD1005-WAH compatible mode, which employs only the double translation (1 Physical Track = 2 Logical Track). Other operating systems may like to utilize the ESDI drives in a pure Physical manner.

5.2.3 RETRY ALGORITHM

5.2.3.1 DATA OPERATIONS:

The ESDI drive allows both track and data strobe offsets to facilitate disk operations in the event of read errors due to slight head mispositions. This may eliminate the need to invoke data error correction.

The algorithm for data error correction employed by Western Digital is to reread up to 8 times and archieve 2 matching sets of syndromes before any correction attempt.

Combining the two methods yields the following algorithm wich is currently implemented:

Below is a table showing the maximum number of READ retries performed for IDnf errors:

	F/W	x	50C12	=	TOTAL
initially, no offsets ---------->	8	x	2	=	16
track offsets + 1, data strobe offset 0 -->	8	x	2	=	16
track offsets - 1, data strobe offset 0 -->	8	x	2	=	16
track offsets 0, data strobe offset +1 ->	8	x	2	=	16
track offsets 0, data strobe offset -1 ->	8	x	2	=	16
reccal, reseek, no offsets ---------->	1	x	2	=	2
total IDnf retries ---------->					82

Below is a table showing the maximum number of Read retries performed for ECC errors:

	F/W	x	50C12	=	TOTAL
initially, no offsets ---------->	8	x	1	=	8
track offsets +1, data strobe offset 0 --->	8	x	1	=	8
track offsets -1, data strobe offset 0 --->	8	x	1	=	8
track offsets 0, data strobe offset +1 --->	8	x	1	=	8
track offsets 0, data strobe offset -1 --->	8	x	1	=	8
reference read to obtain syndromes ------->	1	x	1	=	1
re-read to obtain matching syndromes ----->	8	x	1	=	8
total ECC retries ---------->					49

Below is a table showing the maximum number of WRITE retries performed by different revision levels for IDnf errors:

	REV. 0 F/W	x	50C12	=	TOTAL
initially, no offsets ---------->	1	x	20	=	20
recal, reseek, no offsets ---------->	1	x	20	=	20
total IDnf retries ----->					40

Note:
If any read, at any time, has no ECC error, then the data is assumed to be correct and the operation will continue normally.

5.2.3.2 COMMAND TRANSFERS TO FILE:

Errors in the transfer of data to and from the file during ESDI command operations are reported as aborted command errors after retries are attempted. The ESDI Informational Bulletin - Recommended ESDI Interface Initilization and Error Recording Procedures is supported.

5.3 WD37C65 FLOPPY DISK CONTROLLER

5.3.1 WD37C65 STATUS/DATA REGISTERS

Figure 5-5 summarizes the WD37C65 main status and data read/write registers and bit assignments with respect to the system lower byte data bus. The main status register (FDMSR) contains the controller primary status and may be accessed at any time. It is used to indicate drive busy status and to facilitate host/controller data transfers. The data register (FDDTR) is actually a register stack that is written during the WD37C65 command phase and read during the result phase. The register definitions may differ slightly due to the WD1007A-WA2 design requirements (for example, the module supports only two floppy drives where the WD37C65 can support four drives). Where differences exist, the descriptions in this document should take precedence.

REGISTER	7	6	5	4	3	2	1	0
FDMSR	RQM	DIO	EXM	CB	0	0	D1B	D0B
FDDTR	READ/ WRITE DATA							

FIGURE 5-5
WD37C65 STATUS AND DATA REGISTERS

where:
RQM = Transfer Request To/From Host
DIO = Transfer Direction, '1' is from WD37C65 to Host
EXM = Not DMA Transfer Mode during command execution phase
CB = Read or Write Command in Progress (Busy)
D1B = Drive B in Seek Mode (Busy)
D0B = Drive A in Seek Mode (Busy)

5.3.2 DATA READ/WRITE REGISTER STACK

Figures 5-6 and 5-7 illustrate each of the command phase write and result phase read stack registers. The register stacks are shown for reference only as not all registers or their contents apply to all commands. The registers are assigned a mnemonic for reference in other sections and have their bit positions shown in accordance with the WD1007A-WA2 requirements.

The stack is accessed at the FDDTR register address 3F5 (375) and all registers associated with a given command must be input/output. A more complete description is provided in the referenced WD37C65 documentation.

WD37C65 REGISTER MNEMONIC	BIT ASSIGNMENT							
	7	6	5	4	3	2	1	0
CMD	MT	MF	SK	CMD CODE				
SEL	0	0	0	0	0	HS	0	US0
C	0	CYLINDER NUMBER						
H	0	0	0	0	0	0	0	HA
R	0	0	0	0	SECTOR NUMBER			
N	0	0	0	0	0	0	1	0
EOT	0	0	0	0	TRACK FINAL SECTOR #			
GPL	FORMAT GAP LENGTH							
DTL	1	1	1	1	1	1	1	1
SC	0	0	0	0	SECTORS PER CYLINDER			
D	(FORMAT) DATA FILLER BYTE							
STP	0	0	0	0	0	0	STP	STP
SHT	STEP RATE TIME (SRT)				HEAD UNLOAD TIME (HUT)			
HLD	HEAD LOAD TIME (HLT)							ND
NCN	0	NEW CYLINDER NUMBER						

FIGURE 5-6
WD37C65 WRITE STACK REGISTER SUMMARY

where:

MT = Multi-track Mode
MF = MFM Data Mode
SK = Skip Deleted Address Mark
US0 = Unit (Drive) Select B
HS = Head Select 1
HA = Head Address 1
STP = 1 = Scan Compare Contiguous Sectors
= 2 = Scan Compare Alternate Sectors
ND = Non-DMA Transfer Mode

The MT, MF and SK command bits are not used for all commands and are set to zero when not defined. The drive is selected by the WD37C65 digital operations register (FDDOR) and the unit select bit (US0) is shown for reference only. The head is selected by the state of the HD bit and the head address bit (HA) is used for sector identification only.

WD37C65 REGISTER MNEMONIC	BIT POSITION							
	7	6	5	4	3	2	1	0
ST0	IC		SE	EC	NR	HS	0	US0
ST1	EN	0	DE	OR	0	ND	NW	MA
ST2	0	CM	DD	WC	SH	SN	BC	MD
ST3	FT(0)	WP	RY(1)	T0	WP	HS	US1	US0
C	0	CYLINDER NUMBER						
H	0	0	0	0	0	0	0	HA
R	0	0	0	0	SECTOR NUMBER			
N	0	0	0	0	0	0	BYTES	
PCN	0	PRESENT CYLINDER NUMBER						

FIGURE 5-7
WD37C65 STACK READ REGISTER SUMMARY

where:

IC = Interrupt Code = 0 = Normal Command Termination
= 1 = Abnormal (Error) Command Termination
= 2 = Invalid Command
= 3 = Abnormal (Drive Ready Change) Termination

SE = Seek End
EC = Equipment Check
NR = Drive Not Ready
HS = Current Head Adr
US0 = Unit Select B
EN = End of Cylinder
DE = Data Error
OR = Overrun Error
ND = No Data Transferred
NW = No Write
MA = Missing Addr Mark
CM = Control Mark Found
DD = Data Field Error
WC = Wrong Cylinder
SH = Scan Equal Hit
SN = Scan Not Hit
BC = Bad Cylinder
MD = Missing Data Mark
FT = Drive Fault
WP = Drive Wrt Protect
RY = Drive Ready
T0 = Track 0 Flag
TS = Drive Two Sided
HD = Drive Head Address

US1/0 = Drive Select Code = 0 Drive A, = 1 = Drive B

It should be noted that Status Register 3 (ST3) contains the status of the selected drive while status registers 0, 1 and 2 contain information on the controller status and command execution. Registers C, H, R and N contain sector identification information following command execution. Register PCN indicates the current cylinder number (head position) following the 'sense interrupt status' command.

5.3.3 FLOPPY DISK COMMAND SUMMARY

The floppy disk section commands are listed below along with their respective command codes, command phase (write) register stack and result phase (read) register stack. More detailed descriptions of each command may be found in the referenced WD37C65 literature.

READ DATA (MT,MF,SK,00110)
(CMD,SEL,C,H,R,N,EOT,GPL,DTL)
(ST0,ST1,ST2,C,H,R,N)

The host outputs the nine command phase bytes and the FDC selects the drive, loads the drive heads (if previously unloaded) and begins reading ID address marks and ID data fields to locate the selected sector. When the sector is found data is transferred (via DMA) to host memory. Multi-sector and multi-track operations are allowed. Completion of the command updates the result phase registers, interrupts the system processor (if interrupt enabled) and unloads the heads following the head unload interval.

The 'READ DELETED DATA' command (MT,MF,SK,01100) and 'READ A TRACK' command (0,MF,SK,00010) have the same command and result phase register requirements except for the command opcode. The read deleted data transfers sectors which have the deleted data address mark and the read track command transfers all sectors from the index mark through the 'end of track' sector.

READ ID (0,MF,001010)
(CMD,SEL)
(ST0,ST1,ST2,C,H,R,N)

A read identification field command transfers the first correct ID field data to the sector identification result registers and interrupts the host. Sector data is not transferred to system memory. It should be noted that the result register stack is the same as a normal read command but the commmand phase requires only the command and select register information.

WRITE DATA (MT,MF,000101)
(CMD,SEL,C,H,R,N,EOT,GPL,DTL)
(ST0,ST1,ST2,C,H,R,N)

The host outputs the nine command phase bytes and the FDC selects the drive, loads the heads and searches the sector ID fields. When the C, H, R and N sector fields match the command register data the FDC transfers byte data via DMA to the drive. Command completion updates the result registers and interrupts the host processor.

The 'WRITE DELETED DATA' command (MT,MF,001001) is the same as a normal write except that a deleted data address mark is written at the beginning of the data field in place of a normal data address mark.

FORMAT A TRACK (0,MF,001101)
(CMD,SEL,N,SC,GPL,D)
(ST0,ST1,ST2,C,H,R,N)

The selected track is formatted from index through the last track sector with address marks, ID fields, data fields and field gaps for either the standard single or double density format. The ID field data (four bytes) is furnished by the host for each sector. The data field is filled with the data defined in the command stack register D.

SCAN EQUAL (MT,MF,SK,10001)
(CMD,SEL,C,H,R,N,EOT,GPL,STP)
(ST0,ST1,ST2,C,H,R,N)

The selected sector is compared on a byte basis between the drive information and the host data. If the scan condition is satisfied the SH (scan equal hit) bit is set in status register 2.

The 'SCAN LOW OR EQUAL' (MT,MF,SK,11001) and 'SCAN HIGH OR EQUAL' (MT,MF,SK,11101) commands are similar except for the logical compare condition. If the scan condition is not satisfied the SN (scan not hit) bit is set in result register ST2.

RECALIBRATE (00000111)
(CMD,SEL)

The heads of the selected drive are retracted to track position 0. Thetrack 0 position flag is available as a separate signal from the selected drive and in the ST3 status byte.

SEEK (00001111)
(CMD,SEL,NCN)

The selected drive is stepped to the new cylinder position.

SPECIFY (00000011)
(CMD,SHT,HLD)

The specify command sets the head load and unload rates, the drive step rate and the DMA data transfer mode.

SENSE INTERRUPT STATUS (00001000)
(CMD)
(ST0,PCN)

Controller status register 0 and the current cylinder are available in the result registers following this command. The command will clear the floppy section interrupt level.

SENSE DRIVE STATUS (00000100)
(CMD,SEL)
(ST3)

The command returns selected drive status (ST3) during the result phase.

5.4 WD1007 CONTROL AND STATUS REGISTERS

5.4.1 HARD DISK ALTERNATE STATUS REGISTER (HDASR) 3F6/376 (RO)

This register is contained within the AMAC array and provides fixed disk status to the system processor. The register contains a 'real time' section (bits 7, 6, 3 and 1) and a 'register' section set by the control processor at sector transfer time (bits 5, 4, 2 and 0).

7	6	5	4	3	2	1	0
BZY	RDY	WFT	SKC	DRQ	CRD	IDX	ERR

FIGURE 5-8
ALTERNATE STATUS REGISTER

where:
BZY = Controller Busy Flag
RDY = Ready from selected drive
WFT = Write Fault Flag from IC 8753 Prog.
SKC = Seek Complete Flag from IC 8753 Prog.
DRQ = Data Transfer Request Flag
CRD = Corrected Data Flag from IC 8753 Prog.
IDX = Index Pulse from selected drive
ERR = Error Flag from IC 8753 Prog.

This register reflects the same status as the WD50C12 status register except for bit position 1 where the drive index signal replaces the command in progress (CIP) flag. It should be remembered that the index bit is not latched and thus follows the drive control signal (approximately a 200 microsecond pulse every 16.7 milliseconds). For multi-sector read operations the reported sector number (flagged by the corrected data status bit) will be the 'error sector plus one'. All other error conditions will report the 'error sector'.

The Write Fault bit is also set for all the ESDI error conditions (refer to bit 1 - 7 of table 7-6 of ESDI document ver.1.3). The host processor can detect the exact drive's error by issuing the Initiate ESDI command to read the drive's status.

The register may be interrogated by the host processor at any time without interference with other control functions. The fixed disk interrupt will not be cleared by a host status input at this address.

5.4.2 HARD DISK DIAGNOSTIC INPUT REGISTER (HDDIR) 3F7/377 (RO)

The fixed disk diagnostic input register reflects the current state of the floppy diskette change flag and the fixed disk drive select, head select and drive write gate signals (complimented form). When the floppy disk option is not installed bit 7 remains tri-stated.

7	6	5	4	3	2	1	0
DCG	WTG-	HS3-	HS2-	HS1-	HS0-	DS2-	DS1-

FIGURE 5-9
WFDC DIAGNOSTIC INPUT REGISTER

where: DCG = Diskette Change flag
WTG- = Write Gate on
HS3-/0- = Drive Head Select (binary)
DS2-/1- = Drive Select

Note that the Head Select signals are generated by the IC 8753 Prog. microcontroller and not transparent as in previous WD WDCs. The IC 8753 Prog. needs to be waked-up to update the head select signals before the HDASR can be read correctly.

5.4.3 HARD DISK AUXILIARY CONTROL REGISTER (HDFDR) 3F6/376 (WO)

The Hard Disk Auxiliary Control Register is contained within the AMAC and is used to allow programable controller reset and to provide enable and disable control of the fixed disk priority interrupt.

7	6	5	4	3	2	1	0
0	0	0	0	0	RST	IDS	0

FIGURE 5-10
AUXILIARY CONTROL REGISTER

where: RST = Program controlled (master) reset
IDS = Data Transfer Interrupt Disable

NOTE: The software controlled reset bit (RST) will maintain the fixed disk section logic reset as long as the bit is on. The bit must be turned on (for a minimum of 10.0 microseconds), then off, to complete the reset function.

Additionally, it should be noted that the interrupt disable control bit does not clear the interrupt level in the disabled state. A pending interrupt will occur when the interrupt is again enabled. The interrupt is disabled following a system master reset.

5.5 FIXED DISK DATA REGISTERS

The controller reserves system I/O address 1F0/170(H) for fixed disk programmed I/O data transfers and all system bus data transactions between the controller and the system processor at this address use the 16-bit word transfer bus mode. The controller (and AMAC array) provide read and write data 'pipeline' registers to allow the sector data memory to function as a dual port memory to support the 1:1 interleave format and multi-sector operations. For write operations (system to controller data transfers) the most significant byte (SD15/08) is written directly to a 8-bit storage register, while the

LSB (SD07/00) is written to the AMAC 'post-write' pipeline register. The AMAC logic then writes both registered bytes to RAM in the interval between I/O cycles.

For read data transactions, the AMAC logic 'prefetches' the first data bytes to an internal AMAC register and external upper byte register. The first host input transfers data from these registers and initiates a prefetch of the next two bytes. Subsequent host read operations transfer the MSB from the controller register, the LSB from the AMAC register and automatically prefetch the next two bytes. The use of the pipeline registers permits memory access sharing between the host and the WD50C12. When the 'long' read or write mode is used the additional bytes must be transferred to or from the sector buffer using the system processor byte I/O mode. Refer to Figures 5-11 and 5-12 for a diagram of the read/write data transfer path and fixed disk data format.

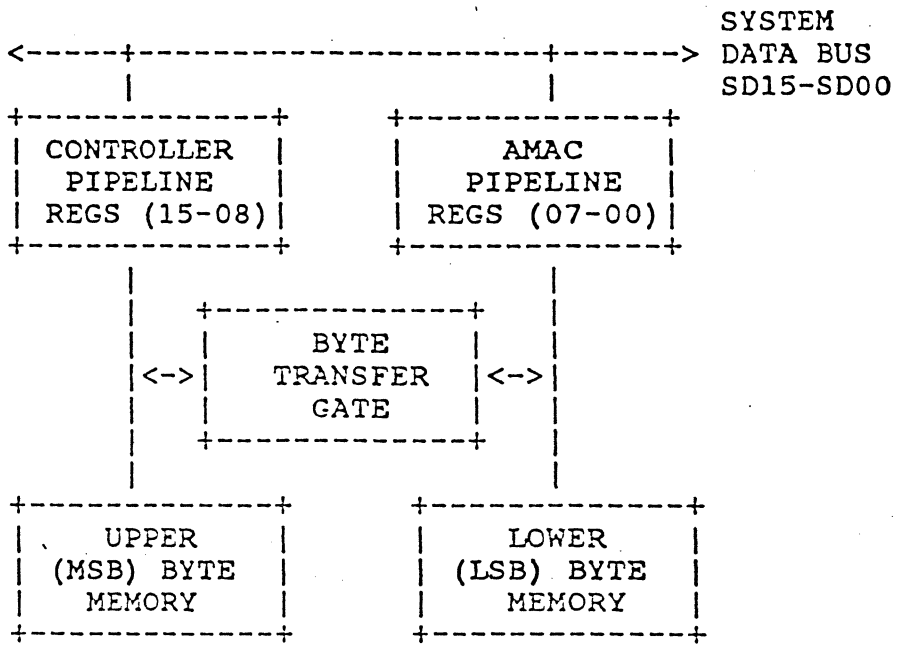


FIGURE 5-11
R/W DATA TRANSFER PATH

ID FIELDS	WORD 000 LSB	WORD 000 MSB		WORD 255 LSB	WORD 255 MSB	CHECK FIELDS

FIGURE 5-12
FIXED DISK (WORD) DATA FORMAT

1007A-WAH JUMPER CONFIGURATION TABLES

WD1005 MODE	W8
	JUMPED

	W10
DIGITAL INPUT REG. LATCHED (COMPAQ MODE)	JUMPED
NON LATCH	NON JUMPED

PRIMARY/SECONDARY HARD DISK ADDRESSES	W12
1FX	NON JUMPED
17X	JUMPED

SECTOR'S TRANSLATION DISABLE	W14
	JUMPED

CACHE DISABLE (FUTURE OPTION)	W15
	JUMPED

5.6 FLOPPY AUXILIARY CONTROL REGISTERS

5.6.1 OPERATIONS REGISTER (FDDOR) 3F2/372 (WO)

The operations register is used to select the floppy drive, provide drive motor control, enable/disable the floppy interrupt and DMA functions and to provide a WD37C65 software reset command - see Figure 5-13.

7	6	5	4	3	2	1	0
RSV	RSV	MBE	MAE	IDE	RST	RSV	DSB

FIGURE 5-13
FLOPPY CONTROL REGISTER

where:
RSV = Reserved
MBE = Drive B Motor Enable
MAE = Drive A Motor Enable
IDE = Interrupt and DMA Enable
RST = Floppy Section Reset
DSB = Drive B Select

The floppy control section is held reset when the reset control bit is off (default state following a system reset) and the bit must be set under system software control to enable floppy operation. Similarly, the floppy section interrupt and DMA enable control bit disables interrupt and DMA requests in the reset state and the bit must be set to enable floppy section operation.

5.6.2 FLOPPY CONTROL REGISTER (FDFCR) 3F7/377 (WO)

The floppy control register is used to select one (of four standard) read/write data rates as shown in Figure 5-14. The 250 Kbps rate is the default state following any reset. See referenced WD37C65 documentation for all possible standard and non-standard rates.

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FR1	FR0

FIGURE 5-14
FLOPPY DATA RATE REGISTER

where:
FR1/FR0 = 00 = 500 Kbps (MFM)
= 01 = 300 Kbps (MFM)
= 10 = 250 Kbps (MFM)
= 11 = 125 Kbps (FM)

5.7 SYSTEM INTERRUPTS

The WFDC requests fixed disk read/write data transfers via a system interrupt (IRQ14). The interrupt level is set by the IC 8753 Prog. and will interrupt the system processor when the level is enabled (bit IDS in auxiliary control register HDFDR reset) and the WFDC is not busy; i.e., read data is ready for transfer, write data is required or a non-data type command is complete. The interrupt level clears on any command or normal status read from the system processor, programmed reset or master reset.

The floppy disk section uses interrupt priority level 6 (IRQ6) for the command and result phase data transfers, the execution phase data transfers for the programmed I/O mode and for command completion. The level clears on a system or software reset, the associated data transfer or via a 'sense interrupt status' command.

5.8 IC 8753 Prog. COMMANDS

The IC 8753 Prog. communicates with the AMAC support logic via a set of R/W commands at preset addresses. The commands are used internal to the controller only and are not available to the system processor. A description of each command is given in the AMAC specification.

ADDRESS	R/W	COMMAND
20	R/W	Host memory address block counter
21	R/W	WDC memory address block counter
22	W	Clear host memory address counter
22	R	Set sleep mode (clear busy)
23	W	Clear WDC memory address counter
23	R	Set 7 byte ECC mode
24	W	Set data request latch
24	R	Set interrupt
25	W	Set read mode
25	R	Set memory prefetch
26	W	Set multiple sector mode
26	R	Clear multiple sector mode
27	W	Set sector block counter
27	R	Set idle mode

FIGURE 5-15
CP SUPPORT COMMANDS

Addresses 00-07(H) and 10-17(H) are reserved for CP communication with the AMAC and WD5010 task file registers respectively. Address range 30-3F(H) is reserved for special IDE and command control.

NOTE: The two high order address bits are not used in the AMAC address decode of the IC 8753 Prog. support commands. For example, the 'Set Multiple Mode' write command (26 hex) may appear in some of the referenced documentation as with the high order bits on (E6 hex).

6.0 LOGIC DESCRIPTION

This section is intended to augment the descriptions of Sections 4 and 5 with a more detailed description of the WFDC logic with reference to the WD1007A-WA2 schematic diagrams. It is assumed the reader is familiar with standard TTL components and conventional logic symbols. Further, it is necessary for the reader to be familiar with the referenced VLSI components (WD50C12, IC 8753 Prog., WD37C65, and AMAC).

6.1 SIGNAL CHARACTERISTICS

6.1.1 Logical Notation

Positive logic notation is used throughout and all signals which are active in the low state have the negation symbol (SIGNAL-) and are identified with the low state drawing identifier bubble; for example:

FUNCTION	DEFINITION		
	ELECTRICAL	LOGICAL	STATE
SIGNAL	H	1 TRUE	ACTIVE, ASSERTED
	L	0 FALSE	
SIGNAL-	L	1 TRUE	ACTIVE, ASSERTED
	H	0 FALSE	

NOTE: The system bus signals which are active in the low state are shown
with the negation symbol preceding the term (-SIGNAL). The WFDC logic diagrams follows this convention for system bus signals only.

6.1.2 Electrical Description

Signals that have the negation symbol have a logical/electrical relation that is:

LOGICAL STATE	ELECTRICAL STATE	RECEIVER	DRIVER
0	H = TTL HI STATE	5.25v>H>2.00v	5.25v>H>2.40v
1	L = TTL LO STATE	0.80v>L>0.50v	0.50v>L>0.00v

and signals that do not have the negation symbol have a

logical/electrical relation that is:

LOGICAL STATE	ELECTRICAL STATE	RECEIVER	DRIVER
0	L = TTL LO STATE	0.80v>L>0.00v	0.50v>L>0.00v
1	H = TTL HI STATE	5.25v>H>2.00v	5.25v>H>2.40v

6.2 WD50C12 WINCHESTER DISK CONTROLLER

The WD50C12 Winchester disk controller device is shown on sheet 4. A complete description of the device and it's I/O signals is contained in the referenced documentation. It is important to note that the device data bus (WD7-0), register file address, chip select and read/write strobes connect directly to the AMAC where all bus switching, address selection, etc. is controlled.

The WD50C12 accesses sector data memory via bus control and accessarbitration logic in the AMAC device.

6.3 IC 8753 Prog. BUFFER MANAGER CONTROL PROCESSOR

Primary control is provided by the IC 8753 Prog. control processor . The IC 8753 Prog. can access registers in both the WD50C12 and the AMAC array and functions primarily to aid in the execution of host generated commands, in management of the sector data buffer addressing and in error recovery procedures. The control processor also performs several module self-tests following a 'diagnose' command, master reset or programmed reset (refer to Section 8.0).

The processor input port (port 3) allows firmware interrupts from the WD50C12 operation completion signal (INTRQ-) and buffer request signal (BDRQ-), the drive attention signal (ATTN-) and command completed signal (CMDCPLT), and by the AMAC generated 'wakeup'signal (WAUPL-). The (port 2) is used to receive the drive hand-shake signal (TXAK), the configuration status data (CSD) and the drive selected signals (D0SLTD/D1SLTD); port 2 also drives the activity indicator, selects between WD1005/WD1007 mode, and Translated/Non Translated Mode. Port 1 of the processor is used to select the drive read/write head (HSEL3-0), to request the serial communication with the drive (TXREQ) and send the command data to the drive (CMDDAT), to communicate with the WD50C12 (BRDY and WF). Port 1 also allows CP control of the WD50C12 reset input.

All processor program code and program-related data is stored in internal IC 8753 Prog. ROM and RAM. The module RAM sector data buffer is restricted to disk read/write data and the WD50C12 ECC correction process; i.e., it is not used to store IC 8753 Prog. program variables. The firmware descriptions and listings are contained in separate IC 8753 Prog. and firmware 'protocol' specifications.

6.5 BUFFER MANAGER GATE ARRAY

The WD12C00-22 (AMAC) gate array logic is shown as a single logic

block on sheet 3. The primary function of the AMAC logic is to provide host address and command decoding, task file control and status image registers, data transfer pipeline registers, bus controls and sector data RAM address control (see Figure 6-1).

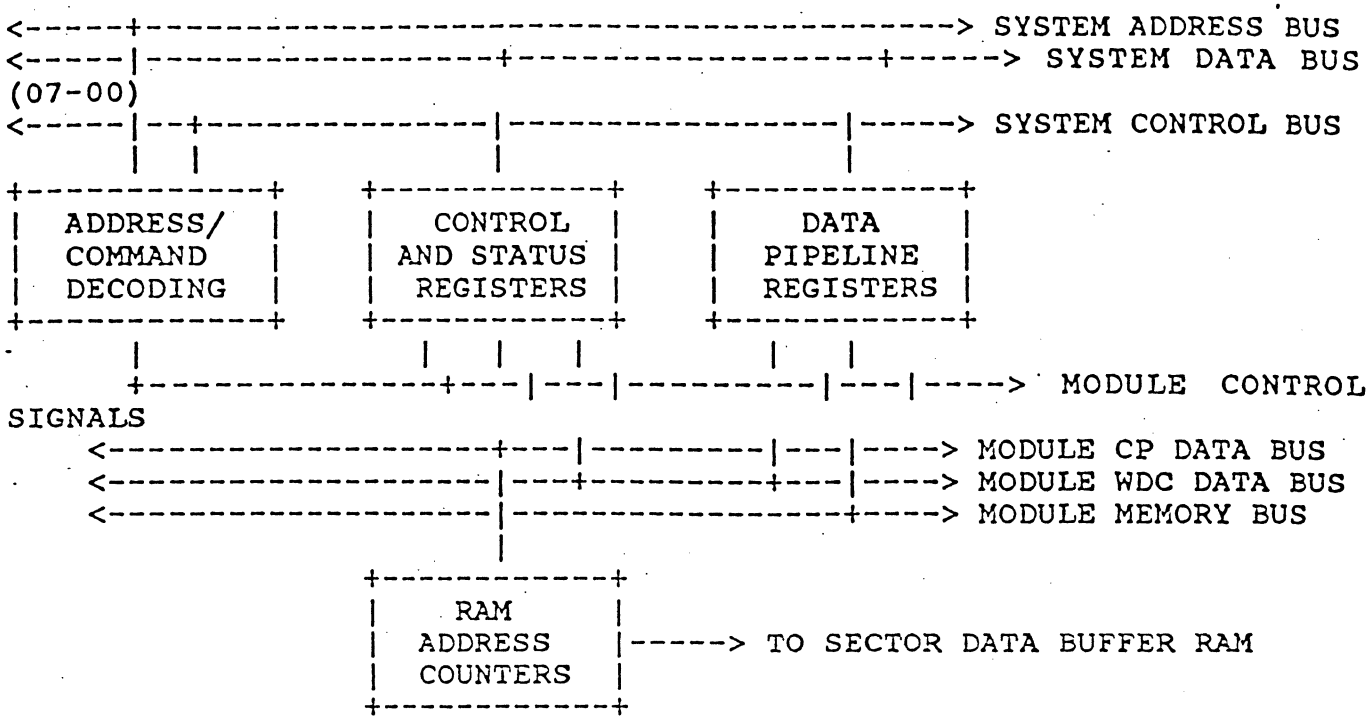


FIGURE 6-1
AMAC BLOCK DIAGRAM

6.5.2 ADDRESS DECODE

The AMAC device address and command decoding range is externally selected by the decode PAL and jumper select shown on the left portion of sheet 3.
The decoding logic controls the host task file and auxiliary registeraddress ranges (1F0-7/170-7 and 3F6-7/376-7). Individual register decoding is provided internal to the AMAC.

6.5.3 TASK FILE REGISTERS

The control and status task file registers within the AMAC are an image of the normal WD50C12 registers. The host has access to the AMAC registers (only) while the control processor can access both the AMAC and WD50C12 register set.

6.5.3 DATA PIPELINE REGISTERS

The lower byte data transfer pipeline registers for both host and WDC input prefetch and output postwrite are included in the AMAC. These registers (and the external host upper byte equivalent) allow the module to perform the concurrent host and WDC data memory accesses necessary for multi-sector 1:1 interleave operation. This necessity requires the AMAC to arbitrate simultaneous host and WDC requests and to gate the appropriate address counter to external memory. See

Figure 6-2 for a simple timing and arbitration illustration.

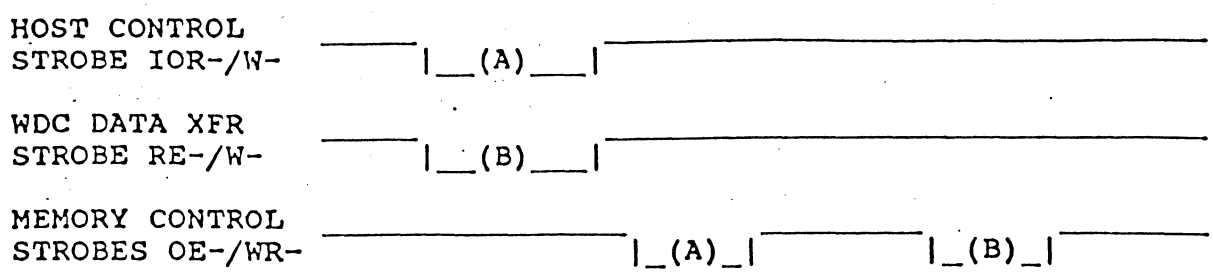


FIGURE 6-2
AMAC TIMING ILLUSTRATION

The timing of the two AMAC generated strobes is controlled by a clocked sequencer that resolves priority (in favor of the host request) and generates the external memory (and byte transfer gate) control signals.

6.5.4 MEMORY ADDRESS COUNTERS

The RAM address counters (host and WDC) are sequential 14-bit counters with the multiplexed high order 13 bits addressing the two 8K controller memories (the low order byte control is provided by internal AMAC logic).

6.5.5 AMAC EQUATIONS

Refer to AMAC Engineering Specification

6.6 SYSTEM BUS INTERFACE

Sheet 3 shows the system bus address, data and control interface signals.
It is particularly important to note that the I/O address lines (SA09-00) and the address control signal (AEN) connect to the address decode PAL for module selection and lines SA9 and SA2-0 connect to the AMAC for individual register addressing. The low order data byte (SD07-00) connects directly to the AMAC and the device provides the necessary bus drive current. Figure 6-3 illustrates the I/O read and write signal relationship. The signal timing specification is included in Section 9.

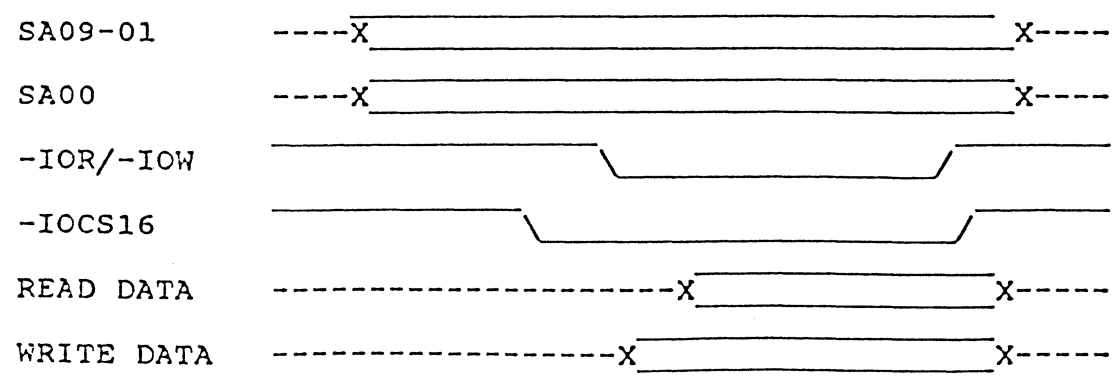


FIGURE 6-3
SYSTEM BUS SIGNALS

6.7 FIXED DISK DRIVE INTERFACE

Sheets 4 and 5 show the data and control interface to the disk drives.

6.7.1 CONTROL INTERFACE

The control input signals (sheet 4) are terminated with standard 150 ohm line terminators and buffered by 74LS14 Schmitt Trigger inverters. The Index, Command complete, Write fault and Drive Ready signals connect to the WD50C12 and AMAC for control and status information.

Sheet 5 also shows the drive select, drive head select and write gate control drivers (type 7438).

6.7.2 R/W DATA INTERFACE

U16 and U14 are the differential data drivers and receivers for each of two drives and connect to separate radial data cables.

6.8 BUFFER MEMORY

The RAM data buffer memory is shown on sheet 3. The RAM address is provided by the multiplexed output of the host and WD50C12 address counters from the AMAC. The RAM chip select inputs (CS1- and CS2) are always enabled with the RAM write and output enable signals generated by the AMAC logic.

6.9 CLOCK OSCILLATOR

The IC 8753 Prog. and AMAC clock inputs are driven by a 9.6MHZ oscillator. The WD50C12 read/write clock input is the multiplex signal of the system clock and the drive read/reference clock input.

6.10 MODULE RESET CIRCUIT

The module power on and low VCC monitor reset control circuitry is shown on sheet 1. Resistor R7 and Zener diode CR1 set the low VCC trip point at approximately 3.6 volts. The AMAC logic includes a clocked delay counter (approximately 12 milliseconds at a 10 MHZ input) to provide an adequate power on reset interval and to insure the module clock is operative.

6.11 LED DRIVER

The LED (activity) indicator driver and connector are shown on Sheet 2. The driver is controlled by the IC 8753 Prog. and indicates controller activity.
A current limiting resistor on the controller limits the indicator current to approximately 20 milliamperes.

6.12 BIOS ROM/RAM OPTION

The BIOS ROM/RAM option components are shown on sheet 7 and include the (P)ROM (type 2732 or 2764), the 2K x 8 Static Ram, the address range control PAL and the system bus data gate. The ROM program

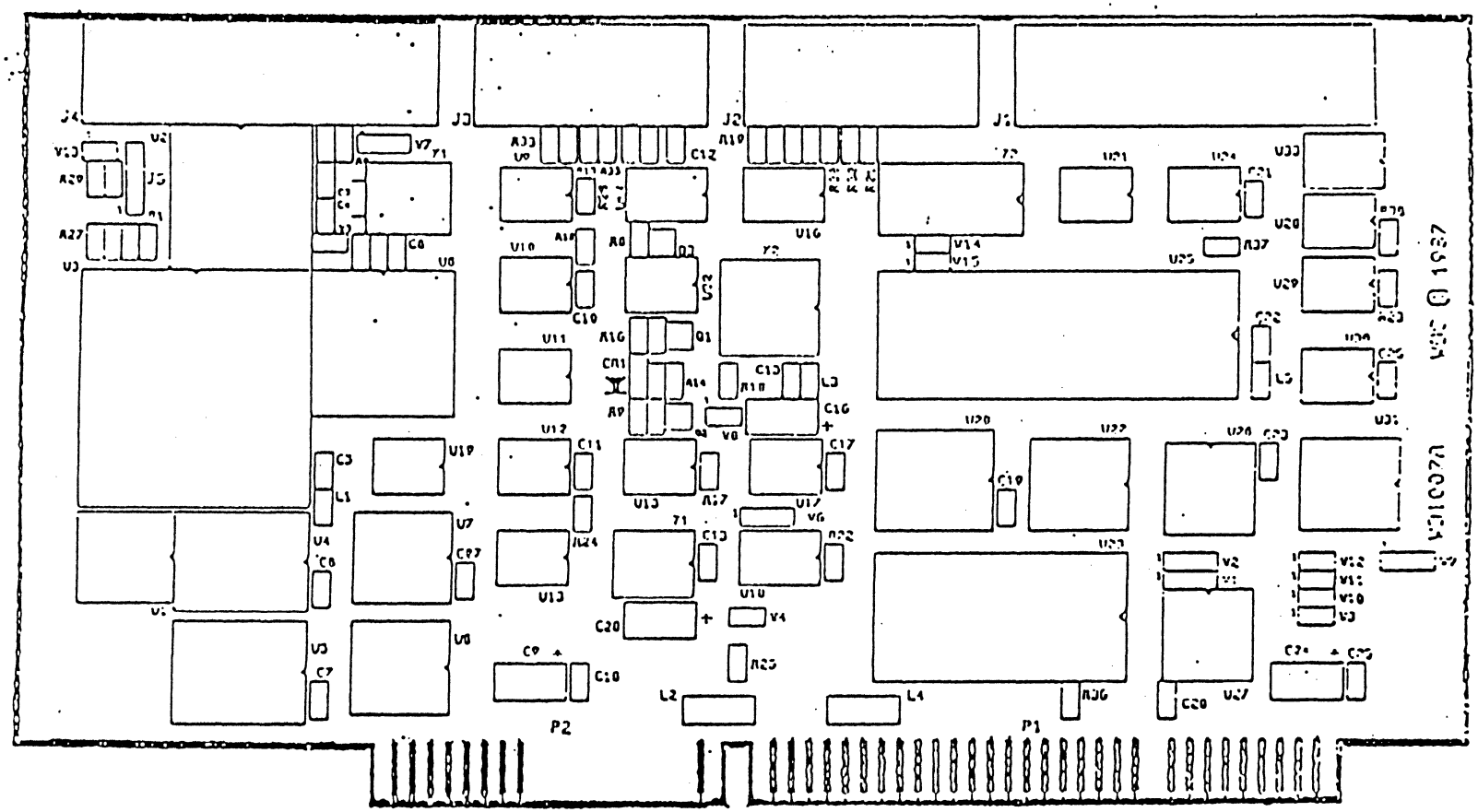


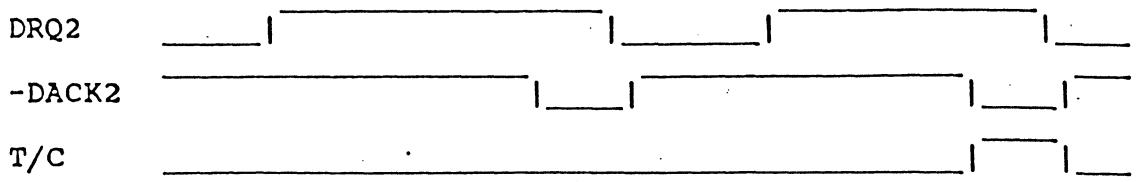
Figure 7.1

Controller Module Layout

information is contained in separate documentation - see referenced PAL specification for PAL equations and address range selection.

6.13 WD37C65 FLOPPY DISK CONTROLLER

Sheet 6 of the schematic diagram shows the WD37C65 controller along with the floppy section address decoder. The operation of the WD37C65 is covered in the referenced literature - refer to Section 5.0 for a summary of the controller commands and a definition of the operations register bits.



6.14 FLOPPY DISK DRIVE INTERFACE

The floppy disk control and data drivers and receivers are contained within the WD37C65 which interfaces directly to the drive interface connector. All output drivers are (7438 equvalent) open-collector drivers.
The input signals are terminated by Z2 (150 ohm termination) and buffered by Schmitt type receivers.

7.0 INSTALLATION

The controller module may be installed in any suitable PC slot that provides both the P1 and P2 connectors.

7.1 MECHANICAL

Figure 7-1 illustrates the general module jumper placement and approximate connector locations. The module dimensions are 13.12 by 4.2 inches and a mounting bracket is included.

7.2 ADDRESS SELECT JUMPERS

The module primary address range (1F0-1F7 and 3F6-3F7) is factory selected by circuit etch at address jumper positions W12. The secondary address range (170-177 and 376-377) is selected by jumping W12.

7.3 MODE SELECT JUMPERS

7.3.1 DIAGNOSTIC REGISTER LATCH CONTROL

Jumper position W10 (installed) enables the diagnostic Digital Input Register to operate in the latched mode; i.e., the register outputs are latched when the register is accessed. The jumper is normally not used.

7.3.3 IC 8753 Prog. MODE CONTROL

Jumpers W8, W14, W15 are used to provide three external mode selects to the control processor. The modes are defined in the IC 8753 Prog.

05 = IC 8753 Prog. ROM checksum error
= IC 8753 Prog. RAM data error

8.3 SYSTEM TESTS

Module software tests designed to operate in the PC-AT system are not covered in this document. These tests would include the WD HDT/ESDIdiagnostic tests or any host test software.

9.0 GENERAL SPECIFICATIONS

9.1 POWER AND ENVIRONMENTAL

9.1.1 Power Requirements

+5 VDC	+/- 5.0% < 1.200 amps

9.1.2 Environmental

Temperature	
Operating	10 to 50 degrees Celsius
Non-operating	-40 to 60 degrees Celsius
Humidity	
Operating	8% to 85% non-condensing
Non-operating	5% to 95% non-condensing
Shock and Vibration	
Shock	35G/20MS square wave maximum
Vibration	1G/0-600Hz, dwell not to exceed 30 seconds at (any) resonance
Altitude	
Operating	0 to 3000 meters maximum
Non-operating	0 to 5000 meters maximum

9.2 FIXED DISK

9.2.1 RECORDING SPECIFICATIONS

Encoding Method	RLL/MFM
Data Rate	10 - 15 MBS
Sector format	512 bytes/sector, 32-36 sectors/track hard sectored format
Drives supported	2 maximum
Heads supported	16 maximum
Tracks supported	18,360 maximum (1224 cylinders)

9.2.3 ERROR CORRECTION SPECIFICATIONS

Method	Polynomial division
Degree	56
Forward polynomial	X^56 + X^52 + X^50 + X^43 + X^41 + X^34 + X^30 + X^26 + X^24 + X^8 +1
Reciprocal polynomial	X^56 + X^48 + X^32 + X^30 + X^26 + X^22 + X^15 + X^13 + X^06 + X^04 + 1
Record length (r)	519 X 8 bits maximum
Correction span (b)	11 bits
Single burst detection span With b = 11	r = 519 X 8 32 bits
Double burst detection span With b = 11	r = 519 X 8 11 bits
Non-detection probability	1.39(E-17), r = 519 X 8, b = 11
Miscorrection probability	5.84(E-11), r = 519 X 8, b = 11

9.3 FLOPPY DISK

9.3.1 FLOPPY DISK RECORDING SPECIFICATIONS

Data Rates (Standard)	500 Kbps (MFM), 250 Kbps (MFM) 125 Kbps (FM)
Data Rates (Non-standard)	300 Kbps (MFM)
WD37C65 Clocking Rate	500 Kbps (16.0 MHz) 250 Kbps (16.0 MHz) 125 Kbps (16.0 MHz) 300 Kbps (9.6 MHz)
Write Precompensation	125 nsec. early/late standard 187 nsec. early/late selectable
Sector Format	512 bytes/sector, 15 sectors/track maximum - soft sectored format
Drives supported	2 maximum
Heads supported	2 maximum
Tracks supported	160 maximum
Hard Error Rate	less than 1 per 10(E12) bits read
Soft Error Rate	less than 1 per 10(E09) bits read
Seek Error Rate	less than 1 per 10(E06) seeks

9.3.2 ERROR DETECTION/CORRECTION SPECIFICATIONS

ID Field CRC	X^16 + X^12 + X^5 + 1
Data Field CRC	X^16 + X^12 + X^5 + 1

9.3.3 FLOPPY DISK DATA SEPARATOR SPECIFICATIONS

Bit Jitter Tolerance	60% (minimum) of window
Capture Range	+/- 6% (minimum)
Reference	WD92C32 DPLL

9.4 DRIVE INTERFACE

All control and data drivers, receivers and signal terminations are per the ESDI interface specification. Drive attachment is restricted to two units. Drives with up to sixteen heads are supported.

9.4.1 FIXED DISK DRIVE CONTROL CONNECTOR

WD Part No. 41-000022-000 (AMP type 1-10xxxx-x), Pin 15 polarization

9.4.2 FIXED DISK DATA CONNECTORS

WD Part No. 41-000023-000 (AMP type 1-10400x-x)

9.4.3 FLOPPY DISK DRIVE CONTROL/DATA CONNECTOR

WD Part No. 41-001127-000 (AMP type 1-10400x-x), Pin 5 polarization

9.4.4 LED Connector

WD Part No. 41-001088-000 (AMP type 104005-3)

9.5 SYSTEM BUS INTERFACE

Programmed I/O is used for all fixed disk control and data transactions.
All data transfers are 16-bits and use the channel 'fast I/O' protocol.
All control transfers are 8-bits wide and use the lower bus data byte. Floppy control and data transfers are all 8-bits wide and use the lower bus data byte only. Floppy disk data execution phase data transfers may use DMA channel 2. The module I/O primary and secondary address range, DMA channel and priority interrupt assignments are fixed.

Bus loading for all WFDC input signals will not exceed 2 standard LSTTL loads in either logic sense. Module output low state sink current (Iol) at Vol = 0.4 volts is 12 ma. on all tri-state outputs and 16 ma. on open collector output -IOCS16.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
	-IOCS16 from SA09-01		79	nsec
	-IOCS16 from SA00		38	nsec
	+IOCS16 from +IOR/+IOW		71	nsec
	SD15-08 from -IOR		35	nsec
	SD07-00 from -IOR, Fixed Disk		70	nsec
	SD07-00 from -IOR, Floppy Disk		90	nsec
	SD15-08 HIZ from +IOR		43	nsec
	SD07-00 HIZ from +IOR, Fixed Disk		75	nsec
	SD07-00 HIZ from +IOR, Floppy Disk		65	nsec
	SD15-08 setup to +IOW	00		nsec
	SD07-00 setup to +IOW, Fixed Disk	20		nsec
	SD07-00 setup to +IOW, Floppy Disk	80		nsec
	+IOW to SD15-08 HIZ (hold time)	20		nsec
	+IOW to SD07-00 HIZ (hold time)	20		nsec
Note 1	-IOR/-IOW pulse width (16 bit I/O)	70		nsec
Note 1	-IOR/-IOW pulse width (8 bit I/O)	70		nsec
Note 2	+IOR/+IOW to -IOR/-IOW (16 bit I/O)	375		nsec
	-DACK2 to -DRQ2	140		nsec
	DRQ2 period	3.2		usec
	TC pulse width	60		nsec

Notes: 1. Does not include host read data setup time
2. 10 MHZ clock input

FIGURE 9-1
SYSTEM BUS TIMING CHARACTERISTICS

APPENDIX

A. SYSTEM BUS CONNECTOR P1

Pins and signals are viewed as looking down at the connector with the module component side to the right.

B01	*GND*	*A01*	
B02	*RESET*	*A02*	*SD07*
B03	*VCC*	*A03*	*SD06*
B04		*A04*	*SD05*
B05		*A05*	*SD04*
B06	*DRQ2*	*A06*	*SD03*
B07		*A07*	*SD02*
B08		*A08*	*SD01*
B09	*+12VDC*	*A09*	*SD00*
B10	*GND*	*A10*	
B11		*A11*	*AEN*
B12	*-SMEMR*	*A12*	*SA19*
B13	*-IOW*	*A13*	*SA18*
B14	*-IOR*	*A14*	*SA17*
B15		*A15*	*SA16*
B16		*A16*	*SA15*
B17		*A17*	*SA14*
B18		*A18*	*SA13*
B19		*A19*	*SA12*
B20		*A20*	*SA11*
B21		*A21*	*SA10*
B22	*IRQ6*	*A22*	*SA09*
B23		*A23*	*SA08*
B24		*A24*	*SA07*
B25		*A25*	*SA06*
B26	*-DACK2*	*A26*	*SA05*
B27	*T/C*	*A27*	*SA04*
B28	*BALE*	*A28*	*SA03*
B29	*VCC*	*A29*	*SA02*
B30		*A30*	*SA01*
B31	*GND*	*A31*	*SA00*

B. SYSTEM BUS CONNECTOR P2

Pins and signals viewed as looking down on the connector with the module
component side to the right

D01		*C01*	
D02	*-I/OCS16*	*C02*	
D03		*C03*	
D04		*C04*	
D05		*C05*	
DO6		*C06*	
D07	*IRQ14*	*C07*	
D08		*C08*	
D09		*C09*	
D10		*C10*	
D11		*C11*	*SD08*
D12		*C12*	*SD09*
D13		*C13*	*SD10*
D14		*C14*	*SD11*
D15		*C15*	*SD12*
D16	*VCC*	*C16*	*SD13*
D17		*C17*	*SD14*
D18	*GND*	*C18*	*SD15*

C. FIXED DISK DRIVE CONTROL CONNECTOR J1

Drive control connector viewed as looking at the connector from module component side. (WD connector type 41-000022-000)

01	*GND*	*02*	*HS3-*
03	*GND*	*04*	*HS2-*
05	*GND*	*06*	*WRG-*
07	*GND*	*08*	*CSD-*
09	*GND*	*10*	*XACK-*
11	*GND*	*12*	*ATN-*
13	*GND*	*14*	*HS0-*
15	*KEY*	*16*	*SCT-*
17	*GND*	*18*	*HS1-*
19	*GND*	*20*	*INDEX-*
21	*GND*	*22*	*DRDY-*
23	*GND*	*24*	*TXREQ-*
25	*GND*	*26*	*DS0-*
27	*GND*	*28*	*DS1-*
29	*GND*	*30*	*RESERVED*
31	*GND*	*32*	*RG-*
33	*GND*	*34*	*CMDDAT-*

D. FIXED DISK DRIVE DATA CONNECTORS J2/J3

The drive data connectors are shown as looking at the connector from the module component side. (WD connector type 41-000023-000)

01 D0/1SLTD-	*02 PULL-UP*
03 D0/1CMCPLT-	*04 AM0/1-*
05 GND	*06 GND*
07 WCLK0/1+	*08 WCLK0/1-*
09 NU	*10 RCLK0/1+*
11 RCLK0/1-	*12 GND*
13 WDATA0/1+	*14 WDATA0/1-*
15 GND	*16 GND*
17 RDATA0/1+	*18 RDATA0/1-*
19 GND	*20 NU*

E. FLOPPY DRIVE CONNECTOR J4

The floppy connector is shown from the component side looking at the connector. (WD connector type 41-001127-000)

01 GND	*02 FWC-*
03 GND	*04*
05 KEY	*06*
07 GND	*08 IDX-*
09 GND	*10 MO1-*
11 GND	*12 FDS2-*
13 GND	*14 FDS1-*
15 GND	*16 MO2-*
17 GND	*18 DIRC-*
19 GND	*20 FSTEP-*
21 GND	*22 FWD-*
23 GND	*24 FWE-*
25 GND	*26 FTR000-*
27 GND	*28 FWP-*
29 GND	*30 RDD-*
31 GND	*32 HS-*
33 GND	*34 DISK_CHANGE-*

F. EXTERNAL INDICATOR CONNECTOR J5

(WD connector type 41-001088-000)

01 LED+	*02 LEDO-*
03 LEDO-	*04 LED+*

E. JUMPER CONFIGURATIONS

WD1007A-WA2 JUMPERS CONFIGURATION TABLES

TABLE I

BIOS ADDRESS RANGES	JUMPER SETTINGS		
	W1	W2	W3
C8000 - C9FFF	2 - 3	2 - 3	JUMPED
CA000 - CBFFF	2 - 3	1 - 2	JUMPED
CC000 - CDFFF	1 - 2	2 - 3	JUMPED
CE000 - CFFFF	1 - 2	1 - 2	JUMPED
DISABLE			NON JUMPED

TABLE II

FLOPPY CONTROLLER	W4	W13 IN ETCH
ENABLE	NON JUMPED	UNCUT
DISABLE	JUMPED	CUT

TABLE III

DRIVE TYPE INPUT	W5
2 SPEEDS SPINDLE MOTOR	JUMPED
SINGLE SPEED	NON JUMPED

TABLE IV

FLOPPY ADDRESS RANGES	W6
37X	1 - 2
3FX	2 - 3

TABLE V

HIGH DENSITY SELECTION	W7
5.25", 1.2M	1 - 2
3.5", 1.44M	2 - 3

TABLE VI

WD1005 MODE	W8	JUMPED
WD1007 MODE		NON JUMPED

TABLE VII

SSIS GROUND & DIGITAL GROUND	W9
CONNECTED	2 - 3
UNCONNECTED	1 - 2

WD1007A-WA2 - DEFAULT SETTING		WD1007A-WAH DEFAULT SETTING	
W1	2 - 3	W1	2 - 3
W2	2 - 3	W2	2 - 3
W3	JUMPED	W3	JUMPED
W4	NON JUMPED		
W5	NON JUMPED		
W6	2 - 3		
W7	1 - 2		
W8	NON JUMPED	W8	NON JUMPED
W9	2 - 3	W9	2 - 3
W10	NON JUMPED	W10	NON JUMPED
W11	JUMPED	W11	NON JUMPED
W12	NON JUMPED	W12	NON JUMPED
W13	UNCUT		
W14	NON JUMPED	W14	NON JUMPED
W15	NON JUMPED	W15	NON JUMPED

TABLE VIII

DIGITAL INPUT REG MODE	W10
LATCHED	JUMPED
NON LATCHED	NON JUMPED

TABLE IX

DISKCHANGE INPUT	W11
WITH FDC OPTION	JUMPED
WITHOUT FDC OPTION	NON JUMPED

TABLE X

PRIMARY/SECONDARY HARD DISK ADDRESSES	W12
1FX	NON JUMPED
17X	JUMPED

TABLE XI

SECTOR TRANSLATION	W14
ENABLE	NON JUMPED
DISABLE	JUMPED

TABLE XII

ECC SELECTION	W15
7 BYTES	JUMPED
4 BYTES	NON JUMPED