MODEL TC-131 TAPE CONTROLLER
HARDWARE MANUAL

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PRELIMINARY

western peripherals

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GENERAL DESCRIPTION

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SECTION I

GENERAL DESCRIPTION

1.1 DESCRIPTION OF EQUIPMENT

1.2 The Western Peripherals Model TC-131 is a magnetic tape controller/formatter which is hardware and software compatible with the DEC PDP-11 family of computer systems, providing both NRZI and phase encoded (PE) format capability in an embedded controller. Only the NRZI format capability is provided with model TC-131N. Mounted in any standard Small Peripheral Controller (SPC) slot in a standard backplane system unit,the controller consists of a single standard hex-wide board and contains a microprocessor plus all interface, control,status, and formatting electronics to emulate the TM-11/TU-10 tape subsystem. The controller installs directly into any available location in the computer or expansion chassis. Three ribbon cables interconnect the controller with the tape drives through cable adapters, which also provide daisy-chaining capabilities for multiple drive installations.

1.3 DRIVE COMPATIBILITY

1.4 The controller will handle up to eight industry-compatible (IBM/ANSI) read-after-write (dual gap) tape drives. The controller is capable of handling tape drives in varying combinations of speeds, densities, and formats. The controller can select either of two switch selectable speeds in the range from 25 to 125 inches per second (ips).

1.5 Single or dual density NRZI and PE tape drives may be used with densities of 800 bits per inch (bpi) NRZI 9-track, and 1600 bpi PE 9-track. Software density control is available for dual density operation. The controller is compatible with all industry-standard tape drives.

1.6 OTHER FEATURES

1.7 The controller is compatible with the Unibus and with existing magnetic tape software, utilizing the standard TU-10/TM-11 magnetic tape controller registers. Enhancements of the standard registers provide other features which add to the usefulness of the controller. Transfers of register information between the tape controller and the computer are made using standard register addresses 772520 through 772532 with 224 as the standard interrupt vector. Alternate addresses and vectors may be used for a second tape system if over eight tape drives are used or if other system requirements are such that a second controller must be used. The address and vector may be changed by moving jumpers. Data transfers are in a 16-bit word or 8-bit byte format via the Unibus.

1.8 Both DEC (normal) and standard IBM (selectable) byte packing modes are available. This bit-selectable IBM packing mode allows reading and writing IBM/industry-compatible tapes. Accomplished without special software, the"automatic read and write on-the-fly" feature allows non-stop operation when doing consecutive read or write operations. The controller writes and recognizes IBM/ANSI - compatible end-of-file tape marks. The controller provides an "EDIT" feature which allows a record anywhere on a previously

recorded tape to be replaced with an updated record.(widow)

1.9 65 bytes of data buffering provide flexibility in assigning priorities when programming data transfers to the computer. The tape motion control, Cyclic Redundancy Check character (CRC) and the Longitudinal Redundancy Check character (LRC) generation and checking, inter-record gap generation and status reporting are included. No screwdriver adjustments are required or provided. While the controller can read or write only in the forward direction, it can space (or move to a new position) in both directions.

1.10 The controller may address up to eight drives but can only read, write or space one drive at a time, except for the Rewind Command. This function requires only initiation by the controller. That transport can then be left to rewind while the controller services another drive.

1.11 Programmed instructions are used to specify the starting address in computer memory, the number of bytes to transfer, the drive number, and the function to be performed. Programmed instructions are also used to transfer status, address, byte count and other information from the tape controller to the computer. Data transfers during read and write operations are accomplished by the controller, which becomes "bus master" to accomplish these transfers.

1.12 SPECIFICATIONS

1.13 The following information summarizes the specifications of the tape controller.

1. Computer Interface
   a. Compatibility - The controller is fully hardware and software compatible with the DEC PDP-11 computer system family and all other systems emulating the Unibus.
   b. Emulation - The controller emulates the standard TM-11/TU-10 tape subsystem.
   c. The controller interfaces directly with the Unibus through any standard SPC board slot.
   d. Bus Loading - One bus load.
   e. Tape Commands*:
      Off line
      Read
      Write
      Write EOF
      Space Forward
      Space Reverse
      Write with Extended Record Gap
      Rewind
   f. Other Mode Controls:
      Density Selection *
      Byte Mode Selection *
      Controller Clear
      Unit Selection *

Interrupt Enable *

Command Execution (GO) *

Edit Mode *

Byte Count *

Memory Address *

For Diagnostics:

Check Character Read Selection *

Bad Tape Error Simulation *

g. Controller Status:

Status of the above-mentioned commands marked with an asterisk (*) may be checked in addition to the following:

Illegal Command

End of File

Parity/Format Error

Bus Grant Late

End of Tape

Record Length Excessive (Read Mode)

Bad Tape Error

Non-Existent Memory

Drive On-Line

Beginning of Tape

Write-Protected

Drive Rewinding

Drive Ready

Error Summary

Controller Ready

Correctable Parity Error (Read)

PE Identification

For Diagnostics:

Tape Stopping After Rewind

10 KHz Clock

Gap Shutdown

Read/LRC Bits

CRC/LRC Character

h. Register Addresses: 772520 thru 772532 (standard for TM-11). Alternate addresses are jumper selectable.

i. Interrupt Vector: 224 (standard for TM-11). Alternate vectors are jumper selectable.

2. Format Compatibility

Fully compatible with the industry-standard IBM/ANSI digital tape recording format as described in ANSI specifications X3.22-1973 and X3.39-1973. Both DEC (normal) and standard IBM (selectable) byte packing modes are available.

3. Drive Compatibility

a. Designed to be compatible with the industry standard drives

b. Read-after-Write only (dual gap head)

c. Single or dual density (operator or software switchable)

4. Tape Speed

   25 ips, 37.5 ips, 45 ips, 75 ips, 125 ips

5. Format and Density

   a. NRZI 9-Track - 800 BPI

   b. PE 9-Track - 1600 BPI

6. Data Transfers

   a. 9-Track (1) DEC - compatible byte packing mode, (least significant byte first) - standard operating mode

      (2) IBM - compatible byte packing mode (most significant byte first).

   b. Bus transfers consist of 16-bit word transfers with 8-bit byte transfers for odd bytes at the beginning and/or end of the transfer.

7. Drive Configuration

   a. Up to eight drives in daisy chain configuration

   b. One or two tape drive speeds.

   c. Single or dual densities on the daisy-chain.

8. Hardware

   a. One hex-wide printed circuit board mounted within the computer chassis (or expansion cabinet), containing a 2900 microprocessor and other advanced technology microcircuits.

   b. Three interface cables and adapter boards per tape drive

9. Other Features

   a. Edit mode for correcting pre-recorded tapes

   b. Crystal controlled clocks

   c. Phase-locked loop read tracking in the PE mode

   d. No screwdriver adjustments

10. Error Handling

   a. Generates and checks vertical parity, CRC,LRC preambles and postambles

   b. Detects dead track errors

   c. Corrects PE single channel dropouts

11. Data Buffering

The internal buffer between the CPU and the tape drive provides 65 bytes of buffering to allow for transfers between the controller and the tape drive during the time when the computer bus is unable to service the controller. All data contained in the buffer will automatically be transferred before the operation is aborted. During read operations, the buffer allows a check of false preambles in 9-track PE mode when a single dead track occurs. During read operations, the buffer must be emptied within the maximum times specified below, otherwise a data late error condition is reported.

Maximum Time After End of Record

Tape Speed	9-Track NRZI	9-Track PE
25.0 ips	1.50 ms	2.05 ms
37.5 ips	1.00 ms	1.37 ms
45.0 ips	0.83 ms	1.14 ms
75.0 ips	0.50 ms	0.68 ms
125.0 ips	0.30 ms	0.41 ms

12. Non-Stop "On-the-Fly" Tape Operation

This feature provides continuous tape motion when consecutive tape commands require tape motion in the same direction on the same tape drive. Under these conditions, the controller will time through the inter-record gap (IRG) in the read mode, or will write the IRG in the write mode and execute the next command without stopping the tape.

13. Power Requirements

a. Source - CPU or Expansion Chassis power supply

b. +5VDC $\pm$ 5% @ 9.0 amps

14. Physical Specifications

a. Size

(1) One Standard DEC Hex-sized board

(2) Total Size: 8-7/8 x 15-3/4 inches (22.5 x 40 centimeters)

b. Weight (approximate)

(1) Controller board 22 oz. (0.62 kg)

(2) Cables & Adapters 26 oz. (0.74 kg) per drive

c. Environment

(1) Operation Temperature	0 to 55 degrees C
(2) Storage Temperature	10 to 70 degrees C
(3) Relative Humidity	10 to 90 percent (without condensation)

SELF-TEST SEQUENCE AND DESCRIPTION

LEDS #5 4321	TEST-DESCRIPTION	LISTING PAGE
1F	2910 LOOP CNTR, Q REG	3
1E	INCR/DECR Q REG, CARRY OUT	4
1C	SHIFT Q REG, LITERALS, XOR	5
18	POWER UP CONDITION TEST	6
10	REG FILE SHIFT TEST	7
07	2901 REG. ADDRESSING	8
01	REGISTERS - MOVING ZERO	9
02	CARRY CONTROL TEST	10
03	FIFO OPERATION TEST	11
04	WRITE FIFO TEST	12
05	READ FIFO TEST	13
06	PARITY TEST	14
08	MICRO-INTERRUPT TEST	15
00	PASS	16

SECTION II

INSTALLATION

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SECTION II

INSTALLATION

2.1 INTRODUCTION

2.2 This section provides information necessary to successfully set up and install the TC-131 Tape Controller into the DEC PDP-11 computer system. This information is essential for the initial installation and will also be valuable when the controller is reinstalled after repair.

2.3 The controller consists of a single printed circuit board which plugs directly into a slot in a standard SPC-wired system unit (backplane) in the computer mainframe or in an expansion chassis. Cable Adapter Paddleboards are provided to match the universal controller interface cables to the specific connector requirements of each drive (to be specified by the customer at the time of purchase). All DC power required for the operation of the controller is received from the power supply of the host computer or chassis via the backplane connector.

2.4 UNPACKING AND INSPECTION. After removal of the controller components from the shipping containers, visually inspect them for physical damage. Check off each item on the enclosed packing list. In case of damage, retain all packaging and notify the carrier to make a report. Be sure all minor parts and small items are found before discarding any shipping material.

2.5 SYSTEM COMPONENTS. Check the equipment supplied to ensure that all necessary items are included:

1. Controller Board
2. Drive Cables (3), one set per drive:

   Control cable

   Write cable

   Read cable
3. Adapter Paddleboards (3), one set per drive:

   Control Adapter Paddleboard

   Write Adapter Paddleboard

   Read Adapter Paddleboard

   Including:

   Terminators (on the Write and Control Paddleboards)

   Drive Select Jumpers (on the Control Paddleboard)

   See Figure 2-6 for part identification.
4. Program tapes:

   a. Diagnostic program tape

   b. Reliability program tape
5. Documentation:

   a. Hardware manual

   b. Logic manual

   c. Diagnositc manual
6. Other items which should be available:

   a. Computer

   b. Tape drives

   c. Standard SPC backplane system unit and associated power cable.

d. Unibus terminator, cables/jumpers

e. Unibus repeater, if required

f. Loading device for diagnostics

2.6 PREPARATION

2.7 Locate the position in the computer where the controller will be installed. Remember that the position of the system unit determines priority for DMA and interrupt activity. The tape controller usually works well if placed anywhere in the system. Check the cabling distance to the first drive and to each daisy-chained drive, verifying that all cable lengths will be adequate. Refer to your tape drive manual to install the tape drives. The computer and the tape drives must be prepared for operation before the controller can be expected to operate properly.

WARNING: INCORRECT INSTALLATION WILL CAUSE DAMAGE TO THE SYSTEM WHEN POWER IS APPLIED.

2.8 SYSTEM SET-UP

2.9 The tape system must be set up properly either when installing the system or after servicing. Proper set-up includes: (1) Setting the speed switches to the speed of the drives, (2) Setting the Address, Vector, and Interrupt Bus Level as required by software and (3) Removing the backplane jumper for the NPG signal. Each set of Tape Drive Adapter Paddleboard must have the proper termination (on the last drive), a Drive Select Jumper (except single drive installations), and Configuration Switch selections.

Installation is complete when the system components are plugged in and interconnected. A recheck and inspection of the installation ensures that no item is overlooked. The procedures to set the controller features and to install the controller are in the paragraphs that follow. Locations of setup items on the controller board are shown in Figure 2-1. A complete installation is shown in Figure 2-2. Also, check at the rear of the manual and this section for any special information which may be pertinent to your installation.

2.10 TAPE SPEED SELECTION. Tape drive speed is selected on the controller by the setting of four switches located by the setting of four switches located in a switch pack at location 28G. Speed selection provides two tape speeds for both the NRZI and PE modes. Table 2-1 provides the required speed settings for various combinations, (if only one speed is used, it may be selected on either speed A or speed B.)

2.11 CONTROLLER JUMPERS

2.12 ADDRESS JUMPERS. Normally, the controller is assigned to the standard TM-11 Unibus addresses, 772 520-772 532_8. An alternate address may be assigned to the controller when a second controller is used, or when required for any other reason. An alternate address as well as the standard one are shown in Table 2-2. Check the jumpers to ensure that the controller will operate properly. These jumpers are located near IC 13F.

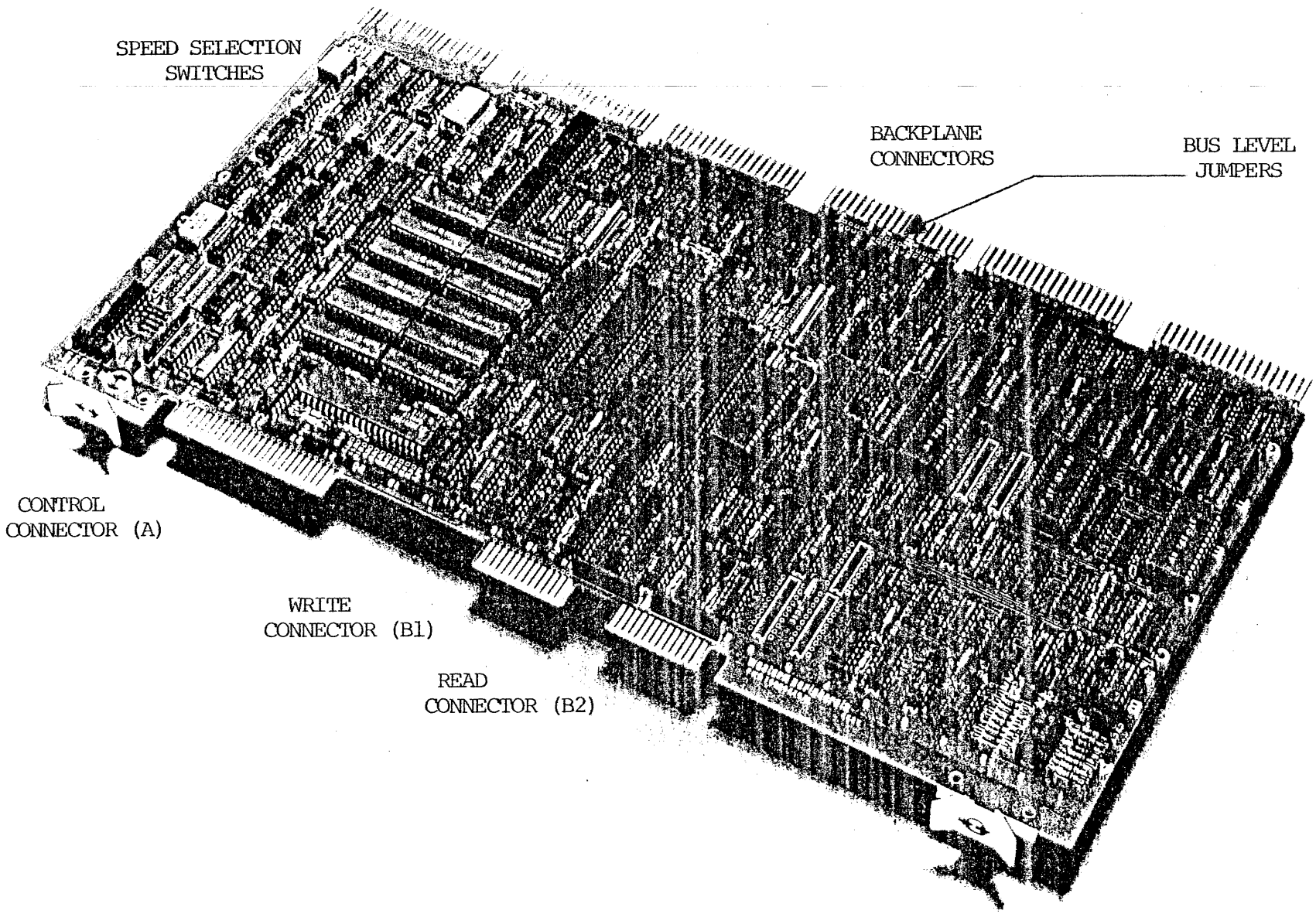


FIGURE 2-1 CONTROLLER INSTALLATION FEATURES

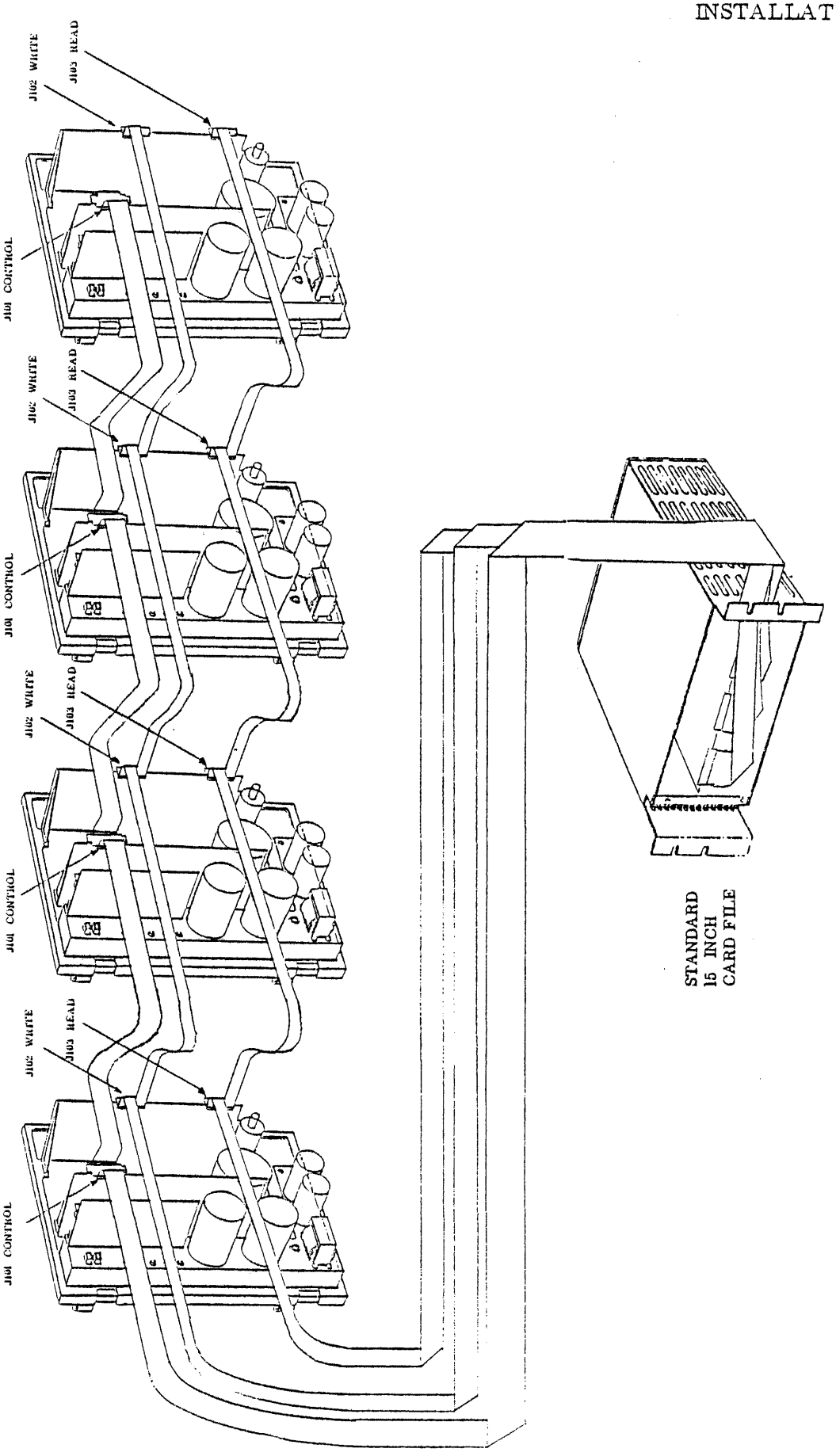


Figure 2-2 Example of Typical System Installation

TAPE SPEEDS (ips)		SWITCHES			
A	B	1	2	3	4
25	37.5			ON	ON
25	45		ON		ON
25	75	ON			
25	125	ON	ON		
37.5	45		ON	ON	
37.5	75	ON			ON
37.5	125	ON	ON		ON
45	75	ON		ON	
45	125	ON	ON	ON	
75	125	ON	ON	ON	ON

ON = CLOSED; ALL OTHERS OFF (OR OPEN)

TABLE 2-1 SPEED SELECTION SWITCHES

2.13 VECTOR JUMPERS. Normally, the controller is assigned to the standard TM-11 Unibus vector, 224_8. An alternate vector may be assigned to the controller when a second controller is used, or when required for any other reason. An alternate vector as well as the standard one are shown in Table 2-3. Check the jumpers to ensure that the controller will operate properly. These jumpers are located near IC 19F.

2.14 NPG JUMPER REMOVAL/BUS LEVEL SELECTION

2.15 PRIORITY JUMPERS. The Direct Memory Access Non-Processor Grant lines are daisy-chained to the I/O devices. As shown in Figure 2-3, each device receives this signal on pin CA1 and sends this signal from pin CB1 to the next device.

BIT NO.	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STANDARD ADDRESS 772520	1	1	1	1	1	1	0	1	0	1	0	1	0	1	X	X	X	X
DESIRED ADDRESS (FILL-IN)	1	1	1	1	1	1									X	X	X	X
INSTALL JUMPER FOR Ø - BIT	(NOT ALTERABLE)						E20 TO E28 *	E19 TO E27	E18 TO E26 *	E17 TO E25	E16 TO E24 *	E15 TO E23	E14 TO E22 *	E13 TO E21	REGISTER ADDRESS			

* STANDARD ADDRESS PROVIDED IN ETCHED JUMPERS.

JUMPERS ARE LOCATED ON SCHEMATIC PAGE 2 AND ON BOARD NEAR IC 13F.

TABLE 2-2 ADDRESS JUMPERS

BIT NO.	7	6	5	4	3	2	1	0
STANDARD VECTOR 224	1	0	0	1	0	1	0	0
DESIRED VECTOR (FILL-IN)								
INSTALL JUMPER FOR Ø - BIT	E34 TO E40	E33 TO E39 *	E32 TO E38 *	E31 TO E37	E30 TO E36 *	E29 TO E35	FIXED	

* STANDARD VECTOR PROVIDED IN ETCH JUMPERS. JUMPERS ARE LOCATED ON SCHEMATIC PAGE 2 AND ON BOARD NEAR IC 19F.

TABLE 2-3 VECTOR JUMPERS

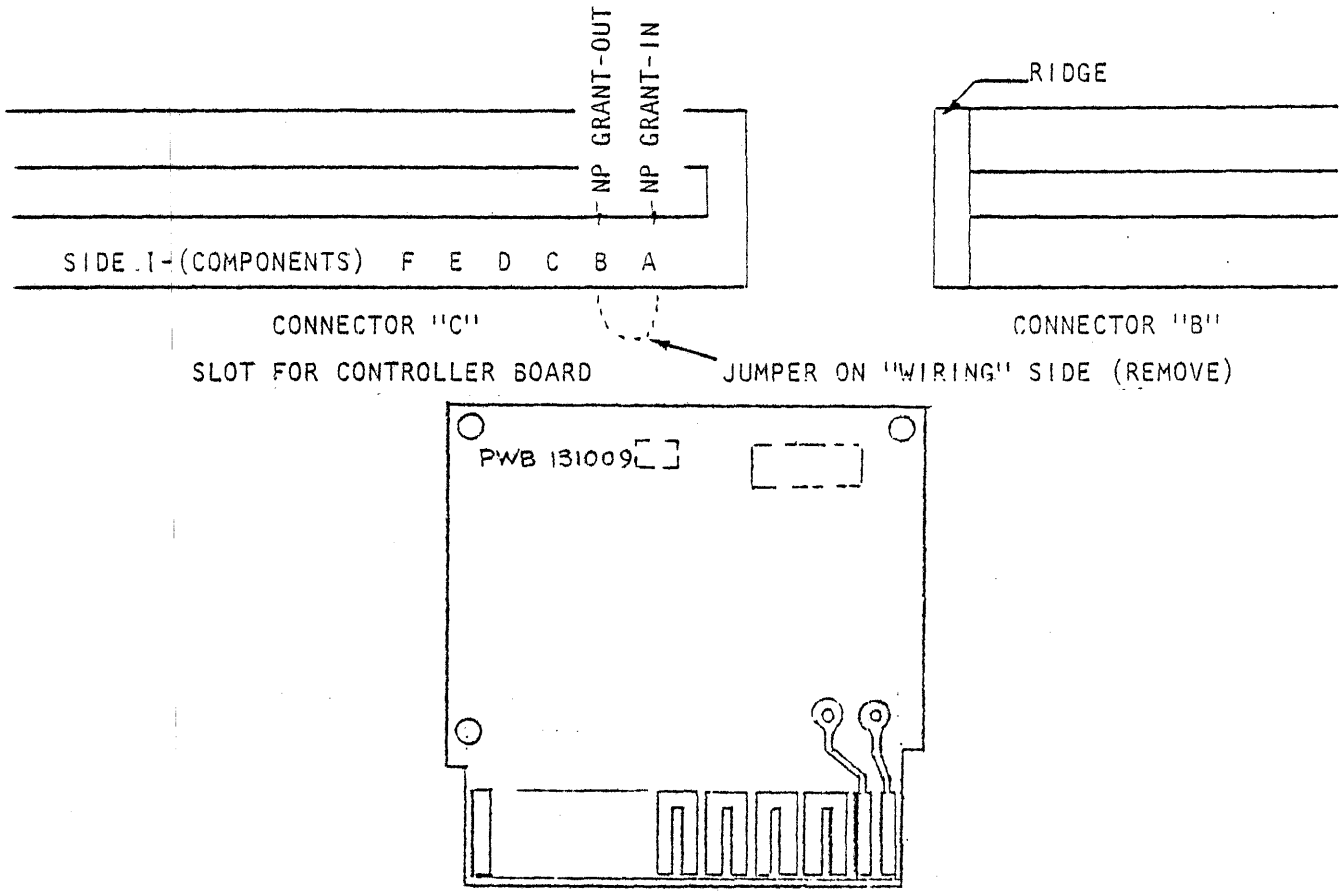


FIGURE 2-3 BACKPLANE JUMPERS

There can be no break in the chain throughout the I/O devices. A previously unused card connector will have jumpers across these pins. When installing the controller, remove the priority jumpers from across the connector pins of the card slot for the controller board and ensure that the priority lines are daisy-chained from the CPU through the devices.

2.16 The interrupt - bus grant lines are also daisy-chained to the I/O devices. When installing the controller, remove the priority jumper card from the "D" connectors of the card slot to be occupied by the controller and check that these lines are daisy-chained through the devices or jumper cards from the CPU.

2.17 BUS LEVEL SELECTION. Interrupts on the Unibus are selectable among four bus levels. The controller is normally operated on Interrupt Bus Level 5. Verify the tape controller bus level of the operating system to select the proper bus level. However, when operating the Reliability test program Bus Level 5 must be used. Install the bus level jumpers according to Table 2-4. These jumpers are located at IC rows 10 through 14 near bus connector "D".

2.18 CONTROLLER INSTALLATION

2.19 CONTROLLER BOARD INSTALLATION. Referring to Figure 2-4, place the controller boards into any convenient location of the system unit. Ensure the boards are oriented correctly (notches on the board connectors must fit the ridges of the system unit), and are seated fully.

WARNING: INCORRECT INSTALLATION WILL CAUSE DAMAGE TO THE SYSTEM WHEN POWER IS APPLIED.

FUNCTION	BUS LEVEL			
	4	5*	6	7
BUS REQUEST	E49-E61	E50-E62	E51-E63	E52-E64
GRANT IN GRANT OUT	E42-E54 E41-E53	E44-E56 E43-E55	E46-E58 E45-E57	E48-E60 E47-E59
BUS GRANT BYPASS	E56-E55 E58-E57 E60-E59	E54-E53 E58-E57 E60-E59	E54-E53 E56-E55 E60-E59	E54-E53 E56-E55 E58-E57

* STANDARD BUS LEVEL 5 JUMPERS ARE PROVIDED IN ETCH. JUMPERS E41 THRU E64 ARE LOCATED AT IC ROWS 10 THRU 14, NEAR BUS CONNECTOR "D".

TABLE 2-4 BUS LEVEL SELECTION

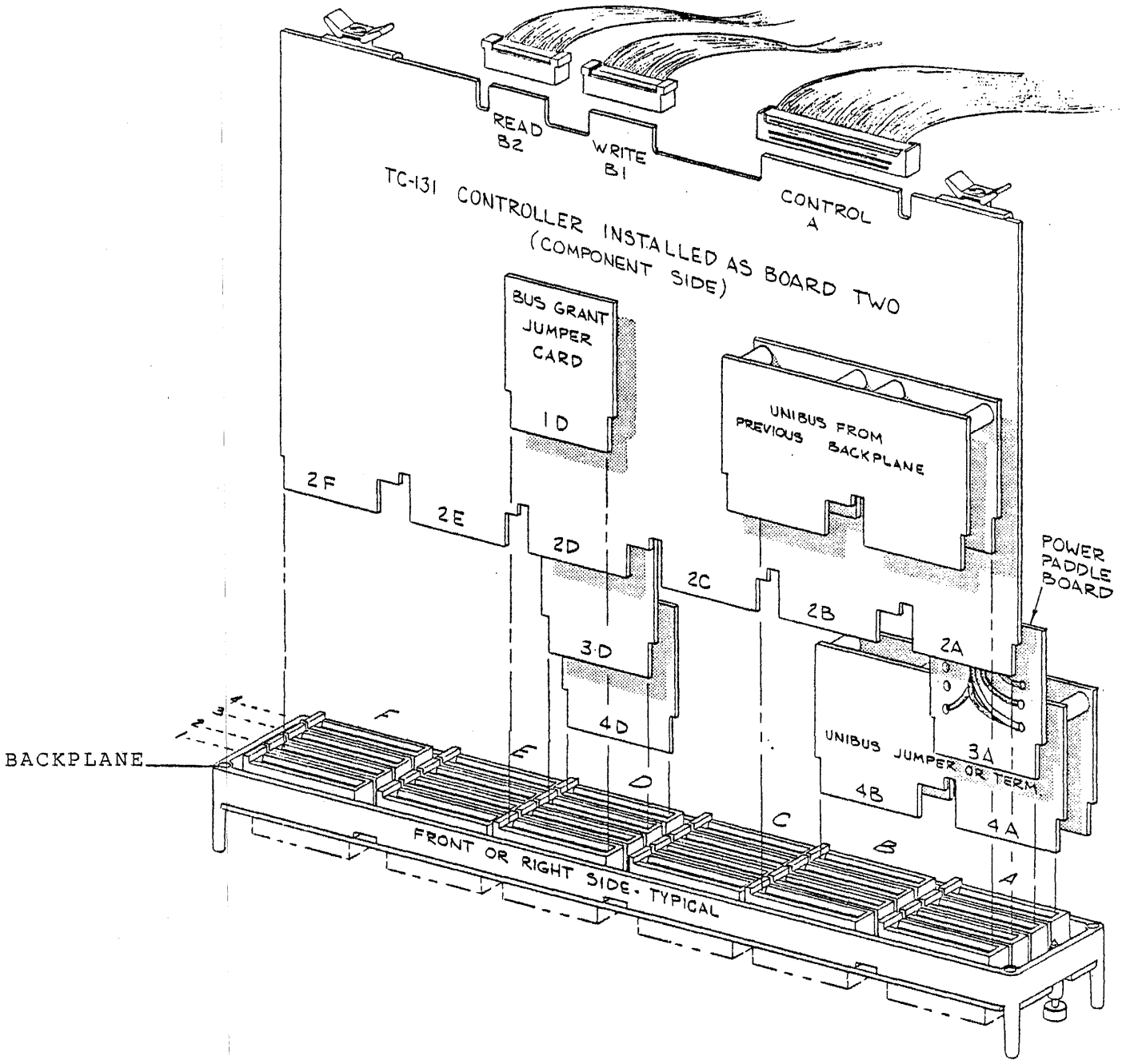


FIGURE 2-4

SYSTEM CONFIGURATION

(TYPICAL)

2.20 **CONTROLLER CABLE CONNECTIONS.** Locate the following cables:

Description	Conductors	Controller-End Marking
Tape Read Cable	26	Top B2
Tape Write Cable	26	Top B1
Tape Control Cable	50	Top A

The ribbon cables are keyed to prevent incorrect connections. Check the ribbon cable connectors to assure that all keys are in place.

2.21 Install the Read, Write, and Control cables (in that order) onto the controller connectors as shown in Figure 2-4. The cables will exit toward the solder side of the boards.

2.22 **TAPE DRIVE INSTALLATION**

2.23 **ADAPTER PADDLEBOARD SETUP.** Locate a set of three Adapter Paddleboards for each tape drive. The Adapter Paddleboards for each drive require proper setup before installation. Setup includes proper termination, switch settings, and installation of drive selection jumper plugs.

2.24 **TERMINATORS.** Consulting the tape manuals for details, remove all termination devices from each drive. Remove the terminators from the Write and Control Adapter Paddleboards, except the Adapter Paddleboards on the drive located farthest from the controller. See Figure 2-5. Ensure that the last Adapter Paddleboards have the terminators installed as shown.

2.25 **CONFIGURATION SWITCHES.** Set the switch module on each Control Paddleboard according to the configuration requirements of the tape drive. Switch settings are given in Table 2-5.

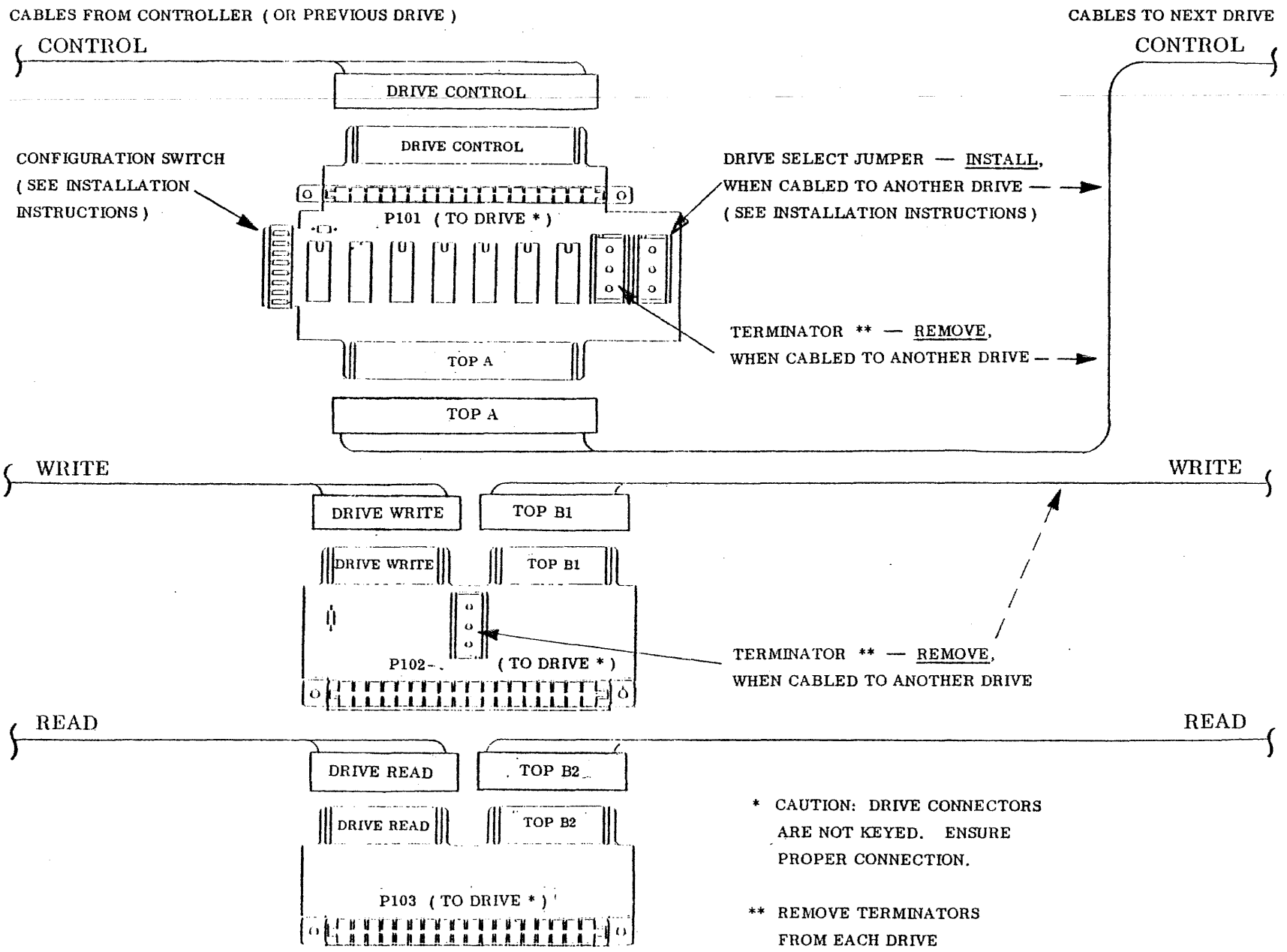


Figure 2-5. Details of Adapter Installation

SWITCH NUMBER	SETTING
1	"ON" for normal operation "OFF for H.P. drives and for some Pertec models
2	OFF
3	OFF
4	ON - For HIGH SPEED drive (Controller speed B) OFF - For LOW SPEED drive (Controller speed A)
5	ON
6	"ON" for 9-track NRZI-only drives "OFF" for all other drives
7	"ON" for either dual density or PE drives made by Kennedy, Digidata, or Qantex "OFF" for all other drives
8	"OFF"

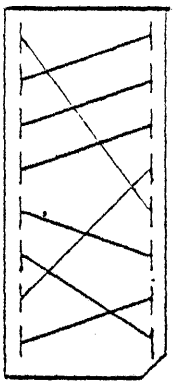
Reference Schematic Number 122036

Table 2-5 Configuration Switches

2.26 **DRIVE SELECT JUMPERS.** Ensure that the correct Drive Select Jumper is installed in the Control Paddleboards. The last drive does not require a Drive Select Jumper (leaving one installed will have no effect).

1. For tape drives without front panel unit select switches, use jumper part number 122012 as shown in Figure 2-6.
2. For tape drives with front panel unit select switches:
   a. Use jumper part number 122010 as shown in Figure 2-6.
   b. On drives with Unit Select Switches that receive the select lines from J101, ensure Control Paddleboard Jumpers are installed from P to R (factory etch), N to M, E to F, and G to H. See Table 2-6.
   c. On drives with externally connected Unit Select Switches, connect as shown in Table 2-6.

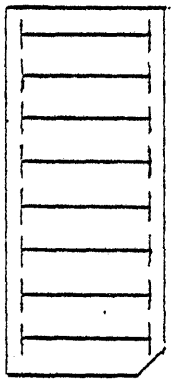
2.27 **TAPE DRIVE INTERCONNECTIONS.** Locate a set of three ribbon cables for each drive (one set is connected to the controller). Check that each connector has its key in place and connect the cables as shown in Table 2-5 and Figures 2-7 and 2-8.



NON-SELECT JUMPER (PN 122012)

For daisy-chained drives

Without front panel Unit Select switches.

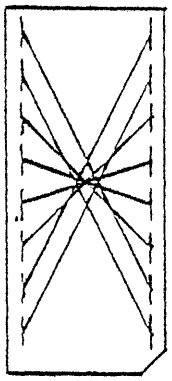


UNIT SELECT JUMPER (PN 122010)

For daisy-chained drives

with Unit Select switch

(Except fourth tape unit)



UNIT SELECT JUMPER (PN 122011)

For daisy-chained drives

with unit select switches

(Install in fourth tape unit)

NOTE: No jumper plug is required on the last tape unit or for single drive installations. However, it should remain in the board for future expansion of the system.

Figure 2-6 Drive Select Jumpers

NOTE: APPLIES TO DRIVE SELECT THUMBWHEEL OPTION ONLY.

Drive Select Line:	Add Jumper:	To Activate J101 Pin:	Connect External Switch To:
Select Ø	P-R (Etch)	J	A
Select 1	N-M	A	B
Select 2	E-F	18	D
Select 3	G-H	V	C
			L (return line from switch)

Table 2-6 Control Adapter Select Options

(Sequence is repeated for each drive)					
Cables		Paddleboards		Cables	
Controller End	Drive End	Controller End	Daisy Chain End	Controller End	Drive End
Top A	Drive Control	Drive Control	Top A	Top A	Drive Control
Top B1	Drive Write	Drive Write	Top B1	Top B1	Drive Write
Top B2	Drive Read	Drive Read	Top B2	Top B2	Drive Read

Table 2-7 Connector Legends and Cable Connections

2.28 Connect the Control, Write and Read Adapter Paddleboard connectors to J101, J102, and J013, respectively, on the tape transport. (Reference the tape drive manual for details.) Connect the paddleboards to the drive with care. The green connectors are not keyed to the drive connectors. Therefore, it is possible to (1) install the connector backwards or (2) to place the Adapter Paddleboard on the wrong drive connector (e.g., Read and Write Connectors reversed.) Avoid incorrect connection by (1) verifying the function of each drive connector and (2) physically checking the pin orientation of the mating connectors. If possible, secure the paddleboard connectors to the drive connectors with screws. Neatly dress and tie all cables so the installation appears neat and professional.

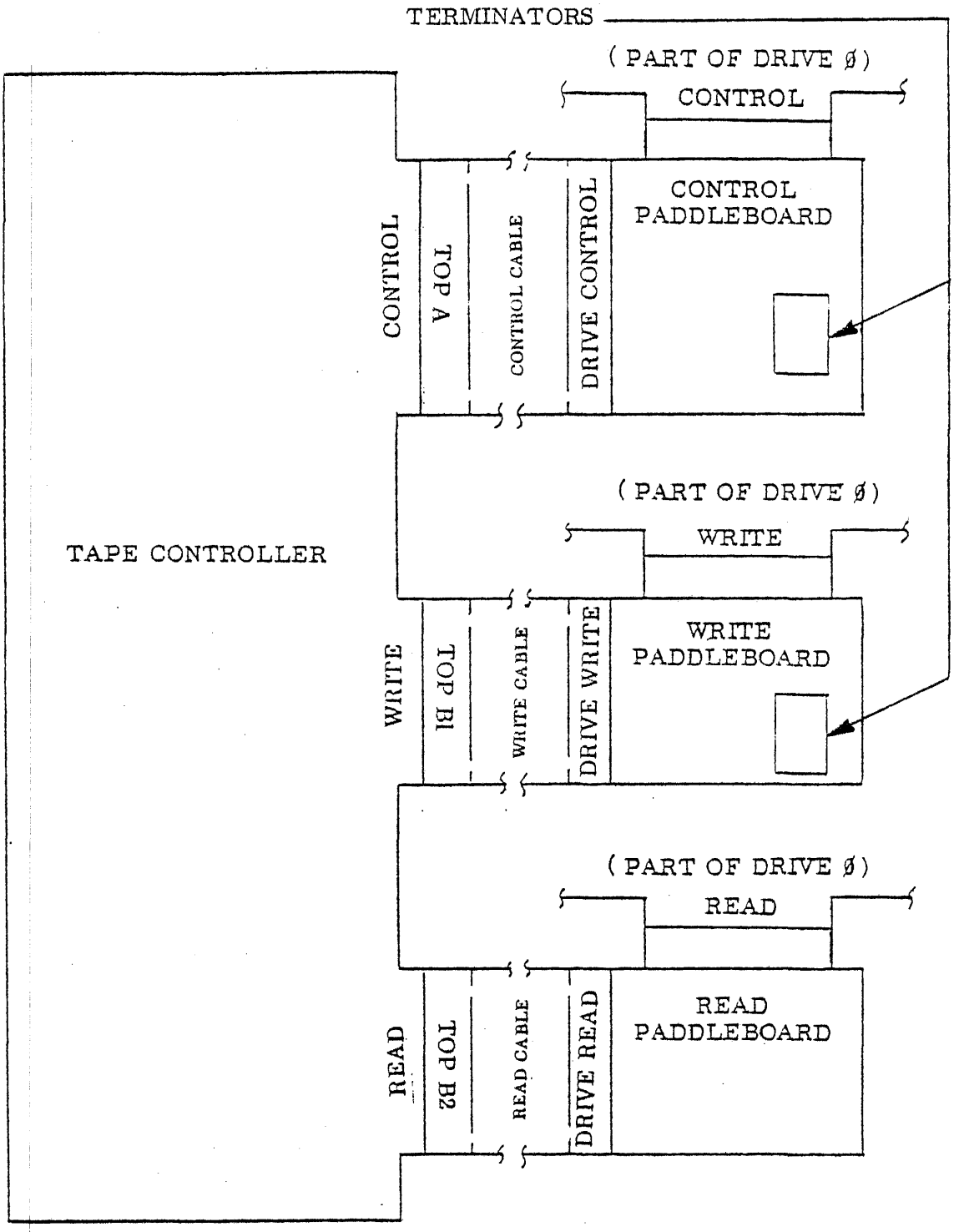


Figure 2-7. Single Tape Drive Connections

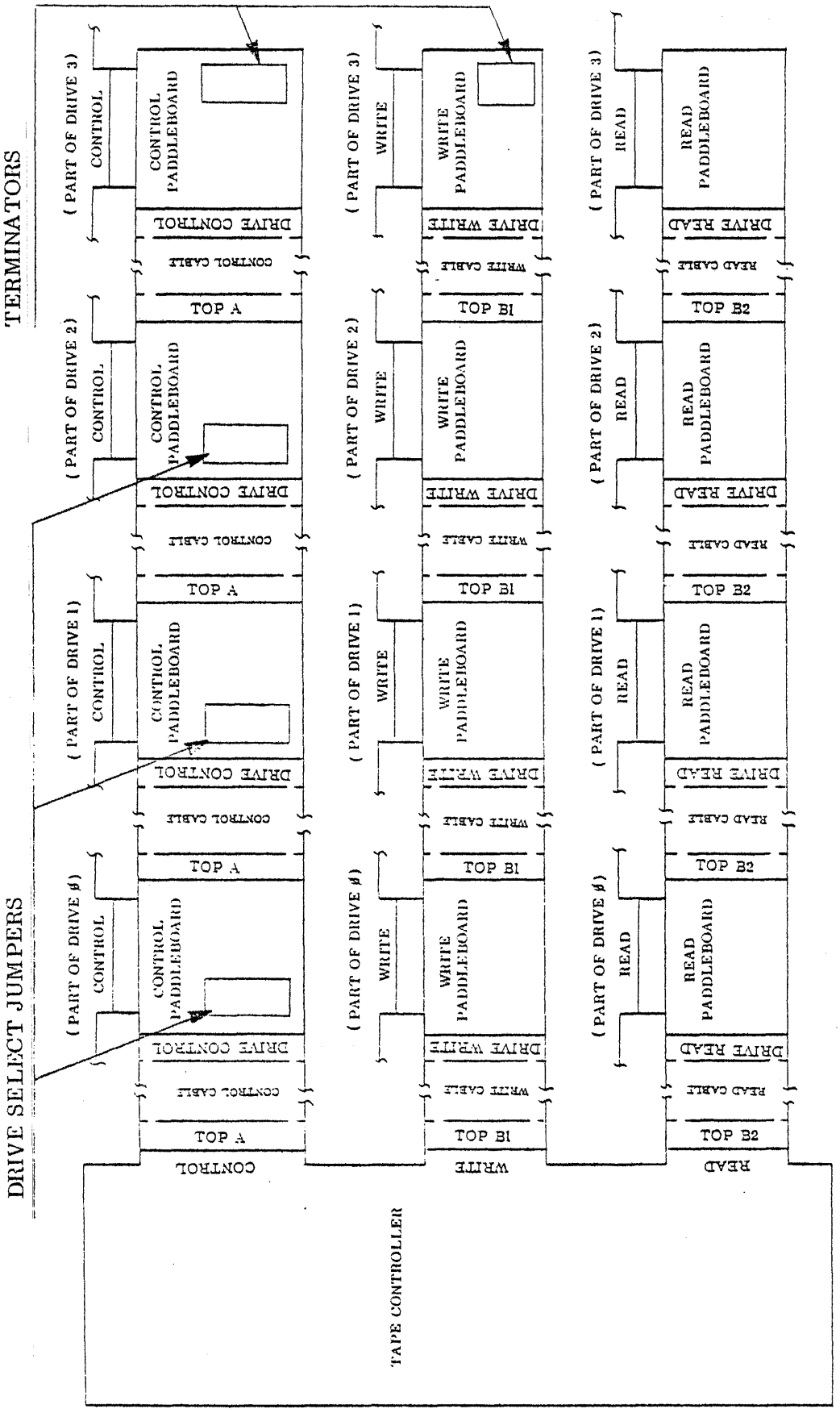


Figure 2-8. Tape Drive Daisy-Chain Connections

2.29 INSTALLATION CHECKLIST

2.30 The installation of the controller is now complete. Doublecheck your installation before testing and operation.

CHECKLIST

( ) Were all items supplied?

( ) Did you choose a location for the controller which will provide the desired bus priority?

( ) Do all cables reach with adequate service loops?

( ) Are the computer and tape drives ready?

( ) Did you properly set up tape speed including setting Speed A, Speed B, and using the correct VCO Speed Chip?

( ) Did you check the address, vector, and bus level jumpers?

( ) Did you check the jumpers for the priority lines on the computer backplane?

( ) Did you install the controller correctly?

( ) Did you connect the cables properly?

( ) Did you set up the Adapter Paddleboards for proper operation, including:

1. Removing termination devices from each tape drive
2. Removing terminator chips from the Control and Write Adapter Paddleboards, except the last paddleboards in the daisy-chain
3. Setting the configuration switches

4. Ensuring that the correct drive jumpers and options are installed?

( ) Did you connect the ribbon cables to the Adapter Paddleboards at each drive?

( ) Did you connect the Adapter Paddleboards to the tape drives?

WARNING: BEFORE POWERING THE SYSTEM, BE SURE THAT ALL PARTS ARE PROPERLY CONNECTED

The tape system is now ready for testing and operation.

NOTE: Refer to the supplementary information at the back of the manuals for additional advice.

IBM PACK	REMOTE DENSITY SELECT
1. STANDARD - Bit 10 in MTRD 2. OPTION 1 - Use of Drive Select-Bit 10 in MTC 3. OPTION 2 - Customer installed jumper or remote switch	1. STANDARD - Drive Density Switch 2. OPTION 1 - Use of Drive Select-Bit 10 in MTC

When using OPTION 1 either IBM Pack OR Remote Density Select can be opted, NOT both. In order for a customer to have both options, the following are the different combinations.

IBM PACK	REMOTE DENSITY SELECT
1. Standard	Standard and/or Option 1
2. Option 1	Standard
3. Option 2	Standard and/or Option 1

IBM PACK	REMOTE DENSITY SELECT	JUMPERS
Standard	Standard	E82 to E83, E84 to E85
Standard	Option 1	E83 to E85, E82 to E84
Option 1	Standard	E83 to E85, E84 to E85, E80 to E81
Option 2	Standard	E82 to E83, E84 to E85, E78 to E79
Option 2	Option 1	E83 to E85, E82 to E84, E78 to E79

TABLE 2-8 IBM AND DENSITY SELECT JUMPERS

SECTION III

PROGRAMMING

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SECTION III

PROGRAMMING

3.1 GENERAL

3.2 This section contains machine-level programming reference information which describes the registers of the controller. Also contained in this section is information on the operation of the controller, addressing, data transfers, and interrupts. This information will be useful in understanding the operating systems as well as the diagnostic programs. A working knowledge of machine-level programming, along with reference to the information contained in this section, will allow the Customer Engineer to create small diagnostic programs for testing specific functions of the controller.

3.3 PROGRAMMED OPERATIONS

3.4 The DEC computer controls devices differently than most other computer systems. Since registers in peripheral devices are assigned addresses on the bus similar to memory, all instructions that address memory locations are, in effect, I/O instructions. Registers in devices can take advantage of all the arithmetic power of the processor. There is no limit to the number of registers that a device may have, providing great flexibility in the design and control of peripheral equipment.

3.5 OPERATION AS A SLAVE DEVICE. All command and status information is transferred with the CPU acting as the master device and the controller acting as the slave. The individual bits within the Command Register control the operations of the device. For example, the command to make the tape

system read a block from tape is provided by properly setting bits 1 through 3 in the Command Register. Status conditions are also handled by the assignment of bits within the registers. All command and status information is written or read by program instructions. Indications of operation complete can be through examination of the status and command registers or by utilizing the system interrupts.

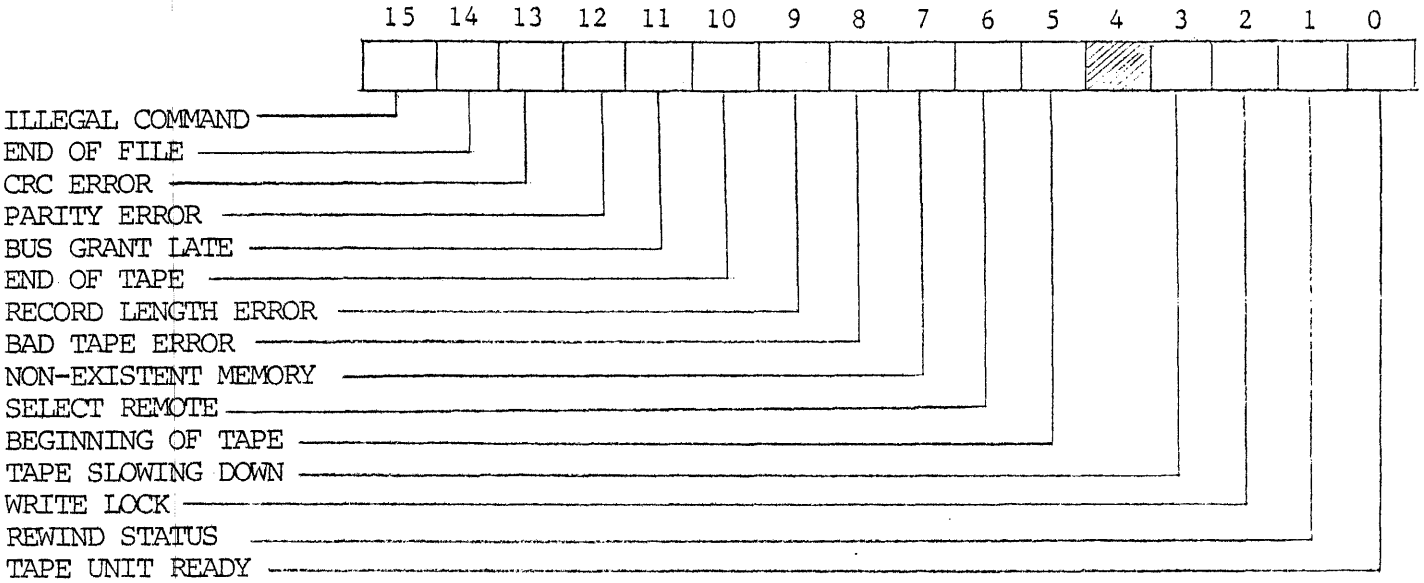
3.6 OPERATION AS A MASTER DEVICE. Once a function command has been issued to the controller, the operation is executed by the controller, utilizing DMA bus transfers to move the data to or from the memory. The Byte/Record Counter Register and the Current Memory Address Register are updated throughout the DMA activity. At the conclusion of an operation, completion is indicated to the CPU through the status bits and also an interrupt (if enabled). The standard interrupt vector (224 octal) is used.

3.7 CONTROLLER REGISTERS

3.8 REGISTER ADDRESSING. The registers of the tape controller occupy bus address locations 772 520 through 772 532 and are addressed by the CPU with the controller being the slave device. These addresses are placed on the bus in the same way that memory is addressed. The controller latches the address until the completion of the transfer.

3.9 STATUS REGISTER (MTS) 772 520. The status register contains only read bits, providing the CPU with status indications from both the tape drive and the controller.

REGISTER BIT ASSIGNMENTS:



1. MTS BIT 15 ILLEGAL COMMAND (ILL COM) - When an illegal command is received, the CU RDY bit remains true, and the command is disregarded. The Illegal Command bit is set for any of the following conditions and sets the ERR bit in the Command Register:
   a. Any tape command initiated during a tape operation (CU RDY bit is false)
   b. Any tape command where the selected drive is not on-line (Select Remote bit is false).
   c. Any write command on a drive which is file protected.
   d. The drives Ready status line going false during an operation.
2. MTS BIT 14 END OF FILE (EOF) - The EOF bit is set when a file mark character is detected during a Read, Space Forward or Space Reverse operation. The EOF bit sets the ERR bit in the Command Register.
3. MTS BIT 13 CRC ERROR - This bit is set when the CRC check fails during, Write, or Write with Extended Record Gap. This bit will

set the ERR bit in the Command Register.

4. MTS BIT 12 PARITY ERROR (PAE) - The Parity Error bit is set when the controller detects a parity error, LRC error, or Postamble error during a Read, Write, or write with Extended Record Gap operation. The PAE bit does not affect the transfer of data. During a Write operation, the entire record will be transferred onto tape or in a Read operation, the entire record will be transferred to memory. The PAE error bit will set the ERR bit in the Command Register.

5. MTS BIT 11 BUS GRANT LATE (BGL) - The Bus Grant Late bit is set when the controller overflows (or empties) its internal buffer and information is lost during an operation. This bit will also be set during a Read operation when the internal buffer of the controller is not emptied before the tape begins to stop. The ERR bit in the Command Register will be set when the BGL bit is true.

6. MTS BIT 10 END OF TAPE (EOT) - The End of Tape bit is set when the EOT marker is encountered while the tape is moving in the forward direction. The bit will be reset when the EOT marker is passed while performing a Rewind or Space Reverse operation. The ERR bit in the Command register will be set when the EOT bit is true.

7. MTS BIT 9 RECORD LENGTH ERROR (RLE) - The Record Length Error bit will be set during a Read operation when the length of the record being read exceeds the memory allocation as indicated by the Byte/Record Counter. When the Byte/Record Counter indicates the

end of the memory allocation, data transfer will stop and the controller will continue to advance the tape to the next interrecord gap. A Record Length Error stops the incrementing of the Byte/Record Counter and the Current Memory Address Register and sets the ERR bit in the Command Register.

8. MTS BIT 8 BAD TAPE ERROR (BTE) - The Bad Tape Error bit sets when a character is detected (read strobe) during the gap shut-down (or the slowing down) for all operations (except rewind). When a Bad Tape Error is detected, the ERR bit in the Command Register is set.

9. MTS BIT 7 NONEXISTENT MEMORY NXM) - The Nonexistent Memory bit is set during direct memory operations (when the controller is bus master and is performing data transfers with the bus) and the controller does not receive a Slave Sync response within 14 microseconds after it issues the Master Sync signal. When the Nonexistent Memory error bus time-out is detected, the Read or Write operation is terminated, stopping the tape in the interrecord gap, and setting the ERR bit in the Command Register.

10. MTS BIT 6 SELECT REMOTE (SELR) - The Select Remote bit is set when the addressed tape drive is on line and cleared when the addressed tape unit is off line, powered off, or disconnected.

11. MTS BIT 5 BEGINNING OF TAPE (BOT) - The Beginning of Tape bit is set when the tape drive detects the Load Point mark at the beginning of the magnetic tape.

12. MTS BIT 4 7 CHANNEL (7 CH) - The seven channel bit is not used and is always a Ø.

13. MTS BIT 3 SLOWING DOWN (SDWN) - The Tape Slowing Down (or Settle Down) bit is set whenever the tape unit is stopping after a rewinding operation.

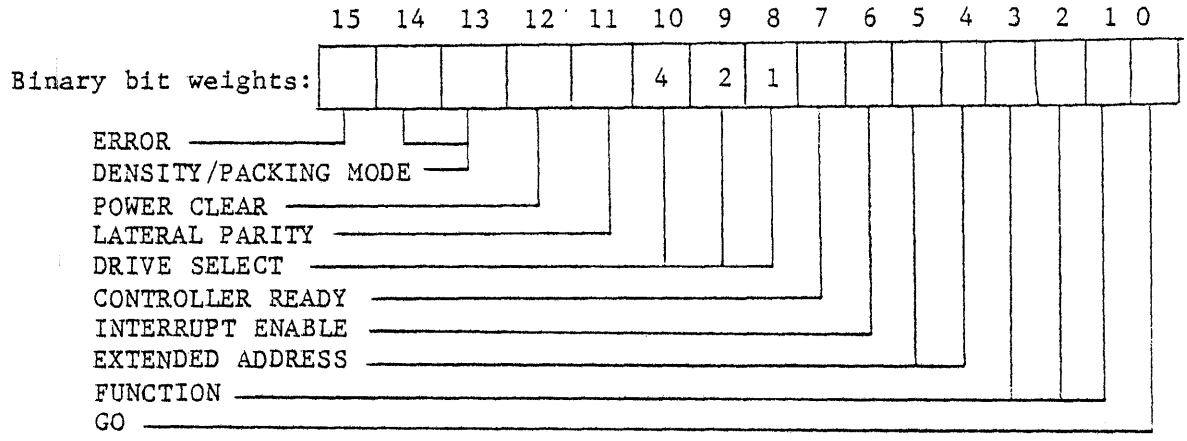
14. MTS BIT 2 WRITE LOCK (WRL) - The Write Lock bit is set to prevent the software from attempting to write information on the tape when the operator has removed the write-enable ring from the supply reel on the tape drive.

15. MTS BIT 1 REWIND STATUS (RWS) - The Rewind Status bit is set by the selected drive when it receives a Rewind command from the controller or operator panel and is cleared by the selected drive when the tape arrives at BOT, completing the Rewind operation.

16. MTS BIT Ø TAPE UNIT READY (TUR) - The Tape Unit Ready bit is set when the selected tape unit is stopped and is cleared when the controller begins to execute a function command.

3.10 COMMAND REGISTER (MTC) 772 522. This register receives operational commands from the CPU and provides status information from the controller and the tape drive.

COMMAND REGISTER BIT ASSIGNMENTS:



1. MTC BIT 15 ERROR (ERR) - Set as a function of bits 7-15 of the Status Register (MTS) being set. This bit is cleared as the result of an Initialize or a Go command to the tape unit.

2. MTC BITS 14, 13 (DEN 8, DEN 5)

Bit 14 (DEN 8) is used to specify the desired density, as follows:

(DEN 8) BIT 14	(DEN 5) BIT 13	
1	X	9 channel 800 bpi - NRZI
Ø	X	9 channel 1600 bpi - PE

3. MTC BIT 12 POWER CLEAR (PCLR) - This bit provides the means for the processor to clear the controller and the tape drives without clearing other devices in the system. The PCLR bit is always read back by the processor as zero.

4. MTC BIT 11 LATERAL PARITY (PEVN) - This bit, when set, selects even lateral parity if required for 7-track operations. Otherwise, odd parity is generated and checked during all data transfer operations.

5. MTC BITS 10-8 DRIVE SELECT (SLT 1, 2, 4) - These bits specify one of the eight possible tape units. All operations defined in the MTC register and all status conditions defined in the MTS register refer to the unit indicated by these bits.

DRIVE NO.	LOGICAL DRIVE ADDRESS	DRIVE SELECT LINES SL1 (Bit 8)	SL2 (Bit 9)	SL4 (Bit 10)
1	Ø	False	False	False
2	1	True	False	False
3	2	False	True	False
4	3	True	True	False
5	4	False	False	True
6	5	True	False	True
7	6	False	True	True
8	7	True	True	True

6. MTC BIT 7 CONTROLLER READY (CUR) - This bit is cleared at the start of a tape operation and is set at the end of a tape operation to indicate that the controller is ready to accept a new command.

7. MTC BIT 6 INTERRUPT ENABLE (INT ENB) - When this bit is set, an interrupt occurs whenever either the Controller Ready bit or the ERR bit goes true or whenever a rewinding tape unit arrives at BOT. In addition, an interrupt occurs for an instruction that sets the INT ENB bit but does not set the GO bit.

8. MTC BITS 5, 4 EXTENDED BYTE ADDRESS (YBA 17, XBA 16) - These bits access the two most significant bits of Current Memory Address Register, providing an 18-bit memory addressing capability.

9. MTC BITS 3 - 1 FUNCTION BITS - These bits select one of eight command functions.

Bit 3	Bit 2	Bit 1	OCTAL	
0	0	0	1	Off Line
0	0	1	3	Read
0	1	0	5	Write
0	1	1	7	Write EOF
1	0	0	9	Space Forward
1	0	1	11	Space Reverse
1	1	0	13	Write/E.R.G.
1	1	1	15	Rewind

a. Off Line Command. This command, which places the selected drive off-line, is usually preceded by a rewind command after completing all operations on the reel of tape. The controller does not go Busy, leaving it free for use with other drives in the system.

b. Read Command. The program must specify a byte count (in twos complement - or negative - form) and an initial address. The controller reads a single record from tape and sends the data via DMA operations to the locations specified by the Address Register until the EOR gap is encountered or the Byte Counter overflows, whichever occurs first. For operations with variable length records, a large byte count ensures that the entire record will be read. The length of the record of unknown size can then be determined after it is read by comparing the Byte Counter at the end of the operation to its initial setting. The setting of BGL status during the record indicates that information has been lost, but data transfers

continue until the byte counter overflows or the EOR gap is detected.

c. Write Command. The program must specify a (negative) byte count and an initial bus address. If Write Lock is true, GO sets Illegal Command, and the controller rejects the operation. Otherwise, the Controller makes an immediate data request for the first word, and writes the data it receives from the locations specified by the address counter onto the magnetic tape until either the byte counter overflows or a BGL or NXM error occurs, at which time the controller terminates the record.

d. Write End of File Command. Unless Write Lock is set, GO starts the controller into operation to write a file mark. With Write Lock true, the command is rejected.

e. Space Forward Command. The program must specify a (negative) byte count equal to the number of records to be spaced. The controller spaces forward over the given number of records unless it encounters a file mark or the end of tape. To space over a file, the program can simply give a zero (maximum) byte count.

f. Space Reverse Command. The program must specify a (negative) byte count equal to the number of records to be spaced. The controller spaces reverse over the given number of records, but it stops the tape automatically upon encountering a file mark or the Load Point. To space over a file, the program can simply specify a zero (maximum) byte count.

g. Write with Extended Record Gap Command. The operation of this command results in a three and one-half inch length of tape being erased before the data is written. This provides a method of erasing a bad record from a damaged portion of tape before rewriting the data farther down on the tape. A Space Reverse One Record operation generally precedes this command.

h. Rewind Command. This command initiates a rewind operation in the addressed tape drive, which rewinds the tape onto the supply reel at high speed, and stops at BOT. The controller does not go Busy, leaving it free for further use by the program during the rewind operation.

3.11 BYTE/RECORD COUNT REGISTER (MTBRC) 772 524. The MTBRC is a 16-bit binary counter which is used to count bytes of memory during Read or Write operations, or to count records in a Space Forward or Space Reverse operation. When used in a Write or Write with Extended Record Gap operation, the MTBRC is initially set by the program to the 2's compliment of the number of bytes to be transferred from memory to tape. The MTBRC increments by one immediately after each byte memory access or by two after each word transfer. The MRBRC overflows to zero after the last byte of the record has been read from memory. Bus transfers are terminated by this byte count zero condition.

3.12 When the MTBRC is used in a Read operation, it is set to the 2's complement of a number equal to or greater than the maximum expected record length, indicating the memory allocation for the read data. A Record Length Error (RLE) occurs when the actual record length is greater than the allocated memory, as indicated by the MTBRC overflowing before the EOR gap is detected.

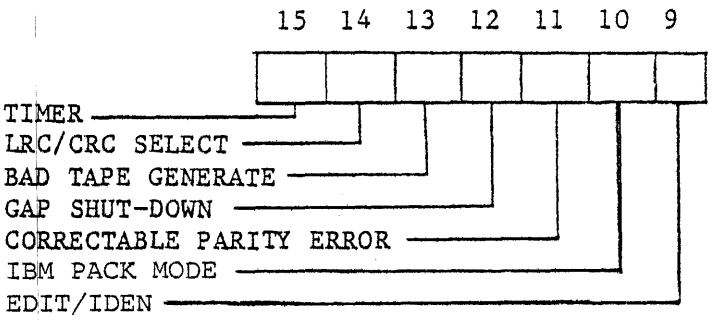
3.13 When the MTBRC is used in a Space Forward or Space Reverse operation, it is set to the 2's compliment of the number of records to be spaced over. It is incremented by one each time a record passes the head whether the tape is moving in the forward or reverse direction.

3.14 CURRENT MEMORY ADDRESS REGISTER (MTCMA) 772 526. The MTCMA register contains 18 memory address counter bits. It is used in DMA operations to provide the memory address for data transfers in Read Write and Write with Extended Record Gap operations. Prior to issuing a command, the MTCMA is set to the memory address to be used for the first data transfer. The MTCMA is incremented by one immediately after each byte transfer and by two after each word transfer. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address of the word following the final transfer for the record. After Bus Grant Late (BGL) and Non-Existent Memory (NXM) error conditions, the MTCMA contains the address of the location in which the failure occurred.

3.15 DATA BUFFER (MTD) 772 530. The data buffer is a register which is used for diagnostic purposes. After the completion of an operation, the 9-bits of the CRC or LRC are placed into the data register and made available to the program, depending upon the TU-10 Register bit 14.

3.16 TU-10 READ LINES (MTRD) 772 532. In addition to its use for diagnostic purposes, this register receives additional command bits from the CPU and provides additional status information from the controller and from the tape drive.

TU-10 READ LINES REGISTER BIT ASSIGNMENTS:



1. MTRD BIT 15 TIMER (10KHz) - This read-only bit provides the diagnostic program with the output of a 10 KHz timer. This timer bit, having a 50% duty cycle, is used by the diagnostic program for measuring the time duration of tape operations.

2. MTRD BIT 14 LRC/CRC SELECT (LRCS) - This write/read bit, when set, disables the CRC word from remaining in the data register at the conclusion of an operation, replacing it with the LRC character.

3. MTRD BIT 13 BAD TAPE GENERATE (BTG) - If set during an operation in progress this write-only diagnostic bit simulates a bad tape error by prematurely setting end-of-record status.

4. MTRD BIT 12 GAP SHUT-DOWN BIT (GSB) - This bit indicates the controller's post-record positioning time period (Main Sequence 2 or 3) to the diagnostic program.

5. MTRD BIT 11 CORRECTABLE PARITY ERROR (CPE) - This bit is true in the Read Mode when a phase encoded tape is being corrected because of a single channel dropout.

6. MTRD BIT 10 IBM PACK MODE - - When this Write/Read bit is set by the CPU, the IBM Pack mode is set, enabling the controller's internal byte swapping circuitry. IBM/industry-compatible tapes may then be read or written by the controller.

7. MTRD BIT 9 EDIT MODE/P.E. IDENTIFICATION (EDIT/IDEN) - When this bit is set by the CPU, the Edit Mode is enabled, issuing the Overwrite command to the tape drive. When read, this bit is true to indicate the Identification Burst of a phase encoded tape is being read by the controller.

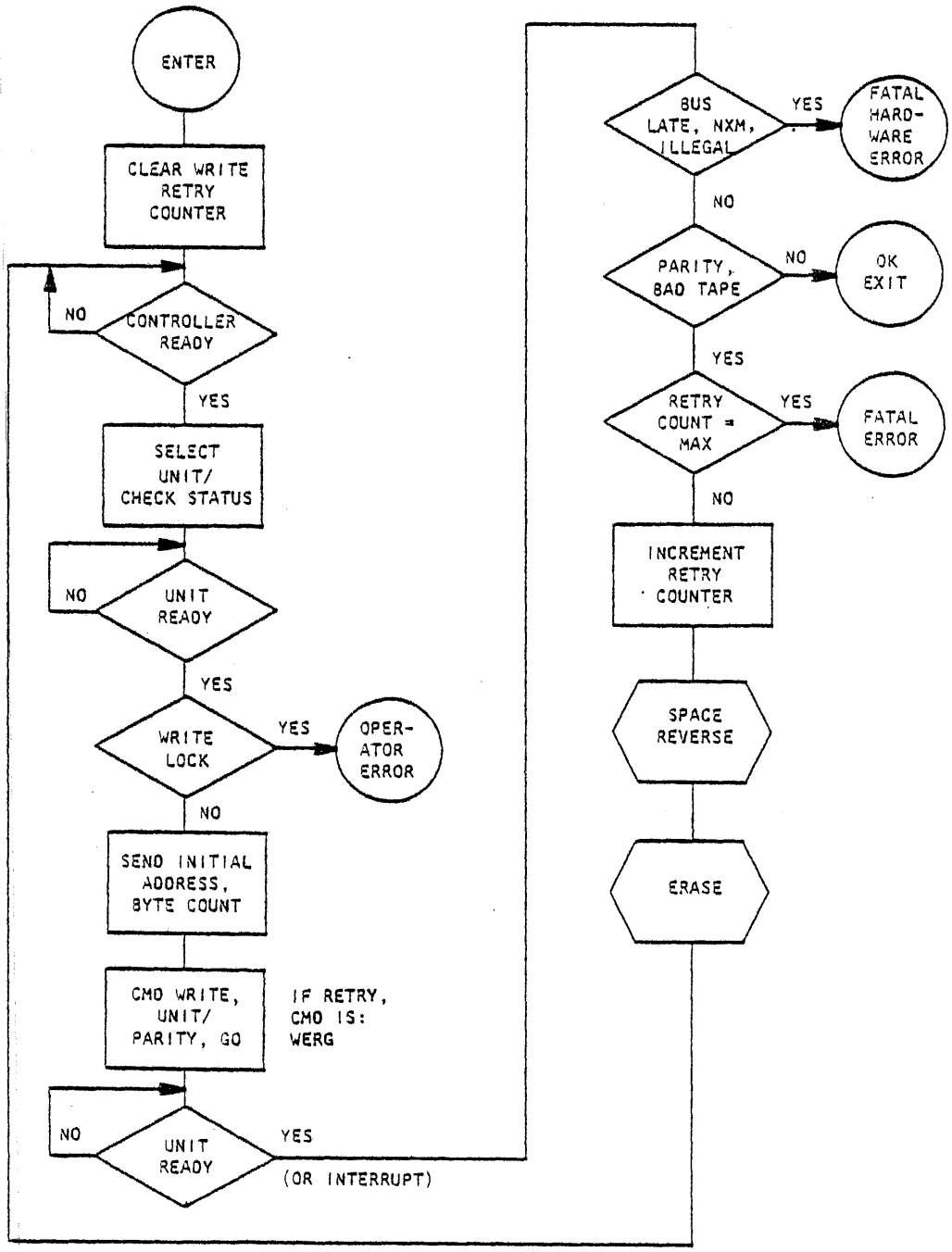


Figure 3-1. "WRITE" Flow Chart

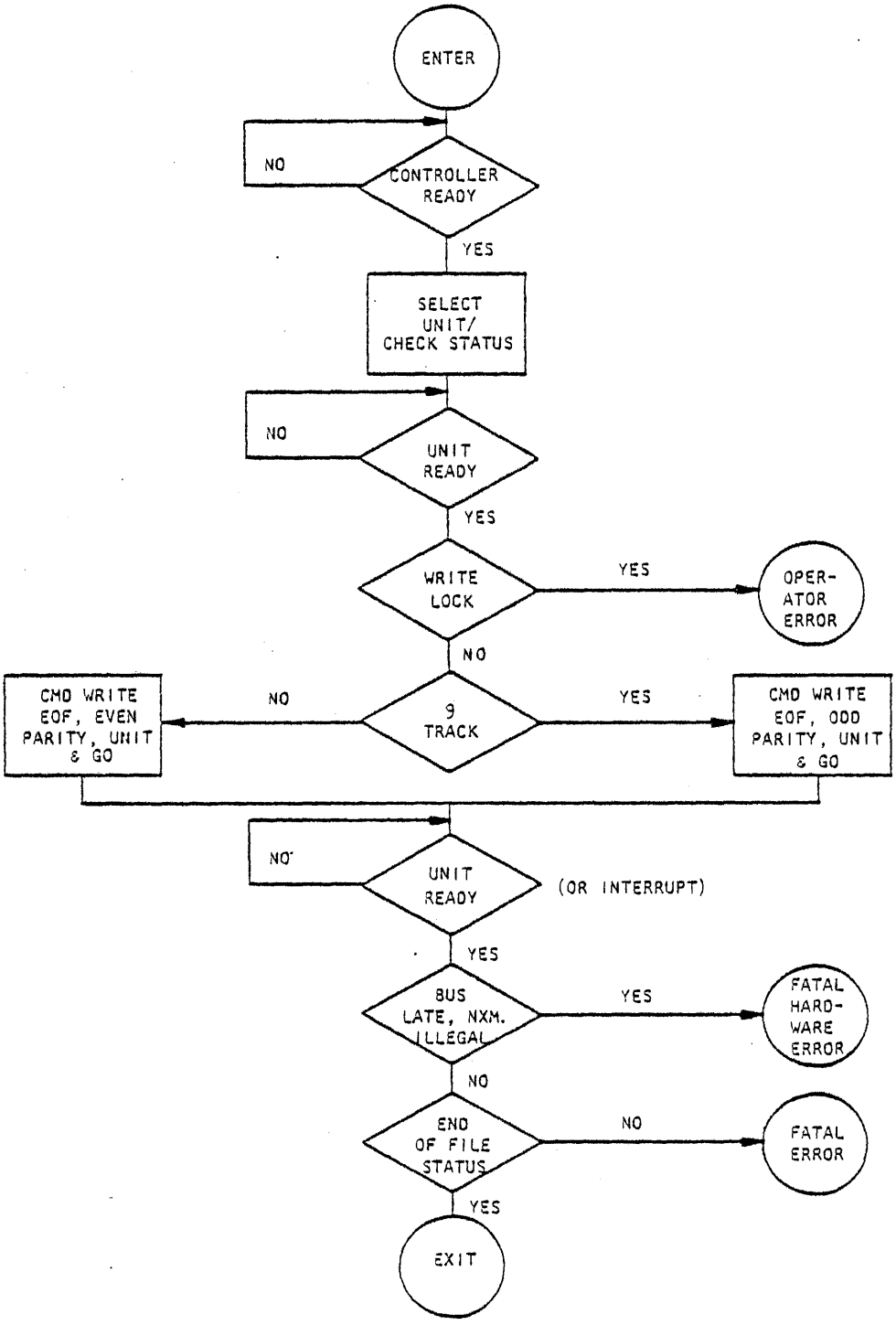


Figure 3-2. "WRITE END OF FILE" Flow Chart

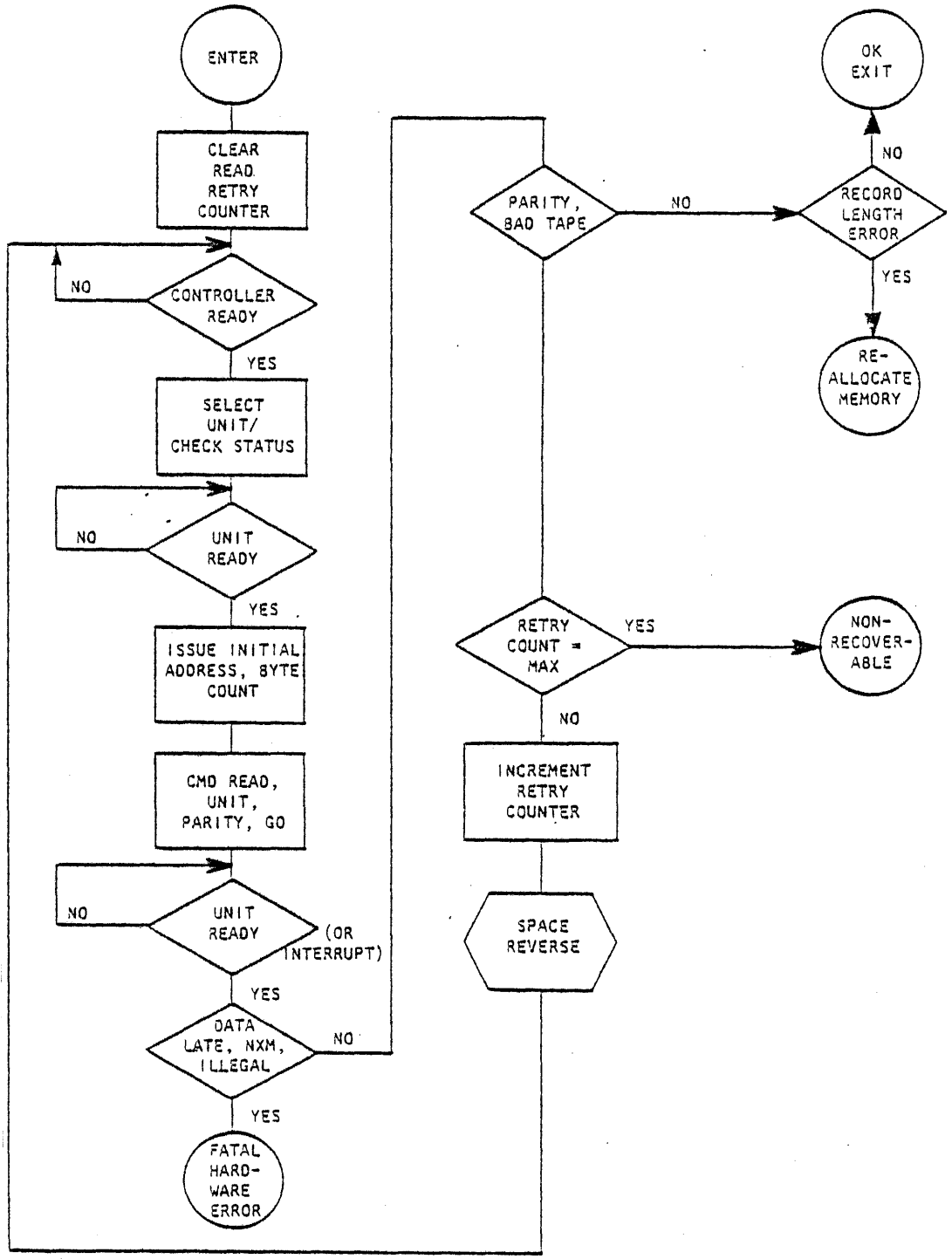


Figure 3-3. "READ" Flow Chart

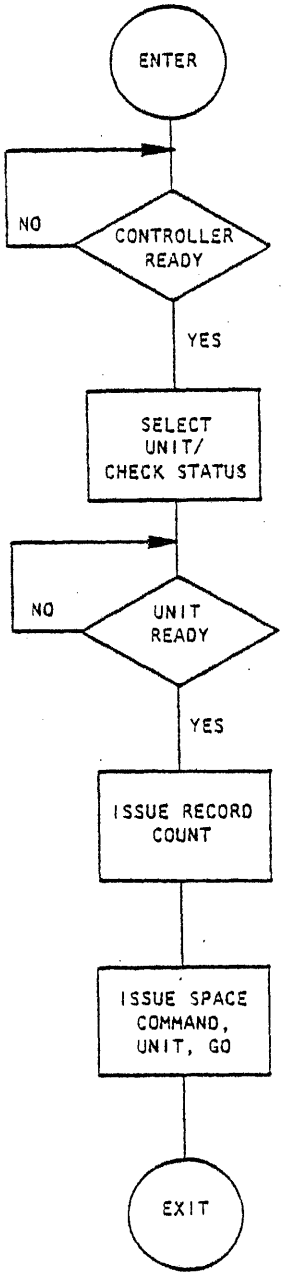


Figure 3-4. "SPACE FORWARD/REVERSE" Flow Chart

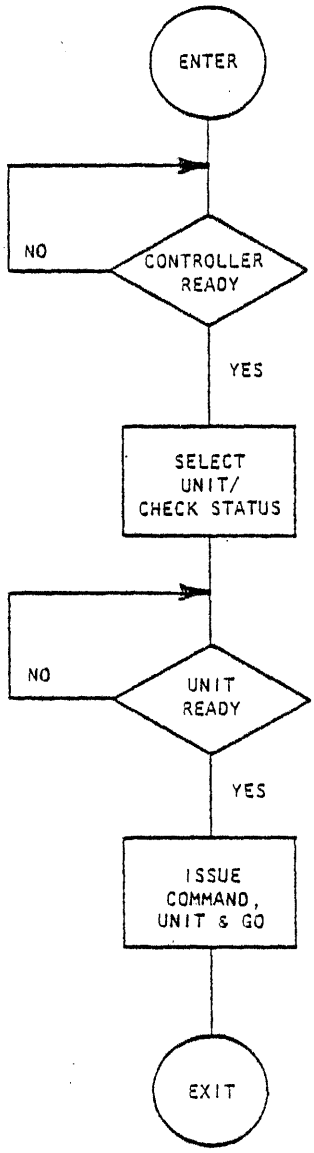


Figure 3-5. "REWIND" Flow Chart

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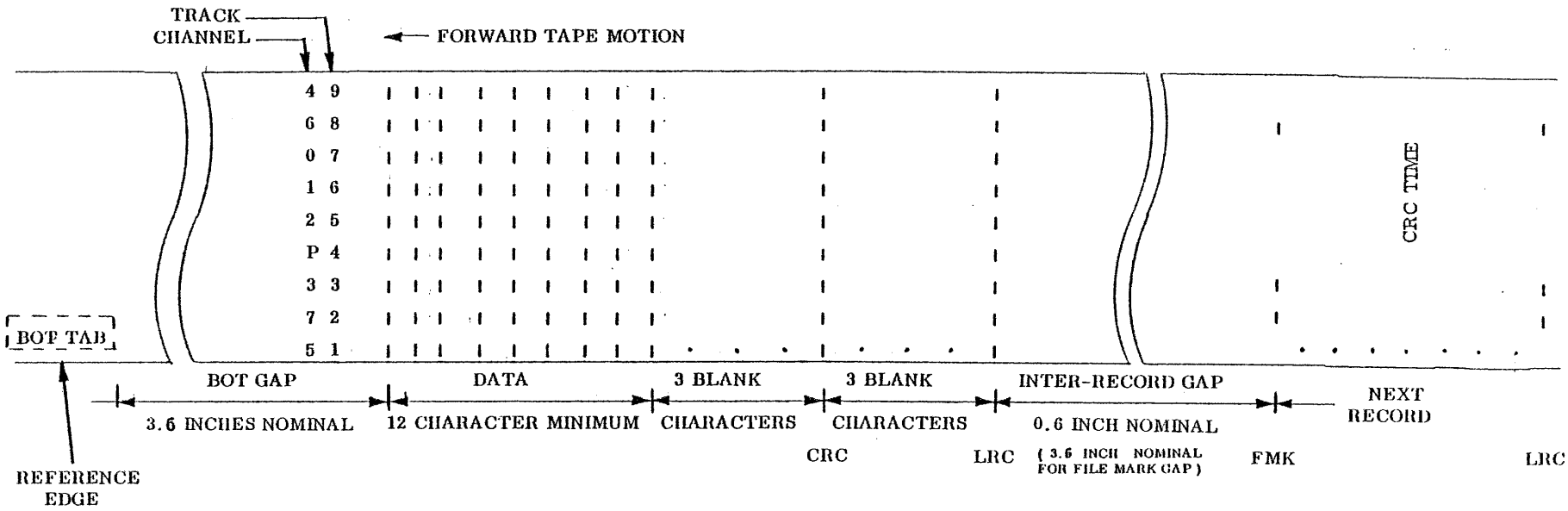
SECTION IV

THEORY OF OPERATION

4.1 TAPE FORMAT

4.2 The Western Peripherals Tape Controller interfaces to industry-standard tape drives which write nine or seven bit characters laterally across the tape. The density of the characters written on the tape is determined by the type of tape drive, the density selection made on the tape drive, and (in some cases) the density selection made in the command issued by the CPU. A data block (record) written on tape consists of data characters and error checking characters (or a preamble and postamble). Every data character consists of the data byte plus a parity bit that is generated by the controller to conform with odd or even parity as specified by the program or the format. A record (or block) of data on tape represents the data transferred to or from a block of memory in one Read or Write operation. The controller separates adjacent records by automatically erasing a 0.6 inch (0.75 inch in 7-track) segment of tape to form an interrecord gap (IRG) between them. The controller always stops and starts the magnetic tape in an interrecord gap.

4.3 NINE-TRACK NRZI FORMAT. As shown in Figure 4-1, each data character contains eight data bits and one odd vertical parity bit. Following the last data character, the End of Record gap (three blank characters) is written, followed by a Cyclic Redundancy Check (CRC) character, followed by three more blank characters, concluded by a Longitudinal Redundancy Check (LRC) character. Following the LRC character, a 0.6 inch IRG is written, in which all nine tracks are erased. The LRC character produces an even longitudinal parity in each of the tracks along the length of the tape. Reading or writ-



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRC AND THE LRC) IS EVEN. IN THE 9-TRACK FORMAT THE LRC WILL NEVER BE AN ALL-ZEROS CHARACTER.
5. IT IS POSSIBLE FOR THIS CRC CHARACTER TO BE ALL ZEROS, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRC. THE CRC CONTAINS ALL ZEROS. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

Figure 4-1 9-Track NRZI Tape Format

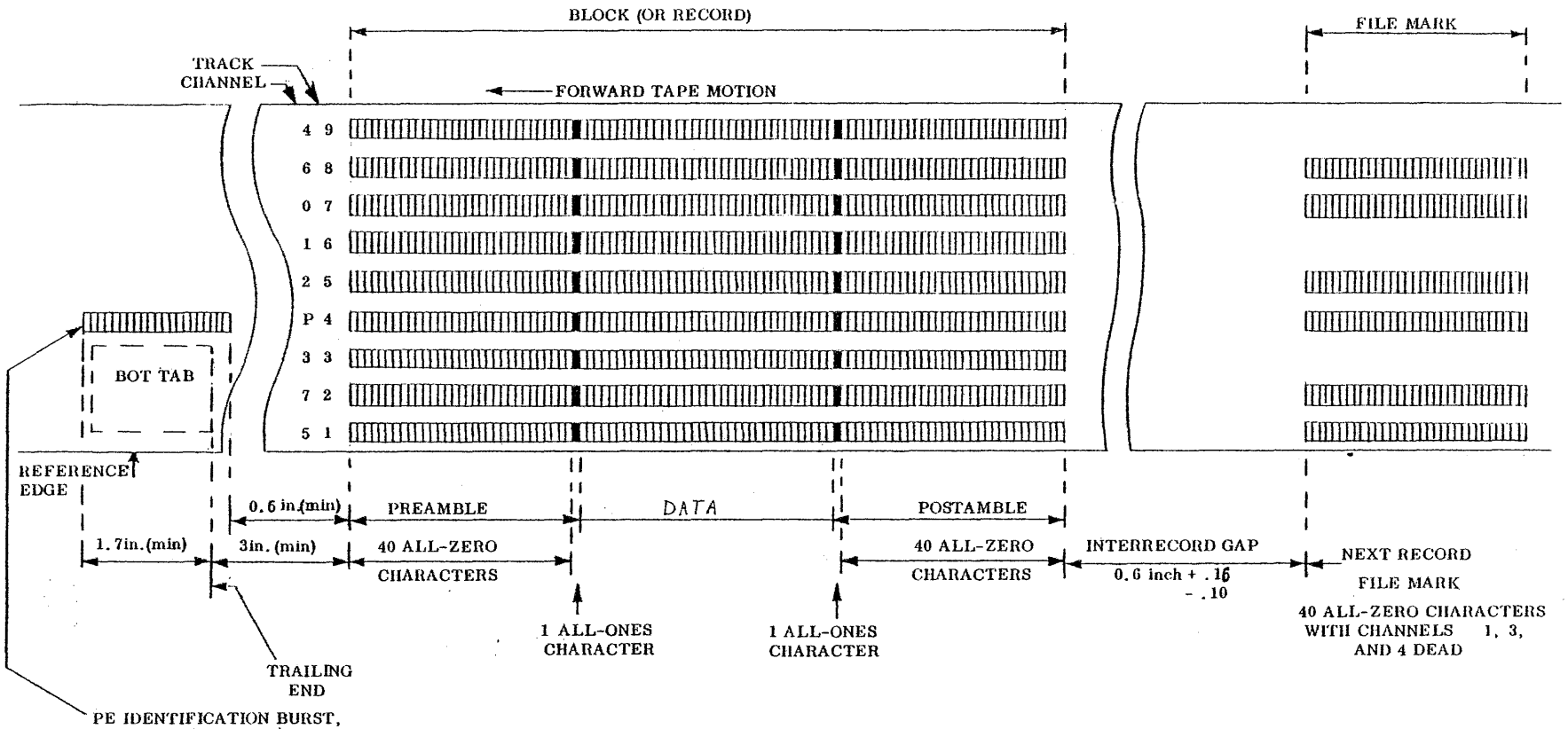
ing, the controller checks to ascertain that the lateral parity of every data character is odd and that every track has even longitudinal parity.

4.4 The 9-track file mark consists of a single character record with a one-bit in channels 3, 6, and 7; the remaining channels contain zeros. The CRC character is left blank, but an LRC character is written which is identical to the file mark character.

4.5 **NINE-TRACK PE FORMAT.** The standard Phase Encoded (PE) 1600 bits per inch format, shown in Figure 4-2, consists of a preamble, a variable length data block, and a postamble. The preamble consists of 40 characters containing zeros in all tracks followed by a character containing ones in all tracks. Each data character contains eight data bits and an odd vertical parity bit. The last data character is followed by the postamble (which is the reverse image of a preamble), an all-ones character followed by 40 all-zeros characters.

4.6 When the tape is at load point (beginning of tape) and the first data block is to be written, it is preceded by an identification burst, consisting of alternate ones and zeros in the parity (P) track, with all other tracks erased. The file mark consists of 40 characters of zero characters similar to those in the preamble, except that channels 1, 3, and 4 are erased.

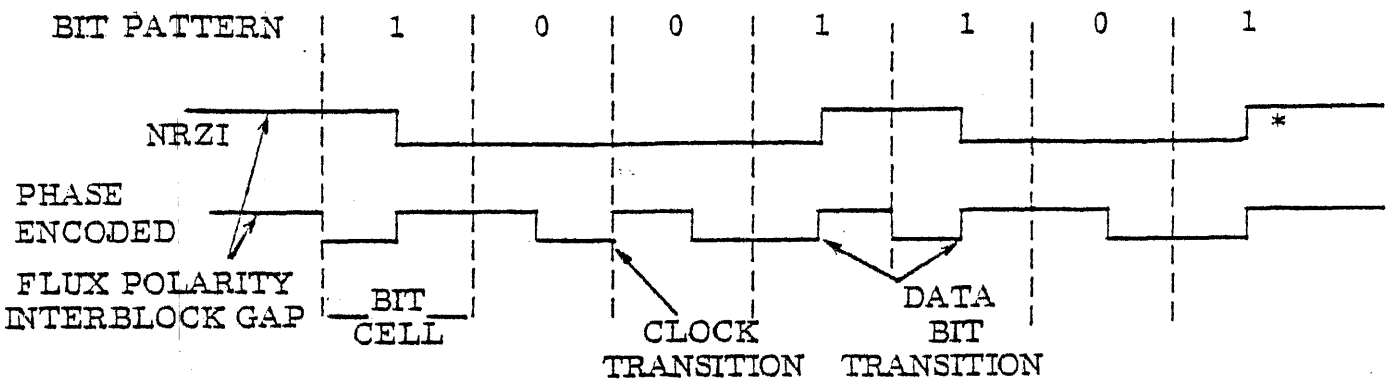
4.7 Phase encoded recording differs from NRZI recording in the recording method as well as the format. In Figure 4-3 NRZI and phase encoded waveforms of similar density are compared. The NRZI waveform shows a change in flux polarity for each binary one bit. A binary zero is represented by the absence of a flux change.



NOTES

1. TAPE SHOWN OXIDE SIDE UP.
2. CHANNELS Ø THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. A FILE MARK IS A 40-CHARACTER PREMABLE BURST WITH CHANNELS 1, 3, AND 4 DEAD. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
5. DATA PACKING DENSITY IS FIXED AT 1600 BITS PER INCH.

Figure 4-2 9-Track PE Tape Format



NOTES:

NRZI--ANY CHANGE IN POLARITY IS A "1" BIT; NO CHANGE IS A "0" BIT.

* LAST CHARACTER IS LRC

PHASE ENCODED--DATA BIT TRANSITION IN DIRECTION OF IBG IS A "1" BIT.

--DATA BIT TRANSITION OPPOSITE IN DIRECTION OF IBG IS A "0" BIT.

Figure 4-3 PE and NRZI Recording Comparison

(Paragraphs 4.9, 4.10, and 4.11 are intentionally missing from this manual)

4.8 Phase encoded recording requires at least one flux change per bit cell. A binary one is represented by a flux change to the flux polarity of the interrecord gap. A binary zero leaves the flux polarized opposite to that of the interrecord gap.

4-9 **MISSING CHARACTERS.** The controller checks for missing characters when reading. Two or more contiguous missing characters will be interpreted as an EOR gap. If this condition occurs in the data portion of the record, Bad Tape Error (BTE) status will be reported.

4.10 **END-OF-FILE MARK.** The program can group sets of data records into files. The end of a file is indicated by an End of File (EOF) mark. The NRZI File Mark is a special record containing one special data character and its LRC. The PE File Mark consists of 40 characters in a combination of active and dead tracks. Each EOF in the NRZI format is preceded by a 3.5 inch IRG. Spacing operations automatically terminate upon detection of the File Mark.

4.11 **TAPE-END MARKERS.** The ends of all tapes contain reflective strips that are detected by photo cells in the transport. The Load Point marker is located at least ten feet in from the beginning of the tape and constitutes the logical Beginning of Tape (BOT). The Space Reverse and Rewind commands automatically stop at this marker. At least three inches of tape intervene between the BOT marker and the first record.

4.12 The end-of-tape (EOT) reflective strip is located at least 14 feet from the end of the tape. The program should not record more than a few feet beyond the EOT marker, leaving at least ten feet of the tape for a trailer. A status bit is set and Space Reverse operations are terminated when the tape passes beyond the EOT marker.

4.13 **RECORD LENGTH.** The minimum record length is two words or four data characters. Maximum length is limited (only by the capacity of the Byte Counter) to 65,536 bytes. When writing, the controller divides each computer word into two data bytes. In reading, the bytes are reassembled into a computer word.

4.14 **EFFECTIVE TRANSFER RATE.** During the actual processing of the data part of a record, the data transfer rate is fixed. However, in a long tape the effective, or average, transfer rate depends somewhat upon record length. Record length determines the percentage of tape taken up by the gaps. At the highest density (1600 bpi) each record gap occupies the space of 960 characters. Figure 4-4 shows the storage capacity of a reel of tape at various record lengths. The effective transfer rate is therefore determined by record length as well as tape speed and density.

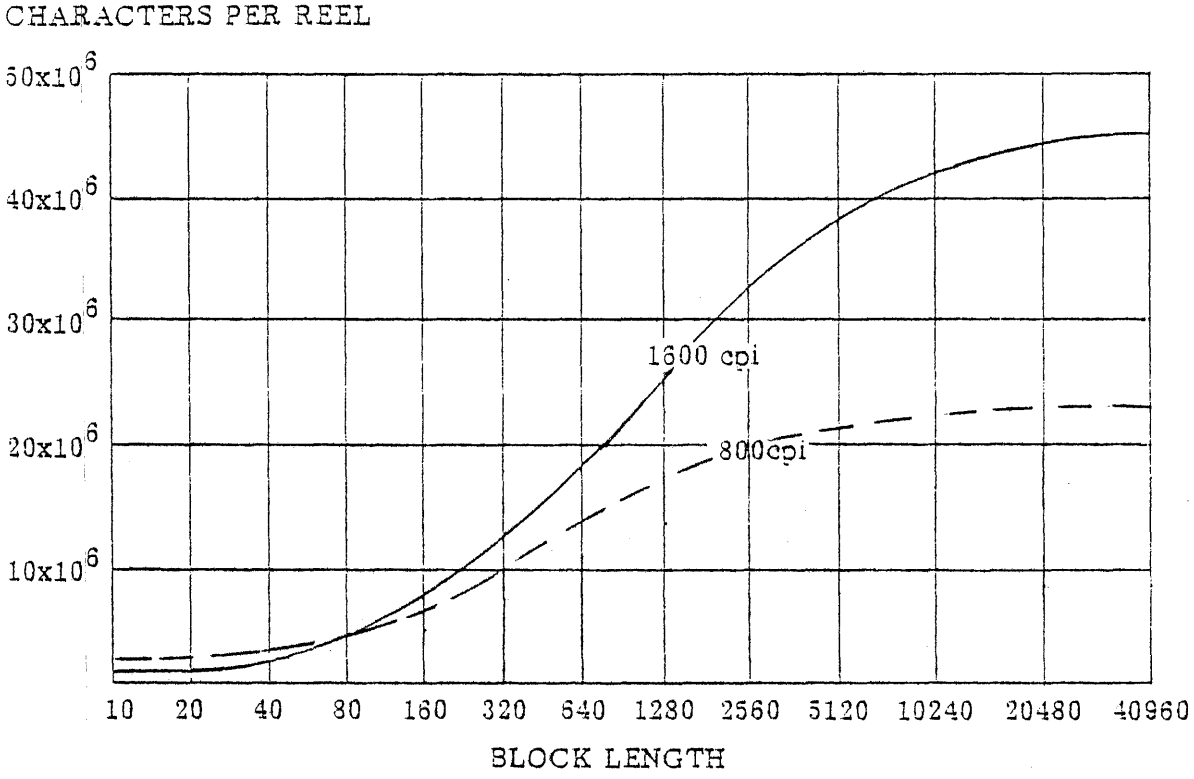


Figure 4-4 Comparison of Packing Density, Phase Encoded and NRZI Formats

4.15 TAPE DRIVE INTERFACE

4.16 INTERFACE SIGNALS. Figure 4-5 shows the signals on the interface between the controller and the tape drives. Table 4-1 lists and describes these signals. The selected tape drive returns status signals to the controller that indicate the type of tape drive, as shown in Table 4-2.

4.17 INTERCONNECTIONS. Three connectors, designated CONTROL, WRITE, and READ, are provided on the controller printed circuit board for making cable connections to the tape drives. Ribbon cable assemblies are provided for each of these three connectors. The other end of each ribbon cable assembly is connected to a connector adaptor assembly (paddleboard). For the WRITE and CONTROL lines, terminators are removed from the tape drives and a termin-

ator chip is installed on the paddleboards in the last tape drive in the daisy chain.

4.18 **DRIVE SELECT LOGIC.** Each tape drive is selected by the controller when its respective select line is activated. Eight select lines are used to control the eight possible tape drives. The active select line is determined by the drive select bits of the Command Register. While the first Control Paddleboard in the daisy chain receives all of the select lines, the propagation of the select lines to the next drive is controlled by the Drive Select Jumper plug.

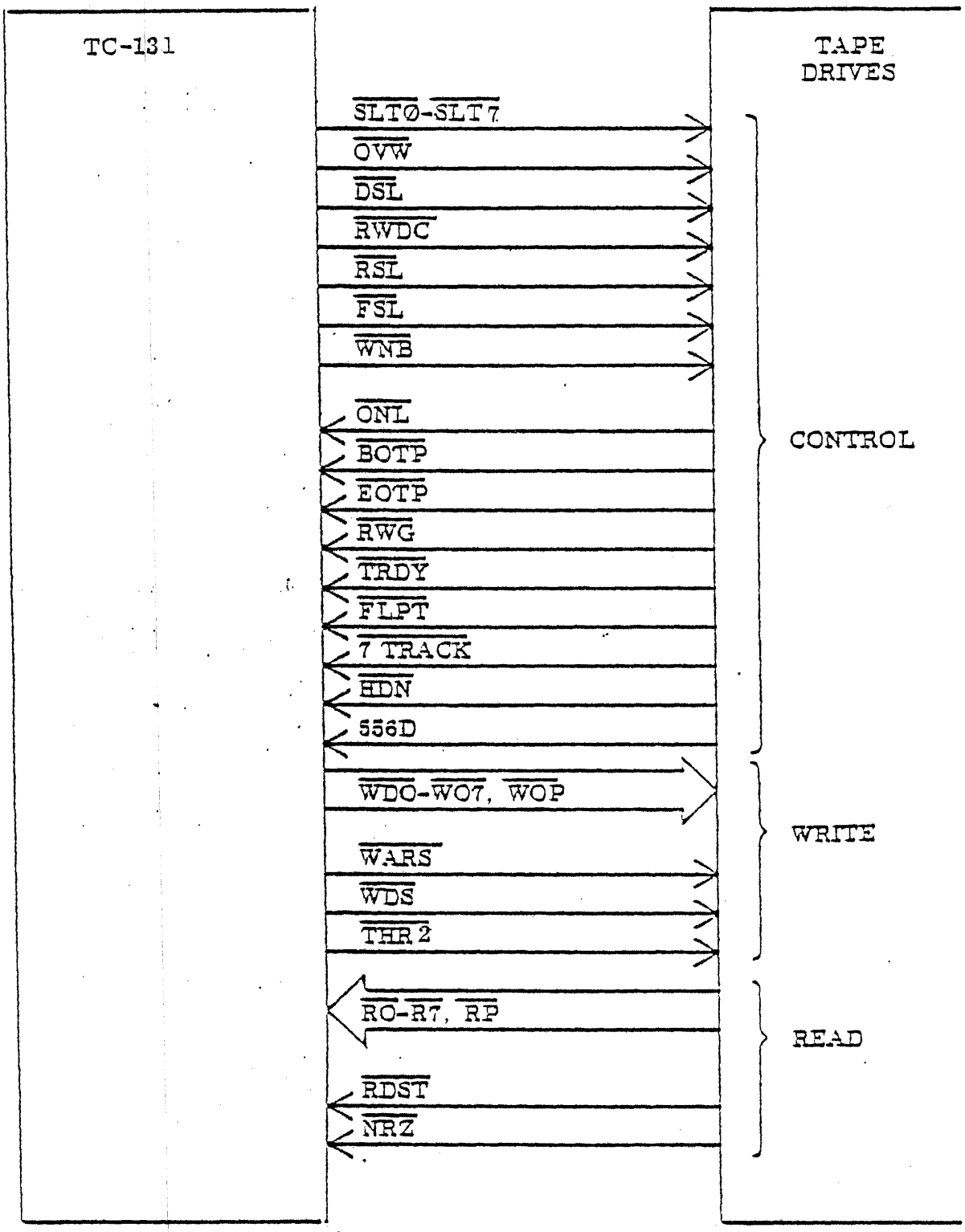


Figure 4-5 Tape Drive Interface

Table 4-1. Tape Drive Interface Signals

MNEMONIC	SOURCE	TERM	COMMENT
CONTROL CABLE:			
SLTØ-7	Controller	Select Drive Ø-7	Tape drive "n" is selected.
WNB	Controller	Write Enable	Enables write operations in selected tape drive.
FSL	Controller	Synchronous Forward Command	The selected tape drive initiates tape motion in the forward direction.
RSL	Controller	Synchronous Reverse Command	The selected tape drive initiates tape motion in the reverse direction.
RWDC	Controller	Rewind Command	The selected tape drive executes a high-speed rewind operation.
OVW	Controller	Overwrite	The edit mode is selected in the selected tape drive.
DSL	Controller	Density Select	When this line is active, high density is selected in the selected tape drive. When the line is inactive, low density is selected.
ONL	Drive	On Line	The selected tape drive is online.
BOTP	Drive	Beginning of Tape	The selected tape drive is at load point.
EOTP	Drive	End of Tape	Tape in the selected tape drive is at the end of tape marker.
RWG	Drive	Rewinding	The selected tape drive is rewinding.
TRDY	Drive	Ready	The selected tape drive is online and ready for operation.
FLPT	Drive	File Protect	The selected tape drive is write-protected so that write operation cannot be executed.

Table 4-1. Tape Drive Interface Signals (cont.)

MNEMONIC	SOURCE	TERM	COMMENT
7 TRACK	Drive	7-Track	The selected tape drive is a 7-track unit.
HDN and	Drive	Density/Tape	Density for 7-track units;
556D		Speed Select	tape speed for 9-track units.
WRITE CABLE:			
WDØ to WD7 and WDP	Controller	Write Data Lines	Tape write data bus.
WARS	Controller	Write Amplifier Reset	Resets tape write amplifiers. Generates LRC character.
WDS	Controller	Write Data Strobe	Strobes tape write data into tape drive.
THR2	Controller	Threshold No. 2 (Not used in this controller)	When this line is active, read threshold No. 2 is selected. When the line is inactive, threshold No. 1 is selected.
READ CABLE:			
RØ to R7 and RP	Drive	Read Data Lines	Tape read data bus.
RDST	Drive	Read Strobe	Strobes read data into the controller.
NRZ	Drive	NRZ	When this line is active from a 9-track drive, it indicates a 9-track NRZ unit; when the line is inactive from a 9-track drive, it indicates a 9-track PE unit.

NOTE: All tape drive interface lines are active low.

4.19 Three kinds of jumper plugs are used: One is for standard drives, one is for drives with drive selection thumbwheel switches, and one is installed in the fourth drive in installations using thumbwheel switches. A standard daisy-chained system is shown in Figure 4-7 where SLT Ø connects to drive Ø, SLT 1 connects to drive 1, etc. Each drive select jumper increments the drive select lines one position so that the next drive in position becomes the next numbered drive. Figure 4-8 illustrates a system using drives with select switches. Four of the select lines are made available to each drive, and the operator selects (with the thumbwheel switch) which select line will activate a particular drive. The operator must ensure that each drive is set to a different number. Caution: A separate installation step is required to connect all four select lines to each drive. Note: Some drive manufacturers mark the thumbwheel switch 1 through 4 for drive selections Ø through 3, respectively, with position Ø sometimes used as an off-line position.

	Status Signal			
Type of Tape Drive	7 TRACK	HDN	556D	NRZ
9-track, Tape Speed A	High	. . .	High	. . .
9-track, Tape Speed B	High	. . .	Low	. . .
9-track, PE (1600 bpi)	High	. . .	. . .	High
9-track, NRZ (800 bpi)	High	. . .	. . .	Low

Table 4-2 Status Signal Indicating Tape Drive Type

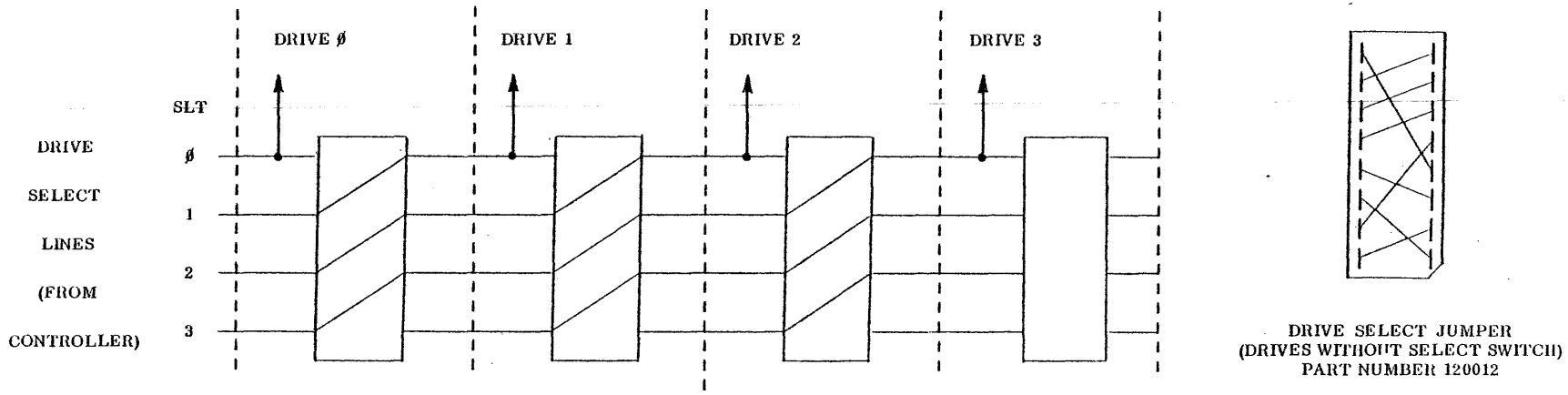


Figure 4-6 Standard Drive Select Logic

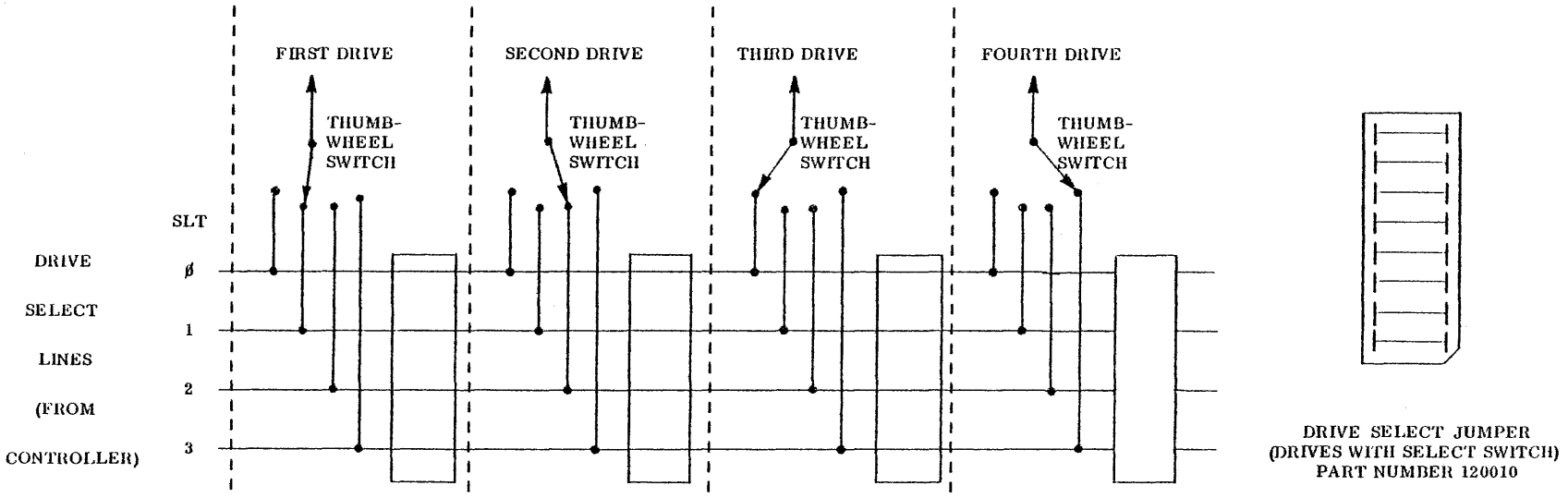


Figure 4-7 Drive Select Logic Using Select Switches

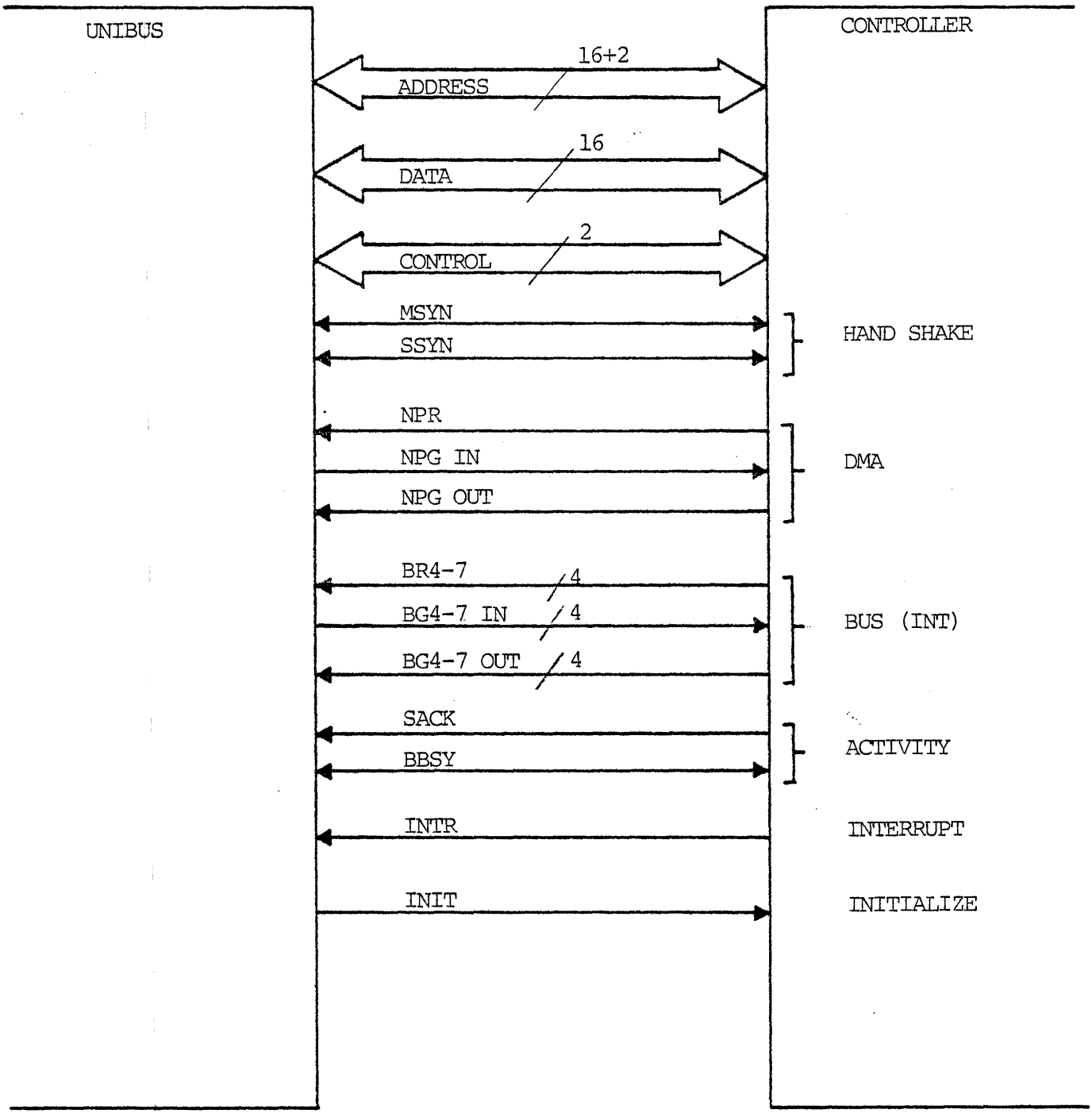
4.20 COMPUTER INTERFACE

4.21 The controller interfaces to the Unibus of the DE PDP-11 computer system. The Unibus is an asyncronous 16-bit data bus with separate address Bus lines. In addition to address and data information, the bus contains signal lines for DMA and Bus Requests, data transfer handshaking, initialization of devices and other miscellaneous control signals.

4.22 BUS INTERFACE SIGNALS (Figure 4-9) The interface signals used by the controller to communicate with the bus are:

1. AØ-A17 (Address lines) - These lines are the 18-line address bus over which memory address and peripheral register address information is communicated. Address information is placed on the bus by the bus master device and received and decoded by the selected slave device. The master device then either receives input data from, or outputs data to the addressed slave device (memory) over the data bus lines. A16 and A17 are referred to as memory expansion bits.
2. DØ-D15, PA, PB (Data and Parity Lines) - These 16 data lines are used to transfer data and register information to and from the controller. The two associated parity lines are not used by the controller. The data lines facilitate transfers of 8-bit bytes as well as full 16-bit computer words.
3. CØ, C1 (Control Lines) - These two lines are coded by the master device to describe the type of transfer:

C1	CØ	OPERATION
Ø	Ø	DATI - Data In (to master)
1	Ø	DATO - Data Out (from master)
1	1	DATOB - Data Out, Byte


UNIBUS
CONTROLLER
16+2
ADDRESS
16
DATA
2
CONTROL
MSYN
SSYN
HAND SHAKE
NPR
NPG IN
NPG OUT
DMA
BR4-7
4
BG4-7 IN
4
BG4-7 OUT
4
BUS (INT)
SACK
BBSY
ACTIVITY
INTR
INTERRUPT
INIT
INITIALIZE

4. MSYN (Master Sync) - This control signal is issued by the master device to indicate that Address and Control information is presented on the bus.

5. SSYN (Slave Sync) - This control signal is issued by the slave device in response to the master device (MSYN or INTR).

6. NPR (Non-Processor Request) - This signal is asserted by the controller to request control of the bus for the purpose of transferring tape data.

7. NPG (Non-Processor Grant) - This signal, daisy-chained through the devices connected to the bus, is generated at the processor in response to NPR. NPG can occur whenever the processor is not using the bus and will be received and regenerated by each device until it reaches the requesting device.

8. BR4-BR7 (Bus Request Lines) - One of these lines will be asserted by the controller to request control of the bus for the purpose of interrupting the processor.

9. BG4-BG7 (Bus Grant Lines) - These daisy-chained lines are asserted by the processor after completing the instruction in progress. Issued in response to the corresponding Bus Reqest line, the Bus Grant will be passed on or regenerated by each device until it reaches the requesting device.

10. SACK (Selection Acknowledge) - This signal is asserted by the controller in response to the processor's NPG or Bus Grant signal, indicating that control of the bus passes to the controller when the current bus master completes its operation.

11. BBSY (Bus Busy) - This signal is asserted by the bus master to indicate the bus is in use. When BBSY goes false, control of the bus is passed to the new bus master.

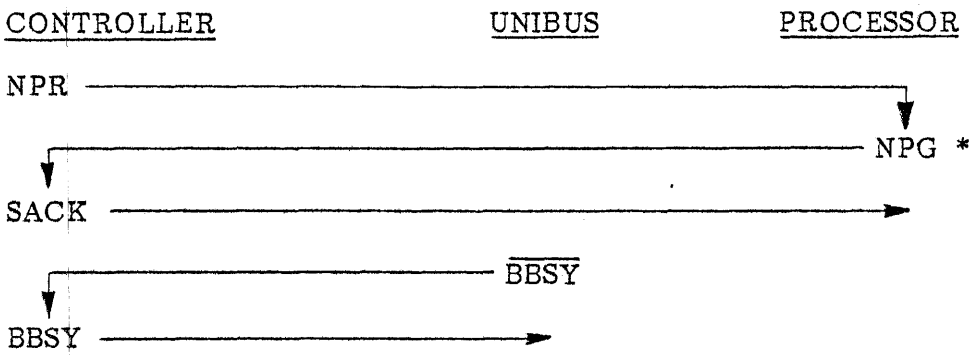
12. INTR (Interrupt Request) - The controller asserts this signal when its Interrupt Enable and Interrupt Request flags are set.

13. INIT (Initialize) - This signal is asserted by the processor to initialize or clear all devices connected to the bus. The signal is generated in response to a power-up condition or for a system reset.

4.23 **BUS OPERATIONS.** The controller receives commands from and provides status information to the processor with the controller being a slave device. After the controller receives the proper commands to trasnsfer data, the controller becomes a bus master device, handling the data transfers directly with the memory, requiring no processor intervention. When the controller has completed all data transfers, it alerts the processor by issuing an Interrupt Request. Devices on the bus are initialized when power is applied or whenever a reset instruction is executed.

4.24 The controller requests a single transfer on the bus by asserting NPR. After completing the current bus cycle, the processor responds by asserting NPG, which allows the controller to become the bus master. It also inhibits initiation of a new bus cycle by the processor.. The controller then asserts SACK and removes NPR causing the processor to terminate NPG. The controller will become bus master when BBSY goes false and it will execute the required data transfer; an input transfer when writing to tape or an output transfer when reading from tape. When the data transfer is completed, the controller relinquishes the bus to the processor by terminating the BBSY signal. The processor then returns to its programmed operations.

4.25 Input operations are used by the processor to receive status information from the controller and are used by the controller when receiving data from memory to be written onto tape. Output operations are used by the



* NOTE: Daisy-chained signal

Figure 4-10 DMA Request/Grant Sequence

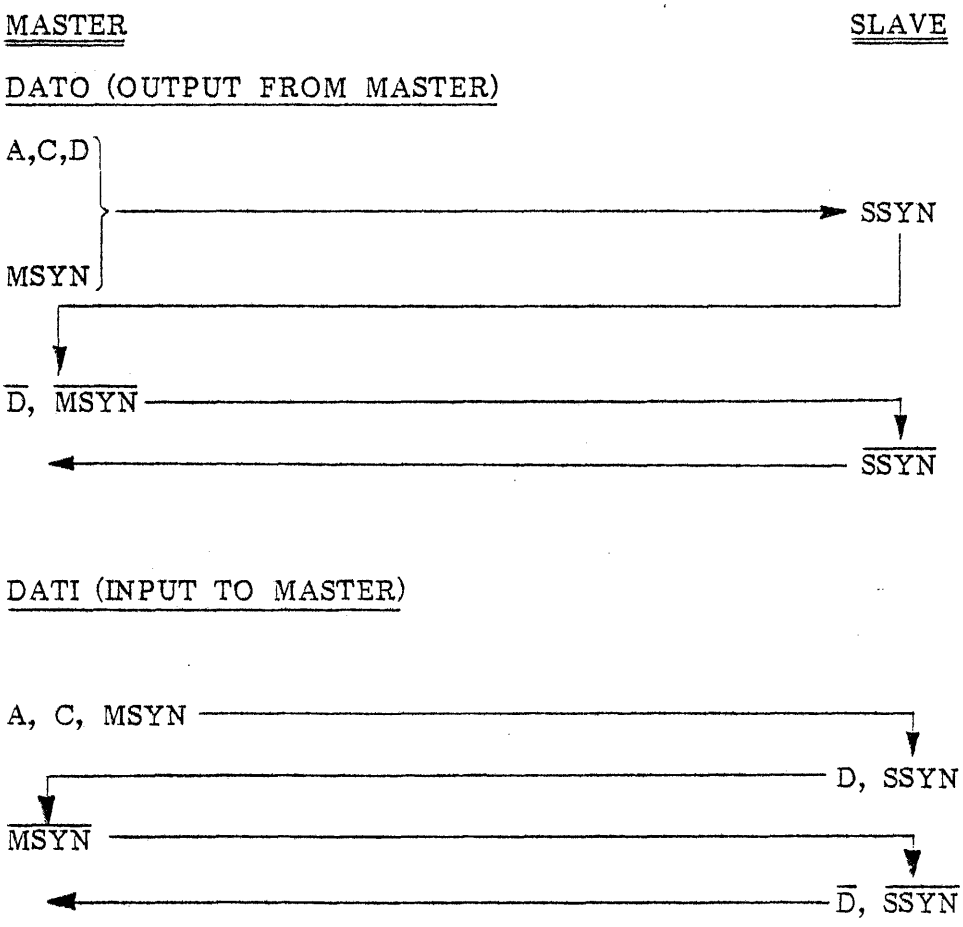


Figure 4-11 BUS TRANSFER SEQUENCE

processor when providing the controller with command information and are used by the controller when transferring information read from tape to the desired section of memory. To begin an input transfer, address, control and MSYN are placed on the bus. The slave device responds with data and SSYN. The master device then receives the data, terminating MSYN, which causes the slave device to remove both SSYN and the data from the bus lines. The BBSY signal is then removed by the master device, terminating the input transfer. For an output transfer, data is placed on the bus by the master device together with MSYN. The slave device accepts the data and acknowledges by asserting the SSYN signal, which causes the master device to remove the data and terminate the MSYN signal. This action by the master device causes the slave to remove the SSYN signal which in turn causes the master to remove the BBSY signal, terminating the output transfer.

4-26 Interrupts are used in the system so that the processor is not burdened with the responsibility of determining when the controller has completed an operation. Interrupt processing allows the processor to continue with its program until alerted by the controller. When enabled in the controller, the Bus Request is issued to the processor upon completion of an operation. If the processor currently is accepting Bus Requests at that priority level, the daisy- chained Bus Grant signal is issued as a response. The Bus Grant signal is passed along by each controller until captured by the requesting device. The interrupting controller will then remove the Bus Request and assert SACK. When the instruction in progress has been completed, further program execution is suspended and the BBSY signal is released, allowing the controller to become bus master. It assets BBSY and INTR and places its hardwired vector number onto the data lines. The vector points to memory locations containing a new processor status word (PSW) and the address of the

interrupt handling routine. The processor saves its current process status work (PSW) and program counter (PC) address and then receives the vector and terminates the SSYN signal. This causes the controller to terminate the BBSY and INTR signals and remove the vector from the bus. The processor will then enter the controller's interrupt service routine to handle the interrupt.

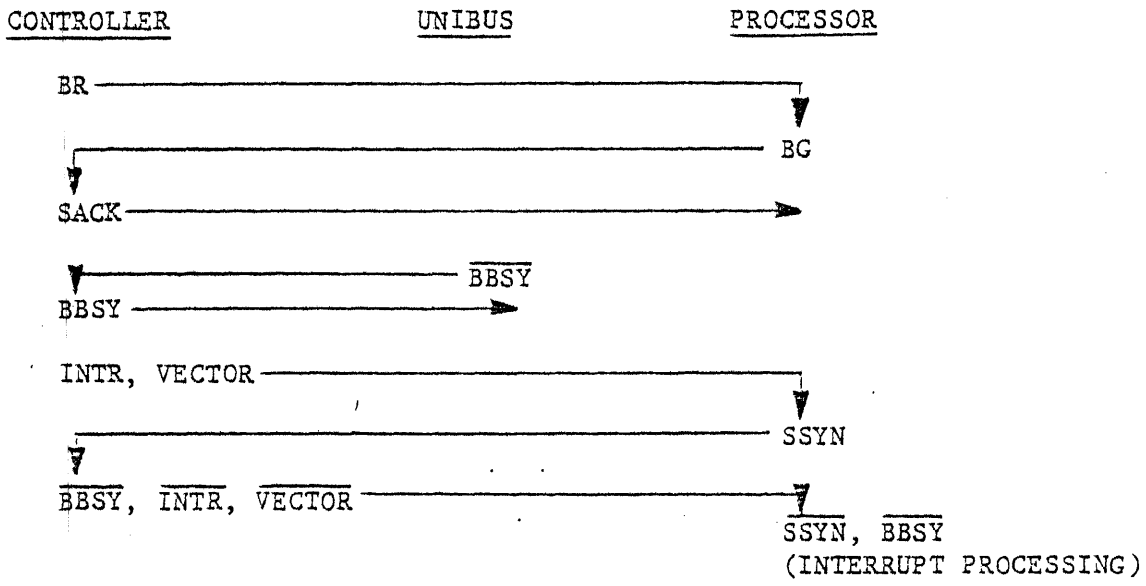


Figure 4-12 Bus Request/Interrupt Sequence

4.27 FUNCTIONAL CONTROLLER ORGANIZATION

4.28 The controller hardware can be logically divided into four sections; tape interface, phase encoded data recovery, microprocessor, and computer interface. Each area will be discussed separately. A block diagram of the controller is shown in Figure 4.13

4.29 TAPE DRIVE INTERFACE

4.30 The Tape Drive Interface consists of all logic directly associated with controlling the tape units excluding the PE Data recovery logic. Refer to Figure 4.14 for a block diagram of this section. All tape motion is controlled by the microprogram loading the tape unit command register. Another microprogram loadable register drives a decoder to generate the eight unit select lines. The write data register is a 9 Bit microprogram loadable register. The first 8 Bits correspond to the data byte and the ninth bit is the vertical parity bit. The parity bit is loaded when the write data register is loaded and is generated by a parity generater monitoring the nine LSB's of the DBUS. The microprogram has the control to load the parity register directly from the DBUS for writing characters which do not require parity (e.g. CRCC, EOF, PE preamble, etc.).

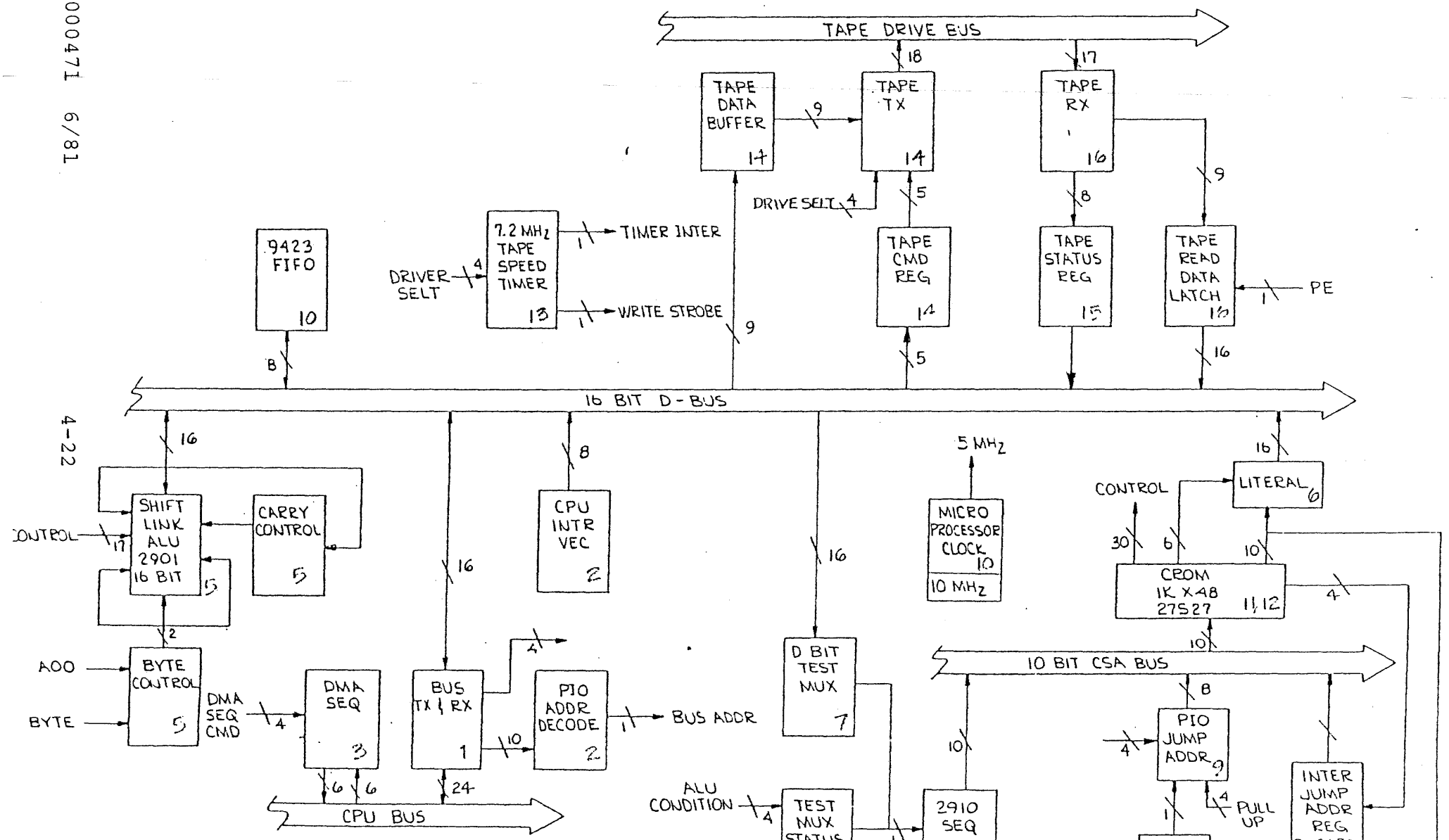


FIGURE 4-13 CONTROLLER BLOCK DIAGRAM

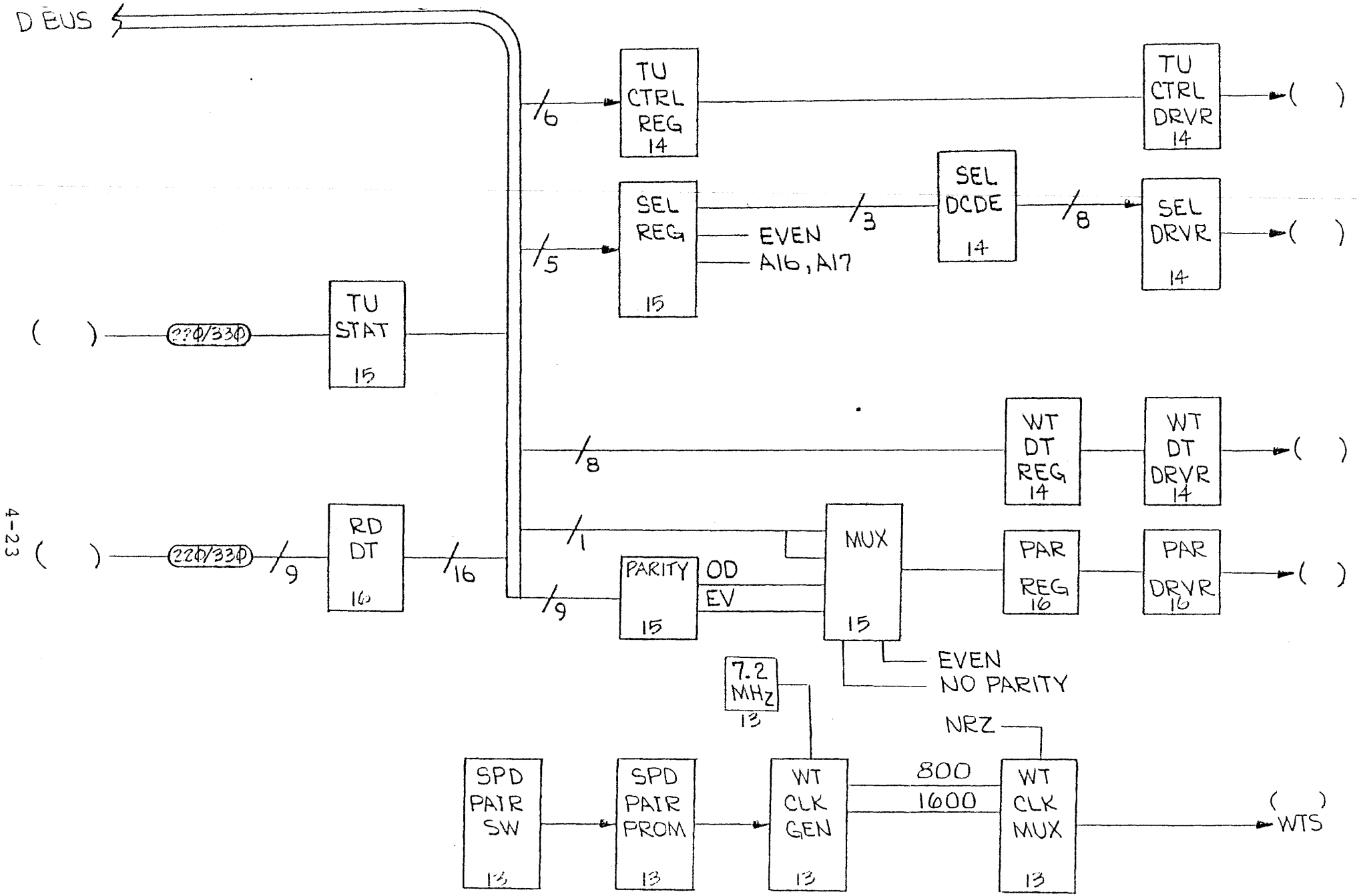


FIGURE 4-14 TAPE UNIT CONTROL

4.31 On the input side, the microprogram has access to the tape unit status and the read data. The read data register in NRZ is 9 Bits of data and parity with the remaining bits always a 0. In PE, the parity bit is extended throughout the upper byte to facilitatew an all ones character recognition. The same parity generater is used to check the read data parity as it is moved across the DBUS.

4.32 Write Data Strobes are generated in the hardware and enabled by the microprogram. The write data frequency is derived from a 7.2 MHZ oscillator driving a counter divider chain preset by the speed pair select PROM. The counter chain produces an 800 and 1600 BPI clock at the selected speed. Two interrupts are generated: the timer, and (when WGATE is set) the write strobe. The write data strobe interrupt signals a request for new data in the write data register. The timer is always the 800 CPI clock and is used for up/down ramp timing, tape gap and IRG timing.

4.33 PHASE ENCODED DATA RECOVERY

4.34 The PE data recovery logic is the largest, most hardware intensive section in the controller. The large amount of hardware is required because each read channel operates independently, requiring individual data recovery logic for each of nine channels. For proper tracking of

the read data and to eliminate changing components for the five speeds supported, four sphase lock loops are used. No component changes or adjustments are required to change speeds; all selection information is received from the speed pair PROM. The remaining logic is involved in initiating a PE read operation or in generating status. Refer to Figure 4.15 for a block diagram of the PE data recovery logic.

4.35 PE ACTIVE CONTROL. A PE read operation is started by the microprogram setting the RDGATE latch. The PE control logic then monitors channel 2 and the parity channel for activity. After several transitions in either or both channels has been detected, the read channel decoders are enabled by LOCKENA. The control logic continues monotoring the data and, after some additional time, LOCKED is generated indicating that all channels should have acquired data by this time. If a channel has not locked on, it should dropout immediately, assuminga dead channel status. The control logic also generates a signal (no data) indicating the IRG has been encountered when no more data is detected in the two channels being monitored.

4.36 PE DATA CHANNEL. Refer to Figure 4.16 for a block diagram of a typical channel. When a read channel is enabled it assumes the incoming data is the all zeroes

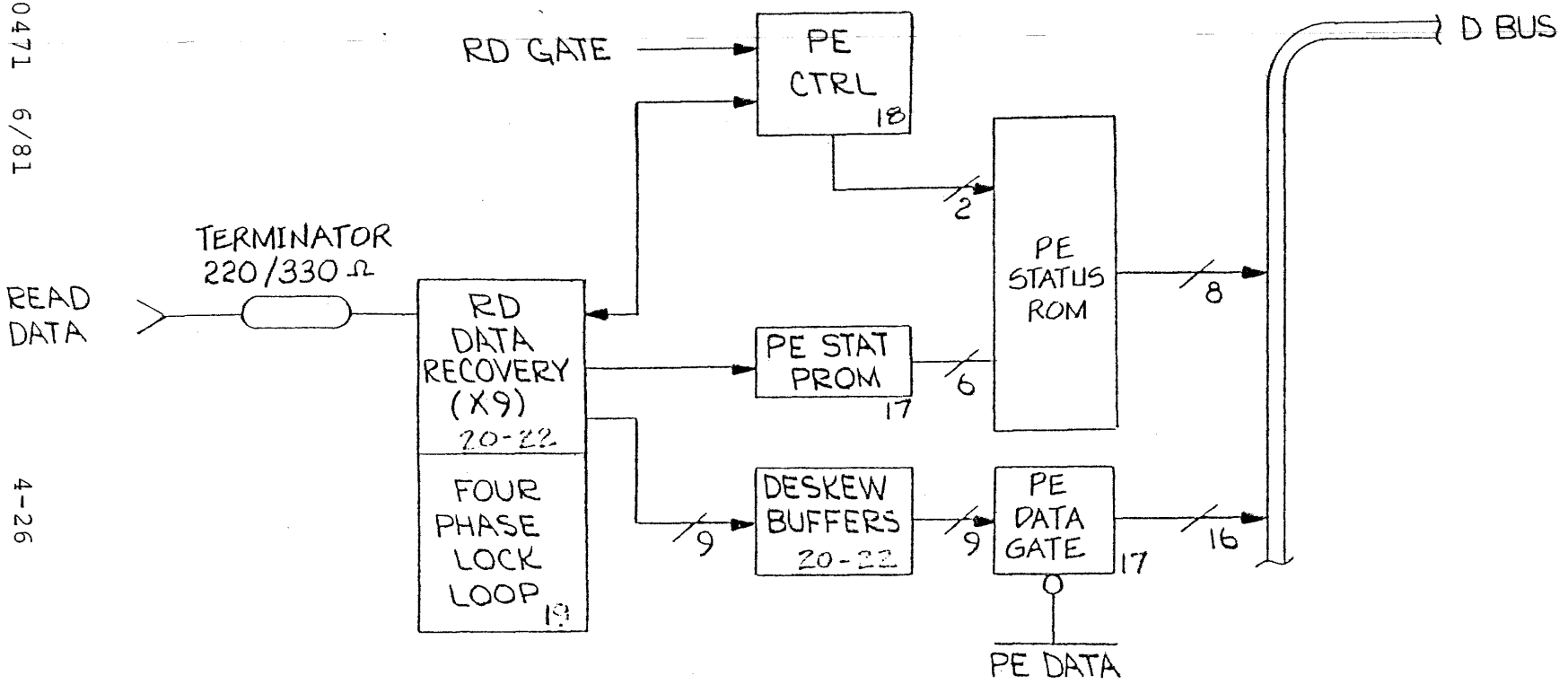


FIGURE 4-15 PHASE ENCODED DATA RECOVERY SECTION

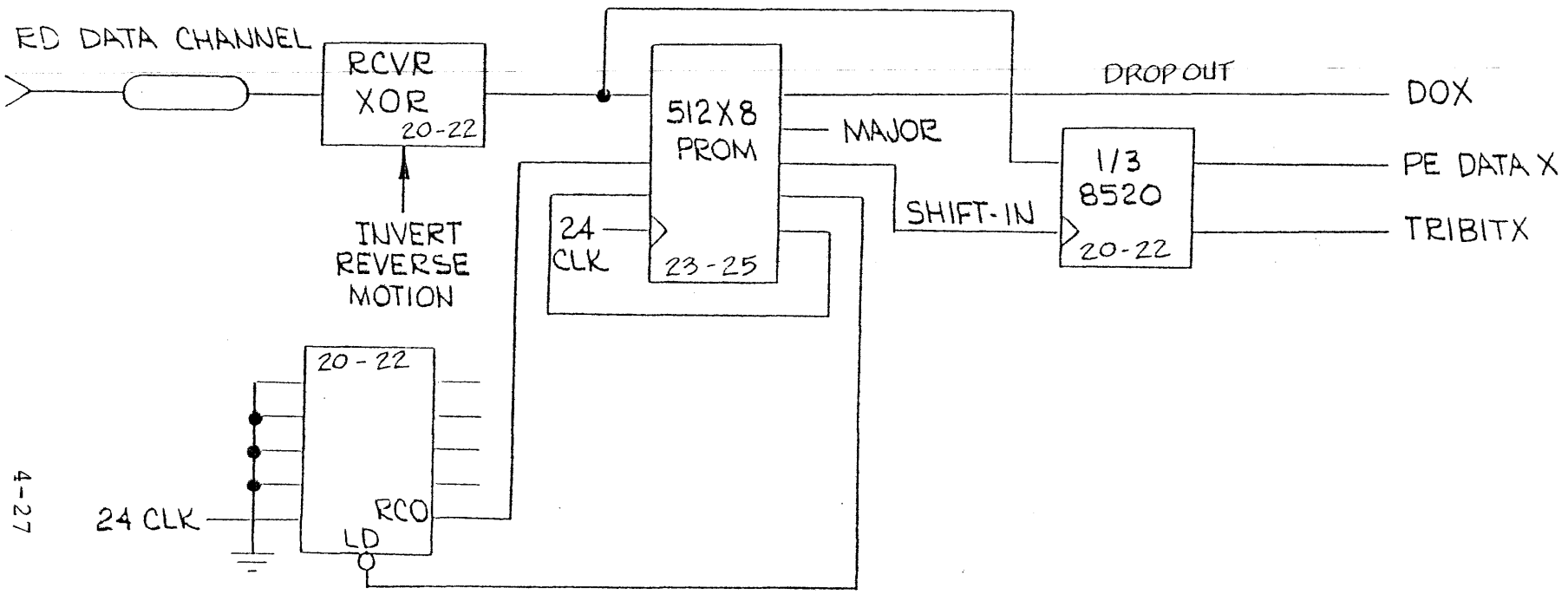


FIGURE 4-16 PE DATA CHANNEL

preamble and a high to low transition on the read data lines is the major transition of a zero bit. If a zero transition is not detected by the time the LOCKED signal is received the channel will dropout and start a continuous stream of Shift In signals to the deskew buffer to allow it to function properly. Once a zero is found, the channel logic advances to state one and begins looking for a one's transition to mark the beginning of the data portion of the record. Once detected the logic advances to state two and generates a Shift In to the deskew buffer for each major transition. The channel logic has stripped off the preamble and the sync byte in states 0 and 1 once state 2 is reached no futher data processing takes place. The channel will continue until a dropout occurs and then will force feed the deskew buffer until disabled.

4.37 PHASE LOCK LOOP. The phase lock loop is used to track the incoming read data to eliminate waveform distortion introduced by long or short term speed variations in tape motion. Four independant PLL's are used to support the five speeds, with one of the slower speeds handled by inserting an additional divide by two stage. The output of the PLL is a clock 24 times the data rate. Refer to Figure 4.17 for a block diagram of the PLL section. The PLL consists of a phase detector, an amplifier/low pass filter, a VCO, and a divide by 24 block.

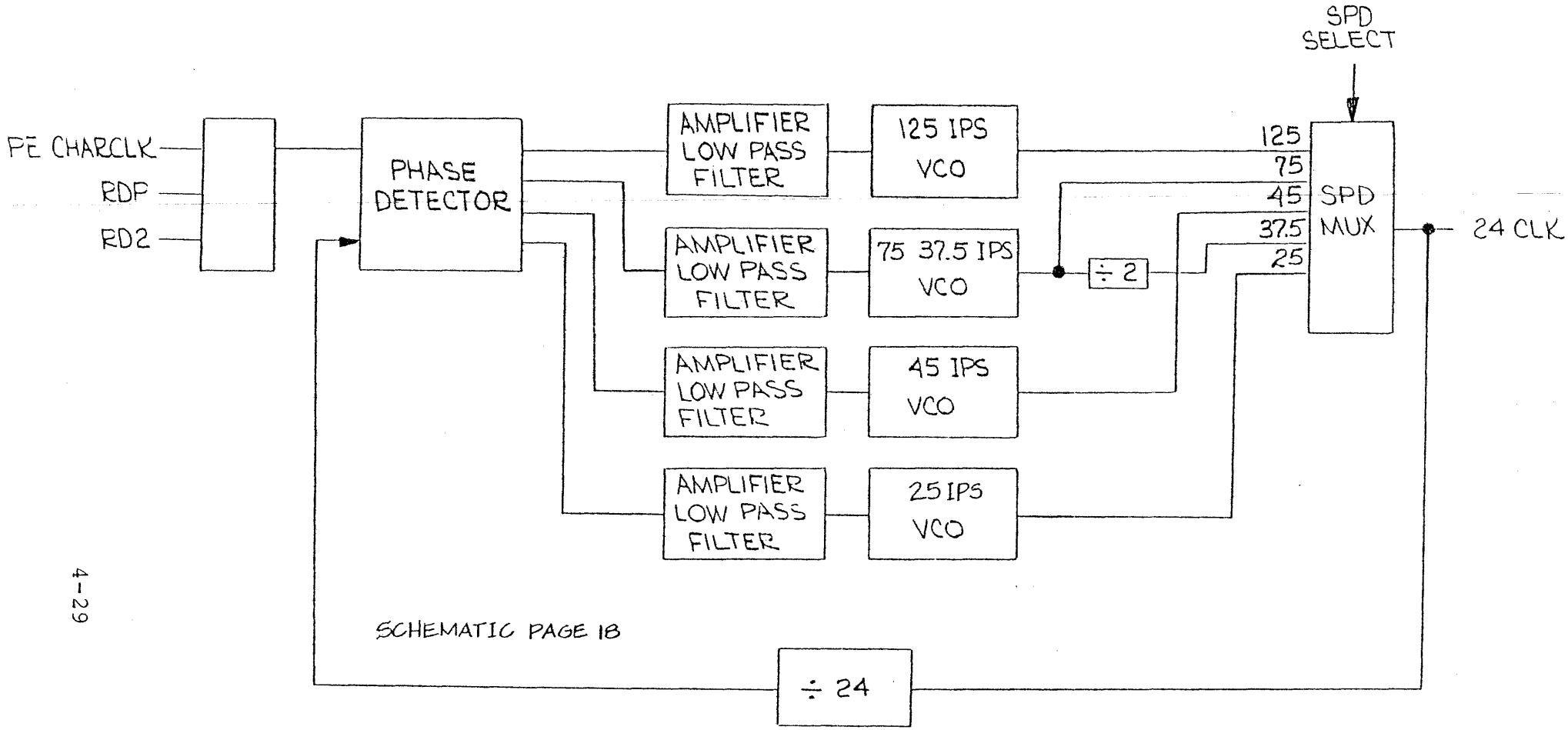


FIGURE 4-17 PE PHASE LOCK LOOP

The phase detector and the divider are common to all loops since thses elements are essentially frequency independent. The VCO and amplifier/low pass filter are unique because of the different VCO center frequencies and low pass filter components to establish the desired dynamic characteristics of the loop. The output of each VCO enters a multiplexer which is controlled by the speed pair PROM, thus only the loop of the selected speed is closed. The PLL tracks the PE character rate clock from the write strobe clock generater until the LOCKED signal is generated and the read data replaces the character clock.The PLL tracks the parity channel unless it drops out, then the PLL will track channel two.

4.38 PE STATUS. The PE status is generated from the drop out condition of all channels. A 512 by 8 prom monitors all nine channels and from the pattern of the drop outs can determine: Single Channel Drop Out, Multiple Channel Drop Out, All Channels Dropped Out, File Mark, and ID Burst.

4.39 MICROPROCESSOR

4.40 The heart of the controller is a high performance 16 bit 2901 bit slice microprocessor coupled with the 2910 micro-program address sequencer. The micro-processor can be micro-processor can be considered two closely coupled processors; a data processor, the 2901, and an address

processor, the 2910. The micro-processor uses a conventional single-level pipeline architecture with a cycle time of 200 nsec, yielding an execution rate of five million instructions per second. The micro-program resides in a 1024 by 48 control store consisting of twelve high speed 512 by 8 registered PROMS.

4.41 Data Processor. The data processor consists of the four 2901's and the control logic for external data sources and destinations. Refer to Figure 4.18A for a block diagram of the data processor.

4.42 The central component of the data processor is the data bus (DBUS) which is 16 bits wide and is used for all data movement within the controller. The microinstruction has two fields of four bits each for controlling the sources and destinations of data on the DBUS. Two additional bits are used, one for enabling the 2901 and the other for placing a 16 bit literal on the DBUS. The external source field and the 2901 A port address overlap in the microinstruction. The external source field is only three bites allowing any source to overlap with two 2901 registers. The external destination field and the 2901 B port address overlap in the microinstruction. Another bit from the microinstruction is used to enable external destination. The external destination field is only three

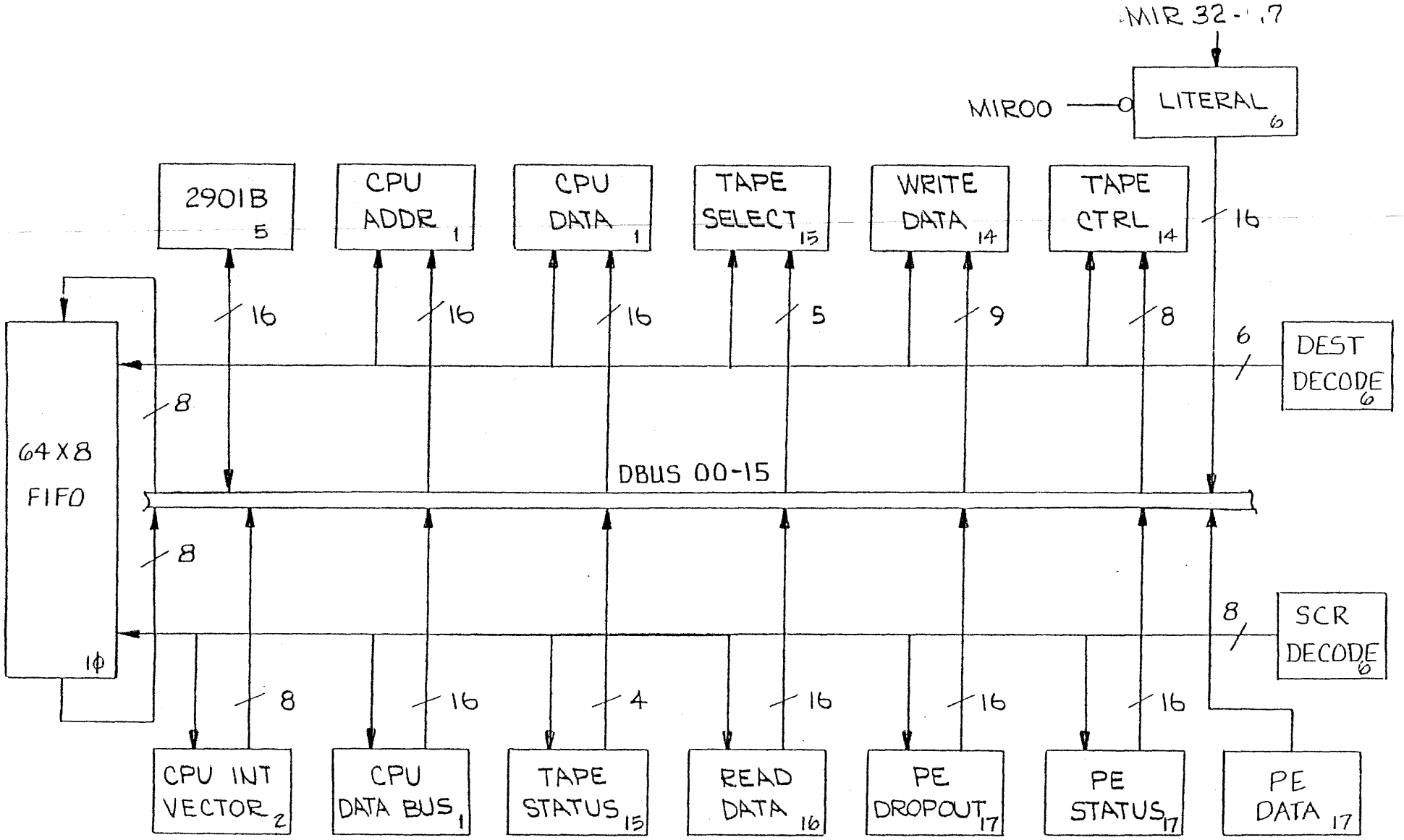


FIGURE 4-18A DATA PROCESSOR

bits allowing any destination to overlap with two 2901 registers.

4.43 MICROPROGRAM ADDRESS PROCESSOR

4.44 The microprogram address processor consist of the 2910 and the associated logic directly used in arriving at the effective address for the current microinstruction. Refer to an AMD specification for the 2910 to understand all the address control available. The microprogram address has three direct sources, the 2910, the PIO vector, and the microinterrupt vector file. Refer to Figure 4.18 B for a block diagram of this section.

4.45 The 2910 is the usual source for the microprogram address. Within the 2910 there are four sources of the address; the direct inputs from the microinstruction the program counter, the stack, and the register/counter. Since the four bits of 2910 instruction come directly from the microinstruction all of the 2910 commands are available. The 2910 instruction field overlaps the data processor's literal filed, therefore when a literal is used only a continue or return instruction is available. Seven bits in the microinstruction are used for controlling cpnditional 2910 instruction execution. MIR27 controls whether or not the 2910 instruction will be conditional and

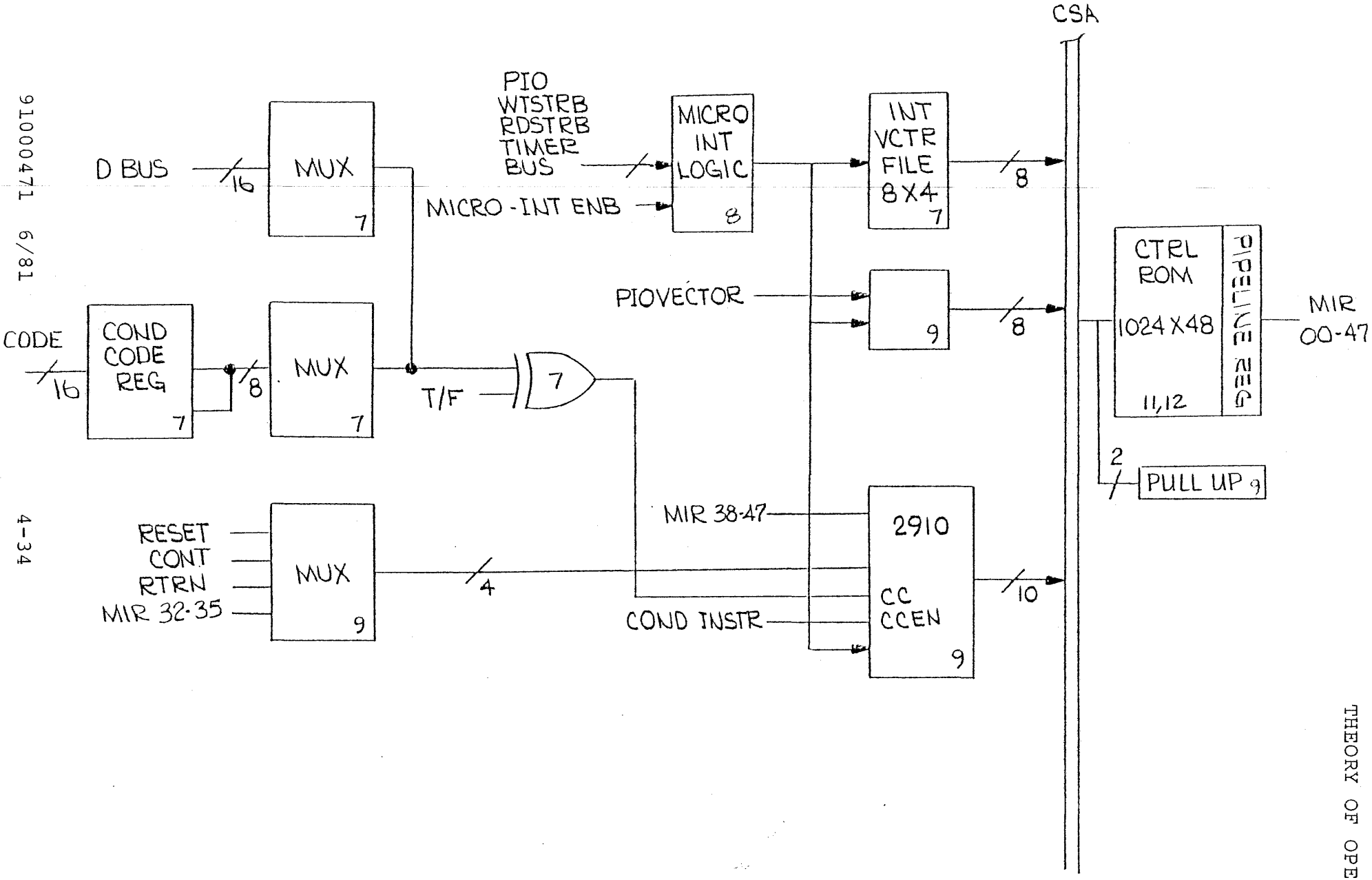


FIGURE 4-18B MICROPROGRAM ADDRESS PROCESSOR

MIR26 determines the true/false sense of the conditional test. MIR25 selects DBIT TEST over condidtion code test. A four bit field, MIR28-31, selects one of 16 conditions codes or one of the bits on the DBUS for testing.

4.46 The second and third sources of microprogram address are the result of one of the five microlevel interrupts. All interrupt vectors are 8 bits wide with the two remaining address lines pulled-up, forcing all interrupts in the range of 300-3FF. PIO interrupts are in the range of 3F0-3FF.

4.47 When the controller's device address is detected by the Unibus sequencer, it generates an interrupt which is processed when microlevel interrupts are enabled and that interrupt has priority. The interrupt vector constructed gives a unique entry point for each TM11 register and whether the register is to be read or written.

4.48 The second interrupt source is the interrupt vector file. The vector file is 8 bits wide and four words deep providing one programmable vector for each of the remaining interrupts. This file provides 256 entry points for the four interrupts, thereby minimizing the overhead to determine the action required when an interrupt occurs.

4.49 UNIBUS INTERFACE

4.50 The controller interfaces to the Unibus through a standard SPC SLOT. DEC Unibus compatible 2908 and 8641 transceivers, 8640 receivers and 7438 drivers are used in the bus interface. The controller interface presents one unit load on the Unibus. Refer to Figure 4.19 for a block diagram of the Unibus interface.

4.51 ADDRESS TRANSCEIVERS AND DECODING. Five 2908's are used to transmit and receive the 18 bits of Unibus address. The transmitter register is loaded from the internal DBUS and is used only during NPR operation. The receiver latch is always in the transparent mode to allow continuous monitoring for the controllers device address. Address recognition is the result of bits A13-A17 and A04 being set and bits A05-A12 matching the device address switches. Bits A01-A03 select the TM11 register and A00 selects the high or low byte. Device address recognition with MSYN generates a micro-level interrupt vectored to hex address 3FX. The offset "X" is defined by A01-A03 and the direction control, C1. Thus, PIO (Programmed Input-out) read operations cause micro-level interrupts to locations 3F0-3F7 and PIO write operations to locations 3F8-3FF. Write byte operations are handled by controlling the clock to the 2901's.

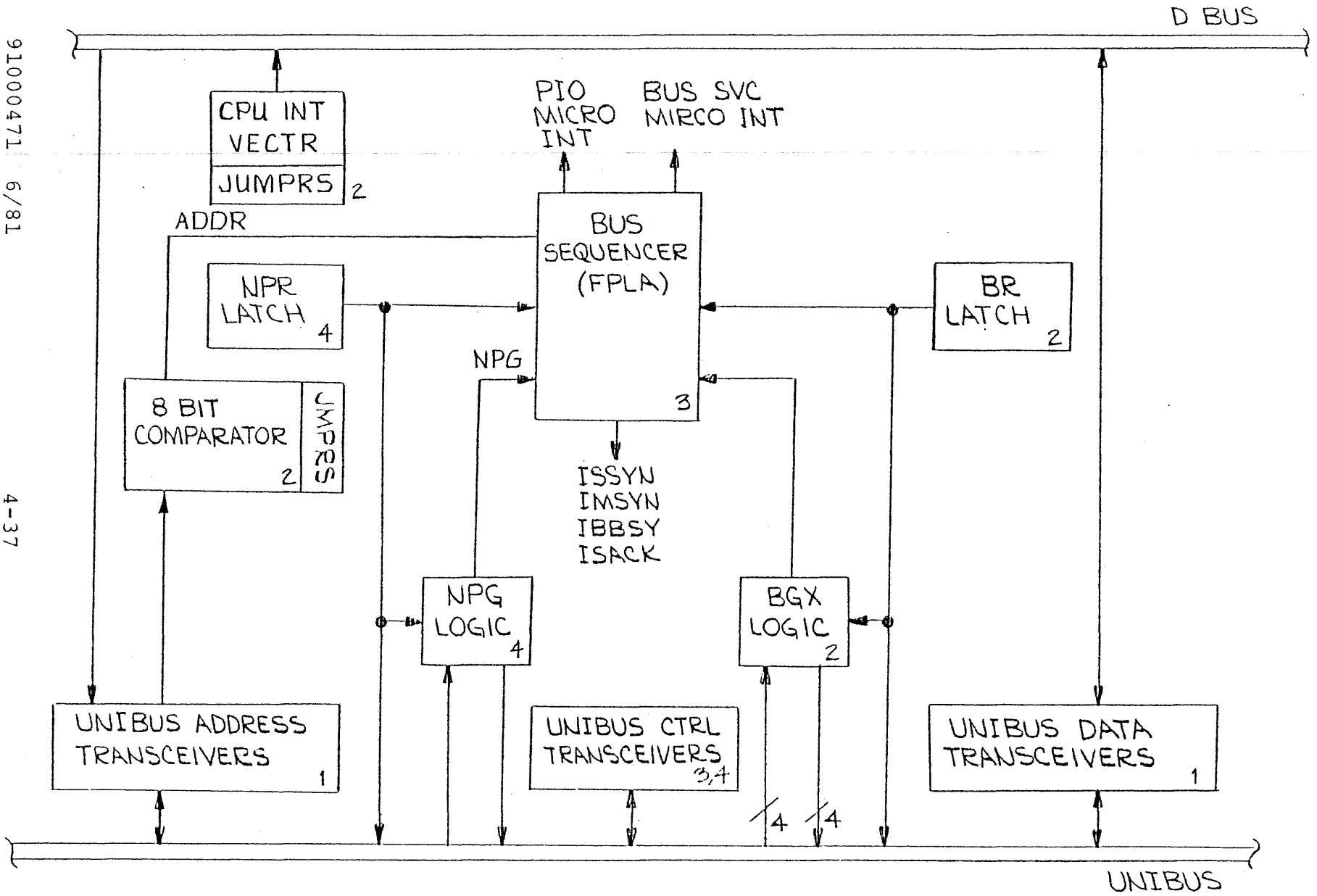


FIGURE 4-19 UNIBUS INTERFACE

4.52 DATA TRANSCEIVERS. Four 2980 transceivers are used to connect the controller internal DBus to the Unibus. The transmitter register is loaded as an exterhal destination on the DBus and is used for PIO read registers and NPR write memory operations. The receiver latch can be read onto the DBus as an external source. PIO write register and NPR read memory operations are terminated only after the micro-processor has input the data from the bus.

4.53 NON-PROCESSOR REQUESTS (DMA). The controller uses NPR's for all data transfers associated with write or read data tape commands to the TM11 controller. An NPR transaction is initiated by the controller's main firmware, executed by the FPLA bus sequencer and the Unibus, and terminated by the main firmware. The NPR signal and transfer direction signal C1 are set and reset by latches controlled by the firmware. Once the NPR signal is set, the FPLA monitors the Unibus for the appropriate responses and assumes bus master. The bus sequencer will generate a micro-level interrupt to request data during a write memory operation or to signify that data is available during a read memory operation. The micro-level vectored interrupt will enter the appropriate interrupt service routine and read or supply data. The routine will then direct the bus sequencer to terminate the operation by resetting NPR.

4.54 BUS REQUEST (INTERRUPT). The bus request is used to interrupt the CPU at a desired point in a TM11 command if the interrupt enable bit in the MTC register is set. A bus request is initiated by the main firmware and executed by the FPLA bus sequencer and the Unibus, and then terminated by the main firmware. The bus sequencer will generate a micro-level interrupt at the point in bus request cycle where the interrupt vector is required. The micro-level interrupt service routine will read the interrupt vector switches and load them into the data bus transmitter register. The bus sequencer is then directed to complete the bus request by the clearing of the BR latch.

SECTION V

FIRMWARE

SECTION V
FIRMWARE

5.1 MICROINSTRUCTION WORD

5.2 The 48-bit microinstruction word is shown in Figure 5.1. The origin of the MIR signals is an array of PROMS labeled collectively the Control ROM (CROM) located on Sheet 11 and 12 of the logic diagrams. The CROM array is addressed by the 10-bit CSA bus.

5.2 MIR 0 - LIT - Literal Select. When LIT is 0, MIR 32-47 form a 16-bit literal which is placed on the DBUS. When this bit is active, latch and interrupt vector loading operations are not available, and the 2910 is restricted to continue and return instructions.

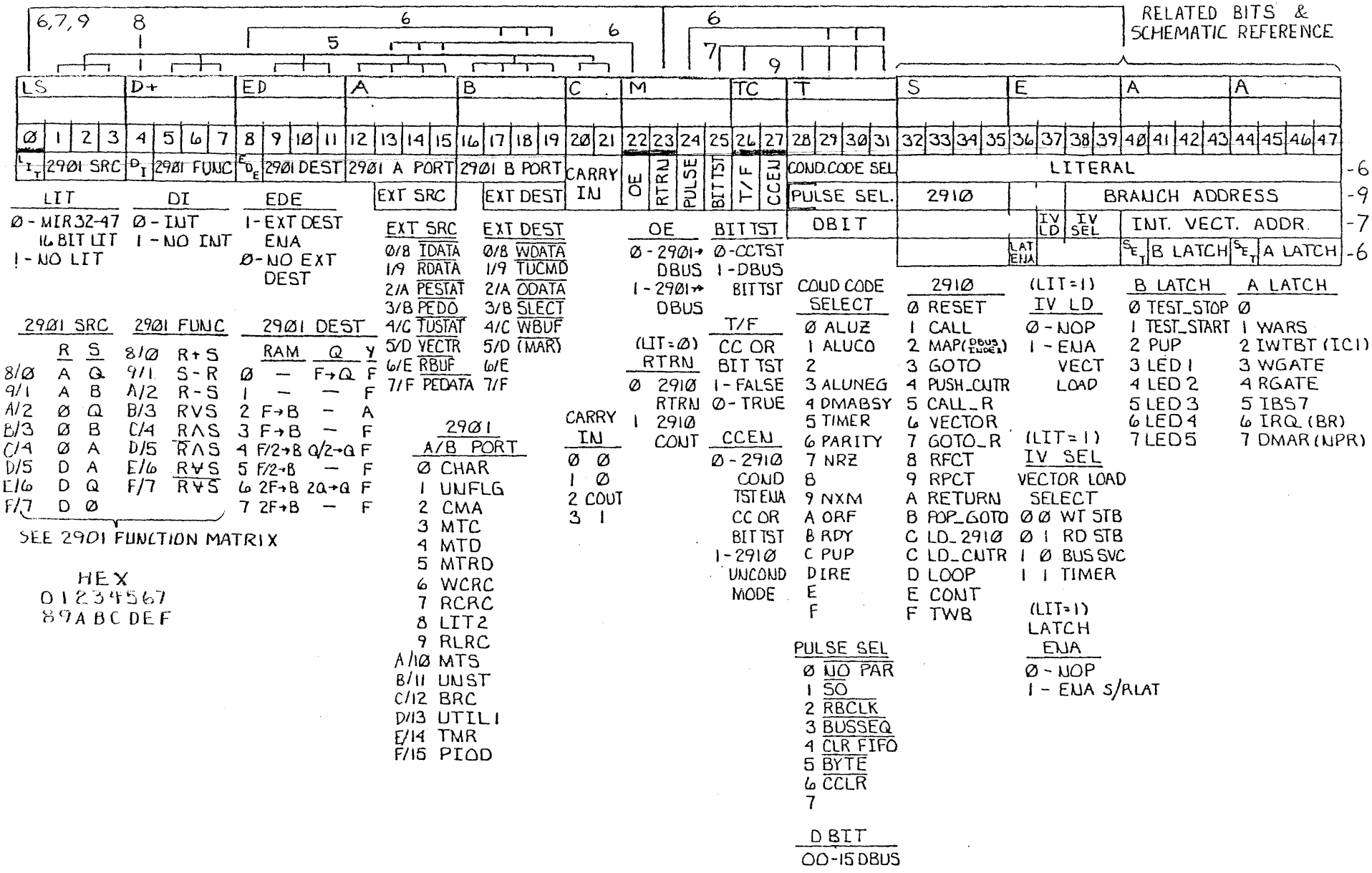


FIGURE 5.1 MICRO INSTRUCTION FORMAT

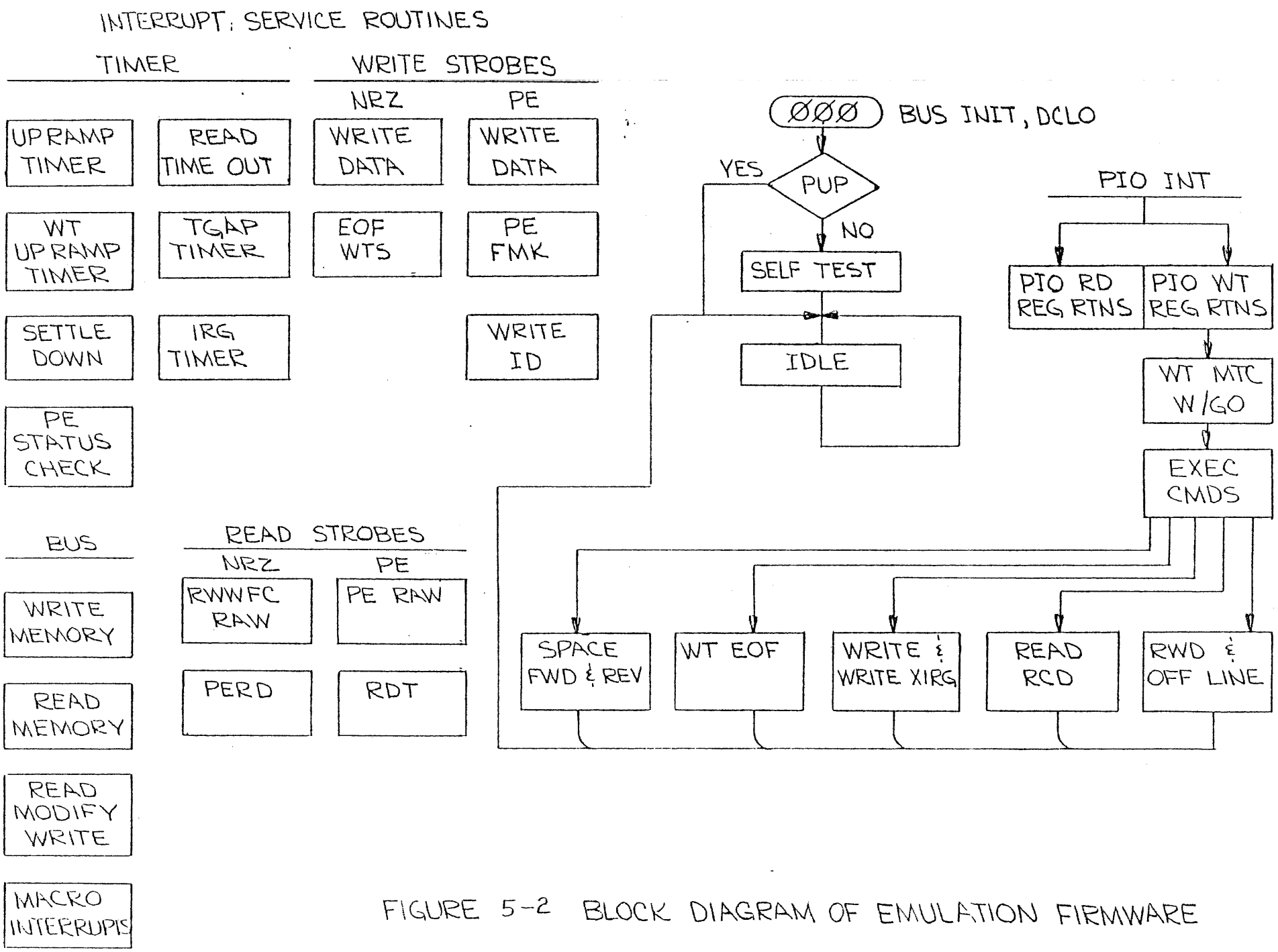


FIGURE 5-2 BLOCK DIAGRAM OF EMULATION FIRMWARE

5.3 MIR 1-3 - 2901 Source. These bits select the iniputs for the 2901 ALU according to the following table:

Value	R	S
0	A	0
1	A	B
2	0	Q
3	0	B
4	0	A
5	D	A
6	D	Q
7	D	0

5.4 MIR 4 - DI - Disable Micro-Level Interrupts. Microlevel interrupts are disabled when DI is logic 1.This bit is always set on any instruction which loads the interrupt vector file.

5.5 MIR 5-7 - 2901 Function. The 8 functions of the ALU are described by bits 5-7.

Value	Function	Description
0	R + S	Add
1	S - R	Subtract
2	R - S	Subtract
3	R v S	Or
4	R ^ S	And
5	-R ^ S	Notrs
6	R v S	Exor
7	-(R v S)	Exnor

5.6 MIR 8 - EDE - External Destination Enable. When Set an external destination clock is generated in accordance with the register selected by the B port field.

5.7 MIR 9-11 - 2901 Destination Control. The outputs of the 2901 are routed according to the following table:

Value	RAM	Q	Y
0	-	F > Q	F
1	-	-	F
2	F > B	-	A
3	F > B	-	F
4	F/2 > B	Q/2 > Q	F
5	F/2 > B	-	F
6	2F > B	2Q > Q	F
7	2F > B	-	F

5.8 MIR 12-15 - A Port/Ext Source

5.9 MIR 16-19 - B Port/Ext Destination. The normal functions of the described bits are as follows:

A or B PORT	Internal	EXTERNAL REGISTER	
VALUE	2901 Register	Source	Destination
0	MTS	IDAT	WDATA
1	CMA	RDATA	TUCMD
2	BRC	PESTAT	ODATA
3	MTC	PEDO	SLECT
4	MTD	TUSTAT	WBUF
5	MTRD/FLAGS	VECTR	MAR
6	WCRC - NRZ	RBUF	-
7	RCRC - NRZ	PEDATA	-
8	LIT2	IDATA	WDATA
9	RLRC	RDATA	TUCMD
A	CHAR REG	PESTAT	ODATA
B	UNST	PEDO	SLECT
C	UNIT FLAG	TUSTAT	WBUF
D	UTILI	VECTR	MAR
E	TMR	RBUF	-
F	PIO	PEDATA	-

The external sources are enabled whenever a Literal (MIR00) or 2901 output (MIR22) are not specified. An external destination is enabled by EDE (MIR 8). The external source and destination register selections are shown in the preceding A and B port list. The external registers are selected by three bits from each field and therefore appear twice in the list.

5.10 MIR 20-21 - CARRY

Value	Carry In
0	0
1	0
2	Carryout
3	1

5.11 MIR 22 - OE - Output Enable. When MIR 22 is Logic 0, the 2901 output is enabled onto the DBUS.

5.12 MIR 23 - RTRN - 2910 Return

LIT	RTRN	Function
0	0	2910 Return
0	1	2910 Continue

5.13 MIR 24 - PULSE. This is the pulse control bit for the pulse selected by MIR 29-31.

5.14 MIR 25 - Bit Test

Value	Function
0	Condition Code Test
1	DBUS Bit Test

5.15 MIR 26 - T/F. For either Condition Code or Bit Test; 0 = True, 1 = False.

5.16 MIR 27 - CCEN - Condition Code Enable

Value	Function
0	2910 Condition Test Enable
1	Unconditional Operation

5.17 MIR 28-31 - Condition Code Select

Value	DBUS Bit	CC	
0	00	ALUZ	- 2901 Funtion had zero results
1	01	ALUCO	- 2901 Carryout
2	02	DECPAK	- DEC vs IBM Byte Packing
3	03	ALUNEG	- 2901 Bit 15 set
4	04	DMABSY	- NPR or Bus Sequencer Busy
5	05	Timer	- Timer (MTRD)
6	06	PARITY	- Parity error on DBUS 00-02

7	07	NRZ	- PE vs NRZ mode
8	08		- Not Used
9	09	NXM	- Non existant memory
A	10	ORE	- Data buffer Fifo output ready
B	11	RDY	- Tape unit ready
C	12	PUP	- Power up latch- Reset by DCLO only
D	13	IRE	- Data buffer Fifo input ready
E	14		- Not Used
F	15		- Not Used

5.18 MIR 29-31 - PULSE SELECT. When Pulse Enables is a logic one, MIR29-31 selects one of 8 pulses to be generated. The pulse width is 100 nsec.

Value	Pulse	
0	NO PARITY	- Write data parity register loaded direct from DBUS bit 09
1	SO	- Shift out data from deskew buffer
2	RBCLK	- Shift out from data buffer FIFO
3	BUSSEQ	- Unibus sequencer continue command
4	CLRFIFO	- Clears data buffer FIFO
5	BYTE	- Controls Byte PIO operations
6	CCLR	- Controller Clear
7	N/U	- Not Used

When Literal, MIR 0, active.

5.19 MIR 32-47 - LITERAL. When Literal, MIR 0 not active.

5.20 MIR 32-35 - 2910 Instruction, 38-47 PIPELINE ADDRESS

Value	2910 Instruction
0	GOTO 0, clear stack
1	Call subroutine
2	GOTO Map
3	GOTO
4	PUSH
5	CALL SUBROUTINE R OR PIPELINE
6	GOTO Vector
7	GOTO R or PIPELINE
8	RFCT
9	RPCT
A	RETURN
B	POP-GOTO
C	LD-CNTR
D	LOOP
E	CONTINUE
F	TWB

5.21 MIR 36 - LATCH ENABLE, 40-43 B LATCH, 44-47 A LATCH

MIR 40 B LATCH SET/RESET
MIR 44 A LATCH SET/RESET

45-47 Value	A LATCH	41-43 Value	B LATCH
0		0	TEST-STOP
1	WARS	1	TEST-START
2	C1	2	PUP
3	WRITE GATE	3	LED1
4	READ GATE	4	LED2
5		5	LED3
6	IRQ		LED4
7	DMAR	7	LED5

5.22 MIR 37 - Microlevel Interrupt Vector Load Enable

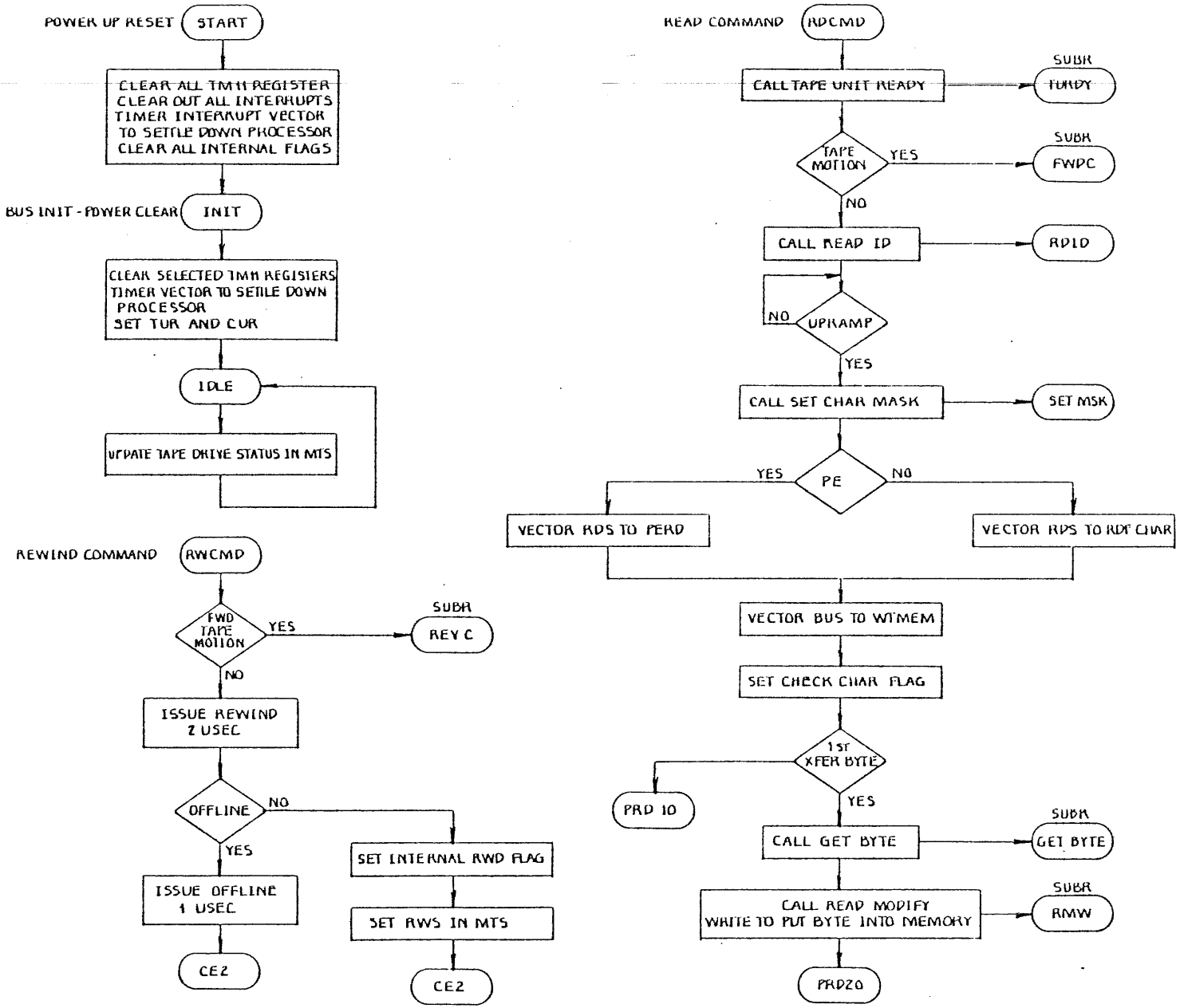
5.23 MIR 38-39 Microlevel Interrupt Vector Select

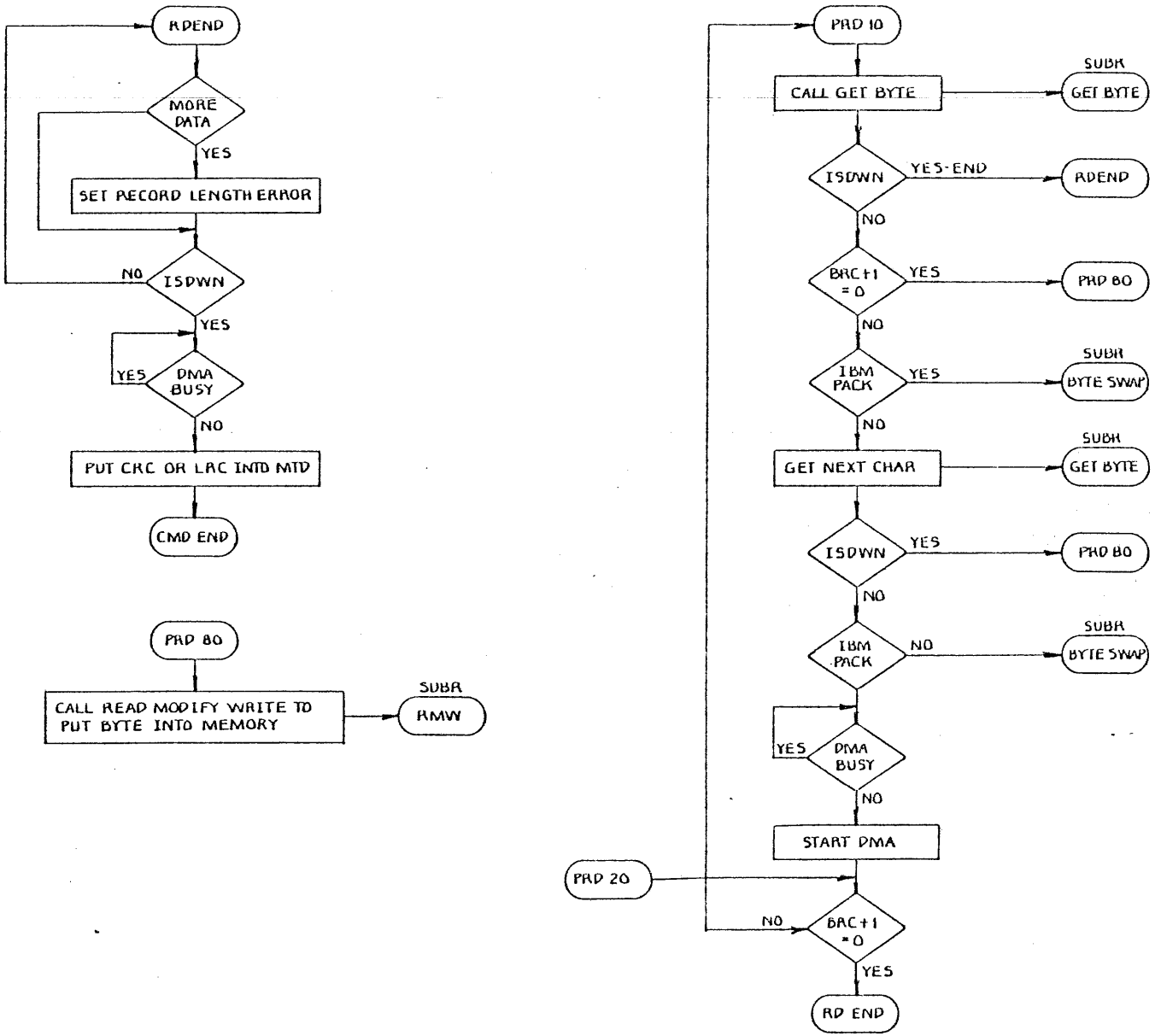
Value	Interrupt
0	WRITE STROBE
1	READ STROBE
2	BUS SERVICE
3	TIMER

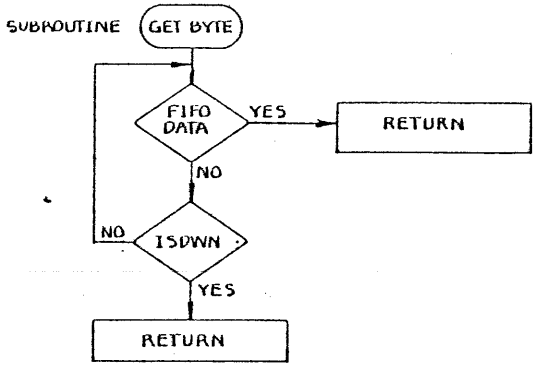
5.24 MIR 40-47 - INTERRUPT VECTOR

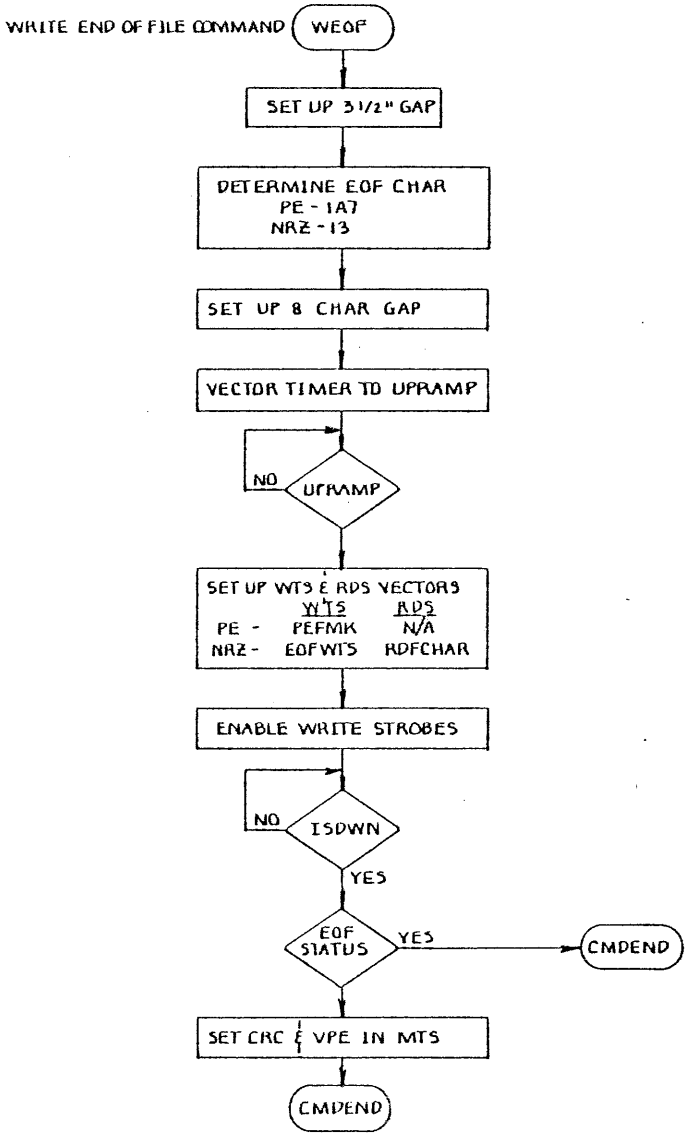
5.25 FIRMWARE FLOW CHARTS

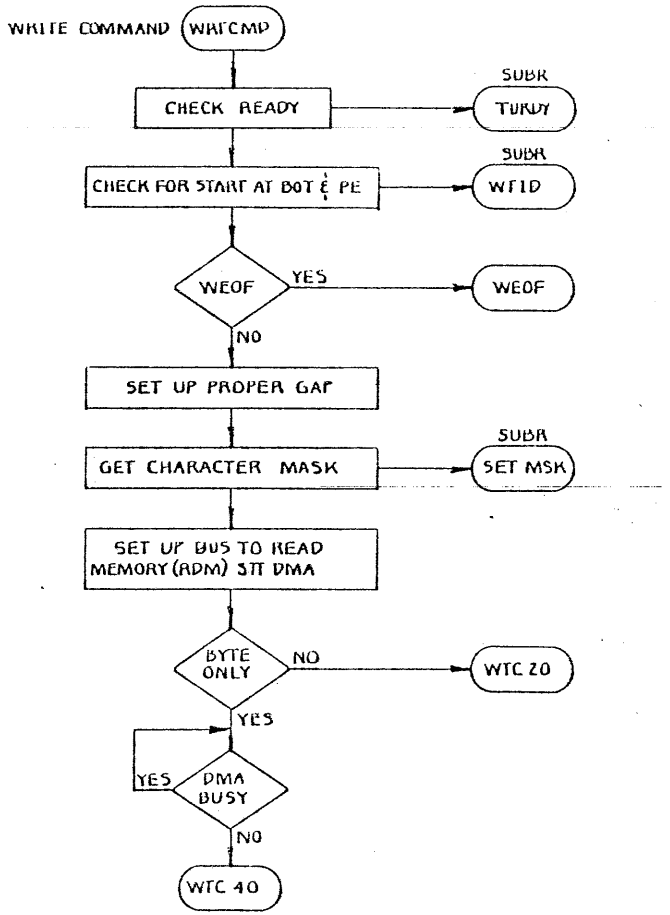
5.26 This section contains the flow charts of the TM11 emulation firmware for the controller. Figure 5.2 gives a block diagram of the Firmware.

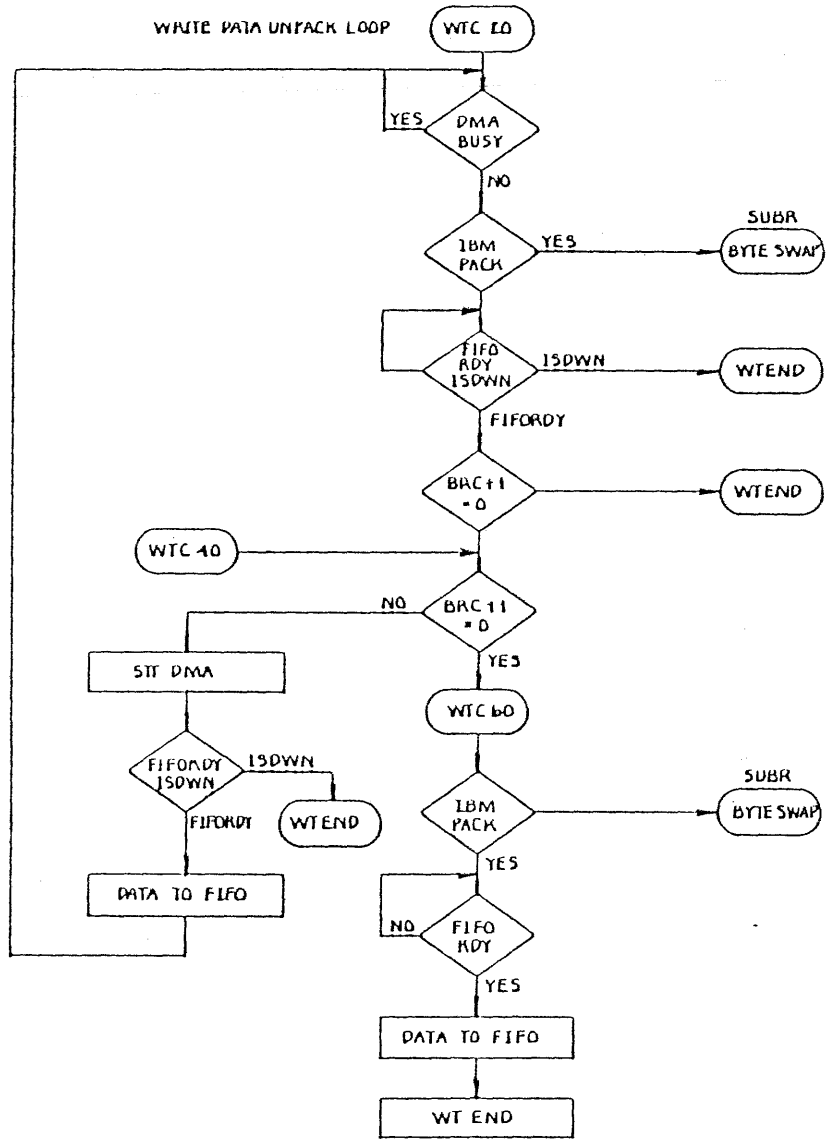

POWER UP RESET
START
CLEAR ALL TMH REGISTER
CLEAR OUT ALL INTERRUPTS
TIMER INTERRUPT VECTOR
TO SETTLE DOWN PROCESSOR
CLEAR ALL INTERNAL FLAGS
BUS INIT - POWER CLEAR
INIT
CLEAR SELECTED TMH REGISTERS
TIMER VECTOR TO SETTLE DOWN
PROCESSOR
SET TUR AND CUR
IDLE
UPDATE TAPE DRIVE STATUS IN MTS
REWIND COMMAND
RWCMD
FWD TAPE MOTION
YES
SUBR
REW C
NO
ISSUE REWIND
2 USEC
OFFLINE
NO
YES
ISSUE OFFLINE
1 USEC
SET INTERNAL RWD FLAG
SET RWS IN MTS
CE2
CE2
READ COMMAND
RDCMD
CALL TAPE UNIT READY
SUBR
TURDY
TAPE MOTION
YES
SUBR
FWPC
NO
CALL READ ID
RDID
NO
UPRAMP
YES
CALL SET CHAR MASK
SET MSK
YES
PE
NO
VECTOR RDS TO PERD
VECTOR RDS TO RDF CHAR
VECTOR BUS TO WTMEM
SET CHECK CHAR FLAG
1 ST XFER BYTE
PRD 10
YES
CALL GET BYTE
SUBR
GET BYTE
CALL READ MODIFY
WRITE TO PUT BYTE INTO MEMORY
SUBR
RMW
PRDZO

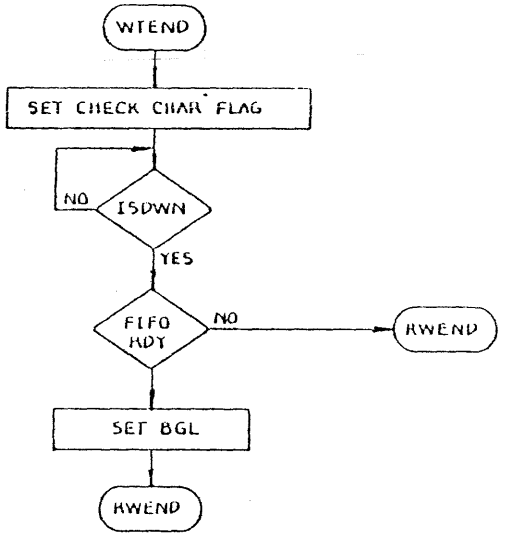

RDEND
MORE DATA
YES
SET RECORD LENGTH ERROR
NO
ISDWN
YES
YES
DMA BUSY
NO
PUT CRC OR LRC INTO MTD
CMD END
PRD 80
CALL READ MODIFY WRITE TO PUT BYTE INTO MEMORY
SUBR
RMW
PRD 10
CALL GET BYTE
SUBR
GET BYTE
ISDWN
YES-END
RDEND
NO
BRC+1 = 0
YES
PRD 80
NO
IBM PACK
YES
SUBR
BYTE SWAP
NO
GET NEXT CHAR
SUBR
GET BYTE
ISDWN
YES
PRD 80
NO
IBM PACK
NO
SUBR
BYTE SWAP
YES
DMA BUSY
NO
START DMA
PRD 20
NO
BRC+1 = 0
YES
RD END

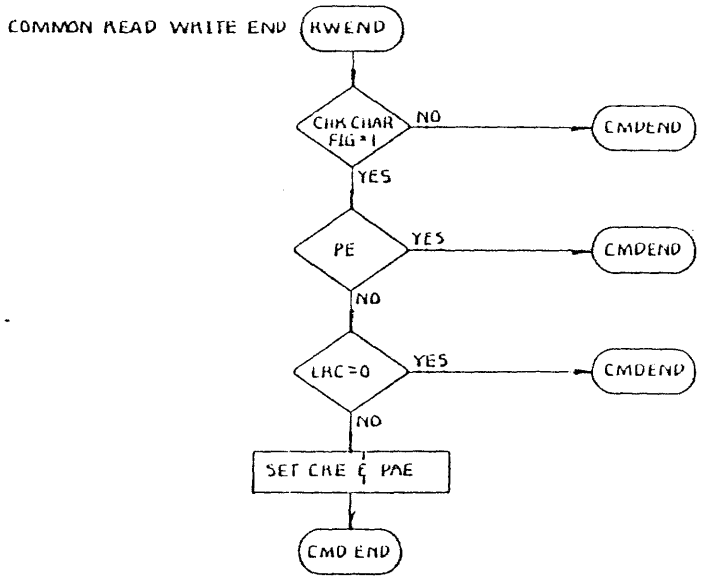

SUBROUTINE
GET BYTE
FIFO DATA
YES
RETURN
NO
NO
ISDWN
YES
RETURN

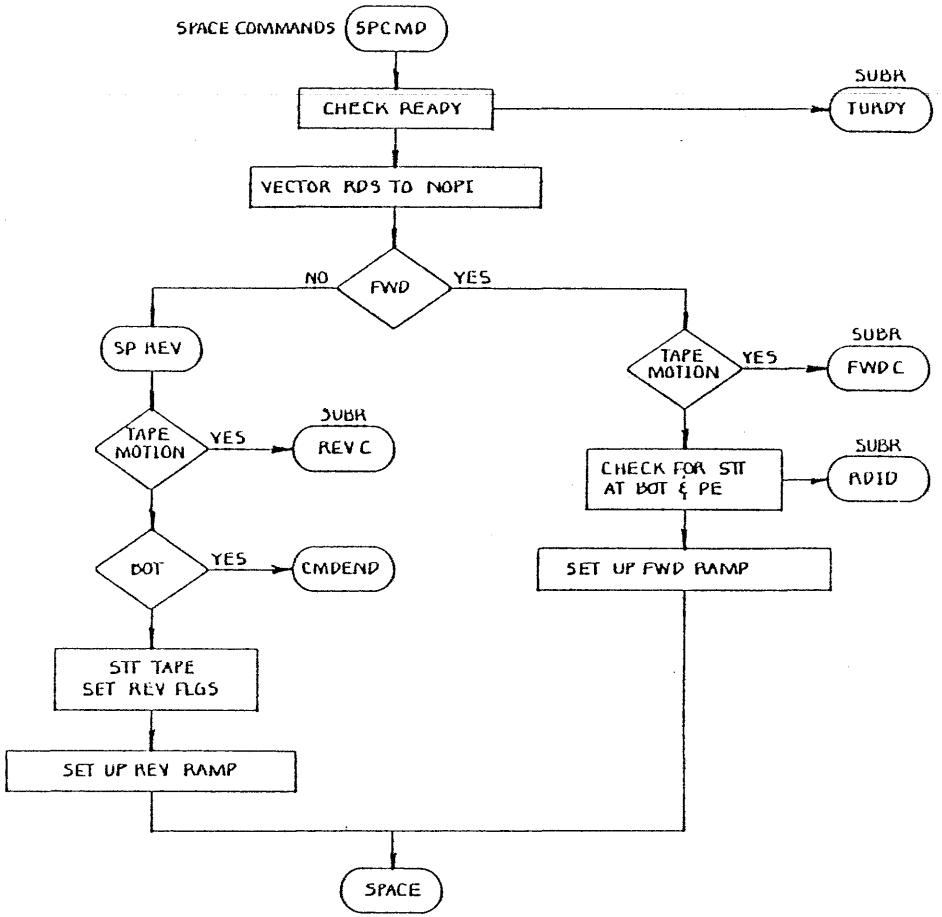

WRITE END OF FILE COMMAND
WEOF
SET UP 3 1/2" GAP
DETERMINE EOF CHAR
PE - 1A7
NRZ - 13
SET UP 8 CHAR GAP
VECTOR TIMER TO UPRAMP
NO
UPRAMP
SET UP WTS & RDS VECTORS
WTS
RDS
PE -
PEFMK
N/A
NRZ -
EOFWTS
RDFCHAR
ENABLE WRITE STROBES
NO
ISDWN
YES
EOF STATUS
YES
CMDEND
SET CRC & VPE IN MTS
CMDEND

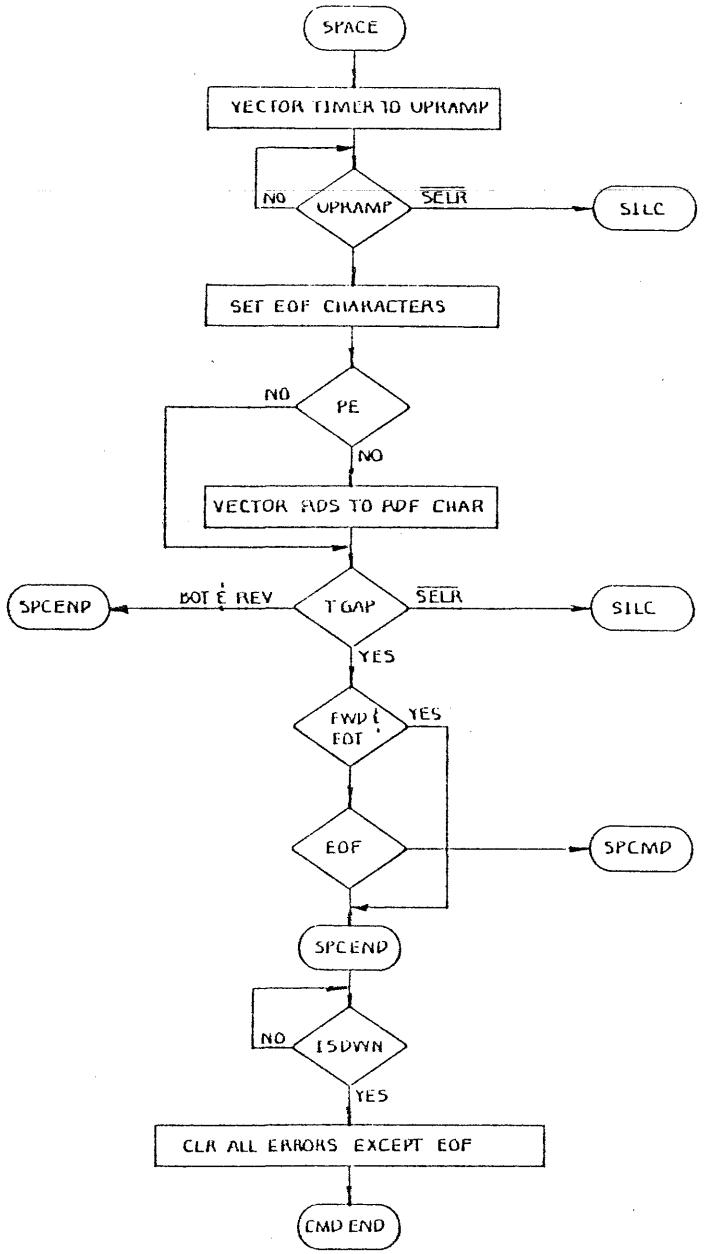

WRITE COMMAND
WRTCMD
CHECK READY
SUBR
TURDY
CHECK FOR START AT BOT & PE
SUBR
WT1D
WEOF
YES
WEOF
NO
SET UP PROPER GAP
GET CHARACTER MASK
SUBR
SET MSK
SET UP BUS TO READ MEMORY (RDM) STT DMA
BYTE ONLY
NO
WTC 20
YES
YES
DMA BUSY
NO
WTC 40


WRITE DATA UNPACK LOOP
WTC E0
YES
DMA BUSY
NO
IBM PACK
YES
SUBR
BYTE SWAP
FIFO RDY ISDWN
ISDWN
WTEND
FIFORDY
BRC+1 = 0
WTEND
WTC 40
NO
BRC 11 = 0
YES
SIT DMA
WTC 60
FIFORDY ISDWN
ISDWN
WTEND
FIFORDY
SUBR
IBM PACK
BYTE SWAP
YES
DATA TO FIFO
NO
FIFO RDY
YES
DATA TO FIFO
WT END

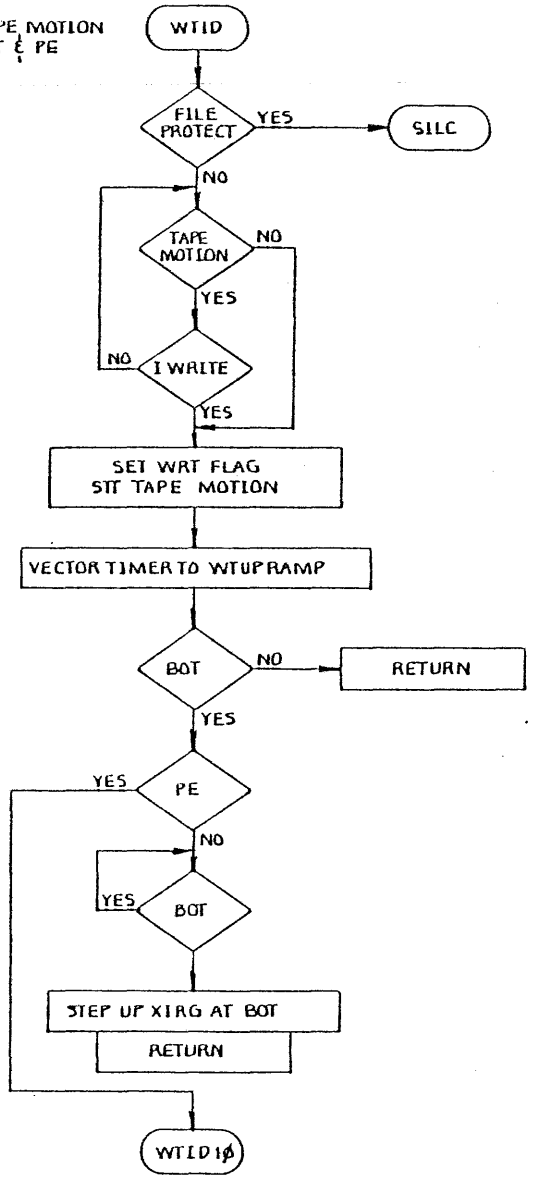

WTEND
SET CHECK CHAR FLAG
NO
ISDWN
YES
FIFO RDY
NO
RWEND
SET BGL
RWEND

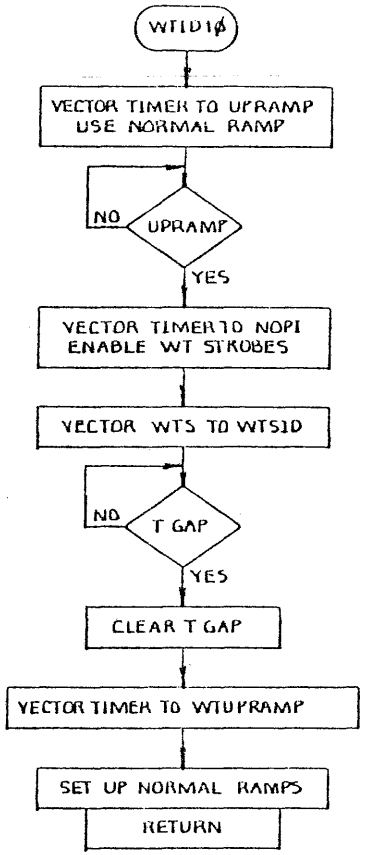

COMMON READ WRITE END
RWEND
CHK CHAR FLG = 1
NO
CMDEND
YES
PE
YES
CMDEND
NO
LRC=0
YES
CMDEND
NO
SET CRE & PAE
CMD END

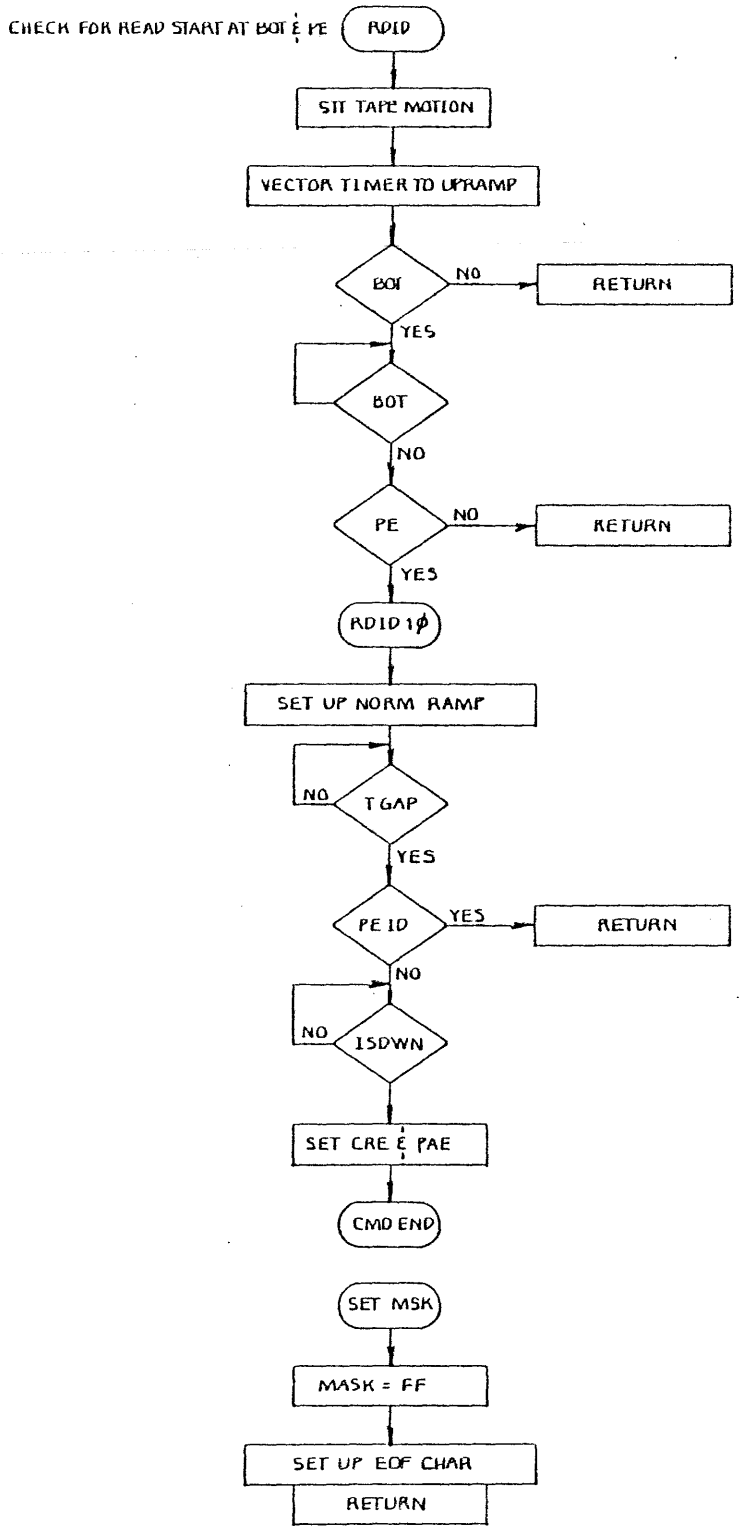

SPACE COMMANDS
SPCMD
CHECK READY
SUBR
TURDY
VECTOR RDS TO NOPI
NO
FWD
YES
SP REV
TAPE MOTION
YES
SUBR
REV C
BOT
YES
CMDEND
STT TAPE
SET REV FLGS
SET UP REV RAMP
TAPE MOTION
YES
SUBR
FWD C
CHECK FOR STT AT BOT & PE
SUBR
RDID
SET UP FWD RAMP
SPACE

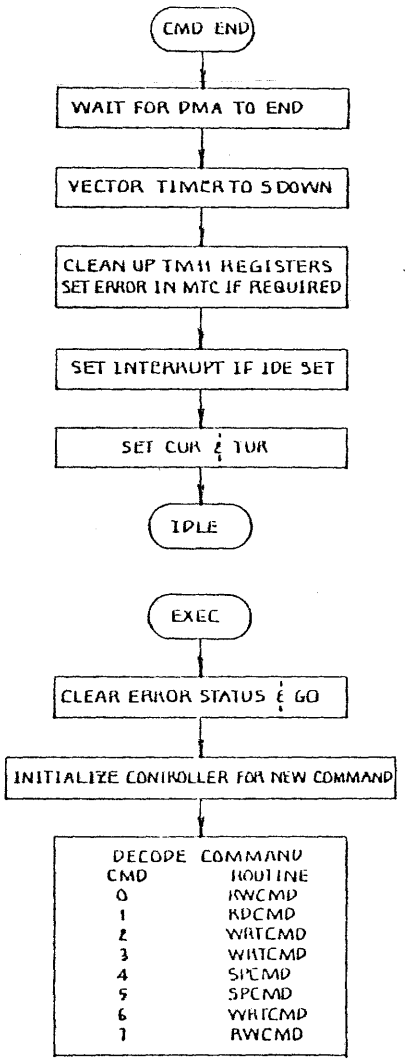

SPACE
VECTOR TIMER TO UPRAMP
NO
UPRAMP
SELR
SILC
SET EOF CHARACTERS
NO
PE
NO
VECTOR RDS TO RDF CHAR
SPCENP
BOT & REV
TGAP
SELR
SILC
YES
FWD & EOT
YES
EOF
SPCMD
SPCEND
NO
ISDWN
YES
CLR ALL ERRORS EXCEPT EOF
CMD END

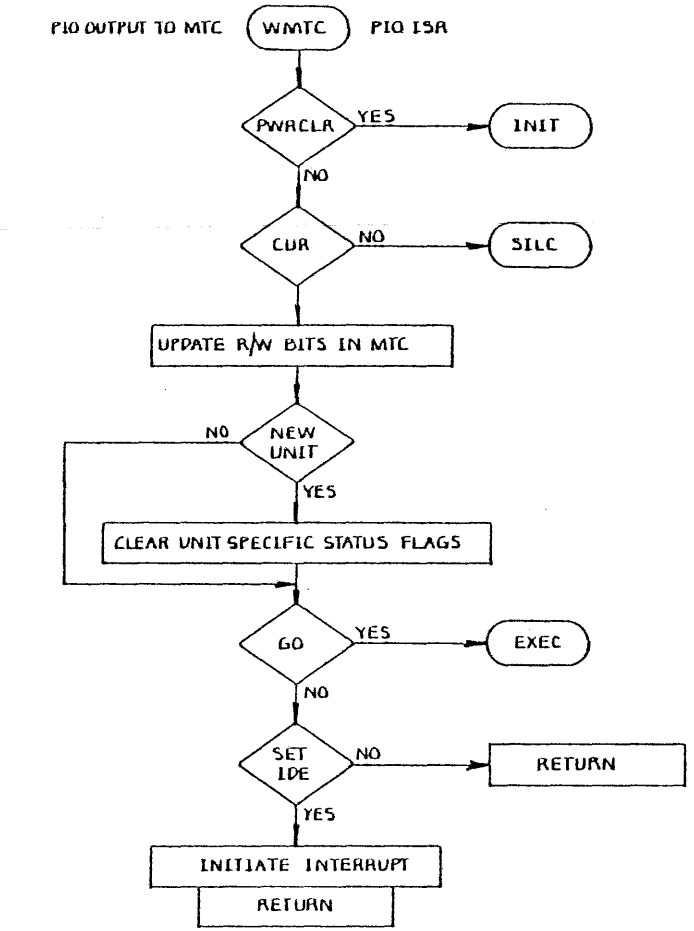
START FORWARD TAPE MOTION AND CHECK FOR BOT & PE

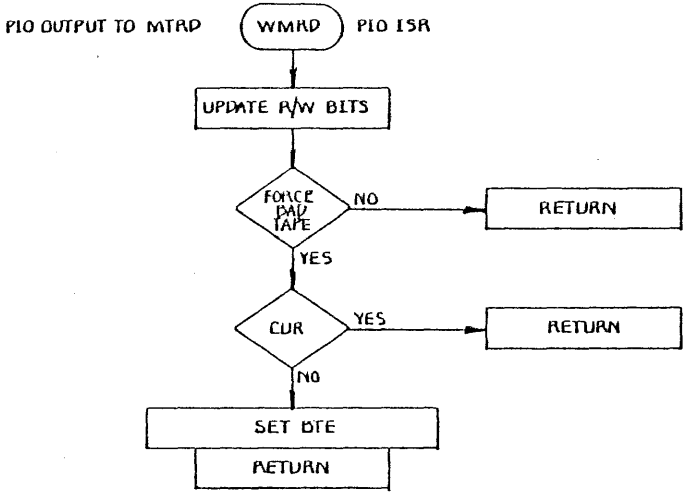


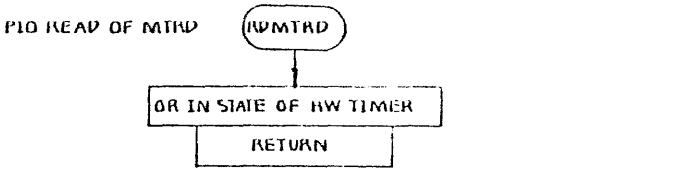


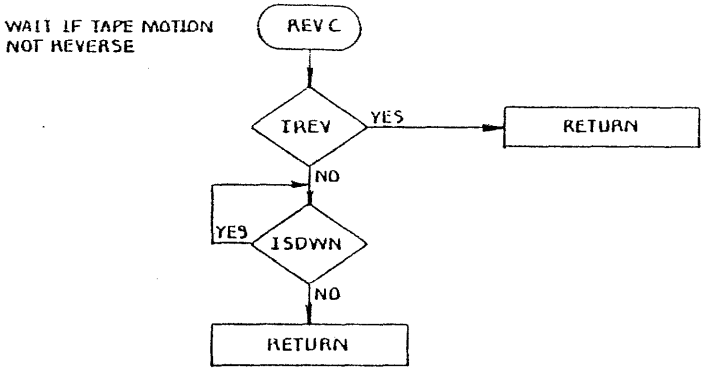

CHECK FOR READ START AT BOT & PE
RDID
SIT TAPE MOTION
VECTOR TIMER TO UPRAMP
BOT
NO
RETURN
YES
BOT
NO
PE
NO
RETURN
YES
RDID 1ϕ
SET UP NORM RAMP
NO
T GAP
YES
PE ID
YES
RETURN
NO
NO
ISDWN
SET CRE & PAE
CMD END
SET MSK
MASK = FF
SET UP EOF CHAR
RETURN

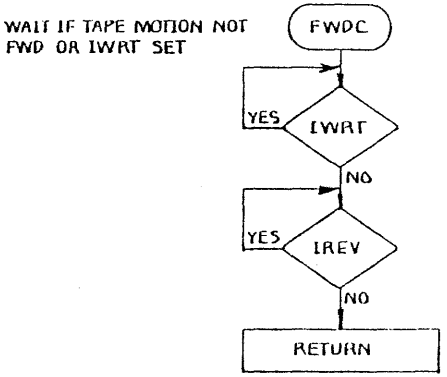

CMD END
WAIT FOR DMA TO END
VECTOR TIMER TO SDOWN
CLEAN UP TM11 REGISTERS
SET ERROR IN MTC IF REQUIRED
SET INTERRUPT IF IDE SET
SET CUR & TUR
IDLE
EXEC
CLEAR ERROR STATUS & GO
INITIALIZE CONTROLLER FOR NEW COMMAND
DECODE COMMAND
CMD ROUTINE
0 RWCMD
1 RDCMD
2 WRTCMD
3 WRTCMD
4 SPCMD
5 SPCMD
6 WRTCMD
7 RWCMD

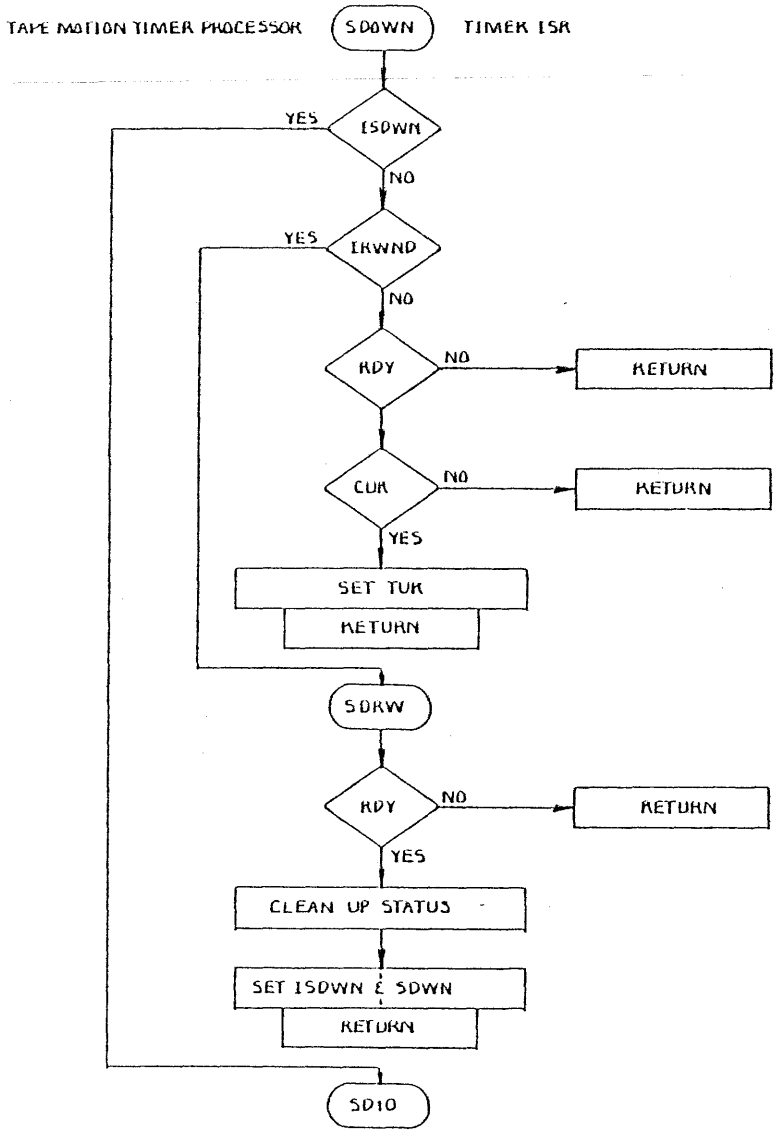

PIO OUTPUT TO MTC
WMTC
PIO ISR
PWRCLR
YES
INIT
NO
CUR
NO
SILC
UPDATE R/W BITS IN MTC
NO
NEW UNIT
YES
CLEAR UNIT SPECIFIC STATUS FLAGS
GO
YES
EXEC
NO
SET IDE
NO
RETURN
YES
INITIATE INTERRUPT
RETURN

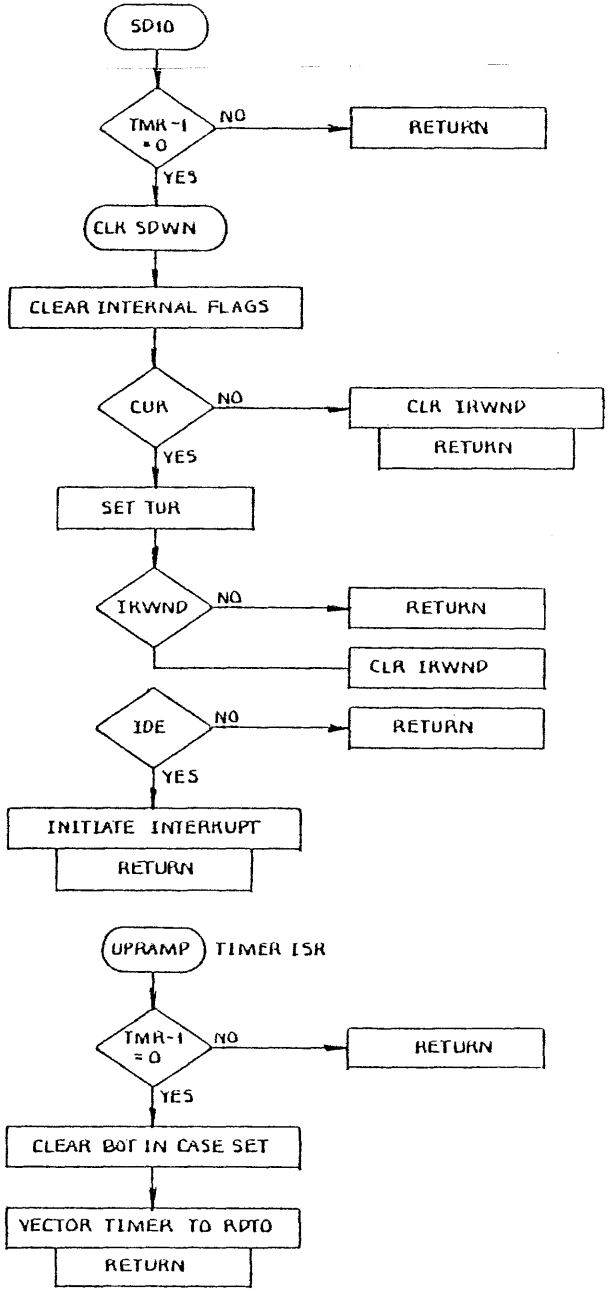

PIO OUTPUT TO MTRD
WMRD
PIO ISR
UPDATE R/W BITS
FORCE BAD TAPE
NO
RETURN
YES
CUR
YES
RETURN
NO
SET DTE
RETURN

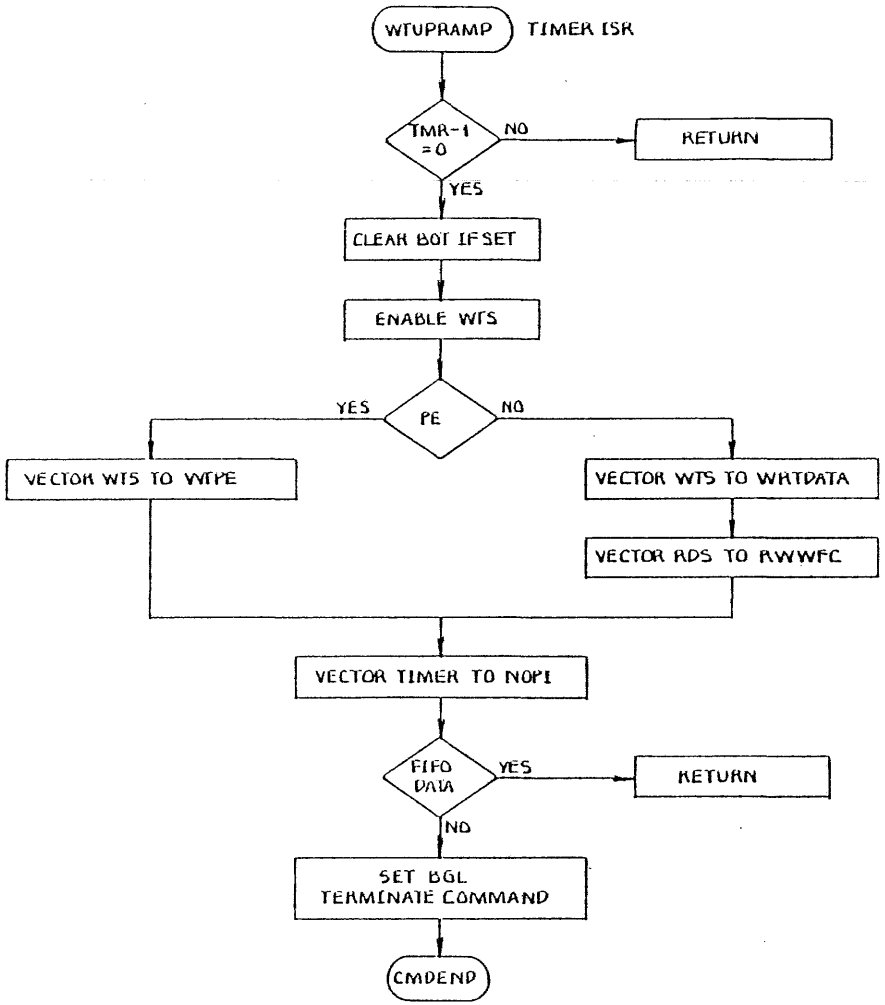

PIO READ OF MTRD
RDMTRD
OR IN STATE OF HW TIMER
RETURN

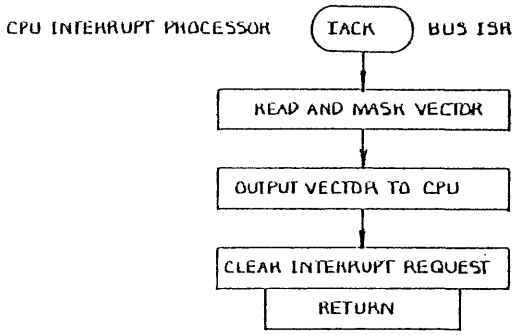

WAIT IF TAPE MOTION NOT REVERSE
REVC
IREV
YES
RETURN
NO
YES
ISDWN
NO
RETURN

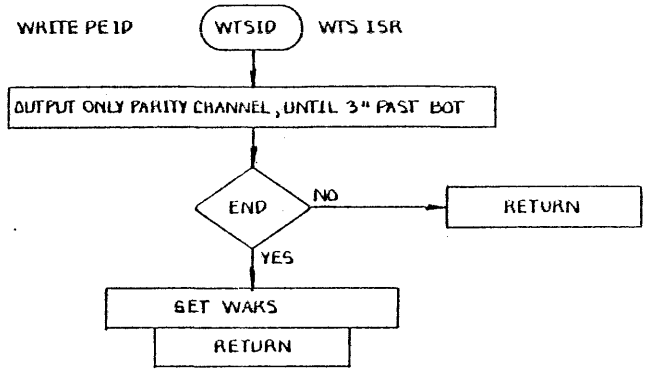

WAIT IF TAPE MOTION NOT FWD OR IWRT SET
FWDC
YES
IWRT
NO
YES
IREV
NO
RETURN

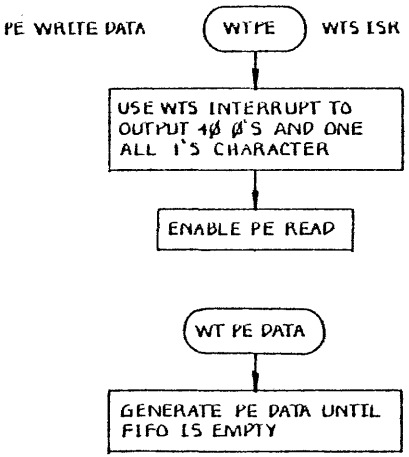

TAPE MOTION TIMER PROCESSOR
SDOWN
TIMER ISR
ISDWN
YES
NO
IRWND
YES
NO
RDY
NO
RETURN
CUR
NO
RETURN
YES
SET TUR
RETURN
SDRW
RDY
NO
RETURN
YES
CLEAN UP STATUS
SET ISDWN & SDWN
RETURN
SD10


SD10
TMR-1 = 0
NO
RETURN
YES
CLR SDWN
CLEAR INTERNAL FLAGS
CUR
NO
CLR IRWND
RETURN
YES
SET TUR
IRWND
NO
RETURN
CLR IRWND
IDE
NO
RETURN
YES
INITIATE INTERRUPT
RETURN
UPRAMP
TIMER ISR
TMR-1 = 0
NO
RETURN
YES
CLEAR BOT IN CASE SET
VECTOR TIMER TO RDTO
RETURN

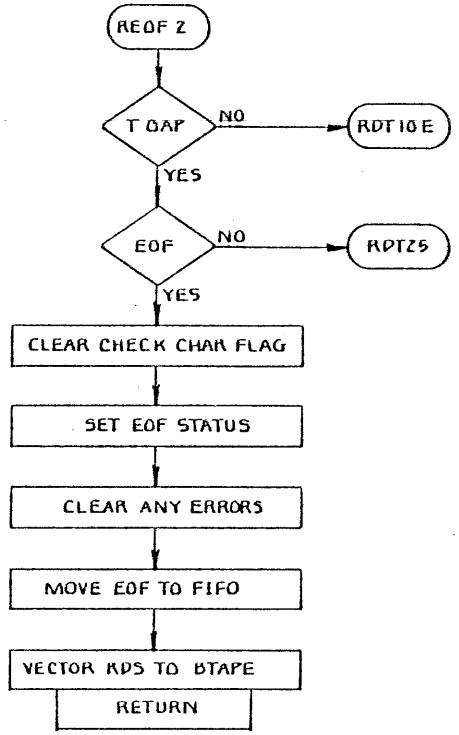

WTUPRAMP
TIMER ISR
TMR-1 =0
NO
RETURN
YES
CLEAR BOT IF SET
ENABLE WTS
YES
PE
NO
VECTOR WTS TO WTPE
VECTOR WTS TO WRTDATA
VECTOR RDS TO RWWFC
VECTOR TIMER TO NOP1
FIFO DATA
YES
RETURN
NO
SET BGL TERMINATE COMMAND
CMDEND

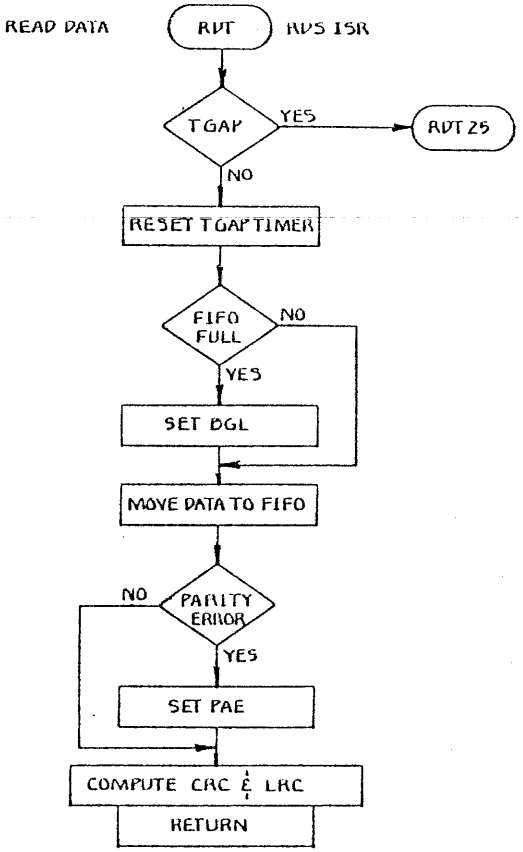

CPU INTERRUPT PROCESSOR
IACK
BUS ISR
READ AND MASK VECTOR
OUTPUT VECTOR TO CPU
CLEAR INTERRUPT REQUEST
RETURN

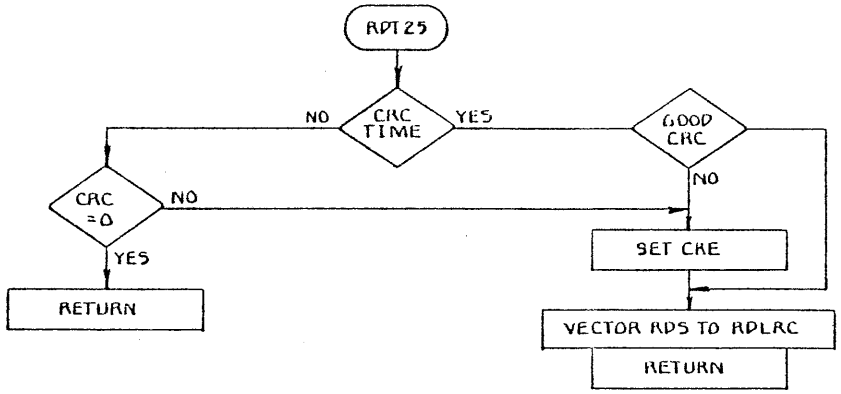

WRITE PE ID
WTSID
WTS ISR
OUTPUT ONLY PARITY CHANNEL, UNTIL 3" PAST BOT
END
NO
RETURN
YES
SET WAKS
RETURN

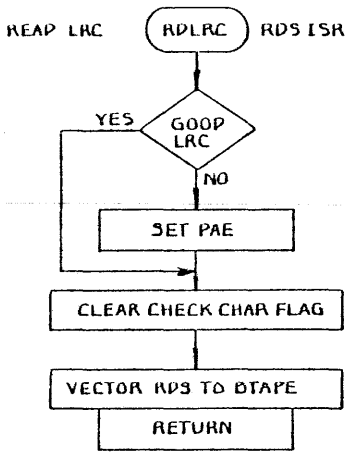

PE WRITE DATA
WTPE
WTS ISR
USE WTS INTERRUPT TO OUTPUT 40 0'S AND ONE ALL 1'S CHARACTER
ENABLE PE READ

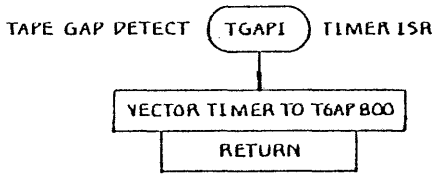
WT PE DATA
GENERATE PE DATA UNTIL FIFO IS EMPTY

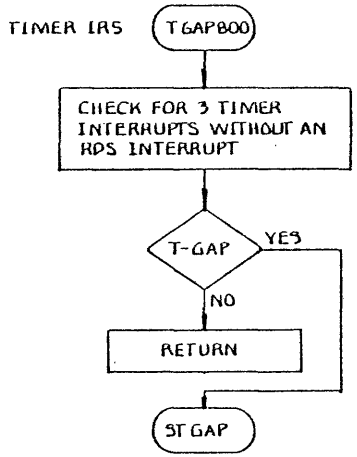

REOF 2
T GAP
NO
RDT10E
YES
EOF
NO
RDT25
YES
CLEAR CHECK CHAR FLAG
SET EOF STATUS
CLEAR ANY ERRORS
MOVE EOF TO FIFO
VECTOR RDS TO BTAPE
RETURN

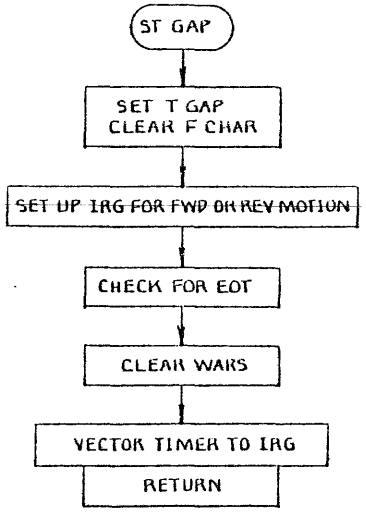

READ DATA
RDT
RDS ISR
T GAP
YES
RDT 25
NO
RESET T GAP TIMER
FIFO FULL
NO
YES
SET DGL
MOVE DATA TO FIFO
NO
PARITY ERROR
YES
SET PAE
COMPUTE CRC & LRC
RETURN

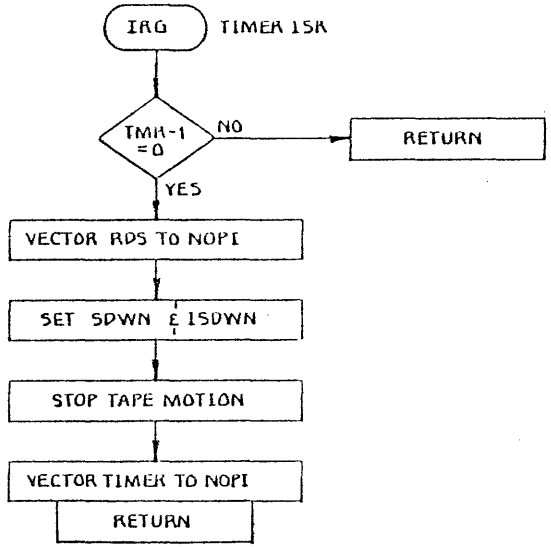

RDT 25
NO
CRC TIME
YES
GOOD CRC
NO
CRC =0
NO
YES
SET CRE
RETURN
VECTOR RDS TO RDLRC
RETURN

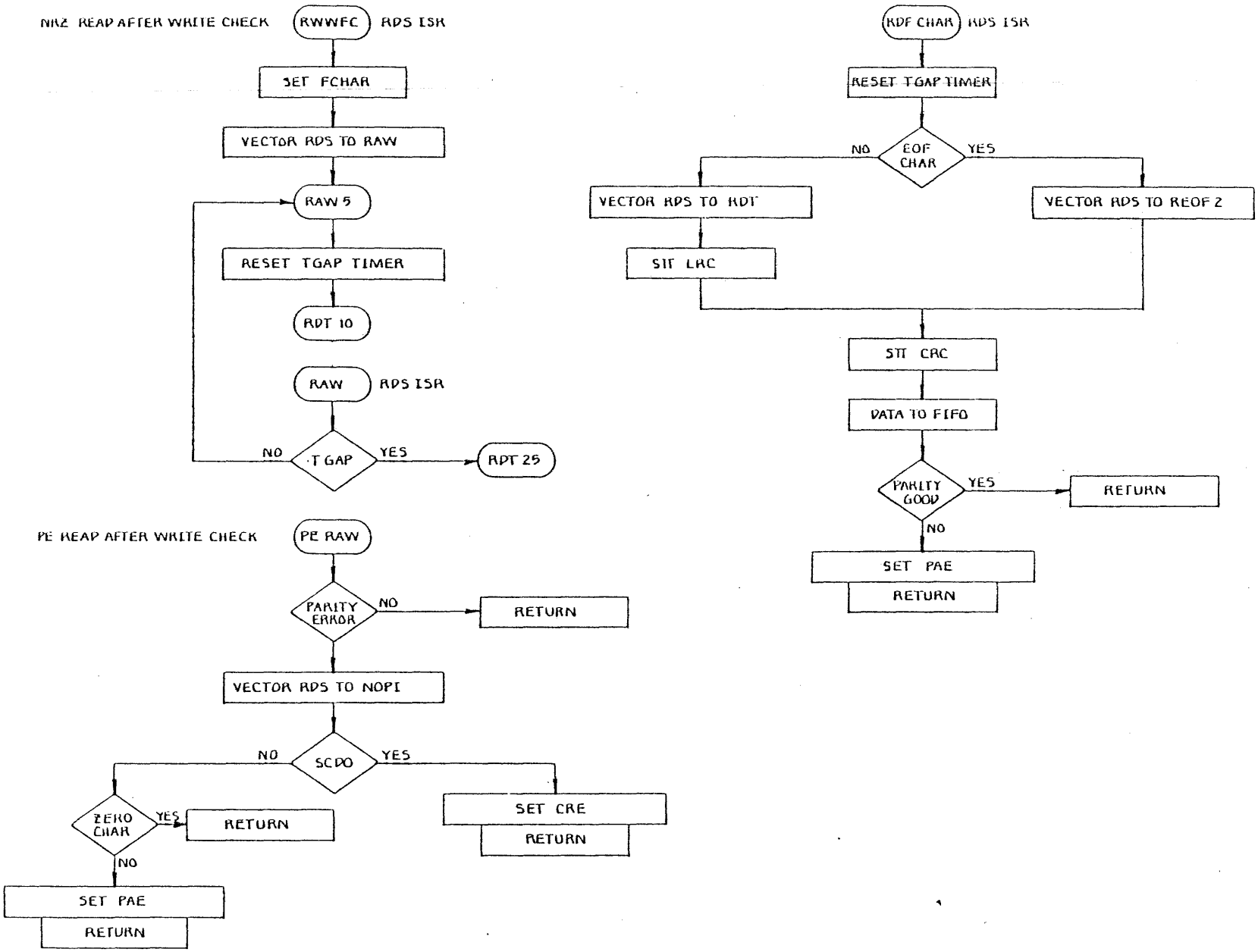

READ LRC
RDLRC
RDS ISR
YES
GOOD LRC
NO
SET PAE
CLEAR CHECK CHAR FLAG
VECTOR RDS TO BTAPE
RETURN

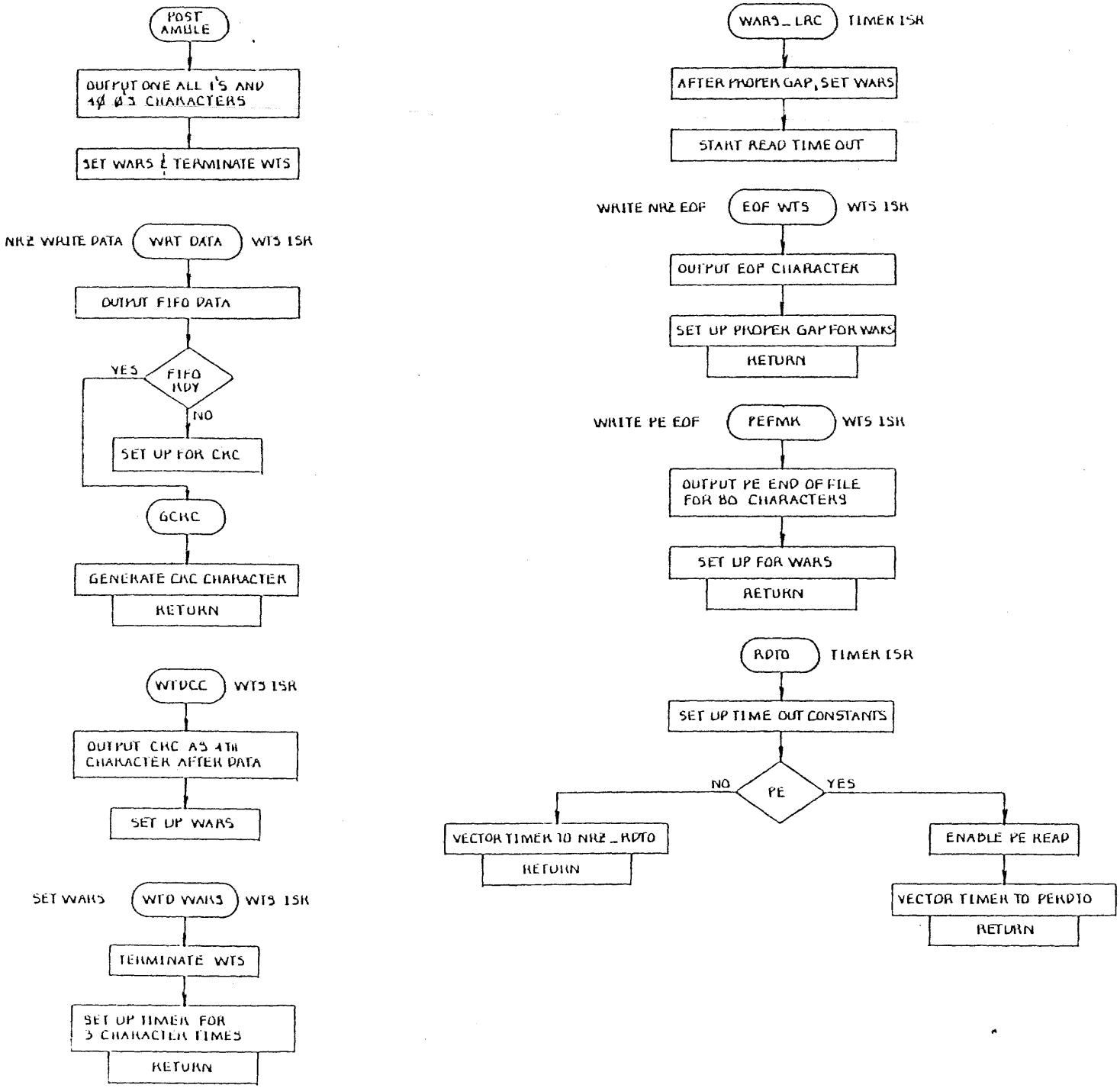

TAPE GAP DETECT
TGAPI
TIMER ISR
VECTOR TIMER TO TGAP800
RETURN

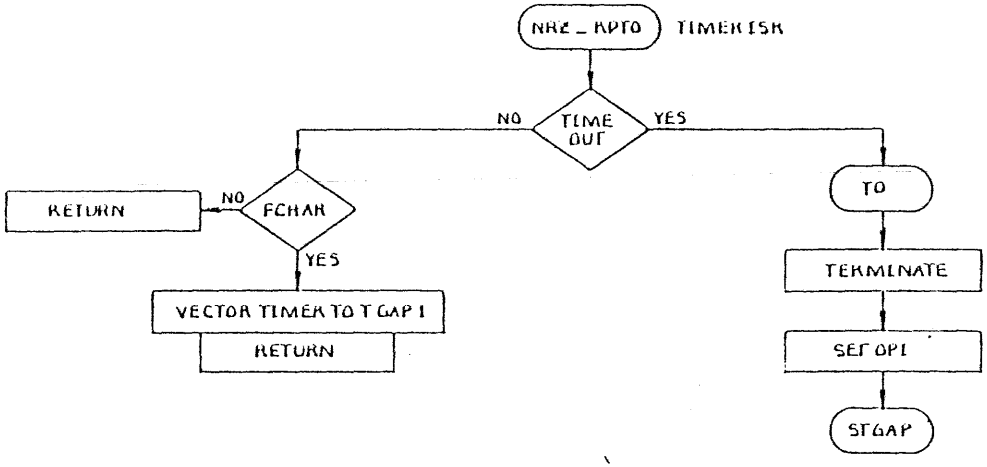

TIMER IRS
TGAP800
CHECK FOR 3 TIMER INTERRUPTS WITHOUT AN RDS INTERRUPT
T-GAP
YES
NO
RETURN
ST GAP

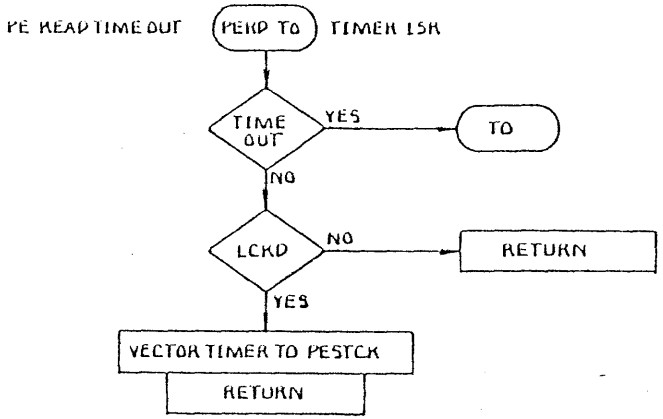

ST GAP
SET T GAP
CLEAR F CHAR
SET UP IRG FOR FWD OR REV MOTION
CHECK FOR EOT
CLEAR WARS
VECTOR TIMER TO IRG
RETURN

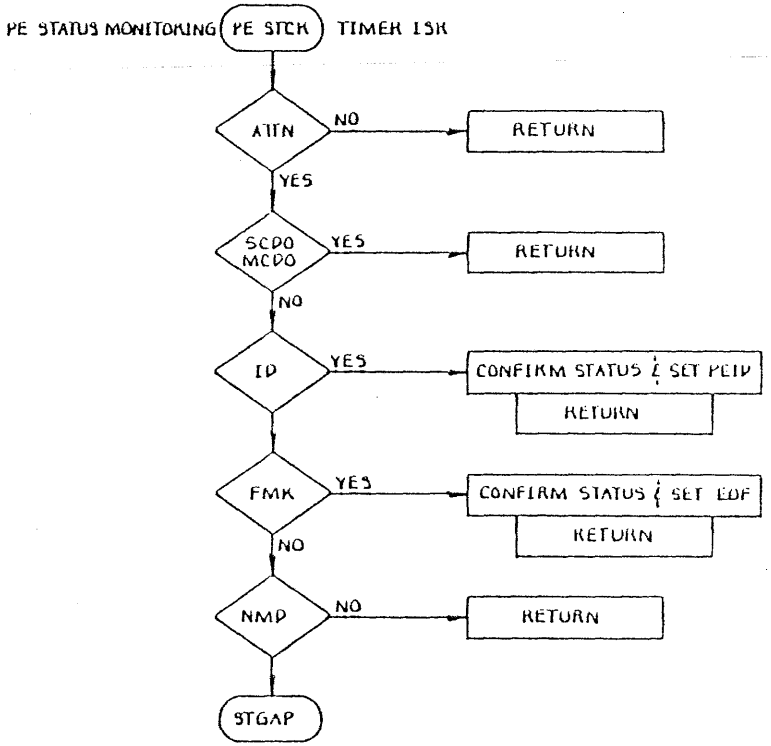

IRG
TIMER ISR
TMR-1 =0
NO
RETURN
YES
VECTOR RDS TO NOPI
SET SDWN & ISDWN
STOP TAPE MOTION
VECTOR TIMER TO NOPI
RETURN


NRZ READ AFTER WRITE CHECK
RWWFC
RDS ISR
SET FCHAR
VECTOR RDS TO RAW
RAW 5
RESET TGAP TIMER
RDT 10
RAW
RDS ISR
NO
T GAP
YES
RPT 25
PE READ AFTER WRITE CHECK
PE RAW
PARITY ERROR
NO
RETURN
VECTOR RDS TO NOPI
NO
SCDO
YES
ZERO CHAR
YES
RETURN
NO
SET PAE
RETURN
SET CRE
RETURN
RDF CHAR
RDS ISR
RESET TGAP TIMER
NO
EOF CHAR
YES
VECTOR RDS TO RDT
SIT LRC
VECTOR RDS TO REOF 2
STT CRC
DATA TO FIFO
PARITY GOOD
YES
RETURN
NO
SET PAE
RETURN


POST AMBLE
OUTPUT ONE ALL 1'S AND 1Ø Ø'S CHARACTERS
SET WARS & TERMINATE WTS
NRZ WRITE DATA
WRT DATA
WTS ISR
OUTPUT FIFO DATA
YES
FIFO RDY
NO
SET UP FOR CRC
GCRC
GENERATE CRC CHARACTER
RETURN
WTDCC
WTS ISR
OUTPUT CRC AS 4TH CHARACTER AFTER DATA
SET UP WARS
SET WARS
WTD WARS
WTS ISR
TERMINATE WTS
SET UP TIMER FOR 3 CHARACTER TIMES
RETURN
WARS_LRC
TIMER ISR
AFTER PROPER GAP, SET WARS
START READ TIME OUT
WRITE NRZ EOF
EOF WTS
WTS ISR
OUTPUT EOF CHARACTER
SET UP PROPER GAP FOR WARS
RETURN
WRITE PE EOF
PEFMK
WTS ISR
OUTPUT PE END OF FILE FOR 80 CHARACTERS
SET UP FOR WARS
RETURN
RDTO
TIMER ISR
SET UP TIME OUT CONSTANTS
NO
PE
YES
VECTOR TIMER TO NRZ_RDTO
RETURN
ENABLE PE READ
VECTOR TIMER TO PERDTO
RETURN


NRE_RPTO
TIMER ISR
TIME OUT
NO
YES
RETURN
NO
FCHAR
YES
VECTOR TIMER TO T GAP 1
RETURN
TO
TERMINATE
SET OPI
STGAP


PE READ TIME OUT
PERP TO
TIMER ISR
TIME OUT
YES
TO
NO
LCKD
NO
RETURN
YES
VECTOR TIMER TO PESTCK
RETURN


PE STATUS MONITORING
PE STCK
TIMER ISR
ATTN
NO
RETURN
YES
SCPO MCPO
YES
RETURN
NO
ID
YES
CONFIRM STATUS & SET PEIP
RETURN
FMK
YES
CONFIRM STATUS & SET EDF
RETURN
NO
NMP
NO
RETURN
STGAP

APPENDIX A

SIGNAL GLOSSARY

TC-131 SIGNAL GLOSSARY

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 1	
AØØ-15	Address lines (internal)
AØØ-15L	CPU Address bus
DBUS ØØ-15	Data Bus (internal)
DØØ-15L	CPU Data bus
SOURCE - SCHEMATIC PAGE 2	
ADDR	Controller Address detected
A16-17L	Extended Address bits
BGFF	Bus Grant Flip-Flop
BGH	Bus Grant High
BG4-7HI	Bus Grant In lines
BG4-7HO	Bus Grant Out lines
BR4-7L	Bus Request lines
CØ,1	Bus Control lines (internal)
CØ,1L	Bus Control lines
DBG	Delayed Bus Grant
SOURCE - SCHEMATIC PAGE 3	
BBSY	Bus Busy (internal)
BBSYL	Bus Busy
DOUT	Data Out

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 3 (CONT.)	
DSSYN	Delayed Slave Sync
IBBSY	Internal Bus Busy
IMSYN	Internal Master Sync
ISACK	Internal Selection Acknowledge
ISSYN	Internal Slave Sync
MSYN	Master Sync (internal)
MSYNL	Master Sync
NXM	Non-Existent Memory
PIO	Programmed I/O interrupt
SSYNL	Slave Sync
SVC	Bus Service interrupt
SOURCE - SCHEMATIC PAGE 4	
DCLO	DC Low Power (internal)
DCLOL	Bus DC Low Power
DNPG	Delayed Non-Processor Grant
INIT	Initialize (internal)
INITL	Bus Initialize
INTRL	Interrupt Request
LEINIT	Lengthened Initialize
NPGFF	Non-Processor Grant Flip-Flop

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 4 (CONT.)	
NPGHI	Non-Processor Grant In
NPGHO	Non-Processor Grant Out
NPRL	Non-Processor Request
RESET	Internal Reset
SACKL	Selection Acknowledge
SOURCE - SCHEMATIC PAGE 5	
ALUCO	Carry Result
ALUNEG	Negative Result
ALUZ	Zero Result
DBUSØØ-15	Data Bus (internal)
LBYTCLK	Lower Byte Clock
QLINK	Q-Register Rotate Connection
RLINK	RAM Rotate Connection
UBYTCLK	Upper Byte Clock
SOURCE - SCHEMATIC PAGE 6	
BR	Bus Request
BUSSEQ	Bus Sequence
BYTE	Byte-Sensitive Operation
CCLR	Controller Clear
CLRFIFO	Clear FIFO

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 6 (CONT.)	
DBUSØØ-15	Data Bus (internal)
IC1	Internal Bus Control 1
IDATA	Input Data
IDSL	Internal Density Select
IWARS	Internal Write Amp. Reset
MAR	Memory Address Register
NOPAR	No Parity
NPR	Non-Processor Request
ODATA	Output Data
PEDATA	PE Data
PEDO	PE Drop Out
PE STATUS	PE Status
PUP	Power Up
RBCLK	Read Buffer Clock
RBUF	Read Buffer
RDATA	Read Data
RDGATE	Read Gate
SO	Shift Out
SLECT	Select (register load)
TUCMD	Tape Unit Command
TUSTAT	Tape Unit Status
VECTR	Vector (read)

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 6 (CONT.)	
WBUF	Write Buffer
WDATA	Write Data
WGATE	Write Gate
SOURCE - SCHEMATIC PAGE 7	
CC	Condition Code
CSAØØ-07	Control Store Address
SOURCE - SCHEMATIC PAGE 8	
INT	Interrupt
IVSEL A,B	Internal Vector Select
PIOVCTR	PIO Vector
SRESET	Stored Reset
VCTR	Vector
SOURCE - SCHEMATIC PAGE 9	
CSAØØ-09	Control Store Address
SOURCE - SCHEMATIC PAGE 10	
DBUSØØ-Ø7	Data Bus
CLK	Clock
CLKFF	Clock Flip-Flop
IRE	Input Register Empty

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 10 (CONT.)	
MIRCLK	Micro Instr. Register Clock
ORF	Output Register Full
OSC	Oscillator Clock
TIMER	Timer Bit
TSTCLK	Test Clock
SOURCE - SCHEMATIC PAGE 11,12	
MIRØØ-47	Micro Instr. Register Bits
SOURCE - SCHEMATIC PAGE 13	
CHARCLK	Character Clock (PE)
CKSEL 1,2,4	PE Clock Select bits
MØ-6	Speed ROM bits
WTS	Write Strobe
800 CHAR	800 bpi Character Clock
SOURCE - SCHEMATIC PAGE 14	
FSL	Forward select (command)
FWD	Forward command (internal)
OVW	Overwrite (edit function)
RSL	Reverse Select (command)
RWC	Rewind Command

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 14 (CONT.)	
SLTØ-7	Drive Select lines
WDØ-7,P	Write Data lines
WNB	Write Enable
SOURCE - SCHEMATIC PAGE 15	
BOTP	Beginning of Tape
EOTP	End of Tape
FLPT	File Protect
IA16,17	Internal Addr. Expansion Bits
ONL	On-Line
PARITY	Parity
RWG	Rewinding status
USEL 1,2,4	Unit Select bits
WTDP	Write Data Parity
SOURCE - SCHEMATIC PAGE 16	
DBUSØØ-15	Data Bus (internal)
DSL	Density Select
NRZ	NRZI status
RDS	Read Strobe
RDY	Ready
RDST	Read Strobe interrupt

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 16 (CONT.)	
SPD	Speed select
TRDY	Tape Ready
WARS	Write Amplifier Reset
WDP	Write Data Parity
WDS	Write Data Strobe
SOURCE - SCHEMATIC PAGE 17	
ACDO	All Channels Dropped-Out
ATTN	Attention bit
DBUSØØ-15	Data Bus (internal)
FMK	File Mark
MCDO	Multiple Channel Drop-Out
PEID	Pe Identification Burst
PEP	PE Parity
SCDO	Single Channel Drop-Out
SOURCE - SCHEMATIC PAGE 18	
LOCKED	Locked
LOCKENA	Lock Enable
NODATA	No Data (gap)
REFCLK	Reference Clock
VERRA,B,C,D	Error Voltage Inputs

TC-131 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 19	
24 CLK	PE Read Clock (24X)
SOURCE - SCHEMATIC PAGE 20-22	
COØ-7,P	Carry Out X
FF1Ø-7,P	Flip-Flop 1X
PEDØ-7 P	PE Data X
RDØ-7,P	Read Data X
TRIBIT Ø-2	Tri-Bit-available lines
SOURCE - SCHEMATIC PAGE 23-25	
DOØ-7	Drop Out X
FF2Ø-7P	Flip-Flop 2X
GATE	Gate (for data transition)
LDØ-7,P	Window Counter Load X
MJRØ-7,P	Major Transition X
SIØ-7,P	Shift In X
STATE 1	State 1 (look for sync)
STATE 2	State 2 (data state)

CPU BITS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Ø
DEC MODE	← SECOND TAPE CHARACTER →								← FIRST TAPE CHARACTER →							
IBM (ANSI) MODE	← FIRST TAPE CHARACTER →								← SECOND TAPE CHARACTER →							
9-TRACK TAPE CHANNEL ASSIGNMENTS:	Ø	1	2	3	4	5	6	7	Ø	1	2	3	4	5	6	7

COMPUTER WORD - TAPE CHANNEL TRANSFER FORMATS

NOTES

UNPACKING AND RECEIVING INSPECTION

Before signing for your shipment which has arrived, use the delivery receipt to check off each package, accounting for all packages listed. Inspect the shipping containers immediately for evidence of mishandling during transit and note the damage on all copies of the delivery receipt before signing it. If a container is damaged, request that the carrier's agent be present when the package is opened.

Compare the packing list attached to the shipping container against your purchase order to verify that the shipment is correct. Notify the department issuing the requisition and the Purchasing department that the shipment has arrived.

Unpack the shipping containers and inspect each item for external or concealed damage such as broken controls and connectors, dented corners, bent panels, scratches, loose or damaged components, damaged subassemblies, etc. If any damage is found while unpacking, notify your supplier and the delivering carrier immediately and request inspection.

Retain the shipping container and packing material for examination in the settlement of claims or for future use. Be sure all minor parts and small items are found before discarding any shipping material.

western peripherals ™

NO. 1

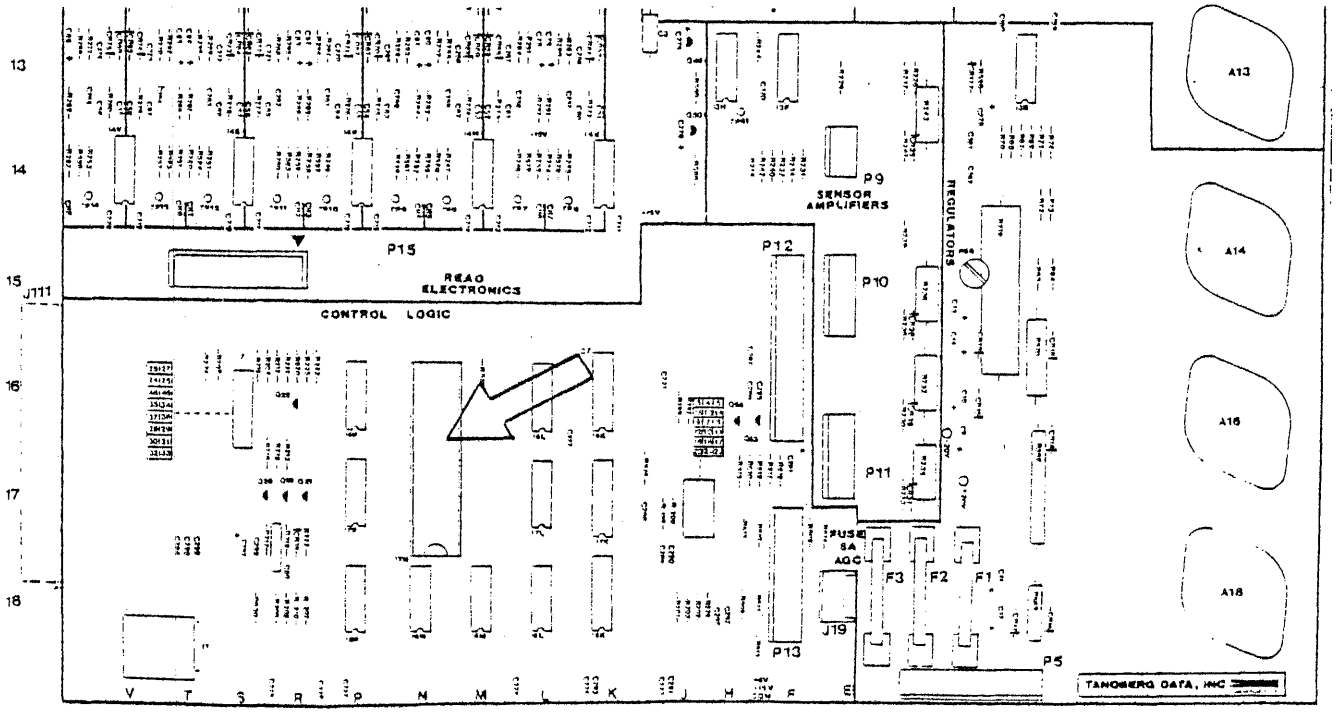
TECH TIPS

TITLE/DESCRIPTION: LRC Character Problems

PRODUCT/MODEL: Tape Drives - CDC Model 92149, Tandberg Model Series TDI 1050, and similar IDT models when used with TC-131 and TC-151 controllers.

SYMPTOM/ACTIVITY: These tape drives exhibit LRC Character problems in the write mode.

ACTION REQUIRED: On the large board of the tape drive, the mask/F8 chip (large device at 17N-see arrow) should be changed from part number 80-00290 to part number 80-00437.



PRINTED CIRCUIT BOARD ASSEMBLY
MAIN ELECTRONICS – STANDARD

DATE: 1-15-81

WARRANTY

WESTERN PERIPHERALS warrants articles of equipment manufactured by it to be free from defects in material and workmanship under normal use and service, its obligation under this warranty being limited to making good at its factory any article of equipment which shall within one year after delivery of such article of equipment to the original purchaser be returned intact to it, or to one of its authorized service stations, with transportation charges prepaid, and which its examination shall disclose to its satisfaction to have been thus defective; this warranty being expressly in lieu of all other warranties expressed or implied and of all other obligations or liabilities on its part, and WESTERN PERIPHERALS neither assumes not authorizes any other persons to assume for it any other liability in connection with the sale of its products.

This warranty shall not apply to any article of equipment which shall have been repaired or altered outside the WESTERN PERIPHERALS factory or authorized service stations, nor which has been subject to misuse, negligence or accident, incorrect wiring by others, or installation or use not in accord with instructions furnished by the manufacturer.

Vaction=224
CSR=172520

SPEED SETTINGS FOR TC-131P

Speed Pairs

Speed A	Speed B	Switch 1	Switch 2	Switch 3	Switch 4
125	75	Closed	Closed	Closed	Closed
125	45	Closed	Closed	Closed	Open
125	37.5	Closed	Closed	Open	Closed
125	25	Closed	Closed	Open	Open
75	45	Closed	Open	Closed	Open
75	37.5	Closed	Open	Open	Closed
75	25	Closed	Open	Open	Open
45	37.5	Open	Closed	Closed	Open
45	25	Open	Closed	Open	Closed
37.5	25	Open	Open	Closed	Closed

Control Paddleboard

Switch		
1	On	
2	Off	
3	Off	
4	On	Set on for high speed drive of speed pair (Speed A)
5	On	
6	Off	
7	On	
8	Off	

SPC Slot Modifications Requried

Remove wire on backplane at location CA1 to CB1 (this is the NPG jumper; must be removed when SPC slot is used for DMA devices)