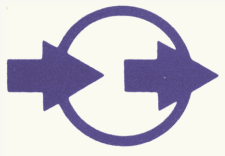


western peripherals™

Division of WESPERCORP™

14321 New Myford Road • Tustin, California 92680 • (714) 730-6250 • TWX: 910 595-1775 • Cable: WESPER

(1)

MODEL TC-151 TAPE CONTROLLER
HARDWARE MANUAL

PUBLICATION NUMBER

91000497 A

western peripherals

14321 MYFORD ROAD
TUSTIN, CALIFORNIA 92680

PRINTED IN U.S.A.

AUGUST, 1981

PREFACE

This manual provides information necessary for the installation and maintenance of the Western Peripherals Model TC-151 Tape Controller used with DEC LSI-11 computers.

The manual is divided into the following sections:

Section I	General Description
Section II	Installation
Section III	Programming
Section IV	Tape Interface
Section V	Computer Interface
Section VI	Theory of Operation
Section VII	Firmware
Section VIII	Maintenance
Appendix A	Signal Glossary

OTHER PUBLICATIONS

91000505	Western Peripherals Model TC-151 Tape Controller Logic Manual
91000448	Western Peripherals DEC-Compatible Diagnostic Manual

SECTION I

GENERAL DESCRIPTION

TABLE OF CONTENTS

PARA-GRAPH		PAGE
1.1	DESCRIPTION OF EQUIPMENT	1-1
1.3	DRIVE COMPATIBILITY	1-1
1.6	OTHER FEATURES	1-2
1.10	SPECIFICATIONS	1-3

SECTION I

GENERAL DESCRIPTION

1.1 DESCRIPTION OF EQUIPMENT

1.2 The Western Peripherals Model TC-151 is a magnetic tape controller/formatter which is hardware and software compatible with the DEC LSI-11 family of computer systems, providing both NRZI and phase encoded (PE) format capability on an embedded controller. Mounted in a standard, unmodified Q-SPC slot in a standard backplane system unit, the NRZI version of the controller consists of a single quad-wide board and contains a microprocessor plus all interface, control status, and formatting electronics to emulate the TM-11/TU-10 tape subsystem. Phase-encoded format capability is added with a dual-wide board mounted in front of the main controller board. The controller installs directly into available locations in the computer or expansion chassis. A short ribbon cable connects the two boards while three interface ribbon cables connect the controller to the tape drives. Adapter boards provide daisy-chaining capabilities for multiple drive installations.

1.3 DRIVE COMPATIBILITY

1.4 The controller will handle up to eight industry-compatible (IBM/ANSI) read-after-write (dual gap) tape drives. The controller is capable of handling tape drives in varying combinations of speeds, densities, and formats. The controller can select either of two switch selectable speeds from 25 to 125 inches per second.

1.5 Single or dual density NRZI and PE tape drives may be used with densities of 800 bpi NRZI 9-track, and 1600 bpi PE 9-track. Software density control is available for dual density operation. The controller is compatible with all industry-standard tape drives.

1.6 OTHER FEATURES

1.7 The Controller is compatible with the Q-bus and existing magnetic tape software, utilizing the standard TU-10/TM-11 magnetic tape registers. Data transfers are in a 16-bit word or 8-bit byte format via the Q-bus. In addition, enhancements of the standard registers provide many other features which add to the usefulness of the controller.

1.8 Both DEC (normal) and standard IBM (selectable) byte packing modes are available. This bit-selectable IBM packing mode allows reading and writing IBM/industry-compatible tapes. The automatic read and write on-the-fly feature allows non-stop operation when doing consecutive read or write operations. The controller writes and recognizes IBM/ANSI - compatible end-of-file tape marks. The controller provides an "EDIT" feature which allows a record anywhere on a previously recorded tape to be replaced with an updated record.

1.9 A 33-byte data buffer provides flexibility in assigning priorities when programming data transfers to the computer. The tape motion control, Cyclic Redundancy Check Character (CRCC)

and the Longitudinal Redundancy Check Character (LRCC) generation and checking, inter-record gap generation and status reporting are included. No screwdriver adjustments are required. While the controller can read or write only in the forward direction, it can space (or move to a new position) in both directions.

1.10 SPECIFICATIONS

1.11 The following information summarizes the specifications of the Tape Controller:

1. Computer Interface
   a. Compatibility - The controller is hardware compatible with the DEC LSI-11 computer systems, emulating the TM-11/TU-10 subsystem.
   b. Connects to the Q-bus through standard Q-SPC slots.
   c. Bus Loading - One bus load.
   d. Tape Commands*:
      Off Line
      Read
      Write
      Write EOF
      Space Forward
      Space Reverse
      Write with Extended Record Gap
      Rewind

e. Other Mode Controls:

Density Selection *

Byte Mode Selection *

Controller Clear

Unit Selection *

Interrupt Enable *

Command Execution (GO) *

Edit Mode *

For Diagnostics:

Check Character Read Selection *

Bad Tape Error Simulation *

f. Controller Status:

Status of the above-mentioned commands marked with an asterish (*) may be checked in addition to the following:

Illegal Command

End of File

Parity/Format Error

Bus Grant Late

End of Tape

Record Length Excessive (Read Mode)

Bad Tape Error

Non-Existant Memory

Drive On-Line

Beginning of Tape

Write-Protected

Drive Rewinding

Drive Ready

Error Summary

Controller Ready

Correctable Parity Error (Read)

PE Identification

For Diagnostics:

Tape Stopping After Rewind

10 KHz Clock

Gap Shutdown

Read/LRC Bits

2. Format Compatibility

Fully compatible with the industry-standard IBM/ANSI digital tape recording standard as described in ANSI specifications X3.22-1973 and X3.39-1973. Both DEC (normal) and standard IBM (selectable) byte packing modes are available.

3. Drive Compatability

a. Designed to be compatible with the industry standard drives

b. Read-after-Write only (dual gap head)

c. Single or dual density (operator or software switchable)

4. Tape Speed

25 ips, 37.5 ips, 45 ips, 75 ips, 125 ips

5. Format and Density

   a. NRZI 9-Track - 800 BPI

   b. PE 9-Track - 166 BPI (with TC-151P Controller)

6. Data Transfers

   a. 9-Track (1) DEC - compatible byte packing mode, (least significant byte first) - standard operating mode

   (2) IBM - compatible byte packing mode (most significant byte first).

   b. Bus transfers consist of 16-bit word transfers with 8-bit byte transfers to odd bytes at the beginning and/or end of the transfer.

7. Drive Configuration

   a. Up to eight drives in daisy chain configuration.

   b. One or two tape drive speeds.

   c. Single or dual densities on the daisy-chain.

8. Hardware

   a. One quad-wide printed circuit board for NRZI format capability mounted within the computer chassis (or expansion cabinet), containing a 2901 microprocessor and other advanced technology microcircuits.

   b. For phase-encoded format capability, one dual-wide board mounts in front of the main controller board and interconnects by ribbon cable.

c. Three interface cables and adapter boards per tape drive

9. Other Features

a. Edit mode for correcting pre-recorded tapes

b. Crystal controlled clocks

c. Phase-locked loop tracking in PE

d. No screwdriver adjustments

10. Error Handling

a. Generates and checks vertical parity, CRC, LRC, preambles and postambles

b. Detects dead track errors

c. Corrects PE single channel dropouts

11. Data Buffering

The internal buffer between the CPU and the tape drive provides 33 bytes of buffering to allow for transfers between the controller and the tape drive during the time that the CPU bus is unable to service the controller. During read operations, the buffer allows a check of false preambles in 9-track PE mode when a single dead track occurs. During read operations, the buffer must be emptied within the maximum times specified below, otherwise a data late error condition is detected.

Maximum Time After End of Record

Tape Speed	9-Track NRZI	9-Track PE
25.0 ips	1.50 ms	2.05 ips
37.5 ips	1.00 ms	1.37 ms
45.0 ips	0.83 ms	1.14 ms
75.0 ips	0.50 ms	0.68 ms
125.0 ips	0.30 ms	0.41 ms

12. Non-Stop "On-the-Fly" Tape Operation

    This feature provides continuous tape motion when consecutive tape commands require tape motion in the same direction on the same tape drive. Under these conditions, the controller will time through the inter-record gap (IRG) in the read mode, or will write the IRG in the write mode and execute the next command without stopping the tape.

13. Power Requirements

    a. Source - CPU or Expansion Chassis power supply

    b. + 5VDC $\pm$ 5% @ 9.0 amps

14. Physical Specifications

    a. Size - Two Standard DEC-sized board

        (1) One quad-wide board

        (2) One dual-wide board (for PE format)

    b. Weight

        (1) Controller boards 22 oz. (624 grams)

        (2) Cables & Adapters 26 oz. (737 grams) per drive

c. Environment

(1) Operation Temperature	0 to 55 Degrees C
(2) Storage Temperature	10 to 70 degrees C
(3) Relative Humidity	10 to 90 percent (without condensation)

SECTION II

INSTALLATION

TABLE OF CONTENTS

PARA-GRAPH		PAGE
2.1	INTRODUCTION	2-1
2.3	PREPARATION	2-1
2.5	System Components	2-2
2.6	SYSTEM SET-UP	2-3
2.8	Tape Speed Selection	2-5
2.9	Controller Board Installation	2-6
2.10	Priority Jumpers	2-7
2.11	Controller Cable Connections	2-8
2.13	TAPE DRIVE INSTALLATION	2-8
2.14	Adapter Paddleboard Setup	2-8
2.15	Terminators	2-8
2.16	Configuration Switches	2-8
2.17	Drive Select Jumpers	2-11
2.18	Tape Drive Interconnections	2-11

SECTION II

INSTALLATION

2.1 INTRODUCTION

2.2 This section provides the necessary information to successfully set up and install the TC-151 Tape Controller into the DEC LSI-11 computer system. This information is essential for the initial installation and will also be valuable when the controller is reinstalled after repair. The controller consists of two printed circuit boards which plug into the slots in a standard Q-SPC-wired system unit (backplane) which may be in the computer mainframe or expansion chassis. Cable Adapter Paddleboards are provided to adapt the universal controller interface cables to the specific connector requirements of each drive (to be specified by the customer at the time of purchase). All DC power required for the operation of the controller is received from the power supply of the host computer or chassis via the backplane.

2.3 PREPARATION

2.4 Locate the position in the computer where the controller will be installed. Remember that the position of the system unit determines priority for DMA and interrupt activity. The tape controller usually works well if placed anywhere in the system. Check the cabling distance to the first drive and to each daisy-chained drive, verifying that all cable lengths will be adequate. Refer to the tape drive manual to install the

tape drives. The computer and the tape drives must be prepared for operation before the controller can be expected to operate properly.

WARNING: INCORRECT INSTALLATION WILL CAUSE DAMAGE TO THE SYSTEM WHEN POWER IS APPLIED

2.5 SYSTEM COMPONENTS. Do not discard any shipping materials until all parts have been checked off on the packing list and any concealed damage has been reported to the carrier. Check the equipment supplied to ensure that all necessary items are included:

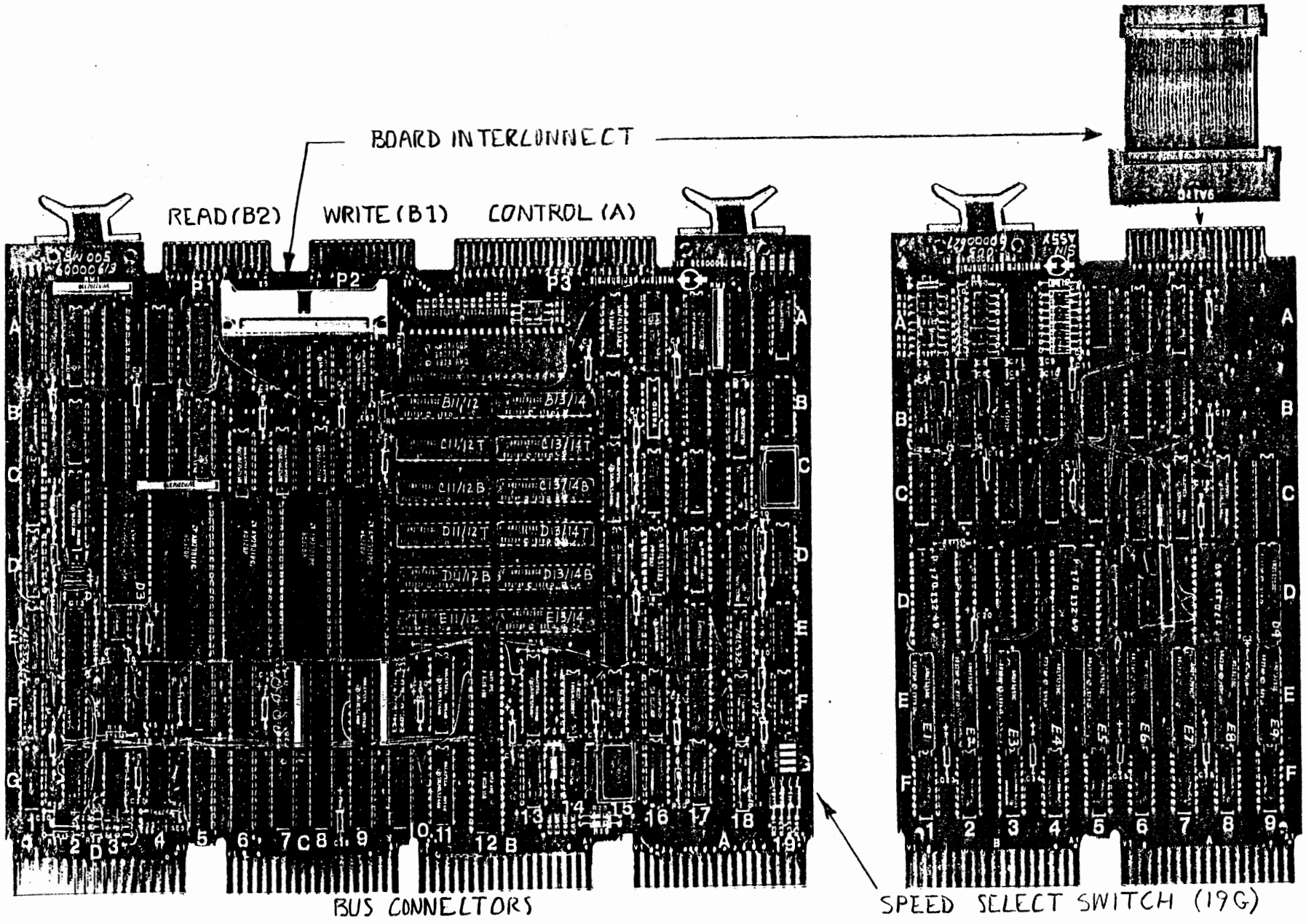
1. Controller Boards (two) with interface cable
2. Optional Standard-type backplane system unit and associated power cable. (Molex plug must match the power supply connector.)
3. Drive Cables (3), one set per drive:
   Control cable
   Write cable
   Read cable
4. Adapter Paddleboards (3), one set per drive:
   Control Paddleboard
   Write Paddleboard
   Read Paddleboard
   Including:
      Terminators (on the Write and Control Paddleboards)
      Drive Select Jumpers (on the Control Paddleboard)
      See Figure 2-6 for part identification.

5. Program tapes:
   a. Diagnostic program tape
   b. Reliability program tape
6. Documentation:
   a. Hardware manual
   b. Logic manual
   c. Diagnostic manual
7. Other items which must be available:
   a. Tape drives
   b. Computer
   c. Standard Q-SPC backplane system unit and associated power cable. (molex plug must match the power supply connector.)
   d. Q-bus terminator, cables/jumpers
   e. Loading device for diagnostics

2.6 SYSTEM SET-UP

2.7 The tape system must be set up properly either when installing the system or after servicing. Proper set-up includes: Setting the speed switches for the speed of the drives and checking backplane priority signals. Each Tape Drive Adapter Paddleboard must have the proper termination (on the last drive) and the Configuration Switch setup. Installation is complete when the system components are plugged in and interconnected. A recheck and inspection of the installation ensures that no item is overlooked. The procedures for setup and installation are in the paragraphs that follow. Locations of installation features on the controller boards are shown in Figure 2-1.

FIGURE 2-1 INSTALLATION FEATURES



2.8 TAPE SPEED SELECTION. Tape drive speed is selected on the controller by the setting of four switches located by the setting of four switches located in a switch pack at location 19G. Speed selection provides two tape speeds for both the NRZI and PE modes. Table 2-1 provides the required speed settings for various combinations, (If only one speed is used, it may be selected on either speed A or speed B.)

TABLE 2-1 SPEED SELECTION SWITCHES

TAPE SPEEDS (ips)		SWITCHES			
A	B	1	2	3	4
25	37.5			ON	ON
25	45		ON		ON
25	75	ON			
25	125	ON	ON		
37.5	45		ON	ON	
37.5	75	ON			ON
37.5	125	ON	ON		ON
45	75	ON		ON	
45	125	ON	ON	ON	
75	125	ON	ON	ON	ON

ON = CLOSED, ALL OTHERS OFF (OR OPEN)

2.9 CONTROLLER BOARD INSTALLATION. Referring to Figure 2-2, place the controller boards into any convenient location of the system unit. Ensure the boards are oriented correctly (notches on the board connectors must fit the ridges of the system unit), and are seated fully.

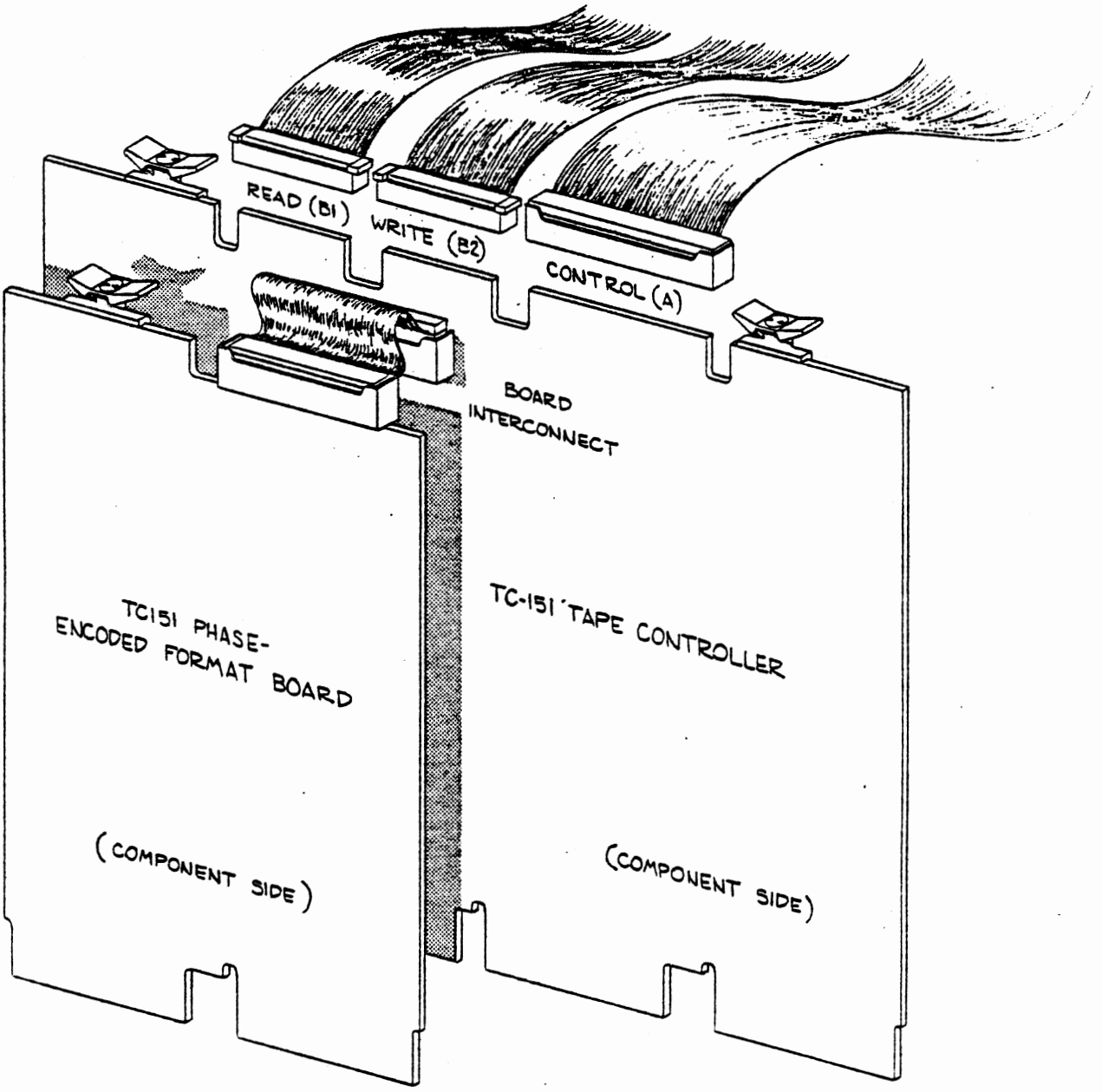


FIGURE 2-2 INSTALLATION - CONTROLLER AND CABLES

2.10 PRIORITY JUMPERS. The DMA Grant and Interrupt Acknowledge lines are daisy-chained to the I/O devices and may be jumpered together by plug-in devices or wires at A, C, and E sections of each Q-Bus connector slot (pin M2 to N2 and pin R2 to S2). Remove any such jumpering from the slot which has been selected for the Controller and any other Q-Bus devices. Any unused slot on the Q-Bus should be jumpered so that the priority lines are daisy-chained, continuously, from the microprocessor to the Q-Bus terminator. Western Peripherals supplies part number 76000223 for Q-Bus jumpering. (See Figure 2-3.)

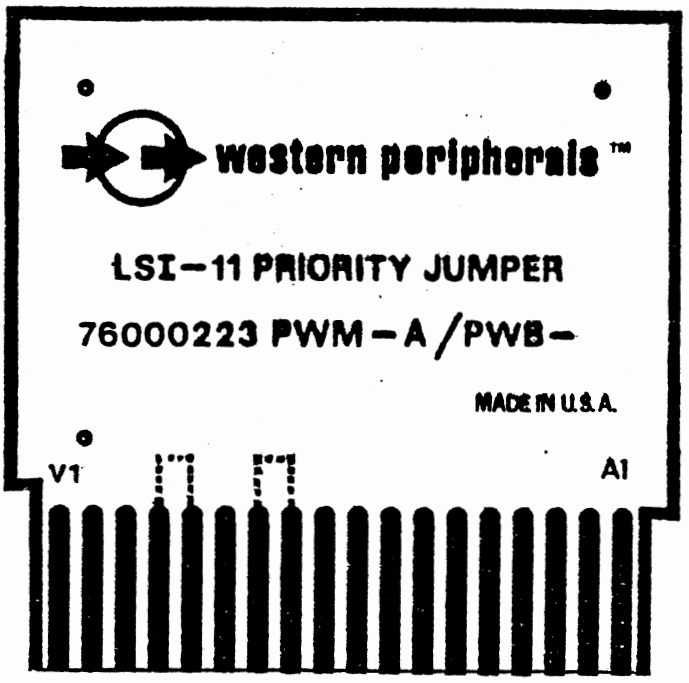


Figure 2-3 Bus Priority Jumper

2.11 **CONTROLLER CABLE CONNECTIONS.** Locate the following cables:

Description	Conductors	Controller-End Marking
Tape Read Cable	26	Top B2
Tape Write Cable	26	Top B1
Tape Control Cable	50	Top A

The ribbon cables are keyed to prevent incorrect connections. Check the ribbon cable connectors to assure that all keys are in place.

2.12 Install the Read, Write, and Control cables (in that order) onto the controller connectors as shown in Figure 2-2. The cables will exit toward the solder side of the boards.

2.13 **TAPE DRIVE INSTALLATION**

2.14 **ADAPTER PADDLEBOARD SETUP.** Locate a set of three Adapter Paddleboards for each tape drive. The Adapter Paddleboards for each drive require proper setup before installation. Setup includes proper termination, switch settings, and installation of drive selection jumper plugs.

2.15 **TERMINATORS.** Consulting the tape manuals for details, remove all termination devices from each drive. Remove the terminators from the Write and Control Adapter Paddleboards, except the Adapter Paddleboards on the drive located farthest from the controller. See Figure 2-5. Ensure that the last Adapter Paddleboards have the terminators installed as shown.

2.16 **CONFIGURATION SWITCHES.** Set the switch module on each Control Paddleboard according to the configuration requirements of the tape drive. Switch settings are given in Table 2-3.

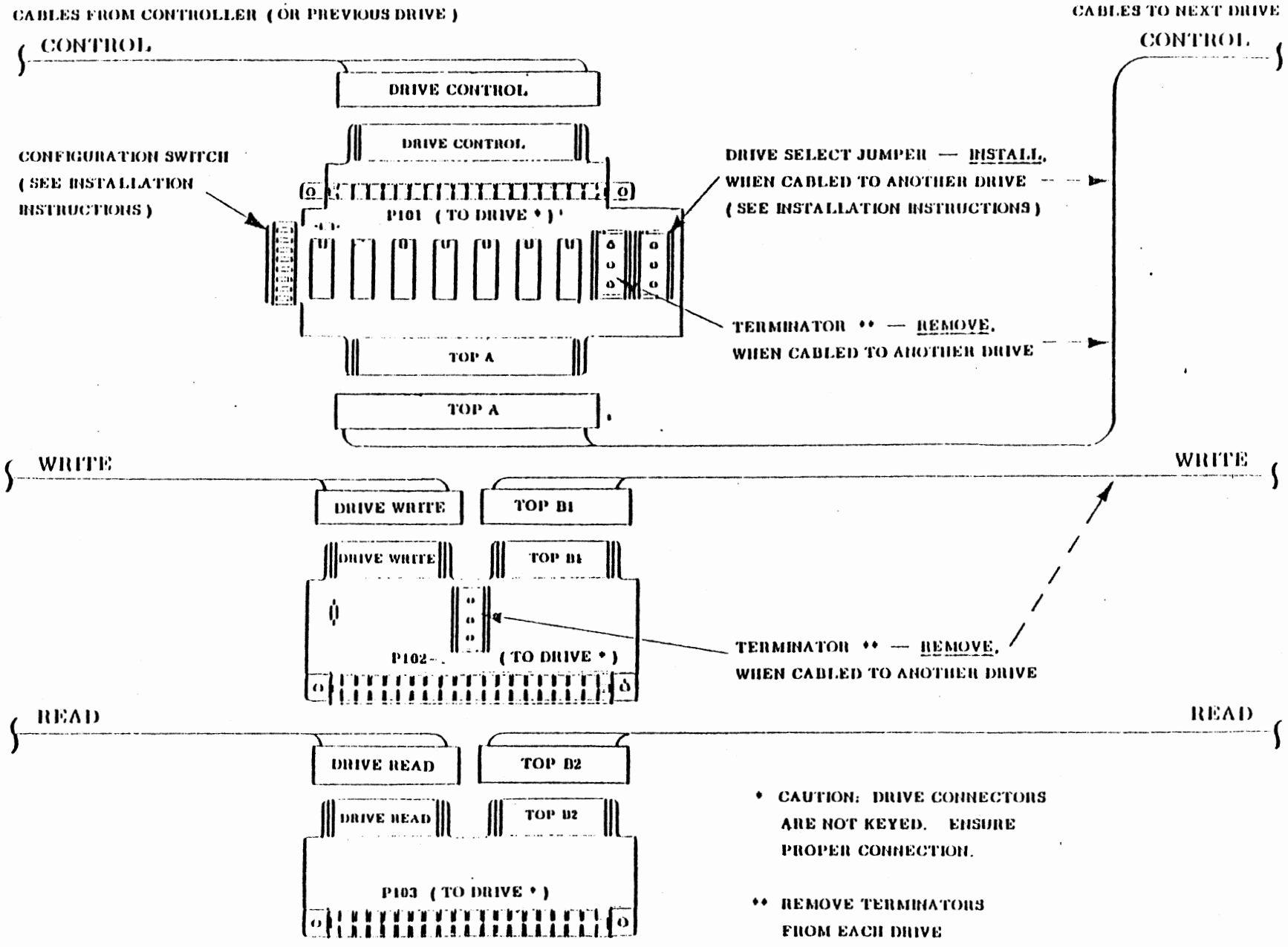


Figure 2-5. Details of Adapter Installation

SWITCH NUMBER	SETTING
1	"ON" for normal operation "OFF for H.P. drives and for some Pertec models
2	OFF
3	OFF
4	ON - For HIGH SPEED drive (Controller speed B) OFF - For LOW SPEED drive (Controller speed A)
5	ON
6	"ON" for 9-track NRZI-only drives "OFF" for all other drives
7	"ON" for either dual density or PE drives made by Kennedy, Digidata, or Qantex "OFF" for all other drives
8	"OFF"

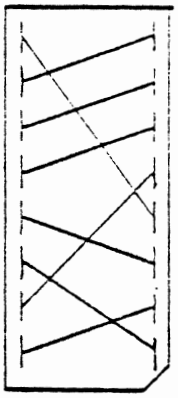
Reference Schematic Number 122036

Table 2-3 Configuration Switches

2.17 **DRIVE SELECT JUMPERS.** Ensure that the correct Drive Select Jumper is installed in the Control Paddleboards. The last drive does not require a Drive Select Jumper (leaving one installed will have no effect).

1. For tape drives without front panel unit select switches, use jumper part number 122012 as shown in Figure 2-6.
2. For tape drives with front panel unit select switches:
   a. Use jumper part number 122010 as shown in Figure 2-6.
   b. On drives with Unit Select Switches that receive the select lines from J101, ensure Control Paddleboard Jumpers are installed from P to R (factory etch), N to M, E to F, and G to H. See Table
   c. On drives with externally connected Unit Select Switches, connect as shown in Table

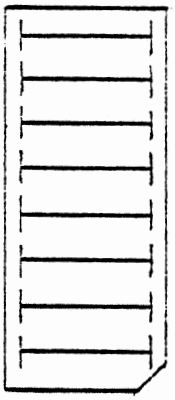
2.18 **TAPE DRIVE INTERCONNECTIONS.** Locate a set of three ribbon cables for each drive (one set is connected to the controller). Check that each connector has its key in place and connect the cables as shown in Table 2-5 and Figures 2-7 and 2-8.



NON-SELECT JUMPER (PN 122012)

For daisy-chained drives

Without front panel Unit Select switches.

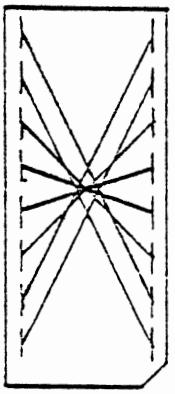


UNIT SELECT JUMPER (PN 122010)

For daisy-chained drives

with Unit Select switch

(Except fourth tape unit)



UNIT SELECT JUMPER (PN 122011)

For daisy-chained drives

with unit select switches

(Install in fourth tape unit)

NOTE: No jumper plug is required on the last tape unit or for single drive installations. However, it should remain in the board for future expansion of the system.

Figure 2-6 Drive Select Jumpers

NOTE: APPLIES TO DRIVE SELECT THUMBWHEEL OPTION ONLY.

Drive Select Line:	Add Jumper:	To Activate J101 Pin:	Connect External Switch To:
Select Ø	P-R (Etch)	J	A
Select 1	N-M	A	B
Select 2	E-F	18	D
Select 3	G-H	V	C
		L	(return line from switch)

Table 2-4 Control Adapter Select Options

	(Sequence is repeated for each drive)					
	Cables		Paddleboards		Cables	
Controller Board	Controller End	Drive End	Controller End	Daisy Chain End	Controller End	Drive End
Board 2	Top A	Drive Control	Drive Control	Top A	Top A	Drive Control
Board 3	Top B1	Drive Write	Drive Write	Top B1	Top B1	Drive Write
Board 4	Top B2	Drive Read	Drive	Top B2	Top B2	Drive Read

Table 2-5 Connector Legends and Cable Connections

2.19 Connect the Control, Write and Read Adapter Paddleboard connectors to J101, J102, and J013, respectively, on the tape transport. (Reference the tape drive manual for details.) Connect the paddleboards to the drive with care. The green connectors are not keyed to the drive connectors. Therefore, it is possible to (1) install the connector backwards or (2) to place the Adapter Paddleboard on the wrong drive connector (e.g., Read and Write Connectors reversed.) Avoid incorrect connection by (1) verifying the function of each drive connector and (2) physically checking the pin orientation of the mating connectors. If possible, secure the paddleboard connectors to the drive connectors with screws. Neatly dress and tie all cables so the installation appears neat and professional.

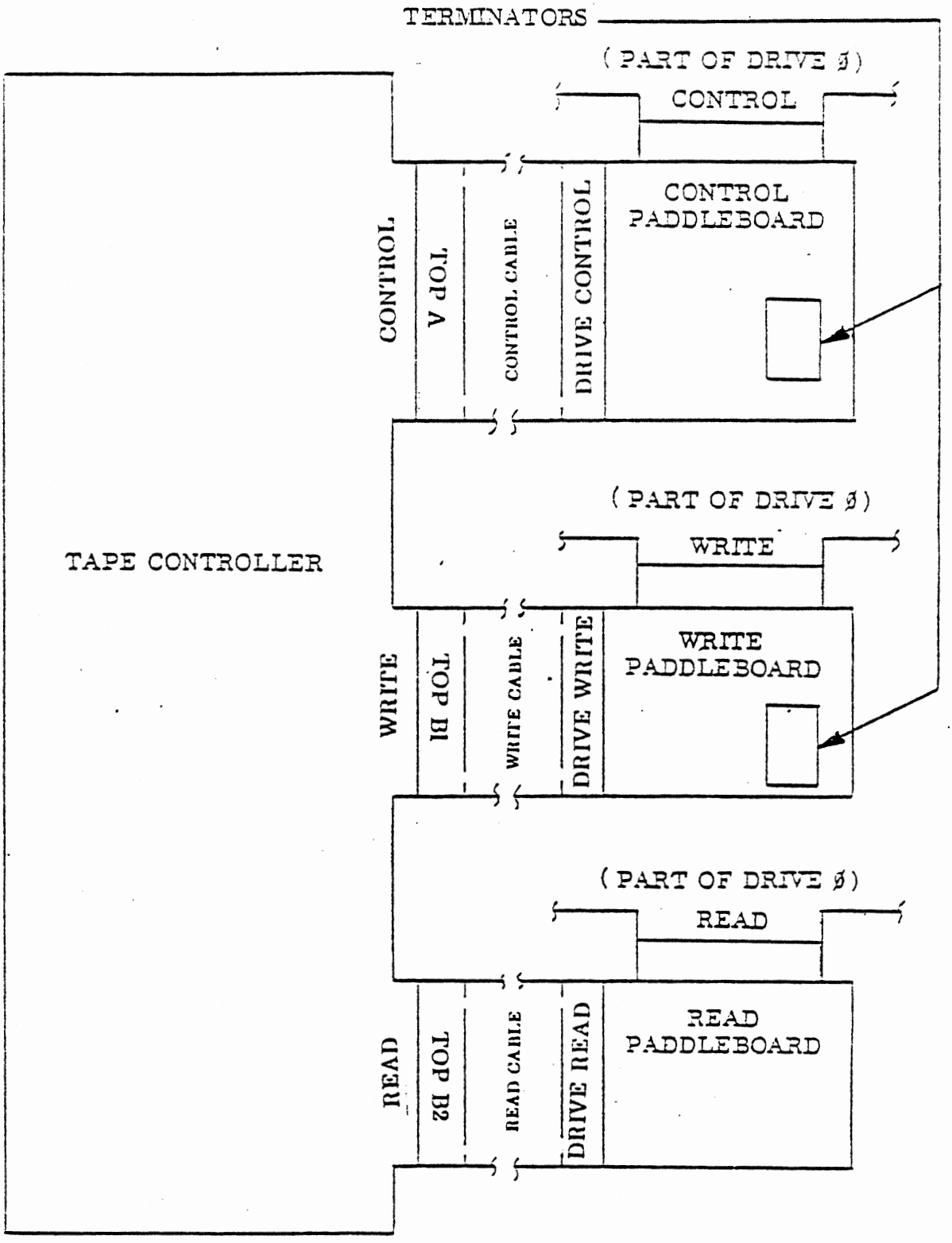


Figure 2-7. Single Tape Drive Connections

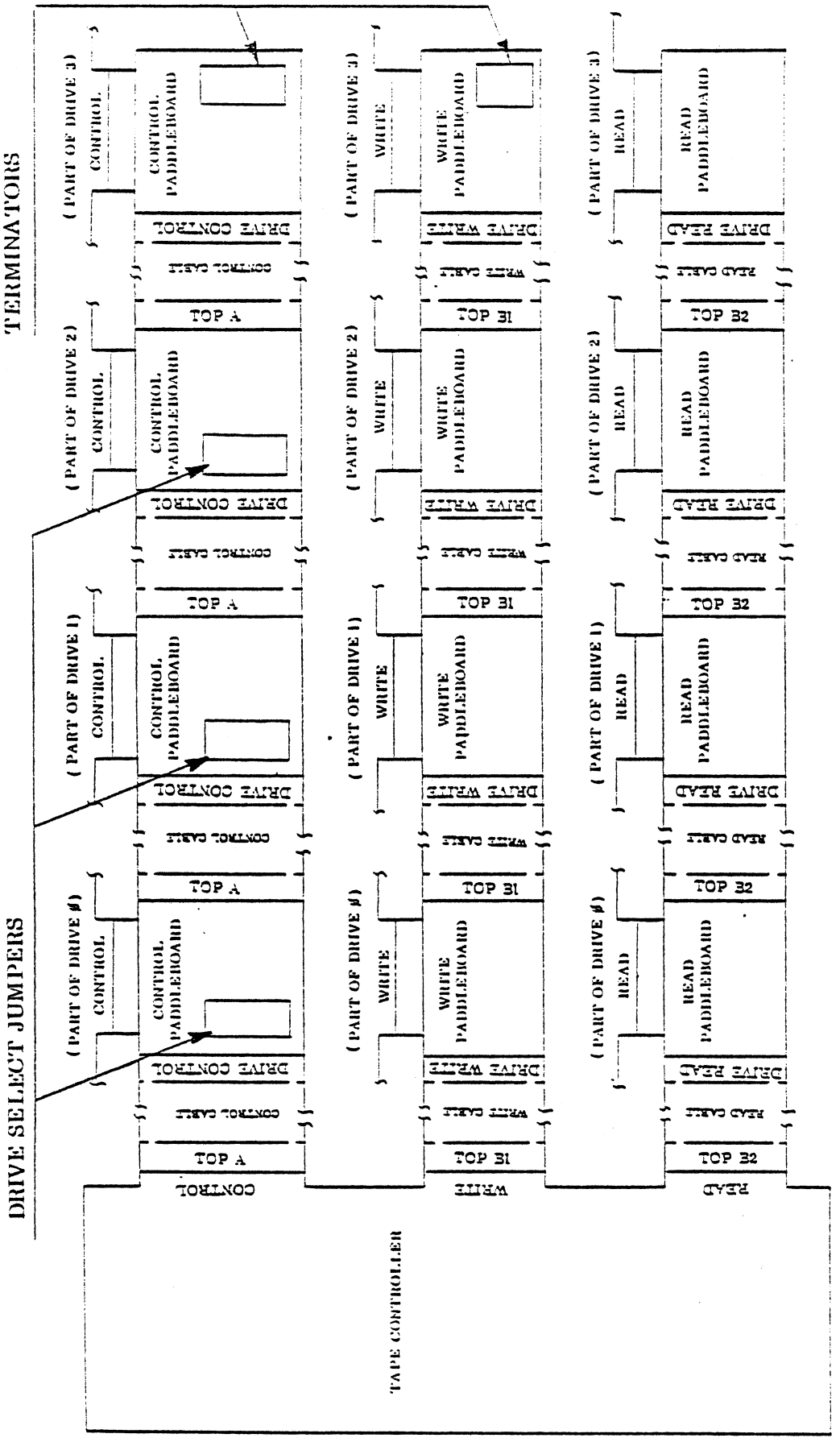


Figure 2-8. Tape Drive Daisy-Chain Connections

SECTION III

PROGRAMMING

TABLE OF CONTENTS

PARA-GRAPH		PAGE
3.1	GENERAL	3-1
3.3	PROGRAMMED OPERATIONS	3-1
3.5	Operation As A Slave Device	3-1
3.6	Operation As A Master Device	3-2
3.7	CONTROLLER REGISTERS	3-2
3.8	Register Addressing	3-2
3.9	Status Register (MTS)	3-2
3.10	Command Register (MTC)	3-6
3.11	Byte/Record Count Register (MTBRC)	3-11
3.14	Current Memory Address Register (MTCMA)	3-12
3.15	Data Buffer (MTD)	3-12
3.16	TU-10 Read Lines (MTRD)	3-12
3.17	PROGRAM FLOWCHARTS	3-14

SECTION III

PROGRAMMING

3.1 GENERAL

3.2 This section contains machine-level programming reference information which describes the registers of the controller. Also contained in this section is information on the operation of the controller, addressing, data transfers, and interrupts. This information will be useful in understanding the operating systems as well as the diagnostic programs. A working knowledge of machine-level programming, along with reference to the information contained in this section, will allow the Customer Engineer to create small diagnostic programs for testing specific functions of the controller.

3.3 PROGRAMMED OPERATIONS

3.4 The DEC LSI-11 computer controls devices differently than most other computer systems. Since registers in peripheral devices are assigned addresses on the bus similar to memory, all instructions that address memory locations are, in effect, I/O instructions. Registers in devices can take advantage of all the arithmetic power of the processor. There is no limit to the number of registers that a device may have, providing great flexibility in the design and control of peripheral equipment.

3.5 OPERATION AS A SLAVE DEVICE. All command and status information is transferred with the CPU acting as the master device and the controller acting as the slave. The individual bits within the Command Register control the operations of the device. For example, the command to make the tape system read a block from tape is provided by properly setting bits 1 through 3 in the Command Register. Status conditions are also handled by the assign-

ment of bits within the registers. All command and status information is written or read by program instructions. Indications of operation complete can be through examination of the status and command registers or by utilizing the system interrupts.

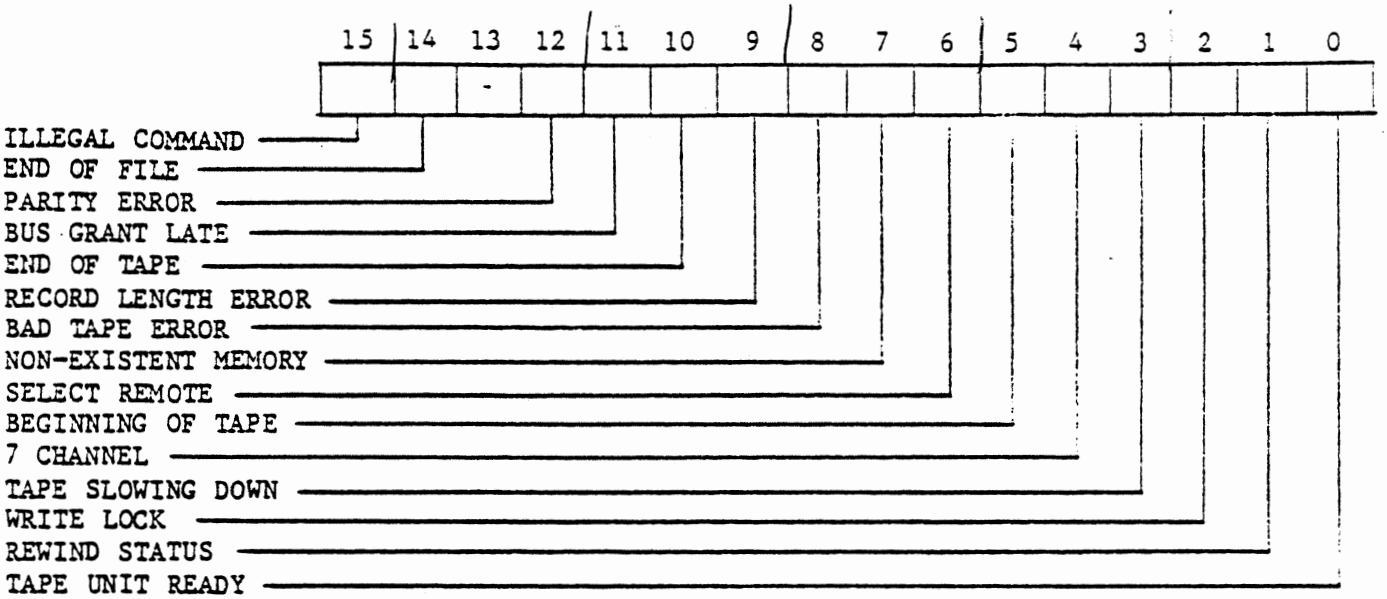
3.6 OPERATION AS A MASTER DEVICE. Once a function command has been issued to the controller, the operation is executed by the controller, utilizing DMA bus transfers to move the data to or from the memory. The Byte/Record Counter Register and the Current Memory Address Register are updated throughout the DMA activity. At the conclusion of an operation, completion is indicated to the CPU through the status bits and also an interrupt (if enabled). The standard interrupt vector (224 octal) is used.

3.7 CONTROLLER REGISTERS

3.8 REGISTER ADDRESSING. The registers of the tape controller occupy bus address locations 772 520 through 772 532 and are addressed by the CPU with the controller being the slave device. These addresses are placed on the bus in the same way that memory is addressed. The controller latches the address until the completion of the transfer.

3.9 STATUS REGISTER (MTS) 772 520. The status register contains only read bits, providing the CPU with status indications from both the tape drive and the controller.

REGISTER BIT ASSIGNMENTS:



1. MTS BIT 15 ILLEGAL COMMAND (ILL COM) - When an illegal command is received, the CU RDY bit remains true, and the command is disregarded. The Illegal Command bit is set for any of the following conditions and sets the ERR bit in the Command Register:
   a. Any tape command initiated during a tape operation (CU RDY bit is false)
   b. Any tape command where the selected drive is not on-line (Select Remote bit is false).
   c. Any write command on a drive which is file protected.
   d. The drives Ready status line going false during an operation.
2. MTS BIT 14 END OF FILE (EOF) - The EOF bit is set when a file mark character is detected during a Read, Space Forward or Space Reverse operation. The EOF bit sets the ERR bit in the Command Register.
3. MTS BIT 13 ODD LENGTH RECORD (OLR) - The OLR status indicates that part of the final word transferred to memory contains insignifi-

cant zeros filled by the controller after reading a record which did not fill the final word in the data register.

4. MTS BIT 12 PARITY ERROR (PAE) - The Parity Error bit is set when the controller detects a parity error, LRC error, or Postamble error during a Read, Write, or write with Extended Record Gap operation. The PAE bit does not affect the transfer of data. During a Write operation, the entire record will be transferred onto tape or in a Read operation, the entire record will be transferred to memory. The PAE error bit will set the ERR bit in the Command Register.

5. MTS BIT 11 BUS GRANT LATE (BGL) - The Bus Grant Late bit is set when the controller overflows (or empties) its internal buffer and information is lost during an operation. This condition causes an immediate termination of the Read or Write operation in progress. This bit will also be set during a Read operation when the internal buffer of the controller is not emptied before the tape begins to stop. The ERR bit in the Command Register will be set when the BGL bit is true.

6. MTS BIT 10 END OF TAPE (EOT) - The End of Tape bit is set when the EOT marker is encountered while the tape is moving in the forward direction. The bit will be reset when the EOT marker is passed while performing a Rewind or Space Reverse operation. The ERR bit in the Command register will be set when the EOT bit is true.

7. MTS BIT 9 RECORD LENGTH ERROR (RLE) - The Record Length Error bit will be set during a Read operation when the length of the record being read exceeds the memory allocation as indicated by the Byte/Record Counter. When the Byte/Record Counter indicates the

end of the memory allocation, data transfer will stop and the controller will continue to advance the tape to the next interrecord gap. A Record Length Error stops the incrementing of the Byte/Record Counter and the Current Memory Address Register and sets the ERR bit in the Command Register.

8. MTS BIT 8 BAD TAPE ERROR (BTE) - The Bad Tape Error bit sets when a character is detected (read strobe) during the gap shut-down (or the slowing down) for all operations (except rewind). When a Bad Tape Error is detected, the ERR bit in the Command Register is set.

9. MTS BIT 7 NONEXISTENT MEMORY NXM) - The Nonexistent Memory bit is set during direct memory operations (when the controller is bus master and is performing data transfers with the bus) and the controller does not receive a Slave Sync response within 14 microseconds after it issues the Master Sync signal. When the Nonexistent Memory error bus time-out is detected, the Read or Write operation is terminated, stopping the tape in the interrecord gap, and setting the ERR bit in the Command Register.

10. MTS BIT 6 SELECT REMOTE (SELR) - The Select Remote bit is set when the addressed tape drive is on line and cleared when the addressed tape unit is off line, powered off, or disconnected.

11. MTS BIT 5 BEGINNING OF TAPE (BOT) - The Beginning of Tape bit is set when the tape drive detects the Load Point mark at the beginning of the magnetic tape.

12. MTS BIT 4 7 CHANNEL (7 CH) - The seven channel bit is not used.

13. MTS BIT 3 SLOWING DOWN (SDWN) - The Tape Slowing Down (or Settle Down) bit is set whenever the tape unit is stopping after a rewinding operation.

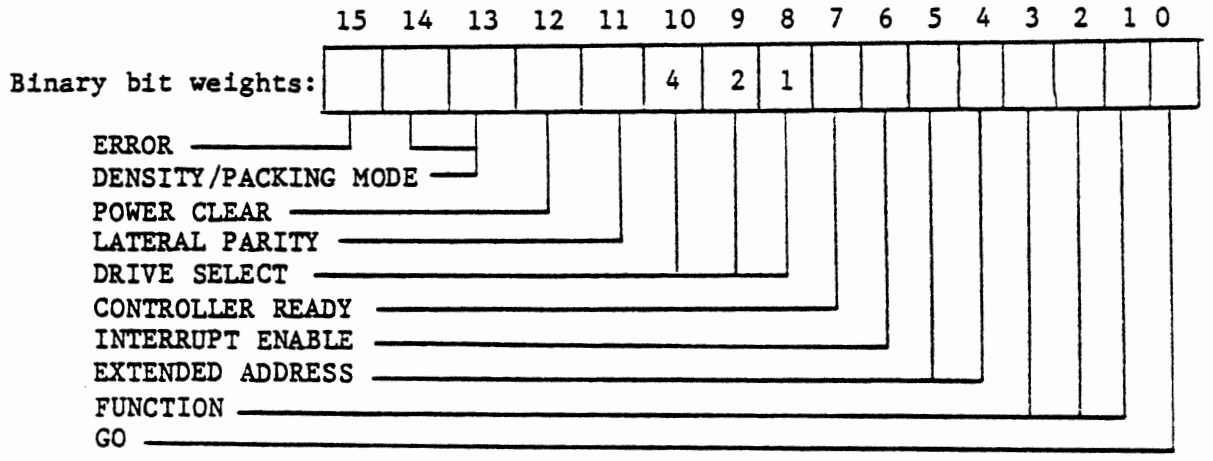
14. MTS BIT 2 WRITE LOCK (WRL) - The Write Lock bit is set to prevent the software from attempting to write information on the tape when the operator has removed the write-enable ring from the supply reel on the tape drive.

15. MTS BIT 1 REWIND STATUS (RWS) - The Rewind Status bit is set by the selected drive when it receives a Rewind command from the controller or operator panel and is cleared by the selected drive when the tape arrives at BOT, completing the Rewind operation.

16. MTS BIT Ø TAPE UNIT READY (TUR) - The Tape Unit Ready bit is set when the selected tape unit is stopped and is cleared when the controller begins to execute a function command.

3.10 **COMMAND REGISTER (MTC) 772 522.** This register receives operational commands from the CPU and provides status information from the controller and the tape drive.

COMMAND REGISTER BIT ASSIGNMENTS:



1. MTC BIT 15 ERROR (ERR) - Set as a function of bits 7-15 of the Status Register (MTS) being set. This bit is cleared as the result of an Initialize or a Go command to the tape unit.

2. MTC BITS 14, 13 (DEN 8, DEN 5) N - These density select bits are not used by the controller. Density is controlled by the tape drive or by bit 10 of this register.

3. MTC BIT 12 POWER CLEAR (PCLR) - This bit provides the means for the processor to clear the controller and the tape drives without clearing other devices in the system. The PCLR bit is always read back by the processor as zero.

4. MTC BIT 11 LATERAL PARITY (PEVN) - This bit is applicable only to 7-track operations, and is ignored by the controller.

5. MTC BITS 10-8 DRIVE SELECT (SLT 1, 2, 4) - These bits specify one of the eight possible tape units. All operations defined in the MTC register and all status conditions defined in the MTS register refer to the unit indicated by these bits. Drive selection of the last 4 drives may be forfeited by jumpers which use bit 10 either to select the IBM pack mode (see MTRD bit 10) or to select high density mode (1600 bpi PE).

DRIVE NO.	LOGICAL DRIVE ADDRESS	DRIVE SELECT LINES SL1 (Bit 8)	SL2 (Bit 9)	SL4 (Bit 10)*	
1	Ø	False	False	False	(NRZI mode or DEC packing)
2	1	True	False	False	
3	2	False	True	False	
4	3	True	True	False	
5/1*	4/0*	False	False	True	(PE mode or IBM packing)
6/2*	5/1*	True	False	True	
7/3*	6/2*	False	True	True	
8/4*	7/3*	True	True	True	

*BIT 10 MAY BE JUMPERED TO SELECT PE MODE OR IBM PACKING.

6. MTC BIT 7 CONTROLLER READY (CUR) - This bit is cleared at the start of a tape operation and is set at the end of a tape operation to indicate that the controller is ready to accept a new command.

7. MTC BIT 6 INTERRUPT ENABLE (INT ENB) - When this bit is set, an interrupt occurs whenever either the Controller Ready bit or the ERR bit goes true or whenever a rewinding tape unit arrives at BOT. In addition, an interrupt occurs for an instruction that sets the INT ENB bit but does not set the GO bit.

8. MTC BITS 5, 4 EXTENDED BYTE ADDRESS (YBA 17, XBA 16) - These bits access the two most significant bits of Current Memory Address Register, providing an 18-bit memory addressing capability.

9. MTC BITS 3 - 1 FUNCTION BITS - These bits select one of eight command functions.

Bit 3	Bit 2	Bit 1	
0	0	0	Off Line
0	0	1	Read
0	1	0	Write
0	1	1	Write EOF
1	0	0	Space Forward
1	0	1	Space Reverse
1	1	0	Write/E.R.G.
1	1	1	Rewind

a. Off Line Command. This command, which places the selected drive off-line, is usually preceded by a rewind command after completing all operations on the reel of tape. The controller does not go Busy, leaving it free for use with other drives in the system.

b. Read Command. The program must specify a byte count (in twos complement - or negative - form) and an initial address. The controller reads a single record from tape and sends the data via DMA operations to the locations specified by the Address Register until the EOR gap is encountered or the Byte Counter overflows, whichever occurs first. For operations with variable length records, a large byte count ensures that the entire record will be read. The length of the record of unknown size can then be determined after it is read by comparing the Byte Counter at the end of the operation to its initial setting. The setting of BGL status during the record indicates that information has been lost, but data transfers

continue until the byte counter overflows or the EOR gap is detected.

c. Write Command. The program must specify a (negative) byte count and an initial bus address. If Write Lock is true, GO sets Illegal Command, and the controller rejects the operation. Otherwise, the Controller makes an immediate data request for the first word, and writes the data it receives from the locations specified by the address counter onto the magnetic tape until either the byte counter overflows or a BGL or NXM error occurs, at which time the controller terminates the record.

d. Write End of File Command. Unless Write Lock is set, GO starts the controller into operation to write a file mark. With Write Lock true, the command is rejected.

e. Space Forward Command. The program must specify a (negative) byte count equal to the number of records to be spaced. The controller spaces forward over the given number of records unless it encounters a file mark or the end of tape. To space over a file, the program can simply give a zero (maximum) byte count.

f. Space Reverse Command. The program must specify a (negative) byte count equal to the number of records to be spaced. If BOT is true, GO sets the Illegal Status bit, and the controller does not go into operation. Otherwise, the controller spaces reverse over the given number of records, but it stops the tape automatically upon encountering a file mark or the Load Point. To space over a file, the program can simply specify a zero (maximum) byte count.

g. Write with Extended Record Gap Command. The operation of this command results in a three and one-half inch length of tape being erased before the data is written. This provides a method of erasing a bad record from a damaged portion of tape before rewriting the data farther down on the tape. A Space Reverse One Record operation generally precedes this command.

h. Rewind Command. This command initiates a rewind operation in the addressed tape drive, which rewinds the tape onto the supply reel at high speed, and stops at BOT. The controller does not go Busy, leaving it free for further use by the program during the rewind operation.

3.11 BYTE/RECORD COUNT REGISTER (MTBRC) 772 524. The MTBRC is a 16-bit binary counter which is used to count bytes of memory during Read or Write operations, or to count records in a Space Forward or Space Reverse operation. When used in a Write or Write with Extended Record Gap operation, the MTBRC is initially set by the program to the 2's compliment of the number of bytes to be transferred from memory to tape. The MTBRC increments by one immediately after each byte memory access or by two after each word transfer. The MTBRC overflows to zero after the last byte of the record has been read from memory. Bus transfers are terminated by this byte count zero condition.

3.12 When the MTBRC is used in a Read operation, it is set to the 2's complement of a number equal to or greater than the maximum expected record length, indicating the memory allocation for the read data. A Record Length Error (RLE) occurs when the actual record length is greater than the allocated memory, as indicated by the MTBRC overflowing before the EOR gap is detected.

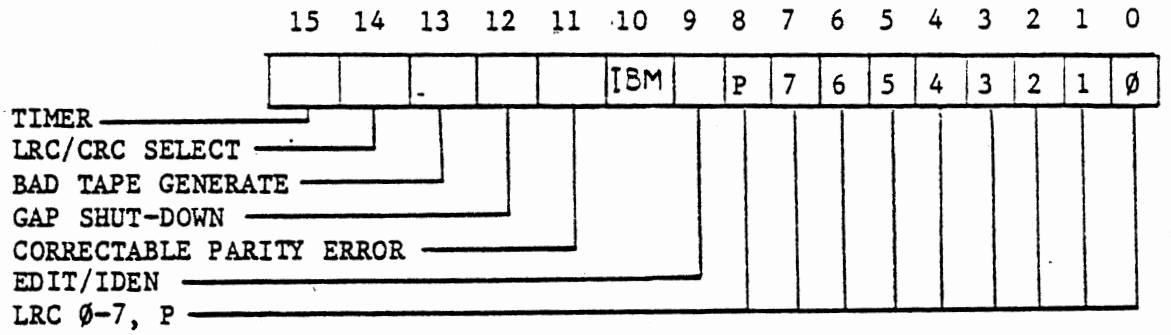
3.13 When the MTBRC is used in a Space Forward or Space Reverse operation, it is set to the 2's compliment of the number of records to be spaced over. It is incremented by one each time a record passes the head whether the tape is moving in the forward or reverse direction.

3.14 CURRENT MEMORY ADDRESS REGISTER (MTCMA) 772 526. The MTCMA register contains 18 memory address counter bits. It is used in DMA operations to provide the memory address for data transfers in Read Write and Write with Extended Record Gap operations. Prior to issuing a command, the MTCMA is set to the memory address to be used for the first data transfer. The MTCMA is incremented by one immediately after each byte transfer and by two after each word transfer. Thus, at any instant of time, the MTCMA points to the next higher address than the one which had most recently been accessed. When the entire record has been transferred, the MTCMA contains the address of the word following the final transfer for the record. After Bus Grant Late (BGL) and Non-Existent Memory (NXM) error conditions, the MTCMA contains the address of the location in which the failure occurred.

3.15 DATA BUFFER (MTD) 772 530. The data buffer is a register which is used for diagnostic purposes. After the completion of an operation, the 9-bits of the CRC or LRC are placed into the data register and made available to the program, depending upon the TU-10 Register bit 14.

3.16 TU-10 READ LINES (MTRD) 772 532. In addition to its use for diagnostic purposes, this register receives additional command bits from the CPU and provides additional status information from the controller and from the tape drive.

TU-10 READ LINES REGISTER BIT ASSIGNMENTS:



1. MTRD BIT 15 TIMER (10KHz) - This read-only bit provides the diagnostic program with the output of a 10 KHz timer. This timer bit, having a 50% duty cycle, is used by the diagnostic program for measuring the time duration of tape operations.

2. MTRD BIT 14 LRC/CRC SELECT (LRCS) - This write/read bit, when set, disables the CRC word from remaining in the data register at the conclusion of an operation, replacing it with the LRC character.

3. MTRD BIT 13 BAD TAPE GENERATE (BTG) - If set during an operation in progress this write-only diagnostic bit simulates a bad tape error by prematurely setting end-of-record status.

4. MTRD BIT 12 GAP SHUT-DOWN BIT (GSB) - This bit indicates the controller's post-record positioning time period (Main Sequence 2 or 3) to the diagnostic program.

5. MTRD BIT 11 CORRECTABLE PARITY ERROR (CPE) - This bit is true in the Read Mode when a phase encoded tape is being corrected because of a single channel dropout.

6. MTRD BIT 10 IBM PACK MODE - - When this Write/Read bit is set by the CPU, the IBM Pack mode is set, enabling the controller's internal byte swapping circuitry. IBM/industry-compatible tapes may then be read or written by the controller.

7. MTRD BIT 9 EDIT MODE/P.E. IDENTIFICATION (EDIT/IDEN) - When this bit is set by the CPU, the Edit Mode is enabled, issuing the Overwrite command to the tape drive. When read, this bit is true to indicate the Identification Burst of a phase encoded tape is being read by the controller.

8. MTRD BITS Ø-8 LONGITUDINAL REDUNDANCY CHARACTER (LRC Ø-7,P) - One or more of these bits will remain set to indicate incorrect longitudinal parity was read by the respective channel. (NRZI Mode)

3.17 PROGRAM FLOWCHARTS

3.18 The following pages contain flowcharts which illustrate the program flow required to handle controller operations, including Write, Write End of File, Read, Space Forward and Reverse, and Rewind operations. These illustrations generalize some of the specific details of controller programming, but do identify overall program requirements for each operation.

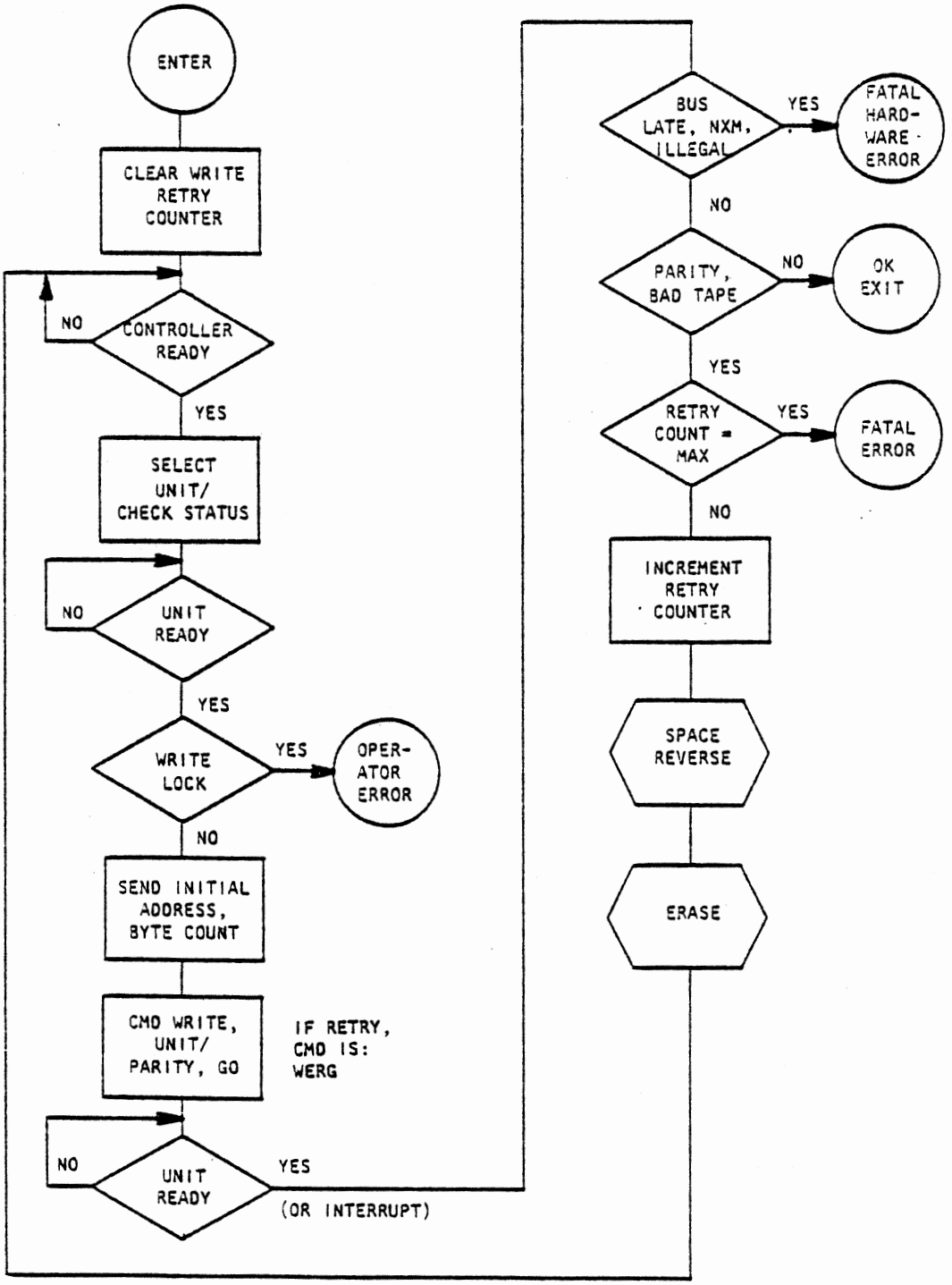


Figure 3-1. "WRITE" Flow Chart

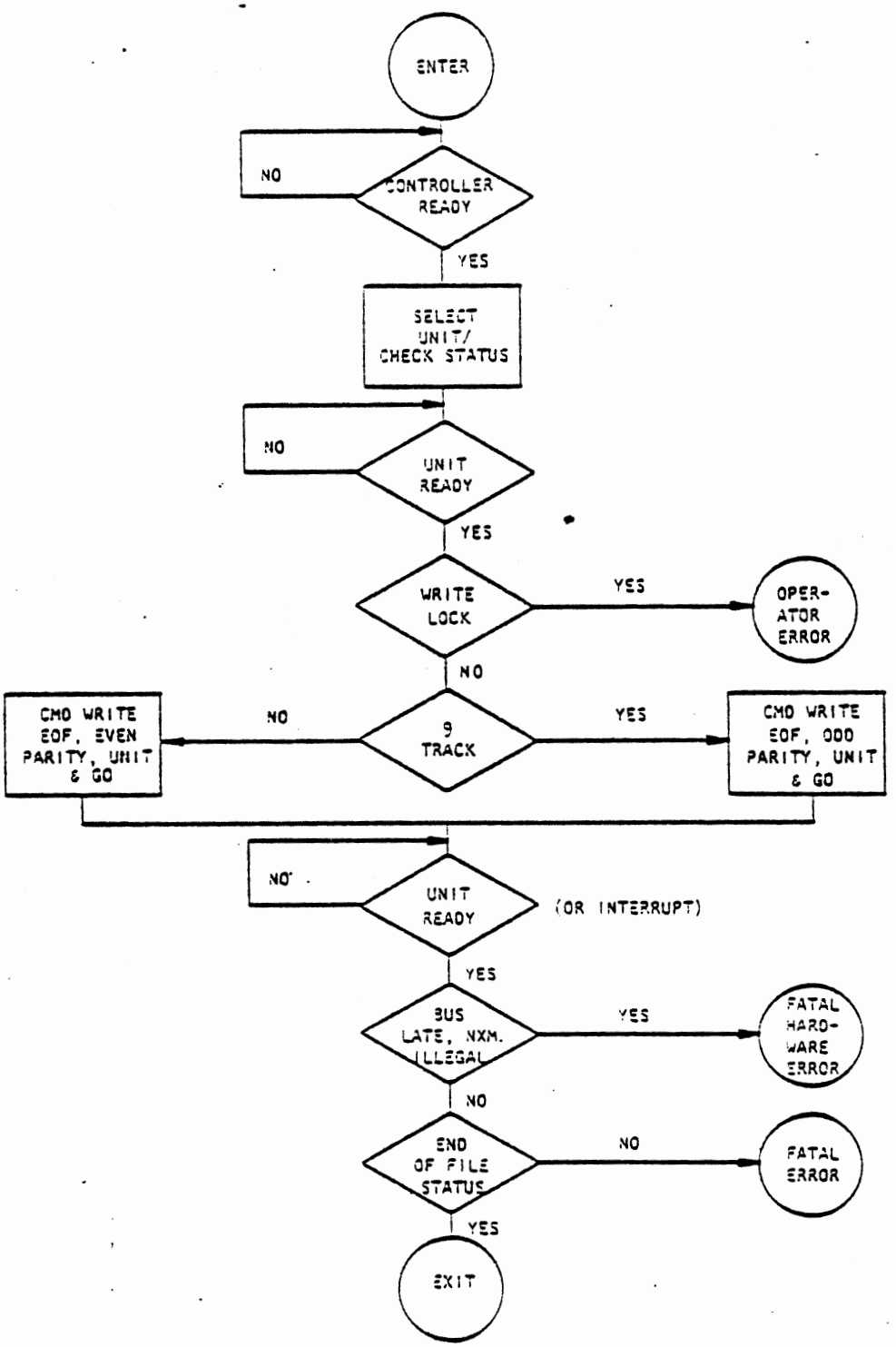


Figure 3-2. "WRITE END OF FILE" Flow Chart

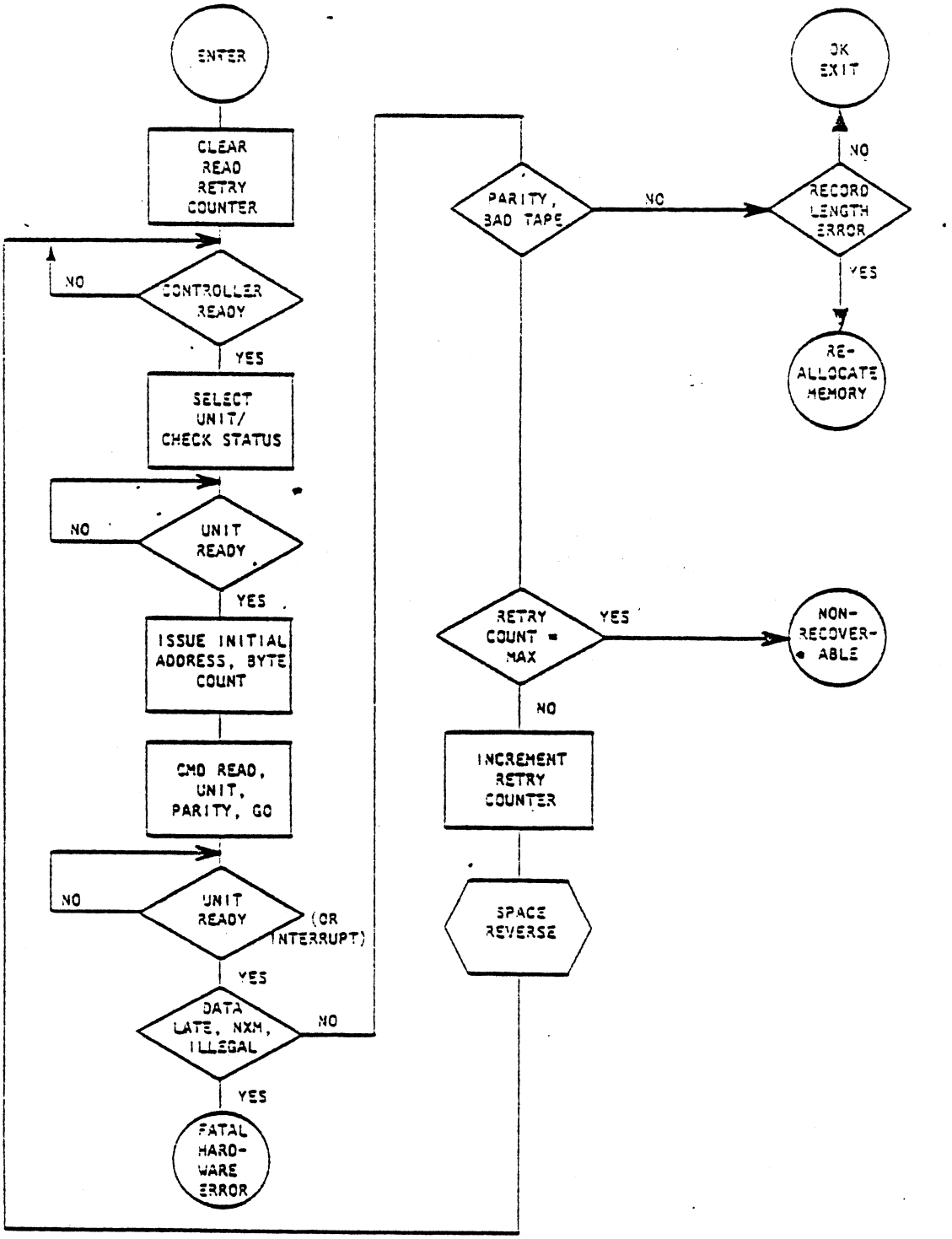


Figure 3-3. "READ" Flow Chart

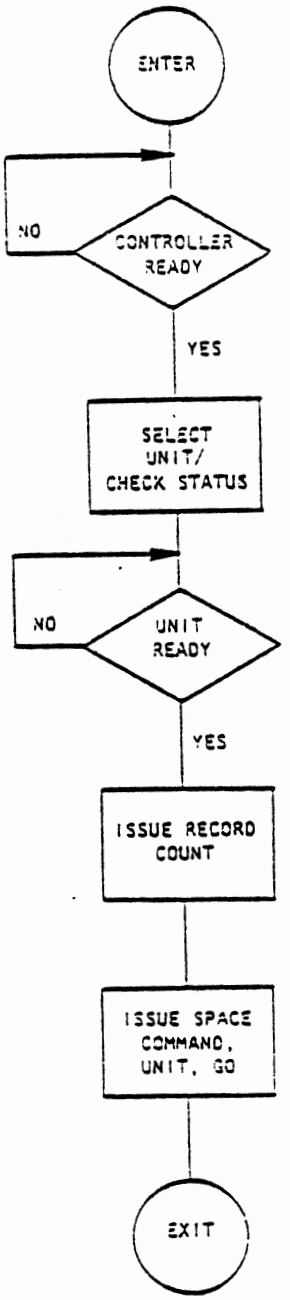


Figure 3-4. "SPACE FORWARD/REVERSE" Flow Chart

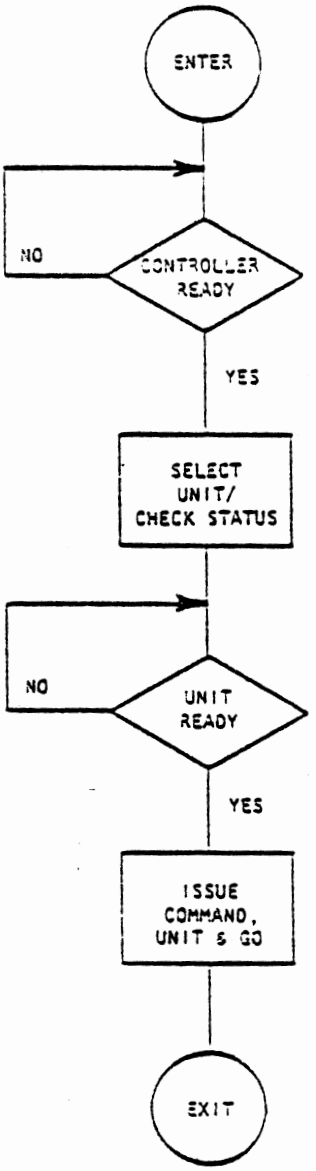


Figure 3-5. "REWIND" Flow Chart

SECTION IV

TAPE INTERFACE

TABLE OF CONTENTS

PARA-GRAPH		PAGE
4.1	TAPE FORMAT	4-1
4.3	Nine-Track NRZI Format	4-1
4.5	Nine-Track PE Format	4-3
4.9	Missing Characters	4-5
4.10	End-Of-File Mark	4-5
4.11	Tape-End Markers	4-6
4.13	Record Length	4-6
4.14	Effective Transfer Rate	4-6
4.15	TAPE DRIVE INTERFACE	4-7
4.16	Interface Signals	4-7
4.17	Interconnections	4-7
4.18	Drive Select Logic	4-8

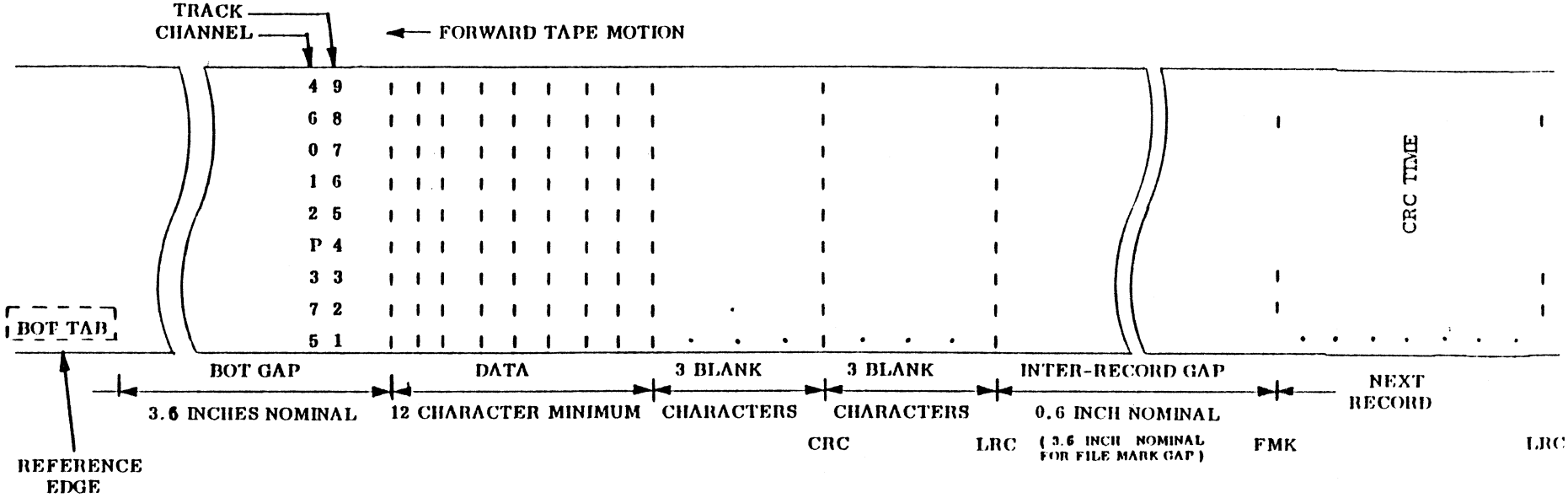
SECTION IV

TAPE INTERFACE

4.1 TAPE FORMAT

4.2 The Western Peripherals Tape Controller interfaces to industry-standard tape drives which write nine or seven bit characters laterally across the tape. The density of the characters written on the tape is determined by the type of tape drive, the density selection made on the tape drive, and (in some cases) the density selection made in the command issued by the CPU. A data block (record) written on tape consists of data characters and error checking characters (or a preamble and postamble). Every data character consists of the data byte plus a parity bit that is generated by the controller to conform with odd or even parity as specified by the program or the format. A record (or block) of data on tape represents the data transferred to or from a block of memory in one Read or Write operation. The controller separates adjacent records by automatically erasing a 0.6 inch (0.75 inch in 7-track) segment of tape to form an interrecord gap (IRG) between them. The controller always stops and starts the magnetic tape in an interrecord gap.

4.3 NINE-TRACK NRZI FORMAT. As shown in Figure 4-1, each data character contains eight data bits and one odd vertical parity bit. Following the last data character, the End of Record gap (three blank characters) is written, followed by a Cyclic Redundancy Check (CRC) character, followed by three more blank characters, concluded by a Longitudinal Redundancy Check (LRC) character. Following the LRC character, a 0.6 inch IRG is written, in which all nine tracks are erased. The LRC character produces an even longitudinal parity in each of the tracks along the length of the tape. Reading or writ-



NOTES

1. TAPE SHOWN WITH OXIDE SIDE UP.
2. CHANNELS 0 THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. EACH BIT OF THE LRC IS SUCH THAT THE TOTAL NUMBER OF "1" BITS IN THAT TRACK (INCLUDING THE CRC AND THE LRC) IS EVEN. IN THE 9-TRACK FORMAT THE LRC WILL NEVER BE AN ALL-ZEROS CHARACTER.
5. IT IS POSSIBLE FOR THIS CRC CHARACTER TO BE ALL ZEROS, IN WHICH CASE A READ DATA STROBE WILL NOT BE GENERATED.
6. A FILE MARK IS A SINGLE CHARACTER RECORD HAVING "1" BITS IN CHANNELS 3, 6, AND 7 FOR BOTH THE DATA CHARACTER AND THE LRC. THE CRC CONTAINS ALL ZEROS. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS RECORD AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
7. DATA PACKING DENSITY IS FIXED AT 800 BITS PER INCH.

Figure 4-1 9-Track NRZI Tape Format

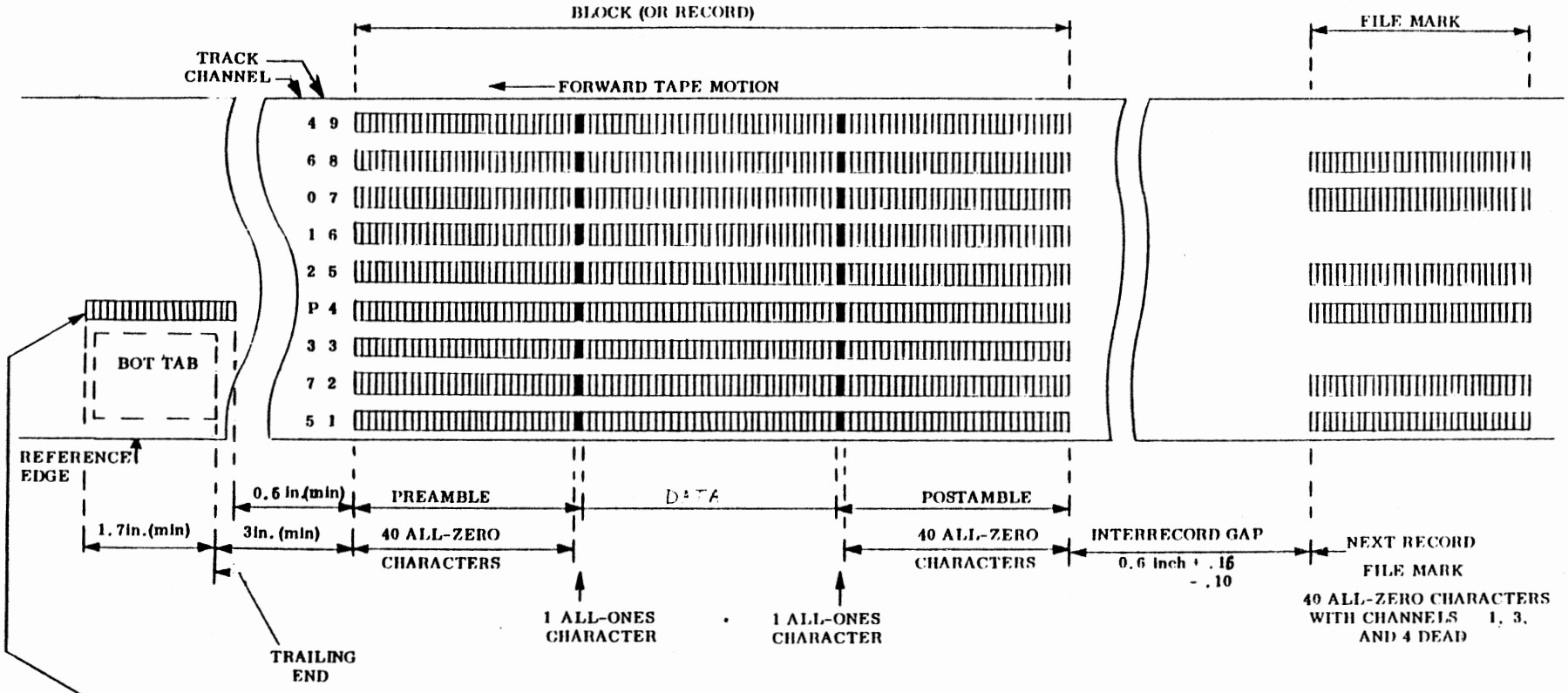
ing, the controller checks to ascertain that the lateral parity of every data character is odd and that every track has even longitudinal parity.

4.4 The 9-track file mark consists of a single character record with a one-bit in channels 3, 6, and 7; the remaining channels contain zeros. The CRC character is left blank, but an LRC character is written which is identical to the file mark character.

4.5 **NINE-TRACK PE FORMAT.** The standard Phase Encoded (PE) 1600 bits per inch format, shown in Figure 4-2, consists of a preamble, a variable length data block, and a postamble. The preamble consists of 40 characters containing zeros in all tracks followed by a character containing ones in all tracks. Each data character contains eight data bits and an odd vertical parity bit. The last data character is followed by the postamble (which is the reverse image of a preamble), an all-ones character followed by 40 all-zeros characters.

4.6 When the tape is at load point (beginning of tape) and the first data block is to be written, it is preceded by an identification burst, consisting of alternate ones and zeros in the parity (P) track, with all other tracks erased. The file mark consists of 40 characters of zero characters similar to those in the preamble, except that channels 1, 3, and 4 are erased.

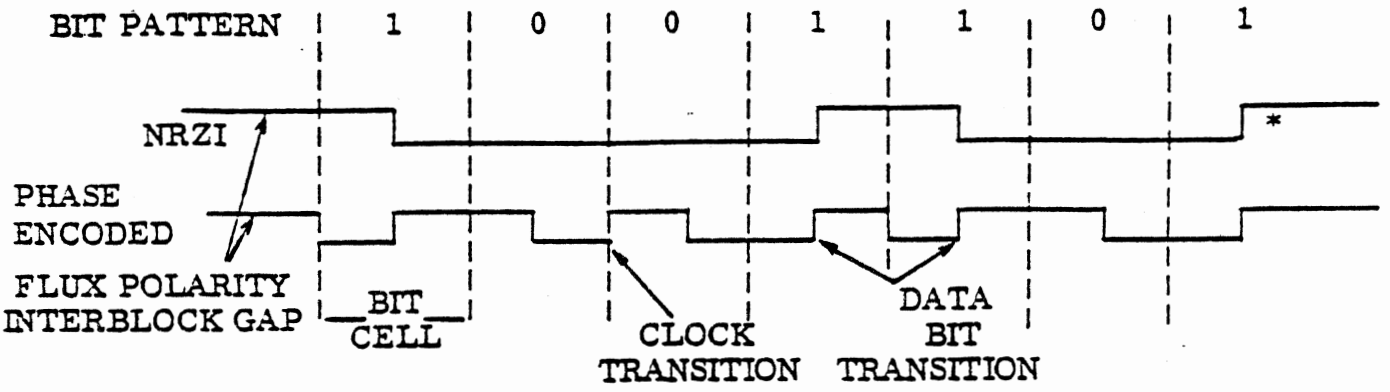
4.7 Phase encoded recording differs from NRZI recording in the recording method as well as the format. In Figure 4-3 NRZI and phase encoded waveforms of similar density are compared. The NRZI waveform shows a change in flux polarity for each binary one bit. A binary zero is represented by the absence of a flux change.



NOTES

1. TAPE SHOWN OXIDE SIDE UP.
2. CHANNELS ∅ THROUGH 7 CONTAIN DATA BITS IN DESCENDING ORDER OF SIGNIFICANCE.
3. CHANNEL P (PARITY) ALWAYS CONTAINS ODD DATA PARITY.
4. A FILE MARK IS A 40-CHARACTER PREMABLE BURST WITH CHANNELS 1, 3, AND 4 DEAD. THIS RECORD IS SEPARATED BY 3.5 INCHES FROM THE PREVIOUS AND BY A NORMAL IRG (0.6 INCH) FROM THE FOLLOWING RECORD.
5. DATA PACKING DENSITY IS FIXED AT 1600 BITS PER INCH.

Figure 4-2 9-Track PE Tape Format



NOTES:

NRZI--ANY CHANGE IN POLARITY IS A "1" BIT; NO CHANGE IS A "0" BIT.

* LAST CHARACTER IS LRC

PHASE ENCODED--DATA BIT TRANSITION IN DIRECTION OF IBG IS A "1" BIT.
--DATA BIT TRANSITION OPPOSITE IN DIRECTION OF IBG IS A "0" BIT.

Figure 4-3 PE and NRZI Recording Comparison

4.8 Phase encoded recording requires at least one flux change per bit cell. A binary one is represented by a flux change to the flux polarity of the interrecord gap. A binary zero leaves the flux polarized opposite to that of the interrecord gap.

4-9 **MISSING CHARACTERS.** The controller checks for missing characters when reading. Two or more contiguous missing characters will be interpreted as an EOR gap. If this condition occurs in the data portion of the record, Bad Tape Error (BTE) status will be reported.

4.10 **END-OF-FILE MARK.** The program can group sets of data records into files. The end of a file is indicated by an End of File (EOF) mark. The NRZI File Mark is a special record containing one special data character and its LRC. The PE File Mark consists of 40 characters in a combination of active and dead tracks. Each EOF in the NRZI format is preceded by a 3.5 inch IRG. Spacing operations automatically terminate upon detection of the File Mark.

4.11 **TAPE-END MARKERS.** The ends of all tapes contain reflective strips that are detected by photo cells in the transport. The Load Point marker is located at least ten feet in from the beginning of the tape and constitutes the logical Beginning of Tape (BOT). The Space Reverse and Rewind commands automatically stop at this marker. At least three inches of tape intervene between the BOT marker and the first record.

4.12 The end-of-tape (EOT) reflective strip is located at least 14 feet from the end of the tape. The program should not record more than a few feet beyond the EOT marker, leaving at least ten feet of the tape for a trailer. A status bit is set and Space Reverse operations are terminated when the tape passes beyond the EOT marker.

4.13 **RECORD LENGTH.** The minimum record length is two words or four data characters. Maximum length is limited (only by the capacity of the Byte Counter) to 65,536 bytes. When writing, the controller divides each computer word into two data bytes. In reading, the bytes are reassembled into a computer word.

4.14 **EFFECTIVE TRANSFER RATE.** During the actual processing of the data part of a record, the data transfer rate is fixed. However, in a long tape the effective, or average, transfer rate depends somewhat upon record length. Record length determines the percentage of tape taken up by the gaps. At the highest density (1600 bpi) each record gap occupies the space of 960 characters. Figure 4-4 shows the storage capacity of a reel of tape at various record lengths. The effective transfer rate is therefore determined by record length as well as tape speed and density.

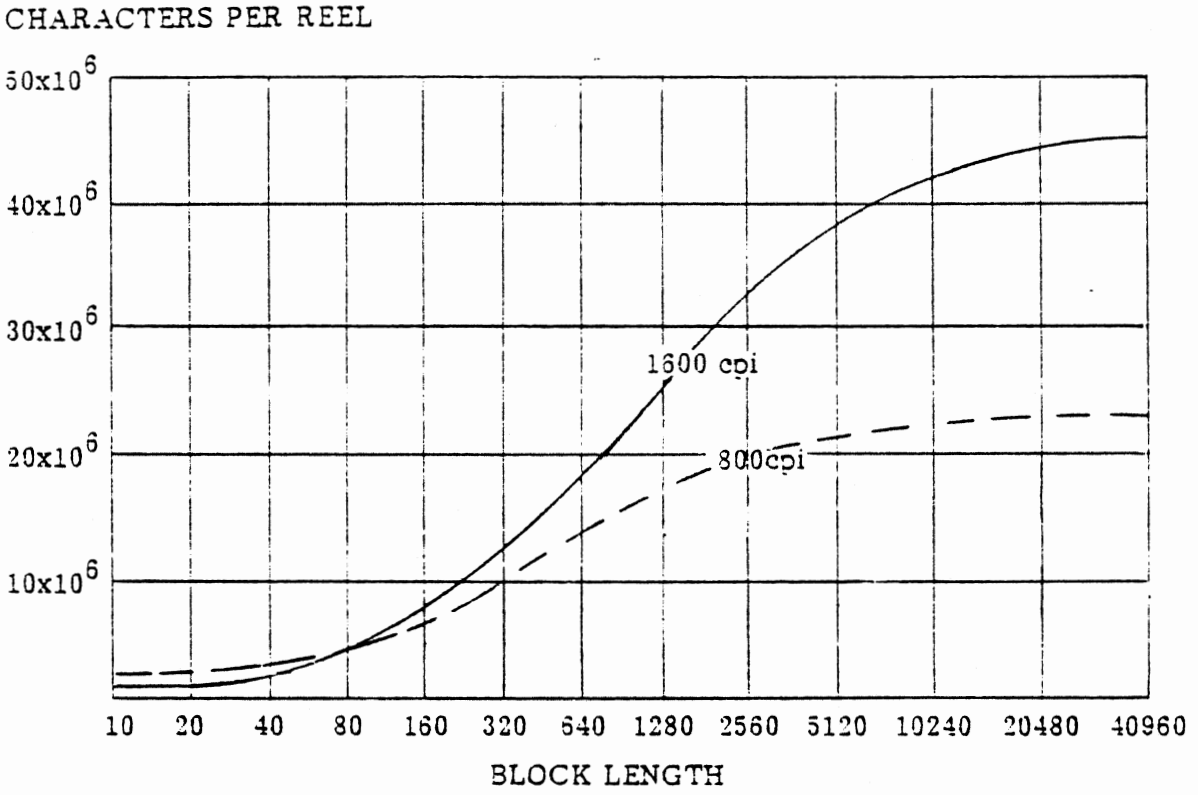


Figure 4-4 Comparison of Packing Density, Phase Encoded and NRZI Formats

4.15 TAPE DRIVE INTERFACE

4.16 INTERFACE SIGNALS. Figure 4-5 shows the signals on the interface between the controller and the tape drives. Table 4-1 lists and describes these signals. The selected tape drive returns status signals to the controller that indicate the type of tape drive, as shown in Table 4-2.

4.17 INTERCONNECTIONS. Three connectors, designated CONTROL, WRITE, and READ, are provided on the controller printed circuit board for making cable connections to the tape drives. Ribbon cable assemblies are provided for each of these three connectors. The other end of each ribbon cable assembly is connected to a connector adaptor assembly (paddleboard). For the WRITE and CONTROL lines, terminators are removed from the tape drives and a termin-

ator chip is installed on the paddleboards in the last tape drive in the daisy chain.

4.18 **DRIVE SELECT LOGIC.** Each tape drive is selected by the controller when its respective select line is activated. Eight select lines are used to control the eight possible tape drives. The active select line is determined by the drive select bits of the Command Register. While the first Control Paddleboard in the daisy chain receives all of the select lines, the propagation of the select lines to the next drive is controlled by the Drive Select Jumper plug.

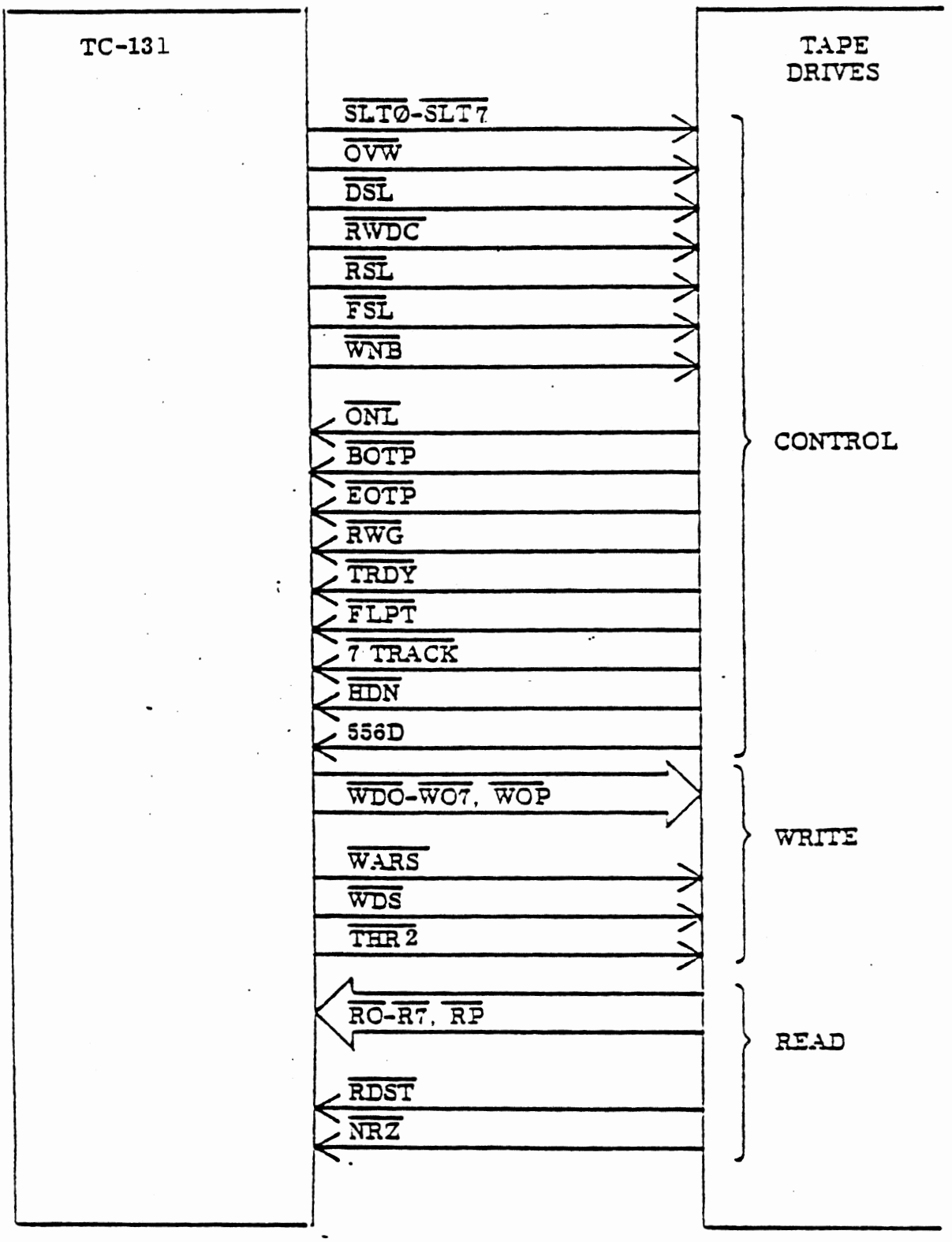


Figure 4-5 Tape Drive Interface

Table 4-1. Tape Drive Interface Signals

MNEMONIC	SOURCE	TERM	COMMENT
CONTROL CABLE:			
SLTØ-7	Controller	Select Drive Ø-7	Tape drive "n" is selected.
WNB	Controller	Write Enable	Enables write operations in selected tape drive.
FSL	Controller	Synchronous Forward Command	The selected tape drive initiates tape motion in the forward direction.
RSL	Controller	Synchronous Reverse Command	The selected tape drive initiates tape motion in the reverse direction.
RWDC	Controller	Rewind Command	The selected tape drive executes a high-speed rewind operation.
OVW	Controller	Overwrite	The edit mode is selected in the selected tape drive.
DSL	Controller	Density Select	When this line is active, high density is selected in the selected tape drive. When the line is inactive, low density is selected.
ONL	Drive	On Line	The selected tape drive is online.
BOTP	Drive	Beginning of Tape	The selected tape drive is at load point.
EOTP	Drive	End of Tape	Tape in the selected tape drive is at the end of tape marker.
RWG	Drive	Rewinding	The selected tape drive is rewinding.
TRDY	Drive	Ready	The selected tape drive is online and ready for operation.
FLPT	Drive	File Protect	The selected tape drive is write-protected so that write operation cannot be executed.

Table 4-1. Tape Drive Interface Signals (cont.)

MNEMONIC	SOURCE	TERM	COMMENT
7 TRACK	Drive	7-Track	The selected tape drive is a 7-track unit.
HDN and	Drive	Density/Tape	Density for 7-track units;
556D		Speed Select	tape speed for 9-track units.
WRITE CABLE:			
WDØ to WD7 and WDP	Controller	Write Data Lines	Tape write data bus.
WARS	Controller	Write Amplifier Reset	Resets tape write amplifiers. Generates LRC character.
WDS	Controller	Write Data Strobe	Strobes tape write data into tape drive.
THR2	Controller	Threshold No. 2 (Not used in this controller)	When this line is active, read threshold No. 2 is selected. When the line is inactive, threshold No. 1 is selected.
READ CABLE:			
RØ to R7 and RP	Drive	Read Data Lines	Tape read data bus.
RDST	Drive	Read Strobe	Strobes read data into the controller.
NRZ	Drive	NRZ	When this line is active from a 9-track drive, it indicates a 9-track NRZ unit; when the line is inactive from a 9-track drive, it indicates a 9-track PE unit.

NOTE: All tape drive interface lines are active low.

4.19 Three kinds of jumper plugs are used: One is for standard drives, one is for drives with drive selection thumbwheel switches, and one is installed in the fourth drive in installations using thumbwheel switches. A standard daisy-chained system is shown in Figure 4-7 where SLT Ø connects to drive Ø, SLT 1 connects to drive 1, etc. Each drive select jumper increments the drive select lines one position so that the next drive in position becomes the next numbered drive. Figure 4-8 illustrates a system using drives with select switches. Four of the select lines are made available to each drive, and the operator selects (with the thumbwheel switch) which select line will activate a particular drive. The operator must ensure that each drive is set to a different number. Caution: A separate installation step is required to connect all four select lines to each drive. Note: Some drive manufacturers mark the thumbwheel switch 1 through 4 for drive selections Ø through 3, respectively, with position Ø sometimes used as an off-line position.

	Status Signal			
Type of Tape Drive	7 TRACK	HDN	556D	NRZ
9-track, Tape Speed A	High	. . .	High	. . .
9-track, Tape Speed B	High	. . .	Low	. . .
9-track, PE (1600 bpi)	High	. . .	. . .	High
9-track, NRZ (800 bpi)	High	. . .	. . .	Low

Table 4-2 Status Signal Indicating Tape Drive Type

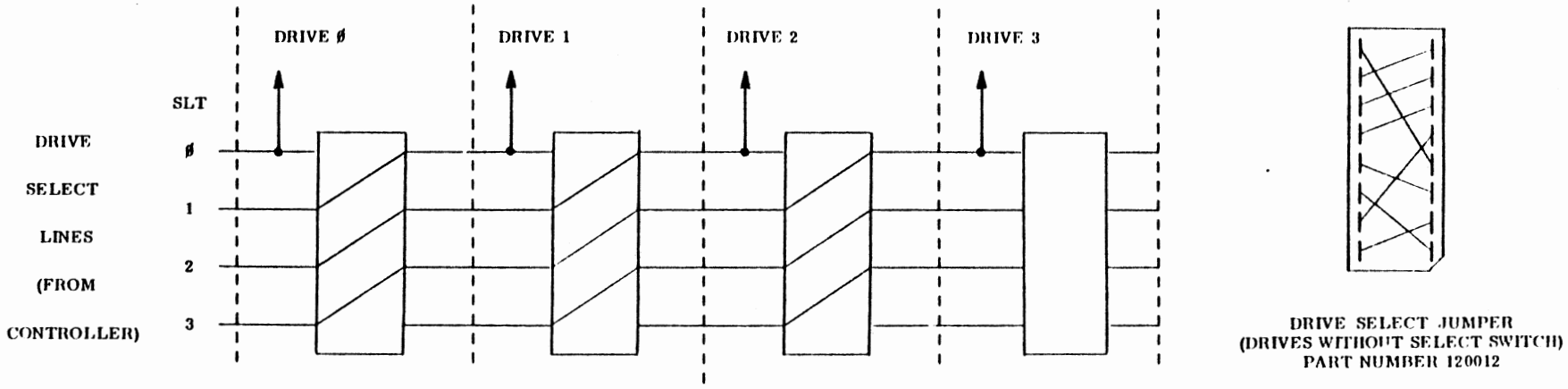


Figure 4-6 Standard Drive Select Logic

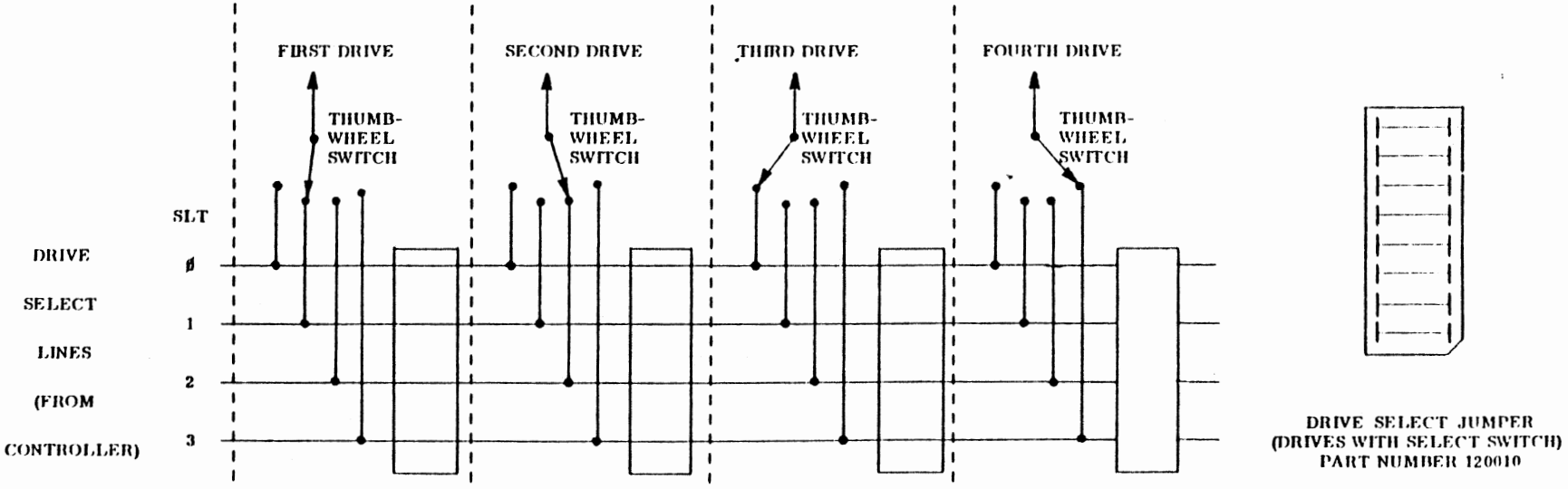


Figure 4-7 Drive Select Logic Using Select Switches

SECTION V

COMPUTER INTERFACE

TABLE OF CONTENTS

PARA-GRAPH		PAGE
5.1	COMPUTER INTERFACE	5-1
5.3	Bus Interface Signals	5-1
5.4	Bus Operations	5-5

SECTION V

COMPUTER INTERFACE

5.1 COMPUTER INTERFACE

5.2 The controller interfaces to the Q-Bus of the LSI-11 microprocesor-based computer system. The Q-Bus is an asyncronous 16-bit I/O bus which multiplexes address and data information over the same 16 bus lines. In addition to address and data information, the bus contains signal lines for DMA and interrrupt requests, data transfer handshaking, initialization of devices and other miscellaneous control signals.

5.3 **BUS INTERFACE SIGNALS.** The interface signals used by the controller to communicate with the LSI-11 are typically prefixed by "B" for bus and suffixed by "L" to indicate the signal is low-true. The bus signals are:

1. BS7 (Bank 7 Select) - The bus master asserts BS7 when an address in the 28 - 32K range (the upper 4K bank) is placed on the bus.
2. DALØ-15 (Data/Address Lines) - These lines are the 16-line multiplexed data/address bus over which address and data information are communicated. Address information is first placed on the bus by the bus master device. The same device then either receives input data from, or outputs data to the addressed slave device (memory) over the same bus lines.
3. DIN (Data Input) - This signal is used for two types of bus operations:
   a. When asserted during SYNC time, DIN implies an input transfer with respect to the current bus master, and requires a response (RPLY). DIN is asserted when the master device is ready to accept data from a slave device.
   b. When asserted without SYNC, it indicates that an interrupt operation is occurring.

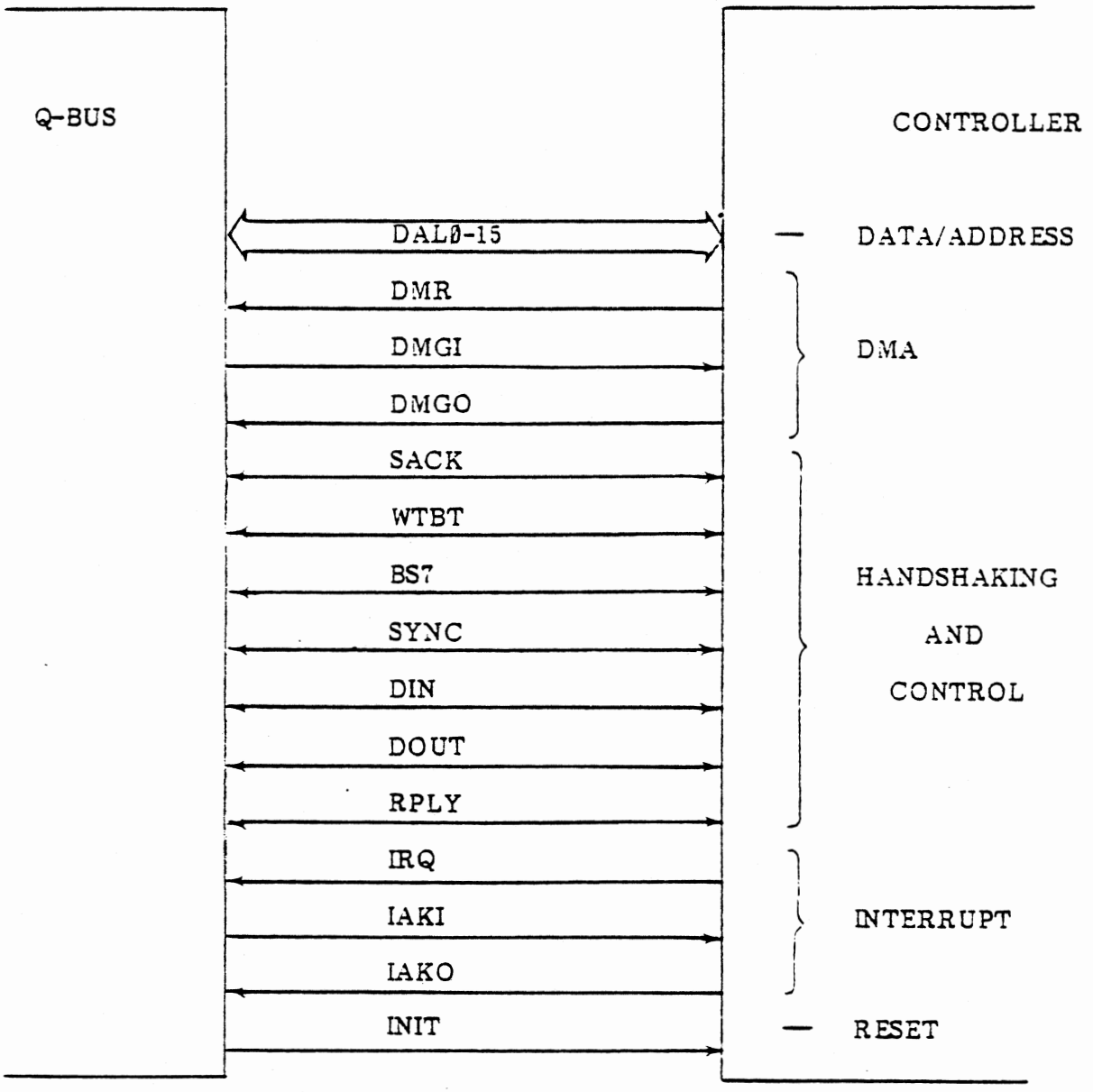


Figure 5-1 Computer Interface

4. DMGI & DMGO (DMA Grant Input and DMA Grant Output) - These are the processor-generated daisy-chained signals which grant bus mastership to the highest priority DMA device along the bus. The processor generates DMGO, which is routed to the DMGI pin of the first device on the bus. If it is requesting the bus, it will inhibit passing DMGO. If it is not requesting the bus, it will inhibit passing DMGO. If it is not requesting the bus, it will pass the DMGI signal to the next (lower priority) device via its DMGO pin. The device asserting DMR is the device requesting the bus, and it responds to the DMGI signal by negating DMR, asserting SACK, assuming bus mastership, and executing the required bus cycle. DMA device transfers are single transfers which do not interfere with memory refresh.

5. DMR (Direct Memory Access Request) - A device asserts this signal to request bus mastership. The processor arbitrates bus mastership between itself and all DMA devices on the bus. If the processor is not bus master it grants bus mastership to the requesting device by asserting DMGO The device responds by negating DMR and asserting SACK.

6. DOUT (Data Output) - DOUT, when asserted, implies that valid data is available on the data lines and that an output transfer, with respect to the bus master device, is taking place. The slave device responding to the DOUT signal must assert RPLY to complete the transfer.

7. IAKI & IAKO (Interrupt Acknowledge Input and Interrupt Acknowledge Output) - These are the daisy-chained interrupt acknowledge signals which are generated by the processor in response to an interrupt request. The processor asserts IAKO, which is routed to the IAKI pin of the first device on the bus. If it is requesting an interrupt, it will inhibit passing IAKO. If it is not asserting IRQ, the device will pass IAKI to the next (lower priority) device.

8. INIT (Initialize) - This signal is asserted by the processor to initialize or clear all devices connected to the bus. The signal is generated in response to a power-up condition.

9. IRQ (Interrupt Request) - A device asserts this signal when its Interrupt Enable and Interrupt Request flip-flops are set. If the processor's PS word bit 7 is 0, the processor acknowledges the request by asserting DIN and IAKO.

10. RPLY (Reply) - This signal is asserted in response to DIN or DOUT and during interrupt acknowledge transactions. It is generated by a slave device to indicate that it has placed its data on the bus or that it has accepted data from the bus.

11. SACK (Selection Acknowledge) - This signal is asserted by a DMA device in response to the processor's DMGO signal, indicating that the DMA device is bus master.

12. SYNC (Synchronize) - The bus master device asserts this signal to indicate that it has placed an address on the bus. The transfer is in process until SYNC is negated.

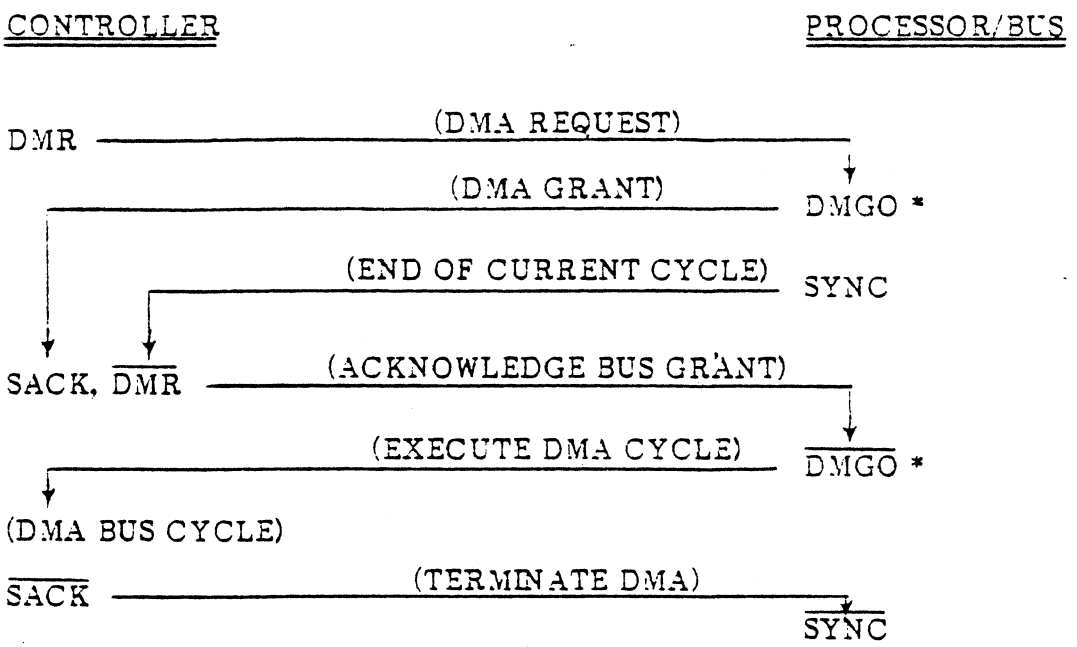
13. WTBT (Write/Byte) - This signal is ued in two ways to control a bus cycle:

    a. It is asserted during SYNC to indicate that an output sequence is to follow.

    b. It is asserted during DOUT in a DATOB bus cycle for byte addressing.

5.4 **BUS OPERATIONS.** The controller receives commands from and provides status information to the processor with the controller being a slave device. After the controller receives the proper commands to transfer data, the controller becomes a bus master device, handling the data transfers directly with the memory, requiring no processor intervention. When the controller has completed all data transfers, it alerts the processor by issuing an interrupt request. Devices on the bus are initialized when power is applied or whenever a reset instruction is executed.

5.5 The controller requests a single transfer on the bus by asserting DMR. After completing the current bus cycle, the processor responds by asserting DMGO, which allows the controller to become the bus master. It also inhibits further processor initiation of a new bus cycle. The controller then asserts SACK and removes DMR, causing the processor to terminate DMGO. The controller is now bus master and it will execute the required data transfer; an input transfer when writing to tape or an output transfer when reading from tape. When the data transfer is completed, the controller returns the bus to the processor by terminating the SACK signal. The processor then returns to its programmed operations.



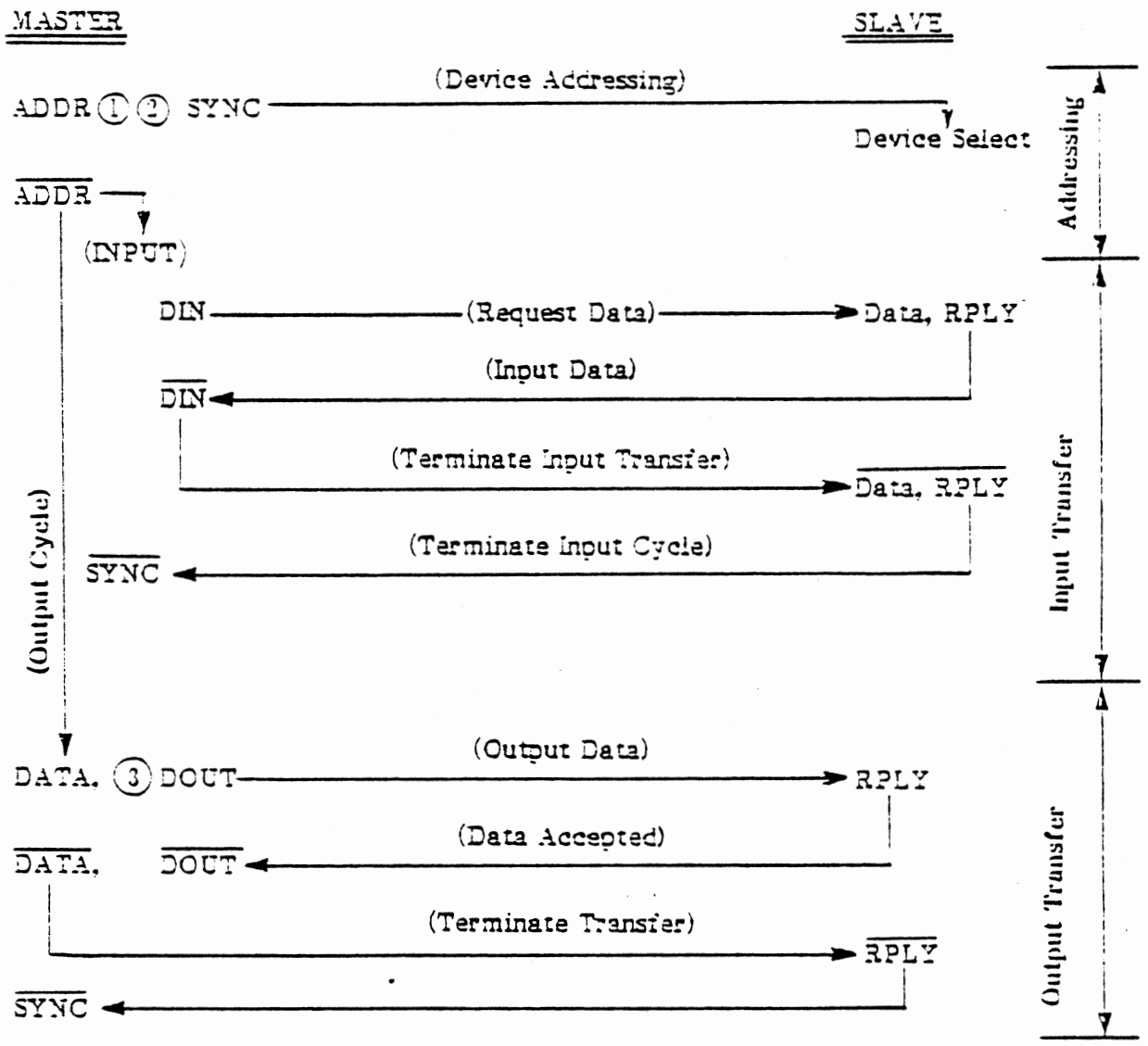
* NOTE: Daisy-chained signal

Figure 5-2 DMA Request/Grant Sequence

5.6 Input operations are used by the processor to receive status information from the controller and are used by the controller when receiving data from memory to be written onto tape. Output operations are used by the processor when providing the controller with command information and are used by the controller when transferring information read from tape to the desired section of memory. Input/output operations (equivalent to read-modify-write operations) are not used by the controller for DMA transfers. To begin a transfer, SYNC and the address are placed on the data lines together with BS7 (if the address is in the 28-32K range) and WTBT (if the transfer is an output transfer). After the device is selected and the address taken off of the bus lines, DIN is asserted for an input transfer, addressing the slave

device to respond with data and RPLY. The master device then receives the data, terminating DIN, which causes the slave device to remove RPLY and the data from the bus lines. The SYNC signal is then removed by the master device, terminating the input transfer. For an output transfer, the DOUT signal replaces the DIN signal and is asserted by the bus master together with the output data on the WTBT signal (if it is a byte transfer). The slave device accepts the data and acknowledges by asserting the RPLY signal, which causes the master device to remove the data and terminate the DOUT signal. This action by the master device causes the slave to remove the RPLY signal which in turn causes the master to remove the SYNC signal, terminating the output transfers.

5.7 Interrupts are used in the system so that the processor is not burdened with the responsibility of determining when the controller has completed an operation. Interrupt processing allows the processor to continue with its program until alerted by the controller. When enabled in the controller, the interrupt request is issued to the processor upon completion of an operation. If the processor currently is accepting interrupts, program execution is suspended (saved) and the DIN is asserted, together with the daisy-chained IAKO signal. The interrupt acknowledge is passed along by each controller until captured by the interrupting device. The interrupting controller will then remove the interrupt request, assert RPLY, and place its hard-wired vector number onto the data lines. The vector points to memory locations with a new processor status word and the address of the interrupt handling routine. The processor receives the vector and terminates the IAKO and DIN signals, causing the controller to terminate the RPLY signal and remove the



NOTES:

① Assert BST with address, if address = 28-32K Range

② Assert WTBT with address if output transfer

③ Assert WTBT with data, if byte transfer

Figure 5-3 DMA Bus Transfer Sequence

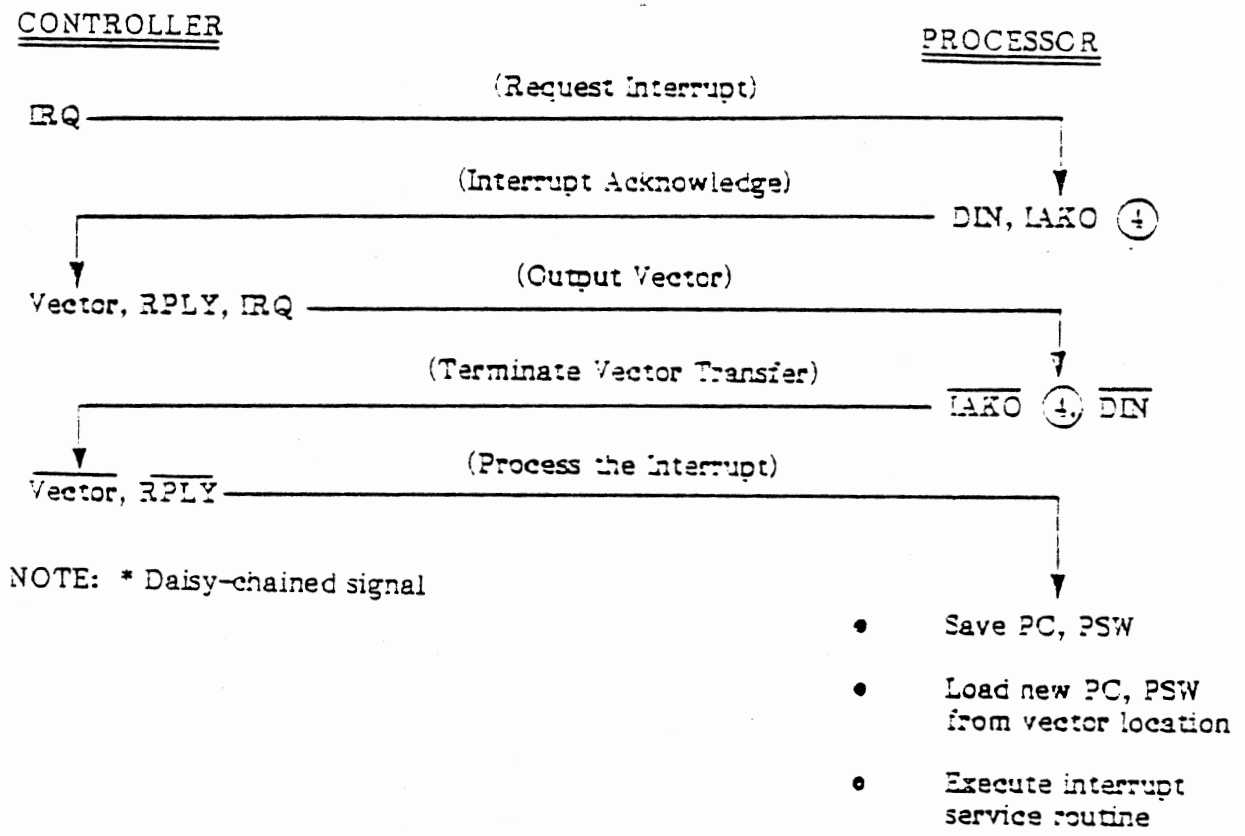


Figure 5-4 Interrupt Sequence

vector from the bus. The processor will then enter the controller's interrupt service routine.

SECTION VI

THEORY OF OPERATION

TABLE OF CONTENTS

PARA-GRAPH		PAGE
6.1	FUNCTIONAL CONTROLLER ORGANIZATION	6-1
6.3	TAPE DRIVE INTERFACE	6-1
6.7	PHASE ENCODED DATA RECOVERY	6-4
6.9	PE Activity Control	6-5
6.10	PE Data Channel	6-5
6.11	Phase Lock Loop	6-8
6.12	PE Status	6-10
6.13	MICROPROCESSOR	6-10
6.15	Data Processor	6-11
6.17	MICROPROGRAM ADDRESS PROCESSOR	6-13
6.23	Q-Bus Interface	6-16
6.24	Address/Data Transceivers	6-18
6.25	Direct Memory Access Requests (DMAR)	6-19
6.26	Bus Interrupt Request	6-19

SECTION VI

THEORY OF OPERATION

6.1 FUNCTIONAL CONTROLLER ORGANIZATION

6.2 The controller hardware can be logically divided into four sections; tape interface, phase encoded data recovery, microprocessor, and computer interface. Each area will be discussed separately. A block diagram of the controller is shown in Figure 6-1.

6.3 TAPE DRIVE INTERFACE

6.4 The Tape Drive Interface consists of all logic directly associated with controlling the tape units excluding the PE Data recovery logic. Refer to Figure 6-2 for a block diagram of this section. All tape motion is controlled by the microprogram loading the tape unit command register. Another microprogram loadable register drives a decoder to generate the eight unit select lines. The write data register is a 9 Bit microprogram loadable register. The first 8 Bits correspond to the data byte and the ninth bit is the vertical parity bit. The parity bit is loaded when the write data register is loaded and is generated by a parity generater monitoring the nine LSB's of the DBUS. The microprogram has the control to load the parity register directly from the DBUS for writing characters which do not require parity (e.g. CRCC, EOF, PE preamble, etc.).

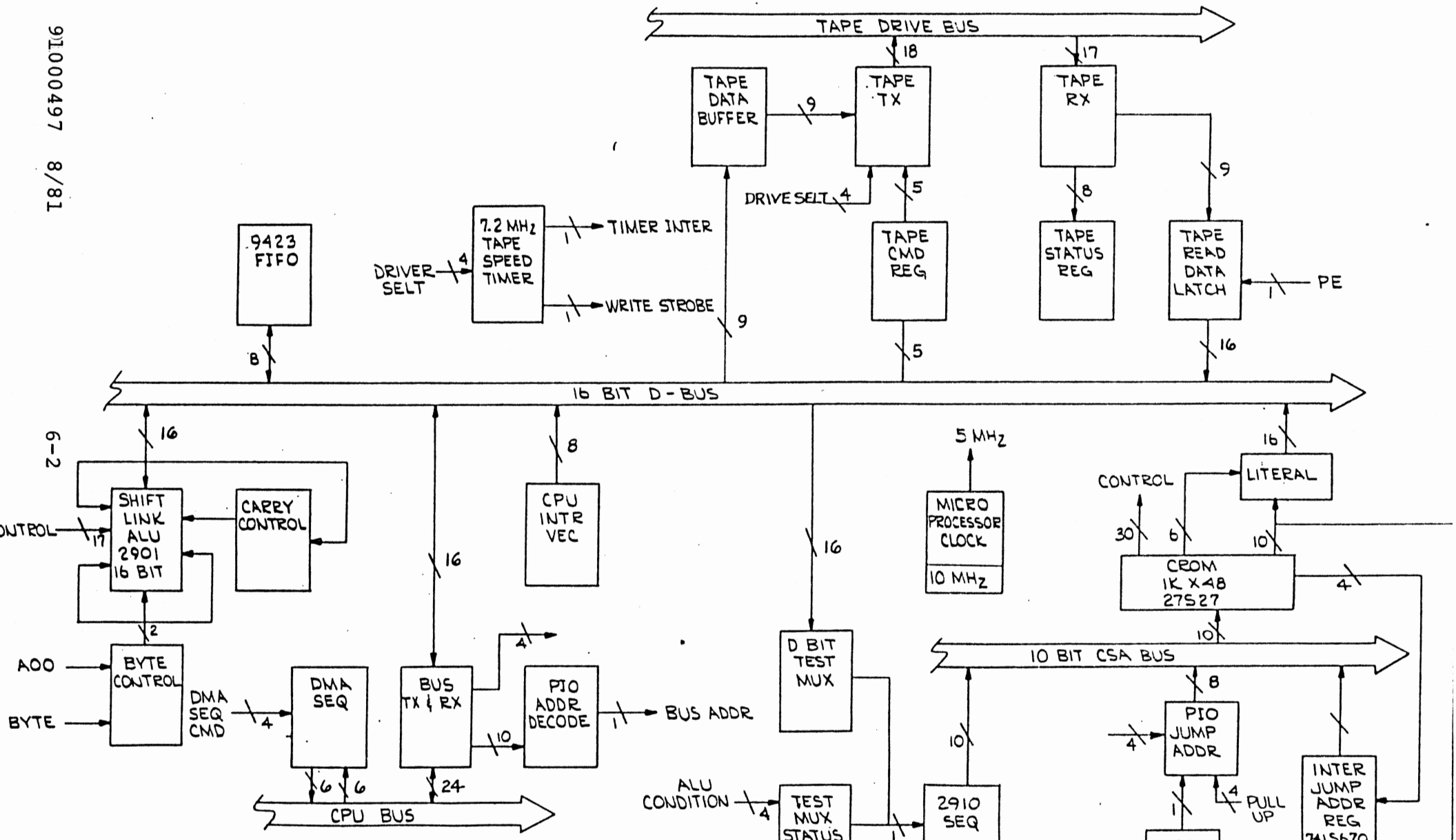


FIGURE 6-1 CONTROLLER BLOCK DIAGRAM

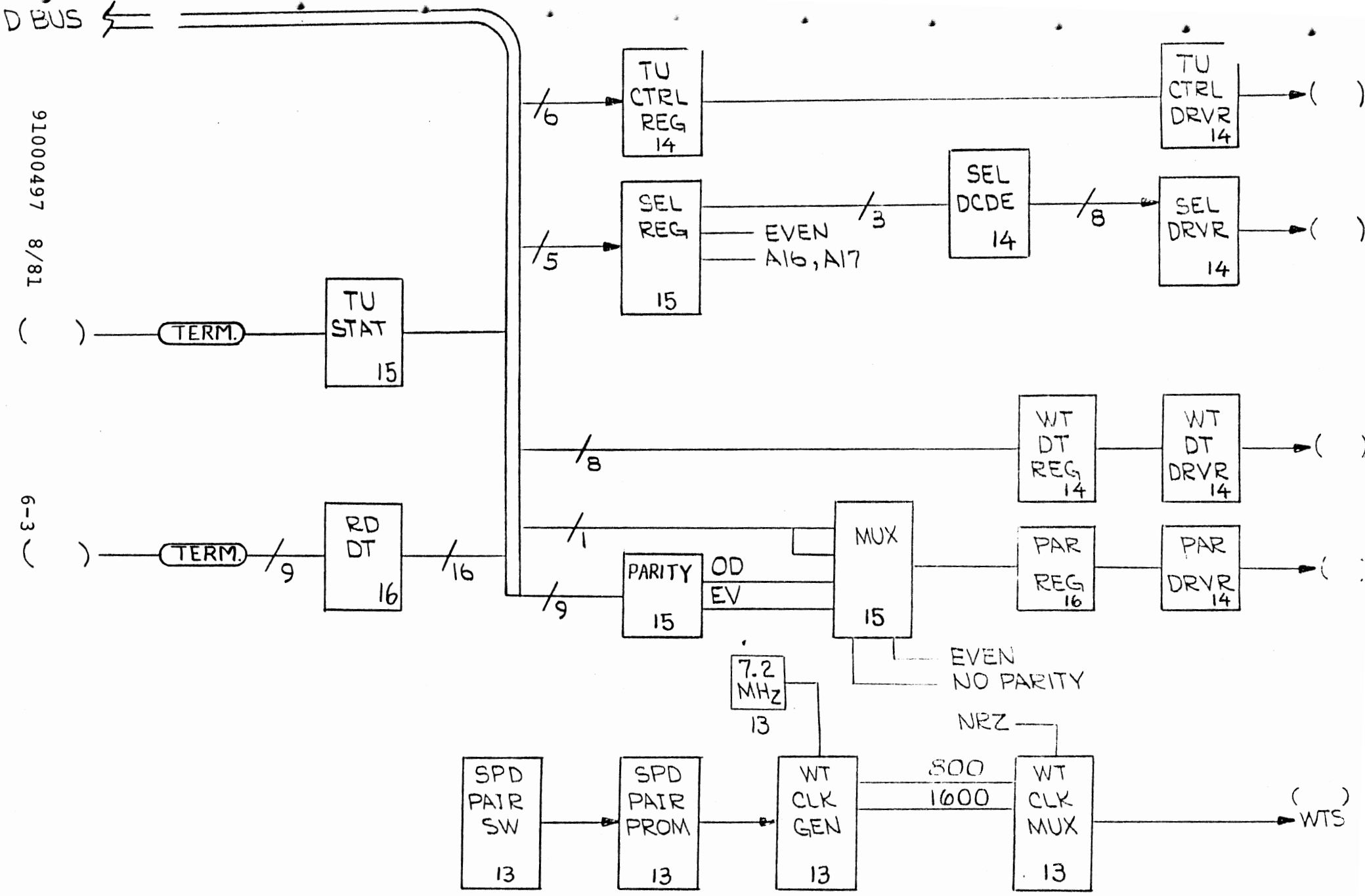


FIGURE 6-2 TAPE UNIT CONTROL

6.5 On the input side, the microprogram has access to the tape unit status and the read data. The read data register in NRZ is 9 Bits of data and parity with the remaining bits always a 0. In PE, the parity bit is extended throughout the upper byte to facilitatew an all ones character recognition. The same parity generater is used to check the read data parity as it is moved across the DBUS.

6.6 Write Data Strobes are generated in the hardware and enabled by the microprogram. The write data frequency is derived from a 7.2 MHZ oscillator driving a counter divider chain preset by the speed pair select PROM. The counter chain produces an 800 and 1600 BPI clock at the selected speed. Two interrupts are generated: the timer, and (when WGATE is set) the write strobe. The write data strobe interrupt signals a request for new data in the write data register. The timer is always the 800 CPI clock and is used for up/down ramp timing, tape gap and IRG timing.

6.7 PHASE ENCODED DATA RECOVERY

6.8 The PE data recovery logic is the largest, most hardware intensive section in the controller. The large amount of hardware is required because each read channel operates independently, requiring individual data recovery logic for each of nine channels. For proper tracking of

the read data and to eliminate changing components for the five speeds supported, four sphase lock loops are used. No component changes or adjustments are required to change speeds; all selection information is received from the speed pair PROM. The remaining logic is involved in initiating a PE read operation or in generating status. Refer to Figure 6-3 for a block diagram of the PE data recovery logic.

6.9 PE ACTIVITY CONTROL. A PE read operation is started by the microprogram setting the RDGATE latch. The PE control logic then monitors channel 2 and the parity channel for activity. After several transitions in either or both channels has been detected, the read channel decoders are enabled by LOCKENA. The control logic continues monotoring the data and, after some additional time, LOCKED is generated indicating that all channels should have acquired data by this time. If a channel has not locked on, it should dropout immediately, assuminga dead channel status. The control logic also generates a signal (no data) indicating the IRG has been encountered when no more data is detected in the two channels being monitored.

6.10 PE DATA CHANNEL. Refer to Figure 6-4 for a block diagram of a typical channel. When a read channel is enabled it assumes the incoming data is the all zeroes

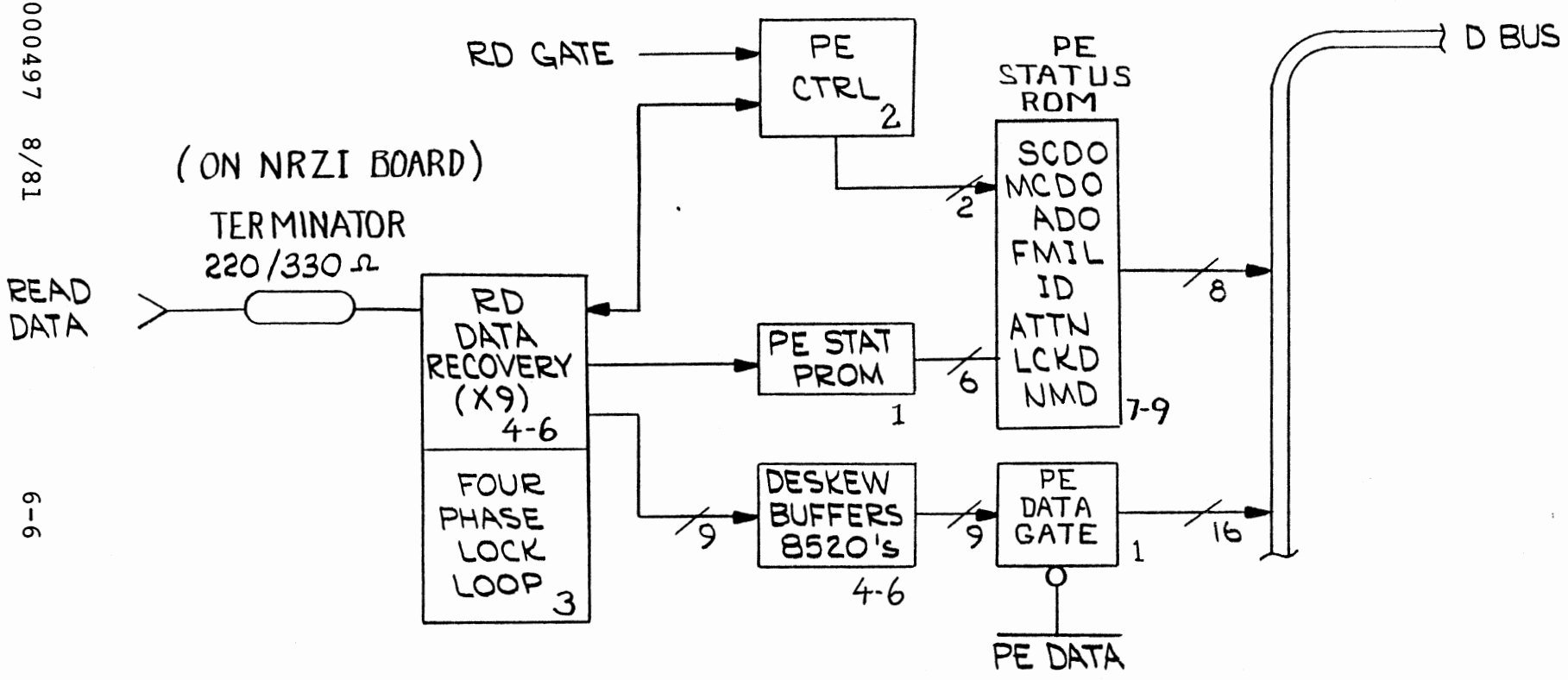


FIGURE 6-3 PHASE ENCODED DATA RECOVERY SECTION

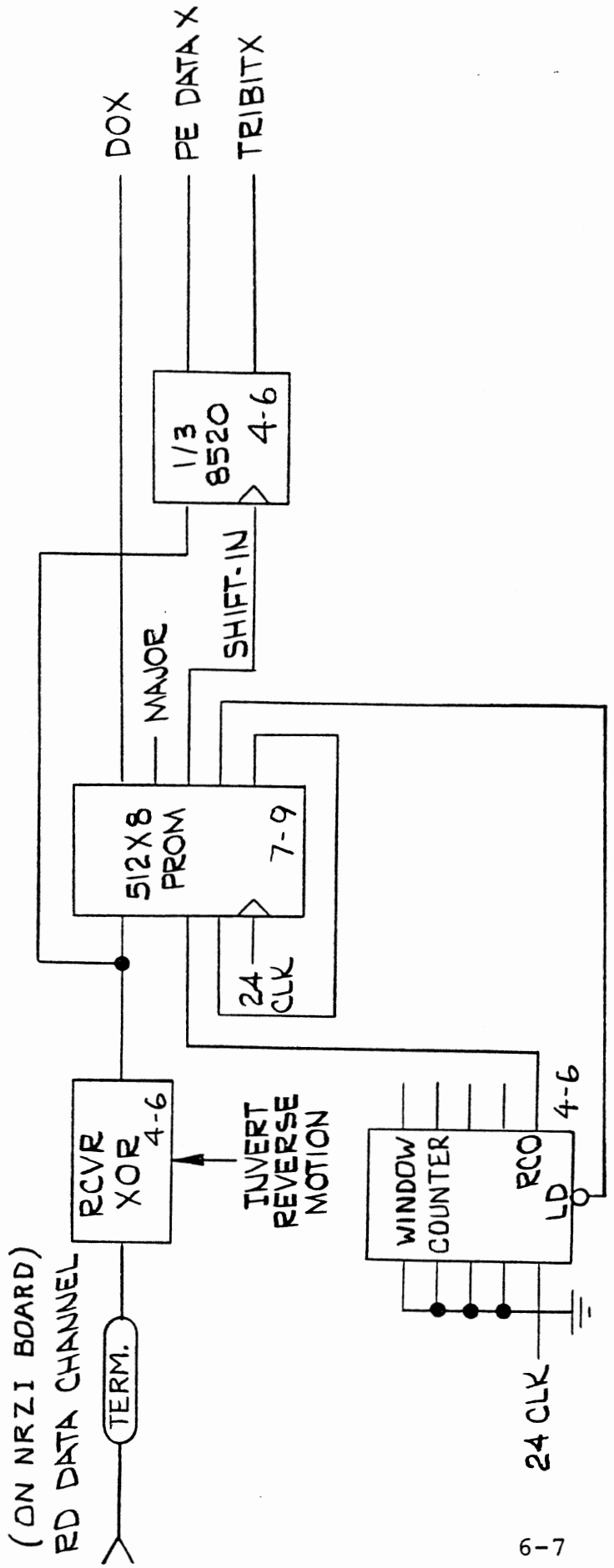


FIGURE 6-4 PE DATA CHANNEL

preamble and a high to low transition on the read data lines is the major transition of a zero bit. If a zero transition is not detected by the time the LOCKED signal is received the channel will dropout and start a continuous stream of Shift In signals to the deskew buffer to allow it to function properly. Once a zero is found, the channel logic advances to state one and begins looking for a one's transition to mark the beginning of the data portion of the record. Once detected the logic advances to state two and generates a Shift In to the deskew buffer for each major transition. The channel logic has stripped off the preamble and the sync byte in states 0 and 1 once state 2 is reached no futher data processing takes place. The channel will continue until a dropout occurs and then will force feed the deskew buffer until disabled.

6.11 PHASE LOCK LOOP. The phase lock loop is used to track the incoming read data to eliminate waveform distortion introduced by long or short term speed variations in tape motion. Four independant PLL's are used to support the five speeds, with one of the slower speeds handled by inserting an additional divide by two stage. The output of the PLL is a clock 24 times the data rate. Refer to Figure 6-5 for a block diagram of the PLL section. The PLL consists of a phase detector, an amplifier/low pass filter, a VCO, and a divide by 24 block.

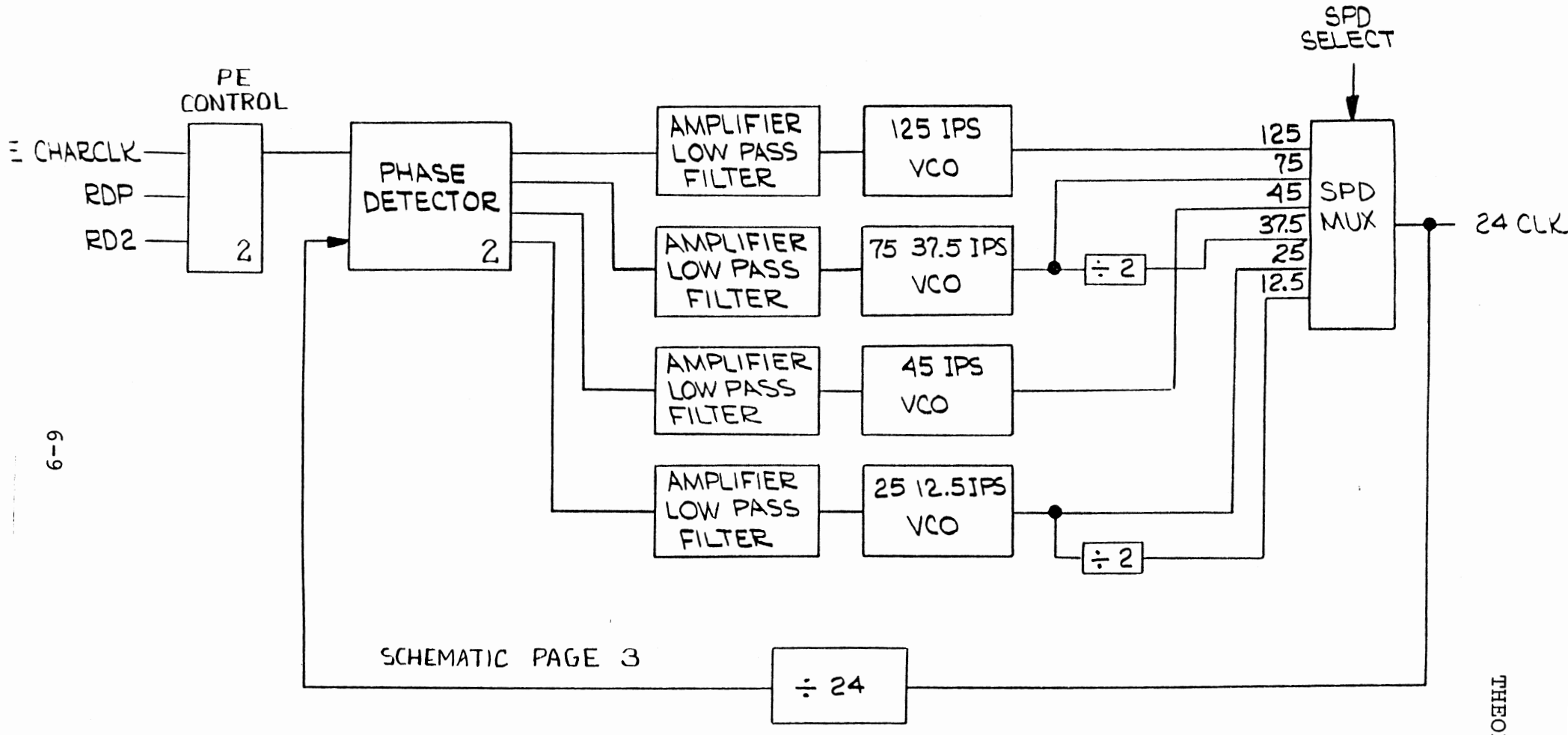


FIGURE 6-5 PE PHASE LOCK LOOP

The phase detector and the divider are common to all loops since thses elements are essentially frequency independent. The VCO and amplifier/low pass filter are unique because of the different VCO center frequencies and low pass filter components to establish the desired dynamic characteristics of the loop. The output of each VCO enters a multiplexer which is controlled by the speed pair PROM, thus only the loop of the selected speed is closed. The PLL tracks the PE character rate clock from the write strobe clock generater until the LOCKED signal is generated and the read data replaces the character clock.The PLL tracks the parity channel unless it drops out, then the PLL will track channel two.

6.12 PE STATUS. The PE status is generated from the drop out condition of all channels. A 512 by 8 prom monitors all nine channels and from the pattern of the drop outs can determine: Single Channel Drop Out, Multiple Channel Drop Out, All Channels Dropped Out, File Mark, and ID Burst.

6.13 MICROPROCESSOR

6.14 The heart of the controller is a high performance 16 bit 2901 bit slice microprocessor coupled with the 2910 micro-program address sequencer. The micro-processor can be micro-processor can be considered two closely coupled processors; a data processor, the 2901, and an address

processor, the 2910. The micro-processor uses a conventional single-level pipeline architecture with a cycle time of 200 nsec, yielding an execution rate of five million instructions per second. The micro-program resides in a 1024 by 48 control store consisting of twelve high speed 512 by 8 registered PROMS.

6.15 Data Processor. The data processor consists of the four 2901's and the control logic for external data sources and destinations. Refer to Figure 6-6 for a block diagram of the data processor.

6.16 The central component of the data processor is the data bus (DBUS) which is 16 bits wide and is used for all data movement within the controller. The microinstruction has two fields of four bits each for controlling the sources and destinations of data on the DBUS. Two additional bits are used, one for enabling the 2901 and the other for placing a 16 bit literal on the DBUS. The external source field and the 2901 A port address overlap in the microinstruction. The external source field is only three bites allowing any source to overlap with two 2901 registers. The external destination field and the 2901 B port address overlap in the microinstruction. Another bit from the microinstruction is used to enable external destination. The external destination field is only three

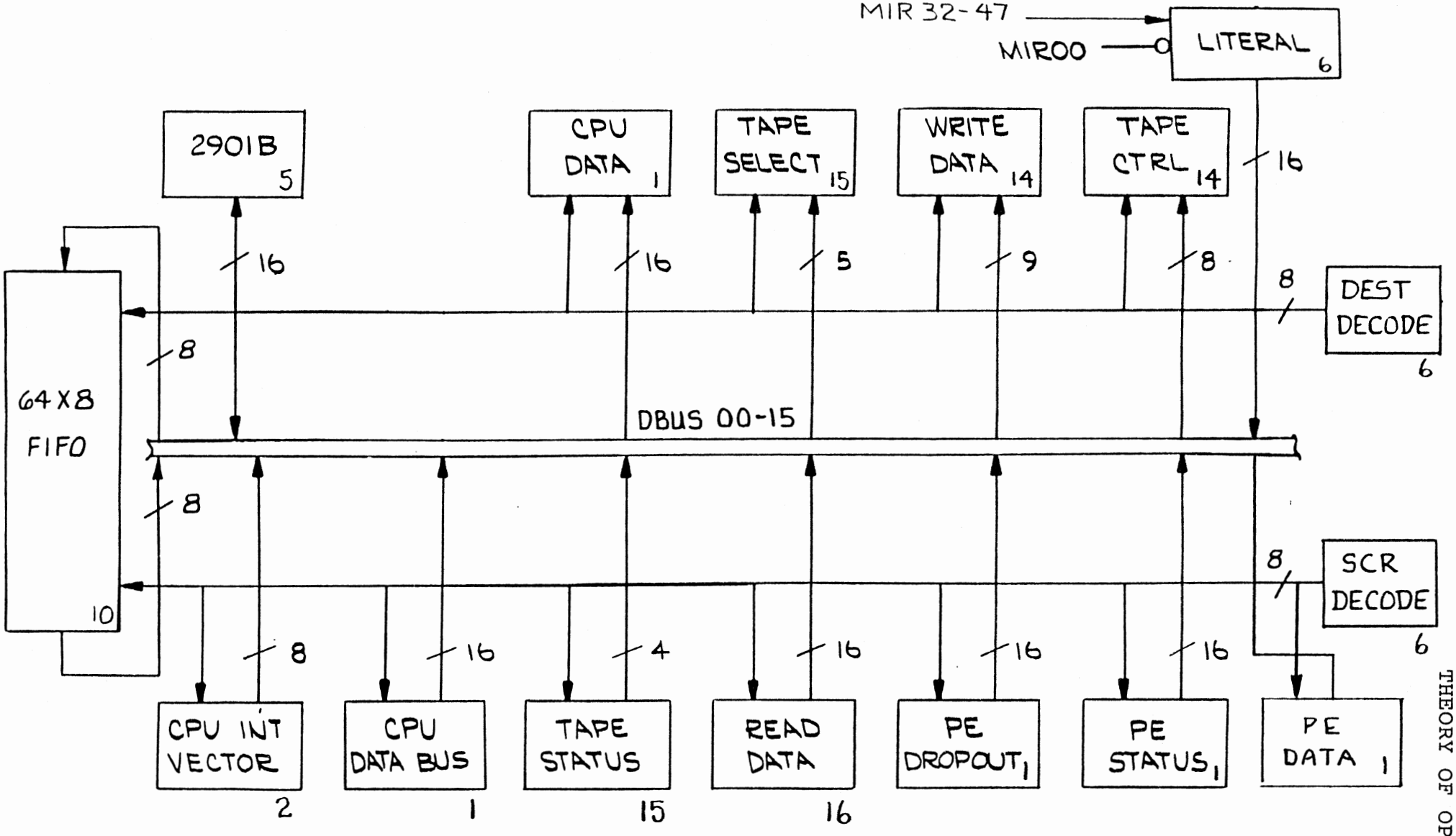


FIGURE 6-6 DATA PROCESSOR

bits allowing any destination to overlap with two 2901 registers.

6.17 MICROPROGRAM ADDRESS PROCESSOR

6.18 The microprogram address processor consist of the 2910 and the associated logic directly used in arriving at the effective address for the current microinstruction. Refer to an AMD specification for the 2910 to understand all the address control available. The microprogram address has three direct sources, the 2910, the PIO vector, and the microinterrupt vector file. Refer to Figure 6-7 for a block diagram of this section.

6.19 The 2910 is the usual source for the microprogram address. Within the 2910 there are four sources of the address; the direct inputs from the microinstruction the program counter, the stack, and the register/counter. Since the four bits of 2910 instruction come directly from the microinstruction all of the 2910 commands are available. The 2910 instruction field overlaps the data processor's literal filed, therefore when a literal is used only a continue or return instruction is available. Seven bits in the microinstruction are used for controlling cpnditional 2910 instruction execution. MIR27 controls whether or not the 2910 instruction will be conditional and

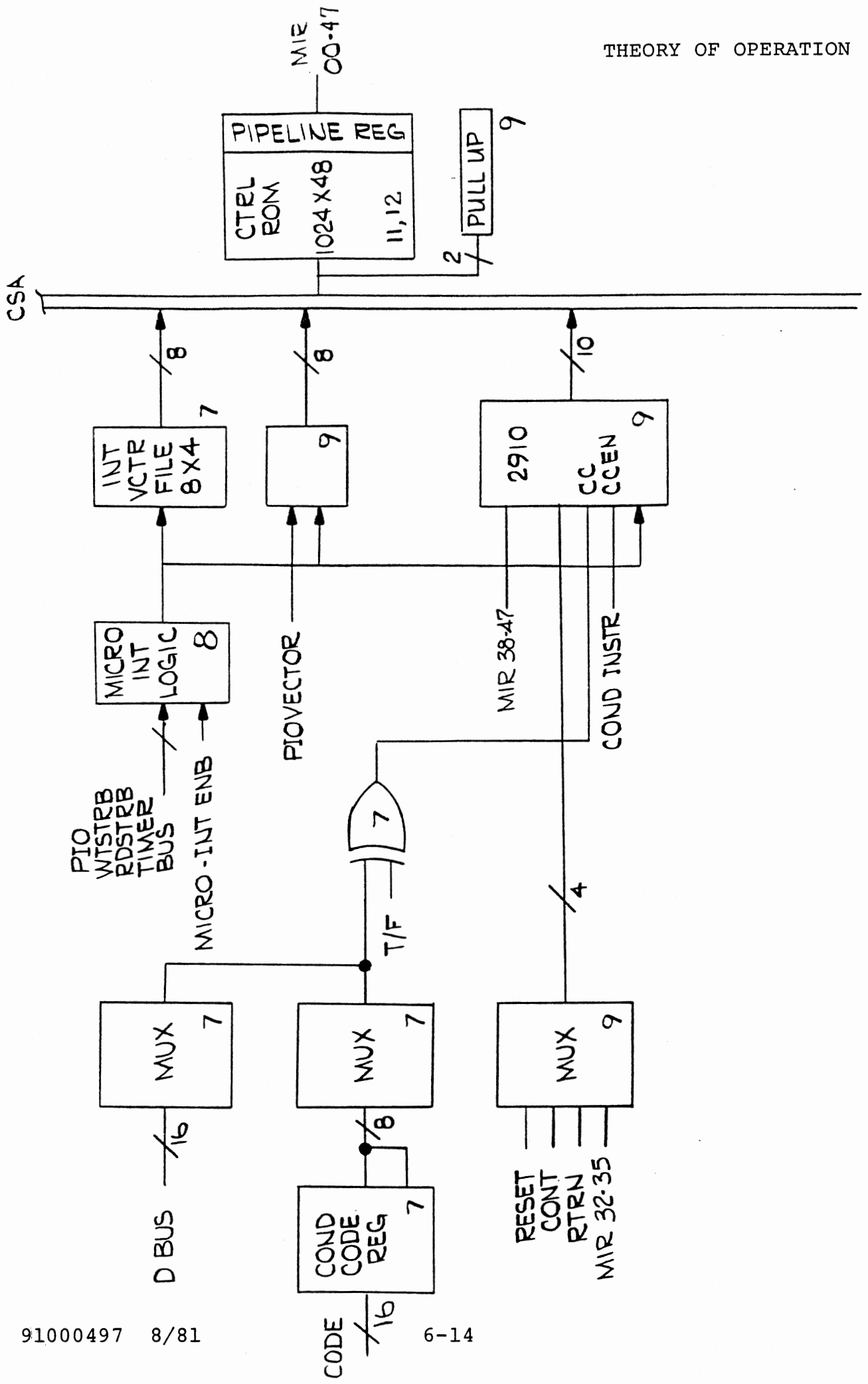


FIGURE 6-7 MICROPROGRAM ADDRESS PROCESSOR

MIR26 determines the true/false sense of the conditional test. MIR25 selects DBIT TEST over condidtion code test. A four bit field, MIR28-31, selects one of 16 conditions codes or one of the bits on the DBUS for testing.

6.20 The second and third sources of microprogram address are the result of one of the five microlevel interrupts. All interrupt vectors are 8 bits wide with the two remaining address lines pulled-up, forcing all interrupts in the range of 300-3FF. PIO interrupts are in the range of 3F0-3FF.

6.21 When the controller's device address is detected by the Unibus sequencer, it generates an interrupt which is processed when microlevel interrupts are enabled and that interrupt has priority. The interrupt vector constructed gives a unique entry point for each TM11 register and whether the register is to be read or written.

6.22 The second interrupt source is the interrupt vector file. The vector file is 8 bits wide and four words deep providing one programmable vector for each of the remaining interrupts. This file provides 256 entry points for the four interrupts, thereby minimizing the overhead to determine the action required when an interrupt occurs.

6.23 Q-BUS INTERFACE. The controller interfaces to the QBUS using only the A and B slots of a quad backplane. The only connection to the C and D slots are to pass priorities. DEC QBUS compatible 2908 and 8641 transceivers, 8640 receivers and 7438 drivers are used in the QBUS interface. The controller presents one unit load on the QBUS. Refer to Figure 6-8 for a block diagram of the QBUS interface.

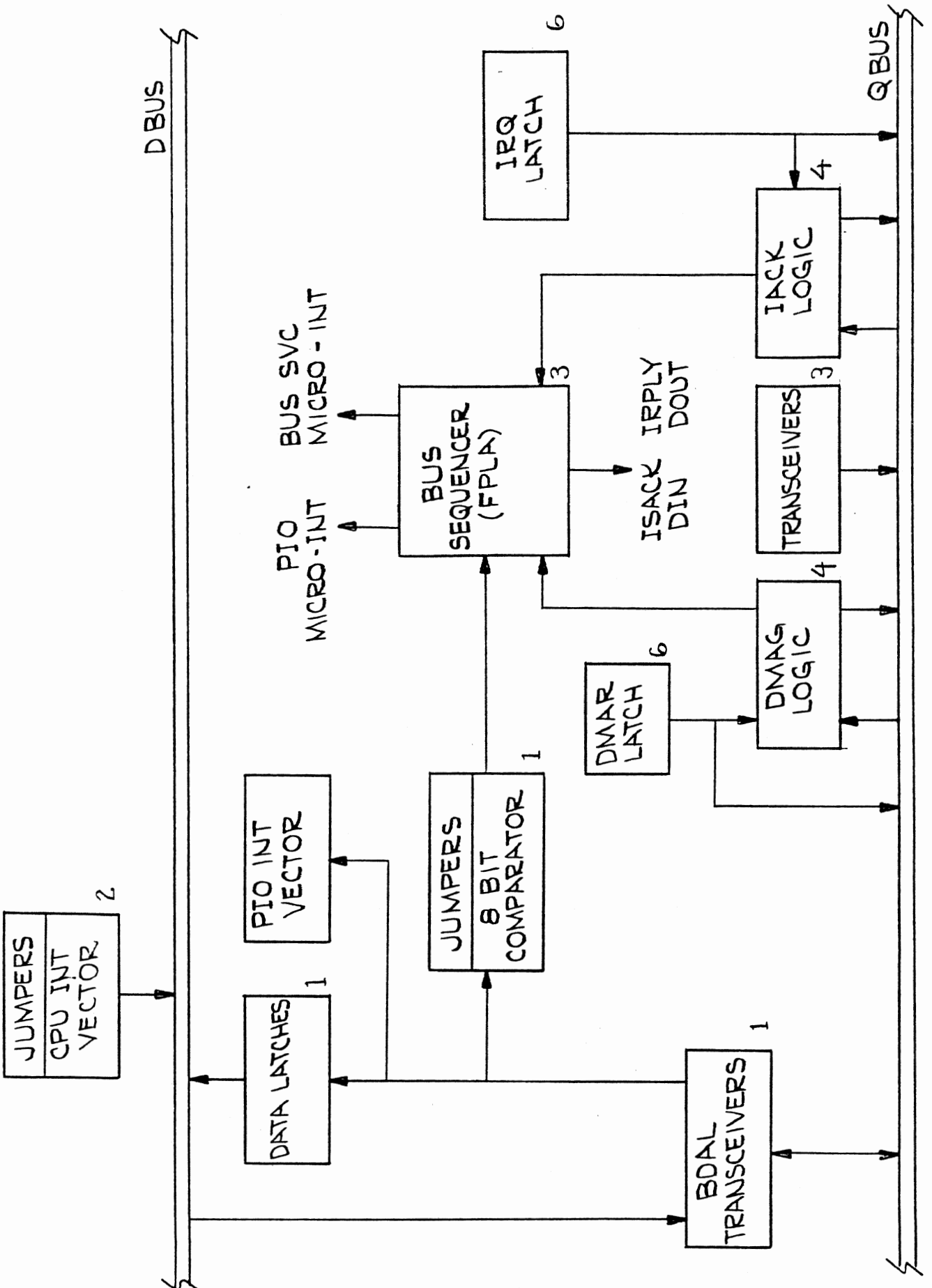


FIGURE 6-8 QBUS INTERFACE

6.24 Address/Data Transceivers

The QBUS time multiplexes the address and data information on one 16 bit bus. Four 2908 transceivers are used to connect with this bus. The bus control and extended addressing signals are handled through two 8641 transceivers. The 2908's receiver latches are always transparent to allow device address monitoring and to feed two octal latches driving the DBUS for access to QBUS data. The 2908 driver registers are loaded directly from the DBUS and are used for PIO reading of TM11 registers and holding the address during DMAR cycles. If the DMAR cycle is a write memory, then the data also passes through the 2908 driver registers.

Device address recognition is the result of BS7 and A04 being set and A05-A12 matching the device address switches at the leading edge of SYNC. Bits A01-A03 select the TM11 register and A00 determines the high or low byte. Device address recognition generates a micro-level interrupt vectored to hex address 3FX. The offset "X" is defined by A01-A03 and the direction control DIN. Thus, PIO read register operations cause microlevel interrupts to locations 3F8-3FF and PIO write operations to locations 3F0-3F7. Write Byte operations are handled by controlling the clock to the 2901's.

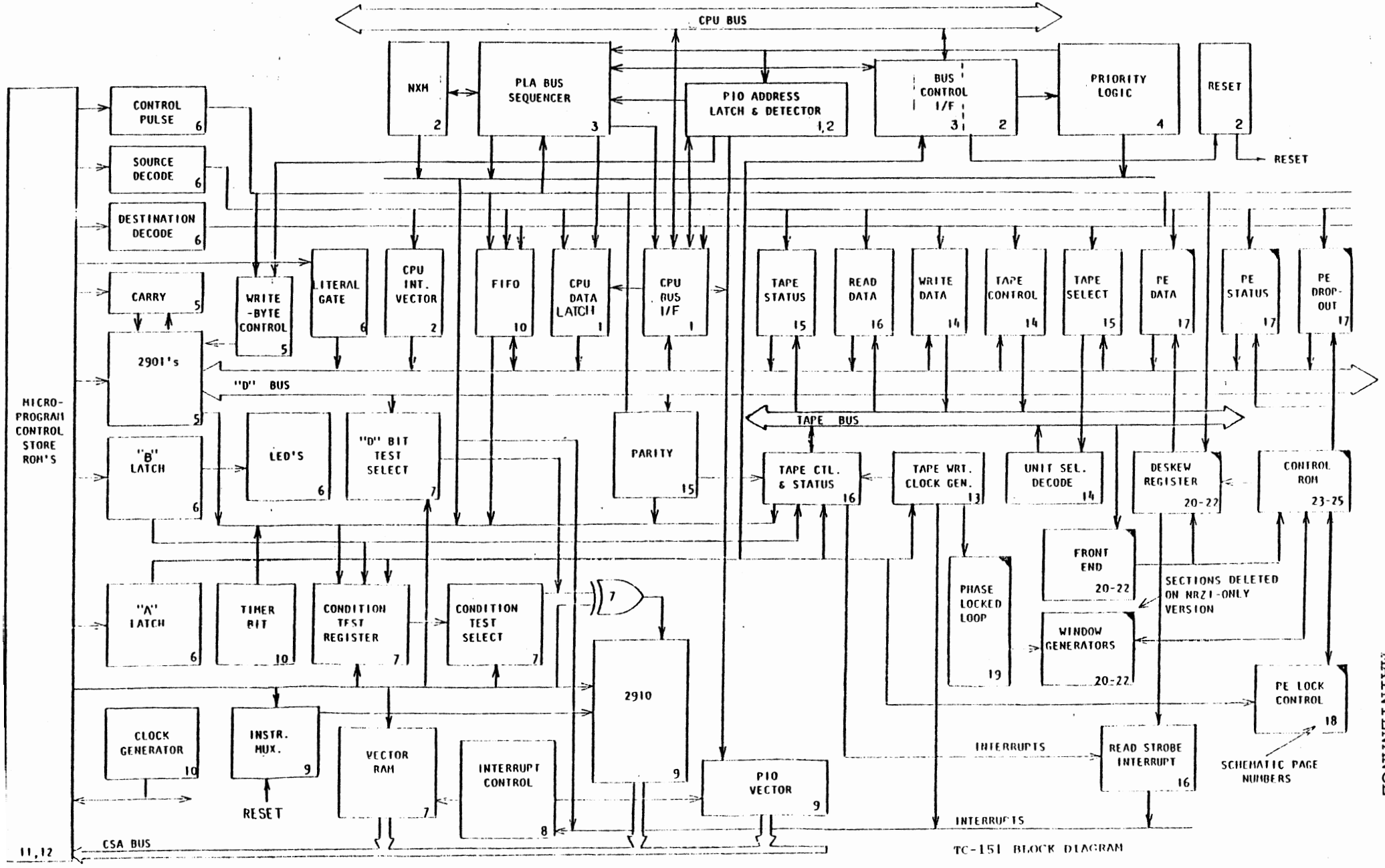
6.25 Direct Memory Access Requests (DMAR)

The controller uses DMAR's for all data transfers associated with write or read data commands to the TM11. A DMAR transaction is initiated by the controller's main firmware, executed by the FPLA bus sequencer and the QBUS, and terminated by the main firmware. The DMAR signal and transfer direction signal, IWTBT are set/reset latches controlled by the firmware. Once the DMAR signal is set the FPLA monitors the QBUS for the appropriate responses and assumes bus master. The bus sequencer will then interrupt the micro-program which loads the memory Address. If it is a Write memory cycle the micro-program will also load the data after the appropriate delay and allow the bus sequencer to complete the cycle by reseting DMAR. If it is a read memory cycle the micro-program turns control over to the bus sequencer which generates another interrupt when the memory responds with data. The micro-program will take the data and direct the bus sequencer to complete the operation by resetting DMAR.

6.26 Bus Interrupt Request

The Bus Interrupt Request is used to interrupt the CPU at a desired point in a TM11 command if the interrupt enable bit in MTC is set. A Bus Interrupt Request is initiated by the firmware, executed by the FPLA bus sequencer and the QBUS, andthen terminated by the main firmware. The IRQ latch is set

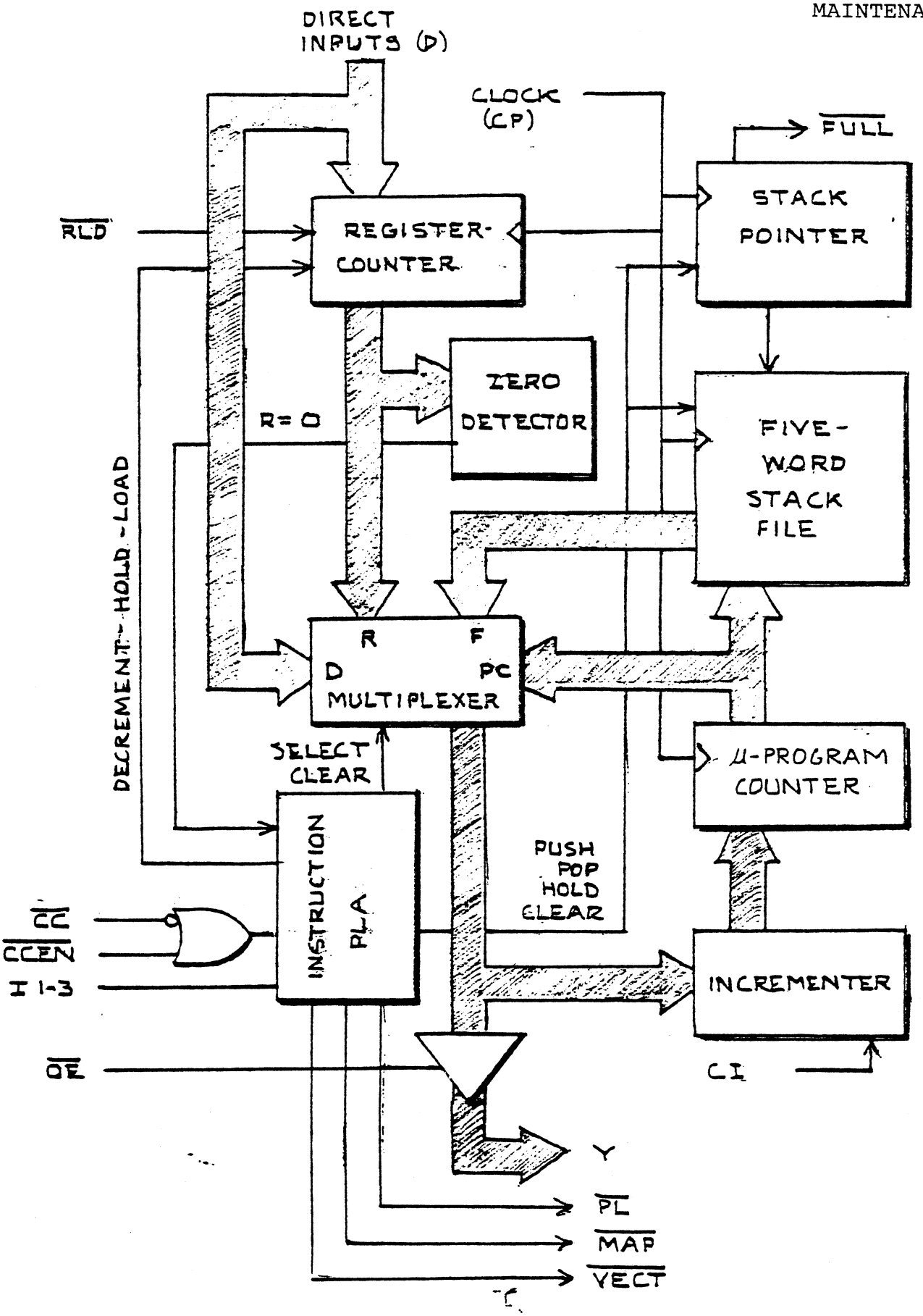
by the firmware and causes the bus sequencer to actively monitor the QBUS and assume bus master. A micro-level interrupt is thengenerated to obtain the vector. The micro-program suppliesthe vector and resets IRQ directing the bus sequencer to complete the bus operation.



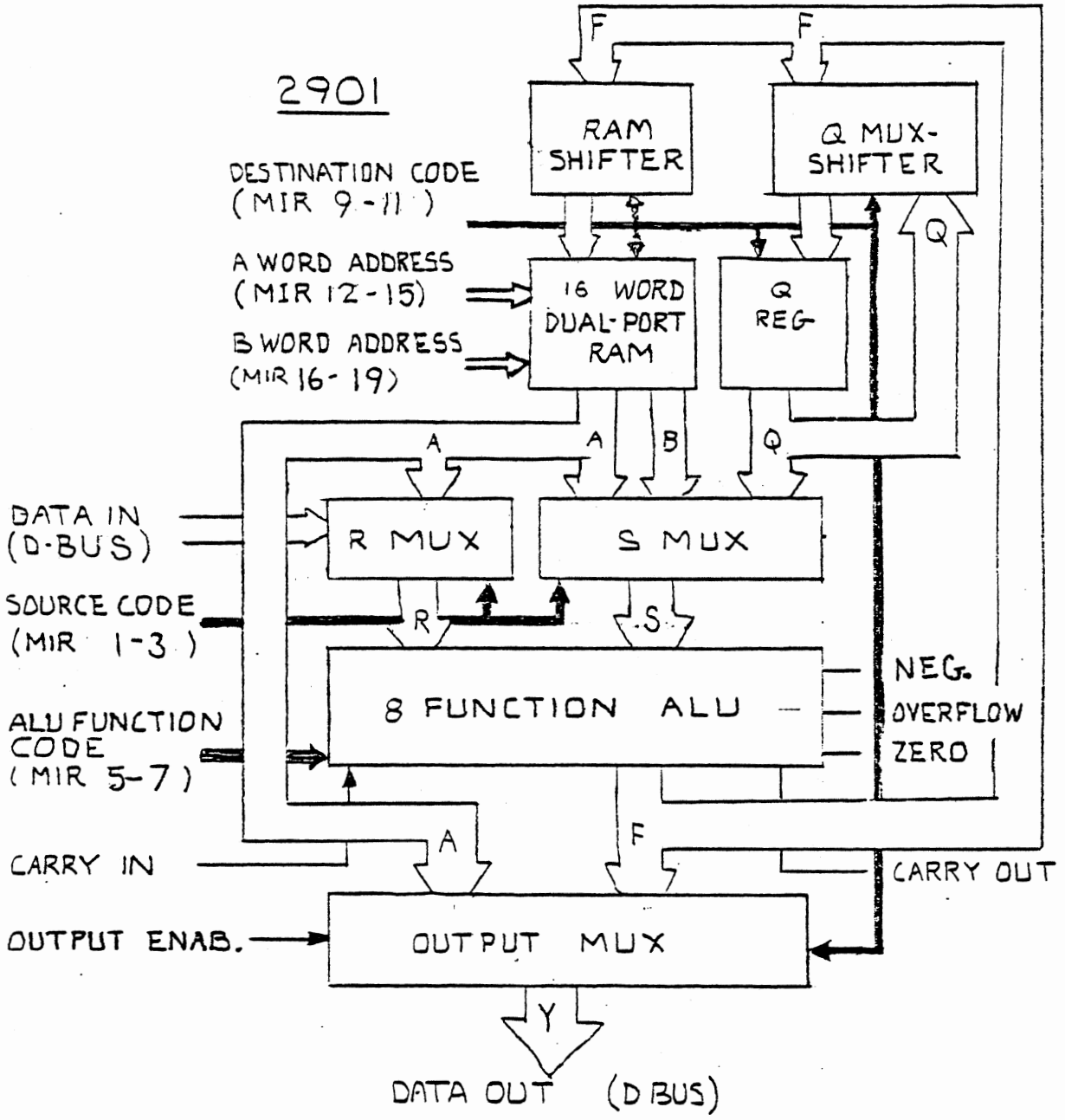
TC-151 BLOCK DIAGRAM

SELF-TEST SEQUENCE AND DESCRIPTION

LEDS #5 4321	TEST-DESCRIPTION	LISTING PAGE
1F	2910 LOOP CNTR, Q REG	3
1E	INCR/DECR Q REG, CARRY OUT	4
1C	SHIFT Q REG, LITERALS, XOR	5
18	POWER UP CONDITION TEST	6
10	REG FILE SHIFT TEST	7
07	2901 REG. ADDRESSING	8
01	REGISTERS - MOVING ZERO	9
02	CARRY CONTROL TEST	10
03	FIFO OPERATION TEST	11
04	WRITE FIFO TEST	12
05	READ FIFO TEST	13
06	PARITY TEST	14
08	MICRO-INTERRUPT TEST	15
00	PASS	16



2910 BLOCK DIAGRAM


2901
F
F
RAM SHIFTER
Q MUX-SHIFTER
DESTINATION CODE (MIR 9-11)
A WORD ADDRESS (MIR 12-15)
B WORD ADDRESS (MIR 16-19)
16 WORD DUAL-PORT RAM
Q REG
Q
A
A
B
Q
DATA IN (D-BUS)
R MUX
S MUX
SOURCE CODE (MIR 1-3)
R
S
8 FUNCTION ALU
NEG.
OVERFLOW
ZERO
ALU FUNCTION CODE (MIR 5-7)
CARRY IN
A
F
CARRY OUT
OUTPUT ENAB.
OUTPUT MUX
Y
DATA OUT (D BUS)

	MAIN CONTROLLER BOARD			
	CONNECTOR A		CONNECTOR B	
	1	2	1	2
A	BIRQ5L-4	*5V-Ø	BDCOKH-2	*5V-Ø
B	BIRQ6L-4			
C	BDAL16L-3	*GND-Ø		*GND-Ø
D	BDAL17L-3		BE2 →	
E		BDOUTL-3	SCHEMATIC	BDAL02L-1
F	SCHEMATIC	BRPLYL-3	CONNECTOR	BDAL03L-1
H	PAGE NUMBER	BDINL-3	SYMBOL	BDAL04L-1
J		BSYNCL-3		BDAL05L-1
K		BWTBTL-3		BDAL06L-1
L		BIRQ4L-4		BDAL07L-1
M		BIAKIL-2 **		BDAL08L-1
N	BDMRL-4	BIAKOL-4 **	BSACKL-4	BDAL09L-1
P		BBS7L-3	BIRQ7L-4	BDAL10L-1
R		BDMGIL-2 **		BDAL11L-1
S		BDMGOL-4 **		BDAL12L-1
T	*GND-Ø	BINITL-2	*GND-Ø	BDAL13L-1
U		BDALOOL-1		BDAL14L-1
V		BDAL01L-1		BDAL15L-1

TC-151 BUS CONNECTIONS

1 = COMPONENT SIDE 2 = SOLDER SIDE

* ONLY INDICATED POWER & GND CONNECTIONS ARE MADE TO CONNECTORS C, D, AND PE ADAPTER CONNECTORS A & B.

** THESE SIGNALS ARE JUMPERED ON CONNECTOR C & PE ADAPTER CONNECTOR A

APPENDIX A

SIGNAL GLOSSARY

TC-151 SIGNAL GLOSSARY

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 1	
ADDR	Controller Address detected
BDALØØL-15L	Data/Address lines
DALØØ-15	Data/Address lines (internal)
DBUSØØ-15	Data Bus (internal)
SOURCE - SCHEMATIC PAGE 2	
AØØ-03	Address lines
BDCOKH	DC Power OK
BDMGIL	DMA Grant In
BIAKIL	Interrupt Acknowledge In
BINITL	Initialize
DBUSØØ-Ø7	Data Bus lines
DCLO	DC Power Low
DMG	DMA Grant
IAKI	Interrupt Acknowledge In
PIO ADDR	Programmed I/O Address
RESET	Controller Reset
SOURCE - SCHEMATIC PAGE 3	
BBS7L	Bank 7 Selected
BDAL16L, 17L	Expanded Data/Address lines
BDINL	Data In

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 3 (CONT.)	
BDOUTL	Data Out
BRPLYL	Reply
BSYNCL	Sync
BS7	Bank 7 Selected
BWTBTL	Write-Byte
DALSTRB	Data/Address Latch Strobe
DDRBUS	Delayed Drive Bus
DIN	Data In
DIO	Data In-Out
DISYNC	Delayed Internal Sync
DRBUS	Drive Bus
DRPLY	Delayed Reply
ISACK	Internal SACK
NXM	Non-Existent Memory
REPLY	Reply
PIO	Programmed I/O Operation
SVC	Service
SYNC	Sync
WTBT	Write-Byte
SOURCE - SCHEMATIC PAGE 4	
BDMGOL	DMA Grant Out
BDMRL	DMA Request

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHFMATIC PAGE 4 (CONT.)	
BIAKOL	Interrupt Acknowledge Out
BIRQ4L-7L	Interrupt Request Lines
BSACKL	Selection Acknowledge
DMABSY	DMA Busy
GRANT	Grant
PRIORITY	Priority
SOURCE - SCHEMATIC PAGE 5	
ALUCO	Carry Result
ALUNEG	Negative Result
ALUZ	Zero Result
DBUSØØ-15	Data Bus (internal)
LBYTCLK	Lower Byte Clock
QLINK	Q-Register Rotate Connection
RLINK	RAM Rotate Connection
UBYTCLK	Upper Byte Clock
SOURCE - SCHEMATIC PAGE 6	
BUSSEQ	Bus Sequence
BYTE	Byte-Sensitive Operation
CCLR	Controller Clear
CLRFIFO	Clear FIFO

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 6 (CONT.)	
DMAR	DMA Request
DBUSØØ-15	Data Bus (internal)
IBS7	Internal Bank 7 Selected
IDATA	Input Data
IDSL	Internal Density Select
IRQ	Interrupt Request
IWARS	Internal Write Amp. Reset
NOPAR	No Parity
ODATA	Output Data
PEDATA	PE Data
PEDO	PE Drop Out
PE STATUS	PE Status
PUP	Power Up
RBCLK	Read Buffer Clock
RBUF	Read Buffer
RDATA	Read Data
RDGATE	Read Gate
SO	Shift Out
SLECT	Select (Register Load)
TUCMD	Tape Unit Command
TUSTAT	Tape Unit Status
VECTR	Vector (Read)
WBUF	Write Buffer
WDATA	Write Data

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 6 (CONT.)	
WGATE	Write Gate
IWTBT	Internal Write-Byte
SOURCE - SCHEMATIC PAGE 7	
CC	Condition Code
CSAØØ-07	Control Store Address
SOURCE - SCHEMATIC PAGE 8	
CLPIO	Clock PIO
INT	Interrupt
IVSEL A,B	Internal Vector Select
PIOVCTR	PIO Vector
SRESET	Stored Reset
VCTR	Vector
SOURCE - SCHEMATIC PAGE 9	
CSAØØ-09	Control Store Address
SOURCE - SCHEMATIC PAGE 10	
DBUSØØ-07	Data Bus
CLK	Clock
CLKFF	Clock Flip-Flop
IRE	Input Register Empty

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 10 (CONT.)	
MIRCLK	Micro Instr. Register Clock
ORF	Output Register Full
OSC	Oscillator Clock
TIMER	Timer Bit
SOURCE - SCHEMATIC PAGE 11,12	
MIRØØ-47	Micro Instr. Register Bits
SOURCE - SCHEMATIC PAGE 13	
CHARCLK	Character Clock (PE)
CKSEL 1,2,4	PE Clock Select Bits
MØ-6	Speed ROM Bits
WTS	Write Strobe
800 CHAR	800 BPI Character Clock
SOURCE - SCHEMATIC PAGE 14	
FSL	Forward Select (Command)
FWD	Forward Command (Internal)
OVW	Overwrite (Edit Function)
RDS	Read Data Strobe
RSL	Reverse Select (Command)
RWC	Rewind Command
SLTØ-7	Drive Select Lines

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 14 (CONT.)	
WDØ-7,P	Write Data Lines
WDS	Write Data Strobe
WNB	Write Enable
SOURCE - SCHEMATIC PAGE 15	
BOTP	Beginning of Tape
DBUS XX	Data Bus Lines
EOTP	End of Tape
FLPT	File Protect
IA16,17	Internal Addr. Expansion Bits
ONL	On-Line
PARITY	Parity
RWG	Rewinding Status
USEL 1,2,4	Unit Select Bits
WTDP	Write Data Parity
SOURCE - SCHEMATIC PAGE 16	
DBUSØØ-15	Data Bus (Internal)
DSL	Density Select
NRZ	NRZI Status
RDS	Read Strobe
RDY	Ready
RDST	Read Strobe Interrupt

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 16 (CONT.)	
SPD	Speed Select
TRDY	Tape Ready
WARS	Write Amplifier Reset
IWDP	Internal Write Data Parity
SOURCE - SCHEMATIC PAGE 1 (PE)	
ACDO	All Channels Dropped-Out
ATTN	Attention Bit
DBUSØØ-15	Data Bus (internal)
FMK	File Mark
MCDO	Multiple Channel Drop-Out
PEID	PE Identification Burst
PEP	PE Parity
SCDO	Single Channel Drop-Out
SOURCE - SCHEMATIC Page 2 (PE)	
LOCKED	Locked
LOCKENA	Lock Enable
NODATA	No Data (gap)
REFCLK	Reference Clock
VERRA,B,C,D,	Error Voltage Inputs

TC-151 SIGNAL GLOSSARY (CONT.)

MNEMONIC	DESCRIPTION
SOURCE - SCHEMATIC PAGE 19	
24 CLK	PE Read Clock (24X)
SOURCE - SCHEMATIC PAGE 20-22	
COØ-7,P	Carry Out X
FF1Ø-7,P	Flip-Flop 1X
PEDØ-7 P	PE Data X
RDØ-7,P	Read Data X
TRIBIT Ø-2	Tri-Bit-Available Lines
SOURCE - SCHEMATIC PAGE 23-25	
DOØ-7	Drop Out X
FF2Ø-7P	Flip Flop 2X
GATE	Gate (For Data Transition)
LDØ-7,P	Window Counter Load X
MJRØ-7,P	Major Transition X
PERDY	PE Ready
SIØ-7,P	Shift In X
STATE 1	State 1 (Look for Sync)
STATE 2	State 2 (Data State)

western peripherals ™

NO. 1

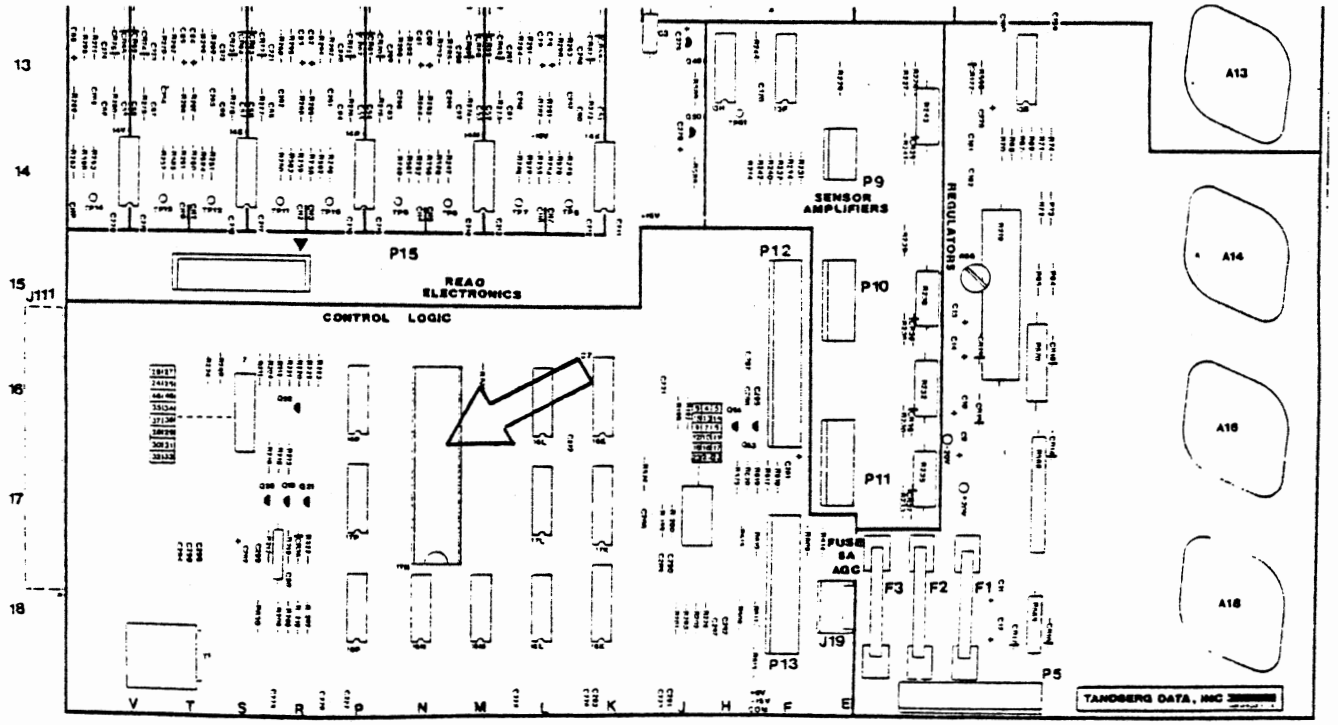
TECH TIPS

TITLE/DESCRIPTION: LRC Character Problems

PRODUCT/MODEL: Tape Drives - CDC Model 92149, Tandberg Model Series TDI 1050, and similar IDT models when used with TC-131 and TC-151 controllers.

SYMPTOM/ACTIVITY: These tape drives exhibit LRC Character problems in the write mode.

ACTION REQUIRED: On the large board of the tape drive, the mask/F8 chip (large device at 17N-see arrow) should be changed from part number 80-00290 to part number 80-00437.



PRINTED CIRCUIT BOARD ASSEMBLY
MAIN ELECTRONICS – STANDARD

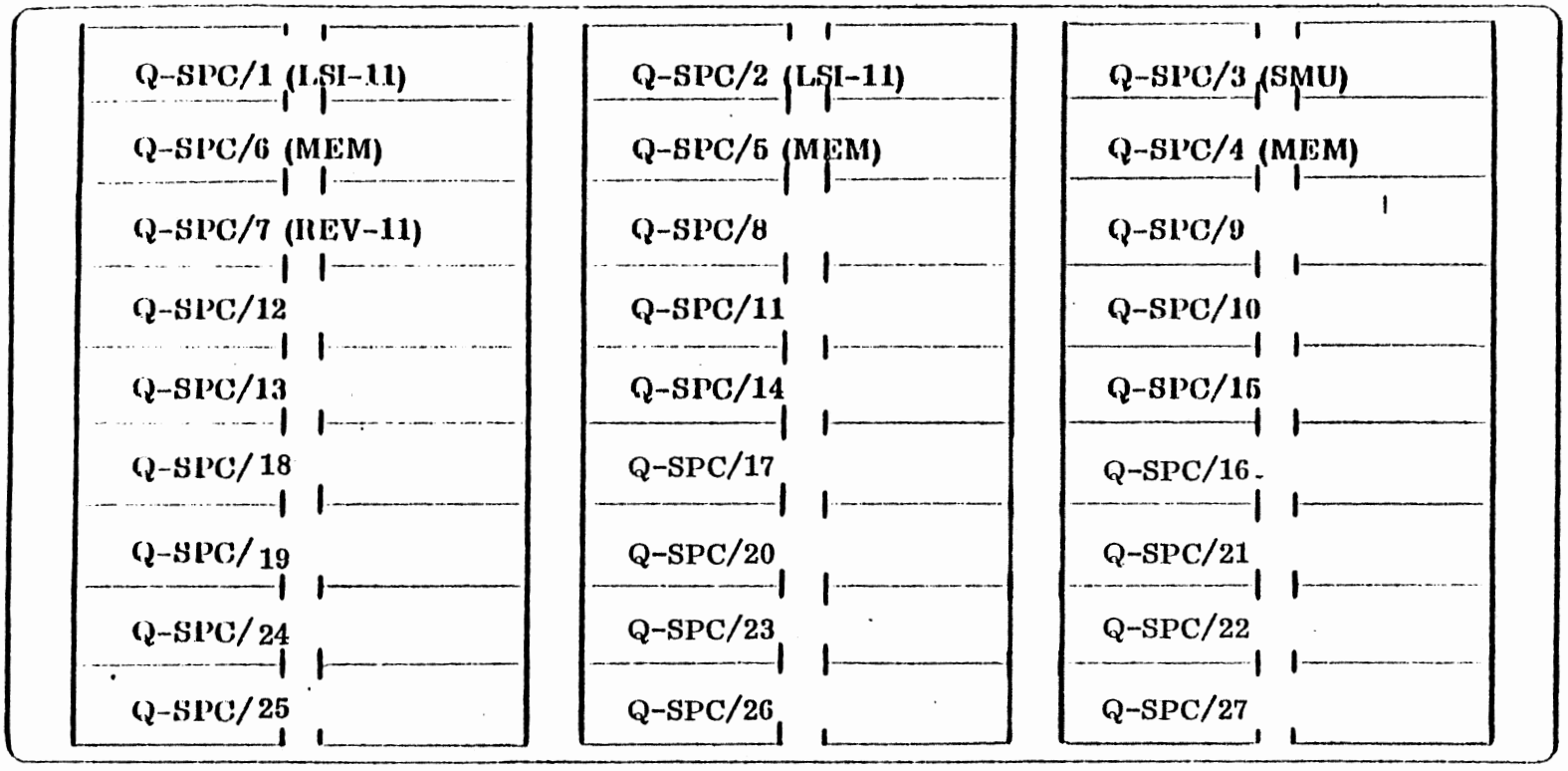
DATE: 1-15-81

NOTE: Items shown in parentheses provide an example of possible configurations. Jumper each unused A, C, and E connector from pin M2 to pin N2 and from pin R2 to pin S2.

WP911/919 Chassis

(Component Side/Side 1)

WP934Q Q-Bus System Unit



(Solder Side/Side 2)

LSI-11 SYSTEM CONFIGURATION

NOTES

WARRANTY

WESTERN PERIPHERALS warrants articles of equipment manufactured by it to be free from defects in material and workmanship under normal use and service, its obligation under this warranty being limited to making good at its factory any article of equipment which shall within one year after delivery of such article of equipment to the original purchaser be returned intact to it, or to one of its authorized service stations, with transportation charges prepaid, and which its examination shall disclose to its satisfaction to have been thus defective; this warranty being expressly in lieu of all other warranties expressed or implied and of all other obligations or liabilities on its part, and WESTERN PERIPHERALS neither assumes not authorizes any other persons to assume for it any other liability in connection with the sale of its products.

This warranty shall not apply to any article of equipment which shall have been repaired or altered outside the WESTERN PERIPHERALS factory or authorized service stations, nor which has been subject to misuse, negligence or accident, incorrect wiring by others, or installation or use not in accord with instructions furnished by the manufacturer.