

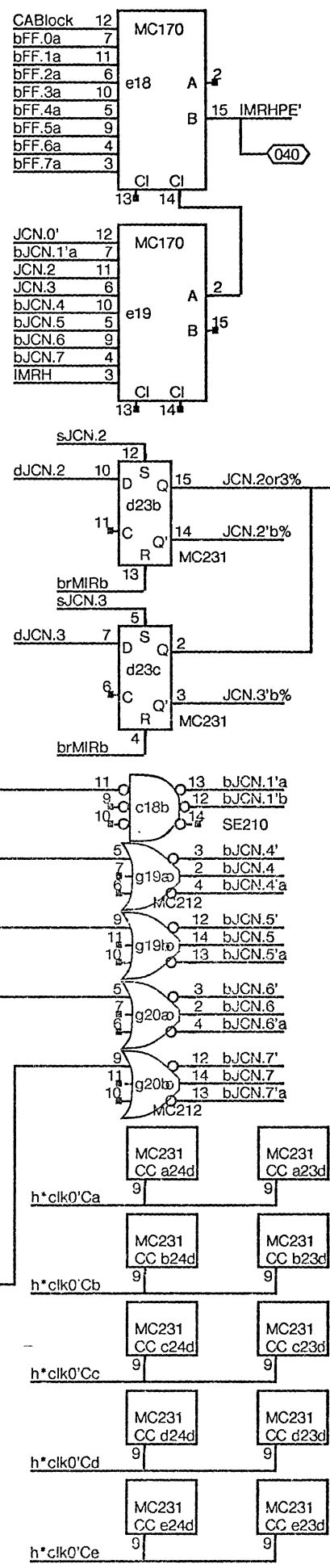
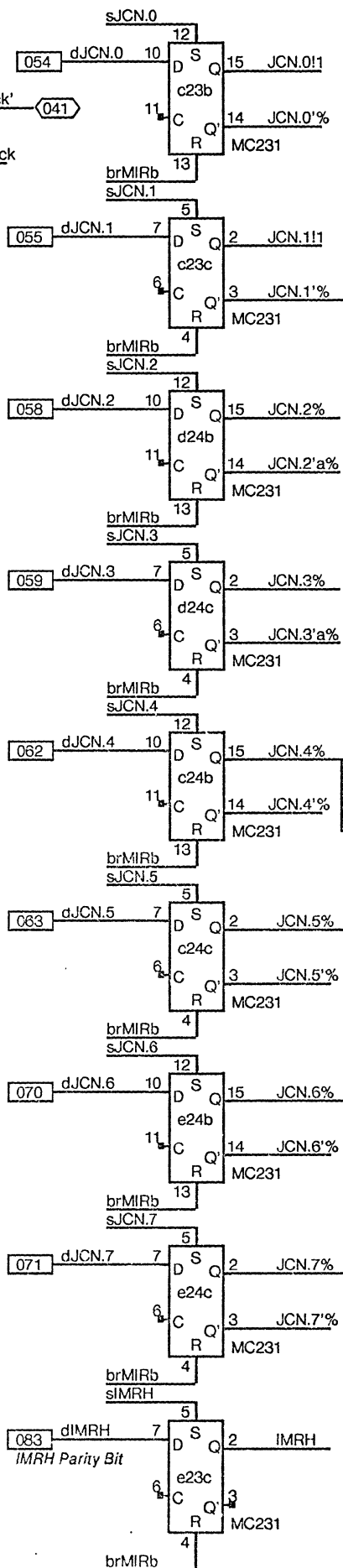
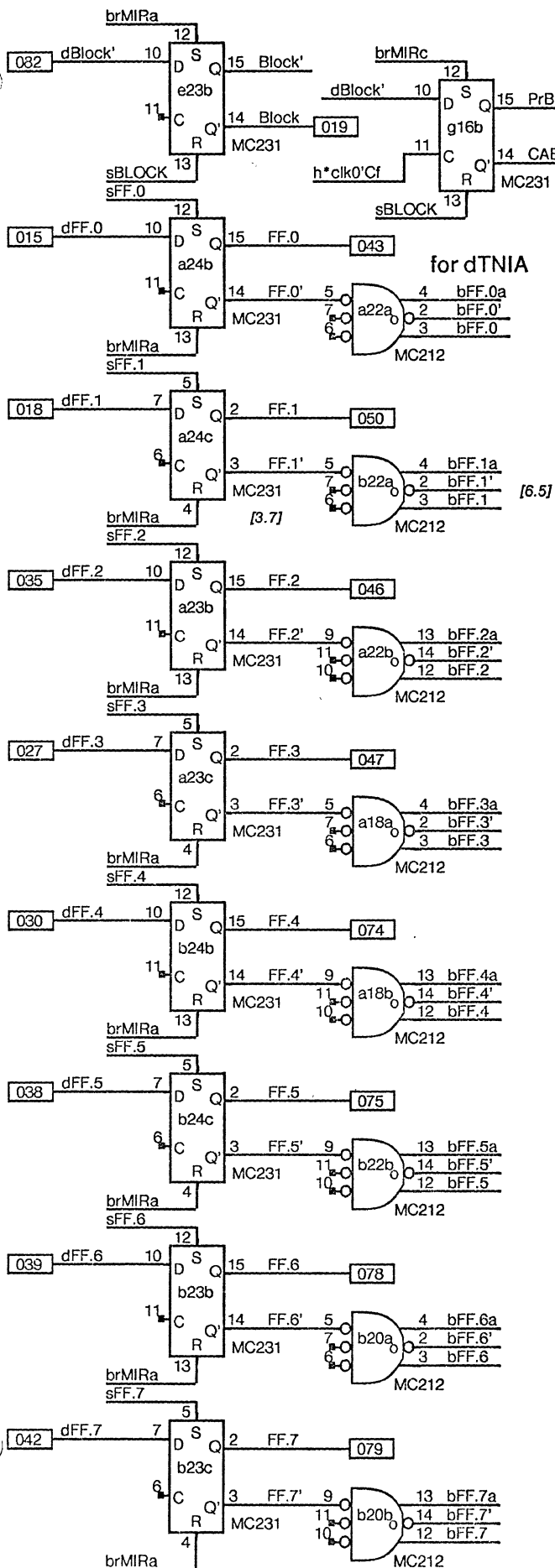
DORADO SCHEMATICS

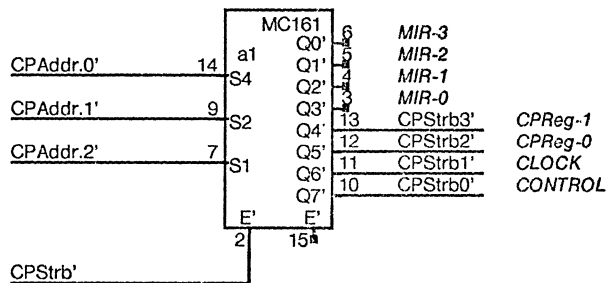
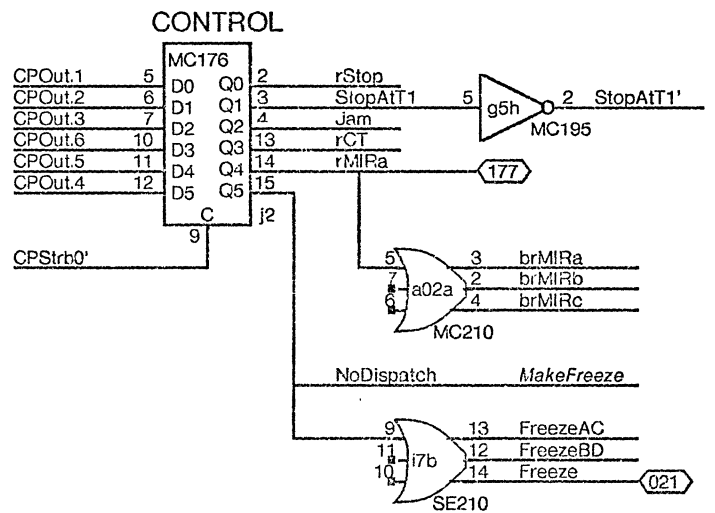
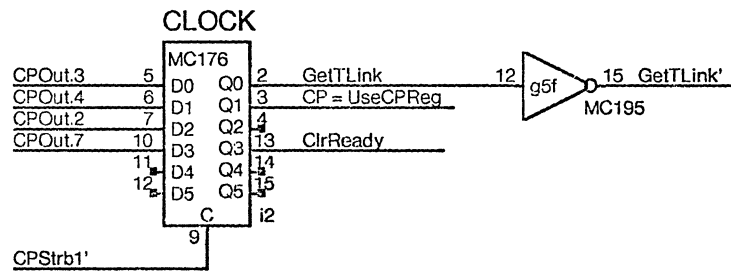
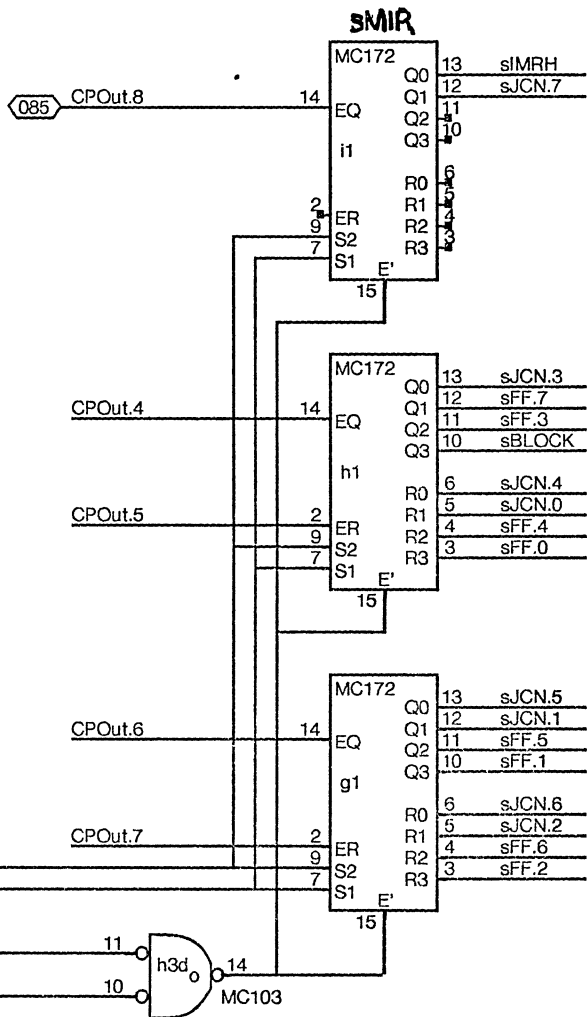
Control A

JUMPER 100 Ω FROM -2V
TO T122 (LC0)

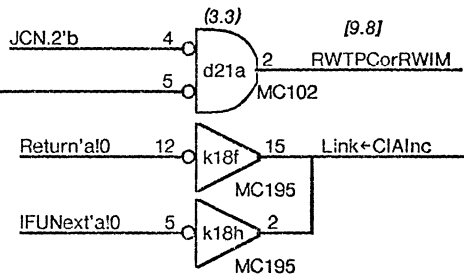
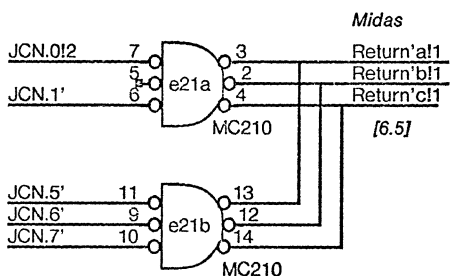
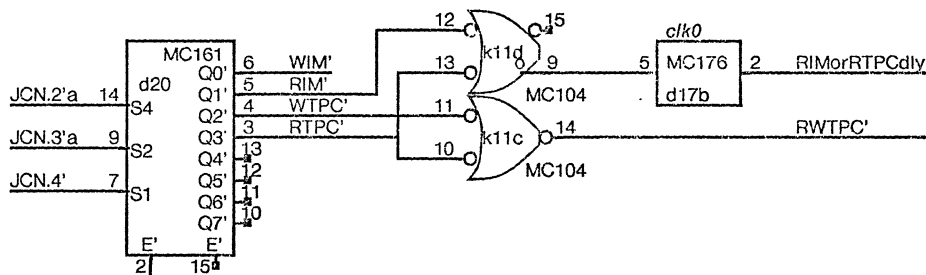
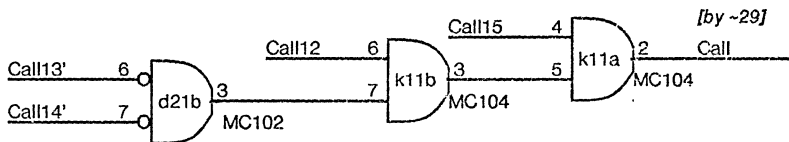
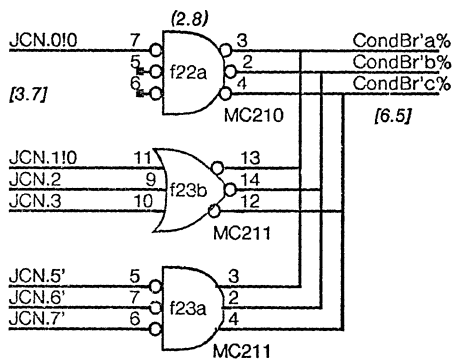
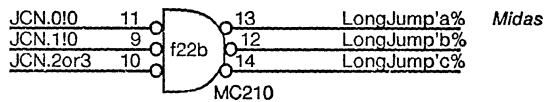
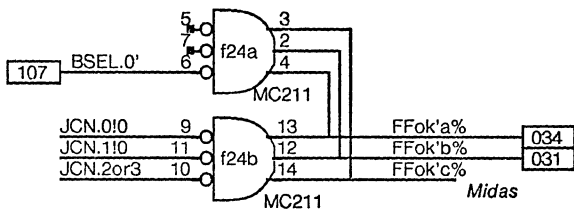
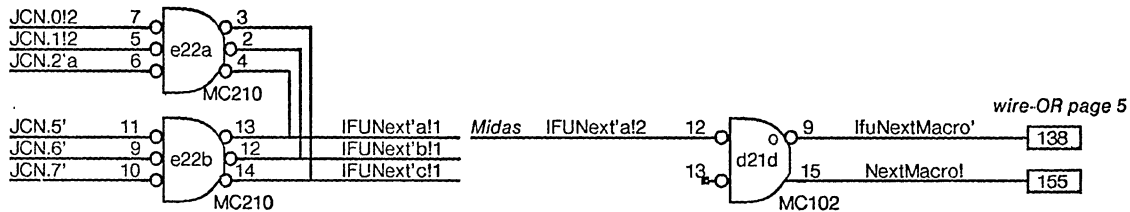
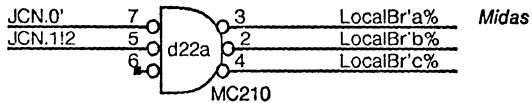
Table of contents

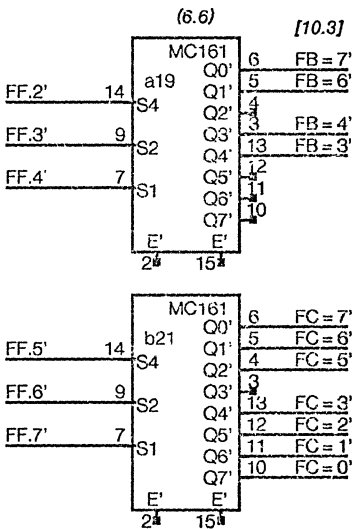
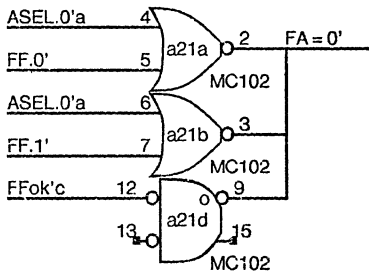
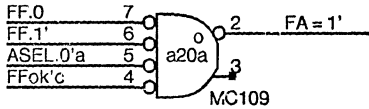
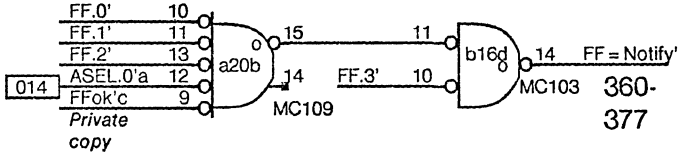
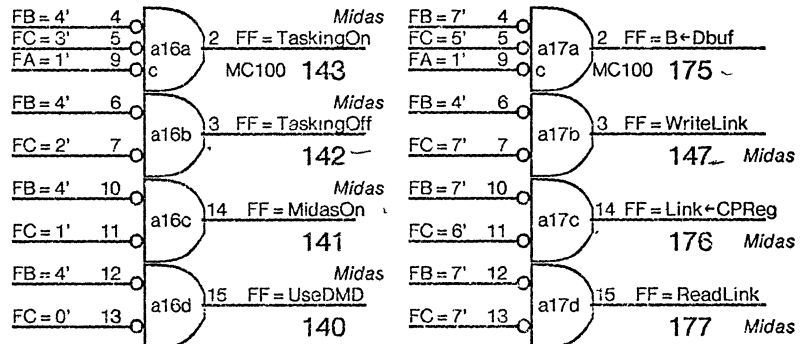
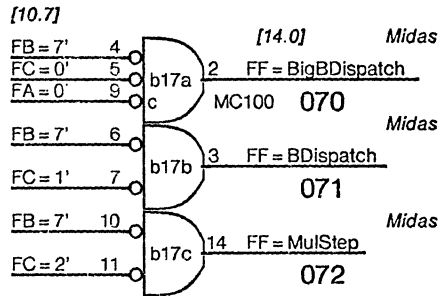
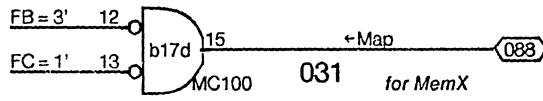
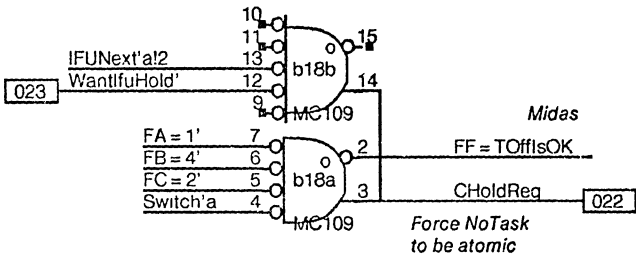
<u>TITLE</u>	<u>Page</u>
MIR- right half _____	01
CP Interface and Set MIR _____	02
JCN Decoding _____	03
FF Decoding _____	04
LinkX and Conditional Branch _____	05
Main Data Path, Bits 00 - 15 _____	06 - 19
Control Slices for Data Path _____	20 - 21
Ready Logic 1 _____	22
Ready Logic 2 _____	23
Wakeup Priority Encoder _____	24
Task Switch logic _____	25
Task Registers: HTASK, BNT, CTASK, CTD, NEXT _____	26
Phase generator _____	27
Midas 1 _____	28
Midas 2 _____	29
Clocks _____	30
PreClock generator _____	31
Memory System Clock generator _____	32
Layout _____	33



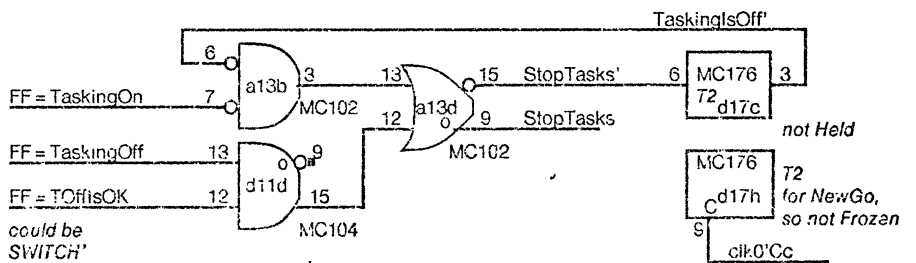
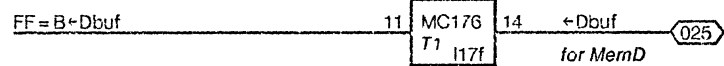
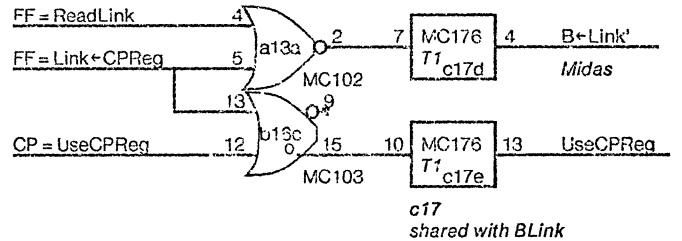
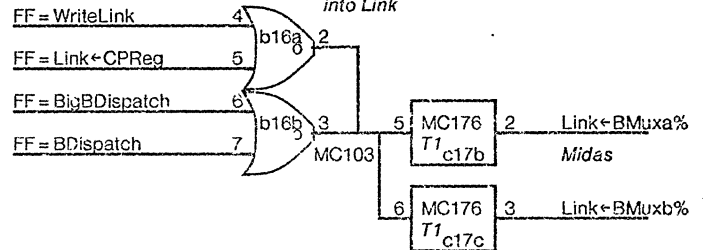


CPReg-1
CPReg-0
CLOCK
CONTROL





FF = Link + CPReg loads compliment of CPReg into Link



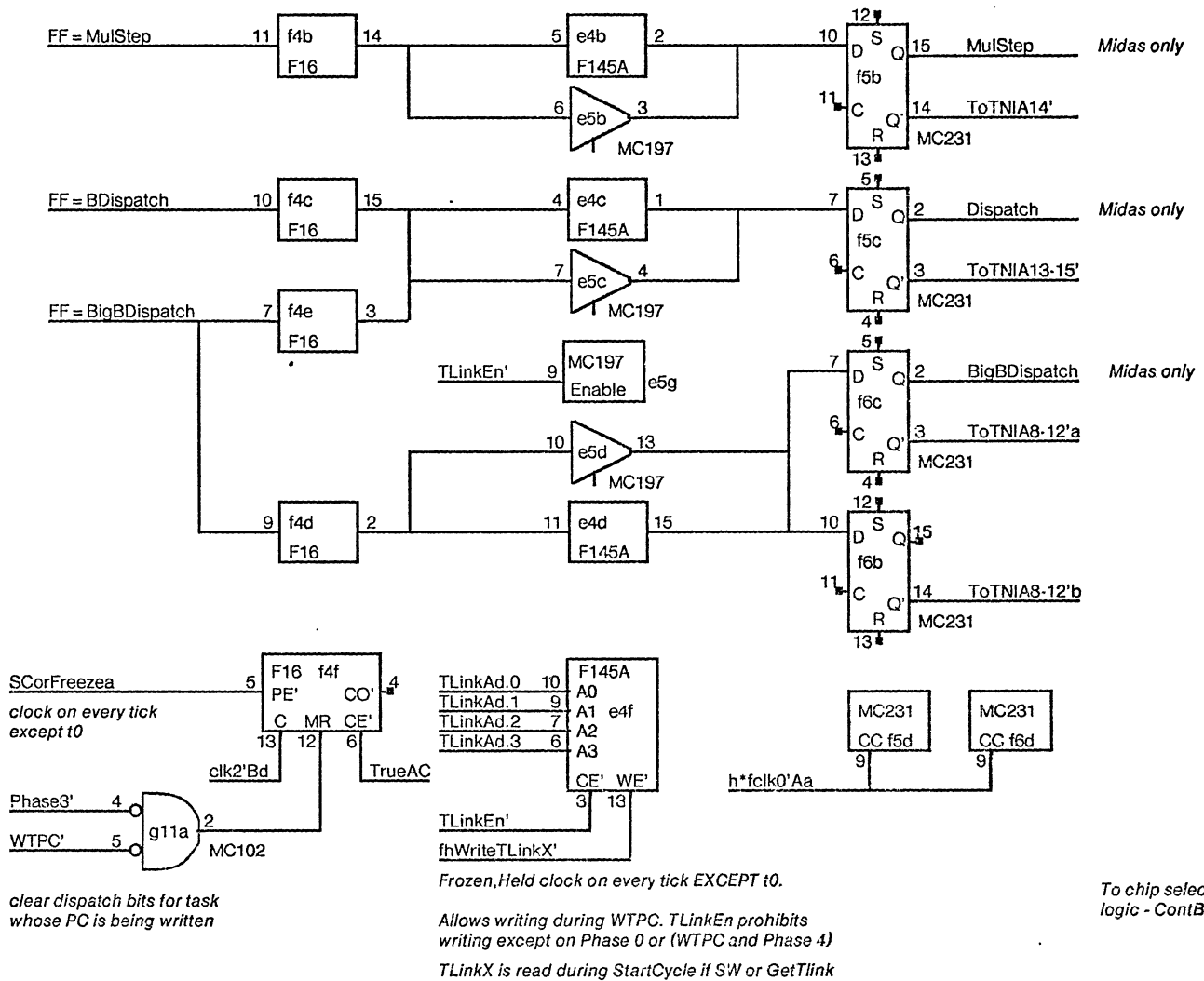
NOTE: TakingOff is aborted and HOLD is requested if Switch is pending when TaskingOff is executed

Link Extension

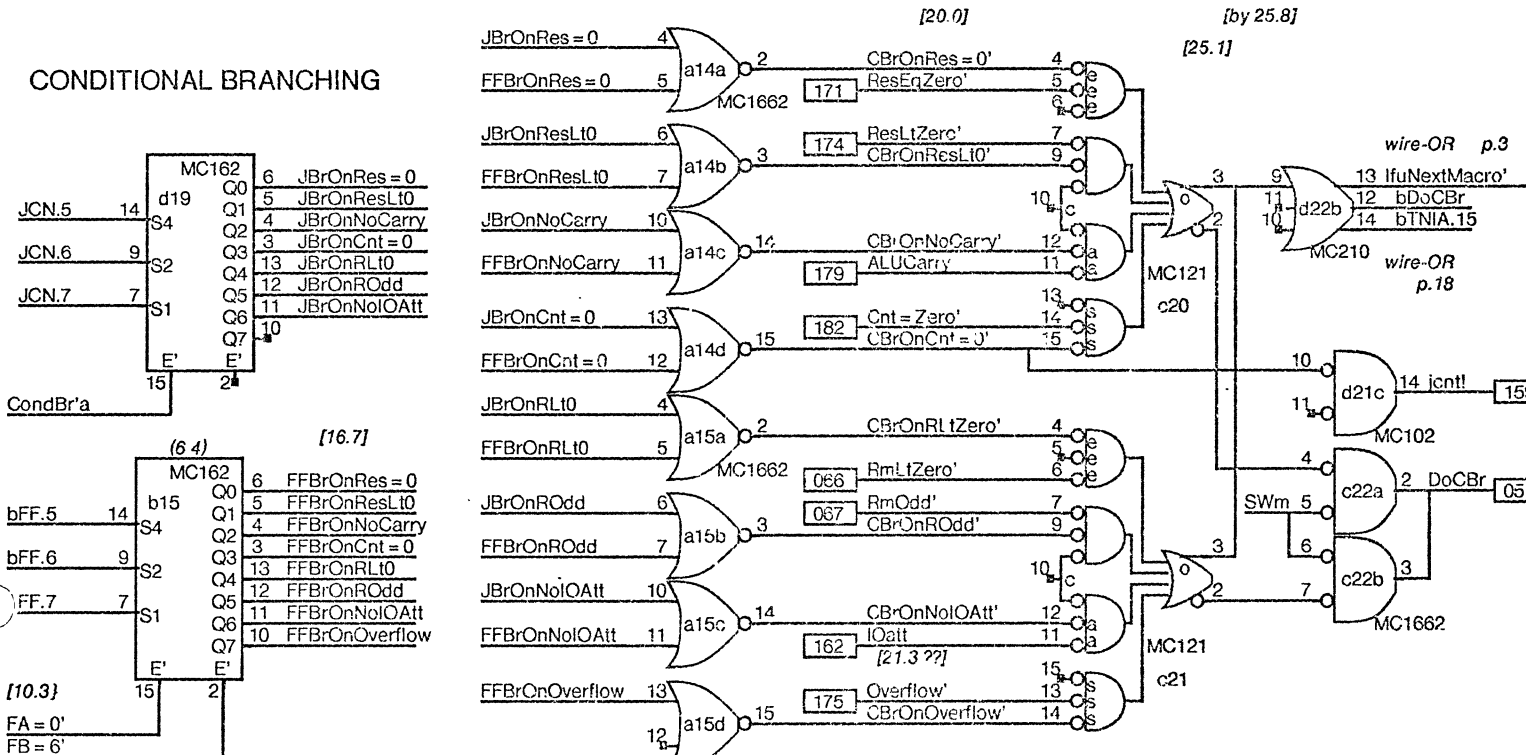
T1.*
no Hold

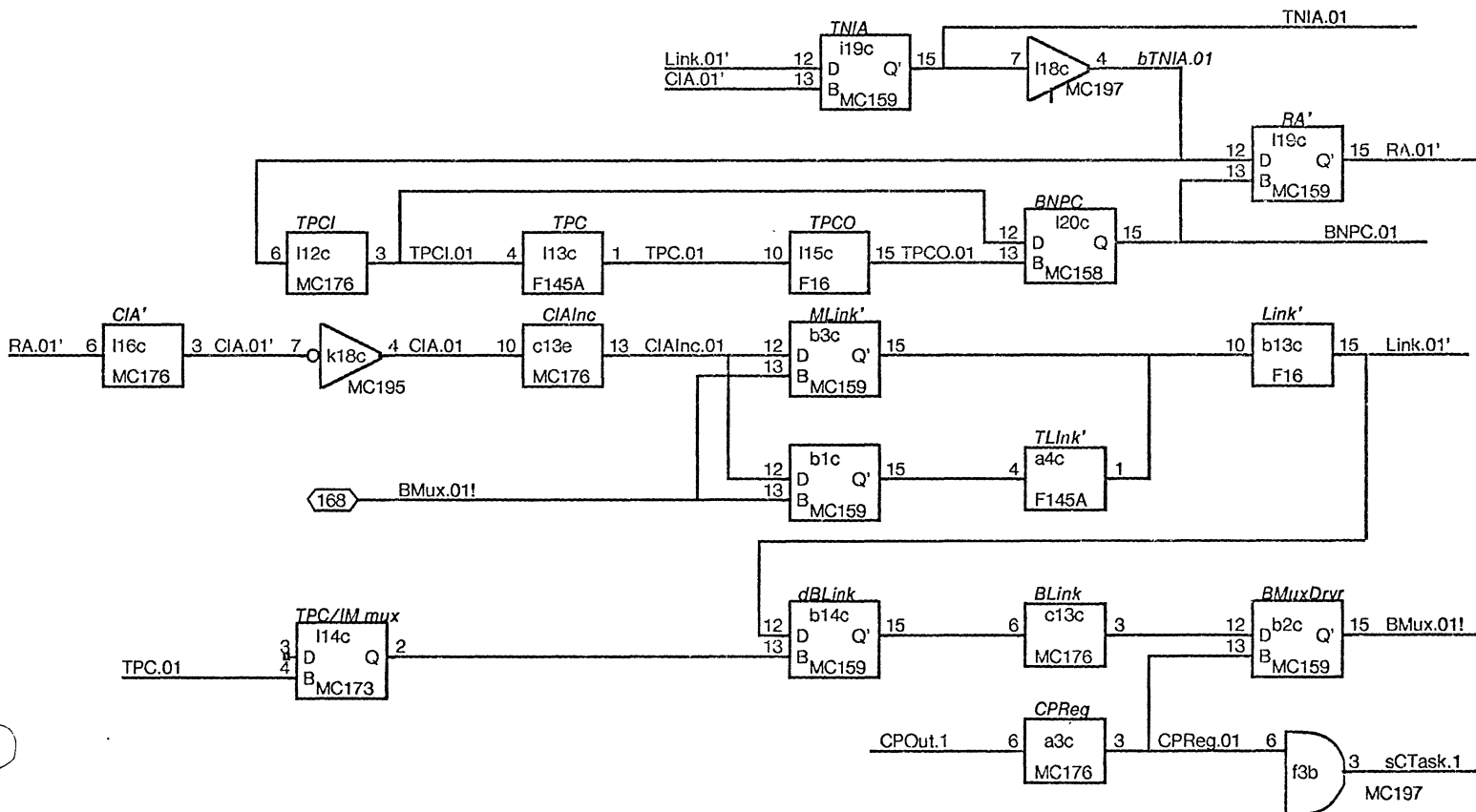
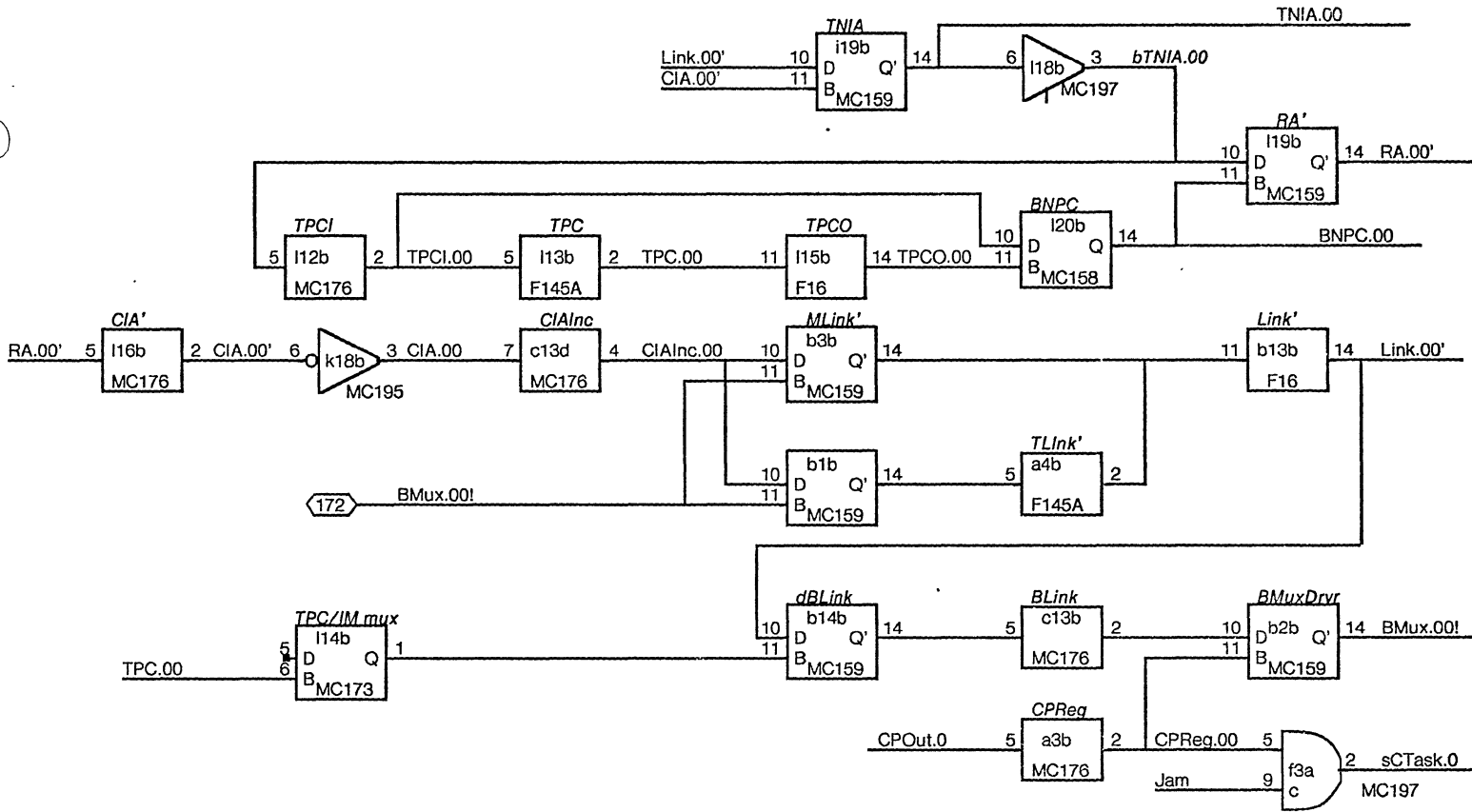
write @ T3
Held

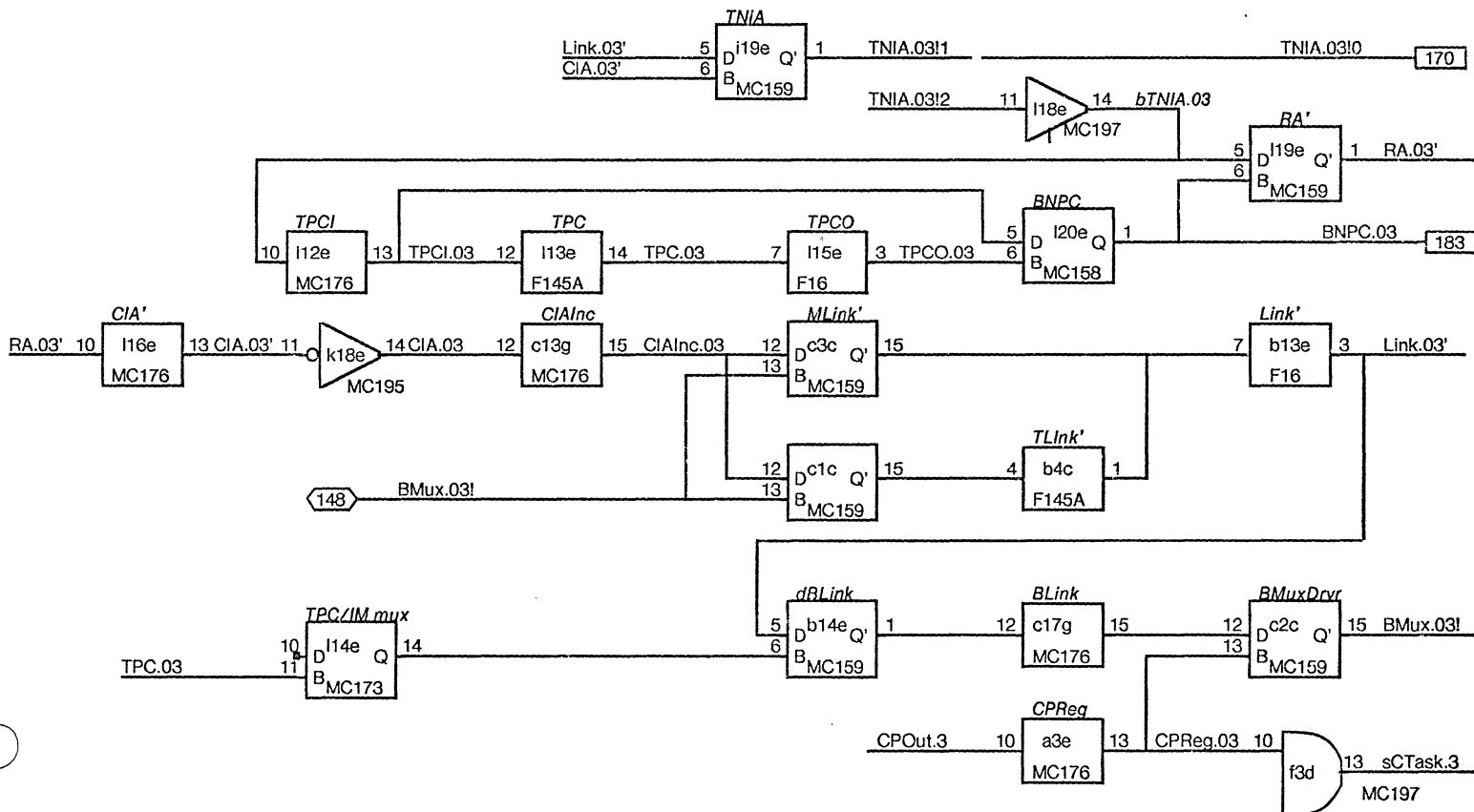
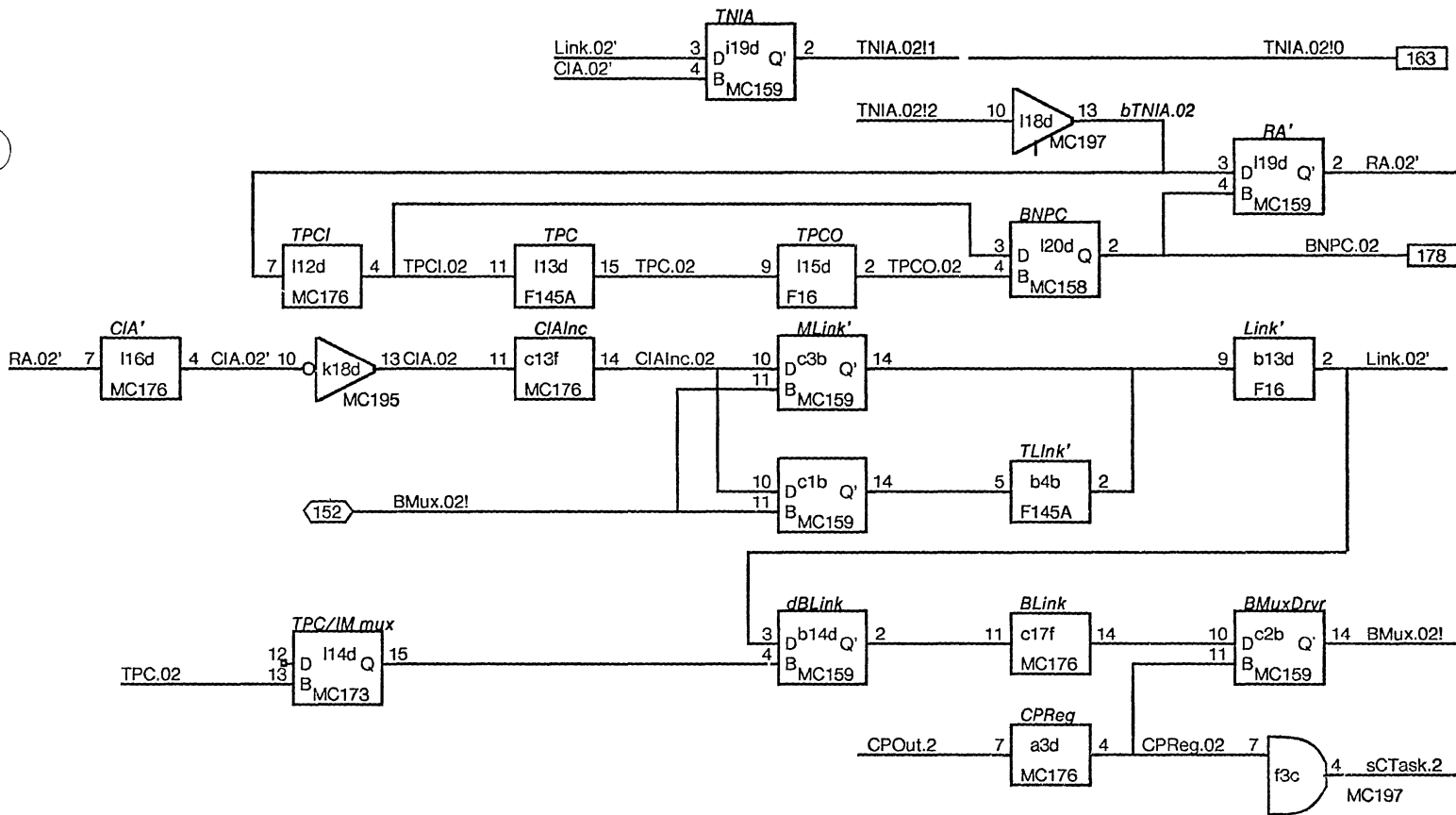
T2
Held unless SwitchUp

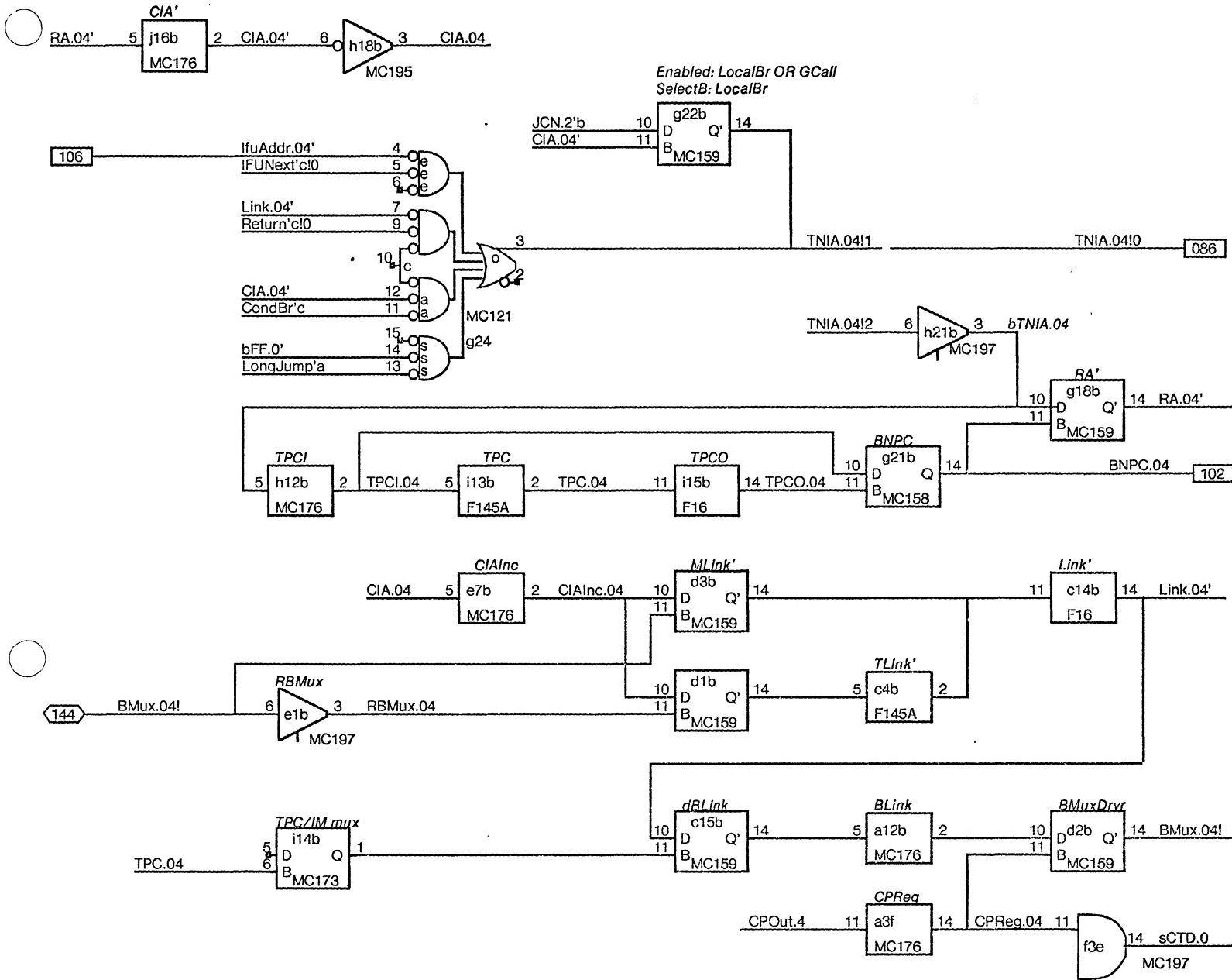


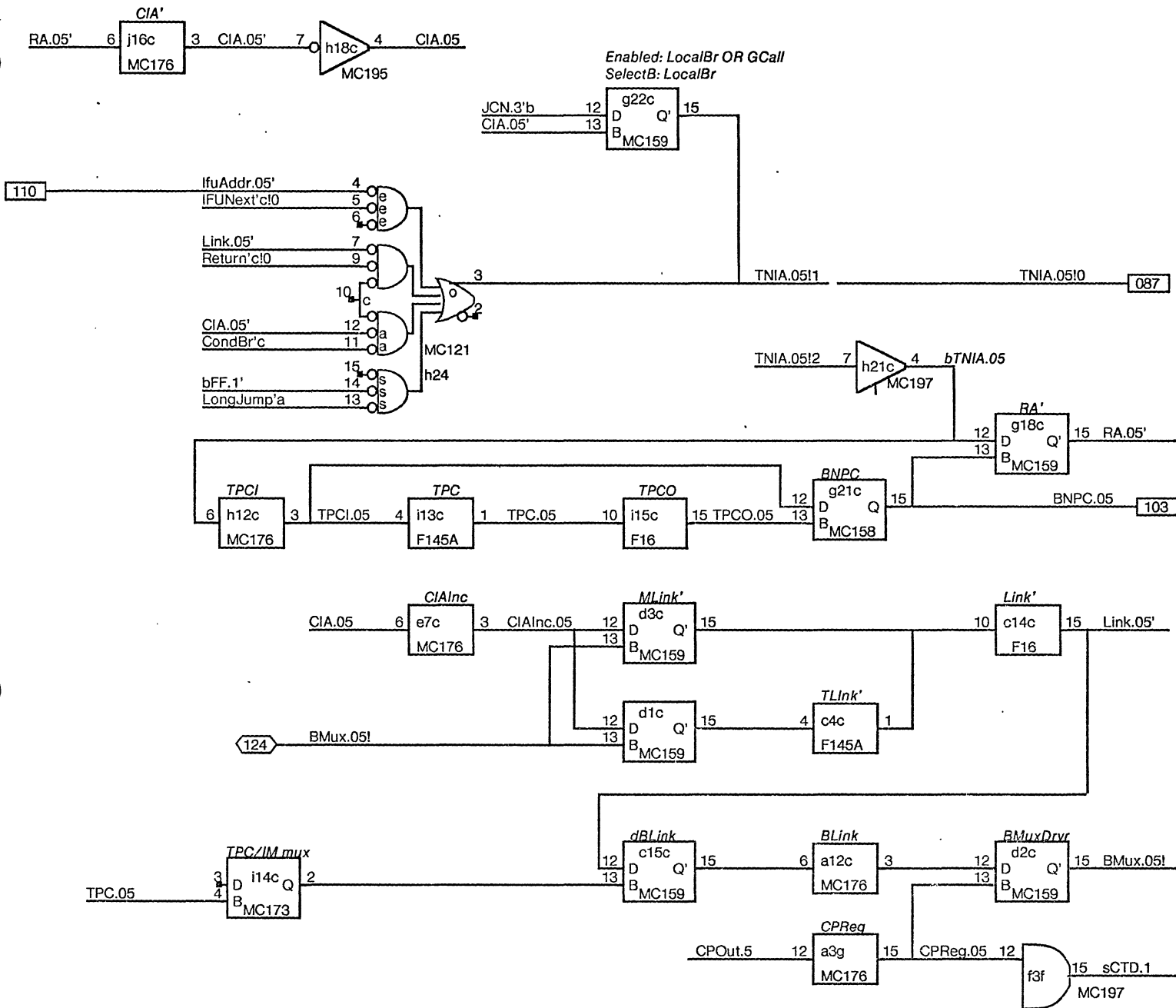
CONDITIONAL BRANCHING

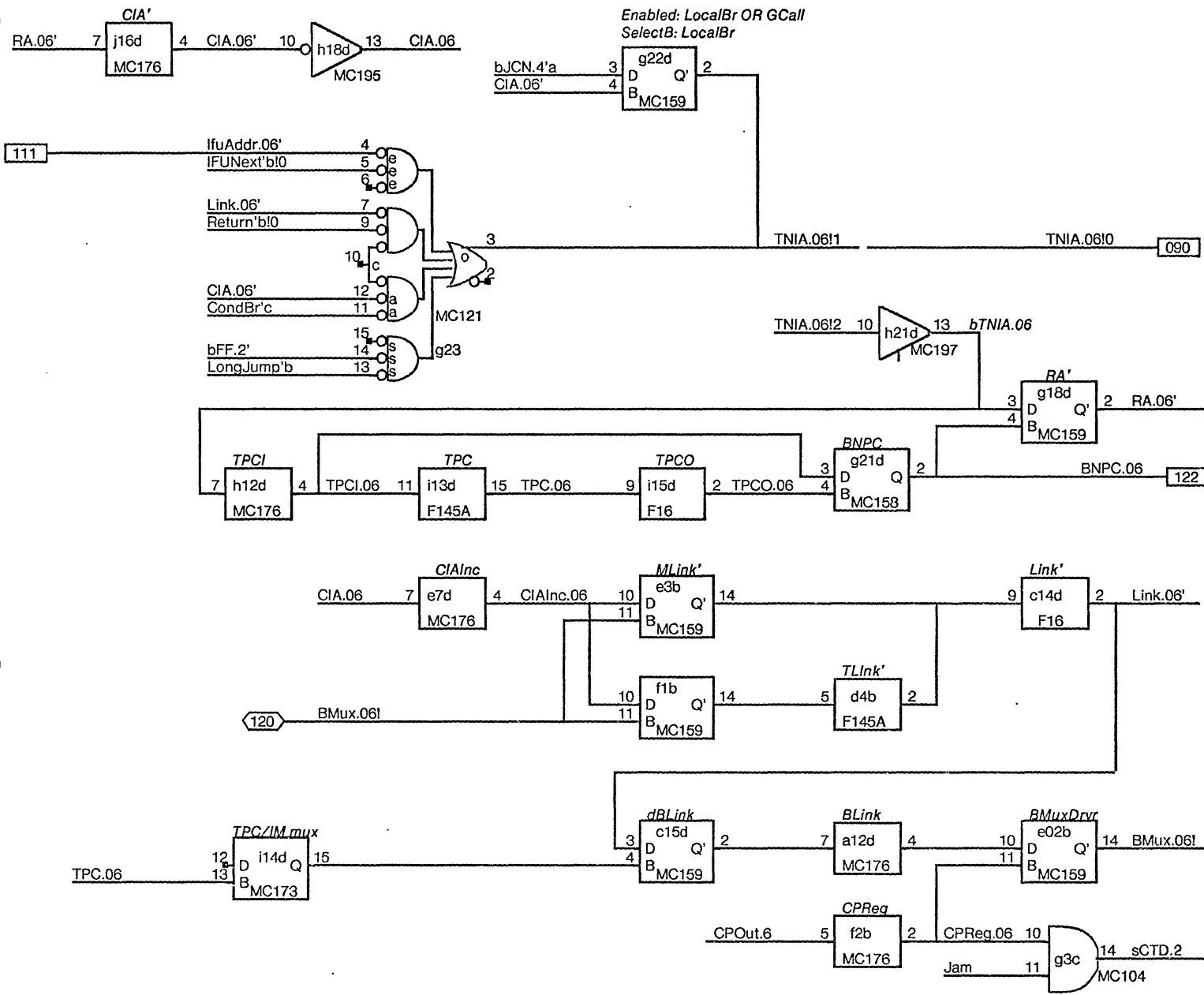


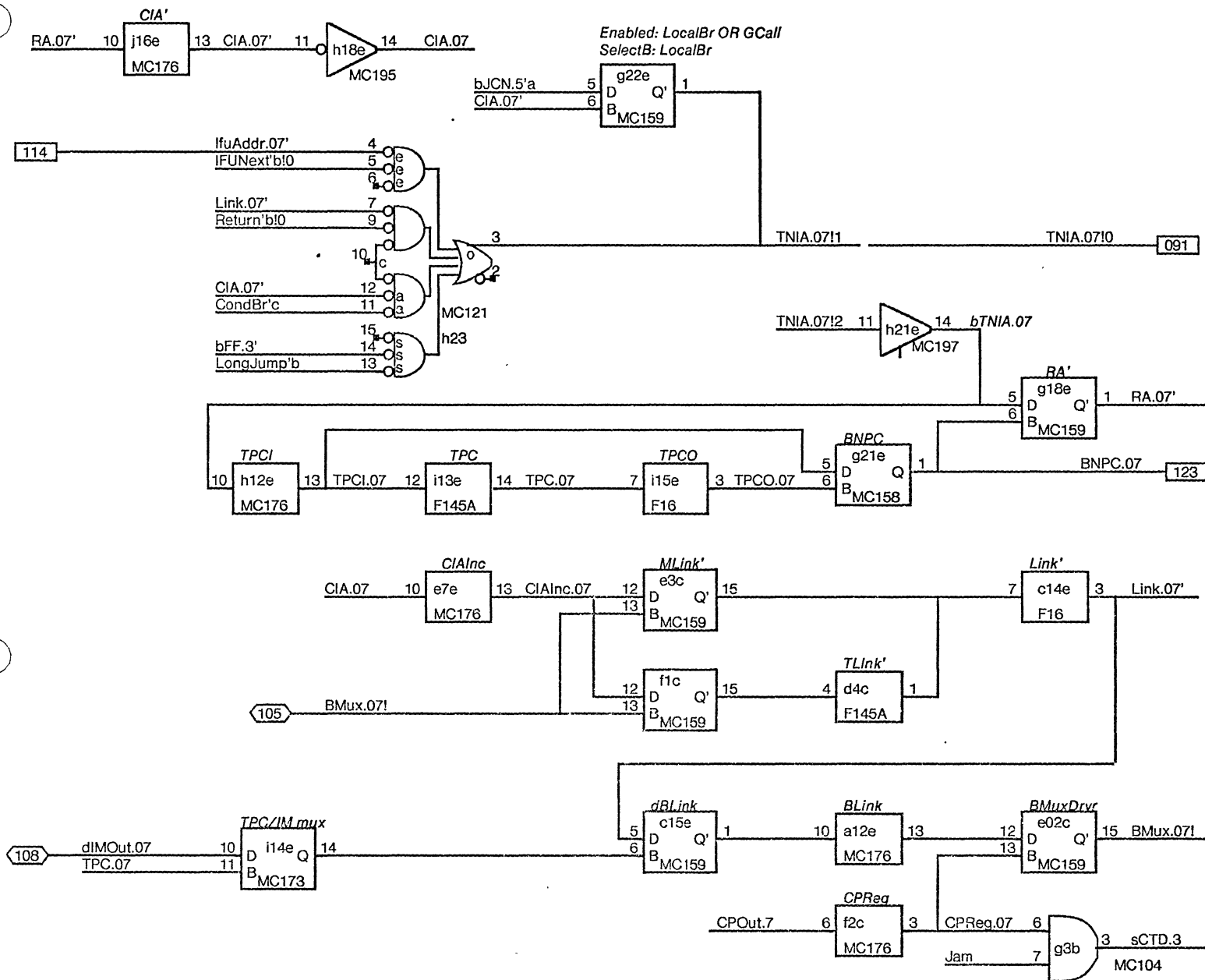


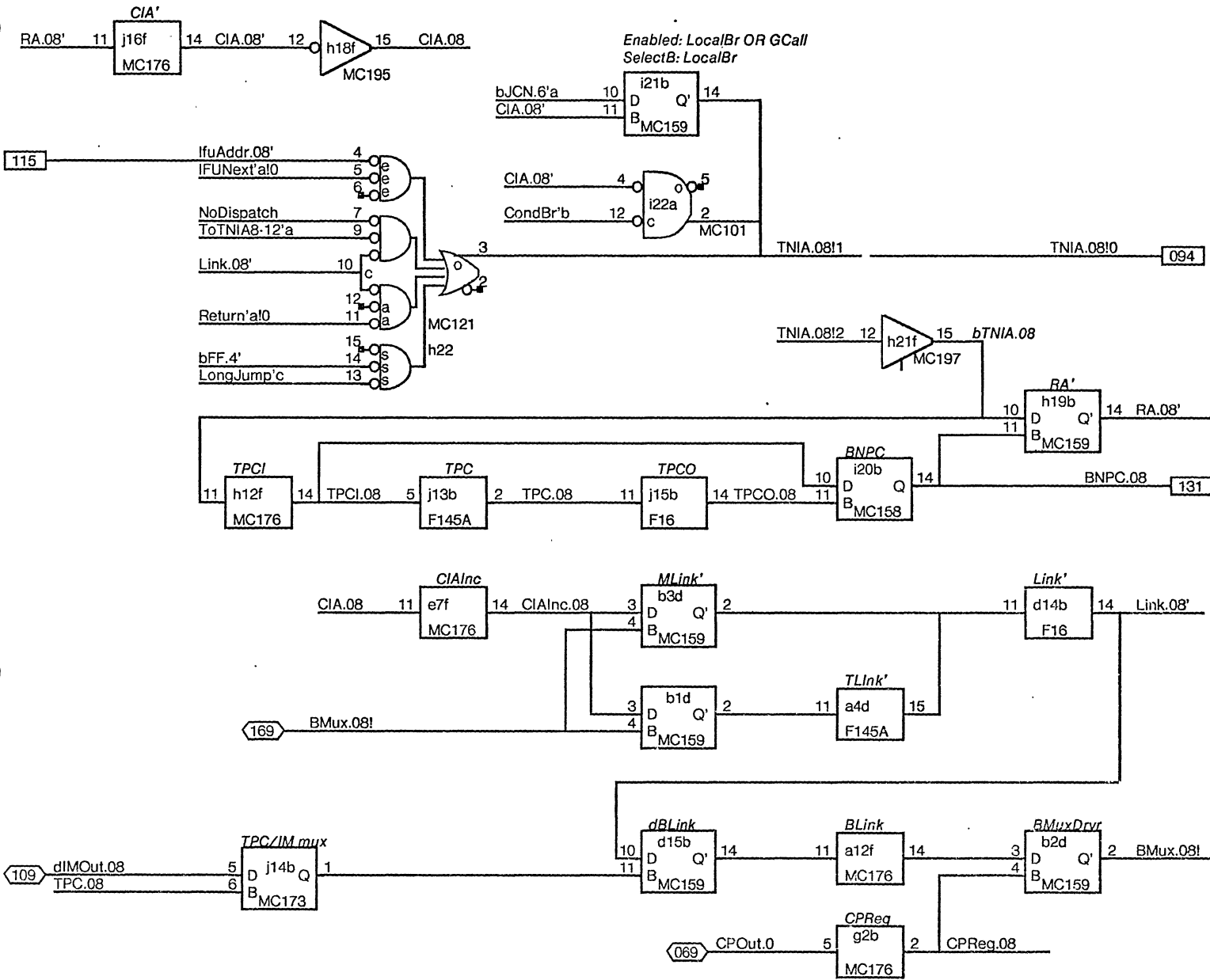


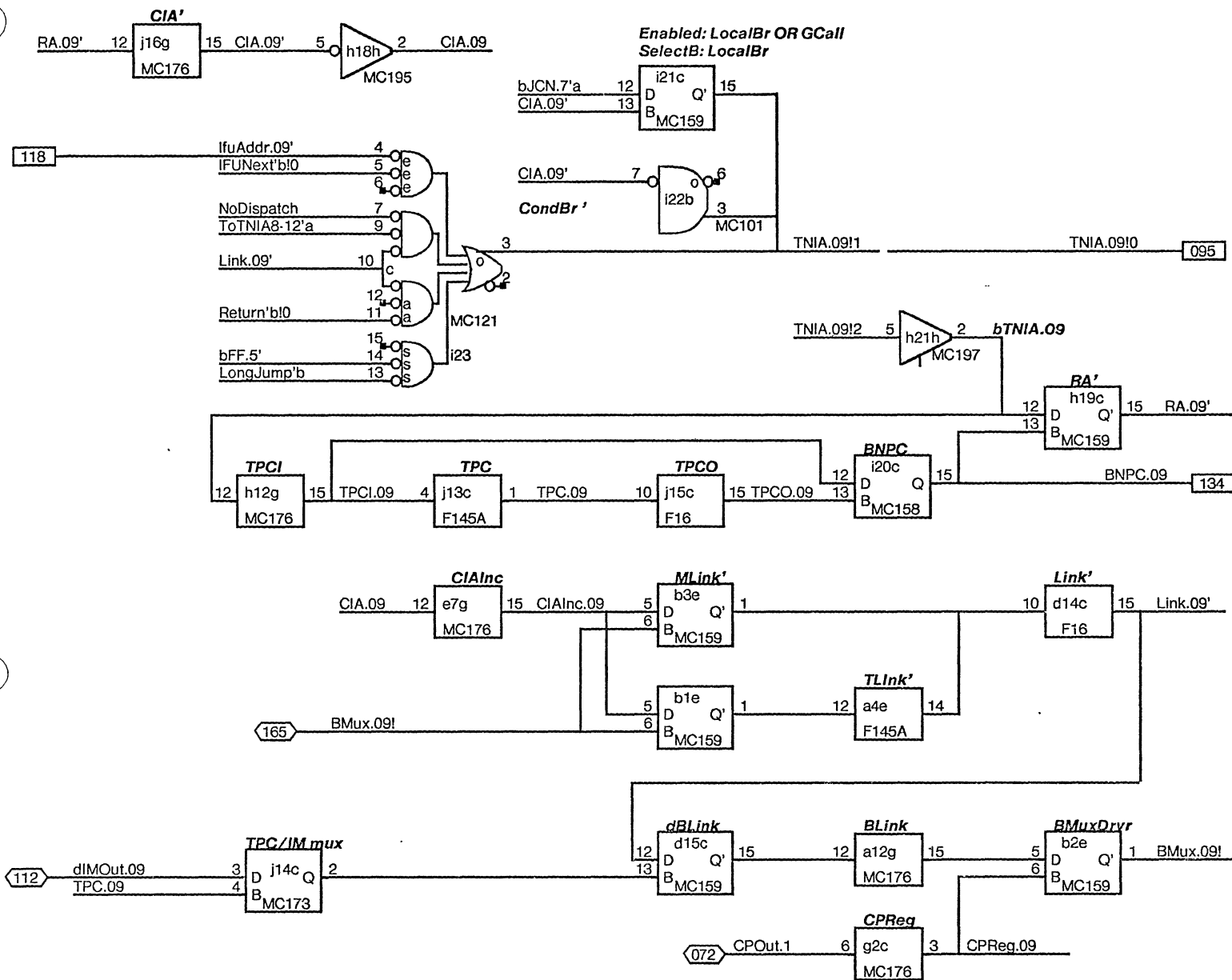


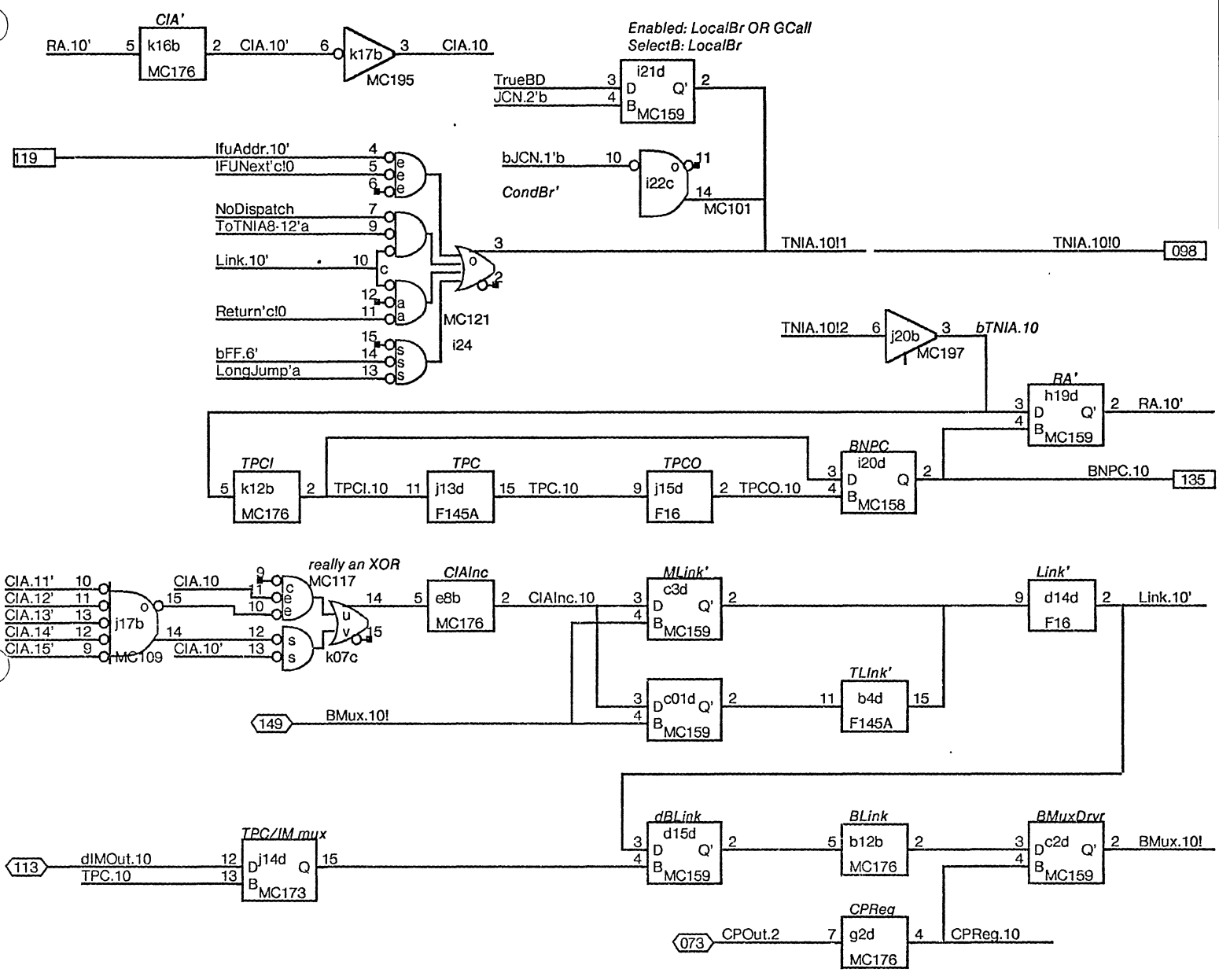


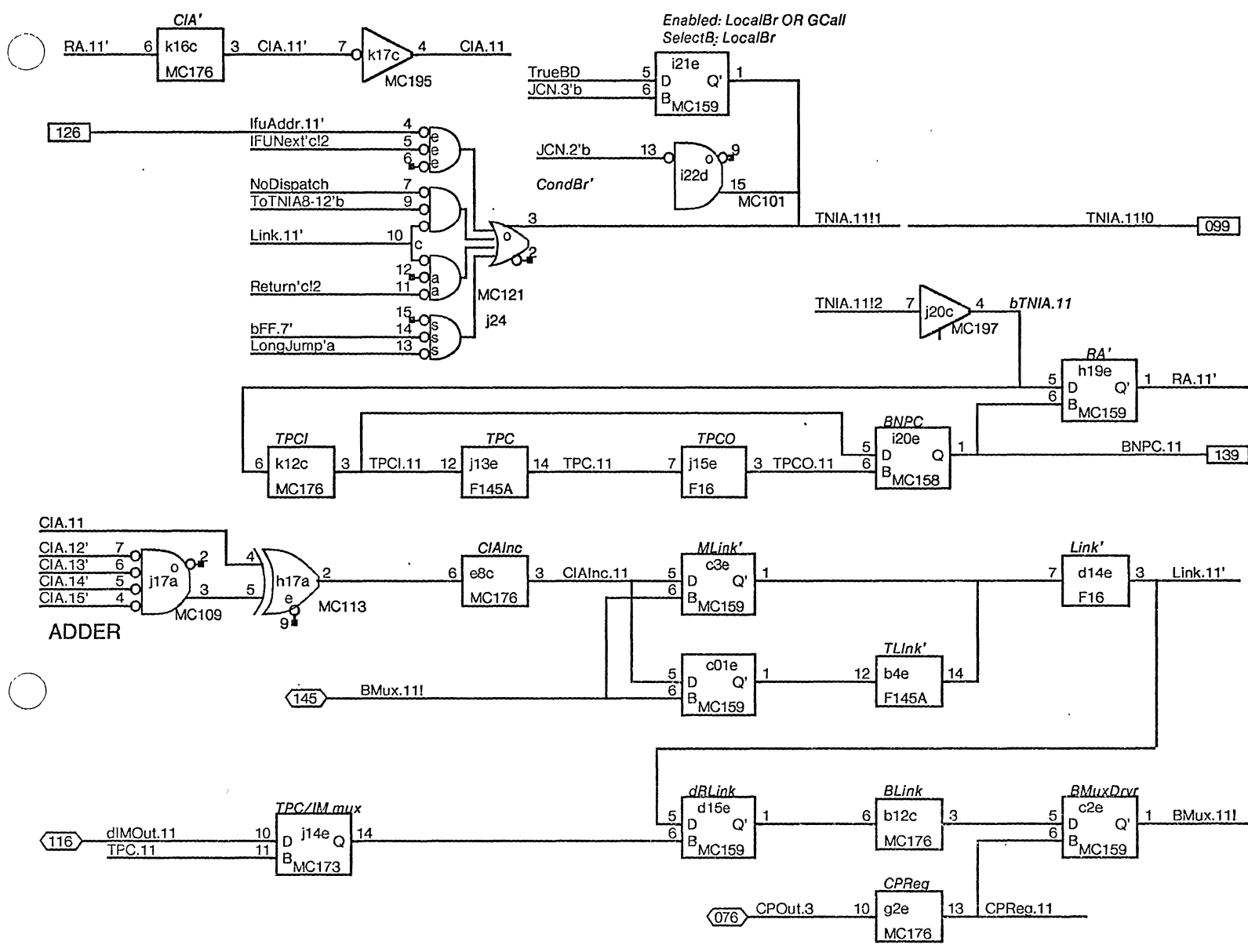


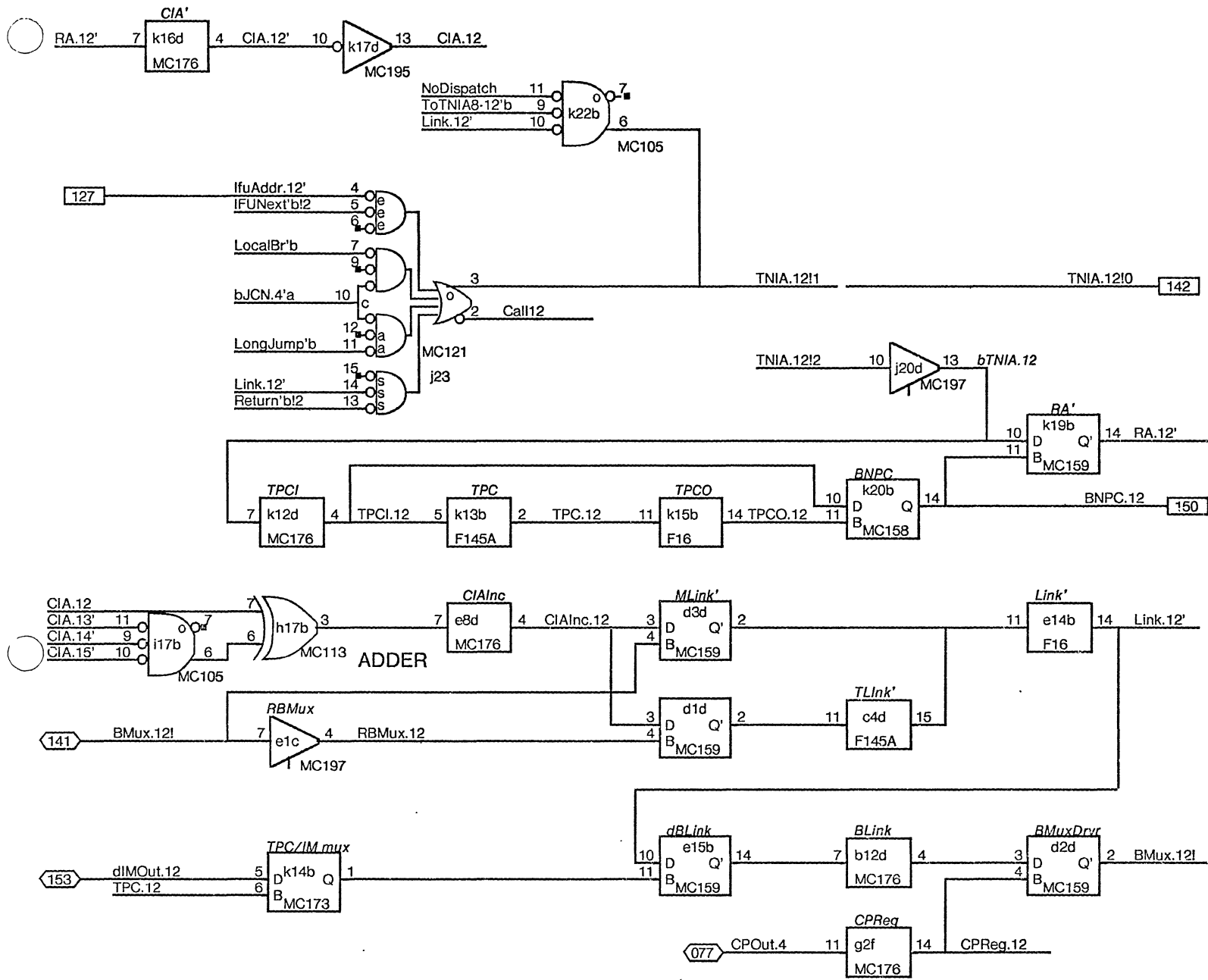


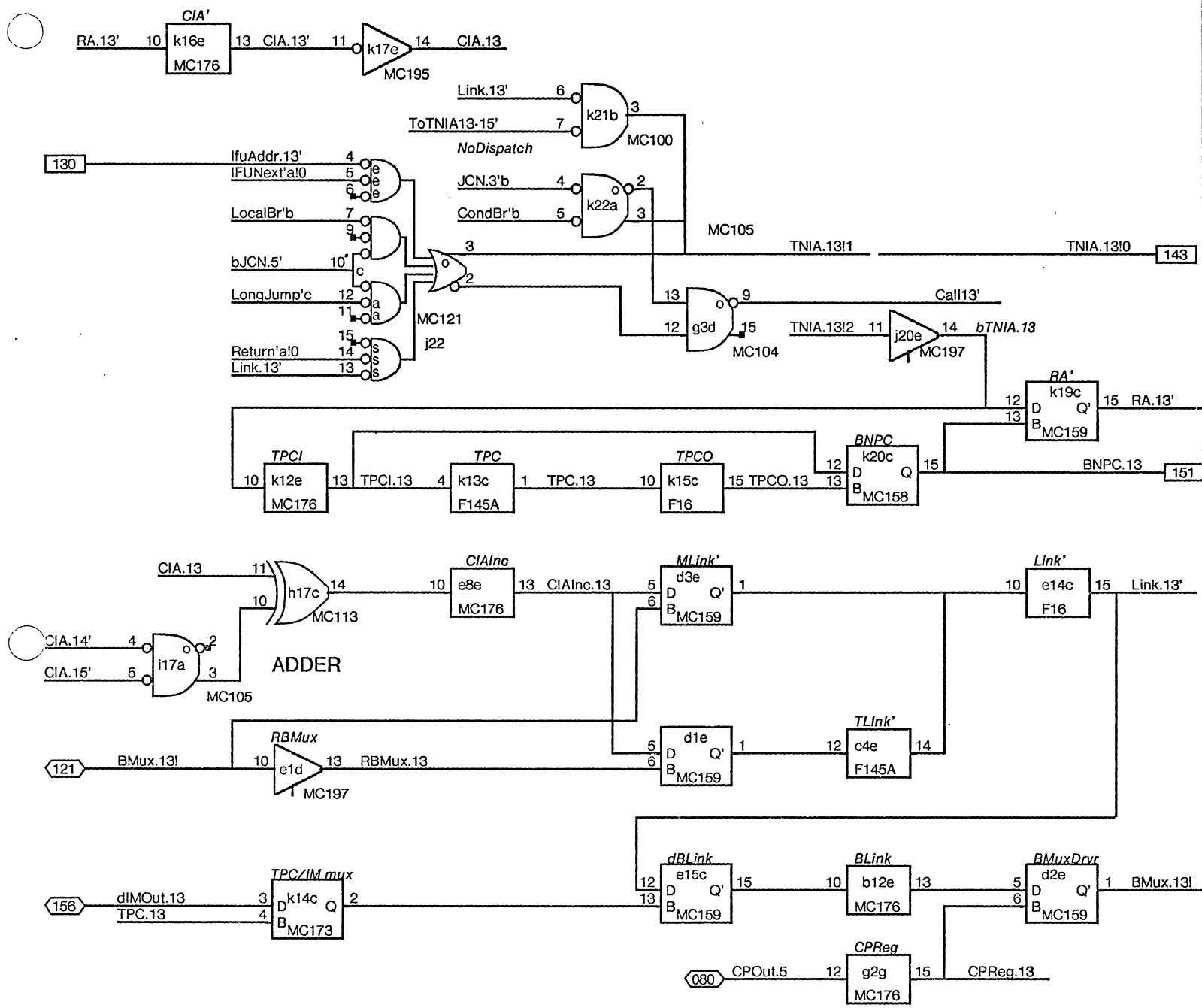


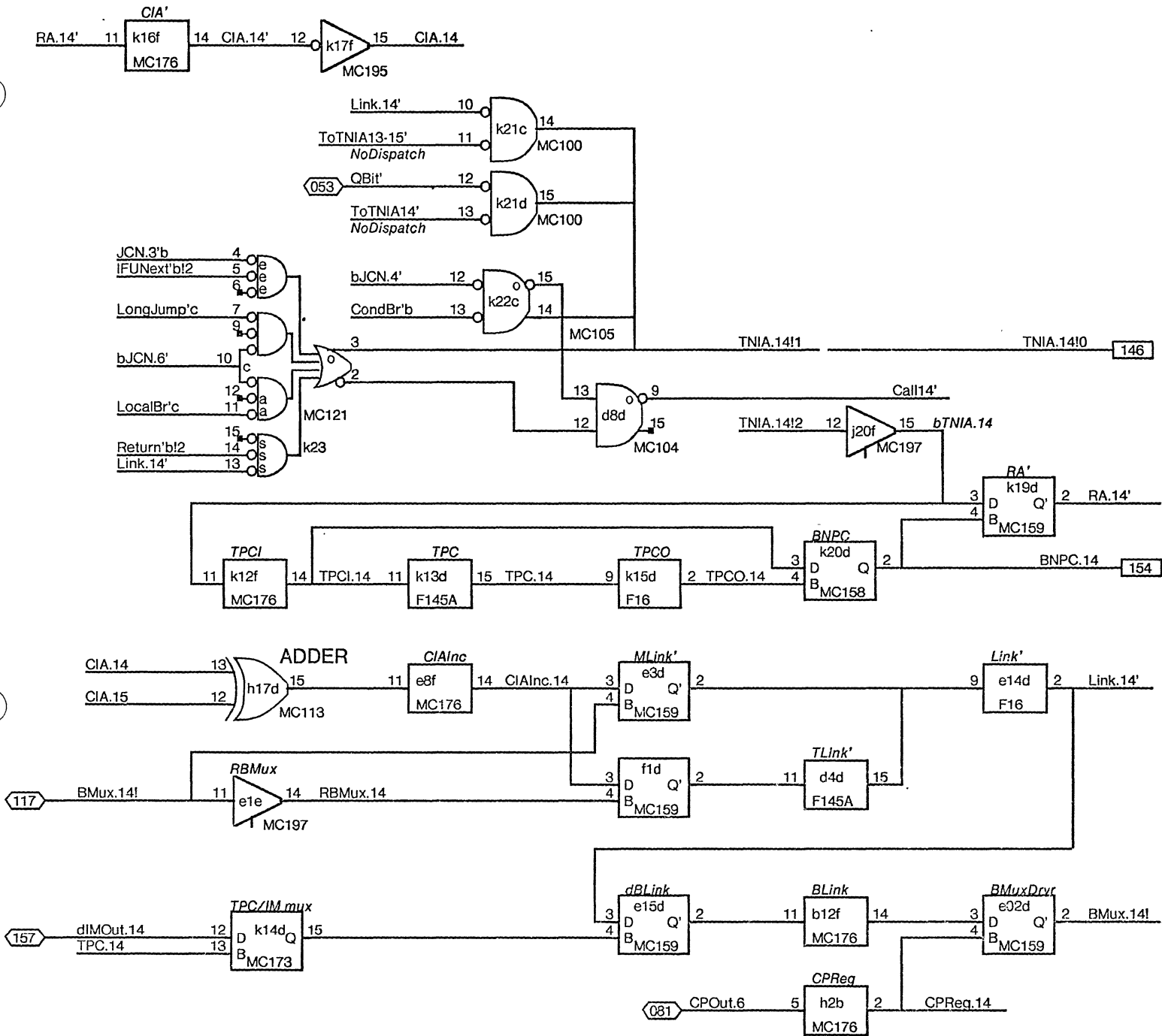


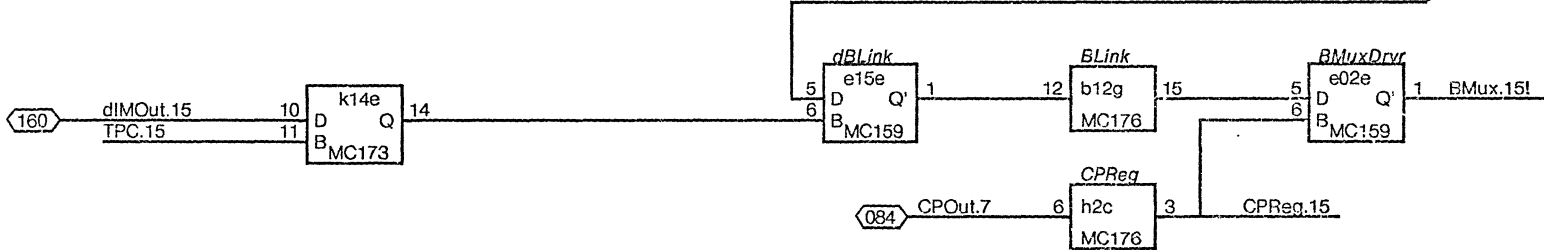
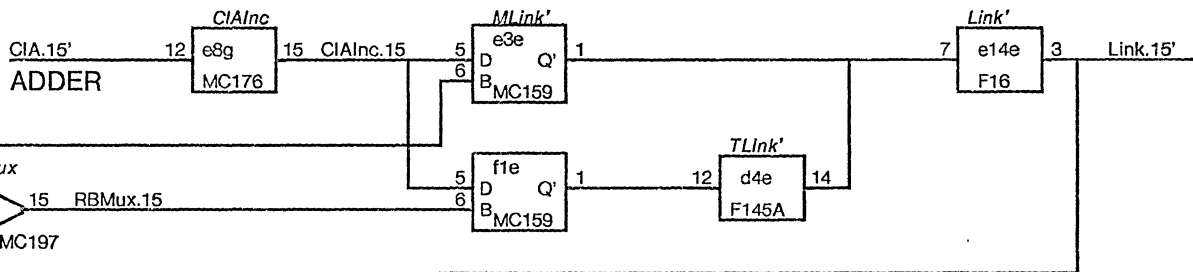
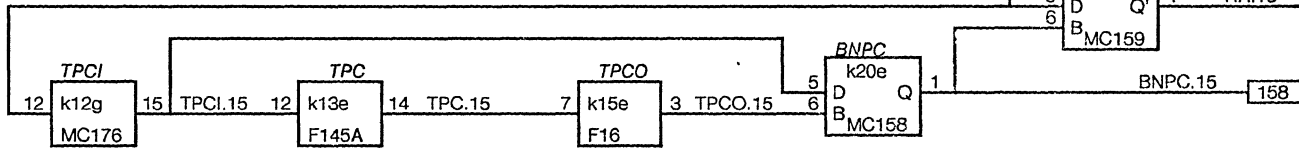
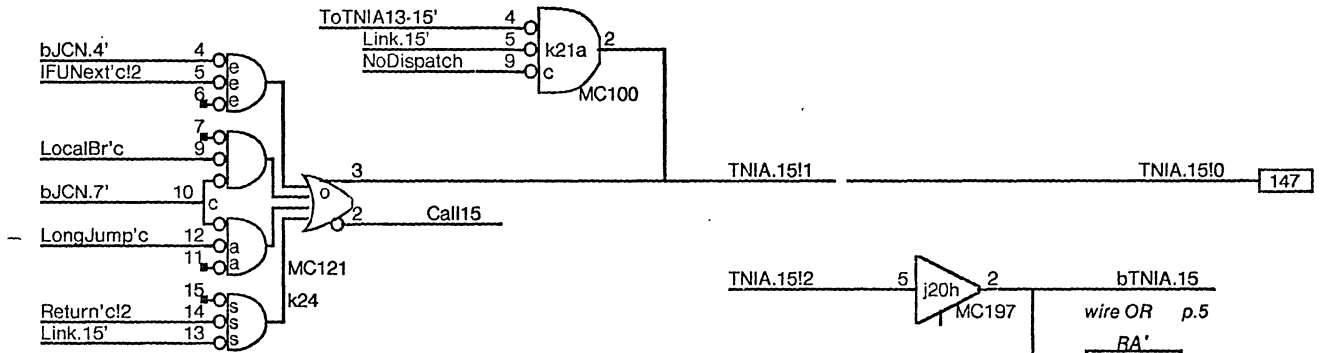
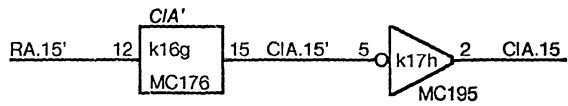


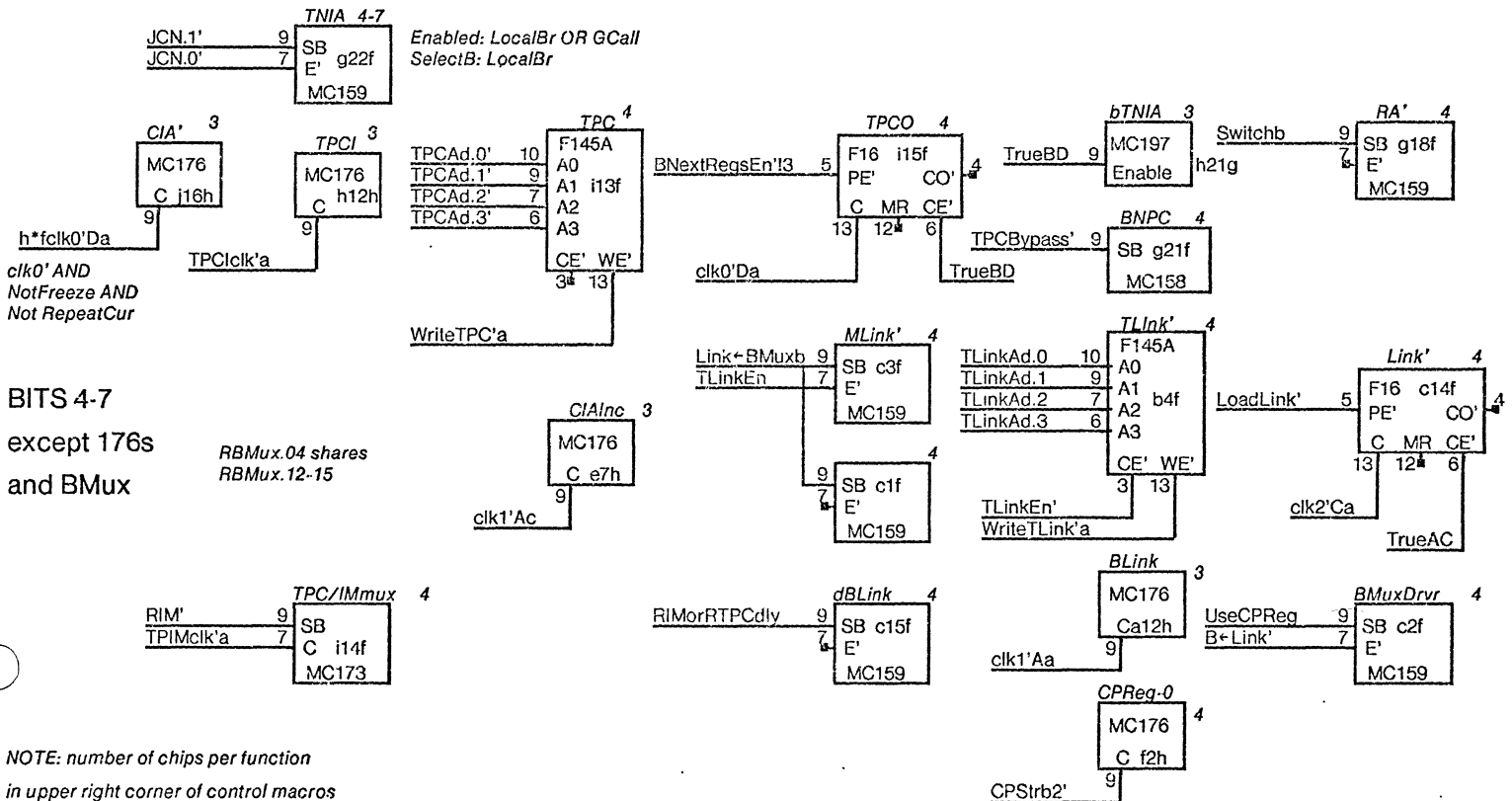
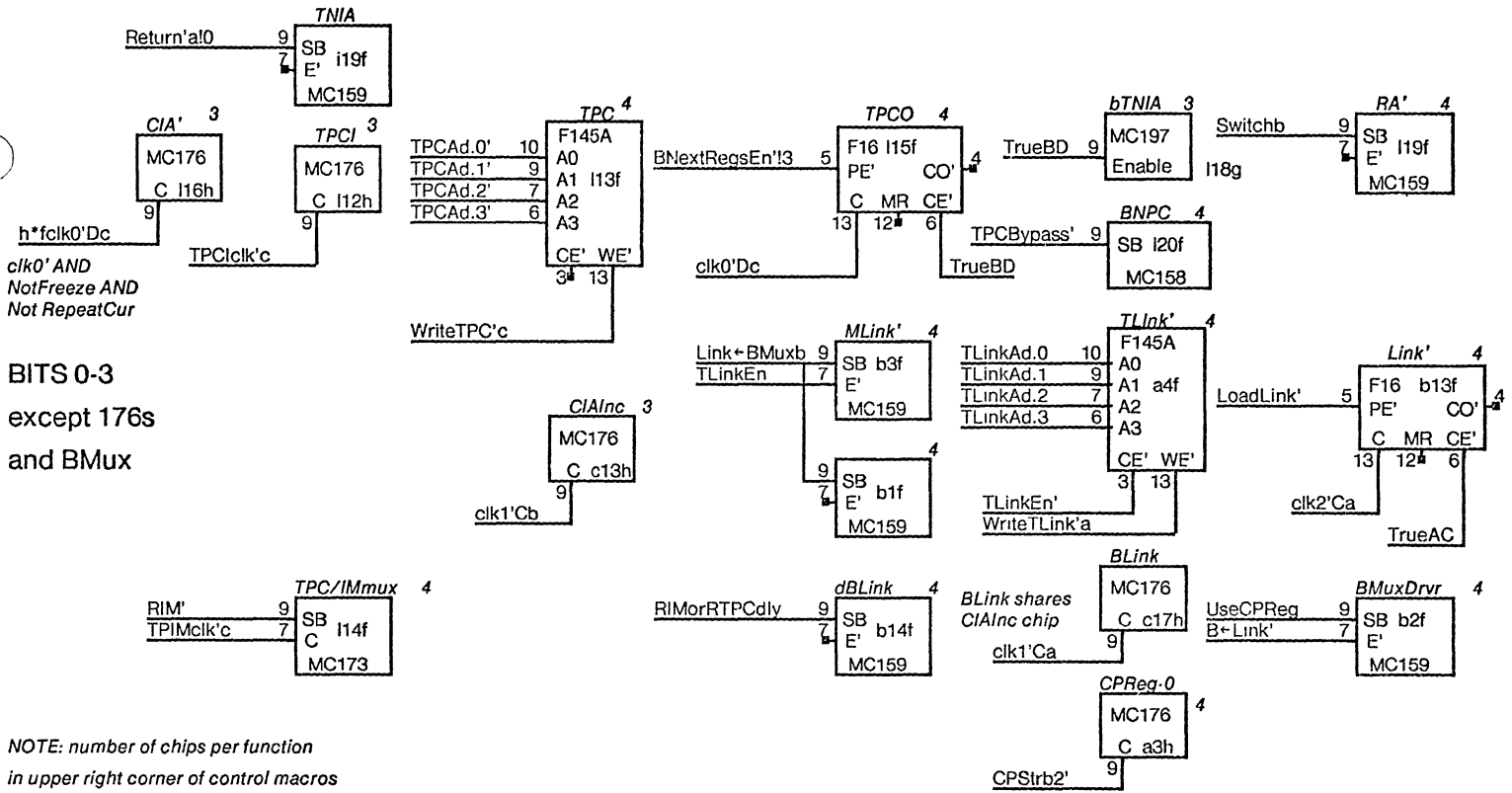




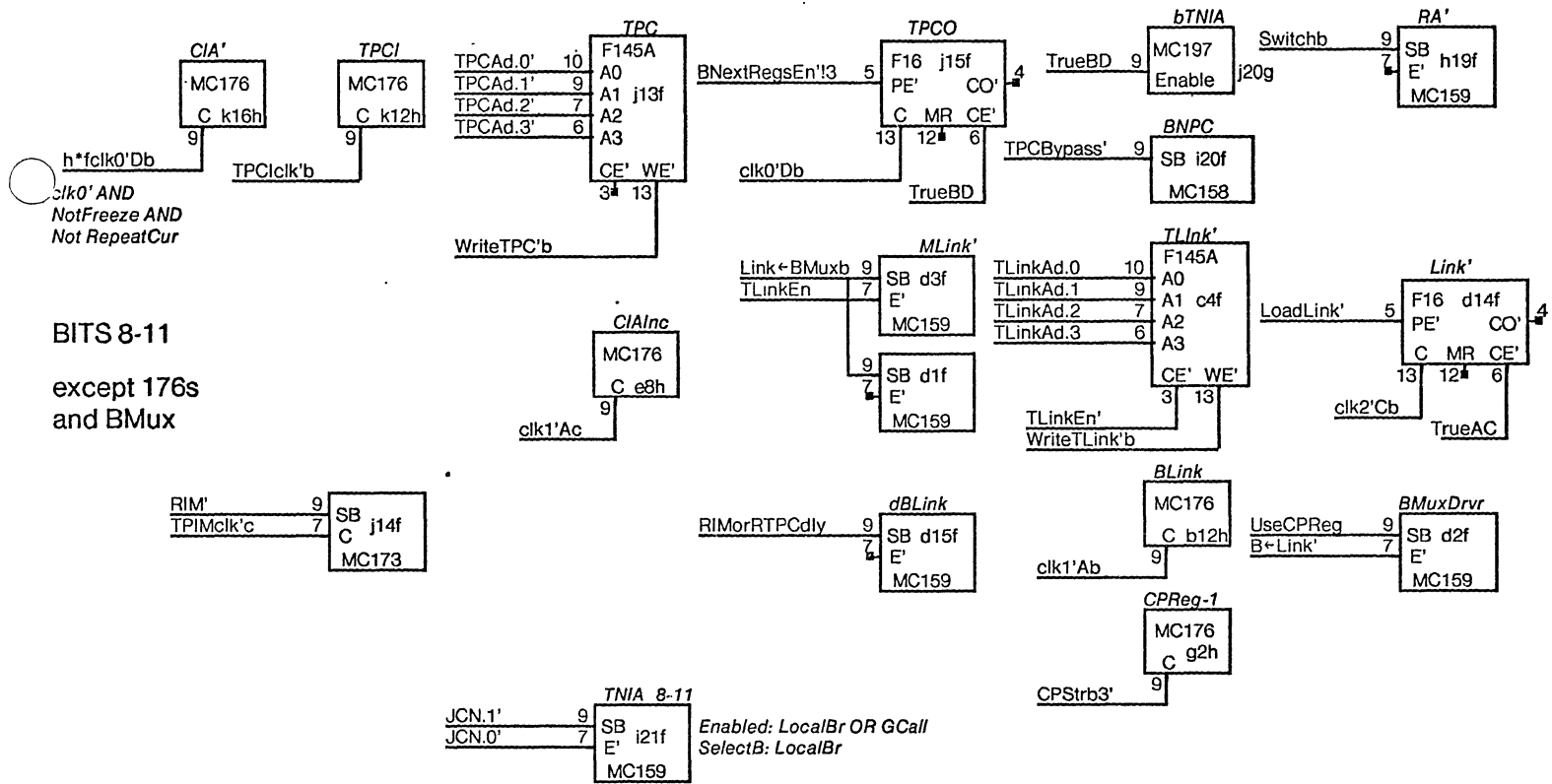




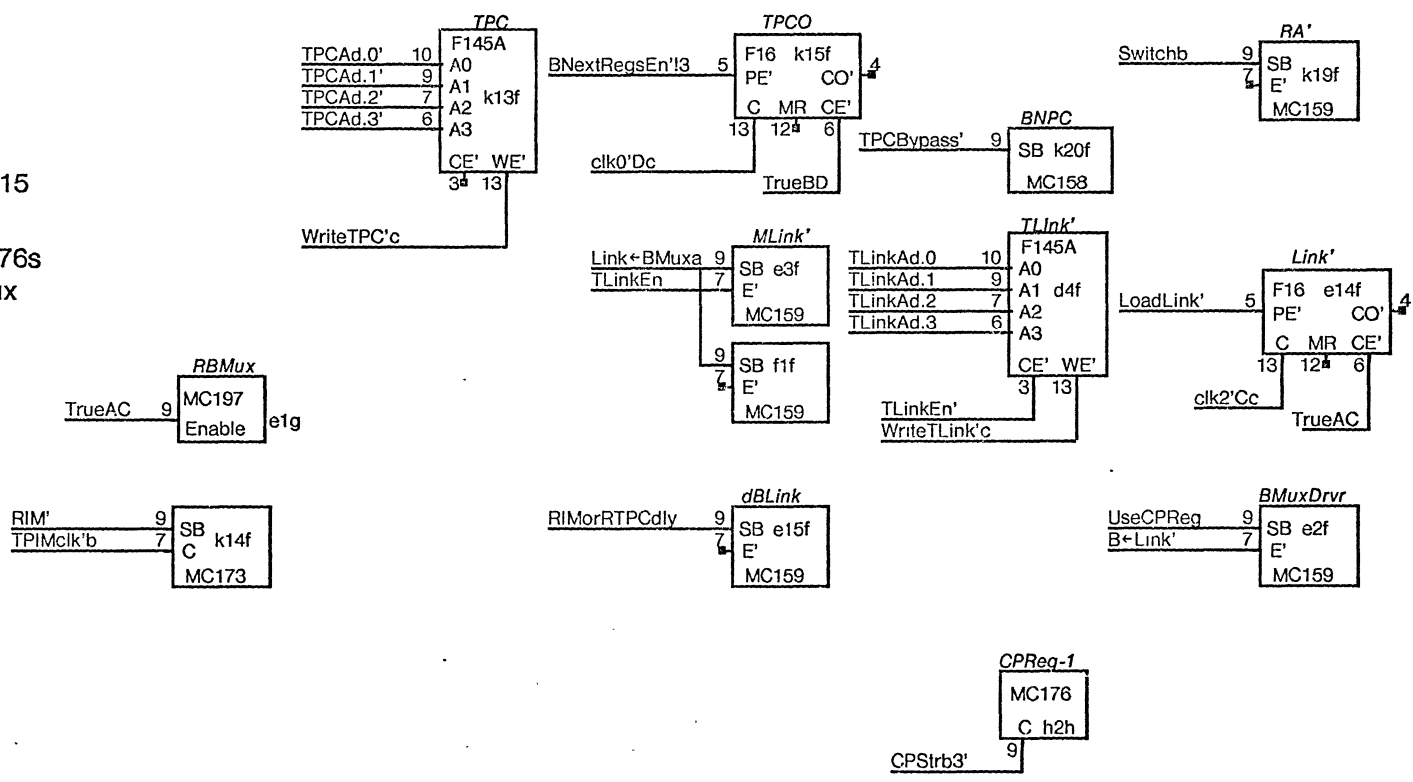




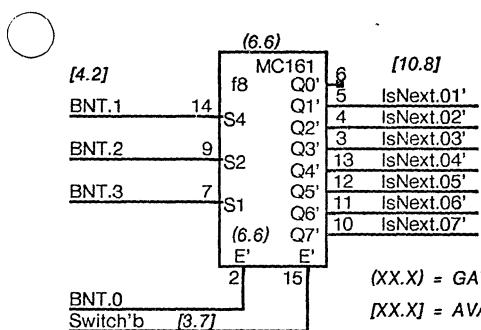
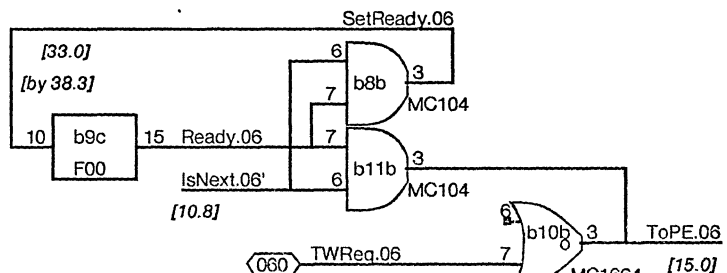
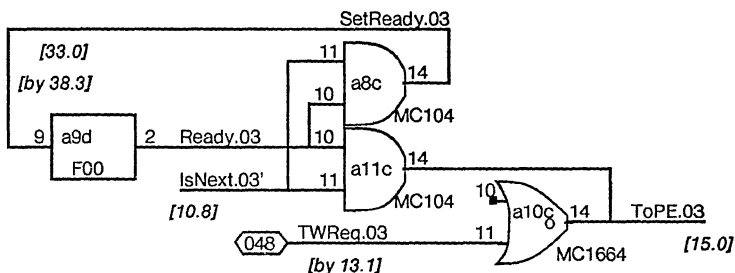
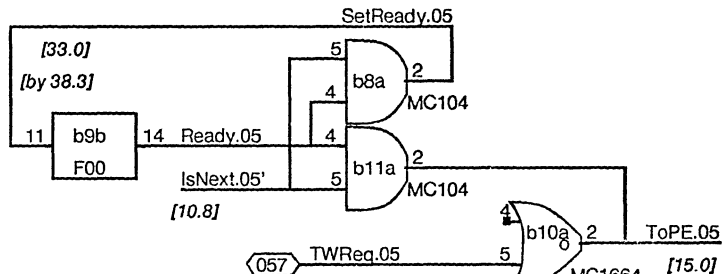
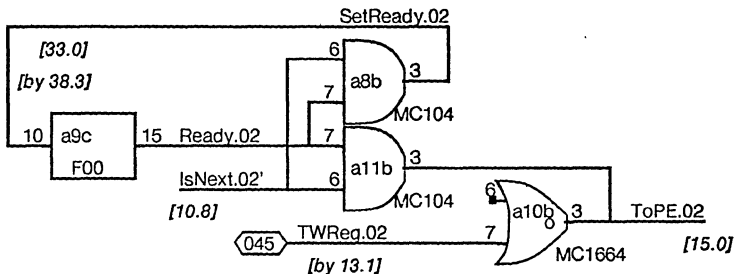
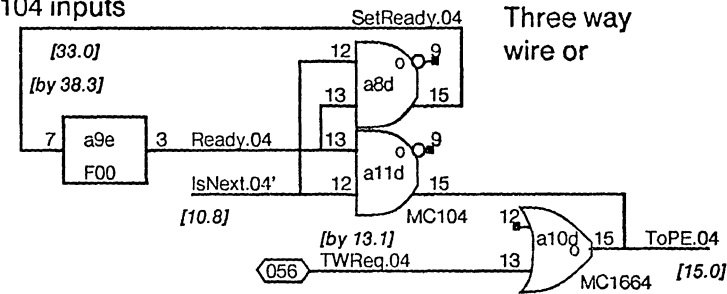
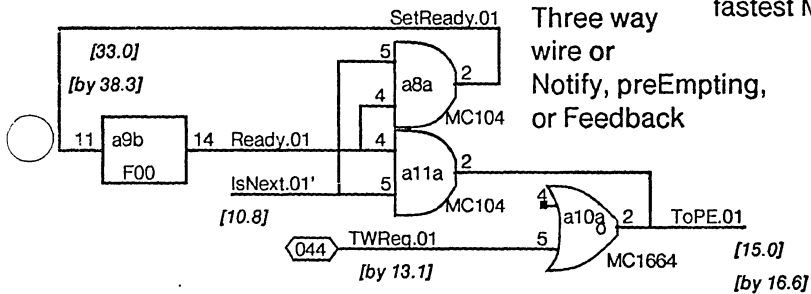
XEROX	Project	Control Section	File	Designer	Rev	Date	Page
PARC	Dorado	Data Paths	ContA20.sil	Pier	Cd	7/13/79	20



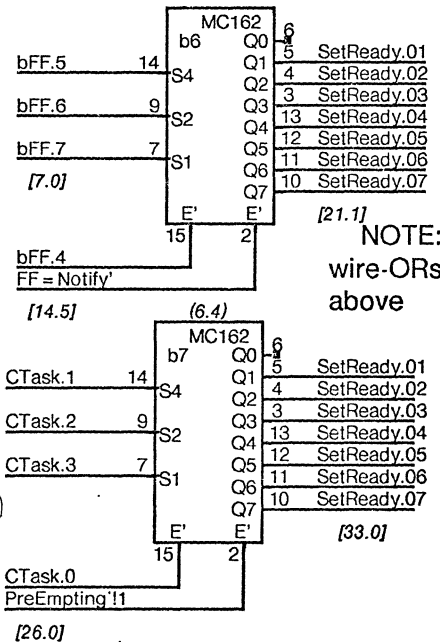
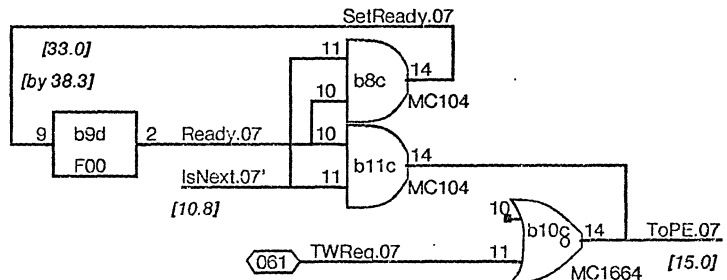
BITS 12-15
except 176s
and BMux



Note: choose IsNext' into fastest MC104 inputs



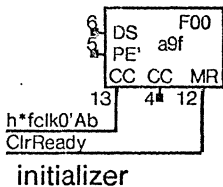
These Can Lie !!



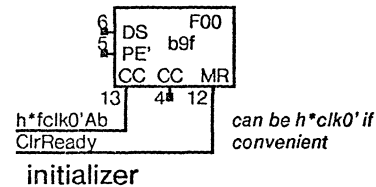
NOTE:
wire-ORs
above

NOTE !!!
Model0 Notify
uses inverted
FFs. These are
uninverted, e.g.
FF = 361b is
Notify[1]

Prevent loading
when IsNext lies

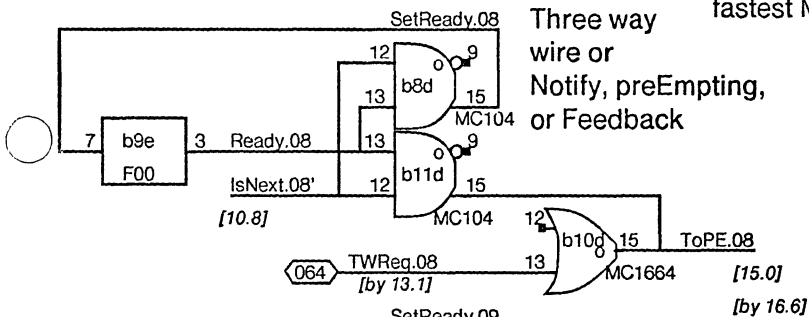


Prevent loading
when IsNext lies

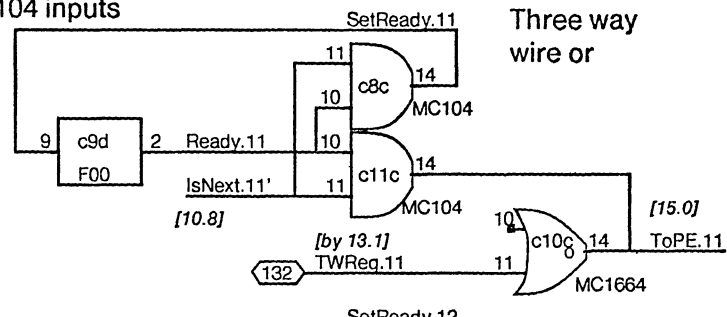


about 11 chips

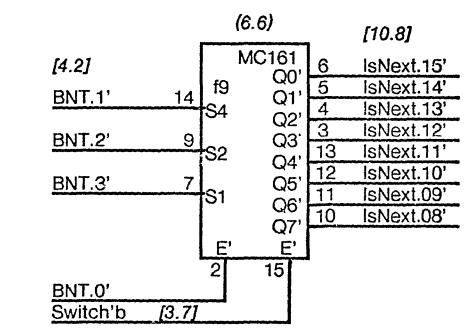
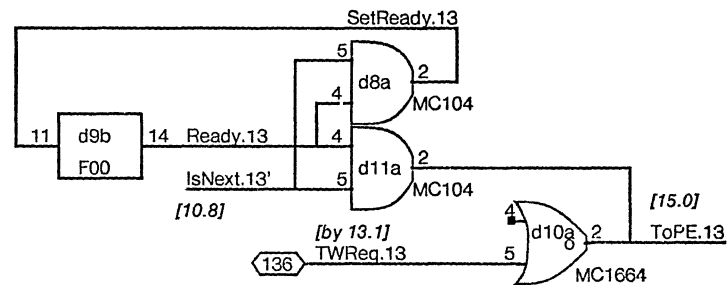
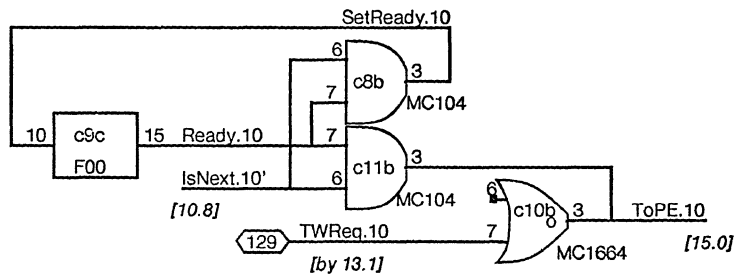
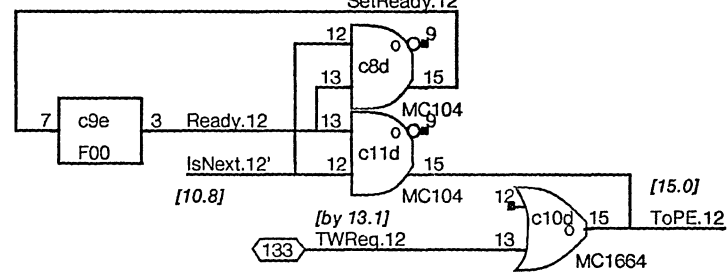
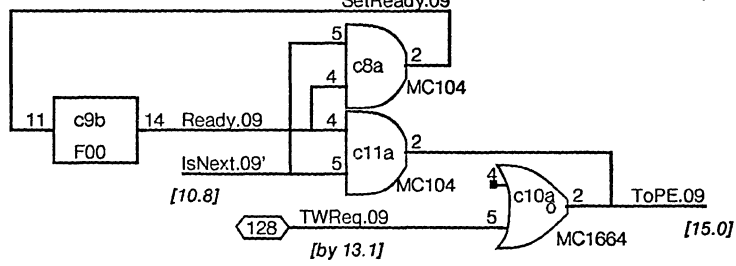
NOTE: choose IsNext' into fastest MC104 inputs



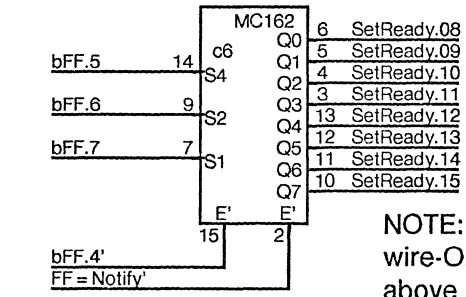
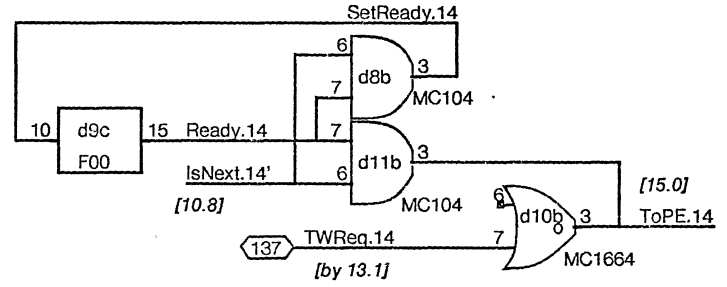
Three way wire or Notify, preEmpting, or Feedback



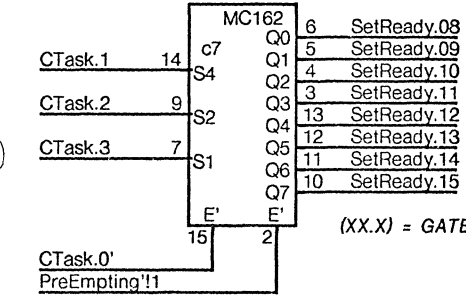
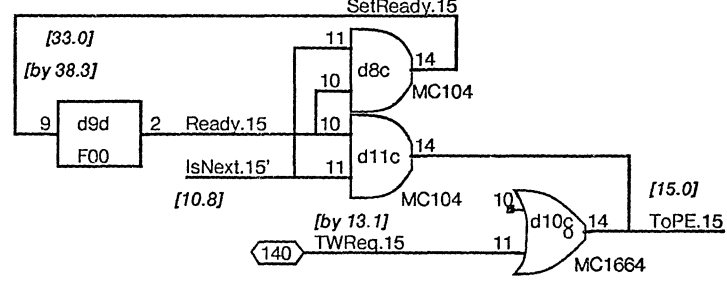
Three way wire or



These Can Lie !!



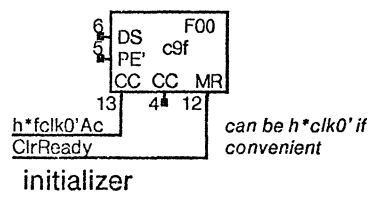
NOTE !!! Model0 Notify uses inverted FFs. These are uninverted, e.g. FF = 371b is Notify[9]



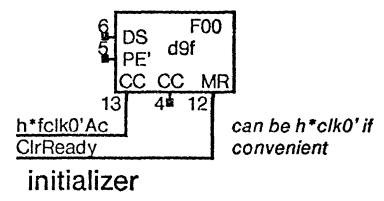
NOTE: wire-ORs above

Prevent loading when IsNext lies

Prevent loading when IsNext lies



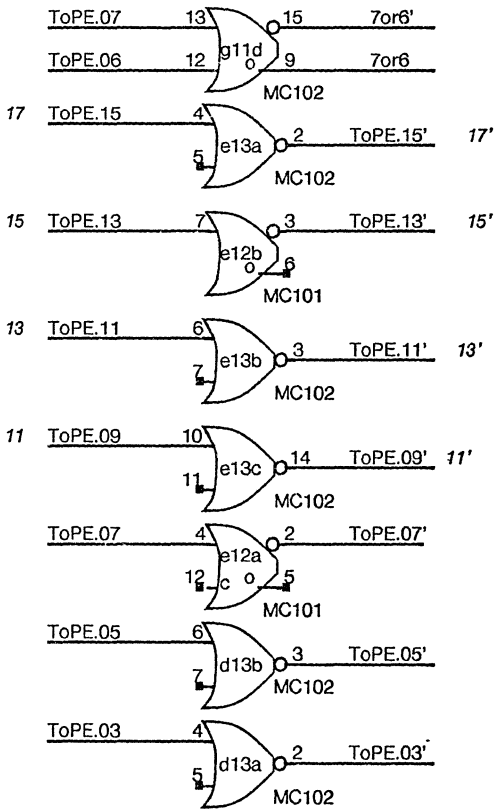
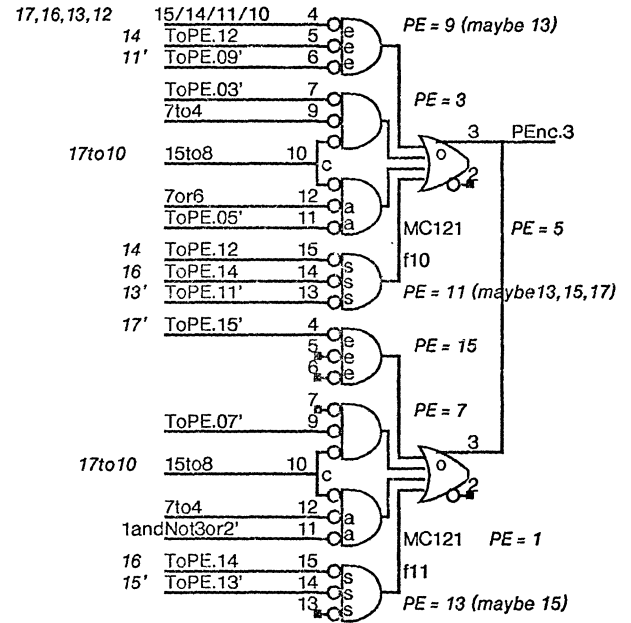
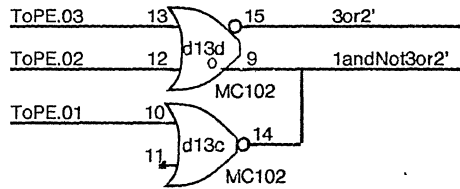
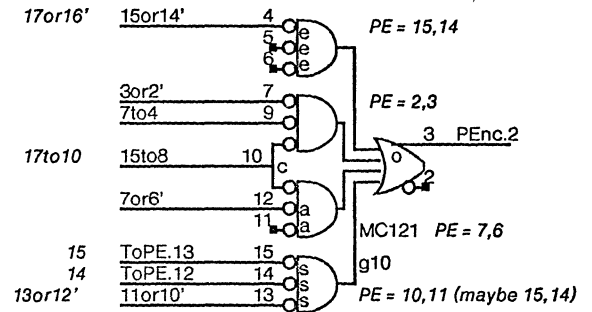
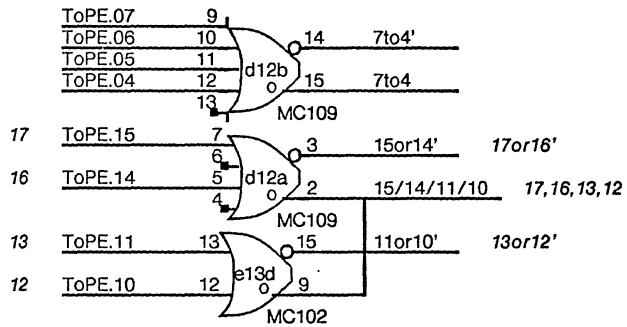
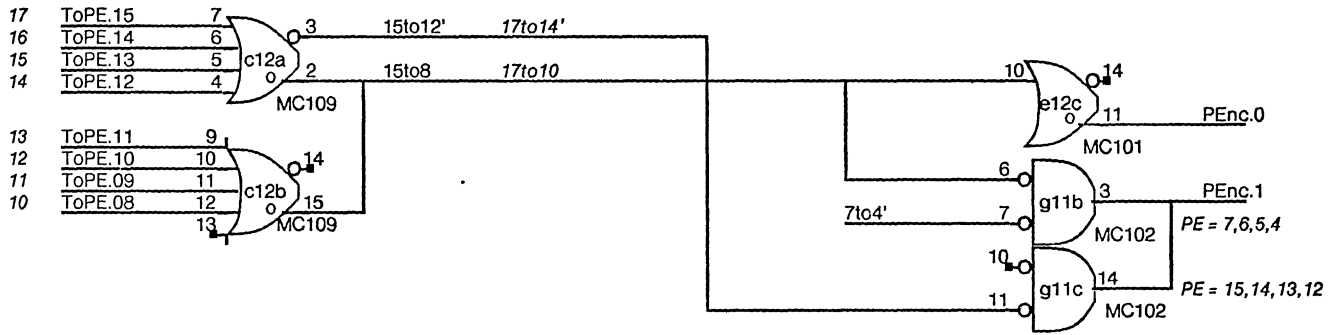
initializer



initializer

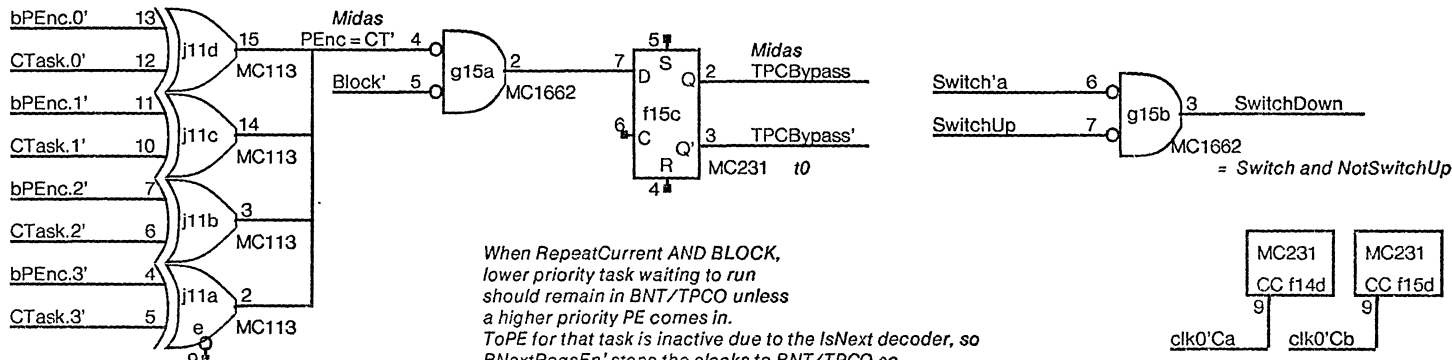
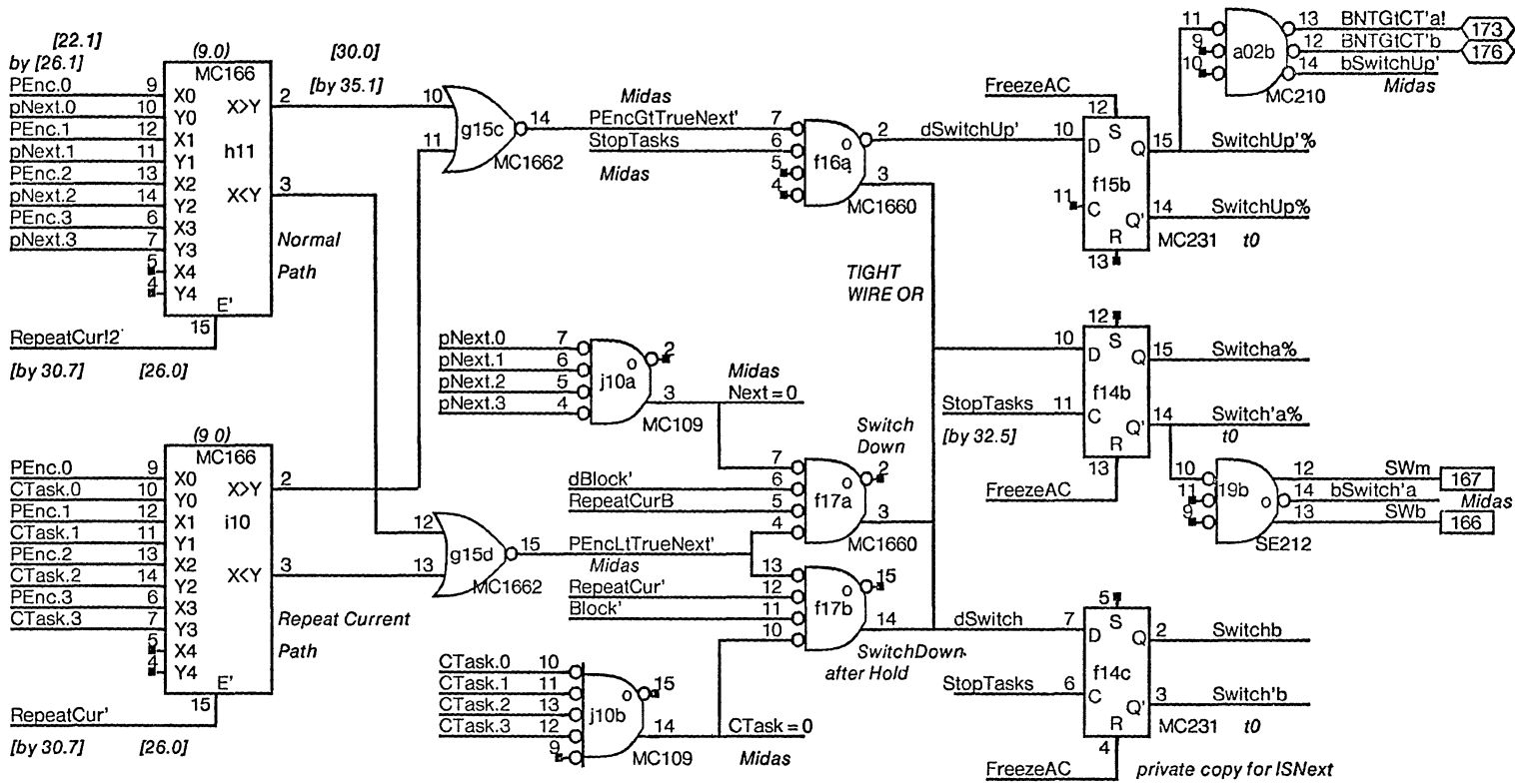
about 11 chips

REQUEST NUMBERS
IN FONT 2 ARE OCTAL

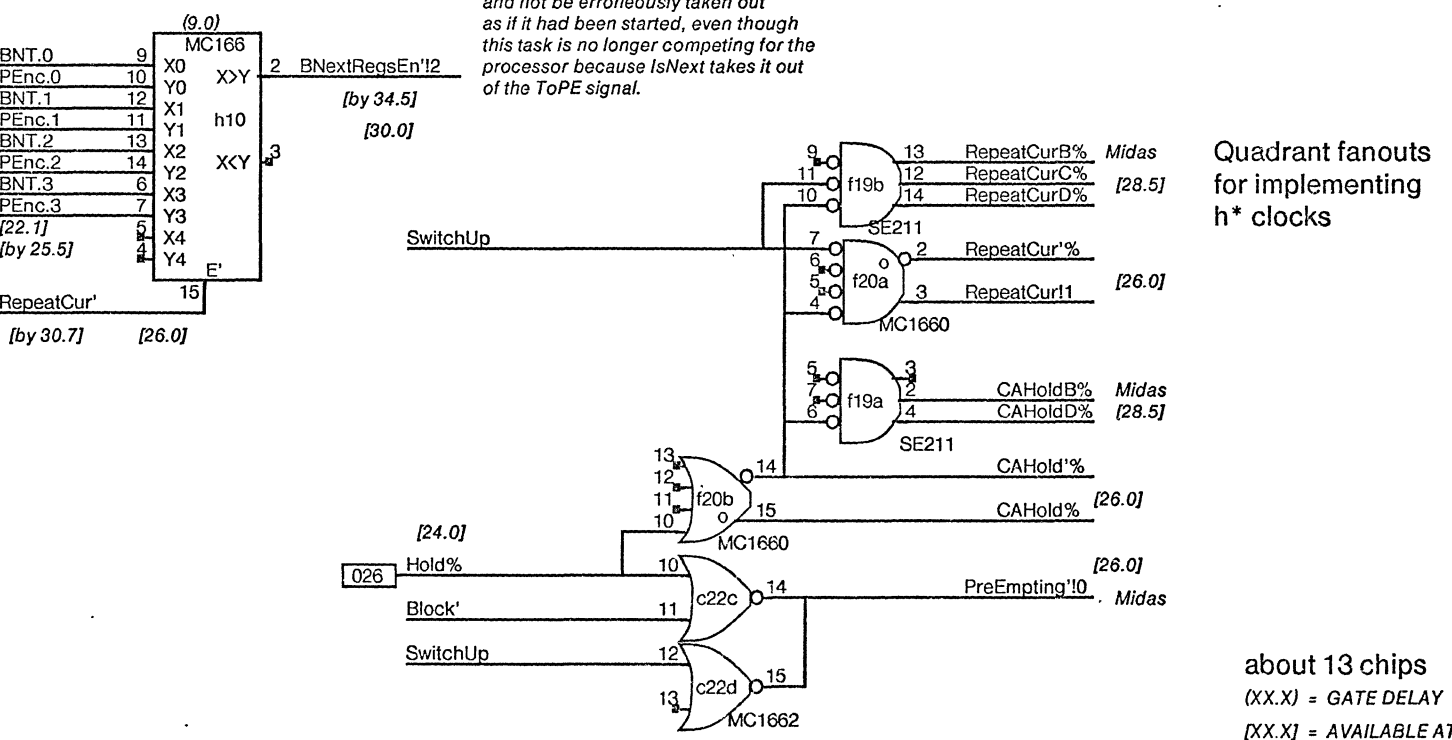


TIMING:
3.3
3.8
7.1 + wire OR

3 - 121
3 - 102
2 - 109
1 - 101 could be 102
.....
9 chips

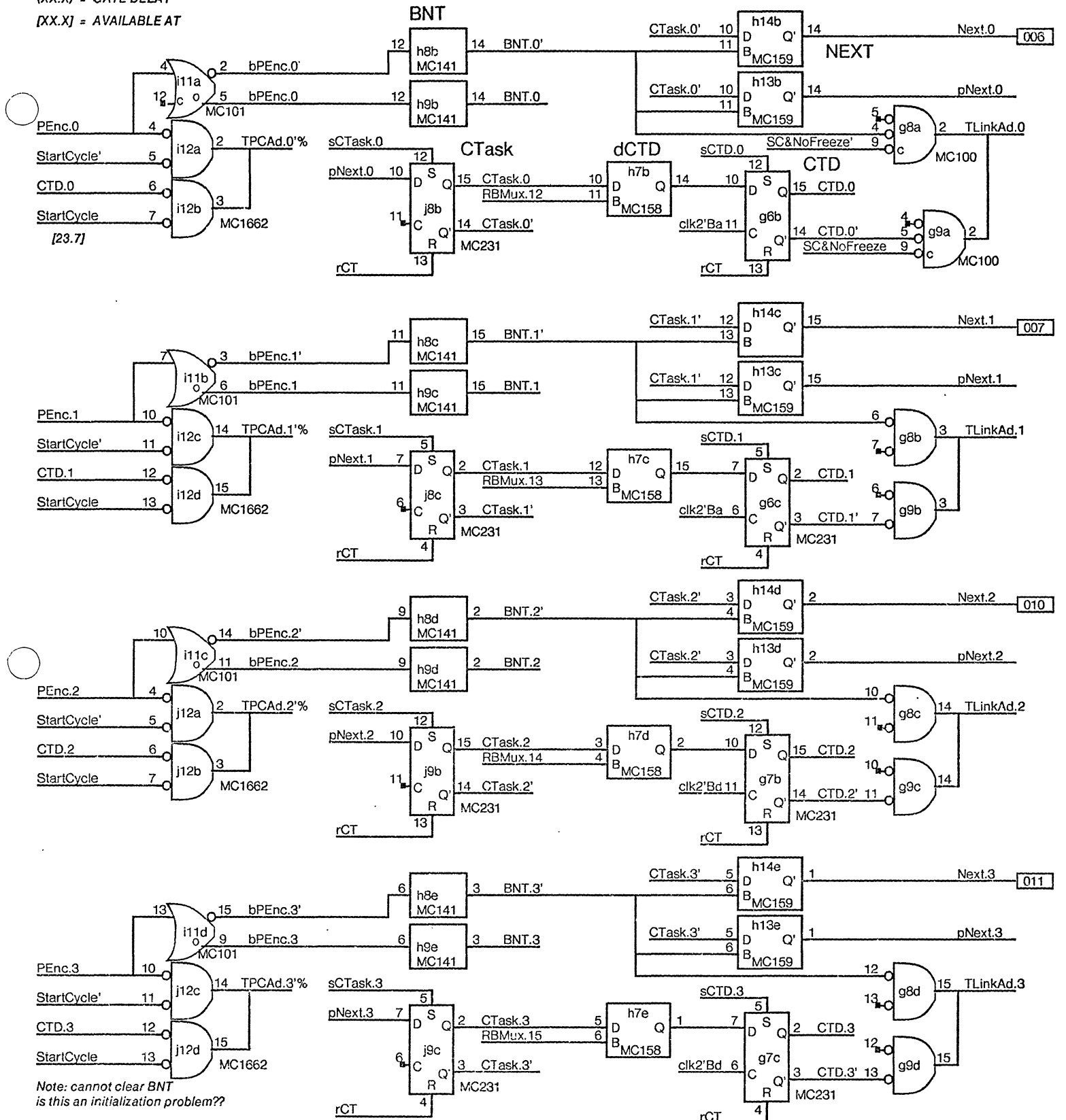


When RepeatCurrent AND BLOCK, lower priority task waiting to run should remain in BNT/TPCO unless a higher priority PE comes in. ToPE for that task is inactive due to the IsNext decoder, so BNextRegsEn' stops the clocks to BNT/TPCO so that the proper task will remain in BNT and not be erroneously taken out as if it had been started, even though this task is no longer competing for the processor because IsNext takes it out of the ToPE signal.

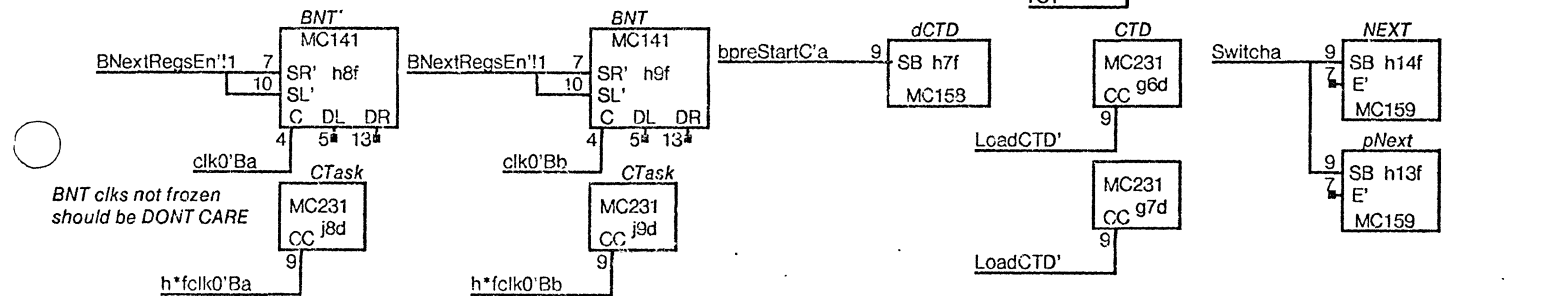


about 13 chips
 (XX.X) = GATE DELAY
 [XX.X] = AVAILABLE AT

(XX.X) = GATE DELAY
 [XX.X] = AVAILABLE AT



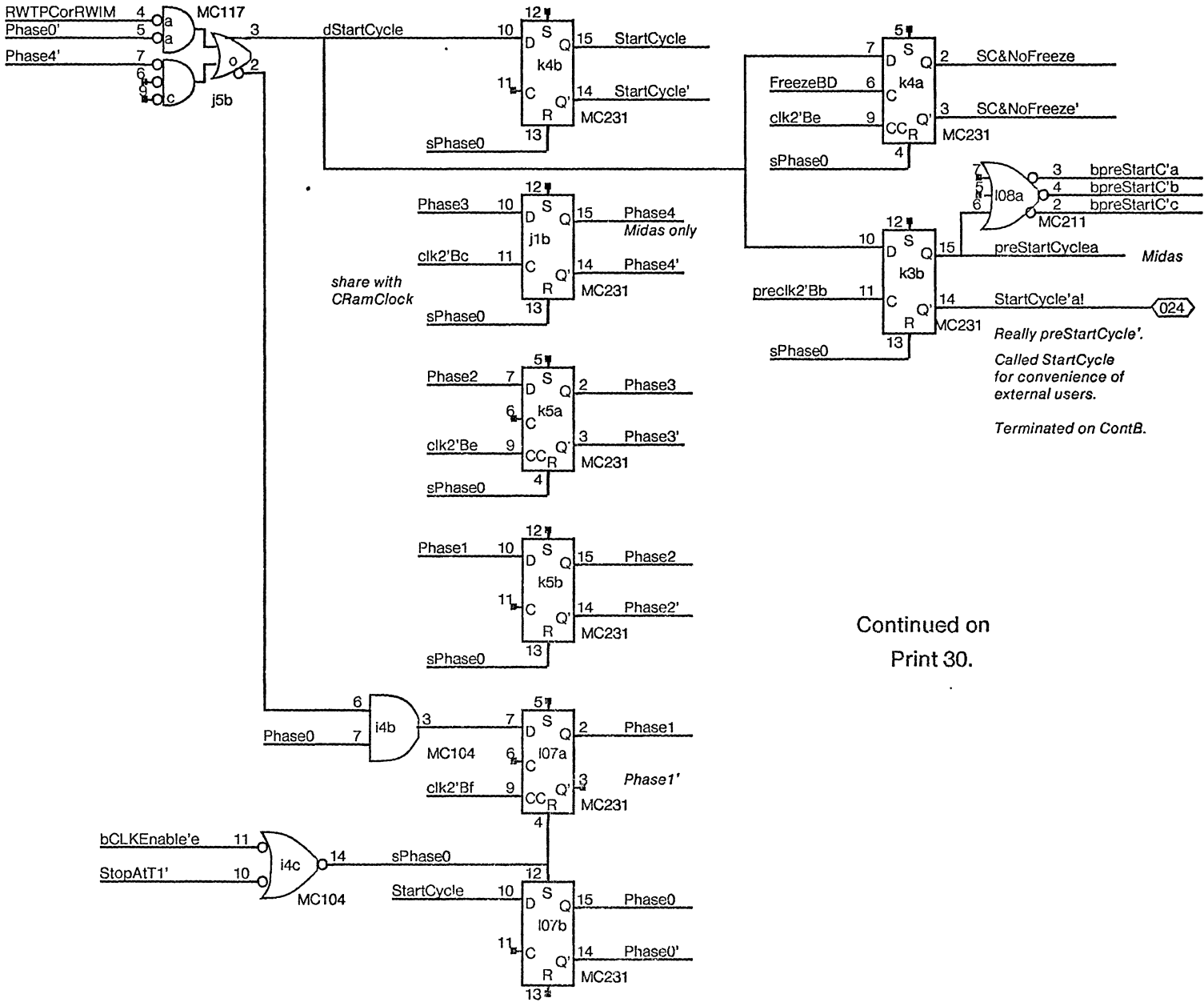
Note: cannot clear BNT
 is this an initialization problem??



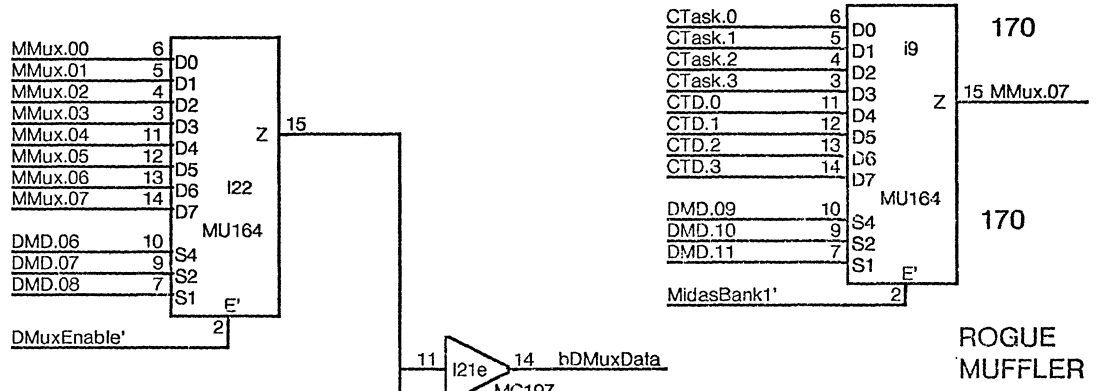
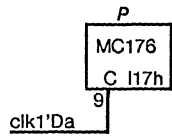
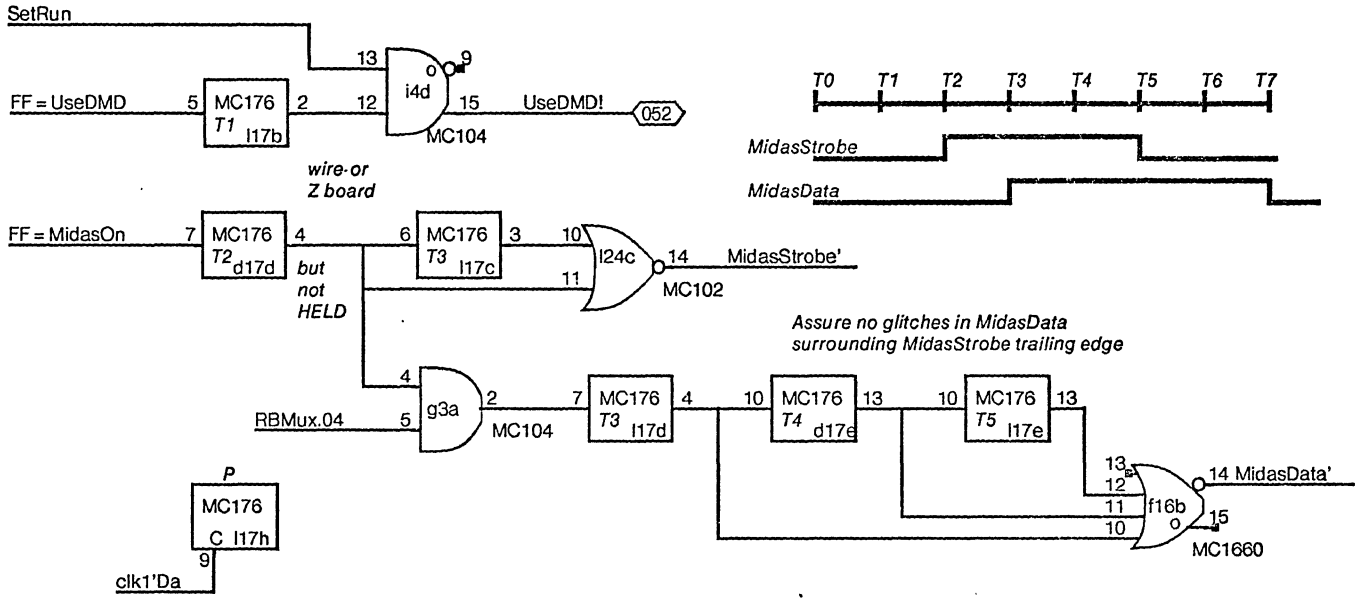
BNT clks not frozen
 should be DONT CARE

[9.8]

[by 10.9]

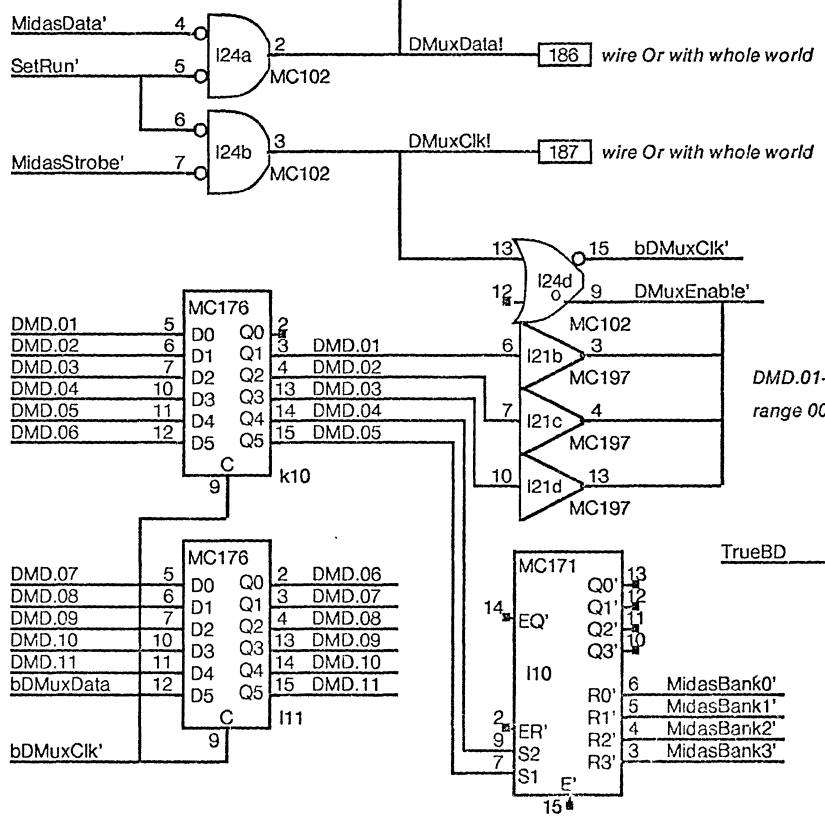


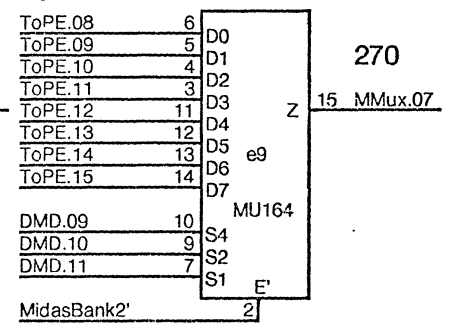
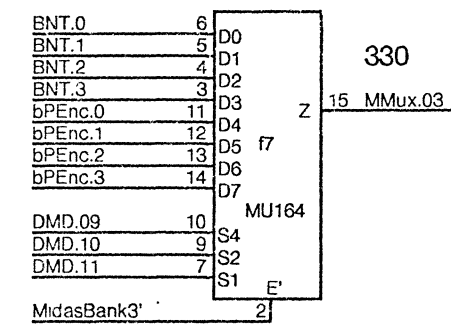
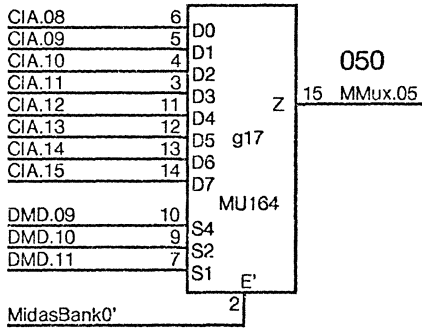
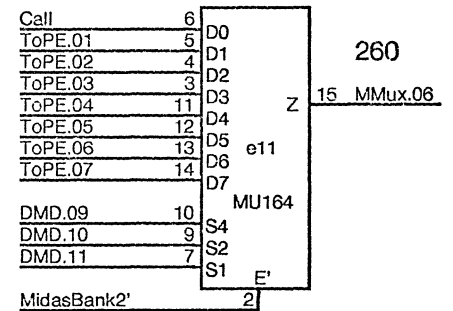
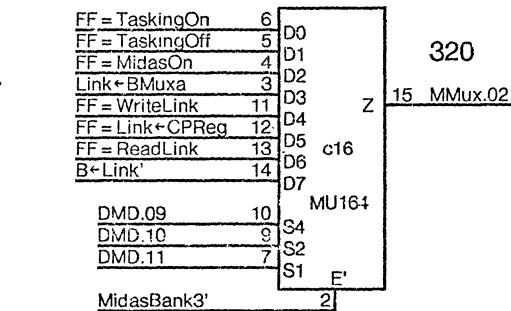
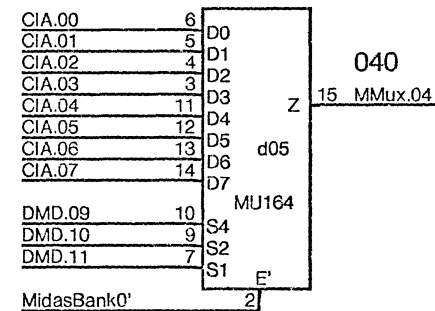
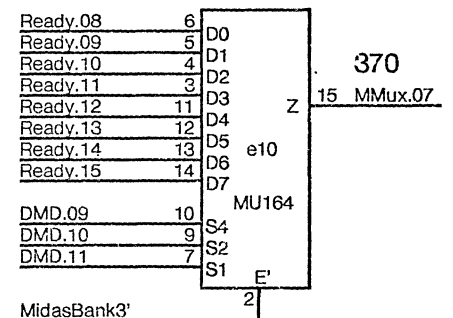
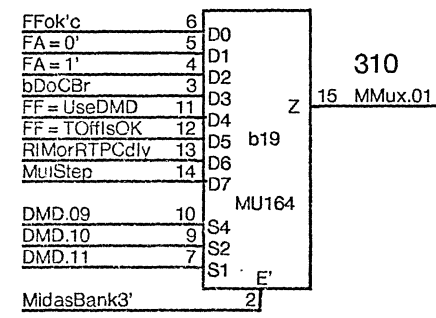
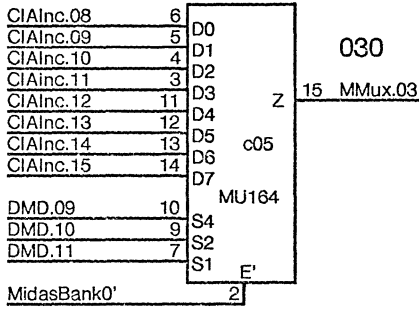
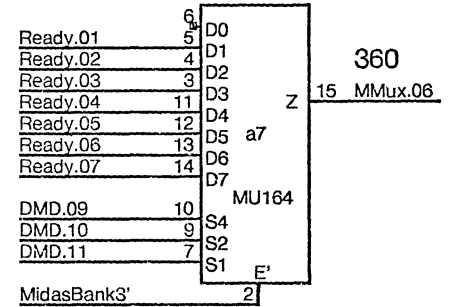
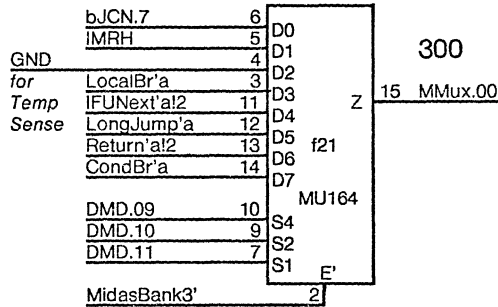
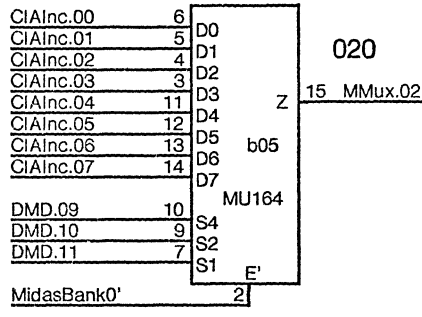
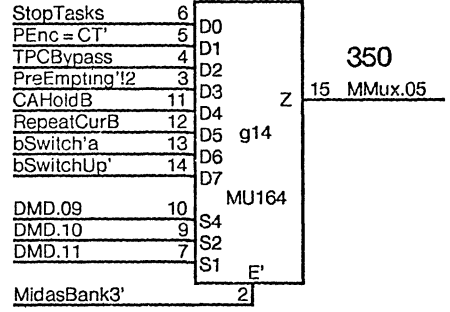
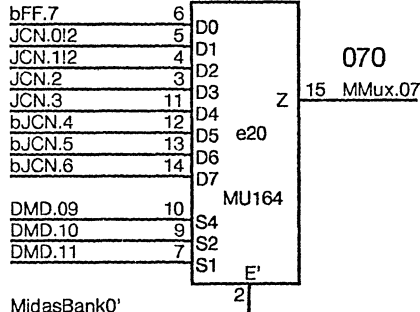
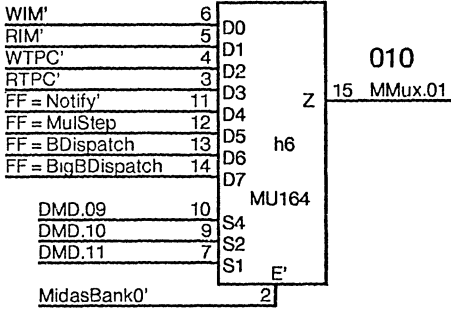
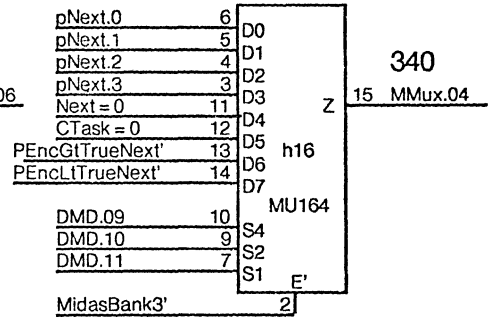
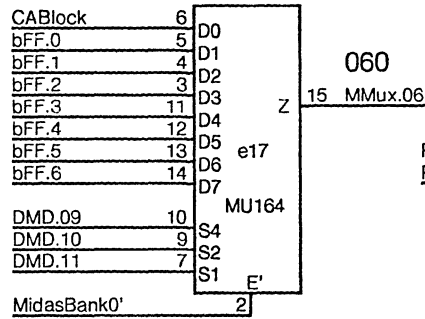
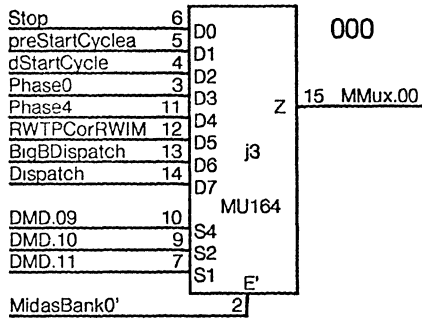
Continued on
Print 30.

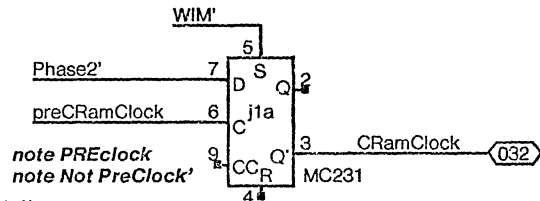
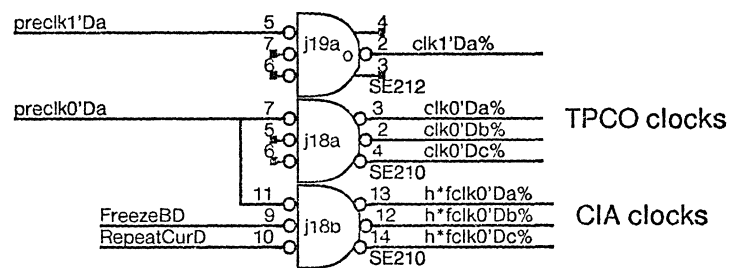
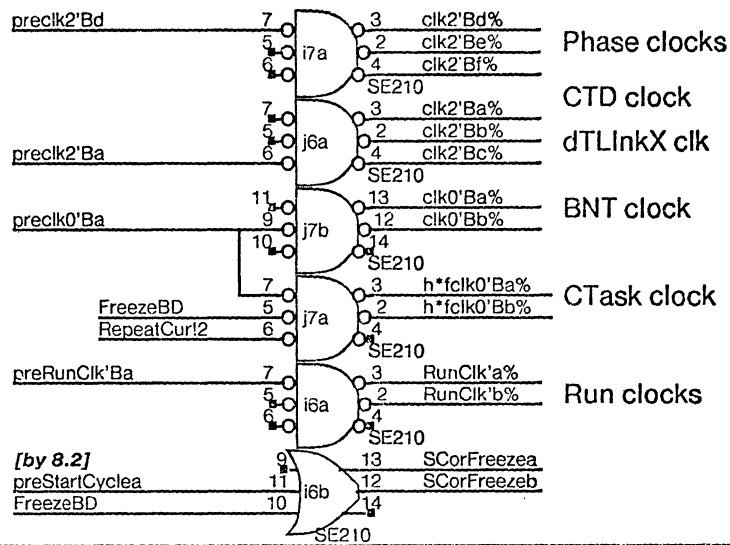
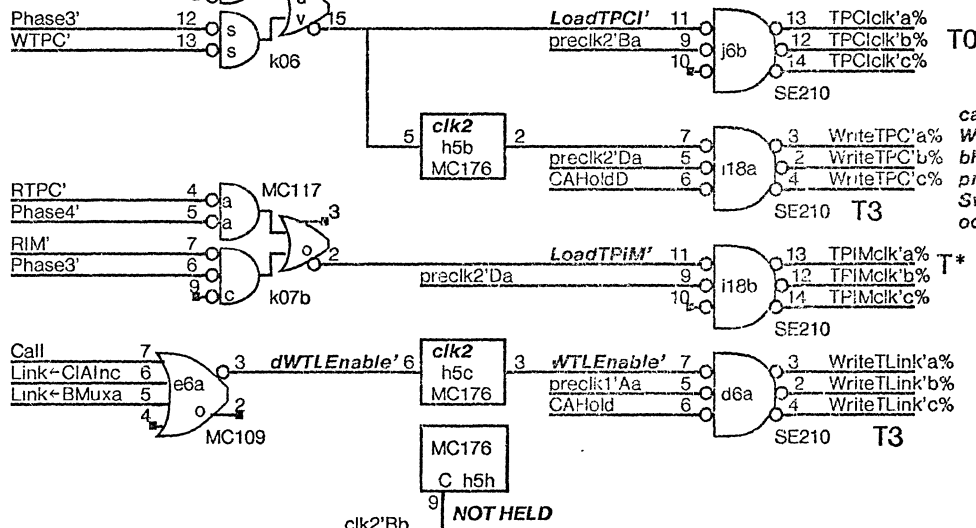
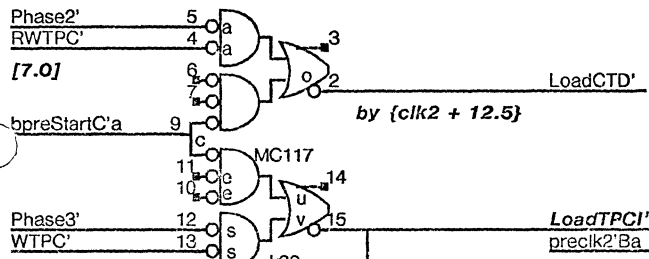
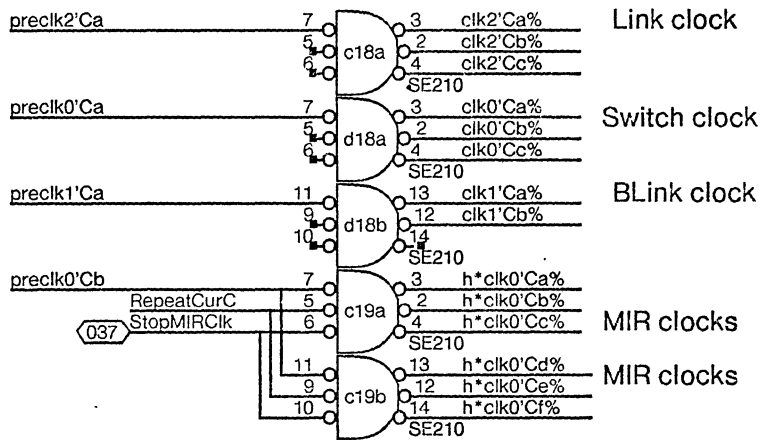
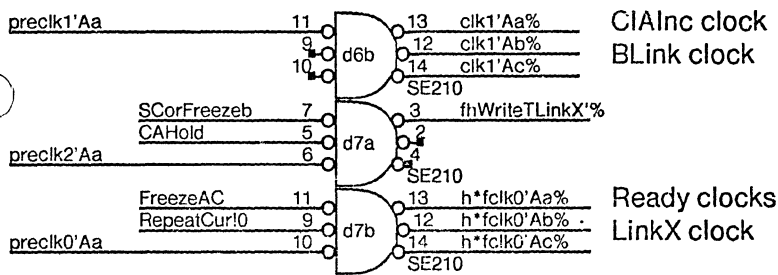


ROGUE MUFFLER

DORADO controls muffler system whenever SetRun is active
 CP must turn off SetRun to use mufflers



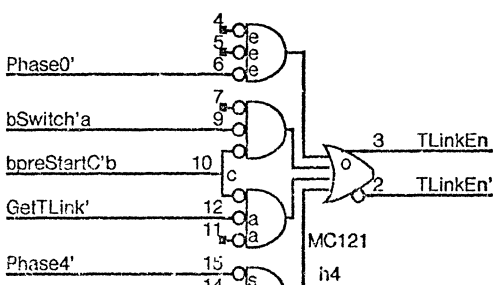
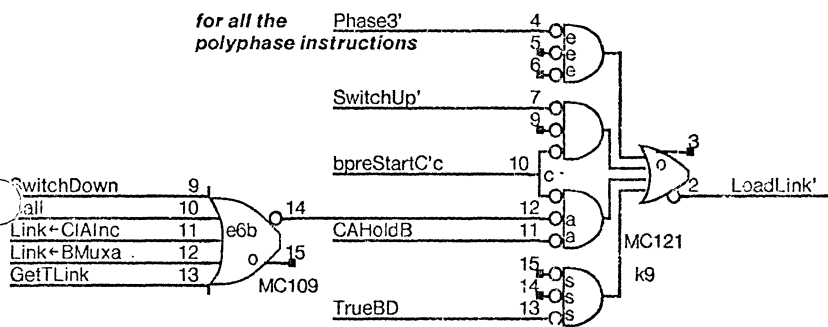
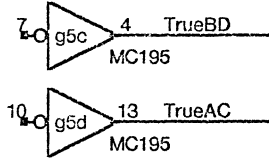




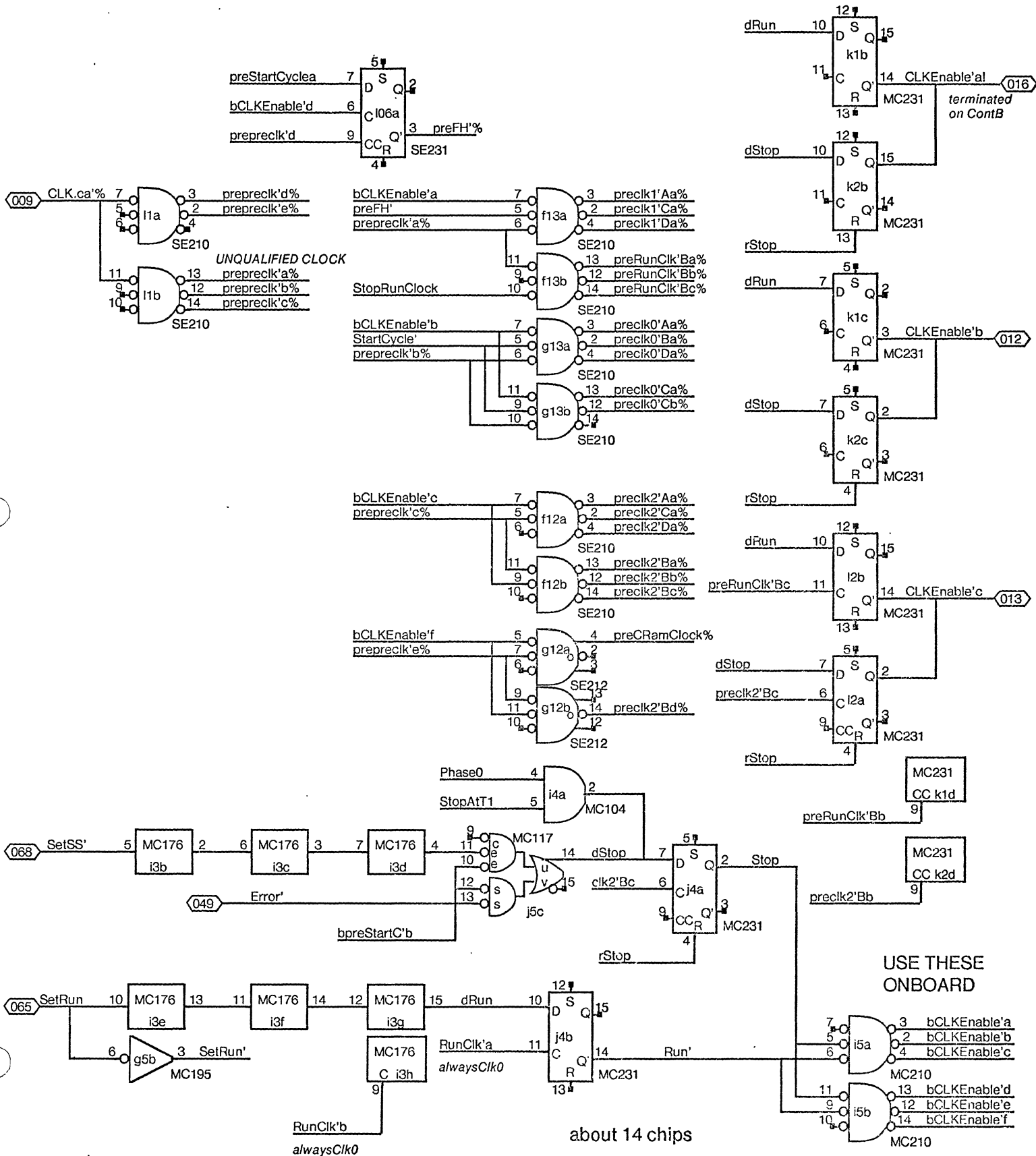
T0
cannot have HOLD and WTPC instruction bHold is needed to prevent writing when SwitchUp and Hold occurs

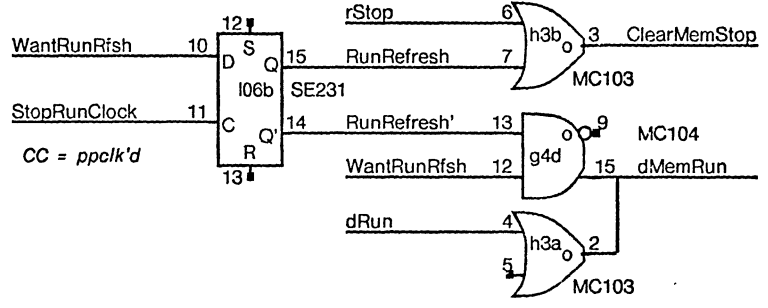
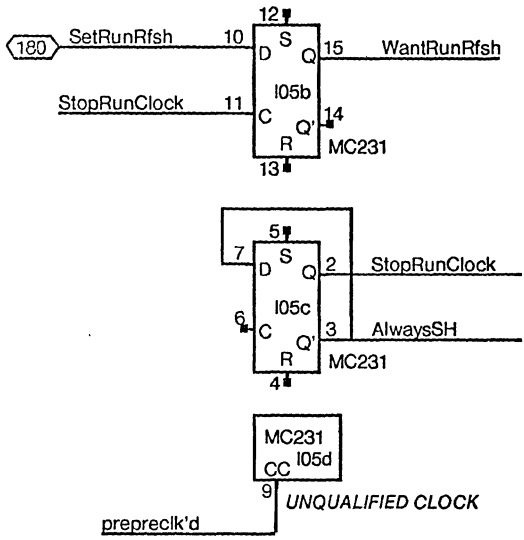
T*

T3



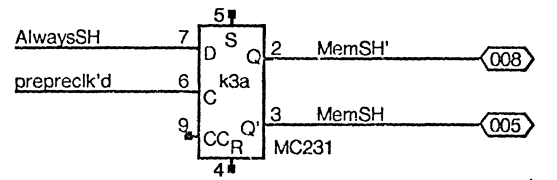
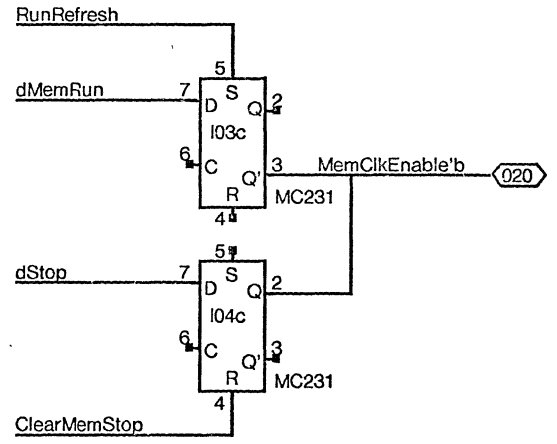
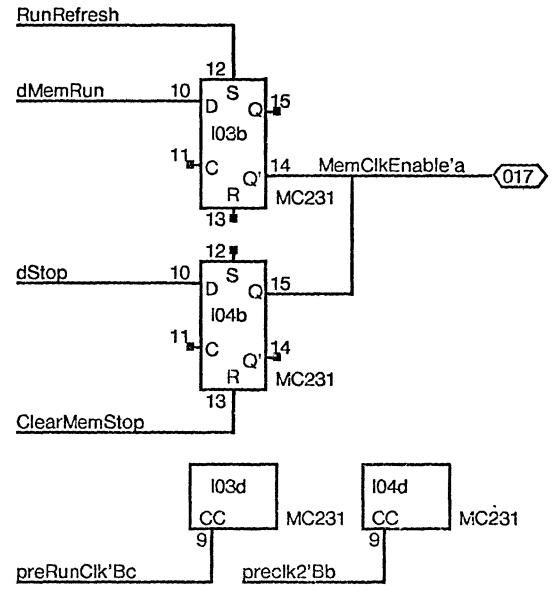
about 16 chips
This term just for TLinkX & WTPC





Whatever1	P1 SPARE
16	P16 a5
8	P8
Whatever1	P1 SPARE
16	P16 a6
8	P8
Whatever1	P1 SPARE
16	P16 d16
8	P8
Whatever1	P1 SPARE
16	P16 e16
8	P8
Whatever1	P1 SPARE
16	P16 f18
8	P8
Whatever1	P1 SPARE
16	P16 h15
8	P8
Whatever1	P1 SPARE
16	P16 h20
8	P8
Whatever1	P1 SPARE
16	P16 i8
8	P8
Whatever1	P1 SPARE
16	P16 i16
8	P8
Whatever1	P1 SPARE
16	P16 j21
8	P8
Whatever1	P1 SPARE
16	P16 k8
8	P8
Whatever1	P1 SPARE
16	P16 i9
8	P8
Whatever1	P1 SPARE
16	P16 i23
8	P8

MultiWire spares



C		MRHPE BNTGICT		dCSOut		TWRq9-15		dCSOut		CP INTERFACE		TWRq1-8		RSTK		CLOCK	
A	a 181	b 168	c 153	d 137	e 124	f 109	93 g	80 h	64 i	48 j	33 k	20 l	B				
1	CPStrobe 161 2	dTLINK 189 159	dTLINK 231011 159	dTLINK 451213 159	RBmux 4.12-15 197	dTLINK 571415 159	SetMIR 172 2	SetMIR 172 2	SetMIR 172 2	CramClk Phase4 231	CLKEN 231	RAWClk 210	1				
2	MIR/BGICT 2,25 210	DrBMux 189 159	DrBMux 231011 159	DrBMux 451213 159	DrBMux 671415 159	CPREG-0 176	CPREG-1 176	CPREG-1 176	CLOCK 176 2	CONTROL 176 2	CLKEN 231	CLKEN 231	2				
3	CPREG-0 176	MLINK 189 159	MLINK 231011 159	MLINK 451213 159	MLINK 671415 159	JAM 197		dMCE OR 32,32C,2 103	dStpRun 176	MU 000	SCycle 27 MemSH' 30 231	MEMCLKEN 231	3				
4	TLINK 145	TLINK 145	TLINK 145	TLINK 145	TLINKX 145 5	dTLINKX F16 5	MemRun 104	TLinkEn 121	sPh0,d.. 31,27,27,28 104	Stp/run 231	SC(NF) 231	MEMCLKEN 231	4				
5		MU 020	MU 030	MU 040	TLINKX bypass 197 5	LINKX 231 5	inverter 195	CLK2 30,30,.... 176	bClkEn 210	Err/dSC 117	2,3 231 25	RunRfsh 231	5				
6		NOTIFY 162	CLK 210	dWTL 109	LINKX 231 5	CTD 231	MU 010	CLK 210	CLK 210	TPCI/CTD 117	FH 231		6				
7	MU 360	PREEMPT 162	CLK 210	CIAInc 176	MU 330	dCTD 158	clk/Freez 210	CLK 210	TPCSclk CIA 117	0,1 231			7				
8	104	SETREADY 104	104	104	76	IS 161	TLink 100	BNT 141	CTASK 231	bSC 27,B 211			8				
9	F00	READY F00	F00	3*23,D F00	MU 270	NEXT 161	Addr 100	141	MU 170	231	LoadLink 121		9				
10	1664	TWREQ 1664	1664	3*23,D 1664	MU 370	PE 121		BNxtEn 166	PE>TN 166	CT = NX = 0 109	DMD 176	MIDAS 171	10				
11	104	ToPE drivers 104	104	3*23,4 104	MU 260	121	102	PE>TN 166	bPE 101	PE = CT 113	CALL 104	DMD 176	11				
12	176	BLINK 176	ToPE rcvrs 109	109	3*24, d101	PRECLK 210	PRECLK 212	176	TPCI 1662	TPCad 1662	TPCI 176	TPCI 176	12				
13	4,4,c,4 102	LINK F16	BLINK CIAInc 176	102	102	PRECLK 210	PRECLK 210	pNext 159	TPC 145	TPC 145	TPC 145	TPC 145	13				
14	102 5	dBLINK 159	LINK F16	LINK F16	LINK F16	SWITCH 231	MU 350	NEXT 159	TPIM 173	TPIM 173	TPIM 173	TPIM 173	14				
15	5,5,5,4 102	FFBR 162 5	dBLINK 159	dBLINK 159	dBLINK 159	SWUp 231	1662		TPCO F16	TPCO F16	TPCO F16	TPCO F16	15				
16	100 4	4,4,5,4 103	MU 320			dSWup 1660	STKSEL 231 1,C	MU 340		CIA' 176	CIA' 176	CIA' 176	16				
17	100 4	100 4	clk1 4*4 BLINK 176 6,8	T2 3,4, 26,26 176 fq	MU 060	dSWdwn 1660	MU 050	113	CIA ADDER 105	109	CIA 195	clk1 4*28,4,g 176	17				
18	bFF 212 1	109 4	CLK 210	CLK 210	IMRH 170 1		RA 159	CIA 195	CLK 210	CLK 210	CIA 195	bTNIA 197	18				
19	FB = 161 4	MU 310	CLK 210	JBr 162 5	IMRH 170 1	Hold 211	bJCN 212 1	RA 159	TNIA 0-3 159	CLK/SW 212	RA 159	RA 159	19				
20	109 4	bFF 212 1	DoCBr 121 5	RW... 161 3	MU 070	RptCur 1660	bJCN 212 1		BNPC 158	bTNIA 197	BNPC 158	BNPC 158	20				
21	102 4	FC = 161 4	DoCBr 121 5 d	3,3,5,3 102	RETURN 210 3	MU 300	BNPC 158	bTNIA 197	bTNIA 159		100	Midas 4*28, 197 th	21				
22	bFF 212 1	bFF 212 1	DoCBr 5 PreEmp 1662	LocalBr 210 3,5	IFUNext 210 3	CBR/LJ 210 3	TNIA 159	8 121	TNIA 101	13 121	105	Midas 164	22				
23	FF2,3 231 1	FF6,7 231 1	JCN0,1 231 1	JCN2or3 231 1	IMRH,BLK 231 1	CBR 211 3	6 121	7 121	9 TNIA 121	12 121	14 121		23				
24	FF0,1 231 1	FF4,5 231 1	JCN4,5 231 1	JCN2,3 231 1	JCN6,7 231 1	FFok 211 3	4 121	5 121	10 121	11 121	15 121	Midas 102	24				

C a 11 b 26 c 39 d 55 e 70 f 86 99 g 114 h 129 i 143 j 159 k 174 l D

E NEXT BLOCK HOLD' FFOK dMIR FF0-3 dMIR BrCond FF4-7 TNIA0-7 BNPC0-2 IFADR TNIA/BNPC BrCond SW DMUX

XEROX PARC	Project Dorado	Reference Control A Layout	File ContA33.sil	Designer Pier	Rev Cd	Date 7/13/79	Page 33
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Page Numbers: Yes First Page: 1
 Columns: 2 Edge Margin: .8" Between Columns: .0"
 Heading:
 ContA-Rev-Cd.ps
 COMPONENTS:

F00:	22	23				
F145A:	5	6	7	8	9	10
	11	12	13	14	15	16
	17	18	19	20	21	
F16:	5	6	7	8	9	10
	11	12	13	14	15	16
	17	18	19	20	21	
MC100:	4	17	18	19	26	
MC101:	12	13	14	15	24	26
MC102:	3	4	5	24	28	
MC103:	2	4	32			
MC104:	3	4	10	11	17	18
	22	23	27	28	31	32
MC105:	16	17	18			
MC109:	4	14	15	24	25	30
MC113:	15	16	17	18	25	
MC117:	14	27	30	31		
MC121:	5	8	9	10	11	12
	13	14	15	16	17	18
	19	24	30			
MC141:	26					
MC158:	6	7	8	9	10	11
	12	13	14	15	16	17
	18	19	20	21	26	
MC159:	6	7	8	9	10	11
	12	13	14	15	16	17
	18	19	20	21	26	
MC161:	2	3	4	22	23	
MC162:	5	22	23			
MC166:	25					
MC1660:	25	28				
MC1662:	5	25	26			
MC1664:	22	23				
MC170:	1					
MC171:	28					
MC172:	2					
MC173:	6	7	8	9	10	11
	12	13	14	15	16	17
	18	19	20	21		
MC176:	2	3	4	6	7	8
	9	10	11	12	13	14
	15	16	17	18	19	20
	21	28	30	31		
MC195:	2	3	6	7	8	9
	10	11	12	13	14	15
	16	17	18	19	30	31
MC197:	5	6	7	8	9	10
	11	12	13	14	15	16
	17	18	19	20	21	28
MC210:	2	3	5	25	31	
MC211:	3	27				
MC212:	1					
MC231:	1	5	25	26	27	30
	31	32				
MU164:	28	29				
SE210:	1	2	30	31		
SE211:	25					
SE212:	25	30	31			
SE231:	31	32				
SPARE:	32					

SIGNAL NAMES:

+	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
	19(1)	20(1)	21(1)	22(1)	23(1)	24(1)
	25(1)	26(1)	27(1)	28(1)	29(1)	30(1)
	31(1)	32(1)				

11or10':	24(2)				
15/14/11/10:	24(2)				
15or14':	24(2)				
15to12':	24(1)				
15to8:	24(4)				
1andNot3or2':	24(2)				
3or2':	24(2)				
7or6:	24(2)				
7or6':	24(2)				
7to4:	24(4)				
7to4':	24(2)				
ALUCarry:	5(1)				
ALwaysSH:	32(2)				
ASEL.0'a:	4(4)				
bCLKEnable'a:	31(2)				
bCLKEnable'b:	31(2)				
bCLKEnable'c:	31(2)				
bCLKEnable'd:	31(2)				
bCLKEnable'e:	27(1)	31(1)			
bCLKEnable'f:	31(2)				
bDMuxClk':	28(2)				
bDMuxData:	28(2)				
bDoCBr:	5(1)	29(1)			
bFF.0:	1(1)	29(1)			
bFF.0':	1(1)	8(1)			
bFF.0a:	1(2)				
bFF.1:	1(1)	29(1)			
bFF.1':	1(1)	9(1)			
bFF.1a:	1(2)				
bFF.2:	1(1)	29(1)			
bFF.2':	1(1)	10(1)			
bFF.2a:	1(2)				
bFF.3:	1(1)	29(1)			
bFF.3':	1(1)	11(1)			
bFF.3a:	1(2)				
bFF.4:	1(1)	22(1)	29(1)		
bFF.4':	1(1)	12(1)	23(1)		
bFF.4a:	1(2)				
bFF.5:	1(1)	5(1)	22(1)	23(1)	29(1)
bFF.5':	1(1)	13(1)			
bFF.5a:	1(2)				
bFF.6:	1(1)	5(1)	22(1)	23(1)	29(1)
bFF.6':	1(1)	14(1)			
bFF.6a:	1(2)				
bFF.7:	1(1)	5(1)	22(1)	23(1)	29(1)
bFF.7':	1(1)	15(1)			
bFF.7a:	1(2)				
BigBDispatch:	5(1)	29(1)			
bJCN.1'a:	1(2)				
bJCN.1'b:	1(1)	14(1)			
bJCN.4:	1(2)	29(1)			
bJCN.4':	1(1)	18(1)	19(1)		
bJCN.4'a:	1(1)	10(1)	16(1)		
bJCN.5:	1(2)	29(1)			
bJCN.5':	1(1)	17(1)			
bJCN.5'a:	1(1)	11(1)			
bJCN.6:	1(2)	29(1)			
bJCN.6':	1(1)	18(1)			
bJCN.6'a:	1(1)	12(1)			
bJCN.7:	1(2)	29(1)			
bJCN.7':	1(1)	19(1)			
bJCN.7'a:	1(1)	13(1)			
BLock:	1(1)				
Block':	1(1)	25(3)			
BMux.00!:	6(2)				
BMux.01!:	6(2)				
BMux.02!:	7(2)				
BMux.03!:	7(2)				
BMux.04!:	8(2)				
BMux.05!:	9(2)				
BMux.06!:	10(2)				
BMux.07!:	11(2)				
BMux.08!:	12(2)				
BMux.09!:	13(2)				
BMux.10!:	14(2)				
BMux.11!:	15(2)				

BMux.12!:	16(2)			
BMux.13!:	17(2)			
BMux.14!:	18(2)			
BMux.15!:	19(2)			
BNextRegsEn'!1:	26(2)			
BNextRegsEn'!2:	25(1)			
BNextRegsEn'!3:	20(2)	21(2)		
BNPC.00:	6(1)			
BNPC.01:	6(1)			
BNPC.02:	7(1)			
BNPC.03:	7(1)			
BNPC.04:	8(1)			
BNPC.05:	9(1)			
BNPC.06:	10(1)			
BNPC.07:	11(1)			
BNPC.08:	12(1)			
BNPC.09:	13(1)			
BNPC.10:	14(1)			
BNPC.11:	15(1)			
BNPC.12:	16(1)			
BNPC.13:	17(1)			
BNPC.14:	18(1)			
BNPC.15:	19(1)			
BNT.0:	22(1)	25(1)	26(1)	29(1)
BNT.0':	23(1)	26(1)		
BNT.1:	22(1)	25(1)	26(1)	29(1)
BNT.1':	23(1)	26(1)		
BNT.2:	22(1)	25(1)	26(1)	29(1)
BNT.2':	23(1)	26(1)		
BNT.3:	22(1)	25(1)	26(1)	29(1)
BNT.3':	23(1)	26(1)		
BNTGtCT'a!:	25(1)			
BNTGtCT'b:	25(1)			
bPEnc.0:	26(1)	29(1)		
bPEnc.0':	25(1)	26(1)		
bPEnc.1:	26(1)	29(1)		
bPEnc.1':	25(1)	26(1)		
bPEnc.2:	26(1)	29(1)		
bPEnc.2':	25(1)	26(1)		
bPEnc.3:	26(1)	29(1)		
bPEnc.3':	25(1)	26(1)		
bpreStartC'a:	26(1)	27(1)	30(1)	
bpreStartC'b:	27(1)	30(1)	31(1)	
bpreStartC'c:	27(1)	30(1)		
brMIRa:	1(9)	2(1)		
brMIRb:	1(11)	2(1)		
brMIRc:	1(1)	2(1)		
BSEL.0':	3(1)			
bSwitch'a:	25(1)	29(1)	30(1)	
bSwitchUp':	25(1)	29(1)		
bTNIA.15:	5(1)	19(1)		
B-Link':	4(1)	20(2)	21(2)	29(1)
CABlock:	1(2)	29(1)		
CAHold:	30(2)			
CAHold%:	25(1)			
CAHold' %:	25(1)			
CAHoldB:	29(1)	30(1)		
CAHoldB%:	25(1)			
CAHoldD:	30(1)			
CAHoldD%:	25(1)			
Call:	3(1)	29(1)	30(2)	
Call12:	3(1)	16(1)		
Call13':	3(1)	17(1)		
Call14':	3(1)	18(1)		
Call15:	3(1)	19(1)		
CBrOnCnt=0':	5(1)			
CBrOnNoCarry':	5(1)			
CBrOnNoIOAtt':	5(1)			
CBrOnOverflow':	5(1)			
CBrOnRes=0':	5(1)			
CBrOnResLt0':	5(1)			
CBrOnRltZero':	5(1)			
CBrOnROdd':	5(1)			
CHoldReq:	4(1)			
CIA.00:	6(1)	29(1)		
CIA.00':	6(2)			

CIA.01:	6(1)	29(1)			
CIA.01':	6(2)				
CIA.02:	7(1)	29(1)			
CIA.02':	7(2)				
CIA.03:	7(1)	29(1)			
CIA.03':	7(2)				
CIA.04:	8(2)	29(1)			
CIA.04':	8(3)				
CIA.05:	9(2)	29(1)			
CIA.05':	9(3)				
CIA.06:	10(2)	29(1)			
CIA.06':	10(3)				
CIA.07:	11(2)	29(1)			
CIA.07':	11(3)				
CIA.08:	12(2)	29(1)			
CIA.08':	12(3)				
CIA.09:	13(2)	29(1)			
CIA.09':	13(3)				
CIA.10:	14(2)	29(1)			
CIA.10':	14(2)				
CIA.11:	15(2)	29(1)			
CIA.11':	14(1)	15(1)			
CIA.12:	16(2)	29(1)			
CIA.12':	14(1)	15(1)	16(1)		
CIA.13:	17(2)	29(1)			
CIA.13':	14(1)	15(1)	16(1)	17(1)	
CIA.14:	18(2)	29(1)			
CIA.14':	14(1)	15(1)	16(1)	17(1)	18(1)
CIA.15:	18(1)	19(1)	29(1)		
CIA.15':	14(1)	15(1)	16(1)	17(1)	19(2)
CIAInc.00:	6(1)	29(1)			
CIAInc.01:	6(1)	29(1)			
CIAInc.02:	7(1)	29(1)			
CIAInc.03:	7(1)	29(1)			
CIAInc.04:	8(1)	29(1)			
CIAInc.05:	9(1)	29(1)			
CIAInc.06:	10(1)	29(1)			
CIAInc.07:	11(1)	29(1)			
CIAInc.08:	12(1)	29(1)			
CIAInc.09:	13(1)	29(1)			
CIAInc.10:	14(1)	29(1)			
CIAInc.11:	15(1)	29(1)			
CIAInc.12:	16(1)	29(1)			
CIAInc.13:	17(1)	29(1)			
CIAInc.14:	18(1)	29(1)			
CIAInc.15:	19(1)	29(1)			
ClearMemStop:	32(3)				
CLK.ca' %:	31(1)				
clk0'Ba:	26(1)				
clk0'Ba%:	30(1)				
clk0'Bb:	26(1)				
clk0'Bb%:	30(1)				
clk0'Ca:	25(1)				
clk0'Ca%:	30(1)				
clk0'Cb:	25(1)				
clk0'Cb%:	30(1)				
clk0'Cc:	4(1)				
clk0'Cc%:	30(1)				
clk0'Da:	20(1)				
clk0'Da%:	30(1)				
clk0'Db:	21(1)				
clk0'Db%:	30(1)				
clk0'Dc:	20(1)	21(1)			
clk0'Dc%:	30(1)				
clk1'Aa:	20(1)				
clk1'Aa%:	30(1)				
clk1'Ab:	21(1)				
clk1'Ab%:	30(1)				
clk1'Ac:	20(1)	21(1)			
clk1'Ac%:	30(1)				
clk1'Ca:	20(1)				
clk1'Ca%:	30(1)				
clk1'Cb:	20(1)				
clk1'Cb%:	30(1)				
clk1'Da:	28(1)				
clk1'Da%:	30(1)				

clk2'Ba:	26(2)			
clk2'Ba%:	30(1)			
clk2'Bb:	30(1)			
clk2'Bb%:	30(1)			
clk2'Bc:	27(1)	31(1)		
clk2'Bc%:	30(1)			
clk2'Bd:	5(1)	26(2)		
clk2'Bd%:	30(1)			
clk2'Be:	27(2)			
clk2'Be%:	30(1)			
clk2'Bf:	27(1)			
clk2'Bf%:	30(1)			
clk2'Ca:	20(2)			
clk2'Ca%:	30(1)			
clk2'Cb:	21(1)			
clk2'Cb%:	30(1)			
clk2'Cc:	21(1)			
clk2'Cc%:	30(1)			
CLKEnable'a!:	31(1)			
CLKEnable'b:	31(1)			
CLKEnable'c:	31(1)			
ClrReady:	2(1)	22(2)	23(2)	
Cnt=Zero:	5(1)			
CondBr'a:	5(1)	29(1)		
CondBr'a%:	3(1)			
CondBr'b:	12(1)	17(1)	18(1)	
CondBr'b%:	3(1)			
CondBr'c:	8(1)	9(1)	10(1)	11(1)
CondBr'c%:	3(1)			
CP=UseCPRreg:	2(1)	4(1)		
CPAddr.0':	2(2)			
CPAddr.1':	2(2)			
CPAddr.2':	2(2)			
CPOut.0:	6(1)	12(1)		
CPOut.1:	2(1)	6(1)	13(1)	
CPOut.2:	2(2)	7(1)	14(1)	
CPOut.3:	2(2)	7(1)	15(1)	
CPOut.4:	2(3)	8(1)	16(1)	
CPOut.5:	2(2)	9(1)	17(1)	
CPOut.6:	2(2)	10(1)	18(1)	
CPOut.7:	2(2)	11(1)	19(1)	
CPOut.8:	2(1)			
CPReg.00:	6(1)			
CPReg.01:	6(1)			
CPReg.02:	7(1)			
CPReg.03:	7(1)			
CPReg.04:	8(1)			
CPReg.05:	9(1)			
CPReg.06:	10(1)			
CPReg.07:	11(1)			
CPReg.08:	12(1)			
CPReg.09:	13(1)			
CPReg.10:	14(1)			
CPReg.11:	15(1)			
CPReg.12:	16(1)			
CPReg.13:	17(1)			
CPReg.14:	18(1)			
CPReg.15:	19(1)			
CPStrb':	2(2)			
CPStrb0':	2(2)			
CPStrb1':	2(2)			
CPStrb2':	2(1)	20(2)		
CPStrb3':	2(1)	21(2)		
CRamClock:	30(1)			
CTask.0:	22(1)	25(2)	26(1)	28(1)
CTask.0':	23(1)	25(1)	26(3)	
CTask.1:	22(1)	23(1)	25(2)	26(1) 28(1)
CTask.1':	25(1)	26(3)		
CTask.2:	22(1)	23(1)	25(2)	26(1) 28(1)
CTask.2':	25(1)	26(3)		
CTask.3:	22(1)	23(1)	25(2)	26(1) 28(1)
CTask.3':	25(1)	26(3)		
CTask=0:	25(1)	29(1)		
CTD.0:	26(2)	28(1)		
CTD.0':	26(1)			
CTD.1:	26(2)	28(1)		

CTD.1':	26(1)		
CTD.2:	26(2)	28(1)	
CTD.2':	26(1)		
CTD.3:	26(2)	28(1)	
CTD.3':	26(1)		
dBlock':	1(2)	25(1)	
dFF.0:	1(1)		
dFF.1:	1(1)		
dFF.2:	1(1)		
dFF.3:	1(1)		
dFF.4:	1(1)		
dFF.5:	1(1)		
dFF.6:	1(1)		
dFF.7:	1(1)		
dIMOut.07:	11(1)		
dIMOut.08:	12(1)		
dIMOut.09:	13(1)		
dIMOut.10:	14(1)		
dIMOut.11:	15(1)		
dIMOut.12:	16(1)		
dIMOut.13:	17(1)		
dIMOut.14:	18(1)		
dIMOut.15:	19(1)		
dIMRH:	1(1)		
Dispatch:	5(1)	29(1)	
dJCN.0:	1(1)		
dJCN.1:	1(1)		
dJCN.2:	1(2)		
dJCN.3:	1(2)		
dJCN.4:	1(1)		
dJCN.5:	1(1)		
dJCN.6:	1(1)		
dJCN.7:	1(1)		
DMD.01:	28(2)		
DMD.02:	28(2)		
DMD.03:	28(2)		
DMD.04:	28(2)		
DMD.05:	28(2)		
DMD.06:	28(3)		
DMD.07:	28(3)		
DMD.08:	28(3)		
DMD.09:	28(3)	29(18)	
DMD.10:	28(3)	29(18)	
DMD.11:	28(3)	29(18)	
dMemRun:	32(3)		
DMuxClk!:	28(1)		
DMuxData!:	28(1)		
DMuxEnable':	28(2)		
DoCBr:	5(1)		
dRun:	31(4)	32(1)	
dStartCycle:	27(1)	29(1)	
dStop:	31(4)	32(2)	
dSwitch:	25(1)		
dSwitchUp':	25(1)		
Error':	31(1)		
FA=0':	4(2)	5(1)	29(1)
FA=1':	4(4)	29(1)	
FB=3':	4(2)		
FB=4':	4(7)		
FB=6':	4(1)	5(1)	
FB=7':	4(7)		
FC=0':	4(3)		
FC=1':	4(4)		
FC=2':	4(4)		
FC=3':	4(2)		
FC=5':	4(2)		
FC=6':	4(2)		
FC=7':	4(3)		
FF.0:	1(1)	4(1)	
FF.0':	1(1)	4(2)	
FF.1:	1(1)		
FF.1':	1(1)	4(3)	
FF.2:	1(1)		
FF.2':	1(1)	4(2)	
FF.3:	1(1)		
FF.3':	1(1)	4(2)	

FF.4:	1(1)					
FF.4':	1(1)	4(1)				
FF.5:	1(1)					
FF.5':	1(1)	4(1)				
FF.6:	1(1)					
FF.6':	1(1)	4(1)				
FF.7:	1(1)					
FF.7':	1(1)	4(1)				
FF=BDispatch:	4(2)	5(1)	29(1)			
FF=BigBDispatch:	4(2)	5(1)	29(1)			
FF=B+Dbuf:	4(2)					
FF=Link+CPReg:	4(3)	29(1)				
FF=MidasOn:	4(1)	28(1)	29(1)			
FF=MulStep:	4(1)	5(1)	29(1)			
FF=Notify':	4(1)	22(1)	23(1)	29(1)		
FF=ReadLink:	4(2)	29(1)				
FF=TaskingOff:	4(2)	29(1)				
FF=TaskingOn:	4(2)	29(1)				
FF=TOffIsOK:	4(2)	29(1)				
FF=UseDMD:	4(1)	28(1)	29(1)			
FF=WriteLink:	4(2)	29(1)				
FFBrOnCnt=0:	5(2)					
FFBrOnNoCarry:	5(2)					
FFBrOnNoIOAtt:	5(2)					
FFBrOnOverflow:	5(2)					
FFBrOnRes=0:	5(2)					
FFBrOnResLt0:	5(2)					
FFBrOnRLt0:	5(2)					
FFBrOnROdd:	5(2)					
FFok'a%:	3(1)					
FFok'b%:	3(1)					
FFok'c:	4(3)	29(1)				
FFok'c%:	3(1)					
fhWriteTLinkX':	5(1)					
fhWriteTLinkX'%:		30(1)				
Freeze:	2(1)					
FreezeAC:	2(1)	25(3)	30(1)			
FreezeBD:	2(1)	27(1)	30(3)			
GetTLink:	2(1)	30(1)				
GetTLink':	2(1)	30(1)				
GND:	29(1)					
Gnd:	1(1)	2(1)	3(1)	4(1)	5(1)	6(1)
	7(1)	8(1)	9(1)	10(1)	11(1)	12(1)
	13(1)	14(1)	15(1)	16(1)	17(1)	18(1)
	19(1)	20(1)	21(1)	22(1)	23(1)	24(1)
	25(1)	26(1)	27(1)	28(1)	29(1)	30(1)
	31(1)	32(1)				
h*c1k0'Ca:	1(1)					
h*c1k0'Ca%:	30(1)					
h*c1k0'Cb:	1(1)					
h*c1k0'Cb%:	30(1)					
h*c1k0'Cc:	1(1)					
h*c1k0'Cc%:	30(1)					
h*c1k0'Cd:	1(1)					
h*c1k0'Cd%:	30(1)					
h*c1k0'Ce:	1(1)					
h*c1k0'Ce%:	30(1)					
h*c1k0'Cf:	1(1)					
h*c1k0'Cf%:	30(1)					
h*fc1k0'Aa:	5(1)					
h*fc1k0'Aa%:	30(1)					
h*fc1k0'Ab:	22(2)					
h*fc1k0'Ab%:	30(1)					
h*fc1k0'Ac:	23(2)					
h*fc1k0'Ac%:	30(1)					
h*fc1k0'Ba:	26(1)					
h*fc1k0'Ba%:	30(1)					
h*fc1k0'Bb:	26(1)					
h*fc1k0'Bb%:	30(1)					
h*fc1k0'Da:	20(1)					
h*fc1k0'Da%:	30(1)					
h*fc1k0'Db:	21(1)					
h*fc1k0'Db%:	30(1)					
h*fc1k0'Dc:	20(1)					
h*fc1k0'Dc%:	30(1)					
Hold%:	25(1)					

IfuAddr.04':	8(1)			
IfuAddr.05':	9(1)			
IfuAddr.06':	10(1)			
IfuAddr.07':	11(1)			
IfuAddr.08':	12(1)			
IfuAddr.09':	13(1)			
IfuAddr.10':	14(1)			
IfuAddr.11':	15(1)			
IfuAddr.12':	16(1)			
IfuAddr.13':	17(1)			
IFUNext'a!0:	3(1)	12(1)	17(1)	
IFUNext'a!1:	3(1)			
IFUNext'a!2:	3(1)	4(1)	29(1)	
IFUNext'b!0:	10(1)	11(1)	13(1)	
IFUNext'b!1:	3(1)			
IFUNext'b!2:	16(1)	18(1)		
IFUNext'c!0:	8(1)	9(1)	14(1)	
IFUNext'c!1:	3(1)			
IFUNext'c!2:	15(1)	19(1)		
IfuNextMacro':	3(1)	5(1)		
IMRH:	1(2)	29(1)		
IMRHPE':	1(1)			
IOatt:	5(1)			
IsNext.01':	22(2)			
IsNext.02':	22(2)			
IsNext.03':	22(2)			
IsNext.04':	22(2)			
IsNext.05':	22(2)			
IsNext.06':	22(2)			
IsNext.07':	22(2)			
IsNext.08':	23(2)			
IsNext.09':	23(2)			
IsNext.10':	23(2)			
IsNext.11':	23(2)			
IsNext.12':	23(2)			
IsNext.13':	23(2)			
IsNext.14':	23(2)			
IsNext.15':	23(2)			
Jam:	2(1)	6(1)	10(1)	11(1)
JBrOnCnt=0:	5(2)			
JBrOnNoCarry:	5(2)			
JBrOnNoIOAtt:	5(2)			
JBrOnRes=0:	5(2)			
JBrOnResLt0:	5(2)			
JBrOnRLt0:	5(2)			
JBrOnROdd:	5(2)			
JCN.0!0:	3(3)			
JCN.0!1:	1(1)			
JCN.0!2:	3(2)	29(1)		
JCN.0':	1(1)	3(1)	20(1)	21(1)
JCN.0%:	1(1)			
JCN.1!0:	3(3)			
JCN.1!1:	1(1)			
JCN.1!2:	3(2)	29(1)		
JCN.1':	3(1)	20(1)	21(1)	
JCN.1%:	1(1)			
JCN.2:	1(1)	3(1)	29(1)	
JCN.2%:	1(1)			
JCN.2'a:	3(2)			
JCN.2'a%:	1(1)			
JCN.2'b:	3(1)	8(1)	14(1)	15(1)
JCN.2'b%:	1(1)			
JCN.2or3:	3(2)			
JCN.2or3%:	1(1)			
JCN.3:	1(1)	3(1)	29(1)	
JCN.3%:	1(1)			
JCN.3'a:	3(1)			
JCN.3'a%:	1(1)			
JCN.3'b:	9(1)	15(1)	17(1)	18(1)
JCN.3'b%:	1(1)			
JCN.4%:	1(1)			
JCN.4':	3(1)			
JCN.4%:	1(1)			
JCN.5:	5(1)			
JCN.5%:	1(1)			
JCN.5':	3(3)			

JCN.5'%:	1(1)				
JCN.6:	5(1)				
JCN.6%:	1(1)				
JCN.6':	3(3)				
JCN.6'%:	1(1)				
JCN.7:	5(1)				
JCN.7%:	1(1)				
JCN.7':	3(3)				
JCN.7'%:	1(1)				
jcnt!:	5(1)				
Link.00':	6(2)				
Link.01':	6(2)				
Link.02':	7(2)				
Link.03':	7(2)				
Link.04':	8(2)				
Link.05':	9(2)				
Link.06':	10(2)				
Link.07':	11(2)				
Link.08':	12(2)				
Link.09':	13(2)				
Link.10':	14(2)				
Link.11':	15(2)				
Link.12':	16(3)				
Link.13':	17(3)				
Link.14':	18(3)				
Link.15':	19(3)				
Link<BMuxa:	21(1)	29(1)	30(2)		
Link<BMuxa%:	4(1)				
Link<BMuxb:	20(2)	21(1)			
Link<BMuxb%:	4(1)				
Link<CIAInc:	3(1)	30(2)			
LoadCTD':	26(2)	30(1)			
LoadLink':	20(2)	21(2)	30(1)		
LocalBr'a:	29(1)				
LocalBr'a%:	3(1)				
LocalBr'b:	16(1)	17(1)			
LocalBr'b%:	3(1)				
LocalBr'c:	18(1)	19(1)			
LocalBr'c%:	3(1)				
LongJump'a:	8(1)	9(1)	14(1)	15(1)	29(1)
LongJump'a%:	3(1)				
LongJump'b:	10(1)	11(1)	13(1)	16(1)	
LongJump'b%:	3(1)				
LongJump'c:	12(1)	17(1)	18(1)	19(1)	
LongJump'c%:	3(1)				
MemClkEnable'a:	32(1)				
MemClkEnable'b:	32(1)				
MemSH:	32(1)				
MemSH':	32(1)				
MidasBank0':	28(1)	29(8)			
MidasBank1':	28(2)				
MidasBank2':	28(1)	29(2)			
MidasBank3':	28(1)	29(8)			
MidasData':	28(2)				
MidasStrobe':	28(2)				
MMux.00:	28(1)	29(2)			
MMux.01:	28(1)	29(2)			
MMux.02:	28(1)	29(2)			
MMux.03:	28(1)	29(2)			
MMux.04:	28(1)	29(2)			
MMux.05:	28(1)	29(2)			
MMux.06:	28(1)	29(3)			
MMux.07:	28(2)	29(3)			
MulStep:	5(1)	29(1)			
Next.0:	26(1)				
Next.1:	26(1)				
Next.2:	26(1)				
Next.3:	26(1)				
Next=0:	25(1)	29(1)			
NextMacro!:	3(1)				
NoDispatch:	2(1)	12(1)	13(1)	14(1)	15(1) 16(1)
	19(1)				
Overflow':	5(1)				
PEnc.0:	24(1)	25(3)	26(1)		
PEnc.1:	24(1)	25(3)	26(1)		
PEnc.2:	24(1)	25(3)	26(1)		

PEnc.3:	24(1)	25(3)	26(1)
PEnc=CT':	25(1)	29(1)	
PEncGtTrueNext':		25(1)	29(1)
PEncLtTrueNext':		25(1)	29(1)
Phase0:	27(2)	29(1)	31(1)
Phase0':	27(2)	30(1)	
Phase1:	27(2)		
Phase2:	27(2)		
Phase2':	27(1)	30(2)	
Phase3:	27(2)		
Phase3':	5(1)	27(1)	30(3)
Phase4:	27(1)	29(1)	
Phase4':	27(2)	30(2)	
pNext.0:	25(2)	26(2)	29(1)
pNext.1:	25(2)	26(2)	29(1)
pNext.2:	25(2)	26(2)	29(1)
pNext.3:	25(2)	26(2)	29(1)
PrBlock':	1(1)		
preclk0'Aa:	30(1)		
preclk0'Aa%:	31(1)		
preclk0'Ba:	30(1)		
preclk0'Ba%:	31(1)		
preclk0'Ca:	30(1)		
preclk0'Ca%:	31(1)		
preclk0'Cb:	30(1)		
preclk0'Cb%:	31(1)		
preclk0'Da:	30(1)		
preclk0'Da%:	31(1)		
preclk1'Aa:	30(2)		
preclk1'Aa%:	31(1)		
preclk1'Ca:	30(1)		
preclk1'Ca%:	31(1)		
preclk1'Da:	30(1)		
preclk1'Da%:	31(1)		
preclk2'Aa:	30(1)		
preclk2'Aa%:	31(1)		
preclk2'Ba:	30(2)		
preclk2'Ba%:	31(1)		
preclk2'Bb:	27(1)	31(1)	32(1)
preclk2'Bb%:	31(1)		
preclk2'Bc:	31(1)		
preclk2'Bc%:	31(1)		
preclk2'Bd:	30(1)		
preclk2'Bd%:	31(1)		
preclk2'Ca:	30(1)		
preclk2'Ca%:	31(1)		
preclk2'Da:	30(2)		
preclk2'Da%:	31(1)		
preCRamClock:	30(1)		
preCRamClock%:	31(1)		
PreEmpting'!0:	25(1)		
PreEmpting'!1:	22(1)	23(1)	
PreEmpting'!2:	29(1)		
preFH':	31(1)		
preFH%:	31(1)		
prepreclk'a%:	31(2)		
prepreclk'b%:	31(2)		
prepreclk'c%:	31(2)		
prepreclk'd:	31(1)	32(2)	
prepreclk'd%:	31(1)		
prepreclk'e%:	31(2)		
preRunClk'Ba:	30(1)		
preRunClk'Ba%:	31(1)		
preRunClk'Bb:	31(1)		
preRunClk'Bb%:	31(1)		
preRunClk'Bc:	31(1)	32(1)	
preRunClk'Bc%:	31(1)		
preStartCyclea:	27(1)	29(1)	30(1) 31(1)
QBit':	18(1)		
RA.00':	6(2)		
RA.01':	6(2)		
RA.02':	7(2)		
RA.03':	7(2)		
RA.04':	8(2)		
RA.05':	9(2)		
RA.06':	10(2)		

RA.07':	11(2)				
RA.08':	12(2)				
RA.09':	13(2)				
RA.10':	14(2)				
RA.11':	15(2)				
RA.12':	16(2)				
RA.13':	17(2)				
RA.14':	18(2)				
RA.15':	19(2)				
RBMux.04:	8(1)	28(1)			
RBMux.12:	16(1)	26(1)			
RBMux.13:	17(1)	26(1)			
RBMux.14:	18(1)	26(1)			
RBMux.15:	19(1)	26(1)			
rCT:	2(1)	26(8)			
Ready.01:	22(1)	29(1)			
Ready.02:	22(1)	29(1)			
Ready.03:	22(1)	29(1)			
Ready.04:	22(1)	29(1)			
Ready.05:	22(1)	29(1)			
Ready.06:	22(1)	29(1)			
Ready.07:	22(1)	29(1)			
Ready.08:	23(1)	29(1)			
Ready.09:	23(1)	29(1)			
Ready.10:	23(1)	29(1)			
Ready.11:	23(1)	29(1)			
Ready.12:	23(1)	29(1)			
Ready.13:	23(1)	29(1)			
Ready.14:	23(1)	29(1)			
Ready.15:	23(1)	29(1)			
RepeatCur!0:	30(1)				
RepeatCur!1:	25(1)				
RepeatCur!2:	25(1)	30(1)			
RepeatCur':	25(3)				
RepeatCur%:	25(1)				
RepeatCurB:	25(1)	29(1)			
RepeatCurB%:	25(1)				
RepeatCurC:	30(1)				
RepeatCurC%:	25(1)				
RepeatCurD:	30(1)				
RepeatCurD%:	25(1)				
ResEqZero':	5(1)				
ResLtZero':	5(1)				
Return'a!0:	3(1)	12(1)	17(1)	20(1)	
Return'a!1:	3(1)				
Return'a!2:	3(1)	29(1)			
Return'b!0:	10(1)	11(1)	13(1)		
Return'b!1:	3(1)				
Return'b!2:	16(1)	18(1)			
Return'c!0:	8(1)	9(1)	14(1)		
Return'c!1:	3(1)				
Return'c!2:	15(1)	19(1)			
RIM':	3(1)	20(2)	21(2)	29(1)	30(1)
RIMorRTPCdly:	3(1)	20(2)	21(2)	29(1)	
rMIRa:	2(1)				
RmLtZero':	5(1)				
RmOdd':	5(1)				
rStop:	2(1)	31(4)	32(1)		
RTPC':	3(1)	29(1)	30(1)		
Run':	31(1)				
RunClk'a:	31(1)				
RunClk'a%:	30(1)				
RunClk'b:	31(1)				
RunClk'b%:	30(1)				
RunRefresh:	32(3)				
RunRefresh':	32(1)				
RWTPC':	3(1)	30(1)			
RWTPCorRWIM:	3(1)	27(1)	29(1)		
sBLOCK:	1(2)	2(1)			
SC&NoFreeze:	26(1)	27(1)			
SC&NoFreeze':	26(1)	27(1)			
SCorFreezea:	5(1)	30(1)			
SCorFreezeb:	30(2)				
sCTask.0:	6(1)	26(1)			
sCTask.1:	6(1)	26(1)			
sCTask.2:	7(1)	26(1)			

sCTask.3:	7(1)	26(1)		
sCTD.0:	8(1)	26(1)		
sCTD.1:	9(1)	26(1)		
sCTD.2:	10(1)	26(1)		
sCTD.3:	11(1)	26(1)		
SetReady.01:	22(3)			
SetReady.02:	22(3)			
SetReady.03:	22(3)			
SetReady.04:	22(3)			
SetReady.05:	22(3)			
SetReady.06:	22(3)			
SetReady.07:	22(3)			
SetReady.08:	23(3)			
SetReady.09:	23(3)			
SetReady.10:	23(3)			
SetReady.11:	23(3)			
SetReady.12:	23(3)			
SetReady.13:	23(3)			
SetReady.14:	23(3)			
SetReady.15:	23(3)			
SetRun:	28(1)	31(1)		
SetRun':	28(1)	31(1)		
SetRunRfsh:	32(1)			
SetSS':	31(1)			
sFF.0:	1(1)	2(1)		
sFF.1:	1(1)	2(1)		
sFF.2:	1(1)	2(1)		
sFF.3:	1(1)	2(1)		
sFF.4:	1(1)	2(1)		
sFF.5:	1(1)	2(1)		
sFF.6:	1(1)	2(1)		
sFF.7:	1(1)	2(1)		
sIMRH:	1(1)	2(1)		
sJCN.0:	1(1)	2(1)		
sJCN.1:	1(1)	2(1)		
sJCN.2:	1(2)	2(1)		
sJCN.3:	1(2)	2(1)		
sJCN.4:	1(1)	2(1)		
sJCN.5:	1(1)	2(1)		
sJCN.6:	1(1)	2(1)		
sJCN.7:	1(1)	2(1)		
sPhase0:	27(7)			
StartCycle:	26(4)	27(2)		
StartCycle':	26(4)	27(1)	31(1)	
StartCycle'a!:	27(1)			
Stop:	29(1)	31(1)		
StopAtT1:	2(1)	31(1)		
StopAtT1':	2(1)	27(1)		
StopMIRClk:	30(1)			
StopRunClock:	31(1)	32(3)		
StopTasks:	4(1)	25(3)	29(1)	
StopTasks':	4(1)			
SWb:	25(1)			
Switch'a:	4(1)	25(1)		
Switch'a%:	25(1)			
Switch'b:	22(1)	23(1)	25(1)	
Switcha:	26(1)			
Switcha%:	25(1)			
Switchb:	20(2)	21(2)	25(1)	
SwitchDown:	25(1)	30(1)		
SwitchUp:	25(3)			
SwitchUp%:	25(1)			
SwitchUp':	30(1)			
SwitchUp' %:	25(1)			
SWm:	5(1)	25(1)		
TaskingIsOff':	4(1)			
TLinkAd.0:	5(1)	20(2)	21(2)	26(1)
TLinkAd.1:	5(1)	20(2)	21(2)	26(1)
TLinkAd.2:	5(1)	20(2)	21(2)	26(1)
TLinkAd.3:	5(1)	20(2)	21(2)	26(1)
TLinkEn:	20(2)	21(2)	30(1)	
TLinkEn':	5(2)	20(2)	21(2)	30(1)
TNIA.00:	6(1)			
TNIA.01:	6(1)			
TNIA.02!0:	7(1)			
TNIA.02!1:	7(1)			

TNIA.02!2:	7(1)		
TNIA.03!0:	7(1)		
TNIA.03!1:	7(1)		
TNIA.03!2:	7(1)		
TNIA.04!0:	8(1)		
TNIA.04!1:	8(1)		
TNIA.04!2:	8(1)		
TNIA.05!0:	9(1)		
TNIA.05!1:	9(1)		
TNIA.05!2:	9(1)		
TNIA.06!0:	10(1)		
TNIA.06!1:	10(1)		
TNIA.06!2:	10(1)		
TNIA.07!0:	11(1)		
TNIA.07!1:	11(1)		
TNIA.07!2:	11(1)		
TNIA.08!0:	12(1)		
TNIA.08!1:	12(1)		
TNIA.08!2:	12(1)		
TNIA.09!0:	13(1)		
TNIA.09!1:	13(1)		
TNIA.09!2:	13(1)		
TNIA.10!0:	14(1)		
TNIA.10!1:	14(1)		
TNIA.10!2:	14(1)		
TNIA.11!0:	15(1)		
TNIA.11!1:	15(1)		
TNIA.11!2:	15(1)		
TNIA.12!0:	16(1)		
TNIA.12!1:	16(1)		
TNIA.12!2:	16(1)		
TNIA.13!0:	17(1)		
TNIA.13!1:	17(1)		
TNIA.13!2:	17(1)		
TNIA.14!0:	18(1)		
TNIA.14!1:	18(1)		
TNIA.14!2:	18(1)		
TNIA.15!0:	19(1)		
TNIA.15!1:	19(1)		
TNIA.15!2:	19(1)		
ToPE.01:	22(1)	24(1)	29(1)
ToPE.02:	22(1)	24(1)	29(1)
ToPE.03:	22(1)	24(2)	29(1)
ToPE.03':	24(2)		
ToPE.04:	22(1)	24(1)	29(1)
ToPE.05:	22(1)	24(2)	29(1)
ToPE.05':	24(2)		
ToPE.06:	22(1)	24(2)	29(1)
ToPE.07:	22(1)	24(3)	29(1)
ToPE.07':	24(2)		
ToPE.08:	23(1)	24(1)	29(1)
ToPE.09:	23(1)	24(2)	29(1)
ToPE.09':	24(2)		
ToPE.10:	23(1)	24(2)	29(1)
ToPE.11:	23(1)	24(3)	29(1)
ToPE.11':	24(2)		
ToPE.12:	23(1)	24(4)	29(1)
ToPE.13:	23(1)	24(3)	29(1)
ToPE.13':	24(2)		
ToPE.14:	23(1)	24(4)	29(1)
ToPE.15:	23(1)	24(3)	29(1)
ToPE.15':	24(2)		
ToTNIA13-15':	5(1)	17(1)	18(1) 19(1)
ToTNIA14':	5(1)	18(1)	
ToTNIA8-12'a:	5(1)	12(1)	13(1) 14(1)
ToTNIA8-12'b:	5(1)	15(1)	16(1)
TPC.00:	6(2)		
TPC.01:	6(2)		
TPC.02:	7(2)		
TPC.03:	7(2)		
TPC.04:	8(2)		
TPC.05:	9(2)		
TPC.06:	10(2)		
TPC.07:	11(2)		
TPC.08:	12(2)		
TPC.09:	13(2)		

TPC.10:	14(2)				
TPC.11:	15(2)				
TPC.12:	16(2)				
TPC.13:	17(2)				
TPC.14:	18(2)				
TPC.15:	19(2)				
TPCAd.0':	20(2)	21(2)			
TPCAd.0'%:	26(1)				
TPCAd.1':	20(2)	21(2)			
TPCAd.1'%:	26(1)				
TPCAd.2':	20(2)	21(2)			
TPCAd.2'%:	26(1)				
TPCAd.3':	20(2)	21(2)			
TPCAd.3'%:	26(1)				
TPCBypass:	25(1)	29(1)			
TPCBypass':	20(2)	21(2)	25(1)		
TPCI.00:	6(1)				
TPCI.01:	6(1)				
TPCI.02:	7(1)				
TPCI.03:	7(1)				
TPCI.04:	8(1)				
TPCI.05:	9(1)				
TPCI.06:	10(1)				
TPCI.07:	11(1)				
TPCI.08:	12(1)				
TPCI.09:	13(1)				
TPCI.10:	14(1)				
TPCI.11:	15(1)				
TPCI.12:	16(1)				
TPCI.13:	17(1)				
TPCI.14:	18(1)				
TPCI.15:	19(1)				
TPCIc1k'a:	20(1)				
TPCIc1k'a%:	30(1)				
TPCIc1k'b:	21(1)				
TPCIc1k'b%:	30(1)				
TPCIc1k'c:	20(1)				
TPCIc1k'c%:	30(1)				
TPCO.00:	6(1)				
TPCO.01:	6(1)				
TPCO.02:	7(1)				
TPCO.03:	7(1)				
TPCO.04:	8(1)				
TPCO.05:	9(1)				
TPCO.06:	10(1)				
TPCO.07:	11(1)				
TPCO.08:	12(1)				
TPCO.09:	13(1)				
TPCO.10:	14(1)				
TPCO.11:	15(1)				
TPCO.12:	16(1)				
TPCO.13:	17(1)				
TPCO.14:	18(1)				
TPCO.15:	19(1)				
TPIMc1k'a:	20(1)				
TPIMc1k'a%:	30(1)				
TPIMc1k'b:	21(1)				
TPIMc1k'b%:	30(1)				
TPIMc1k'c:	20(1)	21(1)			
TPIMc1k'c%:	30(1)				
TrueAC:	5(1)	20(2)	21(3)	30(1)	
TrueBD:	14(1)	15(1)	20(4)	21(3)	28(1) 30(2)
TWReq.01:	22(1)				
TWReq.02:	22(1)				
TWReq.03:	22(1)				
TWReq.04:	22(1)				
TWReq.05:	22(1)				
TWReq.06:	22(1)				
TWReq.07:	22(1)				
TWReq.08:	23(1)				
TWReq.09:	23(1)				
TWReq.10:	23(1)				
TWReq.11:	23(1)				
TWReq.12:	23(1)				
TWReq.13:	23(1)				
TWReq.14:	23(1)				

TWReq.15:	23(1)			
UseCPReg:	4(1)	20(2)	21(2)	
UseDMD!:	28(1)			
WantIfuHold':	4(1)			
WantRunRfsh:	32(3)			
Whatever:	32(13)			
WIM':	3(1)	29(1)	30(1)	
WriteTLink'a:	20(2)			
WriteTLink'a%:	30(1)			
WriteTLink'b:	21(1)			
WriteTLink'b%:	30(1)			
WriteTLink'c:	21(1)			
WriteTLink'c%:	30(1)			
WriteTPC'a:	20(1)			
WriteTPC'a%:	30(1)			
WriteTPC'b:	21(1)			
WriteTPC'b%:	30(1)			
WriteTPC'c:	20(1)	21(1)		
WriteTPC'c%:	30(1)			
WTPC':	3(1)	5(1)	29(1)	30(2)
←Dbuf:	4(1)			
←Map:	4(1)			