DORADO SCHEMATICS

Hi Byte

PROCESSOR

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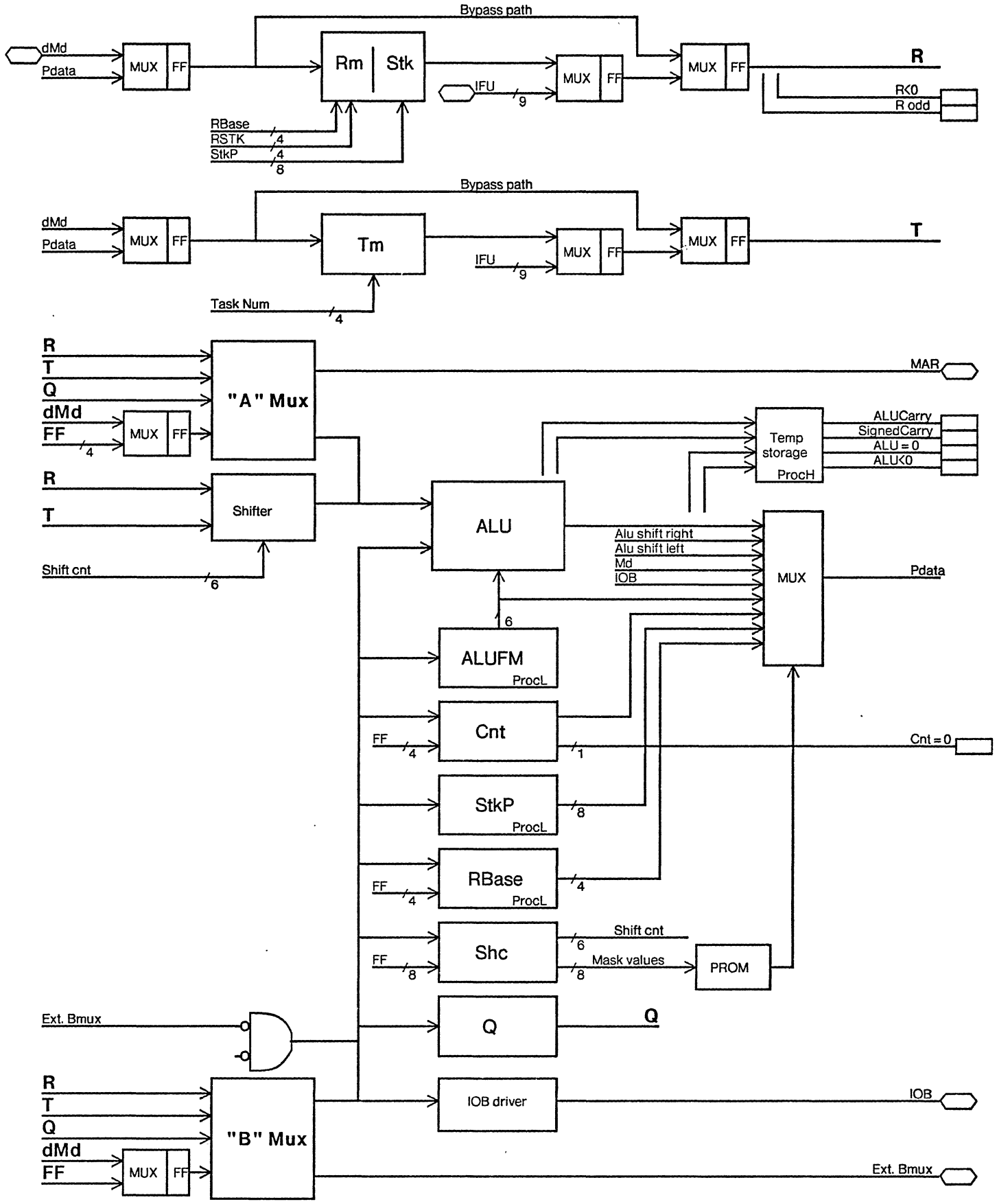
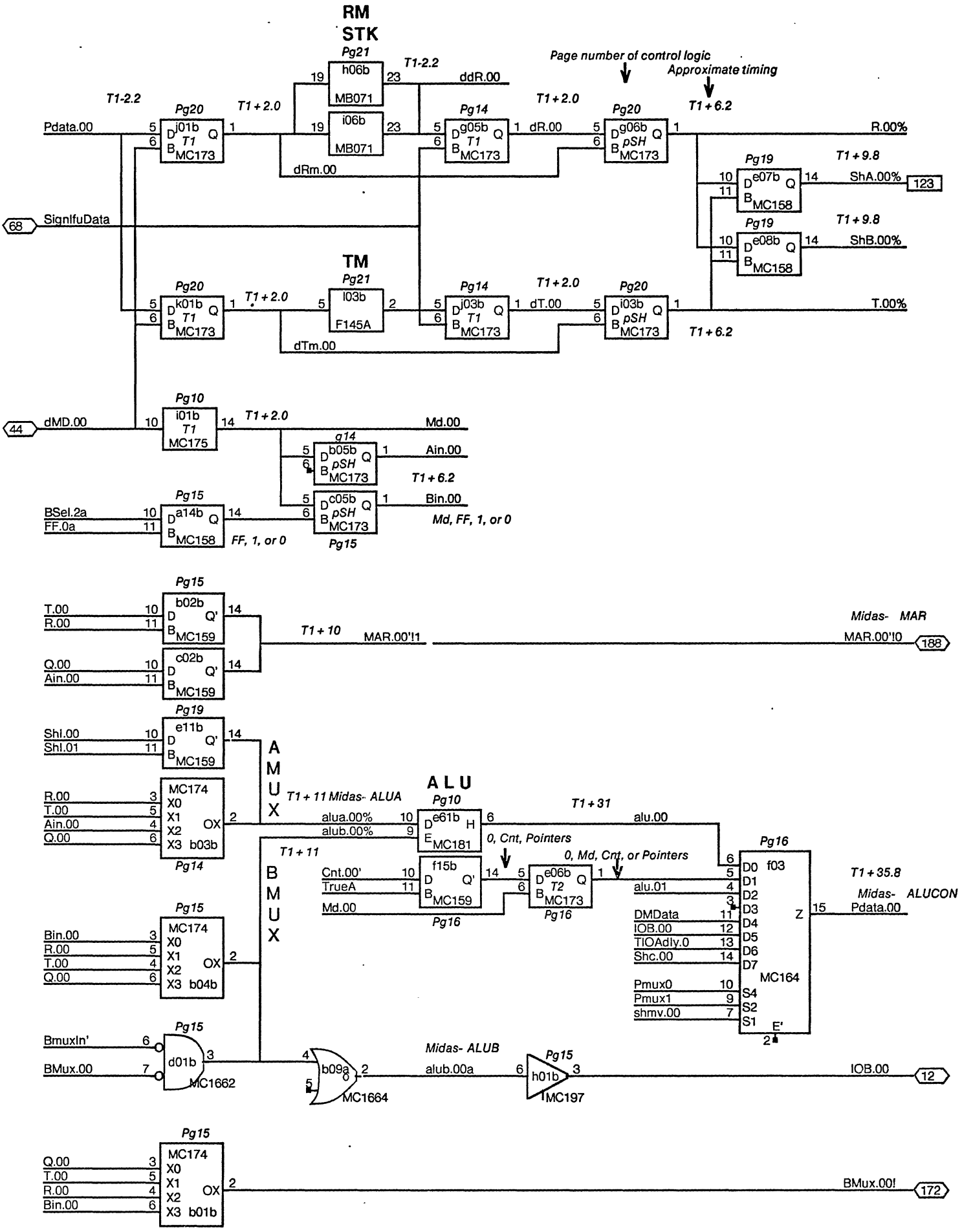
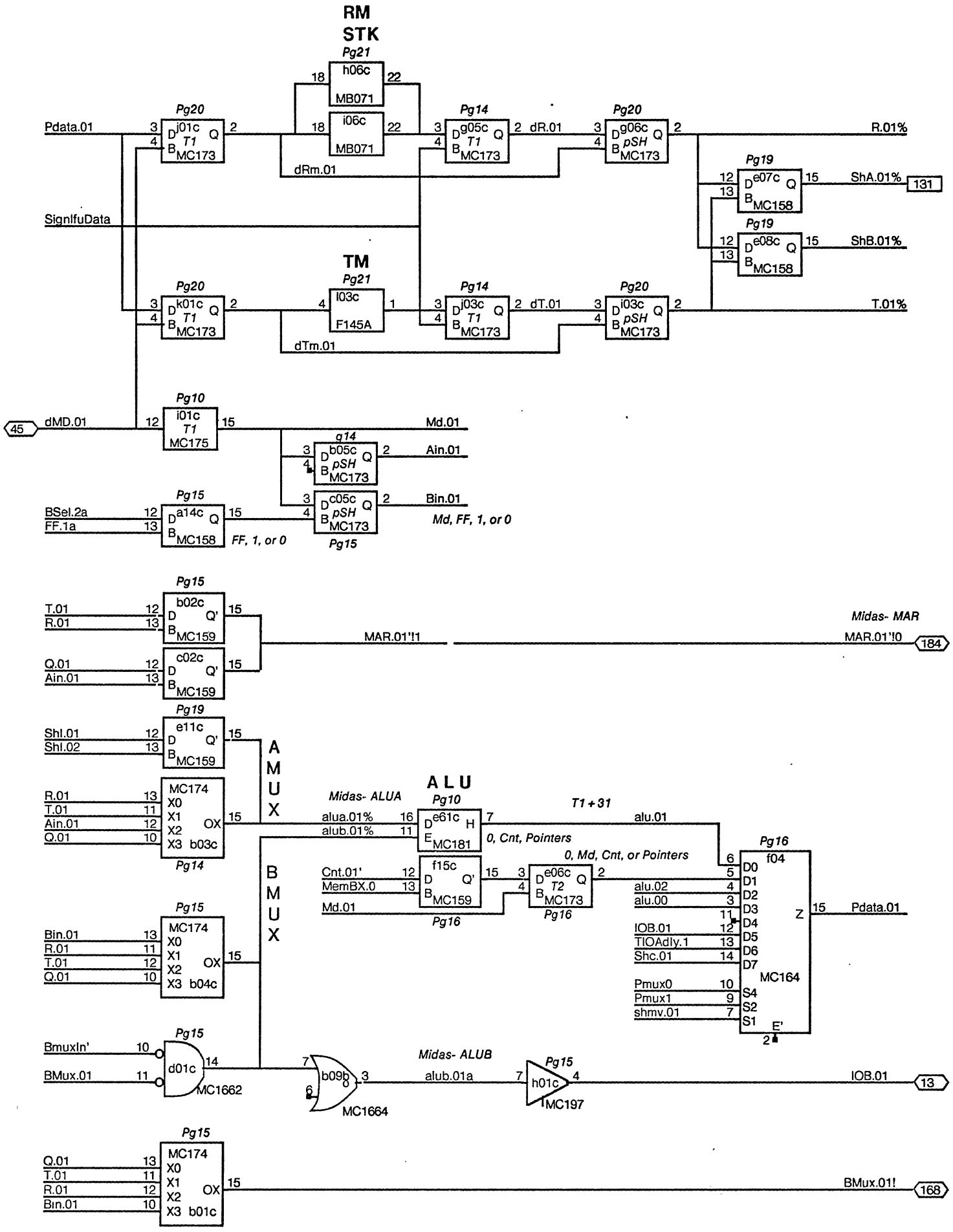


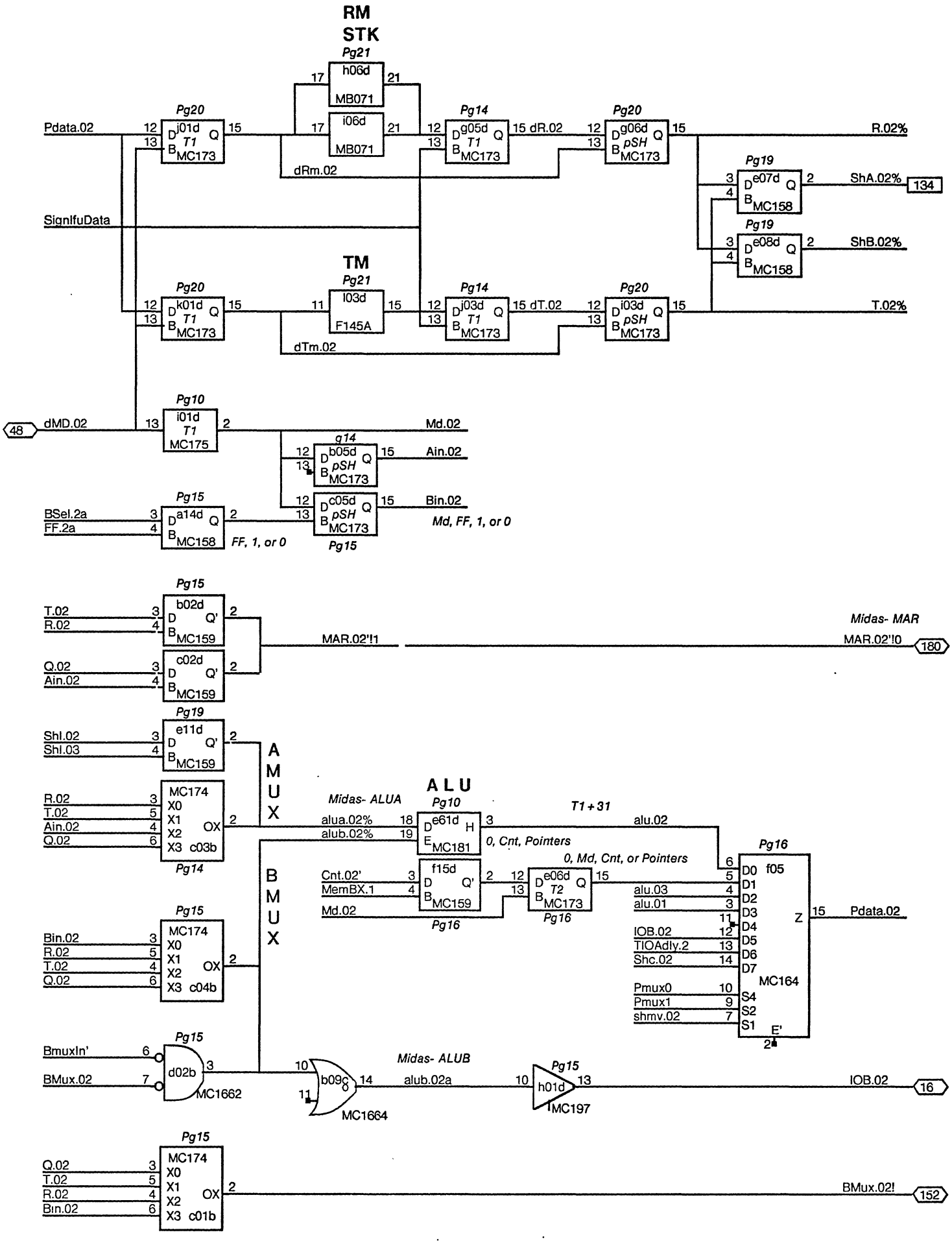
XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Block Diagram	ProcH01.sil	R Bates	Ce	11/15/78	01



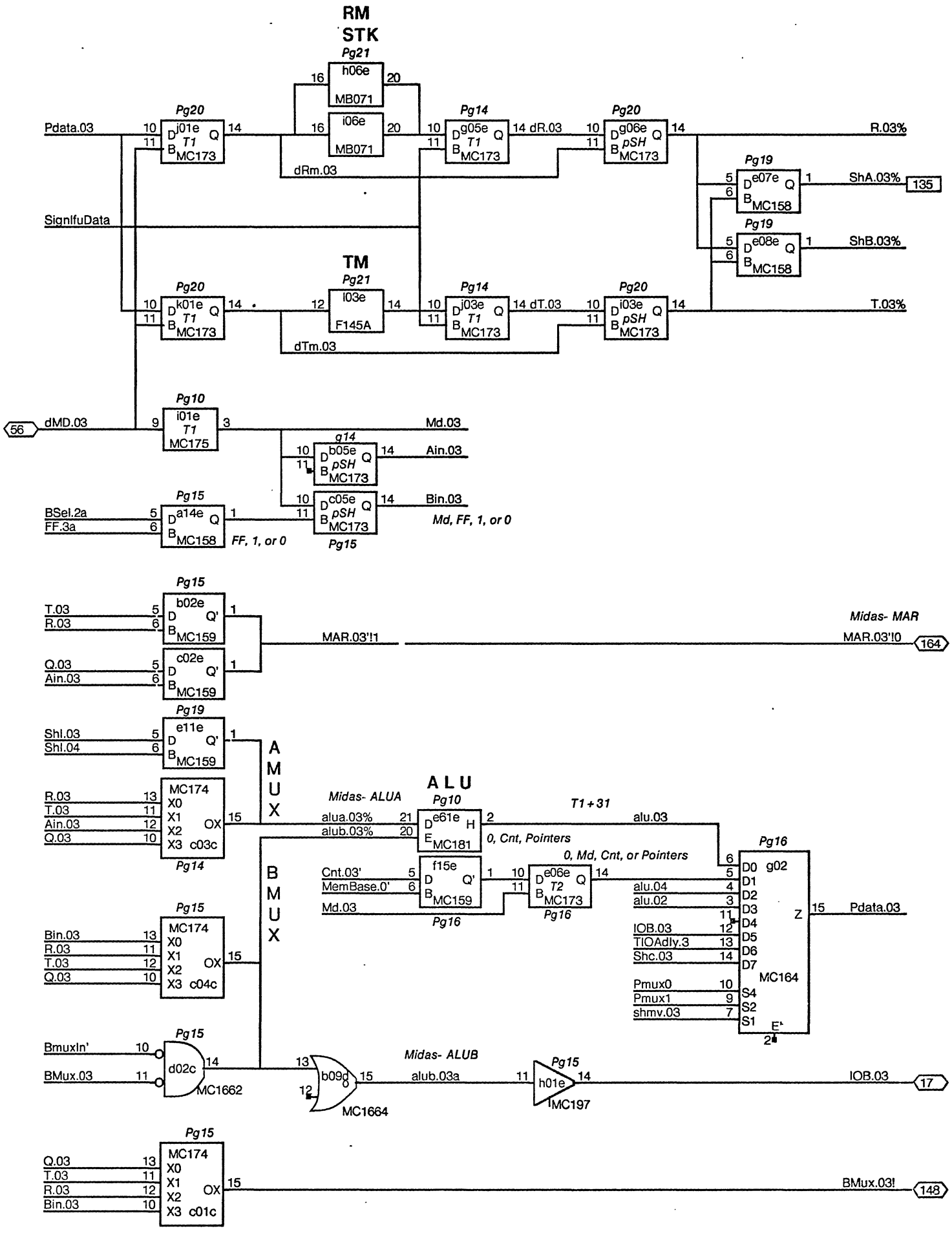
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 00	ProcH02.sil	R Bates	Ce	6/18/79	02



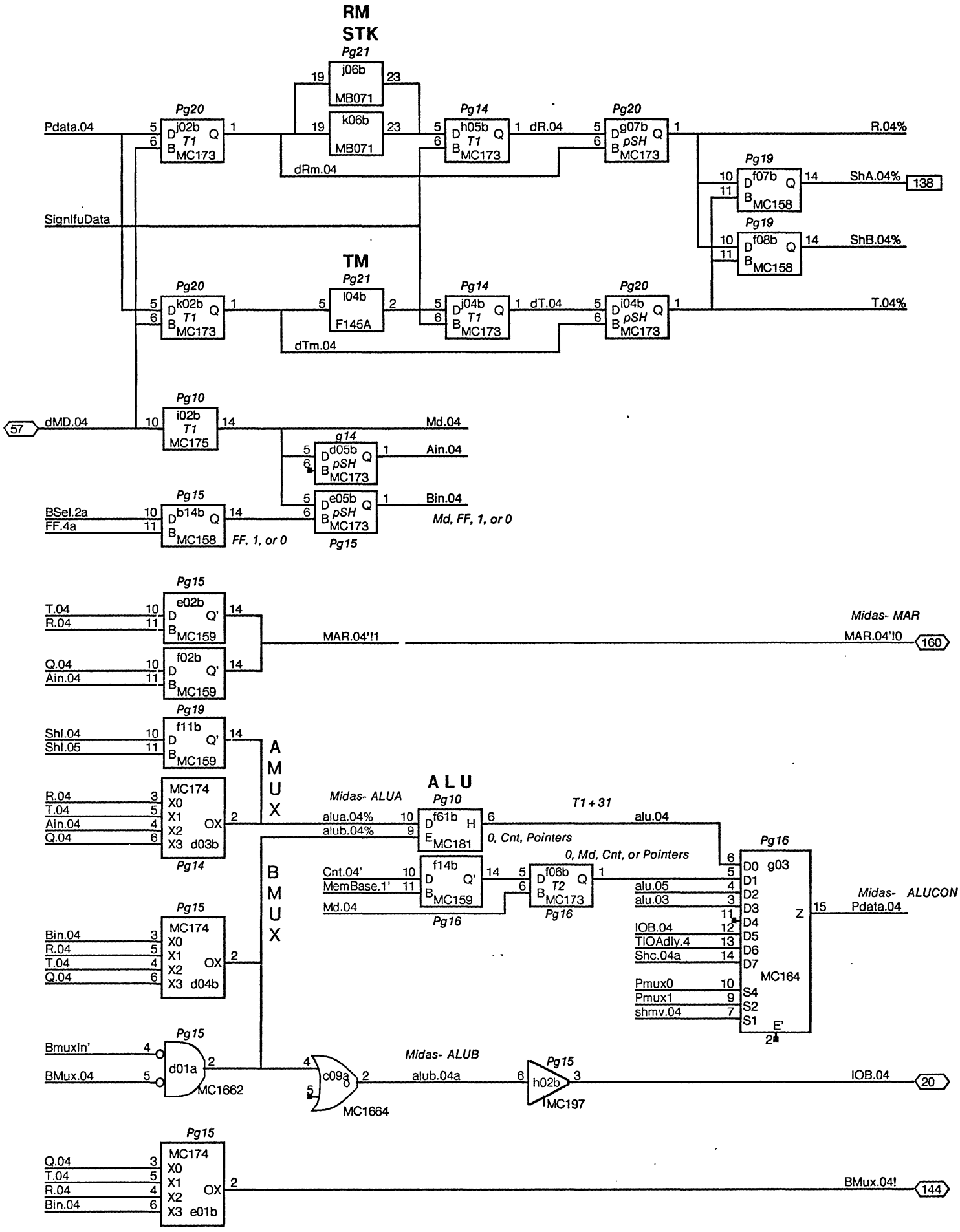
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 01	ProcH03.sil	R Bates	Ce	6/18/79	03



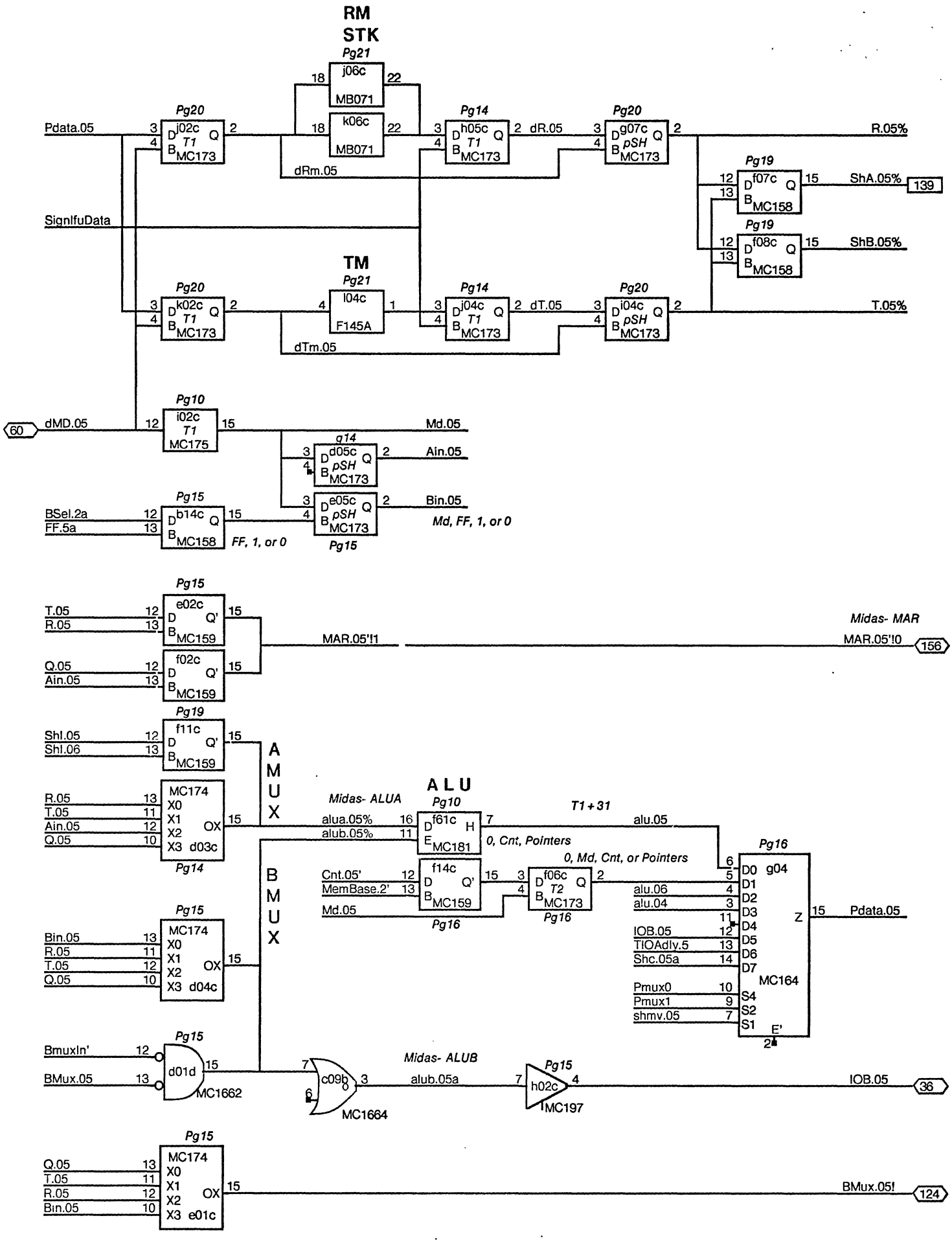
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 02	ProcH04.sil	R Bates	Ce	6/19/79	04



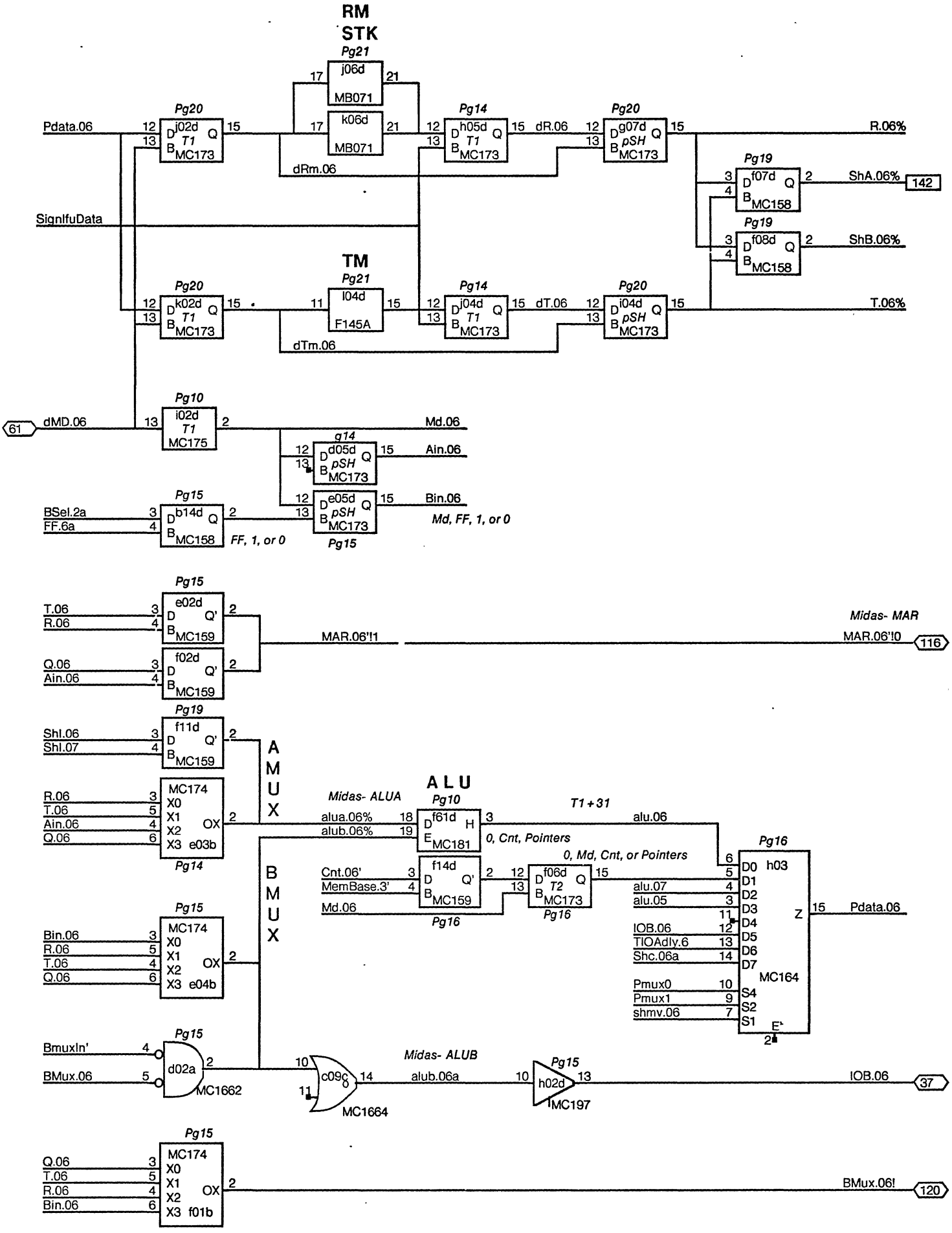
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 03	ProcH05.sil	R Bates	Ce	6/19/79	05



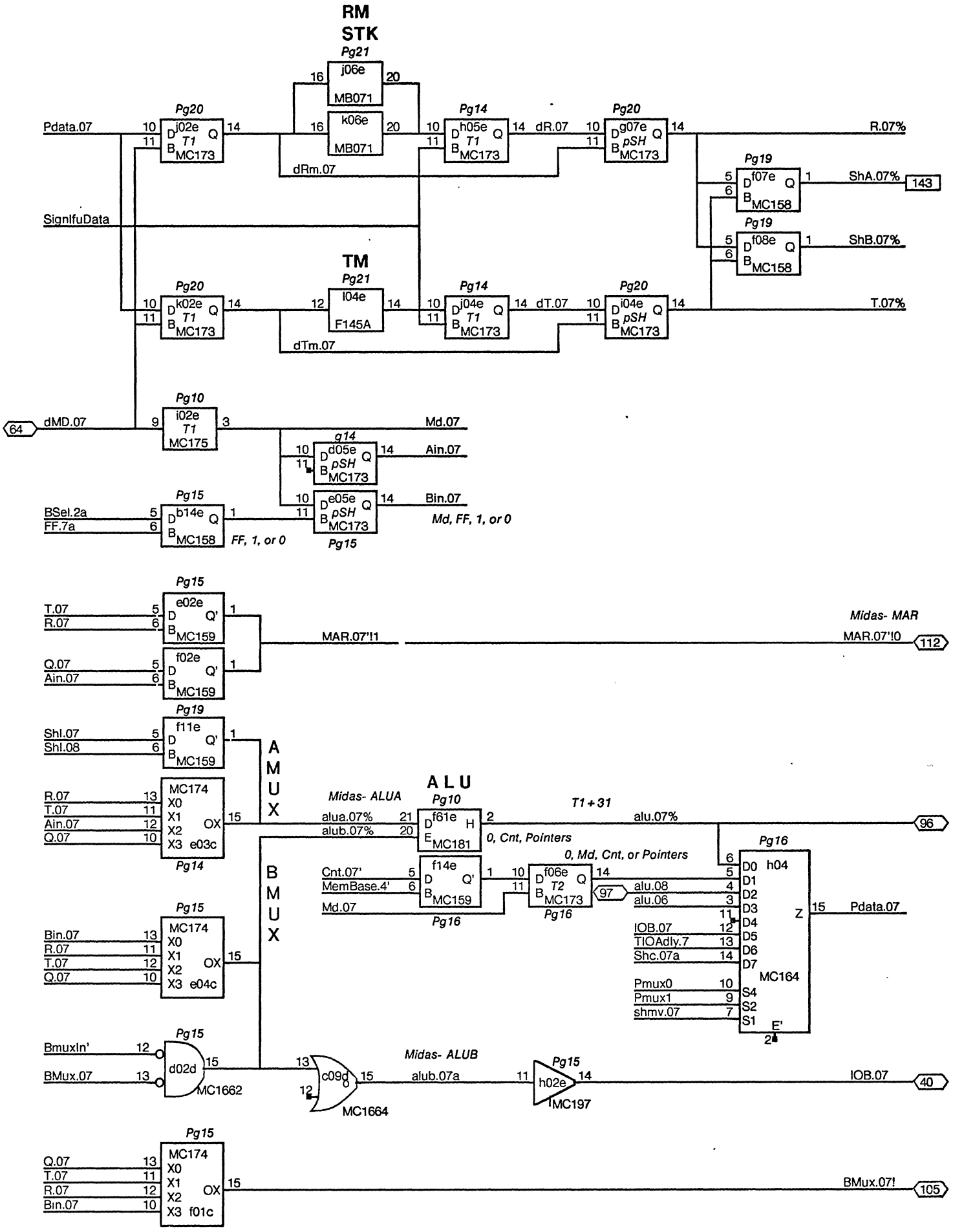
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 04	ProcH06.sil	R Bates	Ce	6/19/79	06



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 05	ProcH07.sil	R Bates	Ce	6/19/79	07



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 06	ProcH08.sil	R Bates	Ce	6/19/79	08



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	BIT SLICE 07	ProcH09.sil	R Bates	Ce	6/19/79	09

ALU delays

Logical function to output = 11.9

Arithmetic operation to data = 20.0

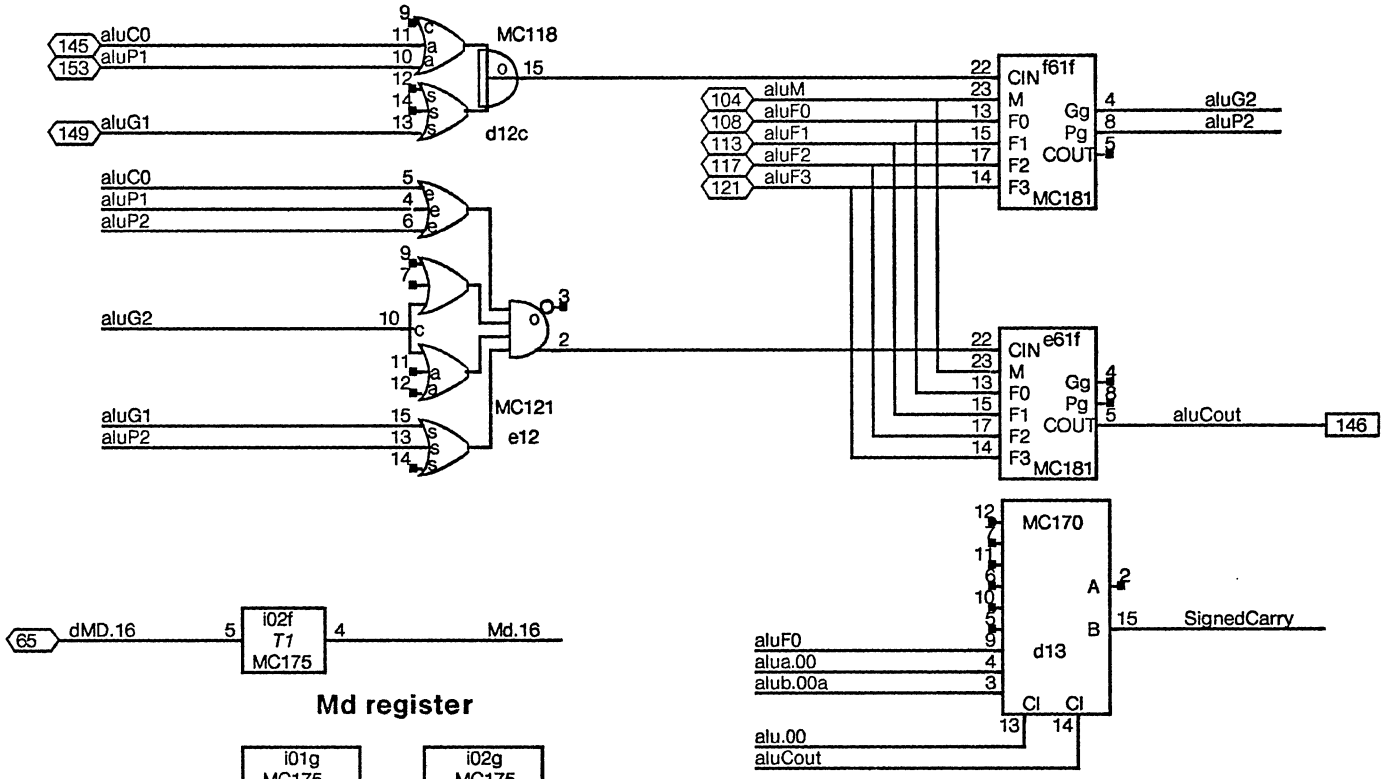
Arithmetic operation to carry = 17.9

ALU output *(assuming 10.2 ns to output of BMux)*

Logical Function = 22.0

Arithmetic operation to data = 30.1

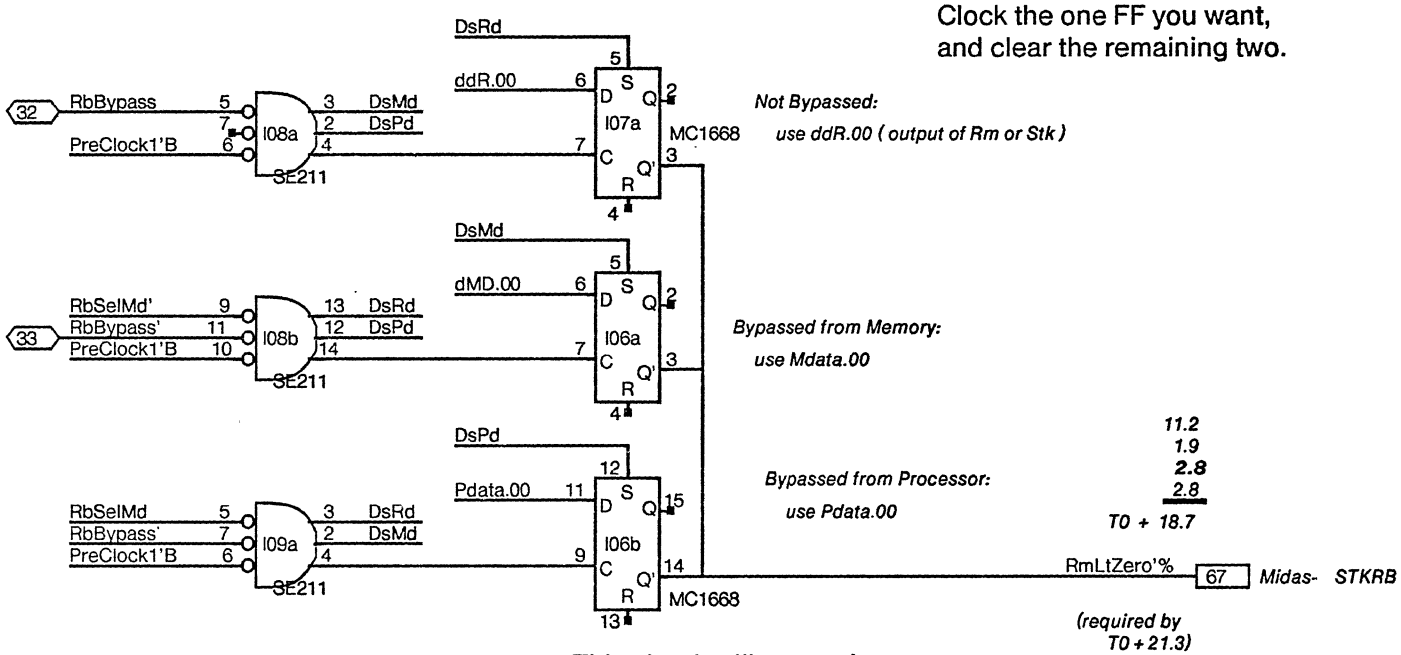
Arithmetic operation to carry = 28.0



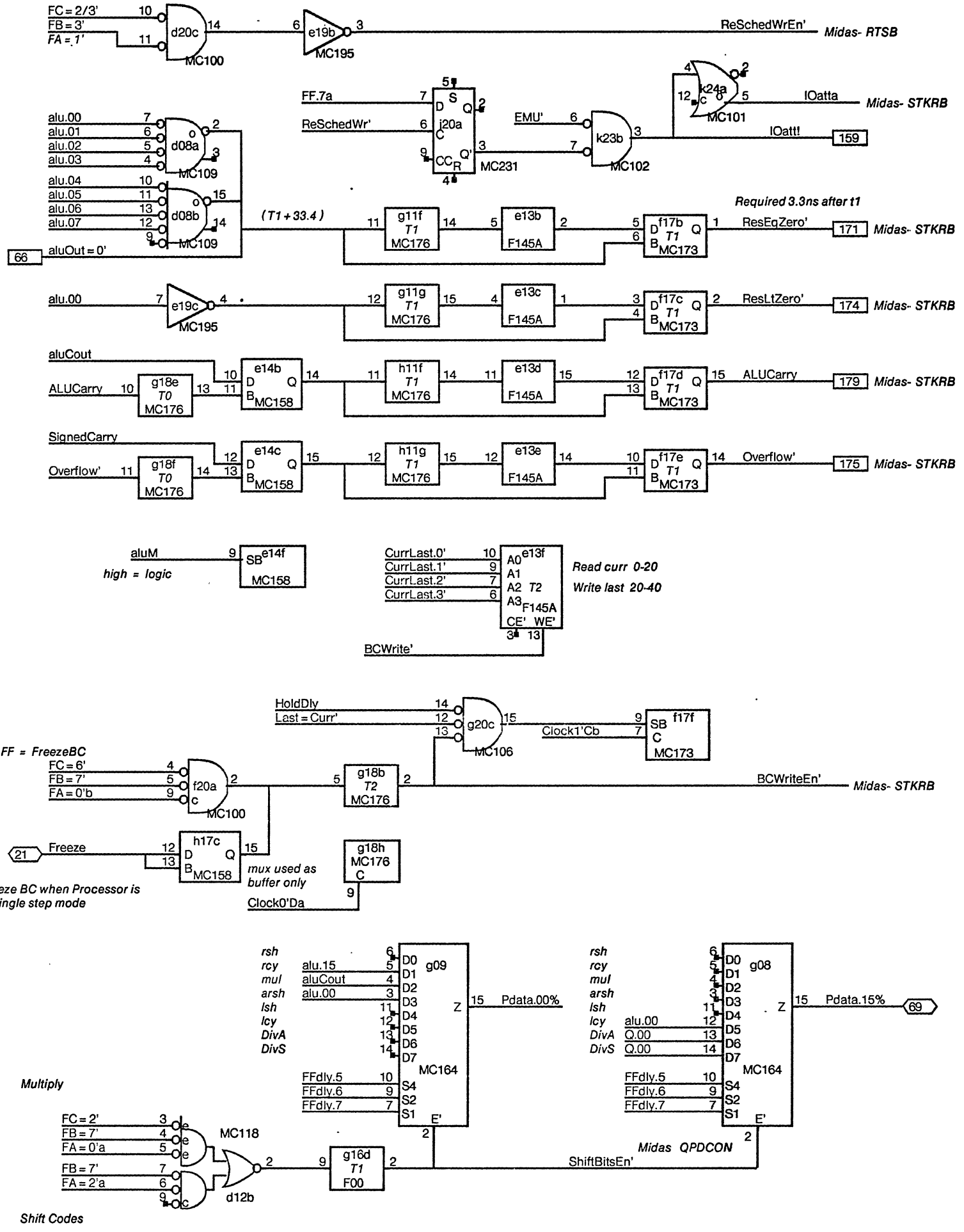
Md register

Fast Branch on Rm < 0

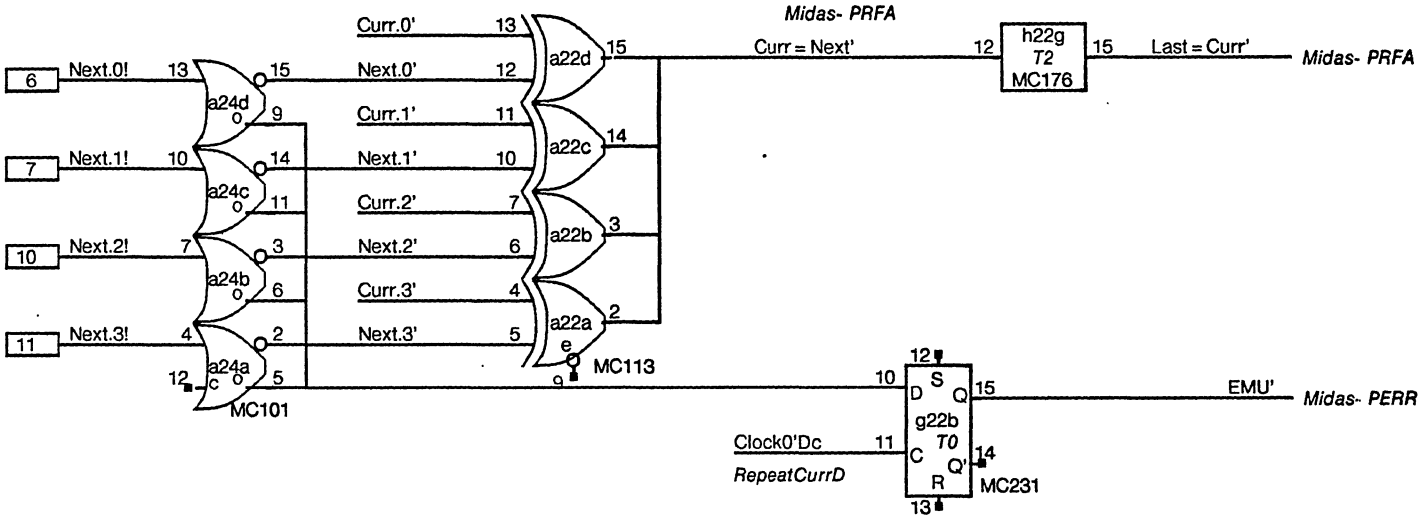
Clock the one FF you want, and clear the remaining two.

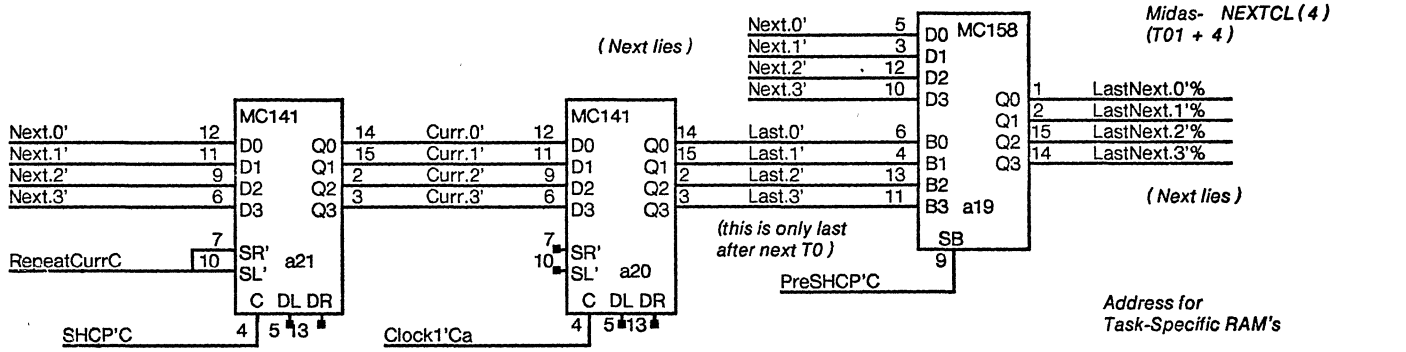


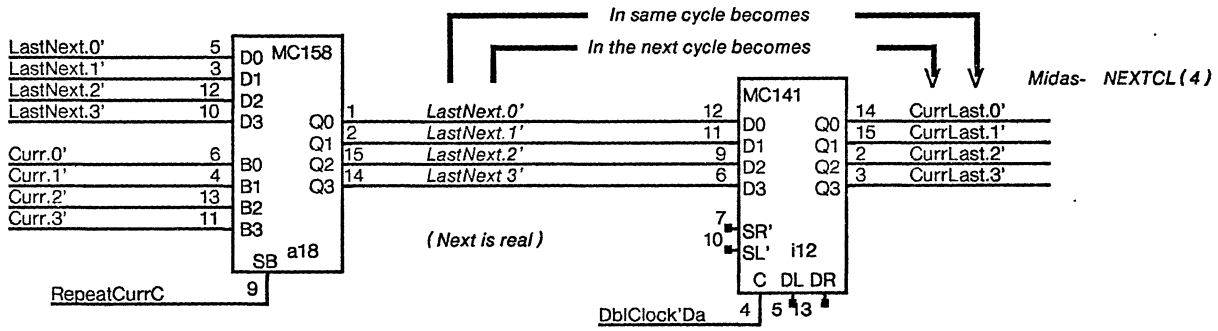
This circuit will correctly bypass R from Pdata or Mdata When "RIsIfData" is in effect, the fast branch will be based on the contents of the addressed RM or STK, bypassed if necessary.



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	L/R ALU shift bits Branch Condition Ram	ProcH11.sil	R. Bates	Ce	6/18/79	11



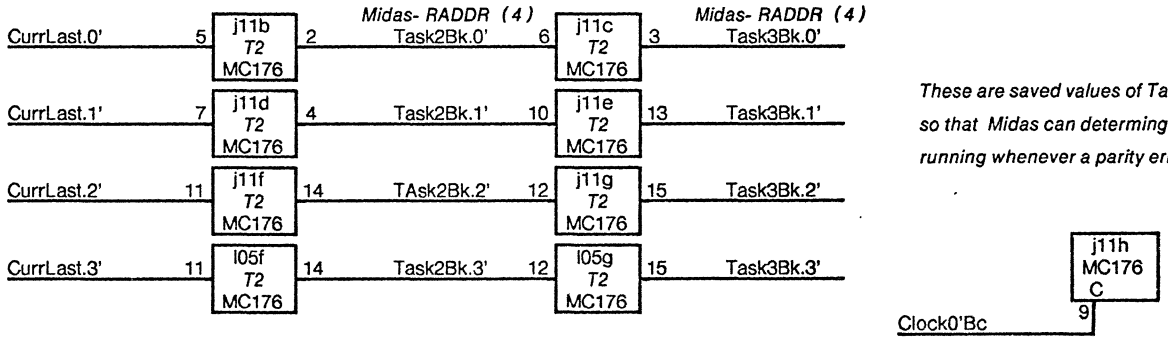




"RepeatCurrent" is asserted on certain occasions when the value on the NEXT bus may be invalid ("Next Lies") due to the combination of Block and Hold.

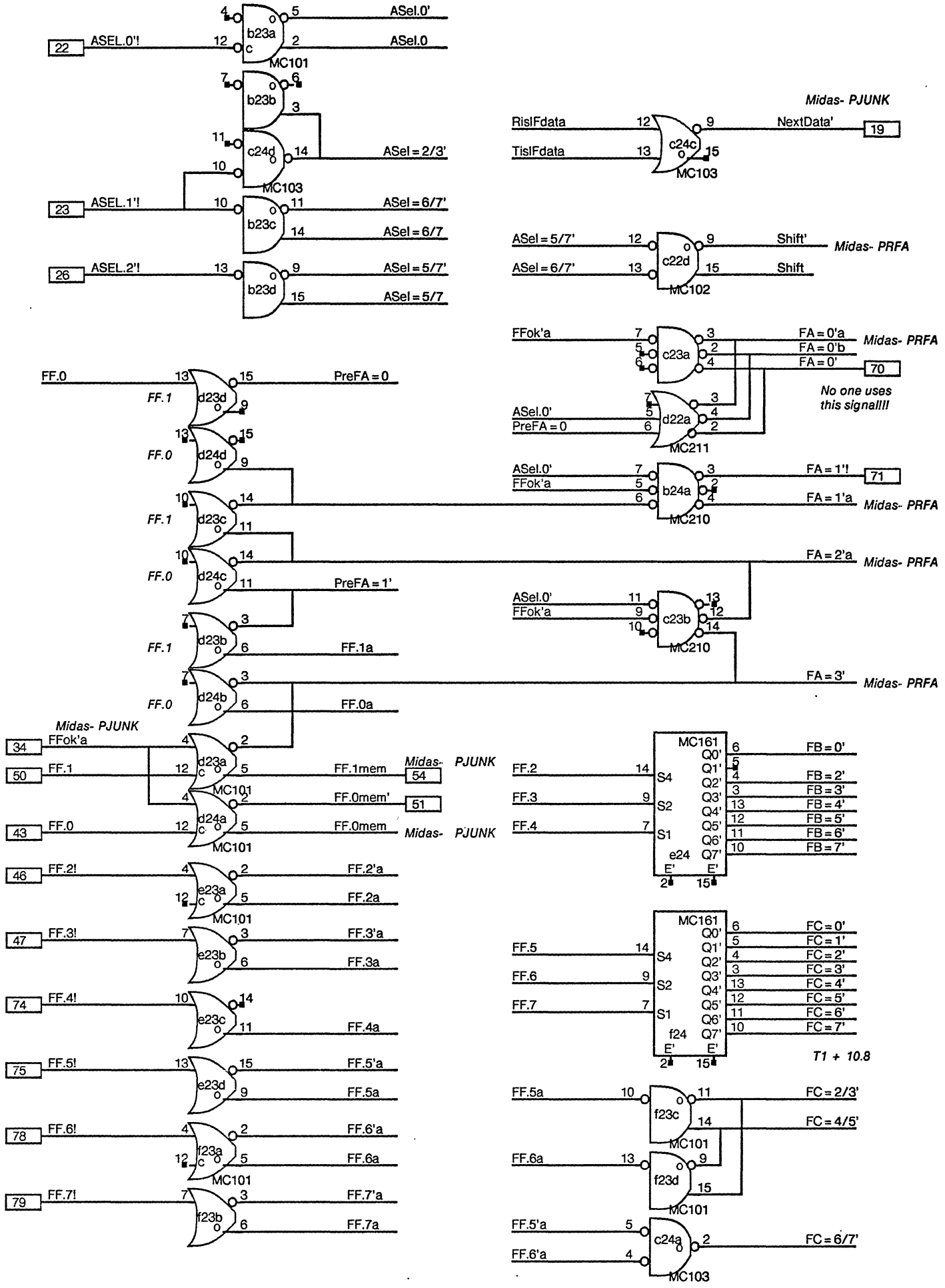
Task number tracking logic

Task number tracking logic (for Midas)



These are saved values of Task number so that Midas can determing the task running whenever a parity error occurs

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Task logic	ProcH12.sil	R. Bates	Ce	7/08/79	12



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Function Field Decoding	ProcH13.sil	R Bates	Ce	6/18/79	13

AMux decoding

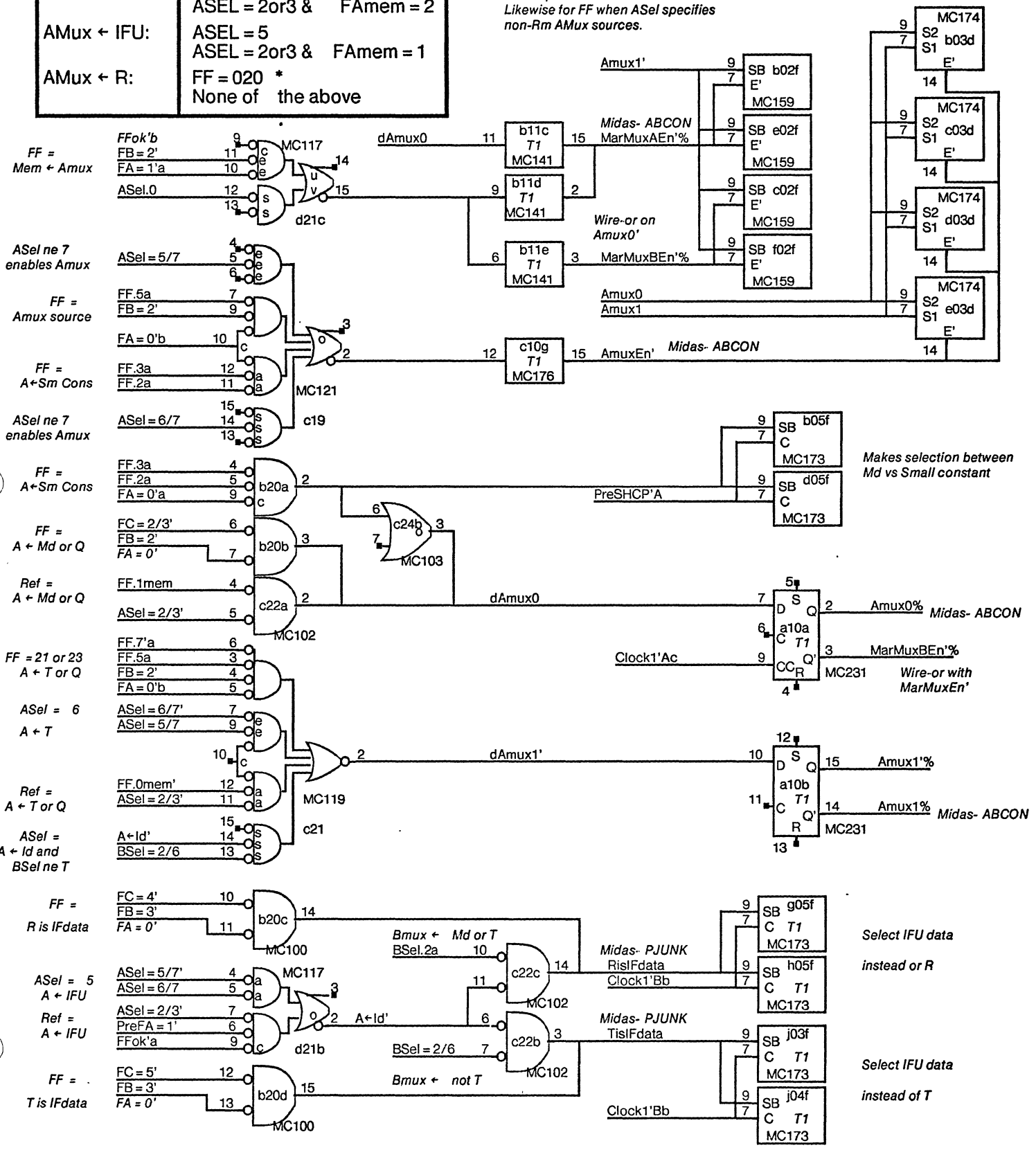
AMux ← FF:	FF = 0-17 *
AMux ← T:	FF = 021 * ASEL = 2or3 & FAmem = 3 ASEL = 6
AMux ← Md:	FF = 022 * ASEL = 2or3 & FAmem = 0
AMux ← Q:	FF = 023 * ASEL = 2or3 & FAmem = 2
AMux ← IFU:	ASEL = 5 ASEL = 2or3 & FAmem = 1
AMux ← R:	FF = 020 * None of the above

* The Amux is disabled by ASEL = 7 unless one of these codes are in effect

NOTE: ASel selects and FF selects for the AMux are "OR'd" by this hardware. Thus ASel codes selecting non-Rm sources of Amux must not be used when an FF specifies an ASel source. Likewise for FF when ASel specifies non-Rm AMux sources.

AMux encoding

Mux Input	Source
0	R or IFU data
1	T or IFU data
2	Md or Small Const.
3	Q



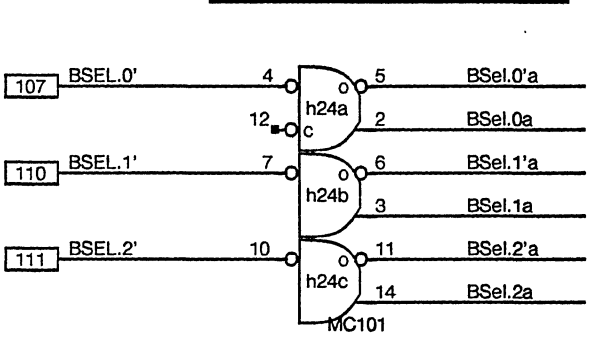
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"A" Multiplexor Control	ProcH14.sil	R. Bates	Ce	6/18/79	14

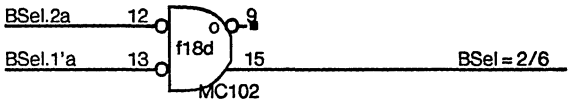
BSEL field decoding

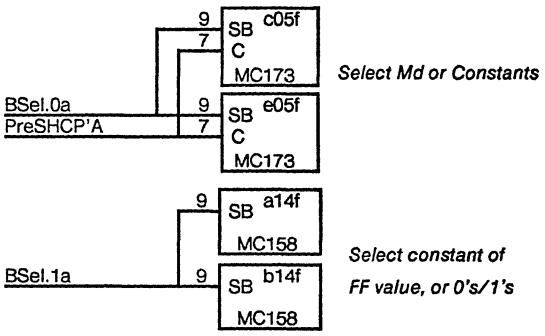
BSEL	INTERNAL	EXTERNAL
0	Md	--
1	R	--
2	T	Hold←B
3	Q	Q ← B
4	0,,FF	--
5	377,FF	--
6	FF,,0	--
7	FF,,377	--

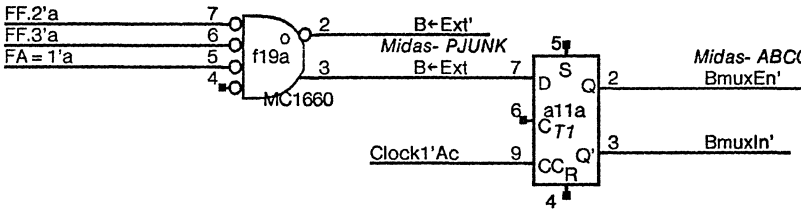
BMux encoding

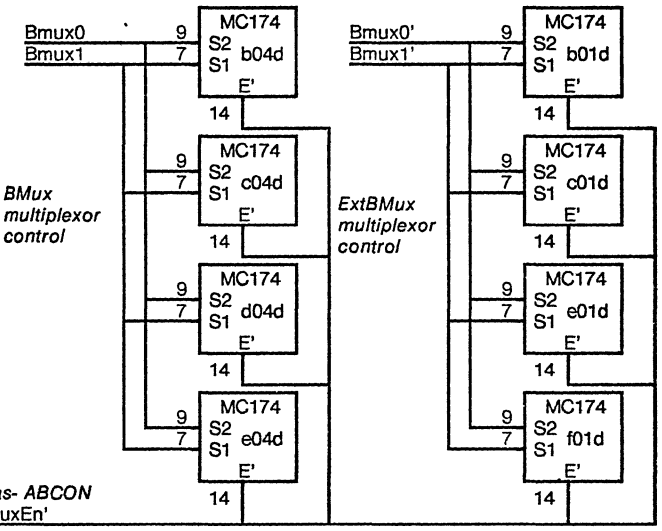
BMux	
0	Md or Constant
1	R
2	T
3	Q

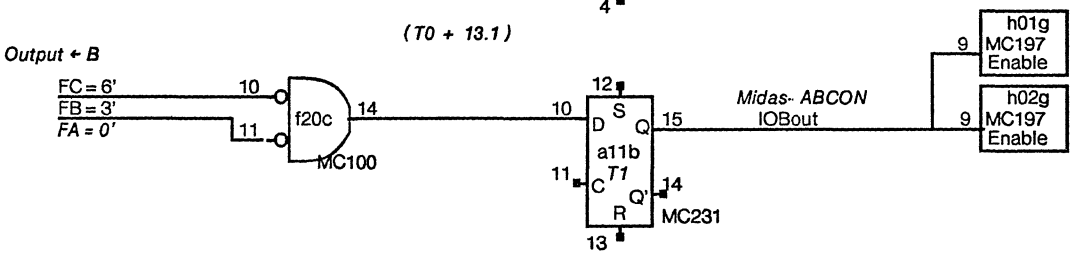


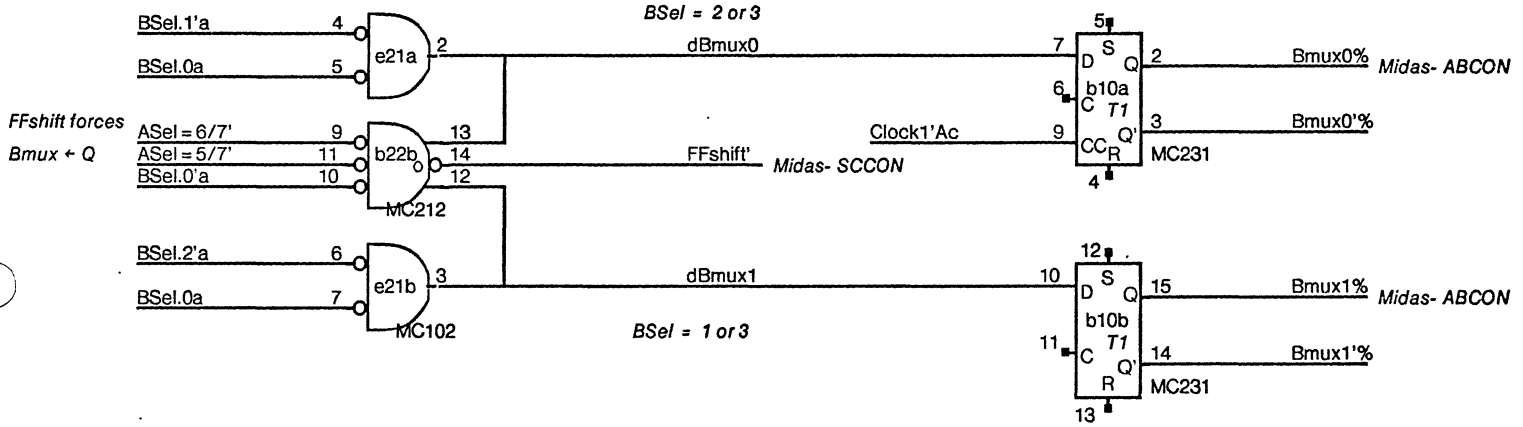




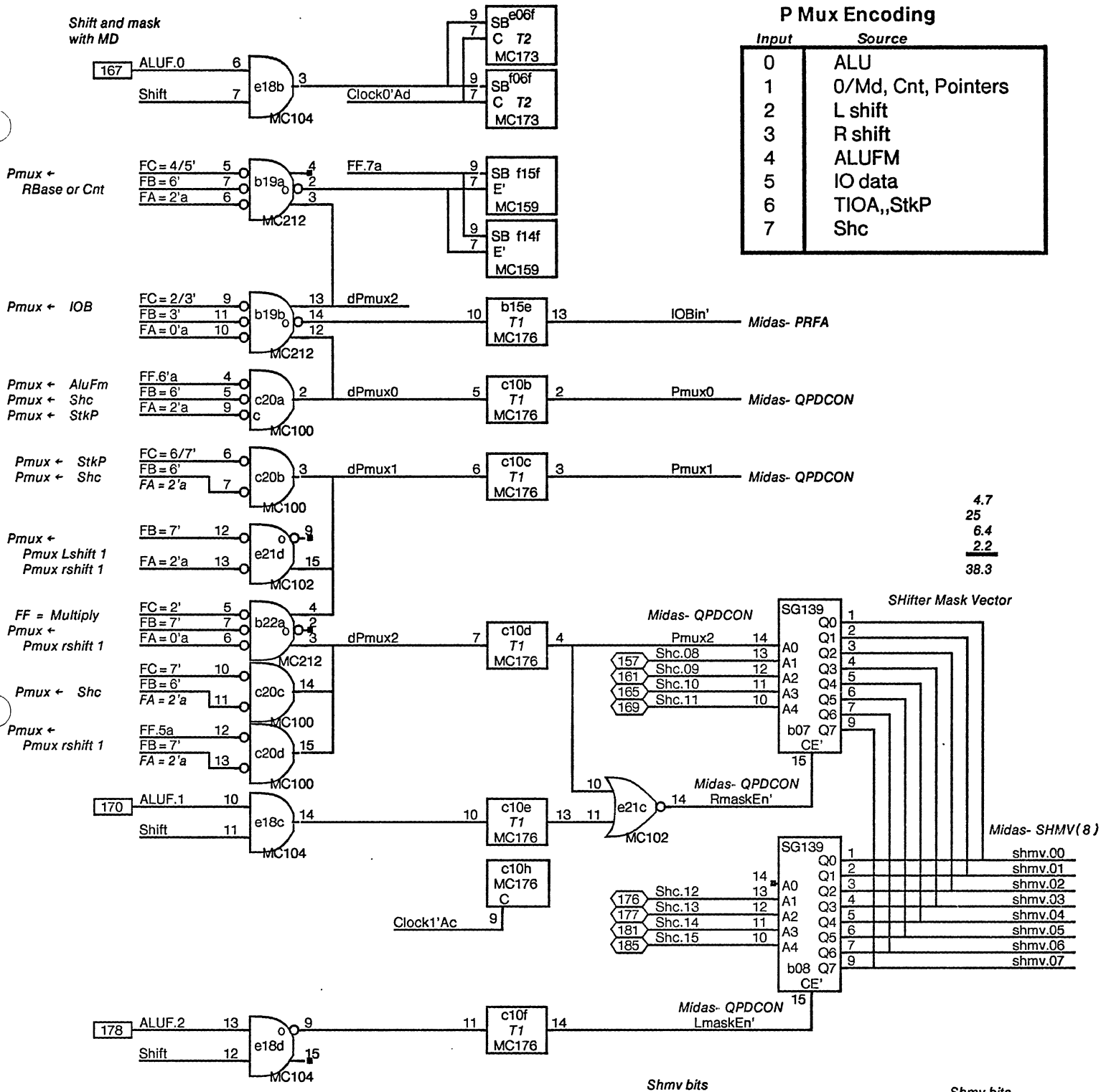








XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	"B" Multiplexor & Cont.	ProcH15.sil	R Bates	Ce	6/20/79	15



P Mux Encoding

Input	Source
0	ALU
1	0/Md, Cnt, Pointers
2	L shift
3	R shift
4	ALUFM
5	IO data
6	TIOA,,StkP
7	Shc

Lmask

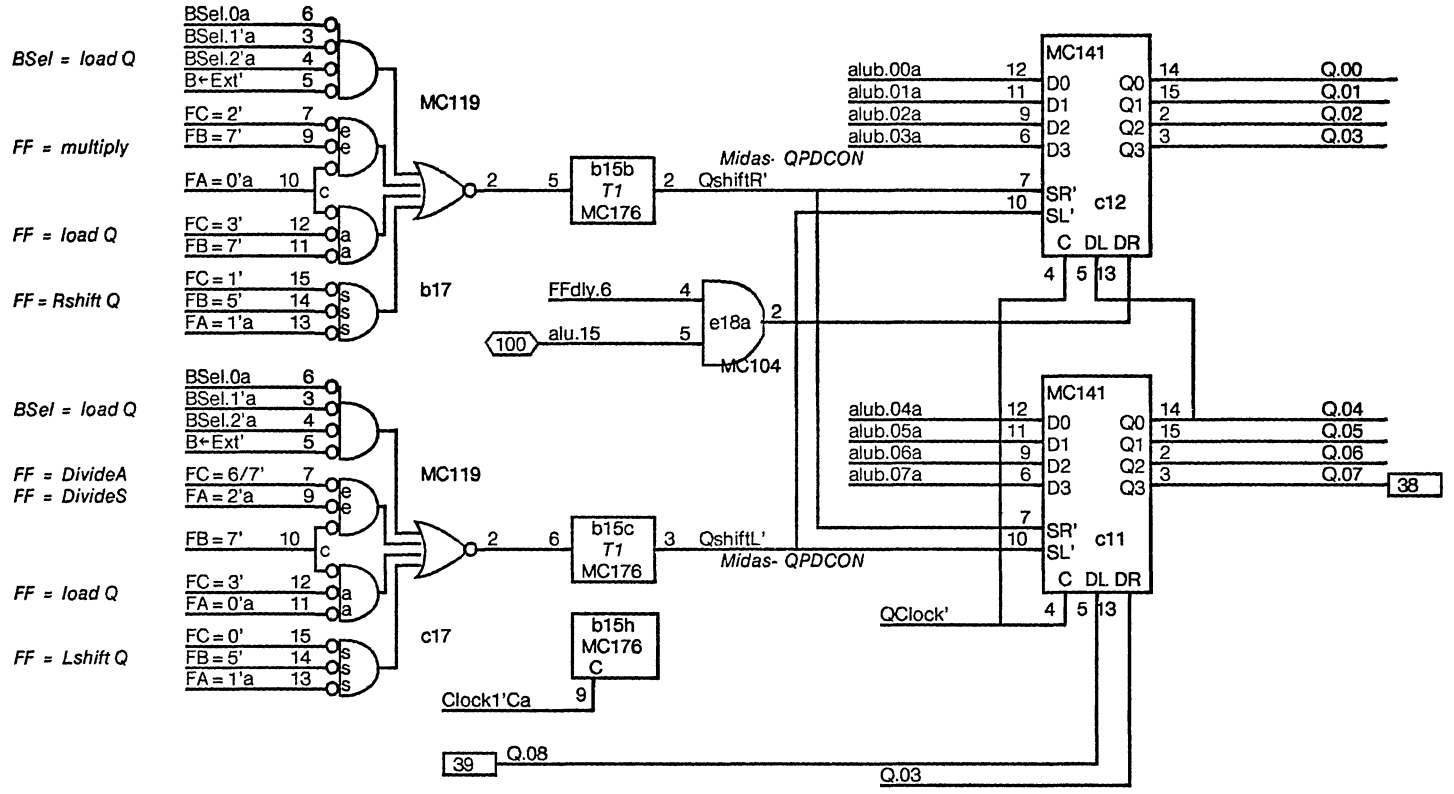
Shc.12-15	Shmv bits 00	01	02	03	04	05	06	07
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	1	1	1	1	0	0
7	1	1	1	1	1	1	1	0
10	1	1	1	1	1	1	1	1
11	1	1	1	1	1	1	1	1
12	1	1	1	1	1	1	1	1
13	1	1	1	1	1	1	1	1
14	1	1	1	1	1	1	1	1
15	1	1	1	1	1	1	1	1
16	1	1	1	1	1	1	1	1
17	1	1	1	1	1	1	1	1
20- 37	1	1	1	1	1	1	1	1

Rmask

Shc.08-11	Shmv bits 00	01	02	03	04	05	06	07
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	1
12	0	0	0	0	0	0	1	1
13	0	0	0	0	0	1	1	1
14	0	0	0	0	1	1	1	1
15	0	0	0	1	1	1	1	1
16	0	0	1	1	1	1	1	1
17	0	1	1	1	1	1	1	1
20- 37	1	1	1	1	1	1	1	1

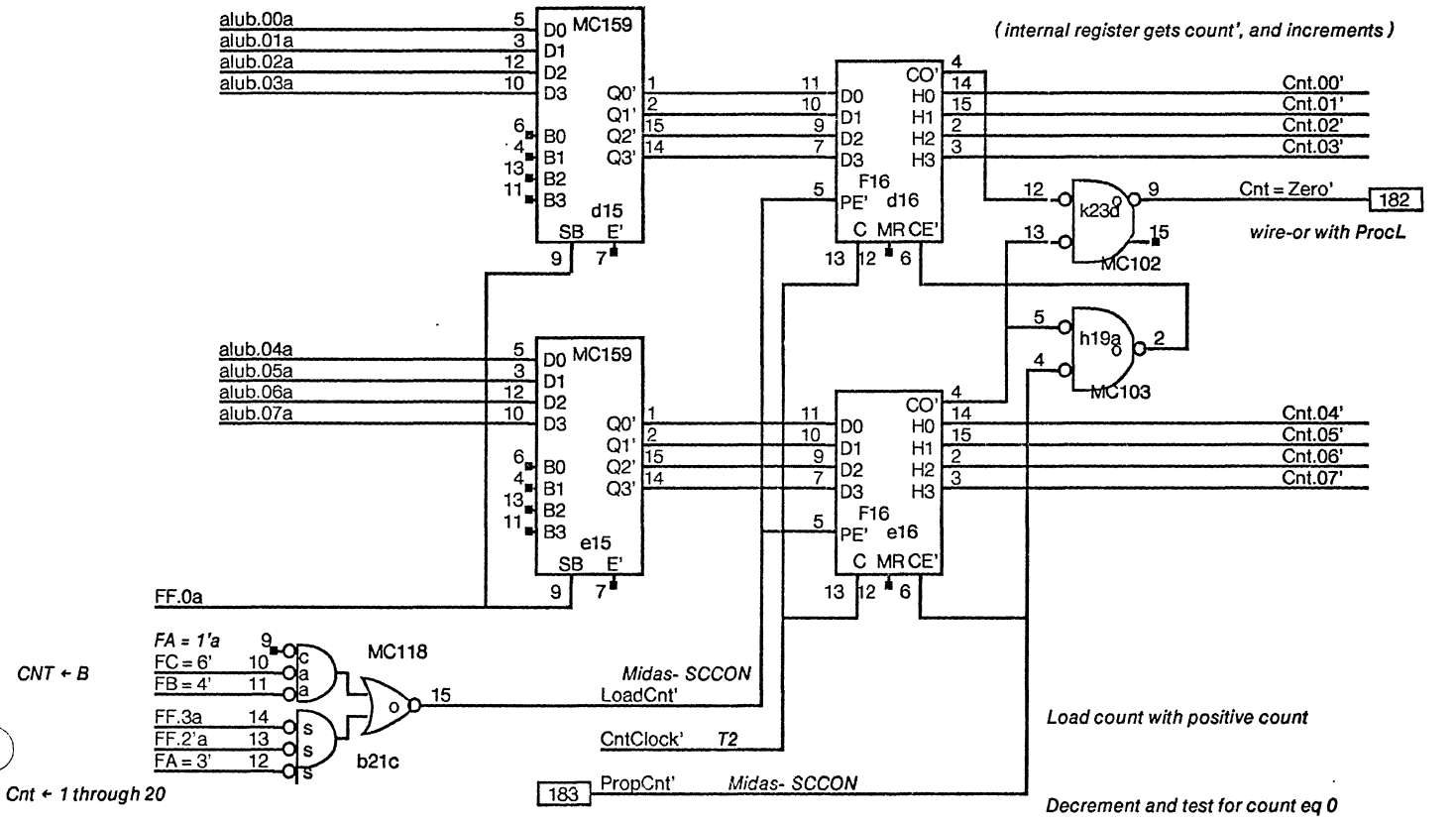
NOTE: The prom patterns are designed so that a one into address bit 0 will produce all 1's on the output. This allows the odd address inputs to Pmux to be selected.

XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Proc Multiplexor & Shift mask Prom	ProcH16.sil	R Bates	Ce	6/18/79	16



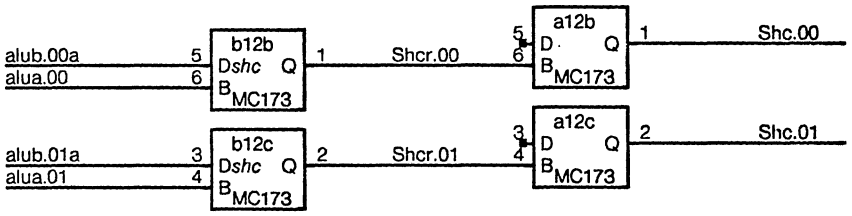
Q Register

Count Register



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Q Register and Count Register	ProcH17.sil	R Bates	Ce	7/08/79	17

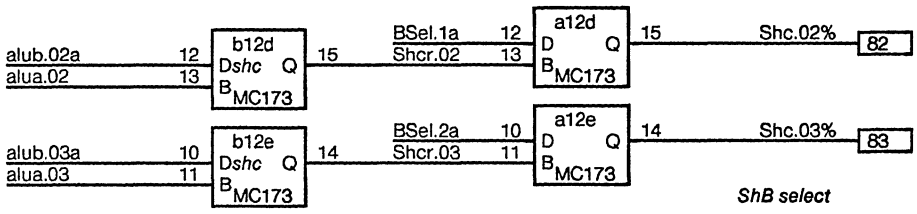
Extra Bits



R/T Select

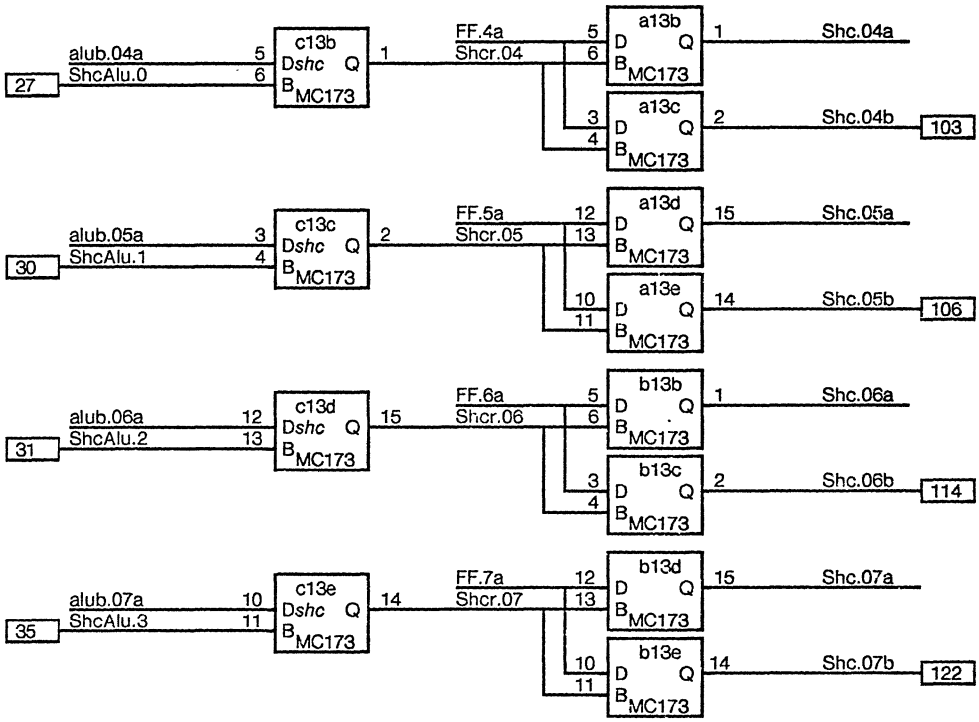
	Shc.02	Shc.03	ProcH ShA	ProcH ShB	ProcL ShA	ProcL ShB
R,,R	0	0	R	R	R	R
R,,T	0	1	R	T	T	R
T,,R	1	0	T	R	R	T
T,,T	1	1	T	T	T	T

Note R selcted with "0"
T selected with "1"

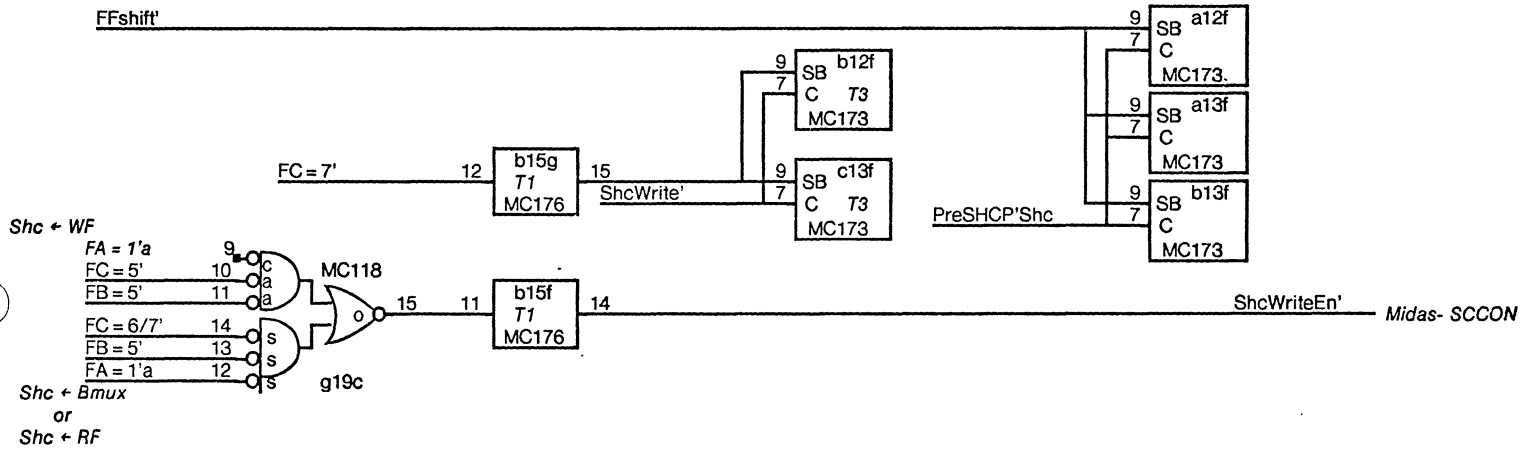


IntBmux RF / WF → **FF** — *Shift control*

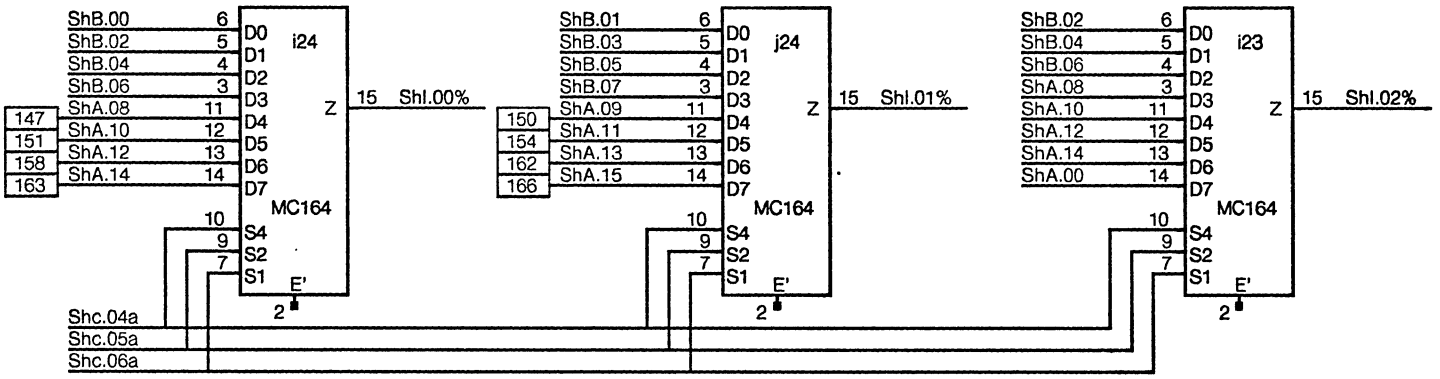
Shift Count

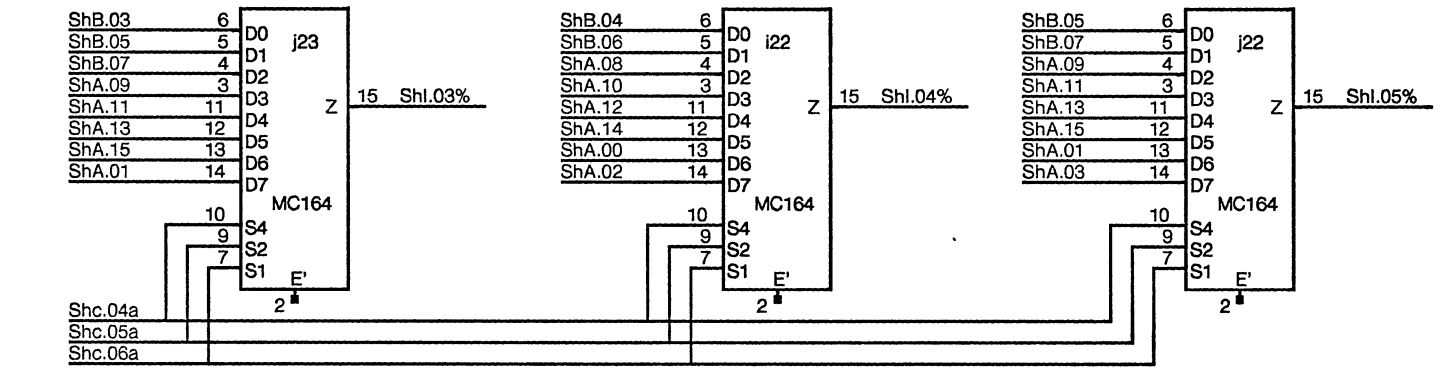


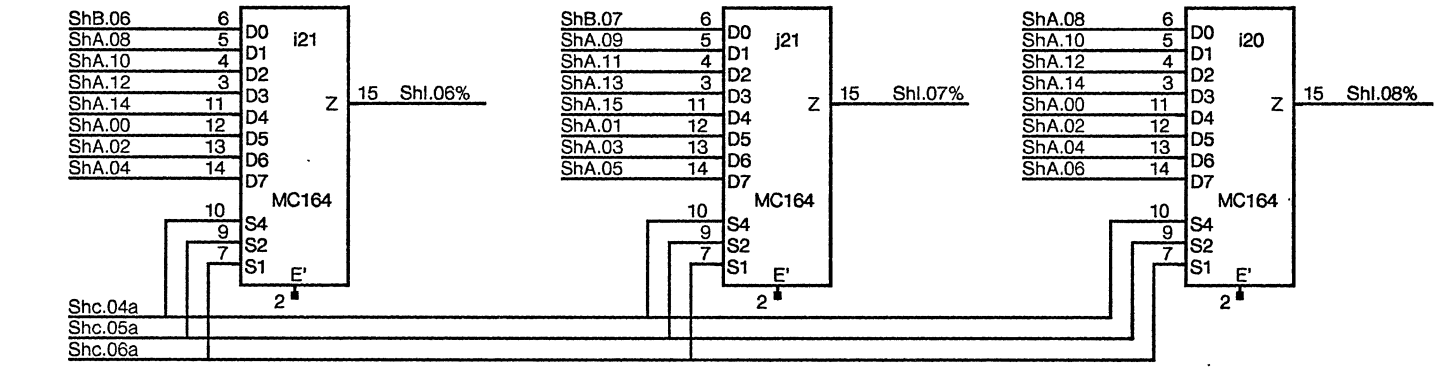
Done this way so FF shifts do not use Shc - IO tasks can use the shifter without saving and restoring Shc.

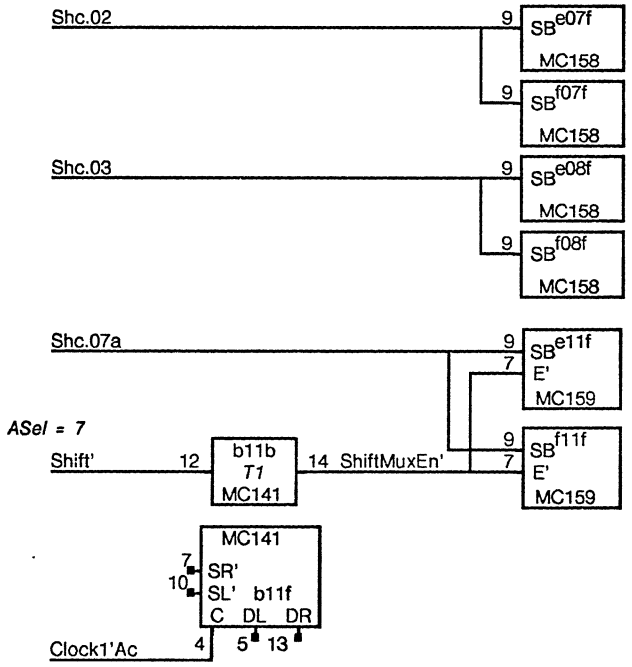


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Shift Register Control	ProcH18.sil	R Bates	Ce	6/18/79	18





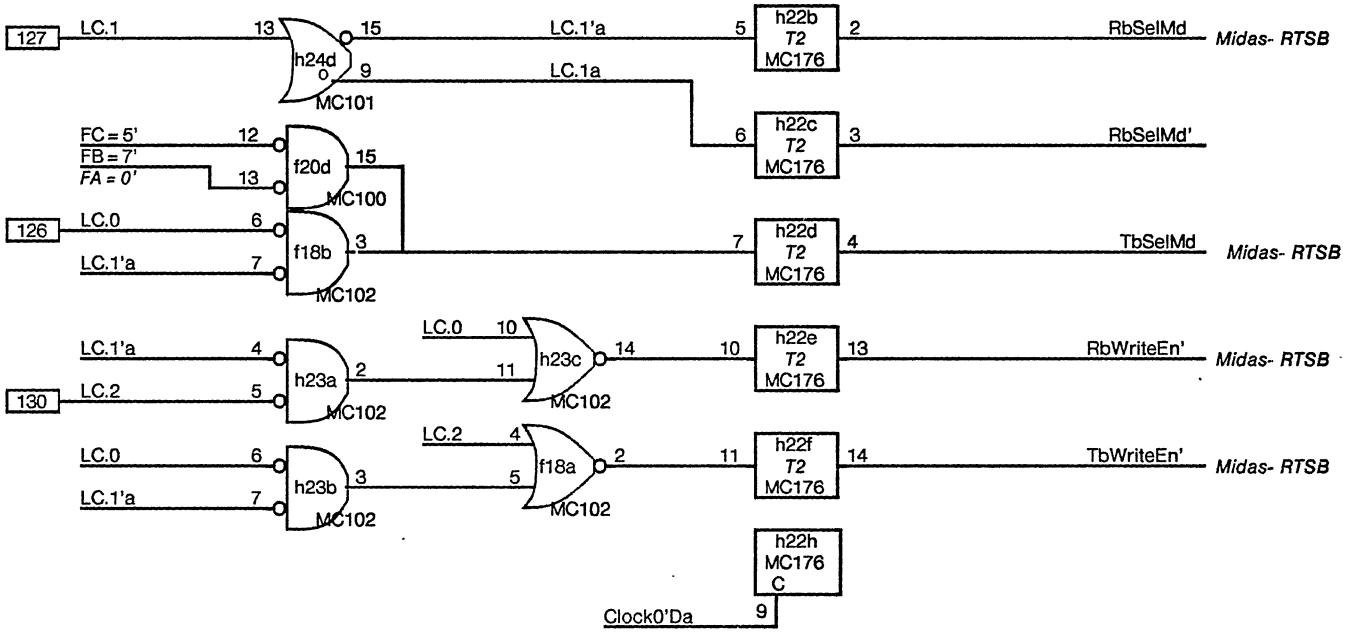


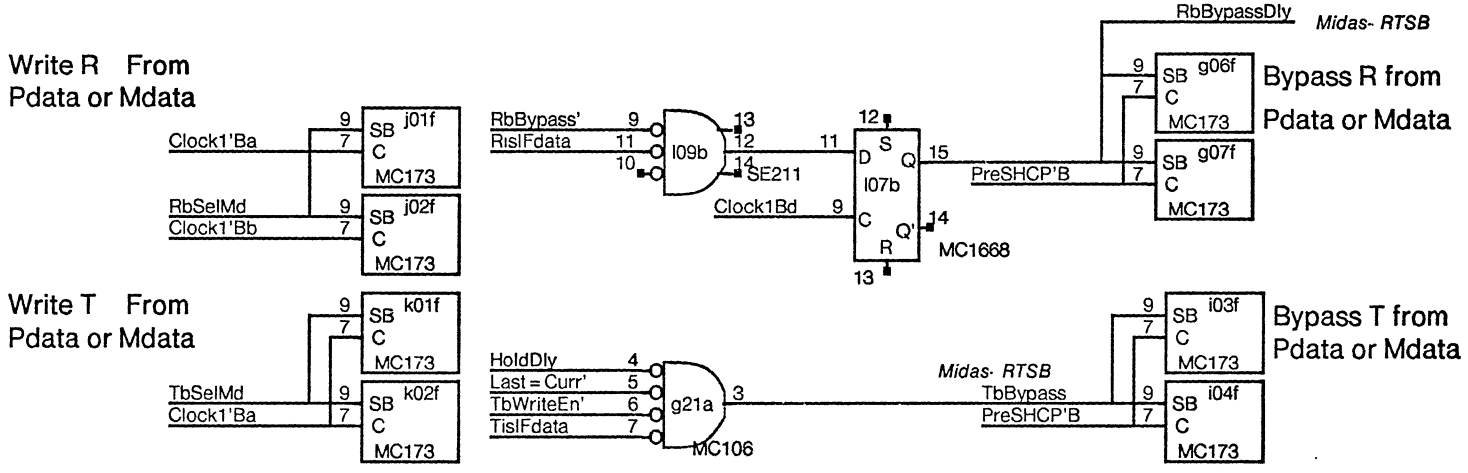


Shc.02	Shc.03	Shc.04 - .07
0	0	16 bit Left cycle of R
0	1	16 bit Left cycle of R,,T
1	0	16 bit Left cycle of T,,R
1	1	16 bit Left cycle of T

LC 0	LC 1	LC 2	R	T
0	0	0	-	-
0	0	1	-	Pd *
0	1	0	Pd	Md
0	1	1	-	Md
1	0	0	Md	-
1	0	1	Md	Pd *
1	1	0	Pd	-
1	1	1	Pd	Pd *

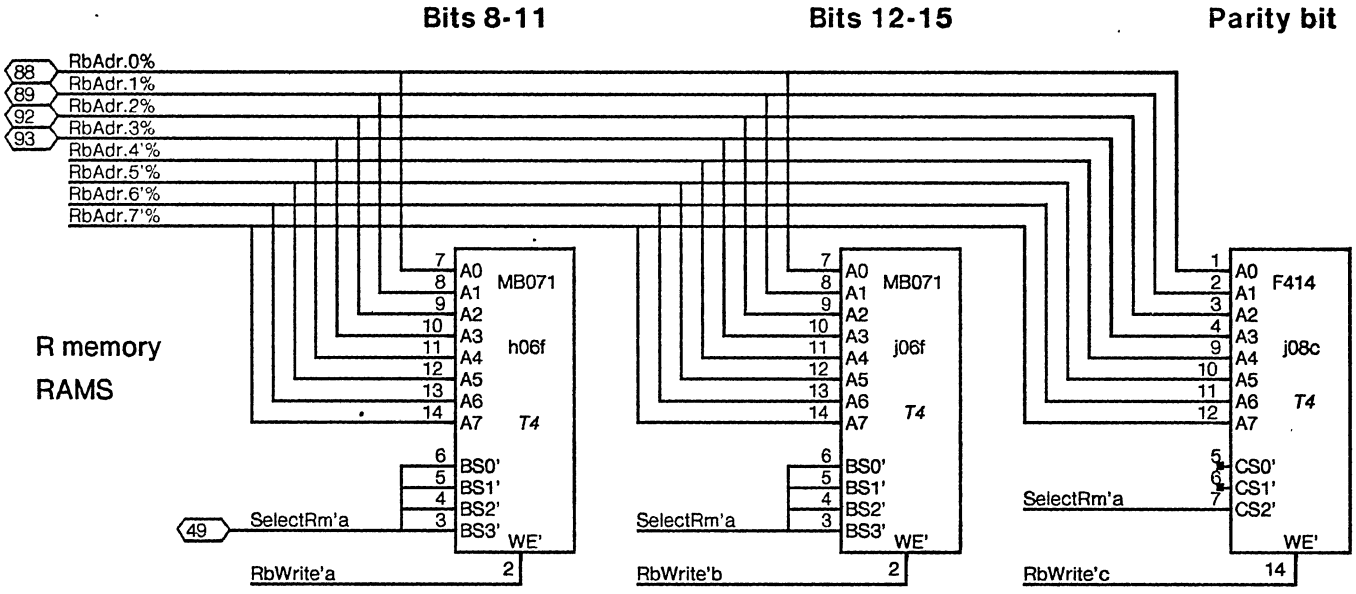
* Md if used when FF = 075

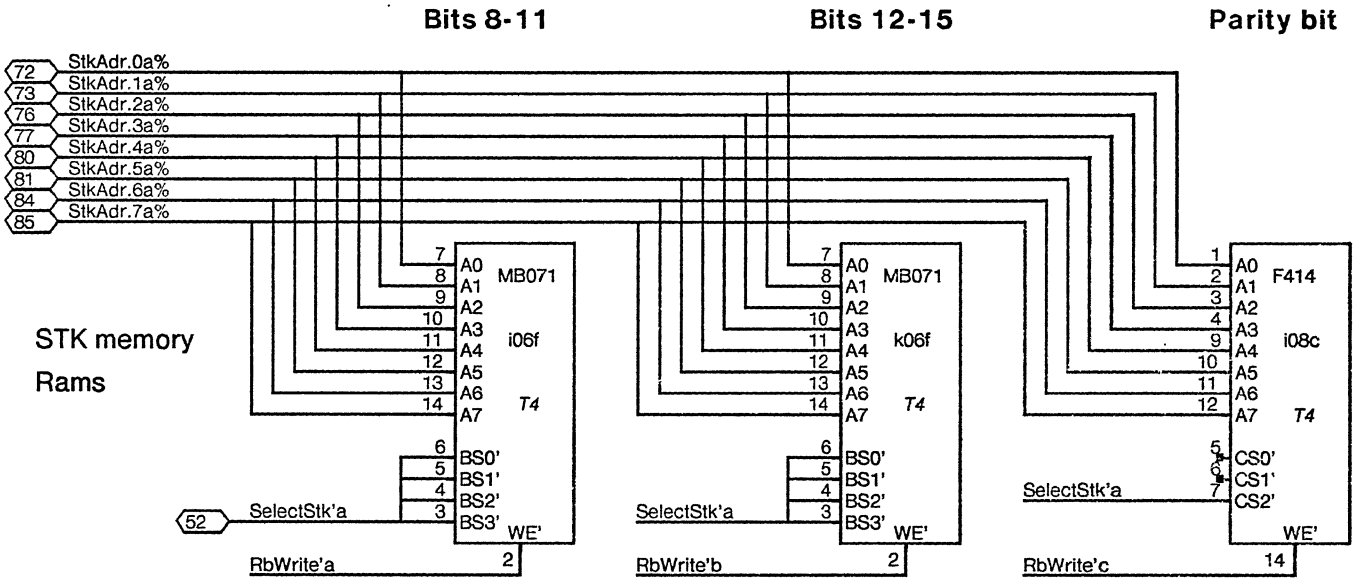


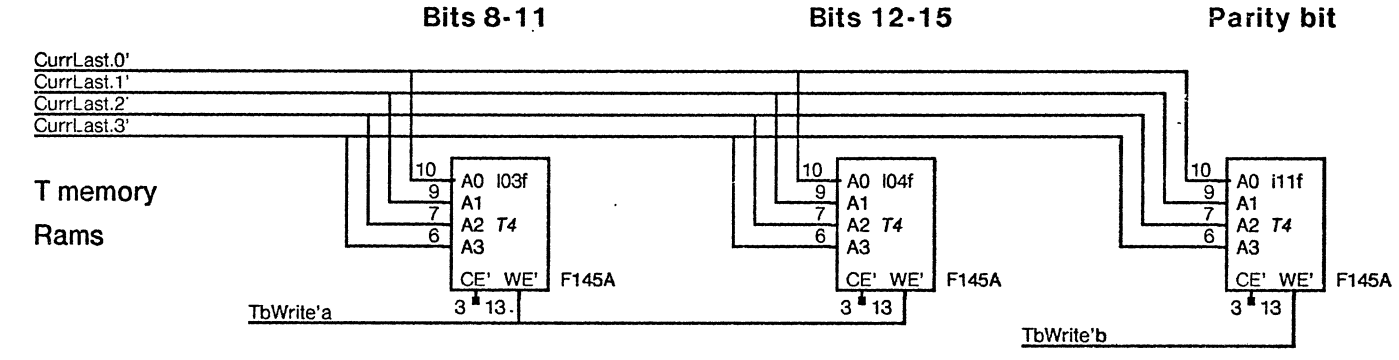


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	LC FIELD RAM ADDRESSES	ProcH20.sil	R Bates	Ce	6/18/79	20

0-3 4-7

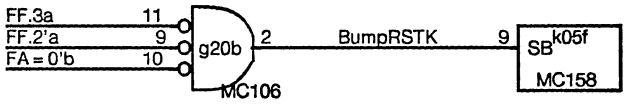






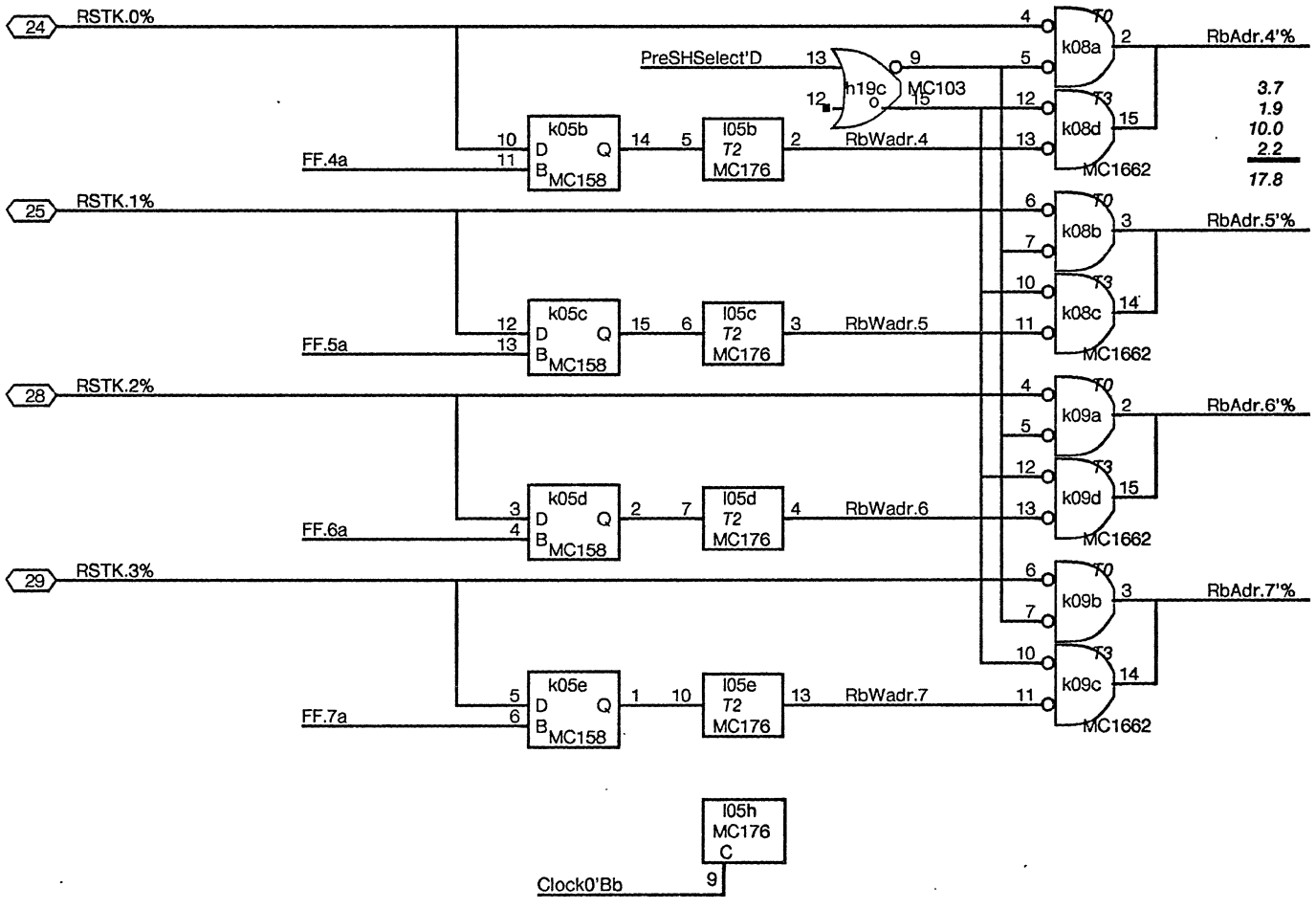
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	RM & STK addressing	ProcH21.sil	R Bates	Ce	6/18/79	21

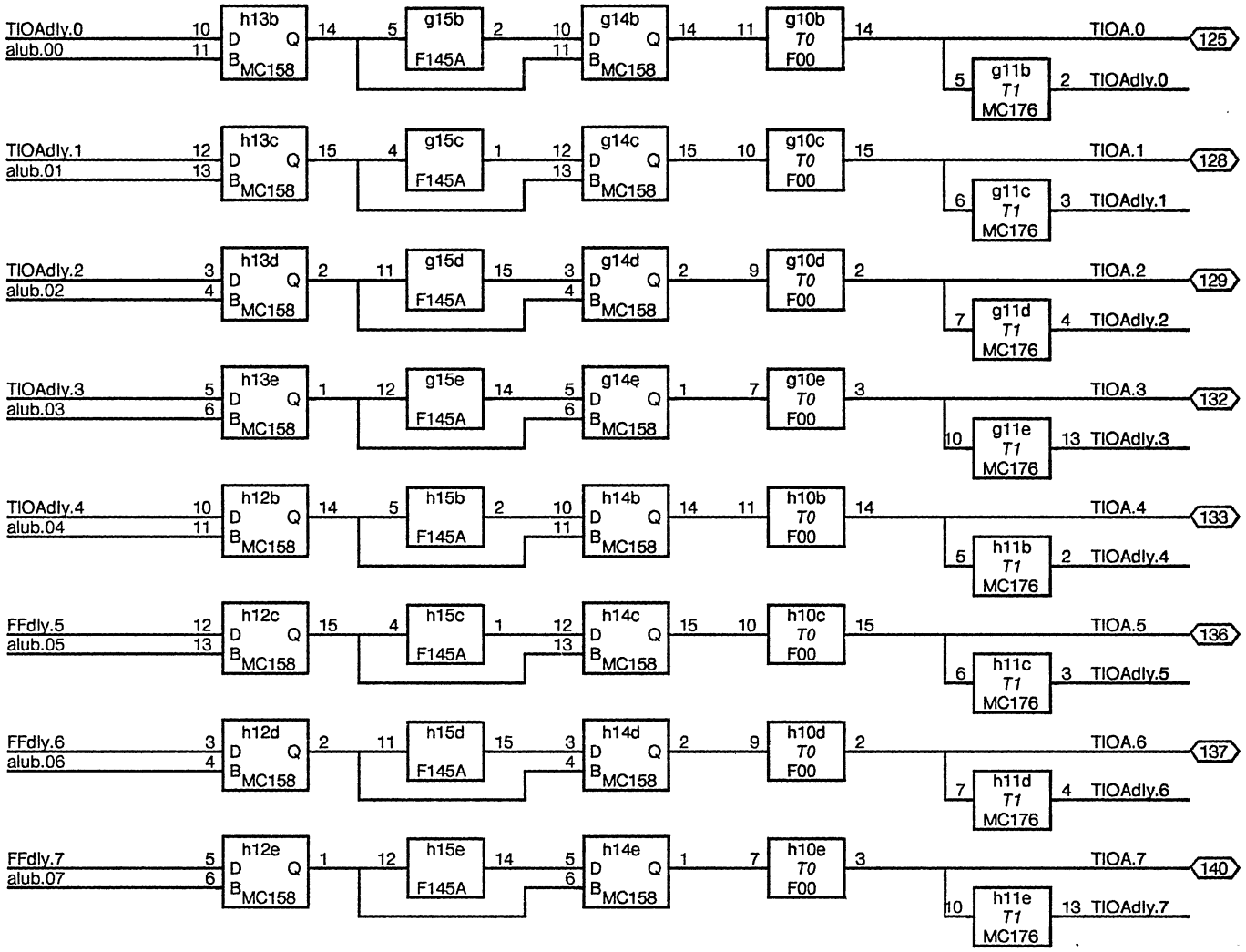
RbWadr ← RBase,,FF

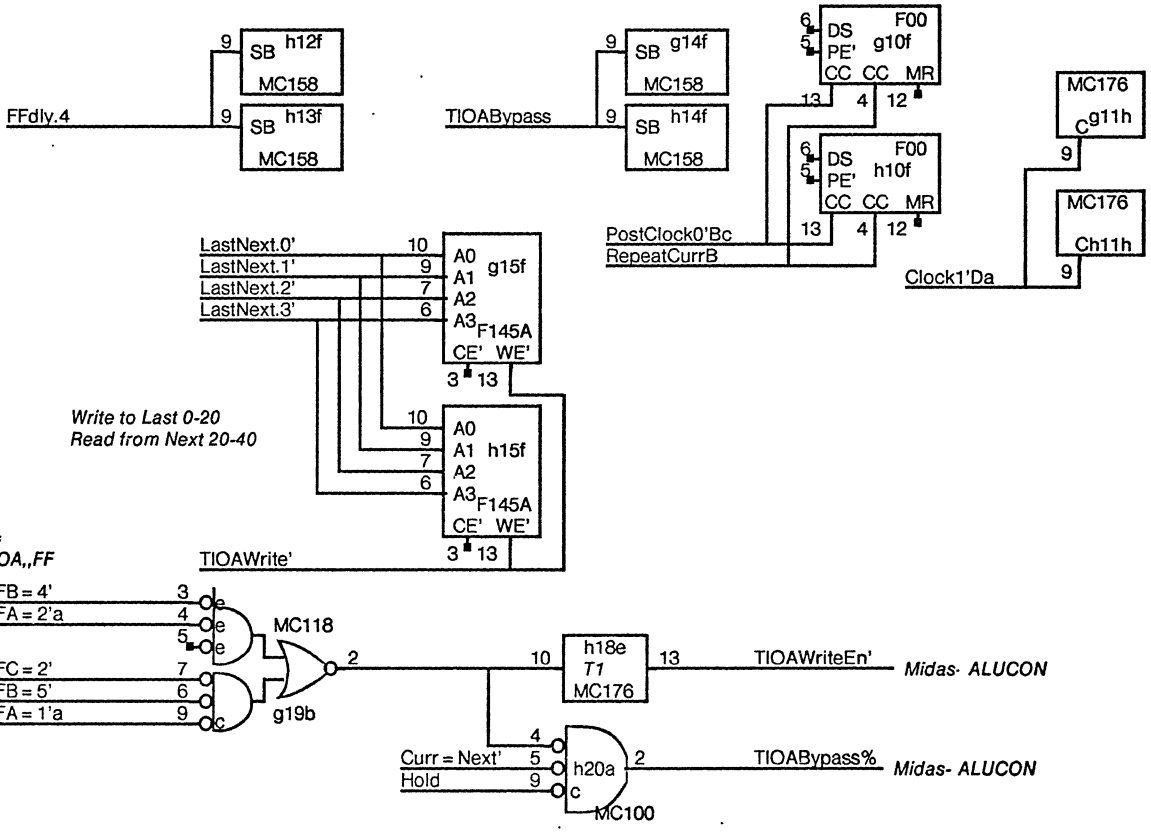


RSTK Control for bits 4 - 7 of the Rm address

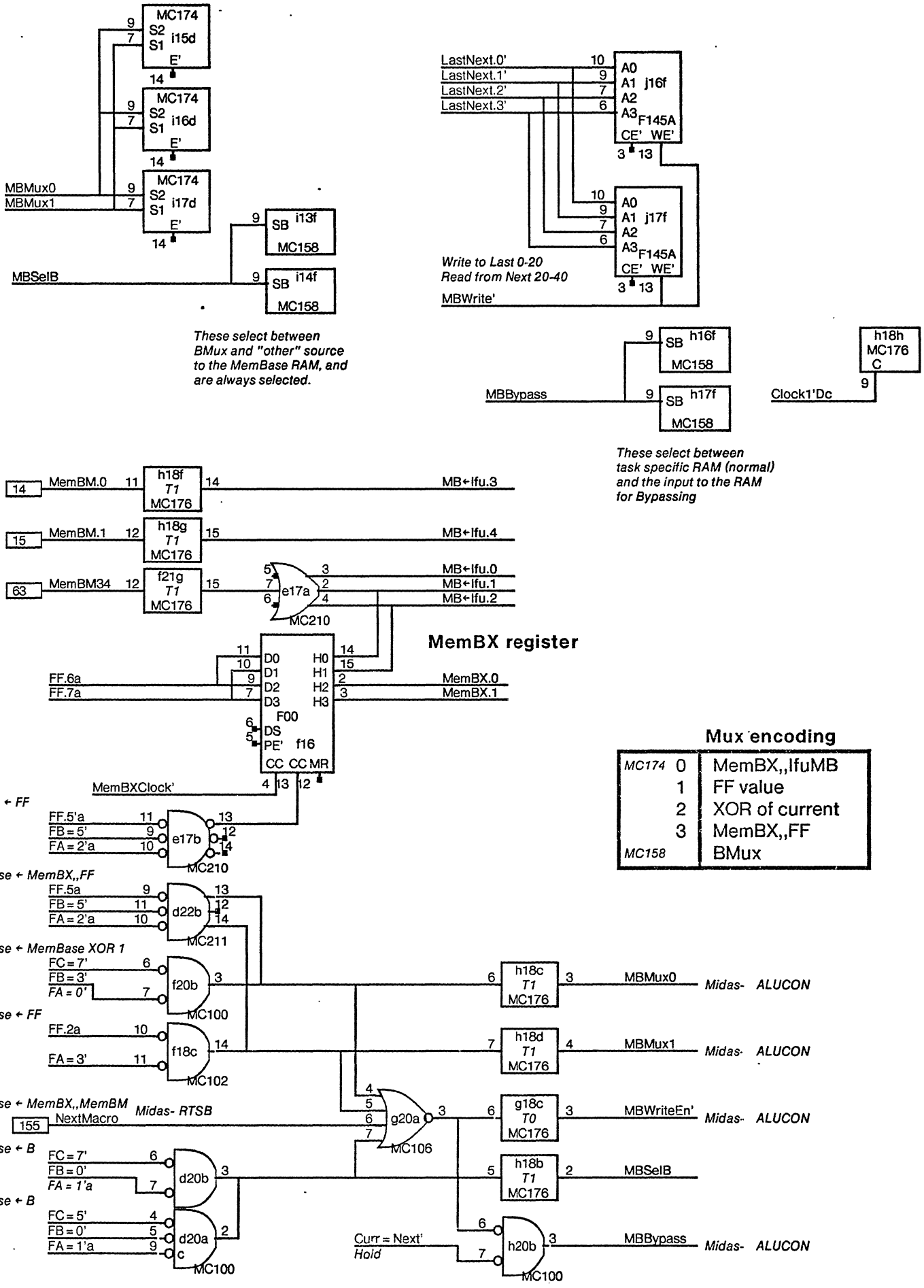
RSTK bits that make up Rm address bits 4-7



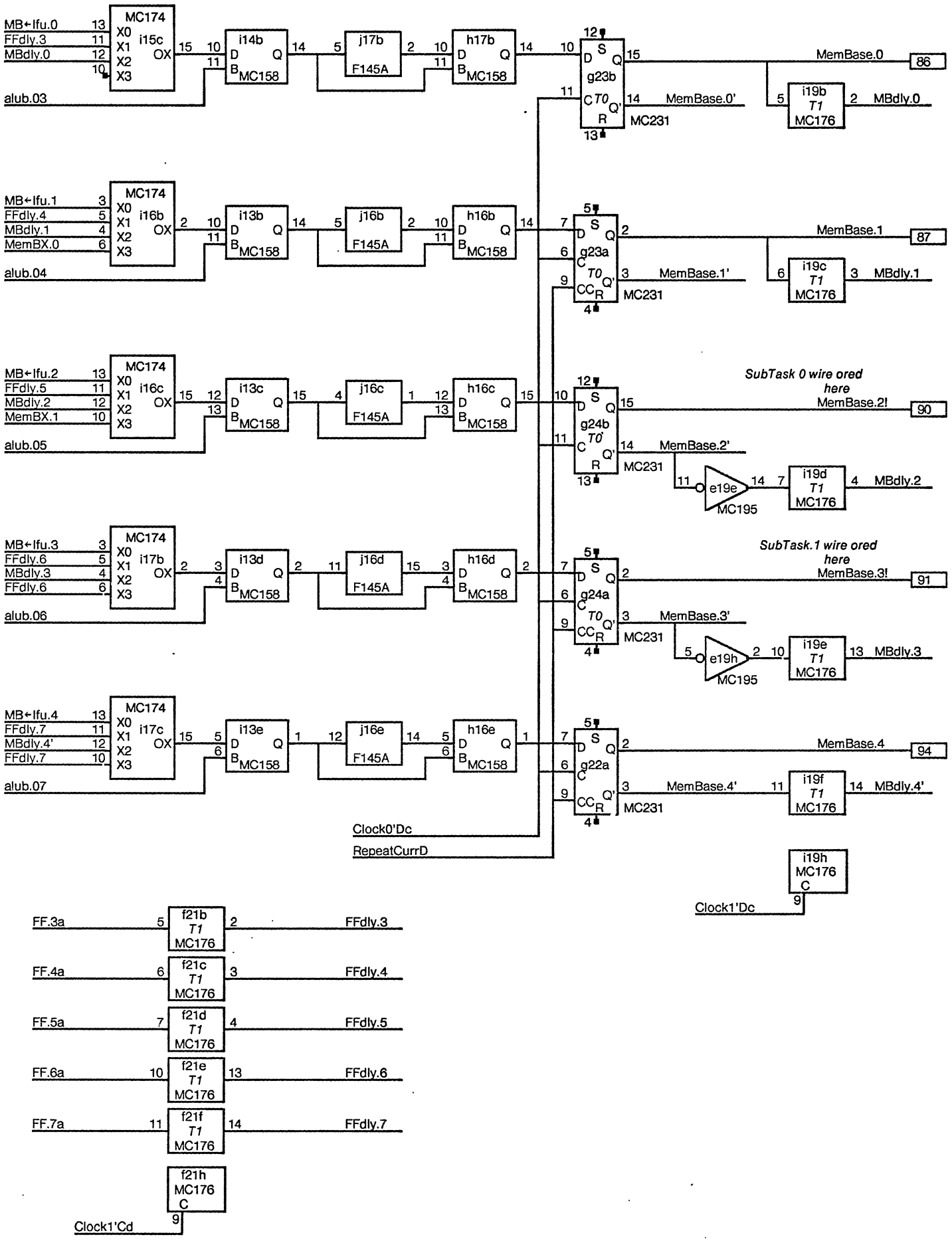




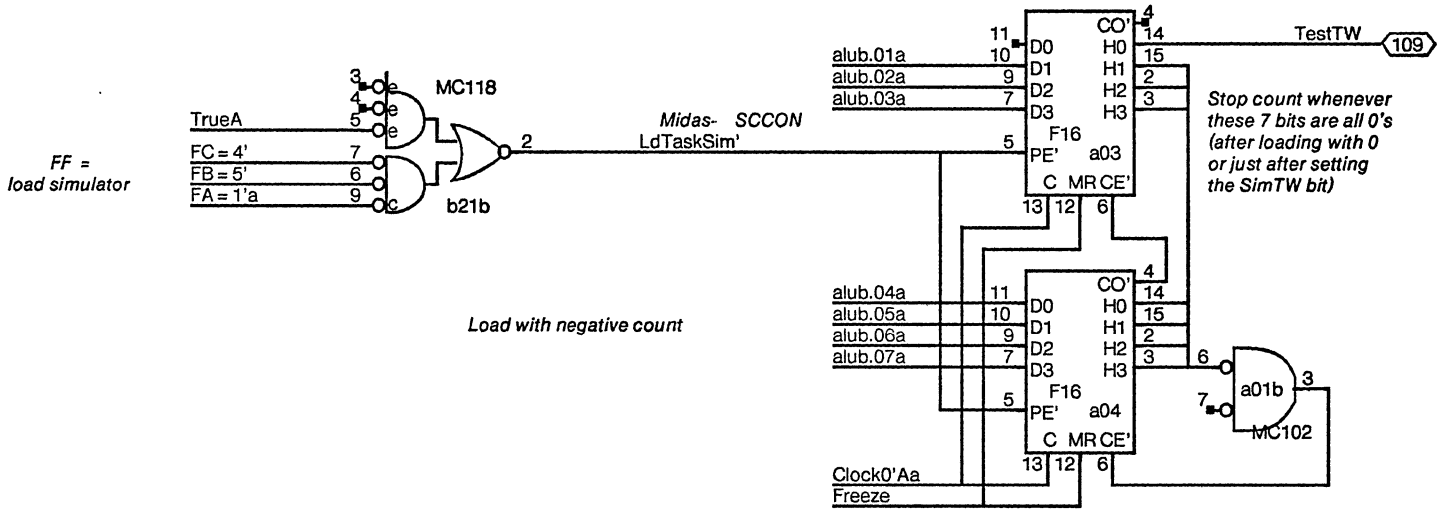
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	I/O ADDRESS RAM	ProcH23.sil	R Bates	Ce	6/18/79	23



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	MemBase Register Cont.	ProcH24.sil	R Bates	Ce	6/18/79	24



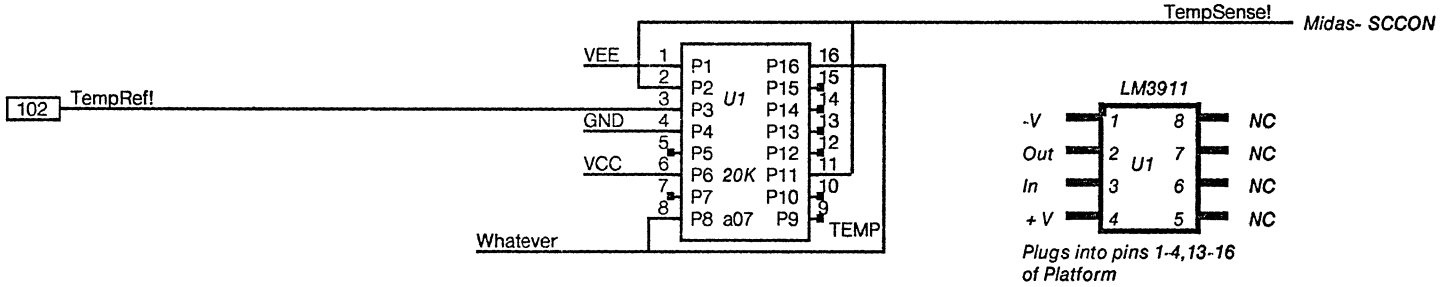
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Map Base Addressing	ProcH25.sil	R Bates	Ce	6/18/79	25



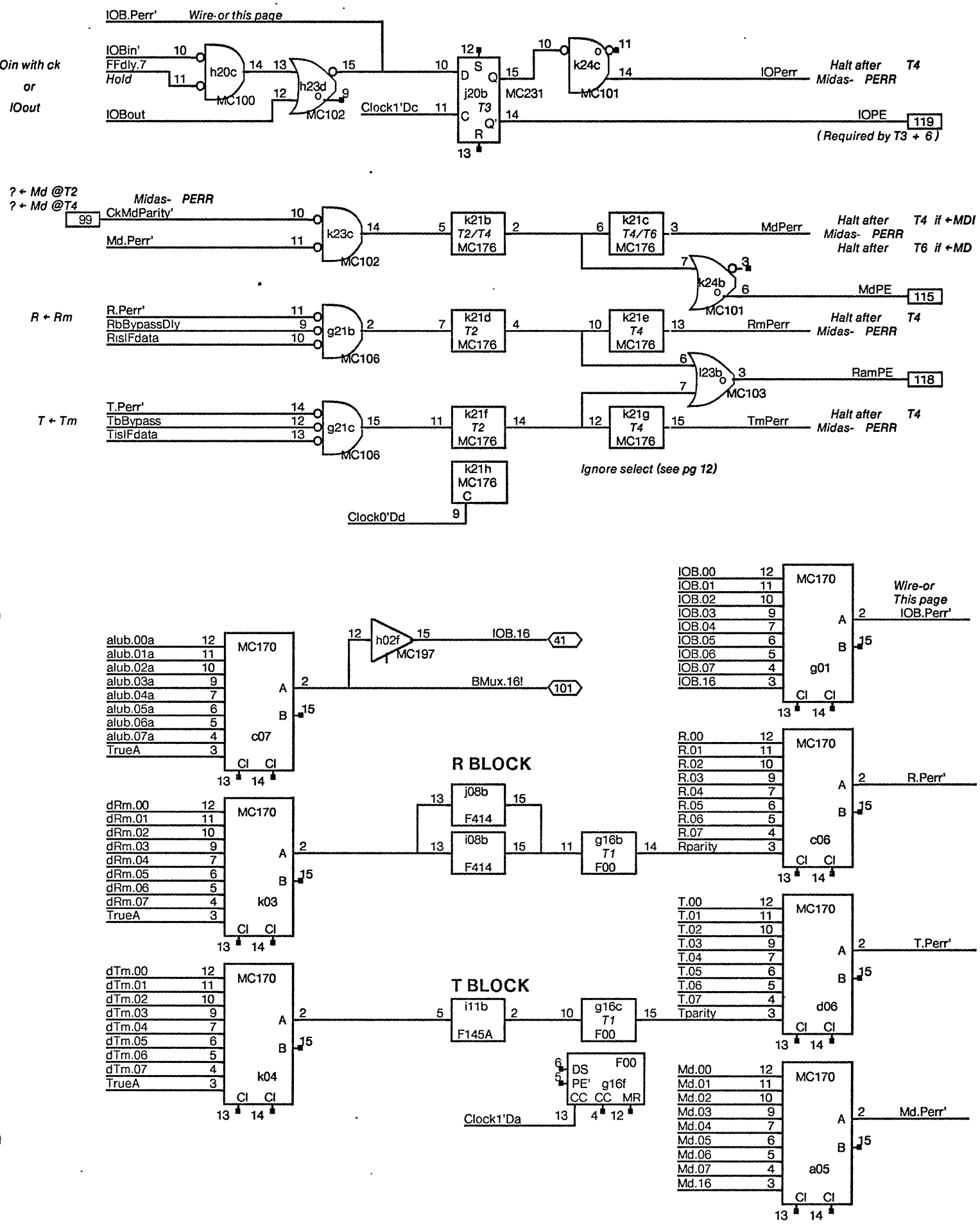
To enable this test circuit be sure there is a jumper to Connect TestTW (<109>) to ContA pin <140>

Task Simulator

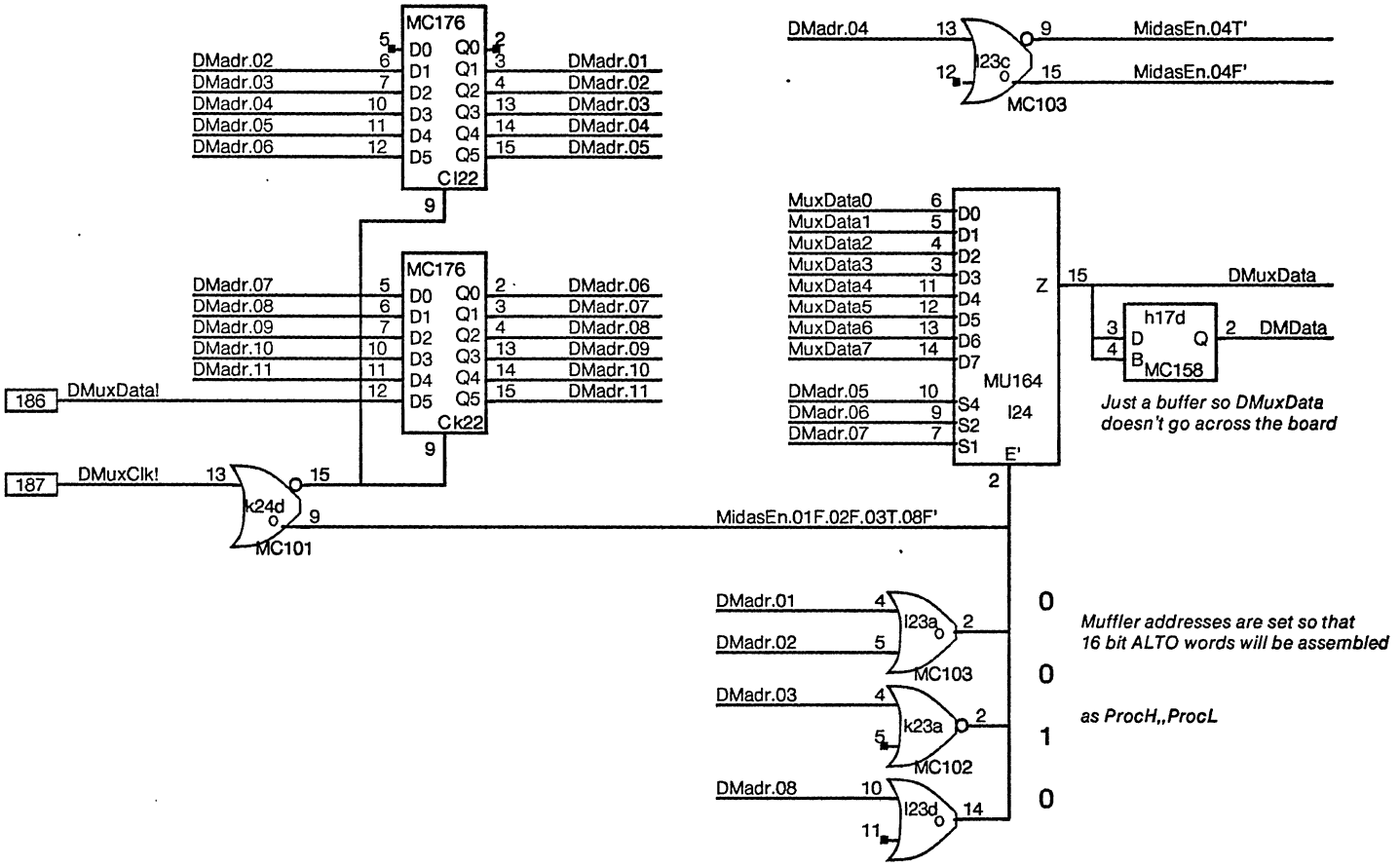
Temperature Sensing Ckt



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Hold Simulator and Temperature Sense	ProcH26.sil	R Bates	Ce	6/19/79	26

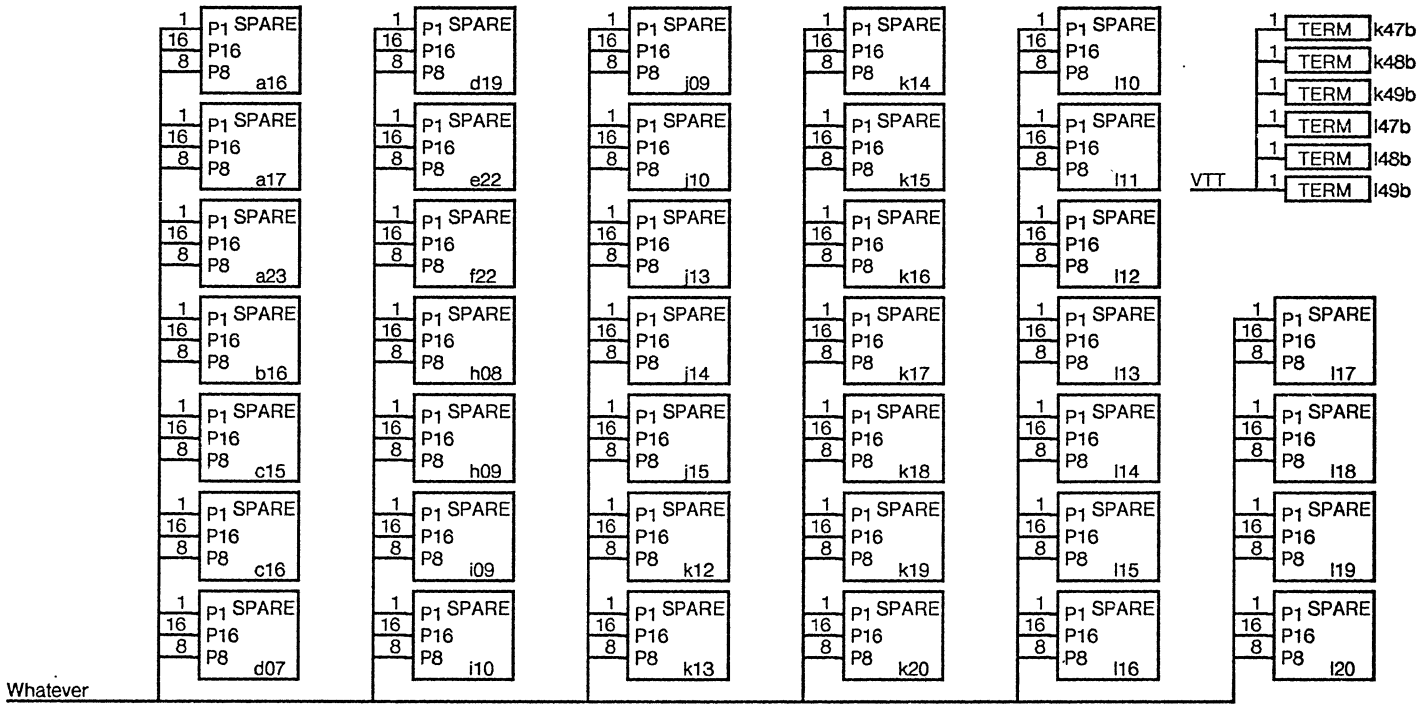


XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Parity Logic	ProcH27.sil	R Bates	Ce	6/18/79	27



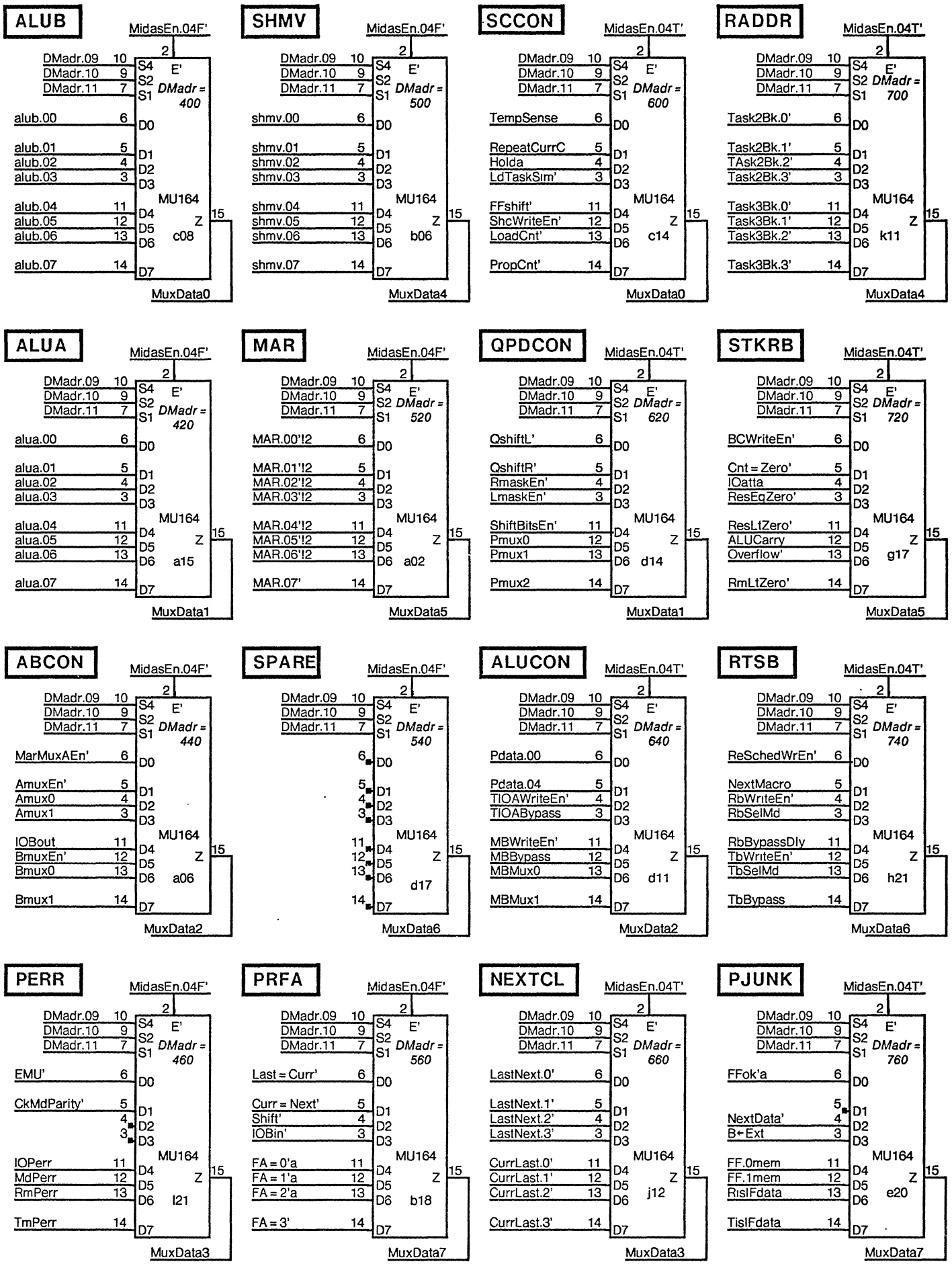
Midas Control

Spare Sockets for Multiwire

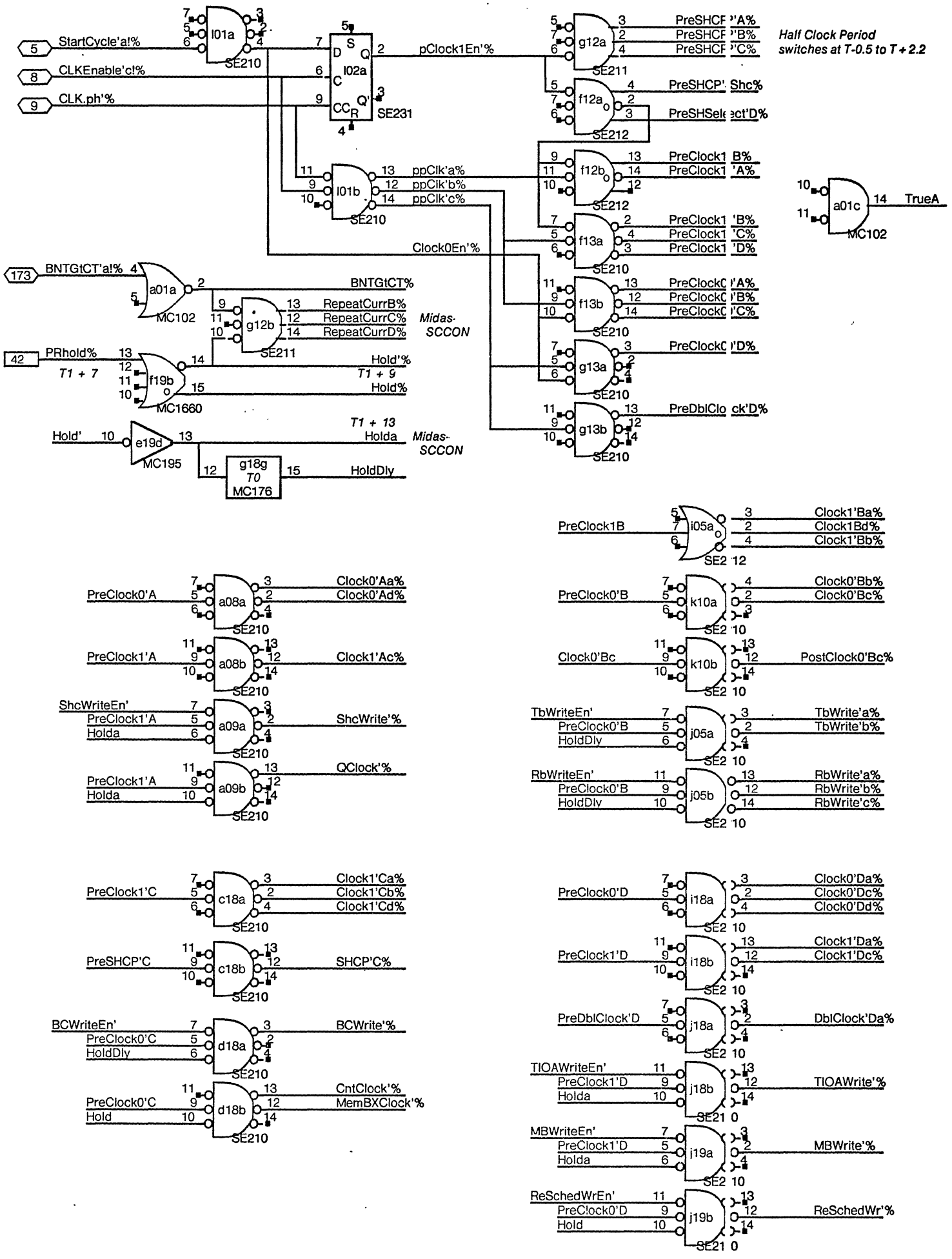


The following Platforms are entered so that route will cause multi-wire drill pattern to include a number of unused locations just in case they need to be used in some way.

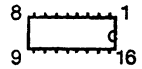
XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	Midas Control	ProcH28.sil	R Bates	Ce	6/18/79	28



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	DMUX MUFFLERS	ProcH29.sil	R Bates	Ce	6/18/79	29



XEROX PARC	Project	Drawing	File	Designer	Rev	Date	Page
	Dorado	CLOCK DRIVERS	ProcH30.sil	R Bates	Ce	6/18/79	30



A B

-2v TIOA IOB IOB Clk +12v

	A (184)	B (168)	C (152)	D (136)	E (120)	F (102)	G (84)	H (68)	I (52)	J (36)	K (20)	L	
1	MC102	Ex Bmux MC174 X	Ex Bmux MC174 X	Ex Bmux MC1662 X	Ex Bmux MC174 X	Ex Bmux MC174 X	IOB par. MC170 X	IOB MC197 X	Md MC175 X	dRm Reg. MC173 X	dTm Reg. MC173 X	Clocks SE210	1
41	MAR MU164 X	Mar Mux MC159 X	Mar Mux MC159 X	Ex Bmux MC1662 X	Mar Mux MC159 X	Mar Mux MC159 X	Pdata MC164 X	IOB MC197 X	Md MC175 X	dRm Reg. MC173 X	dTm Reg. MC173 X	Clocks SE231	41
2	SimHold F141 X	Amux MC174 X	Amux MC174 X	Amux MC174 X	Amux MC174 X	Pdata MC164 X	Pdata MC164 X	Pdata MC164 X	T Reg. MC173 X	dT Reg. MC173 X	dRm Par. MC170 X	T Mem. MC145 X	2
42	SimHold F141 X	Bmux MC174 X	Bmux MC174 X	Bmux MC174 X	Bmux MC174 X	Pdata MC164 X	Pdata MC164 X	Pdata MC164 X	T Reg. MC173 X	dT Reg. MC173 X	dT par. MC170 X	T Mem. MC145 X	42
3	Md Parity MC170 X	Amux In MC173 X	Bmux In MC173 X	Amux In MC173 X	Bmux In MC173 X	Pdata MC164 X	dR Reg. MC173 X	dR Reg. MC173 X	Clocks SE212	Clocks SE210	RSTK MC158 X	RSTK MC176	3
43	Mux Cont MU164	Shmv MU164 X	R Parity MC170 X	T Parity MC170 X	Pdata in MC173 X	Pdata in MC173 X	R Reg. MC173 X	Rm Mem. MB071 X	Stk Mem. MB071 X	Rm Mem. MB071 X	Stk Mem. MB071 X	R<0 MC1668	43
4	Temp LM3911 X	Shmv MC139 X	alub Par MC170 X		ShA MC158 X	ShA MC158 X	R Reg. MC173 X					R<0 MC1668	4
44	Clocks SE210	Shmv MC139 X	alub MU164 X	alu = 0 MC109	AhB MC158 X	AhB MC158 X	Pdata MC164		Stk parity F414 X	Rm parity F414 X	RbAdr MC1662 X	R<0 MC211	44
5	Clocks SE210	alub·a MC101 X	alub·a MC101 X	alu MC181 X		alu MC181 X	Pdata MC164				RbAdr MC1662 X	R<0 MC211	5
45	Amux T1 MC231	Bmux T1 MC231	Mux T1 MC176				TIOA F00 X	TIOA F00 X			Clocks SE210		45
6	Bmux T1 MC231	Mux T1 MC141	Q Reg. MC141 X	ALUFM MU164 X	alua sh MC159 X	alua sh MC159 X	TIOA MC176	TIOA MC176	T mem-P MC145 X	TASKs MC176	TASKs MU164 X		6
46	Shc MC173 X	Shc MC173 X	Q Reg. MC141 X	Carry MC118	Carry MC121	Clocks SE212	Clocks SE211	TIOA MC158 X	CurrLast MC141 X	NextLast MU164 X			46
7	Shc MC173 X	Shc MC173 X	Shc MC173 X	Branches MC170 X	Branches MC145 X	Clocks SE210	Clocks SE210	TIOA MC158 X	MemBase MC158 X				7
47	Bmux In MC158 X	Bmux In MC158 X	Shc MU164 X	P mux MU164 X	Branches MC158	Pdata in MC159 X	TIOA MC158 X	TIOA MC158 X	MemBase MC158				47
8	alua MC164 X	Q Reg. T1 MC176		CntMux MC159 X	CntMux MC159 X	Pdata in MC159 X	TIOA MC145 X	TIOA MC145 X	MemBase MC174 X				8
48				Cnt Reg. F16 X	Cnt Reg. F16 X	MemBX F00 X	Parity T1 F00	MemBase MC158 X	MemBase MC174 X	MemBase MC145			48
9		Q Reg. MC119 X	Q Reg. MC119 X	SPAIR MU164 X	MemBX MC210	Branches MC173 X	MU164 X	MemBase MC158	MemBase MC174 X	MemBase MC145			9
49	CurrLast MC158 X	FA MU164 X	Clocks SE210	Clocks SE210	P mux MC104	Misc. MC102	Misc. T0 MC176	T1 MC176	Clocks SE210	Clocks SE210			49
10	LastNext' MC158 X	Misc. MC212	Amux MC121 X		Misc. MC195	MC1660	MC118	Misc. MC103	MBdly MC176	Clocks SE210			10
50	Last' MC141 X	FA = 0 MC100	FA = 2 MC100	FA = 1 MC100	Misc. MU164 X	FA = 0 MC100	Misc. MC106	Bypass MC100	Shl MC164 X	MC231			50
11	Curr' MC141 X	FA = 1 MC118	Amux MC119 X	Amux MC117 X	Misc. MC102	FFdly T1 MC176	Parity MC106	Rm cont MU164 X	Shl MC164 X	Shl MC164 X	Parity MC176	Parity MU164 X	11
51	Next = Curr MC113 X	P mux MC212	Misc. MC102	ALUF MC211			MemBase MC231	Misc. T0 MC176	Shl MC164 X	Shl MC164 X	Midas MC176 X	Midas MC176 X	51
12		ASel MC101	FF dec. MC210	FF dec. MC101 X	FF·a MC101 X	FF·a MC101 X	MemBase MC231	LC dec. MC102	Shl MC164 X	Shl MC164 X	Misc. MC102	Misc. MC103	12
52	Next MC101 X	MC210	Misc. MC103	FF dec. MC101 X	FF dec MC161 X	FF dec. MC161 X	MemBase MC231	BSel dec. MC101	Shl MC164 X	Shl MC164 X	ALUF MC101	Midas MU164 X	52
	A 10	B 26	C 42	D 58	E 74	F 92	G 110	H 126	I 142	J 158	K 174	L	

-5v Muffler +5v

C D

Spare = 40

XEROX PARC	Project	Reference	File	Designer	Rev	Date	Page
	Dorado	Board Layout	ProcH31.sil	R. Bates	Ce	6/18/79	31

Use Dorado Proms to define the following Proms:

Board Name	Prom Name	location
PorcH	Lmask (High byte)	b07
	Rmask (High byte)	b08

Page Numbers: Yes First Page: 1
Columns: 2 Edge Margin: .8" Between Columns: .0"
Heading:
ProcH-Rev-Ce.ps
COMPONENTS:

F00:	11	23	24	27		
F145A:	2	3	4	5	6	7
	8	9	11	21	23	24
	25	27				
F16:	17	26				
F414:	21	27				
MB071:	2	3	4	5	6	7
	8	9	21			
MC100:	11	14	15	16	20	23
	24	27				
MC101:	11	12	13	15	20	27
	28					
MC102:	11	13	14	15	16	17
	20	24	26	27	28	30
MC103:	13	14	17	22	27	28
MC104:	16	17				
MC106:	11	20	22	24	27	
MC109:	11					
MC113:	12					
MC117:	14					
MC118:	10	11	17	18	23	26
MC119:	14	17				
MC121:	10	14				
MC141:	12	14	17	19		
MC158:	2	3	4	5	6	7
	8	9	11	12	15	19
	22	23	24	25	28	
MC159:	2	3	4	5	6	7
	8	9	14	16	17	19
MC161:	13					
MC164:	2	3	4	5	6	7
	8	9	11	19		
MC1660:	15	30				
MC1662:	2	3	4	5	6	7
	8	9	22			
MC1664:	2	3	4	5	6	7
	8	9				
MC1668:	10	20				
MC170:	10	27				
MC173:	2	3	4	5	6	7
	8	9	11	14	15	16
	18	20				
MC174:	2	3	4	5	6	7
	8	9	14	15	24	25
MC175:	2	3	4	5	6	7
	8	9	10			
MC176:	11	12	14	16	17	18
	20	22	23	24	25	27
	28	30				
MC181:	2	3	4	5	6	7
	8	9	10			
MC195:	11	25	30			
MC197:	2	3	4	5	6	7
	8	9	15	27		
MC210:	13	24				
MC211:	13	24				
MC212:	15	16				
MC231:	11	12	14	15	25	27
MU164:	28	29				
SE210:	30					
SE211:	10	20	30			
SE212:	30					
SE231:	30					
SG139:	16					
SPARE:	28					
TEMP:	26					
TERM:	28					

SIGNAL NAMES:

```
+:              2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                8(1)    9(1)   10(1)   11(1)   12(1)   13(1)
               14(1)   15(1)   16(1)   17(1)   18(1)   19(1)
               20(1)   21(1)   22(1)   23(1)   24(1)   25(1)
               26(1)   27(1)   28(1)   29(1)   30(1)
Ain.00:         2(3)
Ain.01:         3(3)
Ain.02:         4(3)
Ain.03:         5(3)
Ain.04:         6(3)
Ain.05:         7(3)
Ain.06:         8(3)
Ain.07:         9(3)
alu.00:         2(1)    3(1)   10(1)   11(4)
alu.01:         2(1)    3(1)    4(1)   11(1)
alu.02:         3(1)    4(1)    5(1)   11(1)
alu.03:         4(1)    5(1)    6(1)   11(1)
alu.04:         5(1)    6(1)    7(1)   11(1)
alu.05:         6(1)    7(1)    8(1)   11(1)
alu.06:         7(1)    8(1)    9(1)   11(1)
alu.07:         8(1)   11(1)
alu.07%:        9(1)
alu.08:         9(1)
alu.15:        11(1)   17(1)
alua.00:       10(1)   18(1)   29(1)
alua.00%:       2(1)
alua.01:       18(1)   29(1)
alua.01%:       3(1)
alua.02:       18(1)   29(1)
alua.02%:       4(1)
alua.03:       18(1)   29(1)
alua.03%:       5(1)
alua.04:       29(1)
alua.04%:       6(1)
alua.05:       29(1)
alua.05%:       7(1)
alua.06:       29(1)
alua.06%:       8(1)
alua.07:       29(1)
alua.07%:       9(1)
alub.00:       23(1)   29(1)
alub.00%:       2(1)
alub.00a:       2(1)   10(1)   17(2)   18(1)   27(1)
alub.01:       23(1)   29(1)
alub.01%:       3(1)
alub.01a:       3(1)   17(2)   18(1)   26(1)   27(1)
alub.02:       23(1)   29(1)
alub.02%:       4(1)
alub.02a:       4(1)   17(2)   18(1)   26(1)   27(1)
alub.03:       23(1)   25(1)   29(1)
alub.03%:       5(1)
alub.03a:       5(1)   17(2)   18(1)   26(1)   27(1)
alub.04:       23(1)   25(1)   29(1)
alub.04%:       6(1)
alub.04a:       6(1)   17(2)   18(1)   26(1)   27(1)
alub.05:       23(1)   25(1)   29(1)
alub.05%:       7(1)
alub.05a:       7(1)   17(2)   18(1)   26(1)   27(1)
alub.06:       23(1)   25(1)   29(1)
alub.06%:       8(1)
alub.06a:       8(1)   17(2)   18(1)   26(1)   27(1)
alub.07:       23(1)   25(1)   29(1)
alub.07%:       9(1)
alub.07a:       9(1)   17(2)   18(1)   26(1)   27(1)
aluC0:         10(2)
ALUCarry:      11(2)   29(1)
aluCout:       10(2)   11(2)
ALUF.0:        16(1)
ALUF.1:        16(1)
ALUF.2:        16(1)
aluF0:         10(2)
aluF1:         10(1)
aluF2:         10(1)
aluF3:         10(1)
aluG1:         10(2)
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aluG2:          10(2)
aluM:           10(1)   11(1)
aluOut=0':      11(1)
aluP1:          10(2)
aluP2:          10(3)
Amux0:          14(1)   29(1)
Amux0%:         14(1)
Amux1:          14(1)   29(1)
Amux1%:         14(1)
Amux1':         14(1)
Amux1'%:        14(1)
AmuxEn':        14(1)   29(1)
ASel.0:         13(1)   14(1)
ASel.0':        13(4)
ASEL.0'!:       13(1)
ASEL.1'!:       13(1)
ASEL.2'!:       13(1)
ASel=2/3':      13(1)   14(3)
ASel=5/7:       13(1)   14(2)
ASel=5/7':      13(2)   14(1)   15(1)
ASel=6/7:       13(1)   14(2)
ASel=6/7':      13(2)   14(1)   15(1)
A←Id':          14(2)
BCWrite':       11(1)
BCWrite'%:      30(1)
BCWriteEn':     11(1)   29(1)   30(1)
Bin.00:          2(3)
Bin.01:          3(3)
Bin.02:          4(3)
Bin.03:          5(3)
Bin.04:          6(3)
Bin.05:          7(3)
Bin.06:          8(3)
Bin.07:          9(3)
BMux.00:         2(1)
BMux.00!:        2(1)
BMux.01:         3(1)
BMux.01!:        3(1)
BMux.02:         4(1)
BMux.02!:        4(1)
BMux.03:         5(1)
BMux.03!:        5(1)
BMux.04:         6(1)
BMux.04!:        6(1)
BMux.05:         7(1)
BMux.05!:        7(1)
BMux.06:         8(1)
BMux.06!:        8(1)
BMux.07:         9(1)
BMux.07!:        9(1)
BMux.16!:       27(1)
Bmux0:          15(1)   29(1)
Bmux0%:         15(1)
Bmux0':         15(1)
Bmux0'%:        15(1)
Bmux1:          15(1)   29(1)
Bmux1%:         15(1)
Bmux1':         15(1)
Bmux1'%:        15(1)
BmuxEn':        15(1)   29(1)
BmuxIn':         2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                 8(1)    9(1)   15(1)
BNTGtCT%:       30(1)
BNTGtCT'a!%:    30(1)
BSEL.0':        15(1)
BSel.0'a:       15(2)
BSel.0a:        15(4)   17(2)
BSEL.1':        15(1)
BSel.1'a:       15(3)   17(2)
BSel.1a:        15(2)   18(1)
BSEL.2':        15(1)
BSel.2'a:       15(2)   17(2)
BSel.2a:         2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                 8(1)    9(1)   14(1)   15(2)   18(1)
BSel=2/6:       14(2)   15(1)
BumpRSTK:       22(1)
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B←Ext:          15(1)   29(1)
B←Ext':         15(1)   17(2)
CkMdParity':    27(1)   29(1)
CLK.ph'%:       30(1)
CLKEnable'c!%:  30(1)
Clock0'Aa:      26(1)
Clock0'Aa%:     30(1)
Clock0'Ad:      16(1)
Clock0'Ad%:     30(1)
Clock0'Bb:      22(1)
Clock0'Bb%:     30(1)
Clock0'Bc:      12(1)   30(1)
Clock0'Bc%:     30(1)
Clock0'Da:      11(1)   20(1)
Clock0'Da%:     30(1)
Clock0'Dc:      12(1)   25(1)
Clock0'Dc%:     30(1)
Clock0'Dd:      27(1)
Clock0'Dd%:     30(1)
Clock0En'%:     30(1)
Clock1'Ac:      14(1)   15(2)   16(1)   19(1)
Clock1'Ac%:     30(1)
Clock1'Ba:      10(1)   20(2)
Clock1'Ba%:     30(1)
Clock1'Bb:      14(2)   20(1)
Clock1'Bb%:     30(1)
Clock1'Ca:      12(1)   17(1)
Clock1'Ca%:     30(1)
Clock1'Cb:      11(1)
Clock1'Cb%:     30(1)
Clock1'Cd:      25(1)
Clock1'Cd%:     30(1)
Clock1'Da:      23(1)   27(1)
Clock1'Da%:     30(1)
Clock1'Dc:      24(1)   25(1)   27(1)
Clock1'Dc%:     30(1)
Clock1Bd:       20(1)
Clock1Bd%:      30(1)
Cnt.00':         2(1)   17(1)
Cnt.01':         3(1)   17(1)
Cnt.02':         4(1)   17(1)
Cnt.03':         5(1)   17(1)
Cnt.04':         6(1)   17(1)
Cnt.05':         7(1)   17(1)
Cnt.06':         8(1)   17(1)
Cnt.07':         9(1)   17(1)
Cnt=Zero':      17(1)   29(1)
CntClock':      17(1)
CntClock'%:     30(1)
Curr.0':        12(3)
Curr.1':        12(3)
Curr.2':        12(3)
Curr.3':        12(3)
Curr=Next':     12(1)   23(1)   24(1)   29(1)
CurrLast.0':    11(1)   12(2)   21(1)   29(1)
CurrLast.1':    11(1)   12(2)   21(1)   29(1)
CurrLast.2':    11(1)   12(2)   21(1)   29(1)
CurrLast.3':    11(1)   12(2)   21(1)   29(1)
dAmux0:         14(2)
dAmux1':        14(1)
DblClock'Da:    12(1)
DblClock'Da%:   30(1)
dBmux0:         15(1)
dBmux1:         15(1)
ddR.00:          2(1)   10(1)
DMadr.01:       28(2)
DMadr.02:       28(3)
DMadr.03:       28(3)
DMadr.04:       28(3)
DMadr.05:       28(3)
DMadr.06:       28(3)
DMadr.07:       28(3)
DMadr.08:       28(3)
DMadr.09:       28(2)   29(16)
DMadr.10:       28(2)   29(16)
DMadr.11:       28(2)   29(16)
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dMD.00:          2(1)   10(1)
dMD.01:          3(1)
dMD.02:          4(1)
dMD.03:          5(1)
dMD.04:          6(1)
dMD.05:          7(1)
dMD.06:          8(1)
dMD.07:          9(1)
dMD.16:         10(1)
DMData:          2(1)   28(1)
DMuxClk!:       28(1)
DMuxData:       28(1)
DMuxData!:      28(1)
dPmux0:         16(1)
dPmux1:         16(1)
dPmux2:         16(2)
dR.00:           2(1)
dR.01:           3(1)
dR.02:           4(1)
dR.03:           5(1)
dR.04:           6(1)
dR.05:           7(1)
dR.06:           8(1)
dR.07:           9(1)
dRm.00:          2(1)   27(1)
dRm.01:          3(1)   27(1)
dRm.02:          4(1)   27(1)
dRm.03:          5(1)   27(1)
dRm.04:          6(1)   27(1)
dRm.05:          7(1)   27(1)
dRm.06:          8(1)   27(1)
dRm.07:          9(1)   27(1)
DsMd:           10(3)
DsPd:           10(3)
DsRd:           10(3)
dT.00:           2(1)
dT.01:           3(1)
dT.02:           4(1)
dT.03:           5(1)
dT.04:           6(1)
dT.05:           7(1)
dT.06:           8(1)
dT.07:           9(1)
dTm.00:          2(1)   27(1)
dTm.01:          3(1)   27(1)
dTm.02:          4(1)   27(1)
dTm.03:          5(1)   27(1)
dTm.04:          6(1)   27(1)
dTm.05:          7(1)   27(1)
dTm.06:          8(1)   27(1)
dTm.07:          9(1)   27(1)
EMU':           11(1)   12(1)   29(1)
FA=0':          13(1)
FA=0'a:         11(1)   13(1)   14(1)   16(2)   17(2)   29(1)
FA=0'b:         11(1)   13(1)   14(2)   22(1)
FA=1'!:         13(1)
FA=1'a:         13(1)   14(1)   15(1)   17(2)   18(1)   23(1)
                24(1)   26(1)   29(1)
FA=2'a:         11(1)   13(1)   16(3)   17(1)   23(1)   24(2)
                29(1)
FA=3':          13(1)   17(1)   24(1)   29(1)
FB=0':          13(1)   24(2)
FB=2':          13(1)   14(4)
FB=3':          11(1)   13(1)   14(2)   15(1)   16(1)   24(1)
FB=4':          13(1)   17(1)   23(1)
FB=5':          13(1)   17(2)   18(2)   23(1)   24(2)   26(1)
FB=6':          13(1)   16(4)
FB=7':          11(3)   13(1)   16(3)   17(3)   20(1)
FC=0':          13(1)   17(1)
FC=1':          13(1)   17(1)
FC=2':          11(1)   13(1)   16(1)   17(1)   23(1)
FC=2/3':        11(1)   13(1)   14(1)   16(1)
FC=3':          13(1)   17(2)
FC=4':          13(1)   14(1)   26(1)
FC=4/5':        13(1)   16(1)
FC=5':          13(1)   14(1)   18(1)   20(1)   24(1)
```

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FC=6':          11(1)   13(1)   15(1)   17(1)
FC=6/7':        13(1)   16(1)   17(1)   18(1)
FC=7':          13(1)   16(1)   18(1)   24(2)
FF.0:           13(2)
FF.0a:           2(1)   13(1)   17(1)
FF.0mem:        13(1)   29(1)
FF.0mem':       13(1)   14(1)
FF.1:           13(1)
FF.1a:           3(1)   13(1)
FF.1mem:        13(1)   14(1)   29(1)
FF.2:           13(1)
FF.2!:          13(1)
FF.2'a:         13(1)   15(1)   17(1)   22(1)
FF.2a:           4(1)   13(1)   14(2)   24(1)
FF.3:           13(1)
FF.3!:          13(1)
FF.3'a:         13(1)   15(1)
FF.3a:           5(1)   13(1)   14(2)   17(1)   22(1)   25(1)
FF.4:           13(1)
FF.4!:          13(1)
FF.4a:           6(1)   13(1)   18(1)   22(1)   25(1)
FF.5:           13(1)
FF.5!:          13(1)
FF.5'a:         13(2)   24(1)
FF.5a:           7(1)   13(2)   14(2)   16(1)   18(1)   22(1)
                24(1)   25(1)
FF.6:           13(1)
FF.6!:          13(1)
FF.6'a:         13(2)   16(1)
FF.6a:           8(1)   13(2)   18(1)   22(1)   24(1)   25(1)
FF.7:           13(1)
FF.7!:          13(1)
FF.7'a:         13(1)   14(1)
FF.7a:           9(1)   11(1)   13(1)   16(1)   18(1)   22(1)
                24(1)   25(1)
FFdly.3:        25(2)
FFdly.4:        23(1)   25(2)
FFdly.5:        11(2)   23(1)   25(2)
FFdly.6:        11(2)   17(1)   23(1)   25(3)
FFdly.7:        11(2)   23(1)   25(3)   27(1)
FFok'a:         13(4)   14(1)   29(1)
FFshift':       15(1)   18(1)   29(1)
Freeze:         11(1)   26(1)
GND:            26(1)
Gnd:             2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                 8(1)    9(1)   10(1)   11(1)   12(1)   13(1)
                14(1)   15(1)   16(1)   17(1)   18(1)   19(1)
                20(1)   21(1)   22(1)   23(1)   24(1)   25(1)
                26(1)   27(1)   28(1)   29(1)   30(1)
Hold:           23(1)   30(2)
Hold%:          30(1)
Hold':          30(1)
Hold'%:         30(1)
Holda:          29(1)   30(5)
HoldDly:        11(1)   20(1)   30(4)
IOatt!:         11(1)
IOatta:         11(1)   29(1)
IOB.00:          2(2)   27(1)
IOB.01:          3(2)   27(1)
IOB.02:          4(2)   27(1)
IOB.03:          5(2)   27(1)
IOB.04:          6(2)   27(1)
IOB.05:          7(2)   27(1)
IOB.06:          8(2)   27(1)
IOB.07:          9(2)   27(1)
IOB.16:         27(2)
IOB.Perr':      27(2)
IOBin':         16(1)   27(1)   29(1)
IOBout:         15(1)   27(1)   29(1)
IOPE:           27(1)
IOPerr:         27(1)   29(1)
Last.0':        12(1)
Last.1':        12(1)
Last.2':        12(1)
Last.3':        12(1)
Last=Curr':     11(1)   12(1)   20(1)   29(1)
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LastNext.0':    12(1)   23(1)   24(1)   29(1)
LastNext.0'%:   12(1)
LastNext.1':    12(1)   23(1)   24(1)   29(1)
LastNext.1'%:   12(1)
LastNext.2':    12(1)   23(1)   24(1)   29(1)
LastNext.2'%:   12(1)
LastNext.3':    12(1)   23(1)   24(1)   29(1)
LastNext.3'%:   12(1)
LC.0:           20(3)
LC.1:           20(1)
LC.1'a:         20(4)
LC.1a:          20(1)
LC.2:           20(2)
LdTaskSim':     26(1)   29(1)
LmaskEn':       16(1)   29(1)
LoadCnt':       17(1)   29(1)
MAR.00'!0:       2(1)
MAR.00'!1:       2(1)
MAR.00'!2:      29(1)
MAR.01'!0:       3(1)
MAR.01'!1:       3(1)
MAR.01'!2:      29(1)
MAR.02'!0:       4(1)
MAR.02'!1:       4(1)
MAR.02'!2:      29(1)
MAR.03'!0:       5(1)
MAR.03'!1:       5(1)
MAR.03'!2:      29(1)
MAR.04'!0:       6(1)
MAR.04'!1:       6(1)
MAR.04'!2:      29(1)
MAR.05'!0:       7(1)
MAR.05'!1:       7(1)
MAR.05'!2:      29(1)
MAR.06'!0:       8(1)
MAR.06'!1:       8(1)
MAR.06'!2:      29(1)
MAR.07':        29(1)
MAR.07'!0:       9(1)
MAR.07'!1:       9(1)
MarMuxAEn':     29(1)
MarMuxAEn'%:    14(1)
MarMuxBEn'%:    14(2)
MBBypass:       24(2)   29(1)
MBdly.0:        25(2)
MBdly.1:        25(2)
MBdly.2:        25(2)
MBdly.3:        25(2)
MBdly.4':       25(2)
MBMux0:         24(2)   29(1)
MBMux1:         24(2)   29(1)
MBSelB:         24(2)
MBWrite':       24(1)
MBWrite'%:      30(1)
MBWriteEn':     24(1)   29(1)   30(1)
MB←Ifu.0:       24(1)   25(1)
MB←Ifu.1:       24(1)   25(1)
MB←Ifu.2:       24(1)   25(1)
MB←Ifu.3:       24(1)   25(1)
MB←Ifu.4:       24(1)   25(1)
Md.00:           2(2)   27(1)
Md.01:           3(2)   27(1)
Md.02:           4(2)   27(1)
Md.03:           5(2)   27(1)
Md.04:           6(2)   27(1)
Md.05:           7(2)   27(1)
Md.06:           8(2)   27(1)
Md.07:           9(2)   27(1)
Md.16:          10(1)   27(1)
Md.Perr':       27(2)
MdPE:           27(1)
MdPerr:         27(1)   29(1)
MemBase.0:      25(1)
MemBase.0':      5(1)   25(1)
MemBase.1:      25(1)
MemBase.1':      6(1)   25(1)
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MemBase.2!:     25(1)
MemBase.2':      7(1)   25(1)
MemBase.3!:     25(1)
MemBase.3':      8(1)   25(1)
MemBase.4:      25(1)
MemBase.4':      9(1)   25(1)
MemBM.0:        24(1)
MemBM.1:        24(1)
MemBM34:        24(1)
MemBX.0:         3(1)   24(1)   25(1)
MemBX.1:         4(1)   24(1)   25(1)
MemBXClock':    24(1)
MemBXClock'%:   30(1)
MidasEn.01F.02F.03T.08F':       28(1)
MidasEn.04F':   28(1)   29(8)
MidasEn.04T':   28(1)   29(8)
MuxData0:       28(1)   29(2)
MuxData1:       28(1)   29(2)
MuxData2:       28(1)   29(2)
MuxData3:       28(1)   29(2)
MuxData4:       28(1)   29(2)
MuxData5:       28(1)   29(2)
MuxData6:       28(1)   29(2)
MuxData7:       28(1)   29(2)
Next.0!:        12(1)
Next.0':        12(3)
Next.1!:        12(1)
Next.1':        12(3)
Next.2!:        12(1)
Next.2':        12(3)
Next.3!:        12(1)
Next.3':        12(3)
NextData':      13(1)   29(1)
NextMacro:      24(1)   29(1)
Overflow':      11(2)   29(1)
pClock1En'%:    30(1)
Pdata.00:        2(2)   10(1)   29(1)
Pdata.00%:      11(1)
Pdata.01:        3(2)
Pdata.02:        4(2)
Pdata.03:        5(2)
Pdata.04:        6(2)   29(1)
Pdata.05:        7(2)
Pdata.06:        8(2)
Pdata.07:        9(2)
Pdata.15%:      11(1)
Pmux0:           2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                 8(1)    9(1)   16(1)   29(1)
Pmux1:           2(1)    3(1)    4(1)    5(1)    6(1)    7(1)
                 8(1)    9(1)   16(1)   29(1)
Pmux2:          16(1)   29(1)
PostClock0'Bc:  23(1)
PostClock0'Bc%: 30(1)
ppClk'a%:       30(1)
ppClk'b%:       30(1)
ppClk'c%:       30(1)
PreClock0'A:    30(1)
PreClock0'A%:   30(1)
PreClock0'B:    30(3)
PreClock0'B%:   30(1)
PreClock0'C:    30(2)
PreClock0'C%:   30(1)
PreClock0'D:    30(2)
PreClock0'D%:   30(1)
PreClock1'A:    30(3)
PreClock1'A%:   30(1)
PreClock1'B:    10(3)
PreClock1'B%:   30(1)
PreClock1'C:    30(1)
PreClock1'C%:   30(1)
PreClock1'D:    30(3)
PreClock1'D%:   30(1)
PreClock1B:     30(1)
PreClock1B%:    30(1)
PreDblClock'D:  30(1)
PreDblClock'D%: 30(1)
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```
PreFA=0:          13(2)
PreFA=1':         13(1)   14(1)
PreSHCP'A:        14(1)   15(1)
PreSHCP'A%:       30(1)
PreSHCP'B:        20(2)
PreSHCP'B%:       30(1)
PreSHCP'C:        12(1)   30(1)
PreSHCP'C%:       30(1)
PreSHCP'Shc:      18(1)
PreSHCP'Shc%:     30(1)
PreSHSelect'D:    22(1)
PreSHSelect'D%:   30(1)
PRhold%:          30(1)
PropCnt':         17(1)   29(1)
Q.00:              2(4)   11(2)   17(1)
Q.01:              3(4)   17(1)
Q.02:              4(4)   17(1)
Q.03:              5(4)   17(2)
Q.04:              6(4)   17(1)
Q.05:              7(4)   17(1)
Q.06:              8(4)   17(1)
Q.07:              9(4)   17(1)
Q.08:             17(1)
QClock':          17(1)
QClock'%:         30(1)
QshiftL':         17(1)   29(1)
QshiftR':         17(1)   29(1)
R.00:              2(4)   27(1)
R.00%:             2(1)
R.01:              3(4)   27(1)
R.01%:             3(1)
R.02:              4(4)   27(1)
R.02%:             4(1)
R.03:              5(4)   27(1)
R.03%:             5(1)
R.04:              6(4)   27(1)
R.04%:             6(1)
R.05:              7(4)   27(1)
R.05%:             7(1)
R.06:              8(4)   27(1)
R.06%:             8(1)
R.07:              9(4)   27(1)
R.07%:             9(1)
R.Perr':          27(2)
RamPE:            27(1)
RbAdr.0%:         21(1)
RbAdr.1%:         21(1)
RbAdr.2%:         21(1)
RbAdr.3%:         21(1)
RbAdr.4'%:        21(1)   22(1)
RbAdr.5'%:        21(1)   22(1)
RbAdr.6'%:        21(1)   22(1)
RbAdr.7'%:        21(1)   22(1)
RbBypass:         10(1)
RbBypass':        10(2)   20(1)
RbBypassDly:      20(1)   27(1)   29(1)
RbSelMd:          10(1)   20(2)   29(1)
RbSelMd':         10(1)   20(1)
RbWadr.4:         22(1)
RbWadr.5:         22(1)
RbWadr.6:         22(1)
RbWadr.7:         22(1)
RbWrite'a:        21(2)
RbWrite'a%:       30(1)
RbWrite'b:        21(2)
RbWrite'b%:       30(1)
RbWrite'c:        21(2)
RbWrite'c%:       30(1)
RbWriteEn':       20(1)   29(1)   30(1)
RepeatCurrB:      23(1)
RepeatCurrB%:     30(1)
RepeatCurrC:      12(2)   29(1)
RepeatCurrC%:     30(1)
RepeatCurrD:      25(1)
RepeatCurrD%:     30(1)
ReSchedWr':       11(1)
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ReSchedWr'%:    30(1)
ReSchedWrEn':   11(1)   29(1)   30(1)
ResEqZero':     11(1)   29(1)
ResLtZero':     11(1)   29(1)
RisIFdata:      13(1)   14(1)   20(1)   27(1)   29(1)
RmaskEn':       16(1)   29(1)
RmLtZero':      29(1)
RmLtZero'%:     10(1)
RmPerr:         27(1)   29(1)
Rparity:        27(1)
RSTK.0%:        22(1)
RSTK.1%:        22(1)
RSTK.2%:        22(1)
RSTK.3%:        22(1)
SelectRm'a:     21(3)
SelectStk'a:    21(3)
ShA.00:         19(4)
ShA.00%:         2(1)
ShA.01:         19(3)
ShA.01%:         3(1)
ShA.02:         19(3)
ShA.02%:         4(1)
ShA.03:         19(2)
ShA.03%:         5(1)
ShA.04:         19(2)
ShA.04%:         6(1)
ShA.05:         19(1)
ShA.05%:         7(1)
ShA.06:         19(1)
ShA.06%:         8(1)
ShA.07%:         9(1)
ShA.08:         19(5)
ShA.09:         19(4)
ShA.10:         19(5)
ShA.11:         19(4)
ShA.12:         19(5)
ShA.13:         19(4)
ShA.14:         19(5)
ShA.15:         19(4)
ShB.00:         19(1)
ShB.00%:         2(1)
ShB.01:         19(1)
ShB.01%:         3(1)
ShB.02:         19(2)
ShB.02%:         4(1)
ShB.03:         19(2)
ShB.03%:         5(1)
ShB.04:         19(3)
ShB.04%:         6(1)
ShB.05:         19(3)
ShB.05%:         7(1)
ShB.06:         19(4)
ShB.06%:         8(1)
ShB.07:         19(4)
ShB.07%:         9(1)
Shc.00:          2(1)   18(1)
Shc.01:          3(1)   18(1)
Shc.02:          4(1)   19(1)
Shc.02%:        18(1)
Shc.03:          5(1)   19(1)
Shc.03%:        18(1)
Shc.04a:         6(1)   18(1)   19(3)
Shc.04b:        18(1)
Shc.05a:         7(1)   18(1)   19(3)
Shc.05b:        18(1)
Shc.06a:         8(1)   18(1)   19(3)
Shc.06b:        18(1)
Shc.07a:         9(1)   18(1)   19(1)
Shc.07b:        18(1)
Shc.08:         16(1)
Shc.09:         16(1)
Shc.10:         16(1)
Shc.11:         16(1)
Shc.12:         16(1)
Shc.13:         16(1)
Shc.14:         16(1)
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T.Perr':        27(2)
Task2Bk.0':     12(1)   29(1)
Task2Bk.1':     12(1)   29(1)
TAsk2Bk.2':     12(1)   29(1)
Task2Bk.3':     12(1)   29(1)
Task3Bk.0':     12(1)   29(1)
Task3Bk.1':     12(1)   29(1)
Task3Bk.2':     12(1)   29(1)
Task3Bk.3':     12(1)   29(1)
TbBypass:       20(1)   27(1)   29(1)
TbSelMd:        20(2)   29(1)
TbWrite'a:      21(1)
TbWrite'a%:     30(1)
TbWrite'b:      21(1)
TbWrite'b%:     30(1)
TbWriteEn':     20(2)   29(1)   30(1)
TempRef!:       26(1)
TempSense:      29(1)
TempSense!:     26(1)
TestTW:         26(1)
TIOA.0:         23(1)
TIOA.1:         23(1)
TIOA.2:         23(1)
TIOA.3:         23(1)
TIOA.4:         23(1)
TIOA.5:         23(1)
TIOA.6:         23(1)
TIOA.7:         23(1)
TIOABypass:     23(1)   29(1)
TIOABypass%:    23(1)
TIOAdly.0:       2(1)   23(2)
TIOAdly.1:       3(1)   23(2)
TIOAdly.2:       4(1)   23(2)
TIOAdly.3:       5(1)   23(2)
TIOAdly.4:       6(1)   23(2)
TIOAdly.5:       7(1)   23(1)
TIOAdly.6:       8(1)   23(1)
TIOAdly.7:       9(1)   23(1)
TIOAWrite':     23(1)
TIOAWrite'%:    30(1)
TIOAWriteEn':   23(1)   29(1)   30(1)
TisIFdata:      13(1)   14(1)   20(1)   27(1)   29(1)
TmPerr:         27(1)   29(1)
Tparity:        27(1)
TrueA:           2(1)   26(1)   27(3)   30(1)
VCC:            26(1)
VEE:            26(1)
VTT:            28(1)
Whatever:       26(1)   28(1)
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