9000A-6802
Interface Pod

Instruction Manual

FLUKE®

NOTE

This manual documents the Model 9000A-6802 and its assemblies at the revision levels identified in Section 6. If your instrument contains assemblies with different revision letters, it will be necessary for you to either update or backdate this manual. Refer to the supplemental change/errata sheet for newer assemblies, or to the backdating information in Section 6 for older assemblies.

9000A-6802
Interface Pod

Instruction Manual

P/N 649392
MAY 1982

FLUKE®

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John Fluke Mfg. Co., Inc., P.O. Box C9090, Everett, Washington 98206

Rev. 6/81

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Section 1
Introduction

1-1. PURPOSE OF INTERFACE POD

The purpose of the 9000-6802 Interface Pod, hereafter referred to as the pod, is to interface any 9000 Series Micro System Troubleshooter to a piece of equipment employing a 6802, a 6808, or a 6802NS microprocessor.

The 9000 Series Micro System Troubleshooters are designed to service printed circuit boards, instruments and systems employing bus-oriented microprocessors. While the architecture of the troubleshooter main frame is general in nature and is designed to accomodate processors with up to 32 address lines and 32 data lines, the interface pod adapts the general purpose arclitecture of the 9000 Series to a specific microprocessor, or microprocessor family. The interface pod adapts the 9000 Series to microprocessor-specific functions such as pin layout, status/control functions, interrupt handling, timing, size of memory space, and size of I/O space.

1-2. DESCRIPTION OF INTERFACE POD

The pod consists of a pair of printed circuit board assemblies mounted within a small break-resistant case. A shielded 24-conductor cable connects the printed circuit boards to the troubleshooter; a ribbon cable and connector provide connection to the unit under test, hereafter referred to as the UUT.

Figure 1-1 shows the relationship of the pod to the troubleshooter and to the UUT. Connection from the pod to the troubleshooter is via a front-mounted 25-pin connector. Connection to the UUT is made by plugging the ribbon cable plug directly into the microprocessor socket. The UUT microprocessor socket gives the troubleshooter direct access to all system components which normally communicate with the microprocessor.

The pod contains a 6802 microprocessor and the supporting hardware and control software required to:

- Perform handshaking with the troubleshooter
- Receive and execute commands from the troubleshooter
- Report UUT status to the troubleshooter
- Emulate the UUT microprocessor

The pod is powered by the troubleshooter, but is clocked by the UUT clock signals. Using the UUT clock signals allows the troubleshooter and pod to operate at the designed operating speed of the UUT.

Logic level detection circuits are provided on each line to the UUT. These circuits allow detection of bus shorts, stuck-high or stuck-low conditions, and any bus drive conflict (two or more drivers attempting to drive the same bus line).

Over-voltage protection circuits are also provided on each line to the UUT. These circuits guard against pod damage which could result from:

- Incorrectly inserting the ribbon cable plug in the UUT microprocessor socket.
- UUT faults which place potentially damaging voltages on the UUT microprocessor socket.

The over-voltage protection circuits guard against voltages of +12 to -7 volts on any one pin. Multiple faults, especially of long duration, may cause pod damage.

A power level sensing circuit constantly monitors the voltage level of the UUT power supply (+5V). If UUT power rises above or drops below an acceptable level, the pod notifies the troubleshooter of the power fail condition.

A self test socket provided on the pod enables the troubleshooter to check pod operation. The self test socket is a 40-pin zero-insertion force type connector. The ribbon cable plug must be connected to the self test socket during self test operation. The ribbon cable plug should also be inserted into this socket when the pod is not in use to provide protection for the plug.

1-3. SPECIFICATIONS

Specifications for the 9000A-6802 Interface Pod are listed in Table 1-1.

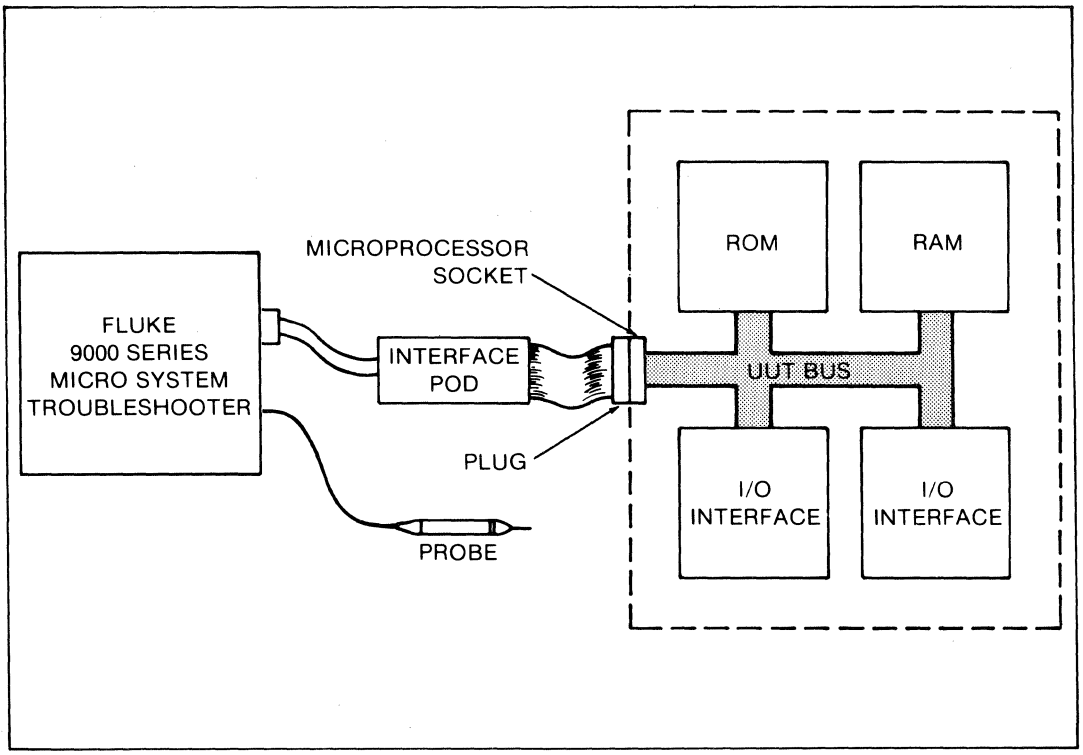


Figure 1-1. Interface Pod with Troubleshooter and UUT

Table 1-1. 6802 Interface Pod Specifications

ELECTRICAL PERFORMANCE	
Power Dissipation	3.0 watts maximum
Electrical Protection	
CLOCK INPUTS VCC STANDBY	-0.3 to +5.5 volts may be applied between these ribbon cable plug pins and ground continuously as long as the pod is powered by the troubleshooter.
OTHER SIGNALS	-7 to +12 volts may be applied between any other ribbon cable plug pin continuously as long as the pod is powered by the troubleshooter.
MICROPROCESSOR SIGNALS	
Input Low Voltage	0V min., +0.8V max.
Input High Voltage	+2.0V min., +5.0V max.
Output Low Voltage	+0.4V max. with Iol = 1.6 mA
Output High Voltage	+2.4V min. with Ioh = -250 μA
Tristate Output Leakage Current	+20 μA
High Level Input Current	20 μA typ. with Vih = +2.7V
Low Level Input Current	
RE, $\overline{\text{RESET}}$, $\overline{\text{HALT}}$, MR, $\overline{\text{NMI}}$	-400 μA max. with Vil = +0.4V
ALL OTHER INPUT LINES	-20 μA typ. with Vil = +0.4V
TIMING CHARACTERISTICS	
Maximum Clock Frequency	2.0 MHz typ.
Added Delays to 6802 Signals	
LOW-TO-HIGH TRANSITIONS	20 ns typ.
HIGH-TO-LOW TRANSITIONS	24 ns typ.
UUT POWER DETECTION	
Detection of Low Vcc Fault	Vcc or Vcc Standby < +4.5V detected
Detection of High Vcc Fault	Vcc or Vcc Standby > +5.5V detected
GENERAL	
Size	3.3 cm High x 10.2 cm Wide x 18.55 cm Deep (1.3 in High x 4.0 in Wide x 7.4 in Deep)
Weight	0.68 kg (1.5 lbs)

Table 1-1. 6802 Interface Pod Specifications (cont)

Environment	
STORAGE	-40° to +70°C, RH < 95%
OPERATING	0° to +25°C, RH < 95% +25° to +40°C, RH < 75% +40° to +50°C, RH < 45%
Protection Class 3	Relates solely to insulation or grounding properties defined in IEC 348.

Section 2
Installation

2-1. GENERAL

Before a 9000 Series Micro System Troubleshooter can be used to perform any testing or fault isolation, it must be connected to the UUT. Connection is madehooting information.

2-2. MAKING CONNECTIONS

Before making any connections to the UUT, take note of the following precautions:

WARNING

TO PREVENT POSSIBLE HAZARDS TO THE OPERATOR OR DAMAGE TO THE UUT, DISCONNECT ALL HIGH-VOLTAGE POWER SUPPLIES, THERMAL ELEMENTS, MOTORS, OR MECHANICAL ACTUATORS WHICH ARE CONTROLLED OR PROGRAMMED BY THE UUT MICROPROCESSOR BEFORE CONNECTING POD.

- Be sure to install the ribbon cable plug correctly in the UUT microprocessor socket.
- The self test socket is intended for use with the ribbon cable plug only. Do not insert any microprocessor removed from a UUT under test, or any other device into this socket.

Connect the pod between the troubleshooter and the UUT as follows:

1. Remove power from the UUT. Remove power from the troubleshooter.
2. Using the round shielded cable, connect the pod to the troubleshooter connector shown in Figure 2-1. Secure the connector using the sliding collar.
3. Apply power to the troubleshooter.
4. Perform a self-test of the pod as described in Section 5 of this manual.
5. With UUT power off, unplug the microprocessor from the UUT.
6. On the pod, turn the self test socket thumbwheel to release the plug from the self test socket.
7. Align the ribbon-cable with the microprocessor socket on the UUT so that the notched corner of the ribbon cable plug aligns with pin 1 of the socket. Insert the plug into the socket as shown in Figure 2-2.

8. Electrically reassemble the UUT. Use extender boards if necessary.

CAUTION

Ensure troubleshooter power is on before turning UUT power on in order to activate pod protection circuits.

9. Apply power to the troubleshooter and the UUT.

2-3. POWER CONNECTIONS

The pod receives +5 volts, -5 volts, and +12 volts from the 9000 Series Micro System Troubleshooter. No external power connections are required.

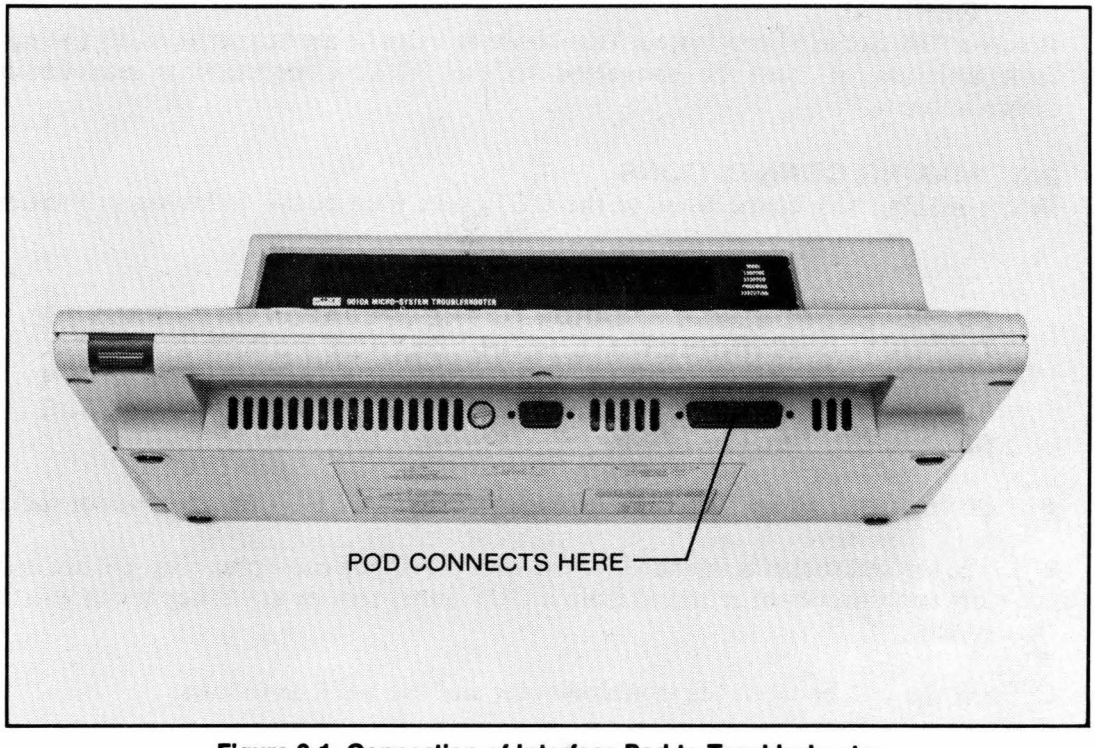


Figure 2-1. Connection of Interface Pod to Troubleshooter

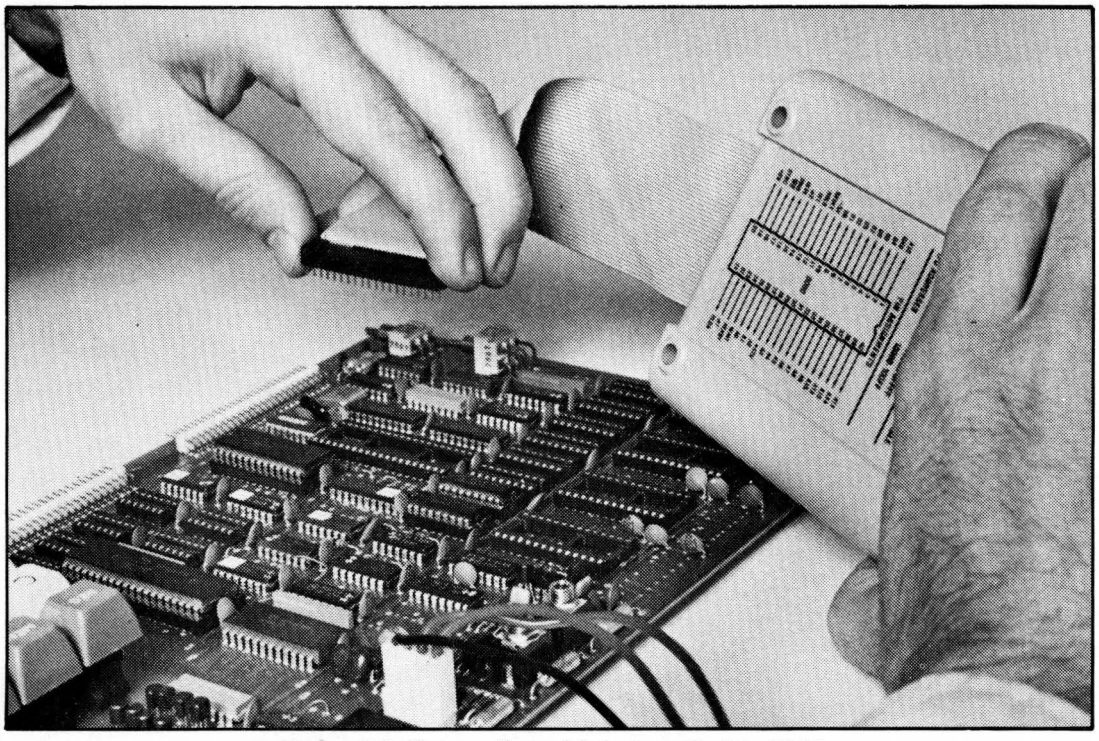


Figure 2-2. Connection of Interface Pod to UUT

Section 3
Microprocessor Data

3-1. INTRODUCTION

This section contains information which may be useful during operation of the troubleshooter. This information includes 6802 signal descriptions, explanations of status/control lines and address space assignment, the effects the pod may have on normal UUT operation, the pod capabilities and limitations, and pertinent pod characteristics.

3-2. 6802 SIGNALS

For reference, Table 3-1 lists all of the 6802 signals and provides a brief description of each. Figure 3-1 shows the pin assignment of 6802 signals.

3-3. STATUS/CONTROL LINES AND ADDRESS SPACE ASSIGNMENTS

3-4. Introduction

The 9000A Series Micro System Troubleshooters are designed to accomodate bus-oriented processors having up to 32 address lines, 32 data lines, 16 status lines, and 8 control lines. The pod provides an interface between the general architecture of the 9000 Series and the specific requirements of the 6802 microprocessor. As part of this interface task, the pod makes specific assignments between the microprocessor lines and the 9000 Series troubleshooter. These assignments include:

- Bit number assignment of 6802 status lines
- User-writeable control lines
- Bit number assignment of control lines
- Address space assignment
- Pin assignments

These assignments are described in the following paragraphs and are summarized for convenience on the pod decal.

3-5. Bit Assignment - Status Lines

When a read status (READ @ STS) operation is performed, the troubleshooter displays the result in binary form, where a "1" indicates a logic high status line and a "0" indicates a logic low status line. To determine which characters of the display correspond to specific status lines, refer to Table 3-2. This table shows that each line is assigned a bit number. Bit number zero ($\overline{\text{HALT}}$) appears at the far right of the display, while bit number 7 (PWR FAIL) appears at the far left side.

Table 3-1. 6802 Signals

SIGNAL NAME	DESCRIPTION
A0 - A15	The 16 address lines are designated A0 through A-15.
D0 - D7	The eight data lines are designated D0 through D7.
$\overline{\text{HALT}}$	The halt line is an input which, when made low, causes the 6802 to stop operation upon completion of the current instruction. In the halt mode, the BA line is high, VMA is low, and the address lines contain the address of the next instruction.
BA	The bus available line is made high by the 6802 when halted, by active Halt signal or a Wait instruction, to indicate that the address bus is available (but not in a tri-state condition).
VMA	The valid memory address line is made high by the 6802 when a valid address is present on the address lines.
R/$\overline{\text{W}}$	The read/write line is made high by the 6802 when in a read mode, and low when in a write mode. The state of the read/write line is high (read) when in the normal standby mode and also when the 6802 is halted.
$\overline{\text{IRQ}}$	The interrupt request line is an input which, when made low, requests an interrupt to the 6802. If interrupts are enabled and the 6802 is not in the Halt state, the interrupt is acknowledged at the end of the instruction currently being executed.
$\overline{\text{NMI}}$	A low-going signal on the non-maskable interrupt line initiates a non-maskable interrupt routine within the 6802 upon completion of the current instruction.
$\overline{\text{RESET}}$	The reset line is an input which requires a low level for three clock cycles or longer. On the low-to-high transition, a restart sequence is begun which sets the program counter and disables the maskable interrupt.
RE	The RAM enable line is an input which controls the on-board RAM. When the RAM enable line is made high, the on-board RAM is enabled to respond to 6802 operations. When the RAM enable line is made low, the on-board RAM is disabled. When the RAM enable line is not used, it is usually tied high or low, as required.
EXTAL	The external clock/crystal input connects to an external clock source when an external clock is employed, or to one side of a crystal when the internal clock circuit of the 6802 is employed.
XTAL	The crystal input connects to one side of a crystal when the internal clock circuit of the 6802 is employed. When using an external clock, the crystal input is tied low.
E	The enable output supplies a single-phase clock signal from the internal clock to the remainder of the system.
MR	The memory ready input provides for controlling the stretching of the enable (E) output to accommodate slow memory or peripheral devices. This input is usually tied high when unused.
VCC Standby	The VCC standby input accepts 5V dc to retain the first 32 bytes of internal RAM during power-up, power-down, and standby conditions.

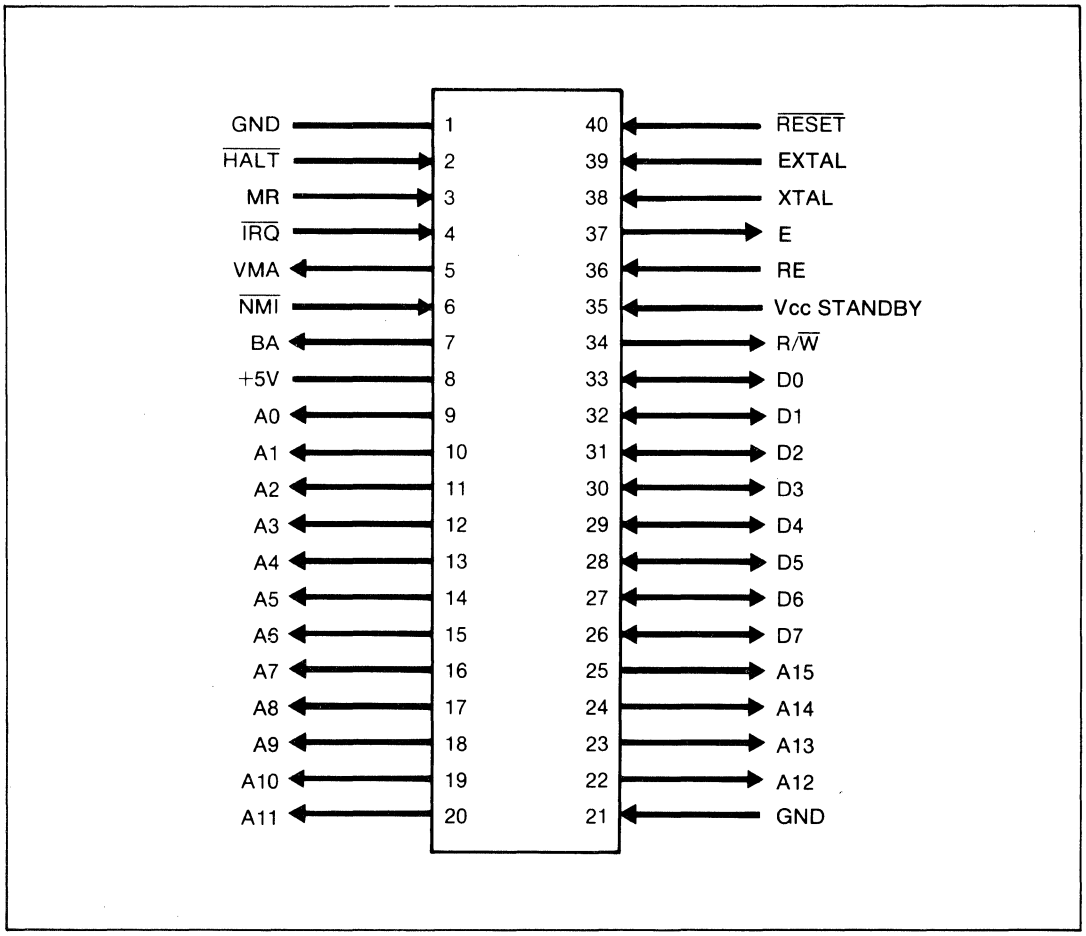


Figure 3-1. 6802 Pin Assignments

Table 3-2. Status and Control Lines Bit Assignments

STATUS LINES		CONTROL LINES	
BIT NO.	**SIGNAL**	**BIT NO.**	**SIGNAL**
7	PWR FAIL	7	VMA
6	—	6	—
5	RE	5	—
4	**$\overline{\text{RESET}}$	4	R/$\overline{\text{W}}$
3	$\overline{\text{IRQ}}$	3	—
2	$\overline{\text{NMI}}$	2	—
1	**MR	1	—
0	**$\overline{\text{HALT}}$	0	*BA

* User Writeable **Forcing Lines

For example, if the $\overline{\text{HALT}}$ (bit number 0) and PWR FAIL (bit number 7) lines are low, and all other status lines are high, the troubleshooter would read *READ @ STS = 0011 1110 OK.* Bit numbers 0 ($\overline{\text{HALT}}$) and 7 (PWR FAIL) are zero to indicate a logic low, while other meaningful bits are ones to indicate logic high. Bit 6, which has no meaning as a 6802 status line, is always represented by zero in the troubleshooter display message.

3-6. User-Writeable Control Lines

The 6802 has a control line which the troubleshooter can write to. This is the BA line. To write to the BA line, a write control function is used as described in the paragraphs that follow. Note that writing to a control line only sets the line to the high or low state for approximately 40 clock cycles; just long enough to verify that it can be driven.

3-7. Bit Assignment - Control Lines

There are two troubleshooting functions which require the entry of binary digits to identify user-writable control lines. These functions are write control (WRITE @ CTL) and data toggle control (DTOG @ CTL).

When performing or programming either of these two functions, the user is prompted for a binary number to identify the control line(s) to be written. Since the 6802 is equipped with only one user-writeable control line, BA, the binary number 1 or 0 is entered in response to the prompt. Entry of a 1 at bit number zero writes the BA line high, while entry of a 0 at bit number zero writes the BA line low.

If any control line cannot be driven, the troubleshooter responds with the message *CTRL ERR @ xxxxxxxx LOOP?,* where x equals a binary 1 if that line cannot be driven. For example, if in the write control operation, the BA line cannot be driven, the troubleshooter displays the message *CTRL ERR @ 00000001 LOOP?.* The binary 1 indicates that the BA line cannot be driven.

The troubleshooter message *CTL ERR xxxxxxxx-LOOP?* can also occur when performing a Bus Test, and various other troubleshooter operations. As in write control and data toggle control, x represents a binary number that identifies which lines can or cannot be driven. A binary 0 represents the ability to drive a line, while a binary 1 represents the inability to drive a line. Table 3-2 lists all control lines and their respective bit numbers.

3-8. Address Space Assignment

The 6802 is capable of addressing up to 65,536 memory locations. The 9000 Series troubleshooter uses a consistent technique of addressing multiple memory locations. In order to access one of the memory locations, the user provides a hexadecimal address in the range of 0000 to FFFF.

3-9. FORCING AND INTERRUPT LINES

Several troubleshooter messages are used to indicate errors and conditions associated with forcing lines and interrupts. Forcing lines are those lines which, when made active, force the microprocessor into some specific action. Forcing lines for the 6802 are $\overline{\text{HALT}}$, MR, and $\overline{\text{RESET}}$. Holding $\overline{\text{HALT}}$ or MR low could cause the pod to stop and timeout. Note that these three lines can be disabled during troubleshooter setup procedures. If the $\overline{\text{RESET}}$ line is pulled low, the pod reports such a condition to the troubleshooter, but pod operation is unaffected.

NOTE

During troubleshooter setup, disabling MR and $\overline{\text{HALT}}$ eliminates any effect they might have on troubleshooter/pod operation. Selecting the non-reporting

(not trapping) of forcing lines or interrupts during setup eliminates the corresponding troubleshooter message, but still allows such conditions to affect troubleshooter/pod operation.

Interrupt lines for the 6802 include $\overline{IRQ}$ and $\overline{NMI}$. The $\overline{IRQ}$ input is software disabled; the $\overline{NMI}$ input is hardware disabled except during operation in the Run UUT mode. When disabled, the $\overline{NMI}$ input is routinely checked by the pod software, and reported to the troubleshooter if held low by the UUT.

3-10. LINES ENABLED DURING TROUBLESHOOTER SETUP

During setup of the troubleshooter, the operator has the option of enabling or not enabling certain forcing lines as a means of preventing UUT faults from disabling the pod microprocessor. For the 6802 the $\overline{HALT}$ and MR lines may be enabled or disabled. Also during troubleshooter setup, the operator may elect to report (trap) or disregard active signals on the forcing lines. Reporting (trapping) active forcing lines halts troubleshooter operation in order to display the forcing line message.

3-11. OPERATION WITH UUTs WHICH USE INTERNAL 6802 RAM

The 6802 contains 128 bytes of internal RAM located at addresses 0000 through 007F. The interface pod supports the use of this RAM, however, the user should be aware of the following operating characteristics.

1. If a RAM Test is attempted on the internal RAM, the troubleshooter will indicate a R/$\overline{W}$ error on the display. This error indication is due to an attempt by the troubleshooter to perform a RAM test on the 6802 within the pod and not the 6802 normally installed on the UUT; and the 6802 in the pod does not require a RAM test.

2. If the RE (RAM enable) line is low, indicating that the internal RAM is not to be used, a RAM Test at addresses 0000 through 007F will access UUT memory space in a normal manner. However, when operating in the Run UUT mode, the internal RAM of the 6802 pod is available for the UUT to access without any restriction.

3-12. OPERATION WITH UUTs WHICH USE VCC STANDBY

The 6802 contains 32 bytes of internal RAM located at addresses 0000 through 001F. This RAM is powered by a separate power supply through the Vcc Standby input, pin 35. This supply also powers the RAM Enable (RE) logic. The interface pod supports this feature by connecting the Vcc Standby line directly out to the UUT.

When operating the troubleshooter in the Run UUT mode, power to the UUT may be applied and removed in order to test the operation of this RAM. Since the processor in the pod is powered by the troubleshooter and not the UUT, it will remain operative when UUT power is removed, but the internal RAM from 0000 to 001F will properly emulate a 6802 and track the condition of the Vcc Standby line.

3-13. CLOCK OPERATIONS

The 6802 microprocessor generates clock signal E from an external crystal/capacitor network connected between pins 38 and 39. If the internal clock generator is not used, a TTL-compatible clock at four times the desired system clock rate is typically applied to pin 39 of the 6802, while pin 38 is grounded.

The interface pod supports both of these clock configurations and contains a crystal oscillator which rejects the added capacitance of the ribbon cable to the UUT. The output of this pod oscillator, which can also be driven directly by a TTL clock signal from the

UUT, is fed directly to the 6802 contained within the pod. This allows a TTL clock source on the UUT to drive the 6802 within the pod. The pod depends on the integrity of this clock system for it to function properly. Should the pod appear inoperative when connected to the UUT, the troubleshooter will display *POD TIMEOUT - ATTEMPTING RESET;* the clock system should be checked first. Check the E output (pin 37) for a clean squarewave. If it is not, check the crystal inputs (Xtal, pin 38; and Extal, pin 39) for proper connections and verify that the E output is not shorted to ground.

3-14. MARGINAL UUT PROBLEMS

3-15. Introduction

The pod is designed to approximate, as closely as possible, the actual characteristics of the microprocessor it replaces in the UUT. However, the pod does differ in some respects. In general, these differences tend to make problems due to marginal UUTs more visible. A UUT may operate marginally with the actual microprocessor installed, but tend to exhibit errors with the pod plugged in. The pod differences tend to make marginal UUT problems more obvious and easier to troubleshoot. Different UUT and pod operating conditions that may reveal problems are described in the paragraphs which follow.

3-16. UUT Operating Speed and Memory Access

UUTs designed to operate at speeds which approach the time limits for memory access, may be operating marginally. Inherent delays present in the pod may result in the reporting of errors in memory, which is otherwise operating marginally.

3-17. UUT Noise Levels

UUTs operate with a certain amount of noise, and as long as the noise level is low enough, normal operation is unaffected. Removing the UUT from its chassis or case may disturb the integrity of the shielding to the point where intolerable noise could exist. The pod may introduce additional noise. In general, marginal noise problems will actually be made worse (and easier to troubleshoot) through use of the pod and troubleshooter.

3-18. Bus Loading

The pod loads the UUT slightly more than the UUT microprocessor. The pod also presents more capacitance than the microprocessor. These effects tend to make any bus drive problems more obvious.

3-19. POD DRIVE CAPABILITY

As a driving source on the UUT bus, the pod provides equal to or better than normal 6802 current drive capability. All pod inputs and outputs are TTL compatible.

3-20. POWER FAILURE DETECTION LIMITS

A power sensing circuit within the pod produces a power fail output to the troubleshooter whenever the +5 volt power supply or the Vcc standby line in the UUT drops below or increases above certain limits. The power failure detection limits are listed in the specifications table, Table 1-1.

Section 4
Theory of Operation

4-1. INTRODUCTION
This section contains two block diagram descriptions of the pod. The first is generalized; it describes the operating concept of the pod and the relationship of the pod to the troubleshooter and UUT. The second description covers pod operation in more detail.

4-2. GENERAL POD OPERATION
The pod may be divided into the following three major areas:

- Processor Section
- UUT Interface Section
- Timing Section

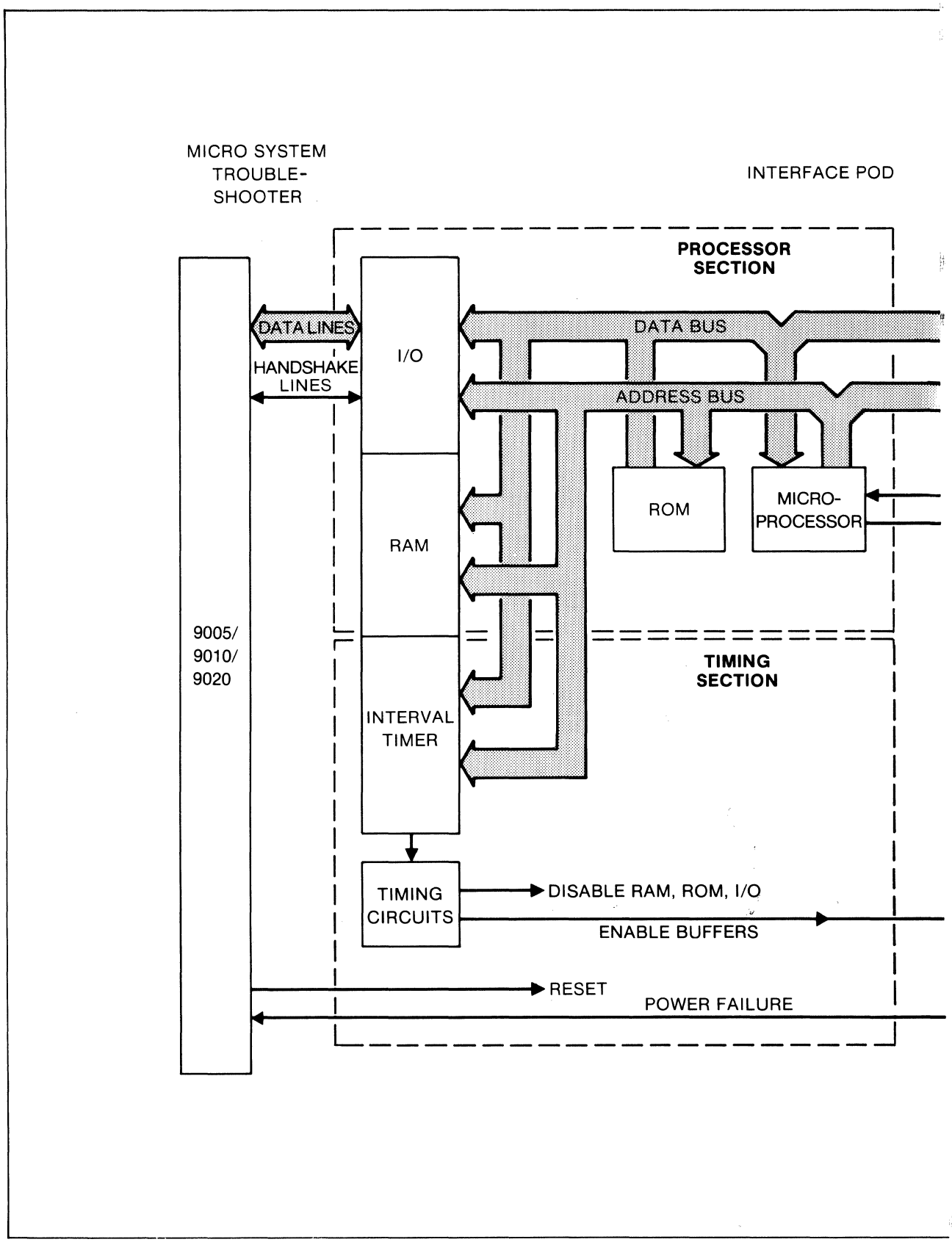
4-3. Processor Section
The Processor Section, shown in Figure 4-1, is made up of a microprocessor, RAM, a ROM, and an I/O interface to the troubleshooter. These elements comprise a small computer system which receives troubleshooter commands and directs all pod operations during execution. All reset, non-maskable interupts, and other disrupting inputs are hardware disabled, or may be software disabled, to prevent UUT faults from disabling the pod microprocessor.

The Processor Section has the capability of operating with the troubleshooter, or with the UUT, but not with both concurrently. The microprocessor spends most of its time monitoring the troubleshooter I/O interface for commands. During this time, the data and address buses of the Processor Section are isolated from the UUT Interface Section (although the pod sends signals to the UUT so that continuous read operations at the reset address appear to be taking place in order to refresh any dynamic RAM).

4-4. UUT Interface Section
The UUT Interface Section, shown in Figure 4-1, include the following elements:

- Data and address buffers
- Protection circuits for signal lines
- Logic level detection circuits for data, address, status and control lines

The data and address buffers are enabled to connect the microprocessor to the UUT, or disabled to isolate the microprocessor from the UUT. Control of the buffers is maintained by the timing section.


MICRO SYSTEM
TROUBLE-
SHOOTER
INTERFACE POD
PROCESSOR
SECTION
DATA LINES
HANDSHAKE
LINES
I/O
DATA BUS
ADDRESS BUS
ROM
MICRO-
PROCESSOR
RAM
9005/
9010/
9020
TIMING
SECTION
INTERVAL
TIMER
TIMING
CIRCUITS
DISABLE RAM, ROM, I/O
ENABLE BUFFERS
RESET
POWER FAILURE

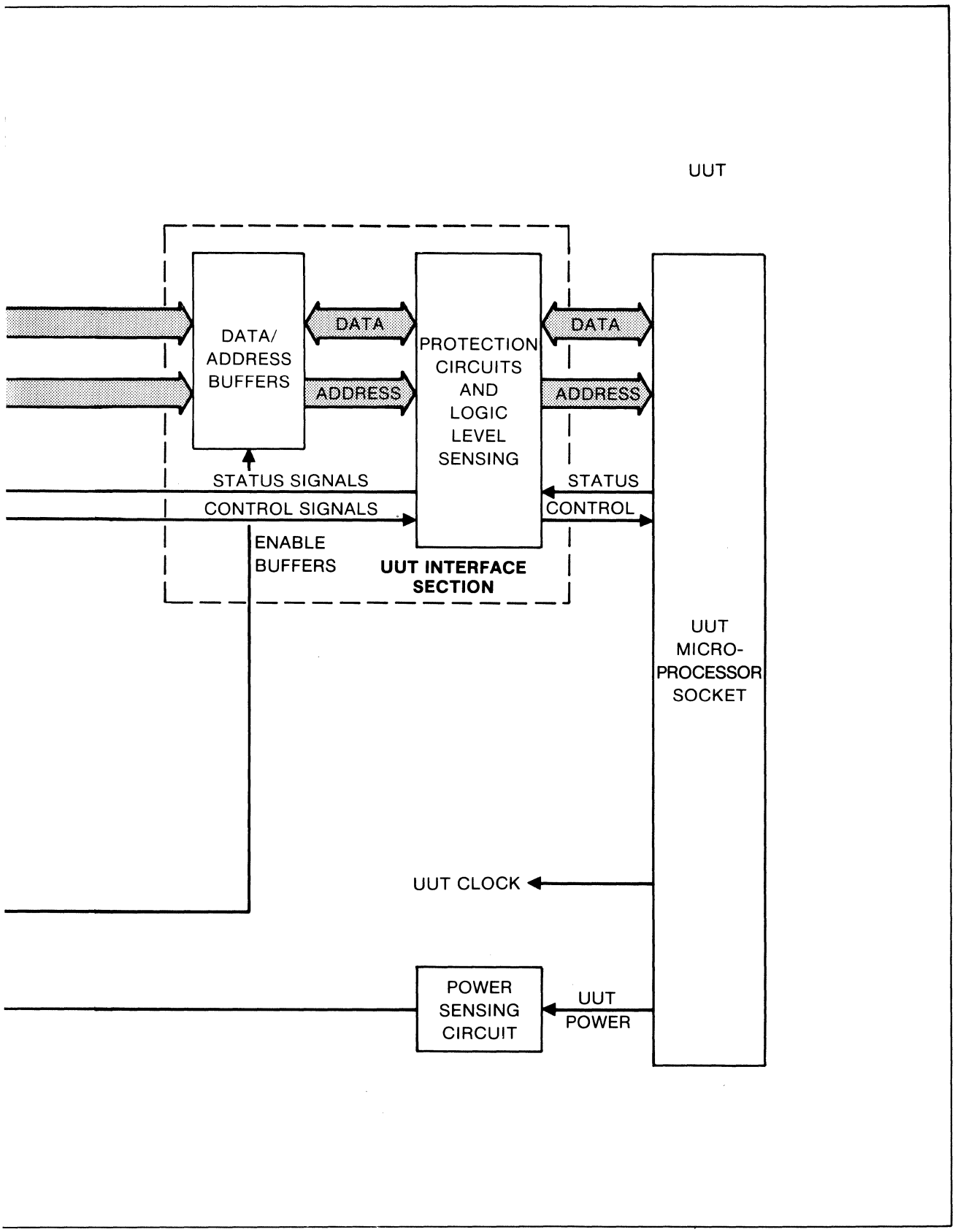


Figure 4-1. General Block Diagram

Each line to the UUT contains a protection circuit. A protection circuit consists of a 100-ohm series-resistor and clipping diodes. This circuit prevents over voltage conditions from damaging pod components.

Each line to the UUT contains a dectection circuit. A detection circuit consists of a latch connected to the UUT side of the 100-ohm protection resistor. The latch senses the level at the UUT side of the protection circuit, and at the conclusion of each UUT operation, stores the level of the UUT line. Each latch is then individually addressed and read by the Processor Section. Their contents are then compared with the desired results as a means of detecting UUT bus faults.

4-5. Timing Section

The primary function of the timing section is to cause the microprocessor to work with either the Processor Section or the UUT Interface Section at a time pre-determined by the microprocessor itself. Causing the microprocessor to work with one section or the other allows it to receive commands from the troubleshooter and then implement them with the UUT.

The Timing Section of the pod, shown in Figure 4-1, consists of an interval timer and an arrangement of timing circuits. The interval timer, preset by the microprocessor, determines the time at which the microprocessor switches from addressing the Processor Section (RAM, ROM and I/O) to addressing the UUT Interface Section (and UUT). This timing is critical, since any attempt by the microprocessor to address the Processor Section with addresses meant for the UUT, or vice versa, would result in improper operation.

In their reset state, the timing circuits cause the microprocessor to operate as a part of the Processor Section, which includes an I/O port to the troubleshooter. When the troubleshooter issues a pod command which calls for a UUT read or write operation, the microprocessor sets the interval timer to a specific value. The value set on the interval timer corresponds to the time needed by the Processor Section to prepare for command execution prior to actually addressing the UUT.

When the interval timer reaches timeout, the timing circuits produce an output to disable RAM, ROM, and I/O, and to enable the buffers of the UUT Interface Section. This action causes the microprocessor to control the UUT Interface Section instead of the Processor Section. At the same time, the microprocessor, having completed preparation for command execution, places a UUT address on the address bus, and UUT data on the data bus (if the command being executed is a write).

After a fixed period of time, the timing circuits terminate the addressing of the UUT, and the microprocessor returns to controlling the RAM, ROM, and I/O elements of the Processor Section. The timing circuits also operate the latches within the logic level detection circuits to store the state of the UUT bus during the UUT bus transaction.

When the Run UUT mode is commanded, the Timing Section causes the microprocessor to change from controlling the Processor Section to controlling the UUT Interface Section, but does not return control back to the Processor Section. In addition, the $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, MR and $\overline{\text{HALT}}$ inputs are inputs are enabled in the Run UUT mode. The RUN UUT mode is terminated by a reset signal from the troubleshooter to the pod, which returns control back to the Processor Section.

4-6. UUT Power Sensing

Figure 4-1 also shows a power sensing circuit which constantly monitors the UUT power supply. This circuit produces an output to the troubleshooter in the event UUT power drops below or rises above established limits. See Table 1-1.

4-7. DETAILED BLOCK DIAGRAM DESCRIPTION

The block diagram description that follows covers each of the three pod sections identified in the previous general description of pod operation. A detailed block diagram of the pod is presented in Figure 4-2.

4-8. Processor Section

Refer to Figure 4-2. The Processor Section of the pod is made up of the following components:

- Microprocessor, U4
- ROM, U3
- RAM (128 X 8), U1
- I/O ports A and B, U1
- Address decoder, U7
- Status line buffers, U6, U9, U10
- Internal RAM Decoder, U13, and U14

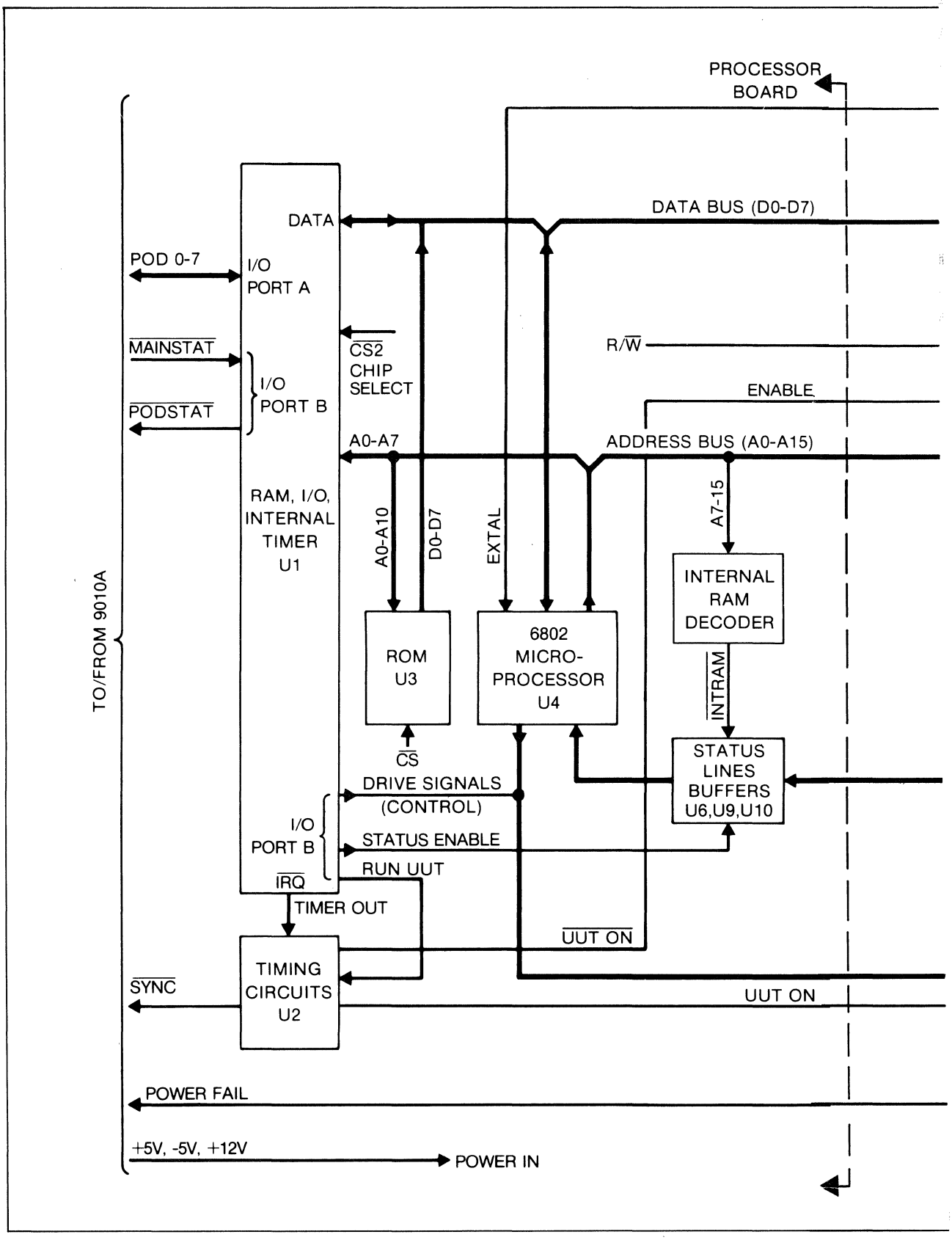
The Processor Section monitors the handshake line, $\overline{\text{MAINSTAT}}$, at I/O port B, waiting for troubleshooter commands. The microprocessor addresses I/O port B by means of address lines A0-A7 and address decoder, U7. The address decoder decodes address lines A12-A14 to produce the $\overline{\text{CS2}}$ signal which selects the RAM-I/O-Interval Timer U1.

The troubleshooter places a low on the $\overline{\text{MAINSTAT}}$ line when a command is placed on lines POD0-7. The microprocessor responds by addressing I/O port A of U4 and reading each byte of the troubleshooter command. As each byte is received, the handshaking lines operate as shown in the upper portion of Figure 4-3 to insure that no data is lost.

Each troubleshooter commands causes the microprocessor to execute a corresponding routine contained in ROM, U3. This routine, when executed, performs the troubleshooter command by first setting the interval timer (U1) and then performing all necessary internal operations in preparation for addressing the UUT. For example, if the troubleshooter command calls for a write to the UUT, the microprocessor must perform the steps necessary to assembly the UUT address, ready the data to be written, and perform housekeeping operations associated with the command.

In addition, the routine directs the actual write and read functions of the UUT, transmits any response data back to the troubleshooter, and produces a fault byte which reflects the current condition of the pod and UUT. During the transmission of data and status back to the troublshooter, the handshake lines operate as shown in the lower portion of Figure 4-3. The handshake insures that no data is lost during the transmission process.

The microprocessor has the capability of software-driving control line BA, as a means of verifying that it can be driven. Also, the microprocessor can control the enabling or disabling of status lines $\overline{\text{HALT}}$ and MR as a means of preventing stuck UUT status lines from interfering with pod operation. Both the drive signals for the control lines and the enable signals for the status lines are written by the microprocessor through I/O port B of U1.


PROCESSOR BOARD
DATA BUS (D0-D7)
DATA
POD 0-7
I/O PORT A
MAINSTAT
PODSTAT
I/O PORT B
CS2 CHIP SELECT
R/W
ENABLE
A0-A7
ADDRESS BUS (A0-A15)
RAM, I/O, INTERNAL TIMER U1
A0-A10
D0-D7
EXTAL
A7-15
INTERNAL RAM DECODER
ROM U3
6802 MICRO-PROCESSOR U4
INTRAM
CS
STATUS LINES BUFFERS U6,U9,U10
DRIVE SIGNALS (CONTROL)
I/O PORT B
STATUS ENABLE
RUN UUT
IRQ
TIMER OUT
UUT ON
TIMING CIRCUITS U2
SYNC
UUT ON
TO/FROM 9010A
POWER FAIL
+5V, -5V, +12V
POWER IN

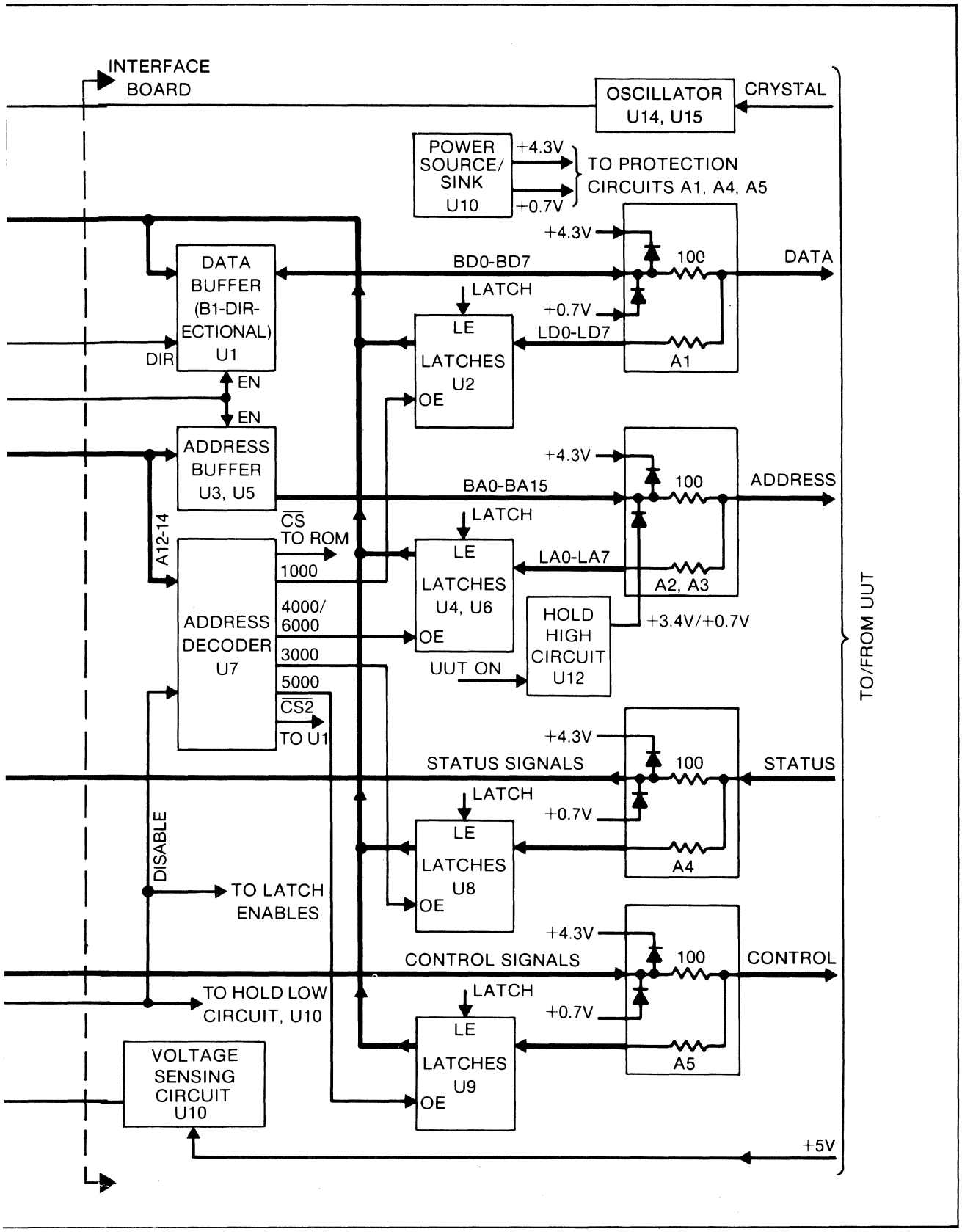


Figure 4-2. Detailed Block Diagram

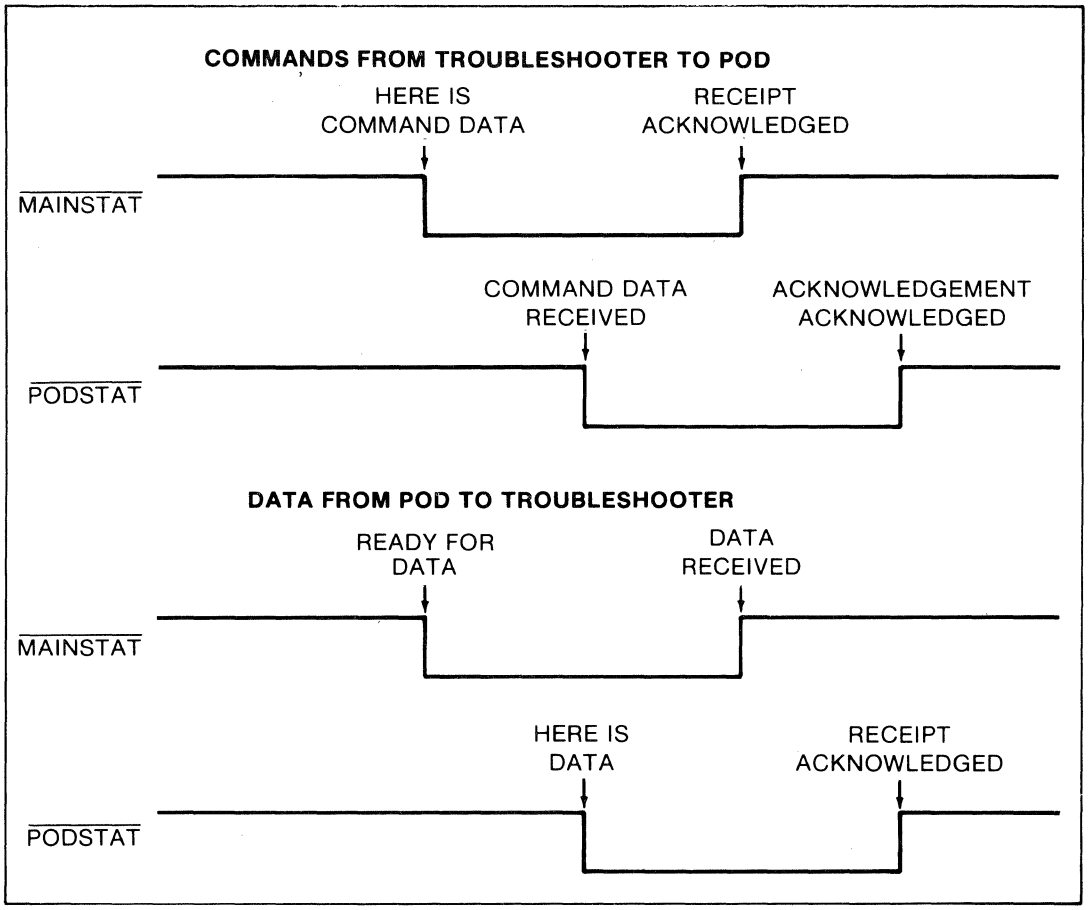


Figure 4-3. Handshake Signals

The internal RAM decoder, U13 and U14, detects when internal RAM is being read. To properly emulate a 6802 microprocessor, a read on internal RAM must place the data read on the data lines to the UUT. When a read from internal RAM is detected by U13 and U14, the bidirectional data buffer, U1, is enabled to direct the read data out to the UUT. Reads from internal RAM are only enabled during operation of the troubleshooter in the Run UUT mode; the internal RAM decoder is disabled at all other times.

4-9. UUT Interface Section - General

The UUT Interface Section includes the following components shown in Figure 4-2:

- Bidirectional data buffer, U1
- Protection circuits, A1 - A5
- Address buffer, U3 and U5
- Sensing latches, U2, U4, U6, U8 and U9
- Hold high circuit, U12 and associated components, to hold address lines at FFFF when the UUT is not accessed
- Power source/sink U10 for protection circuits

4-10. UUT Interface Section - Data Lines

The Data Buffer U1 is disabled by the timing circuits whenever the microprocessor is controlling the Processor Section. This disabling prevents data not meant for the UUT from reaching the UUT. Conversely, the data buffer is enabled by the timing circuits when the microprocessor is not controlling the Processor Section, such as, during a UUT read/write operation via data lines BD0-7. The direction of the data buffer is controlled by the Drive line, a function of the microprocessor R/$\overline{W}$ line.

All data passing between the pod and the UUT is fed through a series of protection circuits; one circuit per line. Each protection circuit consists of a 100-ohm resistor in series with the line, and a pair of clipping diodes. The diodes clip the data line at zero and +5 volts.

The data lines are also equipped with logic level detection circuits; one circuit per line. The detection circuits consist of a series of latches coupled to the UUT side of the respective protection circuits. A series resistor at the input of each latch provides overvoltage protection.

The data lines are coupled to the inputs of latches U2 by lines LD0-7. The input to each latch is logic high if the line is driven high, and logic low if the line is driven low. The Latch signal from the Timing Section latches the data line logic levels, at the time shown in Figure 4-4, to store the logic levels representing the state of each data line.

At the conclusion of a UUT write operation, latches U2 are addressed by the microprocessor. Address decoder U7 produces the address 1000 signal to place the contents of the latches on the data bus. The microprocessor compares the contents of the addressed latches with the intended write data. Any difference between the contents of the latches and the intended data is considered a data error.

4-11. UUT Interface Section - Address Lines

In a manner similar to that described for the data lines, all UUT addresses are fed through a series of protection circuits equipped with resistors and clipping diodes. The diodes used to protect the address lines perform the additional function of holding the address lines at zero volts any time the UUT Interface Section is not controlled by the microprocessor.

Address buffers U3 and U5 are enabled when the microprocessor is controlling the UUT Interface Section. Conversely, the address buffers are disabled to isolate the microprocessor from the UUT whenever the microprocessor is controlling the Processor Section. This isolation prevents the microprocessor from addressing the UUT when operating as part of the Processor Section. In addition, the address lines are held high by the diodes used in the protection circuits.

This holding action is provided by the hold high circuit, made up of U12 and associated components. This circuit drives the +0.7-volt diode clipping voltage up to +3.4 volts whenever the UUT is not being addressed, creating a UUT address of FFFF. Maintaining the UUT at address FFFF prevents any inadvertent operation of the UUT and associated systems equipment.

As described for the data lines, the address lines are equipped with logic level detection circuits; one circuit per line. The detection circuits consist of a series of latches coupled to the UUT side of the respective protection circuits. A series resistor at the input of each latch provides overvoltage protection.

The address lines are coupled to the inputs of latches U4 and U6 by lines LA0-LA15. The input to each latch is logic high if the line is driven high, and logic low if the line is driven

low. The Latch signal from the Timing Section latches the address line logic levels, at the time shown in Figure 4-4, to store the logic levels representing the state of each data line.

At the conclusion of a UUT operation, latches U4 and U6 are separately addressed by the microprocessor. Address decoder U7 produces the address 4000 and 6000 signals to place the contents of the latches on the data bus, one byte at a time. The microprocessor compares the contents of the addressed latches with the actual address. Any difference between the contents of the latches and actual address is considered an address error.

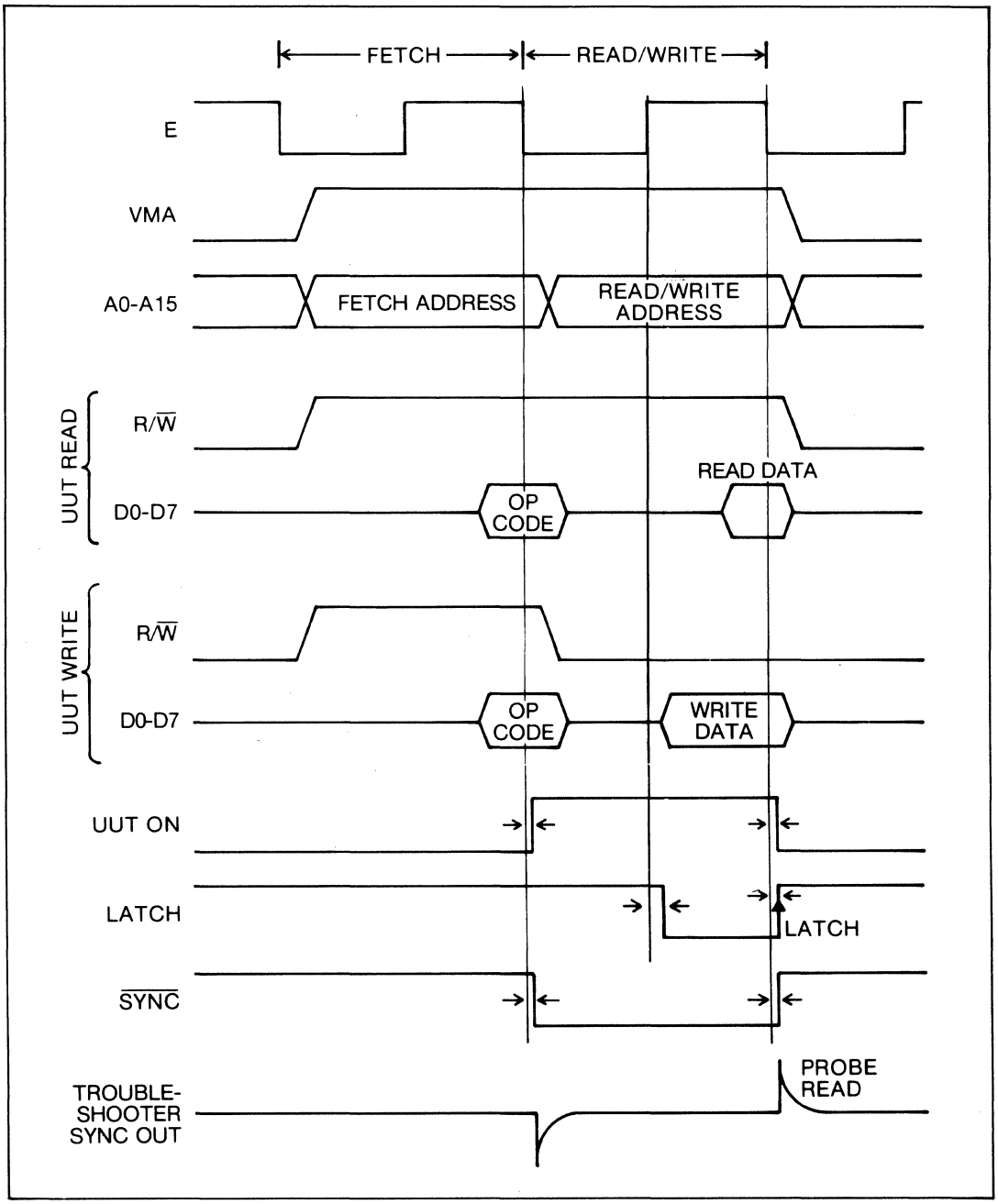


Figure 4-4. UUT ON Signal and Latch Times

4-12. Interface Section - Status and Control Lines

The status and control lines are provided with protection circuits, logic level detection circuits and latches. These circuits operate in a manner similar to those provided with the data and address lines, and described in the previous paragraphs.

4-13. Timing Section

The timing section consists of the interval timer contained in U1, and timing circuits made up of U2. As mentioned in the description of the Processor Section, the microprocessor executes the troubleshooter command by first setting the interval timer and then performing all necessary internal operations in preparation for addressing the UUT. The interval timer is set to a time equal to the amount of time required by the microprocessor to perform all necessary internal operations.

At the time the interval timer is set, and until the timer times out, a high $\overline{IRQ}$ output from U1 holds the timing circuits in their reset state. When the timer times out, the $\overline{IRQ}$ output goes low to enable the timing circuits and produce the UUT On, $\overline{UUT\ On}$, and the $\overline{SYNC}$ signals to enable the data and address buffers, and disable the address decoder and send a $\overline{SYNC}$ pulse back to the troubleshooter. Refer to Figure 4-4 for the timing of the UUT On signal. The UUT On signal also disables the hold high circuit, U12, releasing the address bus from the forced UUT address of FFFF.

With the data and address buffers enabled, and the hold high circuit disabled, data and addresses placed on the buses by the microprocessor are directed to the UUT. The Processor Section is disabled at this point by the address decoder U7 which receives the UUT On signal generated by the timing circuits. With address decoder disabled, the ROM and RAM-I/O-Interval Timer are not selected.

At the time of the next clock pulse, while the microprocessor is still addressing the UUT, the Latch signal is produced to enable input of each latch circuit. The latches store the condition of all UUT lines.

At the end of the instruction cycle (except in the Run UUT mode), the timing circuits return to their reset state to disable the data and address buffers, and enable address decoder, U7. This action switches the microprocessor back to control the Processor Section instead of the UUT Interface Section.

The latches store the UUT line logic levels. When addressed by the microprocessor, via address decoder U7, each latch places the condition of the associated UUT line on the data bus. The microprocessor compares the detected UUT line levels with the expected result and considers any difference to be an error. Any error conditions are indicated in the status byte sent to the troubleshooter at the conclusion of each command.

When the Run UUT mode is commanded, and the interval timer produces the low $\overline{IRQ}$ signal, and the timing circuits produce the high UUT On signal as previously described for the non-Run UUT mode. However, the Run UUT command causes the timing circuits to be held in a state which maintains the UUT On signal and dedicates the microprocessor to the UUT. In this mode, the $\overline{RESET}$, $\overline{NMI}$, $\overline{HALT}$, and MR inputs are enabled, allowing the UUT to utilize the pod microprocessor in place of the microprocessor removed to facilitate pod connection.

The Run UUT mode continues until a $\overline{RESET}$ signal is received from the troubleshooter. The $\overline{RESET}$ signal causes the microprocessor to resume control of the Processor Section.

Section 5
Maintenance

5-1. INTRODUCTION

This section provides maintenance information for the pod, and includes self test information, repair precautions, disassembly procedures, and troubleshooting information.

5-2. SELF TEST

The troubleshooter can perform a self test on any pod which is operational enough to communicate with the troubleshooter. Self test provides fault location to several areas of the pod by creating appropriate display messages on the troubleshooter. In order to perform self test, the Processor Section (6802 RAM, ROM, I/O, and buses) must be operational. Operation of the processor section is necessary in order for the pod to accept and execute self test commands issued by the troubleshooter.

NOTE

Self test does not examine the pod for all conceivable faults, and may indicate an okay pod when not completely operable. An alternative method of checking pod operability is exercising with a known-good UUT and troubleshooter, observing any reported "UUT failures".

Performance of self test requires that the ribbon cable connector be inserted into the self test socket located on the pod. When the ribbon cable plug is inserted into the self test socket, the following electrical connections are made to facilitate testing (refer also to the schematic diagram contained in Section 7):

- The high order address lines are connected back to the data lines through series resistors. This connection allows the high order address bits to become data during a test read operation.
- A clock signal is applied to the clock input of the pod. This clock signal replaces the clock normally supplied by the UUT to operate the pod.
- All forcing lines and interrupts are set to the active state. Setting these lines allows testing of the individual hardware or software buffering.
- +5V dc is applied to pin 8 to simulate UUT power and check the power fail sensing circuit.
- Ground is applied through the ribbon cable to pins 1 and 21 to notify the troubleshooter that the pod is in the self test configuration.

To perform self test, proceed as follows:

1. If not already connected, connect the interface pod to the troubleshooter as shown in Figure 2-1. Secure the connector using the sliding collar.

2. Open the pins of the self test socket by operating the adjacent thumbwheel. Insert the ribbon cable plug into the socket and close the socket using the thumbwheel.

3. Turn the troubleshooter on and press BUS TEST to initiate self test.

4. If the troubleshooter and pod are operating normally, the troubleshooter display reads *POD SELF-TEST 6802 OK.*

5. If the pod is defective, but not completely dead, the troubleshooter displays *POD SELF-TEST 6802 FAIL xx,* where *xx* represents the pod fault listed in Table 5-1. Refer to the troubleshooting procedures to further isolate the problem.

6. If the pod is inoperative, the troubleshooter reads *POD TIMEOUT - ATTEMPTING RESET.* This message indicates that the pod is not responding to commands issued by the troubleshooter. Refer to the troubleshooting procedures to isolate the problem.

Table 5-1. Self Test Failure Codes

CODE	POSSIBLE FAULT
00	1. UUT power sensing circuit failure 2. Control line(s) cannot be driven 3. Address line(s) cannot be driven 4. Wrong data read
01	1. UUT power sensing circuit failure 2. Control line(s) cannot be driven 3. Address line(s) cannot be driven 4. Data line(s) cannot be driven
02	One or more control line not driveable
03	Forcing or interrupt line buffer(s) or associated logic faulty.

5-3. REPAIR PRECAUTIONS

CAUTION

Static discharge can damage MOS components contained in the pod. To prevent this possibility, take the following precautions when troubleshooting and/or repairing the unit.

- Never remove, install, or otherwise connect or disconnect PCB (printed circuit board) assemblies without disconnecting the pod from the troubleshooter.
- Perform all repairs at a static-free work station.
- Do not handle ICs or PCB assemblies by their connectors.

- Attach static ground straps to repair personnel.
- Use conductive foam to store replacement or removed ICs.
- Remove all plastic, vinyl and styrofoam from the work area.
- Use a grounded soldering iron.

The soldering iron used in pod repair should have a rating of 25 watts or less to prevent overheating the PCB assembly.

5-4. TROUBLESHOOTING

5-5. Introduction

Pod failure is usually identifiable from the troubleshooter display. Two types of messages which indicate pod failure are:

- *POD TIMEOUT -ATTEMPTING RESET;* when this message is displayed, the pod does not respond to troubleshooter commands or reset pulses. This message may be due to stuck forcing lines not disabled during troubleshooter setup procedures described in the Operator Manual.
- Any recurring UUT test-failure or error message when testing a known-good UUT indicates pod failure. Since the UUT is known to be good, errors attributed to the UUT by the troubleshooter are actually pod errors.

Troubleshooting the pod is similiar to troubleshooting any other microprocessor-based UUT, and requires the equipment listed in Table 5-2. The troubleshooting information presented in the following paragraphs does not provide step-by-step fault isolation procedures, but provides a troubleshooting guide for use while employing normal fault isolation techniques.

Figure 5-1 shows the non-component side of the interface PCB with component outlines and identification superimposed. Refer to this figure to locate various electrical points on the interface PCB during troubleshooting procedures.

The troubleshooting information should be used in conjunction with the schematic diagrams contained in Section 7 and the Theory of Operation presented in Section 4.

The troubleshooting guidelines presented in the following paragraphs are intended to assist in the isolation of faults within the pod. If attempted troubleshooting fails to reveal the pod fault, return of the pod to the nearest Fluke Service Center is recommended. Refer to the troubleshooter Service Manual for a list of Fluke Service Centers.

Table 5-2. Required Test Equipment for Pod Troubleshooting

EQUIPMENT TYPE	REQUIRED TYPE
Micro System Troubleshooter	Fluke 9000 Series
Interface Pod	Fluke 9000A-6802
Digital Multimeter	Fluke 8020
Oscilloscope	Tektronix 485 or equivalent

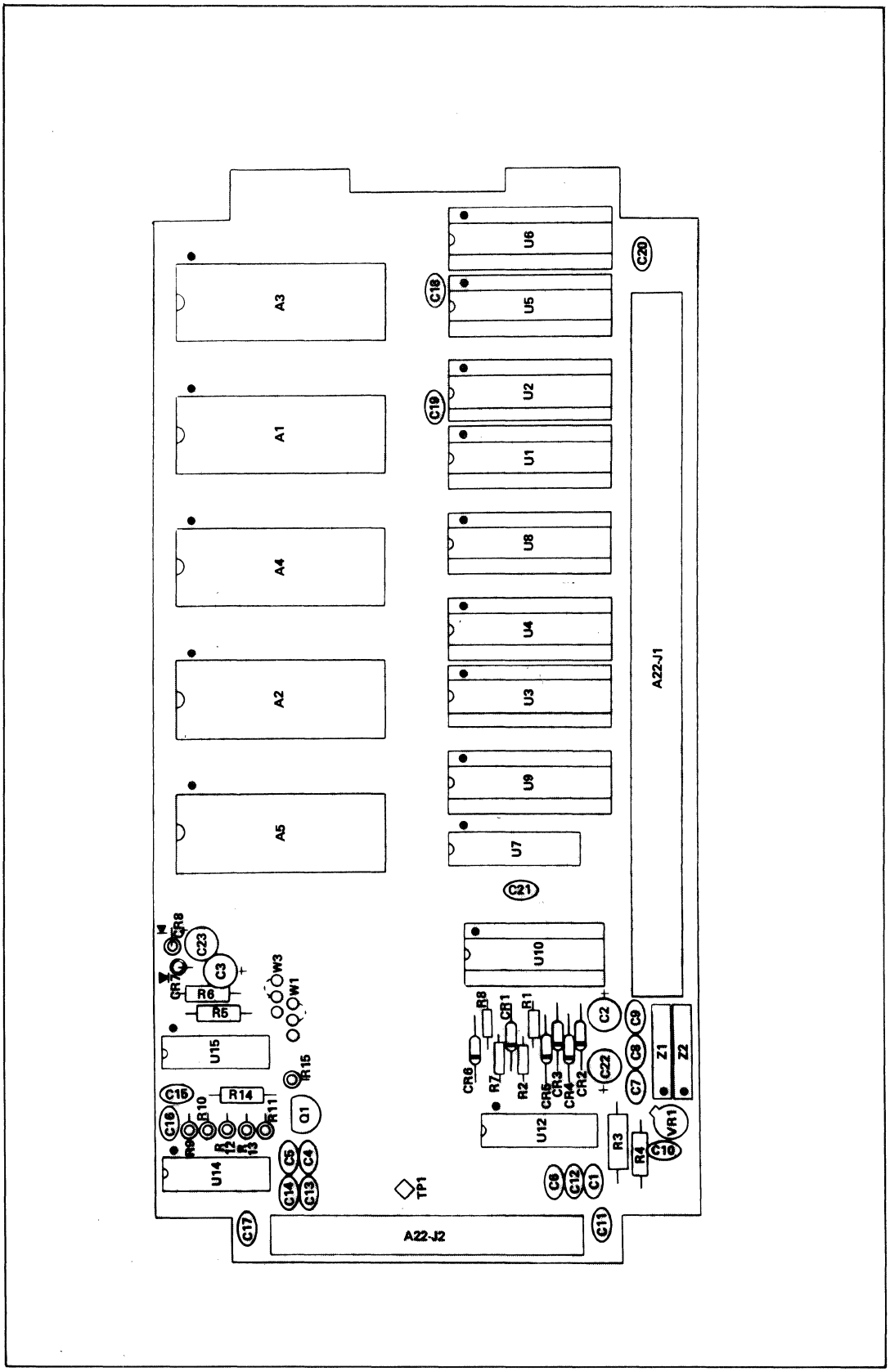


Figure 5-1. Interface PCB, Non-Component Side

5-6. Pod Defective or Inoperative?

Before attempting to repair a faulty pod, the level of failure should be determined. A faulty pod can be catagorized as either defective or inoperative, depending upon the result of the self test.

If the result of a self test produces a troubleshooter display of *POD SELF-TEST 6802 FAIL xx,* the pod is considered to be defective but not inoperative. Troubleshoot a defective pod as described under the heading Troubleshooting a Defective Pod. Select a suitable UUT as described under the heading Selecting a UUT for Pod Testing.

NOTE

It is possible for a pod to produce a self test message of POD SELF-TEST 6802 OK and still be faulty. Such a pod causes the display of test-failure or error messages on the troubleshooter when used to test a known-good UUT. In this case, errors attributed to the UUT are actually pod errors.

If the result of a self test, or any other troubleshooter operation, produces a troubleshooter display of *POD TIMEOUT -ATTEMPTING RESET,* the pod is considered to be inoperative. Troubleshoot an inoperative pod as described under the heading Troubleshooting and Inoperative Pod. Select a suitable UUT as described under the heading Selecting a UUT for Pod Testing.

NOTE

The POD TIMEOUT -ATTEMPTING RESET message can also result from stuck UUT forcing lines which can disable the pod. Forcing lines should be disabled during troubleshooter setup procedures as described in the Operator Manual.

5-7. Selecting a UUT for Pod Testing

In order to troubleshoot a pod, a known-good UUT must be connected to the pod via the ribbon cable and connector. The UUT may be any device which normally employs a 6802 microprocessor and to which power can easily be applied. The UUT is needed to provide the following functions during pod testing:

- RAM and ROM for performing read/write operations
- +5V dc UUT power to check the UUT power sensing circuit

Instead of connection to a known-good UUT, the ribbon cable connector may be connected to the self test socket on the pod. The self test socket provides a 6802 compatible clock signal, +5V dc, and also simulates ROM by connecting the high order address lines back to the data lines (refer to the schematic diagram for details).

However, insertion of the ribbon cable connector directly into the self test socket places pins 1 and 21 at ground. The pod senses the ground at pins 1 and 21 and notifies the troubleshooter of the self test connection. As a result, the troubleshooter inhibits normal operation and allows performance of only self test.

During pod troubleshooting procedures, normal troubleshooter operation must be allowed. Consequently, the pod must be prevented from sensing the ribbon cable connector in the self test socket. To prevent the pod from sensing the self test connection, pins 1 and 21 of the connector must be effectively removed.

To effectively remove pins 1 and 21 of the connector, obtain one of the two replacement ribbon cable connectors "socket savers" supplied with the pod, and modify as follows:

1. Carefully separate the connector body halves using a small screwdriver.

2. Remove pins 1 and 21 from the connector and reassemble the body.

3. Insert the modified replacement connector into the self test socket.

4. Insert the ribbon cable connector into the modified replacement connector.

In addition to modifying the ribbon cable connector, be sure to disable all forcing line and interrupt inputs, and set all forcing line and interrupt traps to NO during Setup Editing as described in the Operator Manual. Disabling these inputs and messages is necessary when utilizing the self test socket since all lines are wired to the active state.

5-8. Troubleshooting a Defective Pod

NOTE

The following paragraphs reference three distinct areas of the pod identified as the Processor Section, the UUT Interface Section, and the Timing Circuits. The components which make up these sections are identified in the Theory of Operation, presented in Section 4.

A pod is considered defective when the performance of self test produces a troubleshooter display of *POD SELF TEST 6802 FAIL xx,* where *xx* represents the pod fault listed in Table 5-1. The fact that a self test can be performed indicates operation of the Processor Section, since operation of the Processor Section is necessary for troubleshooter/pod communication. With the Processor Section proven to be good, the UUT Interface Section of the Timing Circuits contain the fault.

Prepare to troubleshoot the defective pod as follows:

1. Disassemble the pod by removing the PCB assemblies from the case, and the shield from the PCB assemblies. (Refer to disassembly information under the heading Disassembly.) It is not necessary to separate the PCB assemblies at this point.

2. Connect the pod to the troubleshooter, and the ribbon cable connector to the UUT, or the self test socket as shown in Figure 5-2. Note that the troubleshooter is connected to the defective pod by means of the shielded cable, and not by means of a second pod to the microprocessor socket. Also, Figure 5-2 shows the self test socket as the UUT, although any suitable UUT may be used. (Refer to Selecting a UUT for Pod Testing.)

NOTE

All references to data and addresses in the following troubleshooting guide are in hexadecimal notation. Unless otherwise noted, all troubleshooter probe operations are performed in the synchronized mode.

NOTE

When troubleshooting a pod, perform looping tests of the most simple type (such as reads and writes as opposed to ROM and RAM tests) that show a fault symptom. A synchronized probe can then be used to trace a fault once such a looping test has it isolated.

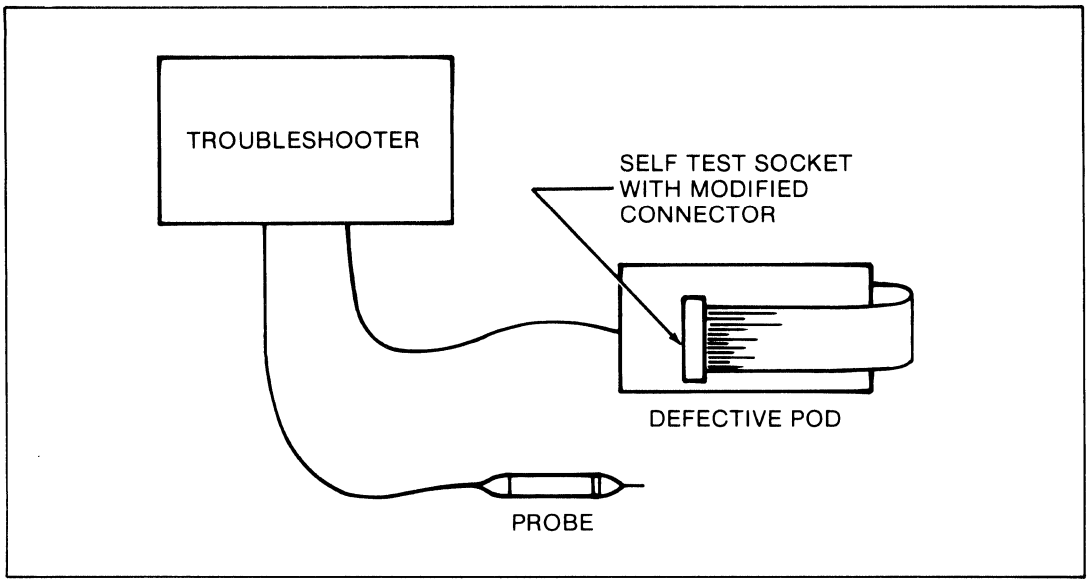


Figure 5-2. Troubleshooting a Defective Pod

5-9. SELF TEST CODE 00

If self test produces a troubleshooter display of *POD SELF-TEST FAIL 6802 FAIL 00,* a UUT read operation has failed and one or more of the following problems is indicated:

- UUT power sensing circuit failure
- Control line(s) cannot be driven
- Address line(s) cannot be driven
- Wrong data read

To further isolate the trouble, prodeed as follows:

1. Check operation of the UUT power sensing circuit by verifying the +5 volt UUT supply at the ribbon cable connector and zero volts on the Power Fail line. Check the Power Fail line at the PCB-to-PCB connector, and if necessary, at the shielded cable connector.

2. Perform a read operation. Use address 0FF0 if using the self test socket as the UUT. (The self test socket sends the upper address byte to the data lines. During self test, read operations at 0FF0 and F00F take place.) Use any address containing known data if using some other UUT.

   a. If the troubleshooter indicates a control line error, examine the entire troubleshooter display to determine the stuck control line(s). While looping on the error, use the probe or a scope to locate the point of control line failure.

   b. If the troubleshooter indicates an address line error, note the failed address line(s) indicated on the troubleshooter display. While looping on the error, use the probe or a scope to locate the point of address line failure.

   c. If the data read, indicated on the troubleshooter display, is not 0F when using the self test socket, or is not identical to the known data of the UUT used for this

test, a data line or address line failure is indicated. Determine the failed line(s) from the display and locate the point of failure using the synchronized probe or a scope while performing a looping read operation.

3. Repeat steps 2b and 2c at different addresses and for different data in order to toggle each of the address and data lines.

4. Check for operation of the interval timer and timing circuits by observing pin 25 ($\overline{IRQ}$) of U1 for a low-going output each time a read operation is executed. If the $\overline{IRQ}$ signal is present, check for a $\overline{SYNC}$ signal at pin 10 of the shielded cable connector, and for a UUT On signal at the PCB-to-PCB connector. The absence of these signals allows the pod to communicate with the troubleshooter, but prevents the latches from detecting addresses, data, and control signals sent to the UUT (or self test socket). Failure of these signals may also prevent data read from the UUT from reaching the pod microprocessor.

5-10. SELF TEST CODE 01

If self test produces a troubleshooter display of *POD SELF-TEST 6802 FAIL 01,* one or more of the following failures is indicated:

- UUT power sensing circuit failure
- Control line(s) cannot be driven
- Address line(s) cannot be driven
- Data line(s) cannot be driven

To further isolate the trouble, proceed as follows:

1. Check operation of the UUT power sensing circuit by verifying the +5 volt UUT supply at the ribbon cable connector and zero volts on the Power Fail line. Check the Power Fail line at the PCB-to-PCB connector, and if necessary, at the shielded cable connector.

2. Perform a write operation; use 0FF0 for the address and 0F for the data.

   a. If the troubleshooter indicates a control line error, examine the entire troubleshooter display to determine the stuck control line(s). While looping on the error, use the probe or a scope to locate the point of control line failure.

   b. If the troubleshooter indicates an address line error, note the failed address line(s) indicated on the troubleshooter display. While looping on the error, use the probe or a scope to locate the point of address line failure.

   c. If the troubleshooter indicates a data line error, note the failed line(s) indicated on the troubleshooter display. While looping on the error, use the probe or a scope to locate the point of failure.

3. Repeat steps 2b and 2c using F00F for the address and F0 for the data to check address and data lines in the opposite state.

4. Check for operation of the interval timer and timing circuits by observing pin 25 ($\overline{IRQ}$) of U1 for a low-going output each time a write operation is executed. If the $\overline{IRQ}$ signal is present, check for a $\overline{SYNC}$ signal at pin 10 of the shielded cable

connector, and for a UUT ON signal at the PCB-to-PCB connector. The absence of these signals allows the pod to communicate with the troubleshooter, but prevents the latches from detecting addresses, data, and control signals sent to the UUT (or self test socket). Failure of these signals may also prevent write data from reaching the UUT.

5-11. SELF TEST CODE 02

If self test produces a troubleshooter display of *POD SELF-TEST 6802 FAIL 02,* failure of one or more of the control lines is indicated. To check each of the control lines, use the troubleshooter to perform a BUS TEST. Refer to the heading Bit Assignment - Control Lines, located in Section 3, for interpretation of the troubleshooter message.

5-12. SELF TEST CODE 03

If self test produces a troubleshooter display of *POD SELF-TEST 6802 FAIL 03,* failure of one or more status line buffers is indicated. Each of the status (forcing) lines, which have the ability to interrupt or otherwise interfere with microprocessor operation, are selectively buffered from the microprocessor.

Buffering of the $\overline{\text{HALT}}$ and MR lines is accomplished by means of gates which are enabled or inhibited by port B outputs of the RAM-I/O-Interval Timer.

5-13. Troubleshooting an Inoperative Pod

NOTE

The following paragraphs reference three distinct areas of the pod identified as the Processor Section, the UUT Interface Section, and the Timing Circuits. the components which make up these sections are identified in the Theory of Operation, presented in Section 4.

A pod is considered inoperative when the performance of self test, or any other troubleshooter operation, produces a troubleshooter message of *POD TIMEOUT - ATTEMPTING RESET.* This troubleshooter message results from a lack of response by the pod to troubleshooter commands. Since it is the function of the Processor Section to respond to troubleshooter commands, lack of response indicates failure of the Processor Section.

With reference to Figure 5-3, prepare to troubleshoot the inoperative pod as follows:

1. Disassemble the pod. Refer to Disassembly.

2. Remove the microprocessor from its socket.

3. Connect the pod under test to +5 volt and –5 volt power supplies. Apply power to the PCB connector normally coupled via the shielded cable to the troubleshooter; use pins 2 and 15 for +5 volts, pin 21 for –5 volts, and pin 25 for ground.

4. Connect a 9000 Series Troubleshooter to a second pod. Apply power to the troubleshooter, then connect the second pod ribbon cable to the microprocessor socket of the pod under test.

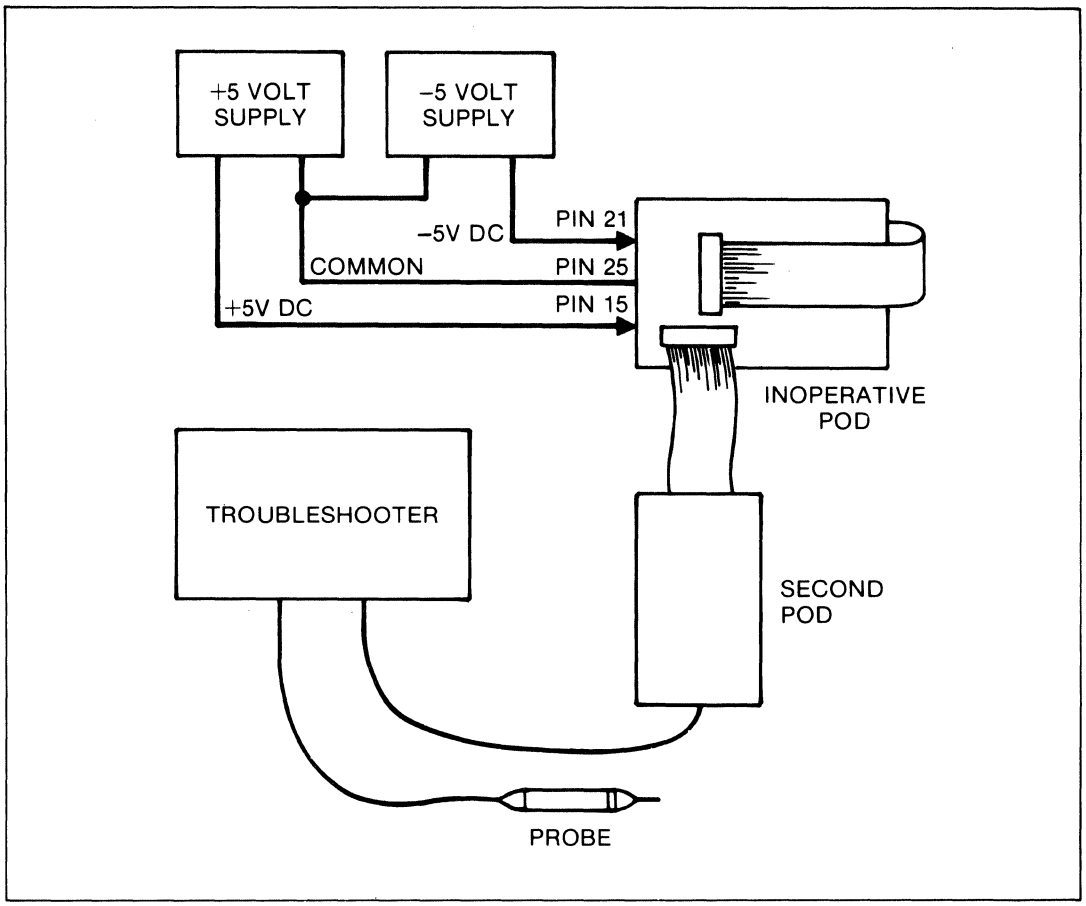


Figure 5-3. Troubleshooting an Inoperative Pod

CAUTION

Do not apply or remove any power with ribbon cable connected between second pod and inoperative pod.

NOTE

All references to data and addresses in the following troubleshooting guide are in hexadecimal notation.

With reference to the Theory of Operation contained in Section 4 and the schematic diagram contained in Section 7, troubleshoot an inoperative pod using the following steps as a guide:

1. Reset the pod by momentarily shorting pins 22 and 23 of the shielded cable connector located on the upper PCB assembly.

2. Perform a Bus Test.

3. Perform a RAM Short and RAM Long Test. The RAM addresses are listed in Table 5-3.

4. Perform a ROM Test. The ROM addresses are listed in Table 5-3.

Table 5-3. 6802 Pod Memory and I/O Addresses

ADDRESSABLE DEVIDE	ADDRESS (HEX)
RAM	0000 - 007F
ROM	F800 - FBFF
I/O - Port A Direction Register	0081
- Port A Data Register	0080
- Port B Direction Register	0083
- Port B Data Register	0082
Interval Timer — Divide by 1	009C
Interval Timer Disable	0094

5. Check the output operation of I/O port A (contained in U1) as follows:

   a. Perform a write operation to the port A direction register to set all lines of I/O port A (PA0-PA7) as outputs. The write address is 0081; write data is FF.

   b. Perform a write operation to the port A data register to set all bits high. The write address is 0080; write data is FF.

   c. Check the port A lines (PA0-PA7) with the probe or scope for all logic high levels.

   d. Repeat step b with 00 as the write data.

   e. Repeat step c, checking for all logic low levels.

6. Check the input operation of I/O port A (contained in U1) as follows:

   a. Perform a write operation to the port A direction register to set all lines of I/O port A (PA0-PA7) as inputs. The write address is 0081; write data is 00.

   b. Perform a read operation at the port A data register, address 0080, while sequentially applying the probe (with high pulses selected) to each of the port A input pins (pins 8-15 of U1) and observing the troubleshooter display. The troubleshooter should indicate each high input of port A.

7. Check the output operation of port B (PB0-PB7) by repeating step 5 and using address 0083 for the port B direction register, and address 1082 for the port B data register.

8. Check the input operation of port B, line PB7 ($\overline{\text{MAINSTAT}}$) by repeating step 6. Use address 0083 for the port B direction register and write data 00 to set line PB7 as an input. Perform the looping read at address 0082 and apply +5 volts to U1, pin 16.

9. Check operation of the interval timer (contained in U1) by performing a write operation at address 009C; write data = 0F. Verify that the $\overline{\text{IRQ}}$ output of U1 goes low in response to the write operation.

10. Check for the occurence of the UUT On signal (produced by the timing circuits as a result of the low $\overline{IRQ}$ signal) at the PCB-to-PCB connector.

11. Check for the occurence of the $\overline{SYNC}$ signal at pin 10 of the shielded cable connector.

12. Check the address decoder by performing read operations at addresses 0000, 1000, 3000, 4000, 5000, 6000, and 7000. Verify that the respective decoder output goes low when addressed.

13. If repairs have been made to the inoperative pod as a result of the preceeding checks, attempt self test. If self test operates, but the pod fails, refer to Troubleshooting a Defective Pod.

The troubleshooting guidelines presented in the preceeding paragraphs are intended to assist in the isolation of faults within the pod. If attempted troubleshooting fails to reveal the pod fault, return of the pod to the nearest Fluke Service Center is recommended. Refer to the troubleshooter Service Manual for a list of Fluke Service Centers.

5-14. DISASSEMBLY

To gain access to the two PCB assemblies within the pod, proceed as follows:

1. Remove the ribbon cable plug from the self test socket.

2. Remove the four phillips screws holding the pod case halves together and carefully open the case.

3. With the PCB assemblies removed from the case halves, remove the screw which retains the shield. Remove the shield.

NOTE

To troubleshoot the pod, it may not be necessary to separate the two PCB assemblies except to replace components. Figure 5-1 shows the location of each component on the lower PCB assembly relative to the accessible non-component side of the board.

4. If it is not necessary to separate the two PCB assemblies, temporarily replace the shield retaining screw; otherwise, remove the second screw from its standoff and carefully pull the boards apart at the connector.

Section 6
List of Replaceable Parts

6-1. INTRODUCTION

This section contains an illustrated parts breakdown of the instrument. Components are listed alphanumerically by assembly.

Parts lists include the following information:

1. Reference Designation.
2. Description of Each Part.
3. Fluke Stock Number.
4. Federal Supply Code for Manufacturers. (See the 9000 Series Troubleshooter Service Manual for Code-to-Name list).
5. Manufacturer's Part Number.
6. Total Quantity of Components Per Assembly.
7. Recommended quantity: This entry indicates the recommended number of spare parts necessary to support one to five instruments for a period of 2 years. This list presumes an availability of common electronic parts at the maintenance site. For maintenance for 1 year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked.

6-2. HOW TO OBTAIN PARTS

Components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. or an authorized representative by using the Fluke Stock Number.

In the event the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

To ensure prompt and efficient handling of your order, include the following information.

1. Quantity.
2. Fluke Stock Number.
3. Description.

4. Reference Designation.

5. Printed Circuit Board Part Number and Revision Letter.

6. Instrument Model and Serial Number.

A Recommended Spare Parts Kit for your basic instrument is available from the factory. This kit contains those items listed in the REC QTY column for the parts lists in the quantities recommended.

Parts price information is available from the John Fluke Mfg. Co., Inc. or its representative. Prices are also available in a Fluke Replacement Parts Catalog, which is available upon request.

CAUTION

Indicated devices are subject to damage by static discharge.

6-3. MANUAL CHANGE AND BACKDATING INFORMATION

Table 6-4 contains information necessary to backdate the manual to conform with earlier pcb configurations. To identify the configuration of the pcbs used in your instrument, refer to the revision letter on the component side of each pcb assembly.

As changes and improvements are made to the instrument, they are identified by incrementing the revision letter marked on the affected pcb assembly. These changes are documented on a supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.

To backdate this manual to conform with an earlier assembly revision level, perform the changes indicated in Table 6-4. There are no backdating changes at this printing. All pcb assemblies are documented at their original revision level.

Table 6-1. 9000A-6802 Final Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
	9000A-6802 POD FINAL ASSEMBLY FIGURE 6-1 (9000A-6802-T&B, 5001)						
A21Ø	PROCESSOR PCB ASSEMBLY	642363	89536	642363	1		
A22Ø	INTERFACE PCB ASSEMBLY	642397	89536	642397	1		
H1	SCREW, PHP, 4-40 X 1/4	185918	89536	185918	2		
H2	SCREW, PHP, 4-40 X 1/2	152132	89536	152132	4		
MP1	ACCUATOR KNOB	582916	89536	582916	1		
MP2	DECAL, POD	647297	89536	647297	1		
MP3	DECAL, SPECIFICATION	647305	89536	647305	1		
MP4	LABEL, STATIC CAUTION	605808	89536	605808	1		
MP5	LABEL, UUT CAUTION	634030	89536	634030	1		
MP6	SHELL, BOTTOM	579573	89536	579573	1		
MP7	SHELL, TOP	579565	89536	579565	1		
MP8	SHIELD	586479	89536	586479	1		
MP9	9000A POD ACCESSORIES (NOT SHOWN)	613885	89536	613885	1		
	CABLE, UTT				1		
	LABEL, UUT CAUTION				1		
	PLASTIC BAG, ACCESSORY				1		
	SOCKET, DIP 40-PIN				2		
TM1	INSTRUCTION MANUAL, 9000A-6802	649392	89536	649392			
U3	E-PROM	649103	89536	649103	1		
W1	CABLE ASSEMBLY, POD	581827	89536	581827	1		
W2	CABLE ASSEMBLY, UUT	585141	89536	585141	1		
	RECOMMENDED SPARE PARTS KIT (9000A-6802)	653469	89536	653469	AR		

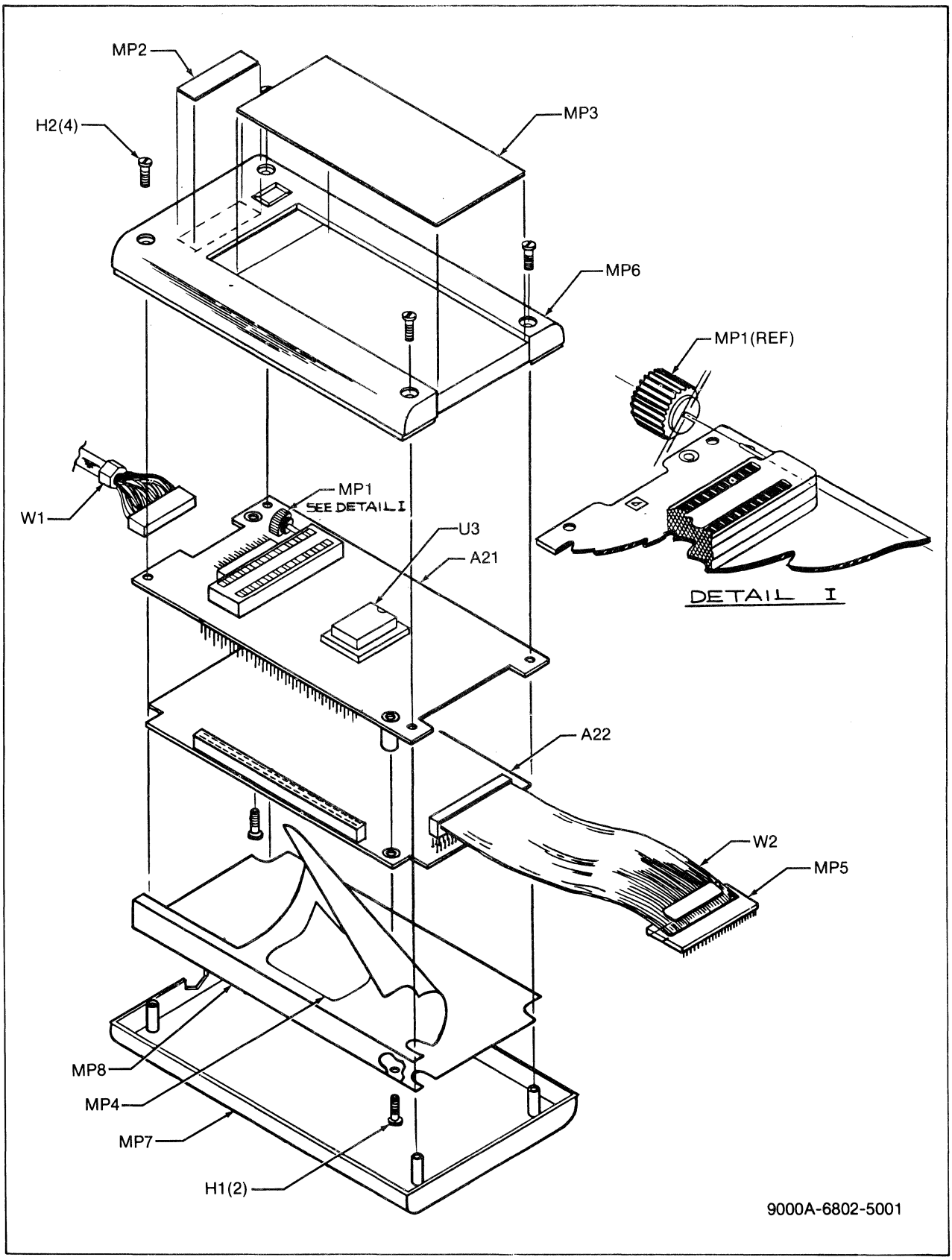


Figure 6-1. 9000A-6802 Final Assembly

Table 6-2. A21 Processor PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
A21⊗	PROCESSOR PCB ASSEMBLY FIGURE 6-2 (9000A-6802-4071)	632363	89536	632363	REF		
C1	CAP, CER, 22 pF +/-5%, 100V	448449	80031	2222-638-10229	1		
C2-C11	CAP, CER, 0.22 uF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	10		
J1	CONNECTOR, RIGHT ANGLE	512590	89536	512590	1		
J2	CONNECTOR, 40-PIN	585133	89536	585133	1		
MP1	SPACER, STANDOFF	602284	89536	602284	2		
P1	CONNECTOR, AMP PIN	649681	00779	3-87022-2	60		
R1	RES, DEP. CAR, 1 +/-5%, 1/4W	357665	80031	CR251-4-5P1E	1		
R2	RES, COMP, 4.7K +/-5%, 1/4W	348821	01121	CB4725	4		
R3	RES, COMP, 4.7K +/-5%, 1/4W	348821	01121	CB4725	REF		
R4	RES, COMP, 4.7K +/-5%, 1/4W	348821	01121	CB4725	REF		
R5	RES, COMP, 4.7K +/-5%, 1/4W	348821	01121	CB4725	REF		
R6	RES, DEP. CAR, 2.2K +/-5%, 1/4W	343400	80031	CR251-4-5P2K2	1		
U1	IC, RAM, I/O, TIMER ARRAY	536417	55576	SYP6532A	1	1	
U2	IC, TTL, DUAL J-K FLIP/FLOP	414029	01295	SN74LS112N	1	1	
U4⊗	IC, NMOS, 8BIT MICROPROCESSOR	647107	04713	MC68B02P	1	1	
U5⊗	IC, TTL, C-MOS, 6800 CLOCK GENERATOR	586065	04713	MC6875L	1	1	
U6	IC, TTL, QUAD 2-INPUT NAND GATE	654210	89536	654210	1	1	
U7	IC, TTL, QUAD BUS BUFFERS	472746	01295	SN74LS125N	1	1	
U8	IC, TTL, POS NAND GATES, HEX INVERTERS	393058	01295	SN74LS04N	1	1	
U9	IC, TTL, QUAD, 2-INPUT POS AND GATE	393066	01295	SN74LS08N	1	1	
U10	IC, TTL, QUAD, 2-INPUT POS OR GATE	393108	01295	SN74LS32N	2	1	
U11	IC, TTL, QUAD, 2-INPUT POS OR GATE	393108	01295	SN74LS32N	REF		
U12	RESISTOR NETWORK, 2K	574905	89536	574905	1	1	
U13	IC, TTL, POS NAND GATES INV W/TP OUTPUTS	404889	01295	SN74LS30N	1	1	
U14	IC, TTL, QUAD, 2-INPUT, NOR GATE	393090	01295	SN74LS27N	1	1	
XU1	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	2		
XU3	SOCKET, IC, 24-PIN	376236	91506	324-AG39D	1		
XU4	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	REF		
Z1	RESISTOR NETWORK	484063	89536	484063	1	1	
Z2	RESISTOR NETWORK	412916	89536	412916	1	1	

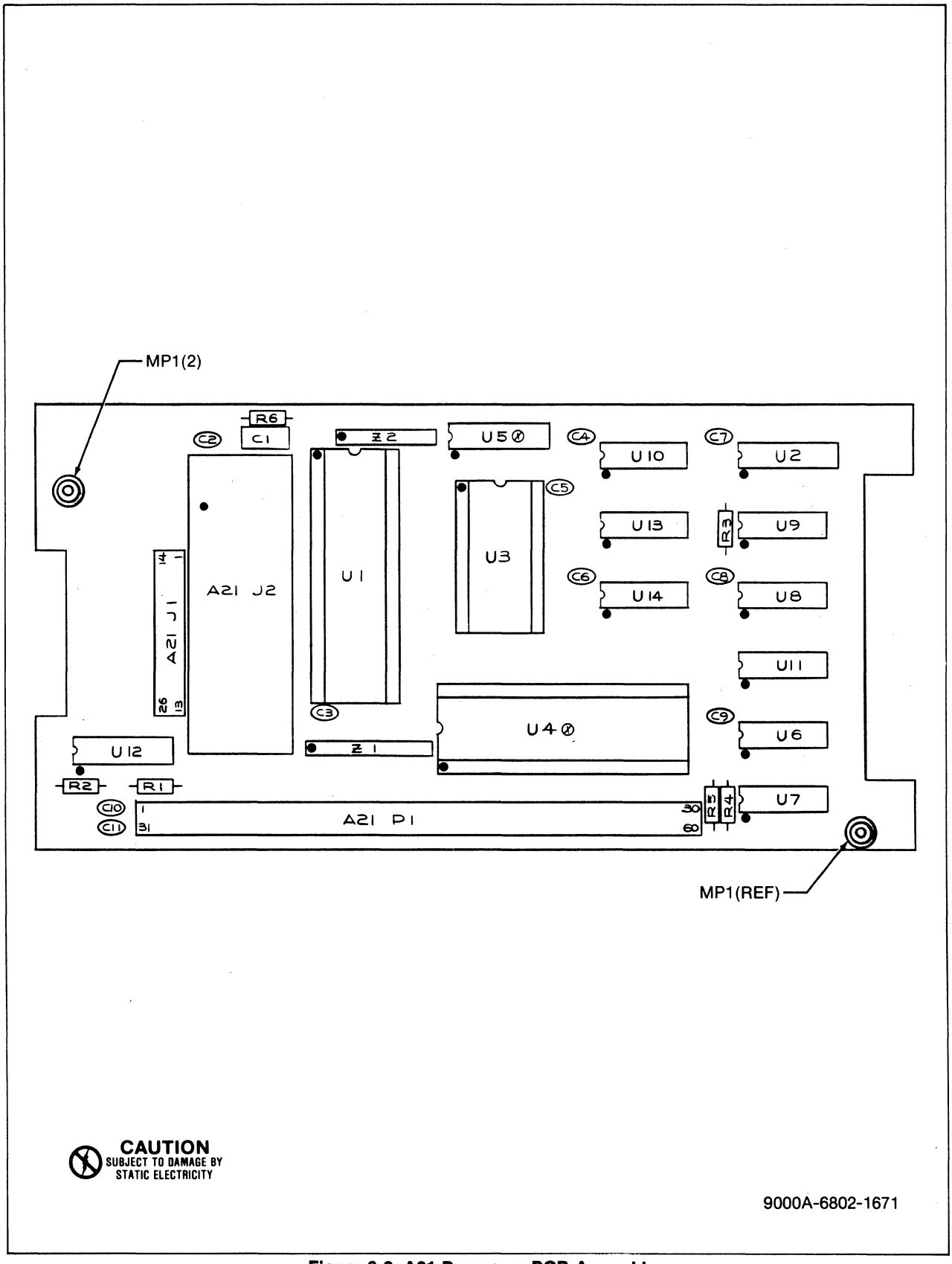


Figure 6-2. A21 Processor PCB Assembly

Table 6-3. A22 Interface PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
A22Ø	INTERFACE PCB ASSEMBLY FIGURE 6-3 (9000A-6802-4072)	642397	89536	642397	REF		
A1	HYBRID, 700< CIRCUIT	582189	89536	582189	1	1	
A2	HYBRID CIRCUIT	582247	89536	582247	4	1	
A3	HYBRID CIRCUIT	582247	89536	582247	REF		
A4	HYBRID CIRCUIT	582247	89536	582247	REF		
A5	HYBRID CIRCUIT	582247	89536	582247	REF		
C1	CAP, CER, 0.01 uF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	1		
C2	CAP, TA, 10 uF +/-20%, 20V	193623	56289	196D106X0020KA1	4		
C3	CAP, TA, 10 uF +/-20%, 20V	193623	56289	196D106X0020KA1	REF		
C4	CAP, CER, 47 pF +/-2%, 100V	512368	89536	512368	2		
C5	CAP, CER, 47 pF +/-2%, 100V	512368	89536	512368	REF		
C6-C21	CAP, CER, 0.22 uF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	16		
C22	CAP, TA, 10 uF +/-20%, 20V	193623	56289	196D106X0020KA1	REF		
C23	CAP, TA, 10 uF +/-20%, 20V	193623	56289	196D106X0020KA1	REF		
CR1-CR5	DIODE, HI-SPEED SWITCHING	203323	15818	1N4448	7	2	
CR6	DIODE, SI, SMALL SIGNAL	313247	28484	HP5082-6264	1	1	
CR7	DIODE, HI-SPEED SWITCHING	203323	15818	1N4448	REF		
CR8	DIODE, HI-SPEED SWITCHING	203323	15818	1N4448	REF		
J1	CONNECTOR, 60-PIN	602813	00779	86396-6	1		
J2	CONNECTOR PINS	267500	00779	87022-1	40		
Q1	TRANSISTOR, PNP, HI-SPEED SWITCHING	369629	07263	2N5771	1	1	
R1	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	4		
R2	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	REF		
R3	RES, COMP, 120 +/-10%, 1/2W	108696	01121	EB1211	1		
R4	RES, DEP. CAR, 2.2K +/-5%, 1/4W	343400	80031	CR251-4-5P2K2	1		
R5	RES, DEP. CAR, 200 +/-5%, 1/4W	441451	80031	CR251-4-5P200E	2		
R6	RES, DEP. CAR, 200 +/-5%, 1/4W	441451	80031	CR251-4-5P200E	REF		
R7	RES, COMP, 820 +/-5%, 1/8W	512806	01121	BB8215	1		
R8	RES, COMP, 3K +/-5%, 1/8W	271379	01121	BB3025	1		
R9	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	REF		
R10	RES, COMP, 330 +/-5%, 1/8W	643965	01121	BB3315	1		
R11	RES, COMP, 10K +/-5%, 1/8W	643940	01121	BB1035	2		
R12	RES, COMP, 10K +/-5%, 1/8W	643940	01121	BB1035	REF		
R13	RES, COMP, 1K +/-5%, 1/8W	643932	01121	BB1025	REF		
R14	RES, DEP. CAR, 220 +/-5%, 1/4W	342626	80031	CR251-4-5P220E	1		
R15	RES, COMP, 36 +/-5%, 1/8W	649855	01121	BB3605	1		
TP1	CONNECTOR, TEST POINT	512889	00779	62395-1	1		
U1Ø	IC, C-MOS, OCTAL BUS TRANSCEIVER	535906	36665	74C245AC	3	1	
U2Ø	IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	5	1	
U3Ø	IC, C-MOS, OCTAL BUS TRANSCEIVER	535906	36665	74C245AC	REF		
U4Ø	IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		
U5Ø	IC, C-MOS, OCTAL BUS TRANSCEIVER	535906	36665	74C245AC	REF		
U6Ø	IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		
U7Ø	IC, TTL, LO-PWR, 3-8 LINE DECODER	407585	01295	SN74LS138N	1	1	
U8Ø	IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		
U9Ø	IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		
U10	IC, PROTECTOR	585992	89536	585992	1	1	
U12	IC, TTL, DUAL 4-INPUT NAND LINE DRIVER	585414	01295	SN74S140N	1	1	

Table 6-3. A22 Interface PCB Assembly (cont)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
U14	IC, LINEAR, 5-XSTR ARRAY	248906	12040	LM3046N	1	1	
U15	IC, TTL, POS NAND GATES, HEX INVERTERS	393058	01295	SN74LS04N	1	1	
VR1	IC, LINEAR, LO-VOLT REF (SELECTED)	452771	89536	452771	1	1	
W1	WIRE, JUMPER, 22AWG	529701	89536	529701	2		
W3	WIRE, JUMPER, 22AWG	529701	89536	529701	REF		
XU1	SOCKET, IC, 20-PIN	454421	01295	C932002	8		
XU2	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU3	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU4	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU5	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU6	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU8	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU9	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU10	SOCKET, IC, 18-PIN	418228	91506	318AG39D	1		
XVR1	INSULATOR	175125	89536	175125	1		
Z1	RESISTOR NETWORK	583476	89536	583476	2	1	
Z2	RESISTOR NETWORK	583476	89536	583476	REF		

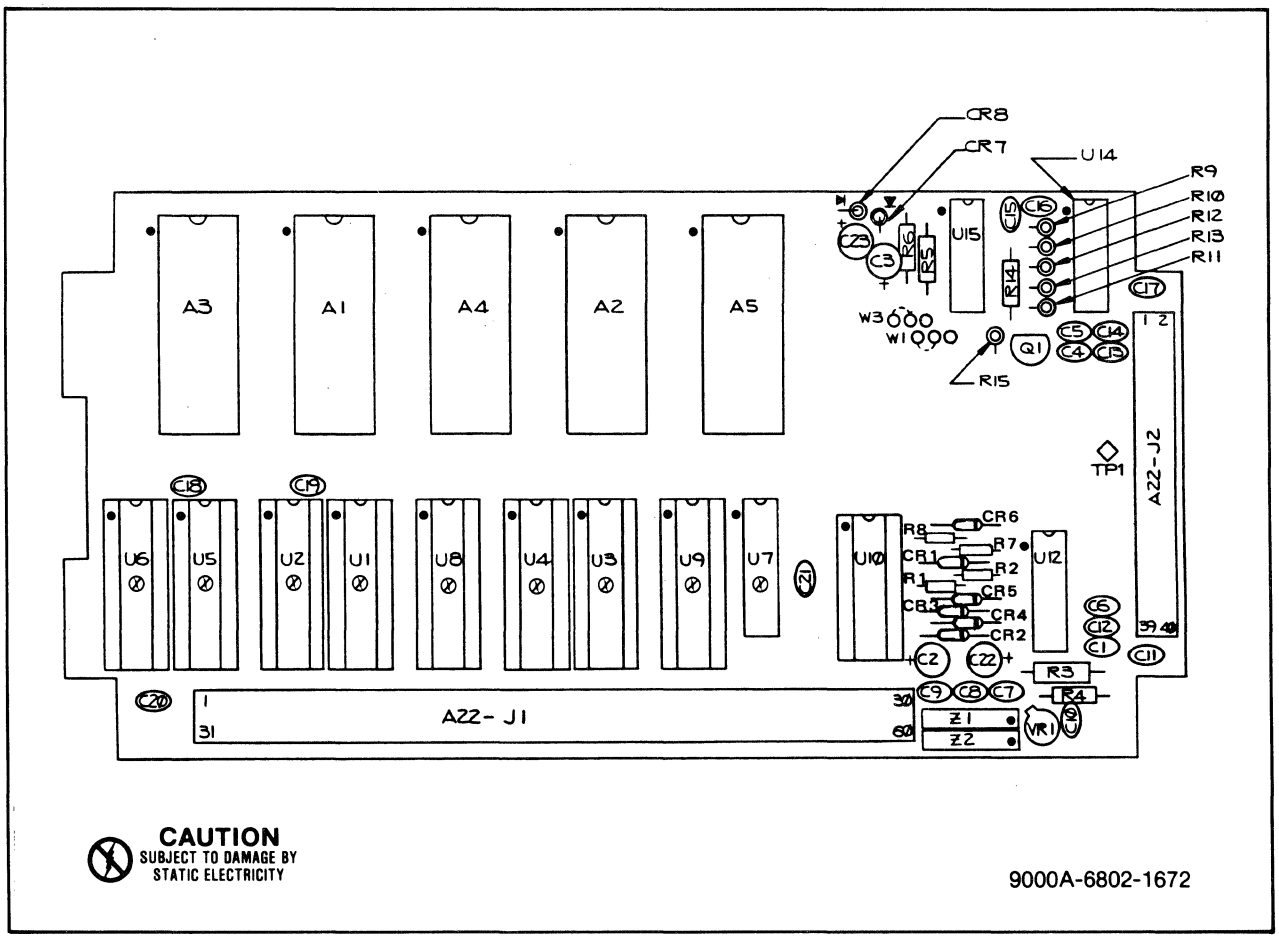


Figure 6-3. A22 Interface PCB Assembly

Table 6-4. Manual Status and Backdating Information

Ref Or Option No.	Assembly Name	Fluke Part No.	* To adapt manual to earlier rev configurations perform changes in desending order (by no.), ending with change under desired rev letter																				
			—	A	B	C	D	E	F	G	H	J	K	L	M	N	P							
A21	Processor PCB Assembly	642363	—																				
A22	Interface PCB Assembly	642397	—																				

* X = The PCB revision levels documented in this manual.
● = These revision letters were never used in the instrument.
–= No revision letter on the PCB.

Section 7
Schematic Diagrams

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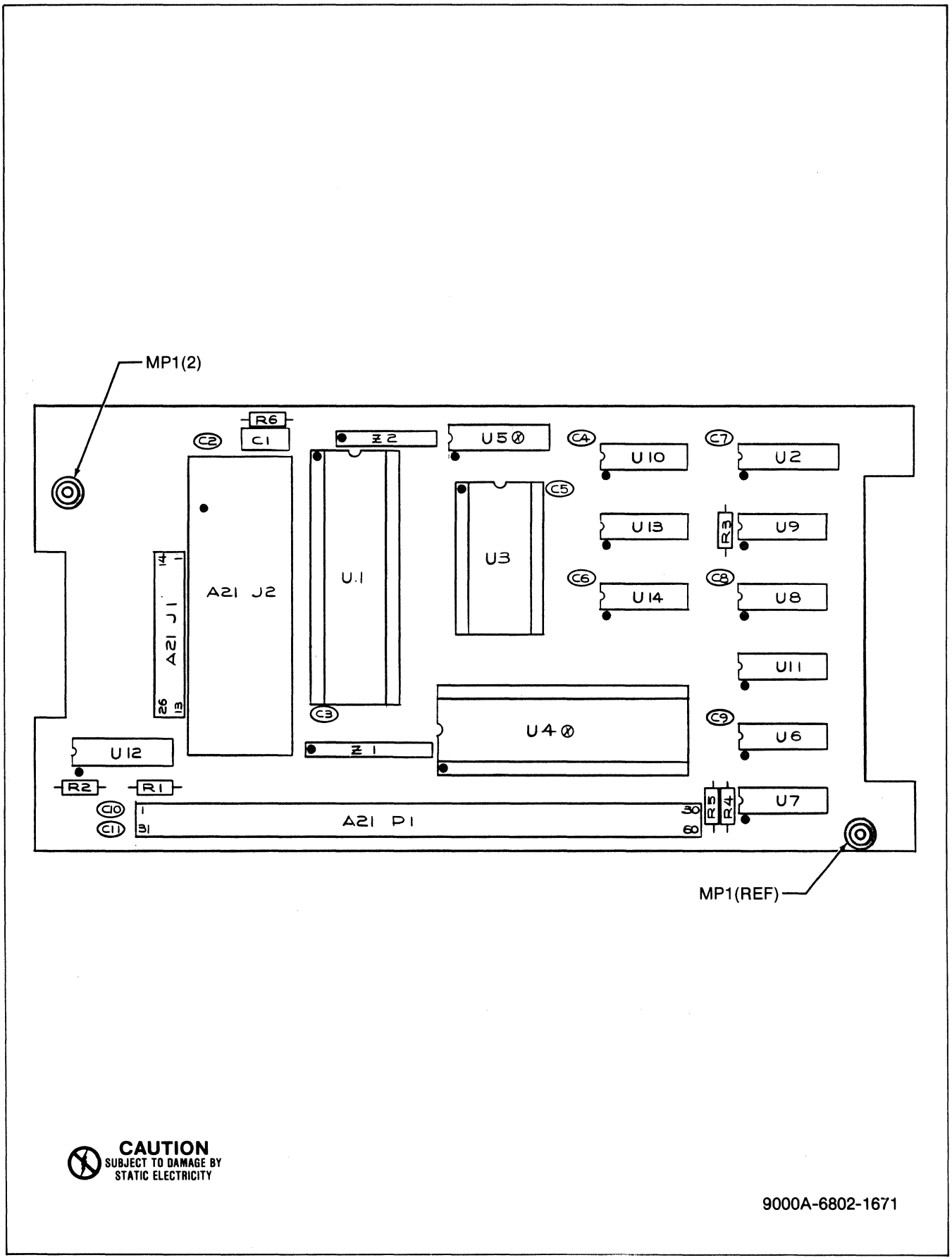
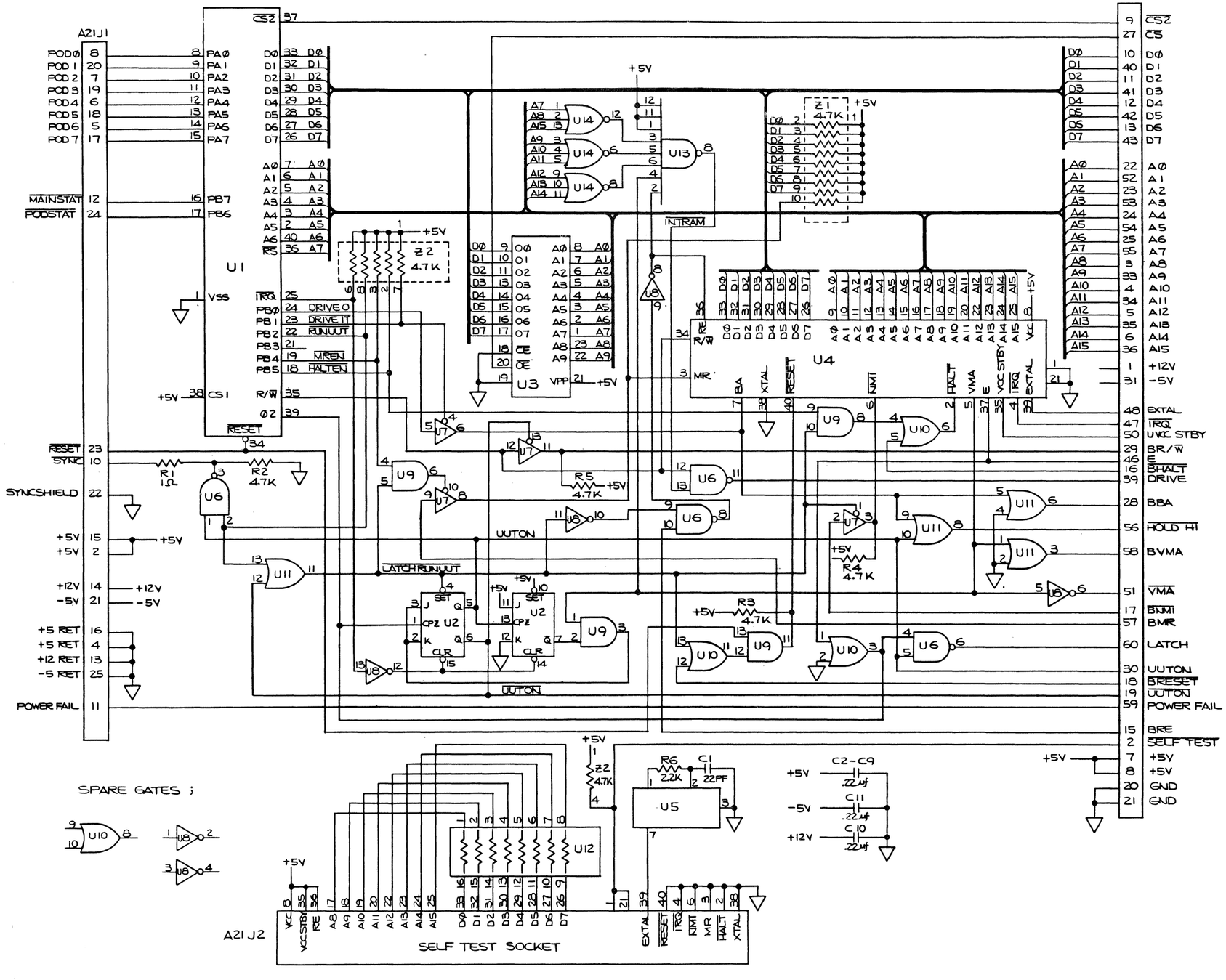


Figure 7-1. A21 Processor PCB Assembly



NOTES ; UNLESS OTHERWISE SPECIFIED.

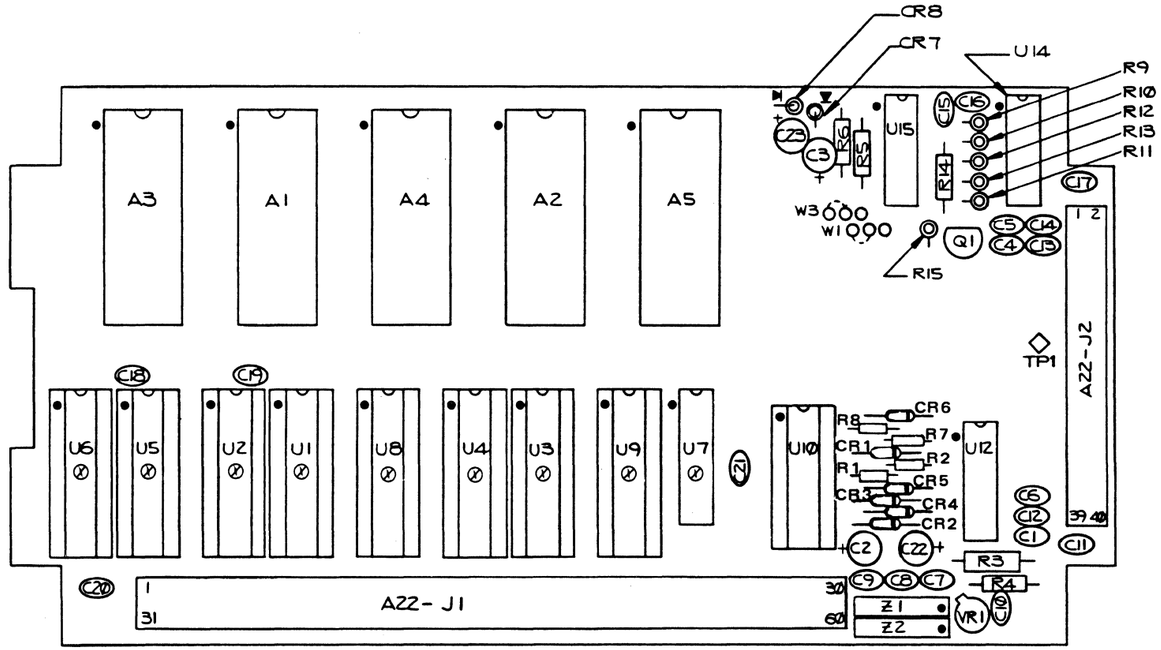
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%
   ALL CAPACITORS ARE IN MICROFARADS.

WARNING: Ⓢ INDICATES USAGE OF MOS DEVICE(S) WHICH MAY BE DAMAGED BY STATIC DISCHARGE. USE SPECIAL HANDLING PER S.O.P. 15.7.

REF DES	DEVICE	+5V	GND	PINS	QTY
Ⓢ U1	RAM I/O 6532A	20,38	1	40	1
U2	74LS112	16	8	16	1
Ⓢ U3	B2716	24	12	24	1
Ⓢ U4	MC68B02	8	1,21,38	40	1
Ⓢ U5	6875 CLOCK	16	3,8	16	1
U6	74LS00	14	7	14	1
U7	74LS125N	14	7	14	1
U8	74LS04	14	7	14	1
U9	74LS08	14	7	14	1
U10,11	74LS32	14	7	14	2
U12	DUAL IN LINE, 2K	—	—	16	1
U13	74LS30	14	7	14	1
U14	74LS27	14	7	14	1
Z 1	RES. NETWORK 4.7K	1	-	10	1
Z 2	RES. NETWORK 4.7K	1	-	8	1

9000A-6802-1071

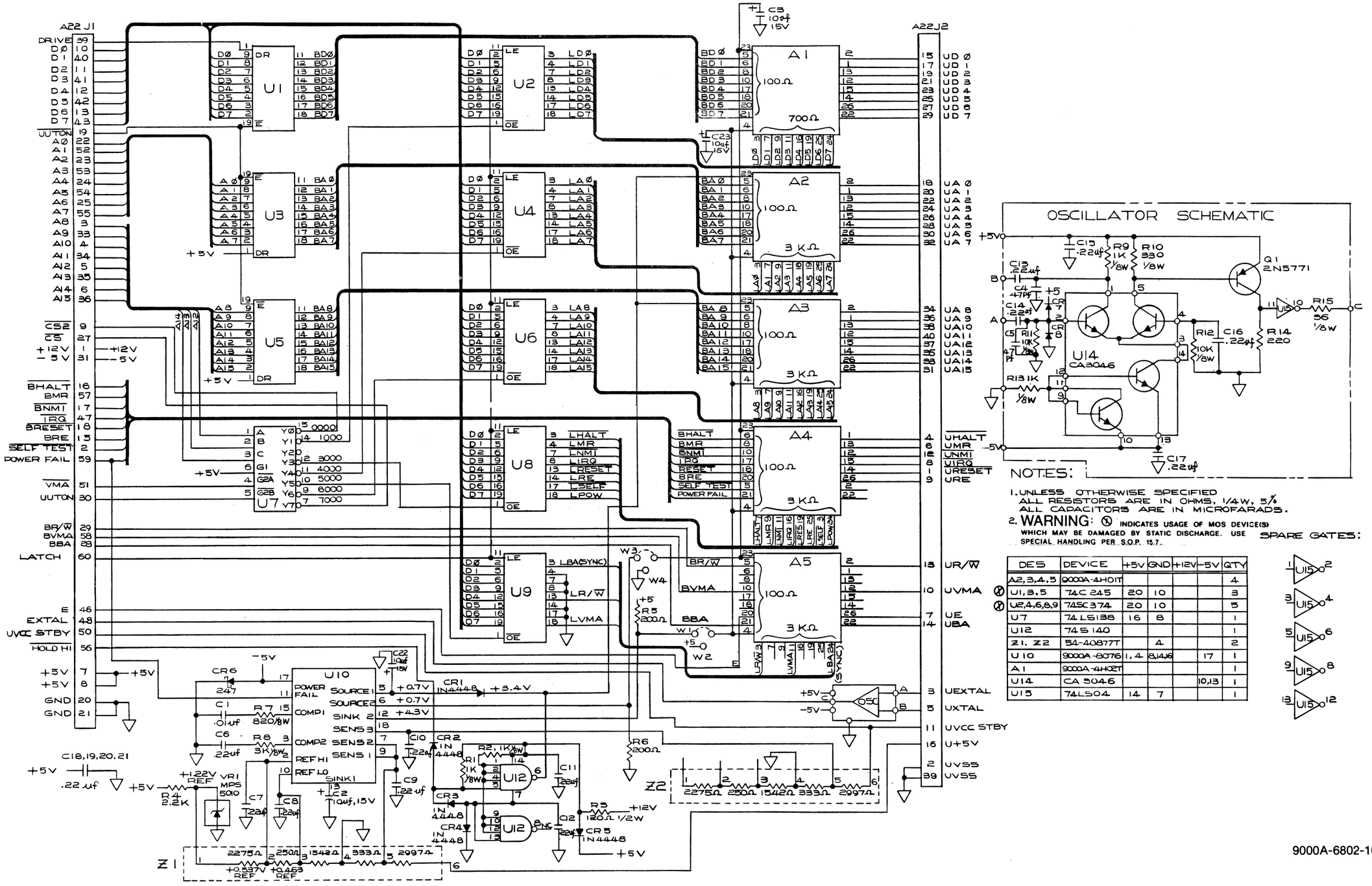
Figure 7-1. A21 Processor PCB Assembly (cont)



CAUTION
SUBJECT TO DAMAGE BY STATIC ELECTRICITY

9000A-6802-1672

Figure 7-2. A22 Interface PCB Assembly



DES	DEVICE	+5V	GND	+12V	-5V	QTY
A2,3,4,5	9000A-4H01T					4
U1,3,5	74C 245	20	10			3
⊗ U2,4,6,8,9	74SC 374	20	10			5
U7	74LS138	16	8			1
U12	74S 140					1
Z1, Z2	54-40877T		4			2
U10	9000A-8076	1, 4	8,14,6		17	1
A1	9000A-4H02T					1
U14	CA 3046				10,13	1
U15	74LS04	14	7			1

Figure 7-2. A22 Interface PCB Assembly (cont)

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CHANGE/ERRATA INFORMATION

ISSUE NO: 1 7/83

This change/errata contains information necessary to ensure the accuracy of the following manual. Enter the corrections in the manual if either one of the following conditions exist:

1. The revision letter stamped on the indicated PCB is equal to or higher than that given with each change.

2. No revision letter is indicated at the beginning of the change/errata.

MANUAL

Title: 9000A-6802
Print Date: May 1982
Rev. and Date: ---

C/E PAGE EFFECTIVITY

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1	7/83
2	7/83
3	7/83

CHANGE #1 - 16649, 16833, 17241
Rev.-C, Final Assembly (9000A-6802-5001)

On page 6-3, Table 6-1:
CHANGE: W2|CABLE ASSEMBLY, UUT|585141|89536|585141|1
TO: W2|CABLE ASSEMBLY, UUT|685479|89536|685479|1

Change the TOT QTY of H1,
FROM: 2
TO: 3

ADD: MP10|RETAINING CLIP|583260|89536|583260|1

On page 6-4, Figure 6-1, add MP10 and H1 as shown in Figure 1.

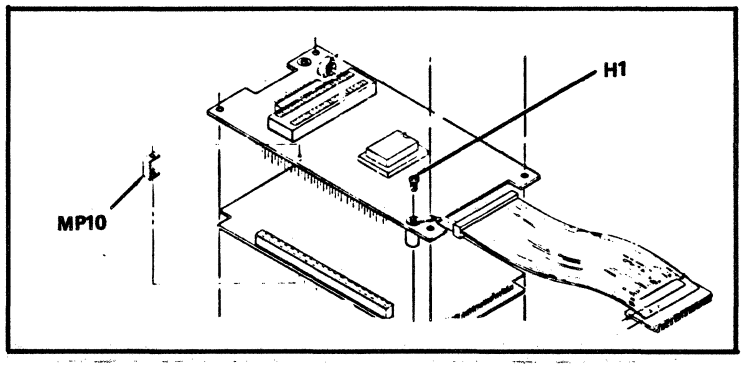

Figure 1.

CHANGE #2 - 17297
Rev.-A, A22 Interface PCB Assembly (9000A-6802-4072)

On page 1-3, Table 1-1:
CHANGE: Tristate Output Leakage Current .. +20 uA
TO: Tristate Output Leakage Current .. +20 uA typ., 200 uA max.

CHANGE: High Level Current ..... 20 uA typ. with Vih = +2.7V
TO: High Level Current ..... 20 uA typ. 200 uA max.

CHANGE: ALL OTHER INPUT LINES ..... -20 uA typ. with Vil = +0.4V
TO: ALL OTHER INPUT LINES ..... -20 uA typ. -200 uA max.

CHANGE: LOW-TO-HIGH TRANSITIONS ..... 20 ns typ.
TO: LOW-TO-HIGH TRANSITIONS ..... 12 ns typ.

CHANGE: HIGH-TO-LOW TRANSITIONS ..... 24 ns typ.
TO: HIGH-TO-LOW TRANSITIONS ..... 15 ns typ.

On page 6-7, Table 6-3:

```
 CHANGE: U1|IC, C-MOS, OCTAL BUS TRANSCEIVER
                                    |535906|36665|74C245AC   |3|1
 TO:     U1|IC, ALSTTL, OCTAL BUS XCVR W/TRISTATE
                                    |647214|01295|SN74ALS245N|3|1

 CHANGE: U3|IC, C-MOS, OCTAL BUS TRANSCEIVER
                                    |535906|36665|74C245AC   |REF
 TO:     U3|IC, ALSTTL, OCTAL BUS XCVR W/TRISTATE
                                    |647214|01295|SN74ALS245N|REF

 CHANGE: U5|IC, C-MOS, OCTAL BUS TRANSCEIVER
                                    |535906|36665|74C245AC   |REF
 TO:     U5|IC, ALSTTL, OCTAL BUS XCVR W/TRISTATE
                                    |647214|01295|SN74ALS245N|REF
```

On page 7-5, Figure 7-2, change the DEVICE for U1, U3 and U5,

```
 FROM:   74C245
 TO:     74ALS245
```

CHANGE #3 - 17487

Rev.-D, Final Assembly (9000A-6802-5001)
Rev.-A, A21, Processor PCB Assembly (9000A-6802-4071T)

On page 6-3, Table 6-1:

```
 CHANGE: W1|CABLE ASSEMBLY, POD |581827|89536|581827|1
 TO:     W1|CABLE POD W/RESISTOR|581819|89536|581819|1
```

On page 6-5, Table 6-2:

```
 CHANGE: R1|RES, DEP. CAR, 1 +/-5%, 1/4W |357665|80031|CR251-4-5P1E |1
 TO:     R1|RES, DEP. CAR, 39 +/-5%, 1/4W|340836|80031|CR251-4-5P39E|1

 DELETE: R2|....

 ADD:    R7|RES, DEP. CAR, 68 +/-5%, 1/4W|414532|80031|CR251-4-5P68E|1

 CHANGE: U6|IC, TTL, QUAD 2-INPUT NAND GATE |654210|89536|654210 |1|1
 TO:     U6|IC, FTTL, QUAD 2-INPUT NAND GATE|654640|07263|74F00PC|1|1
```

On page 6-6, Figure 6-2, delete R2 and add R7 as shown in Figure 2.

On page 7-3, Figure 7-1, make the following changes as shown in Figure 3.

```
 Change the value of R1,
 FROM:   1
 TO:     39

 DELETE: R2
 ADD:    R7
```

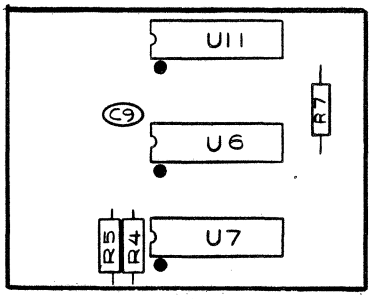

Figure 2.

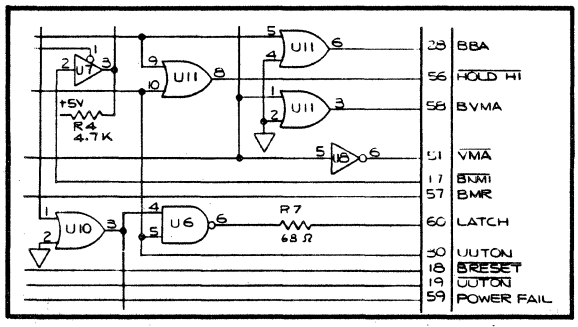

Figure 3.