9000A-8080
Interface Pod

Instruction Manual

FLUKE®

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FLUKE®

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Section 1
Introduction

1-1. PURPOSE OF INTERFACE POD

The purpose of the 9000A-8080 Interface Pod, hereafter referred to as the pod, is to interface any 9000 Series Micro System Troubleshooter to a piece of equipment employing a 8080 microprocessor.

The 9000 Series Micro System Troubleshooters are designed to service printed circuit boards, instruments and systems employing bus-oriented microprocessors. While the architecture of the troubleshooter main frame is general in nature and is designed to accomodate processors with up to 32 address lines and 32 data lines, the interface pod adapts the general purpose architecture of the 9000 Series to a specific microprocessor, or microprocessor family. The interface pod adapts the 9000 Series to microprocessor-specific functions such as pin layout, status/control functions, interrupt handling, timing, size of memory space, and size of I/O space.

1-2. DESCRIPTION OF INTERFACE POD

The pod consists of a pair of printed circuit board assemblies mounted within a small break-resistant case. A shielded 24-conductor cable connects the printed circuit boards to the troubleshooter; a ribbon cable and connector provide connection to the unit under test, hereafter referred to as the UUT.

Figure 1-1 shows the relationship of the pod to the troubleshooter and to the UUT. Connection from the pod to the troubleshooter is via a front-mounted 25-pin connector. Connection to the UUT is made by plugging the ribbon cable plug directly into the microprocessor socket. The UUT microprocessor socket gives the troubleshooter direct access to all system components which normally communicate with the microprocessor.

The pod contains a 8080 microprocessor and the supporting hardware and control software required to:

- Perform handshaking with the troubleshooter

- Receive and execute commands from the troubleshooter
- Report UUT status to the troubleshooter
- Emulate the UUT microprocessor

The pod is powered by the troubleshooter, but is clocked by the UUT clock signals. Using the UUT clock signals allows the troubleshooter and pod to operate at the designed operating speed of the UUT.

Logic level detection circuits are provided on each line to the UUT. These circuits allow detection of bus shorts, stuck-high or stuck-low conditions, and any bus drive conflict (two or more drivers attempting to drive thesame bus line).

Over-voltage protection circuits are also provided on each line to the UUT. These circuits guard against pod damage which could result from:

- Incorrectly inserting the ribbon cable plug in the UUT microprocessor socket.
- UUT faults which place potentially damaging voltages on the UUT microprocessor socket.

The over-voltage protection circuits guard against voltages of +12 to -7 volts on any one pin. Multiple faults, especially of long duration, may cause pod damage.

A power level sensing circuit constantly monitors the voltage level of the UUT power supplies. If any UUT power supply rises above or drops below an acceptable level, the pod notifies the troubleshooter of the power fail condition.

A self test socket provided on the pod enables the troubleshooter to check pod operation. The self test socket is a 40-pin zero-insertion force type connector. The ribbon cable plug must be connected to the self test socket during self test operation. The ribbon cable plug should also be inserted into this socket when the pod is not in use to provide protection for the plug.

1-3. SPECIFICATIONS

Specifications for the 9000A-8080 Interface Pod are listed in Table 1-1.

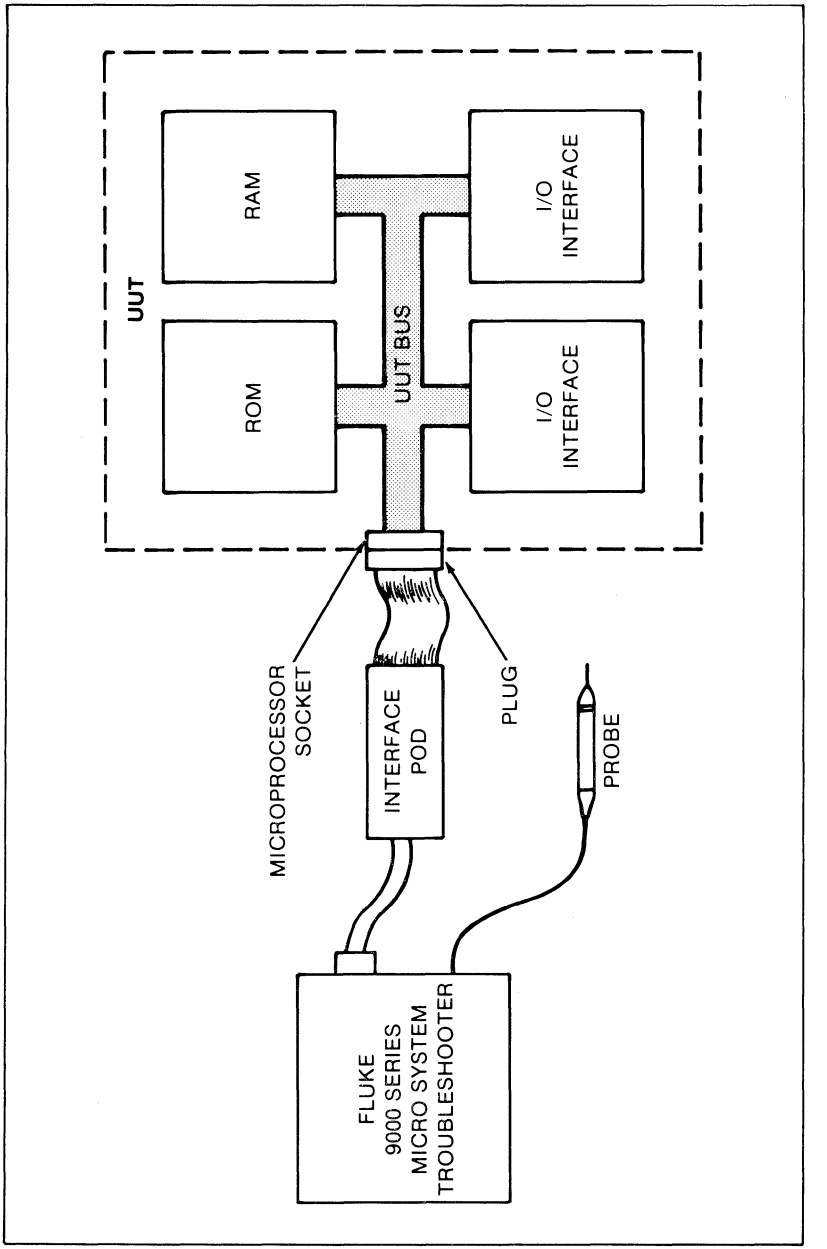

Figure 1-1. Relationship of Interface Pod

Table 1-1. 8080 Interface Pod Specifications

ELECTRICAL PERFORMANCE	
Power Dissipation	3.0 watts maximum
Electrical Protection	
CLOCK INPUTS	-0.5 to +12 volts may be applied between ground and any ribbon cable plug pin continuously cable plug pin continuously as long as the pod is powered by the troubleshooter.
OTHER INPUTS	-7 to +12 volts may be applied between ground and any ribbon cable plug pin continuously as long as the pod is powered by the troubleshooter.
MICROPROCESSOR SIGNALS	
Clock Input Low	0V min., +0.8V max.
Clock Input High	+9.0V min., +13.0V max.
Input Low Voltage	0V min., +0.8V max.
Input High Voltage	+2.0V min., +5.0V max.
Output Low Voltage	+0.4V max. with Iol = 1.9 mA
Output High Voltage	+3.7V min. with Ioh = -250 μA
Tristate Output Leakage Current	$\pm$20 μA
High Level Input Current	20 μA typ. with Vih = +2.7V
Low Level Input Current	
READY, HOLD, RESET	-400 μA max. with Vil = +0.4V
ALL OTHER INPUT LINES	-20 μA typ. with Vil = +0.4V
TIMING CHARACTERISTICS	
Maximum Clock Frequency	3.0 MHz typ.
Added Delays to 8080 Signals	
LOW-TO-HIGH TRANSITIONS	20 ns typ.
HIGH-TO-LOW TRANSITIONS	24 ns typ.

Table 1-1. 8080 Interface Pod Specifications (cont)

UUT POWER DETECTION

Detection of High +5V Fault	Vcc > +5.5V detected
Detection of Low +5V Fault	Vcc < +4.5V detected
Detection of High +12V Fault	Vdd > +13.2V detected
Detection of Low +12V Fault	Vdd < +10.8V detected
Detection of High -5V Fault	Vbb > -5.5V detected
Detection of Low -5V Fault	Vbb < -4.5V detected

GENERAL

Size	3.3 cm High x 10.2 cm Wide x 18.55 cm Deep (1.3 in High x 4.0 in Wide x 7.4 in Deep)
Weight	0.68 kg (1.5 lbs)
Environment	
STORAGE	-40° to +70°C, RH< 95%
OPERATING	0° to +25°C, RH < 95% +25° to +40°C, RH < 75% +40° to +50°C, RH < 45%

Section 2
Installation

2-1. GENERAL

Before a 9000 Series Micro System Troubleshooter can be used to perform any testing or fault isolation, it must be connected to the UUT. Connection is made by means of the pod, which is equipped with two cable assemblies, one shielded-type and one ribbon-type. The procedures for installing and connecting the pod are given in the following paragraphs.

2-2. MAKING CONNECTIONS

Before making any connections to the UUT, take note of the following precautions:

WARNING

TO PREVENT POSSIBLE HAZARDS TO THE OPERATOR OR DAMAGE TO THE UUT, DISCONNECT ALL HIGH-VOLTAGE POWER SUPPLIES, THERMAL ELEMENTS, MOTORS, OR MECHANICAL ACTUATORS WHICH ARE CONTROLLED OR PROGRAMMED BY THE UUT MICROPROCESSOR BEFORE CONNECTING POD.

- Be sure to install the ribbon cable plug correctly in the UUT microprocessor socket.

- The self test socket is intended for use with the ribbon cable plug only. Do not insert any microprocessor removed from a UUT under test, or any other device into this socket.

Connect the pod between the troubleshooter and the UUT as follows:

1. Remove power from the troubleshooter and the UUT.

2. Using the round shielded cable, connect the pod to the troubleshooter as shown in Figure 2-1. Secure the connector using the sliding collar.

3. Perform a self-test of the pod as described in Section 5 of this manual.

4. With UUT power off, unplug the microprocessor from the UUT.

5. On the pod, turn the self test socket thumbwheel to release the plug from the self test socket.

6. Align the ribbon-cable with the microprocessor socket on the UUT so that the notched corner of the ribbon cable plug aligns with pin 1 of the socket. Insert the plug into the socket as shown in Figure 2-2.

7. Electrically reassemble the UUT. Use extender boards if necessary.

CAUTION

Ensure troubleshooter power is on before turning UUT power on in order to activate pod protection circuits.

8. Apply power to the troubleshooter.

9. Apply power to the UUT.

2-3. POWER CONNECTIONS

The pod receives +5 volts, -5 volts, and +12 volts from the 9000 Series Micro System Troubleshooter. No external power connections are required.

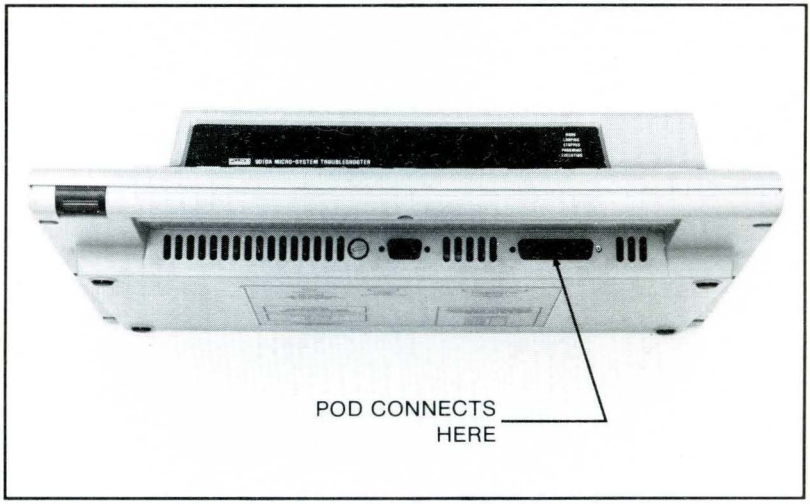

Figure 2-1. Connection of Interface Pod to Troubleshooter

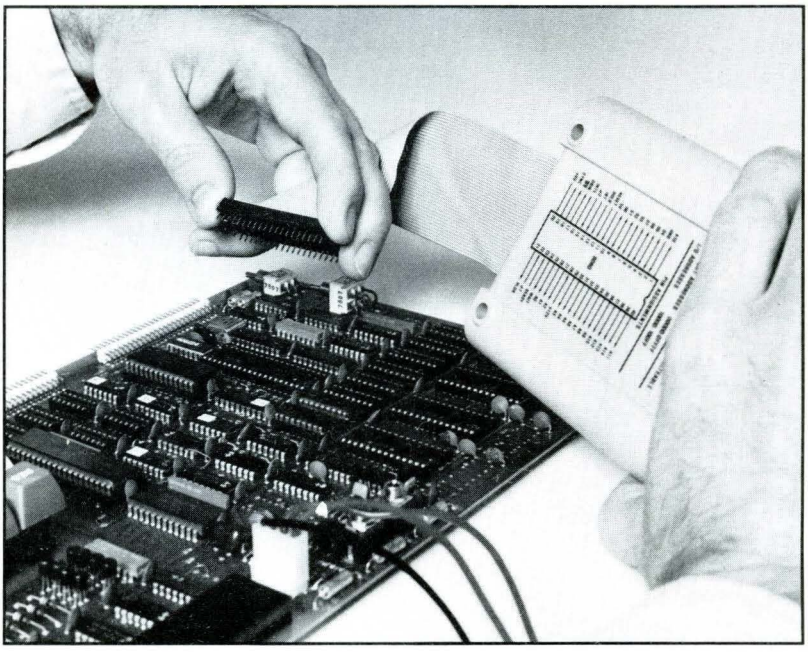

Figure 2-2. Connection of Interface Pod to UUT

Section 3
Microprocessor Data

3-1. INTRODUCTION

This section contains information which may be useful during operation of the troubleshooter. This information includes 8080 signal descriptions, explanations of status/control lines and address space assignment, the effects the pod may have on normal UUT operation, the pod capabilities and limitations, and pertinent pod characteristics.

3-2. 8080 SIGNALS

For reference, Table 3-1 lists all of the 8080 signals and provides a brief description of each. Figure 3-1 shows the pin assignment of 8080 signals.

Table 3-1. 8080 Signals

SIGNAL NAME	DESCRIPTION
Address Lines A0 - A15	The 16 address lines are designated A0 through A15. The address lines are tri-state output and may be logic high, logic low, or floated by the 8080 to a high impedance state. The 8080 places the address lines in a high impedance state to allow devices other than the 8080 to control the address bus during DMA (Direct Memory Access) operations. See HOLD.
Data lines D0 - D7	The 8 data lines are designated D0 through D7. The data lines are bidirectional lines used to input and output data, and also used to output status during the first clock period of any machine cycle. (Status on the data bus identifies events which are to occur during the balance of the machine cycle; refer to manufacturer's data for additional information.) The data lines are tri-state lines. See HOLD.
SYNC Line	The SYNC output goes high during the period of the first phase-two clock pulse for each machine cycle.

Table 3-1. 8080 Signals (cont)

SIGNAL NAME	DESCRIPTION
	The SYNC output permits synchronization of external logic with status information present on the data lines.
DBIN Line	The DBIN line is made output high to indicate that the 8080 is ready to read data via the data lines from either memory or an I/O device. DBIN may be used as a data input strobe.
$\overline{WR}$ Line	The $\overline{WR}$ line is made output low when data on the data bus is stable, indicating the 8080 is ready to write data to either memory or an I/O device. The $\overline{WR}$ line may be used as a write strobe.
READY Line	The READY line is an input which, when placed at a logic low level, causes the 8080 to enter a wait state. During the wait state, the 8080 inserts clock pulses to extend cycle time as required by the external logic selecting the wait state.
WAIT Line	The WAIT line is made output high during the wait state caused by an input to the READY line.
INT Line	The INT line is an input which, when made a logic high level, permits the external interrupt of the 8080.
INTE Line	The INTE line is made output high to indicate that interrupts are enabled by the 8080. The INTE output is made low when an interrupt is acknowledged.
RESET Line	The RESET line is an input which, when placed at a logic low level for a minimum of three clock periods, resets the program counter and other registers to zero.
HOLD Line	The HOLD line is an input which, when placed at a logic high level, causes the 8080 to halt at the completion of the current instruction. During the HOLD state, the 8080 relinquishes control of the system bus by floating the address and data lines to a high impedance state. External control of the system bus is necessary during DMA (direct memory access) operations.
HLDA Line	The HLDA line is made output high when the 8080 acknowledges a HOLD input and floats the system bus to a high impedance state.

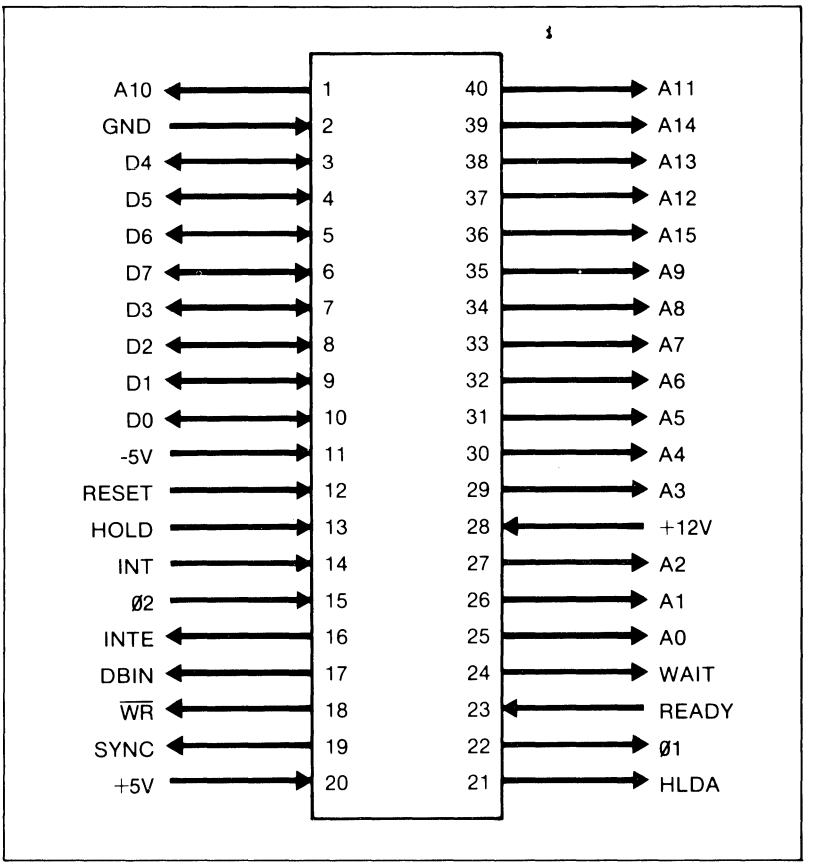

Figure 3-1. 8080 Pin Assignments

3-3. STATUS/CONTROL LINES AND ADDRESS SPACE ASSIGNMENT

3-4. Introduction

The 9000A Series Micro System Troubleshooters are designed to accomodate bus-oriented processors having up to 32 address lines, 32 data lines, 16 status lines, and 8 control lines. The pod provides an interface between the general architecture of the 9000 Series and the specific requirements of the 8080 microprocessor. As part of this interface task, the pod makes specific assignments between the microprocessor lines and the 9000 Series troubleshooter. These assignments include:

- Bit number assignment of 8080 status lines

- User-writable control lines
- Bit number assignment of control lines
- Address space assignment
- Pin assignments

These assignments are described in the following paragraphs and are summarized for convenience on the pod decal.

3-5. Bit Assignment - Status Lines

When a read status (READ @ STS) operation is performed, the troubleshooter displays the result in binary form, where a "1" indicates a logic high status line. To determine which bits of the displayed read status correspond to specific status lines, each line has an assigned bit number, as listed in Table 3-2. Bit number zero (READ) appears at the far right of the display, while bit number 7 (POWER FAIL) appears at the far right.

For example, if the READY (bit number 0) and POWER FAIL (bit number 7) lines are low, and the other status lines are high, the troubleshooter would read *READ @ STS = 0001 1010 OK.* Bit numbers 0 (READY) and 7 (POWER FAIL) are zero to indicate a logic low, while other meaningful bits are ones to indicate logic high. Bits 2, 5 and 6, which have no meaning for 8080 status lines, are always represented by zeros in the troubleshooter display message.

3-6. User-Writeable Control Lines

The 8080 has three control lines which the troubleshooter can write to. These lines are interrupt enable (INTE), wait (WAIT) and hold acknowledge (HLDA). To write to any or all of these lines, a WRITE CTL function is used as described in the paragraphs that follow. Note that writing to a control line only sets the line to the high or low state for approximately 20 microseconds; just long enough to verify that it can be driven.

3-7. Bit Assignment - Control Lines

There are two troubleshooting functions which require the entry of binary digits to identify user-writeable control lines. These functions include write control (WRITE @ CTL) and data toggle control (DTOG @ CTL).

When performing or programming either of these two functions, the user is prompted for a binary number to identify the control line(s) to be written, HLDA, WAIT, and INTE. Table 3-2 shows that these lines have bit numbers 0, 1 and 2 respectively. To perform a write control operation on these three lines,

enter any of the following bit configurations in response to the prompt. As with the status lines, bit number 0 is at the far right of the display.

000	writes all lines low
001	writes HLDA high, WAIT and INTE low
010	writes WAIT high, HLDA and INTE low
011	writes HLDA and WAIT high, INTE low
100	writes INTE high, HLDA and WAIT low
101	writes HLDA and INTE high, WAIT low
110	writes WAIT and INTE high, HLDA low
111	writes all lines high

If any control line cannot be driven, the troubleshooter responds with the message *CTRL ERR @ xxxxxxxx LOOP?*, where x equals a binary 1 if that line is not driveable. For example, if in the write control operation, the WAIT line can be driven, but the INTE and HLDA lines cannot, the troubleshooter displays the message *CTRL ERR @ 00000101 LOOP?*, indicating that the lines represented by bit numbers 0 and 2 cannot be driven. The HLDA line is represented by bit number 0, while the INTE line is represented by bit number 2.

When performing a BUS TEST, and various other troubleshooter operations, the troubleshooter message *CTL ERR xxxxxxxx-LOOP?* can occur, where x represents a binary number that identifies which lines can or cannot be driven. A binary 0 represents the ability to drive a line, while a binary 1 represents the inability to drive a line. Table 3-2 lists all control lines and their respective bit numbers.

Table 3-2. Status and Control Lines Bit Assignments

STATUS LINES		CONTROL LINES	
BIT NO.	**SIGNAL**	**BIT NO.**	**SIGNAL**
7	PWR FAIL	7	—
6	—	6	SYNC
5	—	5	$\overline{WR}$
4	**RESET	4	DBIN
3	INT	3	—
2	—	2	*INTE
1	**HOLD	1	*WAIT
0	**READY	0	*HLDA

*User Writeable ** Forcing Line

3-8. Address Space Assignment

The 8080 is capable of addressing up to 65,536 memory locations and up to 65,536 I/O locations. The 9000 Series troubleshooter uses a consistent technique of addressing multiple memory and I/O locations.

In order to access one of the 65,536 memory locations, the user provides a hexadecimal address in the range of 0000 to FFFF. In order to access one of the I/O locations, the user provides a hexadecimal address in the range of 10000 to 100FF. For convenience, these assignments are also summarized on the pod decal.

3-9. FORCING AND INTERRUPT LINES

Several troubleshooter messages are used to indicate errors and conditions associated with forcing lines and interrupts. Forcing lines are those lines which, when made active, force the microprocessor into some specific action. Forcing lines for the 8080 are RESET, HOLD and READY. Pulling HOLD high or READY low could cause the pod to stop and timeout. Note that these two lines can be disabled during troubleshooter setup procedures. If the RESET line is pulled high, the pod reports such a condition to the troubleshooter, but pod operation is unaffected. The interrupt line for the 8080 is the INT line.

NOTE

During troubleshooter setup, disabling HOLD and READY eliminates any effect they might have on troubleshooter/pod operation. Not reporting (trapping) forcing lines or interrupts during setup simply eliminates the corresponding troubleshooter message.

3-10. LINES ENABLED DURING TROUBLESHOOTER SETUP

During setup of the troubleshooter, the operator has the option of enabling or not enabling certain forcing lines as a means of preventing UUT faults from disabling the pod microprocessor. For the 8080, these lines include HOLD and READY. Also during troubleshooter setup, the operator may elect to report (trap) or disregard active signals on the forcing lines. Reporting active forcing lines halts troubleshooter operation in order to display the forcing line message.

3-11. NON-DETECTABLE 8080 SIGNALS

The pod does not detect the presence of the SYNC signal. However, this signal can be observed, if necessary, by using the probe or scope trigger output of the troubleshooter to trigger a scope. (See timing diagram in Section 4.)

3-12. MARGINAL UUT PROBLEMS

3-13. Introduction

The pod is designed to approximate, as closely as possible, the actual characteristics of the microprocessor it replaces in the UUT. However, the pod

does differ in some respects. In general, these differences tend to make marginal UUT problems more visible. A UUT may operate marginally with the actual microprocessor installed, but tend to exhibit errors with the pod plugged in. The pod differences tend to make marginal UUT problems more obvious and easier to troubleshoot. Different UUT and pod operating conditions that may reveal marginal problems are described in the paragraphs which follow.

3-14. UUT Operating Speed and Memory Access

UUTs designed to operate at speeds which approach the time limits for memory access may be operating marginally. Inherent delays present in the pod may result in the reporting of errors in memory, which is otherwise operating marginally.

3-15. UUT Noise Levels

UUTs operate with a certain amount of noise, and as long as the noise level is low enough, normal operation is unaffected. Removing the UUT from its chassis or case may disturb the integrity of the shielding to the point where intolerable noise could exist. The pod may introduce additional noise. In general, marginal noise problems will actually be made worse (and easier to troubleshoot) through use of the pod and troubleshooter.

3-16. Bus Loading

The pod loads the UUT slightly more than the UUT microprocessor. The pod also presents more capacitance than the microprocessor. These effects tend to make any bus drive problems more obvious.

3-17. Clock Loading

The pod increases the normal load on the UUT clock. While this loading will rarely have any affect on clock operation, it may make marginal clock sources more obvious.

3-18. POD DRIVE CAPABILITY

As a driving source on the UUT bus, the pod provides equal to or better than normal 8080 current drive capability. All pod inputs and outputs (except the clock) are TTL compatible.

3-19. POWER FAILURE DETECTION LIMITS

A power sensing circuit within the pod produces a power fail output to the troubleshooter whenever the power supplies in the UUT drop below or increase above certain limits. The power failure detection limits are listed in the specifications table, Table 1-1.

Section 4
Theory of Operation

4-1. INTRODUCTION

This section contains two block diagram descriptions of the pod. The first is generalized; it describes the operating concept of the pod and the relationship of the pod to the troubleshooter and UUT. The second description covers pod operation in more detail.

4-2. GENERAL POD OPERATION

The pod may be divided into the following three major areas:

- Processor Section
- UUT Interface Section
- Timing Section

4-3. Processor Section

The Processor Section, shown in Figure 4-1, is made up of a microprocessor, RAM, a ROM, and an I/O interface to the troubleshooter. These elements comprise a small computer system which receives troubleshooter commands and directs all pod operations during execution. All reset and other disrupting inputs are hardware disabled, or may be software disabled, to prevent UUT faults from disabling the pod microprocessor.

The Processor Section has the capability of operating with the troubleshooter, or with the UUT, but not with both concurrently. The microprocessor spends most of its time monitoring the troubleshooter I/O interface for commands. During this time, the data and address buses of the Processor Section are isolated from the UUT Interface Section (although the pod sends signals to the UUT so that continuous read operations at the reset address appear to be taking place in order to refresh any dynamic RAM).

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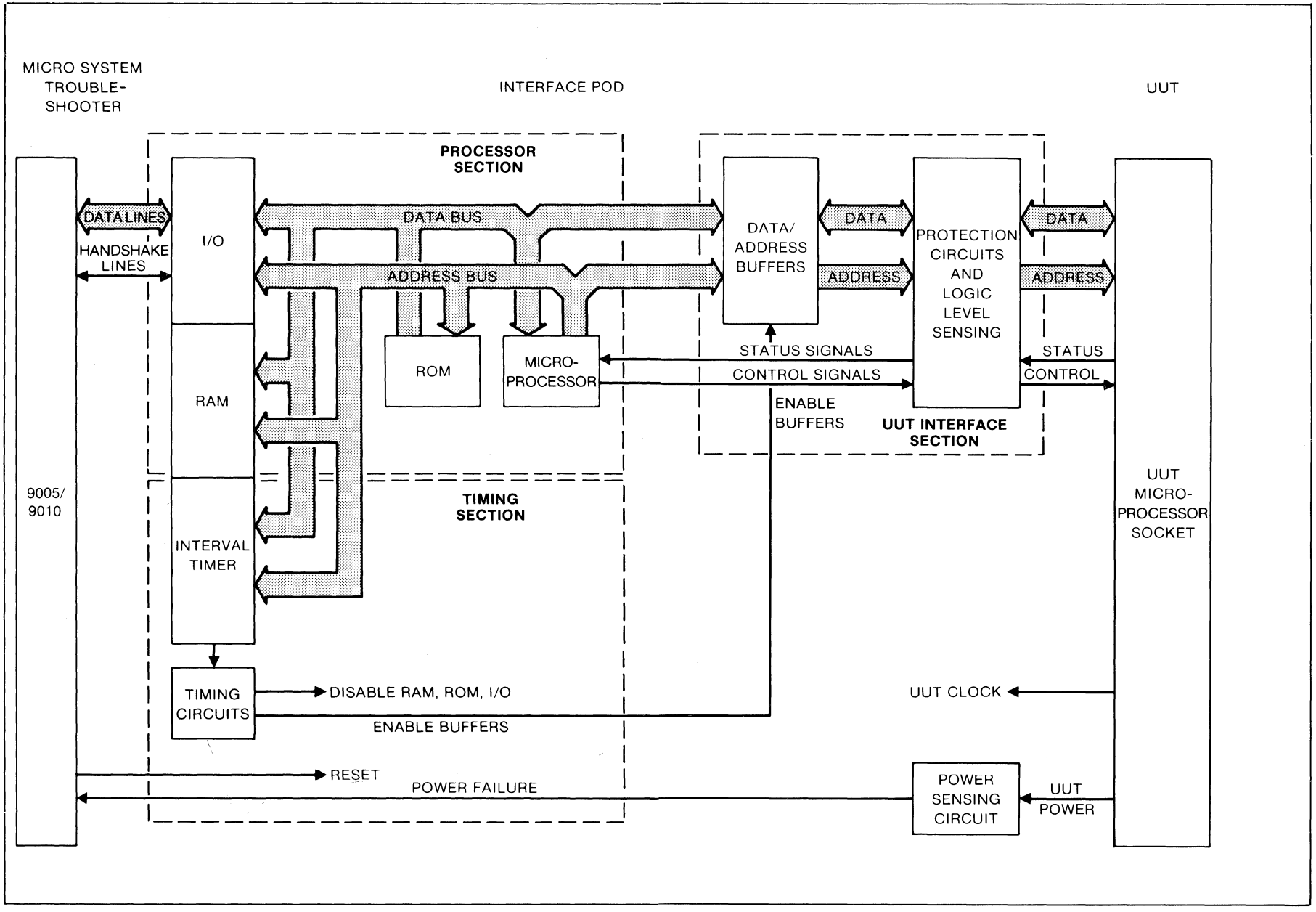

Figure 4-1. General Block Diagram

4-4. UUT Interface Section

The UUT Interface Section, shown in Figure 4-1, include the following elements:

- Data and address buffers
- Protection circuits for signal lines
- Logic level detection circuits for data, address, status and control lines

The data and address buffers are enabled to connect the microprocessor to the UUT, or disabled to isolate the microprocessor from the UUT. Control of the buffers is maintained by the timing section.

Each line to the UUT contains a protection circuit. A protection circuit consists of a 100-ohm series-resistor and clipping diodes. This circuit prevents over voltage conditions from damaging pod components.

Each line to the UUT contains a dectection circuit. A detection circuit consists of a latch connected to the UUT side of the 100-ohm protection resistor. The latch senses the level at the UUT side of the protection circuit, and at the conclusion of each UUT operation, stores the level of the UUT line. Each latch is then individually addressed and read by the Processor Section. Their contents are then compared with the desired results as a means of detecting UUT bus faults.

4-5. Timing Section

The primary function of the timing section is to cause the microprocessor to work with either the Processor Section or the UUT Interface Section at a time pre-determined by the microprocessor itself. Causing the microprocessor to work with one section or the other as required during the execution of troubleshooter commands, permits the use of only one microprocessor in the pod.

The Timing Section of the pod, shown in Figure 4-1, consists of an interval timer and an arrangement of timing circuits. The interval timer, preset by the microprocessor, determines the time at which the microprocessor switches from addressing the Processor Section (RAM, ROM and I/O) to addressing the UUT Interface Section (and UUT). This timing is critical, since any attempt by the microprocessor to address the Processor Section with addresses meant for the UUT, or vice versa, would result in improper operation.

In their reset state, the timing circuits cause the microprocessor to operate as a part of the Processor Section, which includes an I/O port to the troubleshooter. When the troubleshooter issues a pod command which calls for a UUT read or write operation, the microprocessor sets the interval timer to a specific value. The value set on the interval timer corresponds to the time needed by the Processor Section to prepare for command execution prior to actually addressing the UUT.

When the interval timer reaches timeout, the timing circuits produce an output to disable RAM, ROM, and I/O, and to enable the buffers of the UUT Interface Section. This action causes the microprocessor to control the UUT Interface Section instead of the Processor Section. At the same time, the microprocessor, having completed preparation for command execution, places a UUT address on the address bus, and UUT data on the data bus (if the command being executed is a write).

At the end of the READ or WRITE cycle, the timing circuits terminate the addressing of the UUT, and the microprocessor returns to controlling the RAM, ROM, and I/O elements of the Processor Section. The timing circuits also operate the latches within the logic level detection circuits to store the state of the UUT bus during the UUT bus transaction.

When the RUN UUT mode is commanded, the Timing Section causes the microprocessor to change from controlling the Processor Section to controlling the UUT Interface Section, but does not return control back to the Processor Section. In addition, the RESET, HOLD, and READY inputs are enabled in the RUN UUT mode. The RUN UUT mode is terminated by a reset signal from the troubleshooter to the pod, which returns control back to the Processor Section.

4-6. UUT Power Sensing

Figure 4-1 also shows a power sensing circuit which constantly monitors the UUT power supplies. This circuit produces an output to the troubleshooter in the event UUT power drops below or rises above established limits. See Table 1-1.

4-7. DETAILED BLOCK DIAGRAM DESCRIPTION

The block diagram description that follows covers each of the three pod sections identified in the previous general description of pod operation. A detailed block diagram of the pod is presented in Figure 4-2.

4-8. Processor Section

Refer to Figure 4-2. The Processor Section of the pod is made up of the following components:

- Microprocessor, U12
- ROM, U3
- RAM (128 X 8), U2
- I/O ports A and B, U2
- Address decoder, U17
- Status line buffers, U13, U14

8080

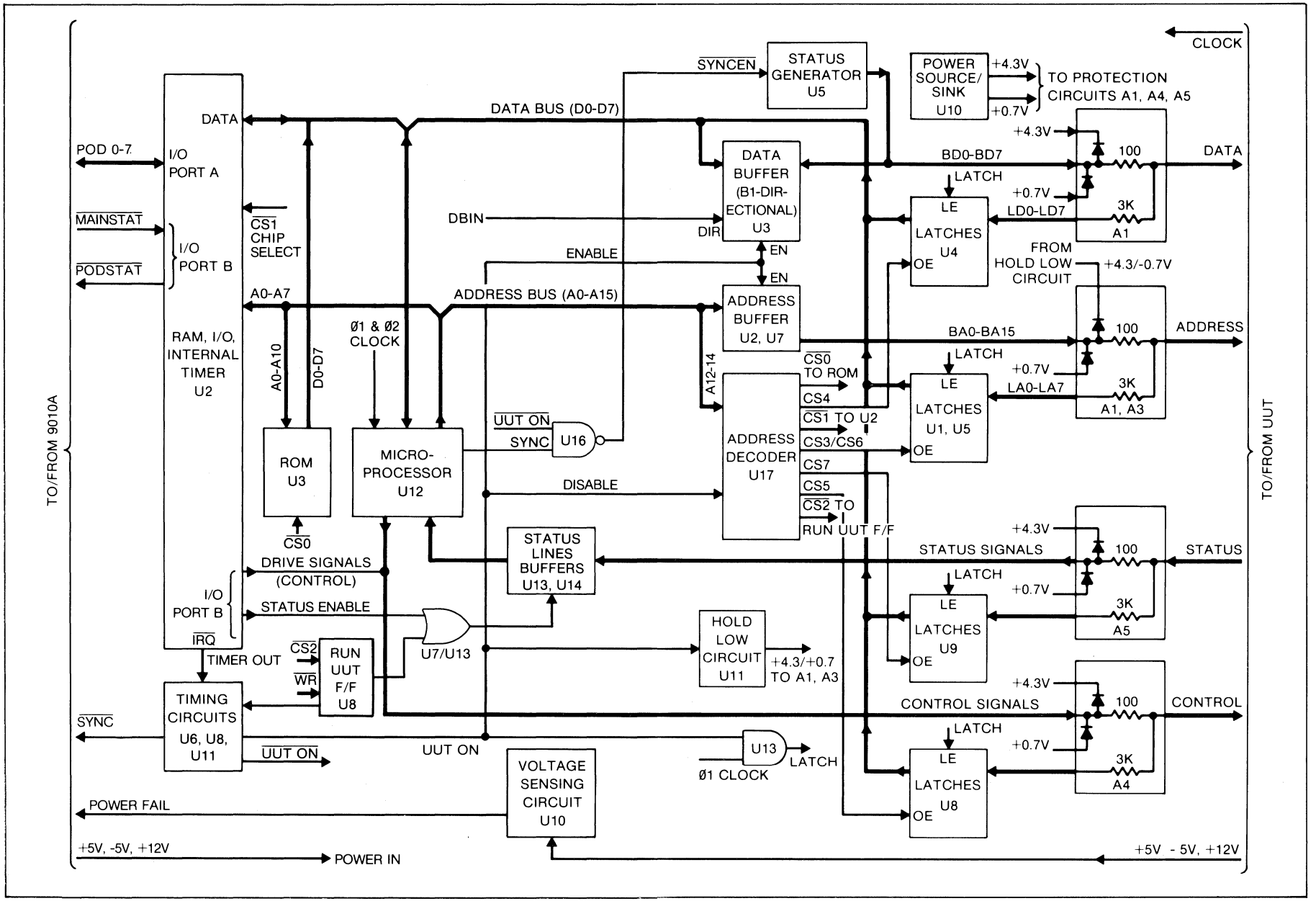

Figure 4-2. Detailed Block Diagram

The Processor section monitors the handshake line, $\overline{\text{MAINSTAT}}$, at I/O port B, waiting for troubleshooter commands. The microprocessor addresses I/O port B by means of address lines A0-A7 and address decoder, U17. The address decoder decodes address lines A12-A14 to produce the $\overline{\text{CS2}}$ signal which selects the RAM-I/O-Interval Timer U2.

The troubleshooter places a low on the $\overline{\text{MAINSTAT}}$ line when a command is placed on lines POD0-7. The microprocessor responds by addressing I/O port A of U2 and reading each byte of the troubleshooter command. As each byte is received, the handshaking lines operate as shown in the upper portion of Figure 4-3 to insure that no data is lost.

Each troubleshooter command causes the microprocessor to execute a corresponding routine contained in ROM U3. This routine, when executed, performs the troubleshooter command by first setting the interval timer (U2) and then performing all necessary internal operations in preparation for addressing the UUT. For example, if the troubleshooter command calls for a write to the UUT, the microprocessor must perform the steps necessary to assemble the UUT address, ready the data to be written, and perform housekeeping operations associated with the command. (As the Processor section performs reads and writes in preparation for addressing the UUT, it sends false reads to satisfy the requirements of certain UUTs.)

In addition, the routine directs the actual write and read functions of the UUT, transmits any response data back to the troubleshooter, and produces a status byte which reflects the current condition of the pod and UUT. During the transmission of data and status back to the troublshooter, the handshake lines operate as shown in the lower portion of Figure 4-3. The handshake insures that no data is lost during the transmission process.

The microprocessor has the capability of software-driving control lines INTE, WAIT and HLDA, as a means of verifying that they can be driven. Also, the microprocessor can control the enabling or disabling of status lines HOLD and READY, as a means of preventing stuck UUT status lines from interfering with pod operation. Both the drive signals for the control lines and the enable signals for the status lines are written by the microprocessor through I/O port B of U2.

4-9. UUT Interface Section - General

Refer to Figure 4-2. The UUT Interface Section includes the following components shown in Figure 4-2:

- Bidirectional data buffer, U3
- Status generator, U6

- Protection circuits, A1 - A5
- Address buffers, U2 and U7
- Sensing latches, U1, U4, U5, U8 and U9
- Hold low circuit, U11 and associated components, to hold address lines at 0000 when the UUT is not accessed.
- Power source/sink U10 for protection circuits

4-10. UUT Interface Section - Data Lines

The Data Buffer U3 is disabled by the timing circuits whenever the microprocessor is controlling the Processor Section. This disabling prevents data not meant for the UUT from reaching the UUT. Conversely, the data buffer is enabled by the timing circuits when the microprocessor is not controlling the Processor Section, such as, during a UUT read/write operation via data lines BD0-7. The direction of the data buffer is controlled by the DBIN line, a function of the microprocessor read cycle.

All data passing between the pod and the UUT is fed through a series of protection circuits; one circuit per line. Each protection circuit consists of a 100-ohm resistor in series with the line, and a pair of clippingdiodes. The diodes clip the data line at zero and +5 volts.

The data lines are also equipped with logic level detection circuits; one circuit per line. The detection circuits consist of a series of latch, coupled to the UUT side of the respective protection circuits. A series resistor at the input of each latch provides overvoltage protection.

The data lines are coupled to the inputs of latches U4 by lines LD0-7. The input to each latch is logic high if the line is driven high, and logic low if the line is driven low. The UUT ON signal from the Timing Section, in conjunction with the phase-two clock signal, latches the data line logic levels, at the time shown in Figure 4-4, to store the logic levels representing the state of each data line.

At the conclusion of a UUT write operation, latches U2 are addressed by the microprocessor. Address decoder U6 produces the 4000 (hex address) signal to place the contents of the latches on the data bus. The microprocessor compares the contents of the addressed latches with the intended write data. Any difference between the contents of the latches and the intended data is considered a data error.

As status generator U6 provides a status byte during the 8080 SYNC pulse when the UUT ON signal is not present. This manufactured status byte, gated by the $\overline{\text{SYNCEN}}$ signal, satisfies any status requirements of the UUT.

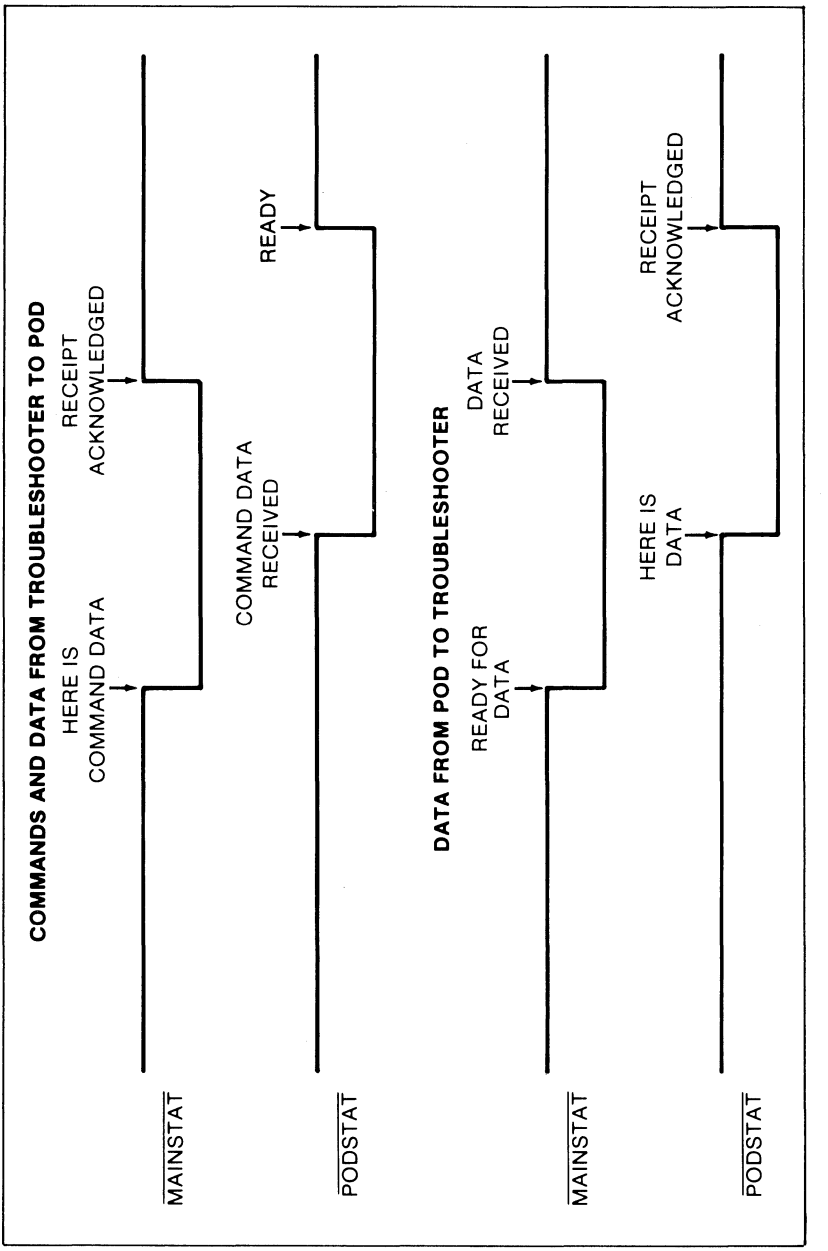

Figure 4-3. Handshaking Signals

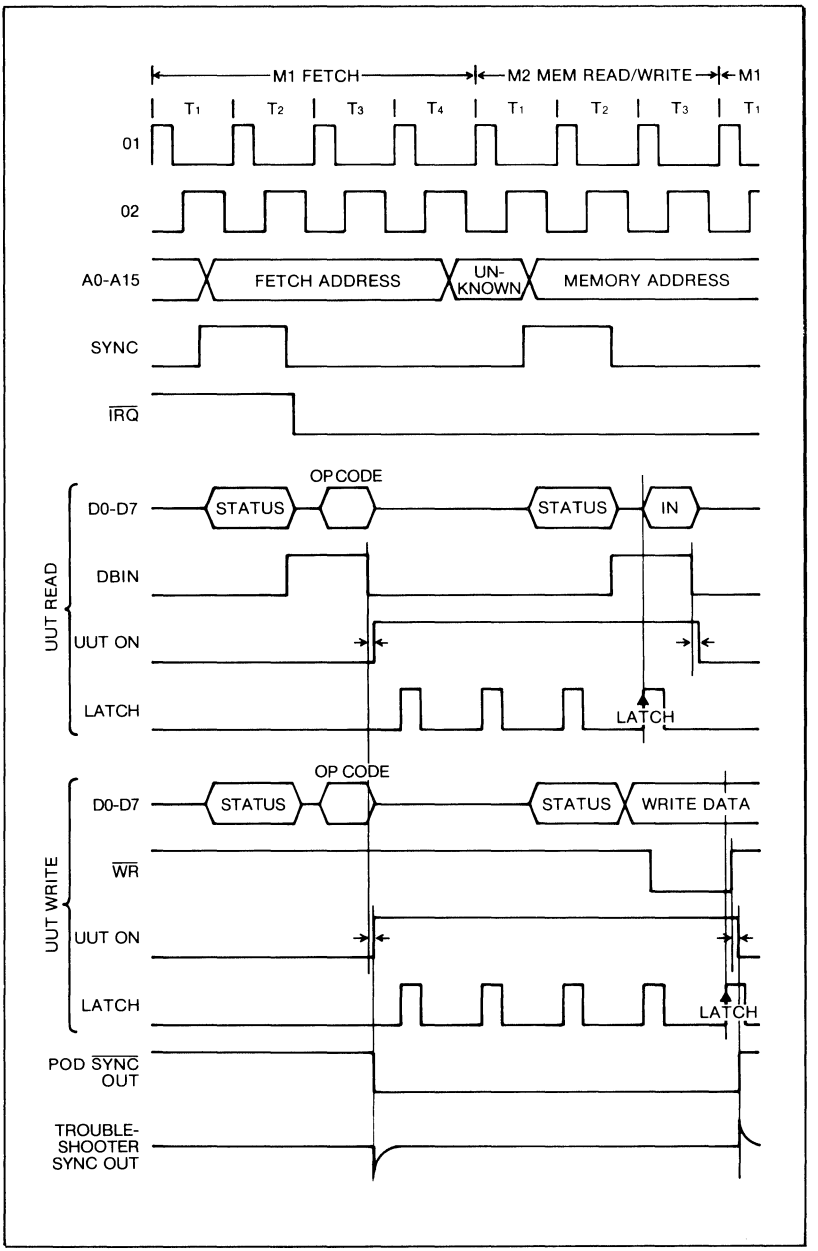

Figure 4-4. UUT ON Signal and Latch Times

4-11. UUT Interface Section - Address Lines

In a manner similar to that described for the data lines, all UUT addresses are fed through a series of protection circuits equipped with resistors and clipping diodes. The diodes using to protect the address lines perform the additional function of holding the address lines at zero volts any time the UUT Interface Section is not controlled by the microprocessor.

Address buffers U1 and U5 are enabled when the microprocessor is controlling the UUT Interface Section. Conversely, the address buffers are disabled to isolate the microprocessor from the UUT whenever the microprocessor is controlling the Processor Section. This isolation prevents the microprocessor from addressing the UUT when operating as part of the Processor Section. In addition, the address lines are held at zero volts by the diodes used in the protection circuits.

This holding action is provided by the hold low circuit, made up of U12 and associated components. This circuit drives the +4.3-volt diode clipping voltage down to -0.7 volts whenever the UUT is not being addressed, creating a UUT address of 0000. Maintaining the UUT at address 0000 prevents any inadvertent operation of the UUT and associated systems equipment.

As described for the data lines, the address lines are equipped with logic level detection circuits; one circuit per line. The detection circuits consist of a series of latches coupled to the UUT side of the respective protection circuits. A series resistor at the input of each latch provides overvoltage protection.

The address lines are coupled to the inputs of latches U4 and U6 by lines LA0-LA15. The input to each latch is logic high if the line is driven high, and logic low if the line is driven low. The UUT ON signal from the Timing Section, in conjunction with the phase-two clock signal, latches the address line logic levels. Figure 4-4, shows the time at which the loatches operate to store the logic levels representing the state of each data line.

At the conclusion of a UUT operation, latches U4 and U6 are separately addressed by the microprocessor. Address decoder U7 produces the 3000 and 6000 (addresses) signals to place the contents of the latches on the data bus, one byte at a time. The microprocessor compares the contents of the addressed latches with the acutal address. Any difference between the contents of the latches and actual address is considered on address error.

4-12. UUT Interface Section - Status and Control Lines

In addition, when the microprocessor controls the Processor section instead of the UUT Interface section (UUT ON signal not present), and performs write operations, gate U11-1 (shown in the schematic diagram of Section 7) allows the

$\overline{WR}$ signals to generate false DBIN signals to the UUT. The false DBIN signals match up with the false status produced by the status generator so that the UUT "sees" only reads at the reset address (0000) whenever the microprocessor controls the Processor section. In this mode, gate U11-1 prevents the $\overline{WR}$ signal from reaching the UUT.

The status and control lines are provided with protection circuits, logic level detection circuits and latches. These circuits operate in a manner similar to those provided with the data and address lines, and described in the previous paragraphs.

4-13. Timing Section

The timing section consists of the interval timer contained in U2, and a series of timing circuits made up of U6, U8, and U11. As mentioned in the description of the Processor Section, the microprocessor executes the troubleshooter command by first setting the interval timer and then performing all necessary internal operations in preparation for addressing the UUT. The interval timer is set to a time equal to the amount of time required by the microprocessor to perform all necessary internal operations.

At the time the interval timer is set, and until the timer times out, a high $\overline{IRQ}$ output from U2 holds the timing circuits in their reset state. When the timer times out, the $\overline{IRQ}$ output goes low to enable the timing circuits and produce the UUT ON signal. The UUT ON signal enables the data and address buffers, disables the address decoder, and disables the hold low circuit. Refer to Figure 4-4 for the timing of the UUT ON signal.

With the data and address buffers enabled, and the hold low circuit disabled, data and addresses placed on the buses by the microprocessor are directed to the UUT. The Processor Section is disabled at this point by theaddress decoder U6 which receives the UUT ON signal generated by the timing circuits. With address decoder disabled, the ROM and RAM-I/O-Interval Timer are not selected.

At the end of the instruction cycle (except in the RUN UUT mode), the timing circuits return to their reset state to disable the data and address buffers, and enable address decoder, U6. This action switches the microprocessor back to control the Processor Section instead of the UUT Interface Section.

At the time of the phase-one clock pulse, after the beginning of the UUT on signal, U13 produces the LATCH signal to latch the UUT line logic levels. The latches store the condition of all UUT lines. (Several LATCH pulses may be produced during each UUT on signal. The data read from the latches is that stored by the last LATCH pulse.) When addressed by the microprocessor, via

address decoder U6, each latch places the condition of the associated UUT line on the data bus. The microprocessor compares the detected UUT line levels with the known expected result and considers any difference to be an error. Any error conditions are indicated in the status byte sent to the troubleshooter at the conclusion of each command.

When the RUN UUT mode is commanded, the microprocessor performs a write to set the Run UUT flip-flop U8 . The Run UUT flip-flop causes the timing circuits to produce the UUT ON signal as previously described for the non-RUN UUT mode. However, the Run UUT flip-flop causes the timing circuits to be held in a state which maintains the UUT ON signal and dedicates the microprocessor to the UUT. In this mode, the RESET, HOLD and READY inputs are enabled, allowing the UUT to utilize the pod microprocessor in place of the microprocessor removed to facilitate pod connection.

The RUN UUT mode continues until a $\overline{\text{RESET}}$ signal is received from the troubleshooter. The $\overline{\text{RESET}}$ signal causes the microprocessor to resume control of the Processor Section.

Section 5
Maintenance

5-1. INTRODUCTION

This section provides maintenance information for the pod, and includes self test information, repair precautions, disassembly procedures, and troubleshooting information.

5-2. SELF TEST

The troubleshooter can perform a self test on any pod which is operational enough to communicate with the troubleshooter. Self test provides fault location to several areas of the pod by creating appropriate display messages on the troubleshooter. In order to perform self test, the Processor Section (8080 RAM, ROM, I/O, and buses) must be operational. Operation of the processor section is necessary in order for the pod to accept and execute self test commands issued by the troubleshooter.

NOTE

Self test does not examine the pod for all conceivable faults, and may indicate an okay pod when not completely operable. An alternative method of checking pod operability is exercising with a known-good UUT and troubleshooter, observing any reported "UUT failures".

Performance of self test requires that the ribbon cable connector be inserted into the self test socket located on the pod. When the ribbon cable plug is inserted into the self test socket, the following electrical connections are made to facilitate testing (refer also to the schematic diagram contained in Section 7):

- The high order address lines are connected back to the data lines through series resistors. This connection allows the high order address bits to become data during a test read operation.

- A clock signal is applied to the clock inputs of the pod. This clock signal replaces the clock normally supplied by the UUT to operate the pod.

- All forcing lines and interrupts are set to the active state. Setting these lines allows testing of the individual hardware or software buffering.

- +5V, -5V, and +12V dc is applied to simulate UUT power and check the power fail sensing circuit.

- Ground is applied through the ribbon cable to pin 2 to notify the troubleshooter that the pod is in the self test configuration.

To perform self test, proceed as follows:

1. If not already connected, connect the interface pod to the troubleshooter as shown in Figure 2-1. Secure the connector using the sliding collar.

2. Open the pins of the self test socket by operating the adjacent thumbwheel. Insert the ribbon cable plug into the socket and close the socket using the thumbwheel.

3. Turn the troubleshooter on and press BUS TEST to initiate self test.

4. If the troubleshooter and pod are operating normally, the troubleshooter display reads *POD SELF-TEST 8080 OK.*

5. If the pod is defective, but not completely dead, the troubleshooter displays *POD SELF-TEST 8080 FAIL xx,* where xx represents the pod fault listed in Table 5-1. Refer to the troubleshooting procedures to further isolate the problem.

6. If the pod is inoperative, the troubleshooter reads *POD TIMEOUT-ATTEMPTING RESET.* This message indicates that the pod is not responding to commands issued by the troubleshooter. Refer to the troubleshooting procedures to isolate the problem.

5-3. REPAIR PRECAUTIONS

CAUTION

Static discharge can damage MOS components contained in the pod. To prevent this possibility, take the following precautions when troubleshooting and/or repairing the unit.

Table 5-1. Self Test Failure Codes

CODE	POSSIBLE FAULT
00	1. UUT power sensing circuit failure 2. Control lines(s) cannot be driven 3. Address lines(s) cannot be driven 4. Wrong data read
01	1. UUT power sensing circuit failure 2. Control line(s) cannot be driven 3. Address line(s) cannot be driven 4. Data line(s) cannot be driven
02	One or more control lines not driveable
03	Forcing or interrupt line buffer(s) or associated logic faulty

- Never remove, install, or otherwise connect or disconnect PCB (printed circuit board) assemblies without disconnecting the pod from the troubleshooter.
- Perform all repairs at a static-free work station.
- Do not handle ICs or PCB assemblies by their connectors.
- Attach static ground straps to repair personnel.
- Use conductive foam to store replacement or removed ICs.
- Remove all plastic, vinyl and styrofoam from the work area.
- Use a grounded soldering iron.

The soldering iron used in pod repair should have a rating of 25 watts or less to prevent overheating the PCB assembly.

5-4. TROUBLESHOOTING

5-5. Introduction

Pod failure is usually identifiable from the troubleshooter display. Two types of messages which indicate pod failure are:

- *POD TIMEOUT -ATTEMPTING RESET;* when this message is displayed, the pod does not respond to troubleshooter commands or reset

pulses. This message may be due to stuck forcing lines not disabled during troubleshooter setup procedures described in the Operator Manual.

- Any recurring UUT test-failure or error message when testing a known-good UUT indicates pod failure. Since the UUT is known to be good, errors attributed to the UUT by the troubleshooter are actually pod errors.

Troubleshooting the pod is similiar to troubleshooting any other microprocessor-based UUT, and requires the equipment listed in Table 5-2. The troubleshooting information presented in the following paragraphs does not provide step-by-step fault isolation procedures, but provides a troubleshooting guide for use while employing normal fault isolation techniques.

Figure 5-1 shows the non-component side of the interface PCB with component outlines and identification superimposed. Refer to this figure to locate various electrical points on the interface PCB during troubleshooting procedures.

The troubleshooting information should be used in conjunction with the schematic diagrams contained in Section 7 and the Theory of Operation presented in Section 4.

The troubleshooting guidelines presented in the following paragraphs are intended to assist in the isolation of faults within the pod. If attempted troubleshooting fails to reveal the pod fault, return of the pod to the nearest Fluke Service Center is recommended. Refer to the troubleshooter Service Manual for a list of Fluke Service Centers.

Table 5-2. Required Test Equipment

EQUIPMENT TYPE	REQUIRED TYPE
Micro System Troubleshooter	Fluke 9000 Series
Interface Pod	Fluke 9000A-8080
Digital Multimeter	Fluke 8020
Oscilloscope	Tektronix 485 or equivalent

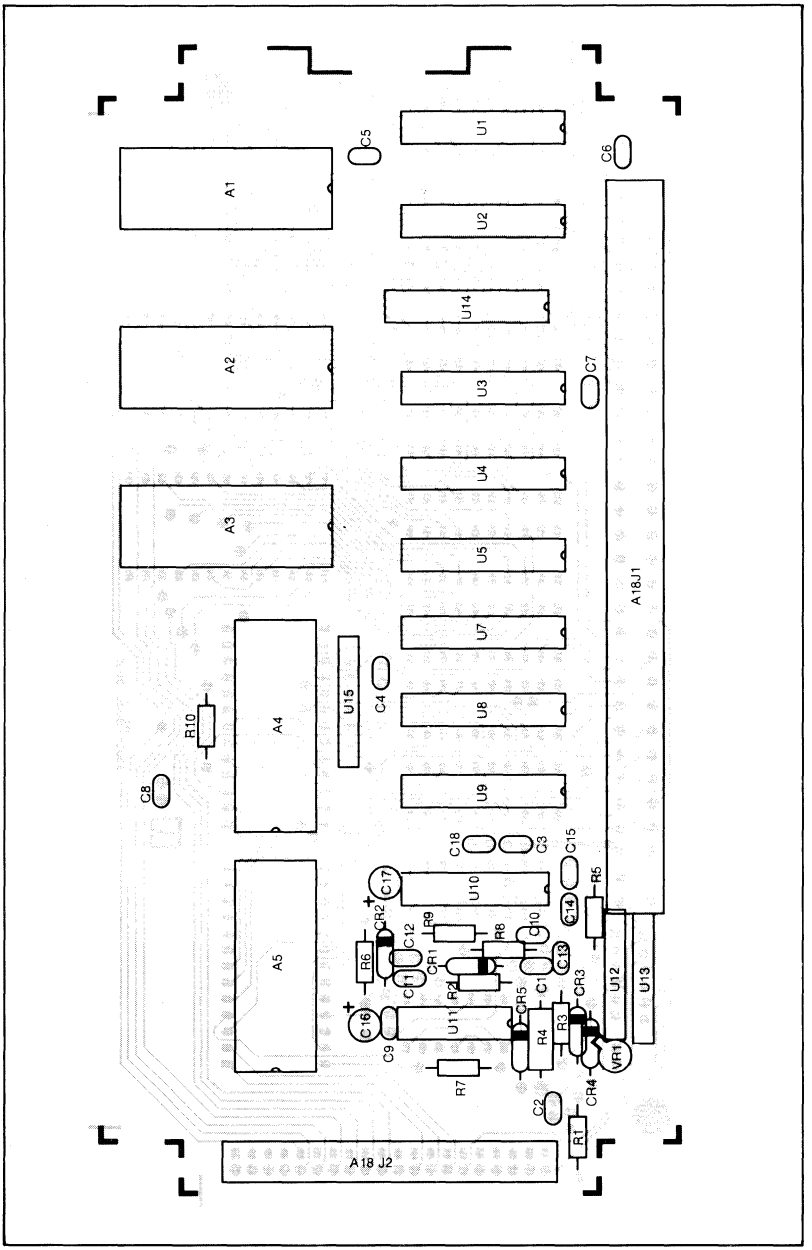

Figure 5-1. Interface Pod, Non-Component Side

5-6. Pod Defective or Inoperative?

Before attempting to repair a faulty pod, the level of failure should be determined. A faulty pod can be categorized as either defective or inoperative, depending upon the result of the self test.

If the result of a self test produces a troubleshooter display of *POD SELF-TEST 8080 FAIL xx,* the pod is considered to be defective but not inoperative. Troubleshoot a defective pod as described under the heading Troubleshooting a Defective Pod. Select a suitable UUT as described under the heading Selecting a UUT for Pod Testing.

NOTE

It is possible for a pod to produce a self test message of POD SELF-TEST 8080 OK and still be faulty. Such a pod causes the display of test-failure or error messages on the troubleshooter when used to test a known-good UUT. In this case, errors attributed to the UUT are actually pod errors.

If the result of a self test, or any other troubleshooter operation, produces a troubleshooter display of *POD TIMEOUT -ATTEMPTING RESET,* the pod is considered to be inoperative. Troubleshoot an inoperative pod as described under the heading Troubleshooting and Inoperative Pod. Select a suitable UUT as described under the heading Selecting a UUT for Pod Testing.

NOTE

The POD TIMEOUT -ATTEMPTING RESET message can also result from stuck UUT forcing lines which can disable the pod. Forcing lines should be disabled during troubleshooter setup procedures as described in the Operator Manual.

5-7. Selecting a UUT for Pod Testing

In order to troubleshoot a pod, a known-good UUT must be connected to the pod via the ribbon cable and connector. The UUT may be any device which normally employs a 8080 microprocessor and to which power can easily be applied. The UUT is needed to provide the following functions during pod testing:

- RAM and ROM for performing read/write operations
- 8080 compatible clock signal to drive the pod
- +5V, -5V, and +12V dc UUT power to check the UUT power sensing circuit

Instead of connection to a known-good UUT, the ribbon cable connector may be connected to the self test socket on the pod. The self test socket provides a 8080 compatible clock signals, +5V, -5V, and +12V dc, and also simulates ROM by connecting the high order address lines back to the data lines (refer to the schematic diagram for details).

However, insertion of the ribbon cable connector directly into the self test socket places pin 2 at ground. The pod senses the ground at pin 2 and notifies the troubleshooter of the self test connection. As a result, the troubleshooter inhibits normal operation and allows performance of only self test.

During pod troubleshooting procedures, normal troubleshooter operation must be allowed. Consequently, the pod must be prevented from sensing the ribbon cable connector in the self test socket. To prevent the pod from sensing the self test connection, pin 2 of the connector must be effectively removed.

To effectively remove pin 2 of the connector, obtain one of the two replacement ribbon cable connectors supplied with the pod, and modify as follows:

1. Carefully separate the connector body halves using a small screwdriver.

2. Remove pin 2 from the connector and reassemble the body.

3. Insert the modified replacement connector into the self test socket.

4. Insert the ribbon cable connector into the modified replacement connector.

In addition to modifying the ribbon cable connector, be sure to disable all forcing line and interrupt inputs, and set all forcing line and interrupt traps to NO during Setup Editing as described in the Operator Manual. Disabling these inputs and messages is necessary when utilizing the self test socket since all lines are wired to the active state.

5-8. Troubleshooting a Defective Pod

NOTE

The following paragraphs reference three distinct areas of the pod identified as the Processor Section, the UUT Interface Section, and the Timing Circuits. The components which make up these sections are identified in the Theory of Operation, presented in Section 4.

A pod is considered defective when the performance of self test produces a troubleshooter display of *POD SELF-TEST 8080 FAIL xx,* where xx

represents the pod fault listed in Table 5-1. The fact that a self test can be performed indicates operation of the Processor Section, since operation of the Processor Section is necessary for troubleshooter/pod communication. With the Processor Section proven to be good, the UUT Interface Section or the Timing Circuits contain the fault.

Prepare to troubleshoot the defective pod as follows:

1. Disassemble the pod by removing the PCB assemblies from the case, and the shield from the PCB assemblies. (Refer to disassembly information under the heading Disassembly.) It is not necessary to separate the PCB assemblies at this point.

2. Connect the pod to the troubleshooter, and the ribbon cable connector to the UUT, as shown in Figure 5-2. Note that the troubleshooter is connected by means of the shielded cable, and not by means of a second pod, to the microprocessor socket. Also, Figure 5-2 shows the self test socket as the UUT, although any suitable UUT may be used. (Refer to Selecting a UUT for Pod Testing.)

NOTE

All references to data and addresses in the following troubleshooting guide are in hexadecimal notation. Unless otherwise noted, all troubleshooter probe operations are performed in the synchronized mode.

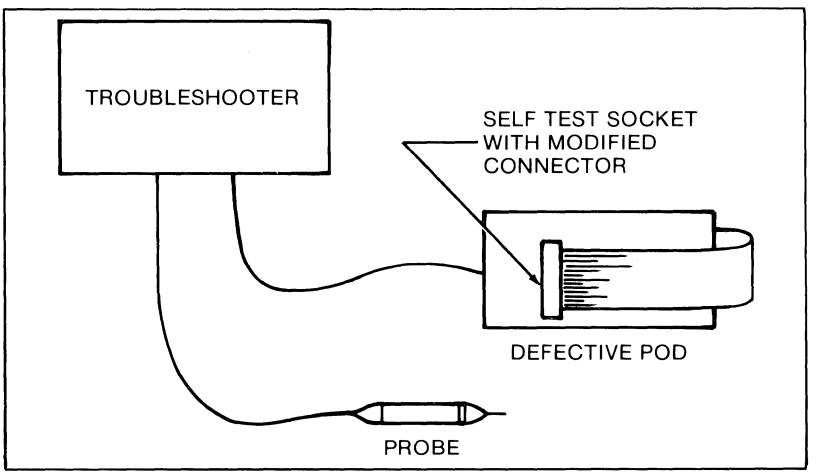

Figure 5-2. Troubleshooting a Defective Pod

NOTE

When troubleshooting a pod, perform looping tests of the most simple type (such as reads and writes as opposed to ROM and RAM tests) that show a fault symptom. A synchronized probe can then be used to trace a fault once such a looping test has it isolated.

5-9. SELF TEST CODE 00

If self test produces a troubleshooter display of *POD SELF-TEST Z80 FAIL 00,* a UUT read operation has failed and one or more of the following problems is indicated:

- UUT power sensing circuit failure
- Control line(s) cannot be driven
- Address line(s) cannot be driven
- Wrong data read

To further isolate the trouble, prodeed as follows:

1. Check operation of the UUT power sensing circuit by verifying +5, -5 and +12 volt UUT supplies at the ribbon cable connector and zero volts on the Power Fail line. Check the Power Fail line at the PCB-to-PCB connector, and if necessary, at the shielded cable connector.

2. Perform a read operation. Use address 0FF0 if using the self test socket as the UUT. (The self test socket sends the upper address byte to the data lines. During self test, read operations at 0FF0 and F00F take place.) Use any address containing known data if using some other UUT.

   a. If the troubleshooter indicates a control line error, examine the entire troubleshooter display to determine the stuck control line(s). While looping on the error, use the probe or a scope to locate the point of control line failure.

   b. If the troubleshooter indicates an address line error, note the failed address line(s) indicated on the troubleshooter display. While looping on the error, use the probe or a scope to locate the point of address line failure.

   c. If the data read, indicated on the troubleshooter display, is not 0F when using the self test socket, or is not identical to the known data of the UUT used for this test, a data line or address line failure is

indicated. Determine the failed line(s) from the display and locate the point of failure using the synchronized probe or a scope while performing a looping read operation.

3. Repeat steps 2b and 2c at different addresses and for different data in order to toggle each of the address and data lines.

4. Check for operation of the interval timer and timing circuits by observing pin 25 ($\overline{IRQ}$) of U2 for a low-going output each time a read operation is executed. If the $\overline{IRQ}$ signal is present, check for a $\overline{SYNC}$ signal at pin 10 of the shielded cable connector, and for a UUT ON signal at the PCB-to-PCB connector. The absence of these signals allows the pod to communicate with the troubleshooter, but prevents the latches from detecting addresses, data, and control signals sent to the UUT (or self test socket). Failure of these signals may also prevent data read from the UUT from reaching the pod microprocessor.

5-10. SELF TEST CODE 01

If self test produces a troubleshooter display of *POD SELF-TEST Z80 FAIL 01,* one or more of the following failures is indicated:

- UUT power sensing circuit failure
- Control line(s) cannot be driven
- Address line(s) cannot be driven
- Data line(s) cannot be driven

To further isolate the trouble, proceed as follows:

1. Check operation of the UUT power sensing circuit by verifying +5, -5 and +12 volt UUT supplies at the ribbon cable connector and zero volts on the Power Fail line. Check the Power Fail line at the PCB-to-PCB connector, and if necessary, at the shielded cable connector.

2. Perform a write operation; use 0FF0 for the address and 0F for the data.

a. If the troubleshooter indicates a control line error, examine the entire troubleshooter display to determine the stuck control line(s). While looping on the error, use the probe or a scope to locate the point of control line failure.

b. If the troubleshooter indicates an address line error, note the failed address line(s) indicated on the troubleshooter display. While

looping on the error, use the probe or a scope to locate the point of address line failure.

c. If the troubleshooter indicates a data line error, note the failed line(s) indicated on the troubleshooter display. While looping on the error, use the probe or a scope to locate the point of failure.

3. Repeat steps 2b and 2c using F00F for the address and F0 for the data to check address and data lines in the opposite state.

4. Check for operation of the interval timer and timing circuits by observing pin 25 ($\overline{IRQ}$) of U2 for a low-going output each time a write operation is executed. If the $\overline{IRQ}$ signal is present, check for a $\overline{SYNC}$ signal at pin 10 of the shielded cable connector, and for a UUT ON signal at the PCB-to-PCB connector. The absence of these signals allows the pod to communicate with the troubleshooter, but prevents the latches from detecting addresses, data, and control signals sent to the UUT (or self test socket). Failure of these signals may also prevent write data from reaching the UUT.

5-11. SELF TEST CODE 02

If self test produces a troubleshooter display of *POD SELF-TEST 8080 FAIL 02,* failure of one or more of the control lines is indicated. To check each of the control lines, use the troubleshooter to perform a BUS TEST. Refer to the heading Bit Assignment - Control Lines, located in Section 3, for interpretation of the troubleshooter message.

5-12. SELF TEST CODE 03

If self test produces a troubleshooter display of *POD SELF-TEST 8080 FAIL 03,* failure of one or more status line buffers is indicated. Each of the status (forcing) lines, which have the ability to interrupt or otherwise interfere with microprocessor operation, are selectively buffered from the microprocessor.

Buffering of the RESET, HOLD, and READY lines is accomplished by means of gates which are enabled or inhibited by port B outputs of the RAM-I/O-Interval Timer.

5-13. Troubleshooting an Inoperative Pod

NOTE

The following paragraphs reference three distinct areas of the pod identified as the Processor Section, the UUT Interface Section, and the Timing Circuits. the components which make up these sections are identified in the Theory of Operation, presented in Section 4.

A pod is considered inoperative when the performance of self test, or any other troubleshooter operation, produces a troubleshooter message of *POD TIMEOUT -ATTEMPTING RESET.* This troubleshooter message results from a lack of response by the pod to troubleshooter commands. Since it is the function of the Processor Section to respond to troubleshooter commands, lack of response indicates failure of the Processor Section.

Prepare to troubleshoot the inoperative pod as follows:

1. Disassemble the pod by removing the PCB assemblies from the case, and the shield from the PCB assemblies. Refer to Disassembly. It is not necessary to separate the PCB assemblies at this point.

2. Remove the microprocessor from its socket.

3. Connect the pod under test to +5, -5, and +12 volt power supplies. Apply power to the connector normally coupled to the troubleshooter; use pins 2 and 15 for +5 volts, pin 14 for +12 volts, pin 21 for -5 volts, and pin 25 for ground. If available, use a second troubleshooter and shielded cable to provide power to the pod.

4. Connect a 9000 Series Troubleshooter to a second pod. Apply power to the troubleshooter, then connect the second pod ribbon cable to the microprocessor socket of the pod under test.

CAUTION

Do not apply or remove any power with ribbon cable connected between second pod and inoperative pod.

NOTE

All references to data and addresses in the following troubleshooting guide are in hexadecimal notation.

With reference to the Theory of Operation contained in Section 4 and the schematic diagram contained in Section 7, troubleshoot an inoperative pod using the following steps as a guide:

1. Reset the pod by momentarily shorting pins 22 and 23 of the shielded cable connector located on the upper PCB assembly.

2. Perform a BUS TEST.

3. Perform a RAM SHORT and RAM LONG TEST. The RAM addresses are listed in Table 5-3.

4. Perform a ROM TEST. The ROM addresses are listed in Table 5-3.

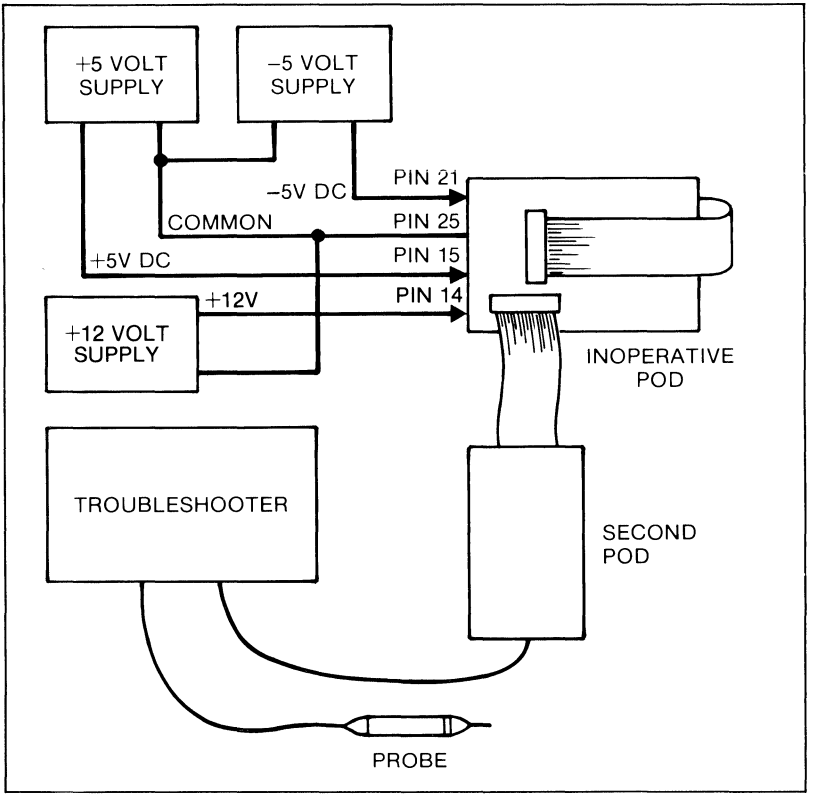

Figure 5-3. Troubleshooting an Inoperative Pod

Table 5-3. 8080 Pod Memory and I/O Addresses

ADDRESSABLE DEVICE	ADDRESS (HEX)
RAM	1000 - 107F
ROM	0000 - 07FF
I/O-Port A Direction Register	1081
Port A Data Register	1080
Port B Direction Register	1083
Port B Data Register	1082
Interval Timer - Divide by 1	109C
Interval Timer Disable	1094

5. Check the output operation of I/O port A (contained in U2) as follows:

a. Perform a write operation to the port A direction register to set all lines of I/O port A (PA0-PA7) as outputs. The write address is 1081; write data is FF.

b. Perform a write operation to the port A data register to set all bits high. The write address is 1080; write data is FF.

c. Check the port A lines (PA0-PA7) with the probe or scope for all logic high levels.

d. Repeat step b with 00 as the write data.

e. Repeat step c, checking for all logic low levels.

6. Check the input operation of I/O port A (contained in U2) as follows:

a. Perform a write operation to the port A direction register to set all lines of I/O port A (PA0-PA7) as inputs. The write address is 1081; write data is 00.

b. Perform a read operation at the port A data register, address 1080, while sequentially applying the probe (with high pulses selected) to each of the port A input pins (pins 8-15 of U2) and observing the troubleshooter display. The troubleshooter should indicate each high input of port A.

7. Check the output operation of port B (PB0-PB70) by repeating step 5 and using address 1083 for the port B direction register, and address 1082 for the port B data register.

8. Check the input operation of port B, line PB7 ($\overline{\text{MAINTSTAT}}$) by repeating step 6. Use address 1083 for the port B direction register and write data 00 to set line PB7 as an input. Perform the looping read at address 1082 and apply +5 volts to U2, pin 16.

9. Check operation of the interval timer (contained in U2) by performing a write operation at address 109C; write data = 0F. Verify that the $\overline{\text{IRQ}}$ output of U2 goes low in response to the write operation.

10. Check for the occurence of the UUT ON signal (produced by the timing circuits as a result of the low $\overline{\text{IRQ}}$ signal) at the PCB-to-PCB connector.

11. Check for the occurence of the $\overline{\text{SYNC}}$ signal at pin 10 of the shielded cable connector.

12. Check the address decoder by performing read operations at addresses 0000, 1000, 2000, 3000, 4000, 5000, 6000, and 7000. Verify that the respective decoder output goes low when addressed.

13. If repairs have been made to the inoperative pod as a result of the preceeding checks, attempt self test. If self test operates, but the pod fails, refer to Troubleshooting a Defective Pod.

The troubleshooting guidelines presented in the preceeding paragraphs are intended to assist in the isolation of faults within the pod. If attempted troubleshooting fails to reveal the pod fault, return of the pod to the nearest Fluke Service Center is recommended. Refer to the troubleshooter Service Manual for a list of Fluke Service Centers.

5-14. DISASSEMBLY

To gain access to the two PCB assemblies within the pod, proceed as follows:

1. Remove the ribbon cable plug from the self test socket.

2. Remove the four phillips screws holding the pod case halves together and carefully open the case.

3. With the PCB assemblies removed from the case halves, remove the screw which retains the shield. Remove the shield.

NOTE

To troubleshoot the pod, it may not be necessary to separate the two PCB assemblies except to replace components. Figure 5-1 shows the location of each component on the lower PCB assembly relative to the accessible non-component side of the board.

4. If it is not necessary to separate the two PCBassemblies, temporarily replace the shield retaining screw; otherwise, remove the second screw from its standoff and carefully pull the boards apart at the connector.

5. To operate the pod with the two printed circuit boards separated from each other, reconnect them in a side-by-side fashion using the test adapter, Fluke part no. 613828. Make sure that correct pin-to-pin relationships are maintained.

Section 6
List of Replaceable Parts

6-1. INTRODUCTION

This section contains an illustrated parts breakdown of the instrument. Components are listed alphanumerically by assembly.

Parts lists include the following information:

1. Reference Designation.

2. Description of Each Part.

3. FLUKE Stock Number.

4. Federal Supply Code for Manufacturers. (See the 9000 Series Troubleshooter Service Manual for Code-to-Name list).

5. Manufacturer's Part Number.

6. Total Quantity of Components Per Assembly.

7. Recommended quantity: This entry indicates the recommended number of spare parts necessary to support one to five instruments for a period of 2 years. This list presumes an availability of common electronic parts at the maintenance site. For maintenance for 1 year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked.

6-2. HOW TO OBTAIN PARTS

Components may be ordered directly from the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. or an authorized representative by using the FLUKE STOCK NUMBER.

In the event the part ordered has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

To ensure prompt and efficient handling of your order, include the following information.

1. Quantity.
2. FLUKE Stock Number.
3. Description.
4. Reference Designation.
5. Printed Circuit Board Part Number and Revision Letter.
6. Instrument Model and Serial Number.

A Recommended Spare Parts Kit for your basic instrument is available from the factory. This kit contains those items listed in the REC QTY column for the parts lists in the quantities recommended.

Parts price information is available from the John Fluke Mfg. Co., Inc. or its representative. Prices are also available in a Fluke Replacement Parts Catalog, which is available upon request.

CAUTION

Indicated devices are subject to damage by static discharge.

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
	9000A-8080 INTERFACE POD FINAL ASSY. FIGURE 6-1 (9000A-8080-5071)	ORDER	BY	MODEL # 9000A-8080			
A17	Ⓧ PROCESSOR PCB ASSEMBLY	581173	89536	581173	1		
A18	Ⓧ INTERFACE PCB ASSEMBLY	581181	89536	581181	1		
H1	SCREW, PHP, 4-40 X 1/4	185918	89536	185918	2		
H2	SCREW, PHP, 4-40 X 1/2	152132	89536	152132	4		
MP1	DECAL, 8080 POD	584243	89536	584243	1		
MP2	DECAL, 8080 SPEC	536409	89536	536409	1		
MP3	CASE, (BOTTOM)	579573	89536	579573	1		
MP4	KNOB, ACCUATOR	582916	89536	582916	1		
MP5	CASE, (TOP)	579565	89536	579565	1		
MP6	SHIELD	586479	89536	586479	1		
W1	CABLE ASSEMBLY, POD	581827	89536	581827	1		
W2	CABLE, UUT	604769	89536	604769	1		

Table 6-1. 9000A-8080 Interface Pod Final Assembly

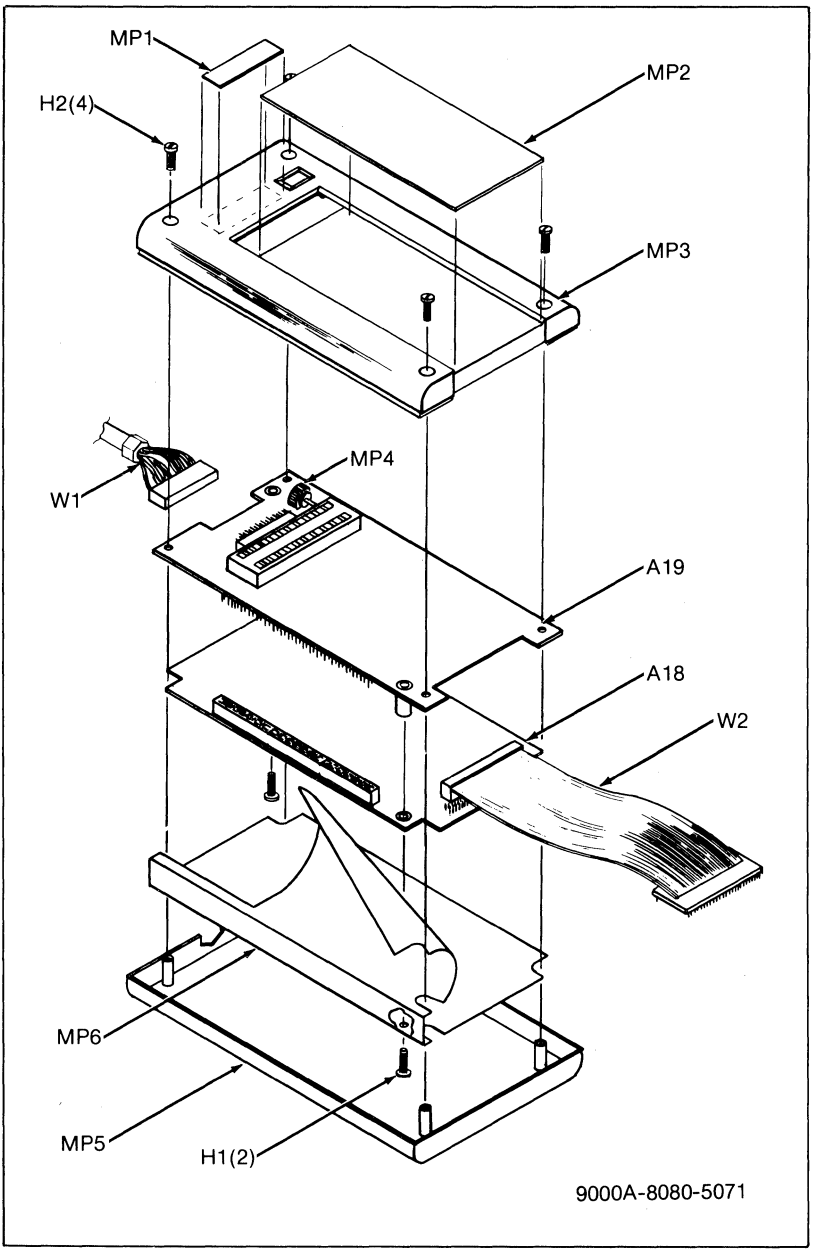

Figure 6-1. 9000A-8080 Interface Pod Final Assembly

Table 6-2. A17 Processor PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
A17	⊗9000A-8080 PROCESSOR PCB ASSEMBLY FIGURE 6-2 (9000A-8080-4071T)	581173	89536	581173	REF		
C1	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	8		
C2	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C3	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C4	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C5	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C6	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C7	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C8	CAP, CER, 0.22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
J3	CONN, 40-PIN	585133	89536	585133	1		
J4	POST CONTACT HEADER, 26-POS	512590	89536	512590	1		
MP1	SPACER, STANDOFF (NOT SHOWN)	602284	89536	602284	2		
P1	CONNECTOR, PIN	513879	00779	4-870221	60		
R1	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	2		
R2	RES, DEP. CAR, 620 +/-5%, 1/4W	442319	80031	CR251-4-5P620E	1		
R3	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R4	RES, DEP. CAR, 51 +/-5%, 1/4W	414540	80031	CR251-4-5P51E	1		
U1	RESISTOR NETWORK, 2K	574905	89536	574905	1	1	
U2	⊗IC, RAM, I/O, TIMER ARRAY	536417	55576	SYP6532A	1	1	
U3	⊗IC, MOS, N-CHANNEL 16K BIT	586164	89536	586164	1	1	
U4	RESISTOR NETWORK, 4.7K	494690	01295	494690	1	1	
U5	IC, OCTAL BUFFERS AND LINE DRIVERS	478347	01295	SN74LS241N	1	1	
U6	IC, TTL, QUAD, 2-INPUT, POS NAND GATE	393033	01295	SN74LS00N	3	1	

Table 6-2. A17 Processor PCB Assembly (cont)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
U7	IC, TTL, QUAD, 2-INPUT, POS NAND GATE	393033	01295	SN74LS00N	REF		
U8	IC, TTL, DUAL J-K FLIP/FLOP	414029	01295	SN74LS112N	1	1	
U10	IC, TTL, LO-PWR, DUAL J-K, F/F	412999	01295	SN74LA109N	1	1	
U11	IC, TTL, QUAD, 2-INPUT NOR GATE	393041	01295	SN74LS02N	1	1	
U12	Ⓧ IC, MOS, 8-BIT N-CHANNEL SILICON GATE	585596	34649	P8080A-1	1	1	
U13	IC, TTL, QUAD, 2-INPUT POS AND GATE	393066	01295	SN74LS08N	1	1	
U14	IC, TTL, QUAD, 2-INPUT POS OR GATE	393108	01295	SN74LS32N	1	1	
U15	Ⓧ IC, TTL, 8080 CLOCK GENERATOR	586230	34649	P8224	1	1	
U16	IC, TTL, QUAD, 2-INPUT, POS NAND GATE	393033	01295	SN74LS00N	REF		
U17	Ⓧ IC, TTL, LO-PWR, 3-8 LINE DECODER	407585	01295	SN74LS138N	1	1	
XU2	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	2		
XU3	SOCKET, IC, 24-PIN	376236	91506	324-AG39D	1		
XU12	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	REF		
Y1	CRYSTAL, QUARTZ, 3.2 MHZ	500348	89536	500348	1	1	

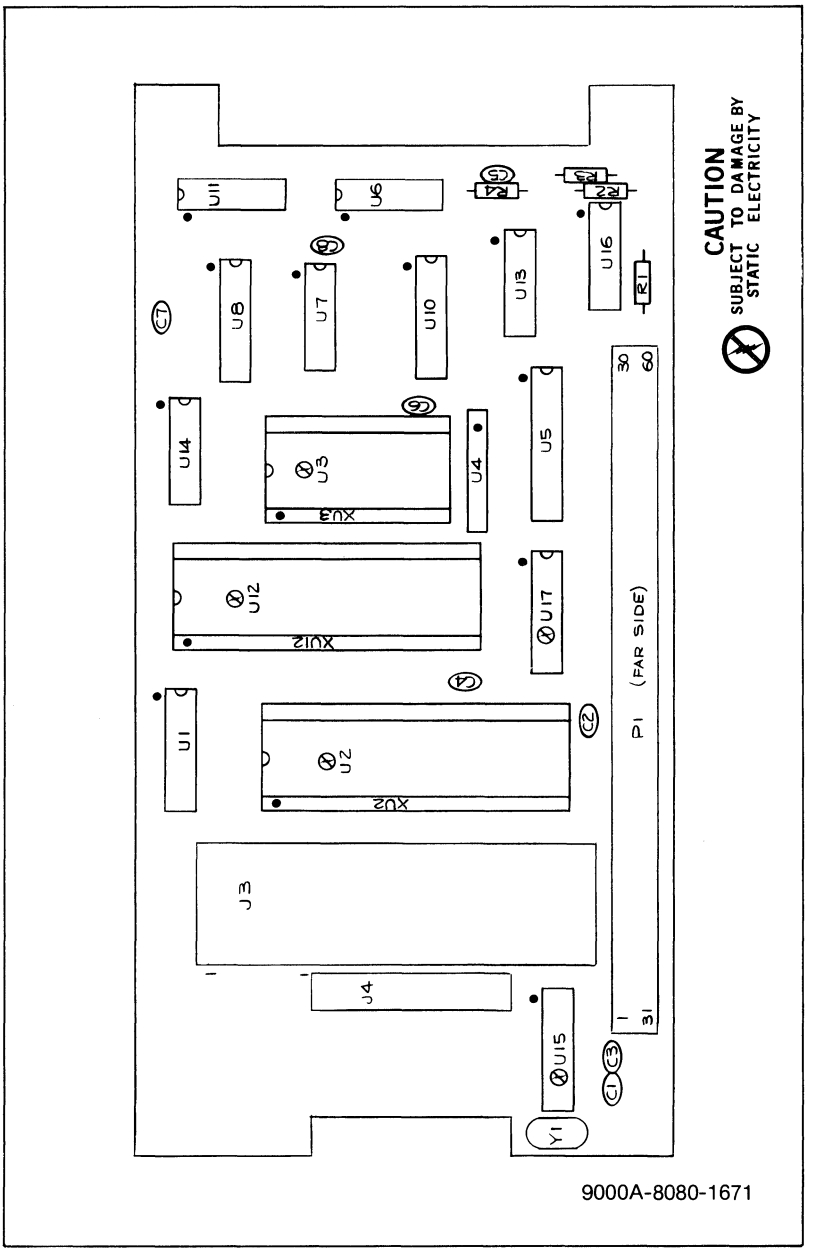

Figure 6-2. A17 Processor PCB Assembly

Table 6-3. A18 Interface PCB Assembly

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
A18	⊗9000A-8080 INTERFACE PCB ASSEMBLY FIGURE 6-3 (9000A-8080-4072T)	581181	89536	581181	REF		
A1	HYBRID, PROTECTION CIRCUIT	583021	89536	583021	4		
A2	HYBRID, PROTECTION CIRCUIT	583021	89536	583021	REF		
A3	HYBRID, PROTECTION CIRCUIT	583021	89536	583021	REF		
A4	HYBRID, PROTECTION CIRCUIT	582270	89536	582270	1		
A5	HYBRID, PROTECTION CIRCUIT	583021	89536	583021	REF		
C1	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	14		
C2	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C3	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C4	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C5	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C6	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C7	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C8	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C9	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C10	CAP, CER, 0.01 UF +/-20%, 100V	407361	72982	8121-A100-W5R-103M	1		
C11	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C12	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C13	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C14	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C15	CAP, CER, .22 UF +/-20%, 50V	519157	51406	RPE111Z5U224M50V	REF		
C16	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015A1	2		
C17	CAP, TA, 10 UF +/-20%, 15V	193623	56289	196D106X0015A1	REF		

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
CR1	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	5	1	
CR2	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	REF		
CR3	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	REF		
CR4	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	REF		
CR5	DIODE, SI, HI-SPEED SWITCHING	203323	07910	1N4448	REF		
J1	CONNECTOR, 60-PIN	602813	00779	86396-6	1		
J2	CONNECTOR, POST	267500	00779	86144-2	40		
R1	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	2		
R2	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R3	RES, DEP. CAR, 1.2K +/-5%, 1/4W	441378	80031	CR251-4-5P1K2	1		
R4	RES, COMP, 56 +/-10%, 1/2W	109009	01121	RC20GF560KS	1		
R5	RES, DEP. CAR, 2.2K +/-5%, 1/4W	343400	80031	CR251-4-5P2K2	1		
R6	RES, DEP. CAR, 200 +/-5%, 1/4W	441451	80031	CR251-4-5P200E	2		
R7	RES, DEP. CAR, 200 +/-5%, 1/4W	441451	80031	CR251-4-5P200E	REF		
R8	RES, DEP. CAR, 820 +/-5%, 1/4W	442327	80031	CR251-4-5P821E	1		
R9	RES, DEP. CAR, 3K +/-5%, 1/4W	441527	80031	CR251-4-5P3K	1		
R10	RES, COMP, 4.7K +/-5%, 1/4W	348821	01121	CB4725	1		
U1	⊗IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	5	1	
U2	⊗IC, C-MOS, OCTAL BUS TRANSCEIVER	535906	36665	74C245AC	4	1	
U3	⊗IC, C-MOS, OCTAL BUS TRANSCEIVER	535906	36665	74C245AC	REF		
U4	⊗IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		
U5	⊗IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		
U7	⊗IC, C-MOS, OCTAL BUS TRANSCEIVER	535906	36665	74C245AC	REF		
U8	⊗IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		
U9	⊗IC, C-MOS, OCTAL LATCH HI-SPEED	585364	36665	74SC374A	REF		

Table 6-3. A18 Interface PCB Assembly (cont)

REF DES	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO.	TOT QTY	REC QTY	NOTE
U10	IC, PROTECTOR	585992	89536	585992	1		
U11	IC, TTL, DUAL 4-INPUT NAND LINE DRIVER	585414	01295	SN74S140N	1	1	
U12	RESISTOR NETWORK	606996	89536	606996	1	1	
U13	RESISTOR NETWORK	583476	89536	583476	1	1	
U14	Ⓐ IC, C-MOS, OCTAL BUS TRANSCEIVER	535906	36665	74C245AC	REF		
U15	RESISTOR NETWORK	494690	89536	494690	1		
VR1	IC, LIN, LOW VOLTAGE REFERENCE	452771	89536	452771	1	1	
XU1	SOCKET, IC, 20-PIN	454421	01295	C932002	9		
XU2	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU3	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU4	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU5	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU7	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU8	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU9	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XU10	SOCKET, IC, 18-PIN	413229	01295	C 93102	1		
XU14	SOCKET, IC, 20-PIN	454421	01295	C932002	REF		
XVR1	INSULATOR (NOT SHOWN)	175125	89536	175125	1		

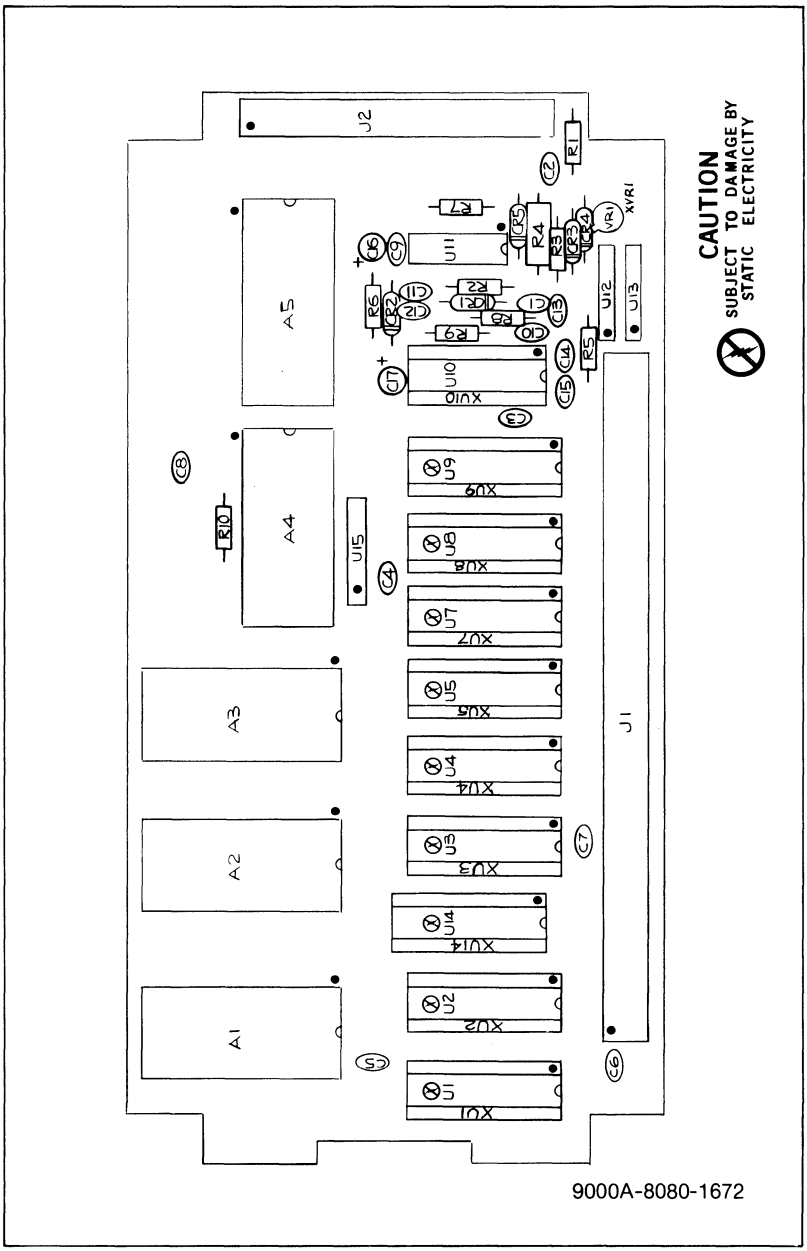

Figure 6-3. A18 Interface PCB Assembly

Section 7
Schematic Diagrams

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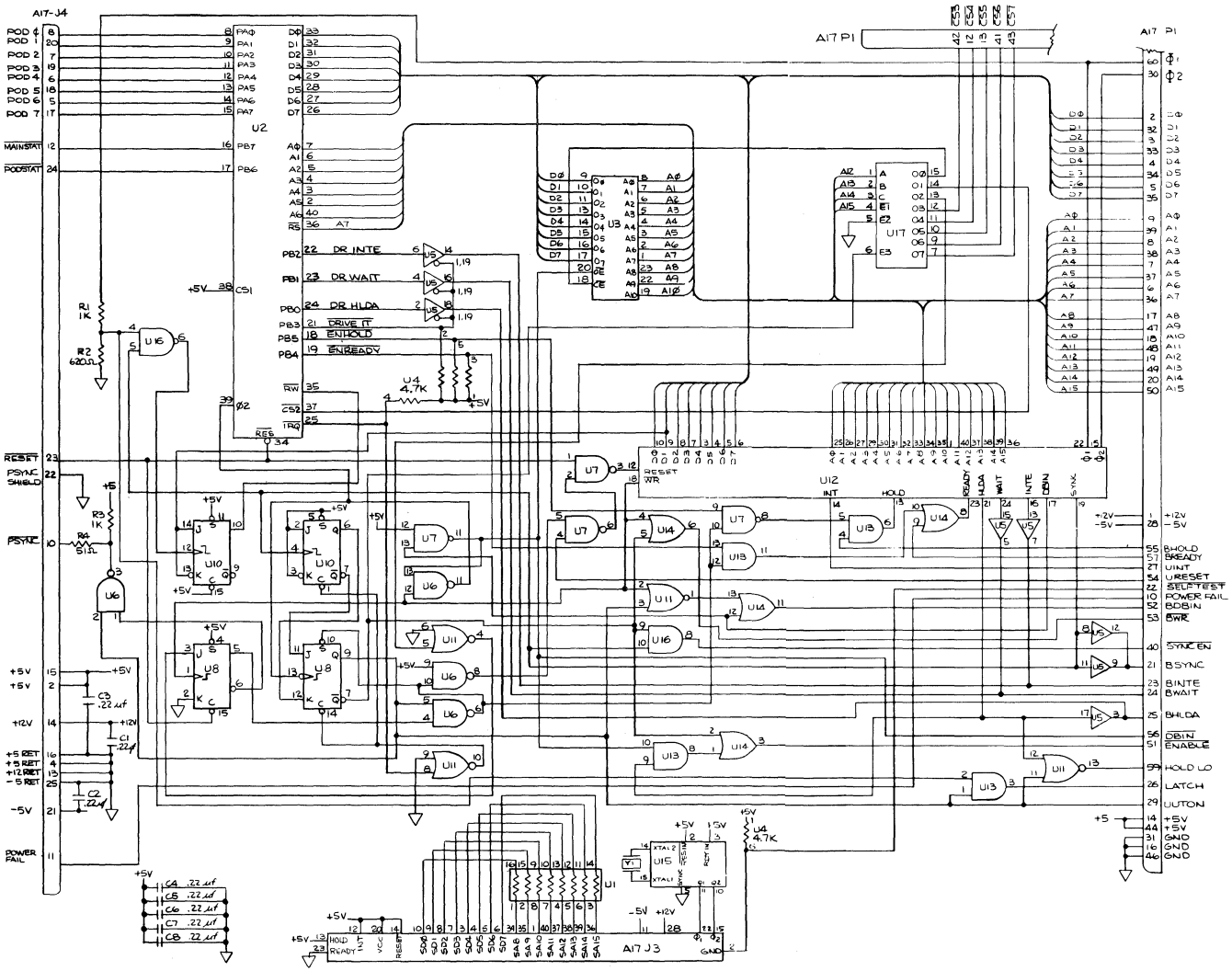
8080



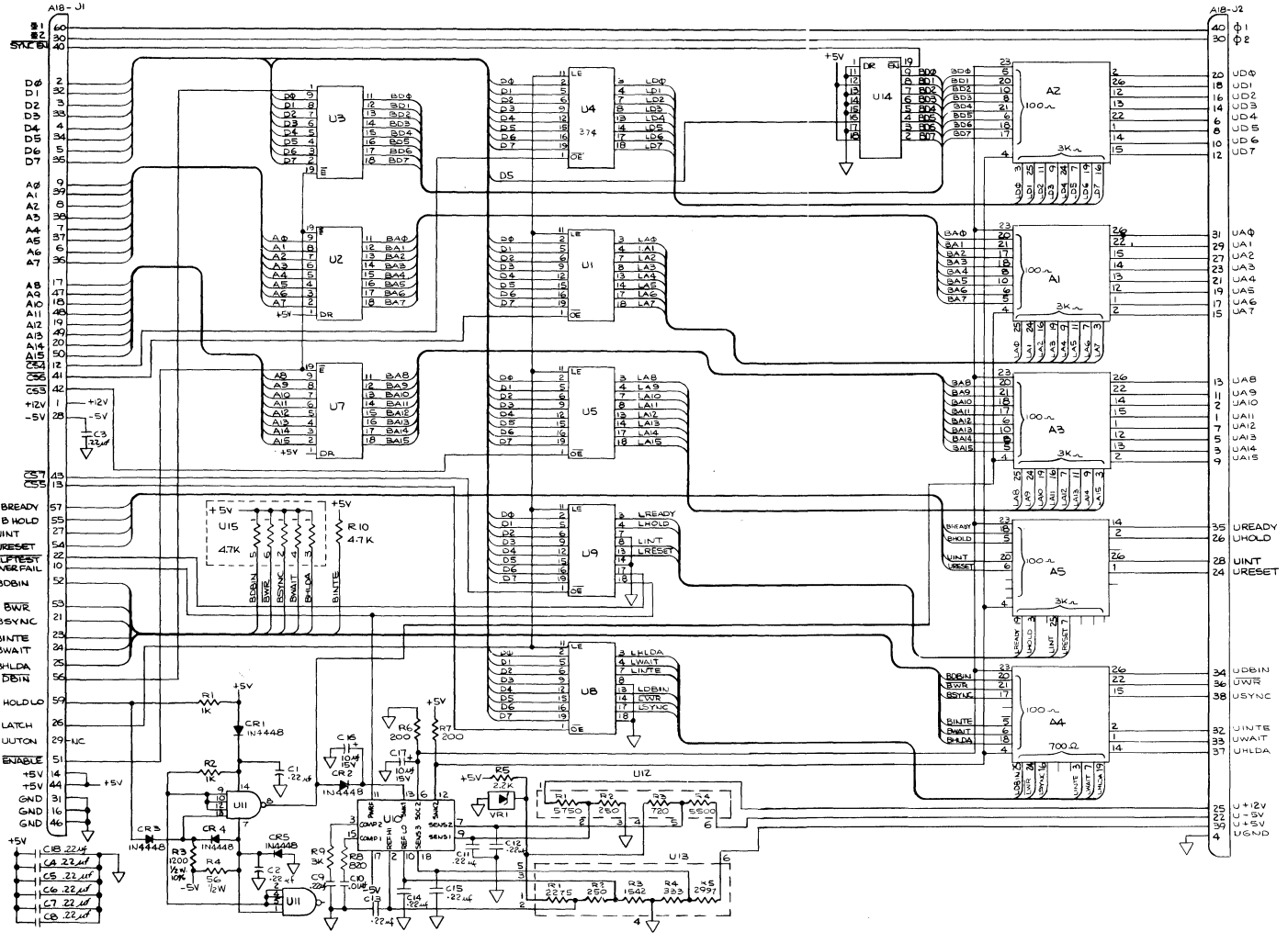
REF DES	DEVICE	NO. OF PINS	+5	GND	-5	+12
U12	8080A1	40	20	2	11	28
U2	6532A	40	20	1	—	—
U3	2716	24	21,24	12	—	—
U4	4.7K RES NET	6	1	—	—	—
U5	74LS241	20	20	10	—	—
U6,16	74LS00	14	14	7	—	—
U8	74LS112	16	16	8	—	—
U10	74LS109	16	16	8	—	—
U11	74LS02	14	14	7	—	—
U1	2K RES NET	16	—	—	—	—
U13	74LS08	14	14	7	—	—
U14	74LS32	14	14	7	—	—
U15	8224	16	16	8	—	9
U17	74LS138	16	16	8	—	—

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4 W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.

9000A-8080-1071

Figure 7-1. A17 Processor PCB Assembly

8080



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.

REF DES	DEVICE	+5V	GND	-5V	+12V
U1	74SC374	20	10	—	—
U2	74C245	20	10	—	—
U3	74C245	20	10	—	—
U4	74SC374	20	10	—	—
U5	74SC374	20	10	—	—
U14	74C245	20	10	—	—
U7	74C245	20	10	—	—
U8	74SC374	20	10	—	—
U9	74SC374	20	10	—	—
U10	9000A-8076	1,4	8,16,14	17	—
U11	74S140	—	—	—	—
A1	9000A-4H66T	—	—	—	—
A2	9000A-4H66T	—	—	—	—
A3	9000A-4H66T	—	—	—	—
A4	9000A-4H68T	—	—	—	—
A5	9000A-4H66T	—	—	—	—
U13	54-4087T	—	4	—	—
U12	54-4088T	—	3	—	—
U15	RES. NET, 4.7K, SIP	1	—	—	—

9000A-8080-1072

Figure 7-2. A18 Interface PCB Assembly

CHANGE/ERRATA INFORMATION

ISSUE NO: 3 3/89

This change/errata contains information necessary to ensure the accuracy of the following manual. Enter the corrections in the manual if either one of the following conditions exist:

1. The revision letter stamped on the indicated PCB is equal to or higher than that given with each change.
2. No revision letter is indicated at the beginning of the change/errata.

MANUAL

Title: 9000A-8080
Print Date: June 1981
Rev.- Date: 1-7/81

C/E PAGE EFFECTIVITY

Page No.	Print Date
1	7/83
2	7/83
3	7/83
4	7/83
5	3/89

CHANGE #1 - 15431
Rev.-D, A18 Interface PCB Assembly (9000A-8080-4072T)

On page 6-9, Table 6-3:
ADD: CR6|DIODE, SI, HI-SPEED SWITCHING|313247|28480|HP5082-6264|1

On page 6-11/6-12, Figure 6-3, add CR6 as shown in Figure 1.

On page 7-4, Figure 7-2, add CR6 as shown in Figure 2.

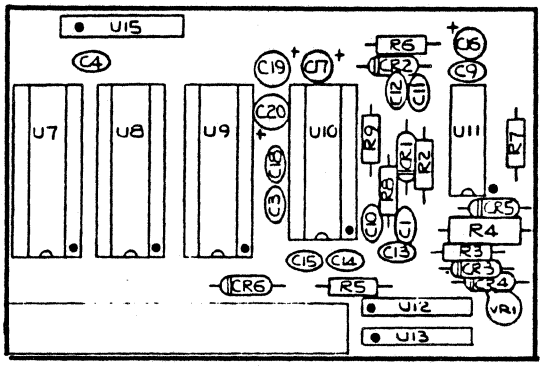


Figure 1.

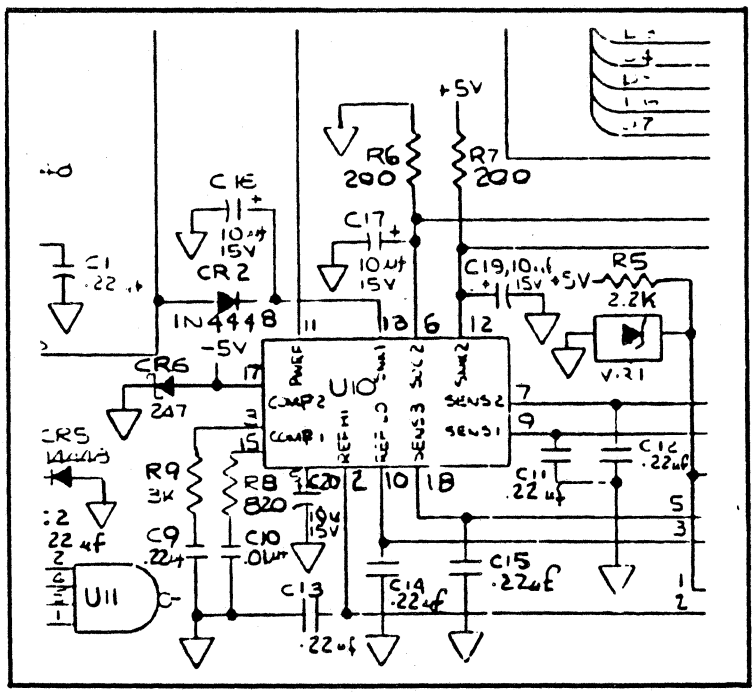


Figure 2.

CHANGE #2 - 15527
Rev.-D, A17 Processor PCB Assembly (9000A-8080-4071T)

On page 6-6, Table 6-2:
ADD: XU16|SOCKET, IC, 14-PIN DIL (NOT SHOWN)
|276527|91506|314-AG39D|1

CHANGE #3 - 16116
Rev.-E, A17 Processor PCB Assembly (9000A-8080-4071T)

On page 6-5, Table 6-2:
CHANGE: U3|IC, MOS, N-CHANNEL 16K BIT|586164|89536|586164|1|1
TO: U3|IC, MOS, N-CHANNEL 16K BIT|540366|89536|540366|1|1

CHANGE #4 - 16245, 16419, 16439
Rev.-F, A17 Processor PCB Assembly (9000A-8080-4071T)

On pages 6-5 and 6-6, Table 6-2:

Change the TOT QTY for R1,
FROM: 2
TO: 1

CHANGE: R3|RES, CEP. CAR, 1K +/-5%, 1/4W|343426|80031|CR251-4-5P1K|REF
TO: R3|RES, DPE. CAR, 4.7K +/-5%, 1/4W
|348821|80031|CR251-4-5P4K7|1

CHANGE: R4|RES, DEP. CAR, 51 +/-5%, 1/4W|414540|80031|CR251-4-5P51E|1
TO: R4|RES, DEP. CAR, 1 +/-5%, 1/4W |357665|80031|CR251-4-5P1E |1

CHANGE: P1|CONNECTOR, PIN |513879|00779|4-870221 |60
TO: P1|CONNECTOR, POST, GOLD|649681|00779|3-87011-2|60

CHANGE: U6|IC, TTL, QUAD, 2-INPUT, POS NAND GATE
|393033|01295|SN74LS00N|3|1
TO: U6|IC, TTL, QUAD, 2-INPUT NAND GATE
|654210|12040|DM74LS00N|3|1

CHANGE: U7|IC, TTL, QUAD, 2-INPUT, POS NAND GATE
|393033|01295|SN74LS00N|REF
TO: U7|IC, TTL, QUAD, 2-INPUT NAND GATE
|654210|12040|DM74LS00N|REF

CHANGE: U16|IC, TTL, QUAD, 2-INPUT, POS NAND GATE
|393033|01295|SN74LS00N|REF
TO: U16|IC, TTL, QUAD, 2-INPUT NAND GATE
|654210|12040|DM74LS00N|REF

On page 7-2, Figure 7-1, change the value of R4,
FROM: 51
TO: 1

CHANGE #5 - 17086
Rev.-E, A18 Interface PCB Assembly (9000A-8080-4072T)

On pages 6-8 thru 6-10, Table 6-3:

Change the TOT QTY for C16,
FROM: 2
TO: 4

ADD: C19,C20|CAP, TA, 10 UF +/-20%, 15V
|193623|56289|196D106X0015A1|REF

On page 6-11/6-12, Figure 6-3, add C19 and C20 as shown in Figure 1.

On page 7-4, Figure 7-2, add C19 and C20 as shown in Figure 2.

CHANGE #6 - 17278
Rev.-B, Final Assembly (9000A-8080-5071)

On page 6-3, Table 6-1:
Change the TOT QTY for H1,
FROM: 2
TO: 3

ADD: MP7|LABEL, STATIC CAUTION|605808|89536|605808|1

ADD: MP8|LABEL, UUT CAUTION|634030|89536|634030|1

ADD: MP9|9000A POD ACCESSORIES
- CABLE, UUT
- LABEL, UUT CAUTION
- PLASTIC BAG
- SOCKET, DIP 40-PIN|582254|89536|582254|1

ADD: MP10|RETAINING CLIP|583260|89536|583260|1

CHANGE: W2|CABLE ASSEMBLY, UUT|604769|89536|604769|1
TO: W2|CABLE ASSEMBLY, UUT|685487|89536|685487|1

On page 6-4, Figure 6-1, add H1 and MP10 as shown in Figure 3.

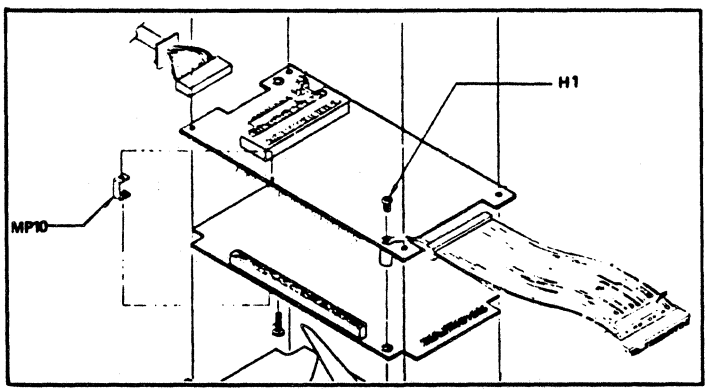


Figure 3.

CHANGE #7 - 17488
Rev.-G, A17 Processor PCB Assembly (9000A-8080-4071T)

On page 6-3, Table 6-1:

CHANGE:	W1	CABLE ASSEMBLY, POD	581827	89536	581827 | 1
TO:	W1	CABLE ASSEMBLY, POD	581819	89536	581819 | 1

On pages 6-5 and 6-6, Table 6-2:

DELETE:	R3	.....			
CHANGE:	R4	RES, DEP. CAR, 1 +/-5%, 1/4W	357665	80031	CR251-4-5P1E | 1
TO:	R4	RES, DEP. CAR, 39 +/-5%, 1/4W	340836	80031	CR251-4-5P39E | 1
CHANGE:	U6	IC, TTL, QUAD 2-INPUT, NAND GATE	654210	12040	DM74LS00N | 3 | 1
TO:	U6	IC, FTTL, QUAD 2-INPUT, NAND GATE	654640	07263	74F00PC | 1 | 1
CHANGE:	U7	IC, TTL, QUAD 2-INPUT, NAND GATE	654210	12040	DM74LS00N | REF
TO:	U7	IC, TTL, QUAD, 2-INPUT, POS NAND GATE	393033	01295	SN74LS00N | REF
CHANGE:	U16	IC, TTL, QUAD 2-INPUT, NAND GATE	654210	12040	DM74LS00N | REF
TO:	U16	IC, TTL, QUAD, 2-INPUT, POS NAND GATE	393033	01295	SN74LS00N | REF

On pages 6-7, Figure 6-2, delete R3 and add R7 as shown in Figure 4.
On page 7-2, Figure 7-1, delete R3, change the value of R4 to 39 and add R7 as shown in Figure 5.

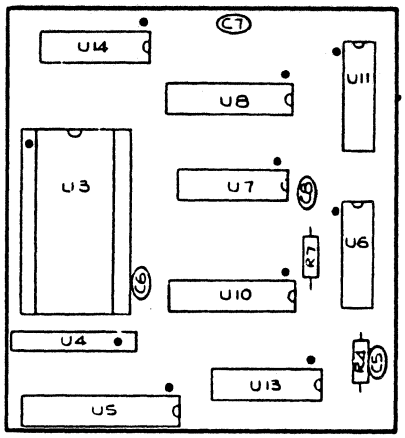


Figure 4.

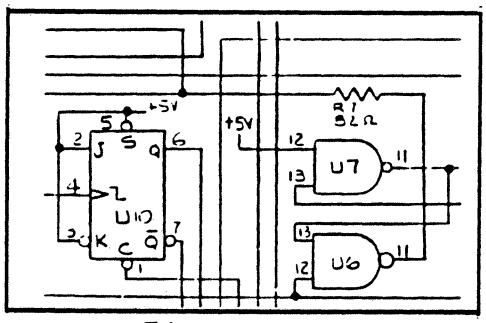


Figure 5.

ERRATA #1

On page 6-3, Table 6-1, make the following changes:

```
CHANGE:    H1|.....................|185918|89536|185918|2
TO:        H1|.....................|185918|COMMERCIAL  |2

CHANGE:    H2|.....................|152132|89536|152132|4
TO:        H2|.....................|152132|COMMERCIAL  |4
```

ERRATA #2

On pages 6-5 and 6-6, Table 6-2, make the following changes:

```
CHANGE:    J4|.....................|512590|89536|512590   |1
TO:        J4|.....................|512590|00779|1-87230-3|1

CHANGE:    MP1|....................|602284|89536|602284      |2
TO:        MP1|....................|602284|9W423|9536B-B-0440|2

CHANGE:    U1|.....................|574905|89536|574905      |1|1
TO:        U1|.....................|574905|91637|MDP1603-202J|1|1
```

ERRATA #3

On page 6-10, Table 6-3, make the following changes:

```
CHANGE:    U15|....................|494690|89536|494690      |1
TO:        U15|....................|494690|91637|CSC06B01472G|1

CHANGE:    VR1|....................|452771|89536|452771 |1|1
TO:        VR1|....................|452771|32293|ITS6935|1|1

CHANGE:    XVR1|...................|175125|89536|175125   |1
TO:        XVR1|...................|175125|07047|10172-DAP|1
```