

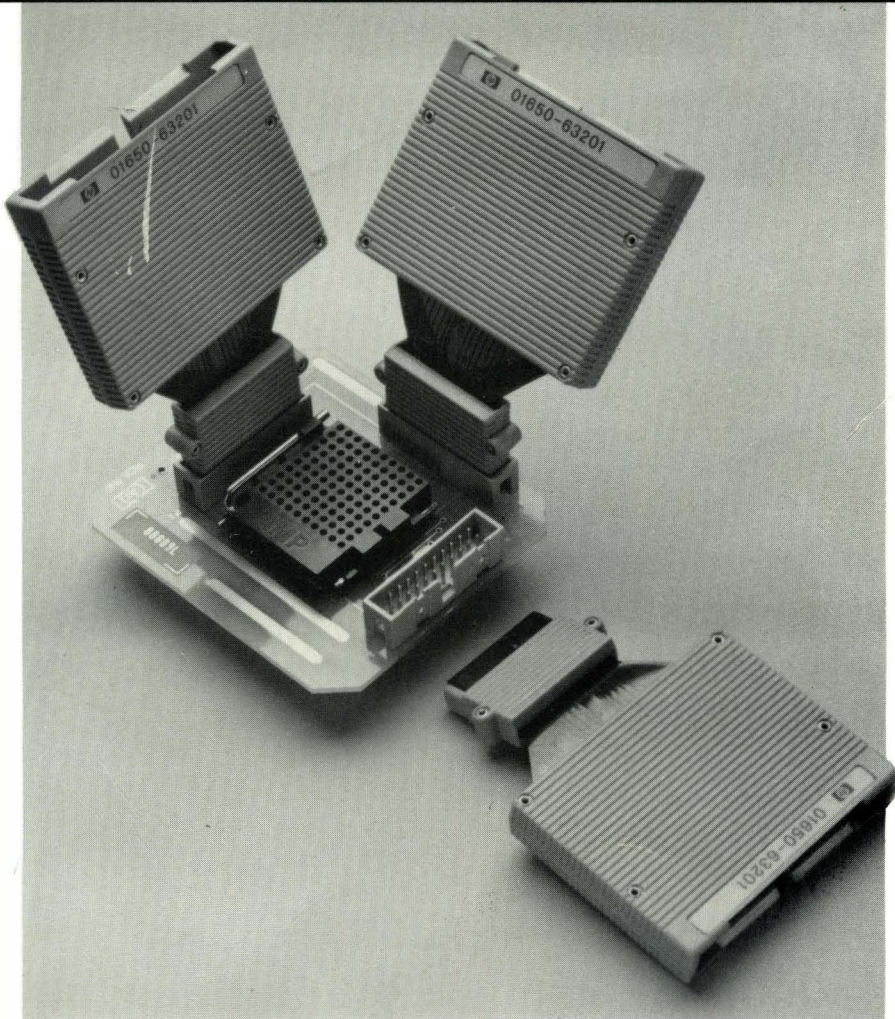
# HP 10311G

# Motorola 68000/68010

# Preprocessor

for the HP 1650A and HP 16510A Logic Analyzers

## Operating Manual



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# **HP 10311G Motorola 68000/68010 Preprocessor Operating Manual**

**for the HP 1650A and HP 16510A Logic Analyzers**

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## List of Effective Pages

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**Pages**

**Effective Date**



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# Table of Contents

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## Chapter 1:

	<b>Analyzing the Motorola 68000/68010</b>
1-1	Introduction
1-2	Installation Overview
1-3	Equipment Supplied
1-3	Equipment Required
1-4	Connecting to the Target System
1-6	Connecting the Termination Adapters
1-7	Connecting to the HP 10311G
1-7	Setting Up the Analyzer from the Disc
1-8	Format Specification
1-9	Symbols
1-10	Listing Menu
1-11	The 68000/68010 Inverse Assembler
1-12	Interpreting Data
1-13	Error Messages
1-14	Status Encoding
1-15	Analyzing the 68000/68010 Directly with Logic Analyzer Probes

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## Chapter 2:

	<b>General Information</b>
2-1	Interface Module Specifications
2-2	Interface Description
2-2	Interface Requirements
2-2	Testing and Troubleshooting





# Analyzing the Motorola 68000/68010

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1

## Introduction

This operating manual includes information on using the 68000/68010 Inverse Assembler with or without the HP 10311G Preprocessor Interface Module.

The HP 10311G Preprocessor Interface Module provides a complete interface between any 68000/68010 target system and the HP 1650A or HP 16510A Logic Analyzer. The interface module connects the signals from the 68000/68010 target microprocessor directly to the logic analyzer inputs.

Since there is no active circuitry between the microprocessor and the logic analyzer to add skew to signals, the interface can be used for timing analysis as well as state analysis.

The 68000/68010 configuration software on the flexible disc sets up the format specification menu of the logic analyzer for compatibility with the 68000/68010 microprocessor. It also loads the inverse assembler for obtaining displays of 68000/68010 data in 68000/68010 assembly language mnemonics. The interface module specifications are given in chapter 2.

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## Installation Overview

1. Connect the 68000/68010 Preprocessor (HP 10311G) to the target system (see page 1-4).
2. Connect the three termination adapters (HP part number 01650-63201) to the interface module (see page 1-6).
3. Plug the logic analyzer probes into the termination adapters on the interface module as follows:

HP 1650A and 16510A Pod	(into)	HP 10311G Connector
1		P1
2		P2
3		P3

4. Load the logic analyzer configuration and inverse assembler by loading the file C68000\_P or C68010\_P from the inverse assembler disc (see page 1-7).

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## Equipment Supplied

The HP 10311G Preprocessor and Inverse Assembler consists of the following:

- The preprocessor hardware, which includes the interface circuit card and connector;
- The three termination adapters (HP part number 01650-63201);
- The inverse assembly software on a 3.5-inch disc; and
- This operating manual.

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## Equipment Required

The minimum hardware for state analysis of a 68000/68010 target system consists of the following:

- An HP 1650A or HP 16510A Logic Analyzer; and
- The 68000/68010 Preprocessor and Inverse Assembler (HP 10311G).

**CAUTION**

*To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the interface module or microprocessor is being connected or disconnected.*

---

## Connecting to the Target System

1. Remove the 68000/68010 microprocessor from its socket on the target system and store it in a protected environment.
2. Plug the interface connector into the microprocessor socket on the target system.

### CAUTION

*Care must be taken to align pin A1 of the connector assembly with pin A1 of the microprocessor socket on the target system to prevent mis-alignment or damage. Pin A1 of the connector assembly socket is identified on the socket board and shown in figure 1-1.*

3. The microprocessor socket on the interface connector is a Zero Insertion Force (ZIF) socket. Before installing the microprocessor, open the socket by raising the small lever on the pin A1 end of the socket.
4. Plug the 68000/68010 microprocessor into the socket of the interface connector.
5. Secure the microprocessor in the socket by pushing down the lever until it clicks into place.

### Note

*The ZIF socket assembly pins, shown in figure 1-1, are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold plated pins of the assembly from damage due to impact.*

*When you're not using the preprocessor, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.*

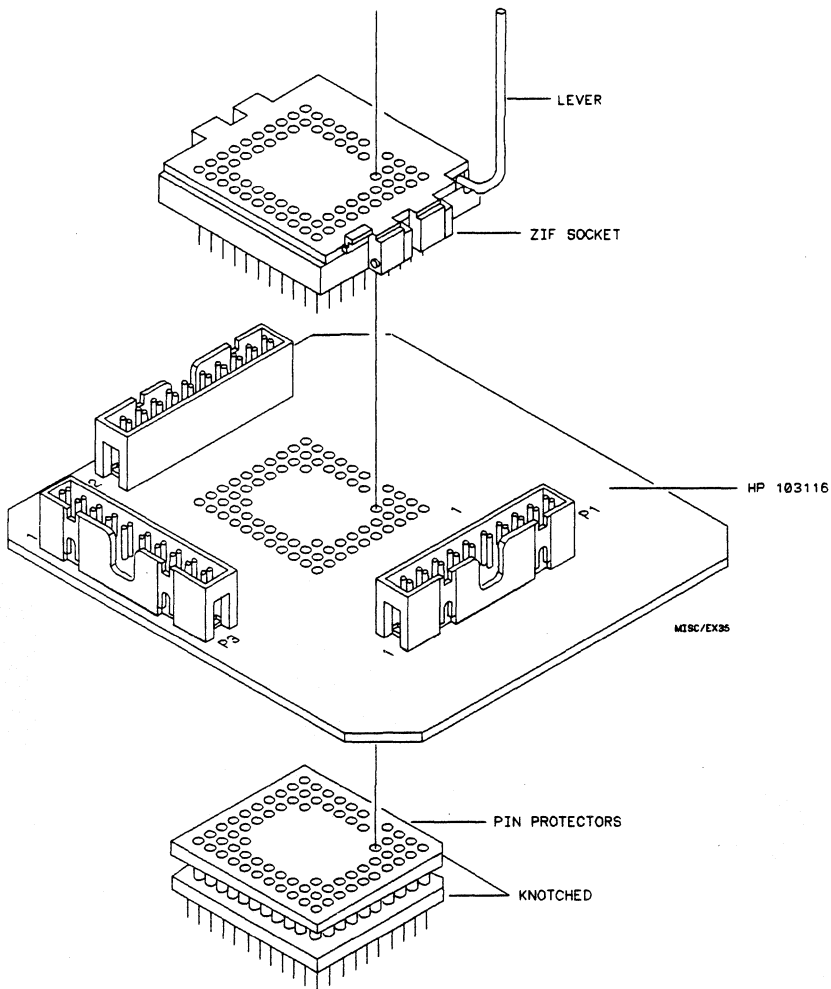


Figure 1-1. Interface Socket Assembly (Exploded View)

### Note

*Additional plastic pin guards can be added if the interface connector interferes with components of the target system or if a higher profile is required. The HP part number for the plastic pin guards is 1200-1353.*

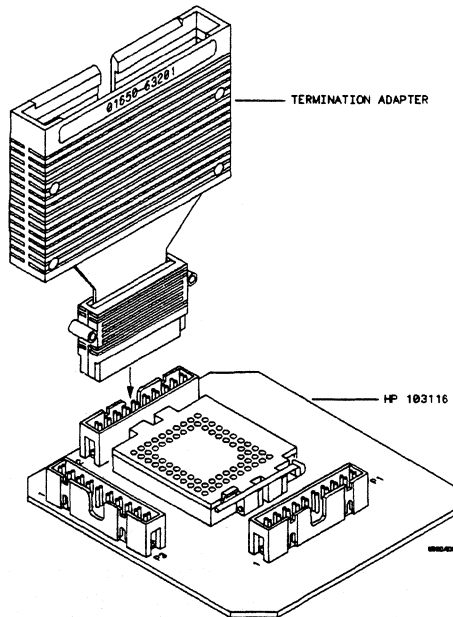
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## Connecting the Termination Adapters

The termination adapter (HP part number 01650-63201) properly terminates the HP 1650A and HP 16510A logic analyzer probes and allows the probes to be connected directly to the HP 10311G Interface Module.

To connect the three termination adapters to the HP 10311G:

1. Align the key on the termination adapter with the slot on the appropriate connector on the HP 10311G.
2. Push the termination adapter into the connector.
3. Repeat steps 1 and 2 for each termination adapter.



*Figure 1-2. Connecting Termination Adapters*

---

## Connecting to the HP 10311G

Connect the HP 1650A or HP 16510A Logic Analyzer pods to the termination adapters on the HP 10311G Interface Module as follows:

HP 1650A and 16510A Pod	(into)	HP 10311G Connector
1		P1
2		P2
3		P3

---

## Setting Up the Analyzer from the Disc

The logic analyzer can be configured for 68000 or 68010 analysis by loading the proper configuration file. Loading this file will also load the inverse assembler file. To load the configuration and inverse assembler:

1. Install the flexible disc labeled "68000/10 Inverse Assembler for use with: HP 1650A and HP 16510A" in the front disc drive of the logic analyzer.
2. Select one of the following menus:
  - For the HP 1650A, select the I/O Disc Operations menu;
  - For the HP 16510A, select the System Front Disc menu.
3. Configure the menu to "Load" the analyzer from the file C68000\_P or C68010\_P, depending on which microprocessor is being used.
4. Execute the load operation to load the file into the HP 1650A or HP 16510A Logic Analyzer.



## Format Specification

When you use the 68000/68010 Interface Module, the format specification will be set up by the software as shown in figure 1-3. Table 1-2 on page 1-16 lists the 68000/68010 signals for the HP 10311G and their corresponding lines to the logic analyzer.

Inputs to the logic analyzer are grouped under functional labels for the convenience of the user. The Address, Data, and Status labels are used by the inverse assembler to generate assembly language mnemonics for displaying the trace list. Pertinent control and clock threshold levels are also part of the format specification.

68000 - State Format Specification Specify Symbols

Clock Period  Clock

	Pod 3	Pod 2	Pod 1
	TTL	TTL	TTL
	Clock	Clock	Clock
Activity >	-----	-----	-----
Label Pol	15 ... 87 ... 0	15 ... 87 ... 0	15 ... 87 ... 0
ADDR	+ *****	+ *****	+ *****
DATA	+ .....	+ .....	+ .....
STAT	+ .....	+ .....	+ .....
SIZE	+ .....	+ .....	+ .....
VMA	+ .....	+ .....	+ .....
	-Off-	-Off-	-Off-
	-Off-	-Off-	-Off-
	-Off-	-Off-	-Off-
	-Off-	-Off-	-Off-
	-Off-	-Off-	-Off-

Figure 1-3. 68000/68010 Format Specification

### Note

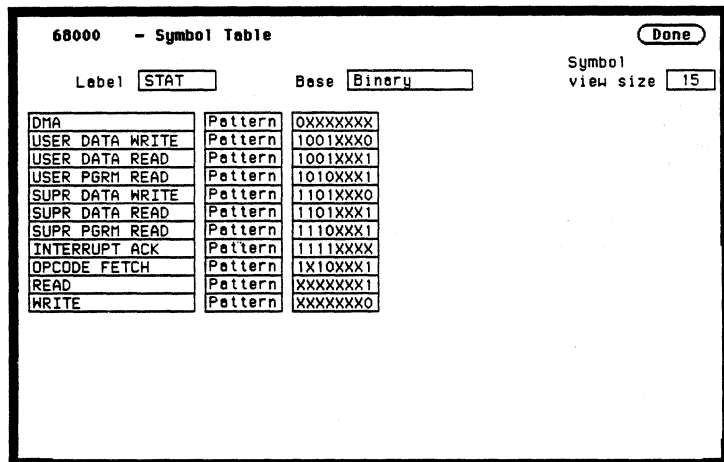
*The Clock Period field in figure 1-3 should remain in the current selection (> 60 ns) for proper HP 10311G operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.*

## Symbols

The Symbol Table of the format specification menu is set up with names to identify values of the status label (see figure 1-4).

Additional labels have been defined in the format specification menu to make triggering on specific 68000 or 68010 cycles easier. Some labels that may be of interest are:

- The "SIZE" label which indicates the size of the transfer on the data bus (8-bit or 16-bit transfer) and which byte of an 8-bit transfer is valid.
- The "VMA" label which monitors the VMA line on the microprocessor. When this line is high, the microprocessor is executing a 6800 cycle.



68000 - Symbol Table

Label: STAT Base: Binary Symbol view size: 15

DMA	Pattern	0XXXXXX
USER DATA WRITE	Pattern	1001XXX0
USER DATA READ	Pattern	1001XXX1
USER PGM READ	Pattern	1010XXX1
SUPR DATA WRITE	Pattern	1101XXX0
SUPR DATA READ	Pattern	1101XXX1
SUPR PGM READ	Pattern	1110XXX1
INTERRUPT ACK	Pattern	1111XXX1
OPCODE FETCH	Pattern	1X10XXX1
READ	Pattern	XXXXXXXX1
WRITE	Pattern	XXXXXXXX0

Figure 1-4. Symbol Table for the 68000/68010

## Listing Menu

Captured data is displayed as shown in figure 1-5. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

Label >	ADDR	68000 Mnemonic	STAT
Base >	Hex	hex	Symbol
+0069	020096	JMP 02009C [PC]	SUPR PRGM READ
+0070	020000	MOVE.L #***** ,*****	SUPR DATA READ
+0071	02009B	0004 program read	SUPR PRGM READ
+0072	02009C	MOVE.L #00000001,D0	SUPR PRGM READ
+0073	02009E	0000 program read	SUPR PRGM READ
+0074	0200A0	0001 program read	SUPR PRGM READ
+0075	0200A2	JMP 0200A5 [PC,D0.W]	SUPR PRGM READ
+0076	0200A4	0001 program read	SUPR PRGM READ
+0077	0200A6	MOVE.L #00000004,D3	SUPR PRGM READ
+0078	0200A8	0000 program read	SUPR PRGM READ
+0079	0200AA	0004 program read	SUPR PRGM READ
+0080	0200AC	JMP 0200AE [PC,D3.L]	SUPR PRGM READ
+0081	0200AE	3800 program read	SUPR PRGM READ
+0082	0200B2	MOVE.L #00000000,A1	SUPR PRGM READ
+0083	0200B4	0000 program read	SUPR PRGM READ
+0084	0200B6	0000 program read	SUPR PRGM READ

Figure 1-5. Listing Menu for the 68000/68010

---

## The 68000/68010 Inverse Assembler

The 68000/68010 microprocessors do not provide enough status information for the inverse assembler to pick out the first word of an opcode fetch from a series of program reads. To insure correct disassembly, you must point to a state that contains the first word on an opcode fetch. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen.

To do this:

1. Select a line on the display that you know is the first state of an instruction fetch.
2. Roll this line to the top of the listing.
3. Select the "Invasm" field at the top of the display. The listing will inverse assemble from the top line down. Any data before this display is left unchanged.

Rolling the display up will inverse assemble the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you must re-synchronize the inverse assembler by repeating steps 1 through 3.

### **Note**

*Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.*

## Interpreting Data

The pair of asterisks (\*\*) displayed in the operand field of an instruction indicates that a byte of an expected operand was not stored in the logic analyzer memory. Four asterisks (\*\*\*\*) indicate that one word of an expected operand was missing and eight asterisks signify a missing long word. Missing operands (or parts of operands) can result from 68000/68010 instruction prefetch activity or storage qualification.

### Examples:

ORI.B	***,D2	(missing byte operand)
ORI.W	****,D1	(missing word operand)
ORI.L	#234A****,D3	(missing "lower" word of the operand)
ORI.L	***** ,D3	(missing both words of the operand)

In general, asterisks indicate that expected operand fetches are not stored in the logic analyzer memory. Operand fetches may be missed when you add storage qualifications to the standard trace and format specifications.

The 68000/68010 is capable of supporting byte, word, and long word (32-bit) operands. During operand reads and writes, entire 16-bit (word) values appear on the microprocessor data bus. In the case of single byte operands, the inverse assembler will display "xx" for the byte of the input data that is ignored by the microprocessor. In this manner, it is possible to determine exactly which byte of data the microprocessor has used as an operand.

### Examples:

ORI.B	#03,D1	xx03 supr program read	(microprocessor uses lower byte only)
ORI.W	#1203,D1	1203 supr program read	(microprocessor uses both bytes of the word)

The 68000 and 68010 microprocessors are prefetching microprocessors. That is, they will fetch the next instruction word while the last opcode is still being executed. When a program executes a single-word instruction that causes a branch, the prefetched word is not used and will be discarded by the microprocessor.

The logic analyzer monitors all bus cycles, including unused prefetches. After disassembly, the inverse assembler marks these unused states by displaying "unused prefetch."

Note that the logic analyzer will capture these states, even if they are not executed. Care must be taken when you're specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused prefetch may generate an unwanted trigger.

Since the microprocessor only prefetches one word, one technique to avoid unwanted triggering from unused prefetches is to add "2" to the trigger address. Then the trigger condition will only be satisfied if the branch is not taken.

**Error Messages** The following list of messages will help you identify operation errors.

Data Error	Trace data collected by the logic analyzer cannot be retrieved from memory. Indicates hardware error or inverse assembler software error.
Illegal Opcode	Undefined opcode encountered. Microprocessor action cannot be determined.

### **Note**

*Do not modify the ADDRESS, DATA, or STATUS labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.*

## Status Encoding

Each of the eight bits of the STATUS label are described below. Table 1-1 lists the precise value of each bit for all types of 68000 or 68010 microprocessor cycles. Bit 0 is the least significant bit of the 8-bit field.

Bit	Status Signals	Description
0	R/W	This signal is high for read cycles and low for write cycles.
1	LDS	This signal is low when the low byte of the data bus is valid.
2	UDS	This signal is low when the high byte of the data bus is valid. A combination of the LDS and UDS signals will allow you to determine the size of the data bus transfer.
3	VMA	This signal is low for 6800 cycles.
4 - 6	FC0 - FC3	These signals indicate the type of cycle the microprocessor is executing.
7	BGACK	This signal is low when the microprocessor has granted control of the bus to another device.

*Table 1-1. Status Field Encoding*

68000 or 68010	Status Bit 7 6 5 4 3 2 1 0
<b>Cycle Type</b>	
Bus Grant 6800 Cycle User Data Write User Data Read User Program Read Supervisor Data Write Supervisor Data Read Supervisor Program Read Interrupt Acknowledge	0 x x x x x x x 1 x x x x 0 x x 1 0 0 1 x x x 0 1 0 0 1 x x x 1 1 0 1 0 x x x 1 1 1 0 1 x x x 0 1 1 0 1 x x x 1 1 1 1 0 x x x 1 1 1 1 1 x x x x
<b>Size of Transfer</b>	
Low Byte Transfer High Byte Transfer Word Transfer	x x x x x 1 0 x x x x x x 0 1 x x x x x x 0 0 x

## Analyzing the 68000/68010 Directly with Logic Analyzer Probes

In order to use the inverse assembler with general purpose probes, you must connect the probes to the 68000/68010 microprocessor as shown in table 1-2. After the specified hookups have been completed, data sampling may begin. Be sure to load the appropriate file for your particular microprocessor before taking any measurements. Load file C68000\_P for the 68000 and file C68010\_P for the 68010 microprocessor. When the disc is read, the format specification for the 68000/68010 is automatically set up. The format specifications correspond with the following interconnections. These correspond directly with the connections made through the HP 10311G Interface Module.



Table 1-2. Connecting Directly to the 68000/68010 with Logic Analyzer Probes

68000/68010 Signal	68000 68010 Pin	Label	HP 1650A and 16510A	
			Pod	Bit
LUDS	B3	ADDRESS	2	0
A1	K4	ADDRESS	2	1
A2	J5	ADDRESS	2	2
A3	K5	ADDRESS	2	3
A4	K6	ADDRESS	2	4
A5	J6	ADDRESS	2	5
A6	K7	ADDRESS	2	6
A7	K8	ADDRESS	2	7
A8	J7	ADDRESS	2	8
A9	K9	ADDRESS	2	9
A10	J8	ADDRESS	2	10
A11	J9	ADDRESS	2	11
A12	H9	ADDRESS	2	12
A13	H8	ADDRESS	2	13
A14	J10	ADDRESS	2	14
A15	G9	ADDRESS	2	15
A16	H10	ADDRESS	3	8
A17	G10	ADDRESS	3	9
A18	F9	ADDRESS	3	10
A19	F10	ADDRESS	3	11
A20	E10	ADDRESS	3	12
A21	D10	ADDRESS	3	13
A22	C10	ADDRESS	3	14
A23	C9	ADDRESS	3	15
D0	B4	DATA	1	0
D1	A3	DATA	1	1
D2	A4	DATA	1	2
D3	B5	DATA	1	3

Table 1-2. Connecting Directly to the 68000/68010 with Logic Analyzer Probes (Continued)

68000/68010 Signal	68000/ 68010 Pin	Label	HP 1650A and 16510A	
			Pod	Bit
D4	A5	DATA	1	4
D5	A6	DATA	1	5
D6	B6	DATA	1	6
D7	A7	DATA	1	7
D8	A8	DATA	1	8
D9	B7	DATA	1	9
D10	A9	DATA	1	10
D11	B8	DATA	1	11
D12	A10	DATA	1	12
D13	C8	DATA	1	13
D14	B9	DATA	1	14
D15	B10	DATA	1	15
R/LW	C3	STATUS	3	0
LLDS	B2	STATUS	3	1
LUDS	B3	STATUS	3	2
LVMA	G1	STATUS	3	3
FC0	K3	STATUS	3	4
FC1	J3	STATUS	3	5
FC2	K2	STATUS	3	6
LBGACK	C1	STATUS	3	7
LAS	A2	(Clock)	1	CLK
LDTACK	B1	(Clock)	2	CLK*

\* This signal is not required to properly clock the logic analyzer. However, it may be useful for other 68000/68010 analysis.

## Interface Module Specifications

### Microprocessor

Compatibility: Motorola MC68000, MC68010, and all microprocessors made by other manufacturers that comply with Motorola MC68000/MC68010 specifications.

Microprocessor Package: 68-pin PGA

Accessories Required: HP 10311G

Maximum Clock Speed: 12.5 MHz Clock Input

Signal Line Loading: 100k ohms plus 18 pF capacitance on all lines

### Microprocessor

Operations Displayed: User Data Read/Write  
User Program Read  
Supervisor Read/Write  
Supervisor Program Read  
Interrupt Acknowledge  
Bus Grant  
6800 Cycle

Additional Capabilities: The logic analyzer captures all bus cycles, including prefetches.

Power Requirements: None

### Logic Analyzer

Required: HP 1650A or HP 16510A

Number of Probes Used: Three 16-channel probes

**Environmental**

Temperature: Operating: 0 to +55 degrees C  
(+32 to +131 degrees F)

Nonoperating: -40 to +75 degrees C  
(-40 to +167 degrees F)

Altitude: Operating: 4600 m (15,000 ft)

Nonoperating: 15,300 m (50,000 ft)

Humidity: To 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

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**Interface  
Description**

The 68000/68010 interface provides an interface between either a 68000 or 68010 target system and the logic analyzer.

Lines are sampled on the rising edge of the address strobe (LAS).

---

**Interface  
Requirements**

The 68000/68010 Interface Module will operate with the 68000 or 68010 microprocessors clocked at rates up to 12.5 MHz. The card adds 100k ohms load to all monitored lines and an interface capacitance of approximately 18 pF.

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**Testing and  
Troubleshooting**

There are no automatic performance tests or adjustments for the HP 10311G Interface Module. If a failure is suspected in the HP 10311G Preprocessor Interface Module, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

## Your Comments Please

HP 10311G

Your comments assist us in meeting your needs better. Please complete this questionnaire and return it to us. Feel free to add any additional comments that you might have. All comments and suggestions become the property of Hewlett-Packard. Omit any questions that you feel would be proprietary.

- |  | Yes                      | No                       |
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| 1. Did you receive your product when expected?                           | <input type="checkbox"/> | <input type="checkbox"/> |
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| Other _____  |                          |                          |

4. What measurements will this preprocessor be used to make?
- \_\_\_\_\_

5. Which logic analyzer are you using?

Type \_\_\_\_\_

6. What do you like most about the preprocessor? \_\_\_\_\_
- \_\_\_\_\_

7. What would you like to see changed or improved? \_\_\_\_\_

8. Which sections of the manual(s) have you used?

- Installation Overview  
 Step-By-Step Procedures  
 Specifications

9. Please rate the manual(s) on the following:

4 = Excellent      3 = Good      2 = Adequate      1 = Poor

- Breadth and depth of information  
 Ability to easily find information  
 Ability to understand and apply the information provided in the manual

Please explain: \_\_\_\_\_

10. What is your experience with logic analyzers and preprocessors?

- No previous experience  
 Less than 1 year experience  
 More than 1 year's experience on one model  
 More than 1 year's experience on several models

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