HEWLETT PACKARD

User's Guide

HP 10314D
Intel 80386DX
Preprocessor Interface

U1A
U1B
U1C
U1D
U1E
U2A
U2C
U2D
U2E
U3C
U4B
U4C
U4D
U4E
XH1
GND
RESET
CLK2
ADS
READY
CLK
8616
EXP
BUS
CYCLE
AMD
8851
P L K J H F E D C B A
10314
86502
REV A
MADE IN USA

HP 10314D Intel 80386DX Preprocessor Interface User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D and HP 16550A Logic Analyzers

Manual Part Number 10314-90915
Microfiche Part Number 10314-90815

Printed in U.S.A. February 1992

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 February 1992 10314-90915

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

Pages **Effective Date**

Product Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of 1 year from date of shipment. During warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard. However, warranty service for products installed by Hewlett-Packard and certain other products designated by Hewlett-Packard will be performed at Buyer's facility at no charge within the Hewlett-Packard service travel area. Outside Hewlett-Packard service travel areas, warranty service will be performed at Buyer's facility only upon Hewlett-Packard's prior agreement and Buyer shall pay Hewlett-Packard's round trip travel expenses.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument.

Hewlett-Packard does not warrant that the operation of the instrument, software, or firmware will be uninterrupted or error-free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Exclusive Remedies

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For assistance, contact your nearest Hewlett-Packard Sales and Service Office.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

Safety

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this user's guide must be heeded.

Contents

Appendix A: Troubleshooting

Introduction

The HP 10314D Preprocessor Interface, when installed in the HP 10269C General Purpose Probe Interface, provides a complete interface between any 80386DX target system and the following logic analyzers: HP 1650A, HP 1650B, HP 16510A, HP 16510B, HP 16511B, HP 1652B, HP 16540/16541A,D, or HP 16550A.

The 80386DX configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 80386DX microprocessor. It also loads the inverse assembler for obtaining displays of 80386DX data in 80386DX assembly language mnemonics.

Logic Analyzers Supported

The following logic analyzers are supported by the HP 10314D Preprocessor Interface:

HP 1650A, HP 1650B, HP 16510A, HP 16510B, and HP 1652B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with 112 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz of timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP 10314D Preprocessor Interface for state and timing analysis with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP 10314D software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP 10314D Preprocessor Interface. It also contains information on servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1

Setting Up the HP 10314D

Introduction

The HP 10314D Preprocessor Interface, when installed in the HP 10269C General Purpose Probe Interface, provides a complete interface between an 80386DX target system and the following HP logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16550A, and an HP 16540A,D with two HP 16541A,D expansion cards. The preprocessor interface connects the signals from the 80386DX target microprocessor to the logic analyzer inputs and generates all status and clock signals required by the software for inverse assembly of the 80386DX instruction set.

The 80386DX Preprocessor Interface operates in the bus mode. In the bus mode all bus cycles, including prefetches, are sent to the logic analyzer as they occur. All coprocessor cycles on the local bus are also captured.

The 80386DX configuration software on the flexible disk sets up the format specification of the logic analyzer for compatibility with the 80386DX microprocessor. It also loads the inverse assembler routine for obtaining displays of 80386DX data in assembly language mnemonics.

The preprocessor interface can be used for timing analysis as well as state analysis. The State/Timing switch on the preprocessor interface board determines which type analysis is obtained. In the Timing position, a minimal amount of skew is added between the signals.

Duplicating the Master Disk

Before you use the HP 10314D software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP 10314D master disk. Store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

Equipment Supplied

The HP 10314D Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card and cable assembly.
- The inverse assembly software on a 3.5-inch disk.
- This user's guide.

Note

The preprocessor interface socket assembly pins are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold-plated pins of the assembly from damage due to impact. When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.

Equipment Required

The minimum hardware required for analysis of an 80386DX target system consists of the following equipment:

- An HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16550A, or HP 16540A,D with two HP 16541A,D expansion cards.
- The HP 10269C General Purpose Probe Interface, which connects the preprocessor interface to the logic analyzer.
- The 80386DX Preprocessor Interface and Inverse Assembler (HP 10314D).

Installation Overview

The following procedure describes the major steps required to perform measurements with the HP 10314D Preprocessor Interface. The page numbers listed in the various steps refer you to sections in the manual that offer more detailed information.

Caution

To prevent equipment damage, remove the power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. If required, move jumpers J5 through J8 to select between signals for analysis. Then update the Format menu to match your current selections (see "Jumpers" page 1-4).

Note

To disable the HLDA line from stopping the logic analyzer clocks, move jumper J9 to the ON position (see page 2-12).

2. Move the State/Timing switch to the appropriate position for state or timing analysis (see page 1-4).
3. Install the 80386DX preprocessor interface (HP 10314D) into the HP 10269C Probe Interface (see page 1-6).
4. Connect the 80386DX microprocessor connector to the target system (see page 1-8).
5. Plug the logic analyzer probes into the probe interface as listed in table 1-1 on page 1-10. Note that the logic analyzers are grouped into three categories. These same groupings apply to the configuration files.
6. Load the logic analyzer configuration and inverse assembler for the specified logic analyzer (see page 1-12). Table 1-2 lists the configuration files and the inverse assemblers (see page 1-10).
7. For timing analysis, select the configuration menu of the logic analyzer and select Timing as the analyzer "Type" (see page 2-15).

Jumpers

The jumpers on the preprocessor interface board allow you to select different signals for analysis. These jumpers are set at the factory to view the READY, ADS, BUSY, and PEREQ signals on status bits 12 through 15. Figure 1-1 shows the location of the jumpers.

- J8 (pod 5, bit 15) allows you to select between READY and NMI.
- J7 (pod 5, bit 14) allows you to select between ADS and INTR.
- J6 (pod 5, bit 13) allows you to select between BUSY and READY.
- J5 (pod 5, bit 12) allows you to select between PER and ADS.

If you move the jumpers, you must update the Format menu to reflect your changes. To update the Format menu:

1. If you move the jumper on J8 to the NMI position, change the READY label to read NMI.
2. If you move the jumper on J7 to the INTR position, modify the ADS label to read INTR.
3. If you move the jumper on J6 to the READY position, assign pod 5 of the READY label to bit 13 instead of bit 15.
4. If you move the jumper on J5 to the ADS position, assign pod 5 of the ADS label to bit 12 instead of bit 14.
5. Turn off any unused labels.

Figure 2-2 (page 2-2) shows the Format menu when the jumpers are set to select the NMI, INTR, READY, and ADS signals.

The State/Timing Switch

The State/Timing switch allows you to configure the HP 10314D preprocessor interface for either state or timing analysis. For state analysis, this switch must be set to the far-right position as shown on the preprocessor interface board (see figure 1-1).

For timing analysis, this switch is set to the far-left position. In this position the signals are buffered straight through the preprocessor interface, adding only minimal skew to signals.

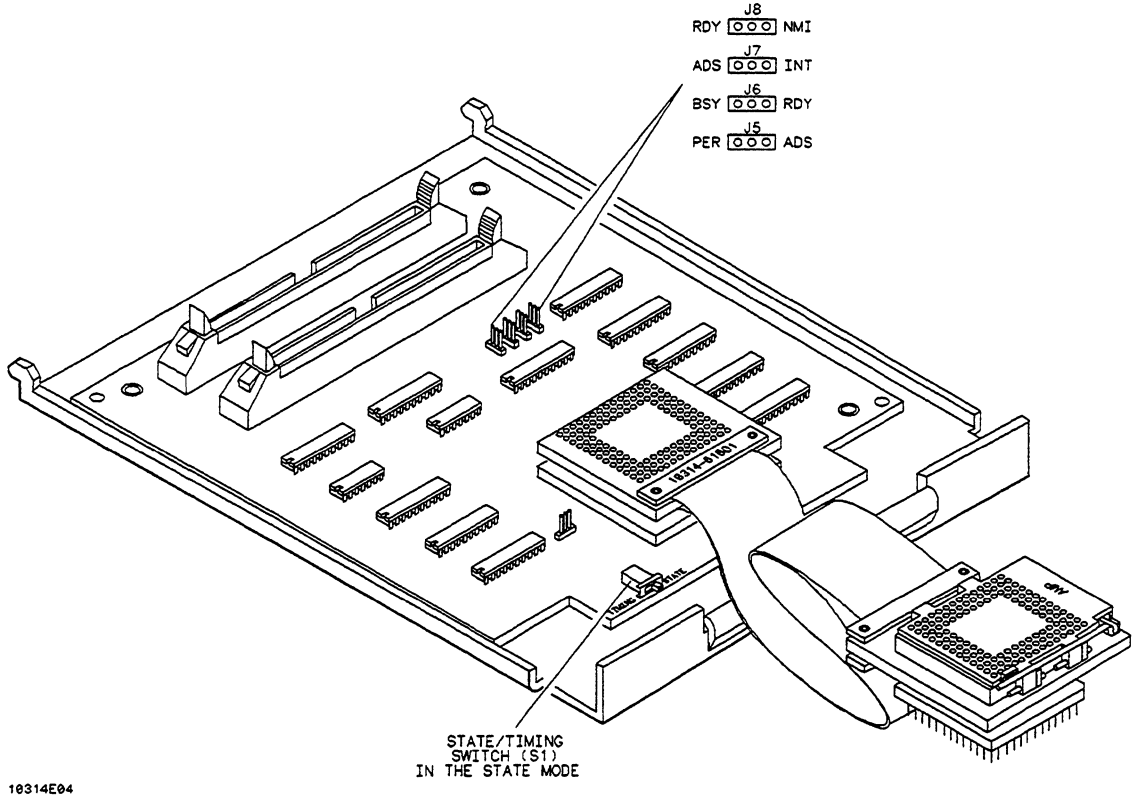


Figure 1-1. State/Timing Switch and Jumpers J5 - J8

Note

The State/Timing switch can be accessed through the slot in the metal cover for the target system ribbon cable without removing the preprocessor interface from the HP 10269C.

Installing the HP 10314D in the HP 10269C

The HP 10269C General Purpose Probe Interface routes the signals from the HP 10314D Preprocessor Interface and provides the correct mechanical connections for the logic analyzer probes. To install the HP 10314D in the HP 10269C:

1. Install the HP 10314D Preprocessor Interface on the underside of the HP 10269C General Purpose Probe Interface Pod (see figure 1-2).

Caution

Care must be used when handling the preprocessor interface to avoid damaging the preprocessor interface cable. Avoid bending, twisting, making contact with sharp edges, and other mechanical stress which may damage the cable.

2. Insert the metal tabs of the preprocessor interface card in the slots of the pod.
3. Connect the two internal pod cables to the preprocessor interface card.
4. Gently fold the preprocessor interface card into the pod and fasten the cable end of the preprocessor interface card to the pod with the two captive screws on the preprocessor interface card.

Caution

To prevent equipment damage, remove the power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

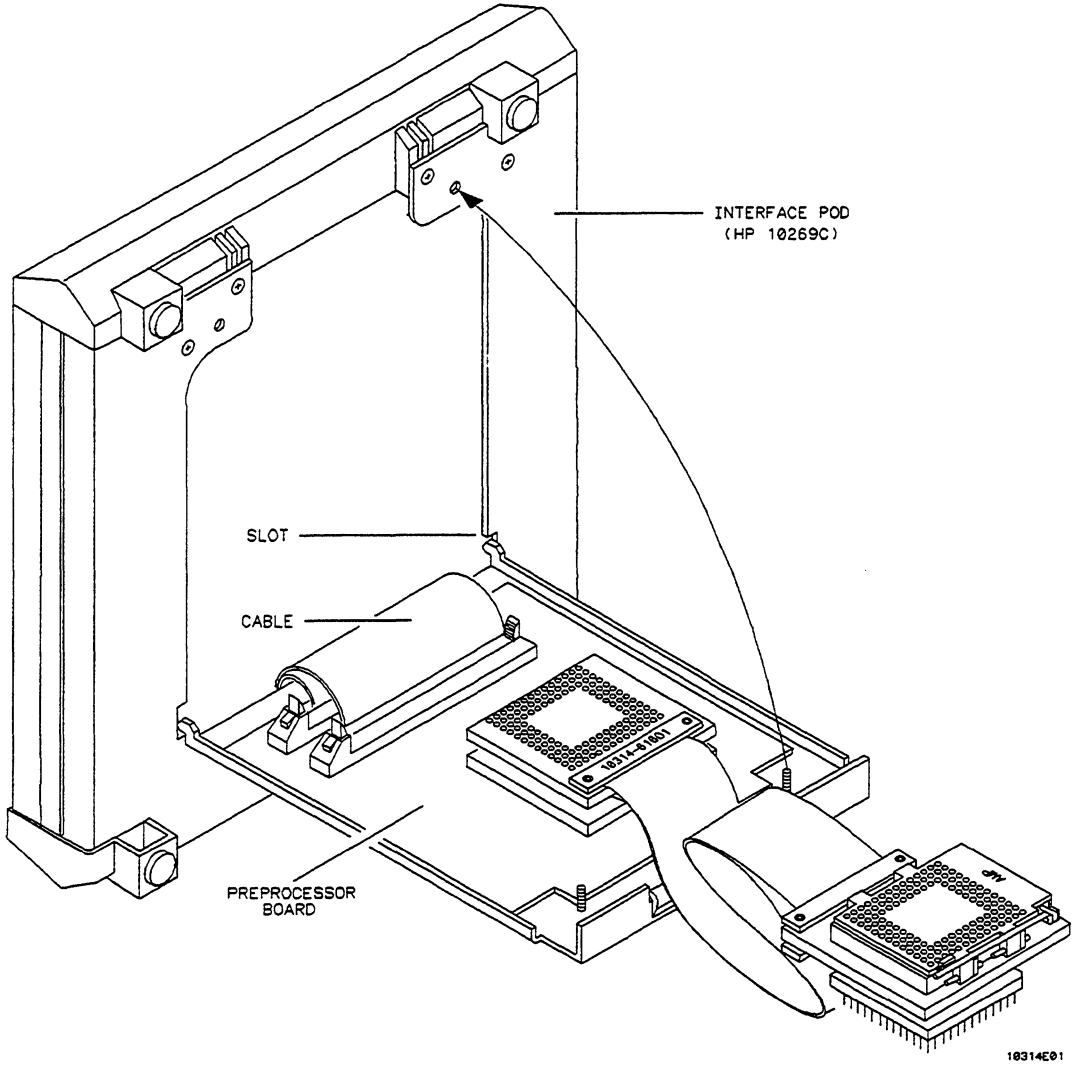


Figure 1-2. Installing the HP 10314D in the HP 10269C

Connecting to the Target System

The microprocessor connector on the preprocessor interface cable will connect directly to a PGA socket on the target system. To connect the microprocessor connector to the target system:

Caution

PROTECT AGAINST STATIC DISCHARGE

The preprocessor interface contains devices that are susceptible to damage by Electrostatic Discharge (ESD). Therefore, precautionary measures should be taken before handling the microprocessor connector attached to the end of the preprocessor interface cable in order to avoid damaging the internal components of the preprocessor interface with static electricity.

Do not install the microprocessor connector of the preprocessor interface in the target microprocessor socket while power is applied to the target system. The preprocessor interface may be damaged if power is not removed from the target system prior to installation.

---

1. Remove the 80386DX microprocessor from the target system microprocessor socket.
2. Store the microprocessor in a protected environment.
3. Place the microprocessor connector, attached to the end of the cable from the preprocessor interface, in the target system microprocessor socket (see figure 1-3).

Caution

Serious damage to the target system and/or preprocessor interface can result from incorrect connection. Take care to note the position of pin A1 on both the connector and socket prior to inserting the connector in the socket. Also, take care to align the microprocessor connector with the target system socket so that all microprocessor pins are making contact.

---

4. If the ZIF socket is not already installed on the target system side of the HP 10314D cable, install it on top of the microprocessor connector (see figure 1-3).

5. Place the microprocessor in the ZIF socket on top of the microprocessor connector.

Note

The ZIF socket on the top of the microprocessor connector allows you to easily load and unload the microprocessor without damaging the device or the microprocessor connector. However, this socket does increase the capacitive load on the target system.

Heavily loaded systems may not operate properly with this additional capacitance. If this is the case, remove the ZIF socket from the microprocessor connector and carefully install the 80386DX directly on the microprocessor connector.

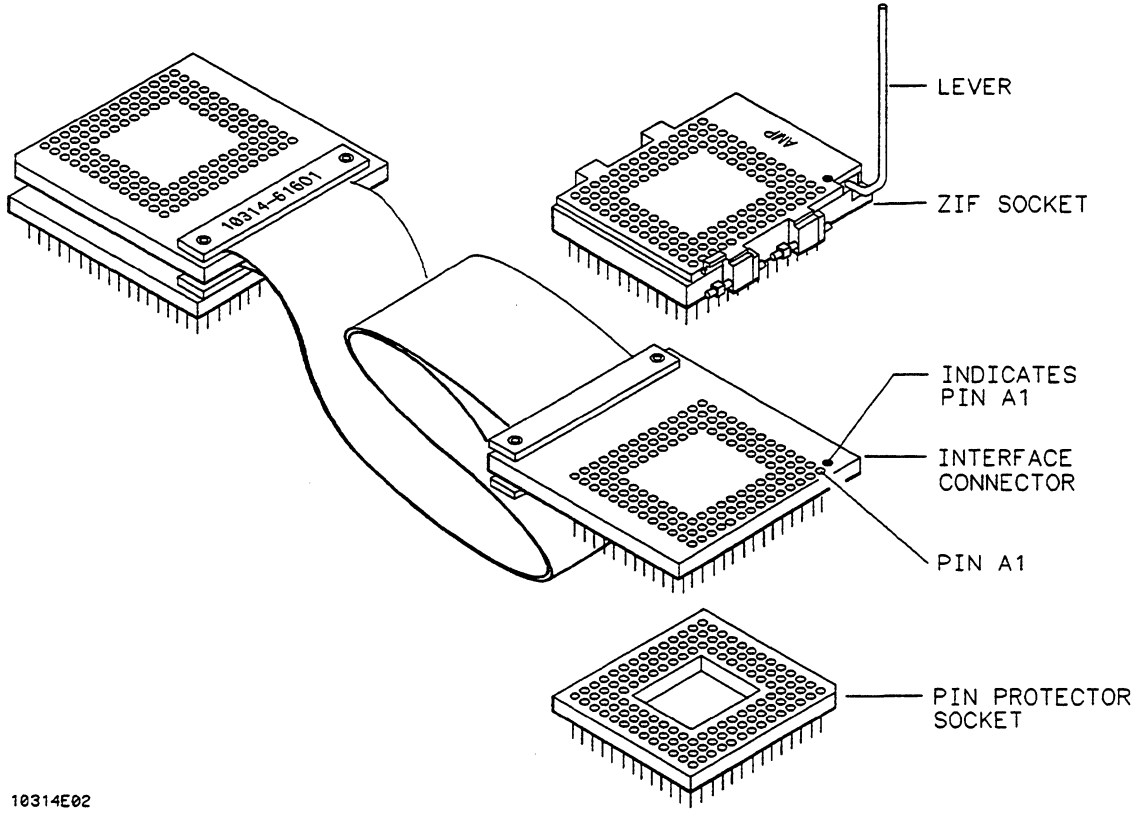


Figure 1-3. Installing the Cable in the PGA Socket

Connecting to the HP 10269C

Connect the logic analyzer pods to the HP 10269C General Purpose Probe Interface as listed in table 1-1. Note that the logic analyzers are grouped into three categories. These same groupings apply to the configuration files.

Table 1-1. Connections

HP 16540/ 16541A,D Logic Analyzer Pod	HP 16511B Logic Analyzer Pod	All Other Logic Analyzers Pod	(Into)	HP 10269C Connector
Master Card, Pod 1	Expander Card, Pod 1	1		1
*Exp. Card 2, Pod 1	Expander Card, Pod 2	2		2
*Exp. Card 1, Pod 1	Expander Card, Pod 3	3		3
*Exp. Card 1, Pod 2	Expander Card, Pod 4	4		4
*Exp. Card 1, Pod 3	Expander Card, Pod 5	5		5

* For the HP 16541A,D Expander Cards, Exp. Card 1 refers to the physically highest HP16541A,D card, and Exp. Card 2 refers to the next physically highest HP 16541A,D card (see figure 1-4).

Table 1-2. Configuration and Inverse Assembler Files

Logic Analyzer	Configuration Filename	Inverse Assembler Filename	Capability
HP 16540/16541A,D	E80386D_I	I80386D_I	Works with all coprocessors. Does not attempt to decode the coprocessor instructions when an ESC instruction is encountered.
HP 16511B	D80386D_I	I80386D_I	
all others	C80386D_I	I80386D_I	
HP 16540/16541A,D	E80386D_87	I80386D_87	Works with systems that use only 80287/80387 coprocessors. When an ESC instruction is encountered, the inverse assembler decodes the math coprocessor operation.
HP 16511B	D80386D_87	I80386D_87	
all others	C80386D_87	I80386D_87	

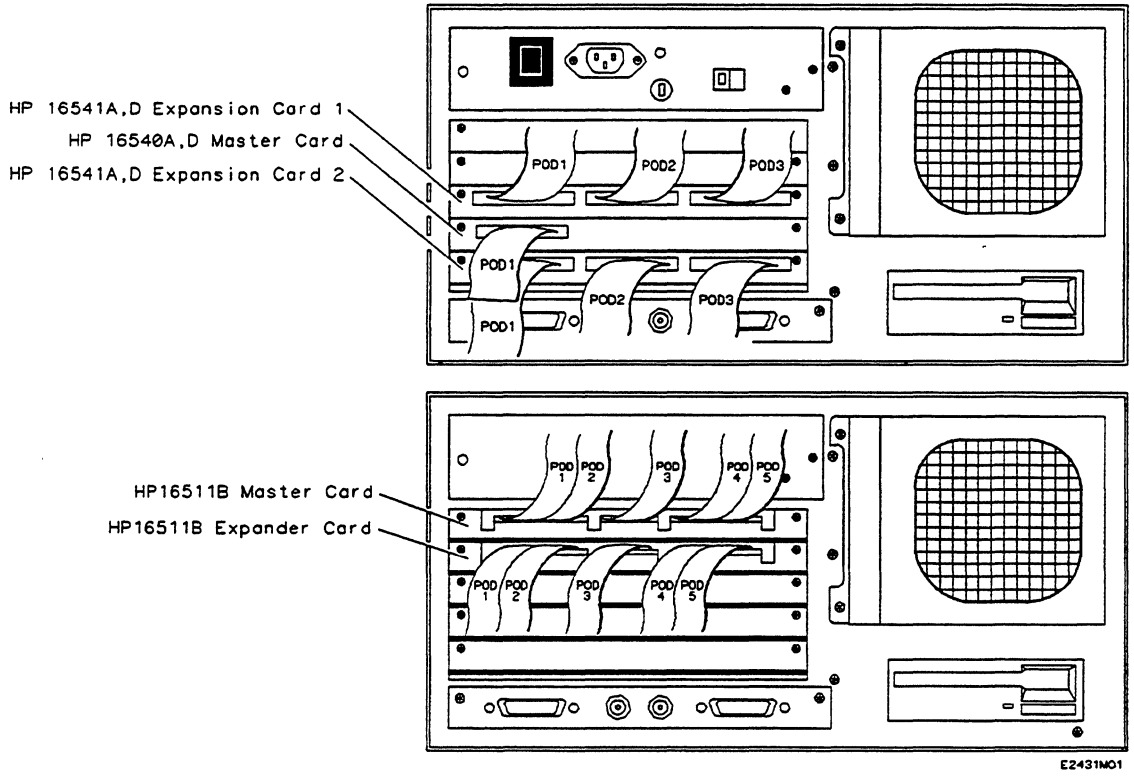


Figure 1-4. Logic Analyzer Card Locations (relative locations, actual slots used may vary)

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for 80386DX analysis by loading the appropriate configuration file. Loading this file will also load the inverse assembler file. The configuration file depends on which logic analyzer you use and which coprocessor your target system is using. Three configuration files can be used with 80386DX systems that use any coprocessor. The other three configuration files should only be used in systems that have an 80287 or 80387 math coprocessor.

To load the configuration file and inverse assembler:

1. Install the flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP 1650 series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500 series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer with the appropriate configuration file (see table 1-2, page 1-10).
4. For HP 16500 series logic analyzers, select the configuration file with the knob, then touch "All" and select the correct module.
5. Execute the load operation to load the file into the logic analyzer.

2

Analyzing the Intel 80386DX

Introduction

This chapter provides reference information on the format specification and symbols configured by the HP 10314D software. It also contains information about the inverse assemblers, status encoding and timing analysis.

Format Specification

The 80386DX configuration files contain predefined format specifications. These format specifications include all labels for monitoring the 80386DX microprocessor and any coprocessors connected directly to the microprocessor (see figures 2-1 and 2-2). There are some slight differences in the displays, according to which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field. Refer to your logic analyzer manual to see which fields and displays are available.

Table 3-1 in chapter 3 lists the 80386DX signals for the HP 10314D Preprocessor Interface and their corresponding lines to the logic analyzers.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field in figures 2-1 and 2-2 should remain in the current selection (> 60 ns) for proper HP 10314D operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

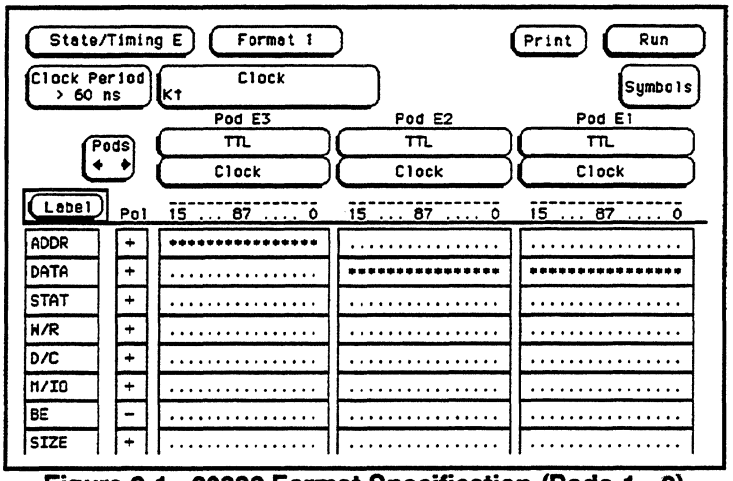


Figure 2-1. 80386 Format Specification (Pods 1 - 3)

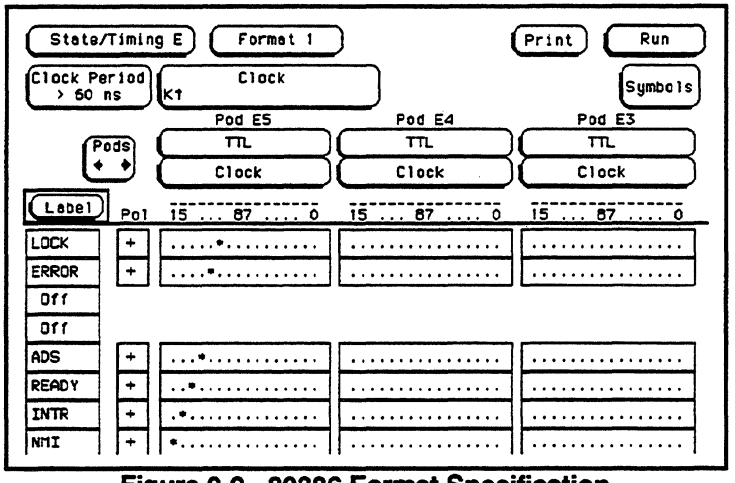


Figure 2-2. 80386 Format Specification (Pods 3 - 5, lower portion of display)

Note

Ten additional labels are listed off the screen. To view these signals, select the Label field and rotate the knob on the front panel clockwise. Figure 2-2 shows some of the lower labels, with the NMI, INTR, READY, and ADS signals selected by jumper (see page 1-4).

Symbols

The HP 10314D configuration software sets up symbol tables on the logic analyzers. The tables contain alphanumeric symbols which identify data patterns or ranges. Additional labels have been defined in the format specification menu to make triggering on specific 80386DX cycles easier. Four of the defined labels are:

- The "STAT" label, which displays 15 status lines.
- The "BE" label, which monitors lines LBE0 to LBE3. These lines indicate valid bytes of the 32-bit data bus during specific transfers.
- The "SIZE" label, which indicates the size of the transfer on the data bus (16-bit or 32-bit transfer).
- The "HALT" label, which differentiates between a HALT cycle caused by executing the HALT instruction and a shutdown caused by protection fault while attempting to process a double fault.

Figures 2-3 and 2-4 show the symbol tables for the STAT and BE labels. Table 2-1 lists the bits assigned to the STAT label. Table 2-2 lists the Status Label encoding for all types of 80386DX microprocessor cycles.

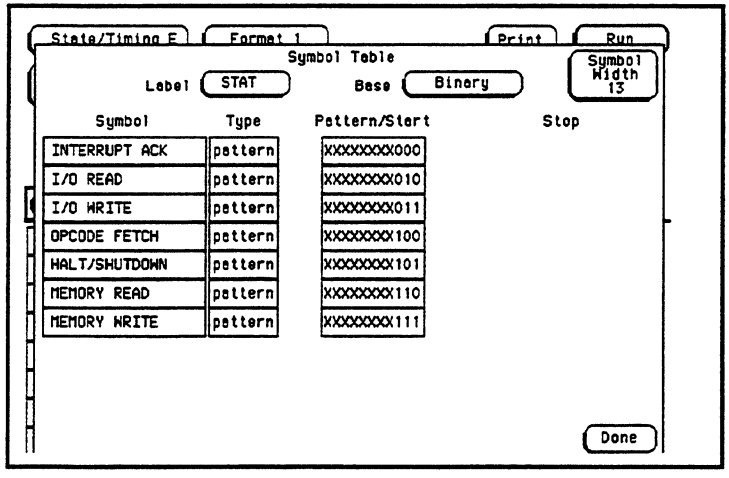


Figure 2-3. Symbol Table for the STAT Label

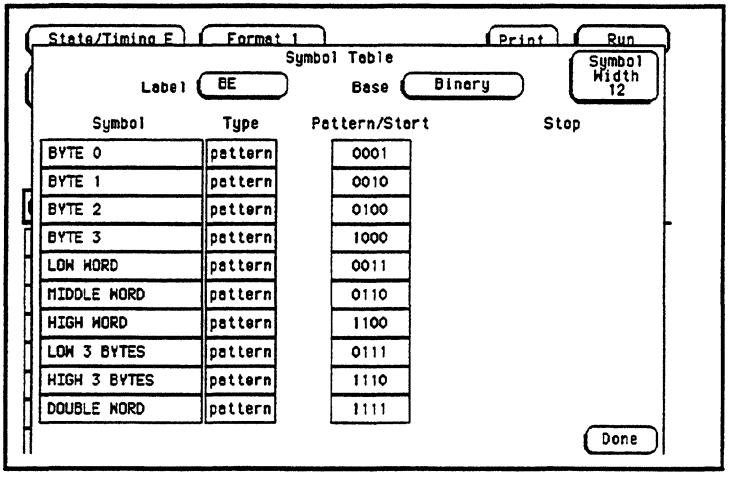


Figure 2-4. Symbol Table for the BE Label

Table 2-1. Description of the Status Bits

Bit	Status Signals	Description
0	D/LC	Signal is high for a data cycle and low for a control cycle.
1	M/LIO	Signal is high for memory and low for I/O.
2	W/LR	Signal is high for a write cycle and low for a read.
3	HLDA	Signal goes high when the microprocessor has relinquished control of the bus.

Table 2-1. Description of the Status Bits (Continued)

Bit	Status Signals	Description
4 - 7	LBE0 - LBE3	Byte Enables with BE0 the least significant byte and BE3 the most significant byte. For opcode fetches, the microprocessor will fetch four bytes unless LBS16 is asserted. When LBS16 is asserted, the microprocessor fetches two bytes.
8	LBS16	If this signal is low for a 16-bit bus cycle, the microprocessor will perform an additional bus cycle if required. For instance, if LBS16 was low during a memory write with all byte enable (LBE) lines low, the microprocessor would perform a second bus cycle using the data from the upper two bytes of the data bus of the first cycle, on the lower two bytes of the data bus for the second cycle.
9	LNA*	When this signal is low it indicates that the system is requesting the next address from the microprocessor.
10	LLOCK	When this signal is low it indicates that the microprocessor has the bus locked to prevent interruption by other bus devices.
11	LERROR*	When this signal is low it indicates that the previous coprocessor instruction generated a coprocessor error.
12	PEREQ*	When this signal is high it requests that the microprocessor perform a data operand transfer for a coprocessor extension.
13	LBUSY*	When this signal is low it indicates the coprocessor is still executing an instruction.
14	LADS*	When this signal is low it indicates a valid bus cycle and address is available on the microprocessor pins.
15	LREADY*	When this signal is low it terminates the bus cycle. This signal is ignored during bus hold acknowledge.

* This signal is used for timing analysis purposes when the HP 10314D is operating in the timing mode.

Table 2-2. Status Field Encoding

80386	Status Bit 10 9 8 7 6 5 4 3 2 1 0
Cycle Type	
Interrupt Acknowledge	x x x x x x x x 0 0 0
I/O Read	x x x x x x x x 0 1 0
I/O Write	x x x x x x x x 0 1 1
Opcode Fetch	x x x x x x x x 1 0 0
Halt/Shutdown	x x x x x x x x 1 0 1
Memory Read	x x x x x x x x 1 1 0
Memory Write	x x x x x x x x 1 1 1
Valid Bytes in Transfer (from LBE0 through LBE3)	
Double Word (all bytes valid)	x x x 0 0 0 0 x x x x
Higher 3 Bytes	x x x 0 0 0 1 x x x x
High Word	x x x 0 0 1 1 x x x x
Byte 3	x x x 0 1 1 1 x x x x
Lower 3 Bytes	x x x 1 0 0 0 x x x x
Middle Word	x x x 1 0 0 1 x x x x
Byte 2	x x x 1 0 1 1 x x x x
Low Word	x x x 1 1 0 0 x x x x
Byte 1	x x x 1 1 0 1 x x x x
Byte 0	x x x 1 1 1 0 x x x x
Size of Transfer	
16-bit Transfer	x x 0 x x x x x x x x
32-bit Transfer	x x 1 x x x x x x x x

Note: X = don't care. The actual status field is a 15 bit field; however, bits 11 through 14 are not shown since they are "don't cares."

Listing Menu

Captured data is displayed in the Listing menu as shown in figure 2-5. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

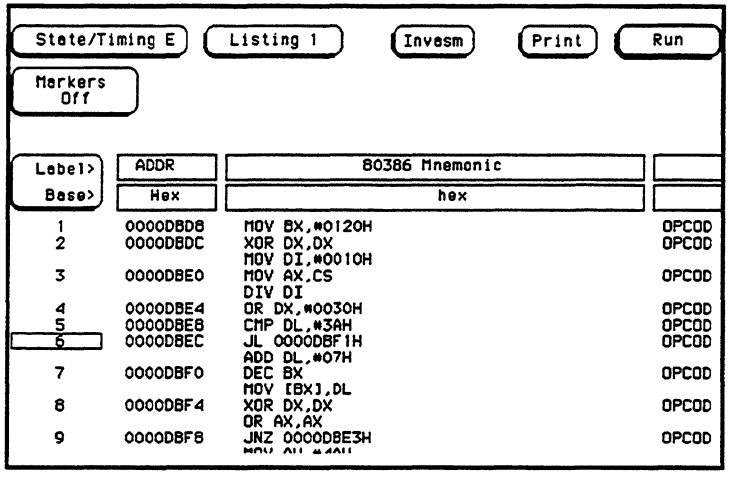


Figure 2-5. Listing Menu for the 80386

Note

If your state trace doesn't appear to be correct (capturing the same RAM address twice, for example), make sure the state/timing switch is in the state position. If it is not in the proper position, place it in the state position and run the trace again.

An incorrect state trace may also result from system noise causing the internal clock of the preprocessor interface to become out of phase with the internal clock of the 80386DX. To get the HP 10314D back in synchronization with the 80386DX, reset the target system and run the trace again.

The 80386DX Inverse Assemblers

The 80386DX inverse assemblers have been designed to support the 80386DX microprocessor with or without coprocessors. The following paragraphs explain the operation of the inverse assemblers and the results you can expect in certain conditions.

The 80386DX microprocessor can fetch instructions up to 4 bytes (32 bits) wide in a single bus cycle. However, the microprocessor does not indicate externally which of the bytes fetched is the first byte of a code fetch. You must "point" to the first byte of an instruction fetch. Once synchronized, the inverse assembler will disassemble from this state through the end of the screen.

In addition, the 80386DX microprocessor can execute two types of object code. The 80386DX can execute the 80386DX instruction set (32-bit), and it can also execute object code from Intel's 16-bit microprocessor family, including software designed for the Intel 8086 and the Intel 80286. The user must tell the logic analyzer what "size" of code is being executed by the microprocessor.

Note

Size, as used here, has no relationship to the physical size of the microprocessor's data bus. In this reference, size is used to indicate whether the code being executed was originally designed to run on Intel's 16-bit or 32-bit microprocessors.

To point to the first byte of a code fetch and to indicate the size of the opcode, do the following:

1. Identify a line on the display that you know contains the first byte of an instruction fetch.
2. Roll this line to the top of the listing.

Note 

The cursor location is not the top of the listing. In figure 2-5, line 1 is the top of the listing.

---

3. Select the "Invasm" field at the top of the display. A pop-up will appear with the following choices:

   Size 16 Byte 0
   Size 16 Byte 1
   Size 16 Byte 2
   Size 16 Byte 3
   Size 32 Byte 0
   Size 32 Byte 1
   Size 32 Byte 2
   Size 32 Byte 3

4. Select the field in this pop-up that describes which byte of the captured state contains the first byte of the code fetch and what kind of object code is being executed by the microprocessor (Size 16 or 32 for Intel's 16- or 32-bit microprocessor families).

The listing will inverse assemble from the top line down. Any data before this screen is left unchanged. Rolling the screen up will inverse assemble the lines as they appear on the bottom of the screen. If you jump to another area of the screen by entering a new line number, you must re-synchronize the inverse assembler by repeating the above steps.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but the activity between those blocks will not be inverse assembled.

Interpreting Data

Unless followed by a lower-case letter, all numeric output from the inverse assembler is in hexadecimal format. Decimal values are indicated by a lower-case "d" (as in the INT instruction).

Up to four instructions may be displayed for a single analyzer state because the 80386DX can fetch a double word with four instruction bytes from program memory. If the least significant byte of this double word contains a single-byte instruction, the next sequential instruction begins in the next higher byte. This process continues from the least significant byte to the most significant byte until all of the bytes of the fetched double word are used. When a single state contains more than one instruction, each instruction will be displayed on a separate line. For example:

```
+0015    =NEG ECX                              OPCODE FETCH
         =MOV BYTE PTR [EBP][-1BH].CL
+0016    =XXXXXXDAH  READ MEM                  MEMORY READ
```

Line number +0015 displays two instructions from a double-word.

Since instructions may begin in any byte position, the last bytes of a multiple-byte instruction may extend into the lower bytes of the next double word fetched. In this instance, the next sequential instruction begins in the next higher byte of the next double-word after the previous instruction and operands. When interpreting a given state, the inverse assembler will ignore bytes used by a previous instruction and will only display the instructions that begin in that state. For example:

Byte Position 3	2	1	0	
01	20	BB	24	Single byte instruction MOV BX (BB) starts in byte 1.
10	BF	D2	31	Double byte instruction XOR DX,DX (31D2) begins in byte 0 and continues into byte 1. Next instruction MOV DI (BF) begins in byte 2.
F7	C8	8C	00	Double byte instruction DIVDI (F7F7) starts in byte 3 and continues into byte 0 of next double word fetched.
30	CA	81	F7	Next instruction ORDX (81CA) begins in byte 2 immediately after last instruction.

Asterisks (*) in the inverse assembler output indicate that a portion (or portions) of an instruction was not captured by the analyzer. Missing opcodes occur frequently and are primarily due to microprocessor

prefetch activity. Storage qualification, or the use of storage windows, can also lead to such occurrences.

The 80386DX has two possible default operand/address sizes, 16 or 32 bits. This attribute is set when a code segment descriptor is loaded, and is impossible for the inverse assembler to detect. Therefore, it must be declared manually by selecting the correct field under the "Invasm" pop-up. Any instruction with an operand size of 32 bits (either by default, or by using the operand override prefix) will be marked with an " = " symbol in the first column of the 80386DX mnemonic field to help you distinguish 32-bit operands from 16-bit operands.

If the inverse assembler seems to be disassembling incorrectly, and the problem is neither prefetch activity nor storage qualification, it is likely that the size attribute is set incorrectly.

The 80386DX microprocessor can perform byte, word, and three-byte transfers, as well as double-word transfers between microprocessor registers and memory. Byte transfers can occur in any byte on the 32-bit data bus. Word and three-byte transfers can occur across any contiguous set of bytes that will hold the transfer. The bytes that are valid in a transfer are indicated by the microprocessor LBE0 through LBE3 lines. The inverse assembler will display "xx" (don't care) for the bytes of a transfer that are ignored by the microprocessor. In this way it is possible to determine exactly which bytes were used by the microprocessor. For example:

xxxxxDBH	read memory	(Byte transfer on byte 0)
xxxx28xxH	read memory	(Byte transfer on byte 1)
xxB3xxxxH	read memory	(Byte transfer on byte 2)
ECxxxxxxH	read memory	(Byte transfer on byte 3)
xxxx28DBH	read memory	(Word transfer on lower word)
xxB328xxH	read memory	(Word transfer on middle word)
ECB3xxxxH	read memory	(Word transfer on upper word)
xxB328DBH	read memory	(3-byte transfer on lower three bytes)
ECB328xxH	read memory	(3-byte transfer on upper three bytes)
ECB328DBH	read memory	(Double-word transfer)

Physical, rather than logical addresses, are used to perform symbolic address mapping. Most instructions, however, specify a 32-bit intrasegment offset and may indicate a segment different from the default segment for that particular instruction. Since the physical address cannot be determined from this information alone, the inverse assembler must attempt to locate the resulting bus cycle so that the physical address may be obtained. If a bus cycle of the type indicated by the initiating instruction is not found, the physical address cannot be determined and an unmapped logical address (segment override, if any, and the 32-bit intrasegment offset) is displayed instead of a mapped physical address.

Error Messages

Any of the following list of error messages may appear during analysis of your target software. Included with each message is a brief explanation.

Illegal Task Request	Displayed if the inverse assembler is used with an instrument other than the supported logic analyzers.
Fatal Data Error	Displayed if the trace memory could not be read properly on entry into the inverse assembler.
Invalid Status	Displayed if the status field for the current state is not valid.
Illegal Opcode	Displayed if the inverse assembler encounters an illegal 80386DX instruction.
Reserved Opcode	Displayed if the I80386_87 inverse assembler encounters a reserved coprocessor instruction.
No Operand	Displayed if the inverse assembler cannot find a complete operand field for an instruction. Prefetch activity or storage qualification is often the cause.

Coprocessor Support

The HP 10314D Preprocessor Interface fully supports the 80287 and 80387 math coprocessors. Using the configuration files which end in "_87," the math coprocessor instructions are inverse assembled and all operand transfers are decoded as I/O reads and writes. When using the configuration files which end in "_I," the inverse assembler will not attempt to inverse assemble coprocessor instructions. Instead, it will display an ESC and the hexadecimal data that followed it.

Instruction Decoding

The HP 10314D Preprocessor Interface will send all of the bus transactions by both the microprocessor and coprocessor to the logic analyzer. The time count will accurately reflect when the end of the bus cycle occurred. No distinction is made between instructions that are executed and those that are only prefetched by the microprocessor. Typically, several states separate the memory (or I/O) transfer from the instruction that caused the transfer.

The logic analyzer is clocked once each bus cycle. The preprocessor interface hardware ensures that the logic analyzer will reliably capture the address, data, and status information during both pipelined and non-pipelined cycles by latching this information during the current bus cycle and sending it to the logic analyzer during the succeeding bus cycle. See the "Preprocessor Interface Description" section in chapter 3 for complete details of this process.

Additional Information on Instruction Decoding

A 32-bit memory cycle on a 16-bit bus is sent to the logic analyzer as two bus transactions.

The preprocessor interface stops generating logic analyzer clocks when the 80386DX asserts HLDA. Bus cycles that assert HLDA, such as DMA cycles, will not be captured by the logic analyzer.

To disable the HLDA line from stopping the logic analyzer clocks, move the jumper on J9 to the ON position (see figure 2-6). This will bypass the HLDA control on the preprocessor interface leaving the preprocessor interface active (ON) for all bus cycles.

Note 

The ADS and READY lines must be operating in normal 80386DX bus cycles when the HLDA line is disabled. If these lines are not present during the HLDA (hold acknowledge) period, the preprocessor interface will not remain in step with following bus cycles. This will result in incorrect capturing of data.

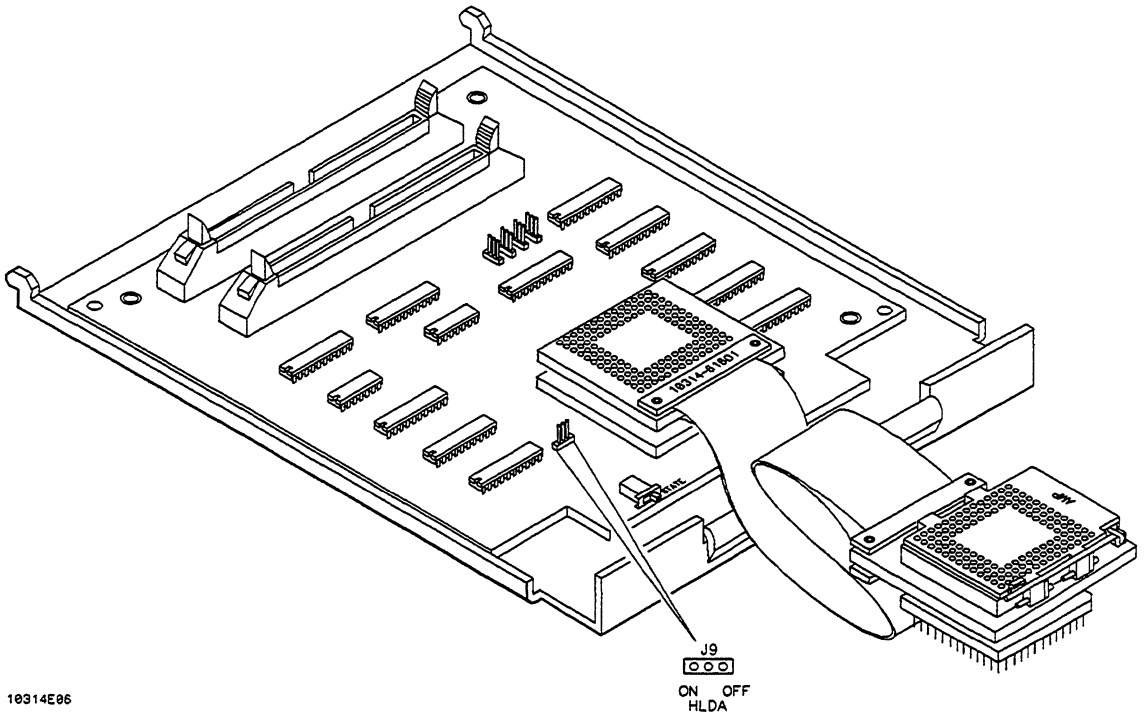


Figure 2-6. HLDA Jumper J9

Timing Analysis

The same format specification loaded for state analysis is also used for timing analysis. To configure the logic analyzer for timing analysis:

1. Move the State/Timing switch (S1) on the preprocessor interface board to the timing position (see figure 1-1, page 1-5).
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field for the 80386DX analyzer and select Timing (see figure 2-7).

Note

BS16 and RESET are not available for timing analysis.

BS16 appears on the format specification, but is not accurate for timing analysis because it is delayed by an edge-triggered latch on the preprocessor interface board.

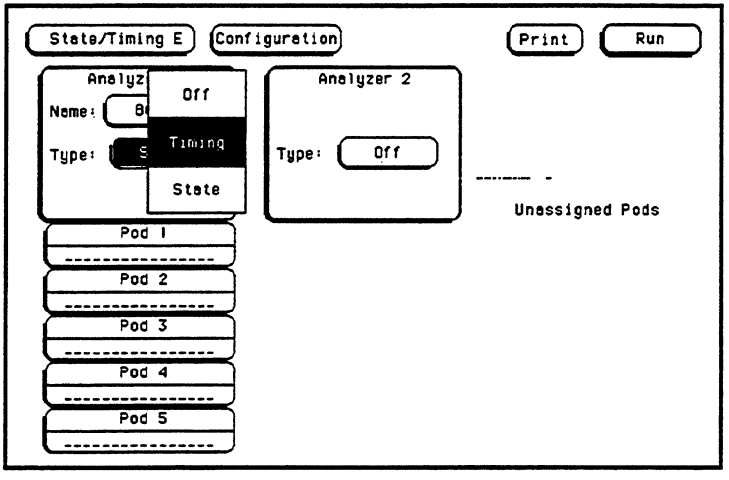


Figure 2-7. Setting Machine 1 to Timing

Timing Format Specification

When the preprocessor interface is used for timing analysis, the format specification will be set up as shown in figures 2-8 and 2-9.

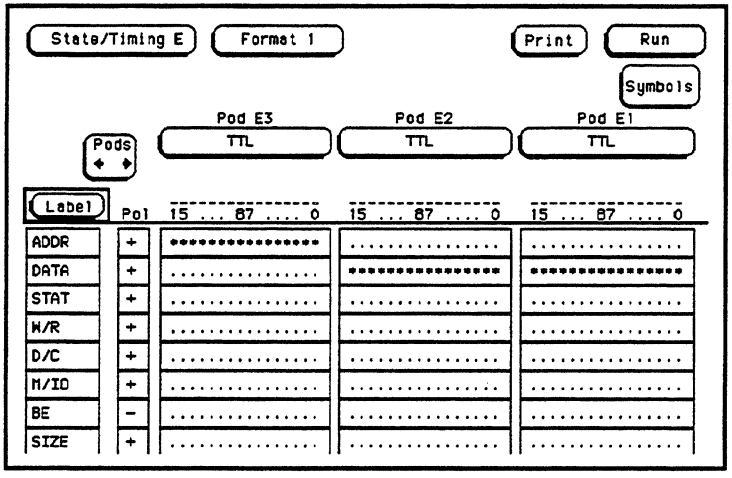


Figure 2-8. Timing Format Specification (Pods 1-3)

Note

The timing format specification has ten additional labels which are listed offscreen. To view these signals, select the Label field and rotate the knob on the front panel clockwise.

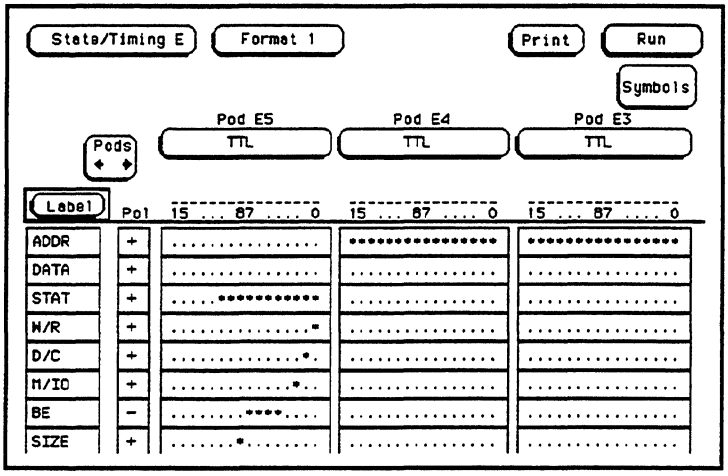


Figure 2-9. Timing Format Specification (Pods 3-5)

Waveforms Menu

Captured data is displayed in the Waveforms menu as shown below.

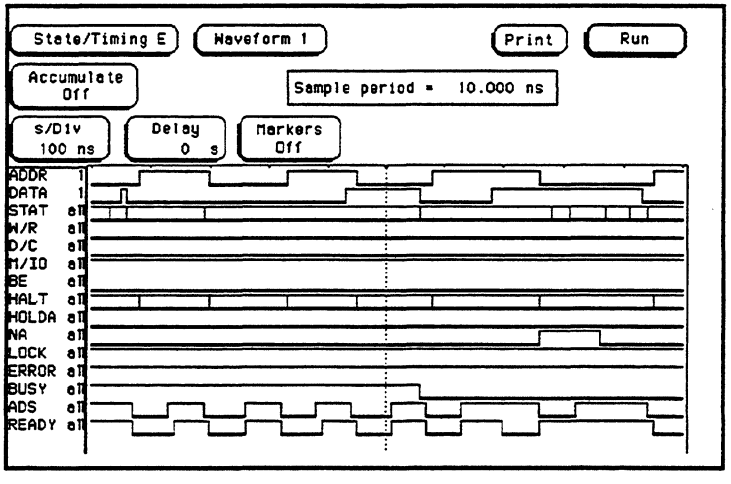


Figure 2-10. Waveforms Display

3

General Information

Preprocessor Interface Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP 10314D Preprocessor Interface. These characteristics are included as additional information for the user.

Microprocessor Compatibility: Intel 80386DX and all microprocessors made by other manufacturers that comply with Intel 80386DX specifications.

CPU Package Supported: 132-pin PGA

Accessories Required: HP 10269C

Maximum Clock Speed: 33 MHz clock output (CLK); 66 MHz clock input (CLK2)

Note 

For the following logic analyzers, the data must be valid for 10 ns before READY is sampled with the rising edge of CLK2: HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B.

State Speed: Four CLK2 cycles per bus cycle.

Maximum Analyzer Clock Speed: 16.5 MHz state speed with CLK2 at 66 MHz.

Signal Line Loading: 1 "F" TTL load plus approximately 45 pF on the following lines:

D0-D31

1 "F" TTL load plus approximately 50 pF on the following lines:

A2-A31, LBS16, LREADY, LLOCK, D/LC, M/LIO, W/LR, LBE0-LBE3

2 "F" TTL loads plus approximately 60 pF on the following line:

HLDA

2 "F" TTL loads plus approximately 70 pF on the following line:

LRESET

1 "F" TTL loads plus approximately 20 pF on the following lines:

CLK2, LADS

Note 

Because of capacitive loading, the HP 10314D may not be compatible with target systems that extensively use CMOS devices.

Microprocessor Operations Displayed:

Memory Read/Write
I/O Read/Write
Opcode Fetch
Interrupt Acknowledge Type 0-255
Halt
Shutdown
80287 or 80387 Coprocessor Operations

Timing Analysis: All signals are buffered except the following signals:

LNA, LERROR, PEREQ, LBUSY, INTR, NMI, and LREADY

Up to 8 ns of skew may exist between the buffered signals and the following signals:

LNA, LERROR, PEREQ, LBUSY, INTR, NMI, and LREADY

Less than 5 ns skew exists between buffered signals.

Power Requirements: 1.0 A at +5 Vdc maximum, supplied by the logic analyzer.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, or HP 16550A

Number of Probes Used: Five 16-channel probes

Environmental Temperature:	Operating:	0 to +55 degrees C (+32 to +131 degrees F)
	Nonoperating:	-40 to +75 degrees C (-40 to +167 degrees F)
Altitude:	Operating:	4600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Preprocessor Interface Description

The primary function of the HP 10314D Preprocessor Interface is to connect the target microprocessor to the logic analyzer through the probe interface, and to perform the interface logic required to identify address pipelining and 16 or 32-bit cycles. The HP 10314D Preprocessor Interface performs this primary function by:

1. Latching and buffering the address, status, and data bus of the 80386DX microprocessor so that address, status, and data can be sent to the logic analyzer at the same time.
2. Generating the logic analyzer clock from the appropriate 80386DX microprocessor signals and bus conditions.
3. Synthesizing address lines A0 and A1 from the LBE0 through LBE3 lines so that the inverse assembler can identify the address for A0 and A1.

The preprocessor interface duplicates the internal CLK signal of the 80386DX by dividing the CLK2 signal by 2 and selecting the correct phase of the resulting signal. This signal is called CLK and is used to identify 80386DX activities inside the PAL on the HP 10314D.

The J and K clocks for latching information into the logic analyzer are generated by the PAL on the HP 10314D each time the LREADY signal goes low.

Figure 3-1 shows a block diagram of the HP 10314D Preprocessor Interface.

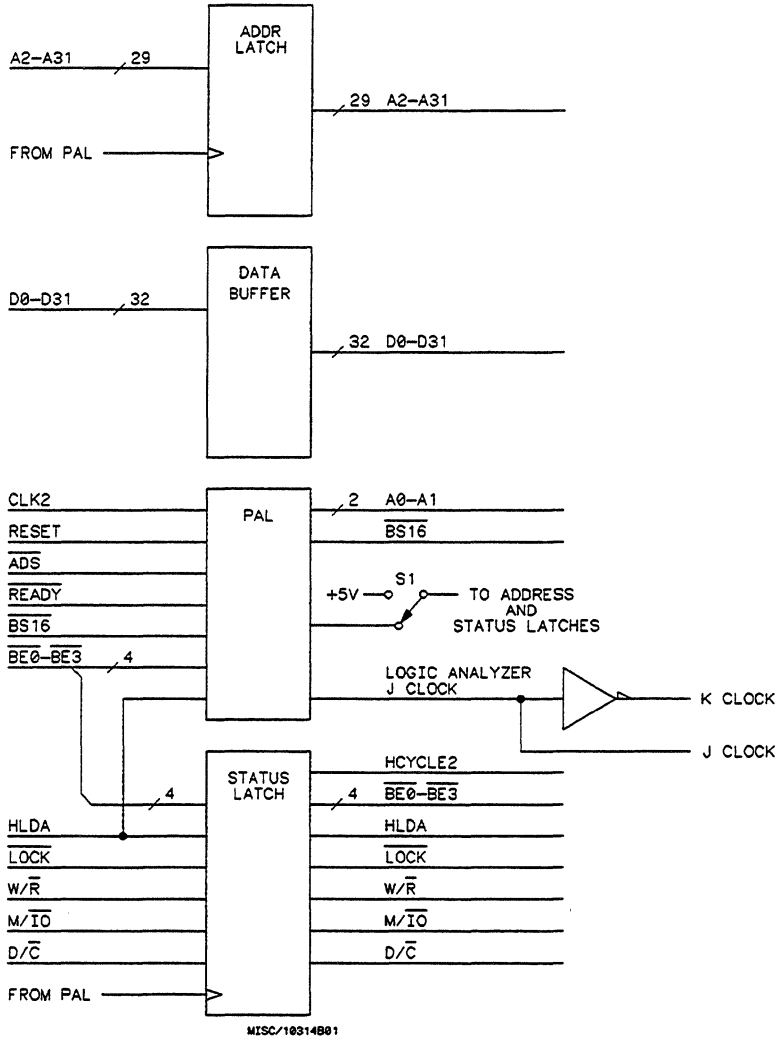


Figure 3-1. HP 10314D Block Diagram

The preprocessor interface detects the start of an 80386DX bus cycle when LADS goes true. The preprocessor interface latches address and status on the following conditions:

- If the 80386DX cycle is a non-pipelined cycle, address and status are latched during the time that ADS is low.
- If the 80386DX cycle is a pipelined cycle, address and status are latched during the first CLK2 cycle after READY is detected low.

Data is latched at the end of the 80386DX cycle. The end of the bus cycle is defined as the rising edge of CLK2 when CLK is high and LREADY is low. The clock for the logic analyzer is generated approximately 8 ns after the end of the cycle.

If J9 is in the OFF position, the logic analyzer clock is suppressed when HLDA is asserted.

Figure 3-2 is the schematic for the HP 10314D. The pin numbers for connector XW1 on the schematic refer to the cable socket on the preprocessor interface board. Table 2-1 lists the pin numbers for the preprocessor interface board socket (XW1) and the corresponding pin numbers (CPU Pin) on the target side of the preprocessor interface cable.

Notice 

The schematics on pages 3-6 through 3-10 are supplied only as an aid to understanding circuit preprocessor interface characteristics. They are not intended to be used as a service or troubleshooting aid. These schematics are NOT subject to a revision or change program to keep them current or accurate. ACCORDINGLY, HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY ARISING FROM THE USE OF THESE SCHEMATICS.

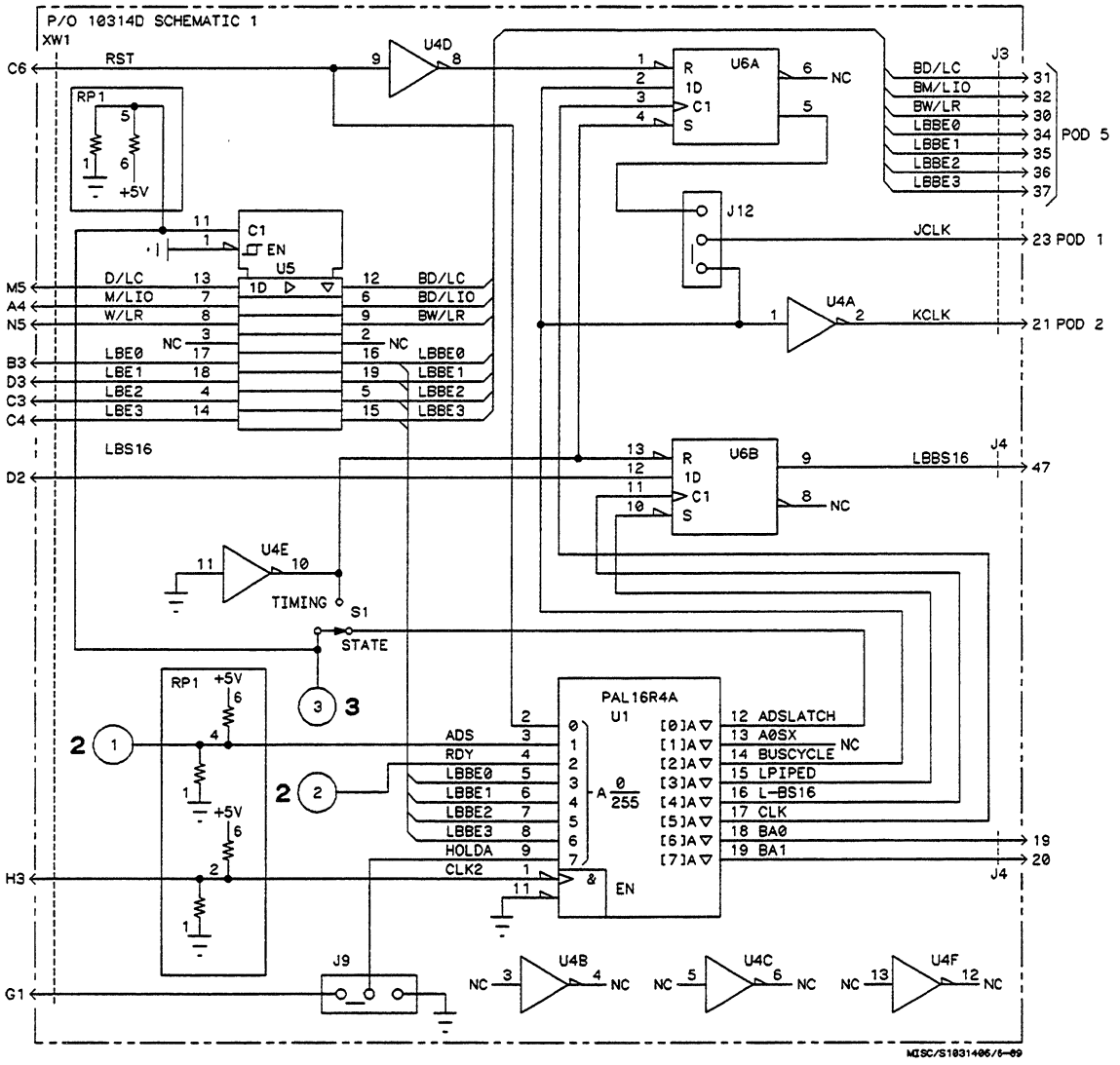


Figure 3-2. HP 10314D Schematic

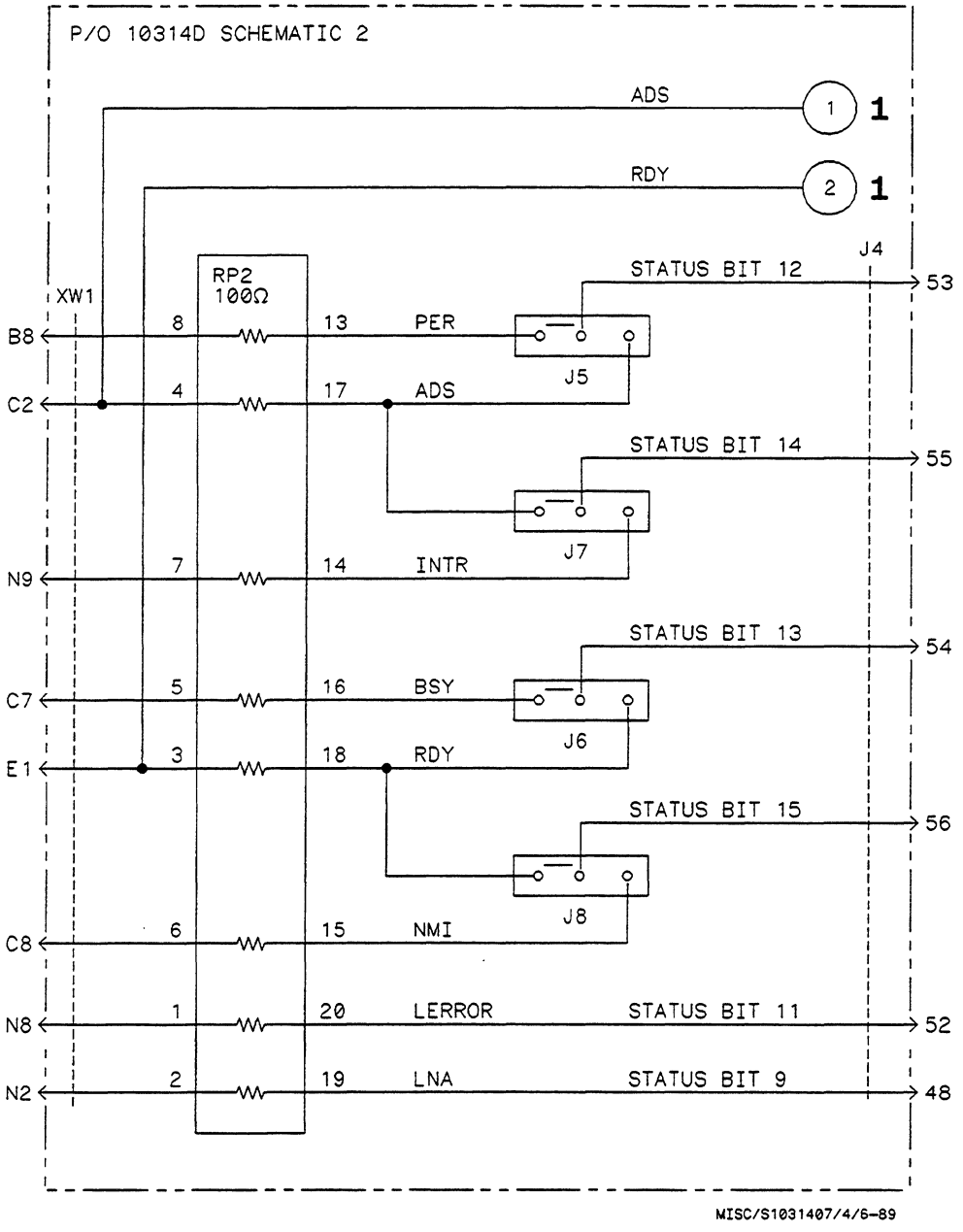


Figure 3-2. HP 10314D Schematic (continued)

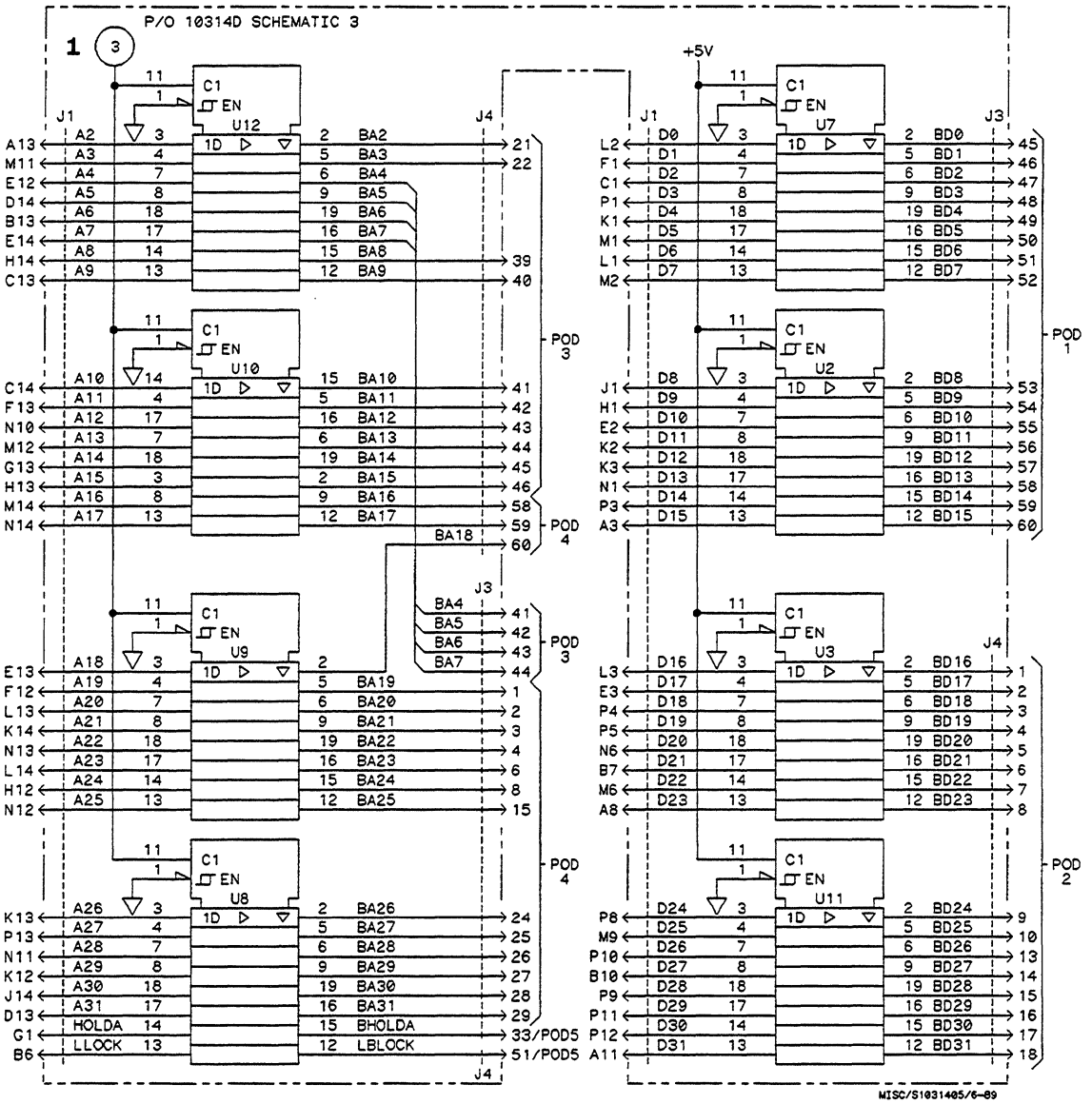
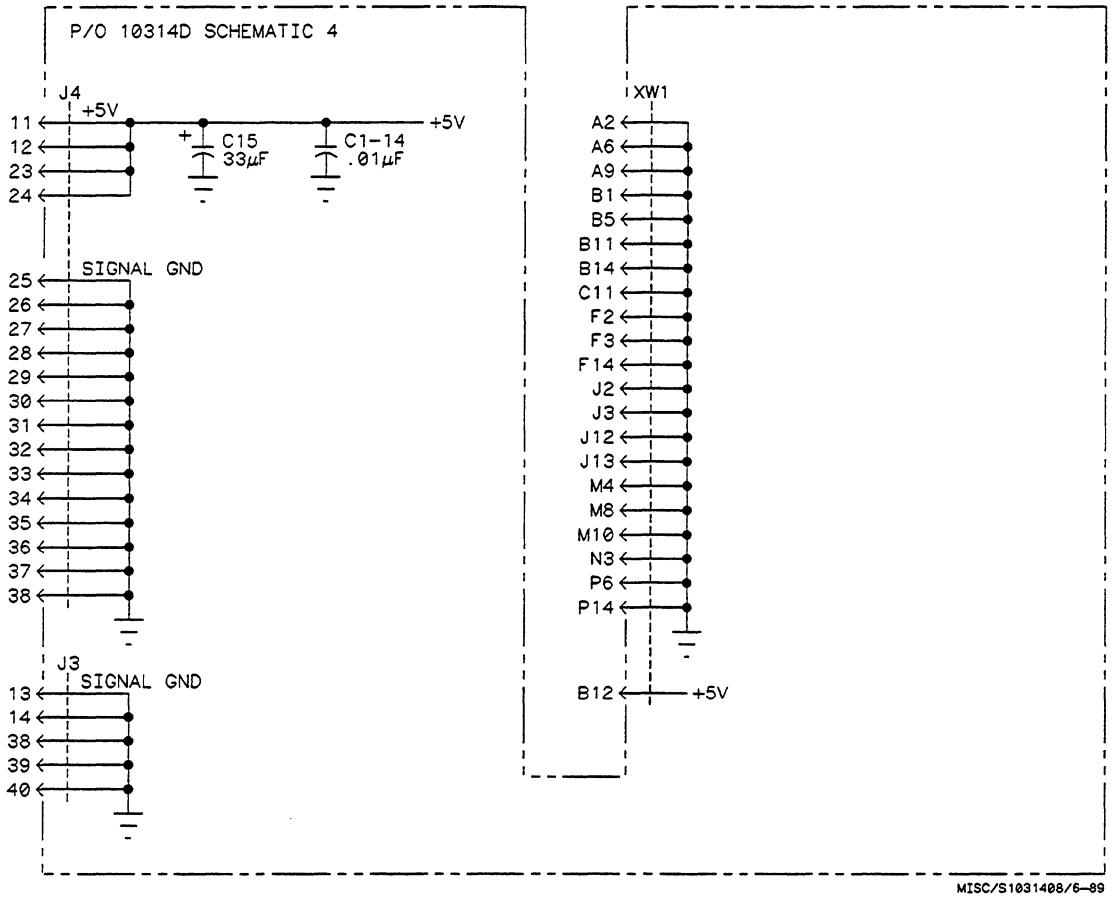


Figure 3-2. HP 10314D Schematic (continued)



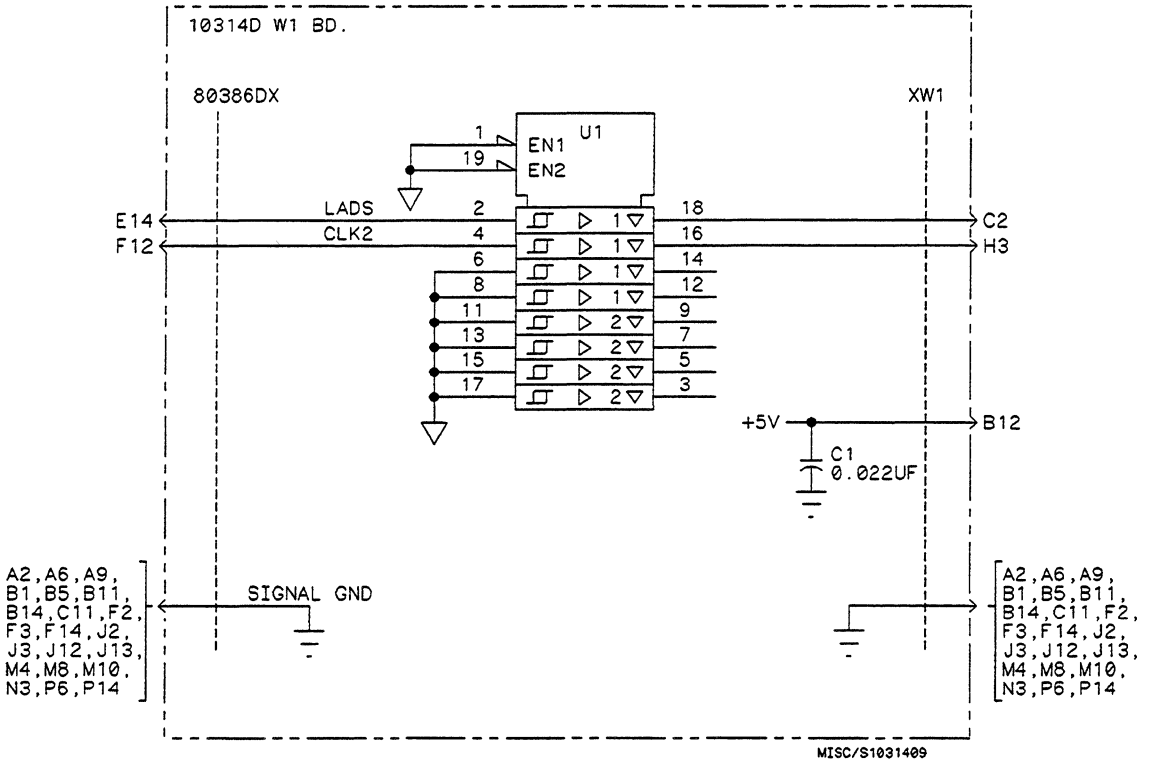
IC DEVICE POWER CONNECTIONS
FOR SCHEMATICS 1,3

SUPPLY	PIN NO.	IC GROUP
+5V GND	20 10	U1-3,5, 7-12
+5V GND	14 7	U4,6

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
RP1 RP1 RP2	180Ω 390Ω 100Ω	6 1	+5V GND

PARTS ON SCHEMATICS 1-4	
C1-15	
J3-9,12	
RP1,2	
U1	16R4
U2,3,5,7-12	74F373
U4	74F04
U6	74F74
XW1	

Figure 3-2. HP 10314D Schematic (continued)



IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5V	20	U1
GND	10	

PARTS ON SCHEMATIC
U1 74F244
C1

Figure 3-3. Cable W1 Board Schematic

Table 3-1 lists the 80386DX signals and their corresponding lines to the HP 10269C General Purpose Probe Interface. The "XW1 Pin" column lists the pin numbers for the preprocessor interface board socket (XW1) and the "CPU Pin" column lists 80386DX pin numbers.

Table 3-1. 80386 Signal List

CPU Signal	CPU Pin	XW1 Pin	Label	HP 10269C	
				Pod	Bit
A0	*	--	ADDR	3	0
A1	*	--	ADDR	3	1
A2	C4	A13	ADDR	3	2
A3	A3	M11	ADDR	3	3
A4	B3	E12	ADDR	3	4
A5	B2	D14	ADDR	3	5
A6	C3	B13	ADDR	3	6
A7	C2	E14	ADDR	3	7
A8	C1	H14	ADDR	3	8
A9	D3	C13	ADDR	3	9
A10	D2	C14	ADDR	3	10
A11	D1	F13	ADDR	3	11
A12	E3	N10	ADDR	3	12
A13	E2	M12	ADDR	3	13
A14	E1	G13	ADDR	3	14
A15	F1	H13	ADDR	3	15
A16	G1	M14	ADDR	4	0
A17	H1	N14	ADDR	4	1
A18	H2	E13	ADDR	4	2
A19	H3	F12	ADDR	4	3
A20	J1	L13	ADDR	4	4
A21	K1	K14	ADDR	4	5
A22	K2	N13	ADDR	4	6
A23	L1	L14	ADDR	4	7

* Derived from LBE0 through LBE3

Table 3-1. 80386DX Signal List (continued)

CPU Signal	CPU Pin	XW1 Pin	Label	HP 10269C	
				Pod	Bit
A24	L2	H12	ADDR	4	8
A25	K3	N12	ADDR	4	9
A26	M1	K13	ADDR	4	10
A27	N1	P13	ADDR	4	11
A28	L3	N11	ADDR	4	12
A29	M2	K12	ADDR	4	13
A30	P1	J14	ADDR	4	14
A31	N2	D13	ADDR	4	15
D0	H12	L2	DATA	1	0
D1	H13	F1	DATA	1	1
D2	H14	C1	DATA	1	2
D3	J14	P1	DATA	1	3
D4	K14	K1	DATA	1	4
D5	K13	M1	DATA	1	5
D6	L14	L1	DATA	1	6
D7	K12	M2	DATA	1	7
D8	L13	J1	DATA	1	8
D9	N14	H1	DATA	1	9
D10	M12	E2	DATA	1	10
D11	N13	K2	DATA	1	11
D12	N12	K3	DATA	1	12
D13	P13	N1	DATA	1	13
D14	P12	P3	DATA	1	14
D15	M11	A3	DATA	1	15
--	--	--	ANALYZER CLOCK	1	J CLK
D16	N11	L3	DATA	2	0
D17	N10	E3	DATA	2	1
D18	P11	P4	DATA	2	2
D19	P10	P5	DATA	2	3

Table 3-1. 80386DX Signal List (continued)

CPU Signal	CPU Pin	XW1 Pin	Label	HP 10269C	
				Pod	Bit
D20	M9	N6	DATA	2	4
D21	N9	B7	DATA	2	5
D22	P9	M6	DATA	2	6
D23	N8	A8	DATA	2	7
D24	P7	P8	DATA	2	8
D25	N6	M9	DATA	2	9
D26	P5	P10	DATA	2	10
D27	N5	B10	DATA	2	11
D28	M6	P9	DATA	2	12
D29	P4	P11	DATA	2	13
D30	P3	P12	DATA	2	14
D31	M5	A11	DATA	2	15
W/LR	B10	N5	STAT	5	0
D/LC	A11	M5	STAT	5	1
M/LIO	A12	A4	STAT	5	2
HLDA	M14	G1	STAT	5	3
LBE0	E12	B3	STAT	5	4
LBE1	C13	D3	STAT	5	5
LBE2	B13	C3	STAT	5	6
LBE3	A13	C4	STAT	5	7
LBSI6	C14	D2	STAT	5	8
LNA	D13	N2	STAT	5	9
LLOCK	C10	B6	STAT	5	10
LERROR	A8	N8	STAT	5	11
PEREQ	C8	B9	STAT	5	12
LBUSY	B9	C7	STAT	5	13
LADS	E14	C2	STAT	5	14
LREADY	G13	E1	STAT	5	15
--	--	--	ANALYZER CLOCK	2	K CLK

Servicing

The repair strategy for the HP 10314D is board replacement. However, table 3-2 lists the cables and some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

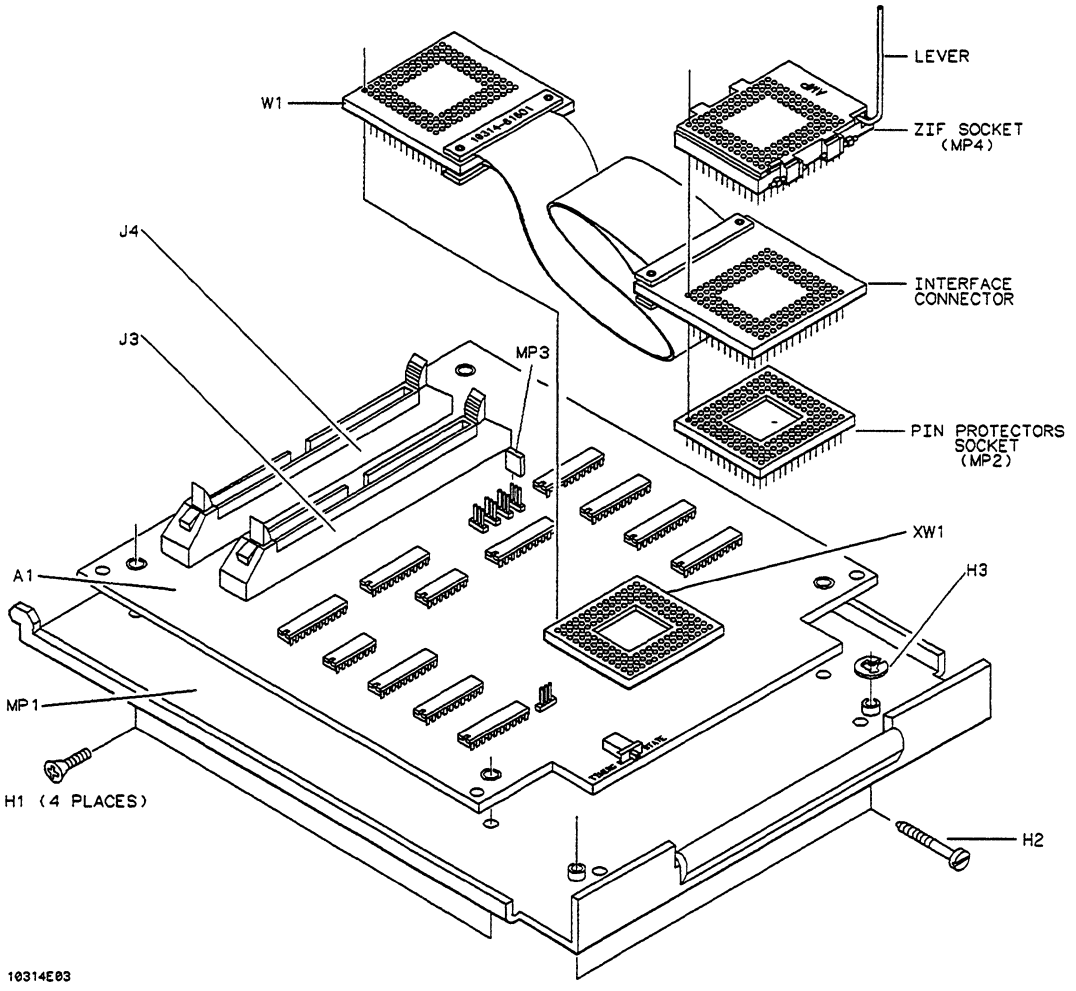


Figure 3-4. HP 10314D Exploded View

Table 3-2. HP 10314D Parts List

Reference Designator	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
--	10314-68705	1	80386DX Disk Pouch	28480	10314-68705
--	10314-90915	1	User's Guide	28480	10314-90915
A1	10314-66505	1	10314D Preprocessor Board	28480	10314-66505
H1	2200-0512	4	Screw 4-40 .312	28480	2200-0512
H2	1390-0393	2	TS Screw Captive	28480	1390-0393
H3	0510-0952	2	Ring-Retainer .094	28480	0510-0952
J3	1251-7575	1	Conn-Post Type .100-Pin-Spcg 60-Cont	28480	1251-7575
J4	1251-7575	1	Conn-Post Type .100-Pin-Spcg 60-Cont	28480	1251-7575
MP1	10314-04102	1	Cover-Bottom	28480	10314-04102
MP2	1200-1506	1	Pin Protector	L9103	PGA132H002B1-1414P
MP3	1258-0141	5	Jumper-Removable for .025-IN-Sq-Pins	28480	1258-0141
MP4	1200-1357	1	Socket-IC ZIF 132-Cont Sqr DIP-SLDR	28480	1200-1357
W1	10314-61601	1	80386 Preprocessor Cable	28480	10314-61601
XW1	1200-1506	1	Pin Protector	L9103	PGA132H002B1-1414P

Table 3-3. List of Manufacturer's Codes

Mfr Code	Manufacturer Name	Address	Zip Code
28480	Hewlett-Packard Co. Corporate HQ	Palo Alto, Ca	94304
L9103	McKenzie Technology	Fremont, Ca	94538

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

HP 16540/16541A,D State:

The HP 16540/16541A,D Master Card is not receiving any clocks.

- Ensure that the target system is On.
- Ensure that connector Pod 1 of the HP 10269C is connected to pod 1 of the Master Card.

HP 16511B State:

The HP 16511B expander card is not receiving state clocks. Ensure that the pod 2 cable from the expander (lower) HP 16511B card is connected to the HP 10269C Pod 2.

HP 1650A,B, HP 16510A,B, or HP 1652B State:

The logic analyzer is not receiving state clocks.

- Ensure that the pod 2 cable from the logic analyzer is connected to the HP 10269C Pod 2.
- Ensure that your target system is running properly.
- For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

Slow Clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP 10269C and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1, next page).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.

- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

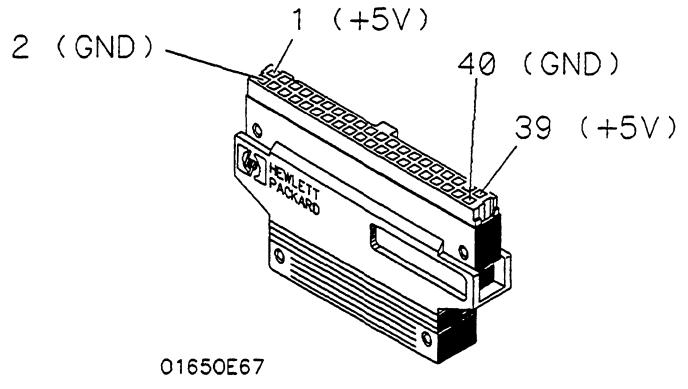


Figure A-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that the memory manager has been disabled. In most cases, if the microprocessor memory manager remains enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. The following techniques will reduce the capacitive loading:

- Remove as many pin protectors, extenders, and adapters as possible.
- If multiple preprocessor interface solutions are available, try using one with lower capacitive loading.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem. Check the circuitry for the state clock delay signal (STCLK) as described in "Slow or Missing Clock."

Note

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, or with the HP 16540/16541A,D, Logic Analyzer, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/16541A,D)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D and HP 16541A,D cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.