

User's Guide

HP E2418A
TI TMS32020/C25
Preprocessor Interface

HP E2418A TI TMS32020/C25 Preprocessor Interface User's Guide

**for the HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A,
HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A
Logic Analyzers**



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Introduction

The HP E2418A Preprocessor Interface provides a complete interface for monitoring external bus operations of a TMS32020/C25 target system with the following logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A.

Since the HP E2418A only monitors external bus operations of the TMS32020/C25, the TMS32020/C25 must be operated in the "microprocessor" mode (versus the "microcomputer" mode). In microprocessor mode, the bus operations to the external program memory are available to be captured by the logic analyzer. Accesses to TMS32020/C25 internal resources are not presented on the external data bus.

The TMS32020/C25 configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the TMS32020/C25 microprocessor. It also loads the inverse assembler for obtaining displays of TMS32020/C25 data in TMS32020/C25 assembly language mnemonics.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2418A Preprocessor Interface:

HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 1660A/61A/62A

The HP 1660A/61A/62A Logic Analyzers provide 4 k of memory depth with 136 channels (HP 1660A), 102 channels (HP 1661A), or 68 channels (HP 1662A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis, or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with one HP 16541A,D Expansion Card

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with up to 64 channels of 100 MHz state or timing analysis.

HP 16542A (Master Card and two expansion cards)

This logic analyzer combination provides 1 M of memory depth with 48 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2418A Preprocessor Interface for state analysis with the supported logic analyzers.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2418A software. It also provides information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2418A Preprocessor Interface. It also contains information on servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

Setting Up the HP E2418A

Introduction

This chapter explains how to install and configure the HP E2418A Preprocessor Interface for state analysis of external bus operations with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2418A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2418A master disk. Store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

Equipment Supplied

The HP E2418A Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card.
- The inverse assembly software on a 3.5-inch disk.
- Three 100 kOhm Termination Adapters (HP part number 01650-63203).
- This user's guide.



The preprocessor interface socket assembly pins are covered at the time of shipment with either a conductive foam wafer or a conductive plastic pin protector. This is done to protect the delicate gold plated pins of the assembly from damage due to impact.

When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam or plastic pin protector.

Minimum Equipment Required

The minimum hardware for analysis of a TMS32020/C25 target system consists of the following equipment:

- An HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A Logic Analyzer.
- The TMS32020/C25 Preprocessor Interface and Inverse Assembler (HP E2418A).

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2418A Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Ensure that the TMS32020/C25 is operating in microprocessor mode. In microprocessor mode, the bus operations to the external program memory are available to be captured by the logic analyzer. Accesses to TMS32020/C25 internal resources are not presented on the external data bus.
2. If they are not already connected, connect the 100 kOhm Termination Adapters to the connectors on the preprocessor interface (see page 1-4).
3. Install the preprocessor interface in the target system (see page 1-5).
4. Connect the logic analyzer probes to the termination adapters on the connectors on the preprocessor interface board as listed in table 1-1 (see page 1-8).
5. Power up the logic analyzer, and then the target system. Since the logic analyzer provides power to the preprocessor interface, it must always be powered up first.
6. Load the logic analyzer configuration file for the specified logic analyzer (see page 1-11). Table 1-1 lists the configuration files.

Connecting the Termination Adapter to the Preprocessor Interface

The 100 kOhm Termination Adapter (HP part number 01650-63203) properly terminates the logic analyzer probes. The following steps explain how to connect the termination adapter to the HP E2418A Preprocessor Interface:

1. Align the key on the small end of the termination adapter with the slot on the appropriate connector on the preprocessor interface.
2. Push the termination adapter into the connector.
3. Repeat steps 1 and 2 for each termination adapter.

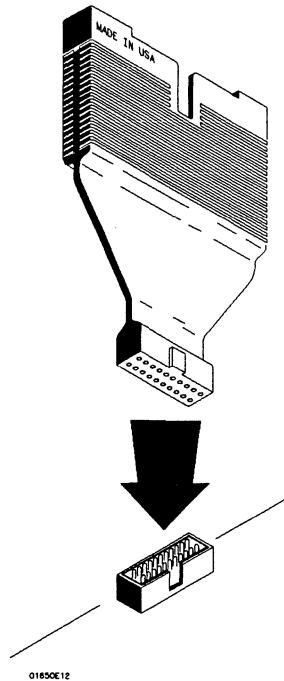


Figure 1-1. Connecting Termination Adapters

Connecting to the Target System

The following steps explain how to connect the HP E2418A Preprocessor Interface to your target system:

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Remove the TMS32020/C25 microprocessor from its socket on the target system and store it in a protected environment.
-

Caution 

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 (figure 1-2) on the preprocessor interface connector and the target system socket prior to inserting the connector in the socket. Also, take care to align the preprocessor interface connector with the socket on the target system so that all microprocessor pins are making contact.

2. Plug the preprocessor interface connector into the microprocessor socket on the target system.
-

Note 

If the preprocessor interface connector interferes with components of the target system or if a higher profile is required, additional plastic pin guards can be added. Plastic pin guards can be ordered from Hewlett-Packard using the part number 1200-1458. However, any 68-pin PGA IC socket with a TMS32020/C25 foot print and gold-plated pins can be used.

3. Plug the TMS32020/C25 microprocessor into the socket of the preprocessor interface board. The socket on the preprocessor interface board is designed with low insertion force pins to allow you to install or remove the microprocessor with a minimum amount of force.

Caution 

Care must be used when removing a microprocessor or socket from the preprocessor interface board to prevent damaging the traces on the board.

4. Power up the logic analyzer, and then the target system.

Note 

Protect your equipment. Since the logic analyzer provides power to the preprocessor interface, the logic analyzer should always be powered up whenever the target system is powered up or down.

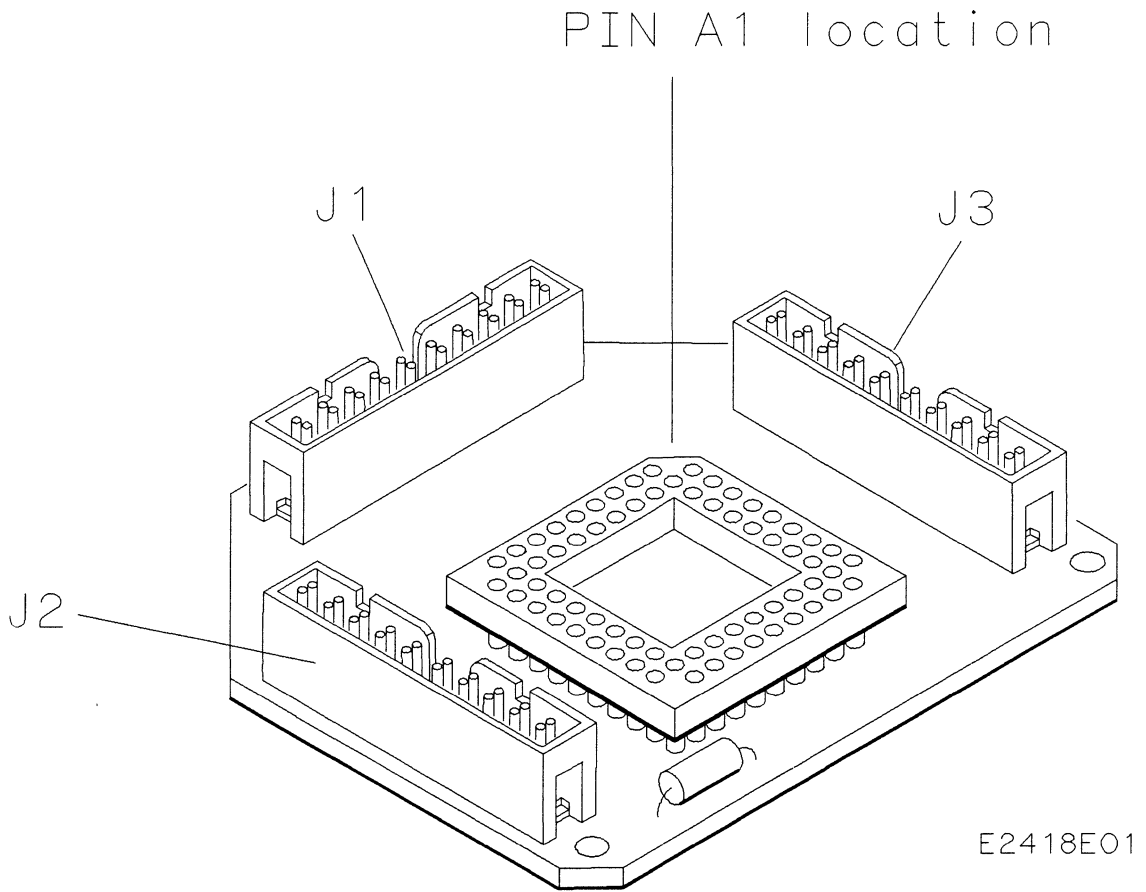


Figure 1-2. Preprocessor Interface Assembly

Connecting to the HP E2418A

Connect the logic analyzer cables to the preprocessor interface as shown in table 1-1. Descriptions such as J1 refer to connectors on the preprocessor interface, while Pod 1 refers to a logic analyzer pod.

Figure 1-3 shows the relative locations of the logic analyzer cards.



HP 16542A with three or four Expansion Cards

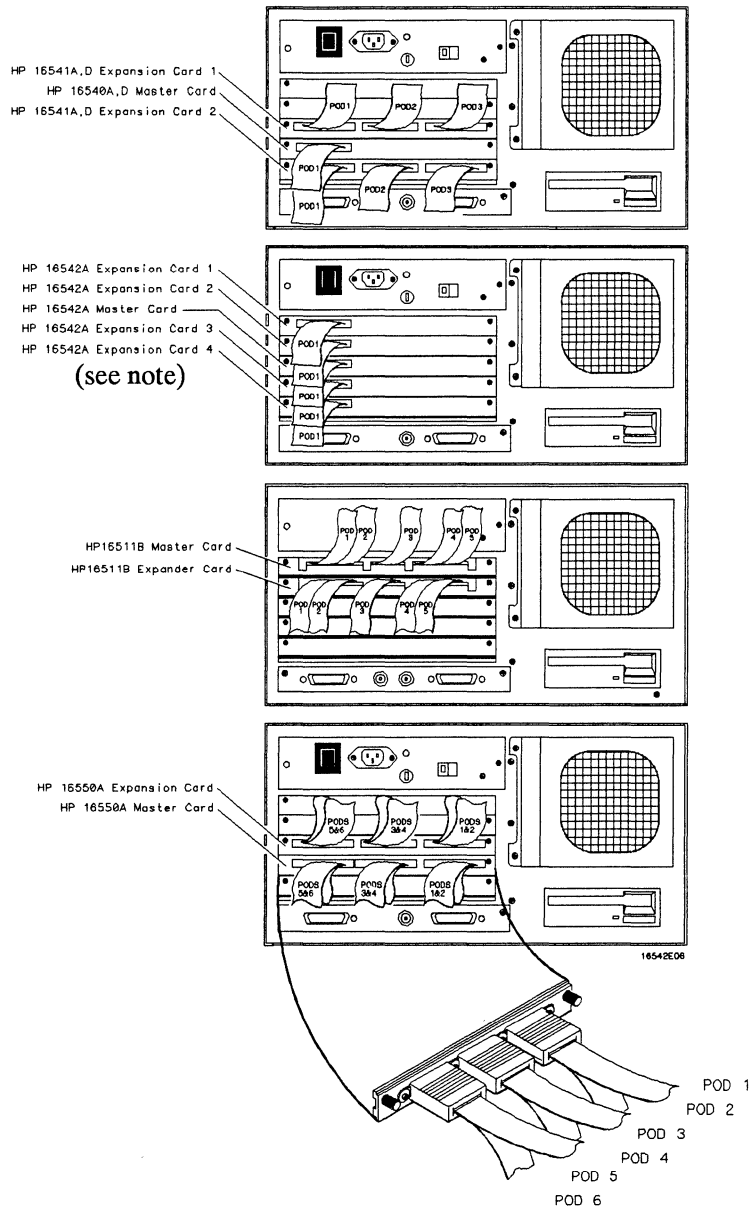
The locations for the HP 16542A expansion cards, relative to the Master Card, depend on the number of expansion cards used. If one or two expansion cards are used, Card 1 is located above the Master Card and Card 2 is located below the Master Card. If three expansion cards are used, two of them are located above the Master Card and the third is located below the Master Card. When four expansion cards are used, they are located as shown in figure 1-3.

Table 1-1 shows the physical locations and connections for a two-expansion-card system. If you are using more than two expansion cards, check the Format menu in the logic analyzer to see where the pods should be connected.

Power Up / Down Sequence

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.



**Figure 1-3. Logic Analyzer Card Locations
 (relative locations, actual slots used may vary)**

Table 1-1. Logic Analyzer Connections and Configuration Files

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 16510A, HP 1652B and HP 16510B	C320C25		--	--	J3 STAT	J2 ADDR clk ↑	J1 DATA
HP 16511B Master (Upper Card)	D320C25		--	--	--	--	--
HP 16511B Expander (Lower Card)			--	--	J3 STAT	J2 ADDR clk ↑	J1 DATA
HP 16541A,D Exp. Card 1 *	E320C25				--	J3 STAT	J1 DATA
HP 16540A,D Master Card							J2 ADDR clk ↑
HP 1661A, HP 16550A	F320C25 **	--	J3 STAT	--	J2 ADDR clk ↑	--	J1 DATA
HP 1660A	F320C25 **	--	(Pod 7) J3 STAT	--	J2 ADDR clk ↑	--	J1 DATA
HP 1660A/61A/62A	C320C25			--	J3 STAT	J2 ADDR clk ↑	J1 DATA
HP 16542A Exp. Card 1	E320C25						J3 STAT
HP 16542A Master Card							J2 ADDR clk ↑
HP 16542A Exp. Card 2							

* For the HP 16541A,D Expander Cards, expansion card 1 is the physically highest HP 16541A,D card (see figure 1-3).

** This configuration provides 8 k acquisition depth.

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for TMS32020/C25 analysis by loading the specified TMS32020/C25 configuration file. Loading this file will also load the inverse assembler file. To load the configuration and inverse assembler:

1. Install the HP E2418A flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
 - For the HP 1650-series logic analyzers, select the I/O Disk Operations menu;
 - For the HP 16500-series and HP 1660-series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer configuration from disk.
4. For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
5. Use the knob to select the appropriate configuration file (see table 1-1).
6. Execute the load operation to load the file into the logic analyzer.

Timing Analysis

The HP E2418A can also be used for timing analysis. The format specification loaded for state analysis is used for timing analysis. To configure the logic analyzer for timing analysis:

1. Load the appropriate state configuration file from the disk.
2. Select the Configuration menu of the logic analyzer.
3. Select the Type field and select Timing.

Analyzing the Texas Instruments TMS32020/C25

Introduction

This chapter provides reference information on the format specification and symbols configured by the HP E2418A software. It also provides information about the inverse assembler and status encoding.

Format Specification

When you use the HP E2418A Preprocessor Interface, the format specification set up by the software will be similar to that shown in figure 2-1. There are some slight differences in the displays, according to which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field. Refer to your logic analyzer manual to see which fields and displays are available.

Table 3-1 in chapter 3 lists the TMS32020/C25 signals for the HP E2418A Preprocessor Interface, and their corresponding lines to the logic analyzer.



For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field should remain in the current selection (< 60 ns) for proper preprocessor interface operation. For more information on the Clock Period settings, refer to your logic analyzer manual.

100/500MHz LA D Format 1 Print Run

State Acquisition Mode Master Clock
 Full Channel/4K Memory/100MHz Lf Symbols

Pod D3 TTL Pod D2 TTL Pod D1 TTL

Pods Master Clock Master Clock Master Clock

Labels 15 ... 87 ... 0 15 ... 87 ... 0 15 ... 87 ... 0

ADDR	+	*****
DATA	+	*****
STAT	+
/HOLDA	+
/PS	+
R/W	+
/IS	+
/DS	+

Figure 2-1. TMS32020/C25 Format Specification

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges. Table 2-1 shows the Status label encoding.

Table 2-1. Status Label Encoding

	Status Bit 5 4 3 2 1 0
TMS32020/C25 Cycle Type	
instruction fetch	x x 1 1 1 1
operand read	x x 1 1 1 0
i/o read	x x 1 0 1 0
i/o write	x x 0 0 1 0
memory read	x x 1 1 0 0
memory write	x x 0 1 0 0

Listing Menu

Captured data is displayed as shown in figure 2-2. This figure displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

Label>		ADDR	TMS320C25 Inverse Assembler	DATA2	STAT	/HD
Base>	Hex	mnemonics		Hex	Binary	Bin
0	0001		reset vector	0022	101110	1
1	0022		DINT	CE01	101111	1
2	0023		LDPK >0000	C800	101111	1
3	0024		RDVM	CE02	101111	1
4	0025		LARP ARO	5588	101111	1
5	0026		SPM 000 [No Shift]	CE08	101111	1
6	0027		RTXM	CE20	101111	1
7	0028		SXF	CE0D	101111	1
8	0029		SSXM	CE07	101111	1
9	002A		CNFD	CE04	101111	1
10	002B		LALK >FFFF	D001	101111	1
11	002C		operand fetch	FFFF	101110	1
12	002D		SACL >0003	6003	101111	1
13	002E		ZAC	CA00	101111	1
14	002F		SACL >0004	6004	101111	1
15	0030		SACL >0005	6005	101111	1

Figure 2-2. State Listing

The TMS32020/C25 Inverse Assembler

The IACK signal and the CLKOUT1 signals are used by the inverse assembler to distinguish an instruction fetch from an operand read. When CLKOUT1 is low, a low IACK indicates an Interrupt Acknowledge. When CLKOUT1 is high, a high IACK indicates Instruction Acquisition.

The inverse assembler examines the value in the ADDR field at each state line to determine if the TMS32020/C25 microprocessor has acknowledged an interrupt (address < 1F hex). The IACK signal is not used to determine when an interrupt has been acknowledged.

The TMS32020/C25 microprocessor does not provide enough status information for the inverse assembler to pick out the first word of an opcode fetch from a series of program reads. To ensure correct disassembly, you may need to point to the 16-bit word that contains the first word of an opcode fetch. Once synchronized, the inverse assembler will disassemble from this point through the end of the screen. Use the following steps to point to the first word of an opcode fetch:

1. Select a line on the display that you know contains the first word of an opcode fetch.
2. Roll this line to the top of the screen.



The cursor location is not the top of the display. In figure 2-2, line 0 is at the top of the display.

3. Select the "Invasm" field at the top of the display.

Rolling the display up will inverse assemble the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-synchronize the inverse assembler by repeating steps 1 through 3.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but activity between those blocks will not be inverse assembled.

Modifying the Trace Specification for a Measurement

The configuration files provided with this product define a trace specification that allows you to make a measurement immediately after the RUN button is pressed. That is, the trigger condition consists of all "don't care" terms.

The /HOLDA signal can be used for state qualification so that multiprocessor activity (DMA, etc.) is filtered out. To filter out multiprocessor activity, specify in the Trace Specification that /HOLDA must be high. To capture multiprocessor activity, specify /HOLDA as "don't care."

Bus operations that are captured when the /HOLDA line is low are not disassembled. They are listed as "hold acknowledge" in the logic analyzer display.

General Information

Introduction

This chapter contains additional reference information including the characteristics and signal mapping for the HP E2418A.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2418A Preprocessor Interface. These characteristics are included as additional information for the user.

Microprocessor

Compatibility:

Texas Instruments TMS32020/C25 and all microprocessors made by other manufacturers that comply with Texas Instruments TMS32020/C25 specifications.

Microprocessor Package: 68-pin PGA.

Accessories Required: None.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A/62A, HP 16510A, HP 16510B, HP 16511B, HP 16550A, HP 16542A (Master Card and two expansion cards), or HP 16540A,D with one HP 16541A,D Expansion Card.

Power Requirements: None.

Number of Probes Used: Three 16-channel probes.

Environmental Temperature:

Operating: 0 to +55° C
(+32 to +131° F)

Nonoperating: -40 to +75° C
(-40 to +167° F)

Altitude:

Operating: 4,600 m (15,000 ft)

Nonoperating: 15,300 m (50,000 ft)

Humidity: Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.

Interface Description

The falling edge of STRB is used to clock the address, data and status into the logic analyzer. The STRB signal is connected to the logic analyzer clock on the preprocessor interface pod J2 (this is the K clock on most logic analyzers).

TMS32020/C25 Signal to HP E2418A Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2418A Preprocessor Interface. Since the pods on the logic analyzers may be numbered differently than the pods on the preprocessor interface, refer to table 1-1 (page 1-10) to correlate the pod numbers.

Table 3-1. TMS32020/C25 Signal List

Preprocessor Pod	Logic Analyzer Probe	Pin Mnemonic	Label
J1	0	D0	DATA
J1	1	D1	DATA
J1	2	D2	DATA
J1	3	D3	DATA
J1	4	D4	DATA
J1	5	D5	DATA
J1	6	D6	DATA
J1	7	D7	DATA
J1	8	D8	DATA
J1	9	D9	DATA
J1	10	D10	DATA
J1	11	D11	DATA
J1	12	D12	DATA
J1	13	D13	DATA
J1	14	D14	DATA
J1	15	D15	DATA
J2	0	A0	ADDR
J2	1	A1	ADDR
J2	2	A2	ADDR
J2	3	A3	ADDR
J2	4	A4	ADDR
J2	5	A5	ADDR
J2	6	A6	ADDR
J2	7	A7	ADDR

Table 3-1. TMS32020/C25 Signal List (Continued)

Preprocessor Pod	Logic Analyzer Probe	Pin Mnemonic	Label
J2	8	A8	ADDR
J2	9	A9	ADDR
J2	10	A10	ADDR
J2	11	A11	ADDR
J2	12	A12	ADDR
J2	13	A13	ADDR
J2	14	A14	ADDR
J2	15	A15	ADDR
J2	KCLK	/STRB	
J3	0	/IACK	STAT
J3	1	/DS	STAT
J3	2	/IS	STAT
J3	3	R/W	STAT
J3	4	/PS	STAT
J3	5	/HOLDA	STAT

Servicing

The repair strategy for the HP E2418A is board replacement. However, table 3-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2418-66501	Circuit Board Assembly
1200-1458	Pin Protector IC Socket
E2418-68703	Inverse Assembler Disk Pouch
01650-63203	100 kOhm Termination Adapter

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501 frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check that the logic analyzer pods are connected to the proper connectors, as listed in table 1-1.

For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

Slow Clock If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP E2418A and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

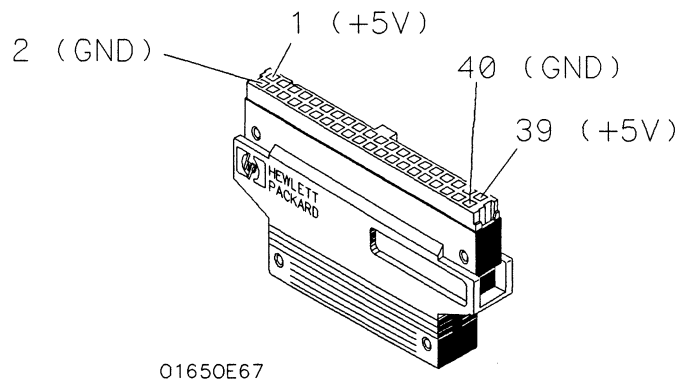


Figure A-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display (not at the input cursor) and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. One technique to reduce the capacitive loading is to remove as many pin protectors, extenders, and adapters as possible.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than ($<$) instead of greater than ($>$). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms." The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/41/42) The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D, HP 16541A,D or HP 16542A cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.