HEWLETT PACKARD

User's Guide

HP E2441B VME/VXI Bus Preprocessor Interface

HP E2441B VME/VXI Bus Preprocessor Interface User's Guide

for the HP 1650A , HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers

Manual Part Number E2441-90901
Microfiche Part Number E2441-90801

Printed in U.S.A. July 1992

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition is published.

A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

Edition 1 July 1992 E2441-90901

List of Effective Pages

The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

Pages	Effective Date

Product Warranty

This Hewlett-Packard product has a warranty against defects in material and workmanship for a period of 1 year from date of shipment. During warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by Hewlett-Packard. However, warranty service for products installed by Hewlett-Packard and certain other products designated by Hewlett-Packard will be performed at Buyer's facility at no charge within the Hewlett-Packard service travel area. Outside Hewlett-Packard service travel areas, warranty service will be performed at Buyer's facility only upon Hewlett-Packard's prior agreement and Buyer shall pay Hewlett-Packard's round trip travel expenses.

For products returned to Hewlett-Packard for warranty service, the Buyer shall prepay shipping charges to Hewlett-Packard and Hewlett-Packard shall pay shipping charges to return the product to the Buyer. However, the Buyer shall pay all shipping charges, duties, and taxes for products returned to Hewlett-Packard from another country.

Hewlett-Packard warrants that its software and firmware designated by Hewlett-Packard for use with an instrument will execute its programming instructions when properly installed on that instrument.

Hewlett-Packard does not warrant that the operation of the instrument, software, or firmware will be uninterrupted or error-free.

Limitation of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by the Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HEWLETT-PACKARD SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Exclusive Remedies

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HEWLETT-PACKARD SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For assistance, contact your nearest Hewlett-Packard Sales and Service Office.

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

Safety

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this user's guide must be heeded.

Contents

Chapter 3: Timing Analysis

Chapter 4: General Information

Appendix A: Troubleshooting

Introduction

The HP E2441B VME/VXI Bus Preprocessor Interface provides a complete interface between any VME/VXI Bus target system using "B" or "C" size cards and the following logic analyzers: HP 1650A , HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A. The preprocessor interface connects the signals from the VME/VXI Bus target system to the logic analyzer inputs. For "B" sized systems, the preprocessor interface board may also be used as an extender board.

The configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with your VME/VXI bus system. When the state configuration file is loaded, an inverse assembler is also loaded which decodes VME/VXI transactions into mnemonics.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2441B Preprocessor Interface:

HP 1650A, HP 1650B, HP 16510A, HP 16510B, and HP 1652B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing.

HP 1660A/61A

The HP 1660A Logic Analyzer provides 4 k of memory depth with 136 channels of 100 MHz state analysis or 250 MHz of timing analysis. The HP 1661A Logic Analyzer provides 4 k of memory depth with 102 channels of 100 MHz state analysis or 250 MHz of timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing.

HP 16540A,D with two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with 112 channels of 100 MHz state or timing analysis.

HP 16542A (five cards)

This logic analyzer combination provides 1 M of memory depth with 80 channels of 100 MHz state or timing analysis.

HP 16550A

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz of timing analysis. The logic analyzer will also support various combinations of mixed state/timing analysis.

How to Use This Manual

This manual is organized into four chapters and one appendix:

- Chapter 1 introduces you to the HP E2441B VME/VXI Bus Preprocessor Interface and lists the minimum equipment required and accessories supplied for VME/VXI bus analysis. This chapter also contains information that is common to both state and timing analysis of the VME/VXI bus.
- Chapter 2 explains how to configure the HP E2441B VME/VXI Bus Preprocessor Interface to perform state analysis on your target system.
- Chapter 3 explains how to configure the HP E2441B to perform timing analysis on your target system.
- Chapter 4 provides some general information including the operating characteristics for the HP E2441B Preprocessor Interface.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1 Analyzing the VME/VXI Bus

Introduction

This chapter introduces you to the HP E2441B VME/VXI Bus Preprocessor Interface and lists the minimum equipment required and accessories supplied for VME/VXI bus analysis. This chapter also contains information that is common to both state and timing analysis of the VME/VXI bus.

Duplicating the Master Disk

Before you use the HP E2441B software, make a duplicate copy of the HP E2441B master disk. Then store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidently deleted.

To make a duplicate copy, use the Duplicate Disk operation in the disk menu of your logic analyzer. For more information, refer to the reference manual for your logic analyzer.

Equipment Supplied

The HP E2441B Bus Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the interface circuit board (HP part number E2441-66501).
- Six jumpers (HP part number 1252-3743) which come installed on the circuit board.
- The inverse assembly software on a 3.5-inch disk.
- This operating manual.

Minimum Equipment Required

The minimum equipment required for analysis of a VME/VXI bus target system consists of the following equipment:

- An HP 1650A , HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A Logic Analyzer.
- The VME/VXI Bus Preprocessor Interface and Inverse Assembler (HP E2441B).

Caution 

To prevent equipment damage, remove power from both the logic analyzer and the target system whenever the preprocessor interface is being connected or disconnected.

Use of the Asterisk

To help define usage, the VME/VXI specification (IEEE STD P1014) assigns an asterisk (*) suffix to signal mnemonics for the following conditions:

- An asterisk (*) follows the signal name of signals which are level-significant to denote that the signal is true or valid when the signal is low.
- An asterisk (*) follows the signal name of signals which are edge-significant to denote that the actions initiated by that signal occur on a high to low transition.

In the symbol tables, the labels for signals or groups of signals which are asserted low are designated with a prefix "/", such as "/BGIN".

Daisy-Chaining

The daisy-chains are used to propagate signal levels from board to board, starting with the first slot and ending with the last slot. Each board in a VME/VXI bus backplane slot can control whether the Bus Grant and IACKIN/OUT signals are passed to the next highest slot. The HP E2441B Preprocessor Interface board allows you to properly jumper the four Bus Grant daisy-chains and the Interrupt Acknowledge daisy-chain on the VME/VXI bus.

Bus Grant and IACKIN/OUT Lines

The Bus Request lines are used to request the use of the Data Transfer Bus (DTB). The Bus Grant lines allow the ARBITER to award use of the bus to one REQUESTER at a time. The ARBITER does this by driving a Bus Grant daisy-chain line low. This low level propagates down the daisy-chain, typically passing through several boards in the process. If a board never uses a particular request/grant level, the signal is passed through that board. If the board uses a request/grant level low, the corresponding signal BGxIN* is stopped on the board. If this board's on-board REQUESTER is currently requesting the DTB on that level, the board does not pass the low level on to its BGxOUT*. Otherwise, the board passes the low level on to the next board.

If the Bus Grant information is required, you must place the preprocessor interface board in a lower number slot than any VME/VXI board in which BGxIN* is occurring. If the preprocessor interface board is in a higher number slot than a VME/VXI board which is requesting the bus, the daisy chain will not pass the necessary information for the preprocessor interface to properly decode the bus arbitration. When this happens, a 3 (hexadecimal) is displayed on the state display listing, instead of the proper bus grant number.

Each of the seven Interrupt Request lines can be shared by two or more INTERRUPTER modules. The Interrupt Acknowledge daisy chain assures that only one INTERRUPTER responds to the Interrupt Acknowledge cycle. This daisy-chain line passes through each board on the VME/VXI bus. Each INTERRUPTER that is driving an interrupt line low waits for a falling edge to arrive at its IACKIN* daisy-chain input. Only upon receiving this falling edge does an INTERRUPTER respond to an Interrupt Acknowledge cycle. The INTERRUPTER does not pass the falling edge on down the daisy chain. This prevents other INTERRUPTERS from responding to the Interrupt Acknowledge cycle.

Jumper J2 provides the daisy chain for the IACKIN/OUT signal. Jumpers J3 through J6 provide the daisy chain for the Bus Grant signals. If either of the following conditions are true, jumpers must be installed across pins 1 and 2 on J2 through J6 at an empty mainframe slot to pass the Bus Grant and IACKIN/OUT signals:

- If a VME/VXI bus backplane slot is not occupied by a board, and there are boards farther down the daisy chain.
- If no VME/VXI board is installed in the HP E2441B Preprocessor Interface board that resides in that slot, and there are boards farther down the daisy chain.

Note 

If the preprocessor interface is used as an extender card, with another VME/VXI Bus card attached to the front of it, the jumpers must be placed across pins 2 and 3, or else removed, to avoid shorting the daisy chain. The VME/VXI Bus card will provide the necessary circuitry for the daisy chain.

Connecting the Jumpers

Figure 1-1 shows the location of the jumpers and the appropriate pin locations. There are six jumpers, J1 - J6. Five of the jumpers (J2 - J6) are for configuring the preprocessor interface according to how it is used in the VME/VXI bus daisy chain. The sixth jumper (J1) selects the signal BERR or IRQ1 for timing measurements.

Jumpers J2 - J6 have the same function as the Bus Grant and IACKIN/OUT jumpers on any VME or VXI card. These jumpers make or break the daisy chain for the Bus Grant lines and the IACKIN/OUT line. J2 is for IACKIN/OUT, and J3 through J6 are BG3 through BG0. The five configuration jumpers must be connected across the pins as shown in the table 1-1. Table 1-2 shows the jumpers for BERR/IRQ1.

Table 1-1. Jumper Connections (J2 - J6)

Jumpers	Condition
Across pins 1 and 2	If there is not a VME/VXI board installed in the HP E2441B Preprocessor Interface board that is installed in a VME/VXI backplane slot, AND there are boards farther down the daisy-chain.
Across pins 2 and 3	If the HP E2441B Preprocessor Interface board is used as an extender, and there is a VME/VXI board installed in the front of the board.
Across pins 2 and 3	If there are not boards installed farther down the daisy-chain from the HP E2441B Preprocessor Interface board.

Note The HP E2441B Preprocessor Interface board is shipped from the factory with jumpers connected across pins 2 and 3 of J2 through J6.

Table 1-2. BERR/IRQ1 Jumper J1 Connections (Timing Only)

Jumper	Signal
Across pins 2 and 3	Selects BERR for timing measurements.
Across pins 1 and 2	*Selects IRQ1 for timing measurements.

* The configuration file is set up for BERR. If you move the jumper to select IRQ1, you must also go to the Format menu on the logic analyzer and reassign (move the asterisk) from BERR on pod 4, bit 6, to bit 1 on IRQ7:1. Remove the asterisk for BERR, and add it for IRQ1.

To move the jumpers, simply remove each jumper, one at a time, and place it across the appropriate pins. The HP part number for the jumpers is 1252-3743.

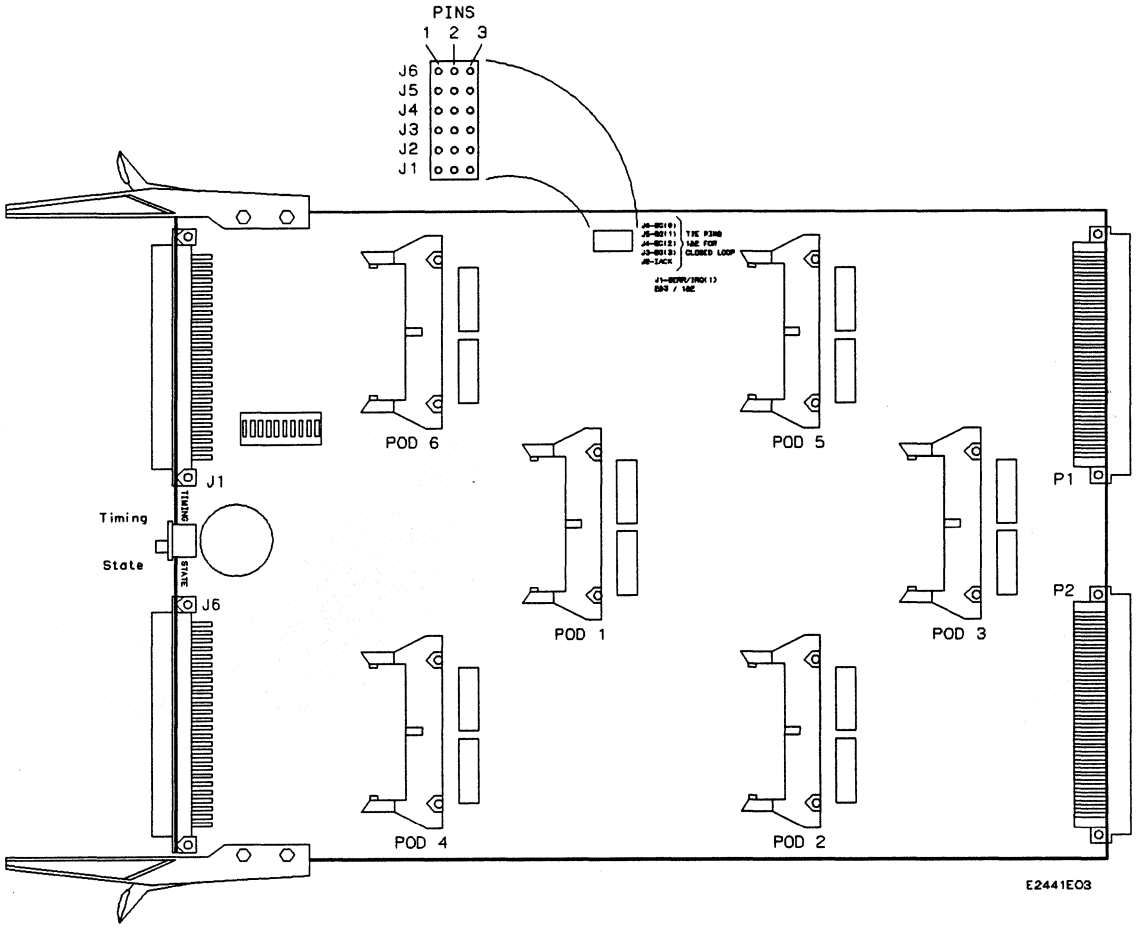

Figure 1-1. Daisy-Chain Jumpers

LED Indicators

An LED light bar containing 10 LEDs (see figure 1-2) is used to inform you of the status of the following signals:

- VME_+5.
- VME_–12.
- VME_+12.
- VME_+5STDBY.
- ACFAIL.
- SYSFAIL.
- SYSRESET.
- VCC (+5 V).

The power indicator LEDs will be illuminated if power is applied to the target system. In order for the preprocessor interface to be operating, the logic analyzer must be supplying power. If ACFAIL, SYSFAIL, or SYSRESET become true (active low), the corresponding LED will be turned on. The first two LEDs are not used.

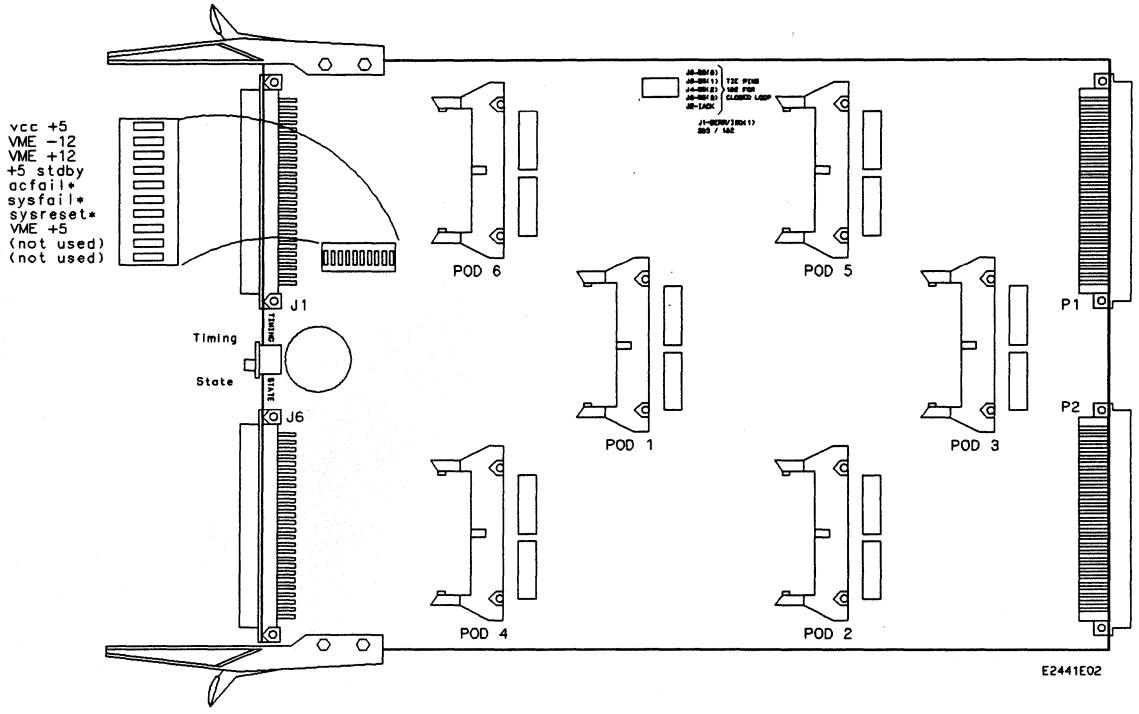

Figure 1-2. LED Display

2

State Analysis

Introduction

This chapter explains how to configure the HP E2441B VME/VXI Bus Preprocessor Interface to perform state analysis on a VME/VXI bus system using "B" or "C" size cards. The state configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the VME/VXI bus target system. The two inverse assemblers interpret both VME and VXI bus transactions for obtaining displays of VME/VXI bus data. The IVXI_IAL inverse assembler decodes memory transactions in the A16 address range C000H to FFFFH in terms of VXI version 1.3 protocols and definition. The IVME_IAL inverse assembler decodes these addresses as pure VME references.

Chapter 3 explains how to configure the HP E2441B VME/VXI Bus Preprocessor Interface to perform timing analysis on a VME/VXI bus system using "B" or "C" size cards.

Installation Quick Reference

The following procedure describes the major steps required to perform state measurements with the HP E2441B Bus Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

1. Set the State/Timing switch to the down (State) position for state analysis (see figure 2-1).
2. Set jumpers across pins 1 and 2 of jumpers J2 through J6 if the daisy chain on signals BG3IN* through BG0IN* and IACK* need to continue to the next slot (see page 1-4). Otherwise, set jumpers across pins 2 and 3. Note that if the preprocessor interface board is used as an extender, the jumpers must be set across pins 2 and 3.
3. Plug the logic analyzer cables into the preprocessor interface board (see table 2-1).
4. If you are installing the preprocessor interface board into a "C" size target system, remove the two board supports on the preprocessor interface board (see page 2-7).
5. Install the preprocessor interface board in the target system and, if necessary, plug the VME/VXI board into the preprocessor interface board (see page 2-6).
6. Load the logic analyzer configuration and IVXI_IAL inverse assembler by loading the appropriate file from the preprocessor interface disk (see page 2-8).
7. If a different inverse assembler is required, load the appropriate inverse assembler:
   - IVME_IAL for VME or VXI inverse assembly without decoding VXI registers (see page 2-8).
   - IVXI_IAL for VME or VXI inverse assembly including decoding VXI registers (see page 2-8).

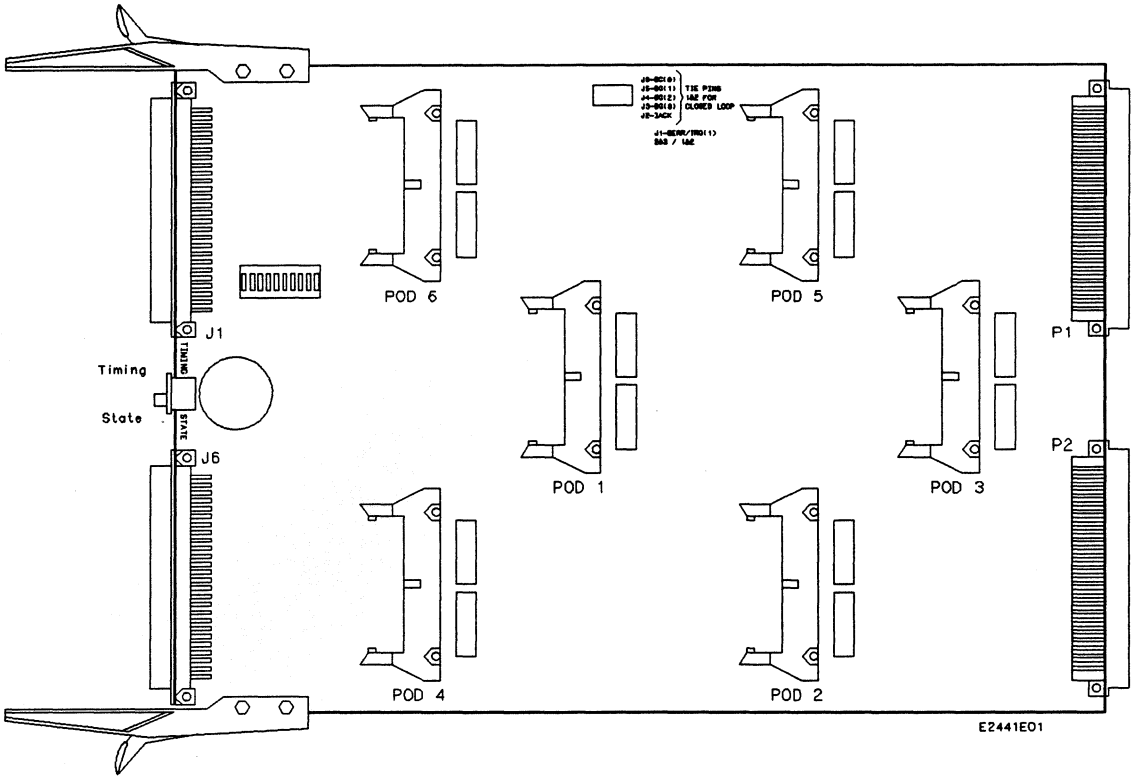

Figure 2-1. HP E2441B Pod Locations

Connecting to the HP E2441B

Connect the logic analyzer cables to the HP E2441B Preprocessor Interface pods as shown in table 2-1. Figure 2-2 shows the relative locations for the logic analyzer cards.

Table 2-1. Connections and Configuration Files (State Analysis)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 16510A, HP 1652B and HP 16510B	CE2441S		P5	P4	P3	P2	P1
HP 16511B Master Card	DE2441S		--	--	--	--	--
HP 16511B Expander Card			P5	P4	P3	P2	P1
HP 16541A,D Exp. Card 1 *	EE2441				P6 **	P2	P1
HP 16540A,D Master Card							P5
HP 16541A,D Exp. Card 2 *					--	P4	P3
HP 16542A ***	GE2441S		Master P5	Exp. 3 P4	Exp. 4 P3	Exp. 1 P2	Exp. 2 P1
HP 16550A, HP 1660A/61A	FE2441	P6 **	P5	P4	P3	P2	P1

* For the HP 16541A,D Expander Cards, expansion card 1 is the physically highest HP 16541A,D card, and expansion card 2 is the next physically highest HP 16541A,D card (see figure 2-2).

** P6 is not required for inverse assembly. It is only used for timing analysis.

*** For the locations of the HP 16542A cards, see figure 2-2.

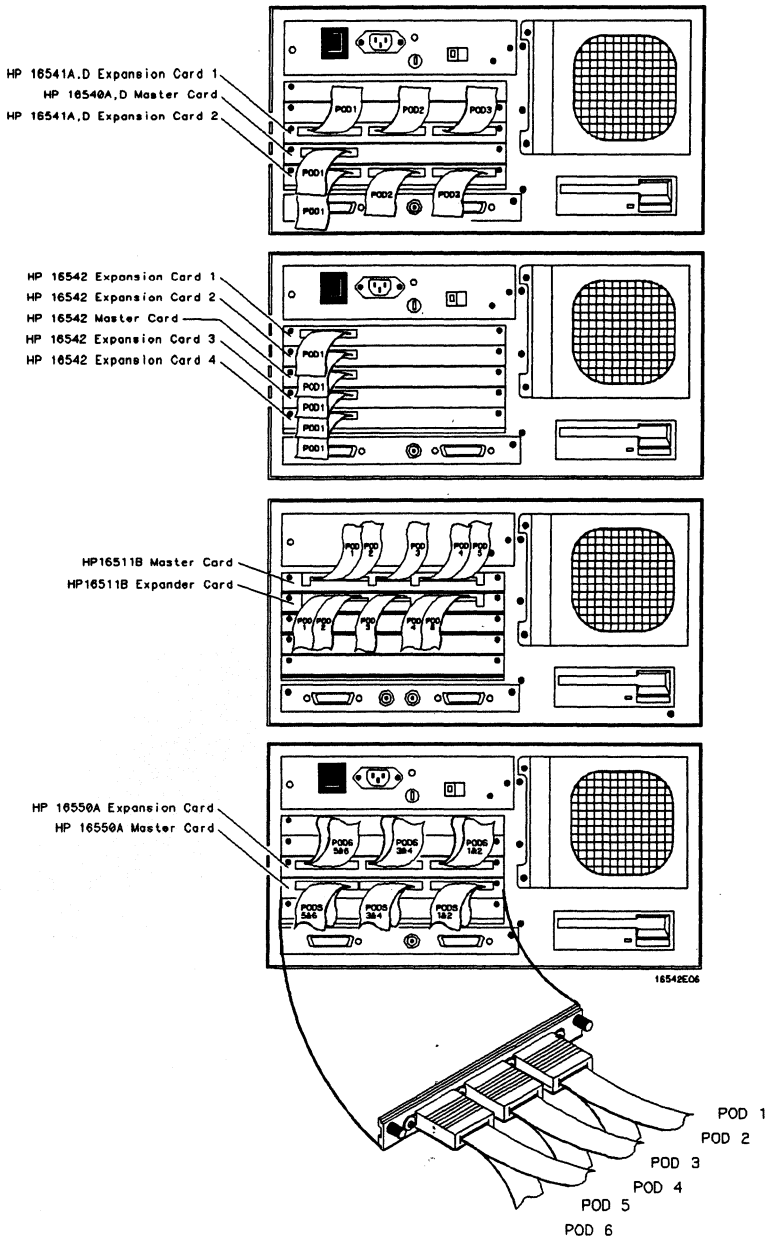

Figure 2-2. Logic Analyzer Card Locations (relative locations, actual slots used may vary)

Installing the HP E2441B

The HP E2441B Preprocessor Interface board can be installed in any slot of the VME/VXI bus system. It can be installed as a separate board or as an extender board in "B" size systems. The following steps explain how to install the HP E2441B Preprocessor Interface board in a "B" or "C" size target system:

Note If there are boards in higher number slots than the preprocessor interface board, refer to the section "Daisy-Chaining" on page 1-4 for information on setting the jumpers.

1. If the HP E2441B Preprocessor Interface board will be used as an extender board, remove the current VME/VXI board from its socket on the target system and store it in a protected environment.
2. If you are installing the preprocessor interface board into a "C" size target system, remove the two board supports from the preprocessor interface board (see figure 2-3).
3. Align the HP E2441B Preprocessor Interface board with the appropriate slot on the target system, and plug the board into the connectors (see figure 2-3).

Note Do not use the HP E2441B Preprocessor Interface as an extender board for VME/VXI "C" size systems.

4. If the HP E2441B Preprocessor Interface board is being used as an extender board in a "B" size target system, align the appropriate VME/VXI board with the slot on the end of the HP E2441B Preprocessor Interface board. Then plug the VME/VXI board into the connectors on the HP E2441B Preprocessor Interface board (see figure 2-3).

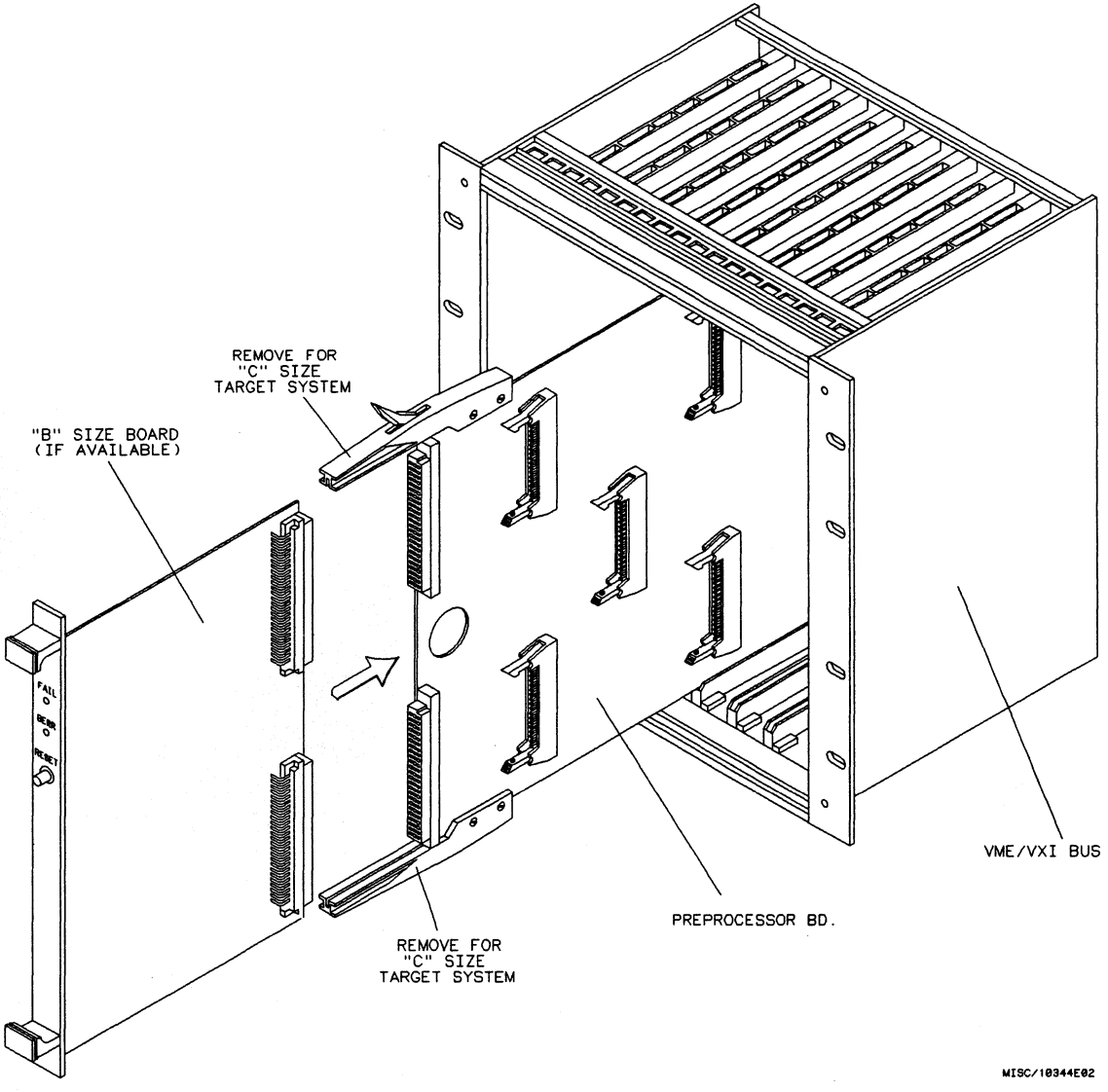

Figure 2-3. Installing the HP E2441B Board

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for VME/VXI bus analysis by loading the appropriate VME/VXI bus configuration file. Loading this file will also load the IVXI_IAL inverse assembler. Both inverse assemblers interpret VME and VXI bus transactions. The IVXI_IAL inverse assembler decodes memory transactions in the A16 address range C000H to FFFFH in terms of VXI protocols and definition. The IVME_IAL inverse assembler decodes these addresses as pure VME references. To load the configuration and inverse assembler:

1. Install the HP E2441B flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP 1650 series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500 series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer with the appropriate configuration file from table 2-1.
4. For the HP 1660A/61A and HP 16500 series logic analyzers, select the configuration file with the knob, then touch "All" and select the correct module.
5. Execute the load operation to load the file into the logic analyzer.
6. For the HP 1660A/61A, HP 16540/16541A,D and HP 16550A Logic Analyzers, go to the "System Configuration" menu and select "State".

If a different inverse assembler is required, configure the menu to "Load" one of the following inverse assemblers, using steps three through five above:

- IVME_IAL for VME or VXI inverse assembly without decoding VXI registers.
- IVXI_IAL for VME or VXI inverse assembly including decoding VXI registers.

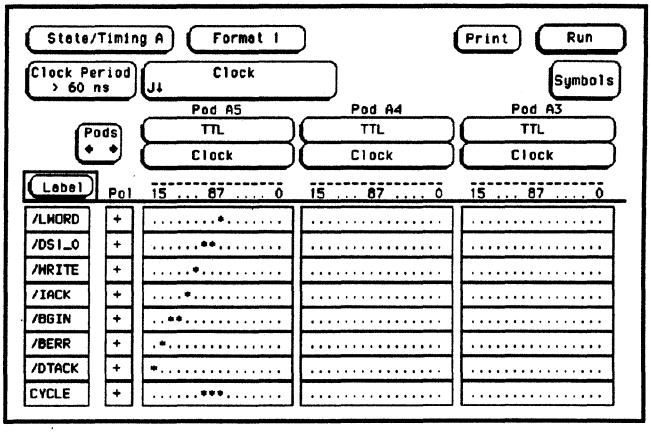

Figure 2-5. State Format Specification

Acquiring Data

To acquire data, touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full or when you touch STOP.

Note

The logic analyzer will flash "Slow or Missing Clock" when data is not being transmitted across the bus.

Listing Menu

Captured data is displayed as shown in figure 2-6. This figure displays the state listing after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual commands, status conditions, messages, and phases of the VME/VXI bus.

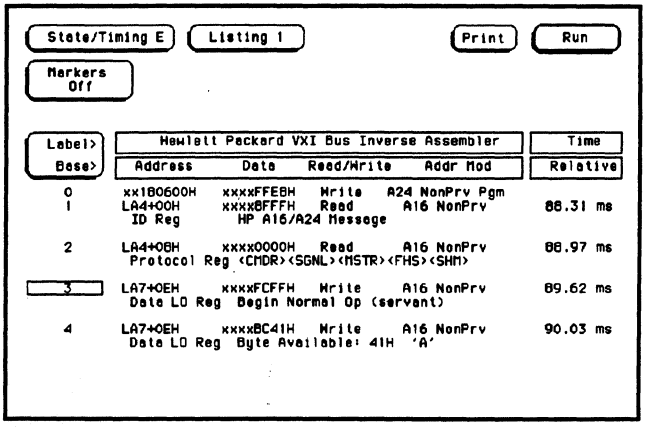

Figure 2-6. State Listing

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges.

Table 2-2 lists the symbols for the ADMOD label. Table 2-3 lists the symbols for the ADDR, /DS1_0, /BGIN, CYCLE, and /WRITE labels. The patterns for each symbol listed in the tables are shown in the binary base. In the actual software, these patterns are listed in the hexadecimal base to conserve display space.

Table 2-2. ADMOD Label Symbols

Label	Symbol	Pattern
ADMOD	A24 SUPRV BLK	1 1 1 1 1 1
	A24 SUPRV PGM	1 1 1 1 1 0
	A24 SUPRV DATA	1 1 1 1 0 1
	A24 NONPRIV BLK	1 1 1 0 1 1
	A24 NONPRIV PGM	1 1 1 0 1 0
	A24 NONPRIV DATA	1 1 1 0 0 1
	A16 SUPRV	1 0 1 1 0 1
	A16 NONPRIV	1 0 1 0 0 1
	USER DEFINED	0 1 x x x x
	A32 SUPRV BLK	0 0 1 1 1 1
	A32 SUPRV PGM	0 0 1 1 1 0
	A32 SUPRV DATA	0 0 1 1 0 1
	A32 NONPRIV BLK	0 0 1 0 1 1
	A32 NONPRIV PGM	0 0 1 0 1 0
	A32 NONPRIV DATA	0 0 1 0 0 1

Table 2-3. ADDR, /DS1_0, /BGIN, CYCLE, and /WRITE Symbols

Label	Symbol	Pattern
ADDR	DEV0 DEV1 DEV2 DEV3	C000 to C03F C040 to C07F C080 to C0BF C0C0 to C0FF
/DS1_0	MULTI EVEN ODD ADDR	0 0 0 1 1 0 1 1
/BGIN	BG0 BG1 BG2 BG3	0 0 0 1 1 0 1 1
CYCLE	ADDR ONLY QUAD 0-3 UNALIGN 1-2 DOUBLE 0-1 DOUBLE 2-3 UNALIGN 0-2 ILLEGAL SINGLE 0 SINGLE 2 UNALIGN 1-3 ILLEGAL SINGLE 1 SINGLE 3	1 1 x x 0 0 0 0 0 0 0 1 0 0 1 0 0 0 1 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 1 1 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1
/WRITE	READ /WRITE	1 0

Bus Grant Interpretation

In the State mode, the four Bus Grant signals are combined logically in the HP E2441B Preprocessor Interface and sent to the logic analyzer as two signals. Figure 2-7 shows the schematic and truth table for the Bus Grant signals.

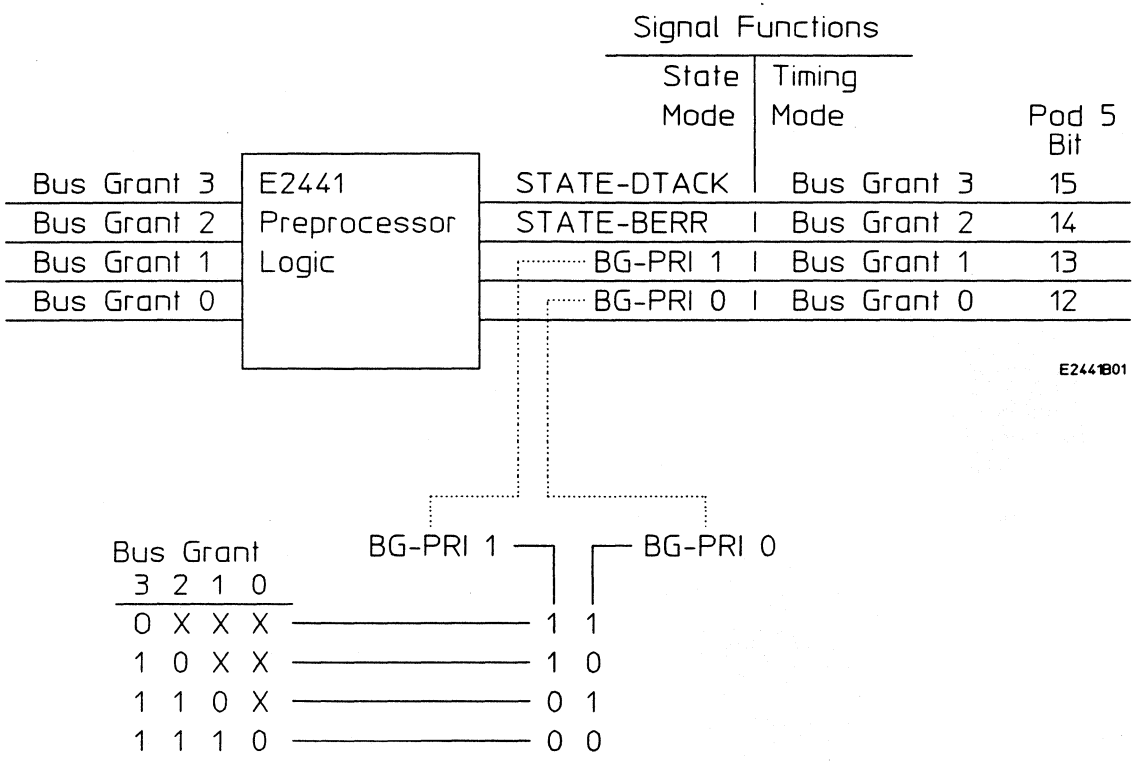

Figure 2-7. Bus Grant Signals

Address Interpretation

If a symbol is defined for the address, or for the range in which the address lies, the symbol (and offset) is displayed by the inverse assembler. For example, the address C000H could be translated as SYMBOL+00H. This format is particularly helpful for VXI cards where certain address ranges are associated with a particular card. For A16 addresses in the range of C000H to FFFFH, which are the VXI configuration registers, the default symbol LA# is supplied. The # sign represents the logical address of the VXI device. Other symbols can be defined in the Symbols menu of the Format menu. For more information, refer to the reference manual for your logic analyzer.

VXI Bus Translation

The ADDRess, DATA, Modifier, and Transfer Type are decoded for all VME and VXI bus transactions. If a bus transaction address lies in the A16 range C000H to FFFFH, then the transaction is decoded as a read or write to a VXI configuration register. A maximum of 256 VXI devices can have configuration registers in this range, on 64 byte offsets. The VME/VXI preprocessor interface treats memory transactions to configuration registers as shown in the following table:

Table 2-3. VXI Bus Translation

Offset	Transaction Type	Interpretation
00	Read	ID Register
00	Write	Assign Logical Address
02	Read	Type Register
02	Write	Reserved
04	Read	Status Register
04	Write	Control Register
06	R/W	Offset Register
08	Read	Message Protocol Register
08	Write	Message Signal Register
0A	Read	Message Response Register
0A	Write	Message Data Extended Register
0C	R/W	Message Data High Register
0E	Read	Message Data Low
0E	Write	Message Word Serial
10	R/W	Message A24 Pointer High
12	R/W	Message A24 Pointer Low
14	R/W	Message A32 Pointer High
16	R/W	Message A32 Pointer Low
18 - 1C	R/W	Undefined

Note 

The decoding may be incorrect if the device is a memory device or a register based device that uses the register offsets 08H to 16H.

When a bus transaction lies within the range of the VXI configuration register, the address is decoded in two parts: a logical address and a register offset. The register offset is used by the VXI inverse assembler to interpret the DATA bit pattern. For example, if the data DEFFH were written to the offset 0EH, it would be interpreted as a Word Serial Byte Request command.

For some registers, such as the Response Register, offset 0AH, the DATA pattern indicates whether particular flags are active. When decoding these registers, the inverse assembler interprets the pattern and shows any flags that are active (TRUE). For example, if LOCKED* = 0, the flag <LOCK> is shown. If no flags are currently active, the message "No Flags Set" is displayed.

Error Messages

The following list identifies the types of errors that are detected by the inverse assembler:

**** ERROR: MUST BE READ FOR IACK* SEQUENCE ****

This message means that the IACK* bit was 0 (indicating that the bus cycle was an interrupt acknowledge), and that the WRITE* line was also 0. This violates the VME/VXI interrupt handler definition.

**** BUS ERROR: Data NOT Transferred ****

This message indicates that the BERR* bit was 0. This bit can be driven low by either the bus timer (when it detects the absence of data acknowledge (DTACK*) during a data bus cycle), or by a card which implements the fast handshake protocol.

**** BAD COMBINATION OF DS1*, DS0*, LWORD*, A01**

This message indicates that an illegal combination of DS1*, DS0*, LWORD*, and A01 was present on the bus. VME defines the illegal cycle types as shown in table 2-4.

Table 2-4. Illegal Cycle Types

DS1*	DS0*	LWORD*	A01	CYCLE
high	low	low	high	DTB
low	high	low	high	DTB

State Format Specification

When you use the HP E2441B VME/VXI Bus Preprocessor Interface for state analysis, the format specification will be set up by the software as shown in figures 2-4 and 2-5.

Note

For those logic analyzers which have a Clock Period field (HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, and HP 16511B), the Clock Period field in figures 2-4 and 2-5 should remain in the current selection (> 60 ns) for proper preprocessor interface operation. For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

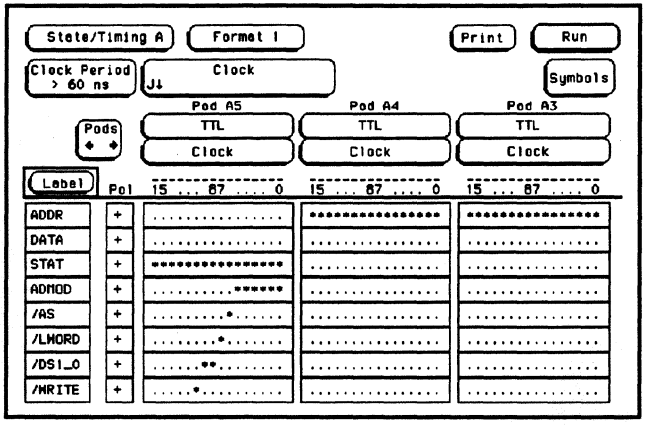

Figure 2-4. State Format Specification

Note

In figures 2-4 and 2-5, additional labels are listed offscreen. To view these signals, select the Label field and rotate the knob on the front panel clockwise.

3 Timing Analysis

Introduction

The HP E2441B VME/VXI Bus Preprocessor Interface board can also be used for timing analysis. This chapter explains how to configure the HP E2441B VME/VXI Bus Preprocessor Interface for timing analysis of a VME/VXI bus system using "B" or "C" size cards.

Pods 1 through 5 on the preprocessor interface carry state or timing information; the function is selected with the State/Timing switch. Pod 6 is only used for timing.

Note 

With the five-pod logic analyzers, the upper sixteen address bits (A31 through A16) are not observed during timing analysis. If you want to observe these bits, substitute Pod 4 for another pod, and reconfigure the Format menu on the logic analyzer.

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2441B VME/VXI Bus Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

1. Set the State/Timing switch to the top (Timing) position for timing analysis (see figure 1-1).
2. Set jumpers across pins 1 and 2 of jumpers J2 through J6 if the daisy chain on signals BG3IN* through BG0IN* and IACK* need to continue to the next slot (see page 1-4). Otherwise, set jumpers across pins 2 and 3. Note that if the preprocessor interface board is used as an extender, the jumpers must be set across pins 2 and 3.
3. Set jumper J1 to select BERR or IRQ1. The factory setting, and the configuration file, are set for BERR. If you select IRQ1, reassign the bit (see page 1-6).
4. Plug the logic analyzer cables into the preprocessor interface board (see table 3-1).
5. If you are installing the preprocessor interface board into a "C" size target system, remove the two board supports on the preprocessor interface board (see page 2-7).
6. Install the preprocessor interface board in the target system and, if necessary, plug the VME/VXI board into the preprocessor interface board (see page 3-4).
7. Load the logic analyzer configuration by loading the appropriate file from the preprocessor interface disk (see page 3-5).

Connecting to the HP E2441B

Connect the logic analyzer cables to the HP E2441B Preprocessor Interface pods as shown in table 3-1. Figure 2-2 (Chapter 2) shows the relative locations for the logic analyzer cards.

Table 3-1. Connections and Configuration Files (Timing Analysis)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A, HP 1650B, HP 16510A, HP 1652B and HP 16510B	CE2441T	P4	P5	**	P3	P2	P1
HP 16511B Master Card	DE2441T		--	--	--	--	--
HP 16511B Expander Card		P4	P5	**	P3	P2	P1
HP 16541A,D Exp. Card 1 *	EE2441				P6	P2	P1
HP 16540A,D Master Card							P5
HP 16541A,D Exp. Card 2 *					--	P4	P3
HP 16542A ***	GE2441T	Exp. 3 P6	Master P5	**	Exp. 4 P3	Exp. 1 P2	Exp. 2 P1
HP 16550A, HP 1660A/61A	FE2441	P6	P5	P4	P3	P2	P1

* For the HP 16541A,D Expander Cards, expansion card 1 is the physically highest HP 16541A,D card, and expansion card 2 is the next physically highest HP 16541A,D card (see figure 2-2).

** To see timing for the signals on the preprocessor interface P4, remove the logic analyzer cable from P2 and connect to P4.

*** For the locations of the HP 16542A cards, see figure 2-2.

Installing the HP E2441B

The HP E2441B Preprocessor Interface board can be installed in any slot of the VME/VXI bus system. It can be installed as a separate board or as an extender board in "B" size systems. The following steps explain how to install the HP E2441B Preprocessor Interface board in a "B" or "C" size target system:

Note If there are boards in higher number slots than the preprocessor interface board, refer to the section "Daisy-Chaining" on page 1-4 for information on setting the jumpers.

1. If the HP E2441B Preprocessor Interface board will be used as an extender board, remove the current VME/VXI board from its socket on the target system and store it in a protected environment.
2. If you are installing the preprocessor interface board into a "C" size target system, remove the two board supports from the preprocessor interface board (see figure 2-3).
3. Align the HP E2441B Preprocessor Interface board with the appropriate slot on the target system and plug the board into the connectors (see figure 2-3).

Note Do not use the HP E2441B Preprocessor Interface board as an extender board for VME/VXI "C" size systems.

4. If the HP E2441B Preprocessor Interface board is being used as an extender board in a "B" size target system, align the appropriate VME/VXI board with the slot on the end of the HP E2441B Preprocessor Interface board. Then plug the VME/VXI board into the connectors on the HP E2441B Preprocessor Interface board (see figure 2-3).

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for VME/VXI bus timing analysis by loading the appropriate VME/VXI bus configuration file. To load the configuration file:

1. Install the HP E2441B flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP 1650 series logic analyzers, select the I/O Disk Operations menu;
   - For the HP 16500 series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer with the appropriate configuration file from table 3-1.
4. For the HP 1660A/61A and HP 16500 series logic analyzers, select the configuration file with the knob, then touch "All" and select the correct module.
5. Execute the load operation to load the file into the logic analyzer.
6. For the HP 1660A/61A, HP 16540/16541A,D and HP 16550A Logic Analyzers, go to the "System Configuration" menu and select "Timing".

Timing Format Specification

When you use the VME/VXI Bus Preprocessor Interface for timing analysis, the format specification will be set up by the software as shown in figures 3-1 through 3-4.

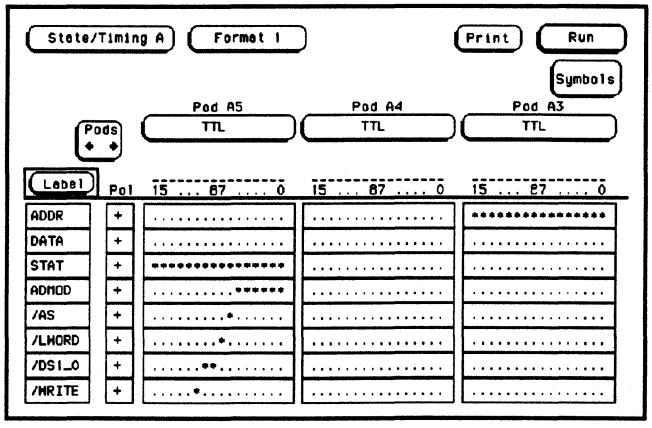

Figure 3-1. Timing Format Specification

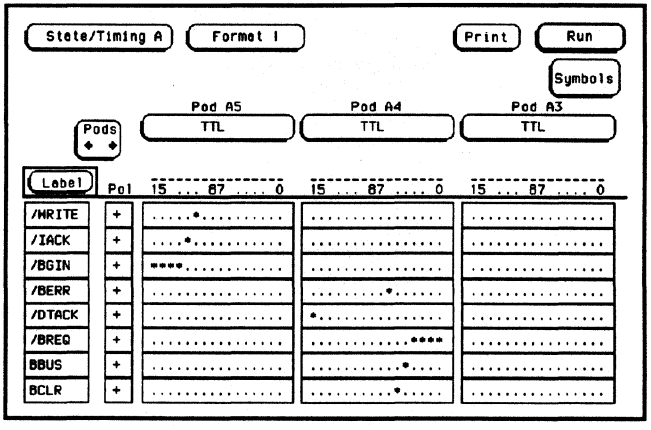

Figure 3-2. Timing Format Specification

Acquiring Data

Touch RUN and, as soon as there is activity on the bus, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer meets its trigger condition or when you touch STOP. The logic analyzer will flash "Waiting for Trigger" when data is not being transmitted across the bus.

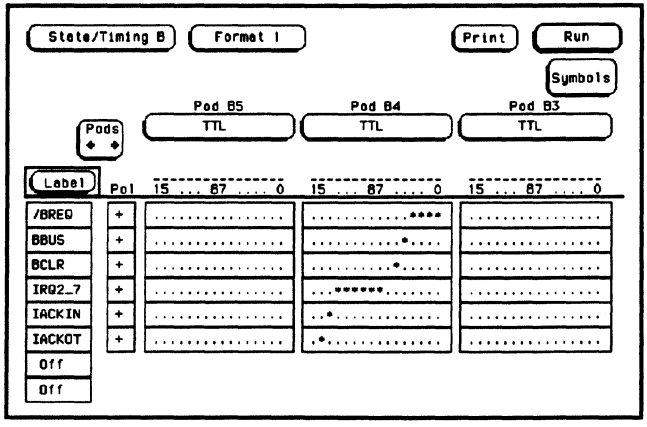

Figure 3-3. Timing Format Specification

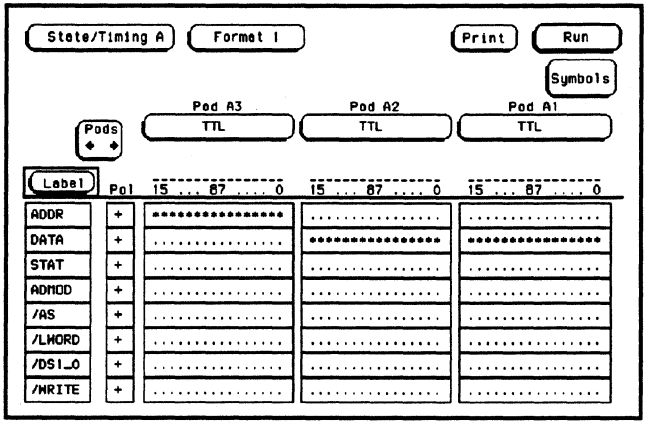

Figure 3-4. Timing Format Specification

Symbols

The configuration files set up symbol tables on the logic analyzer. The tables contain alphanumeric values which identify data patterns or ranges.

Table 3-2 lists the symbols for the /WRITE, /BREQ, AND IRQ2_7 labels. The patterns for each symbol listed in the tables are shown in the binary base. In the actual software, these patterns are listed in the hexadecimal base to conserve display space.

Table 3-2. Timing Symbols

Label	Symbol	Pattern
/WRITE	READ	1
	/WRITE	0
/BREQ	BRQ3	0 x x x
	BRQ2	1 0 x x
	BRQ1	1 1 0 x
	BRQ0	1 1 1 0
IRQ2_7	IRQ7	0 x x x x x
	IRQ6	1 0 x x x x
	IRQ5	1 1 0 x x x
	IRQ4	1 1 1 0 x x
	IRQ3	1 1 1 1 0 x
	IRQ2	1 1 1 1 1 0

Waveforms Menu

Captured data is displayed as shown in figure 3-5.

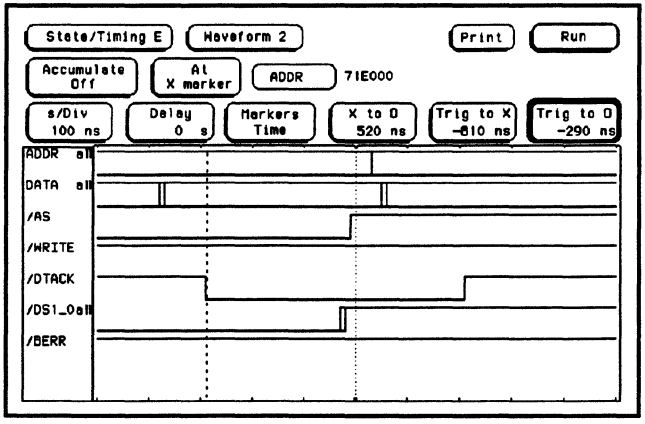

Figure 3-5. Waveforms Display

4

General Information

Introduction

This chapter provides additional reference information including the characteristics and signal connections for the HP E2441B VME/VXI Bus Preprocessor Interface.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2441B VME/VXI Bus Preprocessor Interface. These characteristics are included as additional information for the user.

Preprocessor Interface Compatibility: 16/32-bit VME/VXI bus systems using "B" or "C" size cards.

Standard Supported: VME Rev. C.1 (except for capacitive loading).
Standard VXI Revision 1.3 (except for capacitive loading).

Accessories Required: None.

Power Requirements: Maximum 600 mA at +5 volts from the logic analyzer.

Logic Analyzer Required: HP 1650A, HP 1650B, HP 1652B, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, HP 16550A, or HP 16561/2/3A.

Number of Probes Used: Five or six 16-channel probes.

Signal Line Loading: V_{IL} = –150 μA, plus 30 pF (maximum) on the following lines:

DTACK*, BERR*, DS0*, DS1*, WRITE*, AS*, BBSY*, BGIN(3:0)*

V_{IL} = –150 μA, plus 25 pF (maximum) on all other lines.

Note 

If the HP E2441B Preprocessor Interface board is used as an extender board, you must take into account any additional loading from the board that is installed in the HP E2441B Preprocessor Interface board.

Sampling Time: The following signals are sampled approximately 18 ns after AS goes low true: ADDRESS, ADDRESS MODIFIERS, LWORD and IACK.

The following signals are sampled approximately 18 ns after DS_A goes low true in a WRITE cycle or approximately 18 ns after DTACK goes low in a READ cycle: DATA, DS(1:0) and WRITE.

Timing Measurement Skew: All signals are passed through 74ACT573 buffers in the timing mode. The worst case published skew is 8 ns for these parts (typical skew is less than 4 ns).

Environmental Temperature:

Operating:	0 to +55° C (+32 to +131° F)
Nonoperating:	-40 to +75° C (-40 to +167° F)

Altitude:

Operating:	4,600 m (15,000 ft)
Nonoperating:	15,300 m (50,000 ft)

Humidity: Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation on the preprocessor interface.

Preprocessor Interface Description

The HP E2441B VME/VXI Bus Preprocessor Interface provides an interface between a VME/VXI bus system and the supported logic analyzers. Figure 4-1 shows the block diagram for the clocking circuitry and switches on the HP E2441B Preprocessor Interface.

The HP E2441B has two Programmed Logic Arrays that generate a latching strobe for the signal lines of the VME/VXI bus. The signals are latched into 74ACT573 transparent latches. When the STATE/TIMING switch is in the TIMING position, these latches are in the buffer mode and all signals flow straight through to the logic analyzer.

The on-board logic is an asynchronous state machine for the purpose of decoding address broadcast cycles, pipelined cycles, block transfers or single transfer cycles. This state machine also generates the Master Clock to the logic analyzer.

State/Timing Switch

There are four signals that change between the State and Timing modes. These are the BG_IN(3:0) lines on Pod 5, bits 12 through 15. These four lines are coded for the inverse assembler software in the State mode. In Timing mode, the BG_IN(3:0) lines are buffered straight through for timing analyses. The State/Timing switch selects the appropriate mode. Note that the switch must be in the correct position for proper operation.

The State/Timing switch changes four of the inputs to pod 5. In the State mode, the four most significant inputs to pod 5 are latched values of the Bus Grant lines, BERR, and DTACK. The four Bus Grant lines are priority encoded into two lines, to free up more state lines (see Chapter 2).

In the timing mode, the inputs to pod 5 are the actual BGxIN(3:0)* lines from the VME/VXI bus. These four lines are necessary in order to see the timing during a bus request operation.

Pod 6

Five-pod logic analyzers do not use P6 in the state mode. For timing measurements, P4 can be moved up to P6 to capture the signals available on P6 at the sacrifice of the upper 16 address lines A16 thru A31. In reality the user may sacrifice any of the pods for use in P6, but the pod assignments in the Format menu must match the connections.

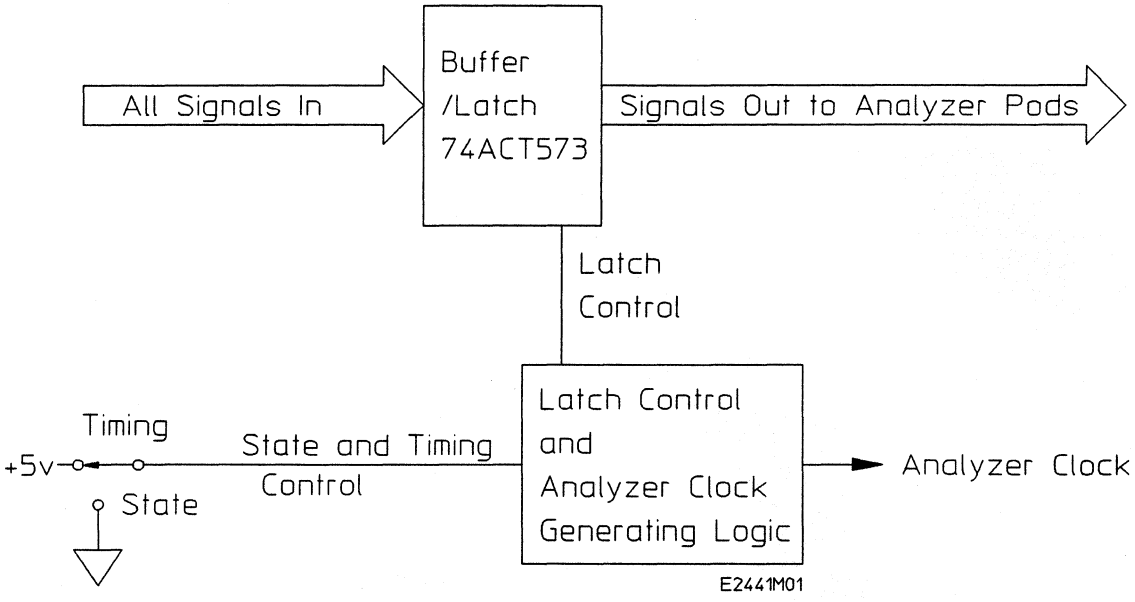

Figure 4-1. HP E2441B Block Diagram

Master Clock

The Master Clock is the falling edge of the J clock on pin 3 of Pod 1. In an address broadcast cycle, the Master Clock is generated when AS goes from low to high. In a Data Transfer cycle the Master Clock is generated when DTACK or BERR goes from low to high.

Signal Connections

The HP E2441B VME/VXI Bus Preprocessor Interface monitors 80 lines for state information and 96 lines for timing information. Table 4-1 lists the VME/VXI bus signals and connections for the logic analyzers.

Table 4-1. HP E2441B Signal Connections

HP E2441B Pod	Logic Analyzer Probe	VME/VXI Pin	Pin Mnemonic	Label
P1	0	J4-A1	D0	DATA
P1	1	J4-A2	D1	DATA
P1	2	J4-A3	D2	DATA
P1	3	J4-A4	D3	DATA
P1	4	J4-A5	D4	DATA
P1	5	J4-A6	D5	DATA
P1	6	J4-A7	D6	DATA
P1	7	J4-A8	D7	DATA
P1	8	J4-C1	D8	DATA
P1	9	J4-C2	D9	DATA
P1	10	J4-C3	D10	DATA
P1	11	J4-C4	D11	DATA
P1	12	J4-C5	D12	DATA
P1	13	J4-C6	D13	DATA
P1	14	J4-C7	D14	DATA
P1	15	J4-C8	D15	DATA
P2	0	J10-B14	D16	DATA
P2	1	J10-B15	D17	DATA
P2	2	J10-B16	D18	DATA
P2	3	J10-B17	D19	DATA
P2	4	J10-B18	D20	DATA
P2	5	J10-B19	D21	DATA
P2	6	J10-B20	D22	DATA
P2	7	J10-B21	D23	DATA

Table 4-1. HP E2441B Signal Connections (Continued)

HP E2441B Pod	Logic Analyzer Probe	VME/VXI Pin	Pin Mnemonic	Label
P2	8	J10-B23	D24	DATA
P2	9	J10-B24	D25	DATA
P2	10	J10-B25	D26	DATA
P2	11	J10-B26	D27	DATA
P2	12	J10-B27	D28	DATA
P2	13	J10-B28	D29	DATA
P2	14	J10-B29	D30	DATA
P2	15	J10-B30	D31	DATA
P3	0	*	A0	ADDR
P3	1	J4-A30	A1	ADDR
P3	2	J4-A29	A2	ADDR
P3	3	J4-A28	A3	ADDR
P3	4	J4-A27	A4	ADDR
P3	5	J4-A26	A5	ADDR
P3	6	J4-A25	A6	ADDR
P3	7	J4-A24	A7	ADDR
P3	8	J4-C30	A8	ADDR
P3	9	J4-C29	A9	ADDR
P3	10	J4-C28	A10	ADDR
P3	11	J4-C27	A11	ADDR
P3	12	J4-C26	A12	ADDR
P3	13	J4-C25	A13	ADDR
P3	14	J4-C24	A14	ADDR
P3	15	J4-C23	A15	ADDR

* This signal is generated on the preprocessor interface.

Table 4-1. HP E2441B Signal Connections (Continued)

HP E2441B Pod	Logic Analyzer Probe	VME/VXI Pin	Pin Mnemonic	Label
P4	0	J4-C22	A16	ADDR
P4	1	J4-C21	A17	ADDR
P4	2	J4-C20	A18	ADDR
P4	3	J4-C19	A19	ADDR
P4	4	J4-C18	A20	ADDR
P4	5	J4-C17	A21	ADDR
P4	6	J4-C16	A22	ADDR
P4	7	J4-C15	A23	ADDR
P4	8	J10-B4	A24	ADDR
P4	9	J10-B5	A25	ADDR
P4	10	J10-B6	A26	ADDR
P4	11	J10-B7	A27	ADDR
P4	12	J10-B8	A28	ADDR
P4	13	J10-B9	A29	ADDR
P4	14	J10-B10	A30	ADDR
P4	15	J10-B11	A31	ADDR
P5	0	J4-B16	AM0	STAT
P5	1	J4-B17	AM1	STAT
P5	2	J4-B18	AM2	STAT
P5	3	J4-B19	AM3	STAT
P5	4	J4-A23	AM4	STAT
P5	5	J4-C14	AM5	STAT
P5	6	J4-A18	AS	STAT
P5	7	J4-C13	LWORD	STAT

Table 4-1. HP E2441B Signal Connections (Continued)

HP E2441B Pod	Logic Analyzer Probe	VME/VXI Pin	Pin Mnemonic	Label
P5	8	J4-A13	DS0	STAT
P5	9	J4-A12	DS1	STAT
P5	10	J4-A14	WRITE	STAT
P5	11	J4-A20	IACK	STAT
P5	12	* / J4-B4	BG_PRI0 / BG0IN	STAT
P5	13	* / J4-B6	BG_PRI1 / BG1IN	STAT
P5	14	* / J4-B8	BERR_STATE / BG2IN	STAT
P5	15	* / J4-B10	DTACK_STATE / BG3IN	STAT
P6	0	J4-B12	BR0	(timing)
P6	1	J4-B13	BR1	(timing)
P6	2	J4-B14	BR2	(timing)
P6	3	J4-B15	BR3	(timing)
P6	4	J4-B1	BBSY	(timing)
P6	5	J4-B2	BCLR	(timing)
P6	6	J4-C11/B30 **	BERR/IRQ1 **	(timing)
P6	7	J4-B29	IRQ2	(timing)
P6	8	J4-B28	IRQ3	(timing)
P6	9	J4-B27	IRQ4	(timing)
P6	10	J4-B26	IRQ5	(timing)
P6	11	J4-B25	IRQ6	(timing)
P6	12	J4-B24	IRQ7	(timing)
P6	13	J4-A21	IACKIN	(timing)
P6	14	J4-A22	IACKOUT	(timing)
P6	15	J4-A16	DTACK	(timing)

* When the State/Timing Switch is in the State position, the signals listed to the left are generated by the preprocessor interface and displayed on the logic analyzer; when the switch is in the Timing position, the signals listed to the right are captured by the logic analyzer.

** This signal is determined by jumper J1 location (see Chapter 1).

Servicing

The repair strategy for the HP E2441B is board replacement. However, table 4-2 lists some mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Table 4-2. Replaceable Parts

HP Part Number	Description
E2441-66501	Circuit Board Assembly
1150-1817	Card Support Ejectors
1252-3743	Jumpers
0535-0069	Nut - Hex (for 96-pin header post)
0515-1908	Screw - 40-pin header post
0515-0678	Screw - 96-pin header post
3050-1239	Spacer for 40-pin header post
3101-0459	Switch
1252-2950	40-pin Eject Header
0590-1637	Threaded insert for cable clamp and 40-pin header post

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface may not be installed properly, or they may not be making electrical contact. Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500/16501 frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly, if there is no activity on the bus, or if the HP E2441B asynchronous circuitry is not recognizing valid bus activity. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in tables 2-2 or 3-2.

Slow Clock

If you have the preprocessor interface hooked up and running and observe a slow clock or no activity from the interface board, the +5 V supply coming from the analyzer may not be getting to the interface board.

To check the +5 V supply coming from the analyzer, disconnect one of the logic analyzer cables from the HP E2441B and measure across pins 1 and 2 or pins 39 and 40 (see figure A-1).

- If +5 V isn't observed across these pins, check the internal preprocessor fuse or current limiting circuit on the logic analyzer. For information on checking this fuse or circuit, refer to the service manual for your logic analyzer.
- If +5 V is observed across these pins and you feel confident that the +5 V is getting to the preprocessor interface, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the board.

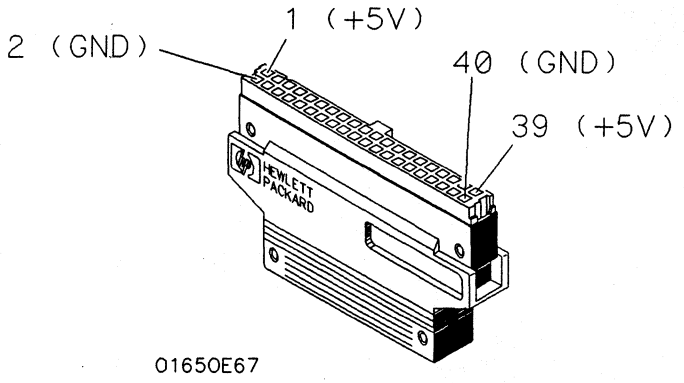

Figure A-1. Pinout of the Logic Analyzer Cable

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted.

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem.

Note 

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to <60 ns. If this error message is observed with the Clock Period set to >60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set, this message indicates:

- For an HP 16511B Logic Analyzer, only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."
- For an HP 1650A,B, HP 1652B, or HP 16510A,B Logic Analyzer, the pattern duration is probably set to less than (<) instead of greater than (>). Since a "don't care" pattern is always true, the "less than" condition is never satisfied. Set the trace menu correctly for the measurement that is desired.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/16541A,D)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D and HP 16541A,D cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.

Hewlett-Packard
Printed in the USA