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PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

2445
OSCILLOSCOPE
SERVICE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

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Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

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OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply and do not appear in this summary.

Terms in This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

Terms as Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the markings, or a hazard to property, including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

Symbols in This Manual

This symbol indicates where applicable cautionary or other information is to be found. For maximum input voltage see Table 1-1.

Symbols as Marked on Equipment

DANGER – High voltage.

Protective ground (earth) terminal.

ATTENTION – Refer to manual.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Power Cord

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

For detailed information on power cords and connectors see Table 2-1.

Use the Proper Fuse

To avoid fire hazard, use only a fuse of the correct type, voltage rating and current rating as specified in the parts list for your product.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Remove Covers or Panels

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICING SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

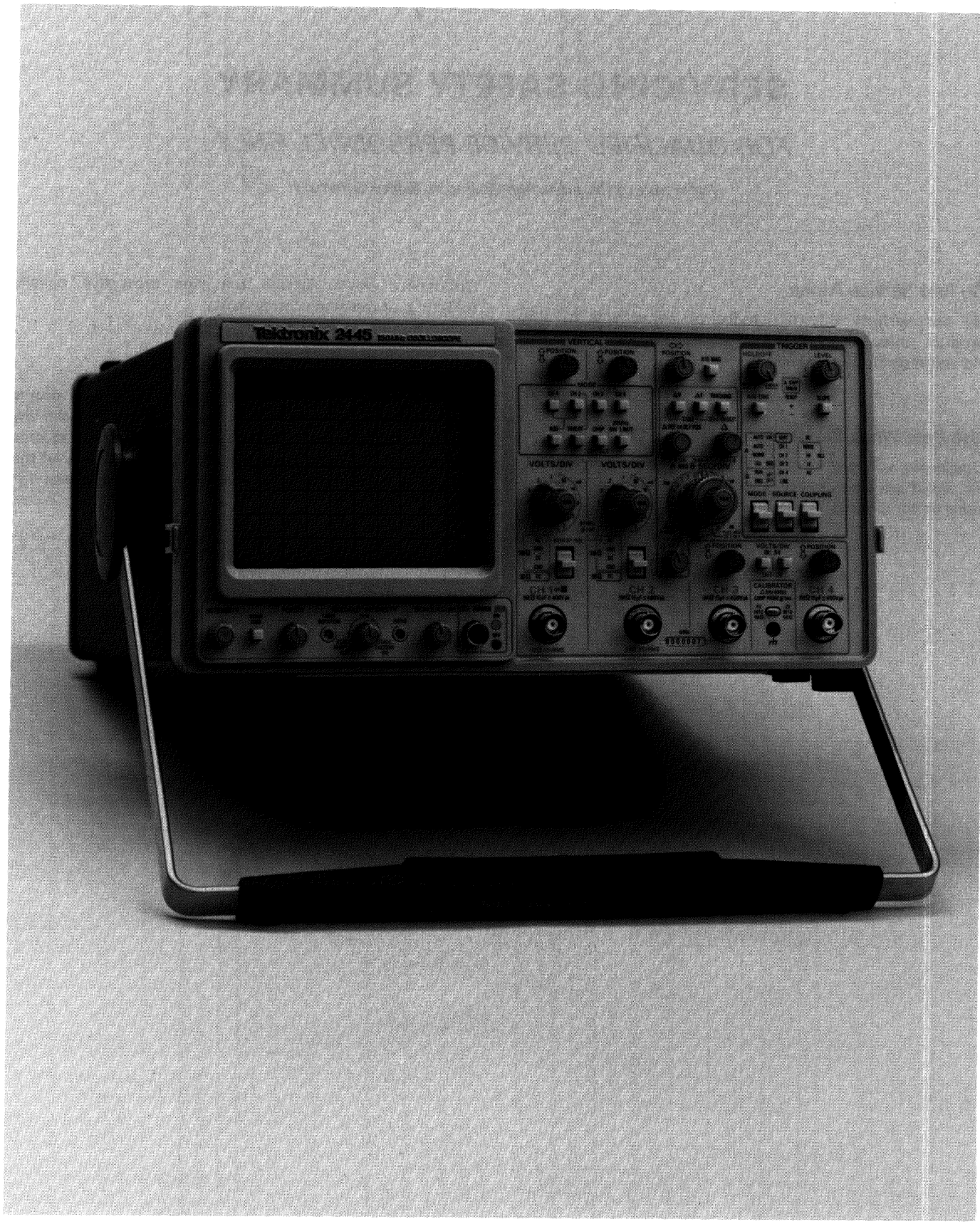
Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections or components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate from a power source that does not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



3829-01

The 2445 Oscilloscope.

SPECIFICATION

INTRODUCTION

The TEKTRONIX 2445 Oscilloscope is a portable 150-MHz instrument having a four-channel vertical deflection system. Channel 1 and Channel 2 provide calibrated deflection factors from 2 mV per division to 5 V per division. For each of these channels, input impedance is selectable between two values: either 1 MΩ in parallel with 15 pF, or 50 Ω internal termination. Input-signal coupling with 1-MΩ impedance can be selected as either AC or DC. Channel 3 and Channel 4 have deflection factors of either 0.1 V or 0.5 V per division. Each of these channels has an input impedance of 1 MΩ in parallel with 15 pF, with DC input-signal coupling. Trigger circuits enable stable triggering over the full bandwidth of the vertical system.

The horizontal deflection system provides calibrated sweep speeds from 1.5 s per division to 1 ns per division. Drive for the horizontal deflection system is obtained from a choice of A, B delayed, A alternated with B delayed sweeps, or CH 1 (for the X-Y display mode).

The 2445 incorporates alphanumeric crt readouts of the vertical and horizontal scale factors, the trigger levels, time-difference measurement values, voltage-difference measurement values, and certain auxiliary information.

The 2445 Oscilloscope is shipped with the following standard accessories:

2 Probe packages
1 Snap-lock accessories pouch
1 Zip-lock accessories pouch
1 Operators manual
1 Service manual
1 Power cord (installed)
1 2-A, 250-V fuse
1 Clear plastic crt filter
1 Blue plastic crt filter (installed)
1 Front-panel cover
1 Operators pocket reference guide

For part numbers and further information about both standard and optional accessories, refer to either "Options and Accessories" (Section 7) in the Operators manual or the Accessories information at the rear of this manual. Your Tektronix representative or local Tektronix Field Office can also provide accessories information and ordering assistance.

PERFORMANCE CONDITIONS

The following electrical characteristics (Table 1-1) are valid for the 2445 when it has been adjusted at an ambient temperature between +20°C and +30°C, has had a warm-up period of at least 20 minutes, and is operating at an ambient temperature between −15°C and +55°C (unless otherwise noted).

Items listed in the "Performance Requirements" column are verifiable qualitative or quantitative limits that define the measurement capabilities of the instrument.

Environmental characteristics are given in Table 1-2. The 2445 Oscilloscope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style C equipment; tested as per paragraph 4.5.5.1.2.2 for humidity, 4.5.5.1.3 for low temperature, and 4.5.5.1.4 for high temperature.

Mechanical characteristics of the 2445 are listed in Table 1-3.

Table 1-1

Electrical Characteristics

Characteristics	Performance Requirements
VERTICAL DEFLECTION SYSTEM–CHANNEL 1 AND CHANNEL 2	
Deflection Factor	
Range	2 mV per division to 5 V per division in a 1-2-5 sequence of 11 steps.
Accuracy	
+15°C to +35°C	Within ±2% at any VOLTS/DIV setting for a 4- or 5-division signal centered on the screen.
−15°C to +15°C and +35°C to +55°C	Add 1% to +15°C-to-+35°C specification.[a]
ΔV Accuracy (using cursors over entire graticule area)	
+15°C to +35°C	± (1.25% of reading + 0.03 division + signal aberrations).
−15°C to +15°C and +35°C to +55°C	Add 1% of reading to +15°C-to-+35°C specification.[a]
ΔV Range	± 8 times the VOLTS/DIV switch setting.[a]
Variable Range	Continuously variable between VOLTS/DIV switch settings. Extends deflection factor of the 5 V per division setting to at least 12.5 V per division.
Frequency Response	Six-division reference signal from a terminated 50-Ω system, with VAR VOLTS/DIV control in calibrated detent.

	VOLTS/DIV setting	**−3 dB bandwidth with standard-accessory probe or internal 50-Ω termination**	**−4.7 dB bandwidth with 50-Ω external termination on 1-MΩ input**
−15°C to +55°C	2 mV	DC to 80 MHz	DC to 80 MHz[a]
−15°C to +35°C	5 mV or greater	DC to 150 MHz	DC to 150 MHz[a]
+35°C to +55°C	5 mV or greater	DC to 100 MHz[a]	DC to 100 MHz[a]

AC Coupled Lower −3 dB Point	
1X Probe	10 Hz or less.[a]
10X Probe	1 Hz or less.
Step Response	
Rise Time	2.33 ns or less for VOLTS/DIV switch settings of 5 mV and up (calculated).[a] 4.4 ns or less for VOLTS/DIV switch setting of 2 mV (calculated).[a] Rise time calculated from: bandwidth x rise time = 0.35.

[a]**Performance Requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
VERTICAL DEFLECTION SYSTEM—CHANNEL 1 AND CHANNEL 2 (cont)	
Common-mode Rejection Ratio (CMRR)	At least 20:1 at 50 MHz for common-mode signals of eight divisions or less, with VAR VOLTS/DIV control adjusted for best CMRR at 50 kHz at any VOLTS/DIV switch setting from 5 mV to 5 V; at least 20:1 at 20 MHz at 2 mV per division.
Channel Isolation	100:1 or greater attenuation of the deselected channel at 100 MHz; 50:1 or greater attenuation at 150 MHz, for an eight-division input signal from 2 mV per division to 500 mV per division, with equal VOLTS/DIV switch settings on both channels.
Displayed Channel 2 Signal Delay with Respect to Channel 1 Signal	Adjustable through a range of at least −500 ps to +500 ps.
Input R and C (1 MΩ)	
Resistance	1 MΩ ±0.5%.[a]
Capacitance	15 pF ±2 pF.[a]
Maximum Input Voltage ⚠	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
Input R (50 Ω)	
Resistance	50 Ω ±1%.[a]
VSWR (DC to 150 MHz)	1.3:1 or less.[a]
Maximum Input Voltage ⚠	5 V rms; 0.5 W·seconds during any 1-s interval for instantaneous voltage from 5 V to 50 V.
Cascaded Operation	CH 2 SIGNAL OUT into Channel 1 input; DC coupled using a 50-Ω RG-58C/U coaxial cable, terminated in 50 Ω at the Channel 1 input. Channel 1 and Channel 2 VOLTS/DIV switch set to 2 mV.
Bandwidth	Dc to 50 MHz or greater.
Deflection Factor	400 μV per division ±10%.
VERTICAL DEFLECTION SYSTEM—CHANNEL 3 AND CHANNEL 4	
Deflection Factor	
Values	0.1 V per division and 0.5 V per division.
Accuracy	Within ±10%.
Frequency Response	Six-division reference signal, from a terminated 50-Ω system.

−3 dB Bandwidth with standard accessory probe	**−4.7 dB Bandwidth with external 50-Ω termination**
DC to 150 MHz	DC to 150 MHz

[a] **Performance Requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
VERTICAL DEFLECTION SYSTEM—CHANNEL 3 AND CHANNEL 4 (cont)	
Step Response	
Rise Time	2.33 ns or less (calculated from bandwidth).[a]
Channel Isolation	50:1 or greater attenuation of the deselected channel at 100 MHz with an eight-division input signal.
Input R and C	
Resistance	1 MΩ ±1%.[a]
Capacitance	15 pF ±3 pF.[a]
Maximum Input Voltage ⚠	400 V (dc + peak ac); 800 V p-p ac at 10 kHz or less.[a]
VERTICAL DEFLECTION SYSTEM—ALL CHANNELS	
Low-frequency Linearity	0.1 division or less compression or expansion of a two-division, center-screen signal when positioned anywhere within the graticule area.
Bandwidth Limiter	Reduces upper 3-dB bandpass to a limit of 13 MHz to 24 MHz.
Vertical Signal Delay	At least 20 ns of the sweep is displayed before the triggering event is displayed.[a]
Chopped Mode Switching Rate	Vertical display switches sequentially through the selected channels at the chop switching rate. If the B SEC/DIV switch is set to sweep speeds outside the range of 20 μs per division to 2 μs per division, the switching rate is 1 MHz ±0.2% (dual-channel cycle rate of 500 kHz). If the B SEC/DIV switch is set within the range of 20 μs per division to 2 μs per division, the switching rate is 2.5 MHz ±0.2% (dual-channel cycle rate of 1.25 MHz). At all sweep speeds, the chop switching rate is desynchronized with the sweep frequency to minimize waveform breaks when viewing repetitive signals.[a]
TRIGGERING	
Minimum P-P Signal Amplitude for Stable Triggering from Channel 1 or Channel 2 Source	
DC Coupled	0.35 division from dc to 50 MHz, increasing to 1 division at 250 MHz.
NOISE REJ Coupled	1.2 divisions or less from dc to 50 MHz, increasing to 3 divisions at 250 MHz.
AC Coupled	0.35 division from 60 Hz to 50 MHz, increasing to 1 division at 250 MHz. Attenuates signals below 60 Hz.
HF REJ Coupled	0.5 division from dc to 30 kHz.
LF REJ Coupled	0.5 division from 80 kHz to 50 MHz, increasing to 1 division at 250 MHz.

[a]Performance Requirement not checked in manual.

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING (cont)	
Minimum P-P Signal Amplitude for Stable Triggering from Channel 3 or Channel 4 Source	Amplitudes are one-half of Channel 1 or Channel 2 source specification.
Minimum P-P Signal Amplitude for Stable Triggering from Composite, Multiple Channel Source in ALT Vertical Mode	Add 1 division to single-channel source specifications.
Maximum P-P Signal Rejected by NOISE REJ COUPLING for Signals Within the Vertical Bandwidth	
Channel 1 or Channel 2 Source	0.4 division or greater for VOLTS/DIV switch settings of 10 mV and higher.
Channel 3 or Channel 4 Source	0.2 division or greater.
Jitter	Less than 100 ps at 150 MHz with A and B SEC/DIV switch set to 10 ns and X10 MAG on.
LEVEL Control Range	
Channel 1 or Channel 2 Source	± 18 times the VOLTS/DIV switch setting.[a]
Channel 3 or Channel 4 Source	± 9 times the VOLTS/DIV switch setting.[a]
LEVEL Control Readout Accuracy (for triggering signals with transition times greater than 20 ns)	
Channel 1 or Channel 2 Source	
DC Coupled	
+15°C to +35°C	Within ± [3% of setting + 3% of p-p signal + 0.2 division + (0.5 mV x probe attenuation factor)].
−15°C to +55°C (excluding +15°C to +35°C)	Add (1.5 mV x probe attenuation factor) to the specification listed for +15°C to +35°C.[a]
NOISE REJ Coupled	Add ±0.6 division to the DC Coupled specification.
Channel 3 or Channel 4 Source	
DC Coupled	Within ± [3% of setting + 4% of p-p signal + 0.1 division + (0.5 mV x probe attenuation factor)].
NOISE REJ Coupled	Within ± [3% of setting + 4% of p-p signal + 0.4 division + (0.5 mV x probe attenuation factor)].
SLOPE Selection	Conforms to trigger-source waveform or ac power-source waveform.
AUTO LVL Mode Maximum Triggering Signal Period	
A SEC/DIV Switch Setting Less than 10 ms	At least 20 ms.[a]
A SEC/DIV Switch Setting from 10 ms to 50 ms	At least four times the A SEC/DIV switch setting.[a]
A SEC/DIV Switch Setting from 100 ms to 500 ms	At least 200 ms.[a]

[a]**Performance Requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
TRIGGERING (cont)	
AUTO Mode Maximum Triggering Signal Period	
A SEC/DIV Switch Setting Less than 10 ms	At least 80 ms.[a]
A SEC/DIV Switch Setting from 10 ms to 50 ms	At least 16 times the A SEC/DIV switch setting.[a]
A SEC/DIV Switch Setting from 100 ms to 500 ms	At least 800 ms.[a]
AUTO LVL Mode Trigger Acquisition Time	Eight to 100 times the AUTO LVL Mode maximum triggering-signal period, depending on the triggering-signal period and waveform.[a]
HORIZONTAL DEFLECTION SYSTEM	
A Sweep Time Base Range	1 s per division to 10 ns per division in a 1-2-5 sequence of 25 steps. X10 MAG feature extends maximum sweep speed to 1 ns per division.
B Sweep Time Base Range	50 ms per division to 10 ns per division in a 1-2-5 sequence of 21 steps. X10 MAG feature extends maximum sweep speed to 1 ns per division.
SEC/DIV VAR Control	Continuously variable and calibrated between settings of the SEC/DIV switch. Extends slowest A Sweep speed to 1.5 s per division. Operates in conjunction with the A SEC/DIV switch when A and B are locked together; operates in conjunction with the B SEC/DIV switch when A and B are not locked together.
Timing Accuracy (+15°C to +35°C, SEC/DIV switch set to 0.1 s per division or less)	
A and B Sweep Accuracy, Time Intervals Measured at Vertical Center with SEC/DIV VAR Control in Detent	**Unmagnified**: ± (0.7% of time interval + 0.6% of full scale). **Magnified**: ± (1.2% of time interval + 0.6% of full scale).
	0.6% of full scale is 0.06 division.
Δt Accuracy, Time Intervals Measured with Cursors, Anywhere on the Graticule (A Sweep Only)	**Unmagnified**: ± (0.5% of time interval + 0.3% of full scale). **Magnified**: ± (1% of time interval + 0.3% of full scale).
Δt Accuracy, Time Intervals Measured with Delayed B Sweep with Both Delays Set at 1% or More of Full Scale from Minimum Delay (no ? displayed in readout)	± (0.3% of time interval + 0.1% of full scale).
Delay Accuracy, A Sweep Trigger Point to Start of B Sweep	± (0.3% of delay setting + 0.6% of full scale) +0 to −25 ns.
Timing Accuracy (A SEC/DIV switch set to 0.5 s or 0.2 s per division)	Add ±0.5% of time interval to all accuracy specifications.

[a]**Performance Requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
HORIZONTAL DEFLECTION SYSTEM (cont)	
Timing Accuracy (A SEC/DIV switch set to 1 s per division)	Add ±2% of time interval to all accuracy specifications.
Timing Accuracy (SEC/DIV VAR control out of detent)	Add 2% of time interval to the A and B Sweep Accuracy specification.
Timing Accuracy (−15°C to +15°C and +35°C to +55°C)	Add ±0.2% of time interval to all Δt and delay specifications. Add ±0.5% of time interval to A and B Sweep accuracy specifications.[a]
Δt Readout Resolution	Greater of either 20 ps or 0.025% of full scale.[a]
Δt Range	± 10 times the A SEC/DIV switch setting.[a]
Delay Pickoff Jitter	Within 0.004% (one part or less in 25,000) of the maximum available delay, plus 100 ps.
Delay Time Position Range	0 to 9.95 times the A SEC/DIV switch setting. Main sweep triggering event is observable on delayed sweep with zero delay setting.[a]
X-Y Operation	
X-Axis Deflection Factor	
Range	Same as Channel 1.[a]
Accuracy	Same as Channel 1.
Variable Range	Same as Channel 1.[a]
X-Axis Bandwidth	Dc to 3 MHz.
Input R and C	Same as Channel 1.[a]
Phase Difference Between X and Y with Normal Bandwidth	1° or less from dc to 1 MHz; 3° or less from 1 MHz to 2 MHz.
X-Axis Low-Frequency Linearity	0.2 division or less compression or expansion of a two-division, center-screen signal when positioned within the display area.
CURSOR AND FRONT-PANEL DISPLAY	
Cursor Position Range	
Delta Volts (ΔV)	At least the center 7.6 vertical divisions.
Delta Time (Δt)	At least the center 9.6 horizontal divisions.
Minimum Setup Time Required to Maintain Front-panel Settings at Power-down	10 seconds or less.[a]

[a]**Performance Requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
Z-AXIS INPUT	
Sensitivity	
Dc to 2 MHz	Positive voltage decreases intensity; +2 V blanks a maximum-intensity trace.
2 MHz to 20 MHz	+2 V modulates a normal-intensity trace.[a]
Input Resistance	9 kΩ ±10%.[a]
Maximum Input Voltage ⚠	±25 V peak; 25 V p-p ac at 10 kHz or less.[a]
SIGNAL OUTPUTS	
CALIBRATOR (A SEC/DIV switch set to 1 ms per division)	
Voltage	
1 MΩ Load	0.4 V ±1%.
50 Ω Load	0.2 V ±1.5%.[a]
Current (short-circuit load)	8 mA ±1.5%.[a]
Repetition Period	Two times the A SEC/DIV switch setting within the range of 200 ns to 200 ms.
Accuracy	±0.1% during sweep time.
Symmetry	Duration of high portion of output cycle is 50% of output period ± (lesser of 500 ns or 25% of period).[a]
Jitter of Pulse Period or Pulse Width	10 ns or less.[a]
CH 2 SIGNAL OUT	
Output Voltage	20 mV per division ±10% into 1 MΩ; 10 mV per division ±10% into 50 Ω.
Offset	±5 mV into 50 Ω, when dc balance has been performed within ±5°C of the operating temperature.
A GATE OUT and B GATE OUT	
Output Voltage	2.4 V to 5 V positive-going pulse, starting at 0 V to 0.4 V.
Output Drive	Will supply 400 μA during HI state; will sink 2 mA during LO state.[a]

[a]**Performance Requirement not checked in manual.**

Table 1-1 (cont)

Characteristics	Performance Requirements
CRT	
Display	80 mm x 100 mm.[a]
Standard Phosphor	P31.[a]
Nominal Accelerating Potential	16 kV.[a]
AC POWER SOURCE	
Source Voltage	
Ranges	
115 V	90 V to 132 V.[a]
230 V	180 V to 250 V.[a]
Source Frequency	48 Hz to 440 Hz.[a]
Fuse Rating	2 A, 250 V, AGC/3AG, Fast blow; or 1.6 A, 250 V, 5 x 20 mm, Quick-acting (F).[a]
Power Consumption	
Typical	70 W (140 VA).[a]
Maximum	120 W (180 VA).[a]
Primary Circuit Dielectric Voltage Withstand Test	1500 V rms, 60 Hz for 10 s without breakdown.[a]
Primary Grounding	Type test to 0.1 Ω maximum. Routine test to check grounding continuity between chassis ground and protective earth ground.[a]

[a]**Performance Requirement not checked in manual.**

Table 1-2

Environmental Characteristics

Characteristics	Performance Requirements
	The 2445 Oscilloscope meets the environmental requirements of MIL-T-28800C for Type III, Class 3, Style C equipment; tested as per paragraph 4.5.5.1.2.2 for humidity, 4.4.5.1.3 for low temperature, and 4.5.5.1.4 for high temperature.
Temperature	
Operating	−15°C to +55°C.
Nonoperating (storage)	−62°C to +85°C.
Altitude	
Operating	To 15,000 ft. Maximum operating temperature decreases 1°C for each 1,000 ft above 5,000 ft.
Nonoperating (storage)	To 50,000 ft.
Humidity (operating and nonoperating)	Stored at 95% relative humidity for five cycles (120 hours) from 30°C to 60°C, with operational performance checks at 30°C and 55°C.
Vibration (operating)	15 minutes along each of three axes at a total displacement of 0.025 inch p-p (4 g at 55 Hz), with frequency varied from 10 Hz to 55 Hz in one-minute sweeps. Held 10 minutes at each major resonance, or if none existed, held 10 minutes at 55 Hz (75 minutes total test time).
Shock (operating and nonoperating)	50 g, half-sine, 11-ms duration, three shocks on each face, for a total of 18 shocks.
Transit Drop (not in shipping package)	12-inch drop on each corner and each face (MIL-T-28800C, paragraph 3.9.5.2 and 4.5.5.4.2).
Bench Handling (with and without cabinet installed)	MIL-STD-810C, Method 512.2, Procedure V (MIL-T-28800C, paragraph 4.5.5.4.3).
EMI (electromagnetic interference)	Meets MIL-T-28800C; MIL-STD-461B, part 4 (CE-03 and CS-02), part 5 (CS-06 and RS-02), and part 7 (CS-01, RE-02, and RS-03—limited to 1 GHz); VDE 0871, Catagory B; Part 15 of FCC Rules and Regulations, Subpart J, Class A; and Tektronix Standard 062-2866-00.
Topple (operating with cabinet installed)	Set on rear feet and allowed to topple over onto each of four adjacent faces.
Packaged Transportation Drop	Meets the limits of the National Safe Transit Association test procedure 1A-B-2; 10 drops of 36 inches.
Packaged Transportation Vibration	Meets the limits of the National Safe Transit Association test procedure 1A-B-1; excursion of 1 inch p-p at 4.63 Hz (1.1 g) for 30 minutes.

Table 1-3

Mechanical Characteristics

Characteristics	Description
Weight	
With Accessories and Pouch	10.2 kg (22.4 lb).
Without Accessories and Pouch	9.3 kg (20.5 lb).
Domestic Shipping Weight	12.8 kg (28.2 lb).
Height	
With Feet and Accessories Pouch	190 mm (7.5 in).
Without Accessories Pouch	160 mm (6.3 in).
Width (with handle)	330 mm (13.0 in).
Depth	
With Front-Panel Cover	434 mm (17.1 in).
With Handle Extended	505 mm (19.9 in).
Cooling	Forced-air circulation.
Finish	Tektronix Blue vinyl-clad material on aluminum cabinet.
Construction	Aluminum alloy chassis (sheet metal). Plastic laminate front panel. Glass laminate circuit boards.

OPERATING INFORMATION

This section of the manual provides information on instrument installation and power requirements; and the functions of controls, connectors, and indicators are described. Operating considerations, intended to familiarize the operator with basic measurement techniques, and operator's checks and adjustments for the 2445 are included. For additional operating information, refer to the 2445 Operators Manual.

PREPARATION FOR USE

SAFETY CONSIDERATIONS

Refer to the Safety Summaries at the front of this manual for power source, grounding, and other safety considerations pertaining to the use of the instrument. Before connecting the oscilloscope to a power source, read entirely both this section and the Safety Summaries.

CAUTION

This instrument may be damaged if operated with the LINE VOLTAGE SELECTOR switch set for the wrong applied ac input-source voltage or if the wrong line fuse is installed.

LINE VOLTAGE SELECTION

The 2445 operates from either a 115-V or a 230-V nominal ac power-input source having line frequency ranging from 48 Hz to 440 Hz. Before connecting the power cord to a power-input source, verify that the LINE VOLTAGE SELECTOR switch, located on the rear panel (see Figure 2-1), is set for the correct nominal ac input-source voltage. To convert the instrument for operation from one line-voltage range to the other, move the LINE VOLTAGE SELECTOR switch to the correct nominal ac source-voltage setting (see Table 2-1). The detachable power cord may have to be changed to match the particular power-source output.

LINE FUSE

To verify that the instrument power-input fuse is of proper value for the nominal ac source voltage selected, perform the following procedure:

1. Press in the fuse-holder cap and release it with a slight counterclockwise rotation.
2. Pull the cap (with the attached fuse inside) out of the fuse holder.
3. Verify proper fuse value (see Table 2-1).
4. Install the proper fuse and reinstall the fuse-holder cap.

NOTE

The two types of fuses listed are not directly interchangeable; they require different types of fuse caps.

POWER CORD

This instrument has a detachable, three-wire power cord with a three-contact plug for connection to both the power source and protective ground. The power cord is secured to the rear panel by a cord-set-securing clamp. The protective-ground contact on the plug connects (through the power-cord protective grounding conductor) to the accessible metal parts of the instrument. For electrical-shock protection, insert this plug into a power-source outlet that has a properly grounded protective-ground contact.

Instruments are shipped with the required power cord as ordered by the customer. Available power-cord information is presented in Table 2-1. Part numbers are listed both in the "Accessories" information at the rear of this manual and in the "Options and Accessories" section of the Operators Manual (Section 7). Contact your Tektronix representative or local Tektronix Field Office for additional power-cord information.

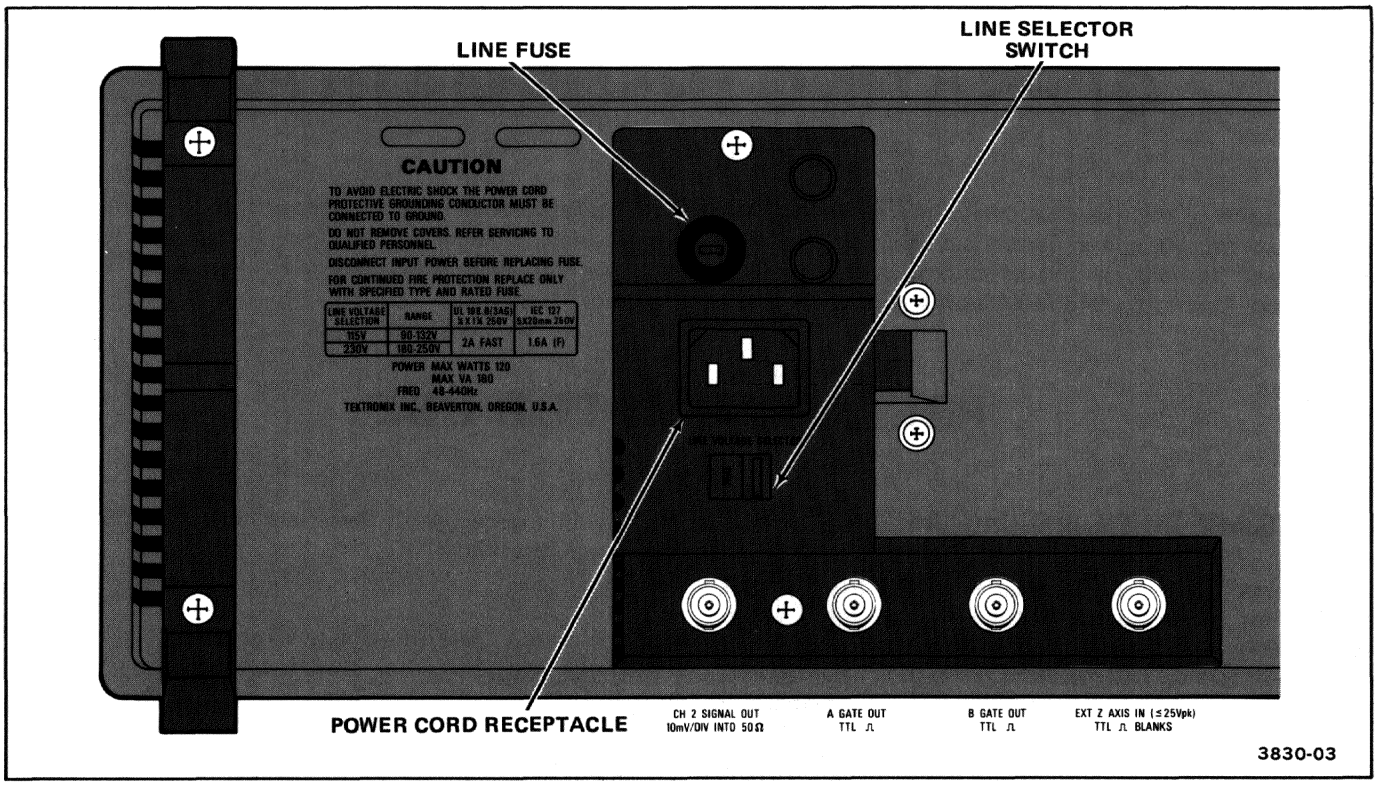


Figure 2-1. Line selector switch, line fuse, and detachable power cord.

INSTRUMENT COOLING

To prevent instrument damage from overheated components, adequate internal airflow must be maintained at all times. Before turning on the power, first verify that both the air-intake holes on the bottom of the cabinet and the fan-exhaust holes in the rear panel are free of any obstruction to airflow.

START-UP

The 2445 automatically performs power-up tests each time the instrument is turned on. The purpose of these tests is to provide the user with the highest possible confidence level that the instrument is fully functional. If no faults are encountered, the power-up tests normally will be completed in under five seconds, after which the instrument will enter the normal operating mode. A failure of any of the power-up tests will be indicated by either a flashing TRIG'D indicator on the instrument front panel or a bottom-line readout on the crt in the form: **TEST XX FAIL YY** (where XX is the test number and YY is the failure code of the failed test).

If a failure of any power-up test occurs, the instrument may still be usable for some applications. To put the instrument into the operating mode after a power-up test failure, press the A/B TRIG button. If the instrument then functions for your particular measurement requirement, it may be used, but refer it to a qualified service technician for repair of the problem at the earliest convenience. Additional information on the power-up tests may be found in the "Maintenance" section of this manual and in Appendix A of the Operators Manual. Consult your service department, your local Tektronix Service Center, or nearest Tektronix representative if additional assistance is needed.

REPACKAGING FOR SHIPMENT

If this instrument is to be shipped by commercial transportation, it is recommended that it be packaged in the original manner. The carton and packaging material in which your instrument was shipped to you should be saved and used for this purpose.

If the original packaging is unfit for use or is not available, repackage the instrument as follows:

1. Obtain a corrugated cardboard shipping carton having inside dimensions at least six inches greater than the instrument dimensions and having a carton test strength of at least 275 pounds.

2. If the instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the following: owner of the instrument (with address), the name of a person at your firm who can be contacted, complete instrument type and serial number, and a description of the service required.

3. Wrap the instrument with polyethylene sheeting or equivalent to protect the outside finish and prevent entry of packing materials into the instrument.

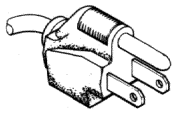
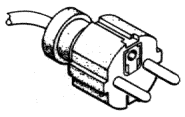
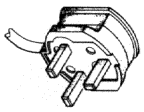
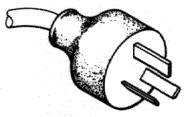
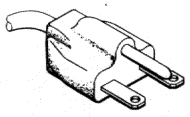
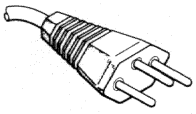
4. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between the carton and the instrument, allowing three inches on each side.

5. Seal the carton with shipping tape or with an industrial stapler.

6. Mark the address of the Tekronix Service Center and your return address on the carton in one or more prominent locations.

Table 2-1

Voltage, Fuse, and Power-Cord Data

Plug Configuration	Category	Power Cord And Plug Type	Line Voltage Selector Setting	Voltage Range (AC)	Factory Installed Instrument Fuse	Fuse Holder Cap	Reference Standards[b]
	U.S. Domestic Standard	U.S. 120V 15A	115V	90V to 132V	2A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.11 NEMA 5-15-P IEC 83 UL 198.6
	Option A1	EURO 240V 10-16A	230V	180V to 250V	1.6A, 250V 5x20 mm Quick-Acting (F) (IEC 127)	5×20 mm	CEE(7), II, IV, VII IEC 83 IEC 127
	Option A2	UK[a] 240V 6A	230V	180V to 250V	1.6A, 250V 5x20 mm Quick-Acting (F) (IEC 127)	5×20 mm	BS 1363 IEC 83 IEC 127
	Option A3	Australian 240V 10A	230V	180V to 250V	1.6A, 250V 5x20 mm Quick-Acting (F) (IEC 127)	5×20 mm	AS C112 IEC 127
	Option A4	North American 240V 15A	230V	180V to 250V	2A, 250V AGC/3AG Fast-blow (UL 198.6)	AGC/3AG	ANSI C73.20 NEMA 6-15-P IEC 83 UL 198.6
	Option A5	Switzerland 220V 6A	230V	180V to 250V	1.6A, 250V 5x20 mm Quick-Acting (F) (IEC 127)	5×20 mm	SEV IEC 127

[a] **A 6A, Type C fuse is also installed inside the plug of the Option A2 power cord.**

[b] **Reference Standards Abbreviations:**

ANSI—American National Standards Institute
AS—Standards Association of Australia
BS—British Standards Institution
CEE—International Commission on Rules for the Approval of Electrical Equipment
IEC—International Electrotechnical Commission
NEMA—National Electrical Manufacturer's Association
SEV—Schweizevischer Elektrotechischer Verein
UL—Underwriters Laboratories Inc.

3832-02

CONTROLS, CONNECTORS, AND INDICATORS

The following descriptions are intended to familiarize the operator with the location and function of the instrument's controls, connectors, and indicators.

POWER AND DISPLAY

Refer to Figure 2-2 for location of items 1 through 9.

(1) **INTENSITY Control**—Adjusts brightness of the crt trace display. This control does not affect intensity of the crt readout display.

(2) **BEAM FIND Switch**—When held in, compresses the display to within the graticule area. Aids the operator in locating off-screen displays.

(3) **FOCUS Control**—Adjusts the display for optimum definition.

(4) **TRACE ROTATION Control**—Operator-adjusted screwdriver control used to align the crt trace with the horizontal graticule lines. Once adjusted, it does not require readjustment during normal operation of the instrument.

(5) **READOUT INTENSITY Control**—Adjusts the intensity of the crt readout display. This control is also used to either enable or disable the scale-factor display. Setting the control to MIN reduces the readout intensity to minimum. Clockwise rotation from midrange increases the readout intensity and enables the scale-factor display; counterclockwise rotation from midrange also increases the intensity but disables the scale-factor display. Delta Volts and Delta Time readouts and control messages will continue to be enabled even when the scale-factor display is disabled.

(6) **ASTIG Control**—Operator-adjusted screwdriver control used in conjunction with the FOCUS control to obtain a well-defined display over the entire graticule area. Once adjusted, it does not require readjustment during normal operation of the instrument.

(7) **SCALE ILLUM Control**—Adjusts the light level of the graticule illumination.

(8) **POWER Switch**—Turns instrument power on and off. Press in for ON; press again for OFF. An internal indicator in the switch shows green when the switch is on and black when it is off. Front-panel settings that were unchanged for at least 10 seconds prior to power-off will be returned when power is reapplied to the instrument.

(9) **CRT**—Has an 80-mm vertical and 100-mm horizontal display area. Internal graticule lines eliminate parallax-viewing error between the trace and the graticule lines. Rise-time measurement points are indicated at the left edge of the graticule.

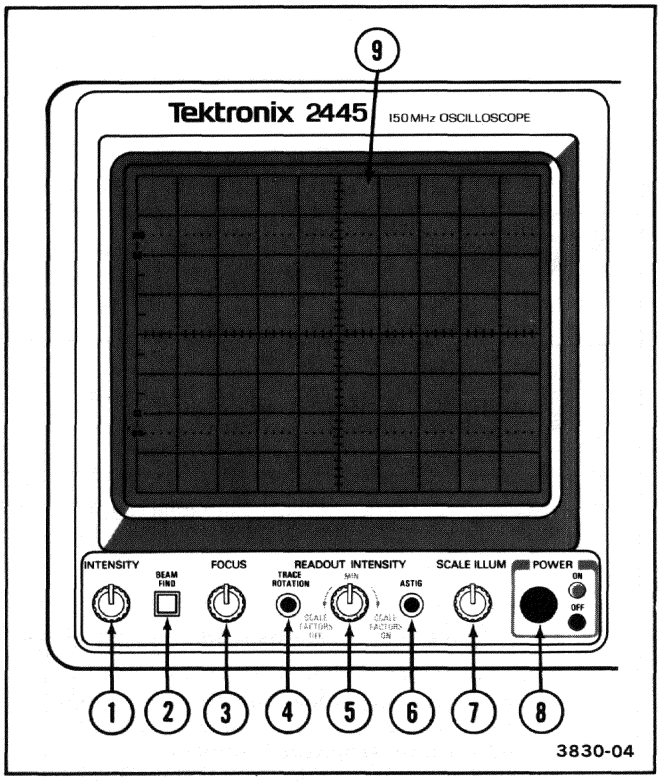


Figure 2-2. Power and display controls.

VERTICAL

Refer to Figure 2-3 for location of items 10 through 17.

(10) **CH 1 OR X and CH 2 Input Connectors**—Provide for application of external signals to the inputs of Channel 1 and Channel 2 vertical attenuators. A signal applied to the CH 1 OR X connector provides the horizontal deflection for an X-Y display. Any one or all of the channels (including Channel 1) may supply the signal for the X-Y display vertical deflection. These connectors each include a coding-ring contact that activates the scale-factor-switching circuitry whenever a scale-factor-switching probe is connected. The internal circuitry recognizes Tektronix attenuation-coded probes.

(11) **Input Coupling Switches and Indicators**—Select the method of coupling input signals to the Channel 1 and Channel 2 vertical attenuators and indicate the selection made. If the Channel 1 and Channel 2 input signals are both AC coupled and if both input coupling switches are pushed up together, the instrument automatically performs a dc balance of Channel 1 and Channel 2 vertical circuitry.

1 MΩ AC—Input signal is capacitively coupled to the vertical attenuator. The dc component of the input signal is blocked. The low-frequency limit (−3 dB point) is 10 Hz or less when using either a 1X probe or a coaxial cable and is 1 Hz or less when using a properly compensated 10X probe.

1 MΩ GND—The input of the vertical amplifier is grounded to provide a zero (ground) reference-voltage display. Input resistance is 1 MΩ to ground. This position of the switch allows precharging of the input-coupling capacitor to prevent a sudden shift of the trace if AC input coupling is selected later.

1 MΩ DC—All frequency components of the input signal are coupled to the vertical attenuator. Input resistance is 1 MΩ to ground.

1 MΩ GND—In this position, the switch operates exactly the same as previously described.

50 Ω DC—All frequency components of the input signal are coupled to the vertical attenuator, with the input terminated by 50 Ω to ground. If excessive signal is applied to either the CH 1 or the CH 2 input connector while 50 Ω DC input coupling is selected, input coupling will revert to 1 MΩ GND and a crt readout will indicate the overloaded condition. Moving the input coupling switch of the affected channel removes the overload message. While power is off, coupling is at 1 MΩ GND.

(12) **Channel 1 and Channel 2 VOLTS/DIV Switches**—Select vertical deflection factor settings in a 1-2-5 sequence with 11 positions. The VAR control must be in the detent (fully clockwise) position to obtain a calibrated deflection factor. Basic deflection factors are from 2 mV per division to 5 V per division. Deflection factors shown in the crt readout reflect actual deflection factors in use when Tektronix attenuation-coded probes are connected to the inputs.

(13) **VAR Controls**—Provide continuously variable, uncalibrated deflection factors between the calibrated settings of the VOLTS/DIV switches. These controls vary the deflection factors from calibrated (fully clockwise detent position) to at least 2.5 times the calibrated deflection factor (fully counterclockwise position). When out of the calibrated detent, a greater than (>) sign appears in front of the associated VOLTS/DIV readout display.

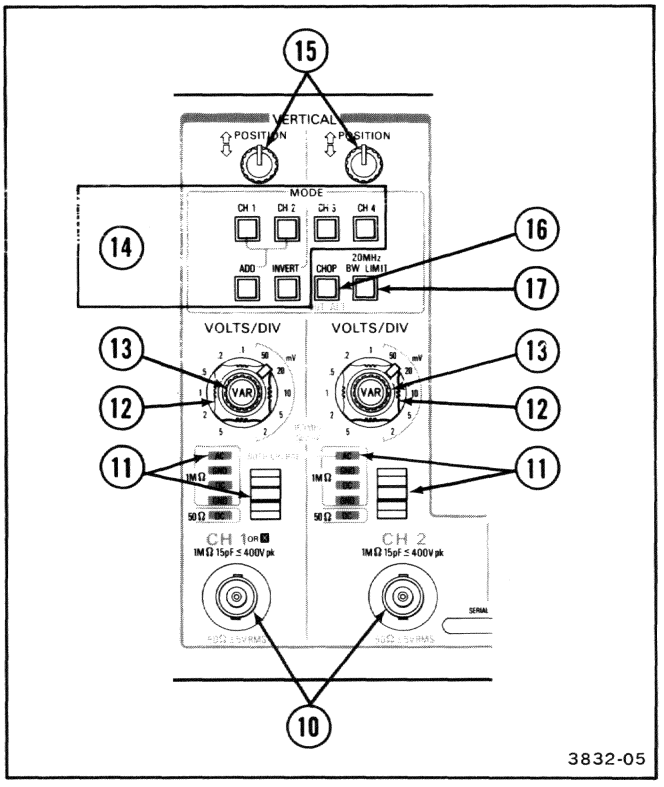


Figure 2-3. Vertical controls and CH 1 OR X and CH 2 connectors.

(14) **MODE Switches**—Select the indicated channel(s) for display when latched in. Any combination of the five possible signal selections can be displayed by pressing in the appropriate push buttons. The Channel 1 signal will be displayed if none of the MODE switches are latched in.

The algebraic sum of Channel 1 and Channel 2 is displayed when the ADD push button is latched in. When both ADD and INVERT buttons are latched in, the waveform displayed is the difference between the Channel 1 and Channel 2 signals. The INVERT button also inverts the polarity of the signal output at the CH 2 SIG OUT connector on the rear panel. At the same time, the Channel 2 trigger-signal polarity is inverted so that if CH 2 is selected as the TRIGGER SOURCE, the displayed slope will agree with the TRIGGER SLOPE switch setting.

When multiple channels are selected, they are displayed sequentially in order of priority. The established priority order is: CH 1, CH 2, ADD, CH 3, then CH 4.

(15) **POSITION Controls**—Set vertical position of the Channel 1 and Channel 2 signal displays. Clockwise rotation of a control moves the associated trace upward. When the X-Y display feature is in use, Channel 1 POSITION control moves the display horizontally; clockwise moves it to the right. The Channel 2, Channel 3, and Channel 4 vertical POSITION controls move the associated X-Y display vertically.

(16) **CHOP-OUT: ALT Switch**—Selects the vertical display mode for multiple-channel displays.

CHOP (latched in)—When more than one channel is selected, the vertical display switches sequentially through the selected channels at the chop-switching rate.

The chop frequency changes between 1 MHz and 2.5 MHz, depending on the SEC/DIV switch setting. At all sweep speeds, the chop-switching rate is desynchronized with the sweep frequency to minimize waveform breaks when viewing repetitive signals.

OUT: ALT (released out)—When more than one channel is selected, the vertical display switches sequentially through the selected channels. Alternate switching occurs during sweep-retrace times. If both A and B Sweeps are displayed, alternate switching occurs at the completion of the B Sweep.

The position of this switch has no effect on the switching rate of multiple X-Y displays. When more than one X-Y display is selected, switching occurs at 2.5 MHz.

(17) **20 MHz BW LIMIT Switch**—Reduces upper 3 dB bandpass of the vertical deflection system to a limit of 13 to 24 MHz when latched in. Full instrument bandwidth is available when push button is out.

Refer to Figure 2-4 for location of items 18 through 22.

(18) **CH 3 and CH 4 Input Connectors**—Provide for application of external signals to Channel 3 and Channel 4. Input coupling from these connectors is DC only. Coding-ring contacts, identical in operation to the CH 1 OR X and CH 2 input connectors, are also provided. Channel 3 and Channel 4 are most useful as digital signal and trigger signal input channels, given their limited choice of deflection factors.

(19) **POSITION Controls**—Set vertical position of the Channel 3 and Channel 4 signal displays. The controls operate identically to the Channel 2 POSITION control, but with less range on their associated traces.

(20) **Channel 3 and Channel 4 VOLTS/DIV Switches**—Select either of two basic deflection factors for Channel 3 and Channel 4. With the push button OUT, the basic deflection factor (using a 1X probe or a coaxial cable input connection) is 0.1 V per division; when it is latched IN, deflection factor is 0.5 V per division.

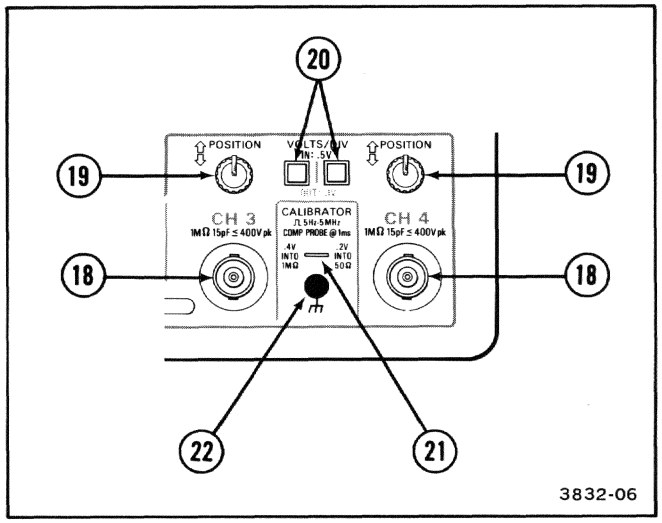


Figure 2-4. Channel 3 and Channel 4 controls and connectors and CALIBRATOR output.

(21) **CALIBRATOR Connector**—Provides a 0.4-V p-p square-wave signal into a 1-MΩ load, a 0.2-V p-p square-wave signal into a 50-Ω dc-coupled load, or an 8-mA p-p square-wave current signal into a short circuit at a sweep speed of 1 ms per division. The CALIBRATOR output signal is useful for checking the sweep, the delays, and the vertical deflection accuracies, as well as compensating voltage probes and checking the accuracy of current probes. The repetition rate of the square wave changes with the setting of the A SEC/DIV switch. For all sweep-speed settings from 100 ms per division to 100 ns per division, the A Sweep display, as seen on the instrument supplying the CALIBRATOR signal, will be five cycles per 10 divisions. At 100 ms per division and slower, the CALIBRATOR frequency will be 5 Hz; at 100 ns per division and faster, the frequency will be 5 MHz. The signal amplitude at 5 MHz will be at least 50% of the signal amplitude obtained when the sweep speed is set to 1 ms per division.

NOTE

Due to internal circuitry constraints, the calibrator signal is not synchronized during trace holdoff. This does not affect the accuracy of the calibrator signal that is present during a trace display. However, if the 2445 CALIBRATOR signal is used to calibrate other instruments, the sweep of the 2445 must be shut off. If it is not, the signal will appear to jitter and will give false (low) frequency counts. The sweep of the 2445 is easily shut off by setting the TRIGGER MODE switch to SGL SEQ.

(22) **Auxiliary Ground Jack**—Provides an auxiliary signal ground when interconnecting equipment under test and the oscilloscope. Hookup is made via a banana-tip connector.

HORIZONTAL AND DELTA MEASUREMENT

Refer to Figure 2-5 for location of items 23 through 33.

(23) **A SEC/DIV Switch**—Selects 25 calibrated A Sweep speeds from 1 s per division to 10 ns per division, or delay ranges from 10 s to 200 ns, in a 1-2-5 sequence. Extreme counterclockwise switch rotation selects the X-Y display mode. In X-Y, the signal applied to the CH 1 OR X input connector drives the horizontal deflection system.

(24) **B SEC/DIV Switch**—Selects 21 calibrated B Sweep speeds from 50 ms per division to 10 ns per division in a 1-2-5 sequence. This switch also controls Horizontal Display Mode switching, as explained in the following descriptions.

Knobs Locked—When both the A SEC/DIV and B SEC/DIV switches are set to the same sweep speed and the B SEC/DIV knob is pushed in, the two knobs are locked together; in this position, only the A Sweep is displayed on the crt.

PULL-INTEN—Pulling the B SEC/DIV knob to the out position intensifies the A Sweep display for the duration of the B Sweep time. When both the A SEC/DIV and B SEC/DIV switches are set to the same sweep speed, the B Sweep is not displayed, but it runs at one of two speeds: either 100 times faster than the A Sweep speed or at 5 ns per division, whichever is slower. The A and B SEC/DIV knobs are interlocked to prevent the B SEC/DIV switch from ever being set to a slower sweep speed than the A SEC/DIV switch setting.

The position of the intensified zone on the A Sweep indicates the delay time between the start of the A Sweep and start of the B Sweep interval. Its position is controlled by the Δ REF OR DLY POS control.

For single-trace displays, when either the Delta Time (Δt) or the reciprocal Delta Time (1/Δt) function is activated, two intensified zones will

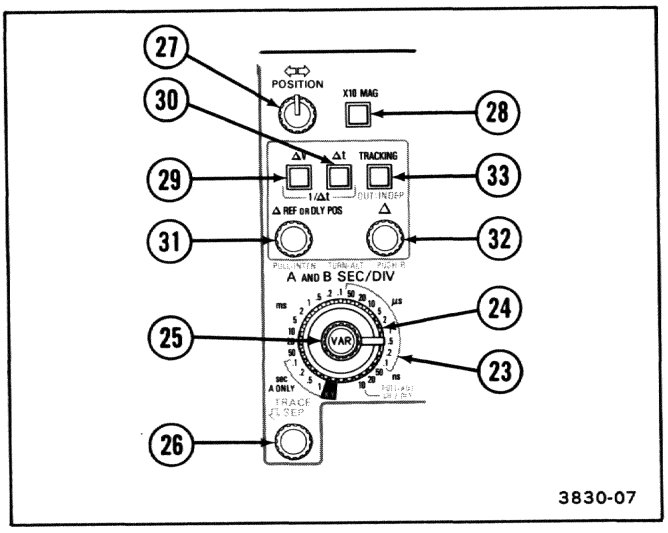


Figure 2-5. Horizontal and delta measurement controls.

appear on the A Sweep if the B TRIGGER MODE is set to RUN AFT DLY. When the B TRIGGER MODE is set to TRIG AFT DLY, intensified zones appear on the A Sweep only if proper B Sweep triggering occurs before the end of the A Sweep. When set to RUN AFT DLY, the position of the Reference zone is controlled by the Δ REF OR DLY POS control as before, and the position of the Delta zone is controlled by the Δ control. In TRIG AFT DLY mode, if the B Sweep is triggered, the positions of both intensified zones are determined by the first triggering events that occur after delay times set by the Δ REF OR DLY POS and the Δ controls have elapsed.

When more than one trace is displayed using ALT VERT MODE, and if the A Sweep is being triggered from a single source, with the Δt or 1/Δt function selected, the Reference zone will appear on the first selected trace from the following sequence: CH 1, CH 2, ADD, CH 3, then CH 4. The Delta zone appears on the second selected trace, and both zones appear on any additional traces. With CHOP VERT MODE or multiple-channel triggering, both zones appear on all traces.

Pulling the B SEC/DIV knob to the out position will cancel the Delta Volts (ΔV) function, if it is activated. Pushing in the B SEC/DIV knob to the locked position will cancel the **NO ΔV WITH DELAY** message on the crt readout, if it is being displayed.

PULL-ADJ CH 2 DLY—When the A SEC/DIV switch is set to 10 ns per division, pulling the B SEC/DIV knob to the out position activates the Channel 2 delay-offset (CH 2 DLY) adjustment feature. See "Matching Channel 2 Delay" in Section 5, "Operator's Checks and Adjustments," to use this feature.

TURN-ALT—Pulling the B SEC/DIV knob to the out position, then turning it to a faster sweep-speed setting than the A SEC/DIV sweep-speed setting, produces the Alternate (ALT) Horizontal Display Mode. The A Sweep with an intensified zone will be alternately displayed with the B Sweep, provided the B TRIGGER MODE is set either to RUN AFT DLY or to TRIG AFT DLY with a proper B triggering signal occurring before the end of the A Sweep. The position of the intensified zone on the A Sweep indicates the approximate delay of the B Sweep, and the length of the intensified zone indicates the approximate B Sweep duration set by the B SEC/DIV switch.

If either Δt or 1/Δt is also activated, intensified zones and associated B Sweeps will be established in the same manner as described in "PULL-INTEN."

PUSH-B—Pushing in the B SEC/DIV knob when the B SEC/DIV switch is set to a faster sweep speed than the A SEC/DIV switch presents only the B Sweep trace(s) on the crt display.

(25) **SEC/DIV VAR Control**—Continuously varies the sweep speed between settings of either the A or the B SEC/DIV switch. This control affects the A Sweep speed when the A and B SEC/DIV switches are locked together. When any of the delayed-sweep horizontal modes are displayed, the control affects only the B Sweep speed.

Fully counterclockwise rotation extends the sweep speed of the slowest A SEC/DIV switch setting (1 s per division) to 1.5 s per division. Fully clockwise rotation (detent position) produces the sweep speed indicated by the position of the SEC/DIV switches. The crt readout displays the actual time-per-division scale factor for all settings of the VAR control.

This control produces fine resolution over a portion of its range, after which it changes to coarse resolution. It reenters the fine-resolution range upon reversing the direction of rotation.

(26) **TRACE SEP Control**—Provides for vertical positioning of the B trace downward from the A trace when TURN-ALT Horizontal Display Mode is selected. Counterclockwise rotation moves the B trace downward. At the fully clockwise stop position of the control, there is no separation between the A and B traces. When the PUSH-B Horizontal Display Mode is selected and when either Δt or 1/Δt measurement mode is active, the TRACE SEP control provides for vertical positioning of the trace or traces associated with the Δ control.

(27) **Horizontal POSITION Control**—Sets the horizontal position of the sweep displays on the crt. Clockwise rotation of the control positions the display to the right. This control produces fine resolution over a portion of its range, after which it changes to coarse resolution. It reenters the fine-resolution range upon reversing the direction of rotation. The Horizontal POSITION control does not affect the X-Y display position on the crt.

(28) **X10 MAG Switch**—Horizontally magnifies the portion of the sweep display positioned at the center vertical graticule line by a factor of 10 when pressed in. When the A trace and the B trace are displayed alternately (TURN-ALT Horizontal Display Mode selected), only the B trace is magnified. Using X10 magnification extends the fastest sweep speed to 1 ns per division. The push button must be pressed in a second time to release it and regain the X1 sweep-speed magnification.

(29) **ΔV Switch**—Activates the Delta Volts (ΔV) measurement function, when momentarily pressed in alone, and cancels any other Delta measurement function in effect. In the A Sweep mode (A and B SEC/DIV switches locked together), two horizontal cursors are superimposed on the crt display. The crt readout displays the equivalent voltage represented by the separation between the two cursors. The position of one cursor on the display is set by the Δ REF OR DLY POS control and the position of the other is set by the Δ control. With multiple-channel displays, the deflection factor of the first channel selected in the display sequence determines the scale factor of the Delta Volts readout on the crt. The Delta Volts readout is displayed as a percentage ratio if either one of the following conditions exists: (1) the channel determining the scale factor is uncalibrated (VAR control out of detent), or (2) ADD is displayed alone when the Channel 1 and Channel 2 deflection factors are not the same (VOLTS/DIV switches are at different settings or are uncalibrated). Either pressing in the ΔV switch or pulling the B SEC/DIV knob to the out position when the Delta Volts function is active, cancels it. Attempting to activate the Delta Volts function while the A and B SEC/DIV knobs are unlocked causes the message **NO ΔV WITH DELAY** to appear in the top row of the crt readout. If displayed, the error message will be canceled (removed from the display) by any of the following actions: pressing either the ΔV or Δt switch; pushing in the B SEC/DIV if it is out or pulling it out if it is in; or locking the A and B SEC/DIV knobs together (set to the same sweep speed with the B SEC/DIV knob in).

(30) **Δt Switch**—Activates the Delta Time measurement function and cancels any other Delta measurements in effect, when momentarily pressed in alone. When the Delta Time function is active, momentarily pressing in the Δt push button cancels the function.

When the A and B SEC/DIV knobs are locked together (A trace only), two vertical cursors are superimposed on the crt display while the Delta Time function is active. In any of the delay-time Horizontal Display modes (PULL-INTEN, TURN-ALT, or PUSH-B), two separate delay times are established by the Delta Time function. One cursor position (or delay time) is set by the Δ REF OR DLY POS control, and the other is set by the Δ control. The crt readout displays either the time difference between the two delays or the equivalent time difference between the two vertical cursors.

If the SEC/DIV VAR control is not in the detent position, Δt cursor difference on the A trace only displays is expressed as a ratio, with five divisions corresponding to a 100% ratio. For the delay-time Horizontal Display modes, the SEC/DIV VAR control varies the B-sweep scale factor as it is rotated, but it has no effect on the delay time.

Pressing in the ΔV and Δt push buttons together activates the 1/Δt measurement function and cancels any other Delta measurement functions in effect. The crt waveform display and operation of both the Δ REF OR DLY POS and Δ controls remain the same as explained for Δt operation. However, with 1/Δt selected, the crt readout shows the reciprocal of the time-difference measurement, with units being frequency (Hz, kHz, MHz, or GHz).

For A trace only displays, with the SEC/DIV VAR control out of the detent (fully clockwise) position, the time difference between 1/Δt cursors is displayed in degrees of phase, with five divisions equal to 360 degrees. As with Δt measurements, the position of the SEC/DIV VAR control has no effect on delay-time displays except to change the B Sweep scale factor, and the readout remains in units of frequency.

When the 1/Δt function is active, pressing both the ΔV and the Δt push buttons together cancels the function and exits the Delta measurement mode. Pressing either ΔV or Δt alone cancels the 1/Δt function and activates the function associated with the button pressed.

(31) **Δ REF OR DLY POS Control**—Sets the reference B Sweep delay time or positions the Reference cursor when ΔV, Δt, or 1/Δt Measurement Mode is active. When any delay-time Horizontal Display Mode (PULL-INTEN, TURN-ALT, or PUSH-B) is selected, the reference B Sweep delay time is determined by the rotation of the Δ REF OR DLY POS control in conjunction with the A SEC/DIV switch setting.

This control produces fine resolution over a portion of its range, after which it changes to coarse resolution. It reenters the fine-resolution range upon reversing the direction of rotation.

(32) **Δ Control**—Sets the alternate B Sweep delay time or positions the Delta-time cursor (vertical line) when either the Δt or 1/Δt Measurement Mode is active. When the ΔV Measurement Mode is active (A Sweep Horizontal Display Mode only), the control positions one of the two horizontal voltage cursors that appear on the crt display.

This control produces fine resolution over a portion of its range, after which it changes to coarse resolution. It reenters the fine-resolution range upon reversing the direction of rotation.

(33) **TRACKING-OUT:INDEP Switch**—Selects either the TRACKING or INDEP (independent) mode for the Δ REF OR DLY POS control. When in the TRACKING mode (push button latched in), the difference between alternate delay times or cursors (in either time or volts Measurement Mode) does not change with rotation of the Δ REF OR DLY POS control. When the Δ REF OR DLY POS control is rotated, the positions of both delays or of both cursors move equally until the limit of either is reached.

If OUT:INDEP is selected (push button released), the cursors (or delay positions) are independently movable using the Δ REF OR DLY POS and Δ controls. In either mode (TRACKING or INDEP) the Delta cursor remains independently movable using the Δ control.

TRIGGER

Refer to Figure 2-6 for location of items 34 through 42.

(34) **MODE Switch and Indicators**—Selects the trigger mode of either the A Sweep or the B Sweep. A single push of the switch steps the MODE selection once; holding the switch up or down causes the MODE selection to step repeatedly. Indicators show the selected trigger mode of either the A Sweep or the B Sweep according to the selected Horizontal Display Mode and as directed by the A/B TRIG switch.

A Trigger Modes:

AUTO LVL—Automatically establishes the trigger level on a triggering signal and free runs the sweep in the absence of a triggering signal. The LEVEL control covers a range between the positive and negative peaks of repetitive triggering signals. If the triggering signal amplitude changes, the trigger level does not change unless a trigger is no longer produced at the established level. The signal peak-reference levels and the trigger level are redefined whenever triggering ceases, whenever the LEVEL control is turned to either extreme, or when the MODE switch is pushed up. If the LEVEL control is set near either end position, the trigger level set by AUTO LVL will be near the corresponding signal peak. If the LEVEL control is set in the midrange between either end, the trigger level set by AUTO LVL will be near the midpoint of the trigger signal amplitude. The established trigger level remains in effect when switching to AUTO or NORM Trigger MODE unless the LEVEL control is moved.

If VERT TRIGGER SOURCE is selected, the lowest-numbered displayed channel (or the algebraic sum of Channel 1 and Channel 2 if ADD vertical display is selected) becomes the trigger-signal source. If Trigger MODE is changed from AUTO LVL to AUTO while more than one channel is displayed, the single-channel trigger source is retained, and the VERT SOURCE indicator is turned off. To regain the VERT TRIGGER SOURCE, press up momentarily on the SOURCE switch.

AUTO—Sweep free runs in the absence of a triggering signal. The triggering level changes only when the LEVEL control is adjusted to a new position.

NORM—Sweep is triggered and runs when a triggering signal compatible with the LEVEL setting is applied. Sweep free runs either when the input coupling of the selected trigger SOURCE is

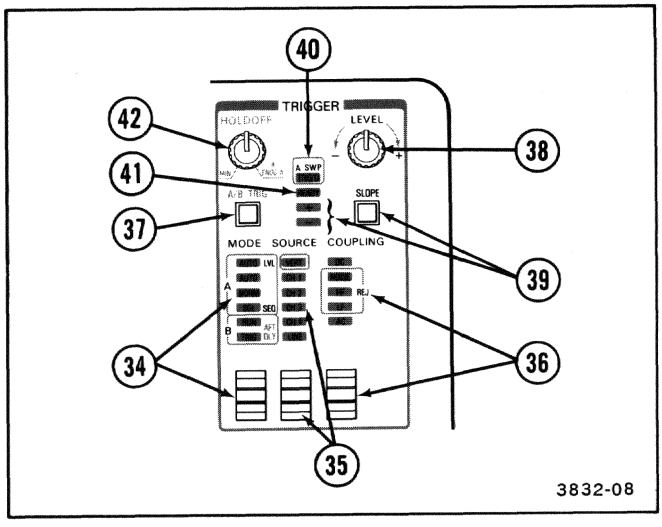


Figure 2-6. Trigger controls and indicators.

set to GND or when the input coupling of both Channel 1 and Channel 2 is set to GND, with ADD VERTICAL MODE and VERT TRIGGER SOURCE selected.

SGL SEQ—When armed by pushing the MODE switch down momentarily, the sweep runs one or more times to produce a single sweep of each of the traces defined by the following controls: VERTICAL MODE, A and B SEC/DIV, and Δt. Each sweep requires a distinct A Sweep triggering event. The READY indicator remains illuminated until the final trace in the sequence is completed. At the end of the sequence the crt readout is written once to present scale factors and other readout data, and scale illumination flashes on momentarily for oscilloscope photography purposes.

B Trigger Modes:

RUN AFT DLY—The B Sweep runs immediately after the established delay time has elapsed. Delay time is set by the A SEC/DIV switch and the Δ POS OR DLY REF control when no Delta Time measurements are selected (neither Δt nor 1/Δt).

When either Δt or 1/Δt measurements are made, two delay times are established: one by the Δ REF OR DLY POS control and the other by the Δ control.

TRIG AFT DLY—The B Sweep runs when triggered by a triggering signal after the established delay time has elapsed, provided the A Sweep has not terminated. Since the B Sweep runs at the time the triggering signal occurs, the display is stable, even with jittering signals; but the actual delay time is greater than the delay-time setting. Therefore, the crt readout shows a question mark in this mode.

(35) **SOURCE Switch and Indicators**—Selects the trigger signal source for either the A or the B Sweep. Indicators show the selection made. A single push of the switch steps the SOURCE selection once; holding the switch up or down causes the SOURCE selection to step repeatedly. Indicators do not illuminate for B triggering signals when RUN AFT DLY is selected.

VERT—The sweep triggers on the displayed channel when only one channel is selected. If multiple vertical displays are selected, both the Trigger MODE in use and position of the CHOP/ALT button affect the trigger-source selection. When ALT VERTICAL MODE is selected, each displayed channel in turn provides the triggering signal, and the respective LED indicator for each displayed channel is illuminated, except in the case of AUTO LVL MODE triggering. For AUTO LVL triggering or CHOP VERTICAL MODE, the lowest numbered channel, or ADD if it is displayed, is the triggering-signal source. The LED indicator for the lowest numbered channel displayed is illuminated, except if ADD is selected. Then, the CH 1, CH 2, and VERT indicators are illuminated.

CH 1, CH 2, CH 3, or CH 4—A triggering signal is obtained from the corresponding vertical channel.

LINE (A Trigger Only)—A triggering signal is obtained from a sample of the ac power-source waveform. This trigger source is useful when vertical input signals are time related (multiple or submultiple) to the frequency of the ac power-source voltage.

(36) **COUPLING Switch and Indicators**—Selects the method of coupling the triggering signal to the A and the B trigger generator circuitry. A single push of the switch steps the COUPLING selection once; holding the switch up or down causes the COUPLING selection to step repeatedly. Indicators show the coupling method selected for either the A triggering signals (when an A TRIGGER MODE is in effect) or the B triggering signals when TRIG AFT DLY is selected for the B TRIGGER MODE. Indicators do not illuminate for B triggering signals when RUN AFT DLY is selected.

DC—All frequency components of the signal are coupled to the trigger-generator circuitry. This coupling method is useful for triggering on most signals.

NOISE REJ—All frequency components of the input signal are coupled to the trigger-generator circuitry, but the peak-to-peak signal amplitude required to produce a trigger event is increased. This coupling method is useful for improving trigger stability on signals accompanied by low-level noise.

HF REJ—Attenuates high-frequency triggering-signal components above 50 kHz. This coupling method is useful for eliminating radio-frequency interference and high-frequency noise components from the signal applied to the trigger-generator

circuitry; it allows stable triggering on the low-frequency components of a complex waveform.

LF REJ—Signals are capacitively coupled, and the dc component of the triggering signal is blocked. Attenuates the low-frequency signal components below 50 kHz. This coupling method is useful for producing stable triggering on the high-frequency components of a complex waveform. Low-frequency components such as power-supply hum are removed from the signal applied to the trigger-generator circuitry.

AC—Signals are capacitively coupled. Frequency components below 60 Hz are attenuated, and the dc component of the input signal is blocked. This coupling method is useful for signals that are superimposed on slowly changing dc voltages. This method will work for most signals when trigger-level readout is not desired.

(37) **A/B TRIG Switch**—Directs the MODE, SOURCE, COUPLING, SLOPE, and LEVEL controls to either the A Trigger or the B Trigger, under the allowed switching conditions. Controls are normally directed to the A Trigger when the A and B SEC/DIV knobs are locked together (A Sweep display only). Controls are normally directed to the B Trigger when the B TRIGGER MODE is set to TRIG AFT DLY and the A and B SEC/DIV knobs are unlocked (PULL-INTEN, TURN-ALT, or PUSH-B Horizontal Display Mode). Pressing and holding in the A/B TRIG switch will direct the trigger controls away from their normal trigger direction, but releasing the A/B TRIG switch will redirect the trigger controls back to the original triggers.

If the A and B SEC/DIV knobs are unlocked and either the B TRIGGER MODE is set to RUN AFT DLY or the A TRIGGER MODE is set to SGL SEQ, the A/B TRIG switch will direct the trigger controls to the opposite trigger each time it is momentarily pressed and released.

Locking the A and B SEC/DIV knobs together will switch the trigger controls to the A Trigger if they are currently directed to the B Trigger. Pulling the B SEC/DIV knob to the out position will cause the trigger controls to revert to the B Trigger if the B TRIGGER MODE is set to TRIG AFT DLY. However, if the B TRIGGER MODE is set to RUN AFT DLY when the B SEC/DIV knob is unlocked from the A SEC/DIV knob, the trigger controls remain directed to the A Trigger until the B Trigger is reselected by the A/B TRIG switch.

(38) **LEVEL Control**—Sets the amplitude point on the triggering signal at which either A or B Sweep triggering occurs. This control produces fine resolution for a portion of its range, after which it changes to coarse resolution. It reenters the fine-resolution range upon reversing the direction of rotation.

When the A TRIGGER MODE is set to AUTO LVL, the effect of the LEVEL control is spread over the A Sweep triggering-signal amplitude from peak to peak. In this case, rotating the control to either extreme causes the triggering level to be redefined by the AUTO LVL circuitry.

(39) **SLOPE Switch and Indicators**—Selects the slope of the signal that triggers either the A Sweep or the B Sweep. Indicators illuminate to show slope selection made for the A Sweep and for TRIG AFT DLY B Sweeps. The + and — indicators do not illuminate for B triggering when RUN AFT DLY is selected.

(40) **A SWP TRIG'D Indicator**—Illuminates to indicate that the A Sweep is triggered. It extinguishes after a nominal length of time when a triggering signal is not received following completion of the sweep.

(41) **READY Indicator**—Illuminates when SGL SEQ MODE is selected and the A Sweep is armed and waiting for a triggering event to occur. It extinguishes following the completion of all the traces selected for the SGL SEQ display.

(42) **HOLDOFF Control**—Varies the amount of holdoff time between the end of the sweep and the time a triggering signal can initiate the next sweep. The ability to obtain stable triggering on some aperiodic signals is improved using this control. In the B ENDS A position (fully clockwise) trigger holdoff time is reduced to minimum, and the A Sweep terminates immediately at the end of the B Sweep. This enables the fastest possible sweep-repetition rate at slow A Sweep speeds.

REAR PANEL

Refer to Figure 2-7 for location of items 43 through 49.

(43) **A GATE OUT and B GATE OUT Connectors**—Provide TTL-compatible, positive-going gate signals that are HI during their respective sweeps and LO while the sweep is not running.

(44) **CH 2 SIGNAL OUT Connector**—Provides an output signal that is a normalized representation of the Channel 2 input signal. The output amplitude into a 1-MΩ load is approximately 20 mV per division of input signal. Into a 50-Ω load, the output amplitude is approximately 10 mV per division of input signal.

(45) **EXT Z-AXIS IN Connector**—Provides an input connection point to apply external Z-axis modulation signals to the Z-Axis Amplifier. Either the sweep or the X-Y display may be intensity modulated. Positive-going signals decrease the intensity. From dc to 2 MHz, an input-signal amplitude of +2 V will blank a maximum-intensity trace; from 2 MHz to 20 MHz, an input-signal amplitude of +2 V will produce noticeable modulation on a normal-intensity trace.

Modulating signals with fast rise and fall times produce the most abrupt intensity changes. External Z-axis signals must be time related to the displayed signal frequency to obtain a stable intensity-modulation pattern on the crt.

(46) **Fuse Holder**—Contains the ac power-source fuse.

(47) **Detachable Power Cord Receptacle**—Provides the connection point for the ac power source to the instrument.

(48) **LINE VOLTAGE SELECTOR Switch**—Selects the nominal instrument operating voltage range. When set to 115V, the instrument operates from a power-source voltage having a range of 90 V to 132 V ac. Set to 230V, the instrument operates on an input-voltage range of 180 V to 250 V ac.

(49) **Mod Slots**—Contain the identification numbers of any installed instrument modifications.

READOUT DISPLAY

The Readout System provides an alphanumeric display of information on the crt along with the analog waveform display. The readout is displayed in two rows of 32 characters each. One row is within the top graticule division, and the other row is within the bottom graticule division.

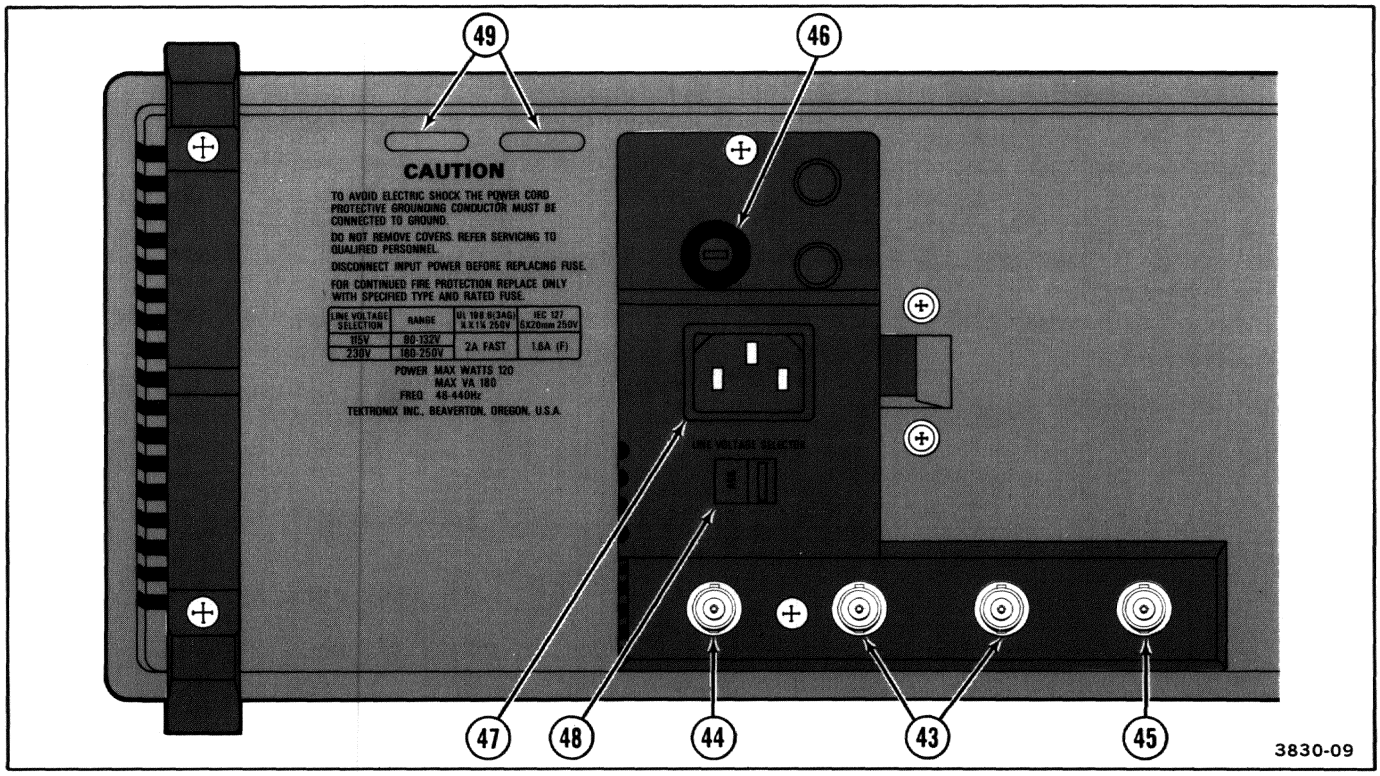


Figure 2-7. Rear-panel controls and connectors.

The locations and types of information displayed under normal operating modes are illustrated in Figure 2-8.

NOTE

Other information is displayed when the instrument is in a diagnostic mode or has experienced a fault. The diagnostic displays are explained in the "Maintenance" section of this manual.

If the bottom row of the readout contains dots in the normally blank spaces, a wrong calibration constant has been encountered. The instrument must be readjusted to remove the incorrect calibration constant from the EAROM.

Each of the scale-factor displays appears when the respective vertical channel or sweep is displayed. When X-Y mode is selected, the Channel 1 scale factor is displayed, and **CH 1 X** appears in place of the A Sweep scale factor.

Special characters or abbreviations are displayed to indicate GND or AC coupling of Channel 1 or Channel 2 signals, ADD, CH 2 INVERT, Vertical bandwidth limited, or HOLDOFF not set to minimum.

The Trigger-Level readout shows the signal voltage (at the probe tip of encoded probes) that will initiate the sweep. The readout appears only if the following conditions exist: a single vertical channel is selected as the trigger source, the vertical input coupling is not AC, the VOLTS/DIV VAR control of the source channel is in the calibrated detent, and trigger coupling is either DC or NOISE REJ.

A question mark may appear in a DLY (delay time), a Δt (delta time), or a $1/\Delta t$ readout when the SEC/DIV knobs are unlocked (not with cursors). This indicates that either the delay time (or one of the two delay times) is set at less than 0.5% of the maximum delay or the B TRIGGER MODE is set to TRIG AFT DLY. A question mark will also appear in a $1/\Delta t$ display readout when the difference between the two delays (or the distance between the two cursors displayed when the A and B SEC/DIV knobs are locked together) is less than 1% of full scale.

The **50 Ω OVERLOAD** display appears if excessive signal is applied to either the CH 1 or the CH 2 input connector while 50 Ω DC input coupling is selected. The readout will return to the normal display when the input coupling of the overloaded channel is switched.

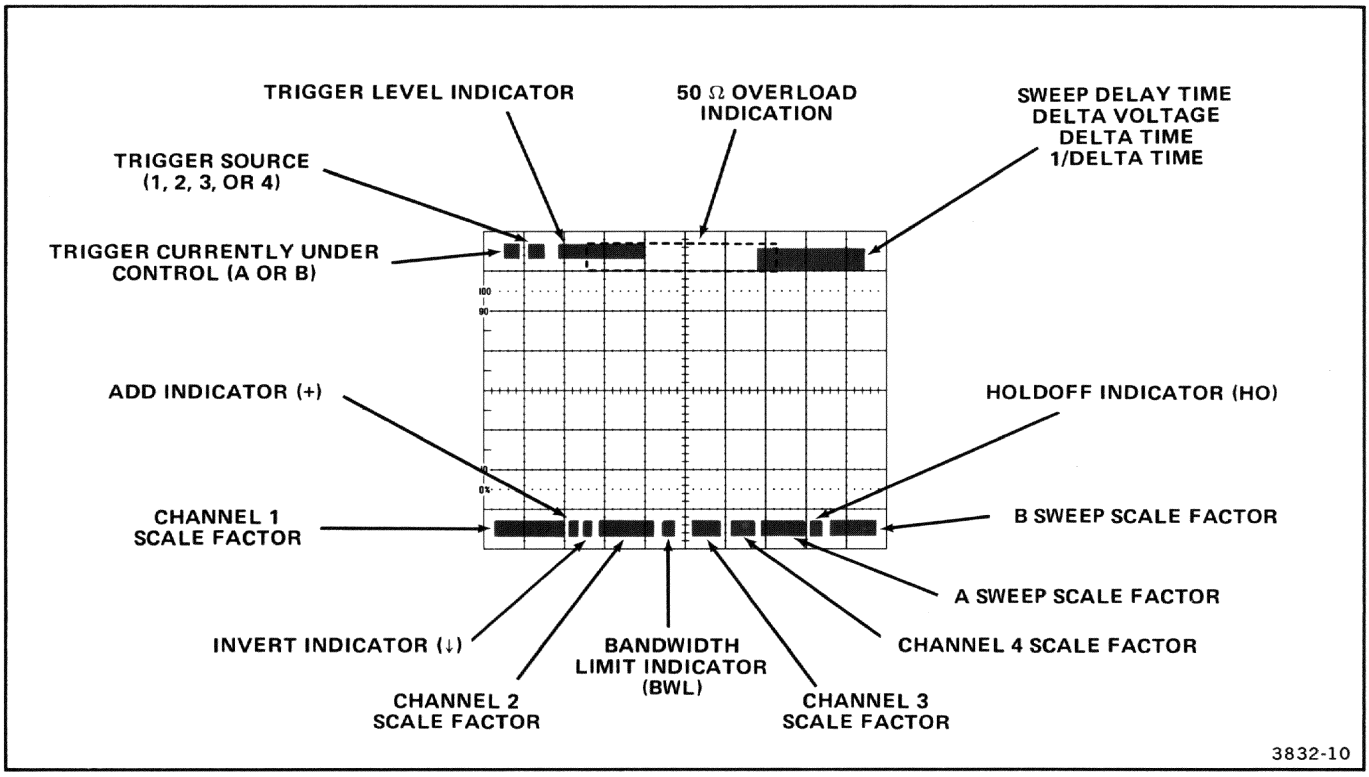


Figure 2-8. Readout display locations

OPERATING CONSIDERATIONS

This part contains basic operating information and techniques that should be considered before attempting to make any measurements with your instrument.

GRATICULE

The graticule is internally marked on the faceplate of the crt to eliminate parallax-viewing error and to enable accurate measurements (see Figure 2-9). It is marked with eight vertical and ten horizontal major divisions. In addition, each major division is divided into five subdivisions. The vertical deflection factors and horizontal timing are calibrated to the graticule so that accurate measurements can be made directly from the crt. Also, percentage marks for the measurement of rise and fall times are located on the left side of the graticule.

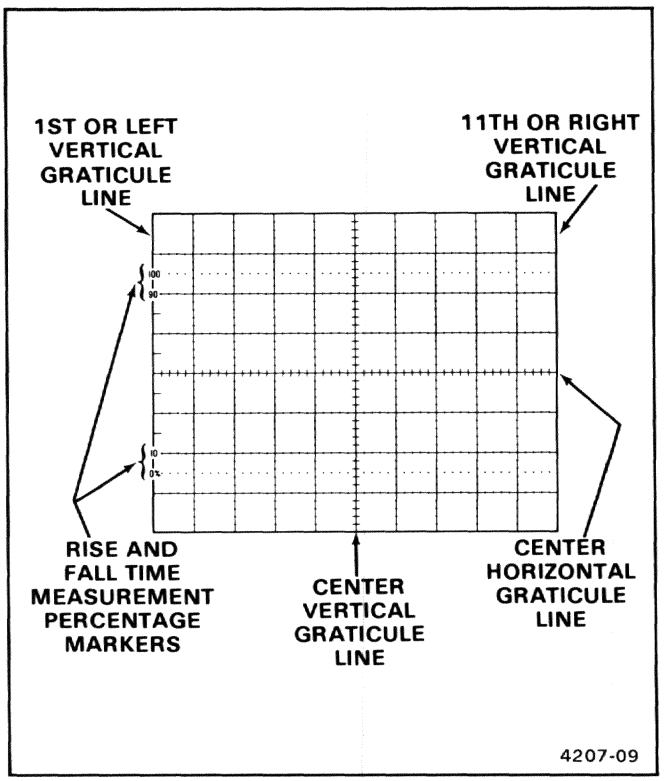


Figure 2-9. Graticule measurement markings.

TIME AND VOLTAGE MEASUREMENTS

The 2445 provides three basic ways to make time measurements and two basic ways to make voltage measurements. These methods require varying degrees of time and care and can result in varying degrees of accuracy.

Using graticule markings for determining voltage or time values produces the least accurate measurement values. This method should be used only for measuring very-low-repetition-rate signals or for single-shot measurements which require a photograph for viewing.

The Δt and ΔV cursors provide for better accuracy and easier operation than using the graticule, and they should be used in most measurement situations. Use of the cursors avoids vertical- and horizontal-gain errors and crt-linearity errors. Cursors also eliminate the inconvenience of counting and interpolating graticule markings.

The Delayed Sweep mode provides the highest accuracy for making time measurements. This method avoids errors introduced either by visual-resolution limits or by slight mismatches between the sweep and the cursors.

More details relating to various measurement techniques are contained in "Basic Applications," Section 6 of the Operators Manual.

GROUNDING

The most reliable signal measurements are made when the 2445 and the unit under test are connected by a common reference (ground lead) in addition to the signal lead or probe. The probe's ground lead provides the best grounding method for signal interconnection and ensures the maximum amount of signal-lead shielding in the probe cable. A separate ground lead can also be connected from the unit under test to the oscilloscope ground receptacle on the front panel.

SIGNAL CONNECTIONS

Probes

Generally, probes offer the most convenient means of connecting an input signal to the instrument. Shielded to prevent pickup of electromagnetic interference, the standard 10X probes supplied with this instrument offer a high input impedance that minimizes circuit loading. This allows the circuit under test to operate with a minimum of change from the normal, unloaded condition. Also, the subminiature body of these probes has been designed for ease of use either when probing circuitry containing close lead spacing or when probing in a confined space.

Both the probe itself and the probe accessories should be handled carefully at all times to prevent damage. Avoid dropping the probe body. Striking a hard surface can cause damage to both the probe body and the probe tip. Exercise care to prevent the cable from being crushed or kinked. Do not place excessive strain on the cable by pulling.

The standard-accessory probe is a compensated 10X voltage divider. It is a resistive voltage divider for low frequencies and a capacitive voltage divider for high-frequency signal components. Inductance introduced by either a long signal or ground lead forms a series-resonant circuit. This circuit will affect system bandwidth and will ring if driven by a signal containing significant frequency components at or near the circuit's resonant frequency. Oscillations (ringing) can then appear on the oscilloscope display and distort the true signal waveform. Always keep both the ground lead and the probe signal-input connections as short as possible to maintain the best waveform fidelity.

Misadjustment of probe compensation is a common source of measurement error. Due to variations in oscilloscope input characteristics, probe compensation should be checked and adjusted, if necessary, whenever the probe is moved from one oscilloscope to another or between channels of a multichannel oscilloscope. See the procedure in the "Operator's Checks and Adjustments" part of this section or consult the probe instruction manual.

Coaxial Cables

Cables may also be used to connect signals to the input connectors, but they may have considerable effect on the accuracy of a displayed waveform. To maintain the original frequency characteristics of an applied signal, only high-quality, low-loss coaxial cables should be used. Coaxial cables should be terminated at both ends in their characteristic impedance. If this is not possible, use suitable impedance-matching devices.

INPUT-COUPLING CAPACITOR PRECHARGING

When the input coupling switch is set to GND, the input signal is connected to ground through the input-coupling capacitor in series with a 1-MΩ resistor to form a precharging network. This network allows the input-coupling capacitor to charge to the average dc voltage level of the signal applied to the probe. Thus, any large voltage transients that may accidentally be generated will not be applied to the amplifier input when input coupling is switched from GND to AC. The precharging network also provides a measure of protection to the external circuitry by reducing the current levels that can be drawn from the external circuitry during capacitor charging.

EXTERNAL TRIGGERING

Both the A and the B trigger signals may be independently obtained from any of the four vertical input channels. When viewing signals that require a trigger source different from one of the displayed vertical signals (traditionally referred to as "external triggering"), any free vertical channel may be used to input a trigger signal. The signal can be viewed on the crt to aid in setting the trigger circuit controls by selecting that respective channel for the vertical display (replaces the usual "trigger view" feature). After establishing the correct triggering, the trigger signal display can then be removed from the vertical signal display or allowed to remain, at the operator's descretion.

Channel 1 and Channel 2 can condition a wide range of signals to produce triggers—over the full vertical deflection range of the channel from millivolts to hundreds of volts in amplitude. Channel 3 and Channel 4 inputs have a much more limited choice of vertical deflection ranges available (0.1 volt and 0.5 volt per division without external attenuation) and are more useful for digital signal amplitudes. However, signals much larger can be processed, provided they do not exceed the maximum-rated signal amplitude for the input.

OPERATOR'S CHECKS AND ADJUSTMENTS

INTRODUCTION

This part contains procedures that may be used to verify the operation and basic accuracy of your instrument before making measurements. Adjustment procedures provided enable the user to optimize the display for viewing as well as compensate several of the oscilloscope control functions for variations in ambient operating temperature. Adjustments beyond the scope of "Operator's Checks and Adjustments" are in the "Adjustment Procedures," Section 5 of this manual.

Before proceeding with these instructions, refer to "Preparation for Use" in this section for first-time start-up considerations.

Verify that the POWER switch is OFF (push button is out), then plug the power cord into the power outlet.

INITIAL SETUP

1. Press in the POWER switch button (ON) and allow the instrument to warm up (20 minutes is recommended for maximum accuracy).

2. Set instrument controls to obtain a baseline trace:

Display

READOUT INTENSITY	Midrange between MIN and fully clockwise
FOCUS	Midrange

Vertical

POSITION	Midrange
MODE	CH 1
BW LIMIT	Off (button out)
CH 1 VOLTS/DIV	10 mV
CH 1 Input Coupling	1 MΩ GND

Horizontal

A AND B SEC/DIV	Locked together at 1 ms
SEC/DIV VAR	Calibrated detent
POSITION	Midrange
10X MAG	Off (button out)

Trigger

HOLDOFF	Fully counterclockwise
LEVEL	Midrange
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC
SLOPE	+

3. Adjust the INTENSITY and READOUT INTENSITY controls for desired display and readout brightness and best trace definition.

4. Adjust the Vertical and Horizontal POSITION controls to position the trace within the graticule area.

TRACE ROTATION ADJUSTMENT

1. Preset instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Use the Channel 1 POSITION control to move the baseline trace to the center horizontal graticule line.

NOTE

Normally, the resulting trace will be parallel to the center horizontal graticule line, and the Trace Rotation adjustment should not be required.

3. If the trace is not parallel to the center horizontal graticule line, use a small-bladed screwdriver to adjust the TRACE ROTATION control (see Figure 2-2) and align the trace with the center horizontal graticule line.

ASTIGMATISM ADJUSTMENT

1. Preset instrument controls and obtain a baseline trace as described in "Initial Setup." Set 20 MHz BW LIMIT On (in)

2. Connect a 10X probe to the CH 1 OR X input connector and connect the probe tip to the CALIBRATOR output.

3. Adjust the Channel 1 POSITION control to center the display on the screen.

4. Set A and B SEC/DIV controls at 1 μs.

5. Slowly adjust the FOCUS control to its optimum setting (best-defined display).

NOTE

If the ASTIG adjustment is correctly set already, all portions of the trace will come into sharpest focus at the same position of the FOCUS control.

6. If focusing is not uniform over the entire graticule area, use a small-bladed screwdriver to adjust the ASTIG control (see Figure 2-2).

7. Since the ASTIG and FOCUS adjustments interact, repeat steps 5 and 6 until the best-defined display over the entire graticule area is obtained.

NOTE

Once it is set, the ASTIG adjustment should be correct for any display. However, it may be necessary to reset the FOCUS control slightly when the INTENSITY control setting is changed.

AUTO DC BALANCE ADJUSTMENT

The 2445 can automatically perform a dc-balance adjustment of Channel 1 and Channel 2. This adjustment assures that the trace shifts associated with attenuator stepping, changing the variable volts per division setting, and switching Channel 2 between noninverted and inverted operation are within nominal limits. The dc balance attained by the Auto DC Balance adjustment remains valid as long as the instrument is operating within 5°C of the ambient temperature at which the adjustment was performed provided a 20-minute warm-up period is allowed before performing the adjustment. To initiate the adjustment, set both the Channel 1 and Channel 2 input coupling switches to AC. Then simultaneously push up on both switches. An alternate method of entering the auto-adjustment mode is possible with only one of the input coupling switches set to AC. Press up and hold the input coupling switch that is not set to AC, then press up the other input coupling switch. With either method, the instrument will enter an auto-adjustment mode for about ten seconds. When the Auto DC Balance adjustment cycle is complete, the instrument will return to the normal operating mode.

NOTE

If a circuit defect prevents accurate dc balance, the routine halts and **LIMIT** *is displayed. Push the Trigger COUPLING switch up to continue balancing the remainder of the circuitry.*

If power to the instrument is interrupted before the balancing cycle is completed, an error will be detected by the next power-on self test. Press A/B TRIG to exit the diagnostic monitor and restart the Auto DC Balance adjustment to allow the cycle to be completed.

PROBE LOW-FREQUENCY COMPENSATION

Misadjustment of probe compensation is one of the sources of measurement error. The attenuator probes are equipped with compensation adjustments. To ensure optimum measurement accuracy, always check probe compensation before making measurements. Probe low-frequency compensation is accomplished as follows:

1. Preset instrument controls and obtain a baseline trace as described in "Initial Setup." Set 20 MHz BW LIMIT On (in).

2. Connect the two 10X probes (supplied with the instrument) to the CH 1 OR X and the CH 2 input connectors. Observe that the CHANNEL 1 SCALE FACTOR on the readout display changes from **10 mV** to **100 mV** when the 10X probe is attached.

3. Connect the Channel 1 probe (using the probe hook tip) to the oscilloscope CALIBRATOR output.

4. Set triggering controls for a stable display. The display should be five cycles of the CALIBRATOR square-wave signal, with an amplitude of four divisions. Center the display on the screen.

5. Check the waveform for overshoot and rolloff (see Figure 2-10). If necessary, use a small-bladed screwdriver to adjust the probe low-frequency compensation for a square front corner on the waveform.

6. Release the CH 1 VERTICAL MODE switch, select CH 2 VERTICAL MODE, and connect the Channel 2 probe input to the CALIBRATOR output. Observe that the CH 2 SCALE FACTOR on the readout display indicates **100 mV** with the 10X probe attached.

7. Use the Channel 2 POSITION control to vertically center the display and repeat step 5 for the Channel 2 probe.

NOTE

Refer to the instruction manual supplied with the probe for more complete information about low-frequency and high-frequency compensation of the probes.

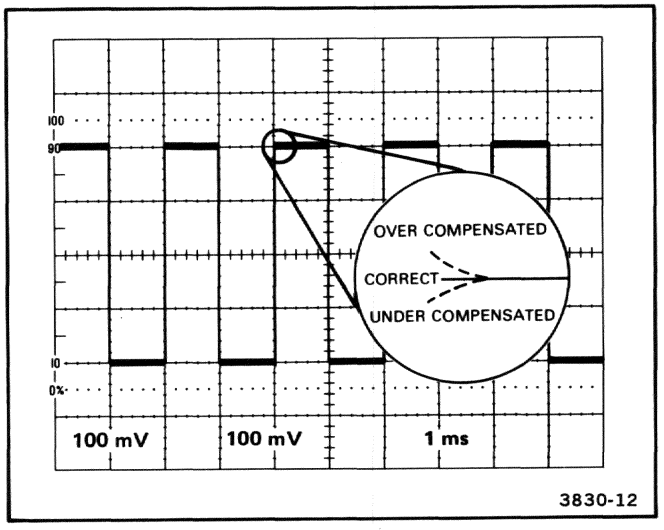


Figure 2-10. Probe low-frequency compensation.

MATCHING CHANNEL 2 DELAY

The apparent signal delay in Channel 2 may be adjusted up to ±500 ps to match the apparent delay present in any of the other three channels. This adjustment is most commonly used to eliminate delay differences between Channel 1 and Channel 2 that may be introduced by the probes and has no effect on common-mode rejection when ADD VERTICAL MODE is selected. Matching Channel 1 and Channel 2 delay is accomplished as follows:

1. Preset the instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Connect the two 10X probes (supplied with the instrument) to the CH 1 OR X and CH 2 input connectors.

3. Check and adjust, if necessary, the probes' low-frequency compensation. Refer to "Probe Low-Frequency Compensation" in this section.

4. Connect both probes via hook tips to a pulse generator fast-rise output.

5. Press in both the CH 1 and CH 2 VERTICAL MODE switches.

6. Set oscilloscope triggering controls for a stable display.

7. Set the A AND B SEC/DIV switches to 10 ns.

8. Adjust the Channel 1 and Channel 2 POSITION controls to vertically overlay the two displayed signals.

9. Pull out the B SEC/DIV switch and observe the message **CH 2 DELAY – TURN Δ** in the upper right-hand corner of the screen.

NOTE

The 2445 can be set to preclude operator adjustment of Channel 2 delay. If the delay-offset feature is disabled, the message **CH 2 DLY DISABLED** *appears in the top row of the readout when attempting to activate the feature. Refer the instrument to a qualified service technician if adjustment of the delay matching is required.*

10. Set X10 MAG ON (button in) and adjust the Δ control until the two signals are overlaid horizontally.

NOTE

The Δ REF OR DLY POS control may also be used to make the Channel 2 delay-offset adjustment when the feature is enabled.

11. Push in the B SEC/DIV switch.

AMPLITUDE CHECK

1. Preset instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Connect a 10X probe to the CH 1 OR X input connector and connect the probe tip to the CALIBRATOR output.

3. Adjust the Channel 1 POSITION control to center the display on the screen.

4. Adjust triggering controls to obtain a stable display.

5. CHECK—Amplitude of the CALIBRATOR signal is between 3.88 and 4.12 divisions as measured on the center vertical graticule line.

6. Repeat this procedure using the Channel 2 connector and controls.

TIMING CHECK

The CALIBRATOR signal on the 2445 automatically changes repetition rate with the setting of the A SEC/DIV switch within the range of 100 ms to 100 ns. This feature allows the operator to make a quick and easy check of the basic operation and adjustment of the oscilloscope timing. Use the following procedure:

1. Preset instrument controls and obtain a baseline trace as described in "Initial Setup."

2. Connect a 10X probe to the CH 1 OR X input connector and connect the probe tip to the CALIBRATOR output.

3. Adjust the Channel 1 POSITION control to center the display on the screen.

4. Adjust triggering controls to obtain a stable display.

5. CHECK—Timing accuracy by confirming that five complete cycles of the square-wave signal are displayed over 10 major divisions (±0.1 division) along the center horizontal graticule line for all A SEC/DIV settings from 100 ms to 100 ns. Confirm that the number of cycles displayed in 10 divisions goes to 2 1/2 and 1 for respective A SEC/DIV settings of 50 ns and 20 ns and that the displayed transition time of the signal remains approximately the same when the A SEC/DIV switch is changed to 10 ns. (The horizontal divisions in which the transition time of the signal at 10 ns per division is displayed should be two times the horizontal divisions occupied by the transition at 20 ns per division.) Return the A SEC/DIV switch to 1 ms and confirm that the display changes to 1/2 cycle over 10 divisions when the X10 MAG switch is pressed in.

THEORY OF OPERATION

INTRODUCTION

SECTION ORGANIZATION

This section contains a functional description of the 2445 Oscilloscope circuitry. The discussion begins with an overview of the instrument functions and continues with detailed explanations of each major circuit. Reference is made to supporting schematic and block diagrams which will facilitate understanding of the text. These diagrams show interconnections between parts of the circuitry, identify circuit components, list specific component values, and indicate interrelationships with front-panel controls.

The detailed block diagram and the schematic diagrams are located in the tabbed "Diagrams" section at the rear of this manual, while smaller functional diagrams are contained within this section near the associated text. The particular schematic diagram associated with each circuit description is identified in the text, and the diagram number is shown (enclosed within a diamond symbol) on the tab of the appropriate foldout page. For optimum understanding of the circuit being described, refer to both the applicable schematic diagram and the functional block diagram.

HYBRID AND INTEGRATED CIRCUIT DESCRIPTIONS

Digital Logic Conventions

Digital logic circuits perform many functions within this instrument. The operation of these circuits is represented by specific logic symbology and terminology. Most logic-function descriptions contained in this manual use the positive-logic convention. Positive logic is a system of notation whereby the more positive of two levels is the TRUE (or 1) state; the more negative level is the FALSE (or 0) state. In the logic descriptions, the TRUE state is referred to as HI, and the FALSE state is referred to as LO. The specific voltages which constitute a HI or a LO vary between individual devices. For specific device characteristics, refer to the manufacturer's data book.

Hybrids

Some of the circuits in this instrument are implemented in hybrid devices. The hybrids are specialized electronic devices combining thick-film and semiconductor technologies. Passive, thick-film components and active, semiconductor components are interconnected to form the circuit on a ceramic carrier. The end result is a relatively small "building block" with enhanced performance characteristics, all in one package. Hybrid circuits are shown on schematics simply as blocks with inputs and outputs identified. Information about hybrid functioning is contained in the related portion of the Detailed Circuit Description.

Linear Devices

The operation of individual linear integrated circuit devices is described in this section using waveforms or other graphic techniques to illustrate their operation.

BLOCK DIAGRAM

The following discussion is provided as an aid in understanding overall operation of the 2445 Oscilloscope circuitry before the individual circuits are discussed in detail. A simplified block diagram of the 2445 Oscilloscope, showing basic interconnections, is shown in Figure 3-1. The diamond-enclosed numbers in each block refer to the schematic diagram(s) at the rear of this manual in which the related circuitry is located.

BLOCK DESCRIPTION

The Low Voltage Power Supply is a high-efficiency, switching supply with active output regulation that transforms the ac source voltage to the various dc voltages required by the 2445. The High Voltage Power Supply circuit develops the high accelerating potentials required by the crt, using voltage multiplication techniques, and the DC Restorer provides interfacing for the low-potential intensity signals from the Z-Axis Amplifier to the crt control grid.

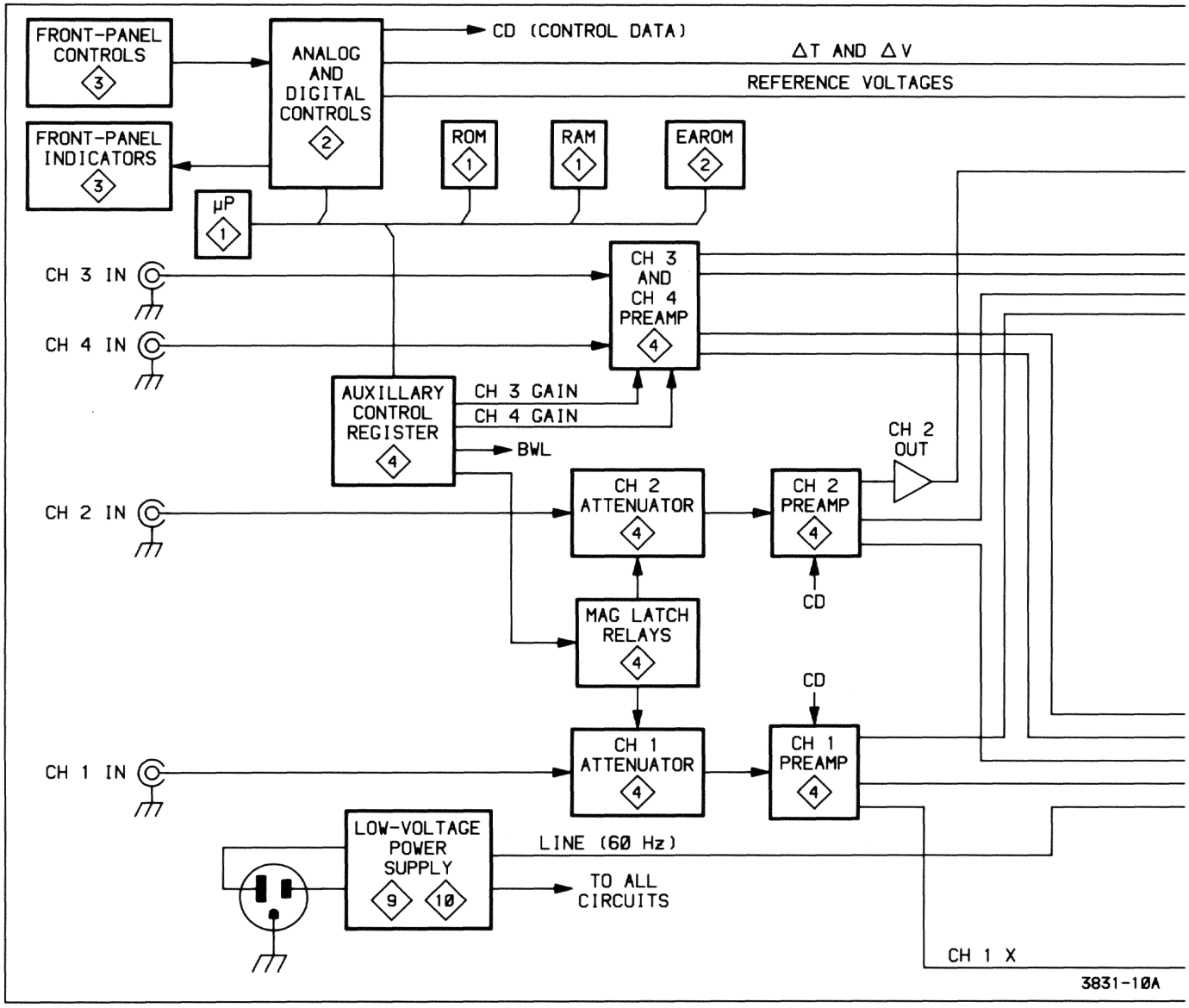


Figure 3-1. Block diagram.

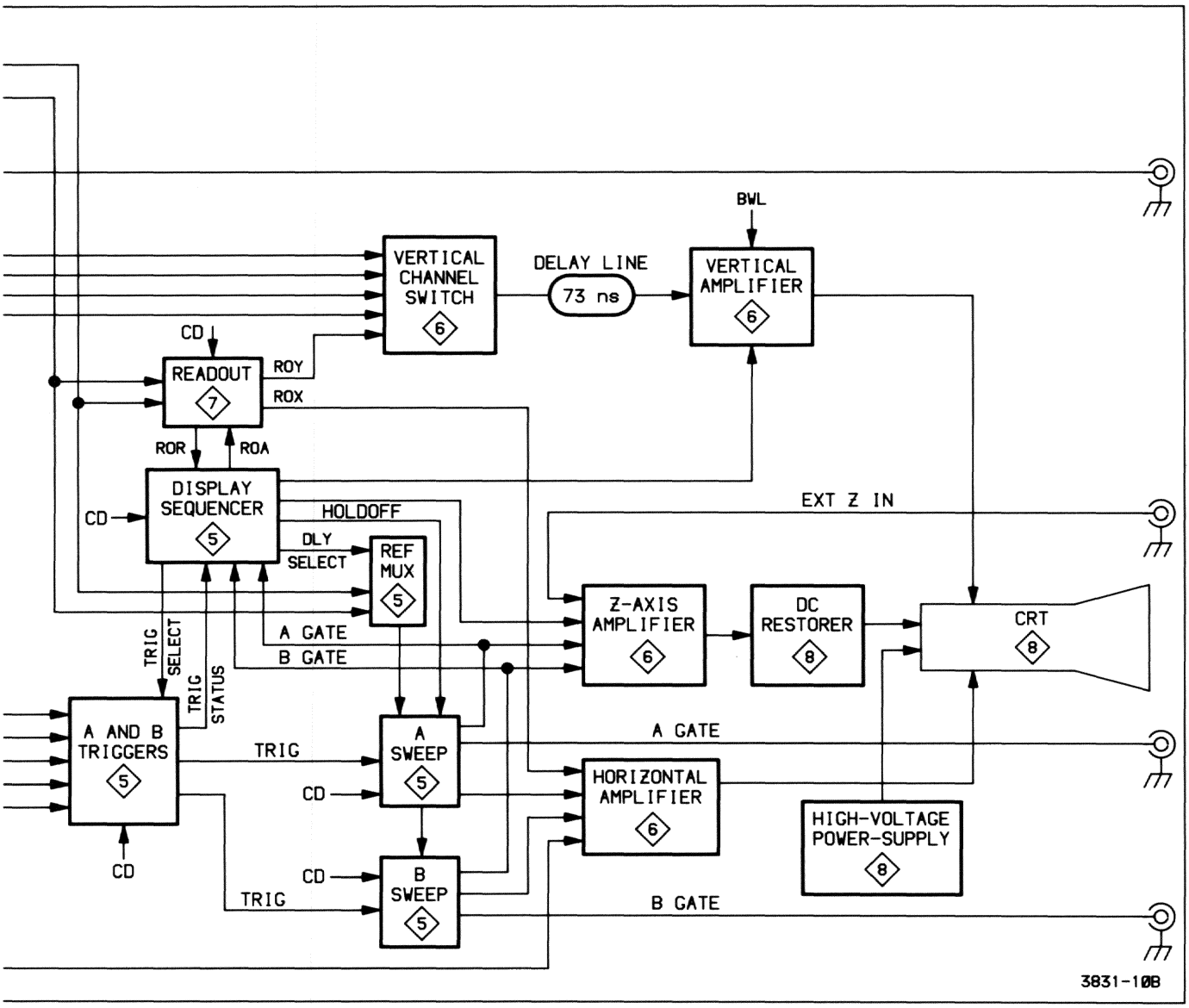


Figure 3-1. Block diagram (cont).

Most of the activities of the 2445 are directed by a Microprocessor. The Microprocessor, under firmware control (firmware is the programmed instructions contained in read-only memory that tells the processor how to operate), monitors instrument functions and sets up the operating modes according to the instructions received.

Various types of data to and from the Microprocessor (program instructions, constants, control data, etc.) are transferred over a group of eight bidirectional signal lines called the Data Bus. The Data Bus is dedicated solely to Microprocessor-related data transfer.

Another group of signal lines, called the Address Bus, are responsible for selecting or "addressing" the memory location or device that the Microprocessor wants to communicate with. Typically, depending on the instruction being executed, the processor places an address on the Address Bus to identify the location the Microprocessor must communicate with. This address, along with some enabling logic, opens up an appropriate data path via the Data Bus; and data is then either read from or written to that location by the processor.

While executing the control program, the Microprocessor retrieves previously stored calibration constants and front-panel settings and, as necessary, places program-generated data in temporary storage for later use. The EAROM (electrically-alterable read-only memory) and RAM (random-access memory) provide these storage functions respectively.

When power is applied to the 2445, a brief initialization sequence is performed, and then the processor begins scanning the front-panel controls. The switch settings detected and the retrieved front-panel data from the EAROM causes the processor to set various control registers and control voltages within the instrument that define the operating mode of the instrument. These register settings and voltage levels control the vertical channel selection and deflection factors, the sweep rate, the triggering parameters, the readout activity, and sequencing of the display. Loading the control data into the various registers throughout the instrument is done using a common serial data line (CD). Individual control clock signals (CC) determine which register is loaded from the common data line.

Coordination of the vertical, horizontal, and Z-Axis (intensity) components of the display most be done in real time. Due to the speed of these display changes and the precise timing relationships that must be maintained between display events, direct sequencing of the display is beyond the capabilities of the processor. Instead, control data from the processor is sent to the Display Sequencer (a specialized integrated circuit) which responds by setting up the various signals that control the stages handling the real-time display signals. The controlled stages are stepped through a predefined sequence that is determined by the control data. Typically, as the sequence is being executed, the Display Sequencer will be changing vertical signal sources, Z-Axis intensity levels, triggering sources, and horizontal sweep signal sources. The specific activities being carried out by the Display Sequencer depend on the display mode called for by the control data.

Vertical deflection for crt displays comes from one or more of the four front-panel vertical inputs and, when displaying readout information, from the Readout circuitry. Signals applied to the front-panel Channel 1 and Channel 2 inputs are connected to their respective Preamplifiers via processor-controlled Attenuator networks. Control data from the Microprocessor defining the attenuation factor selected for each channel is serially loaded into the Auxiliary Control Register and then strobed into the Attenuator Mag-Latch Relays in parallel. The relay switches of each Attenuator network are either opened or closed, depending on the data supplied to the Mag-Latch Relay Drivers. The relays are magnetically latched and remain as set until new control data is strobed in. The Auxiliary Control Register is therefore available, and different mode data is clocked into the register to set up the operating mode of other portions of the instrument.

Attenuated Channel 1 and Channel 2 input signals are amplified by their respective Preamplifiers. The gain factor for the Channel 1 and Channel 2 Preamplifiers is settable by control data from the processor. The Channel 3 and Channel 4 input signals are amplified by their respective Preamplifiers by either of a choice of two gain factors set by control bits from the Auxiliary Control Register. All four of these preamplified signals are applied to the Vertical Channel Switch where they are selected by the Display Sequencer for display when required.

Each of the vertical signals is also applied to the A and B Trigger circuitry via trigger pickoff outputs from the Preamplifier stages. Any one of the signals may be selected as the trigger SOURCE for either the A or the B Trigger circuitry as directed by the Display Sequencer. The line trigger signal provides an added trigger source for A Sweeps only. Control data from the Microprocessor is written to the Trigger circuitry to define the triggering LEVEL, SLOPE, and COUPLING criteria. When the selected trigger signal meets these requirements, a sweep can be initiated. The Trigger circuit initiates both the A Sweep and the B Sweep as required by the display mode selected.

In the case of A Sweeps, the LO state of the trigger holdoff (THO) signal from the Display Sequencer enables the A Sweep circuit and the next A Trigger signal initiates

the sweep. For B Sweeps, and in the case of intensified sweeps, the A Sweep Delay Gate signal ($\overline{DG}$) enables the B Sweep circuit. Depending on the B Trigger mode selected, a B Sweep will be initiated either immediately (RUN AFT DLY) or on the next B Trigger signal (TRIG AFT DLY). The slope of the sweep ramp is dependent on Microprocessor-generated control data loaded into the internal control register of the A and B Sweep circuit hybrids.

Sweep signals generated by each of the Sweep hybrids are applied to the Horizontal Amplifier. The Horizontal Amplifier is directed by the Display Sequencer to select one of the sweep ramps for amplification in sequence. In the case of Readout and X-Y displays, the X-Readout and CH 1 input signals are selected to be amplified, also under direction of the Display Sequencer.

To control the display intensity, the Display Sequencer directs the Z-Axis circuit to unblank the display at the appropriate time for the sweeps and readout displays. When the display is unblanked, the Display Sequencer selects the display intensity for either waveform displays or for readout displays by switching control of the Z-Axis beam current between the front-panel INTENSITY and READOUT INTENSITY potentiometers as appropriate.

During readout displays, the vertical dot-position signal from the Readout circuitry is applied to the Vertical Amplifier via the Vertical Channel Switch. Horizontal dot-position deflection for the readout display is selected by internal switching in the Horizontal Amplifier.

The vertical, horizontal, and Z-Axis signals are applied to their respective amplifiers where they are raised to crt-drive levels. The output signals from the Vertical and Horizontal Amplifiers are applied directly to the crt deflection plates. The Z-Axis Amplifier output signal requires interfacing to the high-potential crt environment before application to the crt control grid. The necessary Z-Axis interfacing is provided by the DC Restorer circuit located on the High-Voltage circuit board. The resulting display may be of waveforms, alphanumeric readout, or a combination of both.

DETAILED CIRCUIT DESCRIPTION

INTRODUCTION

The following discussion provides detailed information concerning the electrical operation and circuit relationships of the 2445 Oscilloscope. Circuitry unique to the 2445 is described in detail, while circuits common in the electronics industry are not. The descriptions are accompanied by supporting illustrations and tables. Diagrams identified in the text, on which associated circuitry is shown, are located at the rear of this manual in the tabbed foldout pages.

PROCESSOR AND DIGITAL CONTROL

The Processor and Digital Control circuitry (diagram 1) directs the operation of most oscilloscope functions by following fimware control instructions stored in memory. These instructions direct the Microprocessor to monitor the front-panel controls and to send control signals that set up the various signal processing circuits accordingly.

Microprocessor

The Microprocessor (U2092) is the center of control activities. It has an eight-bit, bidirectional data bus for data transfer (D0 through D7) and a 16-bit address bus (A0 through A15) for selecting the source or destination of the data. Precise timing of instruction execution, addressing, and data transfer is provided by an external, crystal-controlled clock signal.

The clock signal is developed by the Microprocessor Clock stage and applied to the Microprocessor at pin 39. Using the external clock as a reference, the Microprocessor generates synchronized control output signals [R/$\overline{W}$ (read-write), E (enable), and VMA (valid memory address)] that maintain proper timing relationships throughout the instrument.

Microprocessor Clock

The Microprocessor Clock stage generates a 5-MHz square-wave clock signal to the Microprocessor and a 10-MHz clock signal to portions of the Readout circuitry. Inverter U2556A acts as an oscillator with crystal Y2568 providing feedback at the resonant frequency. The required phase shift for oscillation to occur is produced by C2565, C2566, R2564, and the crystal. The RC network composed of R2571, C2572, R2553, and R2573 biases input pin 1 of U2556A in the active region and establishes approximate

symmetry of the oscillator output. The signal is buffered and inverted by U2556B to provide the 10-MHz clock signal.

Flip-flop U2468A is a divide-by-two circuit that reduces the 10-MHz clock down to a 5-MHz square-wave signal used to clock the Microprocessor and the Display Sequencer. The 10-MHz clock is supplied to the Readout Board for dot timing and is also available for use with option circuitry.

Reset Control

The Reset Control circuitry ensures that, at power-up, the Microprocessor begins program execution from a known point in memory and with all the processor registers in known states. It also allows the processor to reset itself when power is turned off so that the instrument powers down in a known state.

POWER-UP SEQUENCE. Operational amplifier U2435 is configured as a comparator that generates the power-up reset. As power is applied to the instrument, the various power supplies start turning on and pull the noninverting input of U2435C (pin 10) above the inverting input level (pin 9). This action forces output pin 8 HI, and the reference level for the comparator at pin 10 is set to +3.7 volts by the divider network of R2648, R2646, and R2647. The HI from U2435C pin 8 is inverted by U2656A and applied to the processor $\overline{\text{RESET}}$ input (pin 40). When all the power supplies are operating, the PWR UP signal from J251 pin 12 goes HI, and capacitor C2661 begins charging positive through R2652. The time required for C2661 to charge to the comparator switching threshold is approximately 100 ms. When the voltage across C2661 reaches the +3.7-V reference level, the comparator switches states and pin 8 of U2435C goes LO. The $\overline{\text{RESET}}$ signal to the processor then goes HI to enable normal execution to begin, and the processor is directed to the starting address of the power-up routine, which it then performs.

POWER-DOWN SEQUENCE. When the instrument power switch is turned off, the PWR UP signal from J251 pin 12 immediately goes LO. This LO generates the $\overline{\text{NMI}}$ (non-maskable interrupt) request to the processor on pin 6 which causes the processor to branch to the power-down routine. Under direction of that routine, the processor begins shutting down the instrument in an orderly fashion before the power supply outputs can drop below the operating thresholds. This routine also places the EAROM in standby to prevent loss of data from the EAROM and disconnects the CH 1 and CH 2 50-Ω input terminations to protect them from accidental application of excessive voltage during storage or bench handling.

As the operating voltages are falling, the Reset circuitry must not generate a false $\overline{\text{RESET}}$ signal to the processor. Such a restart when the power supply voltages are outside their normal operating range would produce unpredictable processor operation that could possibly alter the contents of the EAROM. When the processor has completed all the other power-down tasks, it finally sets the PWR DOWN signal HI via U2208 (diagram 2). This signal is applied to inverter U2118A at pin 1. Pin 16 of U2118A goes LO and immediately pulls pin 10 of Reset Comparator U2435C LO to prevent a reset to the processor. This LO also forward biases CR2651, and C2661 begins discharging through CR2651 and R2552 to allow the voltage on pin 9 of the comparator to fall to zero. After about 1 ms, C2661 is fully discharged, and the processor sets the PWR DOWN signal to U2118A LO. The output of inverter U2118A then goes HI, and Reset Comparator U2435C immediately switches state to assert the $\overline{\text{RESET}}$ signal to the processor. The $\overline{\text{RESET}}$ signal is held LO until the power supplies have fully discharged.

For diagnostic purposes, the PWR DOWN reset signal can be disabled. Moving jumper P503 to the DIAG (diagnostic) position prevents C2661 from being discharged. The $\overline{\text{RESET}}$ signal is therefore held HI, and the processor can execute a free-running NOP (no operation) loop without interruption if the PWR DOWN bit is set HI while the Address Bus is incrementing.

Data Bus

Tri-state buffer U2194 is used to buffer the data signals to the Microprocessor from other devices on the bus. When not enabled, the device is switched to its high-impedance state to isolate the processor from the buffered Data Bus. Buffer U2194 is enabled via Read-Write Latch U2468B when the processor reads data from another device on the bus.

When the processor writes data onto the bus, Octal Latch U2294 is enabled by Read-Write Latch U2468B. When the E (enable) signal at pin 11 of U2294 is HI, processor data bits are passed asynchronously through the latch to the buffered Data Bus. When the E signal goes LO, data bits meeting setup times are latched into the device. The latched Q outputs provide the required drive current to the various devices on the bus and ensure that data hold times are met for correct data transfer. When the Read-Write Latch places a HI on pin 1 of U2294, the latch is disabled, and the outputs are switched to their high-impedance state.

Data transfer to and from the processor may be interrupted by removing Diag/Norm Jumper P503. This forces a NOP (no operation) condition that is useful for verifying the functionality of the processor (when a data-bus device

is suspected of causing a system failure) or for trouble-shooting the Address Bus and Address Decode circuitry. Removing the jumper removes the operating power from both U2194 and U2294 to disconnect the Microprocessor from the buffered Data Bus. With the Data Bus disconnected, a resistor network pulls the processor Data Bus lines (D0 through D7) to a NOP (no operation) instruction. A NOP causes the Microprocessor to continuously increment through its address field. The Address Decode circuitry may then be checked to determine if it is operating properly.

Address Decode

The Address Decode circuitry generates enabling signals and strobes that allow the Microprocessor to control the various devices and circuit functions. The controlling signals are generated as a result of the Microprocessor placing specific addresses on the Address Bus. Figure 3-2 illustrates the enables and strobes generated by the Address Decode circuitry.

Address decoding is performed by a series of three-line-to-eight-line decoders attached to the Address Bus. The three most significant address bits are decoded by U2480. This device initially separates the total addressable-memory space (64k-bytes) into eight, 8k-byte blocks. Addresses in the top 32k-bytes (address bit A15 HI) select one of four read-only memories (ROM), U2162, U2178, U2362, or U2378. When the VMA (Valid Memory Address) and E (Enable) outputs from the Microprocessor go HI, the

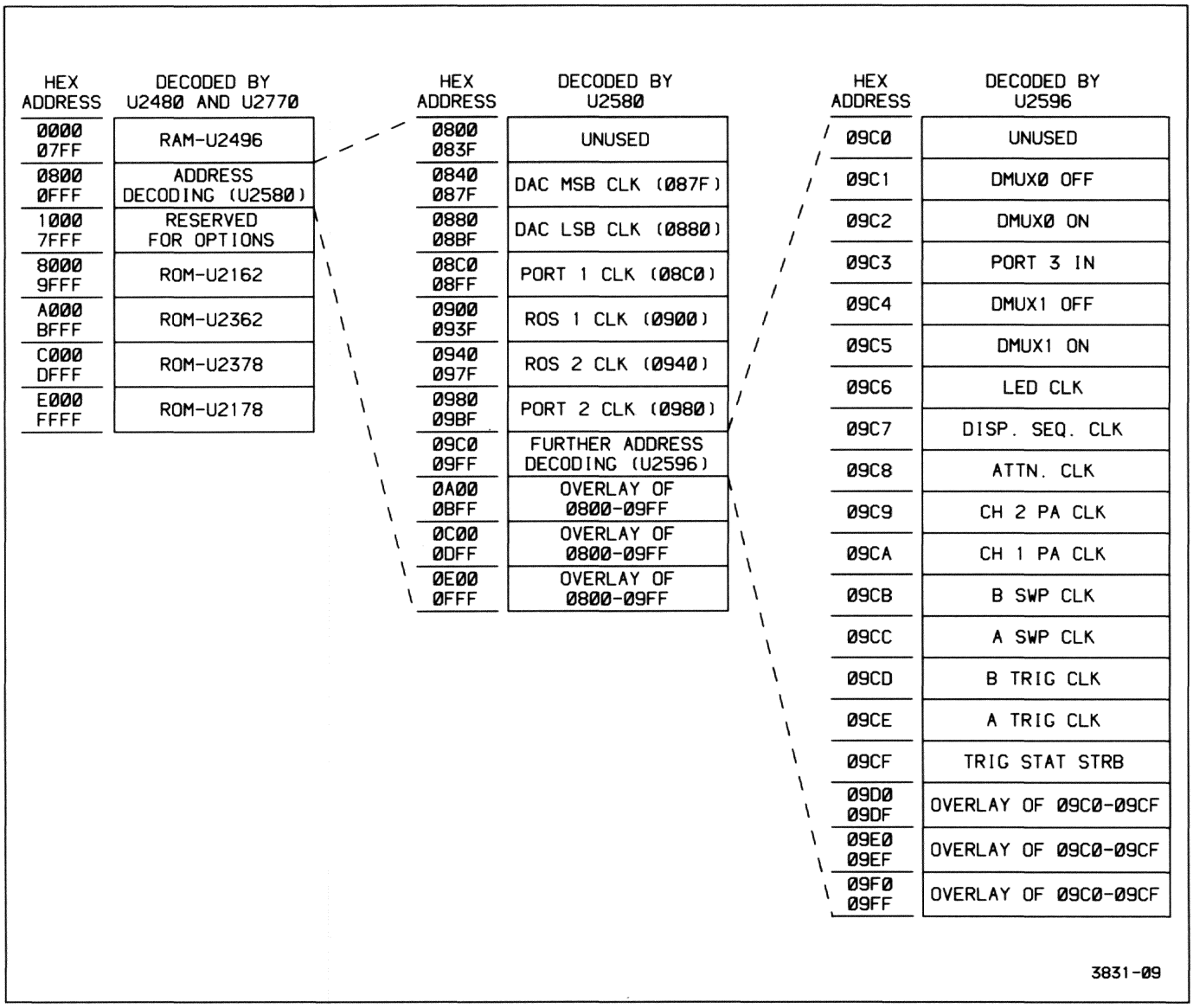


Figure 3-2. Address decoding.

selected ROM is enabled, and data from the selected address location is read out of the ROM.

Of the bottom 32k-bytes of addresses, only the lowest 8k-bytes are further decoded. When addresses in this 8k-byte range are decoded, the Y0 output of U2480 enables decoder U2770. This three-line-to-eight-line decoder separates the lowest 8k-byte address block into 2k-byte blocks. Any address falling into the lowest 2k-byte block of addresses will cause U2770 to generate an enable to the RAM (random-access memory) U2496. Addresses in the next highest 2k-byte block of addresses will enable U2580 to do the next stage of address decoding. The remaining 2k-byte blocks decoded by U2770 are not used.

The level of decoding performed by U2580 uses address bits A6, A7, and A8 to separate the addresses within the 2k-byte block of addresses 0800 to 0FFF into 32 groups of 64 addresses each. Address bits A9 and A10 are not used in the decoding scheme, so each of these 32 blocks is not uniquely identified. This results in four duplicate sections within the address block, each consisting of eight groups of 64 addresses. The upper three sections in the address space are never used; therefore, decoding by U2580 may be more simply thought of as eight groups of 64 address locations. Addresses within these eight groups generate control signals to other portions of the instrument.

The final level of address decoding is done by four-line-to-sixteen-line decoder U2596. When enabled by the Y7 output of U2580, this decoder separates the highest 64-address group decoded by U2580 into 16 individual control signals. In this level of decoding, address bits A4 and A5 are not decoded, so that the 64 possible addresses consist of four overlayed blocks of 16 addresses each.

Each of the control signals generated by the Address Decode circuitry are present only as long as the specific address defining that signal is present on the Address Bus. However, four of the addressable control signals decoded by U2596 are used to either set or reset flip-flops U2656B and U2656D. The control signals are, in effect, latched and remain present to enable multiplexers U2335 (diagram 2) and U170 (diagram 4). When enabled, these multiplexers route analog control signals from DAC (digital-to-analog converter) U2235 (diagram 2) to the various analog control circuits.

Read-only Memory (ROM)

The Read-only Memory consists of four, 8k-byte ROMs that contain the operating instructions (firmware) used to control processor (and thus oscilloscope) operation. Addresses from the Microprocessor that fall within the top 32k-bytes of addressable space cause one of the four read-only memory integrated circuits to be enabled. (See Address Decode description.) Instructions are read out of the enabled ROM (or PROM) IC from the address location present on its 13 address input pins (A0 through A12). The eight-bit data byte from the addressed location is placed onto the buffered Data Bus (BD0 through BD7) to be read by the Microprocessor.

Random-Access Memory (RAM)

The RAM consists of integrated circuit U2496 and provides the Microprocessor with 1k-byte of temporary storage space for data that is developed during the execution of a routine. The RAM is enabled whenever an address in the lowest 2k-byte of addresses is placed on the Address Bus. When writing into the RAM, the write-enable signal ($\overline{WE}$) on pin 21 of U2496 is set LO along with the chip enable ($\overline{CE}$) signal on pin 18. At the same time, the output-enable signal ($\overline{OE}$) on pin 20 is HI to disable the RAM output drivers. Data is then written to the location addressed by the Microprocessor. If data is to be read from the RAM, the $\overline{WE}$ signal is set HI to place the RAM in the read mode, and the $\overline{OE}$ signal is set LO to enable the output drivers. This places the data from the addressed location on the buffered Data Bus where it can be read by the Microprocessor.

Timing Logic

The Timing Logic circuit composed of U2468B, U2556F, U2556C, and U2656C generates time- and mode-dependent signals from control signals output from the Microprocessor. The enable (E) signal output from the Microprocessor is a 1.25-MHz square wave used to synchronize oscilloscope functions to processor timing.

Data applied to the Address Bus, Data Bus, and various control signals are allowed to settle (become valid) before any of the addressed devices are enabled. This is accomplished by switching the E signal HI a short time after each processor cycle begins. The delayed enable signal is inverted by U2556C to provide the active LO signal ($\overline{E}$) that enables the Address Decode circuit after the Address Bus has settled.

Read-Write Latch U2468B is used to delay the read/write signal (R/$\overline{W}$) from the Microprocessor to meet hold-time requirements of the RAM. At the same time, it generates delayed read and write enabling signals of both polarities to meet the requirements of Buffer U2194 and Latch U2294 (in the Microprocessor Data Bus) and various other devices in the Readout circuitry (diagram 7).

When R/$\overline{W}$ goes LO for a write cycle, Read-Write Latch U2468B is reset, and the Q output (pin 9) is held LO. Latch U2294 is in its transparent state at this time, and

data from the Microprocessor is applied asynchronously to the buffered Data Bus. At the end of the write cycle, the R/$\overline{W}$ signal goes HI, and the reset to U2468B is removed. The E signal also goes through a negative transition, and data on the Microprocessor data bus lines is latched into U2294. The next positive transition of the 1.25-MHz E signal (1/2 E cycle after the R/$\overline{W}$ signal goes HI) clocks the HI level at U2468B pin 12 (the D input) to the Q output, and the $\overline{Q}$ output (pin 8) goes LO. The 1/2 E cycle delay between the time R/$\overline{W}$ goes HI and the time that the Q output of U2468B goes HI keeps Latch U2294 outputs on long enough to meet the data hold time for the RAM. At the end of that delay time, pin 1 of U2294 goes HI, and the Latch outputs are switched to the high-impedance state to isolate it from the buffered Data Bus.

A write-enable signal to the RAM is generated by the circuit composed of U2656C and U2556F. The processor R/$\overline{W}$ signal is inverted by U2556F and NANDed with the enable signal (E) by U2656C. The write enable to the RAM at U2656C pin 9 is produced after the address data has settled. This action prevents writing to improper RAM address locations.

READOUT FRAMING AND INTERRUPT TIMING. Binary Counter U2668 is used to generate a readout-framing clock to the Readout circuitry and a real-time interrupt request to the Microprocessor via inverter U2556E. The readout-framing clock is a regular square-wave signal obtained from U2668 pin 14 by dividing the 1.25-MHz $\overline{E}$ signal from U2556C pin 6 by 1024 (2^{10}). This clock tells the readout circuitry to load the next block (subframe) of readout information to be displayed. (See "Readout" description for further information concerning the alphanumeric display.) The real-time interrupt request, which occurs every 3.3 ms, is obtained from pin 2 by dividing the $\overline{E}$ signal by 8192 (2^{13}).

When the real-time interrupt request occurs, $\overline{IRQ}$ (pin 4 of U2092) goes LO, and the processor breaks from execution of its mainline program. The Microprocessor first resets Binary Counter U2668 by setting pin 19 of U2043 (diagram 2) HI (to generate the reset), then it resets pin 19 LO to allow the counter to start again. At this time, the Microprocessor sets analog control voltages and reads trigger status from the Display Sequencer (diagram 11). When this is completed, it reverts back to the mainline program.

In addition to the analog control and trigger status update that occurs with each interrupt, on every fifth interrupt cycle the Microprocessor also scans the front-panel potentiometers. Every tenth interrupt cycle, scanning the front-panel switches and checking the 50-Ω DC inputs for overloads is added to the previously mentioned tasks. If all the tasks are not completed at the end of one interrupt cycle, the real-time interrupt request restarts the analog updates, but as soon as those are accomplished, the Microprocessor will pick up with its additional tasks where it was before the interrupt occurred. This continues until all tasks are completed. If any pot or switch changes are detected, the Miroprocessor updates the analog control voltages and the control register data to reflect those changes prior to reverting back to the mainline program instructions.

ANALOG CONTROL

The Analog Control circuitry (diagram 2), under Microprocessor control, reads the front-panel controls and sets various analog control voltages to reflect these front-panel settings. The calibration constants determined during instrument calibration and the last "stable" front-panel setup conditions (unchanged for approximately seven seconds) are stored in EAROM (elecrically-alterable read-only memory). At power-on the stored front-panel information is used to return the instrument to its previous operating state.

Status Buffer

Data transfer from the Analog Control circuitry to the Microprocessor is via Status Buffer U2108. Data bits applied to the input pins are buffered onto the Data Bus when enabled by the Address Decode circuitry. Via the Status Buffer, the processor is able to (1) determine the settings of front-panel pot and switches, (2) read the EAROM data, (3) find out if the readout display should be switched on or off, (4) determine if a triggered sweep is in progress, and (5) read the contents of the Readout RAM. When disabled, the buffer outputs are switched to high impedance states to isolate them from the buffered Data Bus.

Front Panel Switch Scanning

The Front Panel Switches are arranged in a matrix of ten rows and five columns. Most of the row-column intersections contain a switch. When a switch is closed, one of the row lines is connected to one of the column lines through a diode. Reading of the switches is accomplished by setting a single row line LO and then checking each of the five column lines sequentially to determine if a LO is present (signifying that a switch is closed). After each of the five columns has been checked, the current row line is reset HI and the next row line is set LO for the next column scan cycle. A complete Front Panel Switch scan consists of setting all ten row lines LO in sequence and performing a five-column scan for each of the rows.

Row lines are set LO when the Microprocessor writes a LO to one of the flip-flops in octal registers U2034 and

U2134. The Row data placed on the buffered Data Bus by the Microprocessor is clocked into the registers as two, eight-bit words by clocks from the Address Decode circuitry (DAC LSB CLK for the lower eight bits and DAC MSB CLK for the upper eight bits). All eight outputs of register U2134 and two outputs of register U2034 drive the ten rows of the front-panel switch matrix (the eleventh line is not used in the matrix). Series resistors in the lines limit current flow and eliminate noise problems associated with excessive current flow.

While each row is selected, the processor will scan each of the five lines in sequence. To scan the columns, the processor increments the three data select bits to U2034 that define the column to be checked. Eight-line data selector U2456 connects the associated column line to Status Buffer U2108. As each line is selected, the Microprocessor reads the Status Buffer to determine if the associated switch is open or closed.

In addition to the front-panel switches, the CAL/NO CAL jumper (P501) is checked to determine whether the instrument should be allowed to execute the calibration routines. The levels on U2456 pins 7 and 9 are read by scanning two additional columns at power-up. If the jumper is pulling the CAL bit LO, the operator will be allowed to use the calibration routines stored in firmware. If the NO CAL bit is pulled LO, the calibration routines may not be performed. If the jumper is removed, and neither bit is pulled LO, the Microprocessor is forced into a special diagnostic mode (CYCLE) used to record certain operating failures during long-term testing of the instrument. (See the "Maintenance" section of this manual for an explanation of the diagnostic modes.) Removing P501 or switching it between the CAL and NO CAL positions will not be recognized by the Microprocessor until the instrument is powered down and then turned back on.

The SI (scope identification) bit is checked at power-up to determine if the instrument is a 2445. Some parts of the firmware are shared with a similar instrument, the 2465, and the check is necessary for the Microprocessor to distinguish between the two instruments. A HI on the SI bit indicates that the instrument is a 2445.

The resistors in series with the input lines to U2456 are current-limiting resistors that protect the CMOS eight-line data selector from static discharges. The resistors connected from the input lines to the +5-V supply are pull-up resistors for the front-panel column lines.

Digital-to-Analog Converter (DAC)

DAC U2234 is used to set the various analog references in the instrument and is used to determine the settings of the front-panel potentiometer. The 12-bit digital values to be converted are written to octal registers U2034 and U2134 for application to the DAC input pins. The DAC then outputs two complementary analog currents that are proportional to the digital input data. (Complementary, in this case, means that the sum of the two output currents is always equal to a fixed value.)

The maximum range of the output currents is established by a voltage-divider network composed of R2127, R2227, R2228, and R2229 connected to the positive and negative reference current inputs of the DAC (pins 14 and 15 respectively). A +10-V reference voltage applied to the DAC through R2228 sets the basic reference current. Resistor R2229 and potentiometer R2127 provide a means to adjust this current over a small range for calibration purposes. The nominal reference current is 1 mA, and the DAC full-scale output current is 4 mA. The output currents flow through series resistors R2324 and R2325, connected to the +1.36-V reference, and proportional voltages result.

Pot Scanning

The Pot Scanning circuitry, in conjunction with the DAC, derives digital values for each of the various front-panel potentiometers. Scanning of the pots is accomplished by data selectors U2408 and U2418. Three bits are written to register U2208 and select the pot to be read. The bits are latched in the register and keep the pot selected until the register is reset. The Microprocessor writes a LO to the inhibit input (pin 6) of either U2408 or U2418 via register U2308 to enable the device. The enabled data selector connects the analog voltage at the wiper of the selected pot to comparator U2214.

Comparator U2214 compares the analog voltage of each pot to the output voltage from the DAC (pin 18). To determine the potentiometer output voltage, the processor performs a binary search routine that changes the output voltage from the DAC in an orderly fashion until it most closely approximates the voltage from the pot.

The conversion algorithm is similar to successive approximation and generates an eight-bit representation of the analog level. When the pot's value is determined, the Microprocessor stores that value in memory. Once all the pots have been read and the initial value of each has been stored, the processor uses a shorter routine to determine if any pot setting changes. To do this the DAC output is set to the last known value of the pot (plus and minus a small drift value), and the status bit is read to see that a HI and LO occurs. If within the limits, the processor assumes that the pot setting has not changed and scans the next pot. When the processor detects that a pot setting has changed, it does another binary search routine to find the new value of that pot.

Analog Control

The operating mode and status of the 2445 require that various analog voltages (for controlling instrument functions) be set and updated. The digital values of the controlling voltages are generated by the Microprocessor and converted by the DAC. Analog multiplexers U2335 (on diagram 2) and U170 (on diagram 4) route the DAC voltages to sample-and-hold circuits that maintain the control voltages between updates.

The Microprocessor writes three selection bits to register U2034 that directs the DAC output to the appropriate sample-and-hold circuit and charges a capacitor (or capacitors) to the level of the DAC. When the processor disconnects the DAC voltage from the sample-and-hold circuit (by disabling the multiplexer) the capacitor(s) remains charged and holds the control voltage near the level set by the DAC. Due to the extremely high input impedance of the associated operational amplifiers, the charge on the capacitor(s) remains nearly constant between updates.

EAROM

EAROM (electrically-alterable read-only memory) U2008 provides nonvolatile storage for the calibration constants and the power-down front-panel settings. When power is applied to the 2445, the Microprocessor reads the calibration constants and generates control voltages to set up the analog circuitry. The front-panel settings that were present at power-off are recalled to return the instrument to that same operating mode.

The EAROM is a metal-nitride-oxide-semiconductor device (MNOS) and requires a TTL-to-MNOS level shift of the input control and data signals. A MNOS-to-TTL level shift of the output data is also required. Inputs to U2008 are shifted to MNOS levels by U2118B through U2118F and the associated components while output data is shifted back to TTL levels by Q2025, U2118G, and the associated components.

The EAROM data, address, and mode-control bits are written by the Microprocessor to five flip-flops of register U2208. The register outputs drive the level-shifting network in the associated line. Three of thise latched bits define the EAROM mode and will direct data into and out of the device. These three mode control bits are applied to pins 7, 8, and 9 of U2008 and set the mode to either Accept Address, Accept Data, Write Data, Read Data, or Shift-Data-Out.

When writing data into the EAROM, the mode is first set to Accept Address, then the address of the location to be altered is applied to the I/O port (pin 12) as a specially encoded sequence of 20 single bits via U2118C, R2020, and CR2021. This sequence of bits is two, one-of-ten codes where the position of the first LO bit in the sequence represents the most-significant bit of the address (in decimal) and the position of the second LO represents the least-significant digit (see Figure 3-3).

The processor clocks each of the 20 bits into the internal address register by clocking U2008 pin 6 via the clock level shifting network (U2118C and associated components).

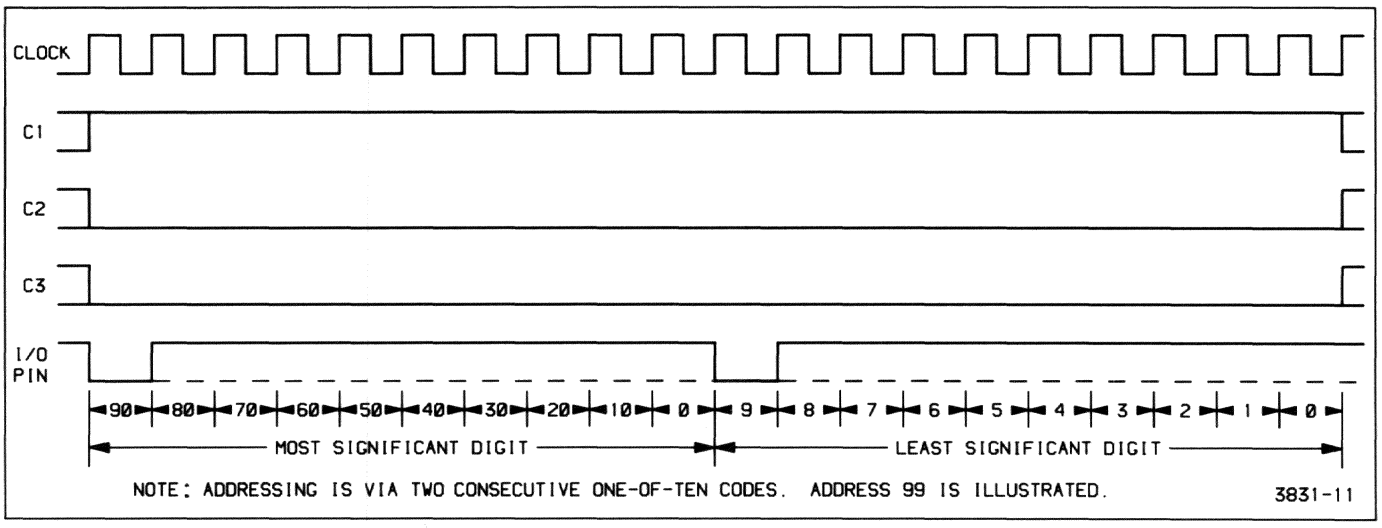


Figure 3-3. Accept address timing.

Internal address decoding within U2008 then enables the selected address location. The three mode-control bits are then set to the Accept Data mode, and the new 14-bit serial data word is applied to the I/O pin. The data bits are clocked into a temporary data-storage register and the mode-control bits are set to the Write mode. A series of clock pulses then writes the data from the temporary data storage register to the addressed location.

When reading from the EAROM, the processor first sets the three-bit mode-control word to Accept Address as in writing, and the 20-bit address is clocked into the EAROM. Now the mode-control word is set to Read Data, and a single clock pulse moves the data from the addressed location to the temporary data-storage register in parallel. The EAROM mode is then set to Shift Data Out, and the 14-bit data word is clocked serially from the temporary storage register to the I/O pin.

The output data is applied to Q2025, U2118G, and the associated components, to shift it to TTL levels. The Status Buffer U2108 applies the data to the Data Bus where the Microprocessor may read it.

FRONT-PANEL CONTROLS

The Front Panel is the operator's interface for controlling the user-selectable oscilloscope functions. Along with the crt, it provides visual feedback to the user about the present operating state of the instrument.

Most of the Front-Panel controls (diagram 3) are "cold" controls; they are not connected directly into the signal path. Therefore, associated circuits are not influenced by the physical parameters (such as capacitance, resistance, and inductance) of the controls. In addition, translating the analog output levels of some of the potentiometers to digital equivalents allows the processor to handle the data in ways that result in a variety of enhanced control features.

To maintain the front-panel operating setup between uses of the instrument, the digitized values of the potentiometers and front-panel switch settings are stored in EAROM at regular intervals (approximately every seven seconds) so that when the instrument power is turned off, these control settings are not lost. Then, when power is next applied, the instrument will power up to the same configuration as when the power was last removed (assuming the settings of the nondigitized pots and switches remain the same).

The Front-Panel controls also allow the user to initiate and direct the diagnostic routines (and when enabled, the calibration routines) programmed into the read-only memory (ROM). These routines are explained in the Maintenance section of this manual.

Front-Panel Switches

The Front-Panel Switches are arranged in a ten-row-by-five-column matrix, with each switch assigned a unique location within the matrix (see Figure 3-4). A closed switch connects a row and a column together through an isolating diode. To detect a switch closure, the switch matrix is scanned once every 32 ms (every tenth Microprocessor interrupt cycle). When scanning, the Microprocessor sequentially sets each individual row line LO. A closed switch enables the LO to be passed through the associated diode to a column line. When the processor checks each of the five column lines associated with the selected row, the LO column is detected. The intersection of the selected row and the detected column uniquely identifies the switch that is closed. Further information about switch scanning is found in the "Front-Panel Switch Scanning" description located in the "Analog Control" discussion.

As each switch is read, the processor compares the present state of the switch to its last-known state (stored in memory) and, if the same, advances to check the next switch. When a switch is detected as having changed, the processor immediately reconfigures the setup conditions to reflect the mode change and stores the new state of the switch in memory. The detected status of the switch on each of the following scan cycles is then compared against the new stored data to determine if the switch changes again. The 32-ms delay between the time a switch is detected as having changed and the next time it is read effectively eliminates the effects of switching noise (switch bounce) that may occur after the switch is actuated.

Front-Panel Potentiometers

The thirteen Front-Panel Potentiometers are "cold" controls that control the linear functions of the instrument. (SCALE ILLUM, READOUT INTENSITY, INTENSITY, and FOCUS are not considered part of the Front-Panel Control circuitry for the purposes of this description.) Of these, eight are digitized and control their functions indirectly. The remaining five potentiometers (four vertical POSITION pots and the TRACE SEP pot) control their respective circuit functions directly. Data Selectors U2048 and U2148 in the Analog Control circuitry (diagram 2) route the wiper arm voltage of the pot being read to comparator U2214 where it is compared with the output of DAC U2234. The processor changes the DAC output until it most closely matches the output voltage of the pot, then stores the digital value of that "match". See the "Front-Panel Switch Scanning" description in the "Analog Control" discussion for further information on the reading of pot values.

Like the switch matrix scanning, the Front-Panel pot scanning routine is performed every 32 ms. When entered, the routine reads the settings of the last-moved pot and one unmoved pot. Each succeeding scan continues to read the last-moved pot, but a new unmoved pot is read. In this way, each pot is monitored, but most of the scan time is devoted to the pot that is most likely to still be moving (needing continuous updating).

As the initial pot settings are determined, a digital representation of each value is stored in memory. The processor then checks each pot against its last-known value to determine if a pot has moved. If a pot is detected as moving, the processor executes a routine that converts the movement (displacement from last-set value) into a corresponding control voltage.

When producing the actual analog control levels, the processor can manipulate the digital values read for the various pots before sending the output data to the DAC. This allows many of the oscilloscope parameters to vary in an enhanced fashion. The pot data is manipulated by the processor in a manner that produces such features as variable resolution, continuous rotation, fine-resolution backlash, and electrically detented controls.

In the cases of the TRIGGER LEVEL, Horizontal POSITION, VOLTS/DIV VAR, and SEC/DIV VAR controls, the processor reads the magnitude and direction of pot rotation and produces variable-resolution control voltages. If a pot's direction of rotation changes, the magnitude of the change from the last-set position remains small, or if it was not the

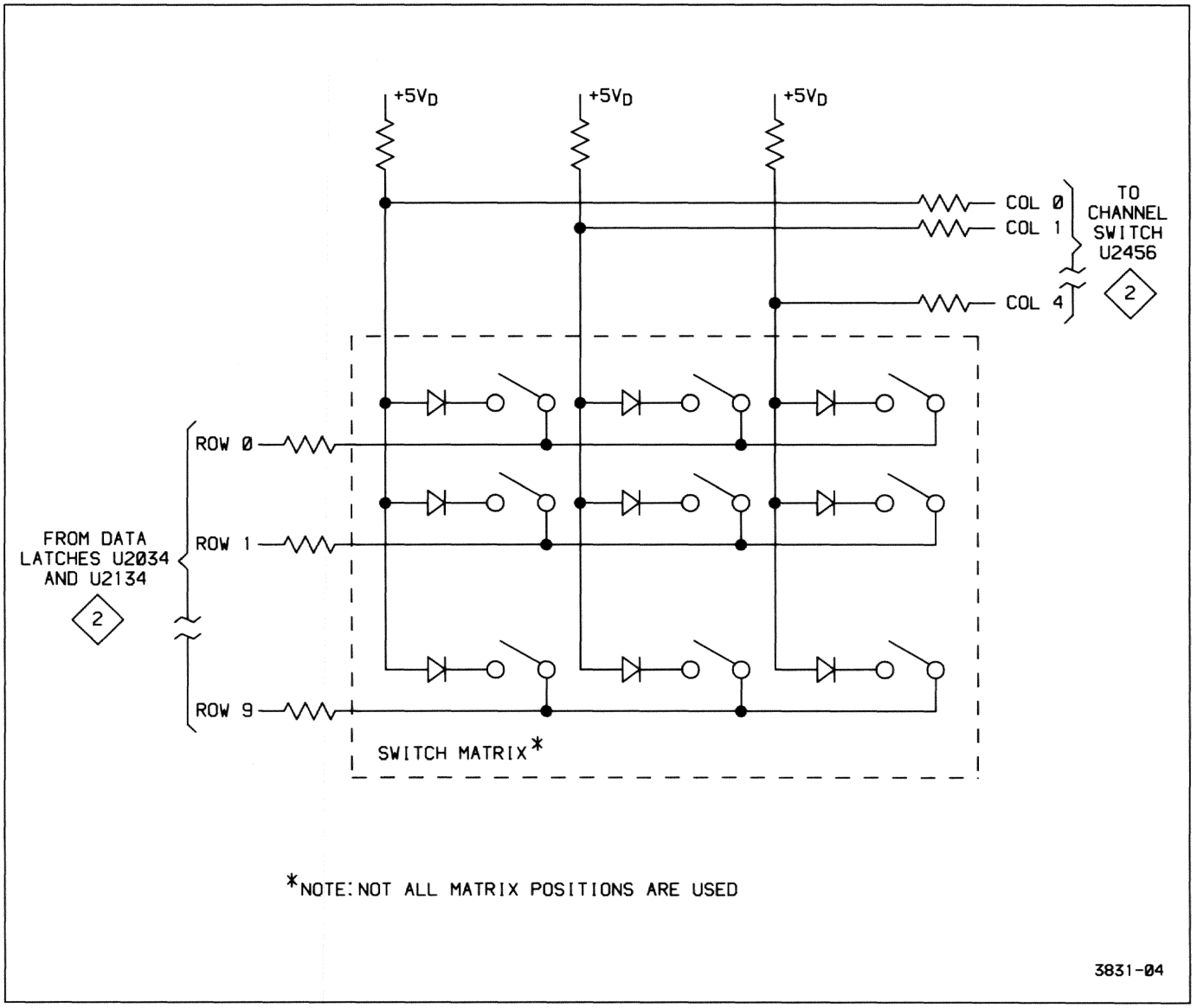


Figure 3-4. Front-Panel Switch matrix.

last pot moved, a fine-resolution control voltage results. In the fine-resolution range, a given rotational displacement will cause a small control voltage change. The same displacement farther away from the last-set reference will cause a proportionally larger control voltage change, producing a coarse-resolution effect. If the changing pot is the last one moved and the direction of rotation remains the same, the algorithm continues from where it left off during the preceding scan; producing control voltage changes with the same increment as it was last using.

The delta reference controls (Δ REF OR DLY POS and Δ) are continuous-rotation potentiometers. They each consist of two pots ganged together with their wiper arms electrically oriented 180° apart. As the wiper of one pot is leaving its resistive element, the wiper of the other pot comes onto its element. The Microprocessor has the ability to watch the output voltage from each wiper and when it detects that the controlling wiper is nearing the end of its range, it will switch control over to the other wiper. The routine the processor uses to watch these pots sets the associated control voltage on the basis of relative voltage changes (ΔV) that occur. Switching between the pots to change control to the opposite wiper arm is based on the specific voltage levels being sensed.

Sensing specific voltage levels is also used when reading the VOLTS/DIV VAR and SEC/DIV VAR controls. These pots have both a mechanical detent and a processor-generated electrical detent. As one of these controls is moved out of the mechanical detent position, the processor watches the analog voltage changes that occur; but the associated control voltage will not change until a specific voltage level (the electrical detent level) is reached. Once the electrical detent value is exceeded, the processor begins to vary the associated control voltage in response to further pot rotation. When returning to the mechanical detent position, the electrical detent level is reached first, and the variable voltage action is stopped before the mechanical detent is entered.

Front-Panel Status LED

Light-emitting diodes (LED) are used to provide visual feedback to the operator about the oscilloscope status and operating mode by backlighting front-panel nomenclature. A 32-bit status word, defining the diodes to be illuminated, is generated by the processor and then serially clocked into the four LED-Status Registers (U3300, U3325, U3350, and U3375). The registers hold the selected diodes on until the next update. Whenever the processor detects that a front-panel control has changed (and a different status display is required), a new status word is generated and applied to pin 1 of U3300. As each of the bits is clocked into the Q_A position of U3300, the preceding bit is shifted to the next register position. After 32 bits have been clocked into (and 24 bits through) U3300, all four LED-Status registers are full and contain the LED illumination pattern to be displayed to the user. A LO at any Q output of the registers illuminates the corresponding front-panel LED.

The TRIG'D LED is not driven by the LED-Status Register. It is driven by the Analog Control circuitry and illuminated whenever a triggered sweep is in progress.

ATTENUATORS AND PREAMPLIFIERS

The Attenuators and Preamplifiers circuitry (diagram 4) allows the operator to select the vertical deflection factors. The Microprocessor reads the Channel VOLTS/DIV switches and VOLTS/DIV VAR controls and then digitally switches the attenuators and sets the preamplifier gains accordingly.

Channel 1 and Channel 2 Attenuators

The Channel 1 and Channel 2 Attenuators are identical in operation, with corresponding circuitry in each channel performing the same function. Therefore, only the Channel 1 circuitry is described.

Input signals from the Channel 1 input connector are routed through an attenuator network by four pairs of magnetic-latch relay contacts. The position of the relays is set by Microprocessor data placed into Auxiliary Control Register U140. Relay buffer U110 provides the necessary drive current to the relays.

Four input coupling modes (1 MΩ AC, GND, 1 MΩ DC, and 50 Ω DC) and three attenuation factors (1X, ÷10, and ÷100) may be selected by closing different combinations of relay contacts. The three attenuation factors, along with the variable gain factors of the Vertical Preamplifier, are used to obtain the crt deflection factors. The relays are magnetically latched and once set, remain in position until new attenuator-relay-setting data and strobes are generated. (See the "Auxiliary Control Register" description for a discussion of the relay-latching procedure.)

The 50 Ω termination resistor has a thermal sensor associated with it that produces a dc voltage (CH 1 OVL) proportional to the input power. Should the input power exceed the normal safe-operating level for the 50 Ω DC input, the termination resistor temperature will exceed the normal operating limit and will change the output voltage of the thermal sensor. The amplitude of this dc level is periodically checked via comparator U2214 and DAC U2234 (on diagram 2) and allows the Microprocessor to detect when an overload condition is present. When an overload occurs, the processor switches the input coupling to the 1 MΩ position to prevent damage to the attenuator and displays **50 Ω OVERLOAD** on the crt.

Compensating capacitor C105 is adjusted at the time of calibration to normalize input capacitance of the preamplifier to the attenuator.

A probe-coding ring around the BNC input connector passes probe-coding information (a resistance value to ground) to the Analog Control circuitry for detection of probe attenuation factors. The readout scale factors are set to reflect the detected attenuation factor of the attached probe.

Auxiliary Control Register

The Auxiliary Control Register allows the Microprocessor to control various mode and range dependent functions of the 2445. Included in these functions are: attenuation factors, Channel 3 and Channel 4 gains, vertical-bandwidth limiting, and the X-Y display mode.

When the Microprocessor sets the input coupling mode and attenuation factors for Channel 1 and Channel 2, a series of eight, 16-bit control words are serially clocked into shift registers U140 and U150 (eight bits in each register). Each control word is used to set the position of one of the eight attenuator and coupling relays (four relays are in each attenuator assembly). Each control word will have only the bit corresponding to the specific relay contact to be closed set HI. Relay buffers U110 and U130A (for Channel 1) and U120 and U130B (for Channel 2) are Darlington configurations that invert the polarities of all bits. This results in a LO being applied to only the coil lead associated with the contact to be closed; all other coil leads are held HI.

To set a relay once the control word is loaded, the Microprocessor generates a ATTN STRB (attenuator strobe) to U130G pin 7 via R129 and C130. The strobe pulses the output of U130G LO for a short time. This output pulse attempts to turn on both Q130 and Q131 (relay drivers) via their identical base-bias networks. Due to the lower level from the turned on Darlington relay buffer (coupled through the associated coil diode and either CR130 or CR131 to one of the bias networks), one transistor will turn on harder as the ATTN STRB pulse begins to forward bias the transistors. The more positive collector voltage of the transistor turning on harder is fed through the bias diode (again either CR130 or CR131) to further turn off the opposite transistor. This action results in one transistor being fully on and the other one being fully off. The saturated transistor sources current through the two stacked relay coils to the LO output of either U140 or U150 (current sink) to close the selected contacts. Once set, the magnetic-latch feature will hold the relay set to this position until opposing data is clocked into the Auxiliary Control Register and strobed into the relay. All coil leads for the remaining relays are set HI, and only the selected relay will be set.

To set the seven remaining Attenuator and coupling relays, the sequence just described is repeated seven more times. Whenever the Microprocessor determines that the attenuation factor or input coupling has changed, the entire relay-setting procedure is repeated for all eight relays.

After the coupling and attenuator relays have been latched into position, the Auxiliary Control Register is free to be used for further circuit-controlling tasks. Eight more bits of control data are then clocked into U140 either to enable or disable the following functions: vertical bandwidth limiting (BWL), triggered X-Y mode (TXY), the A and B Sweep Delay Comparators (BDCA and BDCB), and slow-speed intensity limit (SIL); or to alter the Channel 3 and Channel 4 gain factors (GA3 and GA4). Two other bits are clocked into register U150: one to produce the CTC signal and the other to control the scale illumination circuit during SGL SEQ display mode. The CTC control bit is used to enable a sweep-start linearity circuit in the A Sweep circuitry (diagram 5) on the 2 ns and 20 ns per division sweeps.

Analog Control Multiplexer

When enabled by the Address Decode circuitry, Analog Control Multiplexer U170 directs the analog levels applied to pin 3 from DAC U2234 (diagram 2) to one of six sample-and-hold circuits. In the Preamplifier circuitry, the sample-and-hold circuits maintain the VAR gain and DC Bal control-voltage levels applied to both the Channel 1 and Channel 2 Preamplifiers U100 and U300 between updates. Two of the Multiplexer outputs direct analog levels to the Holdoff and Channel 2 Delay Offset sample-and-hold circuits (diagram 5). Routing is determined by the three-bit address from register U2034 (diagram 2) applied to Multiplexer U170 on pins 9, 10, and 11.

Channel 1 Preamplifier

Channel 1 Preamplifier U100 converts the single-ended input signal from the Channel 1 Attenuator to a differential output signal used to drive the Vertical Channel Switch. The device produces either amplification or attenuation in predefined increments, depending on the control data written to it from the Microprocessor. The Preamp also has provisions for VAR gain, vertical positioning, and a trigger signal pickoff.

The Channel 1 vertical input signal is applied to pin A of Channel 1 Preamp U100. Control data from the processor is clocked into the internal control register of the device via pin 22 (CD) by the clock signal applied to pin 23 ($\overline{CC}$). The data sets the device to have an input-to-output gain ratio of either 2.5 or 1 or to have an attenuation factor of 2, 4, or 10, depending on the VOLTS/DIV control setting.

Two analog control voltages set by the DAC and the Channel 1 vertical position dc level modify the differential output signal at pins 9 and 10. The front-panel Channel 1 POSITION control supplies a dc level to U100 pin 17 that vertically positions the Channel 1 display on the crt. A DC Bal signal is applied to pin 2 of U100 from the DAC via the sample-and-hold circuit composed of U160A and C177. This DC Bal signal is a dc offset-null level that is determined during the automatic DC Bal procedure. The offset value is stored as a calibration constant in the EAROM and is recalled at regular intervals to set the DC Bal level, holding the Preamp in a dc balanced condition.

The Channel 1 VOLTS/DIV VAR control is monitored by the Microprocessor during the front-panel scanning routine. When the processor has determined where the VOLTS/DIV VAR control is positioned, it causes DAC U2234 (diagram 2) to produce a corresponding control level and routes it to the VAR gain sample-and-hold circuit composed of U160D, C179, and associated components. The control voltage at the output of U160D (pin 14) sets the variable gain of the Preamp.

A pickoff amplifier internal to U100 conditions the trigger signal and provides the proper signal level at pin 15 to drive the A/B Trigger Generator (U500, diagram 5). The pickoff point for the trigger signal is prior to the addition of the vertical position offset, so the position of the signal on the crt has no effect on the trigger operation. However, the pickoff point is after the DC Bal and Variable gain signals have been added to the signal so both of these functions will affect trigger operation.

Common-mode signals are rejected from the trigger signal by the circuitry composed of operational amplifier U450A and associated components. The inverting input of U450A (pin 6) is connected to the common-mode point between APO+ (pin 12) and TPO– (pin 15) of U100. Any common-mode signals present are inverted and applied to a common-mode point between R451 and R453 to cancel the signals from the differential output. A filter network composed of LR180 and the built-in circuit board capacitor (5.6 pF) reduces trigger noise susceptibility. Trigger signals for options are obtained by removing P100A and connecting the appropriate connector.

The Channel 1 input signal used to provide the horizontal deflection for the X-Y displays is obtained from U100 pin 11. The components between pin 11 and the Horizontal Output Amplifier provide phase compensation of the signal. During instrument calibration, the delay produced by C115, C116, L115, R115, and variable capacitor C118 is matched to the 78-ns delay of the vertical delay line (DL100, diagram 6).

Channel 2 Preamplifier

Operation of Channel 2 Preamplifier U200 is nearly identical to that of the Channel 1 Preamplifier just described. The exceptions are that the output polarity of the Channel 2 signal may be either normal or inverted and that the signal obtained from the BPO+ output (pin 11) is conditioned differently for a different purpose than in the Channel 1 Preamplifier circuitry.

Inverting the Channel 2 signal for the CH 2 INVERT feature is accomplished by biasing on different amplifiers. The control data clocked into the internal control register from pin 22 sets up the necessary switching.

The Channel 2 BPO+ signal at U200 pin 11 provides an accurate representation of the Channel 2 signal at the rear-panel CH 2 OUT connector. The BPO+ output signal is reduced by divider R460 and R461 and is applied to the emitter of Q460B. Transistor Q460B, configured as a diode, provides thermal compensation for the bias voltage of Q460A and reduces dc level shifts with varying temperature. Emitter-follower Q460A provides the drive and impedance matching to the CH 2 OUT connector and removes the diode drop added by Q460B. Clamp diodes CR460 and CR461 protect Q460B should a drive signal be accidentally applied to the CH 2 OUT connector.

Channel 3 and Channel 4 Preamplifier

The functions provided by the Channel 3 and Channel Preamplifier are similar to those provided by the Channel 1 and Channel 2 Preamplifiers. The single-ended CH 3 and CH 4 input signals are converted to differential signals, and vertical gain and vertical positioning information is added to the output signals. Trigger pickoff signals are generated for both channels and are routed to the Trigger hybrid.

Channel 3 and Channel 4 gains may be either 0.1 volt per division or 0.5 volt per division. The logic levels of control bits applied to U300 pin 30 (GA3) and pin 31 (GA4) from Auxiliary Control Register U140 sets the gain of the Channel 3 and Channel 4 Preamplifiers respectively. Vertical positioning of the Channel 3 and Channel 4 signals on the crt is controlled by the variable voltage levels applied to pin 29 (POS3) and pin 30 (POS4) from the front-panel CH 3 and CH 4 POSITION potentiometers.

Dc offsets in the output signal due to any tracking differences between the +5-V and the –5-V supply to U300 are reduced by the tracking regulator circuit composed of U165A, Q190, and associated components. Operational amplifier U165A and Q190 is configured so that the output of voltage at the emitter of Q190 follows the –5-V supply applied to R198. This tracking arrangement ensures that the supply voltages are of equal magnitudes to minimize dc offsets in the output signals.

Scale Illumination

The Scale Illumination circuit consists of U130C, U130D, U130E, U130F, and associated components. The circuit enables the operator to adjust the illumination level of the graticule marks on the crt face plate using the SCALE ILLUM control.

Components U130C through U130F, depicted on diagram 4 as inverters, are actually Darlington transistor pairs. Figure 3-5 is a simplified illustration of the Scale Illumination circuitry, redrawn to show U130C through F as Darlington transistor pairs for the purpose of the following description.

Darlington transistors U130D and U130E control the current flow to scale-illumination lamps DS100, DS101, and DS102. Base drive current for U130D and U130E via R133 is set by the front-panel SCALE ILLUM pot R134. Voltage at the more negative end of the pot is set by the self-biasing configuration of U130F and R135. The voltage level established by these two components is two diode drops above ground (≈ 1.2 V) so that, at full counter-clockwise rotation, the wiper voltage of the SCALE ILLUM pot will just match the turn-off point of U130D and U130E. The voltage at the other end of the pot is set by the collectors of U130D and U130E. As the SCALE ILLUM pot is advanced, the base drive to U130D and U130E increases, and the voltage on their collectors moves closer to ground potential. This increases the current through the scale-illumination lamps to make them brighter and produces some negative feedback to the base circuit through the SCALE ILLUM pot. Negative feedback stabilizes the base drive to U130D and U130E to hold the illumination level constant at the selected setting of the SCALE ILLUM control.

During SGL SEQ display mode, the graticule is illuminated only once during the sequence for photographic purposes. In this mode, a HI is initially written to Auxiliary Control Register U150 (bit Q_H). This turns on U130C and shunts the base drive current of U130D and U130E to ground. At the point in the sequence when the graticule should be illuminated, the processor writes a LO to bit Q_H, and U130C is turned off. This enables U130D and U130E to turn on the lamps to the illumination level set by the SCALE ILLUM pot.

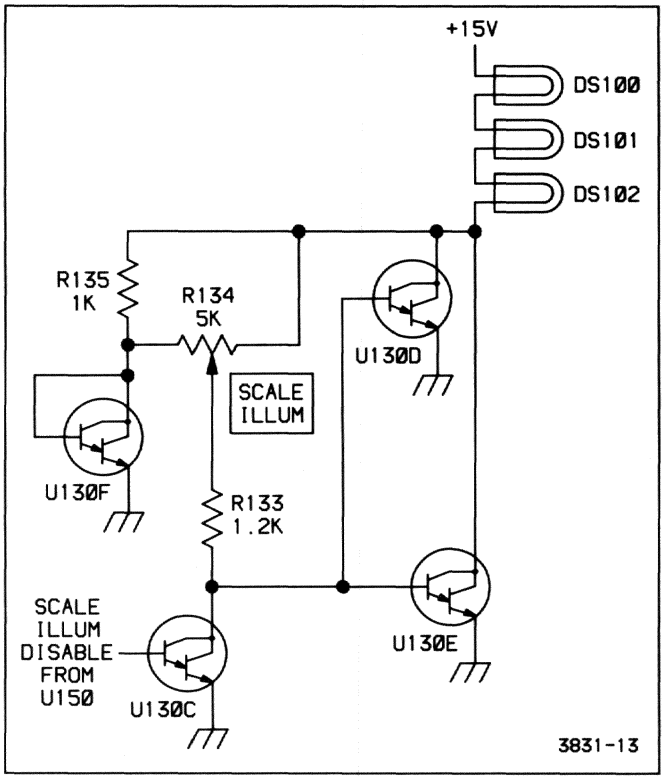


Figure 3-5. Scale Illumination circuit.

DISPLAY SEQUENCER, TRIGGERS, AND SWEEPS

The Display Sequencer circuitry (diagram 5) controls and sequences the "analog-type" oscilloscope functions in real time, dependent on control data it receives from the Microprocessor. The A/B Trigger circuitry, under control of the Display Sequencer, detects when triggering requirements are met and initiates the appropriate sweep. The A Sweep and B Sweep circuits generate sweep ramps under control of the Display Sequencer when triggered by the A/B Trigger circuitry.

Display Sequencer

The Display Sequencer stage consists primarily of integrated circuit U650. This IC accepts analog and digital control signals from various parts of the instrument and, depending on the control data string clocked into its internal control register from the Microprocessor, will change control signals that it sends to other, signal-handling circuits.

Fifty-five bits of serial data from the processor defining the instrument's operating sequence are applied to the Display Sequencer data input, pin 25. The data string is clocked into U650 to the internal control register by the processor-generated control clock applied to pin 24. The data string is organized in several fields, with each field defining the operating mode of one specific instrument function.

Display Sequencer U650 controls the various functions defined by the data fields by setting the levels of the associated control lines. The functions and controlling signal lines for each function are as follows:

Vertical Display Selection

CH 1, CH 2, CH 3, CH 4, ADD, and Readout Y signals are selected by the $\overline{VS1}$, $\overline{VS2}$, $\overline{VS3}$, and $\overline{VS4}$ control signals. See the Vertical Channel Switch description for further information.

Horizontal Display Selection

A Sweep, B Sweep, CH 1 (for X-Y displays) and Readout X are selected by the $\overline{HSA}$ and $\overline{HSB}$ control signals See the Horizontal Output Amplifier description for further information.

Trigger Source Selection

CH 1, CH 2, CH 3, CH 4, ADD, Line, and a sample of the vertical output signal (for calibration purposes only) are selectable as the Trigger SOURCE by the $\overline{SR0A}$, $\overline{SR1A}$, $\overline{SR2A}$, $\overline{SR0B}$, $\overline{SR1B}$, and $\overline{SR2B}$ control lines (pins 28, 27, 29, 32, 31, and 30 respectively). See the A/B Trigger description for further information.

Trigger Holdoff

Sweep recovery time and the circuit initialization time required when front-panel controls are changed are controlled by the THO (trigger holdoff) signal.

Delta Time (Δt) Delay Selection

DLY REF 0 or DLY REF 1 is selected by the DS (delay select) signal.

Trigger and Sweep Activity (Status)

The activity of the Trigger and Sweep circuits, as indicated by the $\overline{SGA}$, $\overline{SGB}$, $\overline{TSA}$, and $\overline{TSB}$ lines, is reported to the Microprocessor via the TSO (trigger status output) line when clocked by the TSS (trigger status strobe) signal.

Intensity Control

The readout intensity, display intensity, and display intensity compensation are controlled by the BRIGHT output level.

Display Blanking

Display blanking for CHOP VERTICAL MODE, Readout transitions, and front-panel control changes is controlled by the BLANK output.

Readout Control

The vertical selection, horizontal selection, and intensity controls are all set to their readout modes either at the end of an A Sweep ($\overline{SGA}$ goes HI) or in response to a readout request ($\overline{ROR}$) from the Readout circuitry (diagram 7). While in the readout mode, the BLANK control signal is driven by the readout blank ($\overline{ROB}$) input signal on pin 5 (also from the Readout circuitry). The readout active line ($\overline{ROA}$, pin 6), when set LO, tells the Readout circuitry that readout dots may be displayed if necessary. The $\overline{ROA}$ signal is always set LO at the start of the trigger holdoff time following sweeps, and it is held there until the holdoff time is almost over. This allows the majority of holdoff time to be used for displaying readout dots. The Display Sequencer will switch the $\overline{ROA}$ signal back to HI before the end of holdoff so that the readout display does not interfere with display of the vertical signal at the triggering event.

Trace Separation

Vertical separation between the A Sweep trace and the B Sweep traces (for alternate horizontal sweep displays), and between the reference B Sweep trace and the delta B Sweep trace (when delta time is selected in B Sweep only mode), is enabled by the TS1 + TS2 output.

X10 Horizontal Magnification

Horizontal X10 magnification is controlled by the $\overline{MAG}$ output.

Calibrator Timing

The 5-Hz to 5-MHz drive signal to the Calibrator circuitry is provided by the CT output.

In the course of developing waveform displays, the Display Sequencer selects one or more vertical channel, sets the trigger source, and selects the horizontal display mode. In most cases, the trigger selection does not change after it has been set unless a front-panel trigger control is changed. An exception is that in VERT TRIGGER MODE, the trigger source tracks the sequencing of the vertical channels (unless AUTO LVL MODE, or CHOP VERTICAL MODE is also selected). Trigger source selection lines are changed only during trigger holdoff time between sweeps.

HOLDOFF RAMP. The holdoff ramp circuit, used to delay the start of a sweep until all circuits have recovered from the previous sweep, is made up of U165C, Q154, Q155, and associated components. Operational Amplifier U165C and capacitor C180 form a sample-and-hold buffer

used to set the charging current for holdoff-ramp integrating capacitor C660. A control voltage from digital-to-analog converter (DAC) U2234 (diagram 2) via multiplexer U170 (diagram 4) is stored on C180. The stored voltage level sets the base voltage for both Q154 and Q155 via amplifier U165C. Transistors Q154 and Q155 form a current-mirror with nearly equal collector currents. Transistor Q154 is a current-to-voltage converter that provides negative feedback to U165C, setting loop gain. Transistor Q155 acts as a constantcurrent source that charges integrating capacitor C660, producing a linear holdoff ramp.

A comparator circuit in U650 detects when the ramp crosses a predefined threshold voltage (approximately +3 V). When the threshold is reached, pin 10 of U650 (HRR) goes LO and the integrating capacitor is discharged. At that same time, an internal counter that keeps track of the holdoff ramp cycles is incremented. The ramps continue to be generated and reset until the holdoff ramp counter has counted the number of ramp cycles defined by the sweep-rate-dependent holdoff data field stored in the Display Sequencer control register. At all sweep speeds except 5 ns per division, the count is at least two holdoff ramp cycles. The front-panel variable HOLDOFF control affects holdoff time by varying the HOLDOFF control voltage to U165C (from the DAC), changing the charging rate of integrating capacitor C660.

When holdoff time requirements are met (determined by the number of ramps counted), the Display Sequencer sets the THO (trigger holdoff) signal LO. This enables both the A Sweep hybrid (U700) and the A Trigger circuitry in U500. The Trigger circuit begins monitoring the selected trigger source line and, when a triggering event is detected that meets the triggering requirements defined by the stored control data, initiates the A Sweep and sets the $\overline{\text{TSA}}$ (trigger status, A Sweep) line to Display Sequencer U650 LO (indicating that the A Sweep has been triggered).

As the A Sweep circuit (U700) responds to the trigger, it sets the $\overline{\text{SGA}}$ (sweep gate A) line LO (via U980A) indicating that an A Sweep is in progress. After the sweep has run to completion, U700 sets the $\overline{\text{SGA}}$ line HI signaling the end of sweep. The Display Sequencer then sets the THO line HI, resetting the A/B Trigger hybrid U500 and A Sweep hybrid U700 in preparation for the next sweep.

DELAY GATE OPERATION. Analog Switches U850B and U850C select the delay references for each sweep. Depending on the display mode and point in the display sequence, the $\overline{\text{DS}}$ control signal (U650 pin 40) routes one of the two analog delay references through U850B and U850C to the two sweep hybrids. The selected reference level is compared against the changing sweep ramp voltages to generate the delay gates that control each sweep's functions.

After an A Sweep has been initiated by a trigger, a delay gate circuit within U700 compares the A Sweep ramp voltage to the selected delay reference. When the sweep ramp reaches the delay reference level, the $\overline{\text{DG}}$ (delay gate) output goes LO, enabling the B trigger portion of U500 and B Sweep hybrid U900. Then, when B triggering occurs (for TRIG AFT DLY mode), the A/B Trigger hybrid sets the $\overline{\text{TGB}}$ (trigger gate B) signal LO, initiating the B Sweep. In RUN AFT DLY mode, however, the $\overline{\text{TGB}}$ signal to U900 is held LO, and the B Sweep is initiated at the end of the A Sweep delay time when the A Sweep delay gate goes LO.

STATUS MONITORING. As the Display Sequencer controls the display system in real time, it continually monitors the trigger and sweep operations and updates the internal trigger status register accordingly. The Microprocessor checks the contents of this register every 3.3 ms to determine the current status of the trigger and sweep circuitry. The Microprocessor reads the trigger status register by generating a series of trigger status strobe (TSS) pulses (U650 pin 19) to serially clock the contents of the register out to the TSO (trigger status output) line and onto the Data Bus (via Status Buffer U2108 on diagram 2). The system status information obtained by this check is used for AUTO LVL triggering, AUTO free-run triggering, detecting the completion of all the sweeps in a SGL SEQ display, and during instrument calibration.

INTENSITY CONTROL. The Display Sequencer controls the intensity for both sweep and readout displays. The analog levels at pins 22 and 23 (set by the front-panel INTENSITY and READOUT INTENSITY controls) determine the basic intensity level of the displays. Two internally generated DAC currents (developed by multiplying the IREF current at pin 20 by two processor-generated numbers stored internally) are added to the basic intensity level currents to produce the display intensity seen on the crt (see Table 3-1). The two DAC currents added to the INTENSITY current are dependent on sweep speed, number of channels being displayed, and whether or not the X10 MAG feature is in use. These added currents increase crt beam current and hold the display intensity somewhat constant under the varying display conditions. The resulting current is applied to Z-Axis Amplifier U950 (diagram 6) from the BRIGHT output of the Display Sequencer (pin 21).

To produce the intensified zone on the A Sweep trace for A intensified by B Sweep displays, an additional current is added to the crt drive signal by the Z-Axis Amplifier during the concurrence of the $\overline{\text{SGAZ}}$ and $\overline{\text{SGBZ}}$ (sweep gate A and B z-axis) signals.

Table 3-1

Intensity Control

Type of Display	Horizontal Selects		Resulting Current at BRIGHT Output
	$\overline{HSA}$	$\overline{HSB}$	
X/Y	LO	LO	DI (display intensity) only
A Sweep	LO	HI	DI + A Swp DAC current
B Sweep	HI	LO	DI + B Swp DAC current
Readout	HI	HI	ROI (readout intensity) only

The readout intensity (ROI) level, controlled from the front-panel READOUT INTENSITY pot, is conditioned by U350A and associated components. Operational Amplifier U350A, configured as a full-wave rectifier, increases readout intensity when the pot is rotated either direction from center. Resistor R360 sets the minimum readout intensity current that occurs at the midpoint of the READOUT INTENSITY pot rotation.

Readout On-Off Comparator U350B detects to which side of center the READOUT INTENSITY control is set. The Microprocessor reads the output of omparator U350B via Status Buffer U2108 (diagram 2) at regular intervals. Depending on the status received, the processor sets up the Readout circuitry (diagram 7) to display either all of the readout information or just the "delta type" readouts.

Blanking of the crt display during CHOP VERTICAL MODE displays or when switching between dot positions in the readout displays is controlled by the Display Sequencer's BLANK output (pin 3). When the signal is LO, the crt z-axis is turned on to the selected intensity level; when HI, the crt display is blanked.

READOUT CONTROL. Readout displays are controlled by the readout request ($\overline{ROR}$) signal, the readout active ($\overline{ROA}$) signal, and the readout blank ($\overline{ROB}$) signal. During the first part of the holdoff time, up until one or two holdoff ramps before holdoff time ends (dependent on the sweep rate), the Display Sequencer sets the $\overline{ROA}$ signal line LO. While the $\overline{ROA}$ line is LO, the Readout circuitry may display readout character dots if necessary. During readout displays, the horizontal and vertical select signals ($\overline{HSA}$, $\overline{HSB}$, $\overline{VS1}$, $\overline{VS2}$, $\overline{VS3}$, and $\overline{VS4}$) are all set HI. This deselects the waveform-related sweep and deflection signals and gives display control to the Readout circuitry. While readout information or cursors are being displayed, the BLANK output signal (pin 3) is controlled by the readout blank ($\overline{ROB}$) signal from the Readout circuitry, and the readout intensity (ROI) signal (pin 23) controls the BRIGHT output level.

During holdoff, the Display Sequencer always sets the readout active ($\overline{ROA}$) line LO. As previously described, setting the $\overline{ROA}$ signal LO allows the Readout circuitry to display readout dots. In some settings of the SEC/DIV switch, with adequate trigger rates, holdoff time is provided for the Readout circuitry to display all the readout information without causing noticeable display flicker.

In those cases where the holdoff time is insufficient to prevent flicker, a portion of the Readout circuitry will request display control by setting the readout request ($\overline{ROR}$) signal LO. The Display Sequencer recognizes all readout requests immediately and switches the horizontal and vertical select lines to the readout display mode. The Readout circuitry displays one readout dot and then resets the readout request HI to switch back to the display of waveforms. Readout requests occur as required during sweep times to keep the readout display caught up. (See "Readout" description for further information).

TRACE SEPARATION. The TRACE SEP feature is used to position the alternate B Delayed Sweep trace downward from the A Sweep when Alternate Horizontal Display Mode (TURN-ALT) is active. It is also used when either the Δt or $1/\Delta t$ measurement function is used with B Sweep only displays. In the latter case, the TRACE SEP control vertically positions the trace(s) associated with the Δ control.

When the Display Sequencer determines that trace separation should be active, the LO TSIN level at pin 7 is routed to pins 9 and 8, the TS1 and TS2 outputs (connected together). This LO output turns off transistor Q600 (diagram 6), thereby enabling the trace separation voltage from the front-panel TRACE SEP pot to be applied to pin 42 of Vertical Output Amplifier U600. To disable the trace separation function, the Display Sequencer sets the TS1 + TS2 control line HI, turning on Q600 and shunting the trace separation signal to ground.

X10 MAG SELECT. The MAG (sweep magnifier) output (pin 39) drives the magnifier control input (pin 14) of Horizontal Output hybrid U800 and the select input (pin 9) of analog switch U860C (diagram 6). Analog switch U860C routes a magnifier gain-control voltage to the Horizontal Amplifier to set the horizontal gain for the X10 magnified displays.

CH 2 DELAY OFFSET. The $\overline{VS2}$ (vertical select, channel 2) output applied to analog switch U860B at pin 10 routes a calibrated offset voltage from sample-and-hold buffer U165D to both sweep hybrids when the Channel 2 vertical signal is being displayed. The offset voltage is used to eliminate the apparent propagation delay between the Channel 2 and the Channel 1 (or CH 2 and either one of the other channels). A step in the calibration procedure allows use of the front-panel Channel 2 Delay Offset feature to be either enabled or disabled. When enabled, the Channel 2 offset may be adjusted up to ±500 ps (with respect to Channel 1) using the Δ control.

CALIBRATOR TIMING. The Calibrator timing signal (CT) from the Display Sequencer is generated by an internal counter. The counter divides the 5-MHz clock input at pin TC (timing clock) by a value that is a function of sweep speed. The resulting square-wave output signal drives the Calibrator circuit. For ease of sweep rate verification, the Calibrator signal provides a display of five complete cycles on the crt at sweep speeds from 100 ms per division to 0.1 μs per division. Below 100 ms per division, the Calibrator output frequency remains at 5 Hz; and above 0.1 μs per division, the Calibrator frequency remains at 5 MHz.

When chopping between vertical channels, the Display Sequencer adds a 200-ns skew at the end of some sweeps to desynchronize the chop frequency from the sweep speed (to prevent the sweep from locking onto the chop frequency). Due to this, the Calibrator signal has an irregular pulse repetition characteristic between sweeps. This will not be apparent when observing the Calibrator signal on the crt of the 2445 since the skew is synchronized to the sweep, but may be observed when the Calibrator output signal is used with other instrumentation. The skew can be eliminated by setting the 2445 to SGL SEQ Mode (to shut off the sweeps).

A/B Trigger

The A/B Trigger hybrid (U500) and associated circuitry select the triggering signal source for each horizontal sweep as directed by the Display Sequencer. When the proper triggering criteria to initiate a sweep are detected, a triggering gate signal is produced to start the selected sweep.

Control data from the processor defining trigger mode, coupling, and slope parameters for each trigger is clocked into two storage registers internal to U500 by the A TRIG CLK signal on pin 23 ($\overline{CCA}$) and the B TRIG CLK signal on pin 47 ($\overline{CCB}$). The Display Sequencer selects the A trigger source with the $\overline{SR0A}$, $\overline{SR1A}$, and $\overline{SR2A}$ signal lines; the B trigger source is selected using the $\overline{SR0B}$, $\overline{SR1B}$, and $\overline{SR2B}$ signal lines. Table 3-2 illustrates trigger source selection.

Table 3-2

Trigger Source Selection

Select Inputs			Trigger Source
$\overline{SR2A(B)}$	$\overline{SR1A(B)}$	$\overline{SR0A(B)}$	
H	H	L	CH 1
H	L	H	CH 2
H	L	L	ADD
L	H	L	CH 3
L	L	H	CH 4
H	H	H	LINE (or BWLB[a])

[a]During calibration routines from the Diagnostic Monitor.

To initiate the A Sweep, the trigger hybrid compares the selected signal to the analog trigger level input at pin 13, TLA (trigger level A). B trigger signals are compared to the TLG (trigger level B) signal at pin 37 when triggered B Sweeps are required. When the proper trigger signal is detected, U500 outputs a trigger gate ($\overline{TGA}$ or $\overline{TGB}$) to the appropriate sweep circuit to initiate that sweep.

When an A Sweep is initiated, the trigger-status line ($\overline{TSA}$) (trigger status A, U500 pin 20) goes LO to signal the Display sequencer that a trigger has occurred. Until the sweep is completed, the $\overline{TGA}$ signal on pin 18 (or $\overline{TGB}$ signal on pin 42 for B Sweeps) remains LO. After the A Sweep is completed, the A Sweep Gate ($\overline{SGA}$) from A Sweep hybrid U700 (via U980A) will go HI, causing the Display Sequencer to set its THO (trigger holdoff) line (pin 13) HI. This resets the sweep hybrid and the trigger hybrid in preparation for the next trigger event.

The B Trigger Holdoff input (THOB, U500 pin 39) is held HI (keeping the B Trigger reset) until the A Sweep Delay Gate ($\overline{DG}$, U700 pin 41) goes LO (see the following A Sweep description). When $\overline{DG}$ goes LO, the B Trigger portion of U500 is enabled. The B Sweep Trigger functions in a manner similar to that of the A Sweep Trigger just described.

A Sweep

When properly triggered, the A Sweep circuit generates linear sweep ramps of selectable slopes. When amplified, these ramp signals horizontally sweep the crt beam across the face of the crt. The A Sweep circuitry consists of U700,

Q709, Q741, U860A, U910B, U980A, and associated components.

The A Sweep ramp signal is derived by charging one of several selectable capacitors from a programmable constant-current source. Capacitor selection depends on the sweep-rate-dependent control data (CD) on pin 29 that is clocked into A Sweep hybrid U700 by the A SWP CLK on pin 28 ($\overline{CC}$). This sweep-rate data causes some internal logic to select either hybrid-mounted capacitors CT0 or CT1 or capacitor C708 at the CT2 (timing capacitor two) pin. An additional capacitor, C709, may be selected (via Q709) if the control data asserts the TCS (timing capacitor select) signal on pin 9. TCS will be HI for A Sweep speeds slower than 1 ms per division. Capacitor C707 and associated circuitry form a linearity compensation circuit.

The constant current to charge the selected capacitor is derived from the DAC-controlled voltage, A TIM REF (A timing reference), generated on the Control Board. The ITREF input (U700 pin 24) is held at zero volts by an internal programmable current-mirror circuit at that input (see Figure 3-6). The A TIM REF voltage is applied to the current mirror via series resistors R723 and R724 to establish the input reference current (ITREF). The output of this current mirror is related to the input reference current by a multiple "M" that is set by a control data field stored in the internal control register of U700. The derived output current (M x ITREF) is connected to another programmable current-mirror circuit, U910B, external to the hybrid. The output of U910B provides the actual charging current and is a control-data-selected multiple of the M x ITREF current.

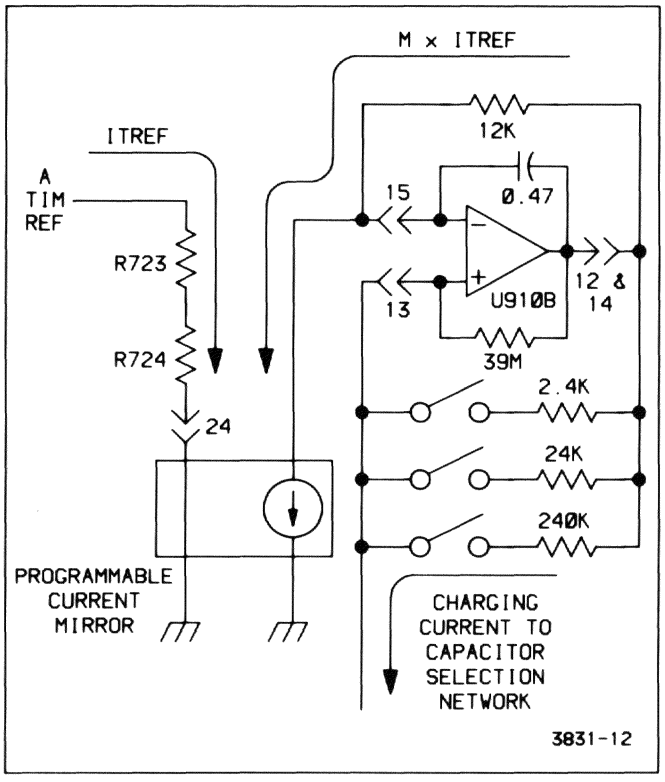


Figure 3-6. Sweep generator.

At the time of calibration, the processor will vary the ITREF input current until the slope of the output ramp for specific current-mirror/timing capacitor combinations is precisely set. The values of A TIM REF at these settings allow the processor to precisely calculate the characteristics of the current-mirror circuits at their various multiplication factors and the charging characteristics of the timing capacitors. These values are stored as calibration constants in nonvolatile memory (EAROM U2008, diagram 2).

Once the calibration constants are set, any setting of the SEC/DIV switch causes the Microprocessor to recall the associated calibration constants from the EAROM. The processor then calculates the proper value of A TIM REF based on the selected timing capacitor and the current-mirror multiplication factors.

If the SEC/DIV VAR control is out of the calibrated detent position, the processor will decrease the A TIM REF voltage from the maximum, in-detent value by an amount proportional to the position setting of the VAR control. At the maximum, fully counterclockwise setting of the VAR control, the ITREF current is one-third that of the normal, in-detent current.

For A Sweep hybrid U700 to initiate a sweep at the selected rate, the $\overline{AUXTRIG}$ (auxiliary trigger) input (pin 3), the THO (trigger holdoff) line from the Display Sequencer (on pin 1), and the $\overline{TRIG}$ (trigger) line from the trigger hybrid (on pin 2) must all be LO. With these three inputs LO, the A SWEEP ramp begins, and the sweep gate ($\overline{SG}$) output (pin 45) goes LO. The buffered sweep gate signal ($\overline{SGA}$) at the output of U980A returns to the Display Sequencer through R981 to indicate that the A Sweep is active. The sweep gate signal is used by various other circuits for their timing activities and is held LO until the A SWEEP ramp ends. The buffered (negative) sweep gate is inverted and routed to the rear-panel A GATE output connector via U975B.

The A Sweep Delay Gate ($\overline{DG}$) signal acts as the trigger holdoff (THO) signal for the B Sweep and the B Trigger circuitry. It is generated by comparing the A SWEEP ramp voltage to the selected delay reference (DR) level from analog switch U850C. As the ramp voltage crosses the delay reference level, the delay gate ($\overline{DG}$) output signal goes LO, removing the HI THO level to the B Sweep. This enables

the B Sweep to run immediately in RUN AFT DLY B Trigger Mode or, when in TRIG AFT DLY B Trigger Mode, enables the B Sweep to run when a triggering event occurs.

The BDCA (A Sweep bypass-delay comparator) input (pin 39) is a data bit from Auxiliary Control Register U140 (diagram 4) that, when HI, sets the A Sweep $\overline{DG}$ output LO at the beginning of the A Sweep. This enables the B Sweep to run immediately at the start of the A Sweep and is used for calibration purposes and for options.

The capacitive load (part of the etched-circuit board) at the RDA (retrace delay adjust) input (pin 4) is used to delay the retrace of the sweep until the Z-Axis drive is fully turned off in response to the $\overline{SGAZ}$ gate going HI. This delay prevents any part of the retrace from being seen.

B Sweep

Operation of B Sweep hybrid U900 is similar to that just described for the A Sweep with the following exceptions: The THO input (and thus sweep enabling) is controlled by the A Sweep hybrid and not the Display Sequencer (see the preceding A Sweep description). The timing capacitor select output, TCS, is not used, and only three timing capacitors are selectable (two on the B Sweep hybrid at CT0 and CT1 and one externally at CT2). Unlike the A Sweep, the delay reference (DR) input (pin 37) and the B Sweep bypass-delay comparator signal (BDCB) input (at pin 39) are used only for factory calibration.

Calibrator

The Calibrator circuit, composed of Q550, U165B, U550A, B, C, and D, and associated components, generates a square-wave output of precise amplitude and frequency characteristics. The CALIBRATOR signal provided at the front-panel output connector is useful for adjusting probe compensation and verifying VOLTS/DIV, SEC/DIV, and Δt (delta time) calibration. Output frequency is controlled by the Display Sequencer and is set to display five cycles across the ten crt graticule divisions at sweep speed settings from 100 ns per division to 100 ms per division. This feature allows quick and easy verification of the sweep rates. The Calibrator circuitry is essentially a voltage regulator that is alternately switched on and off, producing the square-wave output signal.

When the timing signal (CAL) from the Display Sequencer to the base of U550D is LO, U550C (configured as a diode) is forward biased, shunting bias current away from Q550, keeping it turned off. When transistor Q550 is off, the front-panel CAL OUT connector is pulled to ground potential through R558, setting the lower limit of the CALIBRATOR output signal.

As the CAL signal goes from LO to HI, the emitter of U550D is pulled HI to reverse bias U550C. Bias current for Q550 is established, and the transistor is turned on. The voltage at the emitter of Q550 rises to a level of +2.4 volts, determined by the voltage regulator composed of U165B, U550A, U550B, and associated components. This regulated level is applied to the front-panel CALIBRATOR connector through a voltage-divider network composed of R557 and R558. This produces an output voltage of 400 mV with an effective output impedance of 50 Ω.

Since the frequency of the CALIBRATOR signal is controlled by the same divider chain that controls operation of the vertical chopping rate, the intentional 200-ns shift added to the chop signal at the end of some sweeps (to desynchronize the chopping rate from the sweep rate) shows up on the CALIBRATOR signal as an irregular-width pulse. This shift is not apparent when viewing the CALIBRATOR signal on the instrument providing the signal (since the skew occurs during sweep-retrace time), but it should be taken into account when using the 2445 CALIBRATOR signal with other instrumentation. The skew can be eliminated from the signal by setting the 2445 TRIGGER MODE to SGL SEQ (to shut off the sweeps).

VERTICAL CHANNEL SWITCH AND OUTPUT AMPLIFIERS

The Vertical Channel Switch (diagram 6) selects the signal source for vertical deflection of the crt beam. The Vertical, Horizontal, and Z-Axis output amplifiers provide the signal amplification necessary to drive the crt.

Vertical Channel Switch

The Vertical Channel Switch circuitry consists of hybrid Channel Switch U400, that selects one of the vertical signals for application to the Vertical Output Amplifier, and a combined switch/amplifier circuit that converts the single-ended readout vertical signal into a differential signal for application to the Channel Switch.

Channel selection is controlled by the Display Sequencer $\overline{VS1}$ through $\overline{VS4}$ signals applied to the vertical channel selection pins (pin 24, pin 25, pin 13, and pin 14 respectively). (See Table 3-3 for the Vertical Display Selection.) When a vertical select line is LO, the associated input signal pins are connected to the differential output (+OUT, pin 1 and —OUT, pin 3). The CH 5 input signal (Readout Vertical) is added to the output whenever both the $\overline{VS3}$ and $\overline{VS4}$ select signals are HI but will only contain readout information when the readout select logic (U970C and U975A) detects that the Display Sequencer has set both the Horizontal Select signals ($\overline{HSA}$ and $\overline{HSB}$) HI (readout selected).

Table 3-3

Vertical Display Selection

Select Inputs				Vertical Display
$\overline{VS1}$	$\overline{VS2}$	$\overline{VS3}$	$\overline{VS4}$	
L	H	H	H	CH 1
H	L	H	H	CH 2
L	L	H	H	ADD
H	H	L	L	CH 3
H	H	H	L	CH 4
H	H	H	H	Readout (Y)

READOUT SWITCH/AMPLIFIER. Transistors U485A, U485B, U485C, U485D, and U475C, along with their associated components, make up an analog switch circuit that routes either the readout vertical signal at the base of U485A or the ground reference at the base of U485C to the output at the emitter of U475C. The signal selected depends on the complementary voltages applied to the emitter junctions of the two emitter-coupled transistor pairs, U485A and B and U485C and D. The selection voltages are developed by voltage-divider networks on the complementary logic outputs of U975C and U975A.

When readout information is to be displayed, the horizontal select inputs to U980B and U980C go HI and the output of NAND-gate U975C goes LO. The LO applied to the divider network of R498, R484, and R471 pulls the anode of CR484 low enough to reverse bias it. This forward biases the emitter-coupled pair U485A and B via R483. NAND-gate U975A inverts the LO and applies a HI to the junction of R497 and R485. The HI forward biases CR485, and the emitters of U485C and D are pulled to a level in excess of +2 V, reverse biasing the transistor pair. With U485C and D reverse biased, the ground reference level at the base of U485C is isolated from the output, while the readout vertical information is allowed to pass through the forward-biased transistor pair.

When readout information is not being displayed, a HI is present at the output of NAND-gate U975C. The HI forward biases CR484 and, when inverted by U975A, reverse biases CR485. With the biasing conditions reversed, the transistor pair of U485C and D becomes forward biased and U485A and B become reverse biased. The ground reference level present at the base of U485C is coupled to the output, while the readout vertical signal is isolated.

The output signal (either the readout vertical signal or the ground reference level) is applied to the CH5+ input of Channel Switch U400 via R495 and R412. The inverting amplifier circuit composed of U475A, U475B, U475D, and associated components inverts the readout vertical signal for application to the CH5— input. The amplifier is an inverting unity-gain configuration with transistors U475A and U475B connected as an emitter-coupled pair. The base of U475A is referenced to ground through R482. The base of U475B is pulled to the same level by the negative feedback from emitter-follower U475D through R478. The noninverted signal applied is to the base of U475B through R492 and will attempt to increase or decrease the current to the base of U475B, depending on the amplitude and polarity of the signal. However, the negative feedback from the collector of U475B (via U475D and R478) will hold the base of U475B at the ground reference level. The feedback current through R478 develops a voltage drop across R478 that is equal in amplitude but opposite in polarity to the noninverted vertical readout signal. The inverted readout signal is applied to the Channel Switch on pin 2 (CH5—) via R476 and R402.

Resistor R416 (connected to pin 16) sets the high-frequency response of the Channel Switch hybrid.

Delay Line

Vertical deflection signals from the Vertical Channel Switch are delayed approximately 78 ns by Delay Line DL100. This delay allows the Sweep and Z-Axis circuits to turn on before the triggering event begins vertical deflection of the crt beam, thereby permitting the operator to view the triggering event. The pi-filter network, composed of inductors and capacitors built into the circuit board, and adjustments R403 and C404 correct phase-distortion introduced by the delay line and set the overall higher frequency response of the vertical deflection system.

Vertical Output Amplifier

Vertical Output Amplifier U600 is a hybrid device that provides the final amplification of the selected vertical signal, raising it to the level required to drive the crt deflection plates. The vertical signal from the Delay Line is applied to pins 10 and 3 of U600. The RL network connected between pins 8 and 5 (COMPA and COMPB) of U600 compensates the signal for the skin-effect losses associated with the delay line.

Amplifier gain and vertical centering are adjusted by R638 and R639 respectively, primarily to match the amplifier hybrid to the crt installed in the instrument. An intensity-dependent correction current is sinked away from the vertical centering input at pin 39 by the Dynamic Centering circuit. The correction signal holds the vertical

centering stable over a wide range of varying display intensity. Readout jitter adjustment pot R618 is used to minimize thermal distortion in the output amplifier to reduce jitter in the display readout.

The vertical output signal at pins 28 and 33 of U600 (OUT A and OUT B) is applied to the vertical deflection plates of the crt (diagram 8) via L628 and L633. The deflection plates form a distributed-deflection structure that is terminated by a hybrid resistor network. One element of the terminating network is an adjustment potentiometer used to match the network impedance to that of the crt.

BANDWIDTH LIMITING. Bandwidth-limiting coils L644 and L619, along with capacitors built into U600, form a three-pole filter used to roll off high-frequency response of the Vertical Output amplifier above 20 MHz. To limit the vertical bandwidth, the BWL (bandwidth limit) input to U600 (pin 16) is pulled LO. It may be set LO either by the BWL control data bit from Auxiliary Control Register U140 (diagram 4) when the operator selects the Bandwidth Limit feature or automatically by the output of NAND-gate U975A in the Vertical Channel Switch circuitry (via CR616) when the readout is being displayed.

TRACE SEPARATION. The voltage applied to the TS (trace separation) input of U600 (pin 42) is used to offset the output levels of the hybrid to vertically shift the position of trace on the crt. During normal sweep displays, the TS1 + TS2 signal applied to the base of Q600 by the Display Sequencer (diagram 5) is HI, and the transistor is turned on. The TRACE SEP level at the junction of R642 and CR600 is shunted to ground, and no offsetting of the output signal will occur. For those displays in which trace separation should occur, the Display Sequencer switches the base of Q600 to ground level to turn off the transistor. The trace separation level set by front-panel TRACE SEP control R3190 is now applied to the TS input of U600, and a corresponding offset of the displayed trace will occur.

BEAM FIND. As an aid in locating off-screen or over-scanned displays, the 2445 is provided with a beam-finding feature. When the front-panel BEAM FIND button is pushed, the beam-find input pin (BF, pin 15) of U600 will be pulled HI. While BF is HI, the dynamic range of Vertical Output Amplifier U600 is reduced, and all deflected traces will be held to within the vertical limits of the crt graticule.

OUTPUT PROTECTION CIRCUIT. A current-limit circuit composed of transistors Q623 and Q624 protects the Vertical Output Amplifier from a short-circuited output or a bias-loss condition. Either of these fault conditions will cause excessive current to flow into pins 30 and 31 of U600. Current in FET Q624 is limited to the IDSS current, so the voltage at pins 24, 30, and 31 will drop. This decreases the forward bias on pass-transistor Q623 and lowers the voltage at pin 23 of U600 enough and provides some degree of protection for the device.

Horizontal Amplifier

The Horizontal Amplifier circuitry consists of Horizontal Output Amplifier U800, a unity-gain buffer amplifier made up of the five transistors in U735, and associated components.

UNITY-GAIN BUFFER AMPLIFIER. The amplifier circuit composed of U735A, B, C, D, and E along with their associated components, form a unity-gain amplifier that buffers the ramp signal from A Sweep Generator U700 to the Horizontal Output Amplifier. Transistors U735C and D form a differential pair with the negative excursion of their emitters limited to −5 V (clamped by U735E). Negative feedback from the collector of U735C to its base is via emitter-followers U735A and B (in parallel) which drive to the A Sweep input (pin 18, A+) to Horizontal Output Amplifier U800.

HORIZONTAL OUTPUT AMPLIFIER. Integrated circuit U800 provides the final amplification of the selected horizontal-deflection signal required to drive the crt. One of the single-ended input signals applied to the four input pins is converted to a differential-output signal at the output pins of the amplifier. The four deflection signals to U800 are: the A Sweep (pin 18, A+), the B Sweep (pin 16, B+), the Readout Horizontal signal (pin 17, RO), and the Channel 1 signal (used for horizontal deflection of the X-Y displays) at pin 20, the X+ input pin. Signal selection is done by an internal channel switch and is controlled by the $\overline{\text{HSA}}$ (horizontal select A) and $\overline{\text{HSB}}$ (horizontal select B) signals from the Display Sequencer (see Table 3-4).

Table 3-4

Horizontal Display Selection

Control Level		Selected Signal
$\overline{\text{HSA}}$	$\overline{\text{HSB}}$	
H	H	Readout (X)
H	L	B Sweep Ramp
L	H	A Sweep Ramp
L	L	X Input (from CH 1)

Switching between unmagnified (X1) gain and magnified (X10 gain) is also controlled by signals from the Display Sequencer. For normal horizontal deflection, the $\overline{\text{MAG}}$ signal on pin 14 of U800 is HI, and the gain of the output amplifier produces normal sweep deflection. Precise X1 deflection gain is set by adjusting X1 Gain pot R860. When the X10 MAG feature is selected, amplifier gain for the magnified sweeps is increased by a factor of 10. The $\overline{\text{MAG}}$ signal from the Display Sequencer goes LO when magnified sweep is to be displayed. This switches the amplifier gain and switches analog switch U860C from the X1 position to the X10 position. Amplifier gain in the magnified mode is adjusted by adding or subtracting a small bias current using X10 Gain control R850. Dc offsets in the amplifier and crt are compensated for, using Horiz Centering pot R801 to precisely center the display. An intensity-dependent position correction signal, used to hold the horizontal centering stable over a wide range of varying display intensities, is added at this point by the Dynamic Centering circuitry.

As with the Vertical Output Amplifier, the Beam Find feature reduces the dynamic range of the Horizontal Output Amplifier. While the front-panel BEAM FIND button is pressed in, a HI is placed on U800 pin 15 via pull-up resistor R615, and the horizontal deflection is reduced, moving horizontally off-screen displays to within the graticule viewing area.

Timing and linearity of the sweep is set by voltage divider R802-R803.

Z-Axis Amplifier

Z-Axis Amplifier U950 turns the crt beam off and on at the desired intensity levels as the oscilloscope goes through its display sequence. The BRIGHT (brightness) signal applied to U950 pin 44 from the Display Sequencer U650 (diagram 5) is amplified to the level required to drive the crt control grid (via the DC Restorer circuitry) and sets the crt beam intensity. The BLANK input signal applied to U950 pin 5, also from the Display Sequencer, blanks the trace during sweep retrace, chop switching, and readout blanking by reducing the VZOUT signal to a blanked level. Sweep gate z-axis signals ($\overline{\text{SGAZ}}$ and $\overline{\text{SGBZ}}$) from the A Sweep and B Sweep hybrids (U700 and U900 respectively, diagram 5) are applied to the Z-Axis Amplifier on pins 4 and 5. These signals turn the beam current on and off for the related displays and, when used in conjunction with the BLANK signal on pin 5, enable the sweeps to be blanked while still allowing the Readout circuitry to blank and unblank the crt for the readout displays.

Control signals applied to U950 pin 48, pin 2, and pin 1 ($\overline{\text{HSA}}$, $\overline{\text{HSB}}$, and TXY respectively) switch some internal logic circuitry to enable or disable different input signals for the various types of displays. Table 3-5 illustrates the effects of the various input signals on the output signal for different combinations of $\overline{\text{HSA}}$, $\overline{\text{HSB}}$, and TXY.

The Z-Axis hybrid has an internal limiter circuit that prevents the crt from being damaged during high-intensity, high-repetition-rate displays. For high-rep-rate displays, capacitor C956 is shunted to ground via U850A. A signal representative of the intensity setting and the sweep repetition rate is integrated on C957 and results in a control level at pin 7 of U950 used to limit intensity of the crt beam. For the slower repetition rate displays, the SIL bit (slow intensity limit) from Auxiliary Control Register U140 (diagram 4) opens CMOS switch U850A, gently reducing the effective capacitance at pin 7. In this slow-sweep mode, limiting depends primarily on the intensity setting.

Table 3-5

Blanking and Intensity Control Selection

Control Inputs			Intensity Affected By	Blanking Affected By	Typical Display
TXY	$\overline{\text{HSA}}$	$\overline{\text{HSB}}$			
X[a]	H	H	BRIGHT (RO level)	BLANK	Readout
X	H	L	BRIGHT, Z EXT	BLANK, $\overline{\text{SGAZ}}$, $\overline{\text{SGBZ}}$	Delayed Sweep
X	L	H	BRIGHT, $\overline{\text{SGBZ}}$, Z EXT	BLANK, $\overline{\text{SGAZ}}$	Main Sweep
L	L	L	BRIGHT, $\overline{\text{SGBZ}}$, Z EXT	BLANK	X-Y
H	L	L	BRIGHT, $\overline{\text{SGBZ}}$, Z EXT	BLANK, $\overline{\text{SGAZ}}$	X-Y

[a]X = State doesn't matter.

Focus tracking for intensity (VZOUT) level changes is provided by the VQOUT (quadrapole output voltage) signal at pin 22 of U950. The VQOUT signal varies the focusing voltages (and thus the focusing strenth) of two quadrapole lenses in the crt (diagram 8). The VQOUT signal is related to the VZOUT level exponentially and provides the greatest auto-focus control at high-intensity levels. Gain of the VQOUT signal is set by the High-Drive Focus adjustment, R1842. The VQOUT signal also drives the Dynamic Centering circuit and holds the display position stable during wide-range intensity level changes.

Transient response of the Z-Axis Amplifier is adjusted by potentiometer R1834, connected to U950 at pin 13.

Dynamic Centering

The circuit composed of U3401, U3402, and associated components generates compensating signals to offset positioning effects that occur in the crt when the intensity is varied over a wide range. The VQOUT signal from Z-Axis Amplifier U950 is exponentially proportional to the display intensity and dynamically controls the intensity-dependent offsets.

Dynamic Centering adjustment pots R3401 and R3407 set the gain and polarity of the signals at their related outputs by varying the current in the emitter circuit of one of two emitter-coupled pairs of transistors. Adjusting the bias level at pin 4 above $\cong -10.6$ volts (determined by R3410 and R3411 at the complementary input, pin 1) will generate an inverted signal, while adjusting the bias level below −10.6 volts will cause a noninverted signal. Amplitude of the resulting signal is dependent on how far from the −10.6-volt reference the bias is set. The output signal is added or subtracted from the position voltage applied to the Vertical and Horizontal Output Amplifiers. Both pots are adjusted so that position shifts due to display intensity variations are minimized.

READOUT

The Readout circuitry (diagram 7) is responsible for displaying the alphanumeric readout characters on the crt. An eight-bit character code specifying each character (or cursor segment) to be displayed is written from the Microprocessor to a corresponding location in the Character RAM U2920 (a 128-x-8-bit, random-access memory integrated circuit). Each of the lower 64 locations in the RAM corresponds to one of the 64 possible character locations in the crt readout display (see Figure 3-7); 32 locations in the upper graticule row and 32 in the lower graticule row. The upper 64 RAM locations are used to store cursor segment information for the display of the ΔV and Δt measurement cursors. The eight-bit character code written to each location in RAM points to a block of addresses in Character ROM U2930. This block in the ROM contains the dot-position information for the specific character to be displayed at the associated crt position.

Each character is made up of zero (for a space character) or more dots displayed in an eight-wide by sixteen-high dot matrix. Specific blocks of ROM addresses contain all the X-Y offset coordinates for the dots in a particular character in the readout. The coordinates are referenced to the lower-left corner of the character dot matrix. Each individual data byte in the block of ROM addresses contains both the X and the Y coordinates for one dot of the associated character.

To display a character, a combination of the character position on the crt (the RAM address) and the byte of X-Y position data from Character ROM U2930 (relative to that character position) is appled to Horizontal and Vertical DAC (digital-to-analog converters) circuits, U2910 and U2905 respectively. In these circuits, the X-Y position data is converted to analog deflection signals used to position each dot in the crt readout display. Each of the position bytes are read from the block of ROM defining the character under control of the readout timing and sequencing circuitry. The resulting dots, when displayed in sequence, form the character at the proper location on the crt.

Readout I/O

The Readout I/O circuitry, composed of U2860, U2865, U2960, and associated components, provides the interface between the Microprocessor and the Readout board. Two types of data, Readout mode data and character data, are written to the Readout board serially via data bus line BD0.

STORING A CHARACTER. Displaying a character starts with serially clocking 15 of the 16 character data bits into a 16-bit shift register formed by registers U2960 and U2860. The $\overline{\text{ROS1}}$ strobe (readout strobe one) from the Address Decode circuitry (diagram 1) is the clocking signal. The first eight bits of the loaded data indicate the character to be displayed, while the last seven bits select the location on the crt that the character is to be displayed.

On positive-going transitions of the $\overline{\text{ROS1}}$ strobe, the data bit present on the BD0 data line is shifted into the first latch of character address register U2960. The following negative-going edges of the $\overline{\text{ROS1}}$ strobe are inverted by U2965A to produce a positive transition that shifts the data bit present at U2960 pin 9 (Q_{SH}) into U2860. After 15 $\overline{\text{ROS1}}$ strobes have occurred, seven bits of character data are latched into U2860, and the eighth character bit and seven of the character address bits are latched into

character address register U2960 (though they have not been shifted into their correct positions for addressing the RAM).

At this point, the last character bit remains to be shifted into the registers, but the operating mode must be set up first to ensure correct operation upon shifting the final bit. The eight bits of mode data are shifted into the mode control register U2865 by the $\overline{ROS2}$ strobe. Bit Q_4 ($\overline{WRITE}$), along with the $\overline{ROS2}$ and the R/$\overline{W}$ Dlyd signal are applied to the RAM enabling circuitry and determine when new character information will be written into the Character RAM. With U2865 loaded with the mode data, a final $\overline{ROS1}$ strobe clocks the eighth bit of character data from U2960 to U2860 on the negative edge, and the positive edge of the strobe clocks the eighth character address bit (an unused bit) into U2960.

With control bit Q_4 from U2865 LO, the outputs of U2860 are enabled and the eight bits of character data (CD0 through CD7) are written in parallel into the Character RAM at the location selected by the seven-bit address from U2960. Register U2960 is enabled only when the Readout is not displaying characters (the REST signal at pin 15 of U2960 is HI).

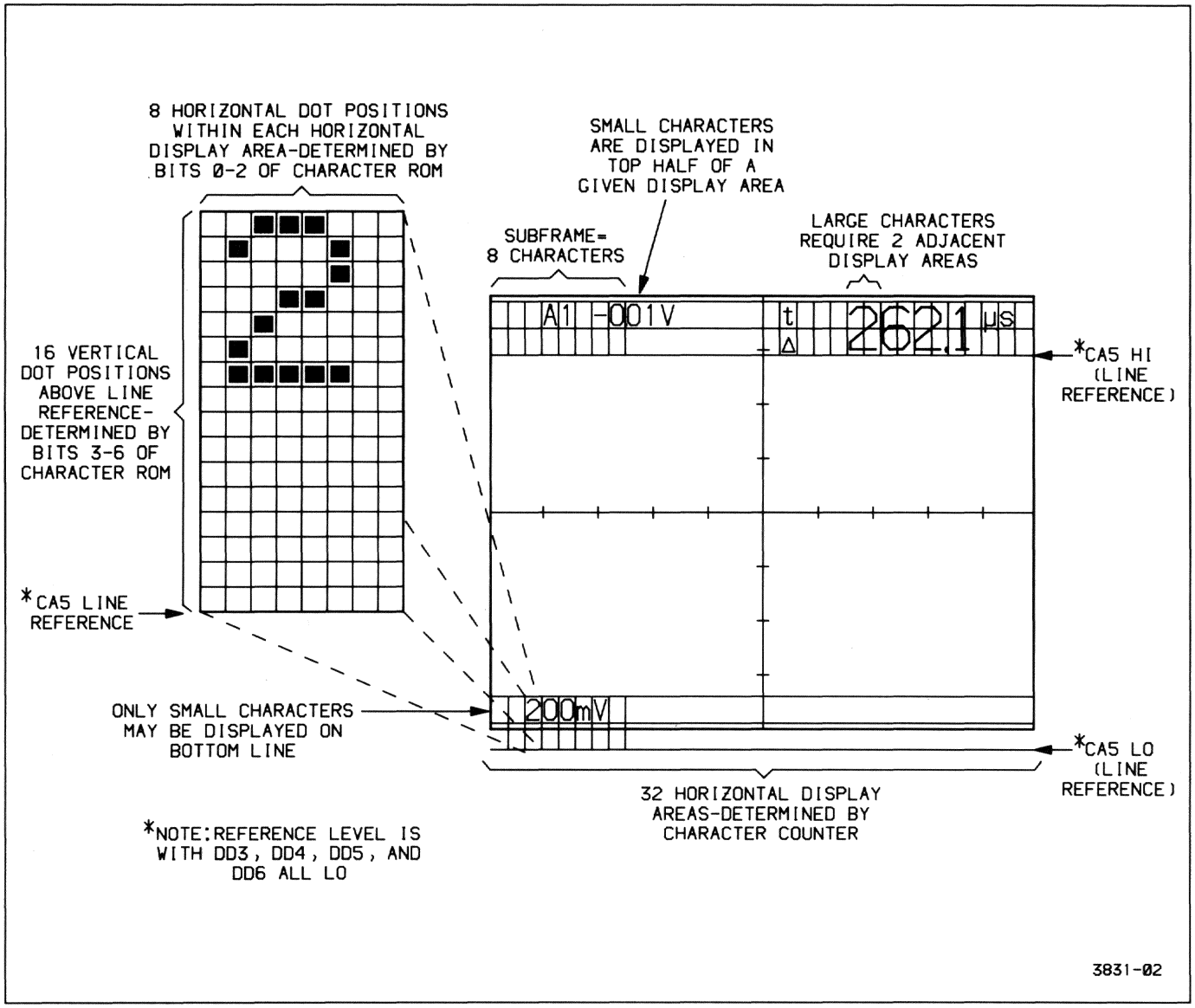


Figure 3-7. Developing the readout display.

The character data register U2860 also provides a means for the Microprocessor to read data from the Character RAM for partial verification of Readout circuit operation (during the power-up tests). The eight bits of parallel data from the Character RAM location selected by character address register U2960 are loaded into U2860 by setting bit Q_3 of mode control register U2865 LO. Inverter U2965C converts the LO to a HI and applies it to character register U2860 at pin 1. The HI on pin 1, in combination with the fixed HI on pin 19 of U2860, switches the character register to the Load mode. The next positive transition of the $\overline{ROS1}$ strobe loads the eight data bits placed on the CD0 through CD7 bus lines into the register in parallel. Bit Q_3 is then returned HI, and the next positive transition of the $\overline{ROS1}$ strobe shifts the Q_A bit to pin 8 (Q_A'), the RO DO (readout data out) line. Seven more $\overline{ROS1}$ strobes shift the remaining seven bits of character data out onto the RO DO line to Status Buffer U2108 (diagram 2) to be read, one at a time, by the processor.

Character RAM

Character RAM U2920 provides temporary storage of the readout character selection data. This character data is organized as 128 eight-bit words that define the character that should be displayed at any given readout position on the crt. Cursor information is also stored in U2920 when cursors are to be displayed.

RAM locations may be addressed either from the Readout I/O stage by character address register U2960, as previously described, or by the Character Counter stage. The lower 64 address locations in RAM each correspond to a specific readout location on the crt, while the upper 64 address locations store cursor information. The eight bits of data written to one of these locations from the Readout I/O stage is a code that identifies the specific character (or cursor segment) that should be displayed at the associated crt location. After the display data is written into the RAM, the Character Counter is allowed to address the RAM, incrementing through the RAM address field. The eight-bit character codes for each display location are output to Character ROM U2930 in sequence.

Character Counter

The Character Counter stage consists of two four-bit counters (U2940A and B) cascaded together to form an eight-bit counter (only seven of which are used) and tri-state buffer U2935 which drives the RAM address lines.

As the Character Counter addresses each RAM location, a sequence of "dot display cycles" is performed in which the individual dots that make up the character are positioned on the crt and turned on. The $\overline{EOCH}$ (end of character) signal applied to U2885A prevents the counter from incrementing until all dots of the character have been displayed. As the last dot of a character is addressed, the $\overline{EOCH}$ bit at pin 2 of U2855A goes LO. The next $\overline{GETDOT}$ pulse increments U2940B, and the next RAM location is addressed to start the display of the next character. Space characters have the $\overline{EOCH}$ bit set LO for the first "dot" of the character and merely advance the Counter to the next character address without displaying any dots. See the Character ROM description for further explanation of the $\overline{EOCH}$ bit.

Character ROM

Character ROM U2930 contains the horizontal and vertical dot-position information for all of the possible characters (or cursor segments) that may be displayed. The eight bits of character data from the Character RAM are applied to the eight most-significant address inputs (A4 through A11) of the Character ROM and select a block of dot-positioning data unique to the character to be displayed. The Dot Counter increments the four least-significant address lines (A0 through A3), causing the ROM to output a sequence of eight-bit words, each defining dot position for the selected character.

The three least-significant bits of a ROM dot-data word (DD0 through DD2) select one of eight horizontal positions for the dot within an eight-by-sixteen character matrix (see Figure 3-7). The next four bits (DD3 through DD6) define the vertical position of the dot within the matrix. These dot-data bits are applied to the Horizontal and Vertical Character DACs, where they are converted to the analog voltages used to position the dot on the crt.

The last dot-data bit DD7 is the $\overline{EOCH}$ (end of character) bit and, when LO, indicates that the last dot of the character is addressed. It is used to reset the Dot Counter (via U2855B) and enables the Character Counter to be incremented (via U2855A) after the last dot of a character has been displayed.

Two servicing jumpers, J401 and J402, have been provided to disable the Character ROM and force the DD7 bit ($\overline{EOCH}$) LO. In certain instances, these two conditions may be useful when troubleshooting the Readout circuitry. To prevent damage to the ROM output circuitry, J402 should only be installed after J401 is installed (to disable the ROM).

Dot Counter

The Dot Counter consists of two four-bit counters (U2870A and B), OR-gate U2835A, inverter U2980D, and inverting input AND-gate U2855B. It sequences through a block of addresses containing dot-position data for a selected character. The Dot Counter is incremented when a dot is finished (via Inverter U2980D) by the $\overline{GETDOT}$ signal from the Dot Cycle Generator.

The counter increments through the block of dot-position data until the last byte of the block is encountered (last dot). This last data byte has the $\overline{\text{EOCH}}$ (end of character) bit (DD7) set LO. The dot is positioned and displayed in the normal manner, but when the $\overline{\text{GETDOT}}$ signal occurs for the next dot display cycle, the $\overline{\text{EOCH}}$ bit is latched into U2905 and generates the $\overline{\text{EOCH1}}$ (end of character, delayed one dot) signal at U2905 pin 19. With $\overline{\text{EOCH}}$ and $\overline{\text{EOCH1}}$ both LO, the HI reset pulse produced at pin 4 of NOR-gate U2855B resets the counter and, except for space characters, the $\overline{\text{EOCH}}$ bit returns HI. As the reset is removed from the Dot Counter, it is reenabled for display of the next character. For space characters, the $\overline{\text{EOCH}}$ bit will be detected as a LO when the first dot is read from the Character ROM, and the Character Counter will advance to the next character on the next rising edge of $\overline{\text{GETDOT}}$.

Counter U2870A and OR-gate U2835A enable characters of more than 16 dots to be displayed. Since most of the readout characters are small, using 16 dots or less, efficient data storage is achieved by storing the dot-position data as 16 consecutive bytes. For displaying these smaller characters, the four bits from U2870B are sufficient to address the 16 possible dot-position bytes.

When larger characters (up to 32 dots) are to be displayed, an additional bit of counter data must be used to address the ROM. This fifth bit comes from U2870A pin 3 and is ORed by U2835A with bit CD0 from the Character RAM. The block address for these larger characters always has bit CD0 set LO, so the counter bit from U2870A pin 3 is in control of the ROM address line at pin 4 of U2930. When displaying these larger characters, the dot count goes beyond 16 dots before the $\overline{\text{EOCH}}$ bit is set LO. On the seventeenth character, the fifth counter bit (pin 3 of U2870A) will go HI to address the next 16-byte block of character data in ROM U2930. The lower four bits of the Dot Counter then sequence through this additional block in the normal manner until the $\overline{\text{EOCH}}$ bit is encountered, resetting the counter.

Horizontal DAC

The Horizontal DAC generates the voltages used to horizontally position dots of the readout display on the crt. Five data bits (CA0 through CA4) from the Character Counter stage position a character to the correct column in the display (32 possible columns across the crt), while three data bits from Character ROM U2930 (DD0 through DD2) horizontally position the dots within the eight-by-sixteen character matrix (see Figure 3-7).

The eight bits of position data are written to the permanently enabled DAC each time a new dot is requested by the Dot Cycle Generator. The $\overline{\text{GETDOT}}$ signal applied to pin 11 (Chip Select) enables the DAC to be written into, and the falling edge of the 5-MHz clock applied to pin 12 (Write) writes the data at the eight DAC input pins into an internal latch. The voltage at the DAC output pin changes to reflect the data present in the latch.

Vertical Character DAC

The function of Vertical Character DAC U2905 is similar to that of the Horizontal DAC just described. It is responsible for vertically positioning each character dot on the crt. The Vertical DAC circuit is made up of five, D-type flip-flops (contained within U2905) and an accompanying resistor weighting network. The outputs of the flip-flop source different amounts of current to a summing node through a resistor weighting network.

The five data bits are latched into U2905 on the rising edge of the $\overline{\text{GETDOT}}$ signal. One bit of character address data (CA5) from the Character Counter switches the vertical display position between the upper and lower readout display lines. When the display is to be in the bottom line, bit CA5 is set LO. With CA5 LO, zener diode VR2925 is biased off and a small current is sourced to the summing node via R2925. Vertical position above this reference is determined by dot data bits DD3 through DD6. When the top line is to be displayed, the CA5 bit is set HI, biasing VR2925 on. A larger current is now sourced into the summing node via R2925 and enough voltage is developed across R2926 to move the display to the top row of the crt. As before, the individual dots are then positioned above this reference level by dot data bits DD3 through DD6.

Mode Select Logic

The Mode Select Logic circuitry is composed of analog switches U2800 and U2805, buffers U2820A and B, gates U2810A, B, C, and D, U2900B and C, and part of U2905. It controls the readout display mode by selecting which deflection signals should drive the Horizontal and Vertical Deflection Amplifiers during a readout display. Five display modes are decoded by the Mode Select Logic: character display, vertical cursor 0, vertical cursor 1, horizontal cursor 0, and horizontal cursor 1.

For normal character displays, cursor select bit CA6 on U2800 pin 1 is LO. This LO signal passes through analog switch U2800 and is latched into U2905 when the $\overline{\text{GETDOT}}$ request from the Dot Cycle Generator goes HI. This latched LO selects the character display mode by forcing the outputs of U2900B and C and U2810A and

B HI. The HI outputs of U2900B and C applied to the select input pins of analog switch U2805 cause the Horizontal DAC output signal applied to U2805 pin 11 to be routed to the Horizontal Amplifier (diagram 6) via buffer U2820B. The same HI logic levels cause NOR-gates U2810C and D to produce a LO at their outputs. This causes analog switch U2800 to route the Vertical DAC output signal applied to pin 12 to the Vertical Output Amplifier (also diagram 6) via buffer U2820A.

For cursor displays, cursor select bit CA6 goes HI. This HI is routed through analog switch U2800 and latched into U2905 when $\overline{\text{GETDOT}}$ next goes HI. This produces a HI at U2905 pin 5, enabling the Mode Select Logic to decode output bits DD3, DD4, and DD5 (from U2905) to determine which of the four possible cursor modes is selected (see Table 3-6). Once one of the cursor modes is entered, analog switch U2800 routes a fixed HI from pin 5, pin 2, or pin 4 to U2905 to keep the Mode Select Logic enabled. Character display mode is reentered only when return-to-character-mode data is decoded (DD4 and DD5 both LO). When that occurs, U2800 routes the CA6 bit to U2905 and, if the bit is LO, the cursor display mode is halted.

CURSOR DEVELOPMENT. Cursors are displayed in short sections, alternating between both vertical positions (for the delta voltage cursors) or both horizontal positions (for the delta time cursors). When displaying delta voltage cursors, the DLY REF 0 level is routed to the Vertical Amplifier by analog switch U2800. This level determines the vertical position of one of the voltage cursors. Horizontal-positioning voltages for one segment of the cursor are routed from Horizontal DAC through analog switch U2805 and buffer U2820B to horizontally position each of the dots making up the cursor segment. DLY REF 1 is then used to vertically position the second cursor, and the Horizontal DAC positions each of the dots for that cursor segment. The cycle is repeated until all segments of both cursors are displayed.

Delta time cursor displays are similar in that the DLY REF 0 and DLY REF 1 signals are used to position the cursors. In this case, however, analog switch U2805 selects the DLY REF 0 and DLY REF 1 signals alternately to position the cursors horizontally, and the Horizontal DAC output is routed via analog switch U2800 and buffer U2820A to vertically position the dots within each cursor segment.

Refresh Prioritizer

The Refresh Prioritizer circuitry consists of U2850A and B, U2950A, U2990A, and U2985. It keeps track of how well the Readout circuitry is doing in displaying all the required readout information and maintains the overall refresh rate. Since the readout display must remain flicker-free and at a constant intensity over the entire sweep rate range, various modes of displaying readout information are provided. The Refresh Prioritizer keeps track of the display status and enables the various readout-display modes as required to produce minimal interference with the displayed waveform trace(s).

Table 3-6

Readout Display Mode Selection

Control Bits						
CA6 (Cursor Select)	DD5	DD4	DD3	Mode Selected	Horizontal Signal	Vertical Signal
L	X[a]	X	X	Character Display	Horiz DAC	Vert DAC
H	L	H	L	Vert Cursor 1	Horiz DAC	DLY REF 1
H	L	H	H	Horiz Cursor 1	DLY REF 1	Horiz DAC
H	H	L	L	Vert Cursor 0	Horiz DAC	DLY REF 0
H	H	L	H	Horiz Cursor 0	DLY REF 0	Horiz DAC
H	L	L	X	Return to Character Display Mode		

[a] X = State doesn't matter.

Ideally, readout information should be displayed only when the oscilloscope is not trying to display waveform traces. These times occur before a trace commences, after a trace is completed, or between consecutive traces. Displaying in this mode corresponds to "priority one" in Figure 3-8 and causes no interference with the displayed waveforms. If the Readout circuitry is able to display all the required readout dots during the holdoff time between sweeps, the prioritizer U2985 will turn off the Dot Start Governor until the next subframe of readout information is to be displayed. When the sweep times are either too fast to finish a readout display during holdoff (at 5 ns per division no identifiable holdoff time exists) or too slow to allow flicker-free readout, readout display modes other than priority one are initiated.

The next most desirable time for dots to be displayed is during "triggerable" time; that time between sweeps when the oscilloscope is waiting for a sweep trigger event to occur. This is designated priority two and may cause slight interference on the leading edge of the displayed trace if a dot is being displayed when the actual trigger occurs.

Finally, the least desirable dot display time is during a waveform trace display. This display time is designated either priority three or priority four. (Priority four indicates a higher demand of display time.) In priorities three and four, dot displays occur during the main portion of the waveform display. However, the waveform blanking associated with these displays is relatively random in nature and is usually not noticeable.

To start a readout display, the ROSFRAME (readout subframe) request from the Timing Logic (diagram 1) clocks the Q output of flip-flop U2850A HI. ROSFRAME is a periodic clocking signal used to hold the overall refresh rate constant and occurs at regular intervals, regardless of the state of the display.

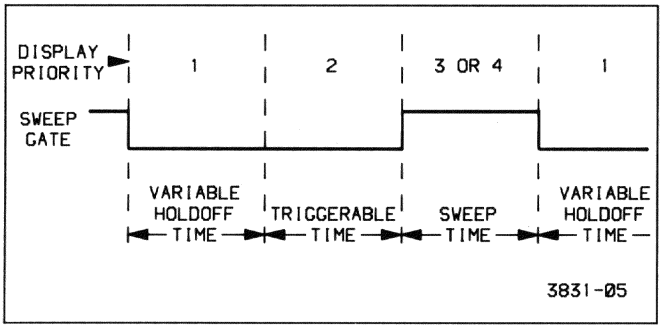


Figure 3-8. Readout display priorities.

As the Dot Cycle Generator runs, it resets U2830B in the Dot Timer at somewhat irregular intervals with the STARTDOT signal (via inverter U2890A). The Dot Timer then starts a timing sequence, and the rising edge of the REFRESH signal from U2830A pin 4 clocks the latched ROSFRAME request from U2850A pin 5 to the Q output (pin 9) of flip-flop U2850B. This HI, applied to the S1 input (pin 10) of prioritizer U2985, sets it up to increment with the next REFRESH clock applied to its clock input (pin 11). The LO $\overline{Q}$ output of U2850B (pin 8) applied to the reset input of U2850A resets the latched ROSFRAME request. See Figure 3-9 for an illustration of the timing sequence involved.

The next REFRESH clock increments the display priority to one by clocking a HI to the Q_D output (pin 12) of prioritizer shift register U2985. (Table 3-7 illustrates the operation of U2985. The same clock latches the now LO ROSFRAME request at U2850B pin 12 to the Q output (pin 9), where it is applied to the S1 input (pin 10) of prioritizer U2985. The LO on the S1 input of the prioritizer will remain until another ROSFRAME request from the Timing Logic occurs, and the encoded priority at the output pins of U2985 will remain as it is presently set.

As each of the consecutive dots of the readout frame are displayed, the Dot and Character Counters increment until all dots of the subframe have been displayed (eight characters). As the Character Counter increments to address the next character of the display (first character of the next frame), the fourth bit of counter U2940B goes HI and sets the S0 input (pin 9) of prioritizer U2985 HI via exclusive-OR-gate U2990A. The Dot Timer then clocks the prioritizer with a REFRESH clock on pin 11 of U2985, and the priority is decremented back to zero (indicating that the subframe is completed). The next ROSFRAME request starts the process over again to display the next subframe of readout display. The sequence just described is the priority one display mode and is used when holdoff time between sweeps allows all dots of the subframe to be displayed before the next ROSFRAME request occurs.

Table 3-7

Operation of Prioritizer Shift Register

Select Inputs		Mode
S0	S1	
H	H	Parallel Load
H	L	L → Q_A (decrease priority)
L	H	H → Q_D (increase priority)
L	L	Hold Data

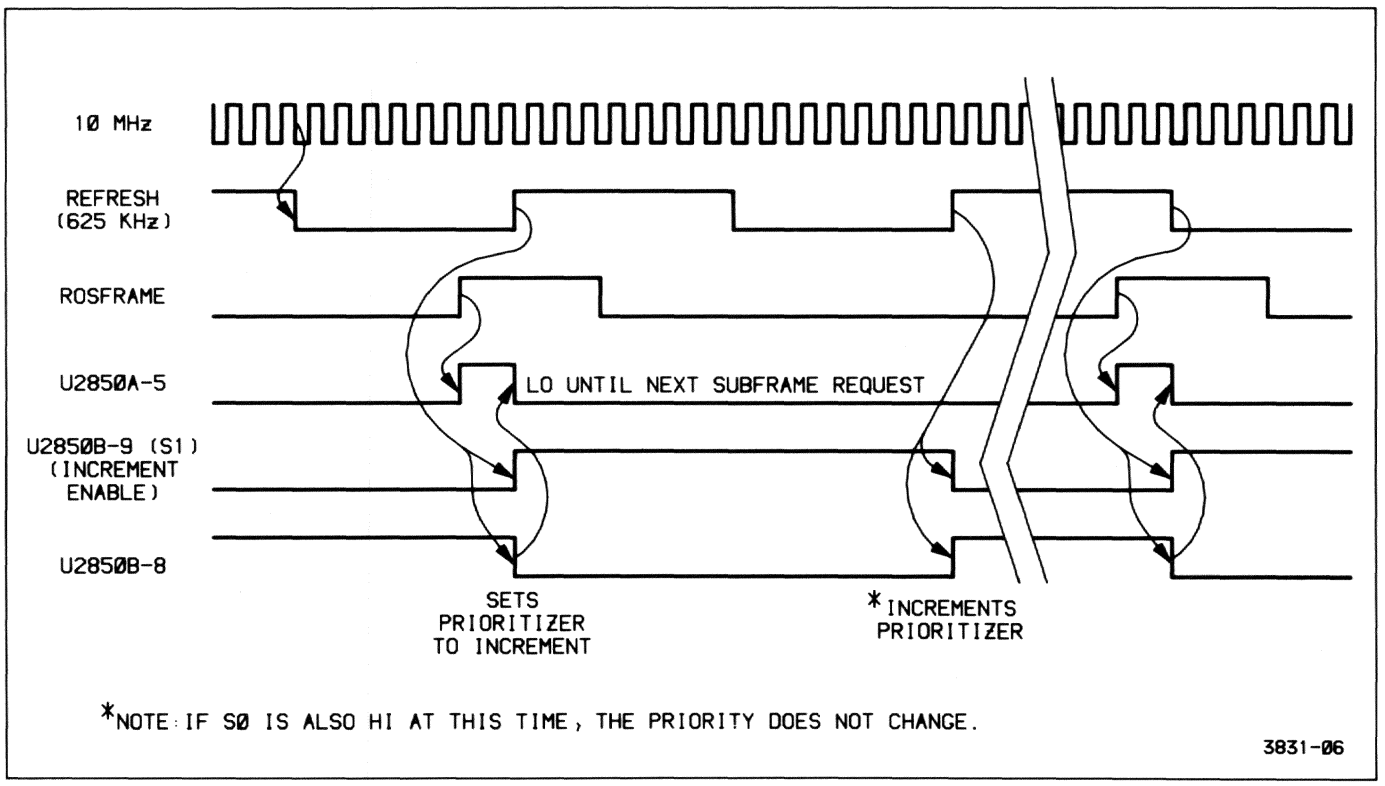


Figure 3-9. Timing of Refresh Prioritizer.

If a second ROSFRAME request occurs before the Character Counter indicates the end of the subframe (to decrement the prioritizer back to zero), input S1 of U2985 will be set HI (while the S0 input pin remains LO) and the Prioritizer will increment to priority two (outputs Q_C and Q_D go HI) on the next STARTDOT cycle. If this display priority still is inadequate to complete the subframe display before the next ROSFRAME request occurs, priority two will be incremented up to priority three, or even to priority four should the condition persist. Priority four is operationally the same as priority three, but it is used to keep the readout circuitry continuously displaying readout data on through the next subframe, thus allowing the display to catch up. If priority four is in effect, the next decrement that occurs at the end of a subframe only returns the prioritizer to priority three, not to priority two.

The circuit composed of flip-flop U2950A and exclusive-OR-gate U2990A enables either edge of the CA3 bit to decrement the priority of the display when a subframe is completed. Either a negative or positive transition on pin 2 of U2990A will cause the output at pin 3 to go HI since the Q output of U2950A is still at the opposite level. The HI from U2990A indicates that the end of the present subframe has occurred, and it sets up the prioritizer to decrement with the next REFRESH clock. At the same time that the prioritizer decrements, the changed level of the CA3 bit is clocked through U2950A and causes the output of exclusive-OR-gate U2990A to return LO until the next subframe is completed.

If the subframe is completed (S0 on U2985 goes HI) when a ROSFRAME request is also pending (S1 is also HI), U2985 does a parallel load, reloading the present priority back into the prioritizer. Since, in this case, the subframe display was completed at the same rate as the ROSFRAME request occurred, the readout display priority is not changed.

Dot Start Governor

The Dot Start Governor detects the display priority from the Refresh Prioritizer and initiates dot-display cycles as the appropriate conditions are met. The conditions tested include display priority, sweep gate completion, dot completion, readout control status, and the readout active enable from the Display Sequencer.

When the readout board status line (ACTIVE/$\overline{\text{ADDRESSABLE}}$) is HI (signifying display) and the REST line goes HI to indicate that the dot cycle is complete, AND-gate U2970C generates a HI at pin 8 (DOTOK) to

signal that a new dot display is allowed. The HI from U2970C enables most of the gating in the Dot Start Governor. If the Refresh Prioritizer has encoded a display priority of either one or two, the output of exclusive-OR-gate U2990B is HI. When DOTOK from U2970C goes HI to enable a dot display, the LO reset from pin 6 of U2970B to pin 1 of flip-flop U2880A is removed. Now, when the A Sweep gate ($\overline{SGA}$) goes HI (beginning of Holdoff), the HI at the D input of U2880A is clocked to the Q output and the $\overline{Q}$ output at pin 6 will go LO, requesting display of a priority one or two dot. This LO dot request is propagated through U2885B, U2890D, U2890B, and U2890C and sets the STARTDOT signal LO. STARTDOT going LO resets Dot Cycle Generator shift register U2995 and counter U2830B of the Dot Timer. Resetting the Dot Cycle Generator shift register causes the REST signal from U2995 pin 13 to go to a LO, removing the HI DOTOK signal at U2970C pin 8. As DOTOK goes LO, STARTDOT at pin 8 of U2890C goes HI to start the Dot Cycle Generator. At the same time the reset to U2880A is asserted via U2970B and the dot request is removed. Both the Dot Timer and the Dot Cycle Generator are now enabled and start the first dot-display cycle during holdoff time.

After the Display Sequencer U650 (diagram 5) has time to respond to the end of the sweep gate, it sets the readout active signal ($\overline{ROA}$) to pin 4 of U2880A LO. This sets pin 5 of U2855B LO, and the signal is propagated through U2855B, U2890D, U2890B, and U2890C, as before, resetting the Dot Timer and the Dot Cycle Generator. REST then goes LO as before and starts the Dot Cycle Generator and Dot Timer. This cycle continues, displaying one dot per cycle (except for the first nondisplayed dot of a character which is automatically initiated by $\overline{EOCH2}$), until the Display Sequencer determines that the readout time is over (sets $\overline{ROA}$ HI) or until the display priority is decremented to zero.

When a display priority of three or four exists, the output of U2990B will be LO, and U2970B, U2880A, and the associated logic gates following it will not be able to initiate a dot cycle. In either of these display priorities, U2970D, U2835C, U2980A, U2965B, and flip-flop U2950B detect the higher priority and generate a readout request signal ($\overline{ROR}$) to the Display Sequencer. The LO from U2950B pin 8 propagates through U2890B and U2890C to initiate a STARTDOT cycle. When the Display Sequencer recognizes that the readout request signal is LO, it will perform the mode-dependent setup functions necessary to give display control to the Readout Board and will then set the $\overline{ROA}$ (readout active) line LO. The LO will be clocked into U2880B, and the Dot Cycle Generator will generate a $\overline{GETDOT}$ signal, resetting the readout request from flip-flop U2950B. Only one dot is displayed for each readout request.

A similar readout display request will be generated when priority-two-or-higher displays are required when sweep gates are not present (dot display during triggerable time after holdoff). This condition is detected by NAND-gate U2885A. AND-gate U2970D allows a readout request to be generated when in the interfere mode. This mode is invoked only during a single-sequence waveform display and ensures that all of the selected sweep combinations are displayed once, followed by a complete readout frame (for the purpose of crt photography).

Dot Cycle Generator

The Dot Cycle Generator, composed of shift register U2995, flip-flop U2880B, and associated gating circuitry, generates time-related signals for the following purposes: unblanking the crt to display a dot; requesting the next byte of dot data in preparation for displaying the next dot; and reenabling itself to repeat the tasks, via the Dot Start Governor (dependent on the display priority).

The timing relationships of the Dot Cycle Generator output signals are controlled by shift register U2995. When the Dot Start Governor initiates a STARTDOT cycle as previously described, the STARTDOT signal initially goes LO, resetting all the Q outputs of U2995 LO and setting the Q output of flip-flop U2880B to a HI. The STARTDOT signal is then returned HI, and Dot Timer counter U2830A and shift register U2995 are enabled. The shift register begins to consecutively shift HI logic levels to its Q output pins with each 5-MHz clock from Dot Timer. After approximately 400 ns, pin 5 (Q_C) of the shift register will go HI. The HI at Q_C propagates through exclusive-OR-gate U2990D and AND-gate U2970A to unblank the crt by setting the readout blanking signal ($\overline{ROB}$) HI.

When the Q_F output of U2995 goes HI (1 μs after STARTDOT), the output of U2990D goes LO and the output of U2990C goes HI. The LO from U2990D propagates through U2970A to blank the crt ($\overline{ROB}$ goes LO) and to clock flip-flop U2880B via inverter U2890C. The $\overline{ROA}$ (readout active) level from the Display Sequencer (diagram 5) is clocked from the D input (pin 12) of U2880B to the Q output; and, if LO (indicating that the readout circuitry had control of the crt when unblanking occurred; thus the dot was displayed), the output of U2980B is set HI. With three HI levels applied to NAND-gate U2885C, a $\overline{GETDOT}$ request is generated to get the next byte of dot-position data for display. The next 5-MHz clock sets the Q_G output of U2995 HI, and the output of U2990C goes LO, removing the LO $\overline{GETDOT}$ signal.

At 1.4 μs after STARTDOT goes HI, U2995 pin 13 (Q_H) goes HI to produce the REST signal, indicating that the current dot cycle is complete and the Dot Cycle Generator is at REST. If the readout ACTIVE/$\overline{\text{ADDRESSABLE}}$ mode bit at U2970C pin 10 is still HI, the REST signal going HI produces a HI DOTOK signal (next dot is allowed) at pin 8. This HI applied to pin 10 of U2890C, along with any of the possible dot requests from the Dot Start Governor, will initiate another STARTDOT cycle for the next dot of the display. As long as the Display Sequencer holds the readout active line ($\overline{\text{ROA}}$) LO, U2885B, U2890D, and U2890B of the Dot Start Governor will automatically initiate dot cycles as soon as the previous one ends (REST goes HI), until the Refresh Prioritizer is decremented to zero.

When the last dot of the character is called from the Character ROM, the $\overline{\text{EOCH}}$ bit (DD7) applied to latch U2905 at pin 8 (in the Mode Select Logic circuitry) is LO. At the end of that dot display cycle, the $\overline{\text{GETDOT}}$ signal clocks the LO $\overline{\text{EOCH}}$ bit into latch U2905. The latched bit becomes the $\overline{\text{EOCH1}}$ signal (end of character, delayed one dot request) and is applied to U2855B, along with the already LO $\overline{\text{EOCH}}$ bit, to reset Dot Counters U2870A and B. The least-significant bits to the Character ROM address pins (A0 through A4) are then zeros, and the first dot of the next character is addressed. The Horizontal and Vertical DACs don't write this first dot position data into their registers until the end of the next $\overline{\text{GETDOT}}$ signal. That same $\overline{\text{GETDOT}}$ signal also clocks $\overline{\text{EOCH1}}$ into U2905 which becomes $\overline{\text{EOCH2}}$ at pin 6 (end of character, delayed by two dot requests). $\overline{\text{EOCH2}}$ is applied to AND-gate U2970A and disables the gate prior to the time the Dot Cycle Generator attempts to unblank the crt for the first dot display; thus the first dot of a character is never displayed.

Disabling the unblanking path for the first dot of each character in the manner just described allows the more radical voltage changes between characters to settle before the actual display of the next character begins. When the dot data for one of these undisplayed dots also has the $\overline{\text{EOCH}}$ bit set LO, it is a space character, and the display is advanced to the next character.

Dot Timer

The Dot Timer, composed of U2890A and U2830A and B, generates three, time-related signals used to synchronize the display and maintain the proper sequencing of the individual character dots.

The two least-significant bits of the Dot Timer, from U2830B pins 11 and 10, are reset at the beginning of a dot cycle by a LO STARTDOT signal applied to the reset input of the counter via U2890A. As the dot-display cycle begins, the STARTDOT signal returns HI and the Dot Timer begins counting in a binary fashion. The 10-MHz clock applied to pin 13 is divided by two to produce the 5-MHz clocking signal at output pin 11. The 5-MHz clock sequences the Dot Cycle Generator through the various phases of the dot-display cycle. The REFRESH output signal from U2830A pin 4 updates the Refresh Prioritizer as each subframe is displayed.

A third clock, from U2830A pin 6, occurs at approximately 8-μs intervals and allows any pending dot requests to generate a $\overline{\text{ROR}}$ signal to the Display Sequencer via flip-flop U2950B. (Readout request generation is described in the Dot Start Governor discussion.)

HIGH VOLTAGE POWER SUPPLY AND CRT

The High Voltage Power Supply and CRT circuit (diagram 8) provides the voltage levels and control circuitry for operation of the cathode-ray tube (crt). The circuitry consists of the High Voltage Oscillator, the High Voltage Regulator, the Cathode Supply, the Anode Multiplier, the DC Restorer, Focus Amplifiers, the CRT, and the various CRT Control circuits.

High Voltage Oscillator

The High Voltage Oscillator transforms power obtained from the −15 V unregulated supply into the various ac levels necessary for the operation of the crt circuitry. The circuit consists primarily of transformer T1970 and switching transistor Q1981 connected in a power oscillator configuration. The low-voltage oscillations set up in the primary winding of T1970 are raised by transformer action to high-voltage levels in the secondary windings. These ac secondary voltages are applied to the DC Restorer, the Cathode Supply, and the Anode Multiplier circuits that provide the necessary crt operating potentials.

Oscillation occurs due to the positive feedback from the primary winding (pin 4 to pin 5) to the smaller base-drive winding (pin 3 to pin 6) that provides base drive to switching transistor Q1981. The frequency of oscillation is approximately 50 kHz and is determined primarily by the resonant frequency of the transformer.

OSCILLATION START-UP. Initially, when power is applied, the High Voltage Regulator circuit detects that the crt cathode voltage is too positive and pulls pin 6 of transformer T1970 negative. The negative level is applied to switching transistor Q1981 through the transformer winding and forward biases it. Current begins to flow in the primary winding through the transistor collector circuit and induces a magnetic field around the transformer primary winding. The increasing magnetic field induces a current in the base-drive winding that further increases the base drive to the transistor. This inphase feedback causes Q1981 to quickly saturate, at which point the current in the primary winding reaches its maximum value. As the rate of change in the primary current peaks and then reverses, the induced magnetic field begins to decay. This decreases the base-drive current and begins to turn Q1981 off.

As Q1981 turns off, the magnetic field around the primary winding continues to collapse, and a voltage of opposite polarity is induced in the base-drive winding. This turns the switching transistor completely off. Once again, as the magnetic field builds and then reverses, the current induced in the base-drive winding changes direction, forward biasing Q1981. At that point, the primary-winding current starts increasing again, and the switching transistor is again driven into saturation by the feedback supplied to the base-drive winding. This sequence of events occurs repetitively as the circuit continues to oscillate.

The oscillating magnetic field couples power from the primary winding into the secondary windings of the transformer. The amplitudes of the voltages induced in the secondary windings are functions of the turns ratios of the transformer windings.

High Voltage Regulator

The High Voltage Regulator consists of U1956A and B and associated components. It monitors the crt Cathode Supply voltage and varies the bias point of the switching transistor in the High Voltage Oscillator to hold the Cathode Supply voltage at the nominal level. Since the output voltages at the other secondary winding taps are related by turns ratios to the Cathode Supply voltage, all voltages are held in regulation.

When the Cathode Supply voltage is at the proper level (−1900 V), the current through R1945 and the 19-MΩ resistor internal to High Voltage Module U1830 holds the voltage developed across C1932 at zero volts. This is the balanced condition and sets base drive in Q1981 via integrator U1956A and voltage-follower U1956B. Varying base drive to Q1981 holds the secondary voltages in regulation.

If the Cathode Supply voltage level tends too positive, a slightly positive voltage will develop across C1932. This voltage causes the outputs of integrator U1956A and voltage-follower U1956B to move negative. The negative shift charges capacitor C1951 to a different level, around which the induced feedback voltage at the base-drive winding will swing. The added negative bias causes Q1981 to turn on earlier in the oscillation cycle, and a stronger current pulse is induced in the secondary windings. The increased power in the secondary windings increases the secondary voltages until the Cathode Supply voltage returns to the balanced condition (zero volts across C1932). Opposite action occurs should the Cathode Supply voltage tend too negative.

Cathode Supply

The Cathode Supply circuit is composed of a voltage doubler and an RC filter network contained within High Voltage Module U1830. This supply produces the −1900-V accelerating potential applied to the CRT cathode and the −900-V slot lens voltage. The −1900-V supply is monitored by the High Voltage Regulator to maintain the regulation of all voltages from the High Voltage Oscillator.

The alternating voltage from pin 10 of transformer T1970 (950 V peak) is applied to a conventional voltage-doubler circuit at pin 7 of the High Voltage Module. On the positive half cycle, the input capacitor of the voltage doubler (0.006 μf) is charged to −950 V through the forward-biased diode connected to ground at pin 9 of the module (charging path is through the diode, so stored charge is negative). The following negative half cycle adds its ac component (−950 V peak) to this stored dc value and produces a total peak voltage of −1900 V across the capacitor. This charges the 0.006-μf storage capacitor (connected across the two doubler diodes) through the second diode (now the forward-biased diode) to −1900 V. Two RC filters follow the voltage doubler to smooth out the ac ripple. A resistive voltage divider across the output of the filter network provides the −900-V slot lens potential.

Anode Multiplier

The Anode Multiplier circuit (also contained in High Voltage Module U1830) uses voltage multiplication to produce the +14-kV CRT anode potential. Circuit operation is similar to that of the voltage-doubler circuit of the Cathode Supply.

The first negative half cycle charges the 0.001-μf input capacitor (connected to pin 8 of the High Voltage Module) to a positive peak value of +2.33 kV. The following positive half cycle adds its positive peak amplitude to the voltage stored on the input capacitor and boosts the charge on the second capacitor of the multiplier (and those following)

to +4.66 kV. Following cycles continue to boost up succeeding capacitors to values 2.33 kV higher than the preceding capacitor until all six capacitors are fully charged. This places the output of the last capacitor in the multiplier at +14 kV above ground potential. Once the multiplier reaches operating potential, succeeding cycles replenish current drawn from the Anode Multiplier by the crt beam. The 1-MΩ resistor in series with the output protects the multiplier by limiting the anode current to a safe value.

Focus Amplifier

The Focus Amplifier, in conjunction with the auto-focus circuitry of Z-Axis hybrid U950 (diagram 6), provides optimum focus of the crt beam for all settings of the front-panel INTENSITY control. The Focus Amplifier itself consists of two shunt-feedback amplifiers composed of Q1851, Q1852, and associated components. The outputs of these amplifiers set the operating points of a horizontally converging quadrapole lens and a vertically converging quadrapole lens within the crt. The convergence strength of each lens is dependent on the electric field set up between the lens elements.

Since the bases of Q1851 and Q1852 are held at constant voltages (set by their emitter potentials), changing the position of the wiper arms of the ASTIG and FOCUS pots changes the amount of current sourced to the base junctions through R1856 and R1857 respectively. This changes the base-drive currents and produces different output levels from the Focus Amplifiers; that, in turn, changes the convergence characteristics of the quadrapole lenses.

Initially, at the time of adjustment, the FOCUS and ASTIG potentiometers are set for optimum focus of the crt beam at low intensity. After that initial adjustment, the ASTIG pot normally remains as set, and the FOCUS control is positioned by the user as required when viewing the displays. When using the FOCUS control, transistor Q1852 is controlled as described above; however, an additional current is also supplied to the base node of Q1851 from the FOCUS pot through R1855. This additional current varies the base-drive current to Q1851 and provides tracking between the two lenses as the FOCUS control is adjusted during use of the instrument.

The convergence strengths of the quadrapole lenses also dynamically track changes in the display intensity. The VQOUT signal, applied to the crt at pins 5 and 6, is exponentially related to the VZOUT (intensity) signal driving the crt control grid and increases the strength of the lenses more at higher crt beam currents. (A higher beam current requires a stronger lens to cause an equal convergence of the beam.)

DC Restorer

The DC Restorer provides crt control-grid bias and couples both the dc and the low-frequency components of the Z-Axis drive signal to the crt control grid. This circuit allows the Z-Axis Amplifier to control the display intensity by coupling the low-voltage Z-Axis drive signal (VZOUT) to the elevated crt control-grid potential (about −1.9 kV).

The DC Restorer circuit (Figure 3-10) operates by impressing the crt grid bias setting and the Z-Axis drive signal on an ac voltage waveform. The shaped ac waveform is then coupled to the crt control grid through a coupling capacitor that restores the dc components of the signal.

GRID BIAS LEVEL. An ac drive voltage of approximately 300 V peak-to-peak is applied to the DC Restorer circuit from pin 7 of transformer T1970. The negative half cycle of the sinusoidal waveform is clipped by CR1953, and the positive half cycle (150 V peak) is applied to the junction of CR1930, CR1951, and R1941 via R1950 and R1953. Transistor Q1980, operational amplifier U1890A, and associated components form a voltage clamp circuit that limits the positive swing of the ac waveform at the junction.

Transistor Q1980 is configured as a shunt-feedback amplifier, with C1991 and R1994 as the feedback elements. The feedback current through R1994 develops a voltage across the resistor that is positive with respect to the +42.6 V on the base of the transistor. The value of this additive voltage plus the two diode drops across CR1950 and CR1951 sets the upper clamping threshold. Grid Bias potentiometer R1878 sinks varying amounts of current away from the base node of the transistor and thus sets the feedback current through R1994. The adjustment range of the pot can set the nominal clamping level between +71 V and +133 V.

When the amplitude of the ac waveform is below the clamping threshold, series diodes CR1950 and CR1951 will be reverse biased and the ac waveform is not clamped. During the time the diodes are reverse biased, transistor Q1980 is kept biased in the active region by the charge retained on C1971 from the previous cycle. As the amplitude of the ac waveform at the junction of CR1930 and CR1950 exceeds the voltage at the collector of Q1980, the two series diodes (CR1950 and CR1951) become forward biased, and the ac waveform is clamped at that level. Any current greater than that required to maintain the clamp voltage will be shunted to the +42-V supply by transistor Q1980.

Operational amplifier U1890A sinks a time-dependent variable current away from the base node of Q1980 that modifies the crt control-grid bias during the first few minutes of instrument operation. The circuit compensates for the changing drive characteristics of the crt as it warms up.

At power-up, capacitor C1990 begins charging through R1991 toward the +15-V supply. The output of U1890A follows the rising voltage on pin 3; and after about ten minutes (for all practical purposes), it reaches +15 V. As the output voltage slowly increases, the charging current through R1992 causes the Grid Bias voltage to gradually lower about ten volts from its power-on level. The charge on C1990 dissipates slowly; therefore, if instrument power is turned off and then immediately back on again, the output of U1890A will still be near the +15-V limit rather than starting at zero volts as when the crt was cold.

Z-AXIS DRIVE LEVEL. The variable-level Z-Axis signal (VZOUT) establishes the lower clamping level of the ac waveform applied to the High Voltage Module. When the amplitude of the waveform drops below the Z-Axis signal level, CR1930 becomes forward biased, and the ac waveform is clamped to the Z-Axis signal level. The VZOUT level may vary between +8 V and +75 V, depending on the setting of the front-panel INTENSITY and READOUT INTENSITY controls.

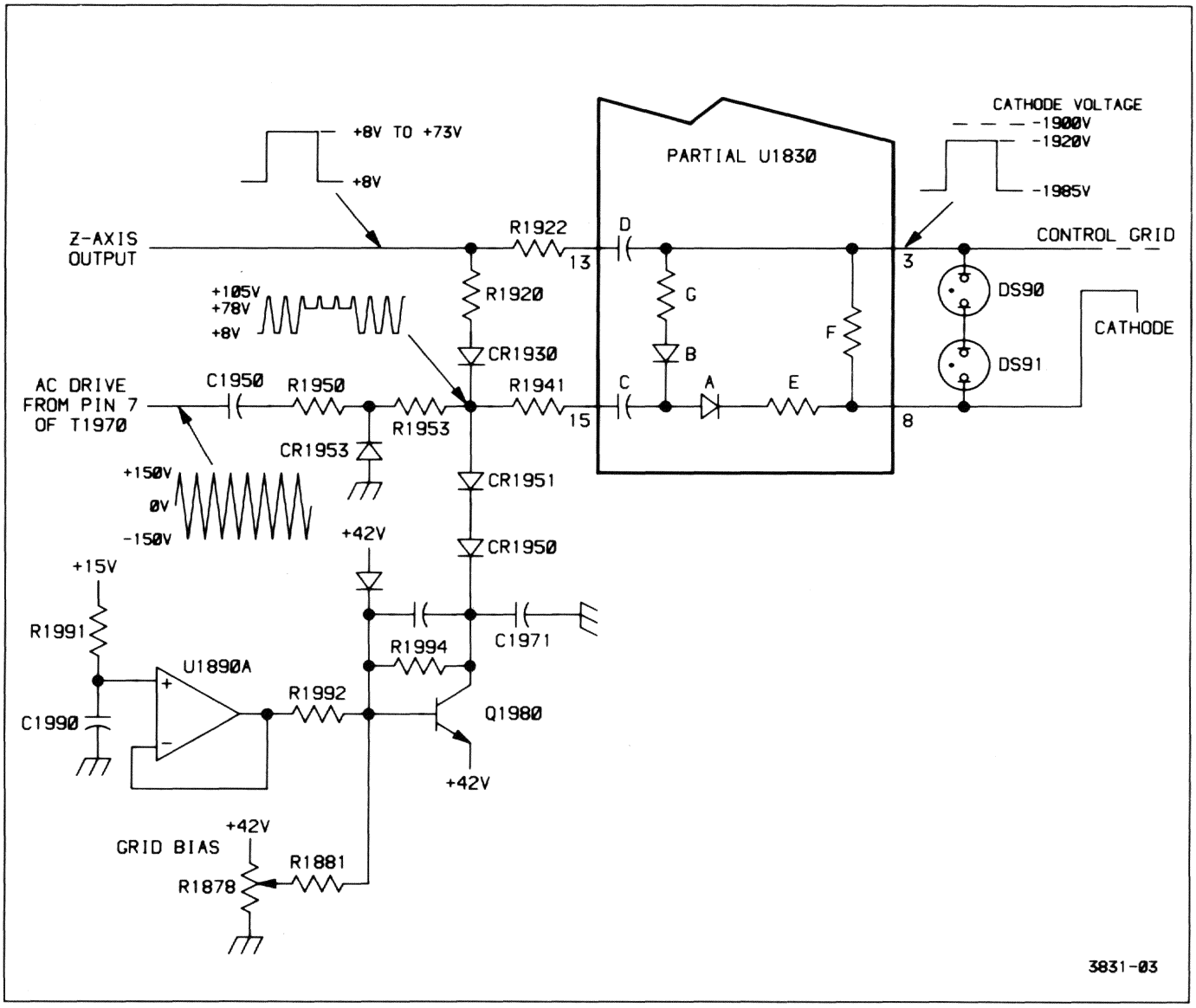


Figure 3-10. Dc Restorer circuit.

The ac waveform, now carrying both the grid-bias information and the Z-Axis drive information, is applied to a DC Restorer circuit in the High Voltage Module where it is raised to the high-voltage levels of the crt control grid.

DC RESTORATION. The DC Restorer circuit in the High Voltage Module is referenced to the crt cathode voltage via a connection within U1830. Capacitor C (in Figure 3-10), connected to pin 15 of U1830, initially charges to a level determined by the difference between the Z-Axis signal level and the crt cathode potential. The Z-Axis signal sets the level on the positive plate of capacitor C through R1920, CR1930, and R1941; the level on the negative plate is set by the crt cathode voltage through resistor E and diode A. Capacitor D is charged to a similar dc level through resistor F and R1922.

When the ac waveform applied to pin 15 begins its transition from the lower clamped level (set by the Z-Axis signal) towards the upper clamped level (set by the Grid Bias potentiometer), the charge on capacitor C increases. The additional charge is proportional to the voltage difference between the two clamped voltage levels.

When the ac waveform begins its transition from the upper clamped level back to the lower clamped level, diode A becomes reverse biased. Diode B becomes forward biased, and an additional charge proportional to the negative excusion of the ac waveform (difference between the upper clamped level and the lower clamped level) is added to capacitor D through diode B and resistor G. The amount of charge added to capacitor D depends on the setting of the front-panel INTENSITY control, as it sets the lower clamping level of the ac waveform. This added charge determines the potential of the control grid with respect to the crt cathode.

The potential difference between the control grid and the cathode controls the beam current and thus the display intensity. With no Z-Axis signal applied (INTENSITY control off), capacitor D will be charged to its maximum negative value, since the difference between the two clamped voltage levels is at its maximum value. This is the minimum intensity condition and reflects the setting of the Grid Bias potentiometer. During calibration, the Grid Bias pot is adjusted so that the difference between the upper clamping level (set by the Grid Bias pot) and the "no signal" level of the Z-Axis drive signal (VZOUT) produces a control grid bias that barely shuts off the crt electron beam.

As the INTENSITY control is advanced, the amplitude of the square-wave Z-Axis signal increases accordingly. This increased signal amplitude decreases the difference between the upper and lower clamped levels of the ac waveform, and less charge is added to capacitor D. The decreased voltage across capacitor D decreases the potential difference between the control grid and the cathode, and more crt beam current is allowed to flow. Increased beam current increases the crt display intensity.

During the periods that capacitor C is charging and discharging, the control-grid voltage is held stable by the long-time-constant discharge path of capacitor D through resistor F. Any charge removed from capacitor D during the positive transitions of the ac waveform will be replaced on the negative transitions.

The fast-rise and fast-fall transitions of the Z-Axis signal are coupled to the crt control grid through capacitor D. This ac-coupled fast-path signal quickly sends the crt electron beam to the new intensity level, then the slower DC Restorer path "cathes up" to handle the dc and low-frequency components of the Z-Axis drive signal.

Neon lamps DS90 and DS91 prevent arcing inside the crt should the control grid potential or cathode potential be lost for any reason.

CRT Control Circuits

The CRT Control circuits provide the various potentials and signal attenuation factors that set up the electrical elements of the crt. The control circuitry is divided into two separate catagories: (1) level setting and (2) signal handling. The level-setting circuitry produces voltages and current levels necessary for the crt to operate, while the signal-handling portion is associated with changing crt signal levels.

LEVEL-SETTING CIRCUITRY. Operational amplifier U1890B, transistor Q1980, and associated components form an edge-focus circuit that sets the voltages on the elements of the third quadrapole lens. The positive lens element is set to its operating potential by Edge Focus adjustment pot R1864 (via R1897). This voltage is also divided by R1893 and R1982 and applied to the non-inverting input of U1890B to control the voltage on the other element of the lens.

The operational amplifier and transistor are configured as a feedback amplifier, with R1891 and R1990 setting the stage gain. Gain of the amplifier is equal to the attenuation factor of divider network R1893 and R1892, so total overall gain of the stage from the wiper of R1864 to the collector of Q1890 is unity. The offset voltage between lens elements is set by the ratio of R1891 and R1990 and the +10-V reference applied to R1990. This configuration causes the two voltages applied to the third quadrapole lens to track each other over the entire range of Edge Focus adjustment pot R1864.

Other adjustable level-setting circuits include Y-Axis Alignment pot R1848, used to rotate the beam alignment after vertical deflection. This adjustment controls the amount of current through the Y-Axis Alignment coil around the neck of the crt and is set to produce precise perpendicular alignment between x- and y-axis deflections. The TRACE ROTATION adjustment R975 is a front-panel screwdriver-adjustable control. The effect of the adjustment is similar to the Y-Axis Alignment pot, but when adjusted, it rotates both the x-axis and the y-axis deflections of the trace on the face of the crt. A final adjustable level-setting control is the Geometry pot R1870, adjusted to optimize display geometry. The potential at pin 8 for the vertical shield internal to the crt is produced by zener diode VR1891 and associated components.

SIGNAL-HANDLING CIRCUITRY. The crt termination adjustment R1301 is set to match the loading characteristics of the crt's vertical deflection structure to the Vertical Output Amplifier.

LOW VOLTAGE POWER SUPPLY

The low voltages required by the 2445 are produced by a high-efficiency, switching power supply. This type of supply directly rectifies and stores charge from the ac line supply; then the stored charge is switched through a special transformer at a high rate, generating the various supply voltages.

Line Rectifier

Ac line voltages of either 115 V or 230 V may provide the primary power for the instrument, depending on the setting of the LINE VOLTAGE SELECTOR switch S90 (located on the instrument rear panel). Power Switch S350 applies the selected line voltage to the power supply rectifier (CR1011).

With the selector switch in the 115-V position, the rectifier and storage capacitors C1021 and C1022 operate as a full-wave voltage doubler. When operating in this configuration, each capacitor is charged on opposite half cycles of the ac input, and the voltages across the two capacitors in series will approximate the peak-to-peak value of the source voltage. For 230-V operation, switch S90 connects the rectifier as a conventional bridge rectifier. Both capacitors charge on both input half cycles, and the voltage across C1021 and C1022 in series will approximate the peak value of the rectified source voltage. For either configuration, the dc voltage supplied to the power supply inverter is the same.

Thermistors RT1010 and RT1016 limit the surge current when the power supply is first turned on. As current flow warms the thermistors, their resistances decrease and have little effect on circuit operation. Spark-gap electrodes E1001 and E1002 are surge-voltage protectors. If excessive source voltage is applied to the instrument, the spark-gaps conduct, and the extra current flow quickly exceeds the rating of F90. The fuse then opens to protect the instrument's power supply. The EMI (electromagnetic interference) filter, inductors L1011 and L1012, capacitors C1014 and C1016, and resistors R1011, R1014, and R1016 form a line-filter circuit. This filter, along with common-mode rejection transformer T1020, prevents power-line interference from entering the instrument and prevents power supply switching signals from entering the supply line.

Preregulator Control

The Preregulator Control circuit monitors the drive voltage applied to the Inverter output transformer T1060 and holds it at the level that produces proper supply voltages at each of the secondary windings.

The Preregulator Control circuit consists primarily of control IC U1030, its switching buffers, and its power supply components. The control IC senses voltage on the primary winding of T2060 and varies the "on time" of a series-switching transistor, depending on whether the sensed voltage is too high or too low. The switching transistor Q1050, rectifier CR1050, choke T1050, and capacitor C1050 form a buck-switching regulator circuit. The output voltage at W1060 is proportional to the product of the rectified line voltage on C1020-C1022 and the duty cycle of Q1050. In normal operation, Q1050 is on about one-half of the time. When Q1050 is off, current flows to W1060 and T1060 through CR1050.

PREREGULATOR CONTROL POWER SUPPLY. Since the Preregulator control network controls supply startup and preregulates the secondary supplies, an independent power source must be established for it before any of the other power supplies will operate. The independent power supply for the control circuitry is composed of Q1021, Q1022, and the associated components.

Initially, when instrument power is applied, the positive plate of capacitor C1025 is charged toward the positive rectified line voltage through R1020. The voltage at the base of Q1022 follows at a level determined by the voltage divider composed of R1022, R1024, CR1023, and the load within U1030. When the voltage across C1025 reaches about +21 V, the base voltage of Q1022 reaches +6.8 V and Q1022 turns on, saturating Q1021. The +21 V on the emitter of Q1021 appears at its collector and establishes the positive voltage supply for the Preregulator IC. With Q1021 on, R1024 is placed in parallel with R1022, and both Q1022 and Q1021 remain saturated.

The +21-V level begins to drain down as the control IC draws current from C1025. If the Preregulator Control IC doesn't start the switching supply (and thus recharge C1025 and C1023 via CR1022) by the time the voltage across C1025 reaches about +8 V, Q1021 will turn off. Resistor R1024 pulls the base of Q1022 low and turns that transistor off also. (Capacitor C1025 would only discharge low enough to turn off the transistors under a fault condition.) In this event, C1025 would then charge again to +21 V, and the start sequence would repeat. Normally, the control IC will start Inverter action before the +8-V level is reached, and current is drawn through T1050 via Q1050. This induces a current in the secondary winding of T1050 and charges C1025 positive via diode CR1022. The turns ratio of T1050 sets the secondary voltage at approximately +15 V; and, as long as the supply is being properly regulated, C1025 will be charged up to that level and held there.

PREREGULATOR START-UP. As the supply for the Preregulator Control IC is established, an internal switching oscillator begins to run. The oscillator generates a repetitive triangular wave (as shown in Figure 3-11) at a frequency determined primarily by R1032 and C1032. The simplified schematic of Figure 3-12 illustrates the voltage control functions of U1030.

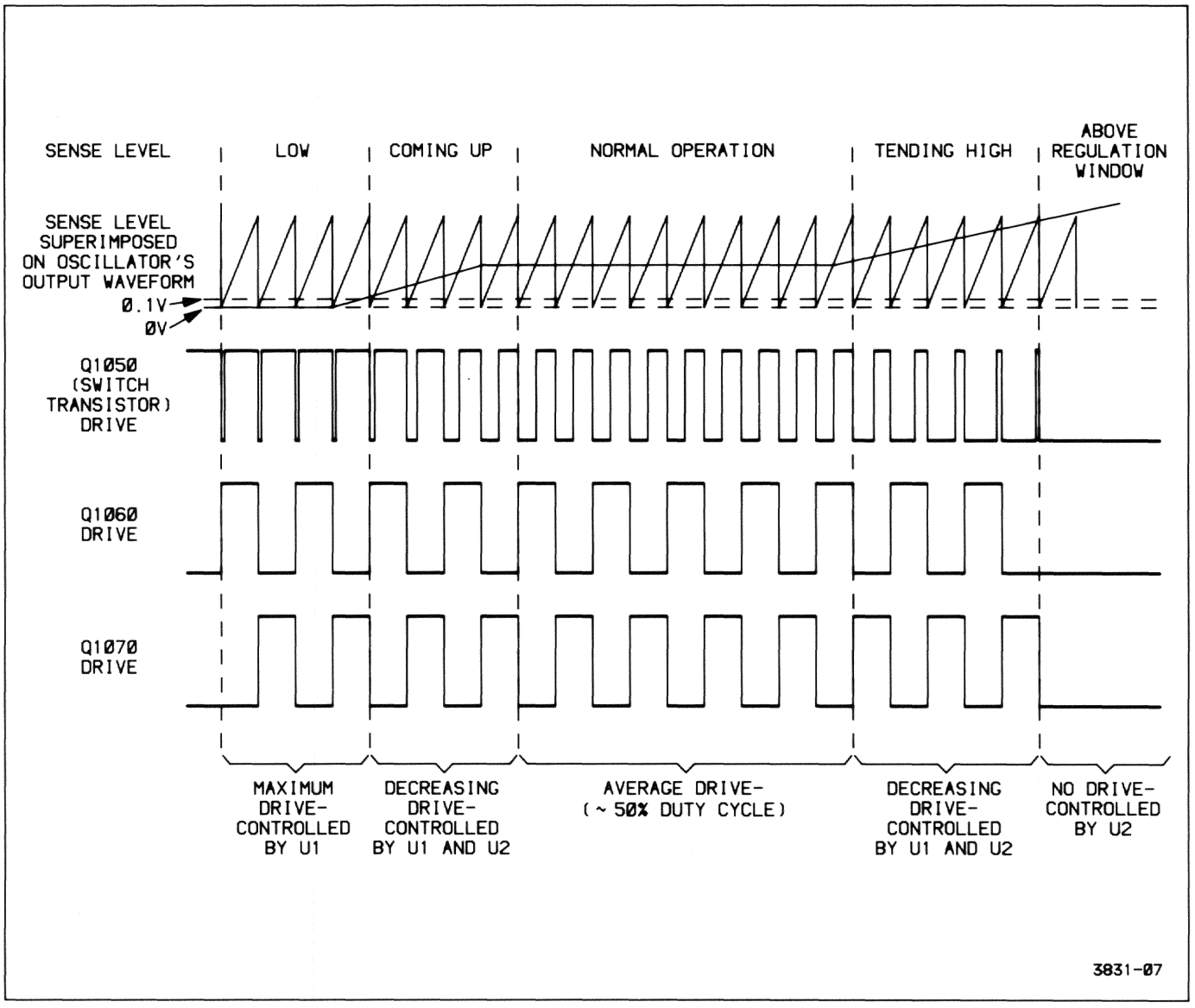


Figure 3-11. Timing relationships of the Inverter Drive signals.

As the Preregulator power supply turns on, capacitor C1034 charges from the +5-V reference level toward ground potential through R1034 and R1037. As it does, the voltage at pin 4 (one input of Dead-Time Comparator U1) will pass through the positive-peak value of the triangular waveform on the other input of the Dead-Time Comparator. The comparator will then begin outputting narrow pulses that become progressively wider as the voltage on pin 4 settles to zero volts. These pulses drive switching transistor Q1050, and their slow progression from narrow to wide causes the various secondary supplies to gradually build up to their final operating levels. The slow buildup prevents a turn-on current surge that would cause the current-limit circuitry to shut down the supply.

During the startup, capacitor C1072 acts as a substantial load, and a relatively large current will flow in the windings of T1050 for the first few cycles of Preregulator switching. These strong current pulses ensure that storage capacitor C1066 becomes charged sufficiently to start the Inverter Drive circuit. Once the Inverter Drive stage is operating, the normal switching current through T1050 maintains the required charge on C1066. (The Inverter Drive power supply is discussed later in this description.)

Dead-Time Comparator U1 is referenced at approximately 0.1 V above the ground level at pin 4 (established when C1034 becomes fully charged) and outputs a narrow,

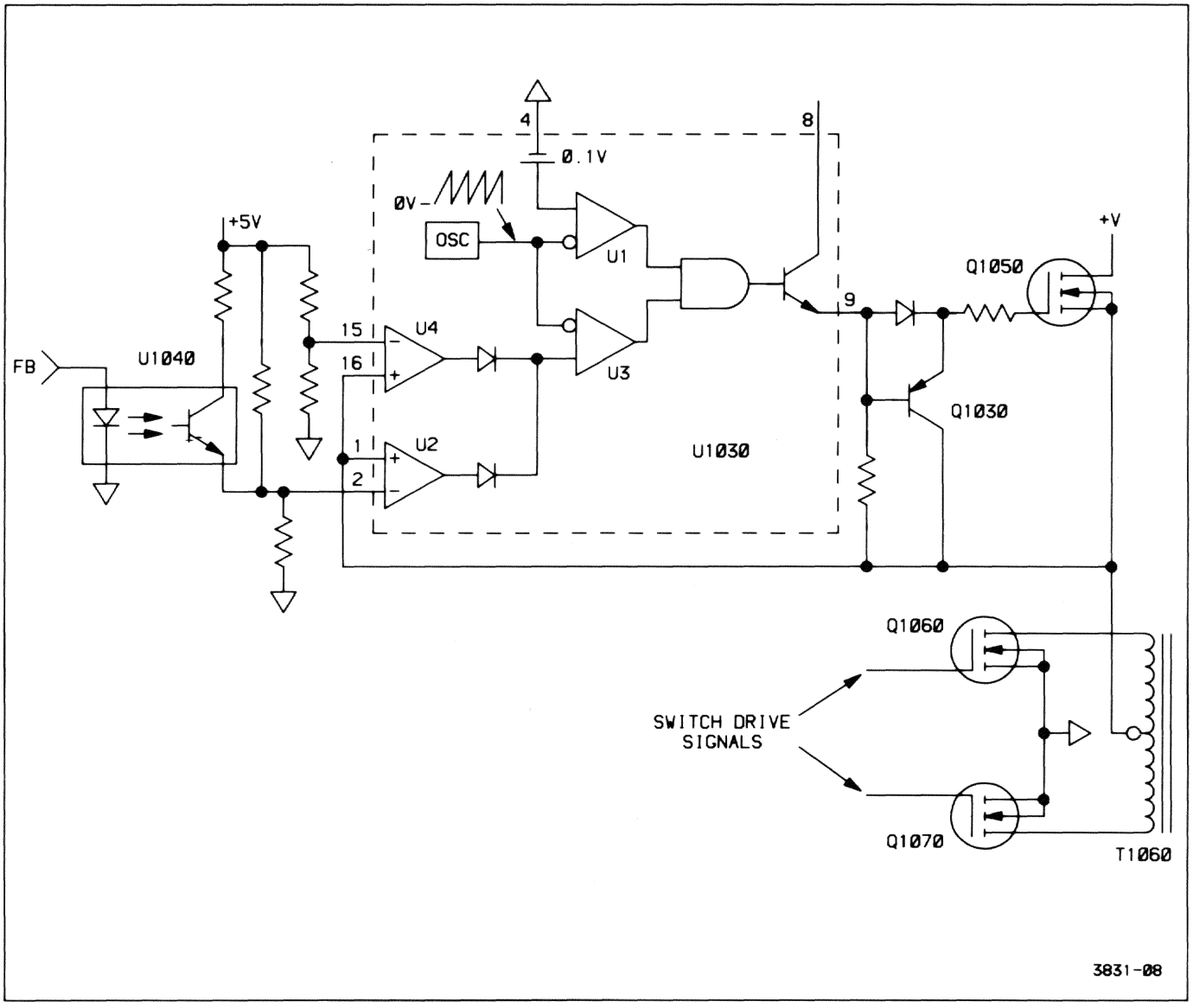


Figure 3-12. Simplified schematic of control network.

negative-going pulse that turns off switching transistor Q1050 for a portion of each switching cycle. This off time ensures that flip-flop U1064B in the Inverter Drive circuit toggles every cycle (thereby maintaining the proper duty cycle), independent of the voltage conditions being sensed by the remainder of the voltage control circuitry.

PREREGULATION. Once the initial charging at power-up is accomplished, as just described, the voltage-sensing circuitry begins controlling the Inverter switching action. The actual voltage sensing is done by error amplifier U2. The level at the center tap of output transformer T1060 is applied to pin 1 and is compared to the reference established by R1045 and R1046 at pin 2. If the sensed level at pin 1 is lower than the reference level at pin 2 (as it will always be for the first few switching cycles), the output of error-amplifier U2 will be LO. The LO, applied to the inverting input of U3, results in a long-duty-cycle drive signal to transistor Q1050 (via CR1030). Since the Inverter Drive stage will alternately turn either Q1060 or Q1070 on, relatively large current pulses will result in the primary winding of inverter output transformer T1060.

These large current pulses, over the period of a few cycles, will increase the charge on the storage capacitors on the secondary side of the transformer and will reduce the current demand on the inverter output transformer. As the demand decreases, the voltage across the primary winding will increase until it reaches the point where the two inputs of U2 are at the same potential. At this point, the output of U2 (to U3) will settle to a level approximately equal to the midpoint of the triangular waveform applied to the other input of U3. The resulting drive signal has an approximate 50% duty cycle and will respond to changes in either the ac line voltage or supply load conditions. Depending on the output levels sensed, the duty cycle of the drive signal will change (sensed level rises or falls with respect to the triangular waveform) to hold the secondary supplies at their proper levels.

Opto-isolator U1040 and resistor R1044 form a control network that allows a voltage sensed at the feedback input (FB) to slightly alter the voltage-sense reference applied to pin 2 of U2. The FB signal is generated by the +5-V Inverter Feedback amplifier (U1371, diagram 10) and is directly related to the level of the +5-V_D supply line. Base drive to the shunt transistor (in opto-isolator U1040) is increased should the FB signal go below its nominal value. Additional current is shunted around R1045 (via R1044) and raises the voltage-sense reference level to error-amplifier U2. This increases the voltage applied to the primary winding of the output transformer, since U2 sensing depends on a balanced condition. Higher currents are induced in the secondary windings, and the secondary voltages begin to return to their nominal values. As the +5-V_D line returns to its nominal level, base drive to the shunt transistor will be reduced and the voltage in the primary winding will follow. Should the FB signal level tend too high, opposite control responses occur. Further information about the FB signal is given in the +5 V Inverter Feedback description.

Error amplifier U4 and the voltage divider composed of R1035 and R1031 provide a backup sensing circuit. Its operation is similar to that of error amplifier U2, just described, but it senses at a slightly higher level. As long as U2 is operating properly, U4 will be inactive. However, should a failure occur in the U2 sensing circuitry, the voltage on the primary winding of T1060 will rise to the sensing level at pin 15 of U4. Sense amplifier U4 will then take over, preventing a damaging over-voltage condition.

Inverter Drive

The Inverter Drive circuit performs the necessary switching to drive the Inverter output transformer. Like the Preregulator Control IC, the Inverter Drive circuit requires an independent power supply, since it must be operational before any of the secondary supply voltages can be generated.

INVERTER DRIVE POWER SUPPLY. This power supply consists of Q1062, VR1062, and their associated components. As power is first applied, the initial charging current through T1050 induces a current in the transformer secondary winding (pins 8 and 9). The alternating current is rectified by the diode bridge composed of CR1062, CR1063, CR1064, and CR1065 and stored on C1066, providing power for the Inverter Drive circuitry.

When the Preregulator Control IC turns switching transistor Q1050 on for the first time, the charge stored on C1066 during the initial charging period is sufficient to properly turn on one of the current-switching transistors (either Q1060 or Q1070) for the first cycle. After that, the alternating drive signals continue to induce current into the secondary winding of T1050 to provide operating power as long as the instrument is turned on.

The current rectified by the diode bridge and stored on capacitor C1066 is regulated down to the required voltage level by R1061, VR1062, and Q1062. Zener diode VR1062 references emitter-follower Q1062 and holds the supply output at approximately +11.4 V.

INVERTER DRIVE GENERATOR. The Inverter Drive generator consists of U1062, U1064, U1066, switching transistors Q1060 and Q1070, and the associated components. The circuitry alternately switches current through each leg of the output transformer primary winding and produces the ac current required for transformer action.

Out-of-phase input signals to comparator U1062C come from two resistive voltage dividers placed in either leg of one secondary winding of T1050. The comparator detects the phase changes (crossover points) of the secondary current caused as Q1050 switches on and off. Every complete on-off cycle of Q1050 produces a positive clock at pin 14 of U1062C that toggles flip-flop U1064B. The toggling alternately turns switching transistors Q1060 and Q1070 on, each with an approximate 50% duty cycle.

Comparators U1062A and U1062B, at the Q and Q output of the flip-flop, detect the precise crossing point of the toggling drive signals and ensure that only one switching transistor will be on at any one time. These mutually-exclusive drive signals are buffered by inverters U1066A and U1066B and applied to switching transistors Q1060 and Q1070 to alternately turn them on and off at one-half the switching rate of Q1050. By alternately switching opposite ends of the primary winding to ground, the current flowing through switching transistor Q1050 will flow alternately in each half of the primary winding. This produces ac voltages at the secondary windings that are rectifiied, providing the various unregulated dc supply voltages.

Current Limit

The Current Limit circuit, composed of transistor Q1040 and the associated components, limits the maximum current flow in the output transformer to about 1 ampere. Resistor R1040 (connected to the Preregulator Control IC +15-V supply) forward biases germanium diode CR1040 and applies approximately +0.3 V across the base-to-emitter junction of Q1040. Current flowing to the output transformer develops a voltage drop across R1050 that adds to the bias developed by CR1040. As the current to the transformer increases, the voltage drop across R1050 also increases until, at around 1 A, the combined voltage drop across R1050 and CR1040 forward biases transistor Q1040. The base of Q1022 is pulled negative through R1042, and the +15-V supply for the Preregulator IC turns off (see Preregulator Control discription). The power supply will try to restart itself; but, as long as the excessive-current condition persists, the current-limit circuit will keep shutting the supply down, protecting the instrument.

Rectifiers

The Rectifiers convert the alternating current from the secondary windings of the inverter output transformer to the various dc supply voltages required by the instrument. Rectification is done by conventional diode rectifier circuits, and filtering is done by conventional LC networks.

The +87-V unregulated supply is produced by a voltage-doubler circuit. The positive plate of C1130 at the anode of CR1132 is referenced at approximately +45 V through diode CR1131 (to the +42-V unregulated supply). As the positive half cycle from the 42-V secondary winding (actually about +45 V peak) is applied to the negative plate of C1130, the positive plate is elevated to a peak value of approximately +90 V. Diode CR1132 becomes forward biased and storage capacitor C1132 is charged to about +90 V. Following cycles replenish the charge drawn off by the loads on the +87-V supply line.

Line Signal

A sample of the ac line voltage is coupled to the Trigger circuit by transformer T1229 and provides the LINE TRIG signal to the Trigger hybrid. Transformer current is limited to a safe value by resistors R1014 and R1015 placed in series with the primary winding leads. The transformer's output characteristics are matched to the input of the Trigger circuit hybrid by R1208 and C1208.

Line Up Signal

The circuit composed of Q1029, opto-isolator U1029, and their associated components, detects when power has been applied to the instrument and the Preregulator Control power supply is functioning properly. When the rectified line voltage reaches proper operating voltage, the voltage divider composed of R1027 and R1028 forward biases Q1029. As soon as the Preregulator Control power supply turns on, current flows through R1029, Q1029, and the opto-isolator LED. The illuminated LED saturates transistor U1029 and the LINE UP signal to the Power-Up Delay circuit (diagram 1) is pulled HI, indicating that the Preregulator Control circuit should now be functioning properly.

POWER DOWN. When instrument power is turned off, the voltage across the primary storage capacitors (C1021 and C1022) begins to fall as the capacitors discharge. As the voltage drops, the bias current through R1027 to the base of Q1029 also drops until the bias voltage across R1028 reaches a point about 2 V above the average transformer drive level at pin 2 of U1029. At this point, Q1029 turns off, and the LINE UP signal to the Power-up Delay circuit goes LO. This LO signals the Microprocessor that it should start its power down routine.

The Line Up circuit tells the Microprocessor that the primary capacitors have started discharging while there is still a stored charge (set by R1027 and R1028) about 40% in excess of that required to keep the power supply voltages in regulation. This allows the Microprocessor to complete the power-down sequence before the supplies drop below their normal operating levels. Further information about the power-down sequence is given in the Microprocessor Reset Control description.

LOW VOLTAGE REGULATORS

The Low Voltage Regulators remove ac noise and ripple from the various unregulated dc supply voltages. Each regulator output is automatically current limited if the output current exceeds the requirements of a normally functioning instrument. This limiting prevents any further component damage.

+10 V Reference

Each of the power-supply regulators control their respective outputs by comparing their output voltages to a known reference level. In order to maintain stable supply voltages, the reference voltage must itself be highly stable. The circuit composed of U1290, U1300C, and associated components establishes this reference.

Resistor R1400 and capacitor C1400 form an RC filter network that smooths the unregulated +15-V supply before it is applied to voltage-reference IC U1290. The +2.5-V output from pin 2 of U1290 is applied to the noninverting input of operational amplifier U1300C. The output of U1300C is the source of the +10-V reference level used by the various regulators. The output level is set by the voltage divider formed by R1291, R1293, and potentiometer R1292. The Volt Ref Adjust pot in the divider allows the reference level to be precisely set. Zener diode VR1292 prevents the reference from exceeding +11 V should a failure in the reference circuitry occur.

+87 V Regulator

The +87 V Regulator is composed of Q1220, Q1221, Q1222, Q1223, U1281A, and the associated components. The circuit regulates and limits both the voltage and current of the supply output.

Initially, as power is applied, the voltage applied to pin 2 of U1281A from the voltage divider formed by R1227 and R1228 is lower than the +10-V reference level applied to pin 3. The output of U1281A is forced high, reverse biasing the base-emitter junction of Q1222 and turning it completely off. With Q1222 off, all the current through R1212 is supplied as base current to Darlington transistor pair Q1221 and Q1220, and maximum current flows in series-pass transistor Q1220. This charges up the various loads on the supply line, and the output level charges positive.

As the regulator output charges toward +87 V, the voltage divider applies a positive-going voltage to the inverting inputs of U1281A. When the output level reaches +87 volts, the inverting input equals the +10-V reference at the noninverting input. The output voltage at pin 1 of U1281A will go negative and the base-emitter junction of Q1222 will be biased into the active region. As Q1222 turns on, base drive for the Darlington pair (Q1221 and pass transistor Q1220) is reduced. The output will be held at the level required for voltage at the two inputs of amplifier U1281A to be in balance (+87 V).

Current limiting is a foldback design and is performed by Q1223 and its associated components. Under normal current demand conditions, Q1223 is off. If the regulator output current exceeds approximately 100 mA (as it might if a component fails), the voltage drop across R1221 and CR1220 reaches a point that forward biases Q1223 via the bias divider formed by R1222 and R1223. As Q1223 turns on, a portion of the base-drive current to Q1221 is shunted away by Q1223. This reduces the base-drive current (and thus the output current) of series-pass transistor Q1220.

+42 V Regulator

The circuit configuration and operation of the +42 V Regulator is identical to that of the +82 V Regulator. Current limiting of the +42-V supply occurs at approximately 400 mA. Base drive to Darlington pair Q1241 and Q1240 is via R1244 and is dependent on proper operation of the +87 V Regulator. This dependency ensures that the relative polarities of the two supplies are never reversed (preventing semiconductor-junction damage in the associated load circuitry).

+15 V Regulator

The +15 V Regulator uses three-terminal regulator U1260 and operational amplifiers U1371A and U1371B, arranged as voltage sensors, to achieve regulation of the +15-V supply. The three-terminal regulator holds its output voltage at pin 2 at 1.25 volts more positive than the reference input level at pin 1. The voltage at the reference pin is established by current flow in either diode CR1262 or CR1263.

Resistors R1261 and R1262 at the regulator output divide the +15-V level down for comparison with the +10-V reference applied to pin 5 of operational amplifier U1371B. When the input voltage at pin 6 (supplied by the voltage divider) is lower than the +10-V reference, the output of amplifier U1371B is high and the output voltage of U1260 is allowed to rise. As the regulator output reaches +15 V, the voltage on pin 6 of U1371B approaches the level on pin 5, and the amplifier begins sinking current away from the reference pin of the three-terminal regulator via diode CR1263. This lowers the voltage on the reference pin and holds the ouput at +15 V.

The other voltage-sensing amplifier (U1371A) ensures that the relative polarity between the +15-V supply and the

+42-V supply is maintained, preventing component damage in the load circuitry. Should the +42-V supply be pulled below +15 V (excessive loading or supply failure), the voltage at pin 3 of U1371A falls below the voltage at pin 2 and the amplifier output voltage goes low. This forward biases CR1262 and lowers the reference voltage for U1260, reducing the output voltage.

Current limiting for the +15-V supply is provided by the internal circuitry of the three-terminal regulator.

+5 V Regulator

Regulation of the +5-V supply is provided by a circuit similar to those of the +87 V and the +42 V Regulators. As long as the relative polarity between the +15-V and the +5-V supplies is maintained, base drive to Q1281 is supplied through R1283. The current through Q1281 provides base drive for series-pass transistor Q1280.

When voltage-sense amplifier U1300B detects that the output voltage has reached +5 V, it begins shunting base-drive current away from Q1281 via CR1281 and holds the output voltage constant.

Current limiting for the +5-V supply is done by U1300A and associated components. Under normal current-demand conditions, the output of U1300A is high and diode CR1282 is reverse biased. However, should the current through current-sense resistor R1281 reach approximately 2 A, the voltage developed across R1281 will raise the voltage at pin 2 of U1300A (via divider R1282 and R1286) to a level equal to that at pin 3. This causes the output of U1300A to go low, forward biasing CR1282. This sinks base drive current away from Q1281 and lowers the output current in series-pass transistor Q1280.

−15 V Regulator

Operation of the −15 V Regulator, composed of three-terminal regulator U1330, operational amplifier U1270C, and their associated components, is similar to that of the +15 V Regulator with the following major changes. The control voltage at the three-terminal regulator's reference pin (pin 1) is established by the current through series-resistors R1333 and R1334. The reference pin is clamped by CR1332 at about −5.6 V should a failure in the sensing network occur. (Clamping also prevents latchup of the operational amplifier during startup of the power supply.) Finally, the sensing divider formed by R1331 and R1332 is referenced to the +10-V reference instead of ground to enable sensing of negative voltage.

−8 V Regulator

Operation of the −8 V Regulator is similar to that of the +87 V and +42 V Regulators. Due to the lower operating voltages of the −8 V Regulator, the common-base transistor present in both the +87 V and the +42 V Regulators is not required. Current limiting in the −8-V supply occurs at about 480 mA.

−5 V Regulator

Operation of the −5 V Regulator is similar to that of the +5 V Regulator. Current limiting in the −5-V supply occurs at about 2 A.

+5 V Inverter Feedback

Operational amplifier U1371C and associated components are configured as a frequency-compensated voltage-sensing network. The circuit monitors the +5-V digital power supply line from the rectifiers and provides feedback to the Preregulator Control IC (U1030) via opto-isolator U1040 (both on diagram 9). The feedback is used to slightly vary the voltage-sensing characteristics of the Preregulator Control circuitry. The feedback (FB) signal slightly varies the voltage to the Inverter output transformer and holds the output of the 5-V secondary windings at an optimum level. Output levels of the other secondary windings are related to the +5-V_D level and are also held at their optimum values. This technique minimizes power losses in the series-pass transistors and increases regulator reliability.

Power-Up Delay

The Power-Up Delay circuit, composed of Q1370, Q1376, U1371D, and the associated components, ensures that the various regulated power supplies have time to reach their proper operating voltages before signaling the Microprocessor that the supplies are up.

When power is first applied, the LINE UP signal from the Preregulator Control circuit goes HI, indicating that the power switch has been closed and that ample supply voltage is available for driving the Inverter transformer. The HI is applied to the base of Q1370, but since the collector is not properly biased yet, no transistor current will flow. As the Inverter begins to run, the various voltages from the secondary rectifiers begin coming up to their proper levels. A +2.5-V reference voltage is applied to operational amplifier U1371D pin 12 and forces the output high, biasing Q1376 on. The resulting LO at the transistor's collector signals the Microprocessor that the power supplies are not yet stable.

Before any of the Low Voltage Regulators may function properly, the +10-V reference voltage must be established as previously described. When the +15 V Regulator turns on, current flows through Q1370, and pin 2 of U1371D is pulled above the +2.5-V reference through divider R1370 and R1372. The output of U1371D goes low, turning off Q1376. The PWR UP signal at the collector goes HI, signaling the Microprocessor that the power supplies should now be operating properly.

When power to the instrument is turned off, the LINE UP signal goes LO (as explained in the Line Up Signal description). The falling LINE UP signal turns Q1370 off and drives the output of U1371D high. The output level from U1371D turns on Q1376 and pulls the PWR UP signal to the Microprocessor LO. This LO initiates the power-down sequence used to store the current front-panel setup conditions in EAROM and to shut down the instrument in an orderly fashion. The delay between the time that the PWR UP signal goes LO and when the regulated power supplies fall below their normal operating levels provides ample time for the Microprocessor to complete the power-down sequence.

Fan Circuit

The fan motor used in this instrument is a brushless, dc motor that uses Hall-effect devices to control its rotation speed. The two Hall-effect devices sequentially drive the four field-control transistors (U1690A, B, C, and D) which in turn control field current to the fan motor windings. The fan's speed is determined by the amount of drive current supplied by Q1698 and varies with ambient temperature.

As the ambient temperature in the cabinet increases, the resistance of RT1696 decreases, and additional base drive is provided to Q1698. The transistor conducts harder, and the fan's motor speed is increased to provide more cooling capacity.

The back EMF produced by the motor field windings is also proportional to motor speed. This back EMF is rectified by diodes CR1691, CR1692, CR1694, and CR1696 and is applied to the base node of Q1698 via R1697. This current opposes the normal bias current of the transistor and acts as a form of negative feedback to stablilize the motor speed from cycle to cycle.

POWER DISTRIBUTION

Schematic diagrams 11 and 12 illustrate the power distribution of the 2445. The connections to the labeled boxes (representing the hybrids and ICs) show the power connections to each device, while connections to non-power lines are shown by the component and schematic number. Power supply decoupling is done with traditional LRC networks as shown on the diagrams.

Several intermediate supply voltages are generated by devices shown on diagrams 11 and 12. An approximate +32-volt supply for the A and B Sweeps is developed by emitter-follower Q700 and its associated components. Zener diodes VR125 and VR225 develop approximate +6.2-volt supplies for the CH 1 and CH 2 Preamps respectively, and zener diode VR2805 establishes an approximate −6.8-volt supply for U2800 and U2805.

INTERCONNECTIONS

Schematic diagram 13 illustrates the circuit board interconnections of the 2445. Connector numbers and cabling types are shown.

PERFORMANCE CHECK AND FUNCTIONAL VERIFICATION PROCEDURE

INTRODUCTION

This procedure is used to verify proper operation of instrument controls and to check the instrument's performance against the requirements listed in the "Specification" (Section 1). This procedure verifies instrument function and may be used to determine need for readjustment. These checks may also be used as an acceptance test and as a preliminary troubleshooting aid.

Removing the wrap-around cabinet is not necessary to perform this procedure. All checks are made using the operator accessible front- and rear-panel controls and connectors.

Within the procedure, steps to verify proper operation of an instrument control or function that is not specified in the "Specification" section begin with the word "VERIFY". These functions ARE NOT specifications and should not be interpreted as such. Steps to check performance specifications begin with the word "CHECK".

PREPARATION

Test equipment items 1 through 17 listed in Table 4-1 are required to perform this procedure. The specific pieces of equipment required to perform the checks within each section are listed at the beginning of that section. The item numbers in parenthesis next to each piece of equipment refer to the numbered equipment list of Table 4-1. Items 18 through 22 are used only for instrument calibration (see the Adjustment Procedure in Section 5).

Before performing this procedure, ensure that the LINE VOLTAGE SELECTOR switch is set for the ac power source being used (see "Preparation for Use" in Section 2). Connect the instrument to be checked and the test equipment to an appropriate power source. Turn the instrument on and ensure that no error message is displayed on the crt. If an error message is present, have the instrument repaired or calibrated by a qualified service technician before performing this procedure.

The procedure is divided into sections to permit functional and performance verifications of individual sections of the instrument without performing the entire procedure. Perform all steps within a section, both in the sequence presented and in their entirety to ensure that control settings are correct for the following step.

When performing partial procedures, the Initial Control Settings at the first of the section should be setup first; then make any changes noted at the first of the subsection to be performed. When performing the procedures in sequence, merely change those controls that have changed from the previous step.

Table 4-1
Test Equipment Required

Item and Description	Minimum Specification	Use	Example of Applicable Test Equipment
1. Variable Power Supply	Variable output voltage: 0V to +16V.	Check input overload switching.	TEKTRONIX PS 503A.
2. Leveled Sine-Wave Generator	Frequency: 50 kHz to 150 MHz. Output: 0 V to 5 V. Reference frequency: 50 kHz.	Check bandwidth and triggering.	TEKTRONIX SG 503.
3. Calibration Generator	Fast-rise, low-abberation amplitudes: to 1 V. Rise time: 1 ns or less. Repetition rate: 1 kHz to 100 kHz. Precision amplitudes: 0.01 V to 50 V ±0.25%.	Signal source for gain and transient response.	TEKTRONIX PG 506.
4. Function Generator	Repetition rate: 1 kHz to 1 MHz. Output to 15 V p-p.	Check triggers and coupling.	TEKTRONIX FG 501A.
5. Time-Mark Generator	Markers: 2 ns to 5 s in a 1-2-5 sequence. Marker accuracy: ±0.1%.	Check horizontal timing.	TEKTRONIX TG 501.
6. Oscilloscope with P6131 10X Standard Accessory Probe.	Bandwidth: 150 MHz. General Purpose.	Check power supply ripple and output signals. Troubleshooting.	TEKTRONIX 2445.
7. T-Connector	Impedance: 50 Ω. Connectors: BNC.	Signal interconnection.	TEKTRONIX Part Number 103-0030-00.
8. Precision BNC Cable	Impedance: 50 Ω. Connectors: BNC. Length: 36 in.	Signal interconnection.	TEKTRONIX Part Number 012-0482-00.
9. BNC Cable (2 required)	Impedance: 50 Ω. Connectors: BNC. Length: 42 in.	Signal interconnection.	TEKTRONIX Part Number 012-0057-01.
10. Dual-Input Coupler (2 required)	Connectors: BNC female-to-dual-BNC male.	Signal interconnection.	TEKTRONIX Part Number 067-0525-02.
11. Termination (2 required)	Impedance: 50 Ω. Connectors: BNC.	Signal interconnection.	TEKTRONIX Part Number 011-0049-01.
12. Adapter	Mini probe-tip-to-BNC male.	Signal interconnection.	TEKTRONIX Part Number 013-0195-00.
13. Adapter	BNC female-to-BNC female.	Signal interconnection.	TEKTRONIX Part Number 103-0028-00.
14. Adapter	Connectors: BNC female-to-dual banana.	Signal interconnection.	TEKTRONIX Part Number 103-0090-00.
15. Attenuator	Attenuation factor: 2X. Impedance: 50 Ω. Connectors: BNC.	Signal attenuation.	TEKTRONIX Part Number 011-0069-02.
16. Attenuator	Attenuation factor: 5X. Impedance: 50 Ω. Connectors: BNC.	Signal attenuation.	TEKTRONIX Part Number 011-0060-02.
17. Attenuator	Attenuation factor: 10X. Impedance: 50 Ω. Connectors: BNC.	Signal attenuation.	TEKTRONIX Part Number 011-0059-02.
18. Digital Multimeter (DMM)	DC volts range to +20 V. Accuracy ±0.2%.	Check power supplies and CALIBRATOR.	TEKTRONIX DM 502A.

Table 4-1
Test Equipment Required

Item and Description	Minimum Specification	Use	Example of Applicable Test Equipment
19. Low-Capacitance Alignment Tool	Shaft length: 2 in.	Adjust variable resistors and capacitors.	TEKTRONIX Part Number 003-0675-00.
20. 1X Probe	Attenuation: 1X. Bandpass: <20 MHz.	Check power supply ripple.	TEKTRONIX P6101.
21. Normalizer	Input resistance: 1 MΩ. Input capacitance: 15 pf.	Check input capacitance.	TEKTRONIX Part Number 067-0537-00.
22. Tunnel Diode Pulser	Rise time: 125 ps or less.	Check transient response.	TEKTRONIX Part Number 067-0681-01.

VERTICAL

Equipment Required (see Table 4-1)

- Power Supply (Item 1)
- Leveled Sine-Wave Generator (Item 2)
- Calibration Generator (Item 3)
- P6131 10X Probe (supplied with 2445) (Item 6)
- Precision 50 Ω BNC Cable (Item 8)
- 50 Ω BNC Cable (Item 9)
- Dual-Input Coupler (Item 10)
- 50 Ω BNC Termination (Item 11)
- Mini Probe Tip-to-BNC Adapter (Item 12)
- BNC Female-to-BNC Female Adapter (Item 13)
- BNC Female-to-Dual Banana Adapter (Item 14)
- 2X Attenuator (Item 15)
- 5X Attenuator (Item 16)
- 10X Attenuator (Item 17)

Initial Control Settings.

Control settings not listed do not affect the procedure.

Set:

VERTICAL MODE	
CH 1	On (button in)
CH 2, CH 3, CH 4, ADD, and INVERT	Off (buttons out)
CHOP/ALT	ALT (button out)
20 MHz BW LIMIT	Off (button out)
VOLTS/DIV	
CH 1 and CH 2	1 V
CH 1 and CH 2 VAR	In detent
CH 3 and CH 4	0.1 V (buttons out)
Input Coupling	
CH 1 and CH 2	1 MΩ GND
A and B SEC/DIV	10 ms (knobs locked)
A and B SEC/DIV VAR	In detent
X10 MAG	Off (button out)
Δt and ΔV	Off (press and release until associated readout is off)
TRACKING	Off (button out)
TRACE SEP	Fully CW
TRIGGER	
HOLDOFF	Fully CCW
LEVEL	Midrange
SLOPE	+ (plus)
A/B TRIG SELECT	A
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC

1. Verify CH 1 and CH 2, 50 Ω OVERLOAD Protection.

a. Connect the Power Supply to the CH 1 OR X input connector via a 50 Ω BNC cable and a BNC female-to-dual banana adapter.

b. Using the CH 1 VERTICAL POSITION control, position the trace on the bottom horizontal graticule line.

c. Change the CH 1 Input Coupling switch to 1 MΩ DC.

d. Turn the Power Supply on.

e. Adjust the Power Supply output level until the CH 1 trace rises to 1 division above the center graticule line (+5 V).

f. Change the CH 1 Input Coupling switch to 50 Ω DC.

g. VERIFY—For a period of one minute, the readout display does not indicate any overload condition (50 Ω OVERLOAD).

h. Change the CH 1 VOLTS/DIV control to 5 V and the CH 1 Input Coupling to 1 MΩ DC.

i. Increase the Power Supply output level until the CH 1 trace rises to the center graticule line (+20 V).

CAUTION

To prevent damage to the input circuitry when in 50 Ω DC, the 20 V source must not be applied to the CH 1 OR X or CH 2 input connectors for longer than 15 seconds. If the automatic OVERLOAD switching does not occur within 15 seconds, turn the Power Supply off immediately.

j. Set the CH 1 Input Coupling switch to 50 Ω DC.

k. VERIFY—Approximately 10 seconds after the CH 1 input coupling switch is set to 50 Ω DC, the readout display indicates "50 Ω OVERLOAD", the CH 1 Input Coupling switch changes to 1 MΩ GND automatically, and the trace returns to the bottom horizontal graticule line.

l. Turn the Power Supply Off.

m. Disconnect the Power Supply.

n. Clear the OVERLOAD condition by pressing up on the CH 1 Input Coupling switch.

o. VERIFY—The CH 1, 1 MΩ DC indicator is lit and the readout display no longer indicates "50 Ω OVERLOAD".

p. Set the VERTICAL MODE switches to display CH 2 and repeat parts a through o to verify 50 Ω OVERLOAD protection for that channel.

2. Check CH 1 and CH 2 Low-Frequency AC Coupling.

a. Set:

VERTICAL MODE	
CH 1	In (button in)
CH 2	Off (button out)
A and B SEC/DIV	10 ms (knobs locked)
VOLTS/DIV	
CH 1 and CH 2	10 mV
Input Coupling	
CH 1 and CH 2	1 MΩ GND

NOTE

Prior to performing the following steps, the 10X probe must be properly compensated. Refer to "Probe Low-Frequency Compensation" in Section 2 of this manual.

b. Connect the CALIBRATOR output signal to the CH 1 OR X input connector using a 10X probe.

c. Position the ground-reference trace 2 divisions below the center horizontal graticule line.

d. Set the CH 1 Input Coupling switch to 1 MΩ DC.

e. CHECK—Displayed signal is vertically centered and has an amplitude of 3.88 to 4.12 divisions.

f. Set the CH 1 Input Coupling to the upper 1 MΩ GND position .

g. Using the CH 1 POSITION control, align the trace with the center horizontal graticule line.

h. Set the CH 1 Input Coupling switch to 1 MΩ AC.

i. CHECK—Displayed signal is a tilted square wave, 4.5 to 4.9 divisions in amplitude, vertically centered on the graticule.

j. Move the probe to the CH 2 input connector.

k. Set the VERTICAL MODE switches to deselect CH 1 and display CH 2.

l. Repeat parts c through i for CH 2.

m. Disconnect the test setup.

3. Check CH 1 and CH 2 VOLTS/DIV, CH 2 INVERT, ΔV and TRIGGER LEVEL Readout Accuracies, Variable VOLTS/DIV, Vertical Linearity, and ADD.

a. Set:

Input Coupling	
CH 1 and CH 2	1 MΩ AC

VERTICAL MODE	
BW LIMIT	On (button in)
ΔV	On (press and release for a ΔV readout)
VOLTS/DIV	
CH 1 and CH 2	2 mV
A and B SEC/DIV	1 ms (knobs locked)
TRIGGER	
MODE	AUTO

NOTE

The instrument must have had at least 20 minutes warmup prior to performing the following steps.

b. Press up and momentarily hold the CH 1 and CH 2 Input Coupling switches in their 1 MΩ AC positions until a moving dot display replaces the normal signal and readout displays (for approximately 15 seconds). This performs a DC Balance of CH 1 and CH 2.

c. When the signal and readout displays automatically return to normal, set the CH 1 and CH 2 Input Coupling to 1 MΩ DC.

d. Connect the Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable. Do not use a termination.

e. CHECK—CH 1 and CH 2 VOLTS/DIV, ΔV, and TRIGGER LEVEL readout accuracies as follows:

1. Set VOLTS/DIV control to the first position listed in Table 4-2.

2. Set the Calibration Generator STD AMPLITUDE output level to the corresponding Standard Amplitude Input Level in Table 4-2.

NOTE

To properly verify TRIGGER LEVEL Readout Accuracy, the Calibration Generator's STD AMPLITUDE output must have rising and falling transition times (10% to 90%) > 20 ns. No overshoot should appear on the waveform.

3. Verify that the generator output meets the requirements noted above.

4. Return the A and B SEC/DIV switch to 1 ms (knobs locked).

5. Use the VERTICAL POSITION control to set the bottom of the signal 2 divisions below graticule center.

6. Rotate the ΔREF OR DLY POS control to align the reference cursor with the bottom of the waveform.

7. Rotate the Δ control to align the Δ cursor with the top of the signal display.

8. CHECK—Vertical Deflection Accuracy (measured against the graticule) and ΔV Readout Accuracy are within the limits listed in Table 4-2.

9. Set the TRIGGER LEVEL control at the most positive voltage that produces a barely triggered, jittering display for each position of the SLOPE switch.

10. CHECK—The A Trigger Level readings (see Figure 2-8) are within the limits given in the +Peak column of Table 4-2.

11. Set the TRIGGER LEVEL control at the most negative voltage that produces a barely triggered, jittering display for each position of the SLOPE switch.

12. CHECK—The A Trigger Level readings are within the limits given in the −Peak column of Table 4-2.

13. Set the TRIGGER LEVEL for a stable display.

14. Pull the SEC/DIV knob out and set the B TRIGGER MODE to TRIG AFT DLY.

15. Adjust ΔREF OR DLY POS control for a delay readout of 0.000 ms.

16. Set the TRIGGER LEVEL control to the most positive voltage that produces an intensified point on the waveform display for each position of the SLOPE switch.

17. CHECK—The B Trigger Level readings are within the limits given in the +Peak column of Table 4-2.

18. Set the TRIGGER LEVEL control to the most negative voltage that produces an intensified point on the waveform display for each position of the SLOPE switch.

19. CHECK—The B Trigger Level readings are within the limits given in the −Peak column of Table 4-2.

20. Push the B SEC/DIV knob in.

21. Change the VOLTS/DIV switch to the next position listed in Table 4-2.

22. Set the Calibration Generator to the corresponding signal amplitude setting.

23. Press and release the ΔV pushbutton to reobtain the ΔV readout display.

24. Repeat subparts 5 through 23 of part e for each VOLTS/DIV setting listed in Table 4-2.

25. Set the TRIGGER COUPLING switch to NOISE REJ.

26. Set the CH 1 and CH 2 Input Coupling switches to 50 mV.

27. CHECK—Trigger Level Readout is within the limits given in Table 4-2 for NOISE REJ Coupling.

f. Return the TRIGGER COUPLING switch to DC.

g. Set the CH 1 VOLTS/DIV switch and the Calibration Generator output level to produce a vertical signal display 5 divisions in amplitude.

h. CHECK—Display amplitude reduces to 2 divisions or less when the VOLTS/DIV VAR control (of the channel under test) is rotated fully CCW. Return the VOLTS/DIV VAR control to its maximum CW (detent) position.

i. Set the Calibration Generator output level and VERTICAL POSITION controls for a 2-division display vertically centered on the graticule. Use the CH 1 VAR control if necessary to obtain the correct display amplitude.

j. Set the VERTICAL POSITION control to align the top edge of the display with the top graticule line.

k. CHECK—Signal display amplitude is 1.9 to 2.1 divisions.

l. Set the VERTICAL POSITION control to align the bottom edge of the signal display with the bottom graticule line.

Table 4-2
Accuracy Limits
CH 1, CH 2, CH 2 INVERT, and Delta Volts Readouts

VOLTS/DIV Switch Setting CH 1 and CH 2	Standard Amplitude Input Level	Vertical Deflection Accuracy (±2% in divisions)	Delta Volts Readout Accuracy (limits) 1.25% + .03 div	Limits of Trigger LEVEL Readout			
				DC Coupling		NOISE REJ Coupling	
				+Peak	−Peak	+Peak	−Peak
2 mV	10 mV	4.90 to 5.10	9.81 mV to 10.20 mV	8.5 mV to 11.5 mV	+1.2 mV to −1.2 mV		
5 mV	20 mV	3.92 to 4.08	19.6 mV to 20.4 mV	17.3 mV to 22.7 mV	+2.1 mV to −2.1 mV		
10 mV	50 mV	4.90 to 5.10	49.0 mV to 50.9 mV	44.5 mV to 55.5 mV	+4 mV to −4 mV		
20 mV	0.1 V	4.90 to 5.10	98.1 mV to 102.0 mV	89 mV to 111 mV	+7.5 mV to −7.5 mV		
50 mV	0.2 V	3.92 to 4.08	196 mV to 204 mV	177 mV to 223 mV	+17 mV to −17 mV	147 mV to 253 mV	+47 mV to −47 mV
0.1 V	0.5 V	4.90 to 5.10	490 mV to 509 mV	0.449 V to 0.551 V	+0.036 V to −0.036 V		
0.2 V	1.0 V	4.90 to 5.10	0.981 V to 1.020 V	0.90 V to 1.10 V	+0.07 V to −0.07 V		
0.5 V	2.0 V	3.92 to 4.08	1.96 V to 2.04 V	1.78 V to 2.22 V	+0.14 V to −0.14 V		
1.0 V	5.0 V	4.90 to 5.10	4.90 V to 5.09 V	4.50 V to 5.50 V	+0.35 V to −0.35 V		
2.0 V	10.0 V	4.90 to 5.10	9.81 V to 10.2 V	9.0 V to 11.0 V	+0.7 V to −0.7 V		
5.0 V	20.0 V	3.92 to 4.08	19.6 V to 20.4 V	17.8 V to 22.2 V	+1.4 V to −1.4 V		

m. CHECK—Signal display amplitude is 1.9 to 2.1 divisions.

n. Move the test signal to CH 2 and set the VERTICAL MODE controls to display CH 2.

o. Repeat parts e through m for CH 2.

p. Rotate the ΔREF OR DLY control CCW until the cursor stops moving.

q. CHECK—Cursor is aligned with the bottom graticule line within ±0.2 division.

r. Rotate the Δ control CW until the cursor stops moving.

s. CHECK—Cursor is aligned with the top graticule line within ±0.2 division.

t. Turn the INVERT function on (button in), return the CH 2 VOLTS/DIV VAR control to the calibrated detent position, and reobtain a 5-division signal as explained in part g above.

u. VERIFY—A down-arrow symbol appears to the left of the CH 2 VOLTS/DIV readout.

v. CHECK—Display amplitude is between 4.9 divisions and 5.1 divisions in amplitude (5 divisions ±2 %). Turn the INVERT function off (button out) when finished.

w. Connect a 5 V standard-amplitude signal from the Calibration Generator to the CH 1 OR X and CH 2 input connectors via a 50 Ω BNC cable and a Dual-Input Coupler.

x. Set:

VOLTS/DIV	
CH 1 and CH 2	2 V
VERTICAL MODE	
CH 1 and CH 2	Off (buttons out)
ADD	On (button in)

y. CHECK—Vertical deflection amplitude is 4.9 to 5.1 divisions.

z. CHECK—Signal amplitude reduces to 0.2 division or less when CH 2 INVERT is on (button in).

aa. Set:

VERTICAL MODE	
CH 3	On (button in)
CH 1, CH 2, CH 4, ADD, and INVERT	Off (buttons out)

bb. Move the Dual-Input Coupler to the CH 3 and CH 4 input connectors.

cc. CHECK—VOLTS/DIV and TRIGGER LEVEL Readout accuracies for both switch setting-input level combinations listed in Table 4-3 as in subparts 5 through 23 of part e.

dd. Set the Calibration Generator output level and VERTICAL POSITION controls for a 2-division display vertically centered on the graticule.

ee. Set the VERTICAL POSITION control to align the top edge of the display with the top graticule line.

ff. CHECK—Signal display amplitude is 1.9 to 2.1 divisions.

Table 4-3
CH 3 and CH 4 Accuracy Limits

VOLTS/DIV Switch Setting CH 3 and CH 4	Standard Amplitude Signal Input Level	Vertical Deflection Accuracy (±10% in divisions)	Trigger LEVEL Readout When Barely Triggered at the Indicated Peak	
			+Peak	−Peak
0.1 V	0.5 V	4.50 to 5.50	0.454 V to 0.545 V	+0.03 V to −0.03 V
0.5 V	2.0 V	3.60 to 4.40	1.81 V to 2.19 V	+0.13 V to −0.13 V

gg. Set the VERTICAL POSITION control to align the bottom edge of the signal display with the bottom graticule line.

hh. CHECK—Signal display amplitude is 1.9 to 2.1 divisions.

ii. Set the VERTICAL MODE switches to disable CH 3 and display CH 4.

jj. Repeat parts cc through hh for CH 4.

kk. Disconnect the test setup.

4. Check Channel 2 Delay.

a. Set:

VERTICAL MODE	
CH 1 and CH 2	On (buttons in)
CH 3 and CH 4	Off (buttons out)
Input Coupling	
CH 1 and CH 2	50 Ω DC
VOLTS/DIV	
CH 1 and CH 2	10 mV
A and B SEC/DIV	1 μs (knobs locked)
TRIGGER	
SOURCE	CH 1

b. Connect a 100 kHz, fast-rise, positive-going signal from the the Calibration Generator to the CH 1 OR X and the CH 2 input connectors via a 50 Ω BNC cable, a 5X attenuator and a Dual-Input Coupler.

c. Set the output level of the Calibration Generator for an approximate 5-division, vertically-centered display for both channels.

d. Use either the CH 1 or CH 2 VAR control to match signal amplitude between both channels.

e. Set:

A and B SEC/DIV	10 ns (knobs locked)
X10 MAG	On (button in)

f. Use the Horizontal POSITION control to move the rising edges of the CH 1 and CH 2 displays to graticule center.

g. Pull the B SEC/DIV knob out to activate the CH 2 DLY feature.

NOTE

If the readout displays "CH 2 DLY DISABLED" instead of "CH 2 DLY—TURN Δ", the delay matching feature has been disabled and the remainder of this subsection cannot be performed. In this case, proceed to subsection 5 below.

h. CHECK—Δ control will position the CH 2 display 1/2 division or more (500 ps) to either side of the CH 1 display.

i. Superimpose the rising edges of the pulses using the Δ control.

j. Turn X10 MAG off (button out) and push in the B SEC/DIV knob.

k. Disconnect the test setup.

5. Check Vertical Bandwidth—All Channels .

a. Set:

A and B SEC/DIV	50 μs (knobs locked)
TRIGGER	
SOURCE	VERT
VOLTS/DIV	
CH 1 and CH 2	2 mV
CH 3 and CH 4	0.1 V (buttons out)
VAR	
CH 1 and CH 2	Calibrated (in detent)
VERTICAL MODE	
CH 1	On (button in)
CH 2, CH 3, and CH 4	Off (buttons out)
Input Coupling	
CH 1 and CH 2	50 Ω DC

b. Connect the output of the Leveled Sine-Wave Generator to the CH 1 OR X input connector via a precision 50 Ω BNC cable and any combination of the 10X, 5X, or 2X Attenuators needed to reduce the signal amplitude to the level called out in the next step.

c. Set the generator output level for a 6-division display at the reference frequency, then change the output frequency to 80 MHz.

d. CHECK—Signal display amplitude is 4.25 divisions or greater.

e. Move the signal to the CH 2 input connector and set the VERTICAL MODE switches to disable CH 1 and display CH 2.

f. Repeat parts c and d for CH 2.

g. Set the CH 1 and CH 2 VOLTS/DIV switch setting to 20 mV.

h. Set the generator output level for a 6-division display at the reference frequency, then change the generator output to 80 MHz.

i. CHECK—Signal display amplitude is 4.25 divisions or greater while sweeping the generator frequency from 80 MHz to 150 MHz.

j. Set the VOLTS/DIV switch to 0.5 V and repeat parts h and i.

k. Set the VOLTS/DIV switch to 1 V and the generator output level for a 4-division display at the reference frequency, then change the generator frequency to 80 MHz.

l. CHECK—Signal display amplitude is 2.82 divisions or greater while sweeping the generator frequency from 80 MHz to 150 MHz.

m. Move the signal to CH 1 OR X input connector and set the VERTICAL MODE switches to disable CH 2 and display CH 1.

n. CHECK—Repeat parts h through l for CH 1.

o. Set the VERTICAL MODE switches to display CH 3 only.

p. Attach the standard-accessory 10X probe (supplied with the instrument) to the CH 3 input connector and the probe tip to the CALIBRATOR terminal.

q. Set the A and B SEC/DIV (knobs locked) to 1 ms.

r. Adjust probe compensation for the best flat top on the square-wave signal display.

s. Disconnect the probe tip from the CALIBRATOR terminal. Remove the grabber tip from the probe, unscrew and remove the plastic barrel, and connect the probe to the output of the Sine-Wave Generator via a 50 Ω termination and a Mini probe-tip-to-BNC adapter.

t. Set the A and B SEC/DIV to 50 μs (knobs locked).

u. Set the generator output for a 4-division display at the reference frequency, then change the generator frequency to 80 MHz.

v. CHECK—Signal display amplitude is 2.82 divisions or greater while sweeping the generator frequency from 80 MHz to 150 MHz.

w. Move the signal to CH 4 and set the VERTICAL MODE switches to display CH 4 only.

x. CHECK—Repeat parts p through v for CH 4.

y. Disconnect the test setup.

6. Check Common Mode Rejection Ratio (CMRR).

a. Set:

VERTICAL MODE	
CH 1, ADD, and INVERT	On (button in)
CH 2, CH 3, and CH 4	Off (buttons out)
VOLTS/DIV	
CH 1 and CH 2	10 mV
CH 1 and CH 2 VAR	In detent
Input Coupling	
CH 1 and CH 2	50 Ω DC
A and B SEC/DIV	50 μs (knobs locked)
TRIGGER	
MODE	AUTO LVL
SOURCE	CH 1

b. Connect a reference frequency signal from the Leveled Sine-Wave Generator to the CH 1 OR X and CH 2 input connectors via a 50 Ω BNC cable, a 5X attenuator, and a Dual-Input Coupler.

c. Set the generator output level for an 8-division display of the reference signal on CH 1.

d. Adjust either the CH 1 VAR control or the CH 2 VAR control for a minimum ADD display amplitude while leaving the other control in the calibrated detent (whichever provides the best CMRR).

e. Set the generator frequency to 50 MHz.

f. Set the SEC/DIV switch to 20 ns.

g. CHECK—ADD display amplitude is 0.4 division or less (discount trace width).

h. Set ADD and INVERT Off (buttons out) and rotate the CH 1 and CH 2 VAR controls CW to their calibrated detent positions.

i. Disconnect the test setup.

7. Check Channel Isolation.

a. Set:

VERTICAL MODE	
CH 1, CH 2, CH 3, and CH 4	On (buttons in)
CHOP/ALT	ALT (button out)
Input Coupling	
CH 1 and CH 2	50 Ω DC
VOLTS/DIV	
CH 1 and CH 2	0.1 V
CH 3 and CH 4	0.1 V (buttons out)
TRIGGER	
SOURCE	CH 1
A and B SEC/DIV	20 ns (knobs locked)

b. Connect the Leveled Sine-Wave Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

c. Set the generator frequency to 100 MHz and adjust the output level for an 8-division display.

d. CHECK—Amplitude of each trace other than CH 1 is 0.08 division or less (discount trace width).

e. Move the signal to the CH 2 input connector and change the TRIGGER SOURCE switch to CH 2.

f. CHECK—Amplitude of each trace other than CH 2 is 0.08 division or less (discount trace width).

g. Add a 50 Ω BNC termination to the BNC cable and move the signal to CH 3.

h. Set the TRIGGER SOURCE switch to CH 3 and adjust the generator output for a signal display amplitude of 8 divisions.

i. CHECK—Amplitude of each trace other than CH 3 is 0.16 division or less (discount trace width).

j. Move the signal to CH 4 input connector and set TRIGGER SOURCE to CH 4.

k. CHECK—Amplitude of each trace other than CH 4 is 0.16 division or less (discount trace width).

l. Connect the generator to the CH 1 OR X input connector.

m. Set the TRIGGER SOURCE switch to CH 1.

n. Set the generator output frequency to 150 MHz and the output level for an 8-division display.

o. CHECK—Amplitude of each trace other than CH 1 is 0.16 division or less (discount trace width).

p. Move the signal to the CH 2 input connector and set the TRIGGER SOURCE switch to CH 2.

q. CHECK—Amplitude of each trace other than CH 2 is 0.16 division or less (discount trace width).

r. Disconnect the test setup.

8. Set CH 1 and CH 2 DC Balance.

NOTE

For an accurate DC Balance setting, the instrument MUST be allowed to warmup for 20 minutes before performing the following steps.

a. Press up and hold both the CH 1 and CH 2 Input Coupling switches in the 1 MΩ AC position for approximately 1 second, then release them.

NOTE

At the completion of the automatic DC Balance, the Input Coupling settings will return to the states they previously held (if they were in those states for at least 7 seconds prior to performing the DC Balance procedure).

b. VERIFY—A moving dot display replaces the normal display for approximately 10 seconds (while the DC Balance levels are automatically reset), then the display returns to normal.

c. VERIFY—There is less than 0.2 division vertical trace shift between adjacent settings of the CH 1 and CH 2 VOLTS/DIV switches as they are rotated through each of their positions.

d. VERIFY—There is less than 1.0 division vertical trace shift as the CH 1 and CH 2 VOLTS/DIV VAR controls are rotated fully CCW.

e. VERIFY—There is less than 0.5 division vertical trace shift when the INVERT button is pressed in.

f. Return the VERTICAL VAR controls to their detent positions and turn the CH 2 INVERT function off (button out).

9. Check CH 2 SIGNAL OUT and Cascaded Operation.

a. Set:

VERTICAL MODE	
CH 1	On (button in)
CH 2, CH 3, and CH 4	Off (buttons out)
BW LIMIT	On (button in)
VOLTS/DIV	
CH 1 and CH 2	2 mV
Input Coupling	
CH 1	50 Ω DC
CH 2	1 MΩ DC
A and B SEC/DIV	1 ms
TRIGGER MODE	AUTO LVL
SOURCE	VERT
COUPLING	NOISE REJ

b. Connect a 1 kHz, 2 mV standard-amplitude signal from the Calibration Generator to the CH 2 input connector via a 50 Ω BNC cable.

c. Connect the CH 2 signal from the rear-panel CH 2 SIGNAL OUT connector to the CH 1 OR X input connector via a precision 50 Ω BNC cable.

d. CHECK—Display amplitude is 4.5 to 5.5 divisions (discount trace width).

e. Set CH 1 Input Coupling to GND and align the trace with the center graticule line.

f. Return CH 1 Input Coupling to 50 Ω DC.

g. Set the CH 1 VOLTS/DIV switch to 5 mV.

h. CHECK—The baseline of the display is within 2 divisions of the ground reference set above (discount trace width).

i. Set the CH 1 Input Coupling to 1 MΩ DC.

j. CHECK—Display amplitude is 3.6 to 4.4 divisions (discount trace width).

k. Disconnect the signal from the CH 2 input connector.

l. Set the CH 1 and CH 2 Input Coupling to 50 Ω DC.

m. Press and release the BW LIMIT button to turn the function off.

n. Connect a 50 kHz signal from the Leveled Sine-Wave Generator to the CH 2 input connector via a precision 50 Ω BNC cable and a 10X attenuator.

o. Set the CH 1 VOLTS/DIV switch to 2 mV.

p. Adjust the generator output level to produce a 6-division CH 1 display.

q. Increase the generator frequency to 50 MHz.

r. CHECK—Display amplitude is 4.24 divisions or greater.

s. If the following step (step 10) is to be performed, skip part t below.

t. Disconnect the test setup.

10. Check BW LIMIT Operation.

a. Set:

VERTICAL MODE	
CH 1	Off (button out)
CH 2	On (button in)
BW LIMIT	On (button in)
A and B SEC/DIV	50 μs (knobs locked)
VOLTS/DIV	
CH 2	10 mV

b. Connect the Leveled Sine-Wave Generator output to the CH 1 OR X input connector via a precision 50 Ω BNC cable.

c. Set the generator frequency to 50 kHz and adjust the output level for a 6-division display on the crt.

d. Gradually increase the generator output frequency until the display amplitude decreases to 4.24 divisions.

e. CHECK—Generator frequency is between 13 MHz to 24 MHz.

f. Turn BW LIMIT off (button out).

g. Disconnect the test setup.

TRIGGERING

Equipment Required (see Table 4-1)

Leveled Sine-Wave Generator (Item 2)
Function Generator (Item 4)
10X Probe (supplied with 2445) (Item 6)
Precision 50 Ω BNC Cable (Item 8)
50 Ω BNC Cable (2 required) (Item 9)
Dual-Input Coupler (2 required) (Item 10)
50 Ω BNC Termination (2 required) (Item 11)

Initial Control Settings.

Control settings not listed do not affect the procedure.

Set:

VERTICAL MODE	
CH 1 and CH 2	On (buttons in)
CH 3, CH 4, ADD and INVERT	Off (buttons out)
CHOP/ALT	ALT (button out)
20 MHz BW LIMIT	Off (button out)
VOLTS/DIV	
CH 1	0.1 V
CH 2	0.5 V
CH 1 and CH 2 VAR	In detent
CH 3 and CH 4	0.5 V (buttons in)
Input Coupling	
CH 1	1 MΩ DC
CH 2	50 Ω DC
A and B SEC/DIV	2 μs (knobs locked)
A and B SEC/DIV VAR	In detent
X10 MAG	Off (button out)
Δt and ΔV	Off (press and release until associated readout is off)
TRACKING	Off (button out)
TRACE SEP	Fully CW
TRIGGER	
HOLDOFF	B ENDS A (fully CW)
LEVEL	Midrange
SLOPE	+ (plus)
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC

1. Check A and B Triggers.

NOTE

The Trigger Level Readout Accuracies are checked in the Vertical Performance Checks.

a. Refer to Table 4-4 to determine what the A Trigger requirements are and at what frequencies various checks are made.

b. Using a 50 Ω BNC cable, connect one of the following test generators to the CH 1 input connector. Select the generator that produces the proper frequency range for the conditions being tested as called out in Tables 4-4 and 4-5. When using the Leveled Sine-Wave Generator, the output must be terminated into 50 Ω (either the 50 Ω input coupling or a 50 Ω termination may be used).

1. Function Generator (30 kHz and 80 kHz)

2. Leveled Sine-Wave Generator (50 MHz to 250 MHz)

NOTE

To obtain signal amplitudes less than 1 division, first set the signal for either 4, 5, or 10 times the specified amplitude; then reduce the amplitude by a factor of 4, 5, or 10 by increasing the VOLTS/DIV settings as necessary.

c. For each combination listed in the table, set the generator Test Frequency and the 2445 TRIGGER COUPLING as indicated, performing the following steps to verify the Triggering levels in each setup.

d. Set the VOLTS/DIV switch and the generator output level to obtain the test signal amplitude indicated for the particular combination being tested.

e. Set the SEC/DIV switch and the X10 MAG switch to obtain a well-defined display of the test signal.

NOTE

Normally, unless trigger sensitivity is very close to the specified limits, it is sufficient to check each of the indicated frequency-coupling combinations listed in the table in Channel 1 only; checks for Channels 2, 3 and 4 need only be done in DC COUPLING (to verify signal path).

f. CHECK—For a stably triggered display (unless otherwise indicated) for each of the Test Frequency-TRIGGER COUPLING combinations listed in Table 4-4. When testing the 250 MHz triggering, check that trigger jitter is < 50 ps (0.05 division at 10 ns/div with X10 MAG).

Table 4-4
CH 1 or CH 2 Triggering Conditions

Test Frequency	Minimum Vertical Display Levels at Which Triggering Should Occur				
	TRIGGER COUPLING				
	DC	NOISE REJ	HF REJ	LF REJ	AC
60 Hz	[a]	[a]	[a]	No Trigger, Freeruns	0.35 Div
30 kHz	[a]	[a]	0.5 Div	[a]	[a]
80 kHz	[a]	[a]	[a]	0.5 Div	[a]
50 MHz	0.35 Div	1.2 Div	No Trigger, Freeruns at 1.2 Div	0.5 Div	0.35 Div
250 MHz (trigger jitter < 50 ps)	1.0 Div	3.0 Div	No Trigger, Freeruns at 3.0 Div	1.0 Div	1.0 Div

[a]Not necessary to check.

g. Press in the ADD button to select the function and press and release the CH 1 button to turn off the CH 1 display.

h. Repeat the DC TRIGGER COUPLING tests of Table 4-4 while in the ADD mode.

i. Move the 50 MHz and 250 MHz signals to the CH 2 input connector and repeat the DC TRIGGER COUPLING tests of Table 4-4 while in ADD mode.

j. Press the CH 2 button in to select the channel and press and release the ADD button to turn off the ADD display.

k. Repeat the DC TRIGGER COUPLING tests of Table 4-4 while in CH 2 mode.

l. If trigger sensitivity is close to the specified limits given in steps c through k above, test all of the frequency-coupling combinations given in Table 4-4 for CH 2.

m. Move the test signal to CH 3 and CH 4 in turn and repeat parts c through f using Table 4-5.

Table 4-5
CH 3 or CH 4 Triggering Conditions

Test Frequency	Minimum Vertical Display Levels at Which Triggering Should Occur				
	TRIGGER COUPLING				
	DC	NOISE REJ	HF REJ	LF REJ	AC
60 Hz	[a]	[a]	[a]	No Trigger, Freeruns	0.18 Div
30 kHz	[a]	[a]	0.25 Div	[a]	[a]
80 kHz	[a]	[a]	[a]	0.25 Div	[a]
50 MHz	0.18 Div	0.6 Div	No Trigger, Freeruns at 0.6 Div	0.25 Div	0.18 Div
250 MHz (trigger jitter < 50 ps)	0.5 Div	1.5 Div	No Trigger, Freeruns at 1.5 Div	0.5 Div	0.5 Div

[a]Not necessary to check.

n. Set:

TRIGGER
MODE — AUTO
LEVEL — Fully clockwise

o. Pull the B SEC/DIV knob out and set it 1 switch setting (CW) faster than the A SEC/DIV setting, then push the B SEC/DIV knob back in.

p. Verify that the crt readout displays DLY and not Δt. If Δt is displayed, press the Δt button in and release it to select the DLY function. When DLY is displayed, rotate the ΔREF OR DLY POS control CCW until the readout display indicates zero delay. (The display will indicate DLY?, which is normal.)

q. Press the A/B TRIG button to select the B TRIGGER.

r. Set B TRIGGER MODE to TRIG AFT DLY and adjust TRIGGER LEVEL for a stable signal display.

s. Repeat parts a through m for B TRIGGER, changing the A and B SEC/DIV and X10 MAG switches as required to maintain a well-defined display.

t. Disconnect the test setup.

2. Check Composite Triggering.

a. Set:

VERTICAL MODE	
CH 1, CH 2, CH 3, and CH 4	On (buttons in)
ADD	Off (button out)
CHOP/ALT	ALT (button out)
Input Coupling	
CH 1	50 Ω DC
CH 2	1 MΩ DC
TRIGGER	
A/B TRIG	A
MODE	NORM
SOURCE	VERT
COUPLING	DC
A and B SEC/DIV	10 μs

b. Connect the Function Generator to the CH 1 and CH 2 inputs via a 50 Ω BNC cable and a Dual-Input Coupler.

c. Set the Function Generator for a 50 kHz, 1.35-division display for CH 1 and CH 2.

d. Connect the Leveled Sine-Wave Generator to the CH 3 and CH 4 input connectors using a 50 Ω BNC cable, a 50 Ω termination and a Dual-Input Coupler.

e. Set the generator output level for a 50 kHz, 0.7-division display for CH 3 and CH 4.

f. CHECK—Display will trigger as the TRIGGER LEVEL control is rotated through its range.

g. Pull the B SEC/DIV knob out, rotate it to 5 μs, and push it back in.

h. Press the A/B TRIG button and set the B TRIGGER MODE to TRIG AFT DLY.

i. Rotate the ΔREF OR DLY POS control CCW until the delay readout indicates DLY? 0.00 μs.

j. CHECK—Display will trigger as the TRIGGER LEVEL control is rotated through its range.

k. Rotate the B SEC/DIV knob back to 10 μs (knobs locked).

l. Disconnect the test setup.

3. Check Trigger Noise Rejection—All Channels.

a. Set:

VERTICAL MODE	
CH 1	On (button in)
Input Coupling	
CH 1 and CH 2	1 MΩ DC
VOLTS/DIV	
CH 1	10 mV
CH 2	0.1 V
CH 3 and CH 4	0.1 V (buttons out)
A and B SEC/DIV	10 μs (knobs locked)
TRIGGER	
MODE	AUTO LVL
SOURCE	VERT

b. Connect the Function Generator to the CH 1 input via a 50 Ω BNC cable, a 50 Ω termination, and a 10X attenuator.

c. Set the Function Generator output frequency and level for a 50-kHz, 4-division display.

d. Set the CH 1 VOLTS/DIV switch to 0.1 V.

e. Set the TRIGGER COUPLING switch to NOISE REJ.

f. CHECK—Display will not trigger (freeruns).

g. Pull the B SEC/DIV knob out, rotate it to 5 μs and push it back in.

h. Press the A/B TRIG button to select the B TRIGGER.

i. Set the TRIGGER MODE switch to B TRIG AFT DLY.

j. CHECK—Display will not trigger for any setting of the LEVEL control.

k. Rotate the B SEC/DIV switch back to 10 μs (knobs locked).

l. Move the input signal to CH 2, CH 3, and CH 4 in turn, selecting each channel as the display source. Repeat parts f through k for each channel.

4. Check Slope Selection and Verify Line Trigger.

a. Set:

A and B SEC/DIV	2 ms (knobs locked)
X10 MAG	Off (button out)
TRIGGER	
MODE	AUTO
SOURCE	LINE
COUPLING	AC
VOLTS/DIV	
CH 1	5 V
Input Coupling	
CH 1	1 MΩ DC

CAUTION

In the next part, DO NOT connect the probe ground lead to the ac power source.

b. Attach the 10X probe to the CH 1 OR X input connector and connect the probe tip to the ac power source.

c. CHECK—Display can be triggered in both the + (plus) and − (minus) positions of the SLOPE switch using the TRIGGER LEVEL control and that the displayed slope agrees with the selected slope.

d. CHECK—Display phase shifts slightly as the TRIGGER COUPLING switch is changed from AC to DC.

e. Disconnect the test setup.

HORIZONTAL

Equipment Required (see Table 4-1)

Leveled Sine-Wave Generator (Item 2)
Calibration Generator (Item 3)
Time-Mark Generator (Item 5)
Precision 50 Ω BNC Cable (Item 8)

Initial Control Settings.

Control settings not listed do not affect the procedure.

Set:	
VERTICAL MODE	
CH 1	On (button in)
CH 2, CH 3, CH 4, ADD, and INVERT	Off (buttons out)
CHOP/ALT	ALT (button out)
20 MHz BW LIMIT	Off (button out)
VOLTS/DIV	
CH 1	0.5 V
CH 1 VAR	In detent
CH 3 and CH 4	0.1 V (buttons out)
Input Coupling	
CH 1	50 Ω DC
A and B SEC/DIV	200 ns (knobs locked)
A and B SEC/DIV VAR	In detent
X10 MAG	Off (button out)
ΔV and Δt	Off (press and release until associated readout is off)
TRACKING	Off (button out)
TRACE SEP	Fully CW
TRIGGER	
HOLDOFF	B ENDS A
LEVEL	Midrange
SLOPE	+ (plus)
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC

1. Check Horizontal Display Modes (A, A INTEN, ALT, and B).

a. Use a 50 Ω BNC cable to connect 200 ns time markers from the Time-Mark Generator to the CH 1 OR X input connector.

b. Adjust the TRIGGER LEVEL control as necessary for a stable signal display.

c. Pull the B SEC/DIV knob out and set the B TRIGGER MODE to RUN AFT DLY.

d. Set the ΔREF OR DLY control for a DLY readout of approx 1000 ns.

e. VERIFY—An intensified zone appears on the displayed signal near graticule center.

f. Rotate the ΔREF OR DLY POS control to center the intensified zone on one of the time markers near graticule center.

g. Set the B SEC/DIV control to 50 ns (knob out).

h. Rotate the TRACE SEP control CCW to separate the the A and B sweep displays.

i. CHECK—The B sweep is displayed with the A sweep.

j. Push the B SEC/DIV knob in.

k. CHECK—Only the B sweep is displayed.

2. Check A and B Timing, A Cursor Accuracies, and A Cursor Range.

a. Set:

A and B SEC/DIV	5 ns (knobs locked)
TRACE SEP	Fully CW
Δt	On (press and release for Δt display)

b. Select 5 ns time markers from the Time-Mark Generator and adjust the TRIGGER LEVEL control for a stable display.

c. Use the Horizontal POSITION control to align the 2nd time marker with the 2nd vertical graticule line (2nd from the left edge of the display).

NOTE

The 2 ns and the 5 ns time markers are sinusodial. Use either the rising or falling zero-crossings as alignment points.

d. Align the ΔREF cursor with the 2nd time marker and align the Δ cursor with the 10th time marker.

e. CHECK—The A Sweep timing and cursor readout accuracies are within the limits given in Tables 4-6 and 4-7.

NOTE

If the 2nd and 10th time markers are within ±0.06 division of the 2nd and 10th vertical graticule lines for unmagnified sweeps and within ±0.1 division for magnified sweeps, the sweep timing accuracy is conservatively within limits. When the timing accuracy is checked at each sweep speed, note any SEC/DIV setting at which the timing error exceeds the 0.6-division limit. Check these sweep speeds against the major-division time-interval limits given in Table 4-7.

NOTE

For A and B SEC/DIV switch settings of 10 ns, the time-marker period is greater than 1 division when the sweep is magnified. At 1 ns per division, 1 ns per division (SEC/DIV setting of 10 ns with X10 MAG), check for 4 cycles between the 2nd and 10th vertical graticule lines (±0.1 division).

f. Repeat parts c, d, and e for each A SEC/DIV-time marker combination given in Table 4-6 for both unmagnified and magnified sweeps.

Table 4-6
Settings for A and B Timing Accuracy Checks and A Cursor Accuracy Limits

A and B SEC/DIV Switch	Unmagnified		X10	
	Time Markers	Limits of Δt Cursor Readout	Time Markers	Limits of Δt Cursor Readout
10 ns	10 ns	79.30 ns to 80.70 ns	2 ns 2 Div/cycle	7.89 ns to 8.11 ns (4 cycles)
20 ns	20 ns	158.60 ns to 161.40 ns	2 ns	15.78 ns to 16.22 ns
50 ns	50 ns	396.5 ns to 403.5 ns	5 ns	39.45 ns to 40.55 ns
0.1 μs	0.1 μs	793.0 ns to 807.0 μs	10 ns	78.90 ns to 81.10 ns
0.2 μs	0.2 μs	1586.0 ns to 1614.0 ns	20 ns	157.80 ns to 162.20 ns
0.5 μs	0.5 μs	3965 ns to 4035 ns	50 ns	394.5 ns to 405.5 ns
1 μs	1 μs	7.930 μs to 8.070 μs	0.1 μs	789.0 ns to 811.0 ns
2 μs	2 μs	15.860 μs to 16.140 μs	0.2 μs	1578.0 ns to 1622.0 ns
5 μs	5 μs	39.65 μs to 40.35 μs	0.5 μs	3945 ns to 4055 ns
10 μs	10 μs	79.30 μs to 80.70 μs	1 μs	7.890 μs to 8.110 μs
20 μs	20 μs	158.60 μs to 161.40 μs	2 μs	15.780 μs to 16.220 μs
50 μs	50 μs	396.5 μs to 403.5 μs	5 μs	39.45 μs to 40.55 μs
0.1 ms	0.1 ms	793.0 μs to 807.0 μs	10 μs	78.90 μs to 81.10 μs
0.2 ms	0.2 ms	1586.0 μs to 1614.0 μs	20 μs	157.80 μs to 162.20 μs
0.5 ms	0.5 ms	3965 μs to 4035 μs	50 μs	394.5 μs to 405.5 μs
1 ms	1 ms	7.930 ms to 8.070 ms	0.1 ms	789.0 μs to 811.0 μs
2 ms	2 ms	15.860 ms to 16.140 ms	0.2 ms	1578.0 μs to 1622.0 μs
5 ms	5 ms	39.65 ms to 40.35 ms	0.5 ms	3945 μs to 4055 μs
10 ms	10 ms	79.30 ms to 80.70 ms	1 ms	7.890 ms to 8.110 ms
20 ms	20 ms	158.60 ms to 161.40 ms	2 ms	15.780 ms to 16.220 ms
50 ms	50 ms	396.5 ms to 403.5 ms	5 ms	39.45 ms to 40.55 ms
A SEC/DIV ONLY	(B Sweep does not have these sweep speeds)			
0.1 s	0.1 s	793.0 ms to 807.0 ms	10 ms	78.90 ms to 81.10 ms
0.2 s	0.2 s	1578.0 ms to 1622.0 ms	20 ms	157.00 ms to 163.00 ms
0.5 s	0.5 s	3945 ms to 4055 ms	50 ms	392.5 ms to 407.5 ms

Table 4-7
Horizontal Timing Accuracy Checked Against the Graticule

Over Any

	1 Div	2 Div	3 Div	4 Div	5 Div	6 Div	7 Div	8 Div	9 Div	10 Div
Time-marker Accuracy (X10 MAG off) Should Be	± 0.07 Div	± 0.07 Div	± 0.08 Div	± 0.09 Div	± 0.10 Div	± 0.10 Div	± 0.11 Div	± 0.12 Div	± 0.12 Div	± 0.13 Div
—or—										
(with X10 MAG on)	± 0.07 Div	± 0.08 Div	± 0.1 Div	± 0.11 Div	± 0.12 Div	± 0.13 Div	± 0.14 Div	± 0.16 Div	± 0.17 Div	± 0.18 Div
As Measured Against These Time-Marker Pairs	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9	1-10	1-11
	2-3	2-4	2-5	2-6	2-7	2-8	2-9	2-10	2-11	
	3-4	3-5	3-6	3-7	3-8	3-9	3-10	3-11		
	4-5	4-6	4-7	4-8	4-9	4-10	4-11			
	5-6	5-7	5-8	5-9	5-10	5-11				
	6-7	6-8	6-9	6-10	6-11					
	7-8	7-9	7-10	7-11						
	8-9	8-10	8-11							
	9-10	9-11								
	10-11									

g. Rotate the ΔREF OR DLY POS control CCW until the cursor stops moving.

h. CHECK—ΔREF cursor aligns with the 1st graticule line within ±0.2 division.

i. Rotate the Δ control CW until the cursor stops moving.

j. CHECK—Δ cursor aligns with the 11th graticule line within ±0.2 division.

k. Set the A and B SEC/DIV switches to 10 ns.

l. Rotate the ΔREF OR DLY and the Δ controls to precisely superimpose the cursors near the 2nd graticule line.

m. CHECK—Δt readout indicates a difference of 0.30 ns or less.

n. Rotate the ΔREF OR DLY and the Δ controls to precisely superimpose the cursors near the 10th graticule line.

o. CHECK—Δt readout indicates a difference of 0.30 ns or less.

p. Set:

B SEC/DIV	10 ns (knob in)
B TRIGGER MODE	RUN AFT DLY
X10 MAG	Off (button out)
Δt	Off (DLY)
ΔREF OR DLY POS	Set for zero delay

q. CHECK—The B sweep timing accuracy as in parts b through f, making sure that the A SEC/DIV switch is set slower than the B SEC/DIV switch. Disregard the cursor accuracy data.

3. Check Delta Time Accuracy using the Delayed Sweep.

a. Set:

A SEC/DIV	20 ns
B SEC/DIV	10 ns (knob in)

X10 MAG	On (button in)
Δt	Off (DLY readout)
TRIGGER	
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC
SLOPE	+ (plus)
LEVEL	As required for a stable display
B TRIG MODE	RUN AFT DLY

NOTE

Certain time marks from the TG 501 (and other Time-Mark Generators) will vary in width and may be displace in time. This will happen in a repeatable sequence and is caused by the loading and interaction of the 2, 5, and 10 dividers. This is most noticable with 10 ns, 20 ns, and 50 ns markers. The following procedure will use the above markers to set up the proper references but the 5 ns markers will be used to make the actual measurement. Close inspection of apparent jitter or mistrigger of the time marks will show the trigger point to be stable with the apparent jitter to be variable with unique combinations of trigger holdoff and sweep speed. This is normal behavior with this type of signal and is not an instrument defect.

It is not necessary to count the number of marks given in the tables. Switching to 10 ns, 20 ns, or 50 ns markers as required and then to 5 ns will show the proper 5 ns mark to be used.

b. Set the Time-Mark Generator for 20 ns markers. Adjust the Vertical VOLTS/DIV as required for a display of 3 to 6 divisions.

c. Adjust the Δ REF OR DLY POS control for a readout display of DLY 21.25 ns.

d. Adjust the Horizontal POSITION control CCW until the cursor stops moving, then CW to display the leading edge of the 2nd time marker near the graticule center. This becomes the reference point for the following procedure. Set the Time-Mark Generator to 5 ns and adjust the Vertical VOLTS/DIV and Trigger LEVEL as required.

e. Press and release the Δt button to obtain the Δt display and rotate the Δ control for a readout display of Δt −20.0 ns. If the time marks are not superimposed, adjust the Δ control to do so.

f. CHECK—Δt readout is within the limits listed in Table 4-8 for the 1st 5 ns time marker; then check that the 4th through 36th time markers are within the given limits as the Δ control is rotated CW to superimpose each successive time marker on the reference time marker.

Table 4-8
Delta Time Display Accuracy

Time-Marker Period and A SEC/DIV Switch Setting	B SEC/DIV Switch Setting	Marker Superimposed using the Δ (Delta) Control	Delta Time Readout Accuracy Limits
20 ns	1 ns[a]	1st	−19.25 ns to 20.25 ns
		4th	−0.20 ns to 0.20 ns
		8th	19.25 ns to 20.25 ns
		12th	39.70 ns to 40.30 ns
		16th	59.60 ns to 60.40 ns
		20th	79.55 ns to 80.45 ns
		24th	99.50 ns to 100.50 ns
		28th	119.45 ns to 120.55 ns
		32nd	139.40 ns to 140.60 ns
		36th	159.30 ns to 160.70 ns
50 ns	1 ns[a]	1st	−49.3 ns to −50.7 ns
		20th	49.3 ns to 50.7 ns
		90th	398.3 ns to 401.70 ns

[a]**10 ns with X10 MAG on (button in).**

g. Set:

A SEC/DIV	50 ns
Δt	Off (DLY readout)

h. Set the Time-Mark Generator for 50 ns time markers and adjust the ΔREF OR DLY POS control for a readout display of 53.2 ns.

i. Position the leading edge of the 1st time marker near graticule center using the Horizontal POSITION control. Set the Time-Mark Generator to 5 ns and adjust the Vertical VOLTS/DIV and Trigger LEVEL as required.

j. Press and release the Δt button to obtain a Δt display and adjust the Δ control for a readout display of Δt −50.00 ns. If the time markers are not superimposed, adjust the Δ control to do so.

k. CHECK—Δt readout is within the limits listed in Table 4-8 for the 1st 5 ns time marker; then check that the 30th and 100th time markers are within the given limits as the Δ control is rotated CW to superimpose each time marker on the reference time marker.

l. Set:

TRACKING/INDEP	TRACKING (button in)
A SEC/DIV	0.1 μs
B SEC/DIV	10 ns (knob out)
X10 MAG	On (button in)

m. Select 0.1 μs time markers from the Time-Mark Generator.

n. Adjust the Δ and ΔREF OR DLY POS controls for a Δt readout display of Δt 800.0 ns.

o. Adjust the Horizontal POSITION control to align the leading edge of the 2nd time marker on the A sweep with the 2nd vertical graticule line.

p. Rotate the TRACE SEP control CCW to separate the traces.

q. Adjust the ΔREF OR DLY POS control to intensify the 2nd and 10th time markers (of the A sweep) and display the leading edges of the displayed B sweep time markers in the center area of the graticule.

r. VERIFY—The horizontal distance between the leading edges of the B sweep time markers is within the conservative guideline listed in Table 4-9. If this guideline is met, accuracy between each marker is ensured, and the following CHECK step need not be performed.

s. CHECK—The horizontal distance between the leading edges of the B sweep time markers is within the specified limits given in Table 4-9. The limit given is for separation between the 2nd and 10th marker; however, separation between the 2nd marker and each suceeding marker should also be checked, calculating the limits from the specification as listed at the top of the table.

t. Repeat part r (and s if necessary) for each combination of A SEC/DIV, B SEC/DIV, and X10 MAG settings listed in Table 4-9. The Δt readout should be set to indicate eight times the A SEC/DIV setting. At the slowest sweep speeds, the B SEC/DIV knob will need to be pushed in (B Sweep only) to increase the display repetition rate.

4. Check Delay Jitter.

a. Set:

TRACKING	Off (button out)
A SEC/DIV	1 ms
B SEC/DIV	0.5 μs (knob out)

b. Select 1 ms time markers from the Time-Mark Generator.

c. Align the intensified zones with the 10th time marker using the ΔREF OR DLY POS and Δ controls. Superimpose the zones to obtain a Δt readout display of 0.000 ms.

d. Push in the B SEC/DIV knob and adjust TRACE SEP to separate the traces.

e. CHECK—For 0.8 division or less of horizontal jitter on the rising edge of both time markers.

Table 4-9
Delayed Sweep Delta Time Accuracy

A SEC/DIV and Time Markers	B SEC/DIV as Displayed on Readout	Displayed Separation of Delayed Time Markers (for 2nd and 10th markers)	
		Conservative Guideline (divisions)	Specified Limit: (±0.3% time) interval +0.1% of full scale (divisions)
0.1 μs	1 ns[a]	2.4	3.4
0.2 μs	2 ns[a]	2.4	3.4
0.5 μs	5 ns[b]	2.4	3.4
1 μs	10 ns	2.4	3.4
2 μs	20 ns	2.4	3.4
5 μs	50 ns	2.4	3.4
10 μs	100 ns	2.4	3.4
20 μs	200 ns	2.4	3.4
50 μs	500 ns	2.4	3.4
0.1 ms	1 μs	2.4	3.4
0.2 ms	2 μs	2.4	3.4
0.5 ms	5 μs	2.4	3.4
1 ms	10 μs	2.4	3.4
2 ms	20 μs	2.4	3.4
5 ms	50 μs	2.4	3.4
10 ms	100 μs	2.4	3.4
20 ms	200 μs	2.4	3.4
50 ms	500 μs	2.4	3.4
0.1 s	1 ms	2.4	3.4
0.2 s	2 ms	6.4	7.4
0.5 s	5 ms	6.4	7.4

[a] X10 MAG On (button in).

[b] For remainder of Table, turn X10 MAG off.

5. Check A and B SEC/DIV VAR Range and Accuracy.

a. Set:

A and B SEC/DIV	10 μs (knobs locked)
A and B SEC/DIV VAR	In detent

Δt	Off (press and release to eliminate Δt readout)

b. Select 10 μs time markers from the Time-Mark Generator and adjust the Time-Mark Generator variable timing control for exactly 1 time marker per division. Note the variable timing % error on the Time-Mark Generator.

c. Adjust the SEC/DIV VAR control for a sweep-speed readout (on bottom line) of 20 μs and adjust the Time-Mark Generator variable timing control for exactly 2 time markers per division.

d. CHECK—The Time-Mark Generator variable timing % of error has changed 2% or less from the reading noted in part b.

e. Adjust the SEC/DIV VAR control fully CCW.

f. CHECK—Sweep speed readout displays 30.0 μs.

g. Set the Time-Mark Generator variable timing control for exactly 3 time markers per division.

h. CHECK—The Time-Mark Generator variable timing % of error has changed 2% or less from the reading noted in part b.

i. Set:

A SEC/DIV	50 μs
B SEC/DIV	10 μs (knob in)
SEC/DIV VAR	CW (in detent)
Δt	Off (DLY readout)
ΔREF OR DLY POS	Zero delay
B TRIGGER MODE	RUN AFT DLY

j. Repeat parts b through h for the B Sweep.

k. Rotate the SEC/DIV VAR control CW to the detent position and disconnect the test setup.

6. Check X-Axis Gain.

a. Set:

VERTICAL MODE	
CH 2	On (button in)
CH 1, CH 3, CH 4, ADD, and BW LIMIT	Off (buttons out)
A and B SEC/DIV	X-Y (knobs locked)
VOLTS/DIV	
CH 1 and CH 2	10 mV
Input Coupling	
CH 1	1 MΩ DC
CH 2	1 MΩ GND

b. Connect a 50 mV standard-amplitude signal from the Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

c. CHECK—Signal display amplitude is 4.9 to 5.1 horizontal divisions.

d. Disconnect the test setup.

7. Check X-Axis Bandwidth.

a. Set the CH 1 Input Coupling to 50 Ω DC.

b. Connect a 50 kHz signal from the Leveled Sine-Wave Generator to the CH 1 OR X input connector via a precision 50 Ω BNC cable.

c. Set the generator output for a 6-division horizontal display.

d. Change the generator frequency to 3 MHz.

e. CHECK—Signal display is ⩾ 4.2 horizontal divisions.

8. Check X-Y Phase Differential.

a. Set the Leveled Sine-Wave Generator for a 1 MHz, 6-division horizontal display.

b. Press and release the CH 2 VERTICAL MODE switch (CH 2 off). CH 1 displays automatically.

c. Use the CH 1 VERTICAL POSITION control to vertically center the display on the graticule.

d. CHECK—Elipse opening is 0.1 division or less, measured horizontally.

e. Press in the CH 2 VERTICAL MODE switch (CH 2 on).

f. Set the generator for a 2 MHz, 6-division horizontal display.

g. Press and release the CH 2 VERTICAL MODE switch (CH 2 off).

h. CHECK—Elipse opening is 0.3 division or less, measured horizontally.

i. Press in the CH 2 VERTICAL MODE switch (CH 2 on).

9. Check X-Axis Low-Frequency Linearity.

a. Set the Leveled Sine-Wave Generator and the CH 1 POSITION control for a 50 kHz, 2-division horizontal display centered on the graticule.

b. Use the CH 1 POSITION control to align the left edge of the signal with the left side vertical graticule line.

c. CHECK—Signal display is 1.8 to 2.2 divisions, measured horizontally.

d. Use the CH 1 POSITION control to position the right edge of the signal on the right side vertical graticule line.

e. CHECK—Signal display is 1.8 to 2.2 divisions, measured horizontally.

f. Disconnect the test setup.

CALIBRATOR, EXTERNAL Z-AXIS AND GATE OUTPUTS

Equipment Required (see Table 4-1)

Calibration Generator (Item 3)
Time-Mark Generator (Item 5)
Oscilloscope with 10X Probe (Item 6)
50 Ω BNC T-Connector (Item 7)
50 Ω BNC Cables (2 required) (Item 9)

Initial Control Settings.

Control settings not listed do not affect the procedure.

Set:

VERTICAL MODE	
CH 1 and CH 2	On (buttons in)
CH 3, CH 4, ADD, and INVERT	Off (buttons out)
CHOP/ALT	CHOP (button in)
20 MHz BW LIMIT	Off (button out)
VOLTS/DIV	
CH 1 and CH 2	0.1 V
CH 1 and CH 2 VAR	In detent
Input Coupling	
CH 1	1 MΩ DC
CH 2	50 Ω DC
A and B SEC/DIV	1 ms (knobs locked)
A and B SEC/DIV VAR	In detent
X10 MAG	Off (button out)
ΔV and Δt	Off (press and release until associated readout is off)
TRIGGER	
HOLDOFF	B ENDS A (fully CW)
LEVEL	Midrange
SLOPE	+ (plus)
MODE	AUTO LVL
SOURCE	CH 1
COUPLING	DC

1. Check CALIBRATOR Repetition Rate.

NOTE

Refer to the Adjustment Procedure to check the accuracy of the CALIBRATOR output levels.

a. Connect a 10X probe from the CALIBRATOR terminal to the CH 1 OR X input connector.

b. Connect 1 ms time markers from the Time-Mark Generator to the CH 2 input connector via a 50 Ω BNC cable.

c. Adjust the CH 2 VOLTS/DIV switch for several divisions of marker display.

d. CHECK—Horizontal drift for any time marker is 1 division or less per second (10 seconds or more for 1 marker to drift 10 horizontal divisions).

e. Set the CH 2 VERTICAL MODE switch to Off (button out).

f. CHECK—1 cycle is displayed per 2 horizontal divisions for each position of the A SEC/DIV switch from 0.1 s to 0.1 μs.

g. Disconnect the test setup.

2. Check External Z-Axis Operation.

a. Set:

INTENSITY	Fully clockwise
A and B SEC/DIV	1 ms
VOLTS/DIV	
CH 1	0.5 V

b. Connect a 1 kHz, 2 V standard-amplitude signal from the Calibration Generator to the CH 1 OR X input connector and the rear-panel EXT Z-AXIS input connector using a 50 Ω BNC T-Connector and two 50 Ω BNC cables.

c. CHECK—The positive portion of the 4-division signal display is blanked out.

d. Disconnect the test setup and adjust the crt INTENSITY as desired.

3. Check A and B GATE Outputs and Verify TRIGGER HOLDOFF.

a. Set:

A SEC/DIV	100 μs
B SEC/DIV	50 μs (knob in)
Δt	Off (DLY readout)
ΔREF OR DLY POS	Zero DLY readout
TRIGGER	
MODE	AUTO
HOLDOFF	Minimum (CCW)

b. Connect a test oscilloscope to the A GATE OUT connector (located on the 2445 rear panel) via a 50 Ω BNC cable.

c. CHECK—Test oscilloscope displays a signal with a high level between 2.4 V and 5 V and a low level between 0 V and 0.4 V.

d. VERIFY—Duration of the high level is between 1 ms and 1.2 ms.

e. VERIFY—Duration of the low level is between 80 μs and 150 μs.

f. VERIFY—Duration of the low level increases to at least 10 times the time measured in part e when the 2445 HOLDOFF control is rotated to the maximum CW position (but not in the detent).

g. Move the 50 Ω BNC cable from the A GATE OUT connector to the B GATE OUT connector.

h. CHECK—Test oscilloscope displays a signal with a high level between 2.4 V and 5 V and a low level between 0 V and 0.4 V.

i. VERIFY—Duration of the high portion of the signal is between 500 μs and 600 μs.

j. Disconnect the test setup.

ADDITIONAL FUNCTIONAL VERIFICATION

Equipment Required (see Table 4-1)

10X Probe supplied with Oscilloscope (Item 6)

Initial Control Settings.

Control settings not listed do not affect the procedure.

Set:

VERTICAL MODE	
CH 1, CH 2, CH 3, CH 4, ADD, and INVERT	Off (buttons out)
CHOP/ALT	ALT (button out)
20 MHz BW LIMIT	Off (button out)
VOLTS/DIV	
CH 1 and CH 2	0.1 V
CH 1 and CH 2 VAR	In detent
CH 3 and CH 4	0.1 V (buttons out)
Input Coupling	
CH 1 and CH 2	1 MΩ DC
A and B SEC/DIV	1 ms (knobs locked)
A and B SEC/DIV VAR	In detent
X10 MAG	Off (button out)
ΔV and Δt	Off (press and release until associated readout is off)
TRACKING	Off (button out)
TRACE SEP	Fully CW
TRIGGER	
HOLDOFF	B ENDS A (fully CW)
LEVEL	Midrange
SLOPE	+ (plus)
A/B TRIG Select	A
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC

1. Verify ALT, CHOP, and ADD Modes and TRACE SEP.

a. VERIFY—CH 1 trace is visible with no VERTICAL MODE buttons selected (all out).

b. Press the CH 2 VERTICAL MODE button in.

c. VERIFY—CH 1 trace is not displayed and the CH 2 trace is displayed.

d. Press the CH 1 VERTICAL MODE button in.

NOTE

Separate the traces by approximately 1 division using the VERTICAL POSITION controls. Do not position either trace precisely at graticule center.

e. VERIFY—Both the CH 1 and the CH 2 traces are displayed.

f. Press in the ADD button.

g. VERIFY—A third trace (ADD) is displayed.

h. Press in the CH 3 VERTICAL MODE button.

i. VERIFY—The CH 3 trace is added to the display.

j. Press in the CH 4 VERTICAL MODE button.

k. VERIFY—The CH 4 trace is added to the display.

l. Set the A and B SEC/DIV controls to 50 ms (knobs locked).

m. VERIFY—5 traces are alternately displayed in the following sequence: CH 1, CH 2, ADD, CH 3, CH 4.

n. Set the TRIGGER MODE switch to SGL SEQ.

o. VERIFY—After the current sequence of traces is complete, no further traces are displayed.

p. Set the TRIGGER SOURCE switch to LINE.

q. Press down and release the TRIGGER MODE switch.

r. VERIFY—Each time the TRIGGER MODE switch is pressed down and released, the 5 signal traces appear once (in sequence), the readout display flashes once and the scale illumination flashes on and off.

s. Set the TRIGGER MODE switch to AUTO LVL and press the CHOP button in.

t. VERIFY—The 5 traces appear to be displayed simultaneously.

u. Set:

TRIGGER SOURCE	CH 4
A SEC/DIV	20 μs
B SEC/DIV	10 μs (knob out and rotated)
CHOP/ALT	ALT (button out)
TRACE SEP	CCW until traces are separated

v. VERIFY—An alternate B sweep trace appears for each A sweep trace (10 traces total).

2. Verify BEAM FIND Operation.

a. Set:

A and B SEC/DIV	1 ms (knobs locked)
VERTICAL MODE	
CH 1	On (button in)
CH 2, CH 3, CH 4 and ADD	Off (buttons out)
X10 MAG	On (button in)
Horizontal POSITION	Midrange
Vertical POSITION	Midrange

b. Press and hold the BEAM FIND button in.

c. VERIFY—The trace is less than 10 divisions long and remains in the graticule area as the CH 1 POSITION control and the Horizontal POSITION control are rotated through their complete ranges.

d. Release the BEAM FIND button and set the VERTICAL POSITION and Horizontal POSITION controls to midrange.

3. Check Probe Encoding.

NOTE

Refer to Figure 2-8, Readout Display Locations, for the positioning of the readout display information.

a. Set:

VOLTS/DIV	
CH 1, CH 2, CH 3, and CH 4	0.1 V

b. Connect the standard accessory 10X probe (encoded) to the CH 1 input connector.

c. CHECK—CH 1 readout changes from 100 mV to 1 V.

d. Move the probe to CH 2 and repeat part c for that channel.

e. Move the probe to CH 3.

f. CHECK—Readout changes from 0.1 to 1.

g. Move the probe to CH 4 and repeat part f for that channel.

h. Disconnect test setup.

ADJUSTMENT PROCEDURE

INTRODUCTION

IMPORTANT—PLEASE READ BEFORE USING THIS PROCEDURE

The "Adjustment Procedure" is used to restore optimum performance or return the instrument to conformance with its "Performance Requirements" as listed in the "Specification" (Section 1). As a general rule, these adjustments should be performed every 2000 hours of operation or once a year if used infrequently.

PARTIAL PROCEDURES

This procedure is divided into subsections to permit calibration of individual sections of the instrument whenever complete instrument calibration is not required. To perform a partial procedure, first set the instrument as directed in the Initial Setup Conditions at the beginning of the section, then make any changes called for within the procedure. Perform all steps within a subsection, both in the sequence presented and in their entirety to ensure that control settings will be correct for the following steps.

The adjustments in CAL 01, 02, 03, and 04 should be performed in numerical sequence, i.e., CAL 01 should be done before CAL 02, CAL 02 should be done before CAL 03, etc. Performing partial procedures when setting the automatic calibration constants (i.e. only one or two of the CAL steps) is not recommended and should only be done if the calibration constants set in the preceding steps are known to be correct.

BEFORE YOU BEGIN:

NOTE

When performing any of the automatic calibration routines (CAL 01 through CAL 04), the CAL/NO CAL jumper P501 must be moved to its CAL position (between pins 1 and 2) before turning the power on. When the desired calibration has been performed, return the jumper to its NO CAL position.

a. Turn instrument Power on.

NOTE

The instrument MUST have a 20-minute warmup period before making any adjustments. Performing the adjustment procedure while the temperature is drifting may cause erroneous calibration settings.

POWER SUPPLIES

Equipment Required (see Table 4-1)

Oscilloscope With 10X P6131 Probe (Item 6)
Digital Multimeter (Item 18)
Alignment Tool (Item 19)
1X Probe (Item 20)

See ADJUSTMENT LOCATIONS 1 *and* ADJUSTMENT LOCATIONS 4 *at the rear of this manual for test point and adjustment locations.*

NOTE

If the instrument displays "DIAGNSTIC. PUSH A/B TRIG TO EXIT" at power on, one of the power-up tests has failed. If the error message on the bottom line of the display is "TEST 04 FAIL xx" where "xx" is 01, 10 or 11, stored calibration data is in error, and the instrument should be recalibrated. If this is the case, pressing the A/B TRIG button will force entry to the normal operating mode; however, the accuracy of any measurement taken could be in error.

If any other error message occurs, the failure is probably not related to calibration. In this case, the instrument should be repaired before attempting calibration.

Initial Control Settings.

Controls settings not listed will not affect the procedure.

VERTICAL VOLTS/DIV	
CH 2	0.1 V
CH 3 and CH 4	0.1 V (buttons out)
CH 1 and CH 2 VAR	In detent
Input Coupling	
CH 1 and CH 2	1 MΩ DC
VERTICAL MODE	
CH 1	On (button in)
CH 2, CH 3, and CH 4	Off (buttons out)
ADD, INVERT, and BW LIMIT	Off (buttons out)
ALT/CHOP	ALT (button out)
VERTICAL POSITION	Midrange
A and B SEC/DIV	X-Y (knobs locked)
A and B SEC/DIV VAR	In detent
Horizontal POSITION	Midrange
TRIGGER	
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC
SLOPE	+ (plus)
LEVEL	Midrange
HOLDOFF	In detent
ΔV and Δt	Off (press and release until readout display disappears
INTENSITY	Visible display
READOUT INTENSITY	Visible display (CCW from MIN)
SCALE ILLUM	Fully CCW
FOCUS	Defocused dot

1. Check/Adjust Power Supply DC Levels, Regulation, and Ripple (R1292).

a. Connect the Digital Multimeter (DMM) negative lead to chassis ground. Connect the positive lead to the first test point listed in Table 5-1 (all test points are on the Main Board).

b. CHECK—That the reading is within the limits given in Table 5-1.

c. ADJUST—Volt Ref Adj (R1292) for a DMM reading of precisely 10.00 V. The adjustment is accessable through a hole in the top cover plate.

Table 5-1
Power Supply Voltage and Ripple Tolerances

Power Supply	Test Point (+ Lead)	Reading	Total p-p Ripple	p-p Ripple at Two Times Line Frequency
+10 V	J119-4	+ 9.99 to +10.01	100 mV	1 mV
+87 V	J119-8	+85.26 to +88.74	80 mV	5 mV
+42.4 V	J119-9	+41.55 to +43.25	80 mV	2 mV
+15 V	J119-6	+14.775 to +15.225	15 mV	11mV
Digital +5 V	J119-2	+4.85 to +5.15	150 mV	30 mV
Analog +5 V	J119-12	+4.925 to +5.075	15 mV	1 mV
−5 V	J119-5	−4.965 to −5.035	15 mV	1 mV
−8 V	J119-11	−7.88 to −8.12	100 mV	1 mV
−15 V	J119-1	−14.775 to −15.225	10 mV	2 mV

d. Repeat parts a and b for the other test points listed in Table 5-1.

e. Disconnect the DMM.

f. Set the test oscilloscope as follows:

Sweep Speed	5 ms/div
Input Coupling CH 1	1 MΩ AC
Vertical controls	To display CH 1
Trigger controls	Line source, triggered display
Volts/Division	2 mV
BW Limit	20 MHz (button in)

g. Using a 1X probe, connect the test oscilloscope probe ground lead to chassis ground. Connect the probe tip to the first test point listed in Table 5-1.

h. CHECK—Ripple at two times the line frequency and the total peak-to-peak ripple do not exceed the values given in Table 5-1.

i. Repeat part h for each test point in Table 5-1.

j. Disconnect the test oscilloscope.

CRT ADJUSTMENTS

Equipment Required (see Table 4-1)

Primary Leveled Sine-Wave Generator (Item 2)	50 Ω BNC Cable (2 required) (Item 9)
Time-Mark Generator (Item 5)	Alignment Tool (Item 19)

See ADJUSTMENT LOCATIONS 2 *at the rear of this manual for location of adjustments and test points.*

NOTE

All crt adjustments (other than the Front-Panel ASTIG, FOCUS, and TRACE ROTATION adjustments) are accessed through the High Voltage shield located on the left side of the instrument near the rear of the crt. The location of each adjustment is indicated on the shield.

Initial Control Settings.

Control settings not listed do not affect the procedure.

VERTICAL VOLTS/DIV	
CH 1 and CH 2	0.1 V
CH 1 and CH 2 VAR	In detent
Input Coupling	
CH 1 and CH 2	1 MΩ GND
VERTICAL MODE	
CH 2 and BW LIMIT	On (buttons in)
CH 1, CH 3, and CH 4	Off (buttons out)
ADD and INVERT	Off (buttons out)
ALT/CHOP	ALT (button out)
VERTICAL POSITION	Midrange
A and B SEC/DIV	X-Y (knobs locked)
A and B SEC/DIV VAR	In detent
Horizontal POSITION	Midrange
TRIGGER	
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC
SLOPE	+ (plus)
LEVEL	Midrange
HOLDOFF	In detent
ΔV and Δt	Off (press and release until readout display disappears
TRACKING/INDEP	INDEP (button out)
INTENSITY	Visible display
READOUT INTENSITY	Scale factors off (CCW from MIN)
SCALE ILLUM	Fully CCW
FOCUS	Best focused display

1. Adjust ASTIG Preset (R977) and Grid Bias (R1878).

a. Position the dot in the center area of the graticule using the CH 1 and CH 2 POSITION controls.

b. Focus the displayed dot as well as possible using the front-panel FOCUS control.

c. ADJUST—ASTIG (R977 on the front panel), in conjunction with the FOCUS control, for the sharpest possible dot.

d. Set the INTENSITY control knob CCW so the index mark points directly left (less than full CCW rotation).

e. ADJUST—Grid Bias (R1878) for a barely visible dot.

f. CHECK—No dot is visible when the INTENSITY control is rotated fully CCW.

g. If necessary, repeat parts d and e until the CHECK in part f is correct.

2. Adjust TRACE ROTATION (R975) and Y-Axis Alignment (R1848).

NOTE

If the previous step was not performed, first setup the Initial Control Settings at the beginning of the CRT adjustments, then proceed as follows.

a. Set:

A and B SEC/DIV	50 μs (knobs locked)
INTENSITY	As required for a well defined trace
Δt	(Δt readout)
INTENSITY	As required for well defined vertical cursors

b. Using the CH 2 Vertical POSITION control, align the trace with the center horizontal graticule line.

c. Position one of the Δt cursors to the center vertical graticule line using either the Δ or the ΔREF OR DLY POS control.

d. ADJUST—TRACE ROTATION (R975 on the front panel) to align the trace with the center horizontal graticule line.

e. ADJUST—Y-Axis Alignment (R1848) to align the Δt cursor with the center vertical graticule line.

f. Repeat parts d and e as necessary for the best aligned display.

3. Adjust Geometry (R1870).

NOTE

If the previous step was not performed, first setup the Initial Control Settings at the beginning of the CRT adjustments, then proceed as follows.

a. Set:

Input Coupling	
CH 2	50 Ω DC
ΔV and Δt	Off (no readout)

b. Connect 10 μs time markers from the Time-Mark Generator to the CH 2 input connector via a 50 Ω BNC cable.

c. Use the Horizontal POSITION control to align the time markers with the vertical graticule lines. Use the CH 2 POSITION control to align the base of the signal with the bottom graticule line.

d. Set the CH 2 VOLTS/DIV switch for at least a 6-division vertical display.

e. Use the CH 2 POSITION control to set the tops of the time markers to graticule center.

f. Set the CH 2 VOLTS/DIV switch one position clockwise to overscan the display.

g. ADJUST—Geometry (R1870) for minimum curvature of the time markers across the entire graticule.

h. Disconnect the test setup.

4. Adjust Edge Focus (R1864).

NOTE

If the previous step was not performed, first setup the Initial Control Settings at the beginning of the CRT adjustments, then proceed as follows.

a. Set:

Input Coupling	
CH 2	50 Ω DC
VOLTS/DIV	
CH 2	0.2 V
INTENSITY	Midrange

b. Connect a 50 kHz, 8-division signal from the Primary Leveled Sine-Wave Generator to the CH 2 input connector via a 50 Ω BNC cable.

c. Center the display on the graticule.

d. ADJUST—Edge Focus (R1864), FOCUS (front-panel control), and ASTIG (R977, front-panel preset) for the most uniform focus over the entire display.

e. Disconnect the test setup.

5. Adjust Z-Axis Transient Response (R1834).

NOTE

If the previous step was not performed, first setup the Initial Control Settings at the beginning of the CRT adjustments, then proceed as follows.

a. Set:

A and B SEC/DIV	50 ns (knobs locked)
Input Coupling CH 2	1 MΩ GND
INTENSITY	Slightly left of center

b. Use the Horizontal POSITION control to place the beginning of the trace within the graticule.

c. ADJUST—Z-Axis Transient Response (R1834) for the most uniform intensity across the first division of display.

6. Adjust High Drive Focus (R1842).

NOTE

If the previous step was not performed, first set up the Intial Control Settings at the beginning of the CRT adjustments, then proceed as follows.

The following adjustment has the most effect on the first two divisions of the trace which will probably cause the readout to be compromised slightly. This will not be a problem as the readout is not used at full intensity.

a. Set:

ΔV	On (ΔV readout)
VOLTS/DIV CH2	0.2 V
Input Coupling CH 2	50 Ω DC
A and B SEC/DIV	200 ns (knobs locked)
READOUT INTENSITY	Fully CW
INTENSITY	Fully CW

b. Connect a 10 MHz, 6-division signal from the Primary Leveled Sine-Wave Generator to the CH 2 input connector via a 50 Ω BNC cable.

c. Center the display on the graticule.

d. ADJUST-High Drive Focus (R1842) for the best overall focus of the trace and readout.

e. Disconnect the test setup.

DAC REF, CH 1 AND CH 2 INPUT CAPACITANCE, AND VERTICAL READOUT JITTER ADJUSTMENTS

Equipment Required (see Table 4-1)

Calibration Generator (Item 3)
50 Ω BNC Cable (Item 9)
50 Ω Termination (Item 11)
Digital Multimeter (DMM) (Item 18)
Alignment Tool (Item 19)
Normalizer (Item 21)

See ADJUSTMENT LOCATIONS 3 *and* ADJUSTMENT LOCATIONS 4 *at the rear of this manual for test point and adjustment locations.*

Initial Control Settings.

Control settings not listed do not affect the procedure.

VERTICAL VOLTS/DIV	
CH 1 and CH 2	0.1 V
CH 1 and CH 2 VAR	In detent
Input Coupling	
CH 1 and CH 2	1 MΩ DC
VERTICAL MODE	
CH 1	On (buttons in)
CH 2, CH 3, and CH 4	Off (buttons out)
ADD, INVERT, and BW LIMIT	Off (buttons out)
ALT/CHOP	ALT (button out)
VERTICAL POSITION	Midrange
A and B SEC/DIV	0.1 ms (knobs locked)
A and B SEC/DIV VAR	In detent
Horizontal POSITION	Midrange
TRIGGER	
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC
SLOPE	+ (plus)
LEVEL	Midrange
HOLDOFF	In detent
Δt	On (Δt readout)
TRACKING/INDEP	INDEP (button out)
INTENSITY	Left of center
READOUT INTENSITY	As required for a visible display
SCALE ILLUM	Fully CCW
FOCUS	Best focused display

1. Adjust DAC Ref (R2127)

NOTE

The objective of this step is to make the total range of the DAC output voltage (sum of the CCW and CW readings) equal to 2.5 V.

a. Connect the digital multimeter (DMM) negative lead to the chassis ground. Connect the positive lead to pin 2 of J118 (on the Main Board).

b. Set the DMM to measure approximately 1.5 Vdc.

c. Rotate the ΔREF OR DLY POS control CCW until the DMM reading remains at a constant value (approximately −1.250 V). Note the reading.

d. Rotate the ΔREF OR DLY POS control CW until the DMM reading remains at a constant value (approximately +1.250 V). Note the reading.

e. Add the absolute values of the readings noted in parts c and d together (approximately 2.500 V).

f. Subtract the total in part e from 2.500 V, then divide the difference by two.

g. ADJUST—DAC Ref (R2127 on the Control Board) to add the (signed) number obtained in part f to the reading obtained in part d.

h. Repeat parts c through g as necessary to obtain a total DAC range of 2.500 V.

2. Adjust CH 1 and CH 2 Input Capacitance (C105 and C205).

NOTE

If the previous step was not performed, first setup the Initial Control Settings before the DAC Ref adjustment, then proceed as follows.

The objective of this adjustment is to match the input capacitance of the 50 mV per division position of the VOLTS/DIV switches to the 0.1 V per division position. The front corner of an input square-wave signal is used to indicate when the capacitances are matched

a. Connect a 1 KHz square-wave signal from the Calibration Generator high-amplitude output to the CH 1 OR X input connector via a 50 Ω BNC cable, a 50 Ω termination, and a normalizer. Adjust the generator output level for a 6-division signal vertically centered on the graticule.

b. Set the normalizer for a square front corner over approximately the first 40 μs (0.4 division) of the positive portion of the waveform.

c. Change the CH 1 VOLTS/DIV switch to the 50 mV position and adjust the generator for a 6-division signal display.

d. ADJUST—The CH 1 50 mV C Adj (C105 on the Main Board) for the same waveform front corner noted in part b.

e. Repeat parts b through d until no change is observed in the waveform front corner when the CH 1 VOLTS/DIV switch is alternated between the 50 mV and 0.1 V positions. When switching between positions, reestablish the reference display amplitude at each position, and observe the square-wave front corner to make the comparison.

f. Move the input signal to CH 2 and change the VERTICAL MODE to display CH 2 only. Adjust the generator amplitude for a 6-division signal amplitude.

g. Set the normalizer for a square front corner over approximately the first 40 μs (0.4 division) of the positive portion of the waveform.

h. Change the CH 2 VOLTS/DIV switch to the 50 mV position and adjust the generator for a 6-division display.

i. ADJUST—The CH 2, 50 mV C Adj (C205 on the Main Board) for the same waveform front corner noted in part g.

j. Repeat parts g through i until no change is observed in the waveform front corner when the CH 2 VOLTS/DIV switch is alternated between the 50 mV and 0.1 V positions. When switching between positions, reestablish the reference signal amplitude at each position, and observe the square-wave front corner to make the comparison.

k. Disconnect the test setup.

3. Adjust Vertical Readout Jitter (R618).

NOTE

If the previous step was not performed, first setup the Initial Control Settings before the DAC Ref adjustment, then proceed as follows.

a. Set the CH 1 Input Coupling to 50 Ω DC.

b. Press and release the ΔV button to obtain a ΔV display.

c. Use the ΔREF OR DLY POS control to position one cursor 3 divisions above graticule center. Use the Δ control to position the other cursor 3 divisions below graticule center.

d. Connect a 1 kHz, fast-rise signal from the Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

e. Set the generator output level for an 8-division display.

f. Use the CH 1 Vertical and Horizontal POSITION controls to center the CH 1 display on the graticule.

g. ADJUST—Vertical Readout Jitter (R618) for minimum vertical jitter of the readout characters and cursors.

h. Disconnect the test setup.

AUTOMATIC CALIBRATION CONSTANTS, HORIZONTAL AND VERTICAL GAIN, CENTERING, AND TRANSIENT RESPONSE ADJUSTMENTS

NOTE

Within the following procedure, the calibration constants for timing, vertical gain, and trigger level are generated by the system microprocessor and are stored in nonvolatile memory. The adjustments in CAL 01, 02, 03, and 04 should be performed in numerical sequence, i.e., CAL 01 should be done before CAL 02, CAL 02 should be done before CAL 03, etc. Performing partial procedures (i.e. only one or two of the CAL steps) is not recommended and should only be done if the calibration constants that would have been set in the preceding steps are known to be correct.

The CAL functions are available only if the CAL/NO CAL jumper (P501 on the Control Board) is in the CAL position (between pins 1 and 2) when power is turned on. When the automatic calibration procedures are completed, return the jumper to the NO CAL position to prevent entry into the calibration routines.

Equipment Required (see Table 4-1)

Calibration Generator (Item 3)
Time-Mark Generator (Item 5)
50 Ω BNC Cable (Item 9)
Dual-Input Coupler (Item 10)
5X Attenuator (Item 16)
Digital Multimeter (DMM) (Item 18)
Alignment Tool (Item 19)

See ADJUSTMENT LOCATIONS 4 *at the rear of this manual for test point and adjustment locations.*

Initial Control Settings.

CAL/NO CAL jumper	CAL position (between pins 1 and 2) prior to turning on power

NOTE

When performing the automatic CAL steps, initial setting of the front-panel controls is not required.

CAL 01—HORIZONTAL

1. Check/Adjust Horizontal Timing, X1 Gain (R860), X10 Gain (R850), Hrz Ctr (R801), and Trans Resp (R802).

a. Simultaneously press in and hold the Δt and the ΔV push buttons, then press and hold the SLOPE switch. Hold all three switches in for approximately one second, then release them.

b. CHECK—Top line of the readout display says: "DIAGNSTIC. PUSH A/B TRIG TO EXIT".

NOTE

The "menu" of calibration, test, and exercise routines are in a loop that may be scrolled through in single steps, either forward or backward. Pressing up or down on the TRIGGER MODE switch and releasing it respectively increments or decrements the menu position by one. As each routine is selected, its name appears in the lower left corner of the readout display.

When performing a calibration step, touch only the specific control or controls called out in the procedure. Movement of other controls may cause erroneous calibration results.

c. Scroll to CAL 01.

CAUTION

Upon entering CAL 01, the Input Coupling is automatically set to 50 Ω DC and the 50 Ω OVERLOAD protection is disabled. Before starting the procedure, make sure any 50 Ω OVERLOAD condition has been cleared.

NOTE

In this procedure, pressing up and releasing the TRIGGER COUPLING switch stores the current calibration parameter being set and increments the routine to the next step (except where otherwise noted).

d. Connect the DMM, set to measure approximately 500 mV, to the CALIBRATOR output.

e. Press up and release the TRIGGER COUPLING switch.

NOTE

The CALIBRATOR output will go to its LO level on odd CAL steps and to its HI level on even steps.

f. CHECK—CALIBRATOR output voltage is 0 mV ±1 mV.

g. CHECK—Readout indicates ADJUST Δ, (step) 1, 100 μs (for A Sweep), and 1 μs (for B Sweep).

NOTE

The readout prompts the operator by showing the control to be moved (upper left corner), the autocal step number (upper right corner), the A Sweep speed (bottom right center), and the B Sweep speed (bottom right corner) as set up by the routine. An example (from step g above) is:

ADJ Δ 1

100 μs 1 μs

h. Connect the Time-Mark Generator, set for 0.1 ms time markers, to the CH 1 OR X input connector via a 50 Ω BNC cable.

i. Set:

VOLTS DIV	As needed for a convenient signal display amplitude
TRACE SEP	As needed to separate the A and B Sweeps
CH 1 POSITION	As needed to view both A and B Sweeps
Horizontal POSITION	Position start of trace at the left graticule line

NOTE

Some sequential pairs of steps are iterative, i.e., the earlier step is recalled if an adjustment is made in the later step. Occasionally, on the earlier of some of these pairs, the readout may indicate "LIMIT" before the correct control setting is reached . If this occurs, proceed to the next AUTOCAL step. After the adjustment at the next step is performed, the previous step will automatically be recalled, and the adjustment may be performed in the normal manner.

j. ADJUST—ΔREF OR DLY POS and Δ controls to align both the intensified zones with the 6th time marker (near graticule center) and to superimpose the delayed B Sweep time markers. Press up and release the TRIGGER COUPLING switch.

k. CHECK—CALIBRATOR output voltage is between 398 mV and 402 mV of the reading noted in part f. Disconnect the DMM when through.

l. CHECK—Readout indicates ADJ Δ, (step) 2, 100 μs (for A Sweep), and 1 μs (for B Sweep).

m. ADJUST—ΔREF OR DLY POS control to intensify the 2nd time marker, and ADJUST—Δ control to intensify the the 10th time marker. Superimpose the delayed B Sweep time markers within 0.2 division.

n. Push up and release the TRIGGER COUPLING switch.

o. CHECK—Readout indicates ADJ Δ, (step) 3, 300 μs (for A Sweep), and 1 μs (for B Sweep).

p. ADJUST—ΔREF OR DLY POS control to intensify the 4th time marker, and ADJUST—Δ control to intensify the 28th time marker. Superimpose the delayed B Sweep time markers within 1.2 division.

q. Press up and release TRIGGER COUPLING switch. If the adjustment in step 3 was changed, step 2 will be recalled; otherwise step 4 will be initiated.

r. CHECK—Readout indicates ADJ Δ, (step) 4, 100 μs (for A Sweep), and 1 μs (for B Sweep). Set the Time-Mark Generator for 5 μs time markers.

s. ADJUST—Δ control CCW until no further movement of the B Sweep display occurs. Note the position of the 1st time marker, then adjust the Δ control CW until the 2nd time marker moves to the left and aligns with the position just noted.

t. Press up and release the TRIGGER COUPLING switch. Set the Time-Mark Generator for 10 μs time markers.

u. CHECK—Readout indicates X1, X10, HRZ CTR, (step) 5, and 10 μs (for A Sweep) and two vertical cursors appear on the display.

v. ADJUST—X1 Gain (R860) and Hrz Ctr (R801) to align the two cursors with the 2nd and 10th vertical graticule lines, then adjust X10 Gain (R850) for 1 time marker per division.

w. Press up and release TRIGGER COUPLING switch. Set the Time-Mark Generator for 10 ms time markers.

x. CHECK—Readout indicates ADJ Δ, (step) 6, 10 ms (for A Sweep), and 100 μs (for B Sweep).

y. ADJUST—ΔREF OR DLY POS control to intensify the 2nd time marker, and ADJUST—Δ control to intensify the 10th time marker. Superimpose the delayed B Sweep time markers within 0.2 division.

z. Press up and release TRIGGER COUPLING switch. Set the Time-Mark Generator for 1 μs time markers.

aa. For each step in Table 5-2, do the following:

1. Adjust the ΔREF OR DLY POS and Δ controls, as necessary, to intensify the indicated time marks on the A Sweep and superimpose the displayed B Sweep markers within the listed limits.

2. Press up and release the TRIGGER COUPLING switch.

NOTE

If the Δ control is adjusted at step 9, 12 or 14, the previous step will be repeated.

Table 5-2
Horizontal Timing

Step No.	Time-Marker Period	ΔREF Marker	Δ Marker	Superposition Tolerance In Tolerance In Divisions
7	1 μs	2	10	0.2
8	2 μs	2	10	0.2
9	2 μs	4	28	1.2
10	10 μs	2	10	0.2
11	50 μs	2	10	0.2
12	50 μs	4	28	1.2
13	0.5 μs	2	10	0.2
14	0.5 μs	4	28	1.2
15	100 ns	2	10	0.2
16	20 ns	2	10	0.1

bb. Set the TRACE SEP fully CW.

cc. For each step in Table 5-3 (except step 28), adjust the Δ control for the listed number of markers over the center 8 divisions, then press up and release the TRIGGER COUPLING switch. If the Δ control is adjusted at step 18, 20, 23, or 25, the previous step will be repeated. The 2445 intentionally skips step 28.

NOTE

Change the CH 1 VOLTS/DIV switch setting as necessary to maintain adequate signal display amplitude.

Table 5-3
Horizontal Timing

Step No.	Time-Marker Period	Markers Over 8 Divisions
17	1 μs	8
18	1 μs	24
19	2 μs	8
20	2 μs	24
21	10 μs	8
22	50 μs	8
23	50 μs	24
24	500 ns	8
25	500 ns	24
26	100 ns	8
27	20 ns	8
28[a]	skipped	
29	1 ms	8

[a]Firmware in the 2445 is shared with a similiar instrument, the 2465, which requires step 28. The 2445 skips step 28.

NOTE

If the remainder of the Adjustment Procedure will not be performed (in totality), readjustment of Horizontal Readout Jitter (R805) may be necessary if the X1 Gain (R860) or the X10 Gain (R850) was changed. See subsection 2 on page 5-17 for that procedure.

dd. Disconnect the test setup.

CAL 02—VERTICAL

2. Check/Adjust Vertical Preamp Gain, Gain (R638), and Vertical Centering (R639).

NOTE

If the previous step (CAL 01) was not performed, the adjustments in this subsection should only be performed if those constants that would have been set in CAL 01 are known to be correct.

a. Set the front-panel INTENSITY control at midrange.

b. Scroll to CAL 02.

c. Press up and release the TRIGGER COUPLING switch. The instrument will automatically increment through steps 100 to 111.

d. CHECK—Readout indicates CH 1 VAR, CH2 POS, (step) 111, 500 mV, and BWL.

NOTE

The readout prompts the operator by showing the controls to be moved (upper left corner and upper center), the autocal step number (upper right corner), the amplitude of signal to be applied to either the CH 1 or CH 2 connectors (lower left corner), and any other scope function that is enabled. An example (from step d above) is:

CH1 VAR CH2 POS	111
500 mV	BWL

e. Connect a 0.5 V, standard-amplitude signal from the Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

f. Use the CH 2 POSITION control to vertically position the trace to within 1 division of the center graticule line.

g. ADJUST—CH 1 POSITION and VOLTS/DIV VAR controls to obtain a 10-division horizontal signal. Press up and release the TRIGGER COUPLING switch.

h. CHECK—Readout indicates MOVE SW, CENTER CH 1 POS, (step) 112, 500 mV, and BWL; then press up and release the TRIGGER COUPLING switch.

i. ADJUST—CH 1 POSITION control carefully until the CH 1 input coupling "1 MΩ DC" indicator remains illuminated, then press up and release the TRIGGER COUPLING switch.

NOTE

In the following steps, if the "LIMIT" message appears, it probably indicates that the TRIGGER COUPLING (step) switch was moved before the required signal was applied. Press down and release the TRIGGER COUPLING switch, verify that the correct signal is applied, then press up and release the TRIGGER COUPLING switch.

j. CHECK—First step number listed in Table 5-4 appears in the readout.

k. Apply the corresponding standard-amplitude signal from the Calibration Generator, then press up and release the TRIGGER COUPLING switch.

l. Repeat steps j and k for each step-signal combination listed in Table 5-4.

Table 5-4
Vertical Calibration Signals

Autocal Step Readout Display	Standard-Amplitude Signal to Apply
113, 114 [a]	0.5 V
115	0.2 V
116	0.1 V
117	50 mV
118	20 mV
119	1 V
120	10 V

[a] When step 113 is performed, step 114 is also automatically done. No indication of step 114 will be shown unless a LIMIT error is encountered.

m. Move the signal to the CH 2 input connector.

n. CHECK—Readout indicates MOVE SW, CENTER CH 2 POS, (step) 121, 500 mV, 500 mV, and BWL.

o. Set the Calibration Generator for a 500 mV standard-amplitude signal, then press up and release the TRIGGER COUPLING switch.

p. ADJUST—CH 2 VERTICAL POSITION control until the CH 1 Input Coupling "1 MΩ DC" indicator remains illuminated, then press up and release the TRIGGER COUPLING switch.

q. CHECK—Readout indicates MOVE SW, CENTER CH 2 POS, (step) 122, 500 mV, 500 mV, and BWL.

r. With the Calibration Generator set for a 500 mV standard-amplitude signal, press up and release the TRIGGER COUPLING switch.

s. ADJUST—CH 2 VERTICAL POSITION control until the CH 1 Input Coupling "1 MΩ DC" indicator remains illuminated, then press up and release the TRIGGER COUPLING switch.

t. CHECK—First step number listed in Table 5-5 appears in the readout.

u. Apply the corresponding standard-amplitude signal, then press up and release the TRIGGER COUPLING switch.

v. Repeat steps t and u for each step-signal combination listed in Table 5-5.

Table 5-5
Vertical Calibration Signals

Autocal Step Readout Display	Standard-Amplitude Signal to Apply
123, 124 [a]	0.5 V
125	0.2 V
126	0.1 V
127	50 mV
128	20 mV
129	1 V
130	10 V

[a] When step 123 is performed, step 124 is also automatically done. No indication of step 124 will be shown unless a LIMIT error is encountered.

w. CHECK—Readout indicates MOVE SW, CENTER CH 2 POS, (step) 131, 10 V, ↓10 V, and BWL; then press up and release the TRIGGER COUPLING switch.

x. ADJUST—CH 2 POSITION control until the CH 1 Input Coupling "1 MΩ DC" indicator remains illuminated, then press up and release the TRIGGER COUPLING switch. The instrument will automatically increment through steps 132 to 142.

y. CHECK—Readout indicates MOVE SW, CENTER CH 1 POS, (step) 142, 50 mV, and BWL.

z. Move the signal to the CH 1 OR X input connector and set the Calibration Generator for a 50 mv standard-amplitude signal, then press up and release the TRIGGER COUPLING switch.

aa. ADJUST—CH 1 POSITION control until the CH 1 "1 MΩ DC" indicator remains illuminated, then press up and release the TRIGGER COUPLING switch. Wait approximately 10 seconds for automatic calibration of the ΔV cursors.

bb. CHECK—Readout indicates VERTICAL CENTER and GAIN.

cc. ADJUST—Gain (R638) for precisely 5 divisions between the two horizontal cursors.

dd. ADJUST—Vertical Centering (R639) to center the cursors on the graticule (align the cursors with the dotted 0% and 100(%) graticule lines).

ee. Press up and release the TRIGGER COUPLING switch.

CAL 03—TRIGGERING

3. Check/Adjust Triggering.

NOTE

If the previous steps (CAL 01 and CAL 02) were not performed, the adjustments in this subsection should only be performed if those constants that would have been set in CAL 01 and CAL 02 are known to be correct and if a DC Balance has been performed after a 20-minute warmup period.

a. Scroll to CAL 03.

b. Press up and release the TRIGGER COUPLING switch.

c. CHECK—Procedure automatically steps from 201 through 214 and stops at 215.

d. CHECK—Readout indicates CH 1, 500 mV, and (step) 215.

NOTE

The readout prompts the operator by showing which connector the input signal should be applied to (upper left corner), the amplitude of that signal (upper center), and the autocal step number (upper right corner). An example (from step d above) is:

CH1 500 mV 215

e. Connect a 0.5 V standard-amplitude signal from the Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

f. Press up and release the TRIGGER COUPLING switch.

g. CHECK—Readout indicates CH 1, 500 mV, and (step) 216.

h. Press up and release the TRIGGER COUPLING switch.

i. CHECK—Readout indicates CH 2, 500 mV, and (step) 217.

j. Move the signal to the CH 2 input connector. Press up and release the TRIGGER COUPLING switch.

k. CHECK—Readout indicates CH 3, 500 mV, and (step) 218.

l. Move the signal to the CH 3 input connector. Press up and release the TRIGGER COUPLING switch.

m. CHECK—Readout indicates CH 3, 2V, and (step) 219.

n. Change the generator output level to 2 V, then press up and release the TRIGGER COUPLING switch.

o. CHECK—Readout indicates CH 4, 500 mV, and (step) 220.

p. Move the signal to the CH 4 input connector and change the generator output level to 0.5 V. Press up and release the TRIGGER COUPLING switch.

q. CHECK—Readout indicates CH 4, 2V, and (step) 221.

r. Change the generator output level to 2 V, then press up and release the TRIGGER COUPLING switch.

s. Disconnect the test setup.

CAL 04—CH 2 DELAY ENABLE/DISABLE

4. Check/Adjust CH 2 Delay Enable/Disable.

a. Scroll to CAL 04.

b. Press up and release the TRIGGER COUPLING switch to initiate the routine.

c. CHECK—Readout alternately indicates "ENABLED" and "DISABLED" each time the TRIGGER COUPLING switch is pressed up and released.

d. Leave the readout display indicating "ENABLED". Press and release the A/B TRIG button to exit the routine.

e. Connect a 100 kHz, positive-going signal from the Calibration Generator fast-rise output to the CH 1 OR X and CH 2 input connectors via a 50 Ω BNC cable, a 5X attenuator, and a Dual-Input Coupler.

f. Set:

VERTICAL MODE	
CH 1 and CH 2	On (buttons in)
VOLTS/DIV	
CH 1 and CH 2	10 mV
Input Coupling	
CH 1 and CH 2	50 Ω DC
A and B SEC/DIV	5 ns (knobs locked)
TRIGGER	
SOURCE	CH 1
MODE	AUTO LVL
COUPLING	DC
SLOPE	+ (plus)

g. Set the generator amplitude for a 3- to 5-division display amplitude. Use the CH 1 and CH 2 POSITION controls to vertically overlay the traces near the center of the graticule area.

h. Set the Horizontal POSITION control to set the rising edge of the signal near the center vertical graticule line.

i. Press the X10 MAG button in to obtain a magnified display.

j. Pull out the B SEC/DIV knob.

k. CHECK—Readout indicates "CH 2 DLY - TURN Δ" and that the Δ control will move the leading edge of the CH 2 trace at least 1 division to either side of the CH 1 trace.

l. ADJUST—Δ control to superimpose the leading edges.

m. Push in the B SEC/DIV knob.

NOTE

If the CH 2 Delay Adjust feature is to be disabled for normal instrument use, perform the following steps; otherwise, proceed to step r below.

n. Reenter the Diagnostic Monitor by pressing the ΔV and Δt buttons simultaneously (hold them in), then press and hold the TRIGGER SLOPE button. Release the buttons after about 1 second.

o. Scroll to CAL 04.

p. Press up and release the TRIGGER COUPLING switch until the readout indicates "DISABLED."

q. Press and release the A/B TRIG button to return to normal operating mode.

r. Return the CAL/NO CAL jumper to the NO CAL position and disconnect the test setup.

DYNAMIC CENTERING, CRT TERMINATION, VERTICAL GAIN, VERTICAL CENTERING, TRANSIENT RESPONSE, HF ADJ, READOUT JITTER, DC BALANCE, AND X-Y PHASE DIFFERENTIAL ADJUSTMENTS

Equipment Required (see Table 4-1)

Primary Leveled-Sinewave Generator (Item 2)
Calibration Generator (Item 3)
50 Ω BNC Cable (Item 9)
5X Attenuator (Item 16)
Alignment Tool (Item 19)
Tunnel Diode Pulser (Item 22)

See ADJUSTMENT LOCATIONS 1 *and* ADJUSTMENT LOCATIONS 4 *at the rear of this manual for location of test points and adjustments.*

Initial Control Settings.

Control settings not listed do not affect the procedure.

VERTICAL VOLTS/DIV	
CH 1 and CH 2	10 mV
CH 1 VAR	CCW (out of detent)
CH 2 VAR	In detent
Input Coupling	
CH 1 and CH 2	50 Ω DC
VERTICAL MODE	
CH 1	On (button in)
CH 2, CH 3 and CH 4	Off (buttons out)
ADD, INVERT, and BW LIMIT	Off (buttons out)
ALT/CHOP	ALT (button out)
VERTICAL POSITION	Midrange
A and B SEC/DIV	20 ns (knobs locked)
A and B SEC/DIV VAR	In detent
Horizontal POSITION	Midrange
TRIGGER	
MODE	AUTO LVL
SOURCE	VERT
COUPLING	DC
SLOPE	+ (plus)
LEVEL	Midrange
HOLDOFF	In detent
ΔV	On (RATIO readout)
TRACKING/INDEP	INDEP (button out)
ΔREF OR DLY POS and Δ	Cursors near the 3rd line above and 3rd line below graticule center (6 division spacing)
INTENSITY	Left of center
READOUT INTENSITY	Right of center
SCALE ILLUM	Fully CCW
FOCUS	Best focused display

1. Adjust Dynamic Centering (R3401 and R3407).

a. Rotate the READOUT INTENSITY control from midrange to fully CW and note any horizontal and vertical shift that occurs in the readout characters.

b. ADJUST—Horizontal Dynamic Centering (R3401) to minimize the horizontal component of the shift.

c. ADJUST—Vertical Dynamic Centering (R3407) to minimize the vertical component of the shift.

d. Repeat steps a through c as necessary to minimize readout shift until no further improvement is noted.

2. Check/Adjust CRT Termination (R1501), Vertical Gain (R638), Vertical Centering (R639), High-Frequency Trans Resp (C404, R403), Vertical Readout Jitter (R618), Horizontal Readout Jitter (R805), and X-Y Phasing (C118).

NOTE

If the previous step was not performed, first setup the Initial Control Settings before the Dynamic Centering adjustments, then proceed as follows.

CRT Termination, High Frequency Transient Response, Vertical Gain, Vertical Centering, and Readout Jitter adjustments are interactive. This procedure optimizes these adjustments together.

a. Rotate the ΔREF OR DLY POS control CCW until the RATIO readout is constant.

b. Rotate the Δ control until the readout display indicates 130.0%.

c. CHECK—One cursor is near the bottom horizontal graticule line and the other is near dotted graticule line marked 100(%).

d. Rotate the ΔREF OR DLY POS control until the readout displays exactly 100.0%. The cursors should now be on or near the dotted graticule lines marked 0% and 100(%).

e. Set the CH 1 VOLTS/DIV VAR to the detent position.

NOTE

Care must be taken not to disturb the position of the controls adjusted in parts b through e during the balance of this procedure. If they are accidentally moved, repeat the procedure from the beginning.

f. Connect the high-amplitude output of the Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable, a Tunnel Diode Pulser, and a 5X attenuator.

g. Set the generator Period switch to 100 kHz, and set the generator amplitude control to maximum.

h. Rotate the pulser Trigger control CW (from a fully CCW position) until a stable signal first appears on the graticule. Display amplitude will be approximately 5 divisions. The oscilloscope TRIGGER LEVEL control may need to be adjusted to obtain a stable display.

NOTE

As a guide when performing the following adjustments, optimum performance is achieved when the CH 1 and CH 2 step response aberrations are ≤ 4% when using 10 mV/division deflection factors (≤ 0.2 division on a 5-division signal).

i. ADJUST—CRT Termination (R1501) for best flat-top approximately 5 ns past the rising edge of the waveform. The adjustment is accessable through a hole in the top cover plate. Squeezing the output leads of the termination inductors (LR1513 and LR1514) toward each other will reduce the spike that may be present approximately 6 ns behind the leading edge.

j. ADJUST—Trans Resp adjustments (C404 and R403) alternately for the best flat top on the first 10 ns of the positive portion of the waveform.

k. ADJUST—Vertical Gain (R638) and Vertical Centering (R639) to vertically center the cursors precisely 5 divisions apart (align with the dotted 0% and 100(%) graticule lines).

l. Press the ΔV button to turn off the cursors.

m. Move the test signal to CH 2 and set the VERTICAL MODE switches to display CH 2.

n. Repeat part j for CH 2, switching between CH 1 and CH 2 as necessary, until both CH 2 and CH 1 aberrations are minimized. When minimized, leave CH 2 selected.

o. Disconnect the Calibration Generator and connect the Leveled Sine-Wave Generator to the CH 2 input via a BNC cable.

p. Set the generator for a 6-division display at the reference frequency.

q. Change the generator output frequency to 150 MHz.

r. CHECK—Display amplitude is between 4.4 divisions and 5 divisions. This bandwidth provides optimum performance of the Vertical system.

s. ADJUST—If necessary, compromise the settings in part j to obtain the best flat top with the proper bandwidth.

t. Move the input signal to CH 1 and select CH 1 for display.

u. Repeat parts p through s for CH 1. If readjustment of C404 or R403 is necessary, repeat parts j through s.

v. Set the A and B SEC/DIV switch to 1 ms.

w. Select CH 1 for display.

x. Press and release the ΔV button to obtain a ΔV display.

y. Use the ΔREF OR DLY POS control to position one cursor 3 divisions above graticule center and use the Δ control to position the other cursor 3 divisions below graticule center.

z. Connect a 1 kHz, fast-rise signal from the Calibration Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

aa. Set the generator output level for an 8-division display.

bb. Use the CH 1 Vertical and the Horizontal POSITION controls to center the CH 1 display on the graticule.

cc. ADJUST—Vertical Readout Jitter (R618) for minimum vertical jitter of the readout characters and cursors.

dd. Press the Δt button to obtain a Δt cursor display.

ee. Using the ΔREF OR DLY POS and Δ controls, position the cursors to the 2nd and 10th graticule lines.

ff. Press the X10 MAG button to magnify the display.

gg. ADJUST—Horizontal Readout Jitter (R805) for minimum horizontal jitter of the readout characters and cursors.

hh. Disconnect the test setup.

3. Set CH 1 and CH 2 DC Balance.

NOTE

The instrument must have had a 20-minute warmup prior to performing the next step to ensure accuracy.

a. Set:

Input Coupling	
CH 1 and CH 2	1 MΩ AC

b. Press up momentarily and release the CH 1 and CH 2 Input Coupling switches simultaneously.

c. CHECK—A moving dot display replaces the normal display for approximately 10 seconds, then the display returns to normal.

d. CHECK—For less than 0.2-division vertical trace shift when the CH 1 VOLTS/DIV switch is rotated through all of its settings.

e. Set the VERTICAL MODE switches to disable CH 1 and display CH 2.

f. CHECK—For less than 0.2-division vertical trace shift when the CH 2 VOLTS/DIV switch is rotated through all of its settings.

4. Adjust X-Y Phasing (C118).

a. Set:

VOLTS/DIV	
CH 1	50 mV
Input Coupling	50 Ω DC
A SEC/DIV	X-Y
VERTICAL MODE	
CH 1	On (button in)
CH 2	Off (button out)

b. Connect the Primary Leveled Sine-Wave Generator to the CH 1 OR X input connector via a 50 Ω BNC cable.

c. Set the generator frequence to 1 MHz and adjust the amplitude for a 6-division vertical signal display.

d. Use the CH 1 POSITION control to vertically center the display on the graticule.

e. ADJUST—X-Y Phasing (C118) for no opening in the elipse.

f. Set the generator frequency to 2 MHz and adjust the amplitude for a 6-division vertical signal display.

g. CHECK—Horizontal opening in the elipse is 0.3 division or less, measured at the center horizontal graticule line.

h. Disconnect the test setup.

i. Turn POWER Off.

MAINTENANCE

This section of the manual contains information for conducting preventive maintenance, troubleshooting, and corrective maintenance on the 2445 Oscilloscope.

STATIC-SENSITIVE COMPONENTS

The following precautions are applicable when performing any maintenance involving internal access to the instrument.

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.

3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by their bodies, never by their leads.

Table 6-1
Susceptibility
to Static Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels[a]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[a]Voltage equivalent for levels: (Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)

1 = 100 to 500 V
2 = 200 to 500 V
3 = 250 V
4 = 500 V
5 = 400 to 600 V
6 = 600 to 800 V
7 = 400 to 1000 V(est.)
8 = 900 V
9 = 1200 V

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists of cleaning, visual inspection, and checking instrument performance. When accomplished regularly, it may prevent instrument malfunction and enhance instrument reliability. The severity of the environment in which the instrument is used determines the required frequency of maintenance. An appropriate time to accomplish preventive maintenance is just before instrument adjustment.

GENERAL CARE

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the 2445. The front cover supplied with the instrument provides both dust and damage protection for the front panel and crt, and it should be on whenever the instrument is stored or is being transported.

INSPECTION AND CLEANING

The 2445 should be visually inspected and cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, prevent efficient heat dissipation. It also provides an electrical conduction path that could result in instrument failure, especially under high-humidity conditions.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of 1% mild detergent with 99% water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior

INSPECTION. Inspect the external portions of the instrument for damage, wear, and missing parts; use Table 6-2 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance. Deficiencies found that could cause personal injury or could lead to further damage to the instrument should be repaired immediately.

Table 6-2
External Inspection Check List

Item	Inspect For	Repair Action
Cabinet, Lid, Front Panel	Cracks, scratches, deformations, damaged hardware or gaskets.	Touch up paint scratches and replace defective components.
Front-panel Controls	Missing, damaged, or loose knobs, buttons, and controls.	Repair or replace missing or defective items.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective parts. Clear or wash out dirt.
Carrying Handle	Correct operation.	Replace defective parts.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective parts.

CAUTION

To prevent getting moisture inside the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

CLEANING. Loose dust on the outside of the instrument can be removed with a soft cloth or small soft-bristle brush. The brush is particularly useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners.

Two plastic light filters, one blue and one clear, are provided with the oscilloscope. Clean the light filters and the crt face with a soft lint-free cloth dampened with either isopropyl alcohol or a mild detergent-and-water solution.

Interior

To gain access to internal portions of the instrument for inspection and cleaning, refer to the "Removal and Replacement Instructions" in the "Corrective Maintenance" part of this section.

INSPECTION. Inspect the internal portions of the 2445 for damage and wear, using Table 6-3 as a guide. Deficiencies found should be repaired immediately. The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

If any electrical component is replaced, conduct a Performance Check for the affected circuit and for other closely related circuits (see Section 4). If repair or replacement work is done on any of the power supplies, conduct a complete Performance Check and, if so indicated, an instrument readjustment (see Sections 4 and 5).

Table 6-3
Internal Inspection Check List

Item	Inspect For	Repair Action
Circuit Boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Clean solder corrosion with an eraser and flush with isopropyl alcohol. Resolder defective connections. Determine cause of burned items and repair. Repair defective circuit runs.
Resistors	Burned, cracked, broken, blistered.	Replace defective resistors. Check for cause of burned component and repair as necessary.
Solder Connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.
Capacitors	Damaged or leaking cases. Corroded solder on leads or terminals.	Replace defective capacitors. Clean solder connections and flush with isopropyl alcohol.
Semiconductors	Loosely inserted in sockets. Distorted pins.	Firmly seat loose semiconductors. Remove devices having distorted pins. Carefully straighten pins (as required to fit the socket), using long-nose pliers, and reinsert firmly. Ensure that straightening action does not crack pins, causing them to break off.
Wiring and Cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace defective wires or cables.
Chassis	Dents, deformations, and damaged hardware.	Straighten, repair, or replace defective hardware.

CAUTION

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

CLEANING. To clean the interior, blow off dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards.

If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 5% mild detergent and 95% water as follows:

CAUTION

Exceptions to the following procedure are the Attenuator assemblies and the Front-Panel module. Clean these assemblies only with isopropyl alcohol as described in step 4.

1. Gain access to the parts to be cleaned by removing easily accessible shields and panels.

2. Spray wash dirty parts with the detergent-and-water solution; then use clean water to thoroughly rinse them.

3. Dry all parts with low-pressure air.

NOTE

Most of the switches used in the 2445 are sealed and the contacts are inaccessible. If cleaning is deemed necessary, use only isopropyl alcohol.

4. Clean switches with isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate. Then complete drying with low-pressure air.

5. Dry all components and assemblies in an oven or drying compartment using low-temperature (125° F to 150° F) circulating air.

LUBRICATION

There is no periodic lubrication required for this instrument.

SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

PERIODIC READJUSTMENT

To ensure accurate measurements, check the performance of this instrument every 2000 hours of operation, or if used infrequently, once each year. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete Performance Check and Adjustment instructions are given in Sections 4 and 5. The Performance Check Procedure can also be helpful in localizing certain troubles in the instrument.

TROUBLESHOOTING

INTRODUCTION

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the "Theory of Operation" and "Diagrams" sections of this manual may be helpful while troubleshooting.

TROUBLESHOOTING AIDS

Diagnostic Firmware

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions. When instrument power is applied, power-up tests are performed to verify proper operation of much of the instrument's circuitry. If a failure is detected, this information is passed on to the operator in the form of either a crt readout or illuminated LED indicators. The failure information directs the operator to the failing block of circuitry. If the failure is such that the processor can still execute the diagnostic routines, the user can call up specific tests to further check the failing circuitry. The specific diagnostic routines are explained later in this section.

Schematic Diagrams

Complete schematic diagrams are located on tabbed foldout pages in the "Diagrams" section. Portions of circuitry mounted on each circuit board are enclosed by heavy black lines. The assembly number and name of the circuit are shown near either the top or the bottom edge of the diagram.

Functional blocks on schematic diagrams are outlined with a wide grey line. Components within the outlined area perform the function designated by the block label. The "Theory of Operation" uses these functional block names when describing circuit operation as an aid in cross-referencing between the theory and the schematic diagrams.

Component numbers and electrical values of components in this instrument are shown on the schematic diagrams. Refer to the first page of the "Diagrams" section for the reference designators and symbols used to identify components. Important voltages and waveform reference numbers (enclosed in hexagonal-shaped boxes) are also shown on each diagram. Waveform illustrations are located adjacent to their respective schematic diagram.

Circuit Board Illustrations

Circuit board illustrations showing the physical location of each component are provided for use in conjunction with each schematic diagram. Each board illustration is found in the "Diagrams" section on the back of a foldout page, preceding the first schematic diagram(s) to which it relates.

The locations of waveform test points are marked on the circuit board illustrations with hexagonal outlined numbers corresponding to the waveform numbers on both the schematic diagram and the waveform illustrations.

Circuit Board Locations

The placement in the instrument of each circuit board is shown in a board locator illustration. This illustration is located on the foldout page along with the circuit board illustration.

Power Distribution Diagrams

Power Distribution diagrams (diagrams 11 and 12) are provided in the "Diagrams" section to aid in troubleshooting power-supply problems.

Circuit Board Interconnection Diagram

A circuit board interconnection diagram (diagram 13) and tables listing the interconnecting pins and signals carried are provided in the "Diagram" section following the Power Distribution diagrams.

Grid Coordinate System

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinates of each component on the circuit board illustration.

Near each circuit board illustration is an alphanumeric listing of all components mounted on that board. The second column in each listing identifies the schematic diagram on which each component can be found. These component-locator tables are especially useful when more than one schematic diagram is associated with a particular circuit board.

Troubleshooting Charts

The troubleshooting charts contained in the "Diagrams" section are to be used as an aid in locating malfunctioning circuitry. To use the charts, begin with the Preliminary Tests flowchart. This chart will help identify problem areas and will direct you to other appropriate charts for further troubleshooting.

Some malfunctions, especially those involving multiple simultaneous failures, may require more elaborate troubleshooting approaches with references to circuit descriptions in the "Theory of Operation" section of this manual.

Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located on the color-coding illustration (Figure 9-1) at the beginning of the "Diagrams" section.

RESISTOR COLOR CODE. Resistors used in this instrument are carbon-film, composition, or precision metal-film types. They are usually color coded with the EIA color code; however, some metal-film type resistors may have the value printed on the body. The color code is interpreted starting with the stripe nearest to one end of the resistor. Composition resistors have four stripes; these represent two significant digits, a multiplier, and a tolerance value. Metal-film resistors have five stripes representing three significant digits, a multiplier, and a tolerance value.

CAPACITOR MARKINGS. Capacitance values of common disc capacitors and small electrolytics are marked on the side of the capacitor body. White ceramic capacitors are color coded in picofarads, using a modified EIA code.

Dipped tantalum capacitors are color coded in microfarads. The color dot indicates both the positive lead and the voltage rating. Since these capacitors are easily destroyed by reversed or excessive voltage, be careful to observe the polarity and voltage rating when replacing them.

DIODE COLOR CODE. The cathode end of each glass-encased diode is indicated by either a stripe, a series of stripes or a dot. For most diodes marked with a series of stripes, the color combination of the stripes identifies three digits of the Tektronix Part Number, using the resistor color-code system. The cathode and anode ends of a metal-encased diode may be identified by the diode symbol marked on its body.

Semiconductor Lead Configurations

Figure 9-2 in the "Diagrams" section shows the lead configurations for semiconductor devices used in the instrument. These lead configurations and case styles are typical of those used at completion of the instrument design. Vendor changes and performance improvement changes may result in changes of case styles or lead configurations. If the device in question does not appear to match the configuration shown in Figure 9-2, examine the associated circuitry or consult a manufacturer's data sheet.

Multipin Connectors

Multipin connector orientation is indexed by two triangles; one on the holder and one on the circuit board. Slot numbers are usually molded into the holder. When a connection is made to circuit board pins, ensure that the index on the holder is aligned with the index on the circuit board (see Figure 6-1).

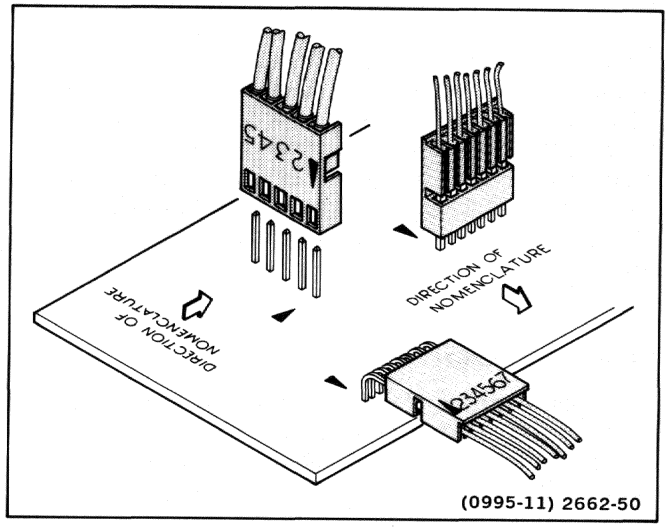


Figure 6-1. Multipin connector orientation.

TROUBLESHOOTING EQUIPMENT

The equipment listed in Table 4-1 of this manual, or equivalent equipment, may be useful when troubleshooting this instrument.

TROUBLESHOOTING TECHNIQUES

The following procedure is arranged in an order that enables checking simple trouble possibilities before requiring more extensive troubleshooting. The first two steps use di-

agnostic aids inherent in the instrument's operating firmware and will locate many circuit faults. The next four procedures are check steps that ensure proper control settings, connections, operation, and adjustment. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, replace it using the appropriate replacement procedure given under "Corrective Maintenance" in this section.

CAUTION

Before using any test equipment to make measurements on static-sensitive, current-sensitive, or voltage-sensitive components or assemblies, ensure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

1. Power-up Tests

The 2445 performs automatic verification of much of the instrument's circuitry when power is first applied. The "Kernel" tests verify proper operation of the Microprocessor, the ROM, and the RAM. If all Kernel tests pass, a second level of checks, the "Confidence" tests, are performed. The Confidence tests, when passed, give the user a high degree of assurance that the instrument is functioning properly.

If a Kernel test or Confidence test fails, the area of failure is identified either by a message on the crt (if the instrument is able to produce a display) or by an error code displayed on the front-panel LED indicators. If a failure occurs, refer to the "Diagnostic Routines" discussion later in this section for definitions of error messages and LED error codes.

Once a problem area has been identified, the associated troubleshooting procedure should be performed to further isolate the problem. The troubleshooting procedures are located on tabbed-foldout pages in the "Diagrams" section at the rear of this manual.

2. Diagnostic Tests and Exerciser Routines

Each of the tests automatically performed at power up, along with several other circuit exercising routines, may be individually selected by the user to further clarify the nature of a suspected failure. The desired test or exerciser is selected by "scrolling" through a menu of the available routines when under control of the "Diagnostic Monitor." Entry into the Diagnostic Monitor and its uses are explained in the "Diagnostic Routines" discussion later in this section.

3. Check Control Settings

Incorrect control settings can give a false indication of instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the "Operating Information" in Section 2 of this manual or to the 2445 Operators Manual.

4. Check Associated Equipment

Before proceeding, ensure that any equipment used with the 2445 is operating correctly. Verify that input signals are properly connected and that the interconnecting cables are not defective. Check that the ac-power-source voltage to all equipment is correct.

5. Visual Check

Perform a visual inspection. This check may reveal broken connections or wires, damaged components, semiconductors not firmly mounted, damaged circuit boards, or other clues to the cause of an instrument malfunction.

6. Check Instrument Performance and Adjustment.

Check the performance of either those circuits where trouble appears to exist or the entire instrument. The apparent trouble may be the result of misadjustment. Complete performance check and adjustment instructions are given in Sections 4 and 5 of this manual.

7. Isolate Trouble to a Circuit

To isolate problems to a particular area, use any symptoms noticed to help locate the trouble. Refer to the troubleshooting charts in the "Diagrams" section as an aid in locating a faulty circuit.

When trouble symptoms appear in more that one circuit, first check the power supplies; then check the affected circuits by taking voltage and waveform readings. Check first for the correct output voltage of each individual supply. These voltages are measured between the power supply test points and ground (see schematic diagrams 8, 9, and 10, and associated circuit board illustrations in the "Diagrams" section). If the power-supply voltages and ripple are within the listed ranges, the supply can be assumed to be working correctly. If they are outside the range, the supply may be either misadjusted or operating incorrectly.

The Low Voltage Power Supply levels are interdependent. All the low voltage supplies use the +10 V reference for their reference levels. If more that one of the low voltage supplies appears defective, repair them in the following order: +10 V REF, +5 V Digital, +87 V, +42 V, +15 V, +5 V Analog, −15 V, −8 V, and −5 V.

A defective component elsewhere in the instrument can create the appearance of a power-supply problem and may also affect the operation of other circuits. Use the power supply troubleshooting charts to aid in locating the problem.

8. Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, again check for loose or broken connections, improperly seated semiconductors, and heat-damaged components.

9. Check Voltages and Waveforms

Often the defective component can be located by checking circuit voltages or waveforms. Typical voltages are listed on the schematic diagrams. Waveforms indicated on the schematic diagrams by hexagonal-outlined numbers are shown adjacent to the diagrams. Waveform test points are shown on the circuit board illustrations.

NOTE

Voltages and waveforms indicated on the schematic diagrams are not absolute and may vary slightly between instruments. To establish operating conditions similar to those used to obtain these readings, see the voltage and waveform setup conditions preceding the waveform illustrations.

Note the recommended test equipment, front-panel control settings, voltage and waveform conditions, and cable-connection instructions. Any special control settings required to obtain a given waveform are noted under the waveform illustration. Changes to the control settings from the initial setup, other than those noted, are not required.

10. Check Individual Components

The following procedures describe methods of checking individual components. Two-lead components that are soldered in place are most accurately checked by first disconnecting one end from the circuit board. This isolates the measurement from the effects of the surrounding circuitry. See Figure 9-1 for component value identification and Figure 9-2 for semiconductor lead configurations.

WARNING

To avoid electric shock, always disconnect the instrument from the ac power source before removing or replacing components.

CAUTION

When checking semiconductors, observe the static-sensitivity precautions located at the beginning of this section.

TRANSISTORS. A good check of a transistor is actual performance under operating conditions. A transistor can most effectively be checked by substituting a known-good component. However, be sure that circuit conditions are not such that a replacement transistor might also be damaged. If substitute transistors are not available, use a dynamic-type transistor checker for testing. Static-type transistor checkers are not recommended, since they do not check operation under simulated operating conditions.

When troubleshooting transistors in the circuit with a voltmeter, measure both the emitter-to-base and emitter-to-collector voltages to determine whether they are consistent with normal circuit voltages. Voltages across a transistor may vary with the type of device and its circuit function.

Some of these voltages are predictable. The emitter-to-base voltage for a conducting silicon transistor will normally range from 0.6 V to 0.8 V. The emitter-to-collector voltage for a saturated transistor is about 0.2 V. Because these values are small, the best way to check them is by connecting a sensitive voltmeter across the junction rather than comparing two voltages taken with respect to ground. If the former method is used, both leads of the voltmeter must be isolated from ground.

If voltage values measured are less that those just given, either the device is shorted or no current is flowing in the external circuit. If values exceed the emitter-to-base values given, either the junction reverse biased or the device is defective. Voltages exceeding those given for typical emitter-to-collector values could indicate either a nonsaturated device operating normally or a defective (open-circuited) transistor. If the device is conducting, voltage will be developed across the resistors in series with it; if open, no voltage will be developed across the resistors unless current is being supplied by a parallel path.

CAUTION

When checking emitter-to-base junctions, do not use an ohmmeter range that has a high internal current. High current may damage the transistor. Reverse biasing the emitter-to-base junction with a high current may degrade the current-transfer ratio (Beta) of the transistor.

A transistor emitter-to-base junction also can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The junction resistance should be very high in one direction and much lower when the meter leads are reversed.

When troubleshooting a field-effect transistor (FET), the voltage across its elements can be checked in the same manner as previously described for other transistors. However, remember that in the normal depletion mode of operation, the gate-to-source junction is reverse biased; in the enhanced mode, the junction is forward biased.

INTEGRATED CIRCUITS. An integrated circuit (IC) can be checked with a voltmeter, test oscilloscope, or by direct substitution. A good understanding of circuit operation is essential when troubleshooting a circuit having IC components. Use care when checking voltages and waveforms around the IC so that adjacent leads are not shorted together. An IC test clip provides a convenient means of clipping a test probe to an IC.

HYBRIDS. Hybrid components can best be checked by observing voltages and waveforms on the circuit board. Measurements should not be made on any hybrid component while out of the circuit as they may easily be damaged. Direct substitution is the best troubleshooting method when a hybrid failure is suspected.

CAUTION

When checking a diode, do not use an ohmmeter scale that has a high internal current. High current may damage a diode. Checks on diodes can be performed in much the same manner as those on transistor emitter-to-base junctions. Do not check tunnel diodes or back diodes with an ohmmeter; use a dynamic tester, such as the TEKTRONIX 576 Curve Tracer.

DIODES. A diode can be checked for either an open or a shorted condition by measuring the resistance between terminals with an ohmmeter set to a range having a low internal source current, such as the R X 1 kΩ range. The diode resistance should be very high in one direction and much lower when the meter leads are reversed.

Silicon diodes should have 0.6 to 0.8 V across their junctions when conducting. Higher readings indicate that they are either reverse biased or defective, depending on polarity.

RESISTORS. Check resistors with an ohmmeter. Refer to the "Replaceable Electrical Parts" list for the tolerances of resistors used in this instrument. A resistor normally does not require replacement unless its measured value varies widely from its specified value and tolerance.

INDUCTORS. Check for open inductors by checking continuity with an ohmmeter. Shorted or partially shorted inductors can usually be found by check the waveform response when high-frequency signals are passed through the circuit.

CAPACITORS. A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter set to one of the highest ranges. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after the capacitor is charged to the output voltage of the ohmmeter. An open capacitor can be detected with a capacitance meter or by checking whether the capacitor passes ac signals.

ATTENUATORS. The Attenuators are built as complete assemblies and should not be taken apart. If an Attenuator is suspected as having failed, direct substitution is the recommended troubleshooting method.

11. Repair and Adjust the Circuit.

If any defective parts are located, follow the replacement procedures given under "Corrective Maintenance" in this section. After any electrical component has been replaced, the performance of that circuit and any other closely related circuit should be checked. Since the power supplies affect all circuits, performance of the entire instrument should be checked if work has been done on the power supplies or if the power transformer has been replaced. Readjustment of the affected circuitry may be necessary . Refer to the "Performance Check" and "Adjustment Procedure", Sections 4 and 5 of this manual.

DIAGNOSTIC ROUTINES

The diagnostic routines contained in the 2445 operating firmware consist of the various power-up tests that are automatically performed when power is first applied and several circuit exerciser routines. The test or exerciser routines are selected by "scrolling" through a menu of available routines when the firmware is under control of the Diagnostic Monitor. Monitor control is indicated by the message "DIAGNSTIC. PUSH A/B TRIG TO EXIT" displayed in the top crt graticule division.

Entry into the monitor is automatic if a power-up test fails. The user may also force entry into the Diagnostic Mon-

itor from the normal operating mode by holding in the front-panel ΔV and Δt push buttons and then pressing the front-panel SLOPE push button. Exiting the monitor is accomplished by pressing in the A/B TRIG push button, as instructed by the crt readout display.

Depending on how the Diagnostic Monitor was entered (from normal mode or as a result of a power-up test failure), the first menu item displayed may vary; entry into the monitor from the normal mode begins at ALL TESTS while entry from power up starts at the first failed test. Since, in a failure mode, the crt readout may not be able to display the selected menu item, the VERT TRIGGER SOURCE indicator illuminates as a reference when ALL TESTS is selected. With the VERT TRIGGER SOURCE indicator illuminated, the user may scroll to the desired test or exerciser routine using the test order called out in Table 6-4. Whether the menu is displayed or not, scrolling is accomplished by pressing the front-panel TRIGGER MODE switch either up to increment or down to decrement the menu position by one.

Table 6-4

Sequence of Diagnostic Tests and Exerciser Routines

Routine Type	Type Number	Routine Name	Error Code	Error Code Meaning
All Tests[a]	00	All	ZZ	The left digit is the option number and the right digit is the test number of the first failing test of the last ALL TESTS run. When looping, it shows the last failing test.
Test	01	Interrupt Request	01	Interrupt request is missing or has wrong period.
Test	02	Switch Stuck	01	Trigger COUPLING down.
			02	Trigger COUPLING up.
			08	CH 1 Coupling down.
			10	CH 1 Coupling up.
			28	CH 2 Coupling down.
			30	CH 2 Coupling up.
			44	Δ t (delta time).
			48	Δ V (delta volts).
			50	Trigger SLOPE
			61	Trigger SOURCE down.
			62	Trigger SOURCE up.
			64	Trigger MODE down.
			68	Trigger MODE up.
			70[b]	A/B TRIG select.
Test	03	Readout Board	01	Shift register failure.
			02	Readout RAM failure.
Test	04	EAROM	X1	Parity error on read (bit 0 set).
			X8	Bad read after write (bit 3 set).
			1X	Bad checksum (bit 4 set).
Test	05	Main Board	01	AUTO LVL failed to trigger.
			X2	Negative level not negative enough.
			X4	Negative level too negative.
			2X	Positive level not positive enough.
			4X	Positive level too positive.
Exerciser	01	Pots and Switches	None	
Exerciser	02	EAROM Examine	None	
Exerciser	03	Cycle Error Clear	None	
Exerciser	04	Display ROM Headers	None	

[a]VERT TRIG SOURCE indicator lights when in ALL TESTS as a visual reference in the event a crt display can not be produced.

[b]If the A/B TRIG switch is stuck on power up, the oscilloscope will branch to "normal" operation after a short delay. The associated error message will only be visible momentarily if the crt is warmed-up.

Routine Control

When the desired Test or Exerciser has been selected, the operator has two types of control that may be exercised over the routine: START/STOP and LOOP.

Starting or stopping the execution of the selected routine is controlled by the front-panel TRIGGER COUPLING switch. Pressing the switch up starts the routine; pressing it down stops it.

All of the test routines, except EAROM—TEST 04, may be set to LOOP mode (continuously repeated) by pressing the front-panel TRIGGER SOURCE switch up while the routine is selected but not executing. The LOOP feature will cause the routine to be continuously repeated once started until stopped when the operator presses the COUPLING switch down. Once the routine is stopped, the LOOP feature may be disabled by pressing the SOURCE switch down.

While a Test or Exerciser routine is executing, the Diagnostic Monitor Control message on the top line of the crt display will be cleared as an indication that a routine is running. When test routines are looping, the message "LOOP" is displayed in the bottom division of the crt graticule.

Display Format

The Tests and Exercisers routines display information about the routine type and number, as well as any test results, at the bottom of the crt display. The readout line is formatted as follows:

OD TYPE XY STATUS ZZ LOOP OD<ABCC>

The information is defined as follows:

"OD" is a two-character option designator identifying the option that this particular line of diagnostic information refers to (see Options manual for details). For the basic instrument, the OD location is blank.

"TYPE" refers to routine type: All Tests (ALL), Test (TEST), Exerciser (EXER), or Calibration (CAL).

"X" indicates which bit of the "Option Select Register" is set to turn on the option called out by "OD" (see Options manual for description of Options Select Register). This bit is zero for the basic instrument.

"Y" is the TYPE number of the routine (see the "Type Number" column of Table 6-4).

"STATUS" shows the results of the last time a selected test routine ran: either PASS or FAIL. This space is blank for exerciser and calibration routines. When the diagnostics are called up from normal operating mode, the space will be blank until the selected test is executed.

"ZZ" is a two-digit error code identifying the nature of the failure in a failed test (see the "Error Code" column of Table 6-4).

"LOOP" indicates when a selected test is set to the LOOP mode.

"OD<ABCC>" is the CYCLE mode failure indicator. When the CYCLE mode is activated (see CYCLE ERROR CLEAR description), data will be written to the EAROM about the first test failure that occurs. This information will be displayed until the operator performs the CYCLE ERROR CLEAR routine (Exerciser 03). The information displayed is an abbreviated version of the previous items:

"OD" is a two-character option designator showing which option failed first while in the CYCLE mode (the same codes as for "OD" at the start of the readout line).

"A" identifies the option-select bit for the failing option (the same code as for "X").

"B" is the test Type Number where the failure occurred (the same codes as for "Y").

"CC" is the error code for the test (the same codes as for "ZZ").

Kernel Tests

The Kernel tests are those tests which, when failed, are considered "fatal" to the operation of the Microprocessor. Failure of a Kernel test will cause the front-panel TRIG'D indicator to flash, and certain of the other front-panel indicators will be illuminated with an error code. The code points to the area of failure as indicated in Table 6-5. Tables 6-6 and 6-7 are used to determine the option and device numbers used in Table 6-5. Only the basic instrument codes are given in Table 6-5. Option codes are defined in the "Options Service Manual."

Table 6-5
Kernel Test Failure Codes

Failure Codes		
Option	**Device**	**Failing Device**
0	0	Control Board RAM
0	1	ROM at E000 (hex)
0	2	ROM at C000 (hex)
0	3	ROM at A000 (hex)
0	4	ROM at 9000 (hex)

Table 6-6
Front-Panel LED Option Codes

Option Code					
CH 1 LED (bit 3)	**CH 2 LED (bit 2)**	**CH 3 LED (bit 1)**	**CH 4 LED (bit 0)**	**Option Number (in hex)**	**Option Name**
OFF	OFF	OFF	OFF	0	Basic Instrument
ON	ON	ON	ON	F	Options Buffer Board

Table 6-7
Front-Panel LED Device Codes

	Device Code		
READY LED (bit 2)	**+ LED (bit 1)**	**− LED (bit 0)**	**Device Number**
OFF	OFF	OFF	0
OFF	OFF	ON	1
OFF	ON	OFF	2
OFF	ON	ON	3
ON	OFF	OFF	4
ON	OFF	ON	5
ON	ON	OFF	6
ON	ON	ON	7

Even if a Kernel test fails, the operator may try to go to normal oscilloscope operation by pressing the A/B TRIG select push button. Depending on the exact nature of the failure, the instrument may or may not be functional.

Kernel tests are automatically executed at power up. The Kernel tests are divided into RAM tests and ROM tests as follows:

RAM TEST. This test is a complete march test. The RAM is first filled with zeros. The first location is then read, checking that only zeros are present. (In later cycles this ensures that a previous write hasn't written to the location.) A "1" is walked through each bit of the addressed location and read back after each write to ensure only one bit at a time changes. Each of the succeeding address locations is read, then written to in the same way until the RAM is filled with ones. After the RAM is filled, a "0" is walked through each bit location in a similar manner.

Test checks: RAM address decoding, RAM address lines, RAM data lines, and Data Bus Buffers.

ROM TEST. The ROM test performs three checks on each of the system read-only memories.

Data Bus Drive—Two locations containing complementary data patterns are read.

Test checks: Data bus lines and the Data Bus Driver.

Correct Part—A byte in the ROM being checked is compared to the most-significant byte of the addressed ROM block (starting address of where the ROM should be installed).

Test checks: ROM address decoding and proper installation of ROM components.

Checksum—A sixteen bit, spiral-add checksum is calculated and compared to a two-byte value stored in ROM being checked.

Test checks: ROM contents, ROM addressing, ROM data lines, and the Data Bus Driver.

Confidence Tests

The Confidence tests provide checks for much of the remaining circuitry to ensure that instrument operation is correct. Confidence tests are performed automatically at power up after the Kernel is determined to be functional or initiated by the operator from the Diagnostic Monitor.

A failure of any Confidence test during power up will pass control to the Diagnostic Monitor; this permits the test results to be examined. Descriptions of the Confidence tests follow.

INTERRUPT REQUEST (Test 01). Ten consecutive interrupt cycles are checked to ensure that succeeding interrupts occur not more than 4.5 ms apart (5600 "E" cycles).

Test checks: Interrupt Timer circuitry.

SWITCH STUCK (Test 02). The front-panel, momentary-contact switches are scanned, checking for a closed switch. At power up, the test runs immediately.

By holding one of the momentary switches in a closed position when power is first applied, this test will fail, and the Diagnostic Monitor will be entered. When the test is started from the Diagnostic Monitor, a one-half second delay is incorporated to allow the COUPLING (test start) switch to return to its normal (open) position. Table 6-4 defines the error codes that may be encountered when a switch is detected as closed.

NOTE

When the user presses the COUPLING switch to stop this test, an error code may be generated. This is normal and does not indicate an actual failure.

Test checks: Momentary switches, row scanning circuitry, and column scanning circuitry.

READOUT BOARD (Test 03). This two-part test checks the interface to the Readout Board from the Microprocessor and the character RAM circuits.

Processor Interface Test—The Microprocessor loads the three, eight-bit shift registers with an alternating bit pattern that is then shifted back to the processor for comparison.

Test checks: Data Registers, data strobes (clocks), and the data input and output lines.

RAM Test—A "1" is rotated through each byte of the Readout RAM, one bit at a time. Each time an additional bit is rotated into the byte, the byte is loaded into the processor interface and clocked back to the processor for comparison. The byte is then restored to its original content, and each successive byte is tested in the same manner.

Test checks: Readout RAM addressing, Readout RAM data lines, and RAM read/write capability.

EAROM (Test 04). Three checks are performed on the EAROM to verify its contents and the interface circuitry.

Read/Write Test—The contents of one location are read, modified, and then reread to verify functioning of the device interface.

Test checks: EAROM input and output lines, EAROM mode control, EAROM reading and writing, and the EAROM clock.

Checksum Test—The contents of locations containing calibration constants are checksummed using a sprial-add technique. The result is compared to the contents of location 0 (the checksum generated at the time of calibration).

Test checks: EAROM addressing and EAROM contents.

Parity Test—As each of the calibration constants is read for the Checksum test above, the parity of each 14-bit word is checked.

Test checks: EAROM data retention and EAROM reading.

MAIN BOARD (Test 05). The AUTO LVL triggering feature (a routine stored in firmware) is operated to detect the peaks of a Line Trigger signal. Detected peaks are compared to expected values to verify operation (and calibration) of interrelated signal processing circuits.

Test checks: Line Trigger source, the A Trigger generation circuitry, and Control DAC U2234 (located on the Control board).

Exerciser Routines

The Exerciser routines allow the operator to set and examine various bytes of control data used in determining instrument function.

POTS AND SWITCHES (Exerciser 01). This routine displays the values that the Microprocessor detects as the various digitized pots and switches are activated. The top line of the crt display has the following format:

AA BB CC DEEE FF GG HI JJ KL

The format is defined as follows:

"AA" is the code of the most-recently-activated potentiometer (see Table 6-8 for definition of pot codes).

"BB" is the current value (in hexadecimal) of pot AA.

"CC" is the previous value (in hexadecimal) of pot AA.

"D" is the DAC Multiplexer code used to select pot AA (see Table 6-9).

"EEE" is the DAC value (in hexadecimal) associated with pot AA.

"FF" is the code of the previously-activated potentiometer (see Table 6-8).

"GG" is the row code of the most-recently-activated switch (see Table 6-10 for definition of row codes).

"H" is the switch-position code: 0 for open; C for closed.

"I" is the column code of the most-recently-activated switch (see Table 6-10).

"JJ" is the row for for the previously-activated switch.

"K" is the switch-position code: 0 for open; C for closed.

"L" is the column code for the previously-activated switch.

NOTE

For all momentary switches (except A/B TRIG) only the closed position will be shown in the switch-position code locations (H and K). The A/B TRIG switch has both the open and the closed positions shown.

Table 6-8

Potentiometer Code Numbers

Code Number	Potentiometer
01	HOLDOFF
02	Trigger LEVEL
03	SEC/DIV VAR
04	Horizontal POSITION
05	Δ (A section)
06	Δ (B section)
07	Δ REF OR DLY POS (A section)
08	Δ REF OR DLY POS (B section)
09	CH 1 VOLTS/DIV VAR
0A	CH 2 VOLTS/DIV VAR

Table 6-9

DAC Multiplexer "D" Codes

D Code	Control Indicated
0	CH 1 VOLTS/DIV VAR
1	A SEC/DIV VAR
2	CH 2 VOLTS/DIV VAR
3	A Trigger LEVEL
5	Horizontal POSITION
6	HOLDOFF

NOTE

In the case of the Δ REF OR DLY POS and Δ controls, the D code position shows the two most-significant bits of the 14-bit DAC output (in hexadecimal).

Table 6-10

Pots and Switches Column and Row Code Definitions

Row Code	Column Code	Definition	Row Code	Column Code	Definition
0	0	Trig COUPLING Down	5	0	B SEC/DIV LSB
0	1	Trig COUPLING Up	5	1	B SEC/DIV Bit 2
0	2	Unused	5	2	B SEC/DIV Bit 3
0	3	CH 1 Coupling Down	5	3	B SEC/DIV Bit 4
0	4	CH 1 Coupling Up	5	4	B SEC/DIV MSB
1	0	CH 4 VOLTS/DIV	6	0	CH 1 VERT MODE
1	1	CH 3 VOLTS/DIV	6	1	CH 2 VERT MODE
1	2	Unused	6	2	ADD VERT MODE
1	3	CH 2 Coupling Down	6	3	CH 3 VERT MODE
1	4	CH 2 Coupling Up	6	4	CH 4 VERT MODE
2	0	CH 1 VOLTS/DIV LSB	7	0	Unused
2	1	CH 1 VOLTS/DIV Bit 2	7	1	B ENDS A
2	2	CH 1 VOLTS/DIV Bit 3	7	2	Unused
2	3	CH 1 VOLTS DIV MSB	7	3	CHOP/ALT
2	4	CH 2 INVERT	7	4	BW LIMIT
3	0	CH 2 VOLTS/DIV LSB	8	0	X10 MAG
3	1	CH 2 VOLTS/DIV Bit 2	8	1	TRACKING/INDEP
3	2	CH 2 VOLTS/DIV Bit 3	8	2	Δ t
3	3	CH 2 VOLTS/DIV MSB	8	3	ΔV
3	4	Horiz Display Select	8	4	Trig SLOPE
4	0	A SEC/DIV LSB	9	0	Trig SOURCE Down
4	1	A SEC/DIV Bit 2	9	1	Trig SOURCE Up
4	2	A SEC/DIV Bit 3	9	2	Trig MODE Down
4	3	A SEC/DIV Bit 4	9	3	Trig MODE Up
4	4	A SEC/DIV MSB	9	4	A/B TRIG Select

EAROM EXAMINE (Exerciser 02). This routine allows the operator to examine the contents of any or all EAROM locations. The EAROM has 100 (decimal) locations (63 hexadecimal). Addresses above 63 (hex) are not defined. When entered, the Exerciser displays the contents of EAROM location 00 (hex) on the top line of the crt display. Calibration constants reside between addresses 01 (hex) and 4C (hex) and each should have odd parity as explained below. The remaining locations may be of either parity. The readout display line has the following format:

AA DDDD P

The format is defined as follows:

"AA" is the eight-bit address in hexadecimal notation.

"DDDD" is the 14-bit word stored at that location (13 bits of data and one parity bit).

"P" is a parity indicator for the data word: X indicates even parity; blank is odd parity.

Pushing the MODE switch up or down will increment or decrement the EAROM address by 16 (10 hex) respectively. Similarly, pushing the SOURCE switch up or down will increment or decrement the address by 1 respectively.

CYCLE ERROR CLEAR (Exerciser 03). This routine provides a way for the operator to clear the cycle-failure data written to the EAROM when a CYCLE mode failure occurs. Until the data is cleared, each time the instrument is powered up, the Diagnostic Monitor is entered and a diagonal line is display across the crt.

CYCLE mode, when entered by removing the CAL/NO CAL jumper (P501), causes the instrument to continuously

LOOP through the Power Up Diagnostic Tests (except for EAROM—Test 04). If a failure occurs, the cycle-failure data, identifying the first failure encountered, is written to a specific location in the EAROM. Thereafter, at each power up, the Diagnostic Monitor is automatically entered, and the failure data is displayed even when the instrument is returned to the normal operating configuration (CAL/NO CAL jumper in the NO CAL position). Intepretation of the cycle failure data is explained in the "Display Format" description provided earlier in this section. The error data must be cleared from the EAROM location to eliminate the CYCLE mode error display.

Clearing the EAROM location is done by scrolling to the EAROM CLEAR exerciser and pressing the following switches in sequence:

COUPLING up (starts exerciser),
SOURCE down,
MODE down, then
COUPLING down.

When the EAROM CLEAR routine is successfully executed, the cycle failure data and the diagonal line will disappear from the display.

DISPLAY ROM HEADERS (Exerciser 04). This routine displays the Standard Tektronix ROM Header of each system ROM on the top line of the crt display. The readout line has the following format:

CCCC PPPP SS AAAA

The definition of the format is as follows:

"CCCC" is a two-byte hexadecimal checksum.

"PPPP" is the four middle digits of the ROM part number.

"SS" is the suffix of the ROM part number (version number).

"AAAA" is the starting address of the ROM (address where the ROM should be installed).

Pressing the COUPLING switch up increments the routine to the next ROM Header; pressing it down exits the routine.

CONTROLLER LATCHES EXERCISER. This routine is not user selectable, but it runs automatically when the Diagnostic Monitor is waiting for a key activation.

The routine first sets latches U2034 and U2134 (diagram 2). It then pulses the BSWPCLK line (pin 13 of U2596, diagram 1), as a scope trigger, and rotates a "0" through 15 of the 16 latched bits. Bit 16 is not set since it would reset Interrupt Timer U2268 (diagram 1) and upset processor interrupt timing. By externally triggering a test oscilloscope on the BSWPCLK signal line and observing the shifted timing relationships of the latched signals, proper operation of the DAC latches may be verified.

NOP KERNEL EXERCISER. This exerciser is not a firmware routine, but rather a forced hardware condition. It is best suited for troubleshooting an inoperative Control Board, as it exercises only the Microprocessor address bus and the associated Address Decode circuitry. By moving Jumper P503 (diagram 1) to the Diagnostic position, Data Bus Buffers U2194 and U2294 are disabled, and the Microprocessor is forced into a NOP (no operation) loop. This causes the address on the address bus to be continuously incremented for exercising the Address Decode circuitry. Troubleshooting of kernel addressing with an oscilloscope or logic analyzer is then possible.

CORRECTIVE MAINTENANCE

INTRODUCTION

Corrective maintenance consists of component replacement and instrument repair. This part of the manual describes special techniques and procedures required to replace components in this instrument. If it is necessary to ship your instrument to a Tektronix Service Center for repair or service, refer to the "Instrument Repackaging Instructions" at the end of this section.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions.

1. Disconnect the instrument from the ac power source before removing or installing components.

2. Verify that the line-rectifier filter capacitors are discharged prior to performing any servicing.

3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).

4. When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can usually be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., please check the "Replaceable Electrical Parts" list for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, some special parts are used in the 2445. These components are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications. The various manufactures can be identified by referring to the "Cross Index-Manufacturer's Code number to Manufacturer" at the beginning of the "Replaceable Electrical Parts" list. Many of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., be sure to include all of the following information:

1. Instrument type (include modification or option numbers).

2. Instrument serial number.

3. A description of the part (if electrical, include its full circuit component number)

4. Tektronix part number.

MAINTENANCE AIDS

The maintenance aids listed in Table 6-11 include items required for performing most of the maintenance procedures in this instrument. Equivalent products may be substituted for the examples given, provided their characteristics are similar.

Table 6-11

Maintenance Aids

Description	Specification	Usage	Example
1. Soldering Iron	15 to 25 W.	General soldering and unsoldering.	Antex Precision Model C.
2. Flat-bit Screwdriver	3-inch shaft, 3/32-inch bit.	Assembly and disassembly.	Xcelite Model R3323.
3. Torx Screwdriver	Tip sizes: #T9, #T10, #T15, #T20.	Assembly and disassembly.	Tektronix Part Numbers #T9 003-0965-00 #T10 003-0815-00 #T15 003-0966-00 #T20 003-0866-00
4. Nutdrivers	3/16 inch, 1/4 inch.	Assembly and disassembly	Xcelite #6 and #8.
5. Open-end Wrenches	1/4 inch, 5/16 inch, 7/16 inch	Assembly and disassembly.	
6. Allen Wrenches	0.050 inch, 1/16 inch	Assembly and disassembly.	
7. Long-nose Pliers		Component removal and replacement.	Diamolloy Model LN55-3.
8. Diagonal Cutters		Component removal and replacement.	Diamalloy Model M554-3.
9. Vacuum Solder Extractor	No static charge retention.	Unsoldering static sensitive devices and components on multilayer boards.	Pace Model PC-10.
10. Spray Cleaner	No-Noise	Switch and Pot cleaning.	Tektronix Part Number 006-0442-02.
11. Pin-replacement Kit		Replace circuit board connector pins	Tektronix Part Number 040-0542-01.
12. IC-Removal Tool		Removing DIP IC packages.	Augat T114-1.
13. Isopropyl Alcohol	Reagent grade.	Cleaning attenuator and front panel assemblies.	2-Isopropanol.

INTERCONNECTIONS

Interconnection in this instrument are made with pins soldered onto the circuit boards. Several types of mating connectors are used for the interconnecting pins. The following information provides the replacement procedures for the various type connectors.

End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnect pins are factory assembled. They consist of machine-inserted pin connectors mounted in plastic holders. If the connectors are faulty, the entire wire assembly should be replaced.

Multipin Connectors

When pin connectors are grouped together and mounted in a plastic holder, they are removed, reinstalled, or replaced as a unit. If any individual wire or connector in the assembly is faulty, the entire cable assembly should be replaced. To provide correct orientation of a multipin connector, an index arrow is stamped on the circuit board, and either a matching arrow is molded into or the numeral 1 is marked on the plastic housing as a matching index. Be sure these index marks are aligned with each other when the multipin connector is reinstalled.

TRANSISTORS, INTEGRATED CIRCUITS, AND HYBRID CIRCUITS

Transistors, integrated circuits, and hybrid circuits should not be replaced unless they are actually defective. If removed from their sockets or unsoldered from the circuit board during routine maintenance, return them to their original board locations. Unnecessary replacement or transposing of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check the performance of any circuit that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend transistor leads to fit their circuit board holes, and cut the leads to the same length as the original component. See Figure 9-2 in the "Diagrams" section for lead-configuration illustrations.

The heat-sink-mounted power supply transistors are insulated from the heat sink with a heat-transferring insulator pad. Reinstall the insulator pads and bushings when replacing these transistors. Do not use any type of heat-transferring compound on the insulator pads.

NOTE

After replacing a power transistor, check that the collector is not shorted to the heat sink before applying power to the instrument.

To remove socketed dual-in-line packaged (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

To remove a soldered DIP IC when it is going to be replaced, clip all the leads of the device and remove the leads from the circuit board one at a time. If the device must be removed intact for possible reinstallation, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

Hybrid circuits and heatsinks are removed as a unit by removing the mounting nuts at the four corners of the heatsink/housing. A firm downward pressure at the center of the housing will aid in removal of the nuts. The hybrid circuit substrate is bonded to the heatsink/housing casting. Attempting to separate the hybrid device from its housing will damage the device.

SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument.

WARNING

To avoid an electric-shock hazard, observe the following precautions before attempting any soldering: turn the instrument off, disconnect it from the ac power source, and verify that the line-rectifier filter capacitors have discharged. (See label on the primary power shield.) If, due to a component failure, the capacitors are not discharging, it may be necessary to discharge them. Use a 1 kΩ, 5-watt resistor and discharge the capacitors from point to point through the access holes in the primary power shield.

Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuits boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure best heat transfer from the iron tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

Circuit boards in this instrument may have as many as four conductive layers. Conductive paths between the top and bottom board layers may connect to one or more inner

layers. If any inner-layer conductive path becomes broken due to poor soldering practices, the board becomes unusable and must be replaced. Damage of this nature can void the instrument warranty.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument.

Desoldering parts from multilayer circuit boards is especially critical. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

CAUTION

Attempts to unsolder, remove, and resolder leads from the component side of a circuit board may cause damage to the reverse side of the circuit board.

The following techniques should be used to replace a component on a circuit board:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing so may damage the board.

NOTE

Some components are difficult to remove from the circuit board due to a bend placed in the component leads during machine insertion. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board.

2. When removing a multipin component, especially an IC, do not heat adjacent pins consecutively. Apply heat to the pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.

3. Bend the leads of the replacement component to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they protrude only a small amount through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.

4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.

5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.

6. Cut off any excess lead protruding through the circuit board (if not clipped to the correct length in step 3).

7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

8. When soldering to the ceramic crt-termination network, a slightly larger soldering iron can be used. It is recommended that a solder containing about 3% silver be used when soldering to the ceramic material to avoid destroying the the bond. The bond can be broken by repeated use of ordinary tin-lead solder or by the application of too much heat; however, occasional use of ordinary solder will not break the bond, provided excessive heat is not applied when making the connection.

REMOVAL AND REPLACEMENT INSTRUCTIONS

WARNING

To avoid electric shock, disconnect the instrument from the ac power source before removing or replacing any component or assembly.

The exploded view drawing in the "Replaceable Mechanical Parts" list at the rear of this manual may be helpful during the removal and reinstallation of individual components or subassemblies. Circuit board and component locations are illustrated in the "Diagrams" section of this manual.

Cabinet Removal

Removal of the instrument wrap-around cabinet is accomplished by the following steps:

1. Unplug the power cord from the ac power source.

2. Unplug the power cord from the rear-panel connector.

3. Install the front-panel cover, place the cabinet handle against the bottom of the cabinet, and set the instrument face down on a flat surface.

4. Unwrap the power cord from the instrument feet.

5. Remove the four screws in the rear-panel feet (see Figure 6-2).

6. Remove the two screws from the top-center and bottom-center of the rear panel (see Figure 6-2).

7. Lift the rear panel and power cord away from the instrument, leaving the rear-panel feet attached.

WARNING

Dangerous potentials exist at several points throughout this instrument. If it is operated with the cabinet removed, do not touch exposed connections or components. Some transistors may have elevated case voltages. Disconnect the ac power source from the instrument and verify that the line-rectifier filter capacitors have discharged before cleaning the instrument or replacing parts (see label on the primary power shield).

8. Slide the cabinet off of the instrument.

To reinstall the wrap-around cabinet, perform the reverse of the preceding instructions. Ensure that the cabinet fits properly into the emi gasket grooves in the front frame and rear panel.

WARNING

The line-rectifier filter capacitors normally retain a charge for a short period (approximately 15 to 20 seconds) after the instrument is turned off and can remain charged for a longer period if a bleeder-resistor or power-supply problem occurs. Before beginning any cleaning or work on the internal circuitry of the oscilloscope, disconnect the ac power source from the instrument and verify that the capacitors have discharged to 24 V or less. Measurement is made at the three points indicated on the plastic primary input shield at the rear of the instrument (after the Top-Cover Plate is removed). If the capacitors retain charges of greater than 24 V for more than 20 seconds, discharge them using a 1 kΩ, 5-watt resistor connected point-to-point across the capacitors (through the access holes). Ensure that the capacitors are discharged before commencing troubleshooting.

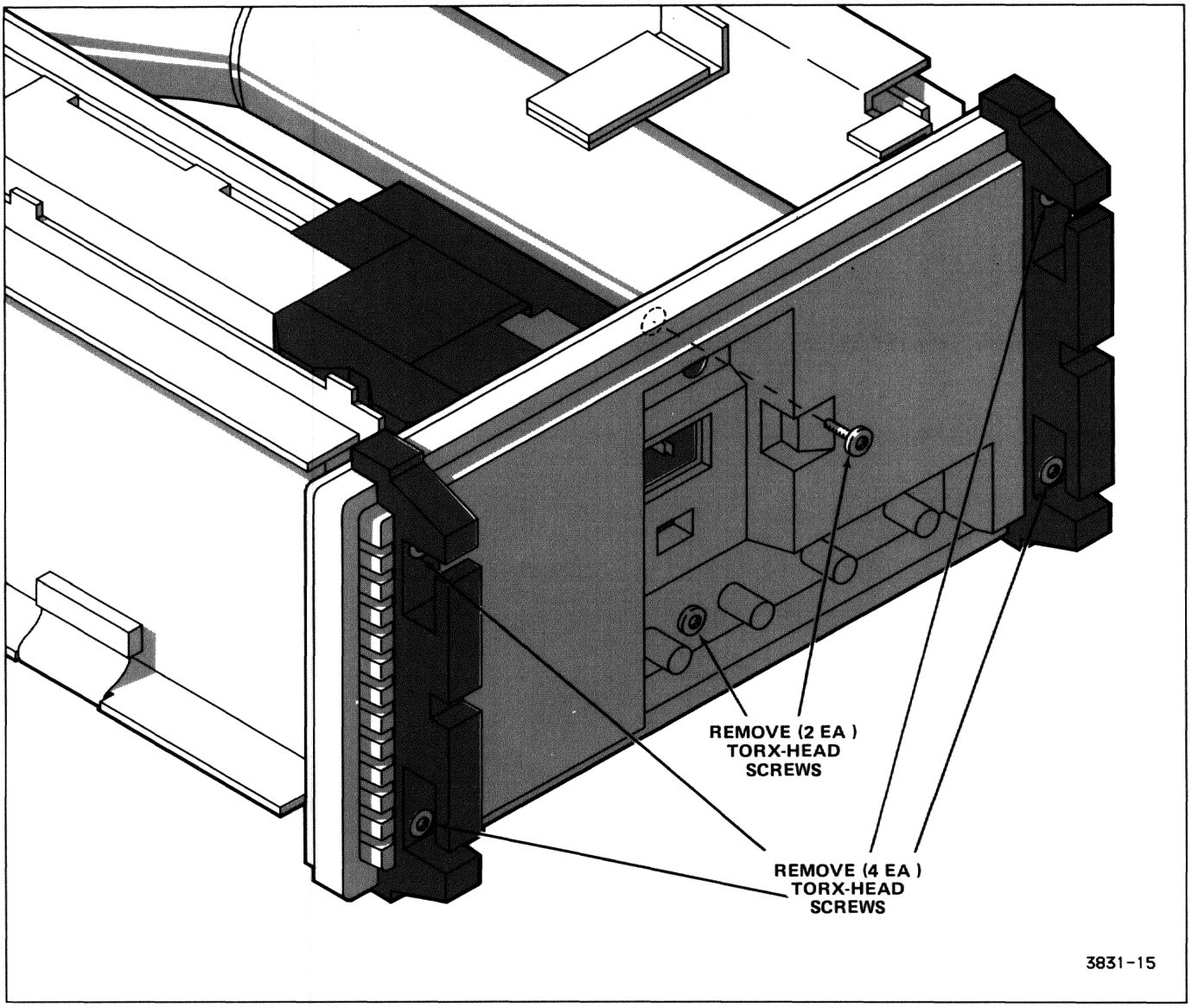


Figure 6-2. Rear panel removal.

Top-Cover Plate Removal

Removal of the Top-Cover Plate is accomplished by the following steps:

1. Remove the instrument cabinet as described in that procedure.

2. Set the instrument, bottom down, on a flat surface.

3. Remove the two securing screws from the top edge of the rear-panel chassis.

4. Remove the securing screw from the left side of the chassis.

5. Remove the two top securing screws at the front edge of the cover plate.

6. Remove the top securing nut at the rear of the cover plate.

7. Lift the Top-Cover Plate up and away from the instrument.

To reinstall the Top-Cover Plate, perform the reverse of the preceding instructions.

A5—Control Board Removal

Removal of the Control Board is accomplished by the following steps:

1. Remove the instrument wrap-around cabinet as described in that procedure.

2. Place the instrument on its left side on a flat surface.

3. Disconnect the three ribbon-cable connectors from the Control board (P251, P651, and P652) (see Figure 6-3).

4. Disconnect the two ribbon-cable connectors from the Main board (P511 and P512).

5. Remove the five mounting screws securing the board to the chassis, one at each corner of the board and one at the center.

6. Lift the Control board away from the chassis.

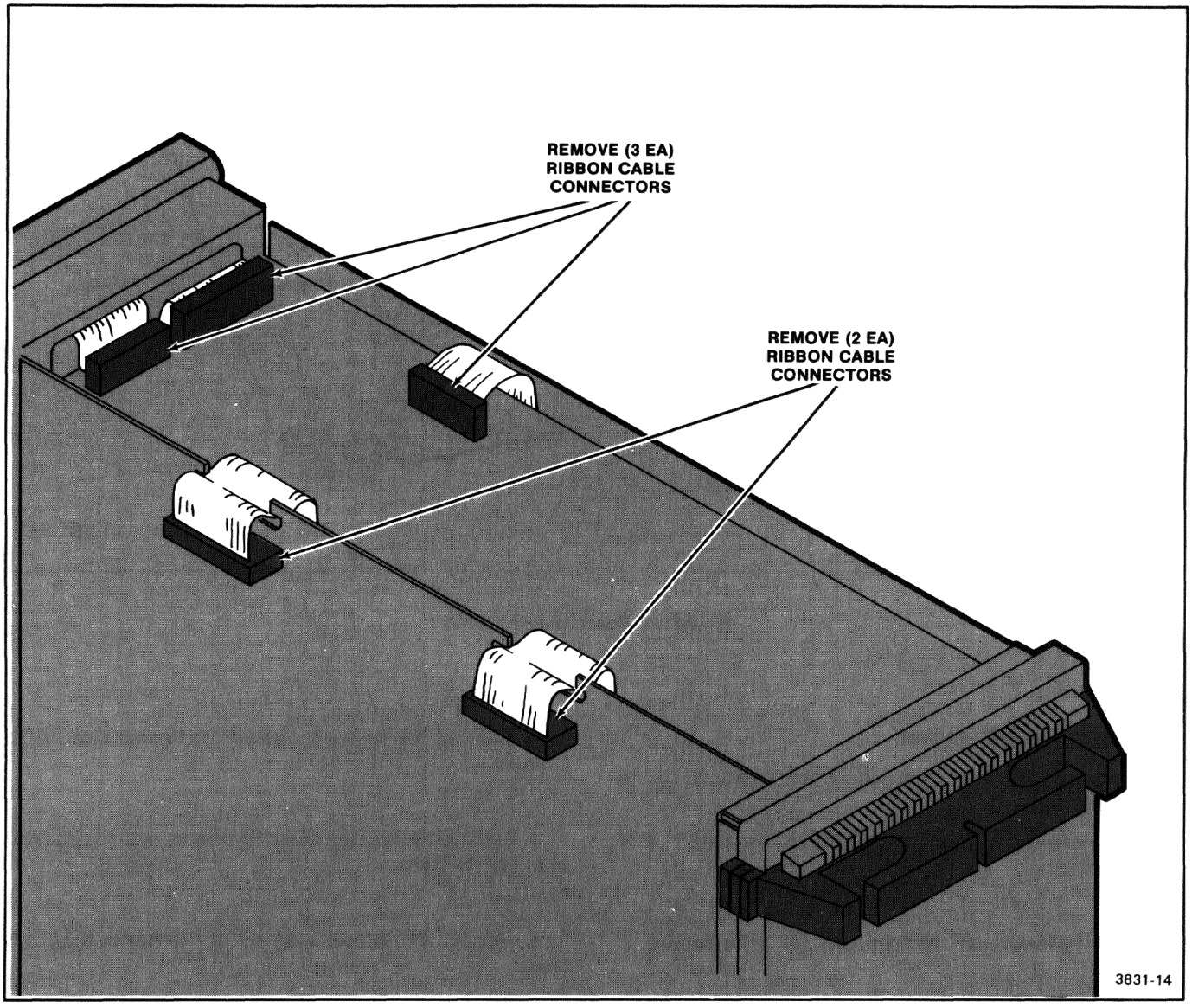


Figure 6-3. Ribbon cable removal.

To reinstall the Control board, perform the reverse of the preceding instructions.

A2, A3, and A12—Power Supply Assembly Removal

Removal of the Power Supply assembly is accomplished by the following steps:

1. Remove the instrument Cabinet as described in that procedure.

2. Remove the Top-Cover Plate as described in that procedure.

3. Loosen, but do not remove, the nut securing the fan blade to the fan motor shaft (a 1/4-inch nut driver is required).

4. Grasp the fan blade and, using firm pressure, pull the fan blade and mounting collar from the motor shaft.

5. Remove the two rear-panel screws holding the plastic primary circuit shield and remove the shield.

6. Remove the two screws holding the rear of the Power Supply assembly to the rear panel.

7. Remove the three screws securing the power-transistor heatsink to the chassis.

8. Disconnect the power supply ribbon-cable connector from the Control board (P251) and feed the cable through the slot in the Control board.

9. Disconnect the two power supply multipin connectors from the Power Supply assembly to the Main board (P121 and P122).

10. Disconnect the four primary power connections at the rear of the supply assembly (P204, P205, P206, and P207). Note their orientation for reinstallation.

11. If the Probe Power option is installed, disconnect the Probe Power connectors from the Power Supply assembly (P201 and P202).

12. Lift the Power Supply assembly from the instrument.

To reinstall the Power Supply assembly, perform the reverse of the preceding instructions.

The following procedures describe the further disassembly of the Power Supply circuit boards once the assembly is removed from the instrument.

FAN REMOVAL. To remove the Fan board and motor from the Power Supply assembly, perform the following steps:

1. Loosen the four screws on the plastic motor mount.

2. Disconnect the multipin connector from the Fan board (P301). Note the connector orientation for reinstallation.

3. Slide the Fan board and motor from the motor mount.

To reinstall the Fan board and motor, perform the reverse of the preceding steps.

INVERTER BOARD AND REGULATOR BOARD SEPARATION. To separate the Inverter and Regulator boards, perform the following steps:

1. Remove the rear-corner securing screw from the Regulator board.

2. Unplug the four thru-pin connectors (J231, J232, J233, and J234).

3. Separate the two circuit boards by unclipping the plastic edge connectors.

To rejoin the Inverter and Regulator boards, perform the reverse of the preceding steps.

A9—High-Voltage Board Removal

Removal of the High-Voltage board is accomplished by the following steps:

1. Remove the instrument Cabinet as described in that procedure.

2. Remove the Top-Cover Plate as described in that procedure.

WARNING

The crt anode lead may retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, ground the crt anode lead to the chassis after disconnecting the plug. Reconnect and disconnect the anode-lead plug several time, grounding the anode lead to chassis ground each time it is disconnected to fully dissipate the charge.

3. Unplug the CRT anode lead and discharge it to chassis ground.

4. Unplug the two leads from the ceramic termination strip to the crt. Use long-nose pliers to pull the connectors straight away from the crt neck pins. Avoid putting excessive pressure on the metal-to-glass seal. Raise the connectors high enough to allow clearance for the crt anode lead (in step 7).

5. Disconnect the single conductor connector from the ceramic termination strip.

6. Remove the screw retaining the high-voltage lead clamp.

7. Slide the high-voltage lead sideways under the termination strip.

8. Loosen the two screws on the left side of the crt socket cover and remove the one on the right side. Remove the cover.

9. Remove the five screws securing the High-Voltage board shield to remove the shield.

10. Remove the four mounting posts securing the High-Voltage board to the chassis.

11. Unplug the crt socket by gently prying evenly on both sides of the socket until the socket can be disengaged from the crt pins. Do not apply excessive side pressure on the socket.

12. Disconnect the two multipin connectors and one single-conductor connector from the front of the High-Voltage board (P902, P903, and P904). Note orientation for reinstallation.

13. Tilt the top of the board out to clear the left-side frame and pull the board up to disengage the High-Voltage board pin connectors from the Main board.

14. Lift the board from the chassis while carefully feeding the crt socket, cabling, and high-voltage lead through the chassis slot.

To reinstall the High-Voltage board, perform the reverse of the preceding instructions.

A4—Readout Board Removal

Removal of the Readout board is accomplished by the following steps:

1. Remove the instrument Cabinet as described in that procedure.

2. Remove the Top-Cover Plate as described in that procedure.

3. Place the instrument, left side down, on a flat surface.

4. Disconnect the Readout Board ribbon-cable connector from the Main board (P411).

5. With the instrument still on its side, pull the circuit board out of its plastic board mounts. Remove the board from the instrument while guiding the ribbon cable and connector through the slots in the Main board and chassis.

To reinstall the Readout board, perform the reverse of the preceding steps.

A6 and A7—Front-Panel and Variable Board Assembly Removal

Removal of the Front-Panel and Variable board assembly is accomplished by the following steps:

1. Remove the instrument Cabinet as described in that procedure.

2. Using a small-bladed screwdriver, pry the trim strip from the top edge of the front-panel trim ring. Gently pry up on the back edge to release it, then pry gently at each of the front edge retaining clips to remove the strip.

3. Remove the five screws from the top edge of the front-panel trim ring.

4. Remove the four screws and the two plastic feet from the bottom edge of the front-panel trim ring.

5. Remove the screw from either side of the front-panel trim ring (screws are recessed in the front-cover catches).

6. Using firm pressure, pull the knobs from the four controls directly below the crt (INTENSITY, FOCUS, READOUT INTENSITY, and SCALE ILLUM).

7. Slide off the front-panel trim ring and outer crt bezel.

8. Disconnect the two ribbon-cable connectors from the front edge of the Control board (P651 and P652).

9. Pull out the Front-Panel and Variable board assembly.

The following steps describe the further disassembly of the Front-Panel and Variable boards once the assembly is removed from the instrument.

ASSEMBLY SEPARATION. Separation of the Variable board from the Front-Panel board is accomplished by the following steps:

1. Using a 1/16-inch Allen wrench, loosen the set screws in the CH 1 VOLTS/DIV VAR, CH 2 VOLTS/DIV VAR, and A and B SEC/DIV VAR knobs and remove the knobs from their control shafts.

2. Disconnect the multipin connector from the Variable board (P671).

3. Remove the two screws securing the Variable board to the mounting posts.

4. Slide the Variable board and the variable-control shafts away from the Front-Panel board.

FRONT-PANEL COVER PLATE REMOVAL. Use the following procedure to remove the front-panel cover plate from the Front-Panel board.

1. Separate the Front-Panel and Variable boards as described above (if not already done).

2. Using a 1/16-inch Allen wrench, loosen the set screws in the CH 1 and CH 2 VOLTS/DIV knobs. Remove the knobs from their control shafts (if not previously removed).

3. Pull the B SEC/DIV knob to the out position to gain access to the two recessed setscrews.

4. Use a 1/16-inch Allen wrench to loosen the two setscrews and remove the B SEC/DIV knob.

5. Loosen the setscrews in the A SEC/DIV collar and remove the collar.

6. Using firm outward pressure, pull the knobs off of the Vertical and Horizontal POSITION controls, the Trigger HOLDOFF and LEVEL controls, the Delta controls, and the TRACE SEP control (ten knobs). Note the differences in the knobs for reinstallation.

7. Remove the three securing screws and two securing studs from the rear of Front-Panel board.

8. Partially separate the board from the front-panel cover plate to expose the B SEC/DIV knob microswitch and multipin connector.

9. Unplug the connector (P601) from the Front-Panel board and separate the board from the cover plate.

To reinstall the Front-Panel and Variable board assembly, perform the reverse of the preceding instructions.

A10 and A11—Channel 1 and Channel 2 Attenuator Assembly Removal

Removal of either the Channel 1 or Channel 2 Attenuator assembly is accomplished by the following steps:

1. Remove the instrument Cabinet as described in that procedure.

2. Remove the Front-Panel and Variable board assembly as described in that procedure.

3. Remove the two screws holding the small mounting bracket under the Attenuator assemblies and remove the bracket.

4. Remove the two screws that hold the Attenuator being removed to the front-panel frame.

5. Remove the two mounting screws holding the Attenuator being removed to the Main board (through access holes in the front-panel compartment).

6. Disconnect the associated multipin connector from the Main board (either P10 for Channel 1 or P11 for Channel 2).

7. Remove the two screws holding the rear attenuator shield and remove the shield.

8. Unsolder the two Attenuator output leads and the compensation capacitor lead.

9. Unplug the Attenuator by gently pulling the assembly straight up and away from the Main board.

To reinstall a removed Attenuator assembly, perform the reverse of the preceding steps.

A1—Main Board Removal

Removal of the Main board is accomplished by the following steps:

1. Remove the instrument Cabinet as described in that procedure.

2. Remove the Top-Cover Plate as described in that procedure.

3. Remove the Front-Panel and Variable board assembly as described in that procedure.

4. Disconnect the two power-supply multipin connectors from the power supply Regulator board (P121 and P122).

5. Disconnect the three ribbon-cable connections from the bottom of the Main board (P411, P511, and P512).

6. Disconnect the vertical and horizontal deflection leads from the crt neck pins. Access is via holes in the Main board. Use long-nose pliers to disconnect the pins by gently pulling straight up on the connectors. Avoid putting excessive side pressure on the metal-to-glass seal of the crt neck pins.

7. Disconnect the rear-panel BNC connector leads from the rear of the Main Board (P106, P107, and P108).

8. Disconnect the CH 2 OUT connector from near the center of the Main board (P105)

9. Disconnect the six multipin connectors for the controls beneath the crt (P111, P112, P113, P114, P115, and P116).

10. Disconnect the two-conductor connector for the Scale Illumination board from between the ASTIG and the SCALE ILLUM control connections (P181).

11. Unsnap the Power-switch rod from the switch hinge at the rear of the instrument by applying counterclockwise torque to the shaft and sliding it out of the hinge.

12. Remove the Power-switch push-button mounting screw from the front of the instrument (on the bottom of the front frame) and extract the Power-switch rod.

13. Remove the two screws holding the small bracket under the Attenuator assemblies and remove the bracket.

14. Remove the six screws holding the Attenuator assemblies and the CH 3 and CH 4 input connectors to the front frame.

15. Remove the Main board mounting screws (eleven screws total securing the Main board to the frame).

16. Raise the rear of the Main board to unplug J191 and separate the Main board from the HV board. When the plug pins are completely disengaged and the rear of the board clears the rear frame, slide the Main board rearward out of the front-panel frame.

17. Lift the Main board and Delay Line clear of the instrument while working the power supply cables through the slot in the frame.

To reinstall the Main board, perform the reverse of the preceding instructions.

A8—Scale Illumination Board Removal

Removal of the Scale-Illumination board is accomplished by the following steps:

1. Remove the instrument Cabinet as described in that procedure.

2. Remove the front-panel trim and outer crt bezel as described in the Front-Panel and Variable board assembly removal instructions.

3. Remove the eight screws holding the crt mounting bezel in place and remove the bezel and plastic gasket. Note the length difference in the screws for reinstallation.

4. Remove the plastic lens from the Scale-Illumination board.

5. Disconnect the scale-illumination multipin connector from the Main board (P181).

6. Remove the Scale-Illumination board by lifting it away from the front frame while working the wires and connector through the slot in the frame.

To reinstall the Scale-Illumination board, perform the reverse of the preceding instructions.

CRT Removal

WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses (preferably a full-face shield) should be worn. Avoid striking the crt on any object which may cause it to crack or implode. When storing a crt, place it in a protective carton or set it face down on a smooth surface in a protected location. When stored face down, it should be placed on a soft, nonabrasive surface to prevent the crt face plate from being scratched.

1. Remove the instrument Cabinet as described in that procedure.

2. Remove the Top-Cover Plate as described in that procedure.

3. Loosen the two screws on the left side of the crt socket cover and remove the one on the right side. Remove the cover.

4. Unplug the crt socket by gently prying the socket evenly on both sides until the pins can be disengaged. Do not apply excessive side pressure on the socket as it is being removed.

WARNING

The crt anode lead and the output terminal of the High-Voltage Multiplier can retain a high-voltage charge after the instrument is turned off. To avoid electrical shock, ground both the crt anode lead and the high-voltage lead to the main instrument chassis. Repeat the grounding process several times to fully dissipate the charge.

5. Disconnect the crt anode lead connector and discharge it to chassis ground.

6. Using long-nosed pliers, disconnect the horizontal and vertical deflection leads from the bottom of the crt. Pull straight out on these connectors to prevent excessive strain on the metal-to-glass seal. (Access to the connectors is through holes in the Main board).

7. Using long-nosed pliers, disconnect the vertical termination leads from the top of the crt.

8. Using long-nosed pliers, disconnect the crt shield resistor from the top of the crt.

9. Disconnect the Y-Axis Alignment coil connector from the front of the High-Voltage board (P903).

10. Remove the front-panel trim ring and outer crt bezel as described in the Front-Panel and Variable board assembly removal instructions.

11. Remove the eight retaining screws from the crt-mounting bezel at the front of the crt. Note the difference in length of the screws for reinstallation.

12. Remove the crt mounting bezel and plastic gasket from the crt.

13. Slide the crt forward slightly by gently pushing on the rear of the crt neck until the front of the crt can be grasped.

14. Slide the crt out of the instrument while feeding the anode lead and Y-Axis Alignment coil leads through their respective holes.

NOTE

Once the crt is removed, it should be stored in such a manner as to protect it from impact. If stored face down, it should be placed on a soft, nonabrasive surface to prevent the crt face plate from being scratched. To reinstall the crt, perform the reverse of the preceding instructions.

OPTIONS

INTRODUCTION

This section contains a general description of instrument options available at the time of publication of this manual. Additional information about instrument options and option availability can be obtained either by consulting the current Tektronix Product Catalog or by contacting your local Tektronix Field Office or representative.

OPTION 22

When ordered with this option, two additional probe packages identical to the standard-accessory probes are supplied with the instrument.

OPTION 1R

When the 2445 Oscilloscope is ordered with Option 1R, it is shipped in a configuration that permits easy installation into a 19-inch-wide electronic-equipment rack.

An optional rear-support kit is also available for use when rackmounting the 2445. Using this optional rear-support kit enables the rackmounted instrument to meet or exceed the requirements of MIL-T-28800C with respect to Type III, Class 5, Style C electronic equipment for vibration and shock. Other electrical and environmental specifications of the 2445 apply to both the rackmounted and the standard instrument with one exception. For the rackmounted instrument, the ambient air temperature operating limits (−15°C to +55°C) are measured at the instrument's air inlet, and its fan exhaust air temperature should not be allowed to exceed +65°C.

Connector-mounting holes are provided in the rackmount front panel. These holes enable convenient accessing of the four BNC connectors (CH 2 SIGNAL OUT, A GATE OUT, B GATE OUT, and EXT Z AXIS IN) located on the rear panel. Additional cabling and connectors required to implement any front-panel access to the rear-panel connectors are supplied by the user; however, these items can be separately ordered from Tektronix.

Complete rackmounting instructions are provided in a separate document shipped with the 2445 Option 1R. These instructions also contain appropriate procedures to convert a standard instrument into the Option 1R configuration by using the rackmounting conversion kit.

POWER CORD OPTIONS

Instruments are shipped with the detachable-power-cord configuration ordered by the customer. Descriptive information about the international power-cord options is provided in Section 2, "Operating Information." The following list identifies the Tektronix part numbers for the available power cords and associated fuses.

Option A1 (Universal Euro)

Power cord (2.5 m)	161-0104-06
Fuse (1.6 A, 250 V, 5 x 20 mm, Quick-acting)	159-0098-00
Fuse cap	200-2265-00

Option A2 (UK)

Power cord (2.5 m)	161-0104-07
Fuse (1.6 A, 250 V, 5 x 20 mm, Quick-acting)	159-0098-00
Fuse cap	200-2265-00

Option A3 (Australian)

Power cord (2.5 m)	161-0104-05
Fuse (1.6 A, 250 V, 5 x 20 mm, Quick-acting)	159-0098-00
Fuse cap	200-2265-00

Option A4 (North American)

Power cord (2.5 m)	161-0104-08
Fuse (2 A, 250 V, AGC/3AG, Fast-blow)	159-0021-00
Fuse cap	200-2264-00

Option A5 (Switzerland)

Power cord (2.5 m)	161-0167-00
Fuse (1.6 A, 250 V, 5 x 20 mm, Quick-acting)	159-0098-00
Fuse cap	200-2265-00

FUTURE OPTIONS

Technical documentation for options not available at the time of publication of this manual will be supplied in separate Operators and Service manuals for each option.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

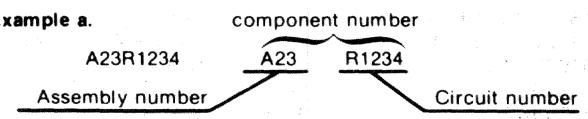
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

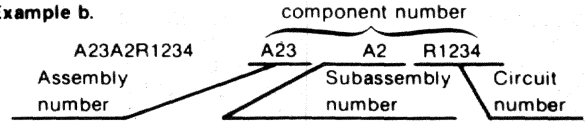
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000FG	RIFA WORLD PRODUCTS INC.	7625 BUSH LAKE RD P.O. BOX 35263	MINNEAPOLIS, MN 55435
000FJ	MARCOM SWITCHES INC.	67 ALBANY STREET	CAZENOVIA, N.Y. 13035
000HX	SAN-O INDUSTRIAL CORP.	170 WILBUR PLACE	BAHEMIA LONG ISLAND, NY 11716
000IG	FUJITSU-AMERICA INC.	1208 E. ARQUES AVE.	SUNNYVALE, CA 94086
000JF	FUJI SEMICONDUCTOR	NEW YURAKUCHO BLDG	TOKYO 100, JAPAN
00213	NYTRONICS, COMPONENTS GROUP, INC., SUBSIDIARY OF NYTRONICS, INC.	ORANGE STREET	DARLINGTON, SC 29532
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
02111	SPECTROL ELECTRONICS CORPORATION	17070 EAST GALE AVENUE	CITY OF INDUSTRY, CA 91745
02113	COILCRAFT INC.	1102 SILVER LAKE RD.	CARY, IL 60013
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
03508	GENERAL ELECTRIC COMPANY, SEMI-CONDUCTOR PRODUCTS DEPARTMENT	ELECTRONICS PARK	SYRACUSE, NY 13201
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON STREET	DOVER, NH 03820
12969	UNITRODE CORPORATION	580 PLEASANT STREET	WATERTOWN, MA 02172
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 E FAIRVIEW ST.	SANTA ANA, CA 92704
14752	ELECTRO CUBE INC.	1710 S. DEL MAR AVE.	SAN GABRIEL, CA 91776
15238	ITT SEMICONDUCTORS, A DIVISION OF INTER NATIONAL TELEPHONE AND TELEGRAPH CORP.	P.O. BOX 168, 500 BROADWAY	LAWRENCE, MA 01841
15454	RODAN INDUSTRIES, INC.	2905 BLUE STAR ST.	ANAHEIM, CA 92806
17856	SILICONIX, INC.	2201 LAURELWOOD DRIVE	SANTA CLARA, CA 95054
20932	EMCON DIV OF ILLINOIS TOOL WORKS INC.	11620 SORRENTO VALLEY RD P O BOX 81542	SAN DIEGO, CA 92121
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
22753	U. I. D. ELECTRONICS CORP.	4105 PEMBROKE RD.	HOLLYWOOD, FL 33021
24546	CORNING GLASS WORKS, ELECTRONIC COMPONENTS DIVISION	550 HIGH STREET	BRADFORD, PA 16701
25088	SIEMENS CORP.	186 WOOD AVE. S	ISELIN, NJ 08830
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
31918	IEE/SCHADOW INC.	8081 WALLACE ROAD	EDEN PRAIRIE, MN 55343
32159	WEST-CAP ARIZONA	2201 E. ELVIRA ROAD	TUCSON, AZ 85706
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL.	SUNNYVALE, CA 94086
34479	RENCO CORP	26 COROMAR DRIVE	GOLETA, CA 93117
50157	MIDWEST COMPONENTS INC.	P. O. BOX 787 1981 PORT CITY BLVD.	MUSKEGON, MI 49443
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51642	CENTRE ENGINEERING INC.	2820 E COLLEGE AVENUE	STATE COLLEGE, PA 16801
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
54937	DEYOUNG MFG., INC.	PO BOX 1806, 1517 130TH AVE.	BELLEVUE, WA 98009
55112	PLESSEY CAPACITORS, DIV. OF PLESSEY INC.	5334 STERLING CENTER DR.	WEST LAKE VILLAGE, CA 91361
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
59821	CENTRALAB INC SUB NORTH AMERICAN PHILIPS CORP	7158 MERCHANT AVE	EL PASO, TX 79915
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
74276	SIGNALITE DIV., GENERAL INSTRUMENT CORP.	1933 HECK AVE.	NEPTUNE, NJ 07753
74970	JOHNSON, E. F., CO.	299 10TH AVE. S. W.	WASECA, MN 56093
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
75915	LITTELFUSE, INC.	800 E. NORTHWEST HWY	DES PLAINES, IL 60016

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
76493	BELL INDUSTRIES, INC., MILLER, J. W., DIV.	19070 REYES AVE., P O BOX 5825	COMPTON, CA 90224
76784	OAK SWITCH SYSTEMS INC SUB OF OAK TECHNOLOGY INC	100 S MAIN ST	CRYSTAL LAKE, IL 60014
76854	OAK INDUSTRIES, INC., SWITCH DIV.	S. MAIN ST.	CRYSTAL LAKE, IL 60014
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80031	ELECTRA-MIDLAND CORP., MEPCO DIV.	22 COLUMBIA ROAD	MORRISTOWN, NJ 07960
81483	INTERNATIONAL RECTIFIER CORP.	9220 SUNSET BLVD.	LOS ANGELES, CA 90069
84411	TRW ELECTRONIC COMPONENTS, TRW CAPACITORS	112 W. FIRST ST.	OGALLALA, NE 69153
90201	MALLORY CAPACITOR CO., DIV. OF P. R. MALLORY AND CO., INC.	3029 E. WASHINGTON STREET P. O. BOX 372	INDIANAPOLIS, IN 46206
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
93410	ESSEX INTERNATIONAL, INC., CONTROLS DIV. LEXINGTON PLANT	P. O. BOX 1007	MANSFIELD, OH 44903
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341
CODE E0	1.6 NOT FOUND		
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1	670-7285-00	B010100	B011399	CKT BOARD ASSY:MAIN	80009	670-7285-00
A1	----- -----			(STANDARD ONLY)		
A1	670-7285-04	B011400	B012499	CKT BOARD ASSY:MAIN	80009	670-7285-04
A1	----- -----			(STANDARD ONLY)		
A1	670-7285-07	B012500	B019999	CKT BOARD ASSY:MAIN	80009	670-7285-07
A1	----- -----			(STANDARD ONLY)		
A1	670-7285-08	B020000		CKT BOARD ASSY:MAIN	80009	670-7285-08
A1	----- -----			(OPTION 10,ALL OTHER OPTIONS)		
A1	670-7285-06	B020000		CKT BOARD ASSY:	80009	670-7285-05
A1	----- -----			(OPTS 01,05,06,09)		
A1	672-1037-00	B010100	B020000	CKT BOARD ASSY:LOW VOLTAGE/PWR SPLY MODULE	80009	672-1037-01
A1	672-1037-02	B013199		CKT BOARD ASSY:LOW VOLTAGE/PWR SPLY MODULE	80009	672-1037-02
A2	----- -----			CKT BOARD ASSY:REGULATOR		
A2	----- -----			(AVAILABLE AT 672-1037-XX LEVEL ONLY)		
A3	----- -----			CKT BOARD ASSY:INVERTER		
A3	----- -----			(AVAILABLE AT 672-1037-XX LEVEL ONLY)		
A4	670-7278-00			CKT BOARD ASSY:READOUT	80009	670-7278-00
A5	670-7279-00	B010100	B013199	CKT BOARD ASSY:DIGITAL CONTROL	80009	670-7279-00
A5	670-7279-04	B013200		CKT BOARD ASSY:DIGITAL CONTROL	80009	670-7279-04
A6	----- -----			CKT BOARD ASSY:FRONT PANEL		
A6	----- -----			(AVAILABLE AT 672-1039-XX LEVEL ONLY)		
A7	670-7284-00			CKT BOARD ASSY:FRONT PANEL VARIABLE	80009	670-7284-00
A8	670-7280-00			CKT BOARD ASSY:SCALE ILLUMINATION	80009	670-7280-00
A9	670-7277-00	B010100	B010999	CKT BOARD ASSY:HIGH VOLTAGE	80009	670-7277-00
A9	670-7277-01	B011000	B012149	CKT BOARD ASSY:HIGH VOLTAGE	80009	670-7277-01
A9	670-7277-02	B012150	B013249	CKT BOARD ASSY:HIGH VOLTAGE	80009	670-7277-02
A9	670-7277-03	B013250		CKT BOARD ASSY:HIGH VOLTAGE	80009	670-7277-03
A10	670-7390-00			CKT BOARD ASSY:FAN MOTOR	80009	670-7390-00
A11	119-1445-01			ATTENUATOR,VAR:PROGRAMMABLE 1X-100X,CH1	80009	119-1445-01
A11	----- -----			(CHANNEL 1)		
A12	119-1445-02			ATTENUATOR,VAR:PROGRAMMABLE,1X-100X,CH2	80009	119-1445-02
A12	----- -----			(CHANNEL 2)		
A13	307-1154-00			PASSIVE NETWORK:CRT TERMINATOR,FINISHED	80009	307-1154-00
A14	670-8000-00			CKT BOARD ASSY:DYNAMIC CENTERING	80009	670-8000-00
A1	670-7285-XX			CKT BOARD ASSY:MAIN	80009	670-7285-00
A1C100	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A1C100	----- -----			(IN COMBO W/R100)		
A1C101	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A1C102	290-0963-00	B010100	B010799	CAP.,FXD,ELCTLT:220UF,+50-10%,25V	54473	ECEA1EV221S
A1C102	290-0973-00	B010800		CAP.,FXD,ELCTLT: 100UF,25%,25VDC	55680	ORD BY DESCR
A1C103	283-0492-00			CAP.,FXD,CER DI:100PF,20%	20932	501EM50DP10SM
A1C104	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A1C105	281-0064-00			CAP.,VAR,PLSTC:0.25-1.5PF,600V	74970	273-0001-101
A1C106	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A1C107	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C108	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C113	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A1C114	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C115	281-0761-00			CAP.,FXD,CER DI:27PF,5%,100V	72982	314-008S2H270J
A1C116	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C117	283-0421-00	B020000		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C118	281-0205-00			CAP.,VAR,PLSTC:5.5-65PF,100V	80031	2810C5R565QJ02F0
A1C119	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1C120	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C121	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C122	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A1C125	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C130	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A1C175	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C176	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C177	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C179	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C180	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C181	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C184	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C185	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C200	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A1C200	----- -----			(IN COMBO W/R200)		
A1C201	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A1C202	283-0492-00			CAP.,FXD,CER DI:100PF,20%	20932	501EM50DP10SM
A1C203	283-0421-00	B010100	B019999	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C203	283-0492-00	B020000		CAP.,FXD,CER DI:0.01 UF,+80-20%,50V	04222	DG015E104Z
A1C205	281-0064-00			CAP.,VAR,PLSTC:0.25-1.5PF,600V	74970	273-0001-101
A1C206	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A1C207	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C217	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C218	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C219	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A1C220	283-0024-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	72982	8121N083Z5U0104Z
A1C221	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C222	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A1C223	281-0770-00			CAP.,FXD,CER DI:0.001UF,20%,100V	04222	GC101C102M
A1C225	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C301	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C302	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C306	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C307	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C310	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C311	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C325	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C329	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A1C332	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A1C336	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C402	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	04222	GC101A270M
A1C404	281-0203-00			CAP.,VAR,PLSTC:2-10PF,100V	80031	2807C00210MJ02F0
A1C405	281-0122-00	B020000		CAP.,VAR,CER DI:2.5-9PF,100V	59660	518-000A2.5-9
A1C412	281-0762-00			CAP.,FXD,CER DI:27PF,20%,100V	04222	GC101A270M
A1C415	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C450	283-0421-00	B010100	B010999	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C454	283-0421-00	B010100	B010999	CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C458	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C460	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C464	281-0763-00			CAP.,FXD,CER DI:47PF,10%,100V	04222	GA101A470KAA
A1C478	281-0759-00			CAP.,FXD,CER DI:22PF,10%,100V	96733	R2735
A1C480	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C487	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	12969	CGB471KDN

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1C488	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C512	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A1C513	281-0775-00	B010100	B019999	CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C520	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C521	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C528	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C536	290-0246-00			CAP.,FXD,ELCTLT:3.3UF,10%,15V	56289	162D335X9015CD2
A1C537	281-0775-00	B010100	B019999	CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C537	283-0479-00	B020000		CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C544	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A1C617	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A1C625	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C645	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A1C650	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	12969	CGB471KDN
A1C653	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A1C660	281-0786-00	B010100	B019999	CAP.,FXD,CER DI:150PF,10%,100V	51642	G1710100NP0151K
A1C660	281-0851-00	B020000		CAP.,FXD,CER DI:18OPF,5%,100VDC	04222	GC10-1-A-181K
A1C669	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C675	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C707	281-0808-00			CAP.,FXD,CER DI:7PF,20%,100V	04222	GC10-1A7ROM
A1C708	285-0676-01			CAP.,FXD,PLSTC:0.1UF,3,5%,35V	80009	285-0676-01
A1C709	285-1060-00			CAP.,FXD,PLSTC:10UF,3%,25V	80009	285-1060-00
A1C710	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C712	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C722	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C723	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C731	290-0963-00	B010100	B010799	CAP.,FXD,ELCTLT:220UF,+50-10%,25V	54473	ECEA1EV221S
A1C731	290-0973-00	B010800		CAP.,FXD,ELCTLT: 100UF,25%,25VDC	55680	ORD BY DESCR
A1C733	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C735	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	12969	CGB471KDN
A1C738	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C740	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A1C742	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A1C803	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C805	281-0823-00			CAP.,FXD,CER DI:470PF,10%,50V	12969	CGB471KDN
A1C806	283-0156-00			CAP.,FXD,CER DI:1000PF,+100-0%,200V	96733	R2670
A1C808	281-0757-00	B010100	B019999	CAP.,FXD,CER DI:10PF,20%,100V	72982	8035-D-COG-100G
A1C809	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A1C810	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C811	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C817	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A1C819	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C822	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C850	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C851	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C852	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C853	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C854	283-0479-00			CAP.,FXD,CER DI:0.47UF,+80-20%,25V	20932	501ES25DP474E
A1C907	281-0808-00			CAP.,FXD,CER DI:7PF,20%,100V	04222	GC10-1A7ROM
A1C908	285-0752-03			CAP.,FXD,PLSTC:1UF,3%,50V	80009	285-0752-03
A1C912	281-0775-00	B010100	B019999	CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C912	283-0421-00	B020000		CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C933	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z

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A1C938	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C940	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C943	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C956	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A1C957	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A1C958	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C966	281-0783-00			CAP.,FXD,CER DI:0.1UF,20%,100V	96733	ADVIXE
A1C967	281-0783-00	B020000		CAP.,FXD,CER DI:0.1UF,20%,100V	96733	ADVIXE
A1C972	281-0756-00			CAP.,FXD,CER DI:2.2PF,0.5%,200V	12969	CGB2R2DFN
A1C973	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C975	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C980	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A1C988	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C990	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A1C995	281-0810-00			CAP.,FXD,CER DI:5.6PF,0.5%,100V	04222	GC10-1A5R6D
A1CR100	152-0323-00			SEMICOND DEVICE:SILICON,35V,0.1A	80009	152-0323-00
A1CR100	----- -----			(IN COMBO W/CR200)		
A1CR101	152-0322-00	B010100	B01319	SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR101	----- -----			(IN COMBO W/CR201)		
A1CR101	152-0323-01	B013200		SEMICOND DEVICE:SILICON,35V,10OMA	03508	DE101
A1CR101	----- -----			(IN COMBO W/CR201)		
A1CR107	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A1CR130	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR131	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR140	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR141	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR142	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR143	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR144	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR145	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR146	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR147	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR148	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR149	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR150	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR151	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR152	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR153	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR154	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR155	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR160	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR161	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR162	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR163	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR200	152-0323-01			SEMICOND DEVICE:SILICON,35V,10OMA	03508	DE101
A1CR200	----- -----			(IN COMBO W/CR100)		
A1CR201	152-0322-00	B010100	B013199	SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A1CR201	----- -----			(IN COMBO W/CR101)		
A1CR201	152-0323-01	B013200		SEMICOND DEVICE:SILICON,35V,10OMA	03508	DE101
A1CR201	----- -----			(IN COMBO W/CR101)		
A1CR355	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR356	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR358	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR359	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R

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A1CR460	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR461	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR476	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR484	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR485	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR495	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR503	152-0141-02	B020000		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR600	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR601	152-0141-02	B011400		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR616	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR619	152-0141-02	B011400		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR620	152-0141-02	B011400		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR621	152-0141-02	B011400		SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR652	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR653	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR707	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR741	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR746	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR747	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR807	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	14433	WG1308
A1CR811	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR871	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR950	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR951	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR956	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A1CR966	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	14433	WG1308
A1CR972	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	14433	WG1308
A1CR987	152-0574-00			SEMICOND DEVICE:SILICON,120V,0.15A	14433	WG1308
A1DL100	119-1490-00			DELAY LINE,ELEC:73NS, 150 OHM	80009	119-1490-00
A1J100	131-0608-00	B010100	B019999	TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A1J110	136-0727-00			SKT,PL-IN ELEK:MICROCKT,8 CONTACT	09922	DILB8P-108
A1J118	136-0727-00			SKT,PL-IN ELEK:MICROCKT,8 CONTACT	09922	DILB8P-108
A1J119	136-0728-00			SKT,PL-IN ELEK:MICROCKT,14 CONTACT	09922	DILB14P-108
A1L101	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L107	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L113	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L115	108-0317-00			COIL,RF:FIXED,15UH	32159	71501M
A1L219	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L307	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L325	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L336	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L521	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L605	108-0735-00			COIL,RF:FIXED,560NH	80009	108-0735-00
A1L606	108-0683-00			COIL,RF:FIXED,900NH	80009	108-0683-00
A1L607	108-0683-00			COIL,RF:FIXED,900NH	80009	108-0683-00
A1L608	108-0735-00			COIL,RF:FIXED,560NH	80009	108-0735-00
A1L609	108-0509-00			COIL,RF:2.45UH	80009	108-0509-00
A1L610	108-0509-00			COIL,RF:2.45UH	80009	108-0509-00
A1L611	108-0317-00			COIL,RF:FIXED,15UH	32159	71501M
A1L612	108-0317-00			COIL,RF:FIXED,15UH	32159	71501M
A1L619	108-0735-00	B010100	B019999	COIL,RF:FIXED,560NH	80009	108-0735-00
A1L619	114-0353-00	B020000		COIL,RF:VARIABLE,0.6 TO 1.0UH	80009	114-0353-00
A1L628	108-0327-00	B020000		COIL,RF:48NH	80009	108-0327-00

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A1L633	108-0327-00	B020000		COIL,RF:48NH	80009	108-0327-00
A1L644	108-0736-00	B010100	B019999	COIL,RF:810NH	80009	108-0736-00
A1L644	114-0353-00	B020000		COIL,RF:VARIABLE,0.6 TO 1.0UH	80009	114-0353-00
A1L733	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L738	108-0317-00			COIL,RF:FIXED,15UH	32159	71501M
A1L740	108-0317-00			COIL,RF:FIXED,15UH	32159	71501M
A1L743	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L938	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1L973	108-0538-00			COIL,RF:2.7UH	76493	JWM#B7059
A1LR101	108-0325-00			COIL,RF:0.5UH	80009	108-0325-00
A1LR107	108-0325-00			COIL,RF:0.5UH	80009	108-0325-00
A1LR180	108-0999-00			COIL,RF:FIXED,105NH ON FORM		
A1LR201	108-0325-00			COIL,RF:0.5UH	80009	108-0325-00
A1LR218	108-0330-00			COIL,RF:0.4UH	80009	108-0330-00
A1LR280	108-0999-00			COIL,RF:FIXED,105NH ON FORM		
A1Q130	151-0622-00			TRANSISTOR:SILICON,PNP	27014	92PU51A
A1Q131	151-0622-00			TRANSISTOR:SILICON,PNP	27014	92PU51A
A1Q154	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A1Q155	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A1Q190	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A1Q460A,B	153-0547-00			SEMICOND DVC SE:SILICON,NPN,MATCHED	80009	153-0547-00
A1Q550	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A1Q600	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A1Q623	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A1Q624	151-1042-01	B010100	B019999	SEMICOND DVC SE:FET,SI,TO-92	17856	J2595
A1Q624	151-1025-00	B020000		TRANSISTOR:SILICON,JFE,N-CHANNEL	01295	SFB8129
A1Q645	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A1Q700	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A1Q709	151-0736-00			TRANSISTOR:SILICON,NPN	04713	SPS8317
A1Q741	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A1R100	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A1R100	----- -----			(IN COMBO W/C100)		
A1R101	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A1R102	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A1R114	321-0130-00			RES.,FXD,FILM:221 OHM,1%,0.125W	91637	MFF1816G221R0F
A1R115	321-0146-00			RES.,FXD,FILM:324 OHM,1%,0.125W	91637	MFF1816G324R0F
A1R117	321-0285-00			RES.,FXD,FILM:9.09K OHM,1%,0.125W	91637	MFF1816G90900F
A1R118	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A1R119	321-0354-00			RES.,FXD,FILM:47.5K OHM,1%,0.125W	91637	MFF1816G47501F
A1R120	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R121	315-0121-00	B010100	B019999	RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A1R123	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A1R125	301-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.50W	01121	EB3615
A1R129	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R130	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A1R131	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A1R133	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A1R135	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R136	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A1R140	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A1R141	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A1R142	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A1R143	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R144	307-0108-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.25W	01121	CB68G5
A1R149	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R152	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
A1R153	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A1R154	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A1R155	321-0210-00	B010100	B019999	RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A1R155	321-0206-00	B020000		RES.,FXD,FILM:1.37K OHM,1%,0.125W	91637	MFF1816G13700F
A1R156	321-0255-00			RES.,FXD,FILM:4.42K OHM,1%,0.125W	91637	MFF1816G44200F
A1R159	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A1R161	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A1R162	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A1R163	321-0242-00			RES.,FXD,FILM:3.24K OHM,1%,0.125W	91637	MFF1816G32400F
A1R165	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R190	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R191	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R192	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R193	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R194	317-0105-00	B010100	B019999	RES.,FXD,CMPSN:1M OHM,5%,0.125W	01121	BB1055
A1R194	315-0103-00	B020000		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R195	315-0301-00			RES.,FXD,CMPSN:300 OHM,5%,0.25W	01121	CB3015
A1R196	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A1R197	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625
A1R198	321-1700-04			RES.,FXD,FILM:10.44K OHM,0.1%,0.125W	91637	MFF1816D10441B
A1R199	321-1700-04			RES.,FXD,FILM:10.44K OHM,0.1%,0.125W	91637	MFF1816D10441B
A1R200	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A1R200	----- -----			(IN COMBO W/C200)		
A1R201	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A1R202	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A1R216	315-0121-00	B010100	B019999	RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A1R217	321-0268-00			RES.,FXD,FILM:6.04K OHM,1%,0.125W	91637	MFF1816G60400F
A1R218	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A1R219	321-0354-00			RES.,FXD,FILM:47.5K OHM,1%,0.125W	91637	MFF1816G47501F
A1R220	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R223	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A1R225	301-0361-00			RES.,FXD,CMPSN:360 OHM,5%,0.50W	01121	EB3615
A1R230	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A1R231	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A1R232	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A1R301	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A1R302	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A1R304	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R311	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R329	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R332	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R334	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A1R353	321-0265-00			RES.,FXD,FILM:5.62K OHM,1%,0.125W	91637	MFF1816G56200F
A1R355	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R357	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A1R358	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A1R359	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A1R360	321-0293-00			RES.,FXD,FILM:11K OHM,1%,0.125W	91637	MFF1816G11001F
A1R361	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A1R362	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R363	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A1R401	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	MFF1816G12400F
A1R402	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R403	311-1137-00	B010100	B019999	RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A1R403	311-2099-00	B020000		RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	73138	72-266-0
A1R405	315-0470-00	B020000		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A1R412	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R416	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A1R430	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A1R431	315-0470-00	B020000		RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A1R440	321-0666-00			RES.,FXD,FILM:3.04K OHM,0.5%,0.125W	91637	MFF1816D30400D
A1R450	321-0310-00			RES.,FXD,FILM:16.5K OHM,1%,0.125W	91637	MFF1816G16501F
A1R451	321-0275-00			RES.,FXD,FILM:7.15K OHM,1%,0.125W	91637	MFF1816G71500F
A1R452	321-0310-00			RES.,FXD,FILM:16.5K OHM,1%,0.125W	91637	MFF1816G16501F
A1R453	321-0275-00			RES.,FXD,FILM:7.15K OHM,1%,0.125W	91637	MFF1816G71500F
A1R454	321-0310-00			RES.,FXD,FILM:16.5K OHM,1%,0.125W	91637	MFF1816G16501F
A1R455	321-0309-00			RES.,FXD,FILM:16.2K OHM,1%,0.125W,TC=TO	01121	ORD BY DESCR
A1R456	321-0303-00	B010100	B019999	RES.,FXD,FILM:14K OHM,1%,0.125W	91637	MFF1816G14001F
A1R456	321-0329-00	B020000		RES.,FXD,FILM:26.1K OHM,1%,0.125W	91637	MFF1816G26101F
A1R457	321-0275-00			RES.,FXD,FILM:7.15K OHM,1%,0.125W	91637	MFF1816G71500F
A1R458	321-0085-00			RES.,FXD,FILM:75 OHM,1%,0.125W	91637	MFF1816G75R00F
A1R459	321-0085-00			RES.,FXD,FILM:75 OHM,1%,0.125W	91637	MFF1816G75R00F
A1R459	----- -----			(COMBO W/C459)		
A1R460	321-0062-00			RES.,FXD,FILM:43.2 OHM,1%,0.125W	91637	CMF55-116G43R20F
A1R461	321-0136-00	B010100	B019999	RES.,FXD,FILM:255 OHM,1%,0.125W	91637	MFF1816G255R0F
A1R461	321-0139-00	B020000		RES.,FXD,FILM:274 OHM,1%,0.125W	91637	MFF1816G274R0F
A1R462	321-0208-00	B010100	B019999	RES.,FXD,FILM:1.43K OHM,1%,0.125W	91637	MFF1816G14300F
A1R462	321-0201-00	B02000		RES.,FXD,FILM:1.21K OHM,1%,0.125W	91637	MFF1816G12100F
A1R463	321-0201-00	B010100	B019999	RES.,FXD,FILM:1.21K OHM,1%,0.125W	91637	MFF1816G12100F
A1R463	321-0193-00	B020000		RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A1R464	321-0063-00			RES.,FXD,FILM:44.2 OHM,1%,0.125W	91637	MFF1816G44R20F
A1R465	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A1R466	321-0275-00	B020000		RES.,FXD,FILM:7.15K OHM,1%,0.125W	91637	MFF1816G71500F
A1R470	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A1R471	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A1R476	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R477	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R478	321-0193-03			RES.,FXD,FILM:1K OHM,0.25%,0.125W	91637	MFF1816D10000C
A1R479	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R480	321-0378-00			RES.,FXD,FILM:84.5K OHM,1%,0.125W	91637	MFF1816G84501F
A1R481	321-0347-00			RES.,FXD,FILM:40.2K OHM,1%,0.125W	91637	MFF1816G40201F
A1R482	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A1R483	321-0347-00			RES.,FXD,FILM:40.2K OHM,1%,0.125W	91637	MFF1816G40201F
A1R484	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R485	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A1R486	321-0347-00			RES.,FXD,FILM:40.2K OHM,1%,0.125W	91637	MFF1816G40201F
A1R487	321-0130-03			RES.,FXD,FILM:221 OHM,0.25%,0.125W	91637	MFF1816D221R0C
A1R488	321-1216-03			RES.,FXD,FILM:1.76K OHM,0.25%,0.125W	91637	MFF1816D17600C
A1R489	321-1216-03			RES.,FXD,FILM:1.76K OHM,0.25%,0.125W	91637	MFF1816D17600C
A1R490	321-0378-00			RES.,FXD,FILM:84.5K OHM,1%,0.125W	91637	MFF1816G84501F
A1R491	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R492	321-0193-03			RES.,FXD,FILM:1K OHM,0.25%,0.125W	91637	MFF1816D10000C
A1R493	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R494	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A1R495	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R497	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R498	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R500	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A1R501	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R502	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A1R503	315-0103-00	B020000		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R504	315-0103-00	B020000		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R511	321-0320-00	B010100	B019999	RES.,FXD,FILM:21K OHM,1%,0.125W	91637	MFF1816G21001F
A1R512	321-0293-00	B010100	B019999	RES.,FXD,FILM:11K OHM,1%,0.125W	91637	MFF1816G11001F
A1R513	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A1R518	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A1R519	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A1R520	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A1R521	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R527	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R529	315-0561-00			RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A1R537	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A1R542	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A1R543	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A1R544	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A1R545	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R550	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A1R551	321-1682-07			RES.,FXD,FILM:5.7K OHM,0.1%,0.125W	91637	MFF1816C57000B
A1R552	321-0641-07			RES.,FXD,FILM:1.8K OHM,0.1%,0.125W	91637	MFF1816C18000B
A1R553	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A1R554	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A1R555	321-0294-00			RES.,FXD,FILM:11.3K OHM,1%,0.125W	91637	MFF1816G11301F
A1R556	321-0282-00			RES.,FXD,FILM:8.45K OHM,1%,0.125W	91637	MFF1816G84500F
A1R557	321-0808-07			RES.,FXD,FILM:300 OHM,0.1%,0.125W	24546	NE55E3000B
A1R558	321-0657-07			RES.,FXD,FILM:60 OHM,0.1%,0.125W	91637	CMF55-116C60R00B
A1R560	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A1R600	315-0270-00			RES.,FXD,CMPSN:27 OHM,5%,0.25W	01121	CB2705
A1R601	307-0108-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.25W	01121	CB68G5
A1R602	307-0108-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.25W	01121	CB68G5
A1R605	321-0112-00			RES.,FXD,FILM:143 OHM,1%,0.125W	91637	MFF1816G143R0F
A1R606	321-0002-00			RES.,FXD,FILM:10.2 OHM,1%,0.125W	91637	MFF1816G10R20F
A1R607	321-0002-00			RES.,FXD,FILM:10.2 OHM,1%,0.125W	91637	MFF1816G10R20F
A1R608	307-0108-00			RES.,FXD,CMPSN:6.8 OHM,5%,0.25W	01121	CB68G5
A1R614	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R615	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R617	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R618	311-1137-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A1R619	315-0270-00			RES.,FXD,CMPSN:27 OHM,5%,0.25W	01121	CB2705
A1R620	315-0472-00	B011400		RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R622	321-0226-00	B010100	B019999	RES.,FXD,FILM:2.21K OHM,1%,0.125W	91637	MFF1816G22100F
A1R622	321-0255-00	B020000		RES.,FXD,FILM:4.42K OHM,1%,0.125W	91637	MFF1816G44200F
A1R624	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A1R638	311-1137-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A1R639	311-2099-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	73138	72-266-0
A1R639	----- -----			(IN SERIES W/W639)		
A1R642	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325

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A1R643	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R644	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R645	321-0625-00			RES.,FXD,FILM:5.88K OHM,1%,0.125W	91637	MFF1816G58800F
A1R646	321-0252-00			RES.,FXD,FILM:4.12K OHM,1%,0.125W	91637	MFF1816G41200F
A1R650	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A1R651	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A1R652	315-0274-00			RES.,FXD,CMPSN:270K OHM,5%,0.25W	01121	CB2745
A1R653	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R654	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A1R655	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R669	321-0406-00			RES.,FXD,FILM:165K OHM,1%,0.125W	91637	MFF1816G16502F
A1R670	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R671	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R672	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R678	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R700	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A1R701	321-0223-00			RES.,FXD,FILM:2.05K OHM,1%,0.125W	91637	MFF1816G20500F
A1R702	321-0252-00			RES.,FXD,FILM:4.12K OHM,1%,0.125W	91637	MFF1816G41200F
A1R707	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A1R708	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A1R709	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A1R710	315-0396-00			RES.,FXD,CMPSN:39M OHM,5%,0.25W	01121	CB3965
A1R713	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R723	321-0245-00			RES.,FXD,FILM:3.48K OHM,1%,0.125W	91637	MFF1816G34800F
A1R724	321-0680-00			RES.,FXD,FILM:35.3K OHM,0.5%,0.125W	91637	MFF1816D35301D
A1R731	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A1R732	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A1R733	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A1R734	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A1R735	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A1R736	321-0209-00	B010100	B019999	RES.,FXD,FILM:1.47K OHM,1%,0.125W	91637	MFF1816G14700F
A1R736	321-0197-00	B020000		RES.,FXD,FILM:1.1K OHM,1%,0.125W	91637	MFF1816G11000F
A1R737	321-0255-00	B010100	B019999	RES.,FXD,FILM:4.42K OHM,1%,0.125W	91637	MFF1816G44200F
A1R738	321-0273-00			RES.,FXD,FILM:6.81K OHM,1%,0.125W	91637	MFF1816G68100F
A1R741	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A1R742	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A1R743	315-0750-00	B010100	B019999	RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R743	315-0102-00	B020000		RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R744	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R745	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A1R746	301-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.50W	01121	EB4705
A1R750	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A1R800	321-0147-00			RES.,FXD,FILM:332 OHM,1%,0.125W	91637	MFF1816G332R0F
A1R801	311-2099-00			RES.,VAR,NONWIR:TRMR,500 OHM,10%,0.5W	73138	72-266-0
A1R801	----- -----			(IN SERIES W/W800)		
A1R802	315-0222-00	B010100	B019999	RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A1R802	315-0821-00	B020000		RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R803	315-0821-00	B010100	B019999	RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A1R803	315-0222-00	B020000		RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A1R804	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A1R805	311-2155-00	B010100	B019999	E:		
A1R805	311-1242-00	B02000		RES.,VAR,NONWIR:200K OHM,10%,0.50W	02111	63X-204-T602
A1R806	315-0204-00			RES.,FXD,CMPSN:200K OHM,5%,0.25W	01121	CB2045

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1R809	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A1R811	301-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.50W	01121	EB3315
A1R817	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A1R820	321-0327-00			RES.,FXD,FILM:24.9K OHM,1%,0.125W	91637	MFF1816G24901F
A1R821	321-0298-00			RES.,FXD,FILM:12.4K OHM,1%,0.125W	91637	MFF1816G12401F
A1R822	315-0271-00			RES.,FXD,CMPSN:270 OHM,5%,0.25W	01121	CB2715
A1R823	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	91637	MFF1816G10000F
A1R839	321-0147-00			RES.,FXD,FILM:332 OHM,1%,0.125W	91637	MFF1816G332R0F
A1R850	311-1137-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A1R852	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A1R853	315-0240-00			RES.,FXD,CMPSN:24 OHM,5%,0.25W	01121	CB2405
A1R855	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A1R856	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A1R858	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A1R860	311-1137-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A1R901	315-0112-00	B020000		RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A1R902	315-0112-00	B020000		RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A1R903	315-0112-00	B020000		RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A1R904	315-0124-00			RES.,FXD,CMPSN:120K OHM,5%,0.25W	01121	CB1245
A1R907	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A1R910	315-0396-00			RES.,FXD,CMPSN:39M OHM,5%,0.25W	01121	CB3965
A1R912	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A1R924	321-0325-00			RES.,FXD,FILM:23.7K OHM,1%,0.125W	91637	MFF1816G23701F
A1R936	321-0217-00			RES.,FXD,FILM:1.78K OHM,1%,0.125W	91637	MFF1816G17800F
A1R937	321-0268-00			RES.,FXD,FILM:6.04K OHM,1%,0.125W	91637	MFF1816G60400F
A1R939	315-0332-00	B020000		RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A1R940	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R941	315-0102-00	B010100	B019999	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A1R941	315-0561-00	B020000		RES.,FXD,CMPSN:560 OHM,5%,0.25W	01121	CB5615
A1R942	321-0256-00	B020000		RES.,FXD,FILM:4.53K OHM,1%,0.125W	91637	MFF1816G45300F
A1R943	315-0121-00			RES.,FXD,CMPSN:120 OHM,5%,0.25W	01121	CB1215
A1R944	317-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.125W	01121	BB3025
A1R945	315-0621-00			RES.,FXD,CMPSN:620 OHM,5%,0.25W	01121	CB6215
A1R950	301-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.50W	01121	EB4705
A1R951	308-0555-00			RES.,FXD,WW:5 OHM,5%,3W	00213	1200S-5R000J
A1R952	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A1R956	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A1R957	321-0291-00			RES.,FXD,FILM:10.5K OHM,1%,0.125W	91637	MFF1816G10501F
A1R972	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A1R973	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A1R981	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A1R995	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A1S615	260-1421-00			SWITCH,PUSH:1 STA,MOMENTARY,NON-SHORT	59821	OBD
A1U100	155-0235-00	B010100	B013249	MICROCIRCUIT,LI:VERTICAL PREAMP,TESTED	80009	155-0235-00
A1U100	153-0235-00	B013250		MICROCIRCUIT,LI:VERTICAL PREAMPS	80009	153-0235-00
A1U100	----- -----			(PART OF A1U200)		
A1U110	156-1245-00			MICROCIRCUIT,LI:7 XSTR,HV/HIGH CUR	04713	MC1413PDS
A1U120	156-1245-00			MICROCIRCUIT,LI:7 XSTR,HV/HIGH CUR	04713	MC1413PDS
A1U130	156-1245-00			MICROCIRCUIT,LI:7 XSTR,HV/HIGH CUR	04713	MC1413PDS
A1U140	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A1U150	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A1U160	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A1U165	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A1U170	156-0513-03			MICROCIRCUIT,LI:CMOS,8 CHAN ANALOG MU	80009	156-0513-03
A1U200	155-0235-00	B010100	B013249	MICROCIRCUIT,LI:VERTICAL PREAMP,TESTED	80009	155-0235-00
A1U200	153-0235-00	B013250		MICROCIRCUIT,LI:VERTICAL PREAMPS	80009	153-0235-00
A1U200	----- -----			(PART OF A1U100)		
A1U300	155-0238-00			MICROCIRCUIT,LI:TRIGGER PREAMP	80009	155-0238-00
A1U350	156-0853-02			MICROCIRCUIT,LI:DUAL OPNL AMPL,CHK	04713	LM358J
A1U400	155-0236-00			MICROCIRCUIT,LI:VERTICAL CHANNEL SWITCH	80009	155-0236-00
A1U450	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A1U475	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U485	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U500	155-0239-00	B010100	B01999	MICROCIRCUIT,LI:TRIGGER TESTED	80009	155-0239-00
A1U500	155-0239-01	B020000		(OPTIONS ONLY)		
A1U550	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U600	155-0237-00			MICROCIRCUIT,LI:VERTICAL OUTPUT,TESTED	80009	155-0237-00
A1U650	155-0244-00			MICROCIRCUIT,DI:SYSTEM LOGIC INTERFACE		
A1U700	155-0240-00			MICROCIRCUIT,LI:VERTICAL OUTPUT,TESTED	80009	155-0240-00
A1U735	156-0048-00			MICROCIRCUIT,LI:FIVE NPN TRANSISTOR ARRAY	02735	CA3046
A1U800	155-0241-01			MICROCIRCUIT,LI:HORIZONTAL AMPLIFIER	80009	155-0241-01
A1U850	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A1U860	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A1U900	155-0240-00			MICROCIRCUIT,LI:VERTICAL OUTPUT,TESTED	80009	155-0240-00
A1U910	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A1U950	155-0242-00	B010100	B011099	MICROCIRCUIT,LI:Z AXIS AUTOFOCUS,TESTED	80009	155-0242-00
A1U950	155-0242-01	B011100		MICROCIRCUIT,LI:Z AXIS AUTOFOCUS,TESTED	80009	155-0242-01
A1U975	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A1U980	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A1VR125	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738RL
A1VR225	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738RL
A1VR550	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A1W101	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W103	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W104	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W105	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W106	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W107	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W121	175-4594-00			CA ASSY,SP,ELEC:7,22 AWG,7.0 L,RIBBON	80009	175-4594-00
A1W122	175-4598-00			CA ASSY,SP,ELEC:8,26 AWG,7.0 L,RIBBON	80009	175-4598-00
A1W171	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W172	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W194	131-0566-00	B010100	B019999	BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W666	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A1W677	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2	----- -----			CKT BOARD ASSY:REGULATOR		
A2	----- -----			(AVAILABLE AT 672-1037-XX LEVEL ONLY)		
A2C1016	285-1222-00			CAP.,FXD,PLSTC:0.068UF,20%,250V	55112	158/.068/M/250/H
A2C1018	285-1222-00			CAP.,FXD,PLSTC:0.068UF,20%,250V	55112	158/.068/M/250/H
A2C1208	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C1220	290-0939-00			CAP.,FXD,ELCTLT:10UF,+100-10%,100V	56289	672D106H100CG2C
A2C1226	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	GC101C271K
A2C1240	290-0939-00			CAP.,FXD,ELCTLT:10UF,+100-10%,100V	56289	672D106H100CG2C
A2C1245	281-0783-00			CAP.,FXD,CER DI:0.1UF,20%,100V	96733	ADVIXE
A2C1246	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	GC101C271K
A2C1260	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A2C1261	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A2C1270	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	GC101C271K
A2C1272	281-0774-00			CAP.,FXD,CER DI:0.022UF,20%,100V	12969	CGE223MEZ
A2C1274	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A2C1280	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A2C1290	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C1291	290-0778-00			CAP.,FXD,ELCTLT:1UF,+50-10%,50V	54473	ECE-A50N1
A2C1300	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A2C1330	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A2C1331	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A2C1350	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A2C1357	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A2C1374	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	GC101C271K
A2C1400	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A2C1402	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A2CR1011	152-0750-00			SEMICOND DEVICE:RECT BRIDGE,600V,3A	80009	152-0750-00
A2CR1220	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1221	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1241	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1242	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1243	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1244	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1260	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1261	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1262	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1263	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1264	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1281	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1282	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1283	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1300	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1301	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1302	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2CR1303	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1330	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1331	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1332	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1334	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1351	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A2CR1376	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A2E1001	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	74276	CG230L
A2E1002	119-0181-00			ARSR,ELEC SURGE:230V,GAS FILLED	74276	CG230L

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2F1330	159-0185-00			FUSE,CARTRIDGE:5.2 X 20MM,0.75A,125V	000HX	TSC.75
A2L1011	108-0473-00			COIL,RF:150UH	80009	108-0473-00
A2L1012	108-0473-00			COIL,RF:150UH	80009	108-0473-00
A2L1402	108-0443-00			COIL,RF:25UH	80009	108-0443-00
A2P204	131-1048-00			TERM.QIK DISC:CKT BD MT,0.11 X 0.02	00779	61134-1
A2P205	131-1048-00			TERM.QIK DISC:CKT BD MT,0.11 X 0.02	00779	61134-1
A2P206	131-1048-00			TERM.QIK DISC:CKT BD MT,0.11 X 0.02	00779	61134-1
A2P207	131-1048-00			TERM.QIK DISC:CKT BD MT,0.11 X 0.02	00779	61134-1
A2Q1220	151-0497-00			TRANSISTOR:SILICON,NPN	04713	SJE1985
A2Q1221	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A2Q1222	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A2Q1223	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A2Q1240	151-0464-00			TRANSISTOR:SILICON,NPN	04713	SJE412
A2Q1241	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A2Q1243	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A2Q1245	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A2Q1280	151-0476-00			TRANSISTOR:SILICON,NPN	02735	68430
A2Q1281	151-0347-00			TRANSISTOR:SILICON,NPN	56289	2N5551
A2Q1300	151-0482-00			TRANSISTOR:SILICON,PNP	80009	151-0482-00
A2Q1301	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A2Q1351	151-0429-00			TRANSISTOR:SILICON,PNP	04713	SJE957
A2Q1354	151-0342-00			TRANSISTOR:SILICON,PNP	07263	S035928
A2Q1370	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A2Q1376	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065
A2R1011	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	01121	CB5605
A2R1012	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	01121	CB5605
A2R1013	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A2R1014	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A2R1015	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A2R1016	301-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.50W	01121	EB6805
A2R1017	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A2R1018	301-0300-00			RES.,FXD,CMPSN:30 OHM,5%,0.50W	01121	EB3005
A2R1204	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R1208	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A2R1212	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A2R1220	304-0822-00			RES.,FXD,CMPSN:8.2K OHM,10%,1W	01121	GB8221
A2R1221	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A2R1222	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R1223	315-0823-00			RES.,FXD,CMPSN:82K OHM,5%,0.25W	01121	CB8235
A2R1226	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R1227	321-0634-00			RES.,FXD,FILM:84.65K OHM,0.25%,0.125W	91637	CMF55-116D84651C
A2R1228	321-0293-03			RES.,FXD,FILM:11K OHM,0.25%,0.125W	24546	NC55C1102C
A2R1229	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A2R1240	303-0202-00			RES.,FXD,CMPSN:2K OHM,5%,1W	01121	GB2025
A2R1241	307-0105-00			RES.,FXD,CMPSN:3.9 OHM,5%,0.25W	01121	CB39G5
A2R1242	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A2R1243	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A2R1244	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A2R1246	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R1247	321-0368-00			RES.,FXD,FILM:66.5K OHM,1%,0.125W	91637	MFF1816G66501F
A2R1248	321-0319-00			RES.,FXD,FILM:20.5K OHM,1%,0.125W	91637	MFF1816G20501F
A2R1249	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A2R1261	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A2R1262	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A2R1264	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A2R1270	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A2R1273	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A2R1274	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A2R1280	303-0470-00			RES.,FXD,CMPSN:47 OHM,5%,1W	01121	GB4705
A2R1281	308-0839-00			RES.,FXD,WW:0.1 OHM,5%,1.0W	75042	BW-20-R/1000J
A2R1282	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R1283	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R1284	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A2R1285	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A2R1286	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A2R1291	321-0334-00			RES.,FXD,FILM:29.4K OHM,1%,0.125W	91637	MFF1816G29401F
A2R1292	311-1138-00			RES.,VAR,NONWIR:1K OHM,20%,0.50W	73138	72XW-44-0-102M
A2R1293	321-0639-00			RES.,FXD,FILM:9.6K OHM,1%,0.125W	91637	MFF1816G96000F
A2R1300	303-0470-00			RES.,FXD,CMPSN:47 OHM,5%,1W	01121	GB4705
A2R1301	308-0839-00			RES.,FXD,WW:0.1 OHM,5%,1.0W	75042	BW-20-R/1000J
A2R1302	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A2R1304	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A2R1305	321-0289-06			RES.,FXD,FILM:10K OHM,0.25%,0.125W	91637	MFF1816C10001C
A2R1306	321-0318-03			RES.,FXD,FILM:20K OHM,0.25%,0.125W	24546	NC55C2002C
A2R1307	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A2R1309	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A2R1331	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	CMF55116G30101F
A2R1332	321-0318-00			RES.,FXD,FILM:20K OHM,1%,0.125W	91637	MFF1816G20001F
A2R1333	315-0751-00			RES.,FXD,CMPSN:750 OHM,5%,0.25W	01121	CB7515
A2R1334	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R1351	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A2R1352	301-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.50W	01121	EB1505
A2R1353	301-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.50W	01121	EB1505
A2R1354	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A2R1355	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A2R1356	315-0512-00	B010185		RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A2R1357	321-0310-00			RES.,FXD,FILM:16.5K OHM,1%,0.125W	91637	MFF1816G16501F
A2R1358	321-0319-00			RES.,FXD,FILM:20.5K OHM,1%,0.125W	91637	MFF1816G20501F
A2R1359	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A2R1370	321-0363-00			RES.,FXD,FILM:59K OHM,1%,0.125W	91637	MFF1816G59001F
A2R1372	321-0299-00			RES.,FXD,FILM:12.7K OHM,1%,0.125W	91637	MFF1816G12701F
A2R1374	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A2R1376	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A2R1378	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A2R1400	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A2R1402	315-0111-00			RES.,FXD,CMPSN:110 OHM,5%,0.25W	01121	CB1115
A2RT1010	307-0350-00			RES.,THERMAL:7.5 OHM,10%,3.9%/DEG C	15454	75DJ7R5R0220SS
A2RT1016	307-0746-00			RES.,THERMAL:5 OHM,10%,7A/DEG C	15454	SG-6
A2S350	260-1849-00			SWITCH,PUSH:DPDT,4A,250VAC,W/BRKT	31918	NE15/F2U103EE
A2T1229	120-1401-00			XFMR,TRIG:	54937	ORD BY DESCR
A2TP201	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A2U1260	156-1161-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	27014	LM317T
A2U1270	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A2U1281	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A2U1290	156-1173-00			MICROCIRCUIT,LI:VOLTAGE REFERENCE	04713	MC1403UDS
A2U1300	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4

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A2U1330	156-0872-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC7912C
A2U1371	156-0495-02			MICROCIRCUIT,LI:QUAD OPNL AMPL,SELECTED	01295	LM324J4
A2VR1293	152-0055-00			SEMICOND DEVICE:ZENER,0.4W,11V,5%	04713	SZG35009K1
A2W1226	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A2W1287	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A3	----- -----			CKT BOARD ASSY:INVERTER		
A3	----- -----			(AVAILABLE AT 672-1037-01 LEVEL ONLY)		
A3C1020	285-1192-00			CAP.,FXD,PPR DI:0.0022UF,20%,250VAC	000FG	PME271Y422
A3C1021	290-0971-00			CAP.,FXD,ELCTLT:290UF,+50-10%,200V	90201	TCG291T200N
A3C1022	290-0971-00			CAP.,FXD,ELCTLT:290UF,+50-10%,200V	90201	TCG291T200N
A3C1023	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A3C1025	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A3C1032	281-0812-00			CAP.,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A3C1033	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A3C1034	290-0524-00	B010100	B013199	CAP.,FXD,ELCTLT:4.7UF,20%,10V	90201	TDC475M010EL
A3C1034	290-0524-01	B013200		CAP.,FXD,ELCTLT:4.7UF,20%,10V		
A3C1035	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A3C1040	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A3C1048	281-0826-00			CAP.,FXD,CER DI:2200PF,5%,100V	12969	CGB222KEX
A3C1050	285-1254-00			CAP.,FXD,PLSTC:0.22UF,10%,400WVDC	84411	X363UW-224104
A3C1051	285-1192-00			CAP.,FXD,PPR DI:0.0022UF,20%,250VAC	000FG	PME271Y422
A3C1052	285-1196-00			CAP.,FXD,PAPER:0.01UF,20%,250V	80009	285-1196-00
A3C1062	281-0850-00			CAP.,FXD,CER DI:820PF,5%,50VDC	96733	R3149
A3C1065	285-1190-00			CAP.,FXD,MTLZD:0.056UF,5%,250V	55112	160.056 J 250C
A3C1066	290-0782-00	B010100	B013199	CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A3C1066	290-0782-01	B013200		CAP.,FXD,ELCTLT:4.7UF,20%,35VDC		
A3C1067	281-0850-00			CAP.,FXD,CER DI:820PF,5%,50VDC	96733	R3149
A3C1071	281-0772-00			CAP.,FXD,CER DI:0.0047UF,10%,100V	04222	GC701C472K
A3C1072	290-0806-00			CAP.,FXD,ELCTLT:3.3UF,+75-10%,350VDC	55680	UHU2V3RTEA
A3C1075	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A3C1101	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A3C1102	290-0942-00			CAP.,FXD.ELCTLT:100UF,+100-10%,25V	56289	672D107H025CG2C
A3C1110	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A3C1111	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A3C1112	290-0782-00	B010100	B013199	CAP.,FXD,ELCTLT:4.7UF,+75-10%,35V	55680	ULA1V4R7TEA
A3C1112	290-0782-01	B013200		CAP.,FXD,ELCTLT:4.7UF,20%,35VDC		
A3C1113	290-0798-00			CAP.,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187HO4ODM5C
A3C1114	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A3C1115	290-0800-00			CAP.,FXD,ELCTLT:250UF,+100-10%,20V	56289	672D257H0200M5C
A3C1116	290-0798-00			CAP.,FXD,ELCTLT:180UF,+100-10%,40V	56289	672D187HO4ODM5C
A3C1120	290-0939-00			CAP.,FXD,ELCTLT:10UF,+100-10%,100V	56289	672D106H100CG2C
A3C1130	290-0939-00			CAP.,FXD,ELCTLT:10UF,+100-10%,100V	56289	672D106H100CG2C
A3C1132	290-0880-00			CAP.,FXD,ELCTLT:10UF,+50-10%,160V	55680	UHU2C100TEA
A3CR1022	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A3CR1023	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR1028	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR1030	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR1034	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR1035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A3CR1040	152-0075-00			SEMICOND DEVICE:GE,25V,40MA	14433	G866
A3CR1050	152-0661-00			SEMICOND DEVICE:RECT,SI,600V,3A,FAST	04713	MR856
A3CR1060	152-0040-00			SEMICOND DEVICE:SILICON,600V,1A	15238	LG109
A3CR1062	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A3CR1063	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A3CR1064	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A3CR1065	152-0333-00			SEMICOND DEVICE:SILICON,55V,200MA	07263	FDH-6012
A3CR1070	152-0040-00			SEMICOND DEVICE:SILICON,600V,1A	15238	LG109
A3CR1072	152-0066-00			SEMICOND DEVICE:SILICON,400V,750MA	14433	LG4016
A3CR1101	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00

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A3CR1102	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1103	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1104	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1105	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1106	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1110	152-0794-00			SEMICOND DEVICE:RECT,SI,10A,30V	81483	95-4269
A3CR1113	152-0633-00			SEMICOND DEVICE:RECT,SI,30V,3A	04713	1N5821
A3CR1114	152-0633-00			SEMICOND DEVICE:RECT,SI,30V,3A	04713	1N5821
A3CR1115	152-0633-00			SEMICOND DEVICE:RECT,SI,30V,3A	04713	1N5821
A3CR1116	152-0633-00			SEMICOND DEVICE:RECT,SI,30V,3A	04713	1N5821
A3CR1121	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1122	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1123	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1124	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1131	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3CR1132	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A3F1101	159-0059-00			FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A3F1102	159-0059-00			FUSE,WIRE LEAD:5A,FAST-BLOW	000HX	SPI-5A
A3L1110	108-0554-00			COIL,RF:5UH	80009	108-0554-00
A3L1113	108-1144-00			COIL,RF:FIXED,27UH	34479	RL1284
A3L1114	108-1144-00			COIL,RF:FIXED,27UH	34479	RL1284
A3L1115	108-1144-00			COIL,RF:FIXED,27UH	34479	RL1284
A3L1116	108-1144-00			COIL,RF:FIXED,27UH	34479	RL1284
A3Q1021	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A3Q1022	151-0192-00	B010100	B013199	TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A3Q1022	151-0192-05	B013200		TRANSISTOR:SILICON,NPN,SEL FROM MP5651		
A3Q1029	151-0254-00			TRANSISTOR:SILICON,NPN	03508	X38L3118
A3Q1030	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A3Q1040	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A3Q1050	151-1152-00			TRANSISTOR:MOSFE,N-CHANNEL,SI,TO-220	04713	STP3002
A3Q1060	151-1152-00			TRANSISTOR:MOSFE,N-CHANNEL,SI,TO-220	04713	STP3002
A3Q1062	151-0302-00			TRANSISTOR:SILICON,NPN	07263	S038487
A3Q1070	151-1152-00			TRANSISTOR:MOSFE,N-CHANNEL,SI,TO-220	04713	STP3002
A3R1017	315-0103-00	B010100	B013199	RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R1018	315-0394-00			RES.,FXD,CMPSN:390K OHM,5%,0.25W	01121	CB3945
A3R1019	315-0394-00			RES.,FXD,CMPSN:390K OHM,5%,0.25W	01121	CB3945
A3R1020	301-0274-00			RES.,FXD,CMPSN:270K OHM,5%,0.50W	01121	EB2745
A3R1021	315-0103-00	B010100	B013199	RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R1022	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A3R1023	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A3R1024	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A3R1025	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A3R1027	321-0431-00			RES.,FXD,FILM:301K OHM,1%,0.125W	91637	MFF1816G30102F
A3R1028	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	24546	NA4D1004F
A3R1029	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A3R1030	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R1031	315-0334-00			RES.,FXD,CMPSN:330K OHM,5%,0.25W	01121	CB3345
A3R1032	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	CMF55116G30101F
A3R1033	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A3R1034	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R1035	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R1036	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R1037	315-0562-00			RES.,FXD,CMPSN:5.6K OHM,5%,0.25W	01121	CB5625

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A3R1040	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A3R1041	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A3R1042	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A3R1044	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A3R1045	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A3R1046	321-0422-00			RES.,FXD,FILM:243K OHM,1%,0.125W	91637	MFF1816G24302F
A3R1050	308-0843-00			RES.,FXD WW:0.2 OHM,5%,1.0W	91637	RS1AR2000JT/R
A3R1052	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A3R1060	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A3R1061	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A3R1062	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A3R1063	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A3R1064	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A3R1065	315-0124-00			RES.,FXD,CMPSN:120K OHM,5%,0.25W	01121	CB1245
A3R1066	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A3R1067	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A3R1068	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A3R1069	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A3R1070	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A3R1071	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A3R1072	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A3R1075	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A3R1101	307-0103-00	B010100	B019999	RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A3R1102	307-0103-00	B010100	B019999	RES.,FXD,CMPSN:2.7 OHM,5%,0.25W	01121	CB27G5
A3R1129	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A3RL1060	108-0329-00			COIL,RF:2.5UH	80009	108-0329-00
A3T1020	120-1449-00	B010100	B013199	XFMR,COM MODE:	02113	P104
A3T1020	120-1244-00	B013200		XFMR,RF:COMMON MODE,13MN,0.5A		
A3T1050	120-1417-00			XFMR,RF:POWER HIGH FREQUENCY	80009	120-1417-00
A3T1060	120-1437-00			XFMR,PWR,STPDN:	80009	120-1437-00
A3U1029	156-0885-00			MICROCIRCUIT,LI:OPTOELECTRONIC ISOLATOR	04713	S0C123A
A3U1030	156-1627-00			MICROCIRCUIT,LI:POWER WIDTH MODULATED CONT	01295	TL594CN
A3U1040	156-0885-00			MICROCIRCUIT,LI:OPTOELECTRONIC ISOLATOR	04713	S0C123A
A3U1062	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A3U1064	156-0366-02			MICROCIRCUIT,DI:DUAL D FLIP-FLOP,CHK	80009	156-0366-02
A3U1066	156-0328-00			MICROCIRCUIT,DI:DUAL CLOCK DRIVER	27014	DS0026C
A3VR1020	152-0166-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ11738RL
A3VR1062	152-0168-00			SEMICOND DEVICE:ZENER,0.4W,12V,5%	04713	SZG35009K4
A3W1021	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A3W1022	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A3W1050	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A3W1060	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A3W1101	131-0566-00	B020000		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A3W1102	131-0566-00	B020000		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

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A4	670-7278-XX			CKT BOARD ASSY:BUS MONITOR	80009	670-7278-00
A4C2830	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2835	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2851	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2855	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2860	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2885	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2901	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2911	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A4C2913	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2926	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2940	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2950	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2960	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2970	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2980	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4C2990	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A4R2805	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R2830	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A4R2841	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R2842	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R2843	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R2844	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R2850	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R2901	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A4R2902	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A4R2903	321-1296-03			RES.,FXD,FILM:12K OHM,0.25%,0.125W	91637	MFF1816D12001C
A4R2905	321-0816-03			RES.,FXD,FILM:5K OHM,0.25%,0.125W	91637	MFF1816D50000C
A4R2910	321-0685-00			RES.,FXD,FILM:30K OHM,0.5%,0.125W	91637	MFF1816D30001D
A4R2911	321-0685-00			RES.,FXD,FILM:30K OHM,0.5%,0.125W	91637	MFF1816D30001D
A4R2912	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A4R2913	321-0198-00			RES.,FXD,FILM:1.13K OHM,1%,0.125W	91637	MFF1816G11300F
A4R2914	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A4R2915	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A4R2920	315-0334-00			RES.,FXD,CMPSN:330K OHM,5%,0.25W	01121	CB3345
A4R2921	321-0724-03			RES.,FXD,FILM:13.6K OHM,0.25W,0.125W	24546	NC55C1362C
A4R2922	321-0756-00			RES.,FXD,FILM:50K OHM,1%,0.125W	24546	NA55D5002F
A4R2923	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A4R2924	321-0414-00			RES.,FXD,FILM:200K OHM,1%,0.125W	91637	MFF1816G20002F
A4R2925	321-0235-02			RES.,FXD,FILM:2.74K OHM,0.5%,0.125W	91637	MFF1816G2741F
A4R2926	321-0225-01			RES.,FXD,FLIM:2.15K OHM,5%,0.125W	80009	321-0255-01
A4R2927	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A4R2928	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R2929	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R2940	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A4R2945	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A4R2975	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A4R2985	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A4U2800	156-0514-01			MICROCIRCUIT,DI:DIFF 4-CHANNEL MUX,SEL	80009	156-0514-01
A4U2805	156-0514-01			MICROCIRCUIT,DI:DIFF 4-CHANNEL MUX,SEL	80009	156-0514-01
A4U2810	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U2820	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A4U2830	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393

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A4U2835	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A4U2850	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A4U2855	156-0383-02			MICROCIRCUIT,DI:QUAD 2-INP NOR GATE	01295	SN74LS02
A4U2860	156-0975-02			MICROCIRCUIT,DI:UNIV SHIFT/STORAGE RGTR	01295	SN74LS299N3/J4
A4U2865	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A4U2870	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A4U2880	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A4U2885	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A4U2890	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U2900	156-0386-02			MICROCIRCUIT,DI:TRIPLE 3-INP NAND GATE	27014	DM74LS10N
A4U2905	156-0982-03			MICROCIRCUIT,DI:OCTAL-D-EDGE FF,SCRN	01295	SN74LS374 N3
A4U2910	156-1555-00			MICROCIRCUIT,LI:D/A CONVERTER	34335	AM6080PC
A4U2920	156-0716-01			MICROCIRCUIT,DI:128 X 8 STATIC RAM,SCRN	80009	156-0716-01
A4U2930	160-1631-00			MICROCIRCUIT,DI:4096 X 8 EPROM	80009	160-1631-00
A4U2935	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3
A4U2940	156-1172-01			MICROCIRCUIT,DI:DUAL 4 BIT CNTR	01295	SN74LS393
A4U2950	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A4U2960	156-0796-01			MICROCIRCUIT,DI:8 STG SHF & STORE BUS RGTR	80009	156-0796-01
A4U2965	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U2970	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A4U2980	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A4U2985	156-0768-01			MICROCIRCUIT,DI:BIDIRECT UNIV SR,SCREENED	01295	SN74LS194A9NP3 O
A4U2990	156-0381-02			MICROCIRCUIT,DI:QUAD 2-INP EXCL OR GATE	01295	SN74LS86
A4U2995	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3 OR
A4VR2805	152-0217-00			SEMICOND DEVICE:ZENER,0.4W,8.2V,5%	04713	SZG20
A4VR2925	152-0662-00			SEMICOND DEVICE:ZENER,0.4W,5V,1%	04713	SZG195
A4W2851	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A4W2913	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

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A5	670-7279-XX			CKT BOARD ASSY:DIGITAL CONTROL	80009	670-7279-00
A5C2041	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2188	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2203	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2217	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2218	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2221	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2222	281-0814-00			CAP.,FXD,CER DI:100PF,10%,100V	04222	GC101A101K
A5C2223	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A5C2224	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A5C2240	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2318	281-0791-00			CAP.,FXD,CER DI:270PF,10%,100V	04222	GC101C271K
A5C2326	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2327	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2328	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2329	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2330	285-1187-00			CAP.,FXD,MTLZD:0.47UF,10%,100V	55112	160.47 K 100F
A5C2346	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2354	290-0943-00			CAP.,FXD,ELCTLT:47UF,+50-10%,25V	55680	ULB1E470TECANA
A5C2440	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2441	285-1187-00			CAP.,FXD,MTLZD:0.47UF,10%,100V	55112	160.47 K 100F
A5C2443	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2475	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2485	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2486	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2524	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2527	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2530	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A5C2536	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2540	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A5C2542	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A5C2550	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2565	281-0816-00			CAP.,FXD,CER DI:82PF,5%,100V	96733	R3247
A5C2566	281-0819-00			CAP.,FXD,CER DI:33PF,5%,50V	72982	8035BC0G330
A5C2572	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2575	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2586	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2637	283-0423-00			CAP.,FXD,CER DI:0.22UF,+80-20%,50V	04222	DG015E224Z
A5C2638	285-1187-00			CAP.,FXD,MTLZD:0.47UF,10%,100V	55112	160.47 K 100F
A5C2640	285-1187-00			CAP.,FXD,MTLZD:0.47UF,10%,100V	55112	160.47 K 100F
A5C2642	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2661	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5C2734	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A5CR2004	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2021	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2122	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2651	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2723	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2731	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2733	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2742	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5CR2744	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A5Q2025	151-0188-00			TRANSISTOR:SILICON,PNP	04713	SPS6868K
A5Q2322	151-0341-00			TRANSISTOR:SILICON,NPN	07263	S040065

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A5R2012	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A5R2013	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2014	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2015	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A5R2016	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A5R2017	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2018	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2019	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A5R2020	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2022	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A5R2023	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A5R2028	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	01121	CB1345
A5R2029	315-0134-00			RES.,FXD,CMPSN:130K OHM,5%,0.25W	01121	CB1345
A5R2040	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2103	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2113	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2123	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A5R2025	315-0103-00	B013200		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2127	311-1137-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A5R2132	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2140	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2141	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2142	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2143	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2144	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2145	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2162	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2185	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2186	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2187	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2224	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2227	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A5R2228	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A5R2229	321-0431-00			RES.,FXD,FILM:301K OHM,1%,0.125W	91637	MFF1816G30102F
A5R2230	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2241	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2242	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2243	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2244	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2245	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2246	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0. 25W	01121	CB1015
A5R2285	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2286	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2287	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2288	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2297	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2298	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2299	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2303	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2312	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2313	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2314	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2315	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2316	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5R2317	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2319	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2320	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2324	321-0177-02			RES.,FXD,FILM:681 OHM,0.5%,0.125W	80009	321-0177-02
A5R2325	321-0177-02			RES.,FXD,FILM:681 OHM,0.5%,0.125W	80009	321-0177-02
A5R2330	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A5R2340	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2341	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2342	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2343	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2344	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2345	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2444	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2445	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2446	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2447	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2448	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2449	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2450	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2451	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2452	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2463	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2504	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2505	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2506	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2507	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2508	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2509	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2510	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2511	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2512	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2513	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2514	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2515	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2516	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2517	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2518	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2519	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2520	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2521	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2522	321-0917-03			RES.,FXD,FILM:27.2K OHM,0.25%,0.125W	91637	MFF1816D27201C
A5R2525	321-0327-03			RES.,FXD,FILM:24.9K OHM,0.25%,0.125W	24546	NC55C2492C
A5R2532	321-0324-00			RES.,FXD,FILM:23.2K OHM,1%,0.125W	91637	MFF1816G23201F
A5R2534	321-0289-02			RES.,FXD,FILM:10K OHM,0.5%,0.125W	91637	CMF55-116D10001D
A5R2535	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A5R2539	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2540	321-1618-02			RES.,FXD,FILM:6.5K OHM,0.5%,0.125W	91637	MFF1618D65000D
A5R2541	321-0923-02			RES.,FXD,FILM:25.1K OHM,0.5%.0.125W	24546	NC55C2512D
A5R2542	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A5R2543	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A5R2545	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2546	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2547	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2549	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815

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A5R2551	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2552	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2553	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2564	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A5R2571	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2573	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5R2608	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A5R2609	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2610	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2611	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2612	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A5R2613	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2614	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2645	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2646	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A5R2647	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A5R2648	315-0243-00			RES.,FXD,CMPSN:24K OHM,5%,0.25W	01121	CB2435
A5R2649	315-0273-00			RES.,FXD,CMPSN:27K OHM,5%,0.25W	01121	CB2735
A5R2650	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2652	315-0225-00			RES.,FXD,CMPSN:2.2M OHM,5%,0.25W	01121	CB2255
A5R2662	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2663	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2703	315-0471-00			RES.,FXD,CMPSN:470 OHM,5%,0.25W	01121	CB4715
A5R2730	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2731	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2732	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A5R2734	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A5R2735	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2741	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A5R2742	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A5R2745	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A5R2764	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A5TP503	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5TP504	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5TP505	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5TP506	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5TP507	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5TP509	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5TP510	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5TP511	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
A5U2008	156-1566-00			MICROCIRCUIT,DI:EPROM,100 X 14	80009	156-1566-00
A5U2034	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A5U2092	156-1342-01			MICROCIRCUIT,DI:MPU,8 BIT W/CLK	07263	F68A08(P OR D)
A5U2108	156-1220-00			MICROCIRCUIT,DI:HEX BUS DRIVER	01295	SN74LS365A
A5U2118	156-1245-00			MICROCIRCUIT,LI:7 XSTR,HV/HIGH CUR	04713	MC1413PDS
A5U2134	156-0865-02			MICROCIRCUIT,DI:OCTAL D-TYPE FF W/CLEAR	01295	SN74LS273NP3
A5U2162	160-1628-03	B010100	B010999	MICROCIRCUIT,DI:4096 X 8 EPROM	80009	160-1628-03
A5U2162	160-1628-04	B011000	B012499	MICROCIRCUIT,DI:8K X 8 EPROM,PRGM	80009	160-1628-04
A5U2162	160-1628-06	B012500		MICROCIRCUIT,DI:4096 X 8 EPROM,PRGM	80009	160-1628-06
A5U2178	160-1625-03	B010100	B010999	MICROCIRCUIT,DI:8192 X 8 EPROM PROG	80009	160-1625-03
A5U2178	160-1625-04	B011000	B012499	MICROCIRCUIT,DI:8192 X 8 EPROM PROG	80009	160-1625-04
A5U2178	160-1625-06	B012500		MICROCIRCUIT,DI:8192 X 8 EPROM PROG	80009	160-1625-06
A5U2194	156-0956-02			MICROCIRCUIT,DI:OCTAL BFR W/3 STATE OUT	01295	SN74LS244NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A5U2208	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A5U2214	156-1126-01			MICROCIRCUIT,LI:VOLTAGE COMPARATOR,SEL	01295	LM311JG4
A5U2234	156-1589-00			MICROCIRCUIT,LI:DA CONVERTER,12 BIT,HI SPD	34335	AM6012PC
A5U2294	156-1065-01			MICROCIRCUIT,DI:OCTAL D TYPE TRANS LATCHES	34335	AM74LS373
A5U2308	156-0391-02			MICROCIRCUIT,DI:HEX LATCH W/CLEAR	01295	SN74LS174
A5U2335	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A5U2362	160-1627-03	B010100	B010999	MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1627-03
A5U2362	160-1627-05	B011000	B012499	MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1627-05
A5U2362	160-1626-06	B012500		MICROCKT,DI:8192 X 8 EPROM,PRGM	80009	1601626-06
A5U2378	160-1626-03	B010100	B010999	MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1626-03
A5U2378	160-1626-05	B011000	B012499	MICROCIRCUIT,DI:8192 X 8 EPROM,PRGM	80009	160-1626-05
A5U2378	160-1626-06	B012500		MICROCKT,DI:8192 X 8 EPROM,PRGM	80009	1601626-06
A5U2408	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A5U2418	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A5U2427	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A5U2435	156-1200-01			MICROCIRCUIT,LI:OPERATIONAL AMPL,QUAD	01295	TL074CN/PEP3
A5U2456	156-1486-00			MICROCIRCUIT,DI:8 CHANNEL DATA SEL,SCREENED	04713	MC14512BCLD
A5U2468	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A5U2480	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A5U2556	156-0385-02			MICROCIRCUIT,DI:HEX INVERTER	01295	SN74LS04
A5U2580	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A5U2596	156-1026-02			MICROCIRCUIT,DI:4/1 LINE DECODER,BURN-IN	80009	156-1026-02
A5U2634	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A5U2656	156-0804-02			MICROCIRCUIT,DI:QUADRUPLE S-R LATCH,SCRN	01295	SN74LS279NP3
A5U2668	156-0895-01			MICROCIRCUIT,DI:14 BIT BINARY CNTR,BURN-IN	04713	MC14020BCLD
A5U2770	156-0469-02			MICROCIRCUIT,DI:3/8 LINE DCDR	01295	SN74LS138NP3
A5VR2003	152-0127-00			SEMICOND DEVICE:ZENER,0.4W,7.5V,5%	04713	SZG35009K2
A5VR2526	152-0278-00			SEMICOND DEVICE:ZENER,0.4W,3V,5%	04713	SZG35009K20
A5W2143	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A5W2526	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A5Y2568	158-0248-00			XTAL UNIT,QTZ:10MHZ, 0.01%,SERIES	80009	158-0248-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6	----- -----			CKT BOARD ASSY:FRONT PANEL		
A6	----- -----			(AVAILABLE AT 672-1038-XX LEVEL ONLY)		
A6CR3000	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3001	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3002	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3003	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3010	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3011	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3012	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3013	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3020	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3021	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3022	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3023	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3025	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3030	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3031	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3032	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3033	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3035	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3050	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3075	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3105	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3110	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3115	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3120	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3175	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3176	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3177	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3178	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3179	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3180	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3181	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3182	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3183	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3184	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3185	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3200	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3210	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3220	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3250	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3260	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6CR3270	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A6DS3300	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3301	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3302	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3303	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3304	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3310	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3311	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3312	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3313	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3314	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3325	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6DS3326	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3327	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3329	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3330	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3331	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3350	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3351	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3352	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3353	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3354	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3375	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3376	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3377	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3378	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3379	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3380	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3390	150-1105-00			LT EMITTING DIO:YELLOW,30MA	50434	QLMP-0449
A6DS3391	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3392	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6DS3393	150-1109-00			LT EMITTING DIO:GREEN, 30MA	73138	SP732
A6R3021	311-2180-00			RES.,VAR,NONWW:LINEAR,2K OHM,30%,0.5W	32997	91Z1A-Z45-EA0019
A6R3031	311-2180-00			RES.,VAR,NONWW:LINEAR,2K OHM,30%,0.5W	32997	91Z1A-Z45-EA0019
A6R3050	311-2180-00			RES.,VAR,NONWW:LINEAR,2K OHM,30%,0.5W	32997	91Z1A-Z45-EA0019
A6R3075	311-2180-00			RES.,VAR,NONWW:LINEAR,2K OHM,30%,0.5W	32997	91Z1A-Z45-EA0019
A6R3100	311-2180-00			RES.,VAR,NONWW:LINEAR,2K OHM,30%,0.5W	32997	91Z1A-Z45-EA0019
A6R3125	311-2181-00			RES.,VAR,NONWW:LINEAR,5K OHM,30%,0.25W	32997	91Z2D-Z45-EA0020
A6R3150	311-2181-00			RES.,VAR,NONWW:LINEAR,5K OHM,30%,0.25W	32997	91Z2D-Z45-EA0020
A6R3190	311-2180-00			RES.,VAR,NONWW:LINEAR,2K OHM,30%,0.5W	32997	91Z1A-Z45-EA0019
A6R3200	311-2182-00			RES.,VAR,NONWW:LINEAR,5K OHM,30%,0.5W	32997	91Z2D-Z45-EA0021
A6R3210	311-2180-00			RES.,VAR,NONWW:LINEAR,2K OHM,30%,0.5W	32997	91Z1A-Z45-EA0019
A6R3300	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A6R3310	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A6R3325	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A6R3326	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A6R3327	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A6R3350	307-0611-00			RES NTWK,FXD FI:7,150 OHM,5%,1.125W	32997	4308R101-151J
A6S3000	260-2094-00			SWITCH,PUSH:4 BTN,SINGLE POLE,VERT CONT	80009	260-2094-00
A6S3010	260-2094-00			SWITCH,PUSH:4 BTN,SINGLE POLE,VERT CONT	80009	260-2094-00
A6S3020	260-2086-00			SWITCH,ROTARY:VOLTS/DIV	76784	T-51621-001
A6S3025	260-2100-00			SWITCH,LEVER:DPDT,1 SECT,3 POSN,30 DEG	22753	OBD
A6S3030	260-2086-00			SWITCH,ROTARY:VOLTS/DIV	76784	T-51621-001
A6S3035	260-2100-00			SWITCH,LEVER:DPDT,1 SECT,3 POSN,30 DEG	22753	OBD
A6S3050	260-2095-00			SWITCH,PUSH:2 BTN,SINGLE POLE,CHAN 3 &4	80009	260-2095-00
A6S3105	260-2087-00			SWITCH,PUSH:1 SINGLE BTN,SINGLE POLE,HO	80009	260-2087-00
A6S3110	260-2093-00			SWITCH,PUSH:3 BTN,SINGLE POLE,HORIZ	80009	260-2093-00
A6S3175	260-2085-00			SWITCH,ROTARY:TIME/DIV	76854	5-51625-001
A6S3185	260-2108-00	B010100	B019999	SWITCH,PUSH:SPST,0.1A,125VAC	80009	260-2108-00
A6S3185	260-2108-01	B020000				
A6S3210	260-2088-00			SWITCH,PUSH:SINGLE BTN,SINGLE POLE,TRIG	80009	260-2088-00
A6S3220	260-2088-00			SWITCH,PUSH:SINGLE BTN,SINGLE POLE,TRIG	80009	260-2088-00
A6S3250	260-2100-00			SWITCH,LEVER:DPDT,1 SECT,3 POSN,30 DEG	22753	OBD
A6S3260	260-2100-00			SWITCH,LEVER:DPDT,1 SECT,3 POSN,30 DEG	22753	OBD
A6S3270	260-2100-00			SWITCH,LEVER:DPDT,1 SECT,3 POSN,30 DEG	22753	OBD

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A6U3300	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3)
A6U3325	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3)
A6U3350	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3)
A6U3375	156-0651-02			MICROCIRCUIT,DI:8 BIT PRL-OUT SER SHF RGTR	01295	SN74LS164(NP3)
A6W651	175-4584-00			CA ASSY,SP,ELEC:20,28 AWG,4.0 L	80009	175-4584-00
A6W652	175-4582-00			CA ASSY,SP,ELEC:26,28 AWG,8.5 L	80009	175-4582-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A7	670-7284-XX			CKT BOARD ASSY:FRONT PANEL VARIABLE	80009	670-7284-00
A7R3420	311-2183-00			RES.,VAR,NONWW:LINEAR,5K OHM,30%,0.5W	32997	91ZID-Z36-EA0024
A7R3430	311-2183-00			RES.,VAR,NONWW:LINEAR,5K OHM,30%,0.5W	32997	91ZID-Z36-EA0024
A7R3475	311-2183-00			RES.,VAR,NONWW:LINEAR,5K OHM,30%,0.5W	32997	91ZID-Z36-EA0024
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A8	670-7280-XX			CKT BOARD ASSY:SCALE ILLUMINATION	80009	670-7280-00
A8DS90	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	74276	NE2V-T
A8DS90	----- -----			(SUBPART OF HV MODULE 152-0805-00)		
A8DS91	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	74276	NE2V-T
A8DS91	----- -----			(SUBPART OF HV MODULE 152-0805-00)		
A8DS100	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15
A8DS101	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15
A8DS102	150-0057-01			LAMP,INCAND:5V,0.115A,WIRE LD,SEL	76854	17AS15

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9	670-7277-XX			CKT BOARD ASSY:HIGH VOLTAGE	80009	670-7277-00
A9C90	283-0115-00	B010100	B012149	CAP.,FXD,CER DI:47PF,5%,200V	59660	805-519-C0G0470J
A9C91	283-0084-00			CAP.,FXD,CER DI:270PF,5%,1000V	59660	838 533X5F0 2715
A9C1812	285-1236-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	84411	TEK-245-22304
A9C1813	285-1236-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	84411	TEK-245-22304
A9C1886	285-1236-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	84411	TEK-245-22304
A9C1888	285-1236-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	84411	TEK-245-22304
A9C1889	285-1236-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	84411	TEK-245-22304
A9C1890	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C1891	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C1909	281-0783-00			CAP.,FXD,CER DI:0.1UF,20%,100V	96733	ADVIXE
A9C1912	281-0798-00			CAP.,FXD,CER DI:51PF,1%,100V	96733	R2928
A9C1915	281-0783-00	B011000		CAP.,FXD,CER DI:0.1UF,20%,100V	96733	ADVIXE
A9C1932	281-0775-00			CAP.,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A9C1950	281-0766-00			CAP.,FXD,CER DI:100PF,20%,200V	04222	GC106C101M
A9C1951	290-0269-00			CAP.,FXD,ELCTLT:0.22UF,5%,35V	56289	162D224X5035BC2
A9C1971	285-1236-00			CAP.,FXD,PLSTC:0.022UF,20%,400V	84411	TEK-245-22304
A9C1972	290-0747-00			CAP.,FXD,ELCTLT:100UF,+50-10%,25V	56289	500D148
A9C1973	281-0771-00			CAP.,FXD,CER DI:0.0022UF,20%,200V	56289	292C Z5U222M200B
A9C1980	281-0773-00			CAP.,FXD,CER DI:0.01UF,10%,100V	04222	SA201C103KAA
A9C1990	285-1096-00			CAP.,FXD,PLSTC:1UF,10%,50V	14752	230B1A105K
A9C1991	281-0771-00			CAP.,FXD,CER DI:0.0022UF,20%,200V	56289	292C Z5U222M200B
A9CR1894	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A9CR1895	152-0400-00			SEMICOND DEVICE:SILICON,400V,1A	80009	152-0400-00
A9CR1915	152-0061-00	B011000		SEMICOND DEVICE:SILICON,175V,100MA	07263	FDH2161
A9CR1930	152-0061-00			SEMICOND DEVICE:SILICON,175V,100MA	07263	FDH2161
A9CR1950	152-0061-00			SEMICOND DEVICE:SILICON,175V,100MA	07263	FDH2161
A9CR1951	152-0787-00	B010100	B010477	SEMICOND DEVICE:RECT,SI,12KV,3MA,A-LZV	000JF	ESJA25-12
A9CR1953	152-0061-00			SEMICOND DEVICE:SILICON,175V,100MA	07263	FDH2161
A9CR1990	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A9DS90	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	74276	NE2V-T
A9DS91	150-0030-00			LAMP,GLOW:NEON,T-2,60 TO 90 VOLTS	74276	NE2V-T
A9L1974	108-0318-00			COIL,RF,CMPSN:100 OHM, 5%, 0.25W	32159	81000M
A9Q1851	151-0443-00			TRANSISTOR:SILICON,PNP	04713	SPS7950
A9Q1852	151-0443-00			TRANSISTOR:SILICON,PNP	04713	SPS7950
A9Q1890	151-0443-00			TRANSISTOR:SILICON,PNP	04713	SPS7950
A9Q1980	151-0444-00			TRANSISTOR:SILICON,NPN	04713	SPS797
A9Q1981	151-0745-00			TRANSISTOR:SILICON,PNP	000IG	2SA1077G
A9R1812	315-0100-02			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A9R1813	315-0100-02			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A9R1820	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A9R1830	307-0110-00	B010100	B013249	RES.,FXD,CMPSN:3 OHM,5%,0.25W	01121	CB30G5
A9R1834	311-1227-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	32997	3386F-T04-502
A9R1842	311-1227-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	32997	3386F-T04-502
A9R1848	311-1227-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	32997	3386F-T04-502
A9R1853	321-0447-00			RES.,FXD,FILM:442K OHM,1%,0.125W	24546	NA55D4423F
A9R1854	321-0435-00			RES.,FXD,FILM:332K OHM,1%,0.125W	91637	MFF1816G33202F
A9R1855	321-0407-00			RES.,FXD,FILM:169K OHM,1%,0.125W	91637	MFF1816G16902F
A9R1856	321-0367-00			RES.,FXD,FILM:64.9K OHM,1%,0.125W	91637	MFF1816G64901F
A9R1857	321-0364-00			RES.,FXD,FILM:60.4K OHM,1%,0.125W	91637	MFF1816G60401F
A9R1858	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A9R1864	311-1230-00			RES.,VAR,NONWIR:20K OHM,20%,0.50W	32997	3386F-T04-203
A9R1870	311-1214-00			RES.,VAR,NONWIR:200K OHM,20%,0.50W	73138	72-16-0
A9R1871	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A9R1872	315-0184-00			RES.,FXD,CMPSN:180K OHM,5%,0.25W	01121	CB1845
A9R1873	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A9R1878	311-1214-00			RES.,VAR,NONWIR:200K OHM,20%,0.50W	73138	72-16-0
A9R1880	315-0434-00			RES.,FXD,CMPSN:430K OHM,5%,0.25W	01121	CB4345
A9R1881	321-0385-00			RES.,FXD,FILM:100K OHM,1%,0.125W	91637	MFF1816G10002F
A9R1890	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A9R1891	321-0481-04			RES.,FXD,FILM:1M OHM,0.1%,0.125W	91637	HFF1816D10003B
A9R1892	321-0693-00			RES.,FXD,FILM:68.1K OHM,0.5%,0.125W	91637	CMF55-116G68101D
A9R1893	321-0481-04			RES.,FXD,FILM:1M OHM,0.1%,0.125W	91637	HFF1816D10003B
A9R1895	~~315-0123-00~~	315-0302-00		RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A9R1896	315-0100-02			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A9R1897	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R1898	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R1910	321-0271-00			RES.,FXD,FILM:6.49K OHM,1%,0.125W	91637	MFF1816G64900F
A9R1911	321-0245-00			RES.,FXD,FILM:3.48K OHM,1%,0.125W	91637	MFF1816G34800F
A9R1913	315-0101-03	B011000		RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A9R1920	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A9R1921	315-0100-02			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A9R1922	315-0101-06	B010100	0 B01079	RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A9R1922	315-0331-03	B010800		RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A9R1933	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A9R1941	315-0201-00			RES.,FXD,CMPSN:200 OHM,5%,0.25W	01121	CB2015
A9R1944	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	01121	CB1635
A9R1945	321-0385-07			RES.,FXD,FILM:100K OHM,0.1%,0.125W	91637	MFF1816C10002B
A9R1946	315-0475-00					
A9R1950	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A9R1951	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A9R1952	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A9R1953	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A9R1971	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A9R1972	315-0224-00			RES.,FXD,CMPSN:220K OHM,5%,0.25W	01121	CB2245
A9R1973	315-0163-00			RES.,FXD,CMPSN:16K OHM,5%,0.25W	01121	CB1635
A9R1990	321-0693-00			RES.,FXD,FILM:68.1K OHM,0.5%,0.125W	91637	CMF55-116G68101D
A9R1991	315-0107-00			RES.,FXD,CMPSN:100M OHM,5%,0.25W	01121	CB1075
A9R1992	315-0244-00			RES.,FXD,CMPSN:240K OHM,5%,0.25W	01121	CB2445
A9R1994	321-0402-00			RES.,FXD,FILM:150K OHM,1%,0.125W	24546	NA55D1503F
A9T1970	120-1418-00	B010100	B013249	XFMR,PWR SU&SDN:HIGH VOLTAGE	80009	120-1418-00
A9T1970	120-1418-01	B013250		XFMR,PWR,SU&SDN:HIGH VOLTAGE	80009	120-1418-01
A9U1890	156-1191-01			MICROCIRCUIT,LI:DUAL BI-FET OP-AMP,8 DIP	01295	TL072ACP3
A9U1956	156-0158-07			MICROCIRCUIT,LI:DUAL OPNL AMPL,SCREENED	01295	MC1458JG4
A9U1830	152-0805-00			SEMICOND DEVICE:HV MULTIPLIER,20KV INPUT	80009	152-0805-00
A9VR1891	152-0282-00			SEMICOND DEVICE:ZENER,0.4W,30V,5%	14552	1N972B
A9W1909	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10	670-7390-XX			CKT BOARD ASSY:FAN MOTOR	80009	670-7390-00
A10B1690	147-0035-00			MOTOR,DC:BRUSHLESS,10-15VDC,145MA	25088	1AD3001-0A
A10C1698	290-0804-00			CAP.,FXD,ELCTLT:10UF,+50-10%,25V	55680	ULA1E100TEA
A10CR1691	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR1692	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR1694	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR1696	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR1699	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10Q1698	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A10R1691	303-0150-00			RES.,FXD,CMPSN:15 OHM,5%,1W	01121	GB1505
A10R1692	321-0062-00			RES.,FXD,FILM:43.2 OHM,1%,0.125W	91637	CMF55-116G43R20F
A10R1693	323-0155-00			RES.,FXD,FILM:402 OHM,1%,0.50W	75042	CECT0-4020F
A10R1694	323-0155-00			RES.,FXD,FILM:402 OHM,1%,0.50W	75042	CECT0-4020F
A10R1695	321-0222-00			RES.,FXD,FILM:2K OHM,1%,0.125W	91637	MFF1816G20000F
A10R1697	321-0190-00			RES.,FXD,FILM:931 OHM,1%,0.125W	91637	MFF1816G931R0F
A10RT1696	307-0124-00			RES.,THERMAL:5K OHM,10%	50157	1D1618
A10U1690	156-0281-00			MICROCIRCUIT,LI:4 TRANSISTOR ARRAY	02735	89164
A13	307-1154-00			PASSIVE NETWORK:CRT TERMINATOR,FINISHED	80009	307-1154-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A14	670-8000-XX			CKT BOARD ASSY:DYNAMIC CENTERING	80009	670-8000-00
A14C3401	283-0421-00			CAP.,FXD,CER DI:0.1UF,+80-20%,50V	04222	DG015E104Z
A14R3401	311-1137-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A14R3402	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A14R3403	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A14R3404	321-0284-00			RES.,FXD,FILM:8.87K OHM,1%,0.125W	91637	MFF1816G88700F
A14R3405	315-0750-00			RES.,FXD,CMPSN:75 OHM,5%,0.25W	01121	CB7505
A14R3406	315-0123-00			RES.,FXD,CMPSN:12K OHM,5%,0.25W	01121	CB1235
A14R3407	311-1137-00			RES.,VAR,NONWIR:5K OHM,20%,0.50W	73138	72PX-67-0-502M
A14R3408	321-0284-00			RES.,FXD,FILM:8.87K OHM,1%,0.125W	91637	MFF1816G88700F
A14R3409	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A14R3410	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A14R3411	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A14U3401	156-0130-02			MICROCIRCUIT,LI:MODULATOR/DEMODULATOR,SCRN	04713	SC77162GH
A14U3402	156-0130-02			MICROCIRCUIT,LI:MODULATOR/DEMODULATOR,SCRN	04713	SC77162GH
A14VR3401	152-0227-00			SEMICOND DEVICE:ZENER,0.4W,6.2V,5%	04713	SZ13903

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				CHASSIS PARTS		
F90	159-0021-00			FUSE,CARTRIDGE:3AG,2A,250V,FAST-BLOW	71400	AGC 2
F90	----- -----			(SUBPART OF STANDARD AND OPT A4 ONLY)		
F90	159-0098-00	B010100	B01304	FUSE,CARTRIDGE:DIN,1.6A	E01.6	T0946
F90	----- -----			(SUBPART OF OPTS.A1,A2,A3,A5)		
F90	159-0229-00	B013050		FUSE,CARTRIDGE:5 X20MM,1.6A,250V,TIME/DLY	75915	213016EAK,1.6
F90	----- -----			(SUBPART OF OPTS.A1,A2,A3,A5)		
L90	108-0327-00			COIL,RF:48NH	80009	108-0327-00
LR1513	108-1132-00			COIL,RF,FXD,TERMINATION COMPENSATION		
LR1514	108-1132-00			COIL,RF,FXD,TERMINATION COMPENSATION		
R134	311-2174-00			RES.,VAR,NONWW:5 OHM,20%,0.5W LINEAR	12697	CM43515
R351	311-1428-00			RES.,VAR,NONWIR:20K OHM,1W	01121	10M959
R352	311-1428-00			RES.,VAR,NONWIR:20K OHM,1W	01121	10M959
R975	311-2174-00			RES.,VAR,NONWW:5 OHM,20%,0.5W LINEAR	12697	CM43515
R976	311-2174-00			RES.,VAR,NONWW:5 OHM,20%,0.5W LINEAR	12697	CM43515
R977	311-2174-00			RES.,VAR,NONWW:5 OHM,20%,0.5W LINEAR	12697	CM43515
S90	260-1967-00			SWITCH,SLIDE:DPDT,5A/250V	000FJ	4021.0512
S90	----- -----			(SUBPART OF 672-1037-01)		
S1020	260-0907-00			SW,THERMOSTATIC:OPEN 97.8,CL 75.6,10A,240V	93410	430-349
S3185	260-2108-00			SWITCH,PUSH:SPST,0.1A,125VAC	80009	260-2108-00
V900	154-0850-00			ELECTRON TUBE:CRT	80009	154-0850-00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it is in the low state.

Abbreviations are based on ANSI Y1.1-1972.

Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966 Drafting Practices.
Y14.2, 1973 Line Conventions and Lettering.
Y10.5, 1968 Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

American National Standard Institute
1430 Broadway
New York, New York 10018

Component Values

Electrical components shown on the diagrams are in the following units unless noted otherwise:

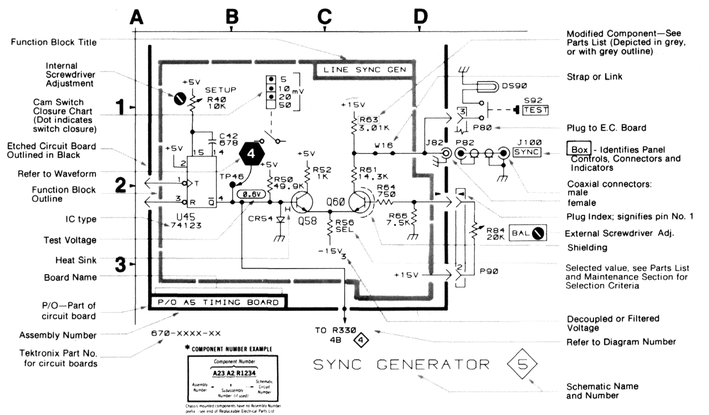
Capacitors = Values one or greater are in picofarads (pF). Values less than one are in microfarads (μF).
Resistors = Ohms (Ω).

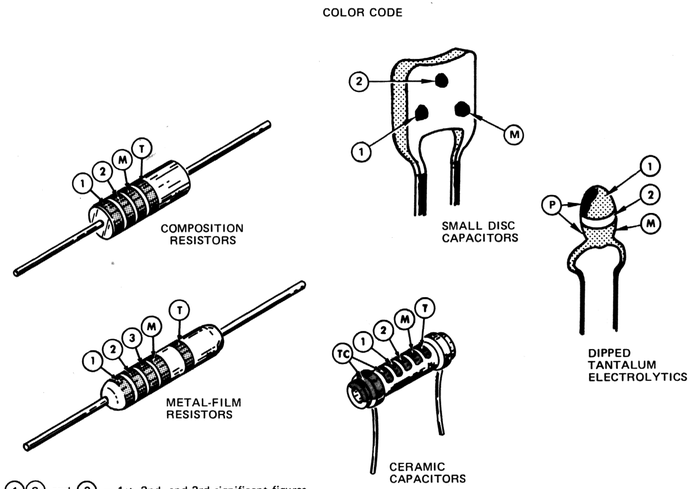
The information and special symbols below may appear in this manual.

Assembly Numbers and Grid Coordinates

Each assembly in the instrument is assigned an assembly number (e.g., A20). The assembly number appears on the circuit board outline on the diagram, in the title for the circuit board component location illustration, and in the lookup table for the schematic diagram and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assemblies in numerical sequence; the components are listed by component number *(see following illustration for constructing a component number).

The schematic diagram and circuit board component location illustration have grids. A lookup table with the grid coordinates is provided for ease of locating the component. Only the components illustrated on the facing diagram are listed in the lookup table. When more than one schematic diagram is used to illustrate the circuitry on a circuit board, the circuit board illustration may only appear opposite the first diagram on which it was illustrated; the lookup table will list the diagram number of other diagrams that the circuitry of the circuit board appears on.





COLOR	SIGNIFICANT FIGURES	RESISTORS		CAPACITORS			DIPPED TANTALUM VOLTAGE RATING
		MULTIPLIER	TOLERANCE	MULTIPLIER	TOLERANCE over 10 pF	TOLERANCE under 10 pF	
BLACK	0	1	———	1	±20%	±2 pF	4 VDC
BROWN	1	10	±1%	10	±1%	±0.1 pF	6 VDC
RED	2	10^2 or 100	±2%	10^2 or 100	±2%	———	10 VDC
ORANGE	3	10^3 or 1 K	±3%	10^3 or 1000	±3%	———	15 VDC
YELLOW	4	10^4 or 10 K	±4%	10^4 or 10,000	+100% −9%	———	20 VDC
GREEN	5	10^5 or 100 K	±½%	10^5 or 100,000	±5%	±0.5 pF	25 VDC
BLUE	6	10^6 or 1 M	±¼%	10^6 or 1,000,000	———	———	35 VDC
VIOLET	7	———	±1/10%	———	———	———	50 VDC
GRAY	8	———	———	10^{-2} or 0.01	+80% −20%	±0.25 pF	———·
WHITE	9	———	———	10^{-1} or 0.1	±10%	±1 pF	3 VDC
GOLD	—	10^{-1} or 0.1	±5%	———	———	———	———
SILVER	—	10^{-2} or 0.01	±10%	———	———	———	———
NONE	—	———	±20%	———	±10%	±1 pF	———

(1861-20A) 2662-48

Figure 9-1. Color codes for resistors and capacitors.

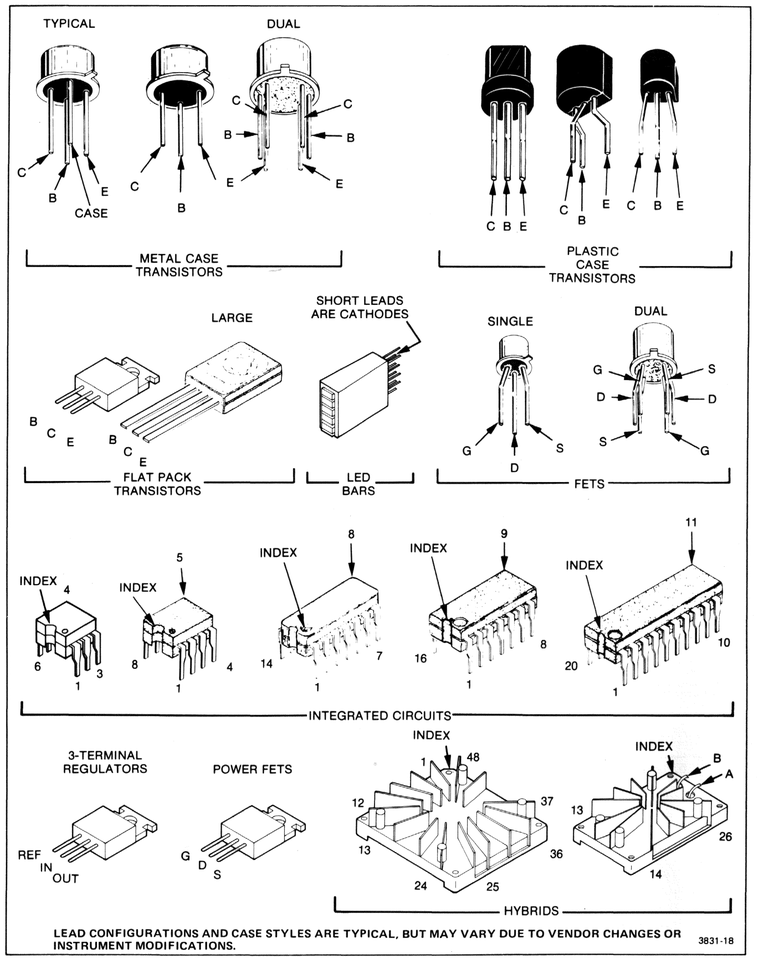


Figure 9-2. Semiconductor lead configurations.

LOCATING COMPONENTS EXAMPLE FIG. 9-3

2445 Service

To identify any component mounted on a circuit board and to locate that component in the appropriate schematic diagram

1. Locate the Circuit Board Illustration

a. In the instrument identify the Assembly Number of the circuit board in question. The Assembly Number is usually printed on the upper left corner of the circuit board on the component side.

b. In the manual locate and pull out tabbed page whose title corresponds with the Assembly Number of the circuit board. Circuit board assembly numbers and board nomenclature are printed on the back side of the tabs (facing the rear of the manual).

2. Determine the Circuit Number

a. Compare the circuit board with its illustration and locate the desired component by area and shape on the illustration.

b. Scan the table adjacent to the Circuit Board Illustration and find the Circuit Number of the desired component.

c. Determine the Schematic Diagram Number in which the component is located.

3. Locate the Component on the Schematic Diagram

a. Locate and pull out tabbed page whose number and title correspond with the Schematic Diagram Number just determined in the table. Schematic diagram nomenclature and numbers are printed on the front side of the tabs (facing the front of the manual).

b. Scan the Component Location Table adjacent to the schematic diagram and find the Circuit Number of the desired component.

c. Under the SCHEM LOCATION column, read the grid coordinates for the desired component.

d. Using the Circuit Number and grid coordinates, locate the component on the schematic diagram.

4. Determine the Circuit Board Illustration and Component Location

a. From the schematic diagram, determine the Assembly Number of the circuit board on which the component is mounted. This information is boxed and located in a corner of the heavy line that distinguishes the board outline.

b. Scan the Component Location Table for the Assembly Number just determined and find the Circuit Number of the desired component.

c. Under the BOARD LOCATION column, read the grid coordinates for the desired component.

5. Locate the Component on the Circuit Board

a. In the manual, locate and pull out the tabbed page whose title and Assembly Number correspond with the desired circuit board. This information is on the back side of the tabs.

b. Using the Circuit Number and grid coordinates, locate the component on the Circuit Board Illustration.

c. In the circuit board location illustration, determine the location of the circuit board in the instrument.

d. Find the circuit board in the instrument and compare it with its illustration in the manual to locate the desired component on the board.

A6 CRT BOARD

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 10

C602	C632	Q668	R625
C603	C641		R626
C609	C643	R604	R627
C671	C651	R605	R630
C615		R608	R632
C616	Q606	R609	
C617	Q610	R610	
C618	Q615	R614	
C619	Q645	R616	
C624	Q656	R623	
C626	Q665	R624	

COMPONENTS LOCATED ON SCHEMATIC DIAGRAM 11

C670	Q670	R677	
C671	Q672	R679	
C673	Q673	R680	
C680			
C681	R671	U617	
P603	R673	U618	
P607	R674	U619	
Q669	R675		

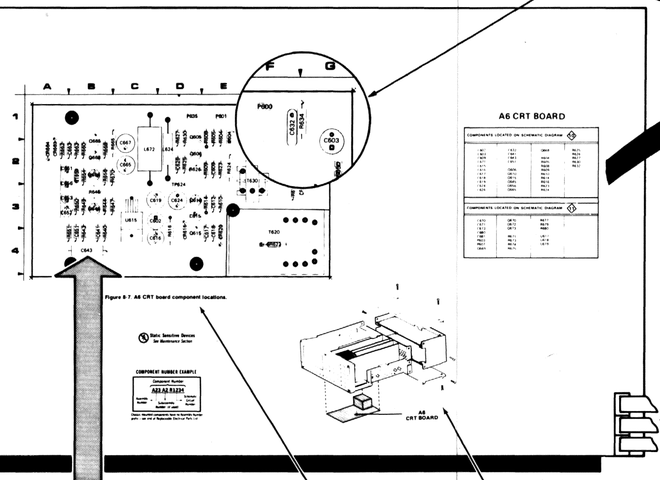
CRT CIRCUIT DIAGRAM 10

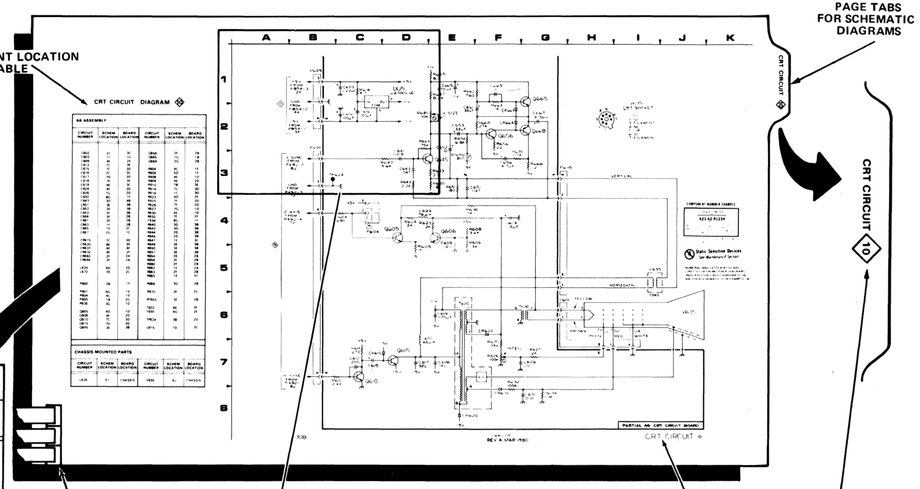
A6 ASSEMBLY

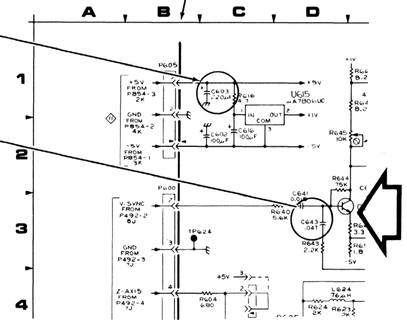
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C602	2C	3C	Q656	2F	2B
C603	1C	1G	Q665	1G	1B
C609	4E	2G	Q668	2G	2B
C612	7C	3E			
C615	7C	3D	R604	4C	1E
C616	2C	3C	R605	5D	1E
C617	7D	3D	R608	4E	1D
C618	7E	3E	R609	4E	2D
C619	6E	3C	R610	7B	3E
C624	4F	3D	R614	7C	3D
C626	7G	2D	R616	1C	3D
C632	8G	1E	R623	4D	2E
C643	3D	4B	R625	7F	2D
C651	3E	3B	R626	7F	2D
			R627	7G	1D
			R630	4F	1D
Q606	4E	2D			
Q610	7C	3D	TP624	3B	2D
Q615	7D	3D	U615	1D	3C
Q645	3E	3B			

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L635	51	CHASSIS	V635	6J	CHASSIS







To identify any component in a schematic diagram and to locate that component on its respective circuit board.

Figure 9-3. Locating components on schematic diagrams and circuit board illustrations.

3516-81

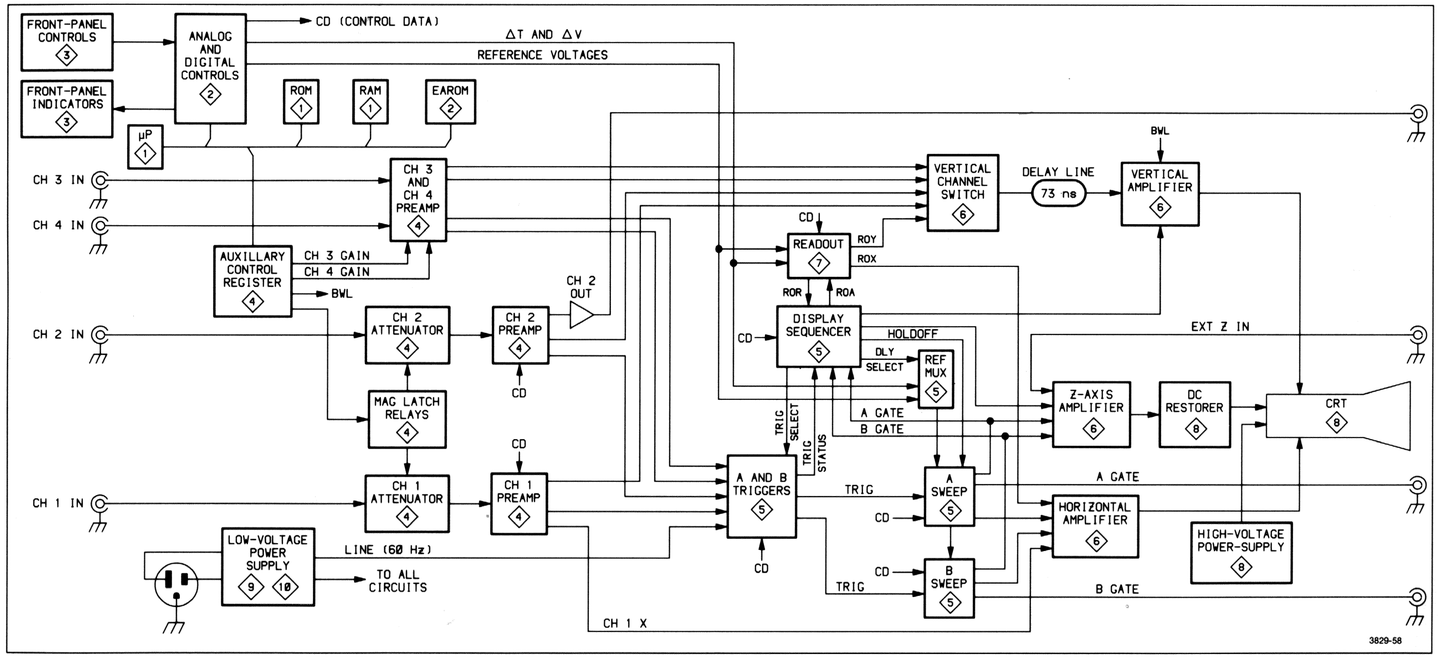


Figure 9-4. 2445 block diagram.

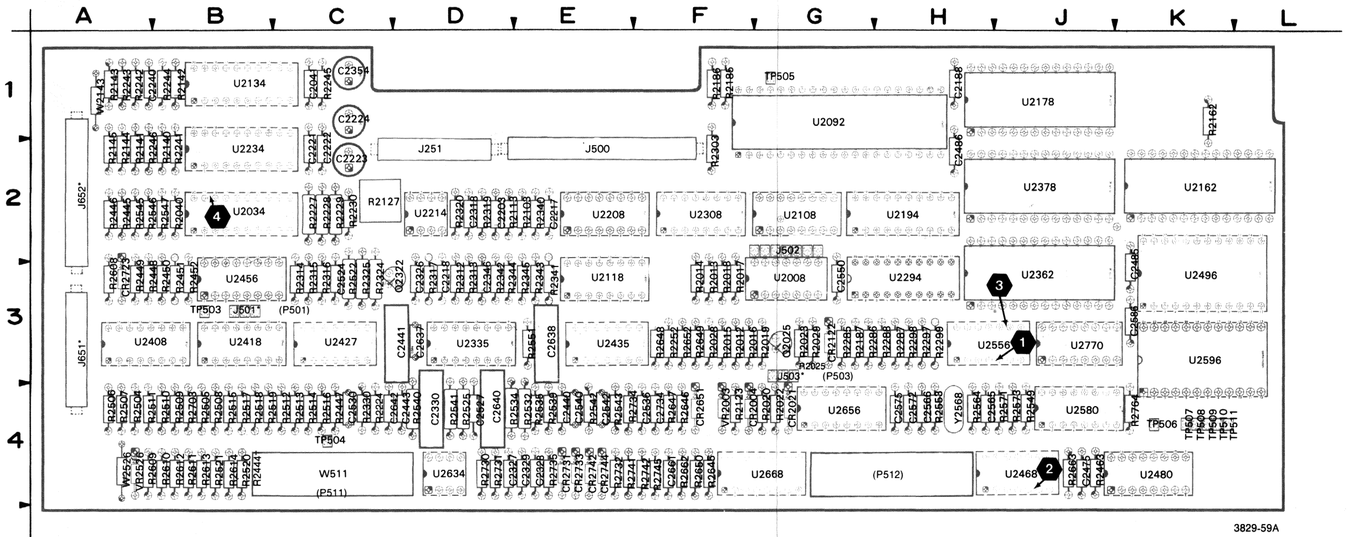
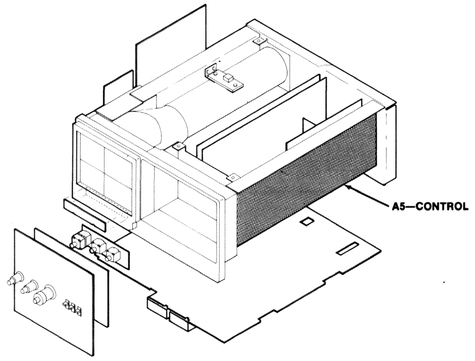
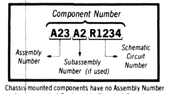


Figure 9-5. A5—Control board.



Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

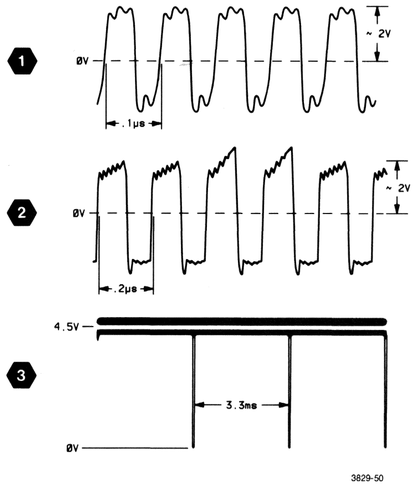
* LABELED ON SOME BOARDS AS "P" VICE "J".

( ) COMPONENTS WITHIN PARENTHESES MAY NOT BE LOCATED PRECISELY AS SHOWN BUT ARE NEAR THEIR INDICATED POSITION.

† INDICATES COMPONENTS THAT WERE MANUALLY ADDED TO THE BOARD AS A RESULT OF MODIFICATION.

TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the accompanying schematic diagram and board dolly. The waveforms are representative of signals that may be expected at the associated points whenever the instrument is running.



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A5—CONTROL BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C2041	12	P503	1	R2317	2	R2614	2	U2362	1
C2188	12	P511	2	R2319	2	R2645	1	U2362	12
C2203	1	P511	2	R2320	2	R2646	1	U2378	1
C2217	12	P511	2	R2324	2	R2647	1	U2378	12
C2218	12	P511	12	R2325	2	R2648	1	U2408	2
C2221	12	P512	1	R2330	2	R2649	1	U2408	12
C2222	2	P512	2	R2340	2	R2650	1	U2418	2
C2223	12	P512	2	R2341	2	R2652	1	U2418	12
C2224	2	P512	2	R2342	2	R2662	1	U2427	2
C2240	12	P512	12	R2343	2	R2663	1	U2427	2
C2318	2	Q2025	2	R2344	2	R2703	2	U2427	2
C2326	2	Q2322	2	R2345	2	R2730	2	U2427	2
C2327	2	R2012	2	R2444	2	R2731	2	U2427	12
C2328	12	R2013	2	R2445	2	R2732	2	U2435	1
C2329	2	R2014	2	R2446	2	R2734	2	U2435	2
C2330	2	R2015	2	R2447	2	R2735	2	U2435	2
C2346	12	R2016	2	R2448	2	R2741	2	U2435	2
C2354	12	R2017	2	R2449	2	R2742	2	U2435	12
C2440	12	R2018	2	R2450	2	R2745	2	U2456	2
C2441	2	R2019	2	R2451	2	R2764	1	U2456	12
C2443	2	R2020	2	R2452	2	TP503	2	U2468	1
C2475	12	R2022	2	R2463	1	TP504	2	U2468	1
C2485	12	R2023	2	R2504	2	TP505	1	U2468	12
C2486	1	R2025	2	R2505	2	TP506	1	U2480	1
C2524	2	R2028	2	R2506	2	TP507	1	U2480	12
C2527	12	R2029	2	R2507	2	TP508	12	U2496	1
C2530	2	R2040	2	R2508	2	TP509	1	U2496	12
C2536	2	R2103	2	R2509	2	TP510	1	U2556	1
C2540	2	R2113	2	R2510	2	TP511	1	U2556	1
C2542	2	R2123	2	R2511	2	U2008	2	U2556	1
C2550	1	R2127	2	R2512	2	U2008	2	U2556	1
C2565	1	R2140	2	R2513	2	U2034	2	U2556	1
C2566	1	R2141	2	R2514	2	U2034	12	U2556	1
C2572	1	R2142	2	R2515	2	U2092	1	U2556	12
C2575	12	R2143	2	R2516	2	U2092	12	U2580	1
C2586	12	R2144	2	R2517	2	U2108	2	U2580	12
C2637	12	R2145	2	R2518	2	U2108	12	U2596	1
C2638	2	R2162	1	R2519	2	U2118	1	U2596	12
C2640	2	R2185	1	R2520	2	U2118	2	U2634	2
C2642	12	R2186	1	R2521	2	U2118	2	U2634	2
C2661	1	R2187	1	R2522	2	U2118	2	U2634	12
C2734	12	R2224	2	R2525	2	U2118	2	U2656	1
CR2004	2	R2227	2	R2532	2	U2118	2	U2656	1
CR2021	2	R2228	2	R2534	2	U2118	2	U2656	1
CR2122	2	R2229	2	R2535	2	U2118	2	U2656	1
CR2651	1	R2230	2	R2539	2	U2134	2	U2656	12
CR2723	2	R2241	2	R2540	2	U2134	12	U2668	1
CR2731	2	R2242	2	R2541	2	U2162	1	U2668	12
CR2733	2	R2243	2	R2542	2	U2162	12	U2770	1
CR2742	2	R2244	2	R2543	2	U2178	1	U2770	12
CR2744	2	R2245	2	R2545	2	U2178	12	VR2003	2
J251	1	R2246	2	R2546	2	U2194	1	VR2526	2
J251	12	R2252	1	R2547	2	U2194	1	W511	2
J500	1	R2285	1	R2549	1	U2208	1	W511	2
J500	1	R2286	1	R2551	1	U2208	2	W511	2
J500	1	R2287	1	R2553	1	U2214	2	W511	12
J501	2	R2288	1	R2564	1	U2214	12	W512	1
J502	2	R2297	1	R2571	1	U2234	2	W512	2
J503	1	R2298	1	R2573	1	U2234	12	W512	2
J651	2	R2299	1	R2608	12	U2294	1	W512	2
J651	2	R2303	2	R2609	2	U2294	1	W512	12
J651	2	R2312	2	R2610	2	U2308	2	W2143	12
J652	2	R2313	2	R2611	2	U2308	12	W2526	12
J652	2	R2314	2	R2612	2	U2335	2	Y2568	1
P501	2	R2315	2	R2613	2	U2335	12		
		R2316	2						

PROCESSOR AND DIGITAL CONTROL DIAGRAM ①

ASSEMBLY A5

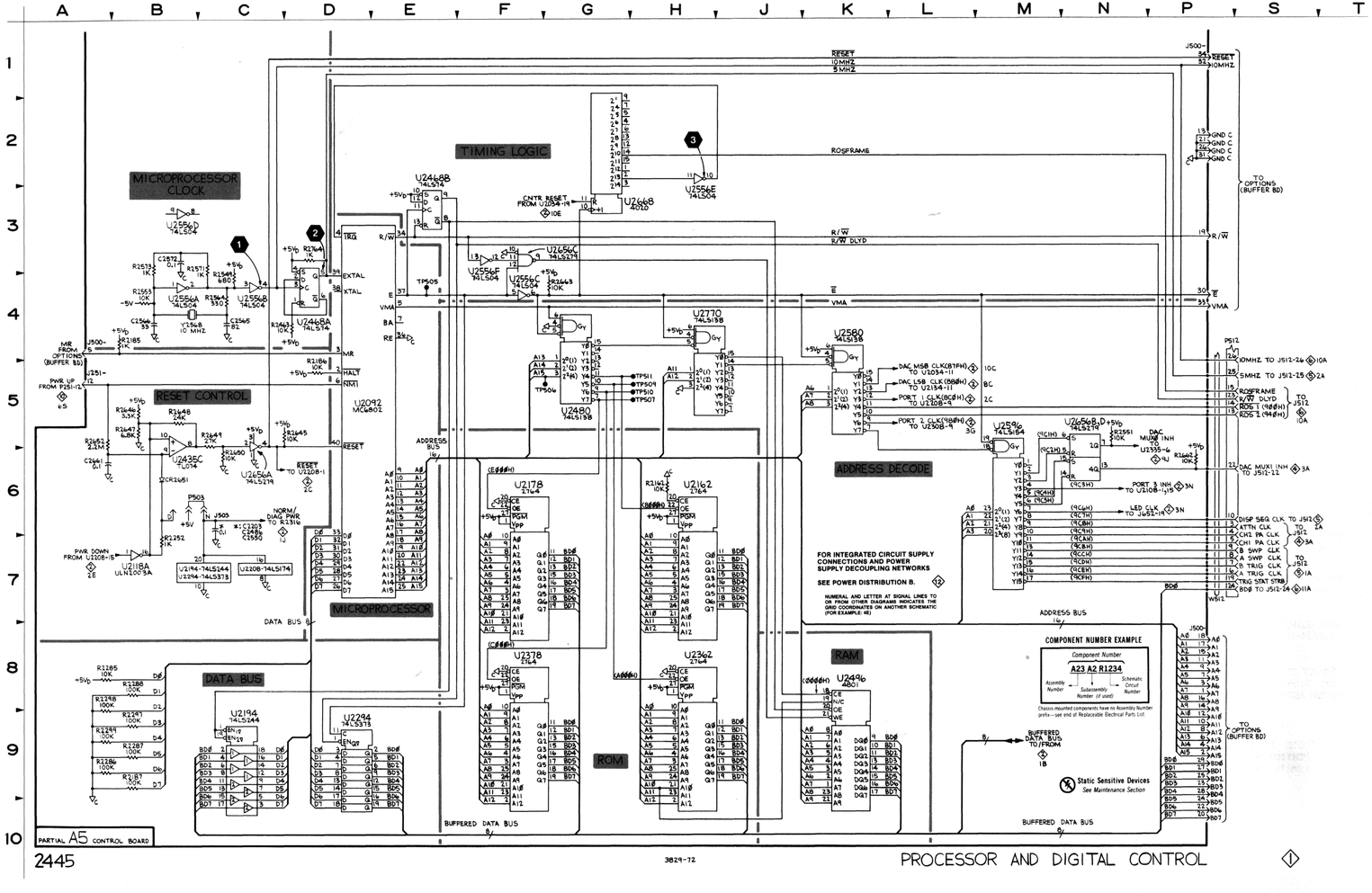
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2203	6C	2D	R2299	9A	3H	U2194	7B	2H
C2486	6C	2H	R2463	4C	4J	U2194	9C	2H
C2550	6C	3G	R2549	4C	4J	U2208	7C	2E
C2565	4C	4H	R2551	5N	3E	U2294	7B	3H
C2566	4B	4H	R2553	4B	4H	U2294	9D	3H
C2572	3B	4H	R2564	4C	4H	U2362	8H	3J
C2661	6A	4F	R2571	3B	4J	U2378	8F	2J
			R2573	3B	4J	U2435C	6B	3E
CR2651	6B	4F	R2645	5D	4F	U2468A	4D	4J
			R2646	5B	4F	U2468B	2E	4J
J251	5A	2D	R2647	5B	4F	U2480	5G	4K
J500	1P	2E	R2648	5B	3F	U2496	8K	3K
J500	4A	2E	R2649	5C	3F	U2556A	4B	3J
J500	8P	2E	R2650	6C	4F	U2556B	4C	3J
J503	6B	3G	R2652	5A	3F	U2556C	4F	3J
			R2662	6P	4F	U2556D	3B	3J
P503	6B	3G	R2663	4G	4J	U2556E	3H	3J
P512	4P	4H	R2764	3D	4K	U2556F	3F	3J
						U2580	4K	4J
R2162	6H	1K	TP505	4E	1G	U2596	5M	3K
R2185	4B	1F	TP506	5G	4K	U2656A	6C	4G
R2186	5D	1F	TP507	5H	4K	U2656B	5N	4G
R2187	9B	3G	TP509	5H	4K	U2656C	3G	4G
R2252	7B	3F	TP510	5H	4K	U2656D	5N	4G
R2285	8A	3G	TP511	5H	4K	U2668	3H	4G
R2286	9A	3H				U2770	4H	3J
R2287	9B	3H	U2092	5D	1G			
R2288	8B	3H	U2118A	7B	3E	W512	7P	4H
R2297	9B	3H	U2162	6H	2K			
R2298	8A	3H	U2178	6F	1J	Y2568	4B	4H

Partial A5 also shown on diagrams 2 and 12.

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

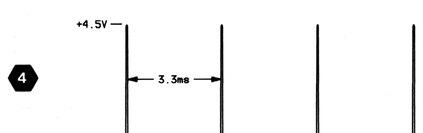
ATTN CLK . . . attenuator clock
A0 – A15 . . . address bits 0 – 15
A000H . . . address block A000 hex
BA . . . bus available
BD0 – BD7 . . . buffered data bits 0 – 7
C000H . . . address block C000 hex
DAC MUX0 INH . . . DAC multiplexer 0 inhibit
DAC MUX1 INH . . . DAC multiplexer 1 inhibit
D0 – D7 . . . data bits 0 – 7
E . . . enable
$\overline{E}$ . . . enable
EXTAL . . . external crystal
E000H . . . address block E000 hex
$\overline{GND}$ C . . . virtual ground "C"
$\overline{IRQ}$ . . . interrupt request
LED CLK . . . LED clock
MR . . . memory ready
NMI . . . non-maskable interrupt
PORT 3 INH . . . port 3 inhibit
RE . . . RAM enable
ROSFRAME . . . readout subframe
ROS1 (900H) . . . readout strobe 1 (address 0900 hex)
ROS2 (940H) . . . readout strobe 2 (address 0940 hex)
R/$\overline{W}$ . . . read/write
R/$\overline{W}$ DLY'D . . . read/write delayed
TRIG STAT STRB . . . trigger status strobe
VMA . . . valid memory address
XTAL . . . crystal
0000H . . . address block 0000 hex
8000H . . . address block 8000 hex
9C1H – 9CFH . . . addresses 09C1 hex – 09CF hex



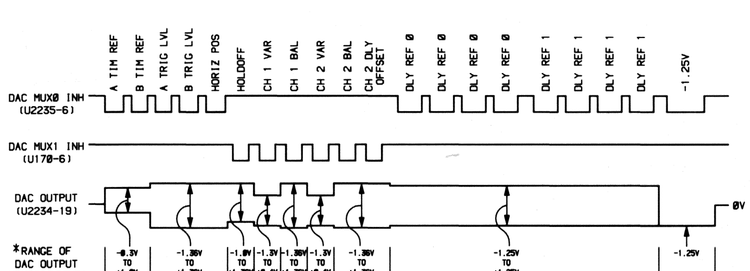
TEST WAVEFORM SETUP INFORMATION

The waveform below was obtained at the test point indicated on the accompanying schematic diagram. The waveform is representative of the signal that may be expected at the test point whenever the instrument is running.

Also shown below is an illustration depicting timing of the D to A Converter and the output ranges that may be expected as the DAC sets up the various analog reference voltages. Test point locations and setup information are called out on the illustration.



3829-51



*NOTE: AS ANY GIVEN CONTROL IS EXERCISED, THE CORRESPONDING PORTION OF THE DAC OUTPUT WAVEFORM SHOULD VARY WITHIN THE LIMITS INDICATED.

3831-19

ANALOG CONTROL DIAGRAM 2

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2222	8H	2C	R2016	2L	3G	R2444	5F	4B	R2732	9N	4E
C2224	8H	1C	R2017	2K	3F	R2445	5G	2A	R2734	9N	4F
C2318	4J	2D	R2018	3K	3F	R2446	5F	2A	R2735	9M	4E
C2326	5P	3D	R2019	2L	3G	R2447	6F	4C	R2741	9M	4F
C2327	8M	4E	R2020	3K	4G	R2448	6G	3B	R2742	10M	4F
C2329	8L	4E	R2022	2K	4G	R2449	6G	3A	R2745	10L	4F
C2330	6K	4D	R2023	2N	3G	R2450	6H	3B			
C2441	6L	3D	R2025*	2N	3G	R2451	6H	3B	TP503	5P	3B
C2443	7N	4D	R2028	3L	3F	R2452	6H	3B	TP504	6P	4C
C2524	5N	3C	R2029	2N	3G	R2504	3E	4A			
C2530	6L	4C	R2040	10C	2B	R2505	2D	4B	U2008	2N	3G
C2536	8N	4F	R2103	4K	2E	R2506	3D	4A	U2008	3N	3G
C2540	9L	4E	R2113	2P	2E	R2507	3E	4A	U2034	9D	2B
C2542	9L	4E	R2123	2N	4F	R2508	3E	4B	U2108	2P	2G
C2638	9L	3E	R2127	8H	2C	R2509	3D	4B	U2118B	2K	3E
C2640	9K	4D	R2140	8G	2B	R2510	3E	4B	U2118C	3K	3E
			R2141	8D	2A	R2511	3D	4A	U2118D	2K	3E
CR2004	1K	4G	R2142	8D	1B	R2512	5E	4C	U2118E	2K	3E
CR2021	3K	4G	R2143	8G	1A	R2513	4D	4C	U2118F	3K	3E
CR2122	2P	3G	R2144	8E	2A	R2514	4D	4C	U2118G	2N	3E
CR2723	5P	3A	R2145	8E	2A	R2515	5D	4B	U2118	1L	3E
CR2731	9M	4E	R2224	6G	4C	R2516	5E	4C	U2134	8D	1B
CR2733	9N	4E	R2227	8H	2C	R2517	5E	4B	U2208	2D	2E
CR2742	9M	4E	R2228	7H	2C	R2518	5E	4B	U2214	5K	2D
CR2744	9L	4E	R2229	7H	2C	R2519	5D	4B	U2234	7J	2B
			R2230	7G	2C	R2520	5D	4B	U2308	3H	2F
J501	7H	3B	R2241	8E	2B	R2521	5D	4B	U2335	8K	3D
J502	2M	2G	R2242	8E	1A	R2522	5N	3C	U2408	4F	3A
J651	2B	3A	R2243	8F	1A	R2525	5N	4D	U2418	5F	3B
J651	5P	3A	R2244	8F	1B	R2532	7N	4E	U2427A	6M	3C
J651	8B	3A	R2245	8F	1C	R2534	7N	4E	U2427B	6L	3C
J652	3P	2A	R2246	8G	2A	R2535	8N	4E	U2427C	7N	3C
J652	5B	2A	R2303	4G	2F	R2539	8N	4E	U2427D	5N	3C
			R2312	2F	3D	R2540	7L	4D	U2435A	9M	3E
P501	7G	3B	R2313	4F	3D	R2541	7L	4D	U2435B	9L	3E
P511	4A	4C	R2314	2J	3C	R2542	9L	4E	U2435D	8N	3E
P511	6S	4C	R2315	2J	3C	R2543	9L	4E	U2456	5J	3B
P511	9A	4C	R2316	2J	3C	R2545	5G	2A	U2634A	7M	4D
P512	10S	4H	R2317	4J	3D	R2546	5H	2A	U2634B	8L	4D
P512	1A	4H	R2319	4J	2D	R2547	5H	2B			
P512	4S	4H	R2320	5J	2D	R2609	3D	4B	VR2003	1K	4F
			R2324	6K	3C	R2610	3D	4B	VR2526	6N	4A
Q2025	2N	3G	R2325	5J	3C	R2611	3D	4B			
Q2322	5P	3D	R2330	6L	4C	R2612	3E	4B	W511	10B	4C
			R2340	10N	2E	R2613	5D	4B	W511	5B	4C
R2012	2L	3F	R2341	10P	3E	R2614	5E	4B	W511	9P	4C
R2013	2K	3F	R2342	10N	3D	R2703	5P	4B	W512	10P	4H
R2014	3K	3F	R2343	10P	3E	R2730	8M	4D	W512	1B	4H
R2015	2L	3F	R2344	10N	3E	R2731	8L	4D	W512	5P	4H
			R2345	10P	3E						

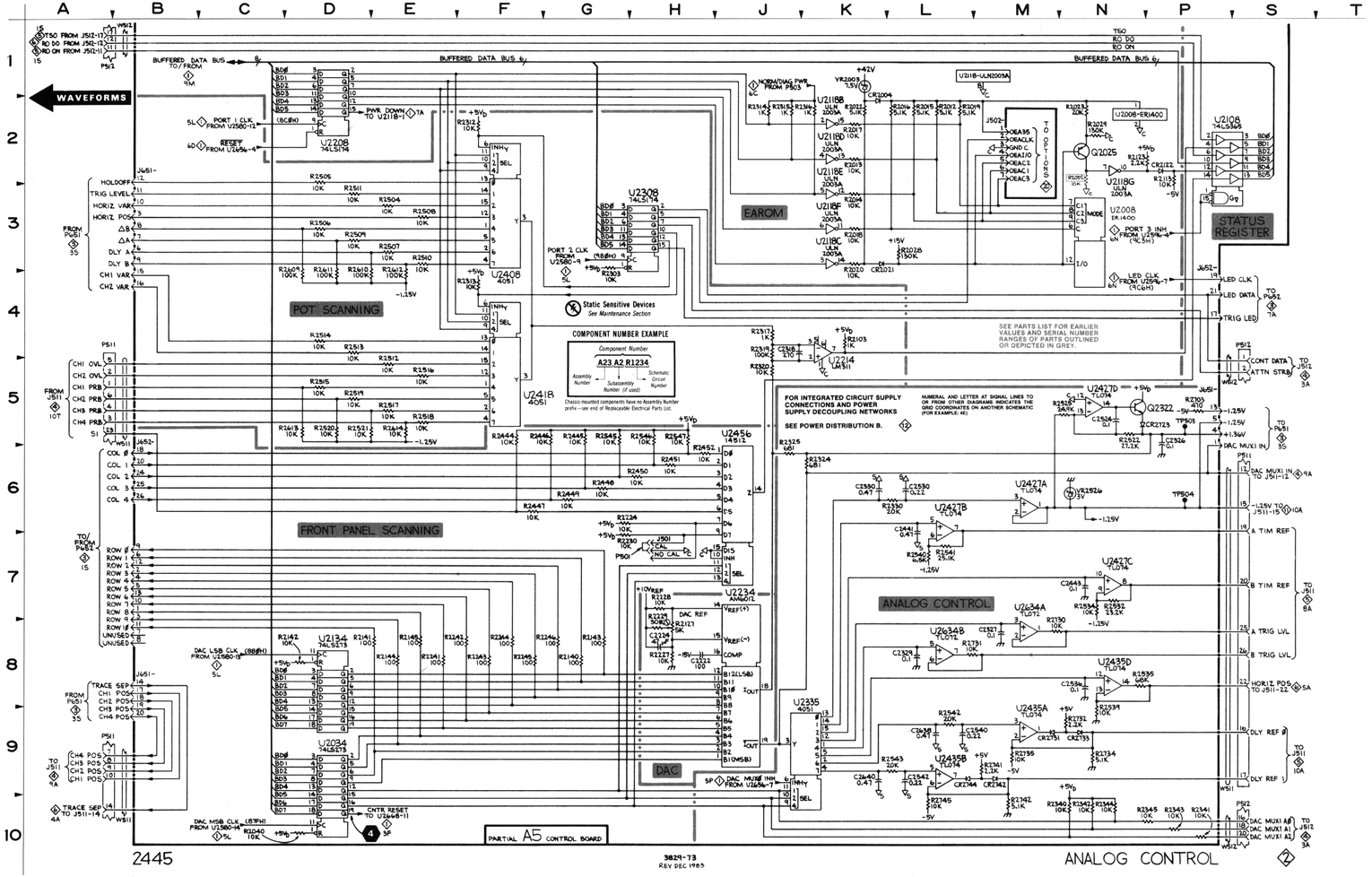
Partial A5 also shown on diagrams 1 and 12.

***See Parts List for serial number ranges.**

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

A TIM REF . . . A timing reference
ATTN STRB . . . attenuator strobe
BD0 – BD7 . . . buffered data bits 0 – 7
B TIM REF . . . B timing reference
CH1 OVL . . . channel 1 overload
CH2 OVL . . . channel 2 overload
CH1 PRB . . . channel 1 probe
CH2 PRB . . . channel 2 probe
CH3 PRB . . . channel 3 probe
CH4 PRB . . . channel 4 probe
CONT DATA . . . control data
DAC MUXO INH . . . DAC multiplexer 0 inhibit
DAC MUX1 A0 . . . DAC multiplexer 1, address bit 0
DAC MUX1 A1 . . . DAC multiplexer 1, address bit 1
DAC MUX1 A2 . . . DAC multiplexer 1, address bit 2
DAC MUX1 IN . . . DAC multiplexer input
GND C . . . virtual ground "C"
OEA35 . . . option EAROM +35 volt
OEACLK . . . option EAROM clock
OEAI/O . . . option EAROM input/output
OEAC1 . . . option EAROM mode code, bit 1
OEAC2 . . . option EAROM mode code, bit 2
OEAC3 . . . option EAROM mode code, bit 3
PORT 3 INH (9C3H) . . . port 3 inhibit
RO DO . . . readout data out
RO ON . . . readout on
SI . . . scope identification
TSO . . . trigger status output



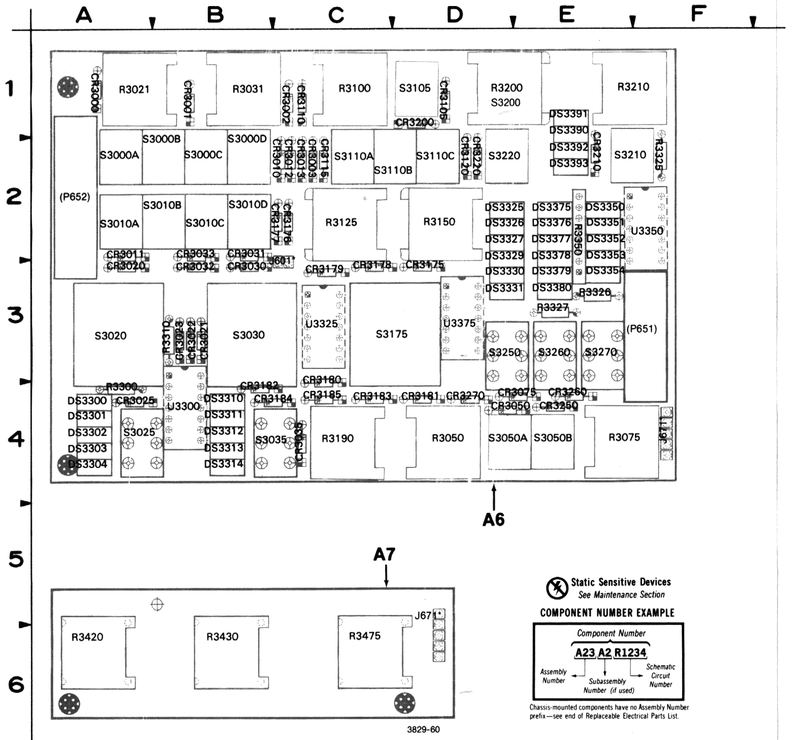


Figure 9-6. A6—Front Panel and A7—Front Panel Variable boards.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
- A23 — Assembly Number
- A2 — Subassembly Number (if used)
- R1234 — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

* LABELED ON SOME BOARDS AS "P" VICE "J".

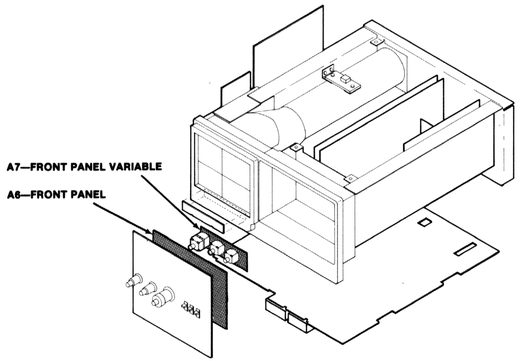
( ) COMPONENTS WITHIN PARENTHESES MAY NOT BE LOCATED PRECISELY AS SHOWN BUT ARE NEAR THEIR INDICATED POSITION.

ALL COMPONENTS MOUNTED ON A7—FRONT PANEL VARIABLE CIRCUIT BOARD ARE SHOWN ON SCHEMATIC DIAGRAM 3

A6—FRONT PANEL & FRONT PANEL CIRCUIT VIEW FIG. 9-6, -7

A6—FRONT PANEL BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
CR3000	3	CR3200	3	DS3392	3	S3010	3
CR3001	3	CR3210	3	DS3393	3	S3010	3
CR3002	3	CR3220	3	J601	3	S3010	3
CR3003	3	CR3250	3	J671	3	S3010	3
CR3010	3	CR3260	3	P651	3	S3020	3
CR3011	3	CR3270	3	P651	12	S3025	3
CR3012	3	DS3300	3	P652	3	S3030	3
CR3013	3	DS3301	3	P652	3	S3035	3
CR3020	3	DS3302	3	P652	12	S3050	3
CR3021	3	DS3303	3	R3021	3	S3050	3
CR3022	3	DS3304	3	R3031	3	S3105	3
CR3023	3	DS3310	3	R3050	3	S3110	3
CR3025	3	DS3311	3	R3075	3	S3110	3
CR3030	3	DS3312	3	R3100	3	S3110	3
CR3031	3	DS3313	3	R3125	3	S3175	3
CR3032	3	DS3314	3	R3150	3	S3175	3
CR3033	3	DS3325	3	R3190	3	S3200	3
CR3035	3	DS3326	3	R3200	3	S3210	3
CR3050	3	DS3327	3	R3210	3	S3220	3
CR3075	3	DS3329	3	R3300	3	S3250	3
CR3105	3	DS3330	3	R3310	3	S3260	3
CR3110	3	DS3331	3	R3325	3	S3270	3
CR3115	3	DS3350	3	R3326	3	U3300	3
CR3120	3	DS3351	3	R3327	3	U3300	12
CR3175	3	DS3352	3	R3350	3	U3325	3
CR3176	3	DS3353	3	R3350	3	U3325	12
CR3177	3	DS3354	3	R3350	3	U3350	3
CR3178	3	DS3375	3	R3350	3	U3350	12
CR3179	3	DS3376	3	R3350	3	U3375	3
CR3180	3	DS3377	3	R3350	3	U3375	12
CR3181	3	DS3378	3	R3350	3	W651	3
CR3182	3	DS3379	3	S3000	3	W651	12
CR3183	3	DS3380	3	S3000	3	W652	3
CR3184	3	DS3390	3	S3000	3	W652	3
CR3185	3	DS3391	3	S3000	3	W652	12



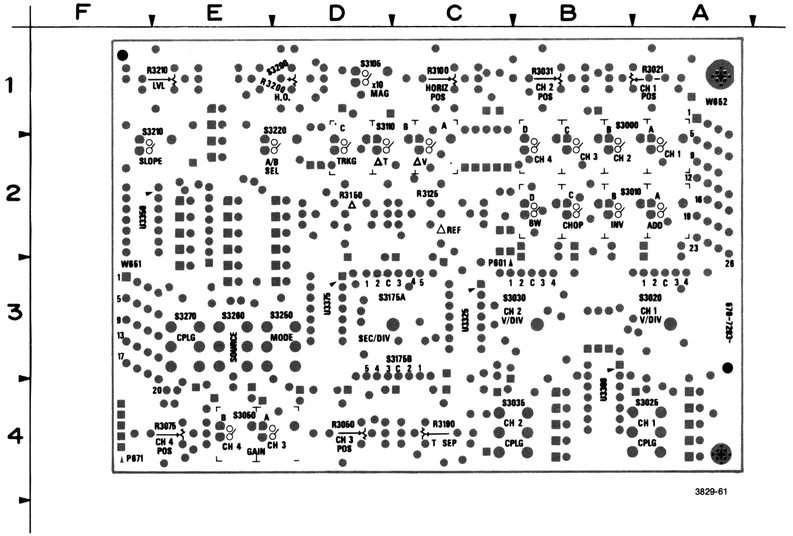


Figure 9-7. Circuit view of A6—Front Panel.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
- A23 — Assembly Number
- A2 — Subassembly Number (if used)
- R1234 — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

FRONT PANEL CONTROLS DIAGRAM 3

ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
CR03000	2J	1A	CR3200	3J	1D	DS3391	10P	1E	S3000B	3K	2B
CR3001	2K	1B	CR3210	4N	2E	DS3392	8L	2E	S3000C	3M	2B
CR3002	2M	1C	CR3220	5L	2D	DS3393	7F	2E	S3000D	3N	2B
CR3003	2N	2C	CR3250	5K	4E				S3010A	3L	2A
CR3010	2L	2C	CR3260	6J	4E	J601	5D	3C	S3010B	3D	2B
CR3011	3D	2A	CR3270	2B	4D	J671	7P	4F	S3010C	3K	2B
CR3012	3K	2C							S3010D	3L	2B
CR3013	3L	2C	DS3300	6B	4A	P651	3S	3F	S3020	3D	3A
CR3020	3B	3A	DS3301	6C	4A	P652	1S	2A	S3025	1B	4A
CR3021	3B	3B	DS3302	6C	4A	P652	7A	2A	S3030	4D	3B
CR3022	3B	3B	DS3303	7C	4A				S3035	2C	4B
CR3023	3C	3B	DS3304	7D	4A	R3021	3P	1A	S3050A	2B	4D
CR3025	2C	4A	DS3310	7D	4B	R3031	4P	1B	S3050B	2A	4E
CR3030	5B	3B	DS3311	7E	4B	R3050	4P	4D	S3105	4J	1D
CR3031	5B	2B	DS3312	7E	4B	R3075	5P	4E	S3110A	4M	2C
CR3032	5B	3B	DS3313	7E	4B	R3100	5P	1C	S3110B	4L	2C
CR3033	5C	2B	DS3314	7F	4B	R3125	5P	2C	S3110C	4K	2D
CR3035	2C	4C	DS3325	8H	2D	R3150	6P	2D	S3175A	3H	3C
CR3050	2C	4D	DS3326	8H	2D	R3190	3P	4C	S3175B	5H	3C
CR3075	2B	4D	DS3327	8G	2D	R3200	6P	1D	S3200	3J	1D
CR3105	4J	1D	DS3329	7G	2D	R3210	6P	1E	S3210	4N	2E
CR3110	4M	1C	DS3330	8J	3D	R3300	6D	4A	S3220	5L	2D
CR3115	4L	2C	DS3331	8J	3D	R3310	7F	3B	S3250	5K	3D
CR3120	4K	2D	DS3350	8J	2E	R3325	8L	2F	S3260	5J	3E
CR3175	2F	3D	DS3351	8K	2E	R3326	9N	3E	S3270	1A	3E
CR3176	2F	2C	DS3352	8K	2E	R3327	9P	3E			
CR3177	2F	2C	DS3353	8L	2E	R3350A	9N	2E	U3300	8B	4B
CR3178	2G	3C	DS3354	8L	3E	R3350B	9M	2E	U3325	9E	3C
CR3179	2G	3C	DS3375	9M	2E	R3350C	8M	2E	U3350	9H	2F
CR3180	5F	3C	DS3376	9M	2E	R3350D	7J	2E	U3375	10L	3D
CR3181	6F	4D	DS3377	9N	2E	R3350E	10P	2E			
CR3182	6F	4B	DS3378	9N	2E	R3350F	7G	2E	W651	8S	3F
CR3183	6G	4C	DS3379	9N	3E	R3350G	7M	2E	W652	10A	2A
CR3184	6G	4B	DS3380	9P	3E				W652	3S	2A
CR3185	5C	4C	DS3390	7G	1E	S3000A	3J	2A			

Partial A6 also shown on diagram 12.

ASSEMBLY A7

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J671	7N	5D	R3420	7M	6A	R3475	8M	6C			
			R3430	7M	6B						

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P601	5D	CHASSIS	S3185	5D	CHASSIS	W671	8N	CHASSIS			
P671	7N	CHASSIS									

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

CH1 VAR . . . channel 1 variable
CH2 VAR . . . channel 2 variable
DAC MUX1 IN . . . DAC multiplexer 1 input
HORIZ VAR . . . horizontal variable

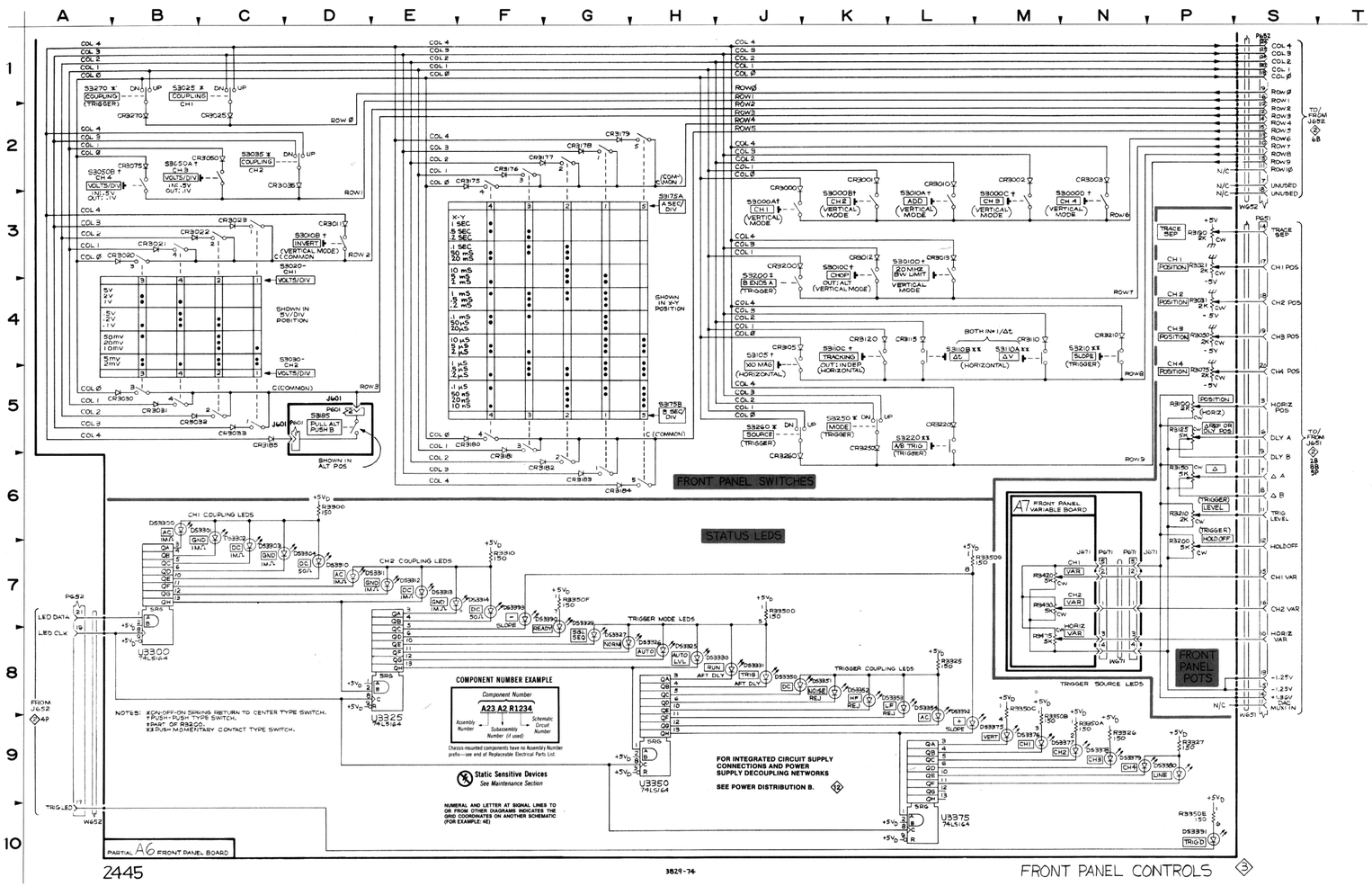
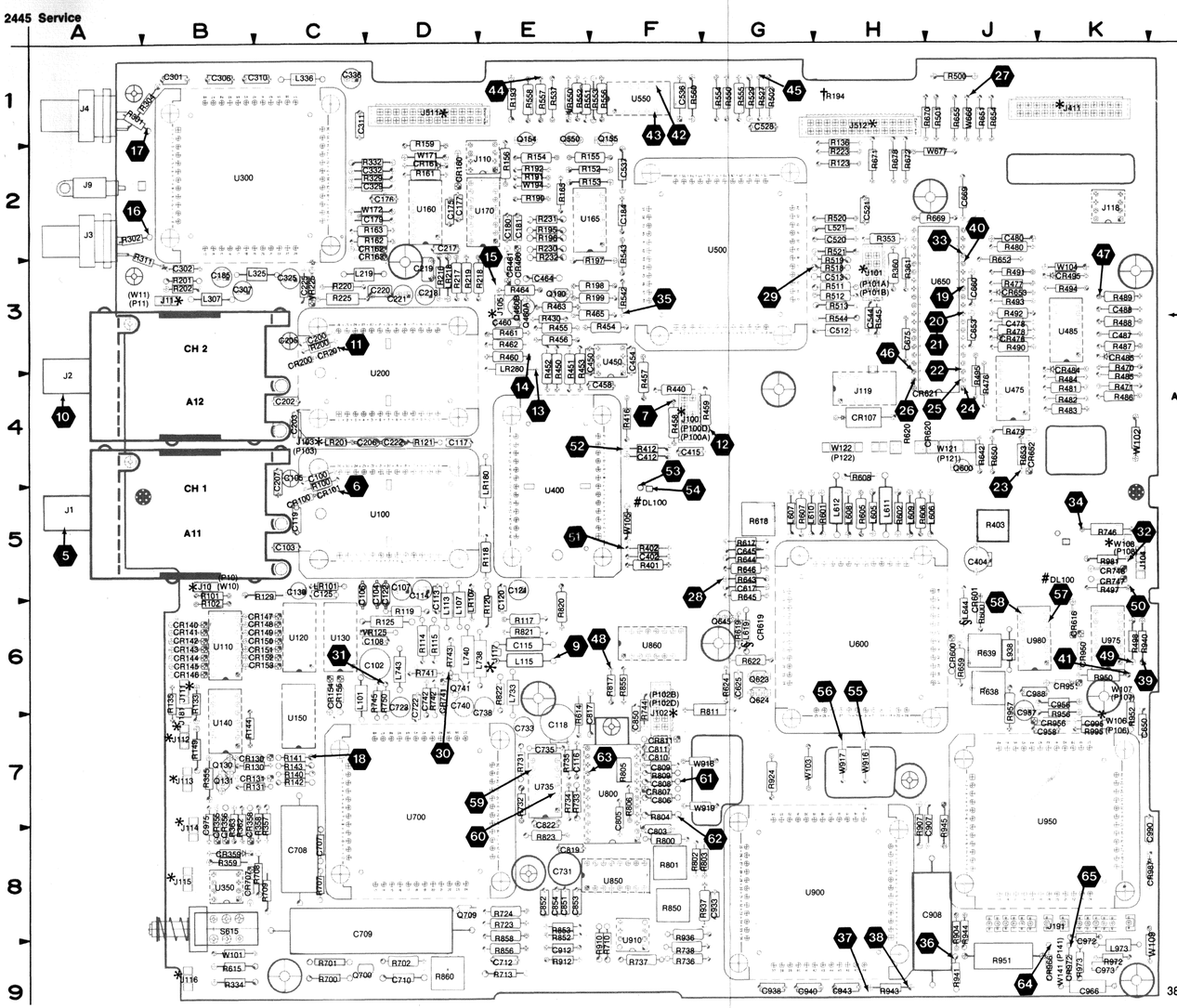
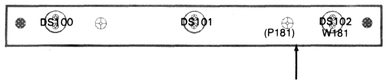
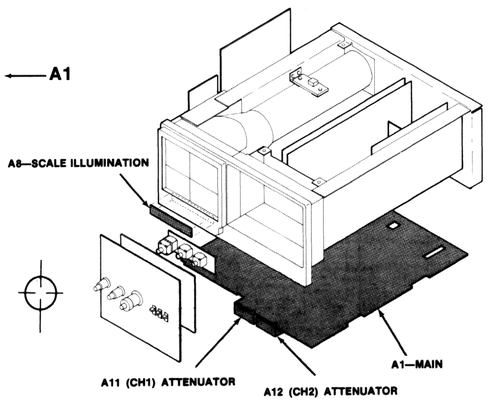


FIG. 9-8





ALL COMPONENTS MOUNTED ON A8—SCALE ILLUMINATION CIRCUIT BOARD ARE SHOWN ON SCHEMATIC DIAGRAM 4



( ) COMPONENTS WITHIN PARENTHESES MAY NOT BE LOCATED PRECISELY AS SHOWN BUT ARE NEAR THEIR INDICATED POSITION.

† INDICATES COMPONENTS THAT WERE MANUALLY ADDED TO THE BOARD AS A RESULT OF MODIFICATION.

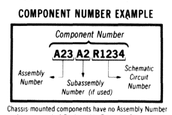
* LABELED ON SOME BOARDS AS "P" VICE "J".

COMPONENT ON BACK OF BOARD.

§ USED FOR FUTURE TV OPTION.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Figure 9-8. A1—Main and A8—Scale Illumination boards.

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A1—MAIN BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C100	4	C723	11	CR747	5	P100	4	R232	4
C102	11	C731	11	CR807	11	P100	4	R301	4
C103	4	C733	11	CR811	11	P101	5	R302	4
C104	4	C735	6	CR950	5	P101	5	R304	4
C105	4	C738	11	CR951	5	P102	5	R311	4
C106	11	C740	11	CR966	6	P102	5	R329	4
C107	11	C742	5	CR966	6	P103	4	R332	4
C108	11	C803	6	CR972	6	P106	6	R334	5
C113	11	C805	6	CR987	11	P107	5	R353	5
C114	11	C806	6	DL100	6	P108	5	R355	5
C115	4	C808	6	J9	5	P121	11	R357	5
C116	4	C809	6	J10	4	P121	11	R358	5
C117	4	C810	11	J11	4	P122	5	R359	5
C118	4	C811	11	J100	4	P122	11	R360	5
C119	11	C817	6	J100	4	P141	6	R361	5
C120	11	C819	11	J100	4	P141	6	R362	5
C121	11	C822	6	J101	5	Q130	4	R363	5
C122	4	C850	11	J101	5	Q131	4	R401	6
C125	11	C851	5	J102	5	Q154	5	R402	6
C130	4	C852	5	J102	5	Q155	5	R403	6
C175	4	C853	5	J102	5	Q190	4	R412	6
C176	4	C854	5	J103	4	Q460	4	R416	6
C177	4	C907	5	J104	5	Q460	4	R430	4
C179	4	C908	5	J104	5	Q550	5	R440	4
C180	5	C912	5	J105	4	Q600	6	R450	4
C181	5	C933	11	J110	4	Q623	6	R451	4
C184	4	C938	11	J111	4	Q624	6	R452	4
C185	4	C940	11	J112	8	Q645	5	R453	4
C200	4	C943	11	J113	5	Q700	11	R454	4
C202	4	C956	6	J114	8	Q709	5	R455	4
C203	4	C957	6	J115	8	Q741	5	R456	4
C205	4	C958	11	J116	5	R100	4	R457	4
C206	4	C966	11	J117	4	R101	4	R458	4
C207	11	C972	6	J118	5	R102	4	R459	4
C217	4	C973	11	J119	11	R114	4	R460	4
C218	11	C975	8	J181	4	R115	4	R461	4
C219	11	C988	11	J191	6	R117	4	R462	4
C220	11	C990	11	J191	11	R118	4	R463	4
C221	11	C995	6	J191	11	R119	4	R464	4
C222	4	CR100	4	J411	5	R120	11	R465	4
C225	11	CR101	4	J411	5	R121	4	R470	6
C301	4	CR107	11	J411	6	R123	4	R471	6
C302	4	CR130	4	J411	6	R125	11	R476	6
C308	5	CR131	4	J411	11	R129	4	R477	6
C307	11	CR140	4	J511	4	R130	4	R478	6
C310	4	CR141	4	J511	4	R131	4	R479	6
C311	4	CR142	4	J511	5	R133	4	R480	6
C325	11	CR143	4	J511	6	R135	4	R481	6
C329	4	CR144	4	J511	11	R136	4	R482	6
C332	4	CR145	4	J511	11	R140	4	R483	6
C336	11	CR146	4	J512	4	R141	4	R484	6
C402	6	CR147	4	J512	5	R142	4	R485	6
C404	6	CR148	4	J512	5	R143	4	R486	6
C412	6	CR149	4	J512	6	R144	4	R487	6
C415	11	CR150	4	J512	6	R149	4	R488	6
C450	4	CR151	4	J512	11	R152	5	R489	6
C454	4	CR152	4	L101	11	R153	5	R490	6
C458	11	CR153	4	L107	11	R154	5	R491	6
C460	4	CR154	4	L113	11	R155	5	R492	6
C464	4	CR155	4	L115	4	R156	5	R493	6
C478	6	CR160	4	L219	11	R159	4	R494	6
C480	11	CR161	4	L307	11	R161	4	R495	6
C487	6	CR162	4	L325	11	R162	4	R497	6
C488	6	CR163	4	L336	11	R163	4	R498	6
C512	5	CR200	4	L521	11	R165	5	R500	6
C513	5	CR201	4	L605	6	R190	4	R501	6
C520	5	CR355	5	L606	6	R191	4	R502	4
C521	11	CR356	5	L607	6	R192	4	R511	5
C528	5	CR358	5	L608	6	R193	4	R512	5
C536	5	CR359	5	L609	6	R194	4	R513	5
C537	5	CR460	4	L610	6	R195	4	R518	5
C544	5	CR461	4	L611	6	R196	4	R519	5
C617	6	CR476	6	L612	6	R197	4	R520	5
C625	6	CR484	6	L619	6	R198	4	R521	5
C645	5	CR485	6	L644	6	R199	4	R527	5
C650	5	CR495	6	L733	11	R200	4	R529	5
C653	5	CR600	6	L738	11	R201	4	R537	5
C660	5	CR601	6	L740	11	R202	4	R542	5
C669	5	CR616	6	L743	11	R216	4	R543	5
C675	11	CR619	6	L938	11	R217	4	R544	5
C707	5	CR620	6	L973	11	R218	4	R545	5
C708	5	CR621	6	LR101	11	R219	4	R550	5
C709	5	CR652	5	LR107	11	R220	11	R551	5
C710	11	CR653	5	LR180	4	R223	4	R552	5
C712	5	CR707	5	LR201	11	R225	11	R553	5
C722	11	CR741	5	LR218	11	R230	4	R554	5
		CR746	5	LR280	4	R231	4	R555	5

TABLE (CONT)

A1—MAIN BOARD (CONT)

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
R556	5	R907	5	U700	5
R557	5	R910	5	U700	11
R558	5	R912	5	U735	6
R560	5	R924	5	U735	6
R600	6	R936	5	U735	6
R601	6	R937	5	U735	6
R602	6	R940	5	U735	6
R605	6	R941	5	U800	6
R606	6	R943	5	U800	11
R607	6	R944	5	U850	5
R608	6	R945	5	U850	5
R614	6	R950	5	U850	6
R615	6	R951	11	U850	11
R617	6	R952	5	U860	5
R618	6	R956	6	U860	5
R619	6	R957	6	U860	6
R620	6	R972	6	U860	11
R622	6	R973	6	U900	5
R624	6	R981	5	U900	11
R638	6	R995	6	U910	5
R639	6	S615	6	U910	5
R642	6	U100	4	U910	11
R643	5	U100	11	U950	6
R644	5	U110	4	U950	11
R645	5	U110	11	U975	5
R646	5	U120	4	U975	5
R650	6	U120	11	U975	6
R651	5	U130	4	U975	6
R652	5	U130	4	U975	11
R653	5	U130	4	U980	5
R654	5	U130	4	U980	5
R655	5	U130	4	U980	6
R659	6	U130	4	U980	6
R669	5	U130	4	U980	11
R670	5	U130	11	VR125	11
R671	5	U140	4	VR225	11
R672	5	U140	11	VR550	5
R678	5	U150	4	W101	11
R700	11	U150	11	W102	11
R701	11	U160	4	W103	11
R702	11	U160	4	W104	11
R707	5	U160	4	W105	11
R708	5	U160	4	W106	6
R709	5	U160	11	W107	5
R710	5	U165	4	W108	5
R713	5	U165	5	W109	11
R723	5	U165	5	W121	11
R724	5	U165	5	W121	11
R731	6	U165	11	W122	5
R732	6	U170	4	W122	11
R733	6	U170	11	W141	6
R734	6	U200	4	W141	6
R735	6	U200	11	W171	4
R736	5	U300	4	W172	4
R737	5	U300	11	W194	4
R738	5	U350	5	W666	5
R741	5	U350	5	W677	5
R742	5	U350	11	W916	6
R743	5	U400	6	W917	6
R744	5	U400	11	W918	6
R745	5	U450	4	W919	6
R746	5	U450	4		
R750	5	U450	11		
R800	6	U475	6		
R801	6	U475	6		
R802	6	U475	6		
R803	6	U475	6		
R804	6	U475	6		
R805	6	U485	6		
R806	6	U485	6		
R809	6	U485	6		
R811	11	U485	6		
R817	6	U485	6		
R820	6	U500	5		
R821	6	U500	11		
R822	6	U550	5		
R823	6	U550	5		
R850	6	U550	5		
R852	5	U550	5		
R853	5	U550	5		
R855	6	U600	6		
R856	6	U600	11		
R858	6	U650	5		
R860	6	U650	11		
R904	5				

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

APO+ . . . auxiliary pickoff, noninverting
ATTN CLK . . . attenuator clock
ATTN STRB . . . attenuator strobe
BDCA . . . bypass delay comparator A
BDCB . . . bypass delay comparator B
BPO+ . . . second auxiliary pickoff, noninverting
BWL . . . bandwidth limit
$\overline{\text{BYP}}$ . . . bypass
$\overline{\text{CC}}$ . . . control clock
CD . . . control data
CH1 OVL . . . CH1 overload
CH2 OVL . . . CH2 overload
CH1 PA CLK . . . CH1 preamp clock
CH2 PA CLK . . . CH2 preamp clock
CH1 PRB — CH4 PRB . . . CH1 — CH4 probe encoding
CONT DATA . . . control data
CTC . . . capacitor, timing compensation
DAC MUX1 INH . . . DAC multiplexer 1 inhibit
DAC MUX1 A0 . . . DAC multiplexer 1, address bit 0
DAC MUX1 A1 . . . DAC multiplexer 1, address bit 1
DAC MUX1 A2 . . . DAC multiplexer 1, address bit 2
DAC MUX1 IN . . . DAC multiplexer 1 input
DO+ . . . display output, noninverting
DO— . . . display output, inverting
DON3 . . . display output, negative CH 3
DOP3 . . . display output, positive CH 3
DON4 . . . display output, negative CH 4
DOP4 . . . display output, positive CH 4
GA3 . . . gain 3
GA4 . . . gain 4
$\overline{\text{SI}}$ . . . scope identification bit
$\overline{\text{SIL}}$ . . . slow intensity limit
TPO— . . . trigger pickoff, inverting
TPO3 . . . CH3 trigger pickoff
TPO4 . . . CH4 trigger pickoff
TPT— . . . trigger pickoff reverse termination
TXY . . . triggered X-Y

TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the accompanying schematic diagram and board dolly. The waveforms are representative of signals that may be expected at the associated points when the following setup conditions are observed. Any change(s) from the given setup conditions required to produce a given waveform are noted with that waveform illustration.

2445 SETUP

Connect a 200-mV, 1-kHz squarewave signal from a signal generator to the CH 1 and CH 2 inputs of the 2445 via a BNC T-connector, a 50-ohm BNC cable and a dual-input coupler.

Set:

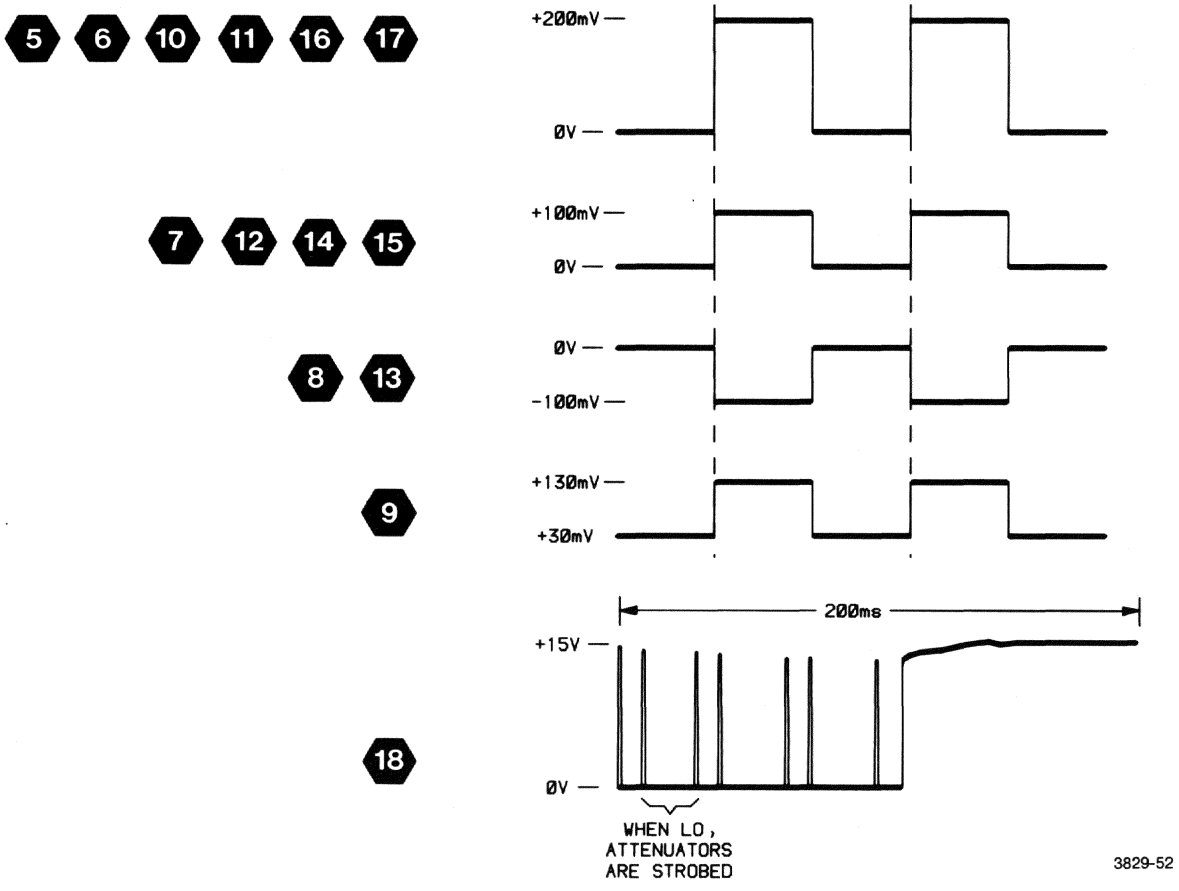
VERTICAL MODE	CH 1
Input Coupling	
CH 1 and CH 2	1 MΩ DC
VOLTS/DIV	
CH 1 and CH 2	50 mV
A and B SEC/DIV	0.5 ms (knobs locked)

TRIGGER	
MODE	AUTO
SOURCE	VERT
COUPLING	DC

All other control settings are irrelevant.

TEST OSCILLOSCOPE SETUP

Connect the 200-mV, 1-kHz squarewave from the BNC T-connector to the External Trigger input of the test oscilloscope using a 50-ohm BNC cable. Externally trigger the test oscilloscope on the rising edge of the 1-kHz signal and, using a X10 probe with the test oscilloscope, set its Volts/Div and Time/Div ranges as required to obtain the indicated displays.



ATTENUATORS AND PREAMPS DIAGRAM 4

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C100	1H	4C	CR150	7F	6C	R114	3N	6D	R329	9L	2D
C103	3G	5C	CR151	7F	6C	R115	3N	6D	R332	9L	2D
C104	2M	5D	CR152	7E	6C	R117	2K	6E	R430	8P	3E
C105	1H	4C	CR153	7E	6C	R118	2L	5E	R440	8K	4F
C115	3P	6E	CR154	4G	6C	R119	2K	6D	R450	2N	3E
C116	3P	7E	CR155	7G	6C	R121	2M	4D	R451	2P	3E
C117	2M	4D	CR160	7L	2D	R123	3C	2H	R452	2N	3E
C118	3S	7E	CR161	7L	2D	R129	6B	5C	R453	2P	3E
C122	2M	5D	CR162	2L	2D	R130	6B	7B	R454	7N	3F
C130	6B	5C	CR163	2L	2D	R131	6C	7B	R455	7N	3E
C175	7K	2D	CR200	8J	3C	R133	5M	6B	R456	7P	3E
C176	7K	2D	CR201	8J	3C	R135	4M	6B	R457	7P	4F
C177	2K	2D	CR460	8S	3E	R136	3B	1H	R458	1S	4F
C179	2K	2D	CR461	8S	3E	R140	6B	7C	R459	7S	4G
C184	9M	2F				R141	6B	7C	R460	8N	3E
C185	9N	3B	J10	2H	5B	R142	5C	7C	R461	8N	3E
C200	8H	3C	J11	8H	3B	R143	6B	7C	R462	8P	4J
C202	7G	4C	J100	1T	4F	R144	5C	7B	R463	8N	3E
C203	8M	4C	J100	7T	4F	R149	4C	7B	R464	8S	3E
C205	7H	3C	J100	8K	4F	R159	7K	1D	R465	8P	3F
C206	7M	4D	J103	8L	4C	R161	7L	2D	R502	3B	1G
C217	7K	2D	J105	8T	3E	R162	2K	2D			
C222	7M	4D	J110	6T	2E	R163	2K	2D	U100	2M	5D
C301	10B	1B	J111	4N	6B	R190	3J	2E	U110	4E	6B
C302	10B	3B	J117	2P	6E	R191	3J	2E	U120	6E	6C
C310	8H	1C	J181	5P	6B	R192	4J	2E	U130A	5G	6C
C311	2H	1C	J511	10T	1D	R193	4J	1E	U130B	5G	6C
C329	9L	2D	J511	9B	1D	R194	3J	1H	U130C	5K	6C
C332	9L	2D	J512	3A	1H	R195	8N	2E	U130D	5M	6C
C450	2P	3F				R196	8M	2E	U130E	5M	6C
C454	7P	3F	L115	3P	6E	R197	9M	2F	U130F	4M	6C
C460	8P	3E				R198	9M	3F	U130G	6B	6C
C464	8S	3E	LR180	2N	4E	R199	9M	3F	U140	5D	7B
			LR280	7N	3E	R200	8H	3C	U150	6D	7C
CR100	1J	5C				R201	8H	3B	U160A	2L	2D
CR101	1J	5C	P100A	2T	4F	R202	8H	3B	U160B	6L	2D
CR130	6C	7B	P100D	7T	4F	R216	7L	3D	U160C	7K	2D
CR131	6C	7B	P103	8L	4C	R217	7K	3D	U160D	1K	2D
CR140	4G	6B				R218	7K	3E	U165A	8M	2F
CR141	4F	6B	Q130	6C	7B	R219	7L	3D	U170	4J	2E
CR142	4F	6B	Q131	6C	7B	R223	3C	2E	U200	7M	4D
CR143	4F	6B	Q190	8N	3E	R230	3D	2E	U300	10M	2B
CR144	4F	6B	Q460A	8P	3E	R231	3B	2E	U450A	7P	3F
CR145	4E	6B	Q460B	8P	3E	R232	3C	3E	U450B	2P	3F
CR146	4E	6B				R301	10A	1A			
CR147	7G	6C	R100	1H	4C	R302	10A	2A	W171	7L	2D
CR148	7F	6C	R101	1H	5B	R304	10A	1B	W172	1L	2D
CR149	7F	6C	R102	2H	5B	R311	10A	2A	W194	3J	2E

Partial A1 also shown on diagrams 5, 6, 8 and 11.

ASSEMBLY A8

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
DS100	5S	1M	DS102	5S	1P	P181	5S	1P	W181	5S	1P
DS101	5S	1N									

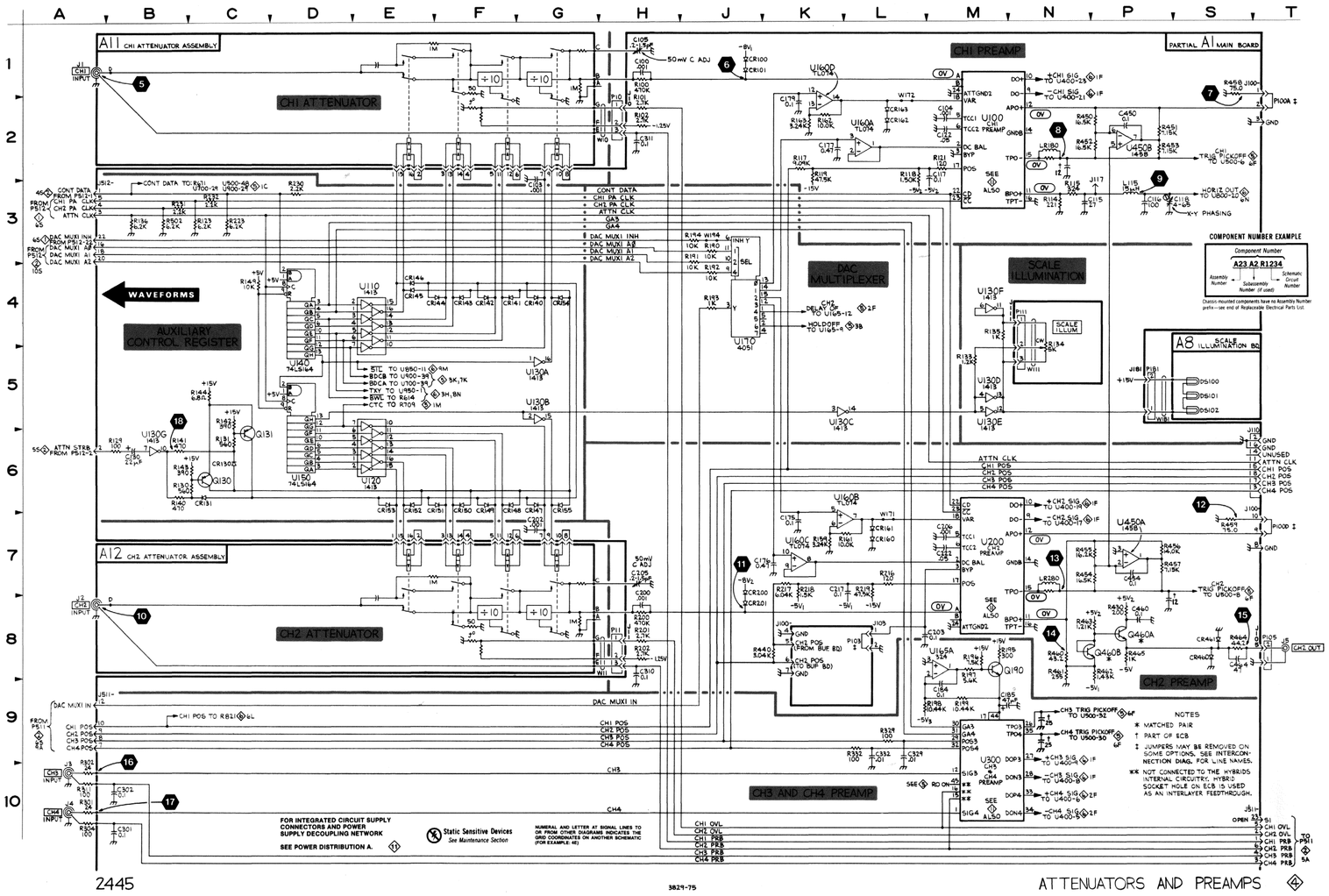
ASSEMBLY A11

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J1	1A	5A	P10	1H	5B	W10	2H	5B			

ASSEMBLY A12

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J2	8A	3A	J3	10A	CHASSIS	P111	4N	CHASSIS	W111	5N	CHASSIS
P11	8H	3B	J4	10A	CHASSIS						
W11	9H	3B	J5	8T	CHASSIS	R134	5N	CHASSIS			



TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the accompanying schematic diagram and board dolly. The waveforms are representative of signals that may be expected at the associated points when the following setup conditions are observed. Any change(s) from the given setup conditions required to produce a given waveform are noted with that waveform illustration. Where B Sweep setup conditions are referenced with a waveform, it is assumed that the B SEC/DIV knob is set to 100 μs/div unless otherwise noted.

2445 SETUP

Connect a 200-mV, 1-kHz squarewave to the CH 1 input of the 2445 using a BNC cable.

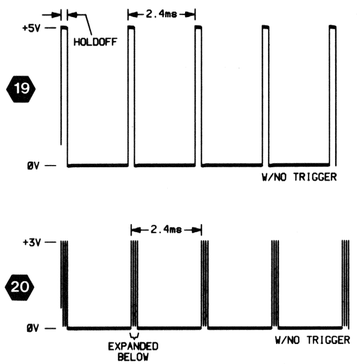
Set:

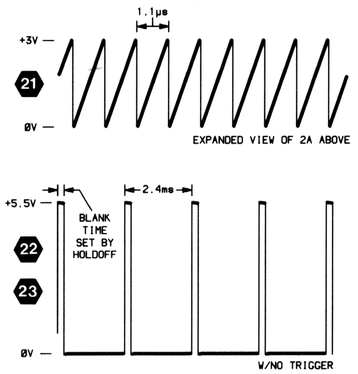
VERTICAL MODE	CH 1
Input Coupling	
CH 1 and CH 2	1 MΩ DC
VOLTS/DIV	
CH 1 and CH 2	50 mV
CH 1 and CH 2 VAR	In detent
A and B SEC/DIV	0.2 ms (knobs locked)
A and B SEC/DIV VAR	In detent
TRIGGER	
MODE	AUTO
SOURCE	VERT
COUPLING	NOISE REJ
HOLDOFF	In detent
SLOPE	+ (plus)
LEVEL	Stably triggered display
Δt	DLY readout
Δ REF OR DLY POS	1000.0 μs readout
INTENSITY	Midrange
READOUT INTENSITY	Minimum (once DLY readout is set)

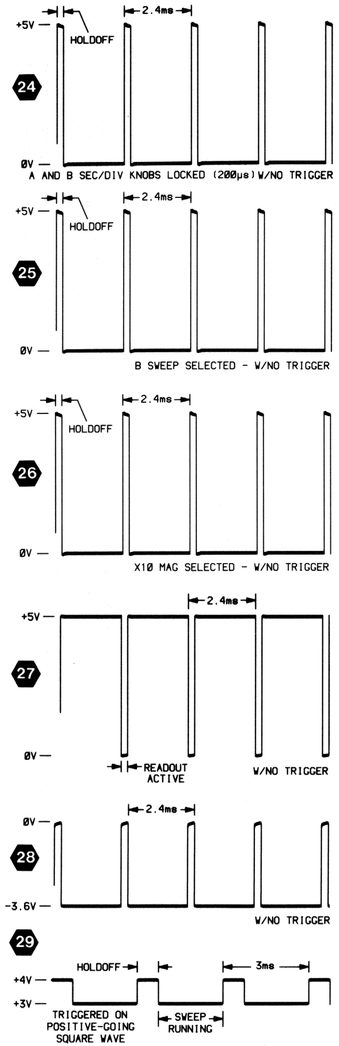
All other control settings are irrelevant.

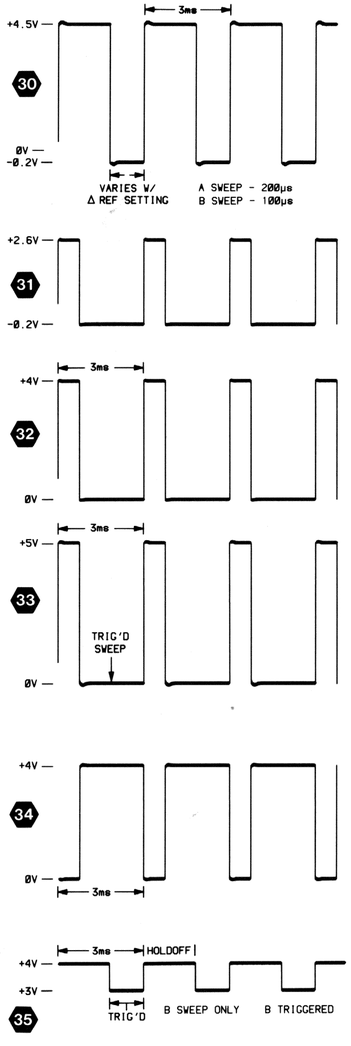
TEST OSCILLOSCOPE SETUP

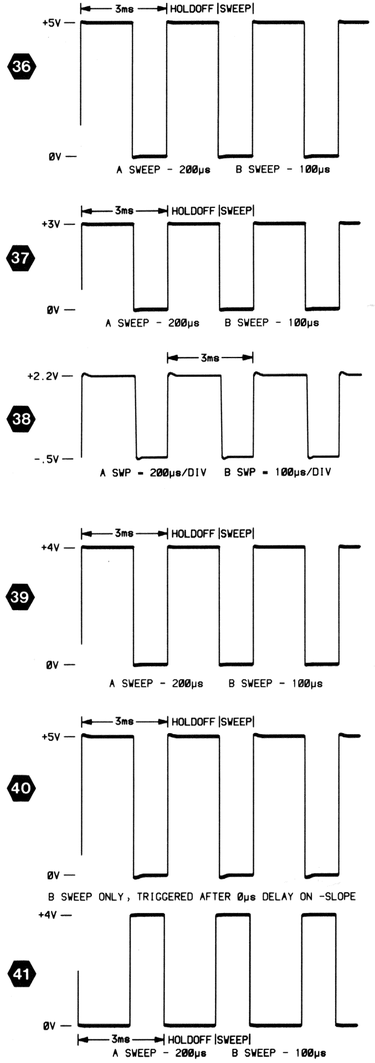
Using a X10 probe with the test oscilloscope, set its Trigger Slope, Trigger Level, Volts/Div and Time/Div ranges as required to obtain the indicated displays.

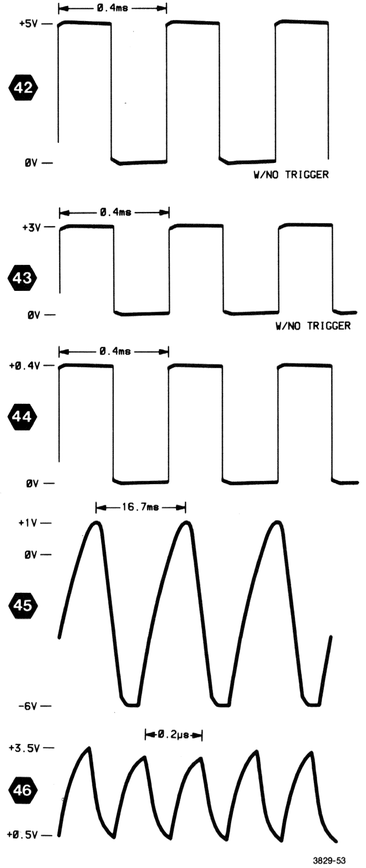












ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

ACA . . . A low-pass capacitor
ACB . . . B low-pass capacitor
AHO . . . A holdoff
A TIM REF . . . A timing reference
B TIM REF . . . B timing reference
BDC . . . bypass delay comparator
BDCA . . . bypass delay comparator A
BDCB . . . bypass delay comparator B
BWLB . . . bandwidth limited B signal
CAL . . . calibrator
CAL OUT . . . calibrator out
$\overline{\text{CC}}$ . . . control clock
$\overline{\text{CCA}}$ . . . control clock A
$\overline{\text{CCB}}$ . . . control clock B
CD . . . control data
CHN5A . . . CH5 (for A trigger)
CHN5B . . . CH5 (for B trigger)
CONT DATA . . . control data
CT . . . calibrator timing out
CTC . . . capacitor, timing compensation
CT0 . . . timing capacitor 0
$\overline{\text{CT2}}$ . . . timing capacitor 2
$\overline{\text{DG}}$ . . . delay gate
DGB . . . delay gate bypass
DI . . . display intensity
DOR . . . delay offset reference
DR . . . delay reference
$\overline{\text{DS}}$ . . . delay select
$\overline{\text{HRR}}$ . . . holdoff ramp reset
$\overline{\text{HSA}}$ . . . horizontal select A
$\overline{\text{HSB}}$ . . . horizontal select B
IREF . . . current reference
IT . . . timing current
ITF . . . timing current feedback
ITR . . . timing current reference
ITREF . . . timing current reference
ITRR . . . timing current reference return
IZD . . . inhibit zero delay
RDA . . . reset delay adjust
$\overline{\text{ROA}}$ . . . readout acknowledge
$\overline{\text{ROB}}$ . . . readout blank
ROI . . . readout intensity
RO ON . . . readout on
$\overline{\text{ROR}}$ . . . readout request
SDO . . . sweep delay offset
$\overline{\text{SG}}$ . . . sweep gate
$\overline{\text{SGA}}$ . . . sweep gate A
$\overline{\text{SGAZ}}$ . . . sweep gate A to Z axis
$\overline{\text{SGB}}$ . . . sweep gate B
$\overline{\text{SGBZ}}$ . . . sweep gate B to Z axis
$\overline{\text{SR0A}}$ . . . A trigger source select 0
$\overline{\text{SR1A}}$ . . . A trigger source select 1
$\overline{\text{SR2A}}$ . . . A trigger source select 2
$\overline{\text{SR0B}}$ . . . B trigger source select 0
$\overline{\text{SR1B}}$ . . . B trigger source select 1
$\overline{\text{SR2B}}$ . . . B trigger source select 2
SSA . . . A selected signal source
SSB . . . B selected signal source
SSR . . . sweep start reference
$\overline{\text{STBA}}$ . . . A compare strobe
$\overline{\text{STBB}}$ . . . B compare strobe
TC . . . timing clock
TCS . . . timing capacitor select
TGA . . . A trigger
$\overline{\text{TGA}}$ . . . inverted A trigger
TGB . . . B trigger
$\overline{\text{TGB}}$ . . . inverted B trigger
THO . . . trigger holdoff
THOA . . . trigger holdoff A
THOB . . . trigger holdoff B
TLA . . . trigger level A
TLB . . . trigger level B
TRIG STAT STRB . . . trigger status strobe
$\overline{\text{TSA}}$ . . . trigger status A
$\overline{\text{TSB}}$ . . . trigger status B
TS IN . . . trace separation input
TSO . . . trigger status output
$\overline{\text{TSS}}$ . . . trigger status strobe
TS1 . . . trace separation voltage 1
TS2 . . . trace separation voltage 2
TS1+TS2 . . . trace separation 1 and 2
VBBI . . . bias voltage in
VBBO . . . bias voltage out
$\overline{\text{VS1}}$ – $\overline{\text{VS4}}$ . . . vertical selects 1 – 4

DISPLAY SEQUENCER, TRIGGERING, A & B SWEEPS DIAGRAM 5

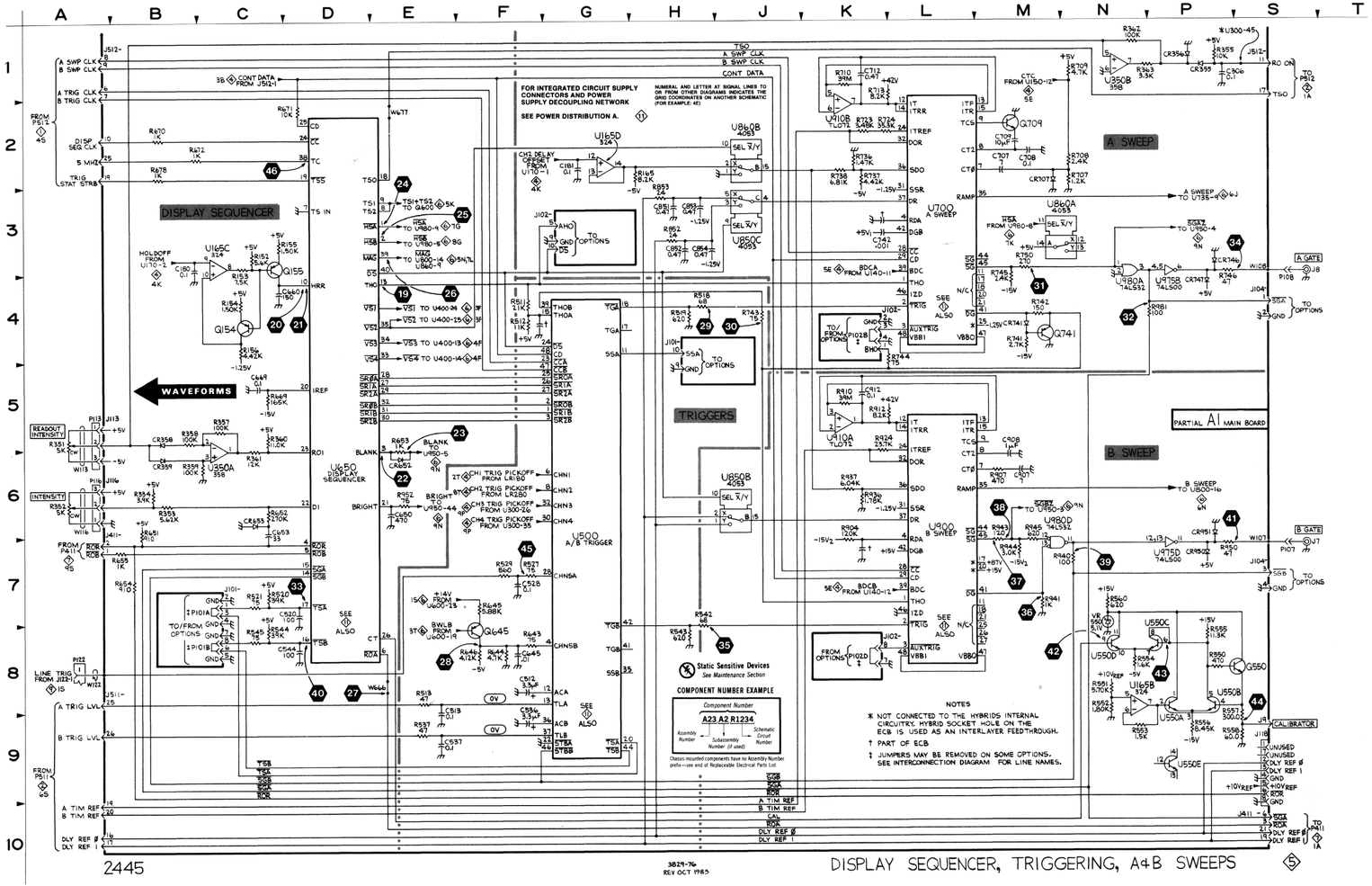
ASSEMBLY A1

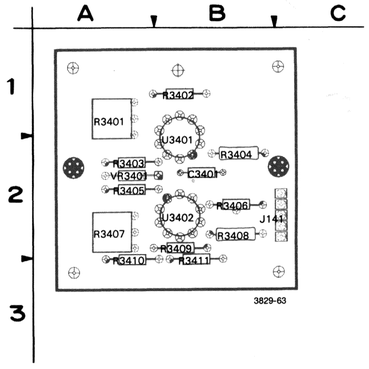
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C180	3B	2E	J113	5A	7B	R537	9E	1E	R907	6M	7H
C181	2G	2E	J116	6A	9B	R542	7H	3F	R910	5K	9F
C306	1P	1B	J118	9S	2K	R543	8H	2F	R912	5K	9E
C512	8F	3H	J411	10S	1K	R544	8C	3H	R924	5K	7G
C513	8E	3H	J411	6A	1K	R545	8C	3H	R936	6K	9F
C520	7D	2H	J511	8A	1D	R550	8P	1G	R937	6K	8G
C528	7F	1G	J512	1A	1H	R551	8N	1E	R940	7M	6K
C536	9F	1F	J512	1S	1H	R552	8N	1E	R941	7M	9J
C537	9E	2F				R553	9N	1F	R943	6M	9H
C544	8D	3H	P101A	7B	3H	R554	8N	1G	R944	7M	8J
C645	8F	5G	P101B	8B	3H	R555	8P	1G	R945	6M	7J
C650	6E	7K	P102B	4K	6F	R556	9P	1F	R950	7P	6K
C653	6C	3J	P102D	8K	6F	R557	9P	1E	R952	6E	7K
C660	4D	3J	P107	7S	6K	R558	9P	1E	R981	4P	5K
C669	5C	2J	P108	4S	5K	R560	7N	1F			
C707	2M	8C	P122	8A	4H	R643	8F	5G	U165B	8N	2F
C708	2M	8C				R644	8F	5G	U165C	3C	2F
C709	2M	8D	Q154	4C	1E	R645	7F	5G	U165D	2G	2F
C712	1K	9E	Q155	3D	1F	R646	8F	5G	U350A	6C	8B
C742	3K	6D	Q550	8S	1E	R651	6B	1J	U350B	1N	8B
C851	3H	8E	Q645	8F	6G	R652	6C	2J	U500	7G	2G
C852	3H	8E	Q709	2M	8D	R653	5E	4J	U550A	9P	1F
C853	3H	8E	Q741	4M	6D	R654	7B	1J	U550B	8P	1F
C854	3H	8E				R655	7B	1J	U550C	8P	1F
C907	6M	7J	R152	3C	2F	R669	5C	2J	U550D	8N	1F
C908	5M	8J	R153	3C	2F	R670	2B	1J	U550E	9P	1F
C912	5K	9E	R154	4C	2E	R671	2D	2H	U650	6D	3J
			R155	3D	2F	R672	2B	2H	U700	3L	7D
CR355	1P	7B	R166	4C	2E	R678	2B	2H	U850B	6J	8F
CR356	1P	7B	R165	2H	2E	R707	2N	8C	U850C	3J	8F
CR358	5B	7B	R334	6B	9B	R708	2N	8C	U860A	3M	6F
CR359	6B	8B	R353	6B	2H	R709	1N	8C	U860B	2J	6F
CR652	6E	4J	R355	1P	7B	R710	1K	9F	U900	6L	8H
CR653	6C	3J	R357	5C	7C	R713	1K	9E	U910A	5K	9F
CR707	2M	8B	R358	5B	7C	R723	2K	8E	U910B	2K	9F
CR741	4M	6D	R359	6B	8B	R724	2K	8E	U975B	4P	6K
CR746	3P	5K	R360	5C	3H	R736	2K	9F	U975D	7P	6K
CR747	4P	5K	R361	6C	3H	R737	2K	9F	U980A	4N	6K
CR950	7P	6K	R362	1N	7B	R738	2K	9F	U980D	6M	6K
CR951	6P	6K	R363	1N	7B	R741	4M	6D			
			R511	4F	3H	R742	4M	6D	VR550	8N	1E
J9	9S	2A	R512	4F	3H	R743	4J	6D			
J101	4H	3H	R513	8E	3H	R744	4L	7F	W107	7S	6K
J101	7C	3H	R518	4H	3H	R745	4M	6D	W108	3S	5K
J102	3F	7F	R519	4H	3H	R746	4P	5K	W122	8A	4H
J102	4K	7F	R520	7C	2H	R750	3M	6D	W666	8E	1J
J102	8K	7F	R521	7C	2H	R852	3H	8E	W677	2E	2J
J104	4S	5K	R527	7F	1G	R853	3H	8E			
J104	7S	5K	R529	7F	1G	R904	6K	8J			

Partial A1 also shown on diagrams 4, 6, 8 and 11.

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J7	7S	CHASSIS	P113	5A	CHASSIS	R351	5A	CHASSIS	W113	6A	CHASSIS
J8	3S	CHASSIS	P116	6A	CHASSIS	R352	6A	CHASSIS	W116	6A	CHASSIS





Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number: A23 A2 R1234
Assembly Number — Subassembly Number (if used) — Schematic Circuit Number

Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

Figure 9-9. A14—Dynamic Centering board.

ALL COMPONENTS MOUNTED ON A14—DYNAMIC CENTERING BOARD ARE SHOWN ON SCHEMATIC DIAGRAM 6

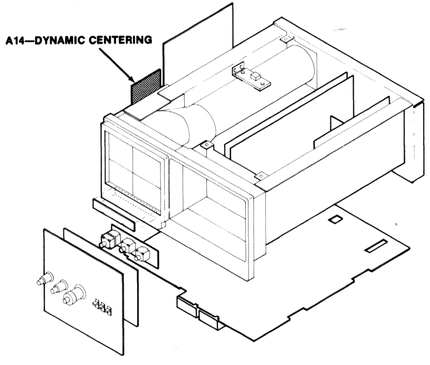


FIG. 9-9
A14—DYNAMIC CENTERING BD & WAVEFORMS

TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the accompanying schematic diagram and board dolly. The waveforms are representative of signals that may be expected at the associated points when the following setup conditions are observed. Any change(s) from the given setup conditions required to produce a given waveform are noted with that waveform illustration. Where B Sweep setup conditions are referenced with a waveform, it is assumed that the B SEC/DIV knob is set to 100 μs/div unless otherwise noted.

2445 SETUP

Connect a 200-mV, 1-kHz squarewave to the CH 1 input of the 2445 using a BNC cable.

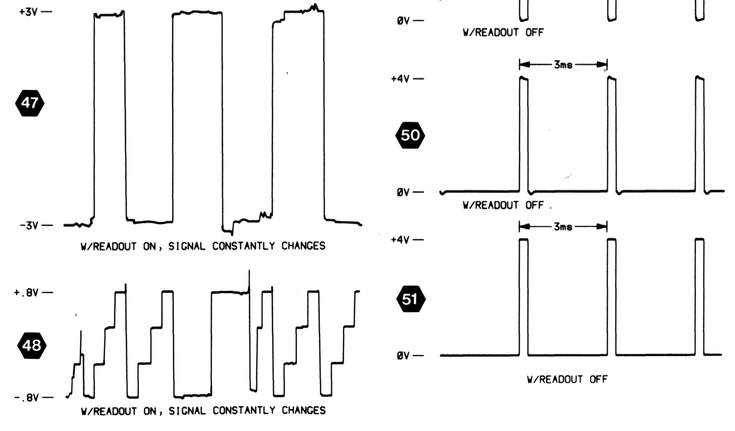
Set:

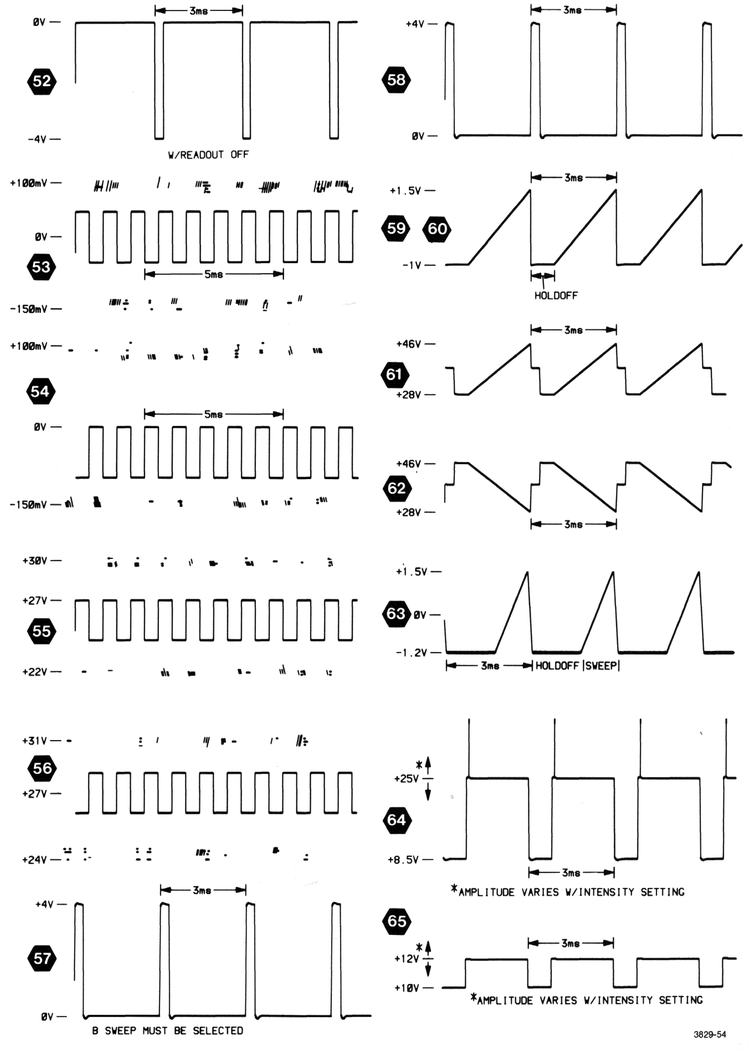
VERTICAL MODE	CH 1
Input Coupling	
CH 1 and CH 2	1 MΩ DC
VOLTS/DIV	
CH 1 and CH 2	50 mV
CH 1 and CH 2 VAR	In detent
A and B SEC/DIV	0.2 ms (knobs locked)
A and B SEC/DIV VAR	In detent
TRIGGER	
MODE	AUTO
SOURCE	VERT
COUPLING	NOISE REJ
HOLDOFF	In detent
SLOPE	+ (plus)
LEVEL	Stably triggered display
Δt	DLY readout
Δ REF OR DLY POS	1000.0 μs readout
INTENSITY	Midrange
READOUT INTENSITY	Minimum (once DLY readout is set)

All other control settings are irrelevant.

TEST OSCILLOSCOPE SETUP

Using a X10 probe with the test oscilloscope, set its Trigger Slope, Trigger Level, Volts/Div and Time/Div ranges as required to obtain the indicated displays.





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ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

A+ . . . A sweep
B+ . . . B sweep
BD0 . . . buffered data bit 0
BF . . . beamfind
BTST . . . bootstrap
$\overline{\text{BWL}}$ . . . bandwidth limit
BWLA1 . . . A bandwidth limit inductor input
BWLA2 . . . A bandwidth limit inductor output
BWLB . . . bandwidth limit B
BWLB1 . . . B bandwidth limit inductor input
BWLB2 . . . B bandwidth limit inductor output
CLB . . . current limit bypass
CMB . . . common mode bypass
COMP A . . . A compensation
COMP B . . . B compensation
GA . . . gain
GADJ . . . gain adjust
$\overline{\text{HSA}}$ . . . horizontal select A
$\overline{\text{HSB}}$ . . . horizontal select B
I BIAS . . . current reference
ISRC . . . current source
MKL RC . . . mean cathode loading RC
MREG . . . mag registration
Q GAIN . . . quadrapole gain
RO DO . . . readout data out
ROSFRAME . . . readout subframe
R/$\overline{\text{W}}$ DLYD . . . read/write delayed
RO . . . readout
$\overline{\text{ROS1}}$ . . . readout strobe 1
$\overline{\text{ROS2}}$ . . . readout strobe 2
$\overline{\text{SGA}}$ . . . sweep gate A
$\overline{\text{SGAZ}}$ . . . sweep gate A to Z-axis
$\overline{\text{SGB}}$ . . . sweep gate B
$\overline{\text{SGAB}}$ . . . sweep gate B to Z-axis
$\overline{\text{SIL}}$ . . . slow intensity limit
TADJ . . . thermal adjust
TRANR . . . transient response
TRANS RESP . . . transient response
TRQ . . . transient response, quadrapole drive
TRZ . . . transient response, Z-axis
TS . . . trace separation
TS1+TS2 . . . trace separation inputs 1 and 2
TXY . . . triggered X-Y
VZOUT . . . variable Z-axis output
VQOUT . . . variable quadrapole output
$\overline{\text{VS1}}$ – $\overline{\text{VS4}}$ . . . vertical selects 1 – 4
X+ . . . noninverting external input
X– . . . inverting external input

CHANNEL SWITCH AND OUTPUT AMPLIFIERS DIAGRAM 6

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C402	3F	5F	L608	2N	5H	R500	10B	1J	R956	8N	7K
C404	2K	5J	L609	2M	5H	R501	10B	1J	R957	8N	7J
C412	2F	4F	L610	2M	5H	R600	3P	6J	R972	9S	9K
C478	3E	3J	L611	2L	5H	R601	2N	5H	R973	9P	9K
C487	2C	3K	L612	2L	5H	R602	2N	5H	R995	9B	7K
C488	2B	3K	L619	3P	6G	R605	2N	5H			
C617	3M	5G	L644	3P	6J	R606	2M	5H	S615	4M	8B
C625	1P	6G	P106	9A	7K	R607	2M	5G			
C735	6K	7E	P141	5F	9K	R608	2M	4H	U400	2G	5E
C803	6N	8F	P141	6C	9K	R614	3H	7E	U475A	3D	4J
C805	7S	7F				R615	4M	9B	U475B	3D	4J
C806	7P	7F	Q600	4L	4J	R617	3M	5G	U475C	1D	4J
C808	5P	7F	Q623	1P	6G	R618	3L	5G	U475D	3E	4J
C809	5S	7F	Q624	1N	6G	R619	3P	6G	U475E	3E	4J
C817	3B	7F				R620*	3T	4H	U485A	2C	3K
C822	5B	8E	R401	2F	5F	R622	4N	6G	U485B	2D	3K
C956	8M	6K	R402	3F	5F	R624	1P	6G	U485C	1B	3K
C957	8M	7J	R403	2K	5J	R638	3N	6J	U485D	1C	3K
C972	9S	9K	R412	2F	4F	R639	4N	6J	U485E	1B	3K
C995	9B	7K	R416	2F	4F	R642	4L	3E	U600	2P	6H
			R470	4C	3K	R650	4K	4J	U735A	5K	7E
CR476	3E	3J	R471	3C	4K	R659	3N	6J	U735B	5K	7E
CR484	4C	3K	R476	3F	4J	R731	5K	7E	U735C	6K	7E
CR485	4C	3K	R477	3E	3J	R732	6J	7E	U735D	6J	7E
CR495	2D	3K	R478	3E	3J	R733	6K	7E	U735E	6K	7E
CR600	4L	6J	R479	2E	4J	R734	6K	7E	U800	5P	7F
CR601*	3S	6J	R480	2D	2J	R735	6K	7E	U850A	8M	8F
CR616	4H	6K	R481	3D	4K	R800	7M	8F	U860C	7L	6F
CR619*	3S	6G	R482	3D	4K	R801	7M	8F	U950	8P	8K
CR620*	3S	4J	R483	2C	4K	R802	6N	8F	U975A	4D	6K
CR621*	3S	4H	R484	3D	4K	R803	6N	8G	U975C	7H	6K
CR956	8N	7K	R485	4C	4K	R804	6S	7F	U980B	8H	6K
CR986	8S	9K	R486	2C	4K	R805	6P	7F	U980C	7H	6K
CR972	9S	9K	R487	2B	3K	R806	7S	7F			
			R488	2B	3K	R809	5S	7F	W106	9B	7K
DL100	2H	5K	R489	2B	3K	R817	2B	6F	W141	7F	9K
J191	8S	8K	R490	1C	3J	R820	6L	6E	W141	9C	9K
J411	10S	1K	R491	1D	3J	R821	6L	6E	W916	2S	7H
J411	2B	1K	R492	2E	3J	R822	5B	6E	W917	3S	7H
J511	4B	1D	R493	2D	3J	R823	6M	8E	W918	5S	7G
J512	10B	1H	R494	2D	3K	R850	6L	8F	W919	6S	7G
J512	9S	1H	R495	2F	4J	R855	6N	6F			
L605	2N	5H	R497	4C	5K	R856	6M	9E			
L606	2M	5J	R498	3D	6K	R858	6M	9E			
L607	2M	5G				R860	6M	9D			

Partial A1 also shown on diagrams 4, 5, 8 and 11.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P191	9L	4B	R1820	9K	1B	R1842	9K	1C			
			R1834	9L	1B						

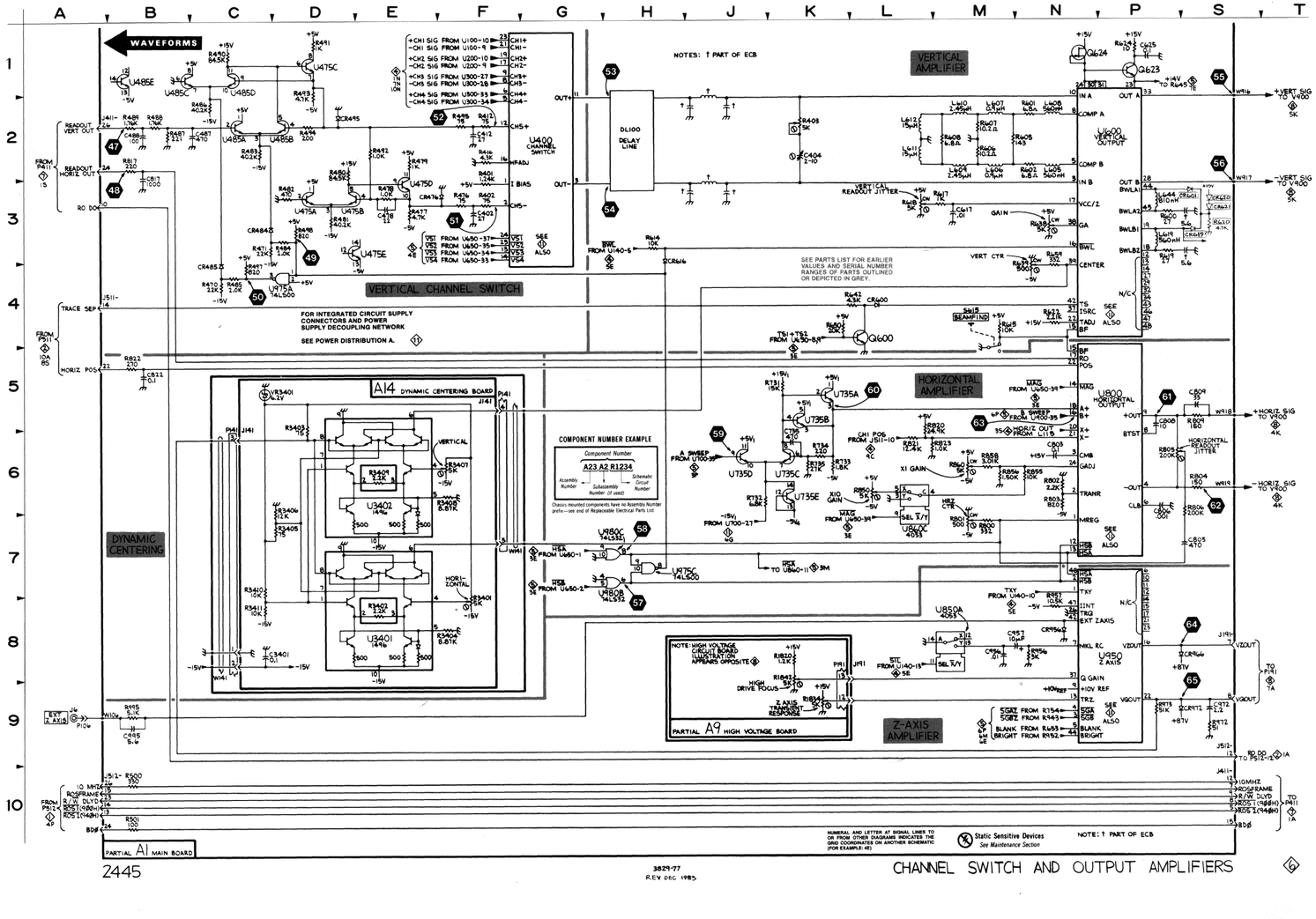
Partial A9 also shown on diagrams 8 and 12.

ASSEMBLY A14

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C3401	9D	2B	R3402	8E	1B	R3408	7F	2B	U3402	7E	2B
			R3403	6D	2A	R3409	6E	2B			
J141	5F	2B	R3404	8F	2B	R3410	8D	3A	VR3401	5D	2A
J141	6C	2B	R3405	7D	2A	R3411	8D	3B			
			R3406	7D	2B						
R3401	8F	1A	R3407	6F	2A	U3401	8E	2B			

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J6	9A	CHASSIS									



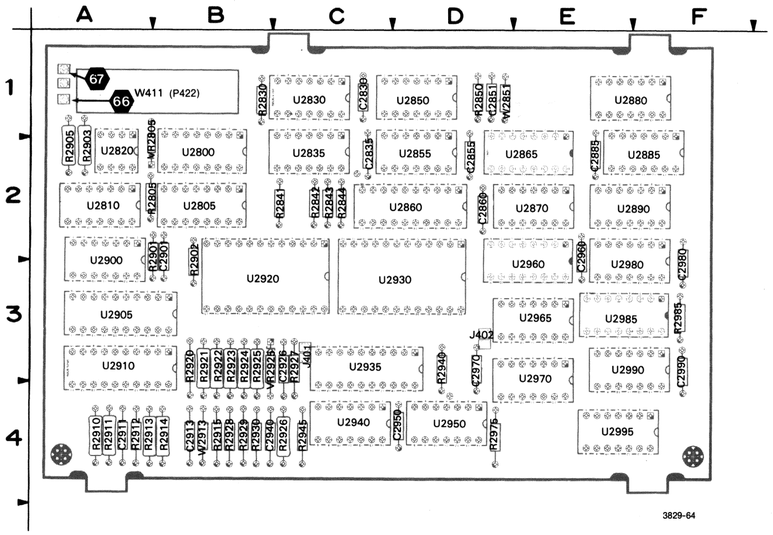
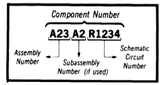


Figure 9-10. A4—Readout board.

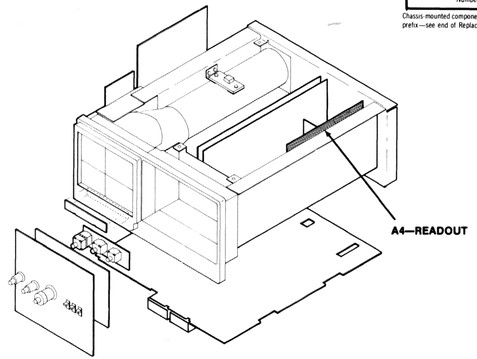
( ) COMPONENTS WITHIN PARENTHESES MAY NOT BE LOCATED PRECISELY AS SHOWN BUT ARE NEAR THEIR INDICATED POSITION.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

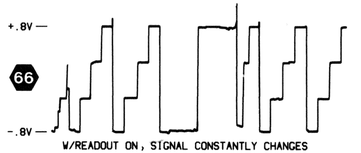


A4—READOUT BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C2830	12	R2920	7	U2855	7	U2940	12
C2835	12	R2921	7	U2855	7	U2950	7
C2851	12	R2922	7	U2855	7	U2950	7
C2855	12	R2923	7	U2855	12	U2950	12
C2860	12	R2924	7	U2860	7	U2960	7
C2885	12	R2925	7	U2860	12	U2960	12
C2901	12	R2926	7	U2865	7	U2965	7
C2911	7	R2927	7	U2865	12	U2965	7
C2913	12	R2928	7	U2870	7	U2965	7
C2926	12	R2929	7	U2870	7	U2965	7
C2940	12	R2930	7	U2870	12	U2965	12
C2950	12	R2940	7	U2880	7	U2970	7
C2960	12	R2945	7	U2880	7	U2970	7
C2970	12	R2975	7	U2880	12	U2970	7
C2980	12	R2985	7	U2885	7	U2970	7
C2990	12	U2800	7	U2885	7	U2970	12
J401	7	U2800	12	U2885	7	U2980	7
J402	7	U2805	7	U2885	12	U2980	7
P411	7	U2805	12	U2890	7	U2980	7
P411	7	U2810	7	U2890	7	U2980	7
P411	7	U2810	7	U2890	7	U2980	12
P411	12	U2810	7	U2890	7	U2985	7
R2805	12	U2810	7	U2890	12	U2985	12
R2830	7	U2810	12	U2900	7	U2990	7
R2841	7	U2820	7	U2900	7	U2990	7
R2842	7	U2820	7	U2900	7	U2990	7
R2843	7	U2820	12	U2900	12	U2990	7
R2844	7	U2830	7	U2905	7	U2990	12
R2850	7	U2830	7	U2905	12	U2995	7
R2901	7	U2830	12	U2910	7	U2995	12
R2902	7	U2835	7	U2910	12	VR2805	12
R2903	7	U2835	7	U2920	7	VR2925	7
R2905	7	U2835	7	U2920	12	W411	7
R2910	7	U2835	7	U2930	7	W411	7
R2911	7	U2835	12	U2930	12	W411	7
R2912	7	U2850	7	U2935	7	W411	12
R2913	7	U2850	7	U2935	12	W2851	12
R2914	7	U2850	12	U2940	7	W2913	12
R2915	7	U2855	7	U2940	7		

TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the accompanying schematic diagram and board dolly. The waveforms are representative of signals that may be expected at the associated points when the indicated setup conditions are observed.



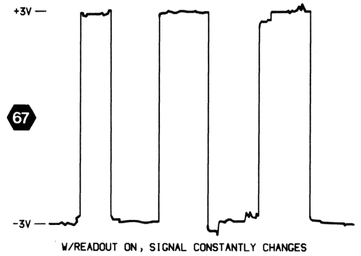


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FIG. 9-10

A4—READOUT BD & WAVEFORMS

READOUT DIAGRAM 7

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2911	2K	4A	R2945	2B	4C	U2900B	5L	2A
			R2975	7M	4D	U2900B	9L	2A
J401	1H	3C	R2985	8E	3F	U2900C	5L	2A
J402	3H	3D				U2905	4K	3A
			U2800	4P	2B	U2910	1K	3A
P411	1A	1A	U2805	2P	2B	U2920	2F	3B
P411	1S	1A	U2810A	6L	2A	U2930	1H	3D
P411	9S	1A	U2810B	6L	2A	U2935	1D	3C
			U2810C	6N	2A	U2940A	2C	4C
R2830	8C	1B	U2810D	5N	2A	U2940B	1B	4C
R2841	5M	2C	U2820A	5P	2A	U2950A	9E	4D
R2842	3B	2C	U2820B	3P	2A	U2950B	9J	4D
R2843	4B	2C	U2830A	8C	1C	U2960	3D	2E
R2844	5B	2C	U2830B	7B	1C	U2965A	5C	3E
R2850	9D	1D	U2835A	6G	2C	U2965B	9H	3E
R2901	5M	2B	U2835B	9K	2C	U2965C	4F	3E
R2902	3F	2B	U2835C	9G	2C	U2965D	9M	3E
R2903	5P	2A	U2835D	2E	2C	U2970A	9N	3E
R2905	5P	2A	U2850A	9D	1D	U2970B	9H	3E
R2910	1K	4A	U2850B	9E	1D	U2970C	7G	3E
R2911	1K	4A	U2855A	7B	2D	U2970D	9G	3E
R2912	2L	4A	U2855B	6E	2D	U2980A	9H	2E
R2913	3L	4A	U2855C	3E	2D	U2980B	8P	2E
R2914	3L	4B	U2855D	3E	2D	U2980C	9N	2E
R2915	4L	4B	U2860	5F	2D	U2980D	5E	2E
R2920	4M	3B	U2865	6D	2E	U2985	8F	3E
R2921	5M	3B	U2870A	6F	2E	U2990A	8E	3E
R2922	5M	3B	U2870B	5F	2E	U2990B	9H	3E
R2923	4M	3B	U2880A	8J	1E	U2990C	9M	3E
R2924	4M	3B	U2880B	8P	1E	U2990D	8M	3E
R2925	4M	3B	U2885A	10H	2F	U2995	9M	4E
R2926	5M	4C	U2885B	8J	2F			
R2927	2H	3C	U2885C	8S	2F	VR2925	4M	3C
R2928	4L	4B	U2890A	8B	2E			
R2929	4L	4B	U2890B	9K	2E	W411	10S	1A
R2930	4M	4B	U2890C	8L	2E	W411	1A	1A
R2940	8D	3D	U2890D	9K	2E	W411	5S	1A

Partial A4 also shown on diagram 12.

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

BD0 . . . buffered data bit 0
CA0 – CA6 . . . character address bits 0 – 7
CD0 – CD7 . . . character data bits 0 – 7
DD0 – DD7 . . . dot data bits 0 – 7
$\overline{\text{EOCH}}$ . . . end of character
$\overline{\text{EOCH1}}$ . . . end of character delayed 1 dot
$\overline{\text{EOCH2}}$ . . . end of character delayed 2 dots
$\overline{\text{RA0}}$ – $\overline{\text{RA6}}$ . . . RAM address bits 0 – 6
$\overline{\text{ROA}}$ . . . readout acknowledge
$\overline{\text{ROB}}$ . . . readout blank
RO DO . . . readout data out
$\overline{\text{ROR}}$ . . . readout request
ROR DOT TIMER DELAY . . . readout request dot timer delay
ROSFRAME . . . readout subframe
$\overline{\text{ROS1}}$ . . . readout strobe 1
$\overline{\text{ROS2}}$ . . . readout strobe 2
R/$\overline{\text{W}}$ DLYD . . . read/write delayed
$\overline{\text{SGA}}$ . . . sweep gate A

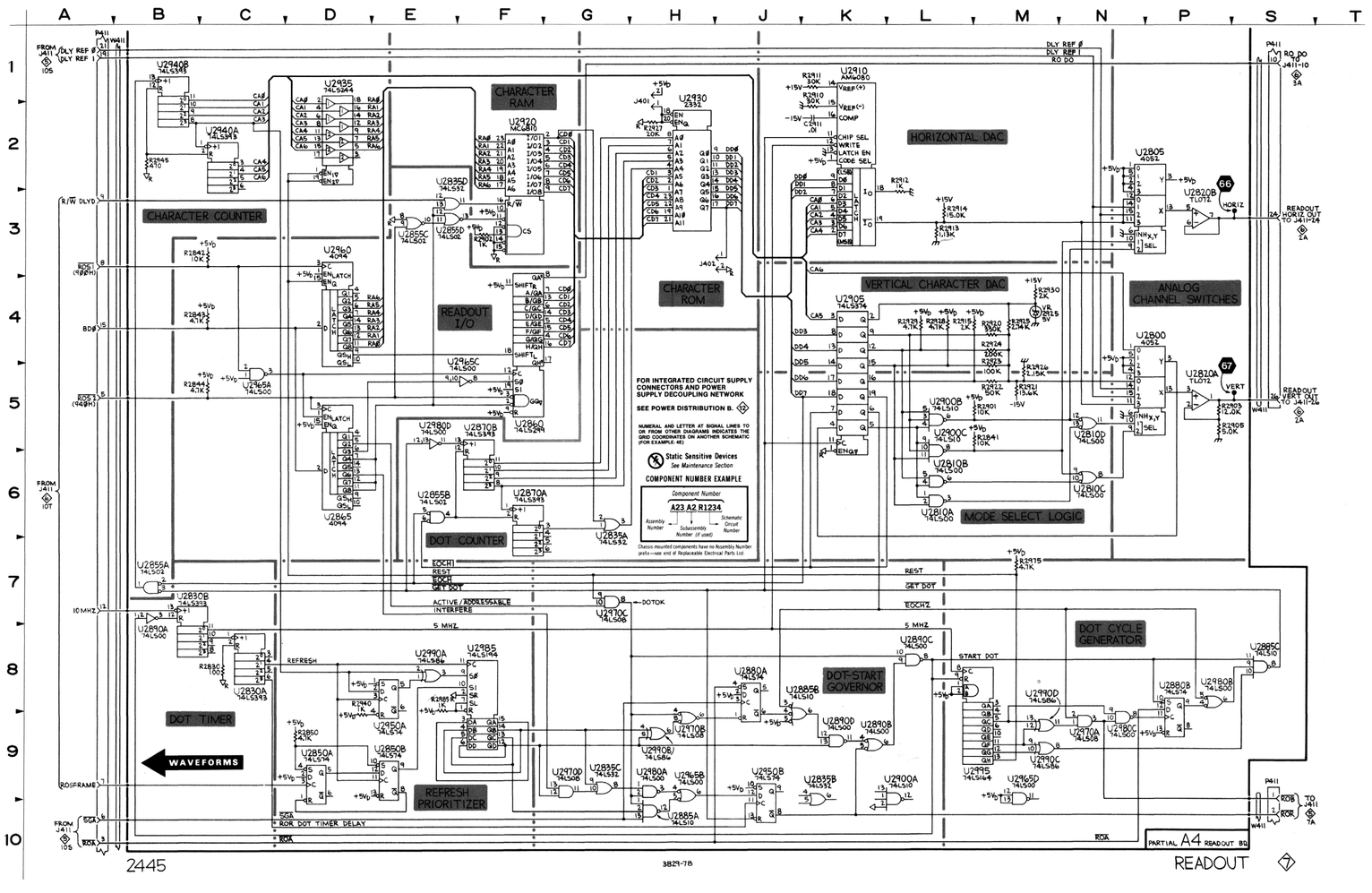


FIG. 9-11
A9—HIGH VOLTAGE BOARD & WAVEFORMS

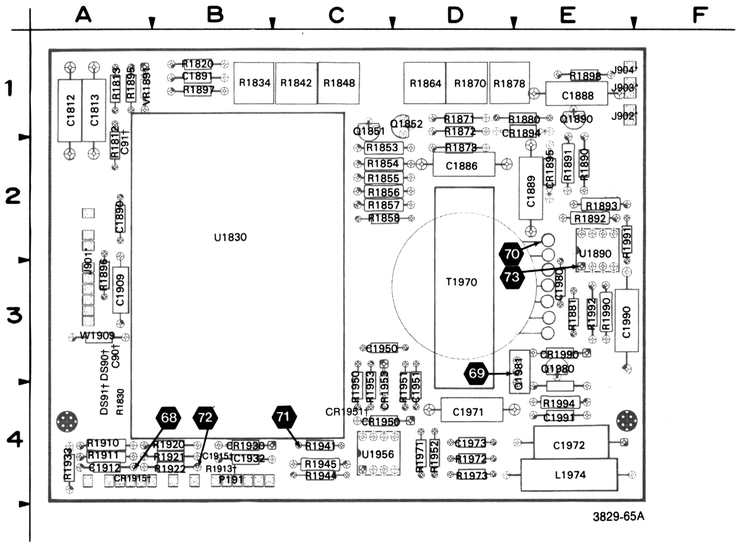


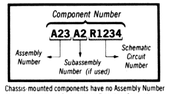
Figure 9-11. A9—High Voltage board.

* LABELED ON SOME BOARDS AS "P" VICE "J".

† INDICATES COMPONENTS THAT WERE MANUALLY ADDED TO THE BOARD AS A RESULT OF MODIFICATION.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

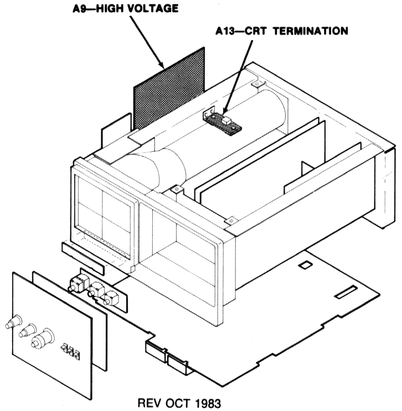
ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

PDA (14KV) . . . post deflection accelerator
VQOUT . . . variable quadrapole out
VZOUT . . . variable Z-axis out

A9—HIGH VOLTAGE BOARD

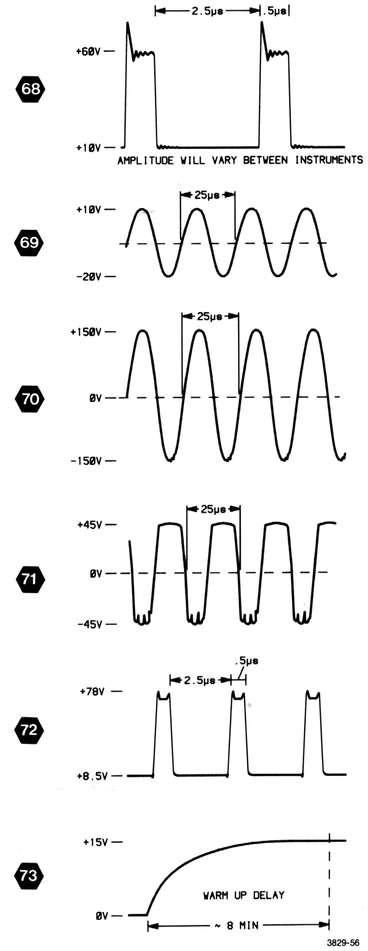
CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C90	8	L1974	8	R1896	8
C91	8	P191	6	R1897	8
C1812	8	P191	8	R1898	8
C1813	8	P191	8	R1910	8
C1886	8	P191	12	R1911	8
C1888	8	Q1851	8	R1913	8
C1889	8	Q1852	8	R1920	8
C1890	8	Q1890	8	R1921	8
C1891	8	Q1980	8	R1922	8
C1909	12	Q1981	8	R1922	8
C1912	8	R1812	8	R1933	12
C1915	8	R1813	8	R1941	8
C1932	8	R1820	6	R1944	8
C1950	8	R1830	8	R1945	8
C1951	8	R1834	6	R1950	8
C1971	8	R1842	6	R1951	8
C1972	8	R1848	8	R1952	8
C1973	8	R1853	8	R1953	8
C1980	8	R1854	8	R1971	8
C1990	8	R1855	8	R1972	8
C1991	8	R1856	8	R1973	8
CR1894	8	R1857	8	R1990	8
CR1895	8	R1858	8	R1991	8
CR1915	8	R1864	8	R1992	8
CR1930	8	R1870	8	R1994	8
CR1950	8	R1871	8	T1970	8
CR1951	8	R1872	8	U1830	8
CR1953	8	R1873	8	U1890	8
CR1990	8	R1878	8	U1890	8
DS90	8	R1880	8	U1890	12
DS91	8	R1881	8	U1956	8
J901	8	R1890	8	U1956	8
J901	8	R1891	8	U1956	12
J901	8	R1892	8	VR1891	8
J902	8	R1893	8	W1909	12
J903	8	R1895	8		
J904	8				



REV OCT 1983

TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the accompanying schematic diagram and board dolly. The waveforms are representative of signals that may be expected at the associated points whenever the instrument is running.



HIGH VOLTAGE SUPPLY AND CRT DIAGRAM 8

ASSEMBLY A1

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C975	3D	7B	J112 J114	3C 2C	7B 8B	J115	4C	8B			

Partial A1 also shown on diagrams 4, 5, 6 and 11.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C90*	9H	3A	CR1990	8E	3E	R1853	4F	2C	R1922	7E	4B
C91	8H	2A				R1854	5F	2C	R1941	7E	4C
C1812	4F	1A	DS90	7H	3A	R1855	4E	2C	R1944	6C	4C
C1813	5F	1A	DS91	8H	4A	R1856	4E	2C	R1945	6D	4C
C1886	8C	2D				R1857	5E	2C	R1950	7C	4C
C1888	3H	1E	J901	3M	3A	R1858	5E	2C	R1951	7A	4D
C1889	8B	2E	J901	4J	3A	R1864	3F	1D	R1952	6B	4D
C1890	5S	2A	J901	5M	3A	R1870	3N	1D	R1953	7C	4C
C1891	3G	1B	J902	2J	1E	R1871	4F	1D	R1971	6B	4D
C1912	6N	4A	J903	4M	1E	R1872	5F	1D	R1972	6C	4D
C1915*	6E	4B	J904	5P	1E	R1873	3F	2D	R1973	6C	4D
C1932	6D	4B				R1878	8D	1D	R1990	3G	3E
C1950	7B	3C	L1974	9A	4E	R1880	4H	1E	R1991	8D	2E
C1951*	7B	4D				R1881	8E	3E	R1992	8E	3E
C1971	8E	4D	P191	2E	4B	R1890	3G	2E	R1994	8E	4E
C1972	8A	4E	P191	7A	4B	R1891	4G	2E			
C1973	6C	4D				R1892	3G	2E	T1970	10B	3D
C1980	8B	3E	Q1851	4F	1C	R1893	3G	2E			
C1990	8D	3E	Q1852	5F	1D	R1895	5S	1A	U1830	8G	2B
C1991	7E	4E	Q1890	3H	1E	R1896	5S	3A	U1890A	8D	2E
CR1894	8C	1E	Q1980	8E	3E	R1897	3H	1B	U1890B	3G	2E
CR1895	8B	2E	Q1981	8B	3E	R1898	4N	1E	U1956A	6C	4C
CR1915*	7E	4B				R1910	6P	4A	U1956B	6B	4C
CR1930	7E	4B	R1812	4F	2A	R1911	6P	4A			
CR1950	7E	4C	R1813	5F	1A	R1913*	7E	4B	VR1891	5S	1A
CR1951	7E	4C	R1830*	9E	4A	R1920	7E	4B			
CR1953	7C	4C	R1848	4N	1C	R1921	6P	4B			

Partial A9 also shown on diagrams 6 and 12.

ASSEMBLY A13

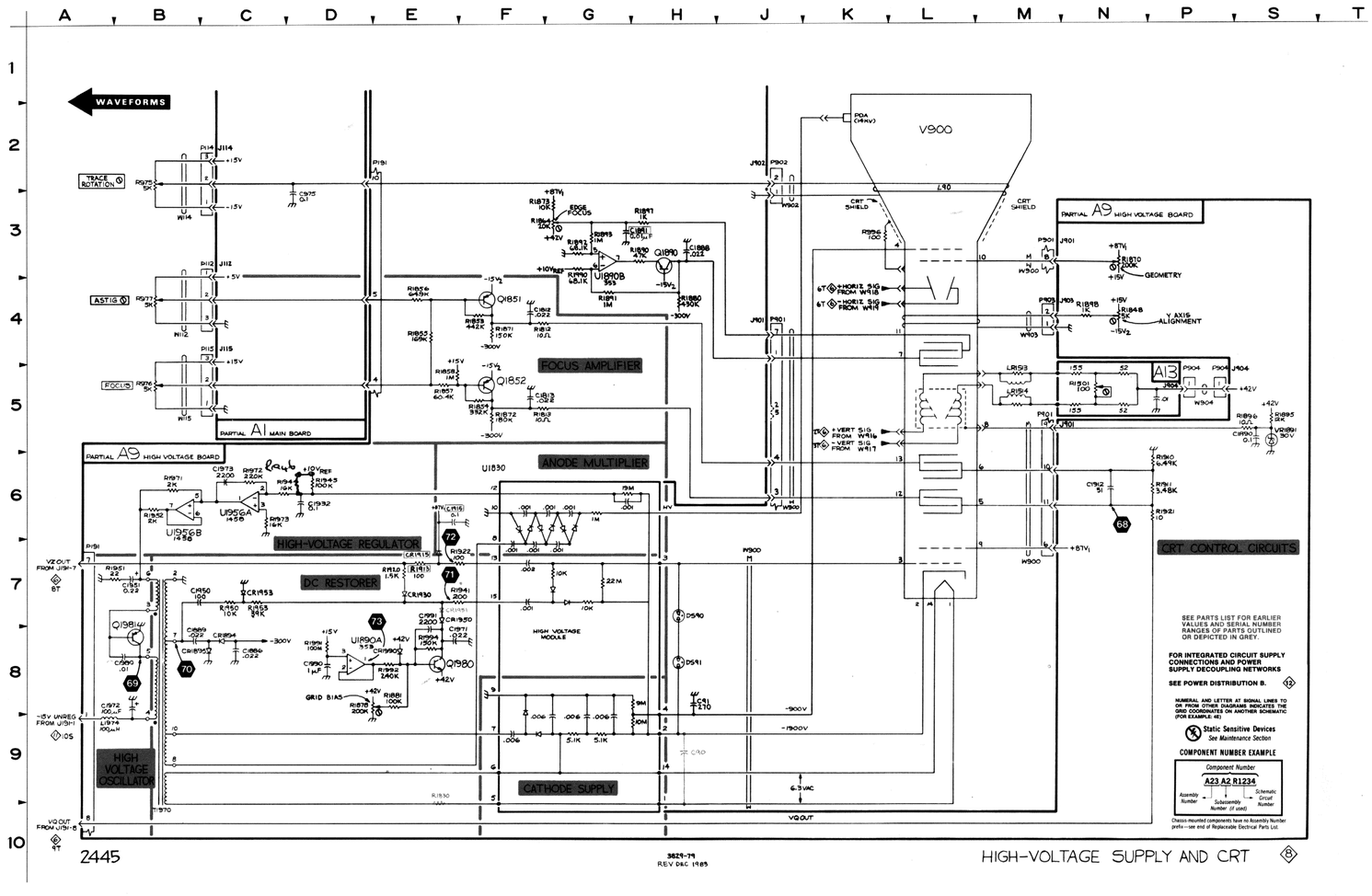
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
J904	5P	**	R1501	5N	**						

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
L90	2L	CHASSIS	P901	3M	CHASSIS	R976	5B	CHASSIS	W115	5B	CHASSIS
			P901	4J	CHASSIS	R977	4B	CHASSIS	W900	3M	CHASSIS
LR1513	5M	CHASSIS	P901	5M	CHASSIS	R996	3K	CHASSIS	W900	6J	CHASSIS
LR1514	5M	CHASSIS	P902	2J	CHASSIS				W900	7J	CHASSIS
			P903	4M	CHASSIS	V900	2L	CHASSIS	W900	7M	CHASSIS
P112	3C	CHASSIS	P904	5P	CHASSIS				W902	3J	CHASSIS
P114	2C	CHASSIS				W112	4B	CHASSIS	W903	4M	CHASSIS
P115	4C	CHASSIS	R975	2B	CHASSIS	W114	3B	CHASSIS	W904	5P	CHASSIS

***See Parts List for serial number ranges.**

**** BOARD ILLUSTRATION NOT SHOWN**



2445

3829-79
REV DEC 1985

HIGH-VOLTAGE SUPPLY AND CRT 8

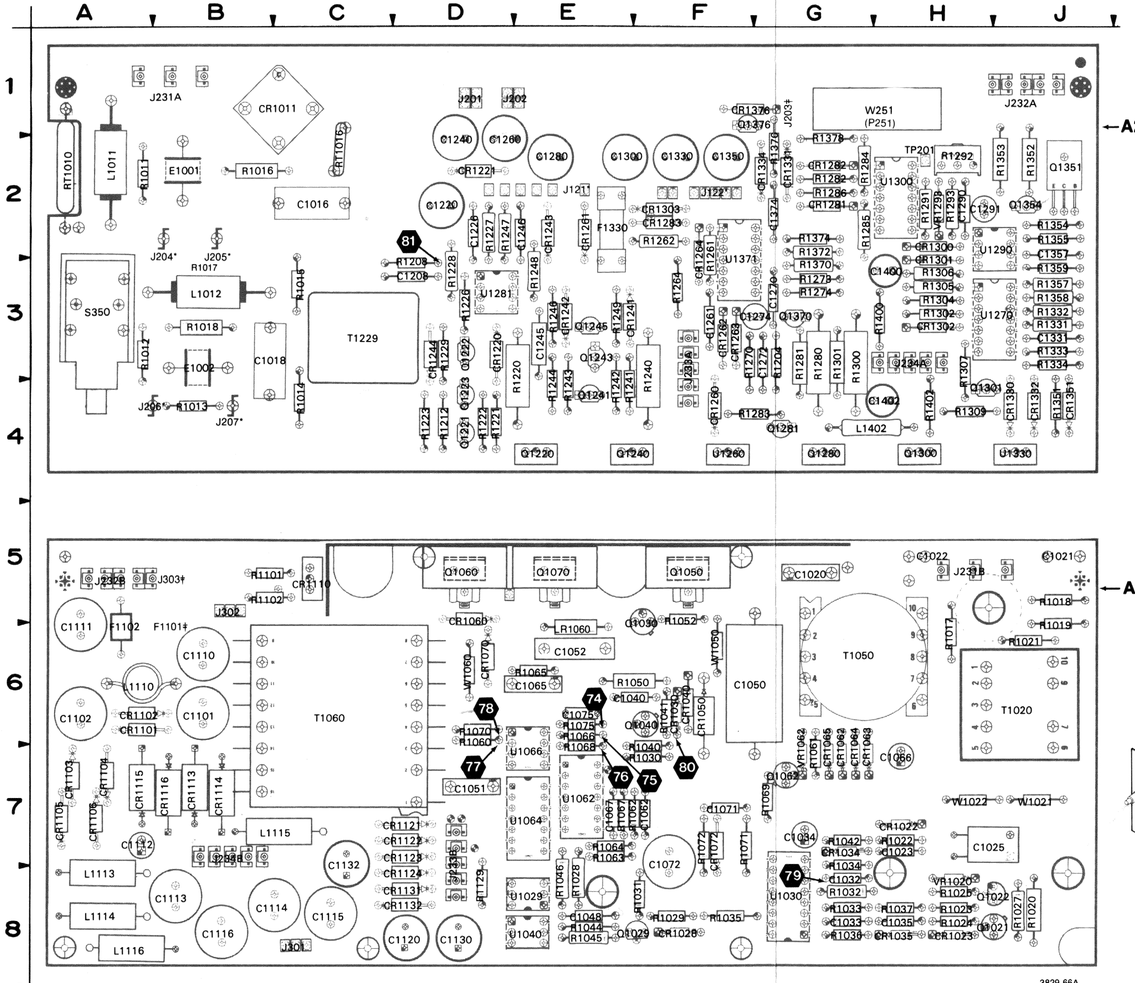


Figure 9-12. A2—Regulator and A3—Inverter boards.

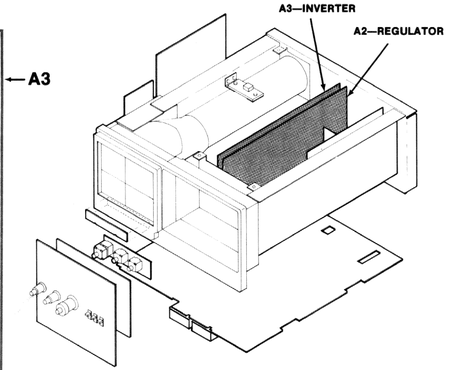
REV DEC 1983

* LABELED ON SOME BOARDS AS "P" VICE "J".

‡ THESE COMPONENTS MAY NOT EXIST IN EARLIER INSTRUMENTS.

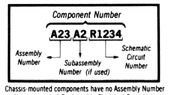
( ) COMPONENTS WITHIN PARENTHESES MAY NOT BE LOCATED PRECISELY AS SHOWN BUT ARE NEAR THEIR INDICATED POSITION.

ALL COMPONENTS MOUNTED ON A3—INVERTER BOARD ARE SHOWN ON SCHEMATIC DIAGRAM 9



Static Sensitive Devices
See Maintenance Section

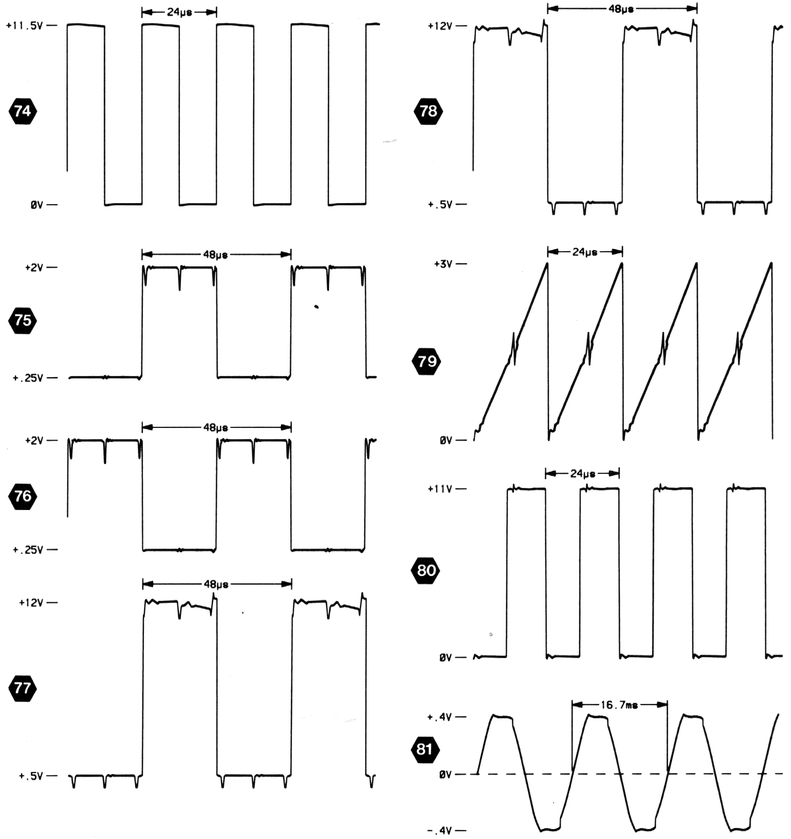
COMPONENT NUMBER EXAMPLE



Chassis-mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

TEST WAVEFORM SETUP INFORMATION

The numbered waveforms below were obtained at the test points indicated on the accompanying schematic diagram and board dolly. The waveforms are representative of signals that may be expected at the associated points whenever the instrument is running.



3829-57

A2—REGULATOR BOARD

CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER	CIRCUIT NUMBER	SCHEM NUMBER
C1016	9	CR1351	10	R1015	9	R1331	10
C1018	9	CR1376	10	R1016	9	R1332	10
C1208	9	E1001	9	R1017	9	R1333	10
C1220	10	E1002	9	R1018	9	R1334	10
C1226	10	F1330	10	R1204	10	R1351	10
C1240	10	J121	10	R1208	9	R1352	10
C1245	10	J122	9	R1212	10	R1353	10
C1246	10	J122	10	R1220	10	R1354	10
C1260	10	J201	10	R1221	10	R1355	10
C1261	10	J202	10	R1222	10	R1357	10
C1270	10	J203	10	R1223	10	R1358	10
C1272	10	J204	9	R1226	10	R1359	10
C1274	10	J205	9	R1227	10	R1370	10
C1280	10	J206	9	R1228	10	R1372	10
C1290	10	J207	9	R1229	10	R1374	10
C1291	10	J231	9	R1240	10	R1376	10
C1300	10	J232	10	R1241	10	R1378	10
C1330	10	J232	10	R1242	10	R1400	10
C1331	10	J233	10	R1243	10	R1402	10
C1350	10	J233	10	R1244	10	RT1010	9
C1357	10	J234	10	R1246	10	RT1016	9
C1374	10	J234	10	R1247	10	S350	9
C1400	10	J234	10	R1248	10	T1229	9
C1402	10	L1011	9	R1249	10	TP201	10
CR1011	9	L1012	9	R1261	10	U1260	10
CR1220	10	L1402	10	R1262	10	U1270	10
CR1221	10	P251	10	R1264	10	U1270	10
CR1241	10	Q1220	10	R1270	10	U1270	10
CR1242	10	Q1221	10	R1273	10	U1270	10
CR1243	10	Q1222	10	R1274	10	U1270	10
CR1244	10	Q1223	10	R1280	10	U1281	10
CR1260	10	Q1240	10	R1281	10	U1281	10
CR1261	10	Q1241	10	R1282	10	U1281	10
CR1262	10	Q1243	10	R1283	10	U1290	10
CR1263	10	Q1245	10	R1284	10	U1300	10
CR1264	10	Q1280	10	R1285	10	U1300	10
CR1281	10	Q1281	10	R1286	10	U1300	10
CR1282	10	Q1300	10	R1291	10	U1300	10
CR1283	10	Q1301	10	R1292	10	U1300	10
CR1300	10	Q1351	10	R1293	10	U1330	10
CR1301	10	Q1354	10	R1300	10	U1371	10
CR1302	10	Q1370	10	R1301	10	U1371	10
CR1303	10	Q1376	10	R1302	10	U1371	10
CR1330	10	R1011	9	R1304	10	U1371	10
CR1331	10	R1012	9	R1305	10	U1371	10
CR1332	10	R1013	9	R1306	10	VR1293	10
CR1334	10	R1014	9	R1307	10	W251	10
				R1309	10		

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

FB . . . feedback
PWM COMPARATOR . . . pulse-width modulator comparator
+5VD . . . +5 V digital

LOW-VOLTAGE POWER SUPPLY DIAGRAM ◈9

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1016	6C	2C	J122	1S	2F	R1011	5B	2A	RT1010	5B	2A
C1018	6B	3B	J204	5B	2B	R1012	6B	3A	RT1016	6C	2C
C1208	1P	3D	J205	6B	2B	R1013	7B	4B			
			J206	6B	4B	R1014	1N	4C	S350	4B	3A
CR1011	5C	1B	J207	7B	4B	R1015	1N	3C			
			J231A	5D	1B	R1016	6C	2B	T1229	1N	3C
E1001	6B	2B				R1017	6A	3B			
E1002	6C	3B	L1011	5B	2A	R1018	6B	3B			
			L1012	6B	3B	R1208	1N	3D			

Partial A2 also shown on diagram 10.

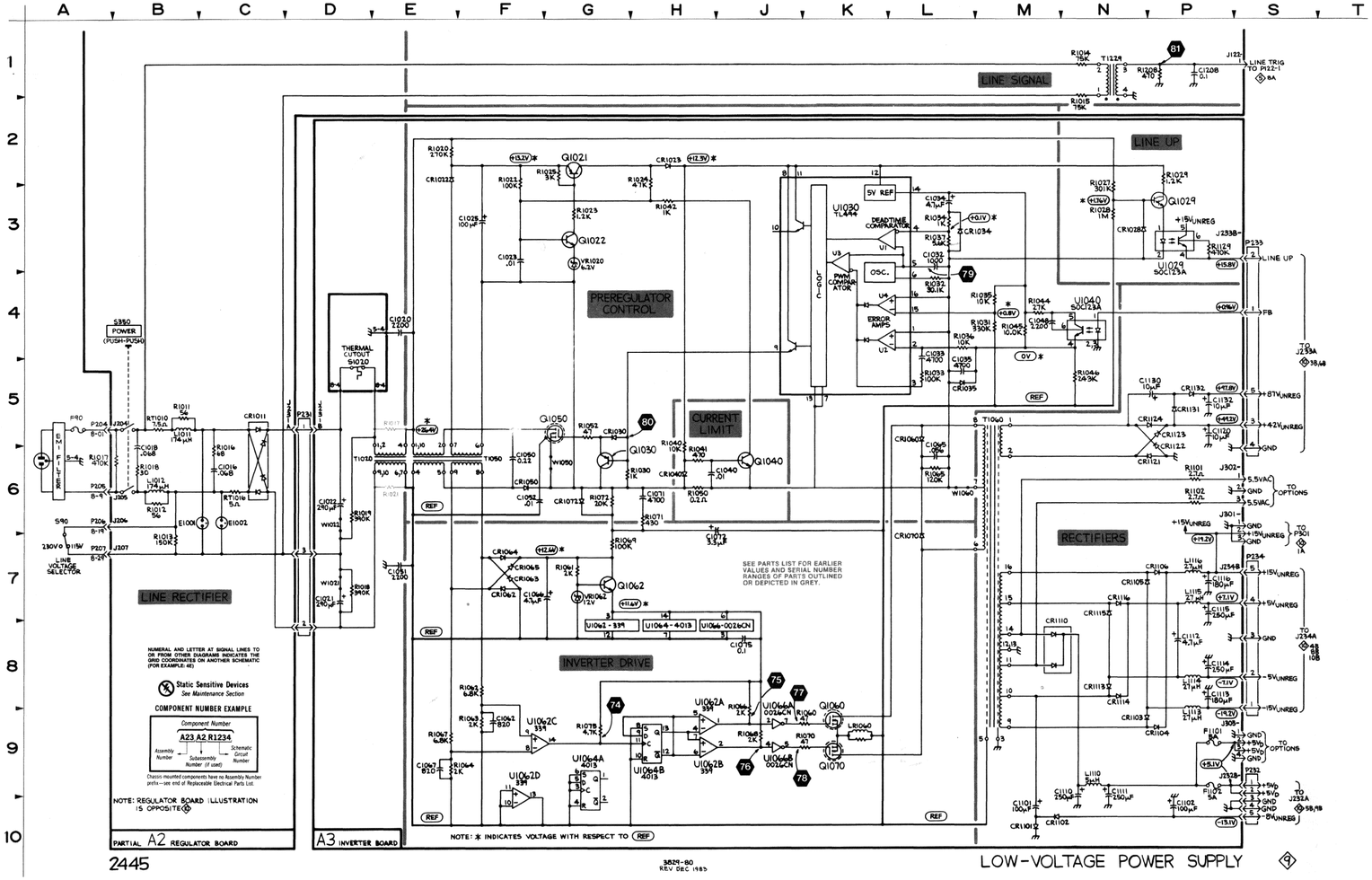
ASSEMBLY A3

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1020	4E	5G	CR1060	5L	5D	Q1021	2G	8J	R1064	9E	7E
C1021	7D	5J	CR1062	7F	7G	Q1022	3G	8J	R1065	6L	6E
C1022	6D	5H	CR1063	7F	7G	Q1029	3P	8F	R1066	8J	6E
C1023	3F	7H	CR1064	7F	7G	Q1030	6H	6F	R1067	9E	7E
C1025	3F	7H	CR1065	7F	7G	Q1040	6J	6F	R1068	9J	6E
C1032	3L	8G	CR1070	7L	6D	Q1050	5G	5F	R1069	7G	7G
C1033	4L	8G	CR1072	6G	7F	Q1060	9K	5D	R1070	9K	6D
C1034	3L	7G	CR1101	10M	6A	Q1062	7G	7G	R1071	6H	7F
C1035	4L	8H	CR1102	10M	6A	Q1070	9K	5E	R1072	6G	7F
C1040	6J	6F	CR1103	9N	7A				R1075	9G	6E
C1048	4M	8E	CR1104	9P	7A	R1017*	5E	6H	R1101	6P	5B
C1050	6F	6F	CR1105	7N	7A	R1018	7D	5J	R1102	6P	5B
C1051	7E	7D	CR1106	7P	7A	R1019	6D	6J	R1129	3P	8D
C1052	6F	6E	CR1110	7M	5C	R1020	2E	8J			
C1062	9F	7F	CR1113	8N	7B	R1021*	6E	6J	LR1060	9K	6E
C1065	5L	6E	CR1114	8N	7B	R1022	2F	7H			
C1066	7F	7H	CR1115	7N	7A	R1023	3G	8H	T1020	6D	6J
C1067	9E	7E	CR1116	7N	7B	R1024	2H	8H	T1050	6F	6G
C1071	6H	7F	CR1121	6P	7D	R1025	2G	8H	T1060	5M	6C
C1072	7H	7F	CR1122	5P	7D	R1027	2N	8J			
C1075	8J	6E	CR1123	5P	7D	R1028	3N	8E	U1029	3P	8E
C1101	10M	6B	CR1124	5P	8D	R1029	2P	8F	U1030	3K	8G
C1102	10P	6A	CR1131	5P	8D	R1030	6H	7F	U1062	8G	7E
C1110	9N	6B	CR1132	5P	8D	R1031	4M	8F	U1040	4N	8E
C1111	9N	6A				R1032	4L	8G	U1062A	8H	7E
C1112	8P	7A	F1101	9P	6B	R1033	5L	8G	U1062B	9H	7E
C1113	8P	8B	F1102	9P	6A	R1034	3L	8G	U1062C	9F	7E
C1114	8P	8C				R1035	4M	8F	U1062D	9F	7E
C1115	7P	8C	J231B	5D	5H	R1036	4L	8G	U1064	8H	7E
C1116	7P	8B	J232B	9P	5A	R1037	3L	8H	U1064A	9G	7E
C1120	5P	8D	J233B	3P	8D	R1040	5H	7F	U1064B	9H	7E
C1130	5P	8D	J234B	7P	7B	R1041	6H	6F	U1066	8J	7E
C1132	5P	8C	J301	6P	8C	R1042	3H	7G	U1066A	8J	7E
			J302	6P	5B	R1044	4M	8E	U1066B	9J	7E
CR1022	2E	7H	J303	9P	5B	R1045	4M	8E			
CR1023	2H	8H				R1046	5N	8E	VR1020	3G	8H
CR1028	3N	8F	L1110	9N	6A	R1050	6H	6F	VR1062	7G	7G
CR1030	5G	6F	L1113	9P	8A	R1052	5G	5F			
CR1034	3L	7G	L1114	8P	8A	R1060	9K	6D	W1021	7D	7J
CR1035	5L	8H	L1115	7P	7C	R1061	7G	7G	W1022	6D	7H
CR1040	6H	6F	L1116	7P	8A	R1062	8F	7E	W1050	6G	6F
CR1050	6F	6F				R1063	9F	7E	W1060	6L	6D

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
F90	5A	CHASSIS	P206	6A	CHASSIS	P233	3S	CHASSIS	S1020	5D	CHASSIS
			P207	7A	CHASSIS	P234	7S	CHASSIS			
P204	5A	CHASSIS	P231	5D	CHASSIS						
P205	6A	CHASSIS	P232	9S	CHASSIS	S90	6A	CHASSIS			

***See Parts List for serial number ranges.**



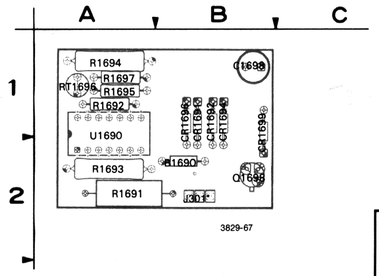


Figure 9-13. A10—Fan Motor board.

Static Sensitive Devices
See Maintenance Section

COMPONENT NUMBER EXAMPLE

Component Number
A23 A2 R1234
Assembly Number
Subassembly Number (if used)
Schematic Circuit Number

Chassis mounted components have no Assembly Number prefix—see end of Replaceable Electrical Parts List.

* LABELED ON SOME BOARDS AS "P" VICE "J".

ALL COMPONENTS MOUNTED ON A10—FAN MOTOR BOARD ARE SHOWN ON SCHEMATIC DIAGRAM 10.

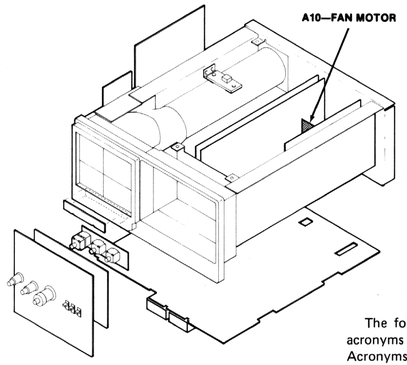


FIG 9-13
A10—FAN MOTOR BOARD

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

FB . . . feedback
+5VD . . . +5 V digital

LOW-VOLTAGE REGULATORS AND FAN DRIVE DIAGRAM 10

ASSEMBLY A2

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1220	2M	2D	CR1351	9H	4J	R1223	1G	4D	R1353	8J	2J
C1226	2F	2D	CR1376	7J	1F	R1226	2F	3D	R1354	8J	2J
C1240	3M	2D				R1227	2G	2D	R1355	8J	2J
C1245	3H	3E	F1330	10F	2E	R1228	2G	3D	R1357	8H	3J
C1246	3H	2E				R1229	1F	3D	R1358	8H	3J
C1260	3M	2D	J121	2P	2E	R1240	2J	3F	R1359	8H	3J
C1261	4J	3F	J122	3P	2F	R1241	2J	4E	R1370	7H	3G
C1270	6C	3G	J201	4P	1D	R1242	2J	4E	R1372	7H	2G
C1272	6B	3G	J202	4P	1D	R1243	2J	4E	R1374	7H	2G
C1274	6B	3F	J203	5P	1G	R1244	2G	4E	R1376	7J	2G
C1280	5M	2E	J232A	5B	1J	R1246	3G	3E	R1378	6K	2G
C1290	5E	2H	J232A	9B	1J	R1247	3H	2D	R1400	4D	3H
C1291	5F	2H	J233A	3B	3F	R1248	3H	3E	R1402	7D	4H
C1300	7M	2E	J233A	6B	3F	R1249	2G	3E			
C1330	9M	2F	J234A	10B	3H	R1261	4K	3F	TP201	5F	2H
C1331	9F	3J	J234A	4B	3H	R1262	4K	2F			
C1350	8M	2F	J234A	8B	3H	R1264	3K	3F	U1260	3J	4F
C1357	8H	2J				R1270	7B	3F	U1270A	6L	3J
C1374	7J	2G	L1402	7D	4H	R1273	6C	3G	U1270B	7L	3J
C1400	5D	3H				R1274	6C	3G	U1270C	9F	3J
C1402	7D	4H	P251	6S	1H	R1280	5M	3G	U1270D	8H	3J
						R1281	5M	3G	U1270	5D	3J
CR1220	2H	3D	Q1220	1H	4E	R1282	5L	2G	U1281A	2F	3D
CR1221	2N	2D	Q1221	1G	4D	R1283	4K	4F	U1281B	3H	3D
CR1241	3J	3E	Q1222	1F	3D	R1284	5L	2G	U1281	5C	3D
CR1242	3H	3E	Q1223	1F	4D	R1285	6L	2G	U1290	5E	2J
CR1243	3N	2E	Q1240	2K	4E	R1286	5L	2G	U1300A	5L	2H
CR1244	2G	3D	Q1241	2J	4E	R1291	5F	2H	U1300B	6L	2H
CR1260	3J	4F	Q1243	2H	3E	R1292	5F	2H	U1300C	5F	2H
CR1261	4N	2E	Q1245	3H	3E	R1293	6F	2H	U1300D	5J	2H
CR1262	3J	3F	Q1280	5M	4G	R1300	7M	3G	U1300	5D	2H
CR1263	4J	3F	Q1281	5L	4G	R1301	7M	3G	U1330	10F	4J
CR1264	4K	3F	Q1300	7M	4H	R1302	7L	3H	U1371A	3J	3F
CR1281	5K	2G	Q1301	7L	4H	R1304	7L	3H	U1371B	4K	3F
CR1282	5K	2G	Q1351	9K	2J	R1305	7L	3H	U1371C	7C	3F
CR1283	5N	2F	Q1354	8J	2J	R1306	6L	3H	U1371D	7J	3F
CR1300	6K	2H	Q1370	7H	3G	R1307	7K	3H	U1371	6D	3F
CR1301	7K	3H	Q1376	7K	1F	R1309	7K	4H			
CR1302	7K	3H				R1331	9G	3J	VR1293	5G	2H
CR1303	7M	2F	R1204	7H	3G	R1332	9G	3J			
CR1330	10F	4J	R1212	1F	4D	R1333	9F	3J	W251	8S	1H
CR1331	9N	2G	R1220	1H	3E	R1334	9F	3J			
CR1332	9F	4J	R1221	1G	4D	R1351	9H	4J			
CR1334	7N	2G	R1222	1G	4D	R1352	8K	2J			

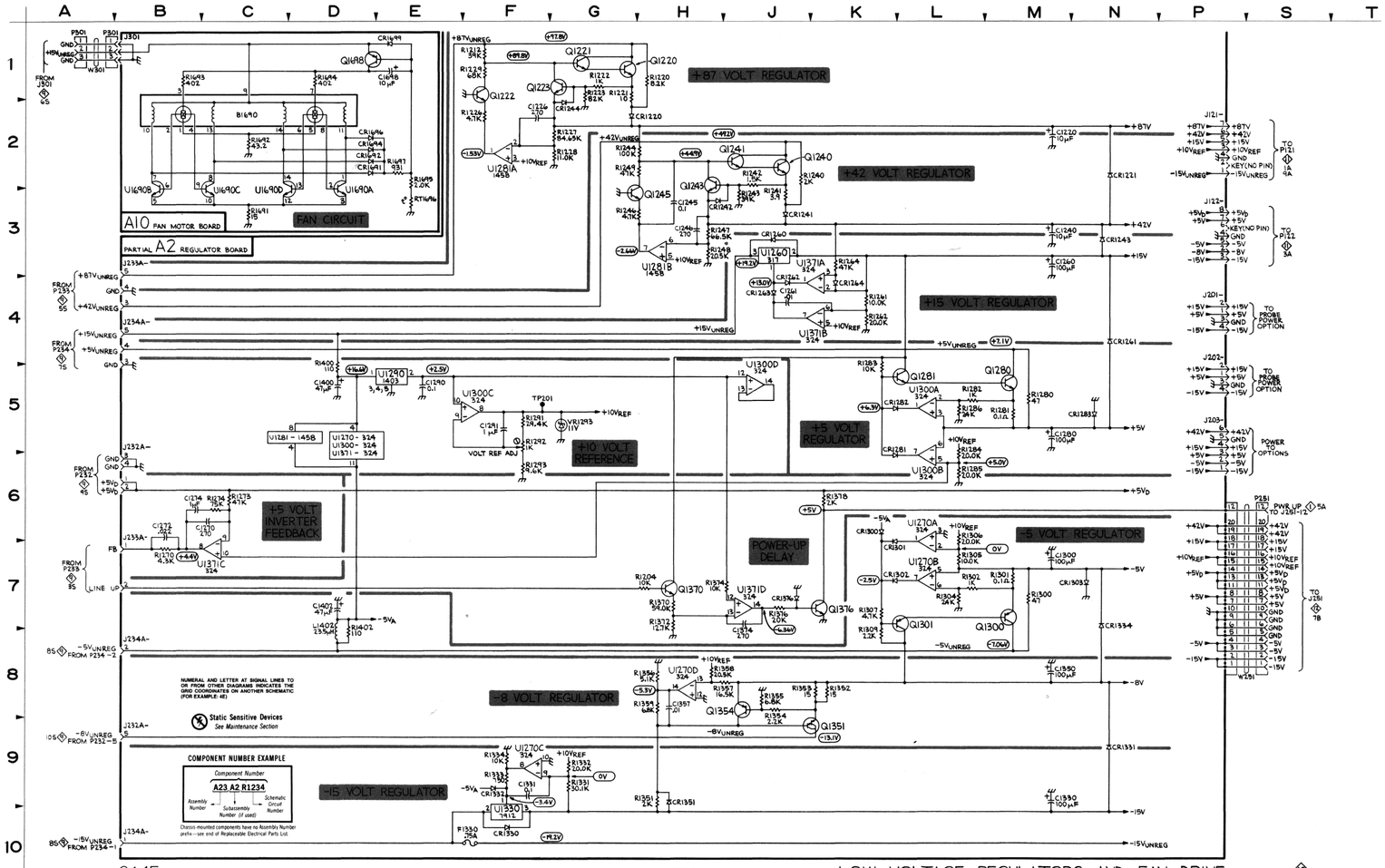
Partial A2 also shown on diagram 9.

ASSEMBLY A10

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
B1690	2C	2B	CR1696	2D	1B	R1691	3C	2A	RT1696	3E	1A
			CR1699	1E	1B	R1692	2C	1A			
C1698	1E	1B				R1693	1B	2A	U1690A	2D	1A
			J301	1B	2B	R1694	1D	1A	U1690B	2B	1A
CR1691	2D	1B	Q1698	1D	2B	R1695	2E	1A	U1690C	2C	1A
CR1692	2D	1B				R1697	2E	1A	U1690D	2C	1A
CR1694	2D	1B									

CHASSIS MOUNTED PARTS

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
W301	1A	CHASSIS	P301	1A	CHASSIS						



POWER DISTRIBUTION A DIAGRAM 11

ASSEMBLY A1

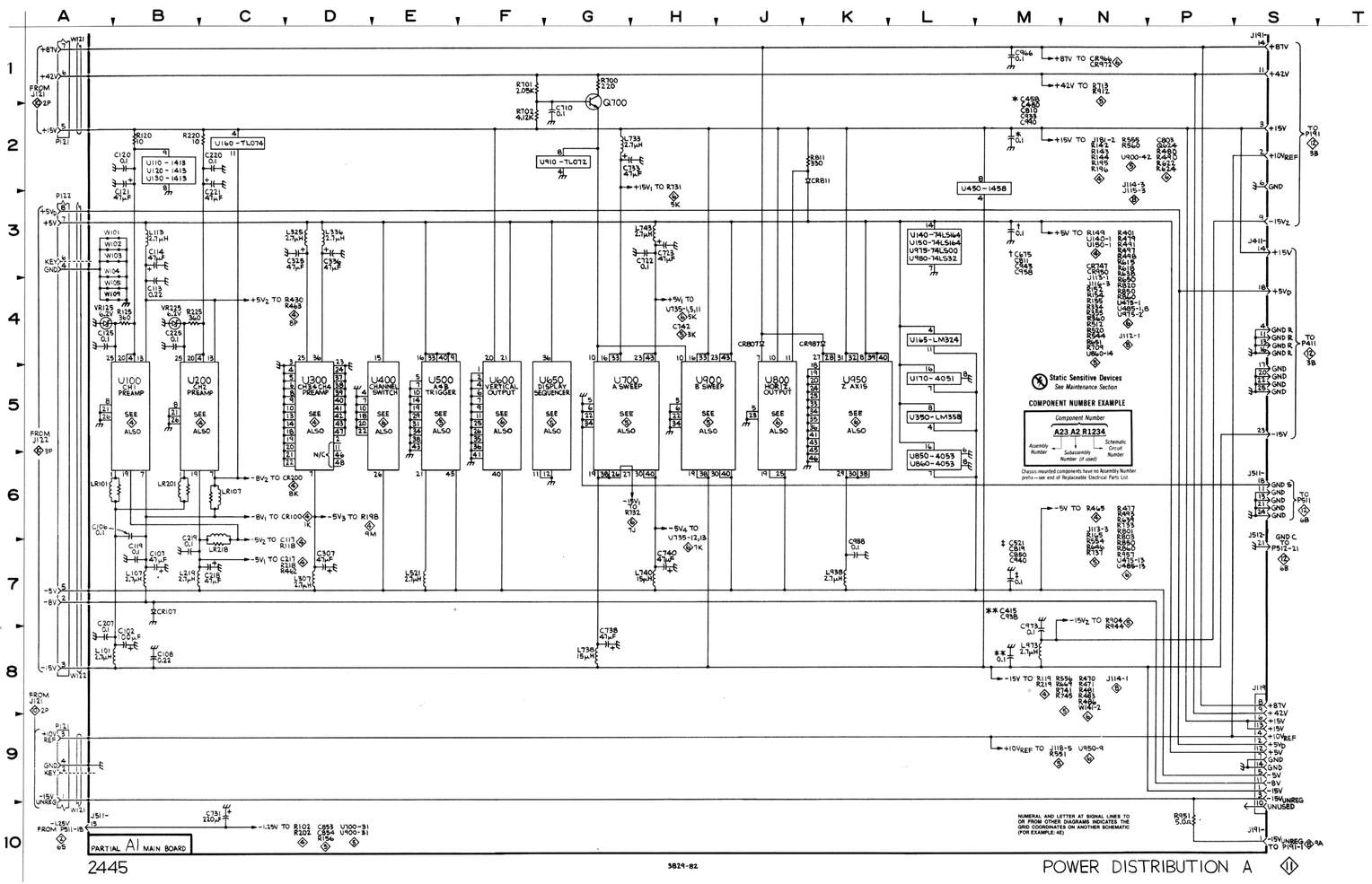
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C102	8B	6D	C850	7M	7F	L740	7H	6D	U170	5L	2E
C106	6A	5D	C933	2M	8G	L743	3H	6D	U200	5C	4D
C107	7B	5D	C938	7M	9G	L938	7K	6J	U300	5D	2B
C108	8B	6D	C940	7M	9H	L973	8M	9K	U350	5L	8B
C113	4B	6D	C943	3M	9H				U400	5E	5E
C114	3B	5D	C958	3M	7K	LR101	6A	5C	U450	2M	3F
C119	7B	5C	C966	1M	9K	LR107	6C	6D	U500	5E	2G
C120	2B	5E	C973	8M	9K	LR201	6B	4C	U600	5F	6H
C121	2B	5E	C988	7K	6K	LR218	7C	3D	U650	5G	3J
C125	4A	5C	C990	2M	8K				U700	5H	7D
C207	8A	4C				P121	2A	4J	U800	5J	7F
C218	7C	3D	CR107	7B	4H	P121	9A	4J	U850	6L	8F
C219	8D	3D	CR807	4J	7F	P122	3A	4H	U860	6L	6F
C220	2C	3D	CR811	2K	7F				U900	5H	8H
C221	2C	3D	CR987	4K	8K	Q700	1G	9C	U910	2G	9F
C225	4B	3C							U950	5K	8K
C307	7D	3B	J119	8S	4H	R120	2B	5E	U975	3L	6K
C325	3D	3C	J191	10S	8K	R125	4B	6D	U980	3L	6K
C336	3D	1C	J191	1S	8K	R220	2B	3C			
C415	7M	4F	J411	3S	1K	R225	4B	3C	VR125	4A	6D
C458	2M	4F	J511	10A	1D	R700	1G	9C	VR225	4B	3C
C480	2M	2J	J511	6S	1D	R701	1F	9C			
C521	7M	2H	J512	6S	1H	R702	2F	9D	W101	3A	9B
C675	3M	3H				R811	2K	7G	W102	3A	4K
C710	1G	9D	L101	8A	6D	R951	10P	9J	W103	3A	7G
C722	3H	6D	L107	7B	6D				W104	3A	3K
C723	3H	6D	L113	3B	6D	U100	5B	5D	W105	4A	5F
C731	10C	8E	L219	7B	3D	U110	2B	6B	W109	4A	9L
C733	2H	7E	L307	7D	3B	U120	2B	6C	W121	10A	4J
C738	8G	6E	L325	3D	3C	U130	2B	6C	W121	1A	4J
C740	7H	6D	L336	3D	1C	U140	3L	7B	W122	8A	4H
C810	2M	7F	L521	7E	2H	U150	3L	7C			
C811	3M	7F	L733	2H	6E	U160	2C	2D			
C819	7M	8E	L738	8G	6E	U165	4L	2F			

Partial A1 also shown on diagrams 4, 5, 6 and 8.

ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

GND C . . . virtual ground "C"
GND R . . . virtual ground "R"
GND S . . . virtual ground "S"
+5VD . . . +5 V digital
+5V1 . . . +5 V decoupled (1)
+5V2 . . . +5 V decoupled (2)
–5V1 . . . –5 V decoupled (1)
–5V2 . . . –5 V decoupled (2)
–5V3 . . . –5 V decoupled (3)
–5V4 . . . –5 V decoupled (4)
–8V1 . . . –8 V decoupled (1)
–8V2 . . . –8 V decoupled (2)
+15V1 . . . +15 V decoupled (1)
–15V2 . . . –15 V decoupled (2)



ACRONYM DICTIONARY

The following listing explains some of the less obvious acronyms and signal labels used on this schematic. Acronyms and labels not shown in this listing may be included in the circuit descriptions (Section 3) and should be obvious if a little thought is given to the intended circuit function.

GND C . . . virtual ground "C"
GND R . . . virtual ground "R"
GND S . . . virtual ground "S"
+5VD . . . +5 V digital
−15V2 . . . −15 V decoupled (2)
+87V1 . . . +87 V decoupled (1)

POWER DISTRIBUTION B DIAGRAM (12)

ASSEMBLY A4

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2830	4C	1C	C2990	4C	3F	U2860	4G	2D	U2960	4G	2E
C2835	4C	2C				U2865	4G	2E	U2965	5H	3E
C2851	4C	1D	P411	3B	1A	U2870	4H	2E	U2970	5H	3E
C2855	4C	2D				U2880	4H	1E	U2980	5H	2E
C2860	4C	2D	R2805	4C	2B	U2885	4H	2F	U2985	4G	3E
C2885	4C	2E				U2890	4H	2E	U2990	5H	3E
C2901	4C	2B	U2800	4D	2B	U2900	5H	2A	U2995	5H	4E
C2913	5B	4B	U2805	4D	2B	U2905	4E	3A			
C2926	4C	3C	U2810	4H	2A	U2910	3D	3A	VR2805	4C	2B
C2940	3B	4C	U2820	3C	2A	U2920	4E	3B			
C2950	4C	4D	U2830	4H	1C	U2930	4F	3D	W411	5B	1A
C2960	4C	2E	U2835	4H	2C	U2935	4G	3C	W2851	4B	1D
C2970	4C	3D	U2850	4H	1D	U2940	5H	4C	W2913	5B	4B
C2980	4C	2F	U2855	4H	2D	U2950	5H	4D			

Partial A4 also shown on diagram 7.

ASSEMBLY A5

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C2041	8C	1C	C2637	7B	3D	U2134	8H	1B	U2496	8G	3J
C2188	8C	1H	C2642	10C	4D	U2162	8F	2J	U2556	8J	3J
C2217	9B	2E	C2734	9C	4F	U2178	8F	1J	U2580	8H	4J
C2218	9B	3D				U2214	9E	2D	U2596	9F	3J
C2221	10C	2C	J251	7B	2D	U2234	8D	2B	U2634	7D	4D
C2223	10B	2C				U2308	9F	2F	U2656	8H	4G
C2240	8C	1A	P511	6B	4C	U2335	8E	3D	U2668	9H	4G
C2328	10C	4E	P512	6B	4H	U2362	8F	3J	U2770	9H	3J
C2346	8C	3D				U2378	8F	2J			
C2354	8B	1C	R2608	6L	3A	U2408	8E	3A	W511	6B	4C
C2440	10C	4E				U2418	8E	3B	W512	7B	4H
C2475	8C	4J	TP508	7L	4K	U2427	7D	3C	W2143	7L	1A
C2485	8C	3K				U2435	7D	3E	W2526	6L	4A
C2527	7C	4D	U2034	8H	2B	U2456	8H	3B			
C2575	8C	4H	U2092	8E	1G	U2468	8J	4J			
C2586	9C	3K	U2108	8H	2G	U2480	8H	4K			

Partial A5 also shown on diagrams 1 and 2.

ASSEMBLY A6

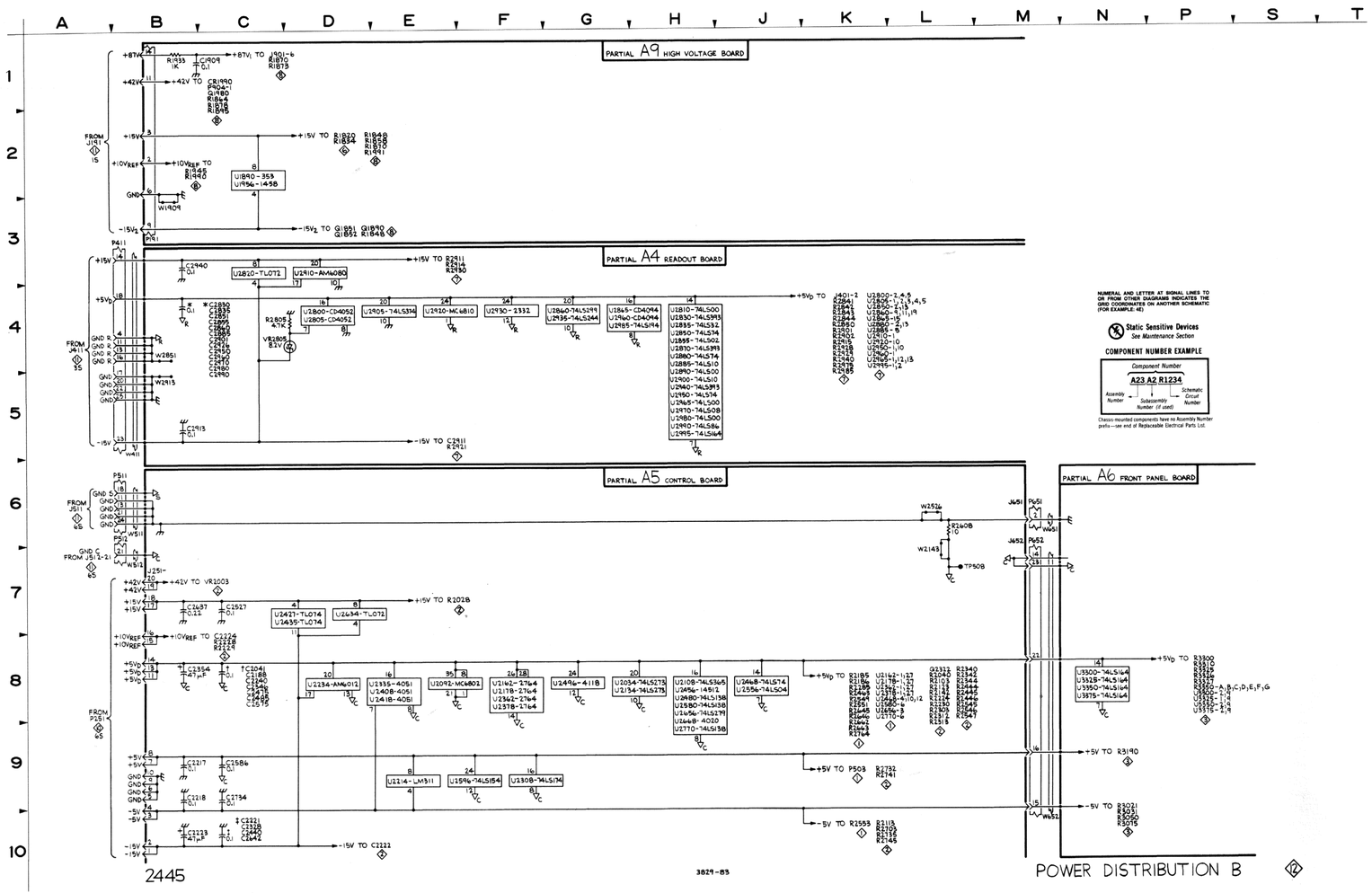
CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
P651	6M	3F	U3300	8N	4B	U3375	8N	3D	W652	10M	2A
P652	6M	2A	U3325	8N	3C						
			U3350	8N	2F	W651	6M	3F			

Partial A6 also shown on diagram 3.

ASSEMBLY A9

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
C1909	1C	3A	R1933	1B	4A	U1956	2C	4C			
P191	3B	4B	U1890	2C	2E	W1909	3B	3A			

Partial A9 also shown on diagrams 6 and 8.


PARTIAL A9 HIGH VOLTAGE BOARD
PARTIAL A4 READOUT BOARD
PARTIAL A5 CONTROL BOARD
PARTIAL A6 FRONT PANEL BOARD
+87V
+42V
+15V
+10V REF
GND
-15V
U1890-353
U1956-1458
U1820-TL072
U2910-AM4080
U2800-CD4052
U2805-CD4052
U2810-74LS00
U2820-74LS32
U2830-74LS393
U2835-74LS32
U2850-74LS74
U2855-74LS02
U2860-74LS74
U2865-74LS10
U2870-74LS00
U2880-74LS393
U2885-74LS10
U2890-74LS00
U2900-74LS10
U2940-74LS393
U2950-74LS74
U2965-74LS00
U2970-74LS08
U2980-74LS00
U2990-74LS86
U2995-74LS64
U2405-74LS534
U2920-MC6810
U2930-2332
U2840-74LS299
U2935-74LS244
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U2940-CD4094
U2985-74LS194
U1810-74LS00
U2845-74LS04
U2855-74LS32
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U2875-74LS08
U2885-74LS10
U2895-74LS00
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U2696-9
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U2408-4051
U2418-4051
U2092-MC6802
U2142-2764
U2178-2764
U2362-2764
U2378-2764
U2496-4118
U2214-LM311
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U2308-74LS174
U3300-74LS164
U3325-74LS164
U3350-74LS164
U3375-74LS164
C1909
C1933
R1933
1K
R1870
R1871
R1872
R1873
R1874
R1875
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R1893
R1894
R1895
R1896
R1897
R1898
R1899
R1900
R1901
R1902
R1903
R1904
R1905
R1906
R1907
R1908
R1909

J110 A1 Test Connector

Pin	Line Name	Schem
1	ATTN CLK	4
2	GND	4
3	CH4 POS	4
4	Unused	4
5	CH1 POS	4
6	GND	4
7	CH3 POS	4
8	CH2 POS	4

J/P/W121 A1 to A2

Pin	Line Name	Schem
1	-15VUNREG	10,11
2	Key [a]	10,11
3	+10VREF	10,11
4	GND	10,11
5	+15V	10,11
6	+42V	10,11
7	+87V	10,11

J/P/W251 A2 to A5

Pin	Line Name	Schem
1	-15V	10,12
2	-15V	10,12
3	-5V	10,12
4	-5V	10,12
5	GND	10,12
6	GND	10,12
7	+5V	10,12
8	+5V	10,12
9	GND	10,12
10	GND	10,12
11	+5VD	10,12
12	PWR UP	1,10
13	+5VD	10,12
14	+5VD	10,12
15	+10VREF	10,12
16	+10VREF	10,12
17	+15V	10,12
18	+15V	10,12
19	+42V	10,12
20	+42V	10,12

J/P/W122 A1 to A2

Pin	Line Name	Schem
1	LINE TRIG	5,9
2	-8V	10,11
3	-15V	10,11
4	GND	10,11
5	-5V	10,11
6	Key [a]	10,11
7	+5V	10,11
8	+5VD	10,11

J/P/W411 A4 to A1

Pin	Line Name	Schem
1	ROB	5,7
2	ROR	5,7
3	ROA	5,7
4	GND R	11,12
5	ROS 2	6,7
6	SGA	5,7
7	ROSFRAME	6,7
8	ROS 1	6,7
9	R/W DLYD	6,7
10	RO DO	6,7
11	GND R	11,12
12	10 MHZ	6,7
13	GND R	11,12
14	+15V	11,12
15	BD0	6,7
16	GND R	11,12
17	GND	11,12
18	+5VD	11,12
19	DLY REF 1	5,7
20	GND	11,12
21	DLY REF 0	5,7
22	GND	11,12
23	-15V	11,12
24	READOUT HORIZ OUT	6,7
25	GND	11,12
26	READOUT VERT OUT	6,7

J/P/W141 A1 to A14

Pin	Line Name	Schem
1	GND	6
2	-15V	6
3	VQOUT	6
4	VERT	6
5	HORIZ	6

J500 A5 to Options

Pin	Line Name	Schem
1	A7	1
2	A15	1
3	A6	1
4	A14	1
5	MR	1
6	A13	1
7	A5	1
8	A12	1
9	A4	1
10	A11	1
11	A3	1
12	A10	1
13	GND C	1
14	A9	1
15	A2	1
16	A8	1
17	A1	1
18	A0	1
19	R/W	1
20	BD7	1
21	GND C	1
22	BD6	1
23	BD3	1
24	BD5	1
25	BD2	1
26	GND C	1
27	BD1	1
28	BD4	1
29	BD0	1
30	E	1
31	GND C	1
32	10MHZ	1
33	VMA	1
34	RESET	1

J502 A5 to Options

Pin	Line Name	Schem
1	OEA35	2
2	OEACLK	2
3	GND C	2
4	OEAI/O	2
5	OEAC2	2
6	OEAC1	2
7	OEAC3	2

J/P/W512 A5 to A1

Pin	Line Name	Schem
1	CONT DATA	2,4
2	ATTN STRB	2,4
3	ATTN CLK	1,4
4	CH2 PA CLK	1,4
5	CH1 PA CLK	1,4
6	A TRIG CLK	1,5
7	B TRIG CLK	1,5
8	A SWP CLK	1,5
9	B SWP CLK	1,5
10	DISP SEQ CLK	1,5
11	RO ON	2,5
12	RO DO	2,6
13	ROS 2	1,6
14	ROS 1	1,6
15	ROSFRAME	1,6
16	DAC MUX1 A0	2,4
17	TSO	2,5
18	DAC MUX1 A1	2,4
19	TRIG STAT STRB	1,5
20	DAC MUX1 A2	2,4
21	GND C	11,12
22	DAC MUX1 INH	1,4
23	R/W DLYD	1,6
24	BD0	1,6
25	5MHZ	1,5
26	10MHZ	1,6

J/P/W652 A6 to A5

Pin	Line Name	Schem
1	ROW 8	2,3
2	ROW 3	2,3
3	ROW 9	2,3
4	ROW 4	2,3
5	ROW 5	2,3
6	ROW 1	2,3
7	Unused	2,3
8	Unused	2,3
9	ROW 0	2,3
10	ROW 7	2,3
11	ROW 10	2,3
12	ROW 2	2,3
13	ROW 6	2,3
14	GND C	12
15	-5V	12
16	+5V	12
17	TRIG LED	2,3
18	COL 0	2,3
19	LED CLK	2,3
20	COL 1	2,3
21	LED DATA	2,3
22	+5VD	12
23	GND C	12
24	COL 2	2,3
25	COL 3	2,3
26	COL 4	2,3

W900 A9 to CRT

Pin	Line Name	Schem
1	HEATER	8
2	CATHODE	8
3	GRID	8
4	SLOT	8
5	Q1+	8
6	Q2+	8
7	Q3-	8
8	PLATE AVERAGE	8
9	FIRST ANODE	8
10	VARIABLE OCTOPOLE	8
11	Q3+	8
12	Q1-	8
13	Q2-	8
14	HEATER	8

J118 A1 Test Connector

Pin	Line Name	Schem
1	Unused	5
2	DLY REF 0	5
3	DLY REF 1	5
4	GND	5
5	+10VREF	5
6	ROR	5
7	Unused	5
8	GND	5

J/P/W511 A5 to A1

Pin	Line Name	Schem
1	CH1 PRB	2,4
2	CH2 OVL	2,4
3	CH4 PRB	2,4
4	CH3 PRB	2,4
5	CH1 OVL	2,4
6	CH2 PRB	2,4
7	CH4 POS	2,4
8	CH3 POS	2,4
9	CH2 POS	2,4
10	CH1 POS	2,4
11	GND	11,12
12	DAC MUX1 IN	2,4
13	GND	11,12
14	TRACE SEP	2,6
15	-1.25V	2,11
16	DLY REF 0	2,5
17	DLY REF 1	2,5
18	GND S	11,12
19	A TIM REF	2,5
20	B TIM REF	2,5
21	GND	11,12
22	HORIZ POS	2,6
23	S1	2,4
24	GND	11,12
25	A TRIG LVL	2,5
26	B TRIG LVL	2,5

J/P/W651 A6 to A5

Pin	Line Name	Schem
1	DAC MUX1 IN	2,3
2	GND	12
3	HORIZ POS	2,3
4	+1.36V	2,3
5	-1.25V	2,3
6	DLY A	2,3
7	ΔA	2,3
8	ΔB	2,3
9	DLY B	2,3
10	HORIZ VAR	2,3
11	TRIG LEVEL	2,3
12	HOLDOFF	2,3
13	-1.25V	2,3
14	TRACE SEP	2,3
15	CH1 VAR	2,3
16	CH2 VAR	2,3
17	CH1 POS	2,3
18	CH2 POS	2,3
19	CH3 POS	2,3
20	CH4 POS	2,3

J/P901 A9 to CRT

Pin	Line Name	Schem
1	Q3-	8
2	Key [b]	8
3	Q1-	8
4	Q2-	8
5	Key [b]	8
6	FIRST ANODE	8
7	Q3+	8
8	VARIABLE OCTOPOLE	8
9	PLATE AVERAGE	8
10	Q2+	8
11	Q1+	8

J119 A1 Test Connector

Pin	Line Name	Schem
1	-15V	11
2	+5VD	11
3	-15VUNREG	11
4	+10VREF	11
5	-5V	11
6	+15V	11
7	GND	11
8	+87V	11
9	+42V	11
10	Unused	11
11	-8V	11
12	+5V	11
13	+15V	11
14	GND	11

J/P191 A1 to A9

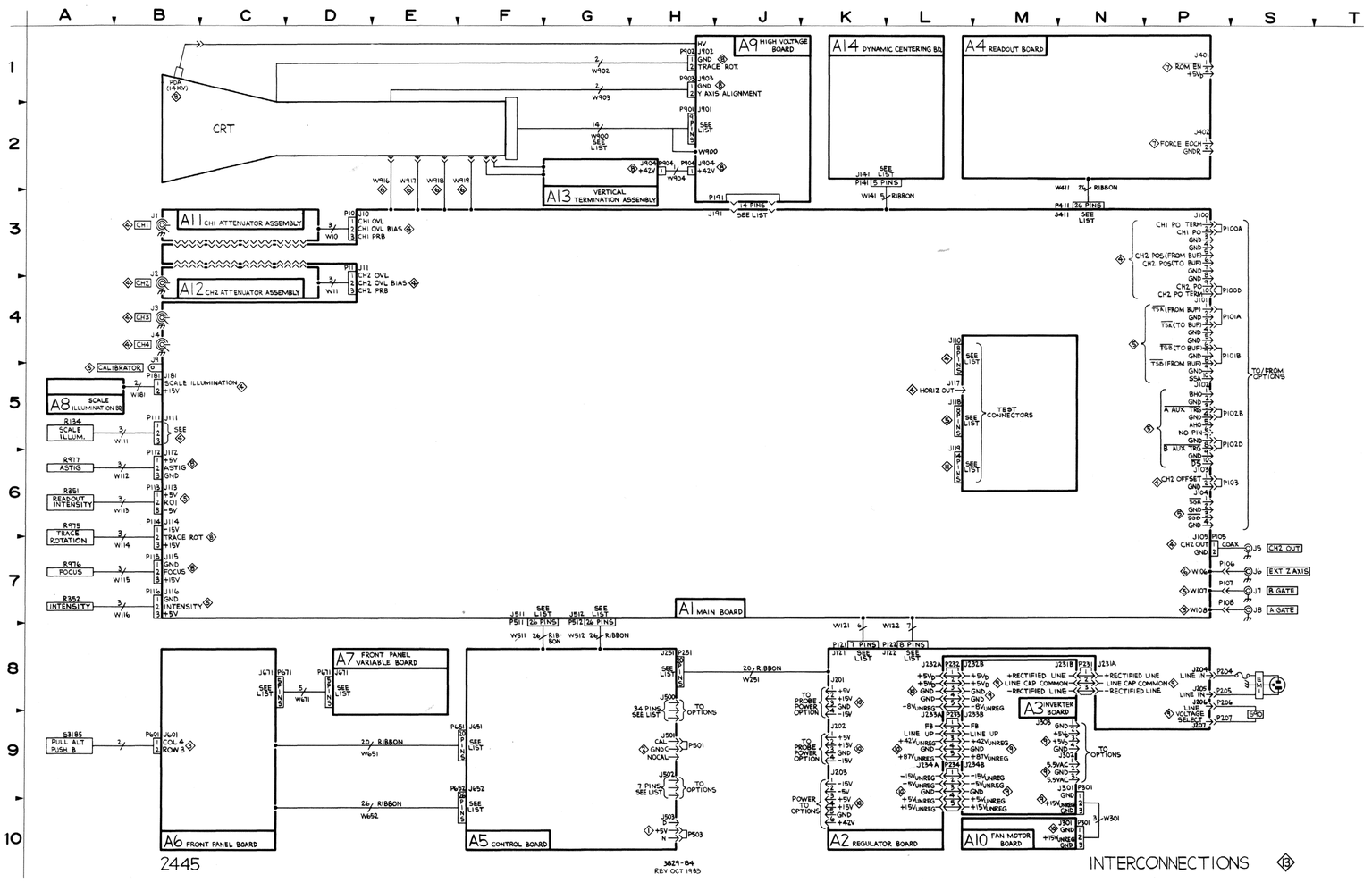
Pin	Line Name	Schem
1	-15VUNREG	8,11
2	+10VREF	11,12
3	+15V	11,12
4	FOCUS	8
5	ASTIG	8
6	GND	11,12
7	VZOUT	6,8
8	VQOUT	6,8
9	-15V2	11,12
10	TRACE ROT	8
11	+42V	11,12
12	TRZ	6
13	QGAIN	6
14	+87V	11,12

J/P/W671 A6 to A7

Pin	Line Name	Schem
1	CH2 VAR	3
2	CH1 VAR	3
3	HORIZ VAR	3
4	-1.25V	3
5	+1.36V	3

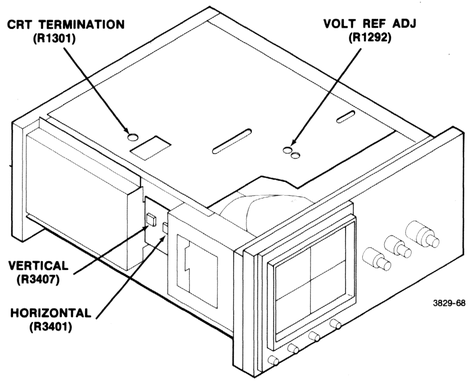
[a] No pins exist in J121-2 and J122-2 positions; no wires exist in W121-2 and W122-2 positions; plugs are installed in P121-2 and P122-2 positions to key the connectors.

[b] No pins exist in J901-2 and -5 positions; plugs are installed infl P901-2 and -5 positions.

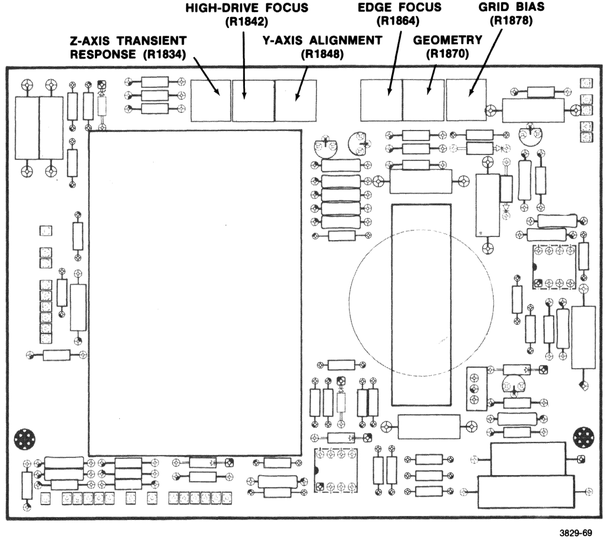

A9 HIGH VOLTAGE BOARD
A14 DYNAMIC CENTERING BD.
A4 READOUT BOARD
CRT
A13 VERTICAL TERMINATION ASSEMBLY
A11 CH1 ATTENUATOR ASSEMBLY
A12 CH2 ATTENUATOR ASSEMBLY
A8 SCALE ILLUMINATION BD.
A7 FRONT PANEL VARIABLE BOARD
A6 FRONT PANEL BOARD
A1 MAIN BOARD
A5 CONTROL BOARD
A2 REGULATOR BOARD
A3 INVERTER BOARD
A10 FAN MOTOR BOARD
TEST CONNECTORS
TO/FROM OPTIONS
INTERCONNECTIONS
2445
3829-84
REV OCT 1983

CHASSIS MOUNTED PARTS

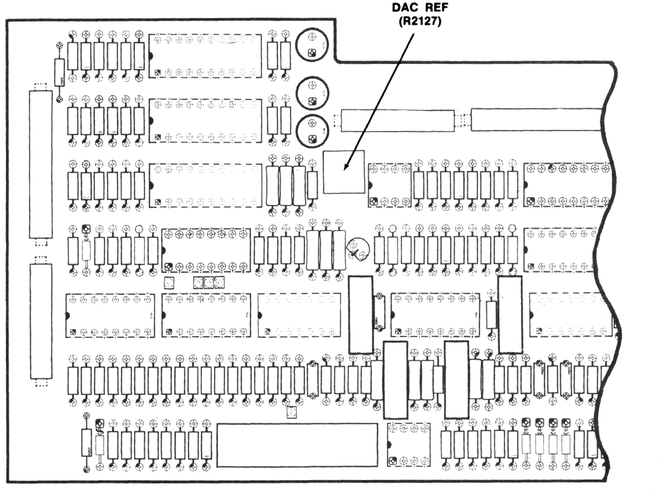
CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	SCHEM LOCATION
F90	9	5A	P904	8	5P
J3	4	10A	R134	4	5N
J4	4	10A	R351	5	5A
J5	4	8T	R352	5	6A
J6	6	9A	R975	8	2B
J7	5	7S	R976	8	5B
J8	5	3S	R977	8	4B
			R996	8	3K
L90	8	2L			
			S90	9	6A
LR1513	8	5M	S1020	9	5D
LR1514	8	5M	S3185	3	5D
P111	4	4N	V900	8	2L
P112	8	3C			
P113	5	5A	W111	4	5N
P114	8	2C	W112	8	4B
P115	8	4C	W113	5	6A
P116	5	6A	W114	8	3B
P204	9	5A	W115	8	5B
P205	9	6A	W116	5	6A
P206	9	6A	W121	10	2S
P207	9	7A	W122	10	3S
P231	9	5D	W122	9	1S
P232	9	8S	W301	10	1A
P233	9	3S	W671	3	8N
P234	9	7S	W900	8	3M
P601	3	5D	W900	8	6J
P671	3	7N	W900	8	7J
P901	8	3M	W900	8	7M
P901	8	4J	W902	8	3J
P901	8	5M	W903	8	4M
P902	8	2J			
P903	8	4M			



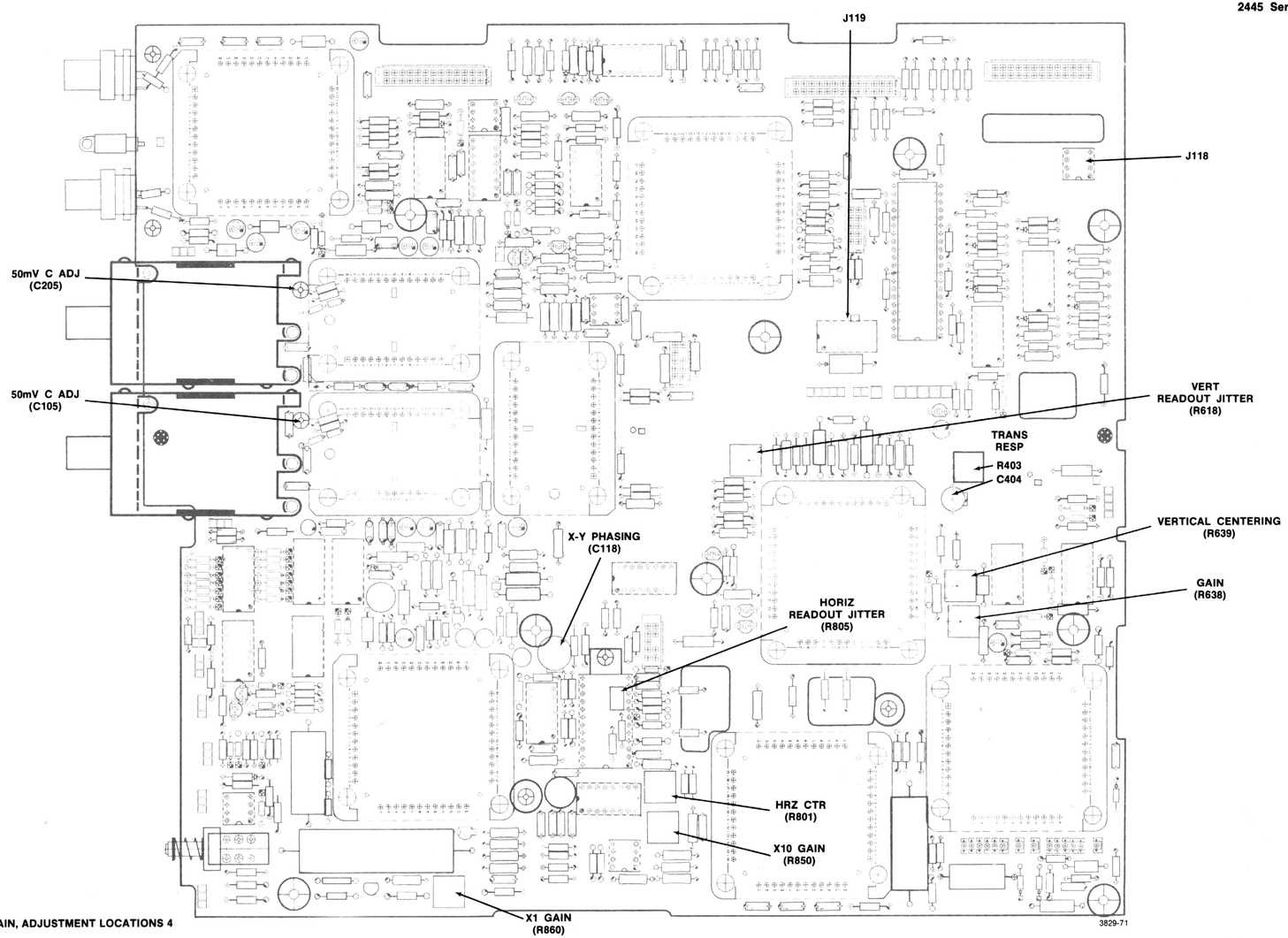
A13—CRT TERMINATION, A14—DYNAMIC CENTERING, ADJUSTMENT LOCATIONS 1



A9—HIGH VOLTAGE, ADJUSTMENT LOCATIONS 2

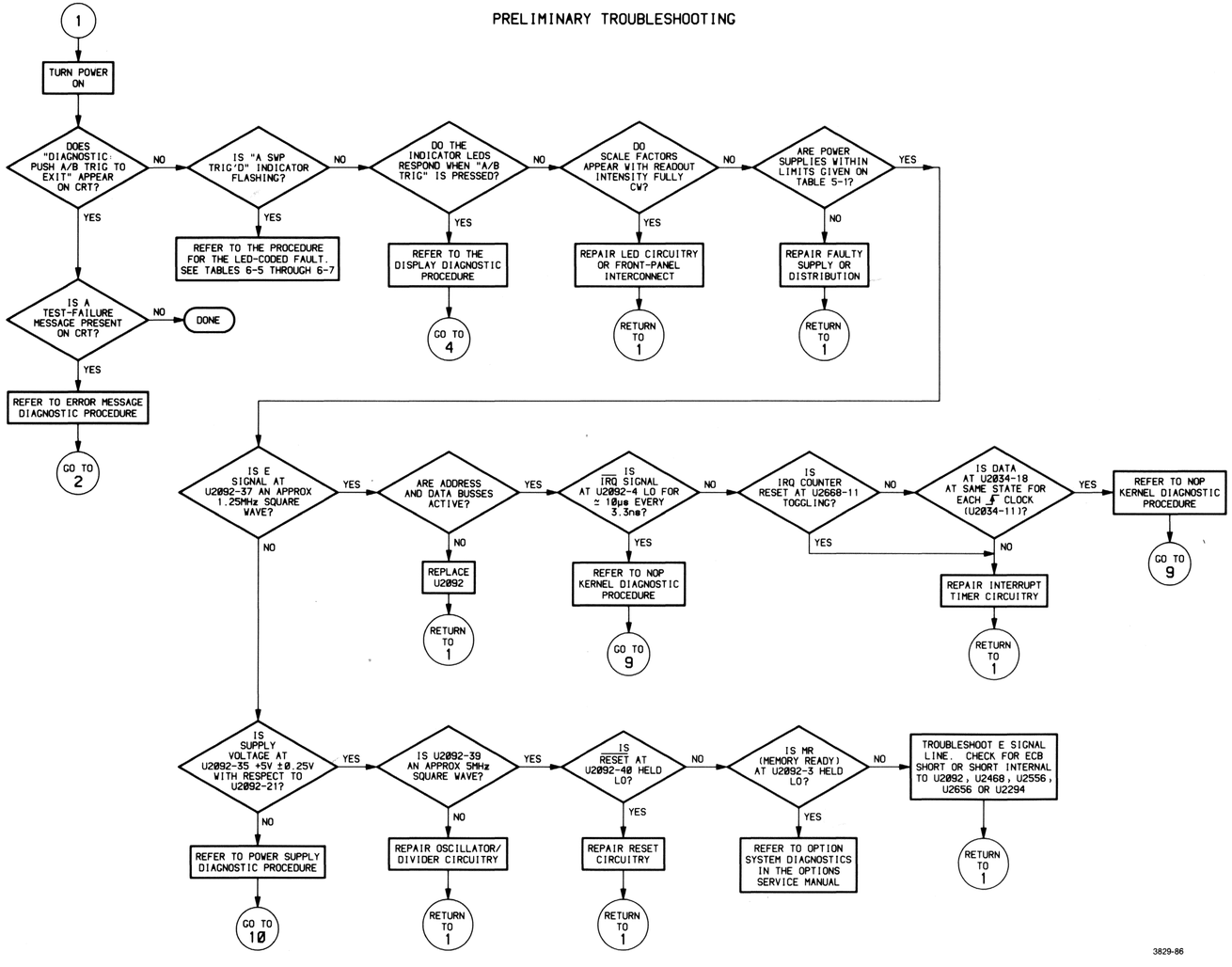


A5—CONTROL, ADJUSTMENT LOCATIONS 3



A1—MAIN, ADJUSTMENT LOCATIONS 4

PRELIMINARY TROUBLESHOOTING

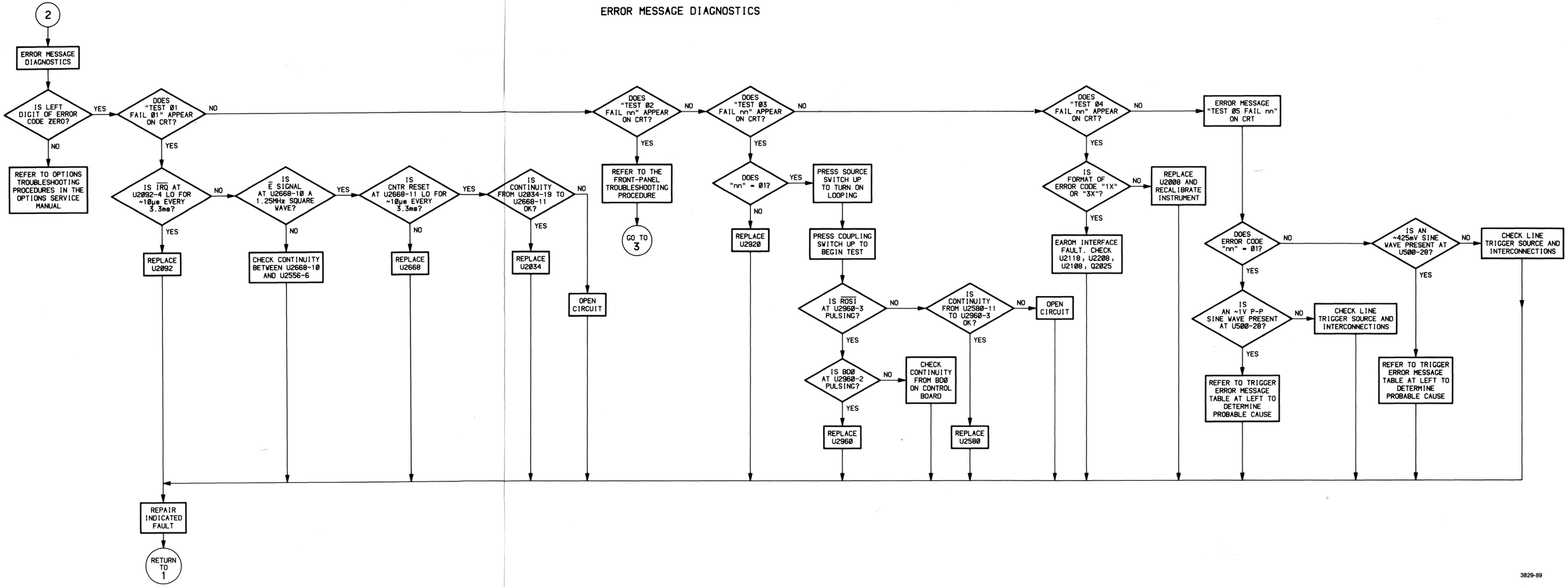


3829-86

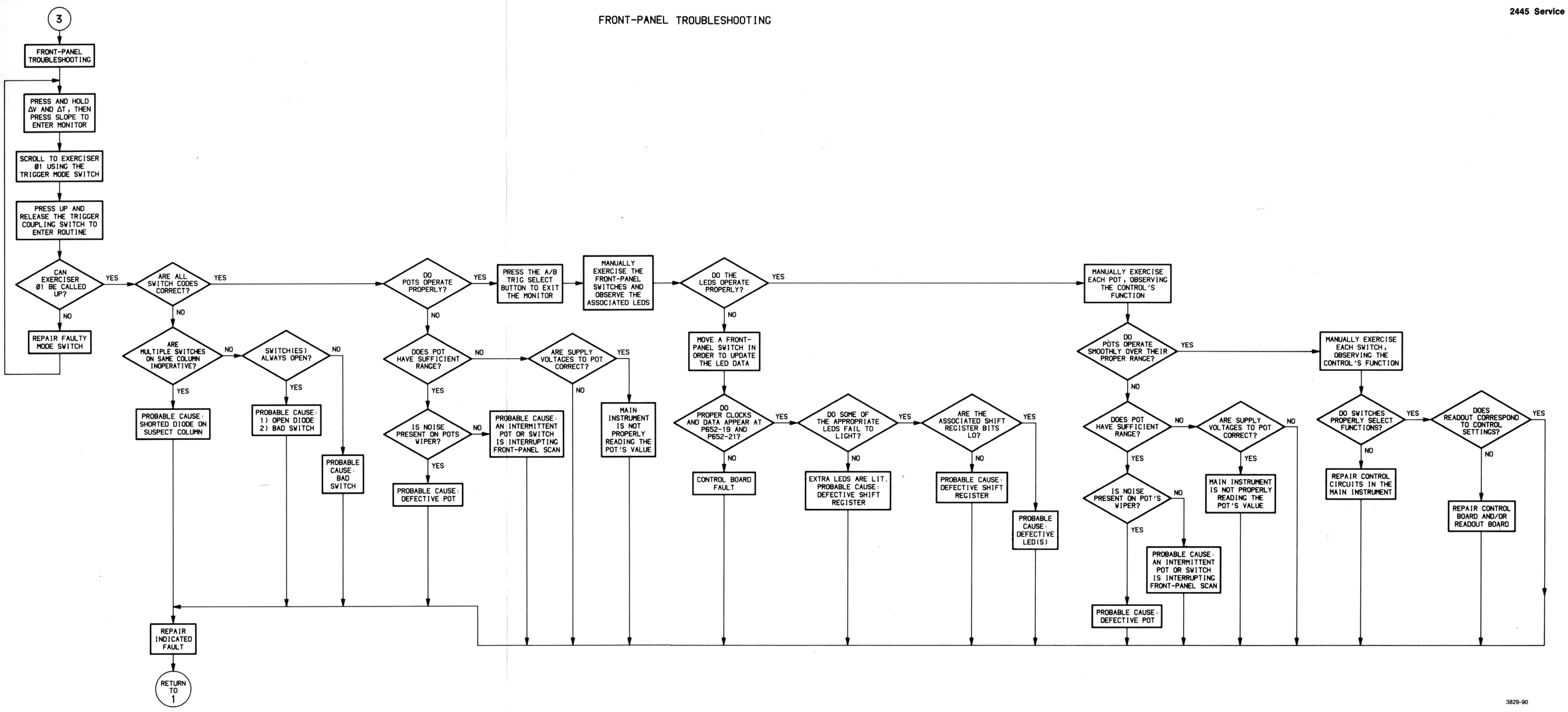
Probable Causes of Trigger Error Messages

Test 05 Fail	Probable Causes of Failure
01	a. Line Signal b. U500 (Trigger) c. U650 (Trigger Status Data to Processor)
02 or 22	a. Line Signal b. U500 (Trigger)
04 or 44	a. U2634A, U2235, or U500 b. Line Signal

ERROR MESSAGE DIAGNOSTICS



FRONT-PANEL TROUBLESHOOTING



3829-90

VERTICAL TROUBLESHOOTING HINTS

With no signals connected to the four Vertical input connectors, select each channel for display and rotate its POSITION control through its entire range.

1. If one or more of the four Vertical channels properly responds to its POSITION control, the problem is in the preamp circuit of the defective channel or in the Vertical Channel Switch circuit. If none of them respond properly, the Channel Switch, Delay Line, Vertical Output Amplifier, and the hybrid power supplies should be suspect.

2. Check the range of the input positioning voltage for a faulty channel. Channel 1 and 2 positioning inputs (pin 17 of U100 and U200) should vary between −4.6 volts and −5.26 volts. Channel 3 and 4 positioning voltages (to pins 29 and 32 of U300) should vary between ground potential and −5 volts.

3. If the faulty channel's input positioning range is okay, check the positioning effect at the outputs of the Channel Switch (connect a DMM across the Delay Line). When the CH 1 or CH 2 POSITION control is rotated through its range, the DMM reading should vary from approximately +700 mV to −700 mV; for Channels 3 and 4, it should vary approximately from +350 mV to −350 mV.

4. If the range at the Delay Line is okay, connect the DMM across the vertical outputs to the crt (between L628 and L633). Range should vary approximately from +11.5 volts to −11.5 volts as the POSITION control of the displayed channel is rotated through its range.

5. If the output voltages to the crt are okay, check that the voltage between the crt termination resistors (CR1513 and CR1514) varies approximately from +11.5 volts to −11.5 volts as the POSITION control is rotated through its range.

See the "Theory of Operation" for further information.

HORIZONTAL TROUBLESHOOTING HINTS

If possible, set the 2445's TRIGGER controls so the TRIG'D LED remains illuminated (triggered sweep is running). Setting the TRIGGER MODE to AUTO LVL will usually do this.

1. Check that the horizontal positioning input (pin 22 of U800) of the Horizontal Output IC varies approximately from −1.25 volts to +1.25 volts as the Horizontal POSITION control is rotated through its range. If it does not, repair the position circuit.

2. Check that the A Sweep Ramp at pin 18 of U800 is ramping from −1.25 volts to +1.25 volts. If it is not, check the buffer amplifier made up of U735 and its associated components. When operating properly, the voltages and waveforms at pins 3 and 9 of U735 will be nearly identical.

3. Check for proper select signals (TTL levels) at the $\overline{HSA}$ and $\overline{HSB}$ inputs of U800.

4. Check the power supply levels to U800.

5. Check the voltage on pin 6 of U800. If it is not > +80 volts, check the +OUT and −OUT pins for shorts.

See the "Theory of Operation" for further information.

HOW TO VERIFY THE CONTROL DATA AND CONTROL CLOCK LINES

1. Power up the 2445 under test.

2. Move the NORM/DIAG jumper (P503 on the scope under test) to the DIAG position. This forces the processor into a NOP loop and exercies the Address Decode circuitry.

3. Trigger the test scope on the DAC MSB CLK at pin 14 of U2580 (on the Control Board). Use NORM TRIGGER and – SLOPE. Set TRIGGER LEVEL to +1.4 volts.

4. Verify that four bursts of clocks appear at 104-ms to 106-ms intervals.

5. Check that each of the outputs of U2850 has similar signals present (diagram 2).

6. Check that each output of U2596 (diagram 2) has four bursts of two pulses each occurring at 104-ms to 106-ms intervals.

7. Turn instrument power off and restore P503 to the NORM position.

8. Power up the 2445 again.

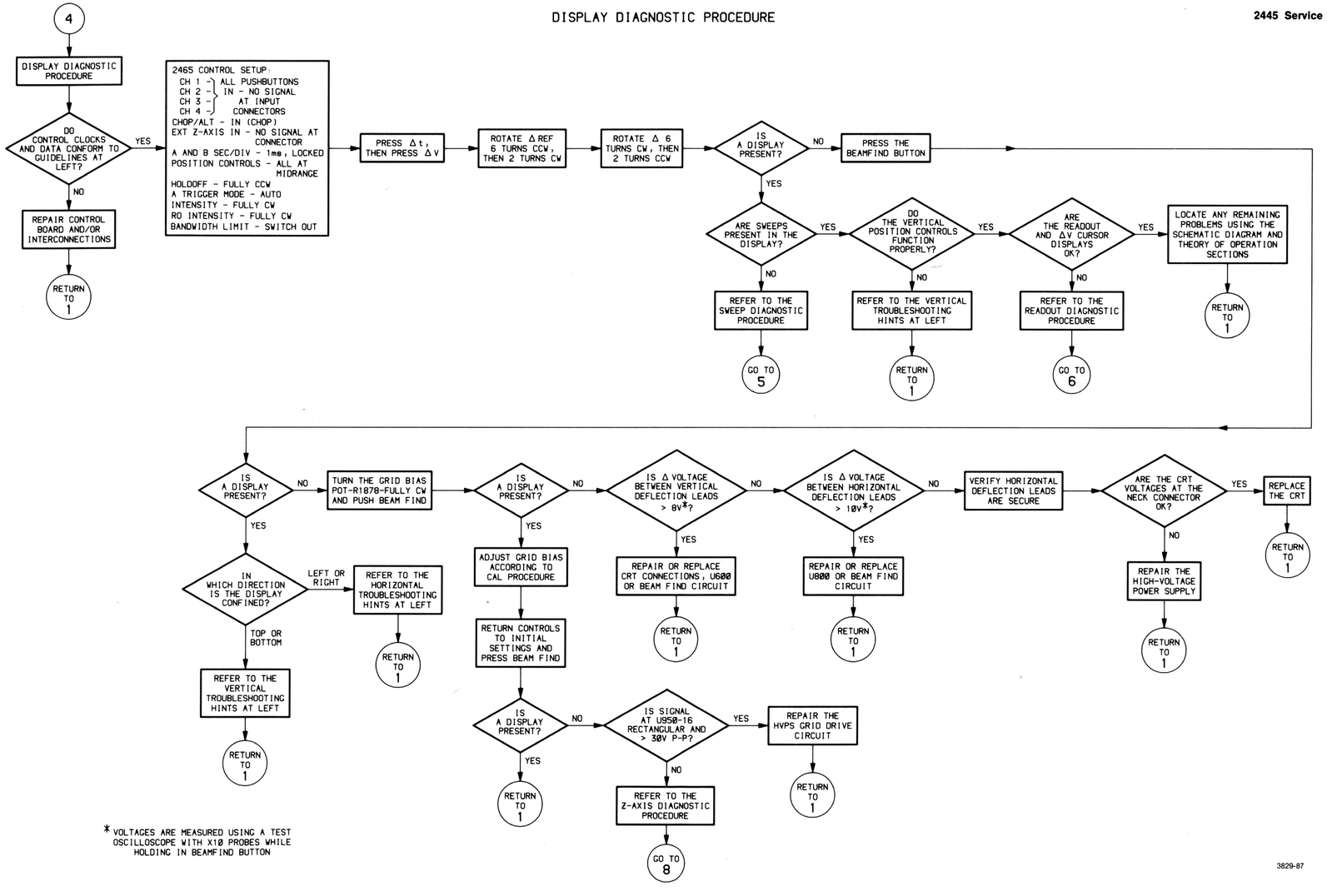
9. Set the 2445's CH 1 and CH 2 input coupling to 1 MΩ DC and TRIGGER MODE to NORM.

10. Lock the TRIGGER COUPLING switch in its up position, using a rubber band looped between the TRIGGER LEVEL control and the switch's lever actuator.

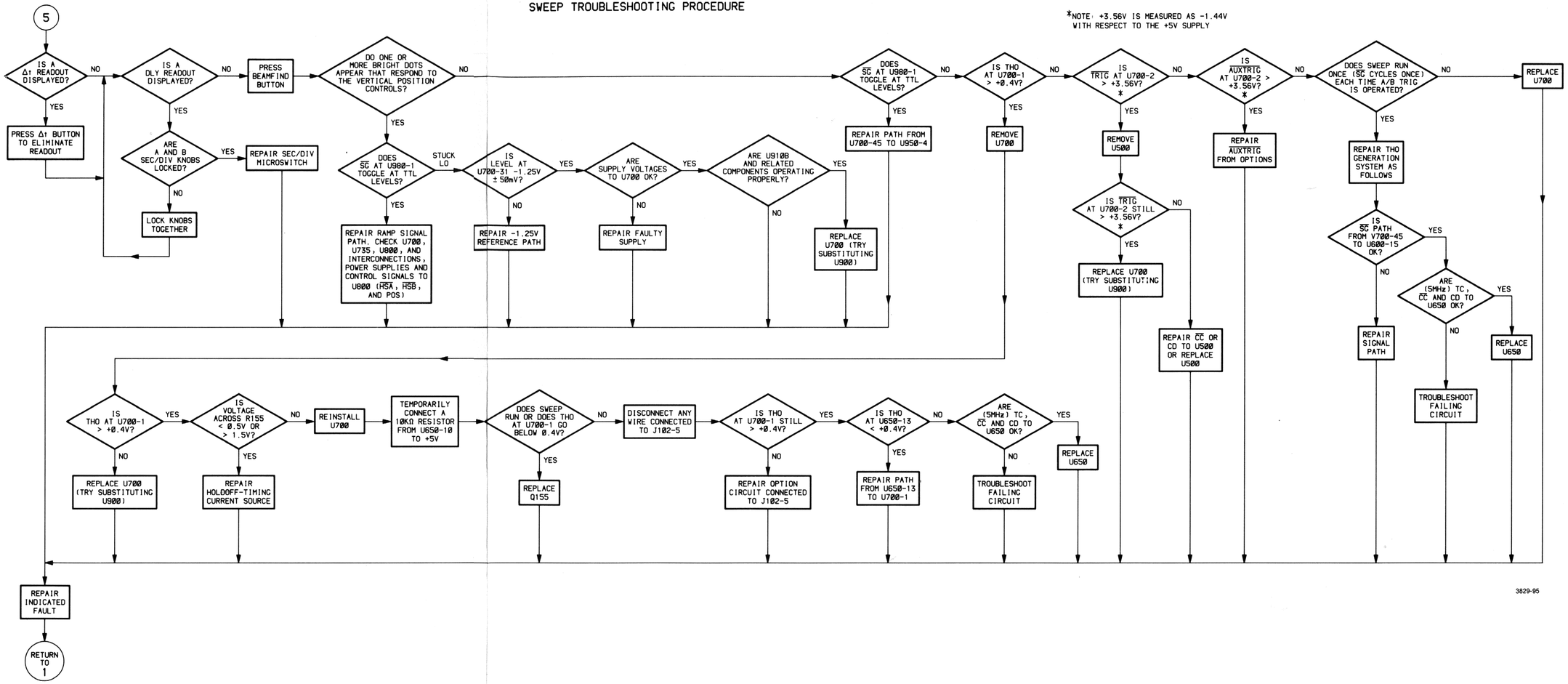
11. Trigger the test oscilloscope on the DISP SEQ CLK (pin 8 of U2596 or pin 10 of P512).

12. With the test scope still triggered on the DISP SEQ CLK, verify that the ATTN STRB at pin 2 of P512 is eight positive-going strobes.

13. Verify that the control data on pin 1 of P512 is toggling at TTL levels.

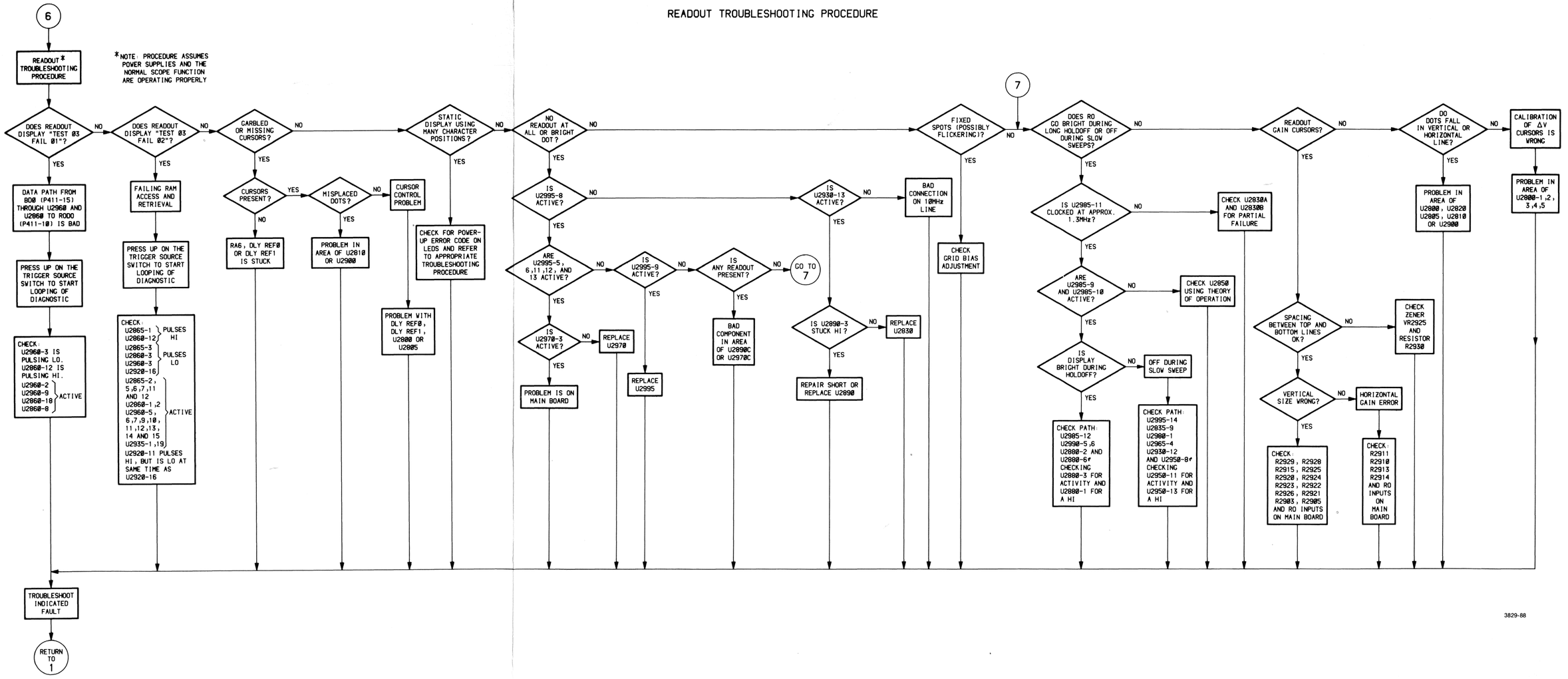


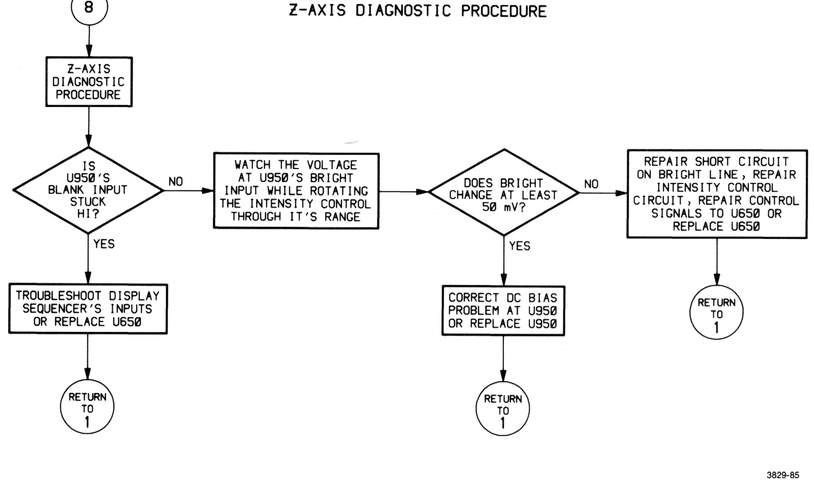
SWEEP TROUBLESHOOTING PROCEDURE



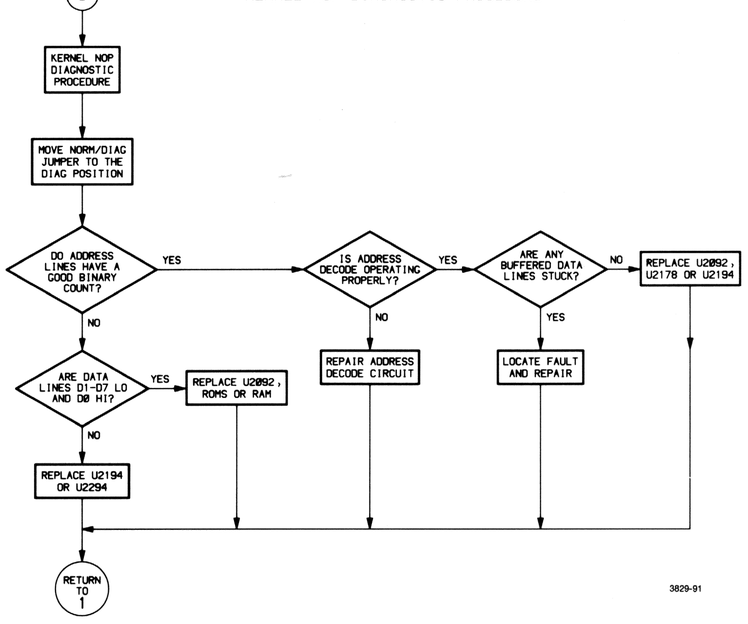
*NOTE: +3.56V IS MEASURED AS -1.44V WITH RESPECT TO THE +5V SUPPLY

READOUT TROUBLESHOOTING PROCEDURE



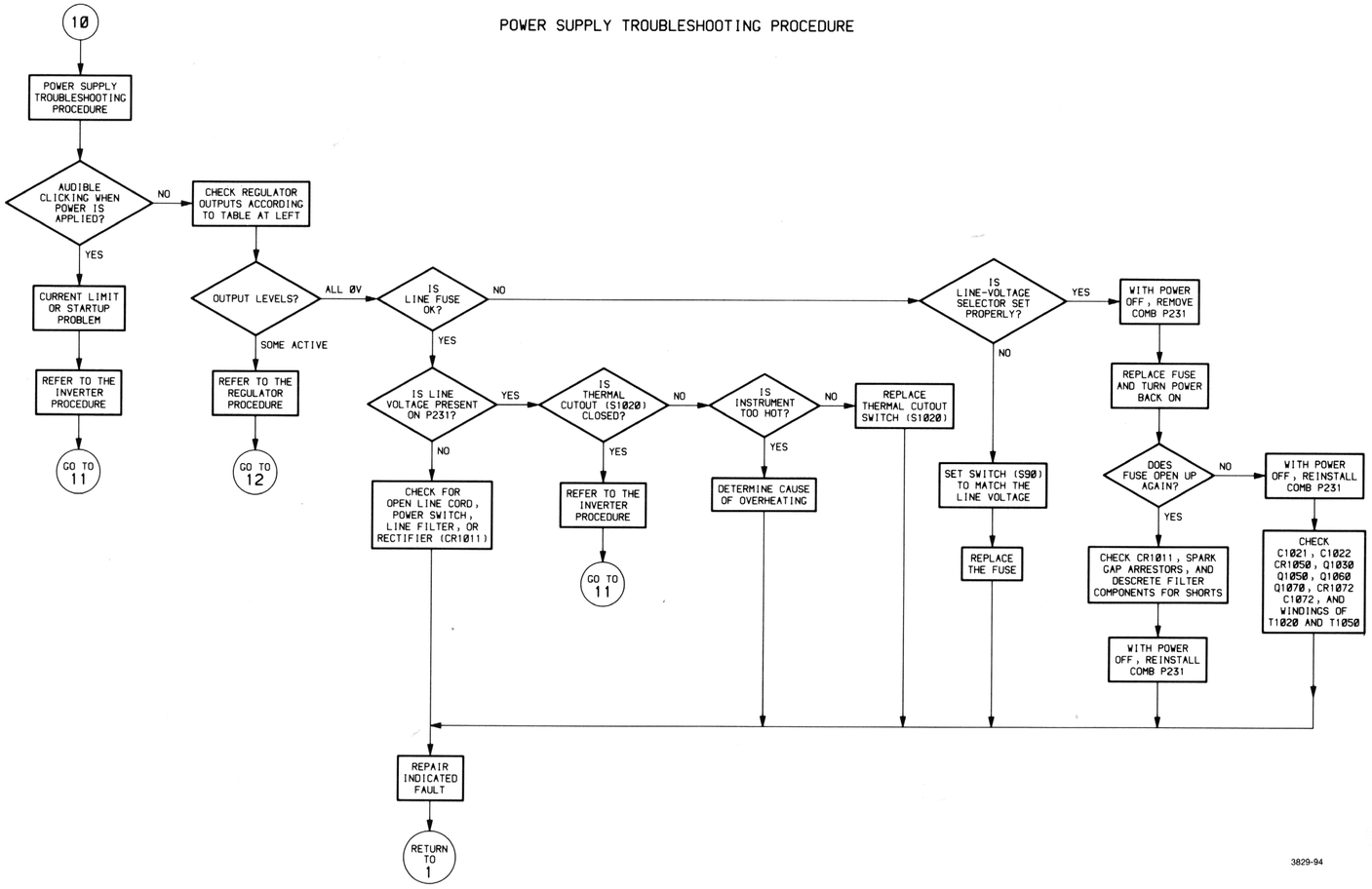

8
Z-AXIS DIAGNOSTIC PROCEDURE
Z-AXIS DIAGNOSTIC PROCEDURE
IS U950'S BLANK INPUT STUCK HI?
NO
YES
WATCH THE VOLTAGE AT U950'S BRIGHT INPUT WHILE ROTATING THE INTENSITY CONTROL THROUGH IT'S RANGE
DOES BRIGHT CHANGE AT LEAST 50 mV?
NO
YES
REPAIR SHORT CIRCUIT ON BRIGHT LINE, REPAIR INTENSITY CONTROL CIRCUIT, REPAIR CONTROL SIGNALS TO U650 OR REPLACE U650
TROUBLESHOOT DISPLAY SEQUENCER'S INPUTS OR REPLACE U650
CORRECT DC BIAS PROBLEM AT U950 OR REPLACE U950
RETURN TO 1
RETURN TO 1
RETURN TO 1

3829-85


9
KERNEL NOP DIAGNOSTIC PROCEDURE
KERNEL NOP DIAGNOSTIC PROCEDURE
MOVE NORM/DIAG JUMPER TO THE DIAG POSITION
DO ADDRESS LINES HAVE A GOOD BINARY COUNT?
YES
IS ADDRESS DECODE OPERATING PROPERLY?
YES
ARE ANY BUFFERED DATA LINES STUCK?
NO
REPLACE U2092, U2178 OR U2194
NO
YES
NO
ARE DATA LINES D1-D7 LO AND D0 HI?
YES
REPLACE U2092, ROMS OR RAM
REPAIR ADDRESS DECODE CIRCUIT
LOCATE FAULT AND REPAIR
NO
REPLACE U2194 OR U2294
RETURN TO 1
3829-91

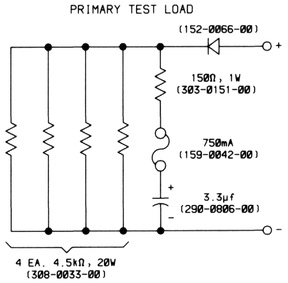
Power Supply Voltage Tolerances		
Power Supply	**Test Point (+ Lead)**	**Reading**
+10 V	J119-4	+9.99 to +10.01
+87 V	J119-8	+85.26 to +88.74
+42.4 V	J119-9	+41.55 to +43.25
+15 V	J119-6	+14.775 to +15.225
Digital +5 V	J119-2	+4.85 to +5.15
Analog +5 V	J119-12	+4.925 to +5.075
–5 V	J119-5	–4.965 to –5.035
–8 V	J119-11	–7.88 to –8.12
–15 V	J119-1	–14.775 to –15.225

POWER SUPPLY TROUBLESHOOTING PROCEDURE



Primary Test Load

The test load illustrated below may be used to test the operation of the Inverter with the output transformer (T1060) and drive transistors (Q1060 and Q1070) disconnected. Connect the + lead of the load to the lifted end of W1060 (see procedure in flowchart at right) and the – lead to the sources of Q1060 and Q1070. A schematic diagram of the load, showing the associated Tektronix part numbers, is given below.



+5 V_D Test Load

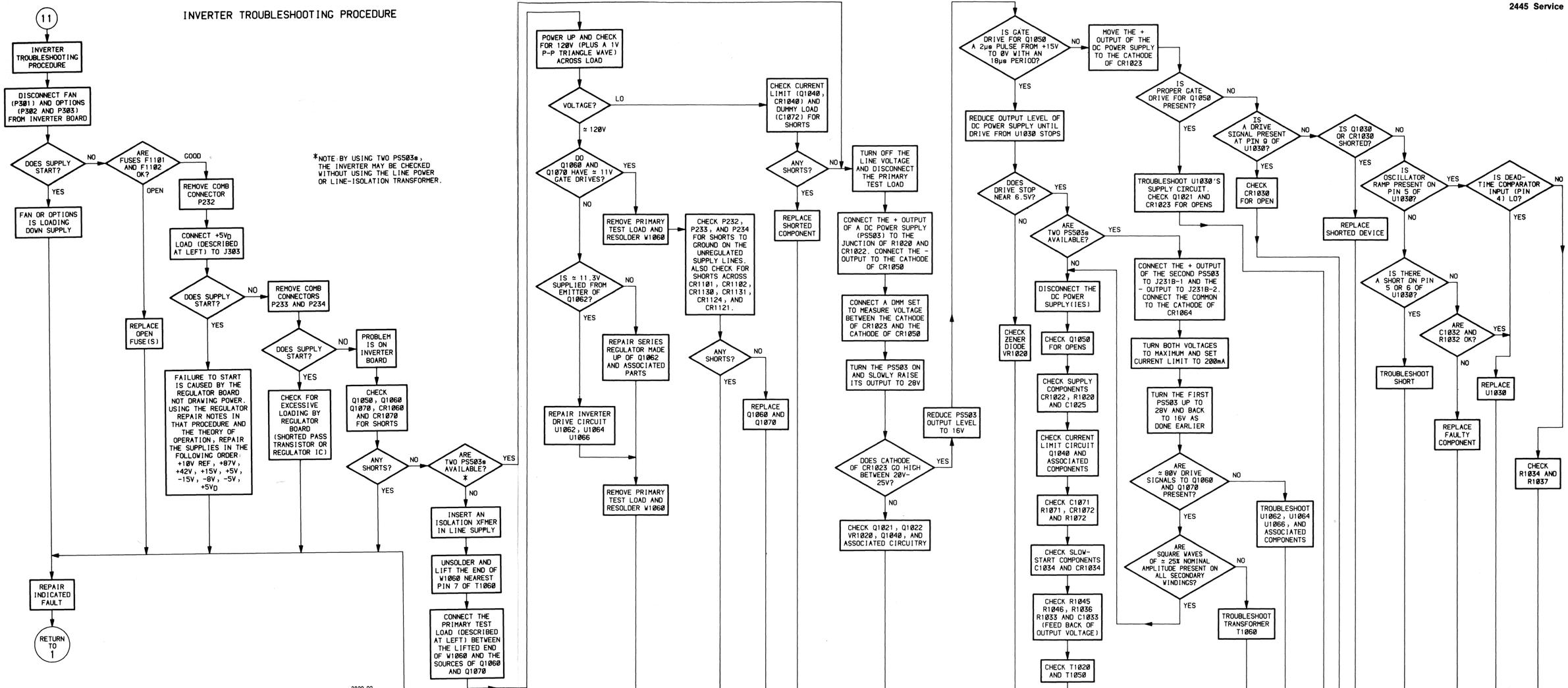
Some load is required for the Inverter to run. When the Power Supply module is removed from the instrument or when the Regulator Board is disconnected from the Inverter Board's output, the test load described below may be used to check operation of the Inverter.

NOTE

Each of the Regulators requires a load to regulate properly; this loading is not provided by the +5-V_D load.

TEST LOAD. Connect two 2-Ω, 25-watt resistors (Tektronix part number 308-0205-00) from the +5-V_D pins of J303 and J232 (on the Inverter Board) to ground.

INVERTER TROUBLESHOOTING PROCEDURE



3829-92

Regulator Repair Notes

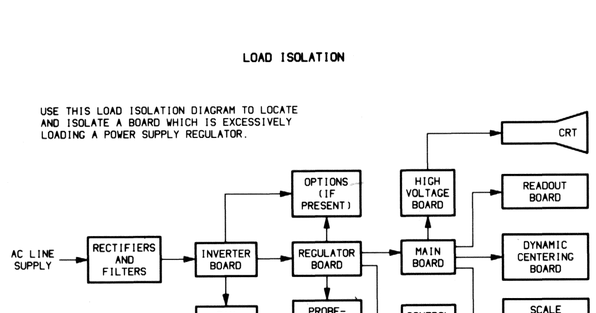
Hints for troubleshooting a faulty supply Regulator:

1. First verify that the +10-V_{REF} level is correctly adjusted; if it is not, do so (see Adjustment Procedure in Section 5).

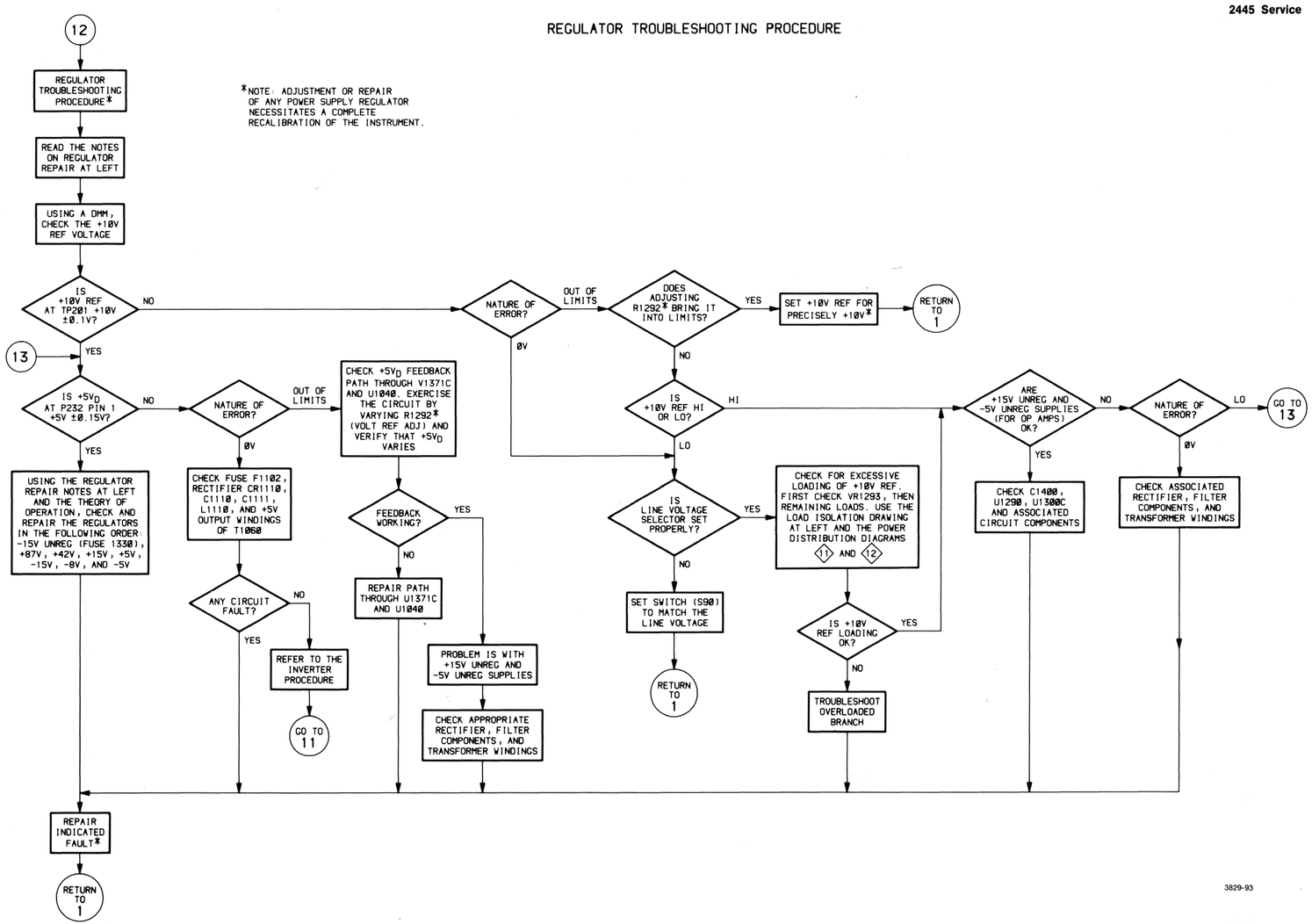
2. Regulator output is high:
   a. Is the output loaded? All Regulators (except +10-V_{REF} require some load to regulate, the lower voltage supplies requiring greater loads. The Regulators between +15 V and −15 V may be loaded using 100-Ω resistors of the proper power ratings.
   b. Check for a short-circuited series-pass device.
   c. Check feedback through the voltage-sense comparator.

3. Regulator output is low:
   a. Check for excessive loading using the Load Isolation diagram below and the Interconnection Schematic (diagram 13).
   b. The operation of the supply Regulators is int dependent. If a supply is out of regulation, veri that the supply of next greater magnitude operating properly. Repair faulty Regulators the following order: +87 V, +42 V, +15 V, +5 −15 V, −8 V, and then −5 V.
   c. Verify that the current-limit circuit is n activated.
   d. Check drive to series-pass device and verify th the device is not open circuited.
   e. Check feedback through the voltage-ser comparator.
   f. If supply goes low only when fully loaded, suspe an open-circuit diode in the associated rectif circuit.

LOAD ISOLATION



REGULATOR TROUBLESHOOTING PROCEDURE



REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

"	INCH
#	NUMBER SIZE
ACTR	ACTUATOR
ADPTR	ADAPTER
ALIGN	ALIGNMENT
AL	ALUMINUM
ASSEM	ASSEMBLED
ASSY	ASSEMBLY
ATTEN	ATTENUATOR
AWG	AMERICAN WIRE GAGE
BD	BOARD
BRKT	BRACKET
BRS	BRASS
BRZ	BRONZE
BSHG	BUSHING
CAB	CABINET
CAP	CAPACITOR
CER	CERAMIC
CHAS	CHASSIS
CKT	CIRCUIT
COMP	COMPOSITION
CONN	CONNECTOR
COV	COVER
CPLG	COUPLING
CRT	CATHODE RAY TUBE
DEG	DEGREE
DWR	DRAWER
ELCTRN	ELECTRON
ELEC	ELECTRICAL
ELCTLT	ELECTROLYTIC
ELEM	ELEMENT
EPL	ELECTRICAL PARTS LIST
EQPT	EQUIPMENT
EXT	EXTERNAL
FIL	FILLISTER HEAD
FLEX	FLEXIBLE
FLH	FLAT HEAD
FLTR	FILTER
FR	FRAME or FRONT
FSTNR	FASTENER
FT	FOOT
FXD	FIXED
GSKT	GASKET
HDL	HANDLE
HEX	HEXAGON
HEX HD	HEXAGONAL HEAD
HEX SOC	HEXAGONAL SOCKET
HLCPS	HELICAL COMPRESSION
HLEXT	HELICAL EXTENSION
HV	HIGH VOLTAGE
IC	INTEGRATED CIRCUIT
ID	INSIDE DIAMETER
IDENT	IDENTIFICATION
IMPLR	IMPELLER
IN	INCH
INCAND	INCANDESCENT
INSUL	INSULATOR
INTL	INTERNAL
LPHLDR	LAMPHOLDER
MACH	MACHINE
MECH	MECHANICAL
MTG	MOUNTING
NIP	NIPPLE
NON WIRE	NOT WIRE WOUND
OBD	ORDER BY DESCRIPTION
OD	OUTSIDE DIAMETER
OVH	OVAL HEAD
PH BRZ	PHOSPHOR BRONZE
PL	PLAIN or PLATE
PLSTC	PLASTIC
PN	PART NUMBER
PNH	PAN HEAD
PWR	POWER
RCPT	RECEPTACLE
RES	RESISTOR
RGD	RIGID
RLF	RELIEF
RTNR	RETAINER
SCH	SOCKET HEAD
SCOPE	OSCILLOSCOPE
SCR	SCREW
SE	SINGLE END
SECT	SECTION
SEMICOND	SEMICONDUCTOR
SHLD	SHIELD
SHLDR	SHOULDERED
SKT	SOCKET
SL	SLIDE
SLFLKG	SELF-LOCKING
SLVG	SLEEVING
SPR	SPRING
SQ	SQUARE
SST	STAINLESS STEEL
STL	STEEL
SW	SWITCH
T	TUBE
TERM	TERMINAL
THD	THREAD
THK	THICK
TNSN	TENSION
TPG	TAPPING
TRH	TRUSS HEAD
V	VOLTAGE
VAR	VARIABLE
W	WITH
WSHR	WASHER
XFMR	TRANSFORMER
XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000BB	BERQUIST COMPANY	4350 WEST 78TH	MINNEAPOLIS, MN 55435
000BK	STAUFFER SUPPLY	105 SE TAYLOR	PORTLAND, OR 97214
000EL	PORTLAND SCREW CO.	6520 N. BASIN AVE.	PORTLAND, OR 97217
000EO	ZEPHER ELECTRONIC SALES CORP.	647 INDUSTRY DRIVE	SEATTLE, WA 98188
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01536	CAMCAR DIV OF TEXTRON INC. SEMS PRODUCTS UNIT	1818 CHRISTINA ST.	ROCKFORD, IL 61108
05006	TWENTIETH CENTURY PLASTICS, INC.	415 E WASHINGTON BLVD.	LOS ANGELES, CA 90015
06915	RICHCO PLASTIC CO.	5825 N. TRIPP AVE.	CHICAGO, IL 60646
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
12327	FREEWAY CORPORATION	9301 ALLEN DRIVE	CLEVELAND, OH 44125
18565	CHOMERICS INC.	77 DRAGON COURT	WOBURN, MA 01801
22161	ADVANCE MACHINE CORP	10200 AVIATION BLVD	LOS ANGELES, CA 90045
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
24931	SPECIALITY CONNECTOR CO., INC.	2620 ENDRESS PLACE	GREENWOOD, IN 46142
28817	CAL-METEX CORP., SUBSIDIARY OF METEX CORP.	509 HINDRY AVE.	INGLEWOOD, CA 90301
49671	RCA CORPORATION	30 ROCKEFELLER PLAZA	NEW YORK, NY 10020
50293	GENERAL ELECTRIC COMPANY, INSTALLATION AND SERVICE ENGINEERING DEPT.	1 RIVER ROAD	SCHENECTADY, NY 12306
54583	TDK ELECTRONICS CORP.	755 EASTGATE BLVD.	GARDEN CITY, NY 11530
70485	ATLANTIC INDIA RUBBER WORKS, INC.	571 W. POLK ST.	CHICAGO, IL 60607
71400	BUSSMAN MFG., DIVISION OF MCGRAW-EDISON CO.	2536 W. UNIVERSITY ST.	ST. LOUIS, MO 63107
73743	FISCHER SPECIAL MFG. CO.	446 MORGAN ST.	CINCINNATI, OH 45206
78189	ILLINOIS TOOL WORKS, INC. SHAKEPROOF DIVISION	ST. CHARLES ROAD	ELGIN, IL 60120
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
80033	PRESTOLE EVERLOCK, INC.	P. O. BOX 278,1345 MIAMI ST.	TOLEDO, OH 43605
82104	STANDARD GRIGSBY CO., DIV. OF SUN CHEMICAL CORPORATION	920 RATHBONE AVENUE	AURORA, IL 60507
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
86928	SEASTROM MFG. COMPANY, INC.	701 SONORA AVENUE	GLENDALE, CA 91201
93907	TEXTRON INC. CAMCAR DIV	600 18TH AVE	ROCKFORD, IL 61101
95987	WECKESSER CO., INC.	4444 WEST IRVING PARK RD.	CHICAGO, IL 60641
S3109	C/O PANEL COMPONENTS CORP.	P.O. BOX 6626	SANTA ROSA, CA 95406
S3629	PANEL COMPONENTS CORP.	2015 SECOND ST.	BERKELEY, CA 94170
T0032	POWELL ELECTRONICS	411 FAIRCHILD DR.	MT. VIEW, CA 94040
T0171	ZEPHER ELECTRONICS	647 INDUSTRY DRIVE	SEATTLE, WA 98188
T1105	J PHILLIP INDUSTRIES INC	5713 NORTHWEST HIGHWAY	CHICAGO, IL 60646
T1167	COLUMBINE PLASTICS	3195 BLUFF ST	BOULDER, CO
T1288	PRODUCTION PARTS INC	4288 SE INTERNATIONAL WAY	PORTLAND, OR 97222
T1302	MOUNTAIN MOULDING	606 SECOND ST	BERTHOUD, CO 80513

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
1-1	334-4658-00			1		MARKER,IDENT:BLANK	80009	334-4658-00
-2	366-2041-01			4		KNOB::GY,BAR,0.172 ID X 0.410 OD	80009	366-2041-01
	377-0512-01			4		INSERT,KNOB:0.125 ID X 0.663 L,AL,0.247	80009	377-0512-01
	366-2036-00			1		PUSH BUTTON:GY,0.206 SQ,1.445 H	80009	366-2036-00
-3	333-2877-00			1		PANEL,FRONT:CRT	80009	333-2877-00
-4	200-2779-00			1		COVER,TOP:TRIM	80009	200-2779-00
-5	348-0740-00			2		FOOT,CABINET:BOTTOM FRONT,PLASTIC	80009	348-0740-00
						**********(ATTACHING PARTS)**********		
-6	211-0718-00			2		SCREW,MACHINE:6-32 X 0.312,FLH,100 DEG	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-7	101-0082-00	B010100	B010999	1		TRIM,DECORATIVE:FRONT,PLASTIC	80009	101-0082-00
	101-0082-01	B011000				TRIM,DECORATIVE:FRONT,PLASTIC	80009	101-0082-00
						**********(ATTACHING PARTS)**********		
-8	211-0718-00			10		SCREW,MACHINE:6-32 X 0.312,FLH,100 DEG	93907	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	214-3374-00	B010100	B011249	1		SPRING,FILTER:23 L	80009	214-3374-00
	214-3374-01	B011250		1		SPRING,FILTER:1.32 L,CU-BE		
-9	337-2926-00			1		SHLD,IMPLOSION:4.33 X 3.56 X 0.06,CLEAR	80009	337-2926-00
	378-0199-00			1		FILTER,LT,CRT:BLUE,4.1 X 3.32 X 0.03	80009	378-0199-00
-10	211-0720-00	B010100	B010999	3		SCR,ASSEM WSHR:6-32 X 0.50 PNH,TORX	01536	ORD BY DESCR
	211-0691-00	B011000		3		SCREW,MACHINE:6-32 X 0.625,PNH	01536	ORD BY DESCR
-11	343-0003-00			1		CLAMP,LOOP:0.25 ID,PLASTIC	95987	1-4-6B
-12	161-0104-00			1		CABLE ASSY,PWR,:3 WIRE,98.0 L,W/RTANG CONN	S3109	ORD BY DESCR
	----- -----			-		(ALSO SEE STD ACCESS)		
-13	334-4378-00			1		MARKER,IDENT:MKD PROBE POWER	80009	334-4378-00
-14	334-4381-00			1		MARKER,IDENT:MKD CONNECTOR IDENT	80009	334-4381-00
-15	334-4377-00	B010100	B013049	1		MARKER,IDENT:MKD CAUTION	80009	334-4377-00
	334-4377-02	B013050		1		MARKER,IDENT:MKD CAUTION	80009	334-4377-02
-16	348-0729-00			2		FOOT,CABINET:W/CORDWRAP,REAR,BLACK	80009	348-0729-00
						**********(ATTACHING PARTS)**********		
-17	212-0154-00			2		SCREW,MACHINE:8-32 X 1.125,PNH,TORX	93907	ORD BY DESCR
	211-0711-00			2		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-18	200-2685-00			1		COVER,REAR:	80009	200-2685-00
-19	334-4659-00			1		MARKER,IDENT:MKD TEKTRONIX	80009	334-4659-00
-20	367-0303-00	B010100	B010999	1		HANDLE,CARRYING:12.864 L,SST	80009	367-0303-01
	367-0303-02	B011000				HANDLE,CARRYING:12.704,SST	80009	367-0303-02
						**********(ATTACHING PARTS)**********		
-21	212-0144-00			2		SCREW,TPG,TF:8-16 X 0.562 L	93907	225-38131-012
-22	346-0195-00	B010100	B010999	2		STRAP,GROUND:STAINLESS STEEL	80009	346-0195-00
						**********(END ATTACHING PARTS)*********		
-23	437-0286-00			1		CABINET,SCOPE:ALUMINUM	80009	437-0286-00

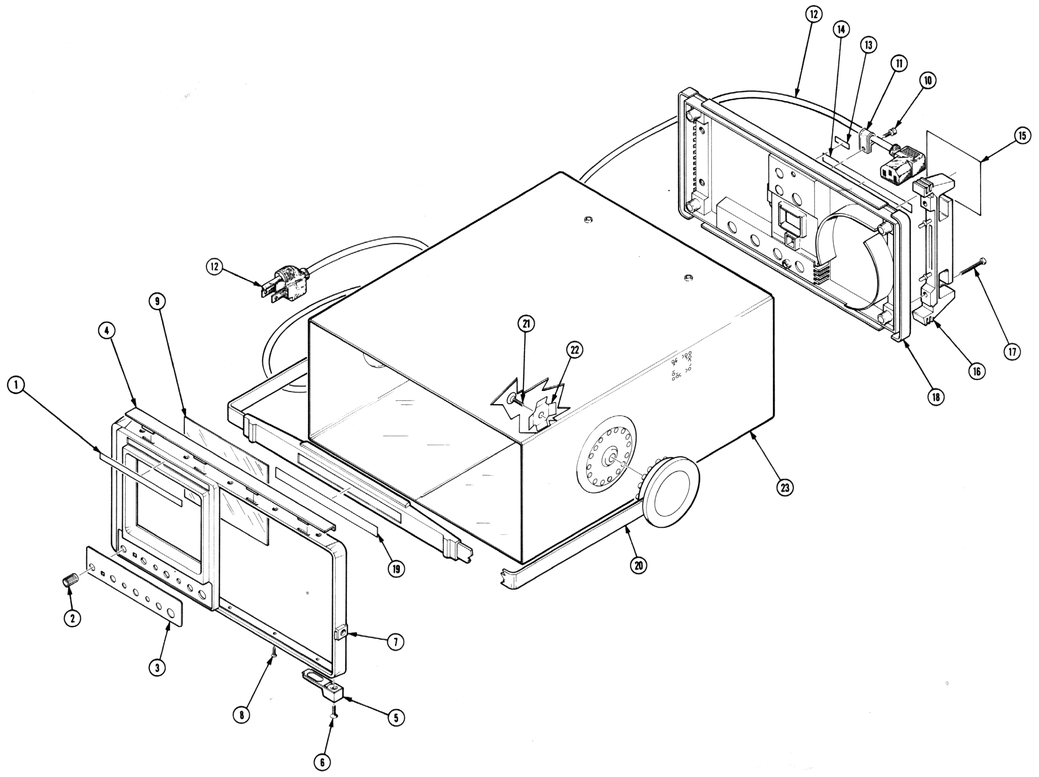


FIG. 1 CABINET

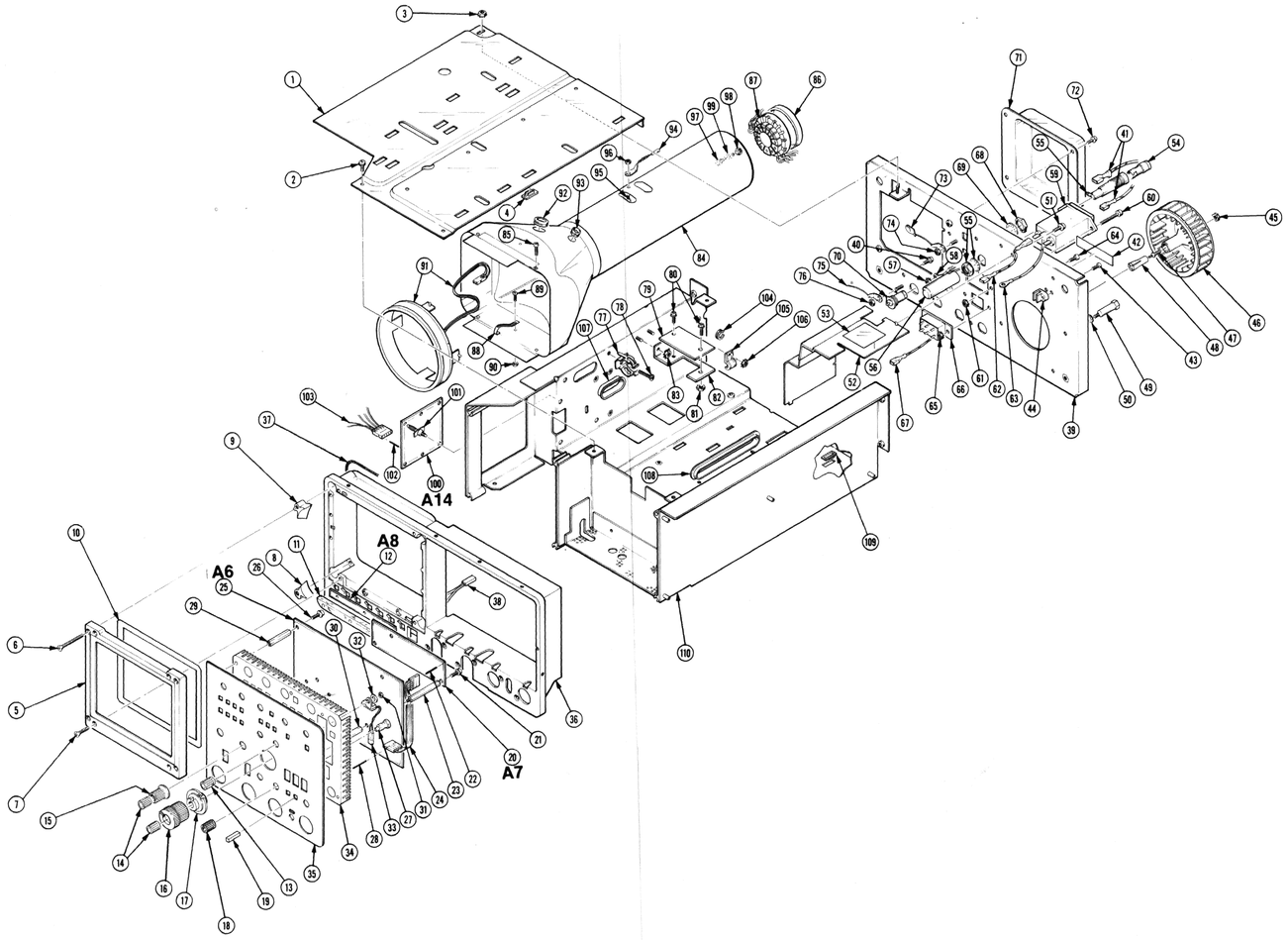

A14
A8
A6
A7

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
2-1	407-2790-00			1	BRACKET,CKT BD:VERTICAL,ALUM	80009	407-2790-00
					**********(ATTACHING PARTS)**********		
-2	211-0711-00			4	SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
-3	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-4	343-1012-00			1	RETAINER,CKT BD:	80009	343-1012-00
-5	426-1864-00			1	FRAME,CRT:	80009	426-1864-00
					**********(ATTACHING PARTS)**********		
-6	211-0713-00			4	SCREW,MACHINE:6-32 X 1.25,FLH,100 DEG,STL	93907	ORD BY DESCR
-7	213-0914-00			4	SCREW,TPG,TR:6-32 X 0.75,FLH,100 DEG,TOR	93907	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-8	343-0992-00			2	RETAINER,CRT:RIGHT,PLASTIC	80009	343-0992-00
	----- -----			-	(UPPER RT/LOWER LEFT/NAT)		
-9	343-0993-00			2	RETAINER,CRT:PLASTIC	80009	343-0993-00
	----- -----			-	(UPPER LEFT/LOWER RT/BLK)		
-10	348-0731-00			1	GASKET:CRT	80009	348-0731-00
-11	378-0204-00			1	REFLECTOR,LIGHT:INT SCALE ILLUMINATION	80009	378-0204-00
-12	670-7280-00			1	CKT BOARD ASSY:SCALE ILLUMINATION	80009	670-7280-00
	----- -----			-	(SEE A8 REPL)		
	175-4593-00			1	.CA ASSY,SP,ELEC:2,26 AWG,4.0 L,RIBBON	80009	175-4593-00
-13	366-1833-00			3	KNOB:GRAY,0.25 ID X 0.392 X 0.39	80009	366-1833-00
-14	366-2145-01			3	KNOB:DOVE GY,TIME/DIV,0.08 ID X	80009	366-2145-01
-15	366-2038-00			2	KNOB:GY,0.25 ID X 0.706 OD X 0.6	80009	366-2038-00
-16	366-2039-00	B010100	B019999	1	KNOB:GY,B SWEEP,0.2 ID X 0.78 OD	80009	366-2039-00
	366-2039-01	B020000		1	KNOB:GY,B SWEEP	80009	366-2039-01
-17	366-2040-00			1	KNOB:CLEAR,A SWEEP,0.252 ID X 1.	80009	366-2040-00
-18	366-2041-01	B010100	B011999	7	KNOB::GY,BAR,0.172 ID X 0.410 OD	80009	366-2041-01
	366-2041-03	B012000		7	KNOB:DOVE GRAY,BAR,0.172 ID X 0.41 OD X 0.	80009	366-2041-03
-19	366-2017-00			16	KNOB:0.18 SQ X 0.644 H,IVORY GY	80009	366-2017-00
	----- -----			-	(SUBPART OF A6 CKT BOARD)		
-20	670-7284-00			1	CKT BOARD ASSY:FRONT PANEL VARIABLE	80009	670-7284-00
	----- -----			-	(SEE A7 REPL)		
					**********(ATTACHING PARTS)**********		
-21	211-0304-00			3	SCREW,MACHINE:4-40 X 0.312,PNH	01536	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-22	131-0608-00			5	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-23	129-0941-00			2	SPACER,POST:1.86 L W/4-40 INT THD	80009	129-0941-00
-24	175-4597-00			1	CA ASSY,SP,ELEC:5,26 AWG,4.0 L,RIBBON	80009	175-4597-00
-25	----- -----			1	CKT BOARD ASSY:FRONT PANEL(SEE A6 REPL)		
	----- -----			-	(REPLACEABLE ONLY AS 672-1039-XX)		
					**********(ATTACHING PARTS)**********		
-26	211-0304-00			5	SCREW,MACHINE:4-40 X 0.312,PNH	01536	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-27	377-0550-00			10	.INSERT,KNOB:0.178 ID X 0.640 THK,0.370	80009	377-0550-00
-28	131-0608-00			7	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
	352-0639-00			2	.HOLDER,LED:BLACK	80009	352-0639-00
	352-0641-00			3	.HOLDER,LED:FIVE,BLACK	80009	352-0641-00
	352-0642-00			1	.HOLDER,LED:FOUR,BLACK	80009	352-0642-00
-29	129-0938-00			5	SPACER,POST:1.102 L W/4-40 THD EACH END	80009	129-0938-00
-30	129-0978-00			2	SPACER,POST:0.375-32 AL,0.5 HEX	80009	129-0978-00
-31	220-0495-00			1	NUT,PLAIN,HEX.:0.375-32 X 0.438 INCH BRS	73743	ORD BY DESCR
-32	210-0012-00			3	WASHER,LOCK:INTL,0.384 ID,INTL,0.022 TH	78189	1220-02-00-0541C
-33	----- -----			-	(SEE CHASSIS PARTS S3185 REPL)		
-34	354-0632-00	B010100	B019999	1	RING,MOUNTING:5.41 X 4.18	22161	OBD
	354-0632-01	B020000		1	RING,MOUNTING:5.41 X 4.18		
-35	333-2915-00	B010100	B019999	1	PANEL,FRONT:	80009	333-2915-00
	333-2915-01	B020000		1	PANEL,FRONT:2445		
	333-2993-00	B020000		1	PANEL,FRONT:		
	----- -----			-	(OPT. 06 ONLY)		
	333-2994-00	B020000		1	PANEL,FRONT:		
	----- -----			-	(OPT. 05 & 06 ONLY)		
	210-0077-00			2	WASHER,SPR TNSN:0.375 ID X 0.0025 OD	78189	3515-20-19-1744
	210-0586-00			3	NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
	214-3373-00			1	SPRING,GROUND:PHOSPHOR-BRONZE	80009	214-3373-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
2-	214-3428-00			2		SPRING,GROUND:VOLTS/DIV,SST	80009	214-3428-00
	348-0769-00			1		SHLD,GSKT,ELEK:TIME/DIV	80009	348-0769-00
-36	386-4728-00			1		SUBPANEL,FRONT:	80009	386-4728-00
-37	348-0276-00			AR		SHLD,GSKT,ELEK:0.026 OD NPRN W/WIRE NET CO	28817	01-0404-3719
-38	175-4593-00			1		CA ASSY,SP,ELEC:2,26 AWG,4.0 L,RIBBON	80009	175-4593-00
	----- -----			-		(SUBPART OF THE SUB-PANEL ASSEMBLY		
	----- -----			-		.NOT ILLUSTRATED)		
	175-4595-00			6		CA ASSY,SP,ELEC:3,22 AWG,2.0 L,RIBBON	80009	175-4595-00
						**********(ATTACHING PARTS)**********		
	210-0583-00			6		NUT,PLAIN,HEX:0.25-32 X 0.312 INCH,BRS	73743	2X20317-402
	210-0046-00			6		WASHER,LOCK:0.261 ID,INTL,0.018 THK,BRS	78189	1214-05-00-0541C
						**********(END ATTACHING PARTS)**********		
-39	386-4713-00	B010100	B019999	1		PLATE,REAR:POWER SUPPLY	80009	386-4713-00
	386-4713-01	B020000		1		PLATE,REAR:POWER SUPPLY		
						**********(ATTACHING PARTS)**********		
-40	211-0711-00			5		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)**********		
	334-3379-00			1		MARKER,IDENT:MARKED GROUND SYMBOL	80009	334-3379-00
-41	195-3984-00			1		LEAD,ELECTRICAL:22 AWG,4.0 L,8-01	80009	195-3984-00
-42	334-4865-00			1		MARKER,IDENT:MKD FAN,CAUTION	80009	334-4865-00
-43	211-0304-00			2		SCREW,MACHINE:4-40 X 0.312,PNH	01536	ORD BY DESCR
-44	386-4863-00			1		SUPPORT,CKT BD:	80009	386-4863-00
-45	220-0555-00			1		NUT,PLAIN,HEX.:8-32 X 0.25 INCH STL	000EL	ORD BY DESCR
-46	369-0043-01			1		IMPLR,FAN ASSY:2.8 DIA,0.25 DIA SHAFT	80009	369-0043-01
-47	355-0192-00			1		STUD,SHLDR & STEP:4-40 THD ONE END,8-32 TH	80009	355-0192-00
-48	343-1040-01			1		COLLAR,FAN MT:	80009	343-1040-01
-49	361-1188-00			4		SPACER,POST:1.15 L,4-40 THD 1 END	80009	361-1188-00
-50	210-0994-00			4		WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
-51	211-0711-00			1		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
-52	337-3021-00			1		SHIELD,ELEC:LVPS PEOPLE	80009	337-3021-00
-53	334-4759-00	B010100	B012699	1		MARKER,IDENT:MKD SHIELDS INVERTER	80009	334-4759-00
	334-5196-00	B012700		1		(STANDARD AND OPTIONS 05,06,09,10		
-54	200-0237-04			1		COVER,FUSE HLDR:PLASTIC,SAFETY CONTROLLED	80009	200-0237-04
-55	204-0832-00			1		BODY,FUSEHOLDER:3AG,5 X 20MM FUSES	S3629	031.1673(MDLFEU)
-56	200-2265-00			1		CAP,FUSEHOLDER:5 X 20MM FUSES	S3629	FEK 031.1663
						**********(ATTACHING PARTS)**********		
-57	210-0457-00			1		NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)**********		
-58	195-3984-00			1		LEAD,ELECTRICAL:22 AWG,4.0 L,8-01	80009	195-3984-00
	195-3986-00			1		LEAD,ELECTRICAL:18 AWG,4.0 L,8-0	80009	195-3986-00
-59	119-1536-00			1		FILTER,RFI:3A,250VAC,50/60 HZ	54583	ZUB2203-000
						**********(ATTACHING PARTS)**********		
-60	211-0332-00			2		SCR,ASSEM WSHR:4-40 X 0.5,PNH,TORX DRIVE	01536	ORD BY DESCR
-61	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)**********		
-62	195-3989-00			1		LEAD,ELECTRICAL:18 AWG,4.0 L,8-9	80009	195-3989-00
-63	195-3990-00			1		LEAD,ELECTRICAL:18 AWG,4.5 L,5-4	80009	195-3990-00
-64	211-0304-00			2		SCREW,MACHINE:4-40 X 0.312,PNH	01536	ORD BY DESCR
-65	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
-66	----- -----			1		(SEE S90 CHASSIS REPL)		
-67	195-3987-00			1		LEAD,ELECTRICAL:22 AWG,4.0 L,8-19	80009	195-3987-00
	195-3988-00			1		LEAD,ELECTRICAL:22 AWG,4.0 L,8-29	80009	195-3988-00
-68	----- -----			4		NUT,PLAIN,KNURL:(FURN WITH 131-1910-01 BNC		
-69	----- -----			4		WASHER,LOCK:(FURN WITH 131-1910-01 BNC'S)		
-70	131-1910-01			4		CONN,RCPT,ELEC:BNC,FEMALE	24931	28JR284-1
-71	200-2686-00			1		COVER,REAR:CRT	80009	200-2686-00
						**********(ATTACHING PARTS)**********		
-72	211-0711-00			1		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)**********		
-73	195-8410-00			1		LEAD,ELECTRICAL:22 AWG,1.65 L	80009	195-8410-00
						**********(ATTACHING PARTS)**********		
-74	210-0551-00			1		NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	ORD BY DESCR
						**********(END ATTACHING PARTS)**********		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
2-75	195-9513-00			1	LEAD,ELECTRICAL:22 AWG,1.4 L	80009	195-9513-00
					**********(ATTACHING PARTS)**********		
-76	210-0551-00			1	NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
	131-1425-00			AR	TERM SET,PIN:(36) 0.025 SQ RTANG,0.15L	22526	65521-136
-77	344-0250-00			1	CLIP,ELECTRICAL:COMPONENT MOUNTING	80033	E50005-007
					**********(ATTACHING PARTS)**********		
-78	211-0504-00	B010100	B019999	1	SCREW,MACHINE:6-32 X 0.25 INCH,PNH STL	83385	ORD BY DESCR
	211-0722-00	B020000		1	SCREW,MACHINE:6-32 X 0.25L, PNH,STL,CD PL,		
					**********(END ATTACHING PARTS)**********		
-79	307-1154-00			1	PASSIVE NETWORK:CRT TERMINATOR,FINISHED	80009	307-1154-00
					**********(ATTACHING PARTS)**********		
-79	211-0324-00			2	SCR,ASSEM WSHR:4-40 X 0.188 L,PNH,TORX,MCH	01536	ORD BY DESCR
-81	210-0457-00			2	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-82	407-2809-00			1	BRACKET,ANGLE:RESISTOR,AL	80009	407-2809-00
					**********(ATTACHING PARTS)**********		
-83	210-0457-00			2	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
	334-1379-00			1	LABEL:CRT,ADHESIVE BACK	80009	334-1379-00
	334-1951-00			1	MARKER,IDENT:CRT WARNING	80009	334-1951-00
-84	337-2931-00			1	SHIELD,CRT:	80009	337-2931-00
					**********(ATTACHING PARTS)**********		
-85	211-0324-00			4	SCR,ASSEM WSHR:4-40 X 0.188 L,PNH,TORX,MCH	01536	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-86	200-0917-01			1	COV,ELECTRON TU:2.052 OD X 0.291" THK,PLST	80009	200-0917-01
-87	198-4603-00			1	WIRE SET,ELEC:	80009	198-4603-00
-88	214-0291-00			2	CONTACT,SPRING:1.188 X 0.375 X 0.25 INCH	80009	214-0291-00
					**********(ATTACHING PARTS)**********		
-89	211-0324-00			2	SCR,ASSEM WSHR:4-40 X 0.188 L,PNH,TORX,MCH	01536	ORD BY DESCR
-90	210-0586-00			2	NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-91	119-1478-00			1	COIL,TUBE DEFL:FXD,TRACE ROTATION	80009	119-1478-00
-92	348-0762-00			1	GROMMET,PLASTIC:BLACK,ROUND,0.54 ID	T1302	OBD
-93	348-0004-00			1	GROMMET,RUBBER:0.281 ID X 0.563 INCH OD	70485	763
-94	195-6851-00			1	LEAD,ELECTRICAL:BRAIDED,1.65 L	80009	195-6851-00
					**********(ATTACHING PARTS)**********		
-95	211-0324-00			1	SCR,ASSEM WSHR:4-40 X 0.188 L,PNH,TORX,MCH	01536	ORD BY DESCR
-96	210-0551-00			1	NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
	195-8410-00			1	LEAD,ELECTRICAL:22 AWG,1.65 L	80009	195-8410-00
					**********(ATTACHING PARTS)**********		
-97	211-0324-00			1	SCR,ASSEM WSHR:4-40 X 0.188 L,PNH,TORX,MCH	01536	ORD BY DESCR
-98	210-0551-00			1	NUT,PLAIN,HEX.:4-40 X 0.25 INCH,STL	000BK	ORD BY DESCR
-99	210-0994-00			1	WASHER,FLAT:0.125 ID X 0.25" OD,STL	86928	5702-201-20
					**********(END ATTACHING PARTS)**********		
-100	670-8000-00			1	CKT BOARD ASSY:DYNAMIC CENTERING	80009	670-8000-00
	----- -----			-	(SEE A14 REPL)		
					**********(ATTACHING PARTS)**********		
-101	361-0067-00			3	.SPACER,CKT BD:0.187,NYLON	06915	LCBS-3M
	211-0711-00			1	.SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
	129-0208-00	B020000		1	.SPACER,POST:0.312" LONG,6-32 ONE END	80009	129-0208-00
	343-1131-00	B020000		1	.CLAMP,LOOP:0.547 X 0.144 ID,METAL		
					.**********(END ATTACHING PARTS)**********		
-102	131-0608-00			5	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-103	175-8010-00			1	CA ASSY,SP,ELEC:5,22 AWG,10.5 L,RIBBON	80009	175-8010-00
-104	348-0757-00			2	GROMMET,PLASTIC:BLACK U SHAPE,0.25 ID	80009	348-0757-00
-105	343-0081-00			1	STRAP,RETAINING:	95987	3/16-H
					**********(ATTACHING PARTS)**********		
-106	210-0457-00			1	NUT,PL,ASSEM WA:6-32 X 0.312,STL CD PL	83385	ORD BY DESCR
					**********(END ATTACHING PARTS)**********		
-107	348-0073-00			1	HINGE BLOCK,STA:L FR,R REAR,BLACK ACETAL	80009	348-0073-00
-108	348-0751-00			1	GROMMET,PLASTIC:BLACK,3.11 X 0.645 OBLONG	80009	348-0751-00
-109	343-1012-00			1	RETAINER,CKT BD:	80009	343-1012-00
-110	441-1618-00	B010100	B019999	1	CHASSIS,SCOPE:MAIN	80009	441-1618-00
	441-1618-01	B020000		1	CHASSIS,SCOPE:MAIN		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-1	337-2932-00			1		SHIELD,ELEC:HIGH VOLTAGE		
						**********(ATTACHING PARTS)**********		
-2	211-0304-00			4		SCREW,MACHINE:4-40 X 0.312,PNH	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
	334-4750-00			1		MARRKER,IDENT:MKD HIGH VOLTAGE	80009	334-4750-00
-3	----- -----			1		CKT BOARD ASSY:HIGH VOLTAGE		
	----- -----			-		(SEE A9 REPL)		
						**********(ATTACHING PARTS)**********		
-4	361-1188-00			6		SPACER,POST:1.15 L,4-40 THD 1 END	80009	361-1188-00
						**********(END ATTACHING PARTS)*********		
-5	131-0592-00			14		.CONTACT,ELEC:0.885 INCH LONG	22526	47353
-6	131-0589-00			13		.TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
-7	352-0661-00			1		.HOLDER,TERMINAL:17 SQUARE PINS	T1167	OBD
	175-4596-00			1		CA ASSY,SP,ELEC:5,22AWG,7.0 L, RIBBON	T0171	OBD
	348-0763-00			1		GROMMET,PIASTIC:NATURAL,OVAL,1.235 ID	80009	348-0763-00
-8	175-4581-00			1		CA ASSY,SP,ELEC:26,28 AWG,5.0 L,RIBBON	80009	175-4581-00
-9	----- -----			1		CKT BOARD ASSY:BUS MONITOR		
	----- -----			-		(SEE A4 REPL)		
-10	131-0608-00			7		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-11	175-4583-00			1		CA ASSY,SP,ELEC:26,28 AWG,2.5 L	80009	175-4583-00
-12	----- -----			1		CKT BOARD ASSY:DIGITAL CONTROL		
	----- -----			-		(SEE A5 REPL)		
						**********(ATTACHING PARTS)**********		
-13	211-0711-00			4		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-14	131-0993-00			1		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-15	131-0608-00			122		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-16	136-0757-00			1		.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-17	136-0755-00			4		.SKT,PL-IN ELEK:MICROCIRCUIT,28 DIP	09922	DILB28P-108
-18	337-2978-00			1		SHIELD,ELEC:LOW VOLTAGE POWER SUPPLY	80009	337-2978-00
						**********(ATTACHING PARTS)**********		
-19	211-0711-00			2		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
-20	211-0304-00			2		SCREW,MACHINE:4-40 X 0.312,PNH	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-21	407-2830-00			1		BRKT,CMPNT MTG:CAP & MOTOR,LEFT,PLASTIC	80009	407-2830-00
						**********(ATTACHING PARTS)**********		
-22	211-0332-00			2		SCR,ASSEM WSHR:4-40 X 0.5,PNH,TORX DRIVE	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-23	407-2829-00			1		BRKT,CMPNT MTG:CAP & MOTOR,RIGHT,PLASTIC	80009	407-2829-00
						**********(ATTACHING PARTS)**********		
-24	210-0586-00			3		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-25	129-0304-00			1		INSULATOR,STDF:0.25 OD X 1.23 INCH LONG	80009	129-0304-00
-26	407-2854-00			1		BRACKET,ANGLE:TRANSISTOR,ALUM	80009	407-2854-00
						**********(ATTACHING PARTS)**********		
-27	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-28	343-1025-00			3		RETAINER,XSTR:	80009	343-1025-00
						**********(ATTACHING PARTS)**********		
-29	210-0406-00			3		NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
						**********(END ATTACHING PARTS)*********		
-30	342-0582-00			3		INSULATOR,PLATE:TRANSISTOR,CERAMIC	80009	342-0582-00
-31	388-8016-01			1		CKT BOARD:INVERTER TRANS	80009	388-8016-01
-32	195-6852-00			1		LEAD,ELECTRICAL:18 AWG,2.375 L,8-4	80009	195-6852-00
						**********(ATTACHING PARTS)**********		
-33	210-0586-00			1		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-34	----- -----			3		TRANSISTOR:MOSFE,N-CHANNEL,SI,TO-220		
	----- -----			-		(SEE A3Q1050,Q1060,Q1070 REPL)		
						**********(ATTACHING PARTS)**********		
-35	210-0586-00			3		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-36	210-0406-00			1		NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-37	210-1002-00			1		WASHER,FLAT:0.125 ID X 0.25 INCH OD,BRS	12327	ORD BY DESCR
	210-1178-00			1		WASHER,SHLDR:U/W T0-220 TRANSISTOR	49671	DF137A
-38	----- -----			1		SEMICOND DEVICE:RECT,SI,10A,30V		
	----- -----			-		(SEE A3CR1110 REPL)		
-39	342-0354-00			1		INSULATOR,PLATE:TRANSISTOR,SILICON RUBBER	000BB	7403-10-52
-40	129-0912-00			1		SPACER,POST:0.62 L W 6/32 THD ONE END	80009	129-0912-00
						**********(ATTACHING PARTS)**********		
-41	211-0711-00			3		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-42	195-9720-00	B010100	B011299	1		LEAD,ELECTRICAL:18 AWG,1.4 L,5-4	80009	195-9720-00
	195-9720-01	B011300		1		LEAD,ELECTRICAL:18 AWG,2.4 L,0-N	80009	195-9720-01
-43	----- -----			1		CKT BOARD ASSY:FAN MOTOR		
	----- -----			-		(SEE A10 REPL)		
-44	131-0608-00			3		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-45	361-1187-00			1		.SPACER,FAN:0.125,POLYPHENYLENE	80009	361-1187-00
-46	175-4728-00			1		CA ASSY,SP,ELEC:2,22 AWG,8.0 L,RIBBON	80009	175-4728-00
-47	175-4585-00			1		CA ASSY,SP,ELEC:20,28 AWG,13.0 L	80009	175-4585-00
-48	407-2825-00			1		BRACKET,ANGLE:TRANSISTOR MTG	80009	407-2825-00
						**********(ATTACHING PARTS)**********		
-49	211-0711-00			3		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
-50	210-0586-00			2		NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-51	210-0406-00			6		NUT,PLAIN,HEX.:4-40 X 0.188 INCH,BRS	73743	12161-50
-52	210-1307-00			6		WASHER,LOCK:0.115 ID,SPLIT,0.025 THK	86928	A384-25N
-53	342-0536-00			6		INSULATOR,XSTR:TO-220,POLYENELENE	80009	342-0536-00
-54	----- -----			4		TRANSISTOR:SILICON,NPN		
	----- -----			-		(SEE A2Q1220,Q1240,Q1280,Q1300 REPL)		
	----- -----			2		MICROCIRCUIT,LI:VOLTAGE REGULATOR		
	----- -----			-		(SEE A2U1260,U1330 REPL)		
-55	342-0563-00			6		INSULATOR,PLATE:TRANSISTOR,FIBERGLAS	18565	ORD BY DESCR
-56	361-1207-00			6		SPACER,PLATE:0.550 X 0.812,ALUM	80009	361-1207-00
-57	131-2779-00			3		CONN,PLUG,ELEC:CKT BD,1 X 5 MALE,0.15 SP	22526	65306-XXX
	131-2780-00			1		CONN,PLUG,ELEC:CKT BD,1 X 3 MALE,0.15 SP	22526	65306-XXX
-58	343-1067-00	B010100	B019999	4		RTNR,ELEC CONN:POLY,BLACK	80009	343-1067-00
	343-1067-01	B020000		4		RTNR,ELEC CONN:POLY,BLACK	80009	343-1067-01
-59	----- -----			1		CKT BOARD ASSY:REGULATOR		
	----- -----			-		(SEE A2 REPL-AVAILABLE AS 672-1037-XX ONLY		
-60	200-2735-00			1		.COVER,POWER SW:	80009	200-2735-00
-61	131-0608-00			16		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-62	136-0263-04			18		.SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-63	----- -----			4		.TERM QIK DISC:CKT BD MNT,0.11 X 0.02		
	----- -----			-		.(SEE A2P204,P205,P206,P207 REPL)		
-64	129-0976-00			1		SPACER,POST:0.86 L X 6-32,POLY,0.3	80009	129-0976-00
-65	361-1132-00	B010100	B010999	6		SPACER,CKT BD:A	80009	361-1132-00
	361-1132-01	B011000		6		SPACER,CKT BD:A POLYCABONATE		
	388-8092-00	B010100	B019999	1		CIRCUIT BOARD:SHIELD, LOW VOLT PWR SUPPLY		
-66	337-3059-00	B020000		1		SHIELD,ELEC:LVPS	80009	337-3059-00
-67	----- -----			1		CKT BOARD ASSY:INVERTER		
	----- -----			-		(SEE A3 REPL-AVAILABLE AS 672-1037-XX ONLY		
-68	131-0608-00			7		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-69	136-0263-04			18		.SOCKET,PIN TERM:FOR 0.025 INCH SQUARE PIN	22526	75377-001
-70	131-0589-00			4		.TERMINAL,PIN:0.46 L X 0.025 SQ	22526	48283-029
	343-1099-00	B020000		1		.RTNR, POWER SUPPLY:LOW VOLTAGE, FRONT PC		
	276-0525-00	B011700		1		.CORE,FERRITE:0.196 ID X 0.437"OD	01121	T037C351A
-71	175-4594-00			1		CA ASSY,SP,ELEC:7,22 AWG,7.0 L,RIBBON	80009	175-4594-00
-72	175-4598-00			1		CA ASSY,SP,ELEC:8,26 AWG,7.0 L,RIBBON	80009	175-4598-00
-73	175-4595-00			1		CA ASSY,SP,ELEC:3,22 AWG,2.0 L,RIBBON	80009	175-4595-00
-74	366-1767-00			1		PUSH BUTTON:BLACK,YELLOW INDICATOR	000EO	FA201
-75	407-2904-00			1		BRACKET,EXT SFT:ABS	80009	407-2904-00
-76	211-0718-00			1		SCREW,MACHINE:6-32 X 0.312,FLH,100 DEG	93907	ORD BY DESCR
-77	214-3328-00			1		SPRING,HLCPS:0.37 OD X 0.7 L,CLOSED ENDS	80009	214-3328-00
-78	384-1631-00			1		EXTENSION SHAFT:12.897 L X 0.375 OD,PLSTC	80009	384-1631-00

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
3-79	407-2800-00			1		BRACKET,PIVOT:EXTENSION SHAFT,PLASTIC	80009	407-2800-00
						**********(ATTACHING PARTS)**********		
-80	211-0711-00			1		SCR,ASSEM WSHR:6-32 X 0.25 L,PNH,TORX	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-81	407-2803-00			1		BRACKET,PVT ARM:EXTENSION SHAFT,PLASTIC	80009	407-2803-00
-82	----- -----			1		CKT BOARD ASSY:MAIN		
	----- -----			-		(SEE A1 REPL)		
-83	386-4735-00			1		.PLATE,CMPNT MTG:ALUM	80009	386-4735-00
						.**********(ATTACHING PARTS)**********		
-84	210-0586-00			2		.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
	361-0382-00			2		.SPACER,PB SW:BROWN,0.275 INCH LONG	80009	361-0382-00
	361-0719-00			2		.SPACER,SLEEVE:0.092 ID X 0.062 IL,PLASTIC	82104	10-0144/0622
-85	131-2716-01			1		.TERMINAL,CAL:	80009	131-2716-01
-86	131-0679-02			2		.CONNECTOR,RCPT,:BNC,MALE,3 CONTACT	24931	28JR270-1
						.**********(ATTACHING PARTS)**********		
-87	213-0006-00			2		.SETSCREW:8-32 X 0.188 INCH,HSS STL	50293	28701-98C-3B
						.**********(END ATTACHING PARTS)*********		
-88	210-0586-00			36		.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
-89	----- -----			9		.MICROCIRCUIT,LI:(A1U700 SHOWN, ALSO SEE		
	----- -----			-		.A1U100,A1U200,U300,U400,U500,U600,U900,		
						.U950 REPL)		
-90	136-0764-00			6		.SKT,PL-IN ELEK:48 LINE CONT IMPD HYBRID	80009	136-0764-00
	119-1445-01			1		.ATTENUATOR,VAR:PROGRAMMABLE 1X-100X,CH1	80009	119-1445-01
	----- -----			-		.(SEE A11 REPL)		
-91	119-1445-02			1		.ATTENUATOR,VAR:PROGRAMMABLE,1X-100X,CH2	80009	119-1445-02
	----- -----			-		.(SEE A12 REPL)		
-92	351-0677-00			2		.GUIDE,MAG CATCH:BLACK POLY	80009	351-0677-00
-93	337-3031-00			1		.SHIELD,ELEC:PRE-AMP	80009	337-3031-00
						.**********(ATTACHING PARTS)**********		
-94	211-0324-00			2		.SCR,ASSEM WSHR:4-40 X 0.188 L,PNH,TORX,MC	01536	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
-95	129-0985-00	B010100	B019999	5		.SPACER,POST:0.350 L,W/4-40 THD THRU	T1288	OBD
	129-0098-00	B020000		5		.POST,ELEC-MECH:0.250 HEX.X0.406 INCH L,BR	80009	129-0098-00
-96	210-0003-00			2		.WASHER,LOCK:#4 EXT,0.015 THK,STL	78189	1104-00-00-0541C
-97	210-0586-00			4		.NUT,PL,ASSEM WA:4-40 X 0.25,STL	83385	ORD BY DESCR
	214-2270-00			2		.SPRING,GROUND:CRT TO SHIELD	80009	214-2270-00
						.**********(ATTACHING PARTS)**********		
	211-0324-00			2		.SCR,ASSEM WSHR:4-40 X 0.188 L,PNH,TORX,MC	01536	ORD BY DESCR
						.**********(END ATTACHING PARTS)*********		
	384-0617-00			1		.SPACER,POST:0.375 L X 0.25 HEX	80009	384-0617-00
	129-0985-00			1		.SPACER,POST:0.350 L,W/4-40 THD THRU	T1288	OBD
-98	214-0973-00			1		.HEAT SINK,ELEC:0.28 X 0.18 OVAL X 0.187"H	80009	214-0973-00
-99	136-0757-00			1		.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-100	136-0727-00			2		.SKT,PL-IN ELEK:MICROCKT,8 CONTACT	09922	DILB8P-108
-101	136-0728-00			1		.SKT,PL-IN ELEK:MICROCKT,14 CONTACT	09922	DILB14P-108
-102	136-0252-07			32		.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-103	131-0993-00			7		.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-104	131-0608-00			142		.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	47357
-105	136-0763-00			3		.SKT,PL-IN ELEK:26 LINE CONT IMPD HYBRID	80009	136-0763-00
	195-3985-00			2		.LEAD,ELECTRICAL:22 AWG,1.7 L,9-N	T0171	OBD
	195-3991-00	B010100	B019999	1		.LEAD,ELECTRICAL:22 AWG, 3.5 L,0-N	T0032	OBD
	195-3991-01	B020000		1		.LEAD,ELECTRICAL:22 AWG, 3.5 L,0-N		
	195-6500-00	B010100	B019999	1		.LEAD,ELECTRICAL:STRD,22 AWG,300V,WHITE,2.	80009	195-6500-00
	195-6500-01	B020000		1		.LEAD,ELECTRICAL:STRD,22 AWG,300V,WHITE,2.	80009	195-6500-01
	175-8010-00	B010100	B019999	1		.CA ASSY,SP,ELEC:5,22 AWG,10.5 L,RIBBON	80009	175-8010-00
	175-8010-01	B020000		1		.CA ASSY,SP,ELEC:5,22 AWG,10.5 L, RIBBON	80009	175-8010-01
	195-6851-00	B010100	B019999	1		.LEAD,ELECTRICAL:BRAIDED,1.65 L	80009	195-6851-00
	195-6851-01	B020000		1		.LEAD,ELECTRICAL:BRAIDED,1.65 L	80009	195-6851-01
	175-2054-00	B011400		1		.WIRE,ELECTRICAL:SOLID,30 AWG,BLACK,KYNAR		
-106	343-0144-00			1		CLAMP,LOOP:0.125 INCH ID,BLK NYLON	95987	1-8-2
						**********(ATTACHING PARTS)**********		
-107	211-0304-00			1		SCREW,MACHINE:4-40 X 0.312,PNH	01536	ORD BY DESCR
						**********(END ATTACHING PARTS)*********		
-108	----- -----			1		CHASSIS,SCOPE:MAIN		
	----- -----			-		(ALSO SEE FIG. 2 RMPL)		

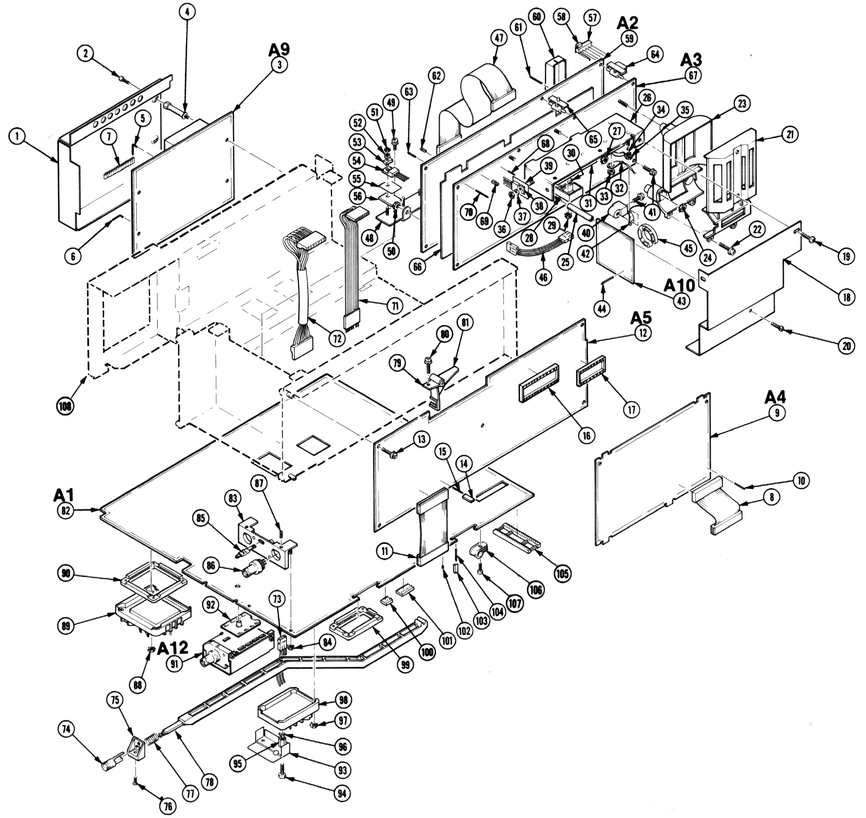


FIG. 3 CIRCUIT BOARDS

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
4-1	015-0227-00			1		ACCESSORY KIT:TWO P6131 PROBE,VOLT W/ACCES	80009	015-0227-00
-2	200-2742-00			1		COVER,PROT:FRONT PANEL	80009	200-2742-00
-3	159-0021-00			1		FUSE,CARTRIDGE:3AG,2A,250V,FAST-BLOW	71400	AGC 2
-4	378-0208-00			1		FILTER,LT,CRT:CLEAR,4.105 X 3.415	80009	378-0208-00
-5	016-0537-00			1		POUCH,ACCESSORY:VINYL,W/ZIPPER	05006	ZIP-6X91D
	016-0692-01			1		POUCH ASSEMBLY:2445/2465	80009	016-0692-01
-6	016-0692-00			1		.POUCH,ACCESSORY:2465/2445	80009	016-0692-00
-7	386-4849-00			1		.PLATRE,MOUNTING:ACCY POUCH,ALUM	80009	386-4849-00
	070-3829-00			1		MANUAL,TECH:SERVICE,2445 OSCILLOSCOPE	80009	070-3829-00
	070-3830-00			1		MANUAL,TECH:OPERATORS,2445 OSCILLOSCOPE	80009	070-3830-00
	070-4178-00			1		CARD,INFO:REF	80009	070-4178-00
	070-4366-00			1		SHEET,TECHNICAL:INSTR,016-0691-00 RACK	80009	070-4366-00
	070-4180-00			1		CARD,INFO:REF	80009	070-4180-00
						OPTIONAL ACCESSORIES		
	015-0227-00					ACCESSORY KIT:TWO P6131 PROBE,VOLT W/ACCES	80009	015-0227-00
	016-0720-00					COVER,PROT:NYLON	80009	016-0720-00
	346-0058-00					FASTENER,STRAP:CARRYING	80009	346-0058-00
	346-0199-00					STRAP,CARRRYING:2213A		
	----- -----					(OPT A5 SWITZERLAND)		
	161-0104-06			1		CABLE ASSY,PWR:3 X 0.75MM SQ,220V,98.0L	S3109	ORD BY DESCR
	----- -----					(EUROPEAN OPT.A1)		
	161-0104-07					CABLE ASSY,PWR:3 X 0.75MM SQ,240V,98.0 L	S3109	ORD BY DESCR
	----- -----					(UNITED KINGDOM OPT. A2)		
	161-0104-05					CABLE ASSY,PWR:3,18 AWG,240V,98.0 L	S3109	ORD BY DESCR
	----- -----					(AUSTRALIAN OPT.A3)		
	161-0104-08					CABLE ASSY,PWR:3,18 AWG,240V,98.0 L	T1105	ORD BY DESCR
	----- -----					(NORTH AMERICAN OPT.A4)		

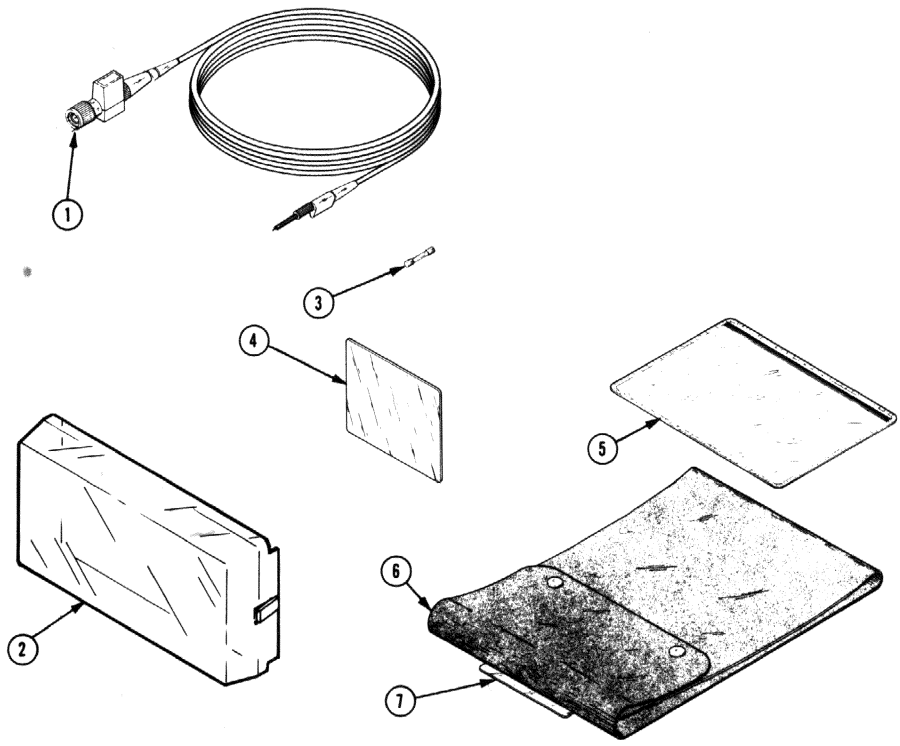


Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5	Name & Description	Mfr Code	Mfr Part Number
						STANDARD ACCESSORIES		
4-1	010-6131-01			2		PROBE,VOLTAGE:P6131,10X W/ACCESSORIES	80009	010-6131-01
-2	200-2742-00			1		COVER,PROT:FRONT PANEL	80009	200-2742-00
-3	159-0098-00			1		FUSE,CARTRIDGE:DIN,1.6A	75915	212 01.6
-4	378-0208-00			1		FILTER,LT,CRT:CLEAR,4.105 X3.415	80009	378-0208-00
-5	016-0537-00			1		POUCH,ACCESSORY:VINYL,W/ZIPPER	05006	ZIP-6X91D
	016-0692-01			1		POUCH ASSEMBLY:2445/2465	80009	016-0692-01
-6	016-0692-00			1		. POUCH,ACCESSORY:2465/2445	80009	016-0692-00
-7	386-4849-00			1		. PLATE,MOUNTING:ACCY POUCH,ALUM	80009	386-4849-00
	070-3829-00			1		MANUAL,TECH:SERVICE,2445 OSCILLOSCOPE	80009	070-3829-00
	070-3830-00			1		MANUAL,TECH:OPERATORS,2445 OSCILLOSCOPE	80009	070-3830-00
	070-4180-00			1		CARD,INFO:REF	80009	070-4180-00
						OPTIONAL ACCESSORIES		
4-1	010-6131-01					PROBE,VOLTAGE:P6131,10X W/ACCESSORIES	80009	010-6131-01
	016-0720-00					COVER,PROT:NYLON	80009	016-0720-00
	346-0058-00					FASTENER,STRAP:CARRYING	80009	346-0058-00
	161-0104-05					CABLE ASSY,PWR:3,18 AWG,240V,98.0 L	86221	OBD
	----- -----					(AUSTRALIAN)		
	161-0104-06					CABLE ASSY,PWR:3 X 0.75MM SQ,220V,98.0L	80126	OBD
	----- -----					(EUROPEAN)		
	161-0104-07					CABLE ASSY,PWR:3 X 0.75MM SQ,240V,98.0 L	80126	OBD
	----- -----					(UNITED KINGDOM)		
	159-0172-00					. FUSE,CARTRIDGE:TYPE C,13 AMP	S3629	PCC-1089
	161-0104-08					CABLE ASSY,PWR:3,18 AWG,240V,98.0 L	80126	OBD

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 12-14-83 Change Reference: C4/1083 REV

Product: 2445 SERVICE Manual Part No.: 070-3829-00

DESCRIPTION

NOTE

The following changes are in effect for all instruments serial numbered B020000 and above (unless noted otherwise).

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A1	670-7285-06	CKT BOARD ASSY: MAIN (OPTIONS 01,05,06,09 OR 1B ONLY)		M52083
A1	670-7285-08	CKT BOARD ASSY: MAIN (STANDARD & ALL OTHER OPTIONS ONLY)		M52083
A2 & A3	672-1037-02	CKT BOARD ASSY: LV/POWER SUPPY MODULE		PC132
A6	672-1039-02	CKT BOARD ASSY: FR PNL MODULE		PC141
A1C102	290-0973-00	CAP,FXD,ELCTLT: 100UF,20%,25VDC	B010800	PC93
A1C203	281-0862-00	CAP,FXD,CER DI: 0.001UF,+80-20%,100V		M51123
A1C203	283-0811-00	CAP,FXD,CER DI: 0.01UF,20%,100V (OPTIONS 01,05,06,09, OR 1B ONLY)	B020115	PC20
A1C513	283-0479-00	CAP,FXD,CER DI: 0.47UF,+80-20%,25V		PC132
A1C537	283-0479-00	CAP,FXD,CER DI: 0.47UF,+80-20%,25V		PC132
A1C660	281-0851-00	CAP,FXD,CER DI: 180PF,5%,100V		PC132
A1C731	290-0944-00	CAP,FXD,ELCTLT: 220UF,+50-10%,10V	B010800	PC93
A1C912	283-0421-00	CAP,FXD,CER DI: 0.1UF,+80-20%,50V		PC132
A1Q624	151-1025-00	TRANSISTOR: FET,N-CHAN,SI		PC132
A1R155	321-0206-00	RES,FXD,FILM: 1.37K OHM,1%,0.125W		PC132
A1R194	315-0103-00	RES,FXD,CMPSN: 10K OHM,5%,0.25W		PC132
A1R403	311-2099-00	RES,VAR,NONWIR: TRMR,500 OHM,10%,0.5W		PC132
A1R456	321-0329-00	RES,FXD,FILM: 26.1K OHM,1%,0.125W		M51123
A1R461	321-0139-00	RES,FXD,FILM: 274 OHM,1%,0.125W		M51123
A1R462	321-0201-00	RES,FXD,FILM: 1.21K OHM,1%,0.125W		M51123
A1R463	321-0193-00	RES,FXD,FILM: 1K OHM,1%,0.125W		M51123
A1R622	321-0255-00	RES,FXD,FILM: 4.42K OHM,1%,0.125W		M51123
A1R736	321-0197-00	RES,FXD,FILM: 1.1K OHM,1%,0.125W		PC132
A1R743	315-0102-00	RES,FXD,CMPSN: 1K OHM,5%,0.25W		PC132
A1R802	315-0821-00	RES,FXD,CMPSN: 820 OHM,5%,0.25W		M51123
A1R803	315-0222-00	RES,FXD,CMPSN: 2.2K OHM,5%,0.25W		M51123
A1R805	311-1242-00	RES,VAR,NONWW: TRMR,200K OHM,0.5W		PC132
A1R941	315-0561-00	RES,FXD,CMPSN: 560 OHM,5%,0.25W		PC132
A1U500	155-0239-01	MICROCKT,LINEAR: TRIGGER(OPTION 01,05,06,09,1B)		PC15
A1U950	155-0242-01	MICROCKT,LINEAR: Z AXIS AUTOFOCUS	B011100	PC111
A4U2930	160-1631-02	MICROCKT,DGTL: 4096 X 8 EPROM,PRGM		PC137
A6DS3329	150-1105-00	LT EMITTING DIODE: YELLOW,30MA		PC154
A6R3350	307-0695-00	RES NTWK,FXD,FI: 9,150 OHM,2%,0.2W EA		
A6S3185	260-2108-01	SWITCH,PUSH: SPDT,0.1A,125VAC		PC141
A6W651	175-8419-00	CA ASSY,SP,ELEC: 26,28 AWG,2.5L,RIBBON		
A6W652	175-8418-00	CA ASSY,SP,ELEC: 20,36 AWG,8.0L,RIBBON		
A9R1922	315-0331-03	RES,FXD,CMPSN: 330 OHM,5%,0.25W	B010800	PC130

REMOVE:

A1C303	281-0547-00	CAP,FXD,CER DI: 2.7PF,10%,500V		PC132
A1C312	281-0547-00	CAP,FXD,CER DI: 2.7PF,10%,500V		PC132
A1C450	283-0421-00	CAP,FXD,CER DI: 0.1UF,+80-20%,50V		PC132
A1C454	283-0421-00	CAP,FXD,CER DI: 0.1UF,+80-20%,50V		PC132
A1R121	315-0121-00	RES,FXD,CMPSN: 120 OHM,5%,0.25W		PC132
A1R216	315-0121-00	RES,FXD,CMPSN: 120 OHM,5%,0.25W		PC132

DESCRIPTION

REPLACEABLE ELECTRICAL PARTS LIST CHANGES (cont)

REMOVE (cont)

A1R511	321-0320-00	RES,FXD,FILM: 21K OHM,1%,0.125W	PC132
A1R512	321-0293-00	RES,FXD,FILM: 11K OHM,1%,0.125W	PC132
A1R737	321-0255-00	RES,FXD,FILM: 4.42K OHM,1%,0.125W	PC132
A1W194	131-0566-00	BUS CONDUCTOR: DUMMY RES,2.375,22AWG	PC132
A3R1101	307-0103-00	RES,FXD,CMPSN: 2.7 OHM,5%,0.25W	PC136
A3R1102	307-0103-00	RES,FXD,CMPSN: 2.7 OHM,5%,0.25W	PC136
A6R3327	315-0151-00	RES,FXD,CMPSN: 150 OHM,5%,0.25W	PC154

ADD:

A1C405	281-0122-00	CAP,VAR,CER DI: 2.5-9PF,100V	M50513
A1C967	281-0783-00	CAP,FXD,CER DI: 0.1UF,20%,100V	PC132
A1C980	281-0421-00	CAP,FXD,CER DI: 0.1UF,20%,50V	M50513
A1CR503	152-0141-02	SEMICOND DVC,DI: SW,SI,30V,150MA	PC132
A1R405	315-0470-00	RES,FXD,CMPSN: 47 OHM,5%,0.25W	M50513
A1R431	315-0470-00	RES,FXD,CMPSN: 47 OHM,5%,0.25W	M50513
A1R466	321-0275-00	RES,FXD,FILM: 7.15K OHM,1%,0.125W	M51123
A1R503	315-0103-00	RES,FXD,CMPSN: 10K OHM,5%,0.25W	PC132
A1R504	315-0103-00	RES,FXD,CMPSN: 10K OHM,5%,0.25W	PC132
A1R901	315-0112-00	RES,FXD,CMPSN: 1.1K OHM,5%,0.25W	PC132
A1R902	315-0112-00	RES,FXD,CMPSN: 1.1K OHM,5%,0.25W	PC132
A1R903	315-0472-00	RES,FXD,CMPSN: 4.7K OHM,5%,0.25W	PC132
A1R939	315-0332-00	RES,FXD,CMPSN: 3.3K OHM,5%,0.25W	PC132
A1R942	321-0256-00	RES,FXD,FILM: 4.53K OHM,1%,0.125W	PC132
A2J203	131-2925-00	CONN,RCPT,ELEC: CKT BD,1 X 6,0.2 SPACING	
A3J303	131-2926-00	CONN,RCPT,ELEC: CKT BD,1 X 2,0.2 SPACING	
A3W1101	131-0566-00	BUS CONDUCTOR: DUMMY RES,2.375,22AWG	PC136
A3W1102	131-0566-00	BUS CONDUCTOR: DUMMY RES,2.375,22AWG	PC136
A6DS3357	150-1109-00	LT EMITTING DIODE: GREEN,30MA	PC154
A6DS3356	150-1109-00	LT EMITTING DIODE: GREEN,30MA	PC154
A6DS3355	150-1109-00	LT EMITTING DIODE: GREEN,30MA	PC154
A6DS3332	150-1109-00	LT EMITTING DIODE: GREEN,30MA	PC154
A6DS3328	150-1105-00	LT EMITTING DIODE: YELLOW,30MA	PC154
A6R3325	315-0151-00	RES,FXD,CMPSN: 150 OHM,5%,0.25W	PC154
A6R3329	315-0151-00	RES,FXD,CMPSN: 150 OHM,5%,0.25W	PC154

REPLACEABLE MECHANICAL PARTS LIST CHANGES

CHANGE TO:

FIG. #	PART #	QTY	DESCRIPTION	
1-7	101-0082-01	1	TRIM,DECORATIVE: FRONT,PLASTIC	PC139
2-28	131-0608-00	10	TERMINAL,PIN: 0.365 L X 0.025 PH BRZ GOLD	
2-34	354-0632-01	1	RING,MOUNTING: 5.41 X 4.18,BRASS	PC142
2-35	333-2915-01	1	PANEL,FRONT:	PC142
2-39	386-4713-01	1	PLATE,REAR: POWER SUPPLY	PC143
2-110	441-1618-01	1	CHASSIS,SCOPE: MAIN	PC139
3-65	361-1132-01	1	SPACER,CKT BD: A POLYCARBONATE	PC143

Under item 2-28, change the quantity of the following parts:

Change the quantity of 352-0639-00 to 1 (one).
Change the quantity of 352-0641-00 to 2 (two).

Add 352-0692-00	2	HOLDER,LED: EIGHT,BLACK	

ADD the following items to the ATTACHING PARTS for item 2-39.

343-1099-00	1	RTNR,POWER SPLY: LOW VOLTAGE,FRONT	PC143
337-3059-00	1	SHIELD,ELEC: LOW VOLTAGE POWER SUPPLY	PC143

DESCRIPTION

DIAGRAM CHANGES

Contained in this insert is a new layout of the A1 board (Main Board) along with a new parts locator table which are to be used with instruments serial numbered B020000 and above.

DIAGRAM 3 FRONT PANEL CONTROLS

For serial numbers B020000 and above use the partial Diagram 3 contained in this insert when referring to the STATUS LEDS. PC154

Also contained in this insert is a new layout of the A6 board (Front Panel) along with a new parts locator table which are to be used for instruments serial numbered B020000 and above.

DIAGRAM 4 ATTENUATORS & PREAMPS

Change C203 (location 8M) to a 0.001μF capacitor. M51123

Change R456 (location 7S) to a 26.1KΩ resistor. M51123

Change R461 (location 9N) to a 274Ω resistor. M51123

Change R462 (location 9P) to a 1.21KΩ resistor. M51123

Change R463 (location 8P) to a 1KΩ resistor. M51123

Change the connections of J100-5 and J100-6 to read NC (No Connection) at location 8K. M51123

Remove C303 (location 11C) and connect R303 to ground. PC132

Remove C312 (location 10C) and connect R312 to ground. PC132

Remove C450 (location 2P) from pins 6 & 7 of U450B. PC132

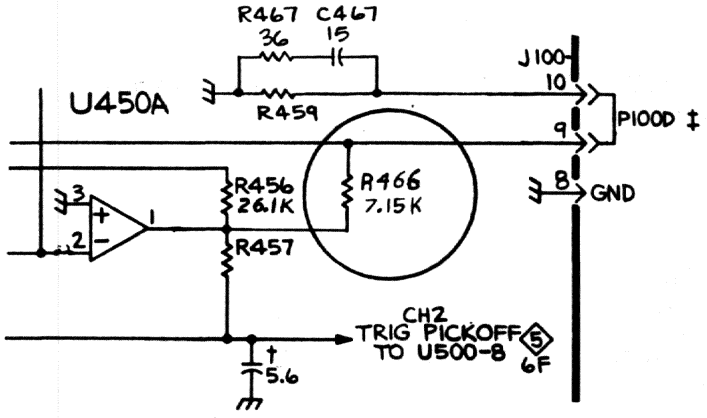
Remove C454 (location 7P) from pins 1 & 2 of U450A. PC132

Remove R121 (location 2M) and connect U100 pin 17 to the remaining circuitry. PC132

Remove R216 (location 7L) and connect U200 pin 17 to the remaining circuitry. PC132

Add R431 (47Ω) in series with C460 (location 8P) to ground. M50513

Add R466(7.15KΩ) to U450A pin 1 (location 7P) as shown here. M51123

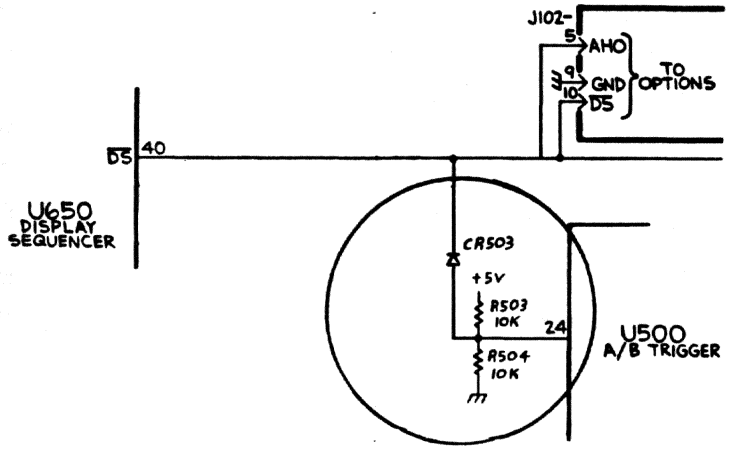


DESCRIPTION

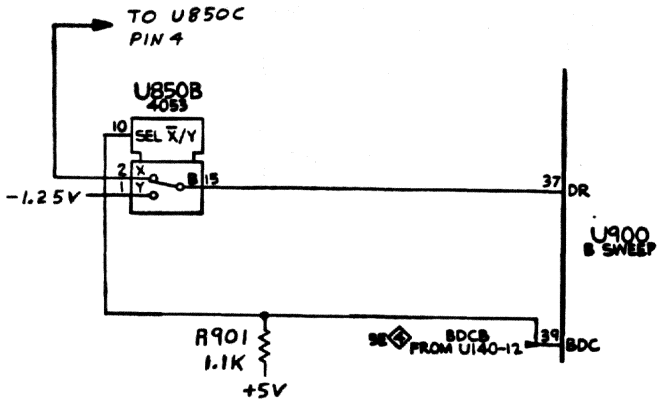
DIAGRAM CHANGES (cont)

DIAGRAM 5 DISPLAY SEQUENCER, TRIGGERING, A & B SWEEPS

Change C513 (location 8E) to a 0.47μF capacitor.	PC132
Change C537 (location 9E) to a 0.47μF capacitor.	PC132
Change C660 (location 4C) to a 180pF capacitor.	PC132
Change C912 (location 5K) to a 0.1μF capacitor.	PC132
Change R155 (location 3C) to a 1.37KΩ resistor.	PC132
Change R736 (location 2K) to 1.1KΩ resistor.	PC132
Change R743 (location 4J) to a 1KΩ resistor.	PC132
Change R941 (location 7M) to a 560Ω resistor.	PC132
Remove R511 & R512 (location 4F) and connect U500 pin 15 directly to U650 pin 13.	PC132
Remove R737 (location 2K).	PC132
Remove W194 (location 3J) and connect R194 directly to U170 pin 6.	PC132
Add R942 (4.53KΩ) from U980D pin 13 (location 6M) to −15V.	PC132
Add CR503, R503, and R504 to U500 pin 24 (lcation 4F) as shown here.	PC132



Disconnect pins 1, 2, and 10 of U850B (location 6J) and connect them as shown here. Also add R901 (1.1KΩ) as shown. PC132

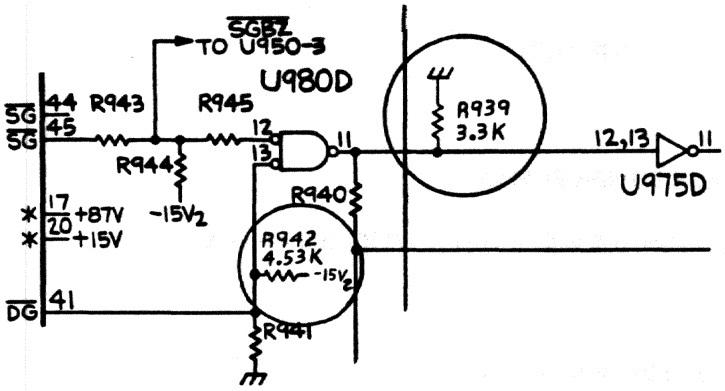


DESCRIPTION

DIAGRAM CHANGES (cont)

DIAGRAM 5 DISPLAY SEQUENCER, TRIGGERING, A & B SWEEPS (cont)

Add R939 (3.3KΩ) and R942 (4.53KΩ) to U980D (location 6M) as shown here. PC132



Replace J101 pins 9 & 10 with P109 & J109 pins 1 & 2 as shown here. PC132
J101 pins 9 & 10 become NC (No Connection).

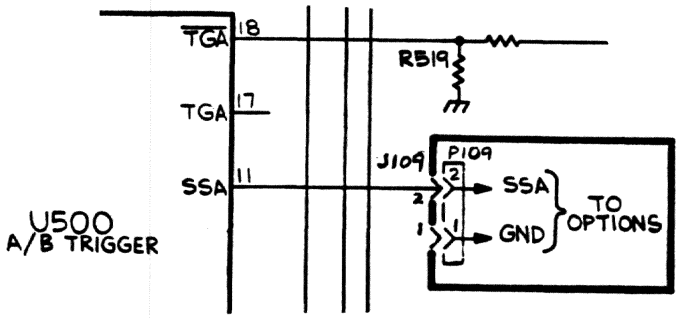
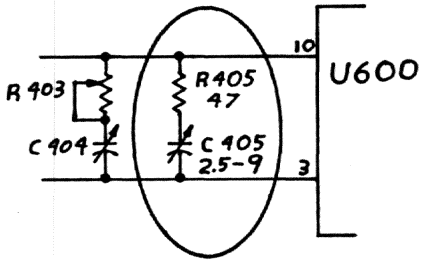


DIAGRAM 6 CHANNEL SWITCH AND OUTPUT AMPLIFIERS

Change R403 (location 2J) to a 500Ω variable resistor. PC132
Change R622 (location 4N) to a 4.42KΩ resistor. M51123
Change R802 (location 7N) to a 820Ω resistor. M51123
Change R803 (location 7N) to a 2.2KΩ resistor. M51123

Add R902 (1.1KΩ) from U850A pin 11 (location 8M) to +5V. PC132
Add R903 (4.7KΩ) from U980C pin 8 (location 7H) to +5V. PC132

Add C405 (2.5-9pF) and R405 (47Ω) to U600 as shown here. M50513



DESCRIPTION

DIAGRAM CHANGES (cont)

DIAGRAM 8 HIGH VOLTAGE SUPPLY AND CRT

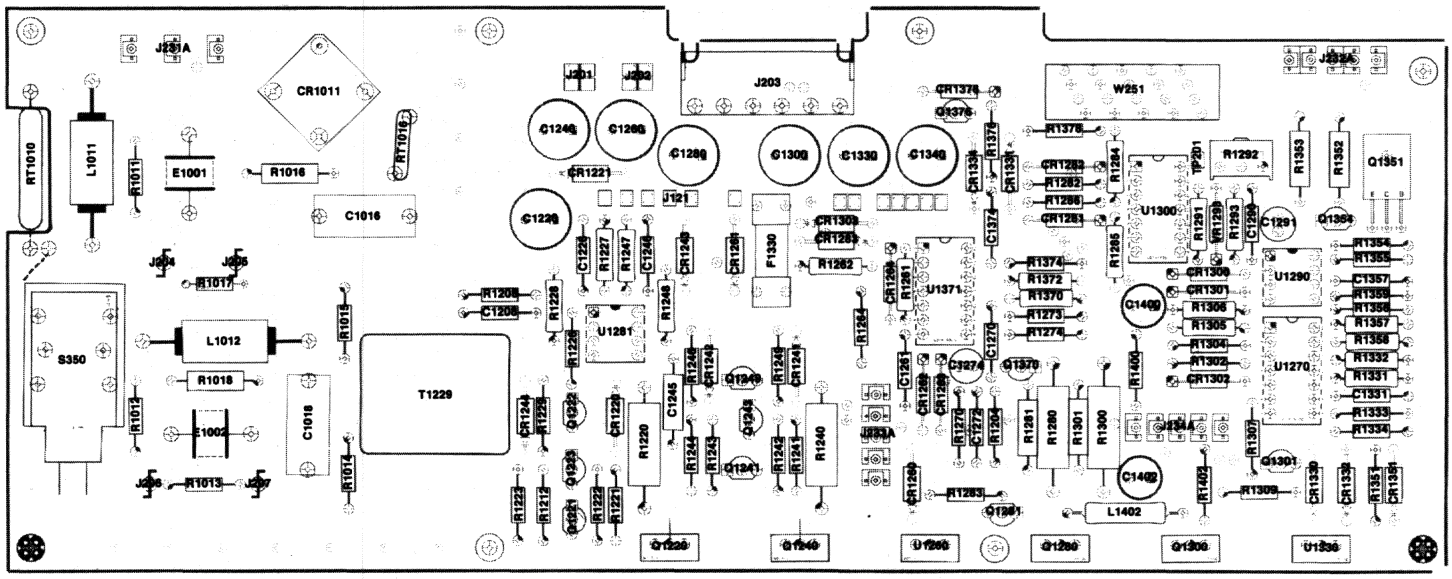
Change R1922 (location 7E) to a 330Ω resistor.	B010800	PC130

DIAGRAM 9 LOW-VOLTAGE POWER SUPPLY

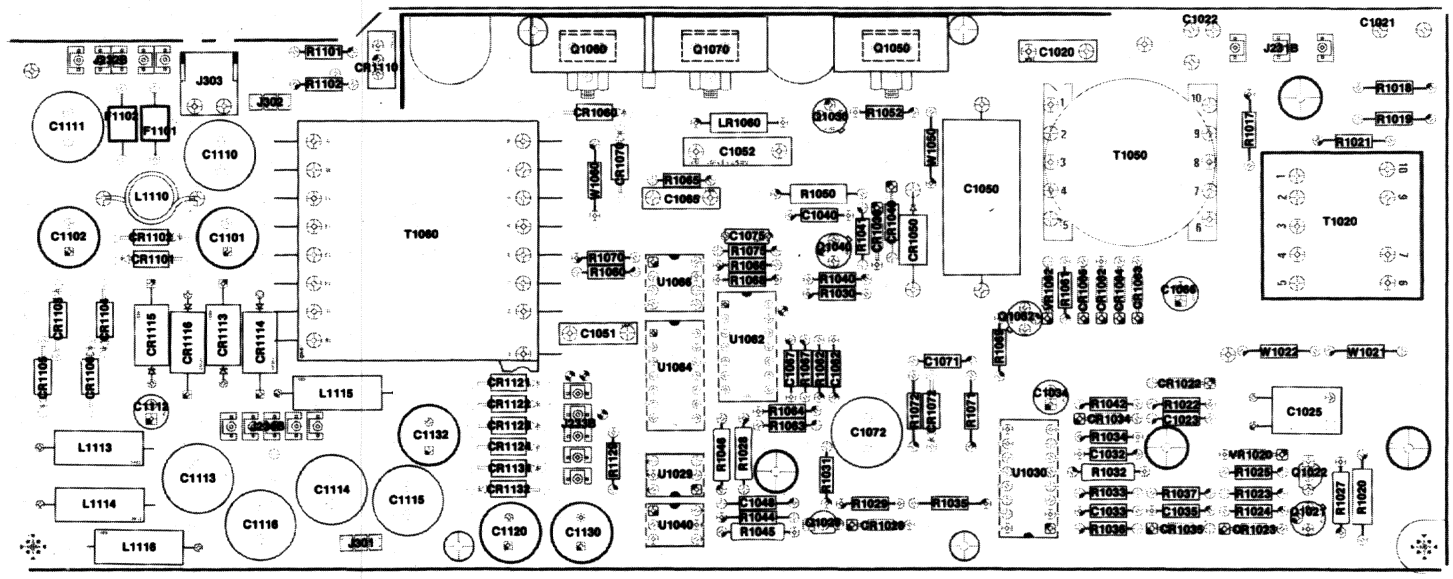
Replace R1101 & R1102 (location 6P) with W1101 & W1102 (0Ω jumpers).		PC132

DIAGRAM 11 POWER DISTRIBUTION A

Add C967 (0.1μF) in parallel with C966 (location 1M).		PC132
Add C980 (0.1μF) in parallel with C675, C811, C943, and C958 (location 3M).		PC134
Change C102 (location 8A) to a 100μF capacitor.	B010800	PC93



A2 REGULATOR BOARD
(SN B020000 AND ABOVE)



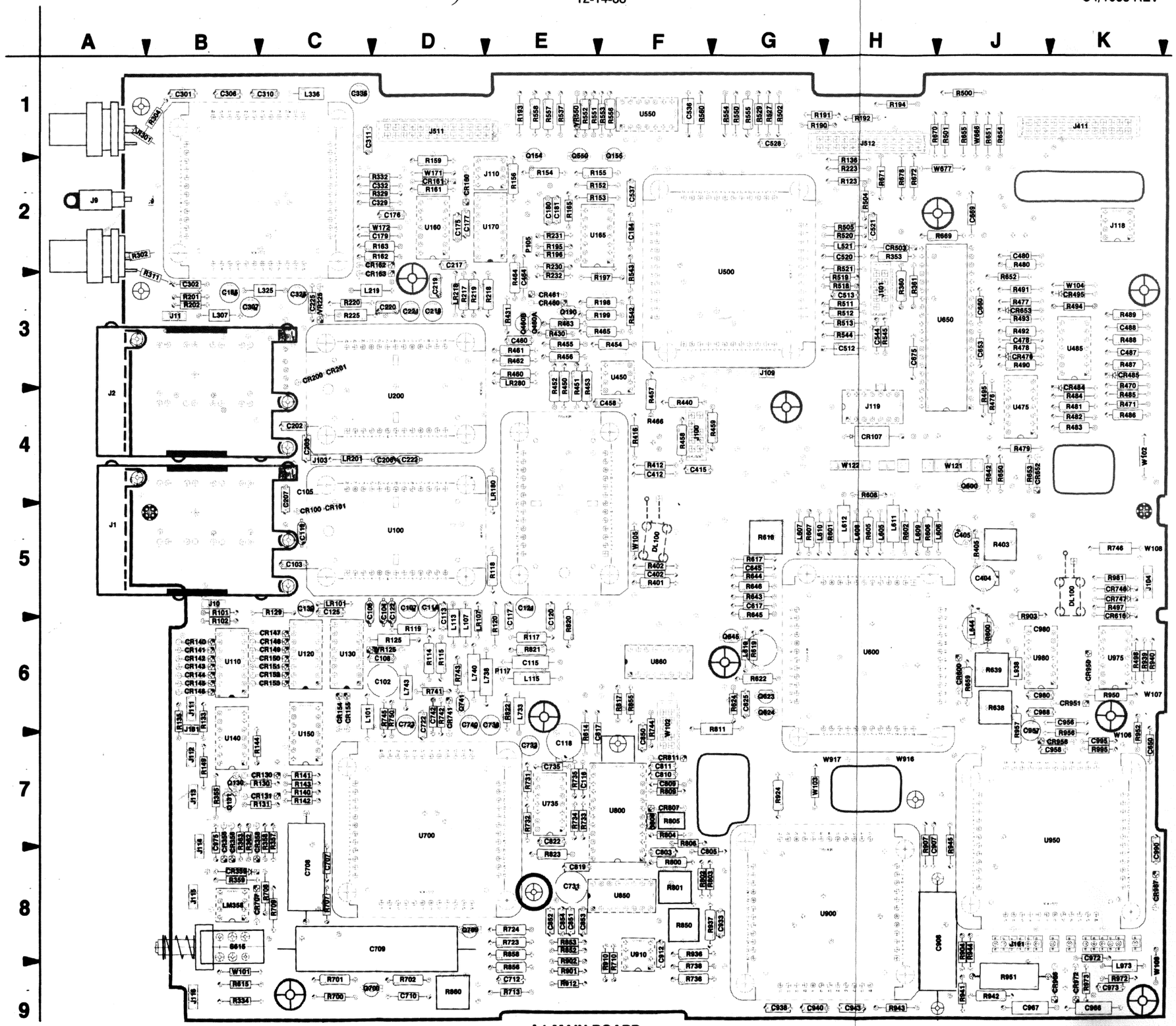
A3 INVERTER BOARD
(SN B020000 AND ABOVE)

A1—MAIN BOARD
(SN B020000 AND ABOVE)

CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION
C100	4	4C	C669	5	2J	CR460	4	3E	L619	6	6G	R192	4	1H	R488	6	3K
C102	11	6D	C675	11	3H	CR461	4	3E				R193	4	1E	R489	6	3K
C103	4	5C	C707	5	8C	CR476	6	3J				R194	4	1H	R490	6	3J
C104	4	5D	C708	5	8C	CR484	6	3K	L644	6	6J	R195	4	2E	R491	6	3J
C105	4	4C	C709	5	8D	CR485	6	3K	L733	11	6E	R196	4	2E	R492	6	3J
C106	11	5D	C710	11	9D	CR495	6	3K	L738	11	6E	R197	4	3F	R493	6	3J
C107	11	5D	C712	5	9E	CR503	5	2H	L740	11	6D	R198	4	3F	R494	6	3K
C108	5	6D	C722	11	6D	CR600	6	6J	L743	11	6D	R199	4	3F	R495	6	4J
C108	11	6D	C723	11	6D	CR616	6	6K	L938	11	6J	R200	4	3C	R497	6	5K
C112	4	6D	C731	11	8E	CR652	5	4J	L973	11	9K	R201	4	3B	R498	6	6K
C113	11	6D	C733	11	7E	CR653	5	3J				R202	4	3B	R500	6	1J
C114	11	5D	C735	6	7E	CR707	5	8B	LR101	11	5C				R501	6	1J
C115	4	6E	C738	11	6E	CR741	5	6D	LR107	11	6D	R217	4	3D	R502	4	1G
C116	4	7E	C740	11	6D	CR746	5	5K	LR180	4	4E	R218	4	3E	R503	5	2H
C117	4	5E	C742	5	6D	CR747	5	5K	LR201	11	4C	R219	4	3D	R504	5	2H
C118	4	7E	C803	6	8F				LR218	11	3D	R220	11	3C	R511	5	3H
C119	11	5C	C805	6	8F	CR807	11	7F	LR280	4	3E	R223	4	2H	R512	5	3H
C120	11	5E	C806	6	7F	CR811	11	7F				R225	11	3C	R513	5	3H
C121	11	5E	C808	6	7F	CR950	5	6K	P100	4	4F	R230	4	2E	R518	5	3H
C122	4	5D	C809	6	7F	CR951	5	6K	P101	5	3H	R231	4	2E	R519	5	3H
C125	11	5C	C810	11	7F	CR956	6	7K	P102	5	7F	R232	4	2E	R520	5	2H
C130	4	5C	C811	11	7F	CR966	6	9K	P103	4	4C	R301	4	1A	R521	5	2H
C175	4	2D	C817	6	7F	CR972	6	9K	P106	6	7K	R302	4	2A	R527	5	1G
C176	4	2D	C819	11	8E	CR987	11	8K	P107	5	6K				R529	5	1G
C177	4	2D	C822	6	7E				P108	5	5K	R304	4	1B	R537	5	1E
C179	4	2D	C850	11	7F	DL100	6	5F	P121	11	4J	R311	4	2A	R542	5	3F
C180	5	2E	C851	5	8E	DL100	6	5K	P122	5	4H				R543	5	2F
C181	5	2E	C852	5	8E				P122	11	4H	R329	4	2D	R544	5	3H
C184	4	2F	C853	5	8E	J9	5	2A	P141	6	9K	R332	4	2D	R545	5	3H
C185	4	3B	C854	5	8E	J10	4	5B				R334	5	9B	R550	5	1G
C200	4	3C	C907	5	7H	J11	4	3B	Q130	4	7B	R353	5	2H	R551	5	1E
C202	4	4C	C908	5	8J	J100	4	4F	Q131	4	7B	R355	5	7B	R552	5	1E
C203	4	4C	C912	5	9E	J101	5	3H	Q154	5	1E	R357	5	7C	R553	5	1F
C205	4	3C	C933	11	8G	J102	5	7F	Q155	5	1F	R358	5	7C	R554	5	1G
C207	11	4C	C940	11	9G	J104	5	5K	Q460	4	3E	R360	5	3H	R556	5	1F
C217	4	2D	C943	11	9H	J105	4	2E	Q550	5	1E	R361	5	3H	R557	5	1E
C218	11	3D	C956	6	6K	J109	5	3G	Q600	6	4J	R362	5	7B	R558	5	1E
C219	11	3D	C957	6	7J	J110	4	2E	Q623	6	6G	R363	5	7B	R560	5	1F
C220	11	3D	C958	11	7K	J111	4	6B	Q624	6	6G	R401	6	5F	R600	6	6J
C221	11	3D	C966	11	9K	J112	8	7B	Q645	5	6G	R402	6	5F	R601	6	5H
C222	4	4D	C967	11	9J	J113	5	7B	Q700	11	9C	R403	6	5F	R602	6	5H
C225	11	3C	C972	6	9K	J114	8	8B	Q709	5	8D				R605	6	5H
C301	4	1B	C973	11	9K	J115	8	8B	Q741	5	6D	R412	6	4F	R606	6	5H
C302	4	3B	C975	8	7B	J116	5	9B				R416	6	4F	R607	6	5G
C306	5	1B	C980	11	6J	J117	4	6E	R100	4	4C				R608	6	4H
C307	11	3B	C988	11	6K	J118	5	2K	R101	4	5B	R430	4	3E	R614	6	7E
C310	4	1C	C990	11	8K	J119	11	4H	R102	4	6B	R440	4	3F	R615	6	9B
C311	4	1C	C995	6	7K	J181	4	6B	R114	4	6D	R450	4	3E	R617	6	5G
C325	11	3C				J191	6	8K	R115	4	6D	R451	4	3E	R618	6	5G
C329	4	2D	CR100	4	5C	J191	11	8K	R117	4	6E	R452	4	3E	R619	6	6G
C332	4	2D	CR101	4	5C	J411	5	1K	R118	4	5E	R453	4	3E	R622	6	6G
C336	11	1C	CR107	11	4H	J411	6	1K	R119	4	6D	R454	4	3F	R624	6	6G
C402	6	5F	CR130	4	7B	J411	11	1K	R120	11	5E	R455	4	3E	R638	6	6J
			CR131	4	7B	J511	4	1D				R456	4	3E	R639	6	6J
C404	6	4F	CR140	4	6B	J511	5	1D	R123	4	2H	R457	4	3F	R642	6	4J
C412	6	4F	CR141	4	6B	J511	6	1D	R125	11	6D	R458	4	4F	R643	5	5G
C415	11	4F	CR142	4	6B	J511	11	1D	R129	4	5C	R459	4	4G	R644	5	5G
C458	11	3F	CR143	4	6B	J512	4	1H	R130	4	7C	R460	4	3E	R645	5	5G
C460	4	3E	CR144	4	6B	J512	5	1H	R131	4	7C	R461	4	3E	R646	5	5G
C464	4	3E	CR145	4	6B	J512	6	1H	R133	4	6B	R462	4	3E	R650	6	4J
			CR146	4	6B	J512	11	1H	R135	4	6B	R463	4	3E	R651	5	1J
			CR147	4	6C				R136	4	1H	R464	4	3E	R652	5	3J
C478	6	3J	CR148	4	6C	L101	11	6D	R140	4	7C	R465	4	3F	R653	5	4J
C480	11	2J	CR149	4	6C	L107	11	6D	R141	4	7C	R466	4	4F	R654	5	1J
C487	6	3K	CR150	4	6C	L113	11	6D	R142	4	7C				R655	5	1J
C488	6	3K	CR151	4	6C	L115	4	6E	R143	4	7C				R659	6	6J
C512	5	3H	CR152	4	6C	L219	11	3D	R144	4	7C	R470	6	3K	R669	5	2J
C513	5	3H	CR153	4	6C	L307	11	3B	R149	4	7B	R471	6	4K	R670	5	1H
C520	5	2H	CR154	4	6C	L325	11	3C	R152	5	2F	R476	6	4J	R671	5	2H
C521	11	2H	CR155	4	6C	L336	11	1C	R153	5	2F	R477	6	3J	R672	5	2H
C528	5	1G	CR160	4	2D	L403	6	4F	R154	5	2E	R478	6	3J	R678	5	2H
C536	5	1F	CR161	4	2D	L521	11	2H	R155	5	2F	R479	6	4J	R700	11	9C
C537	5	2F	CR162	4	2D	L605	6	5H	R156	5	2E	R480	6	4J	R701	11	9C
C544	5	3H	CR163	4	2D	L606	6	5J	R159	4	2D	R481	6	4K	R702	11	9D
C617	6	5G	CR200	4	3C	L607	6	5G	R161	4	2D	R482	6	4K	R707	5	8C
C625	6	6G	CR201	4	3C	L608	6	5H	R162	4	2D	R483	6	4K	R708	5	8C
C645	5	5G	CR355	5	7B	L609	6	5H	R163	4	2D	R484	6	4K	R709	5	8C
C650	5	7K	CR356	5	7B	L610	6	5H	R165	5	2E	R485	6	4K	R710	5	9F
C653	5	3J	CR358	5	7B	L611	6	5H	R190	4	1G	R486	6	4K	R713	5	9E
C660	5	3J	CR359	5	8B	L612	6	5H	R191	4	1G	R487	6	3K	R723	5	8E

A1—MAIN BOARD (cont)
(SN B020000 AND ABOVE)

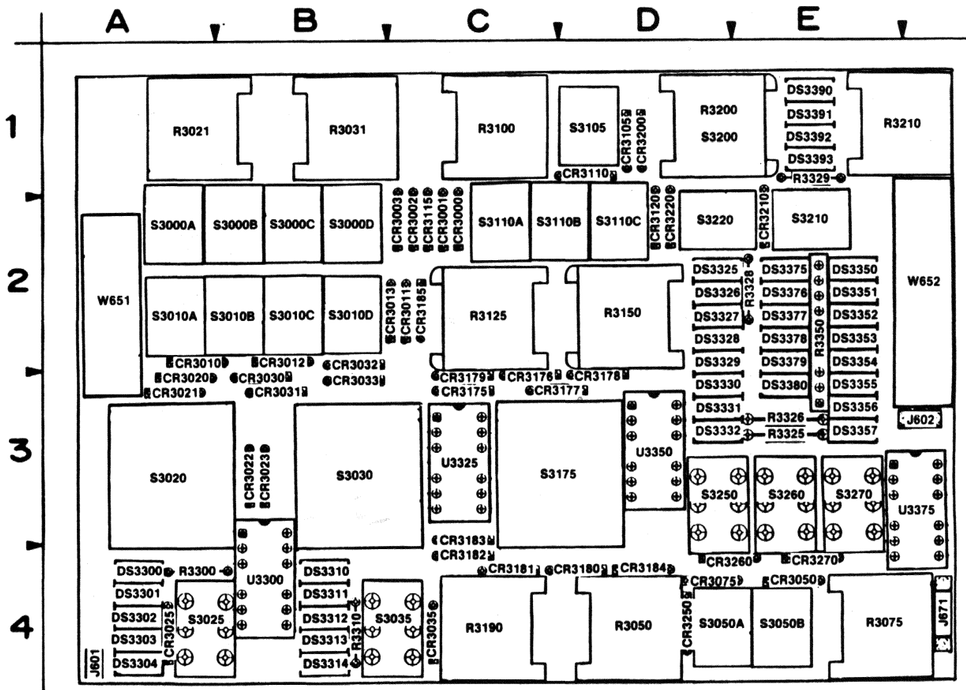
CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION	CIRCUIT NUMBER	SCHEM NUMBER	BOARD LOCATION
R724	5	8E	U160	4	2D
R731	6	7E	U160	11	2D
R732	6	7E	U165	4	2E
R733	6	7E	U165	5	2E
R734	6	7E	U165	11	2E
R735	6	7E	U170	4	2E
R736	5	9F	U170	11	2E
			U200	4	4D
R738	5	9F	U200	11	4D
R741	5	6D	U300	4	2B
R742	5	6D	U300	11	2B
R743	5	6D	U350	5	8B
R744	5	7F	U350	11	8B
R745	5	6D	U400	6	4E
R746	5	5K	U400	11	4E
R750	5	6D	U450	4	3F
			U450	11	3F
			U475	6	4J
			U485	6	3K
			U500	11	3G
R800	6	8F	U550	5	1F
R801	6	8F	U600	6	6H
R802	6	8G	U600	11	6H
R804	6	7F	U650	5	3J
R805	6	7F	U650	11	3J
R806	6	7F	U700	5	7D
R809	6	7F	U700	11	7D
R811	11	7G	U735	6	7E
R817	6	6F	U800	6	7F
R820	6	6E	U800	11	7F
R821	6	6E	U850	5	8F
R822	6	6E	U850	6	8F
R823	6	8E	U850	11	8F
R850	6	8F	U860	5	6F
R853	5	8E	U860	11	6F
R855	6	6F	U900	5	8H
R856	6	9E	U900	11	8H
R858	6	8E	U910	5	8F
R860	6	9D	U910	11	8F
R901	5	9E	U950	6	7K
R902	6	8E	U950	11	8K
R903	6	5J	U975	5	6K
R904	5	8J	U975	6	6K
R907	5	7H	U975	11	6K
R910	5	8F	U980	5	6J
R912	5	9E	U980	6	6J
R924	5	7G	U980	11	6J
R936	5	8F			
R937	5	8G	VR125	11	6D
R939	5	6K	VR225	11	3C
R940	5	6K	VR550	5	1E
R941	5	9J			
R942	5	9J	W101	11	9B
R943	5	9H	W102	11	4K
R944	5	8J	W103	11	7G
R945	5	8J	W104	11	3K
R950	5	6K	W105	11	5F
R951	11	9J	W106	6	7K
R952	5	7K	W107	5	6K
R956	6	7K	W108	5	5K
R957	6	7J	W109	11	9K
R972	6	9K	W121	11	4J
R973	6	9K	W122	5	4H
R981	5	5K	W122	11	4H
R995	6	7K	W141	6	9K
			W171	4	2D
S615	6	8B	W172	4	2D
			W666	5	1J
U100	4	5D	W677	5	2J
U100	11	5D	W916	6	7H
U110	4	6B	W917	6	7H
U110	11	6B			
U120	4	6C	W919	6	7F
U120	11	6C			
U130	4	6C			
U130	11	6C			
U140	4	6B			
U140	11	6B			
U150	4	6C			
U150	11	6C			



FRONT PANEL CONTROLS DIAGRAM 3

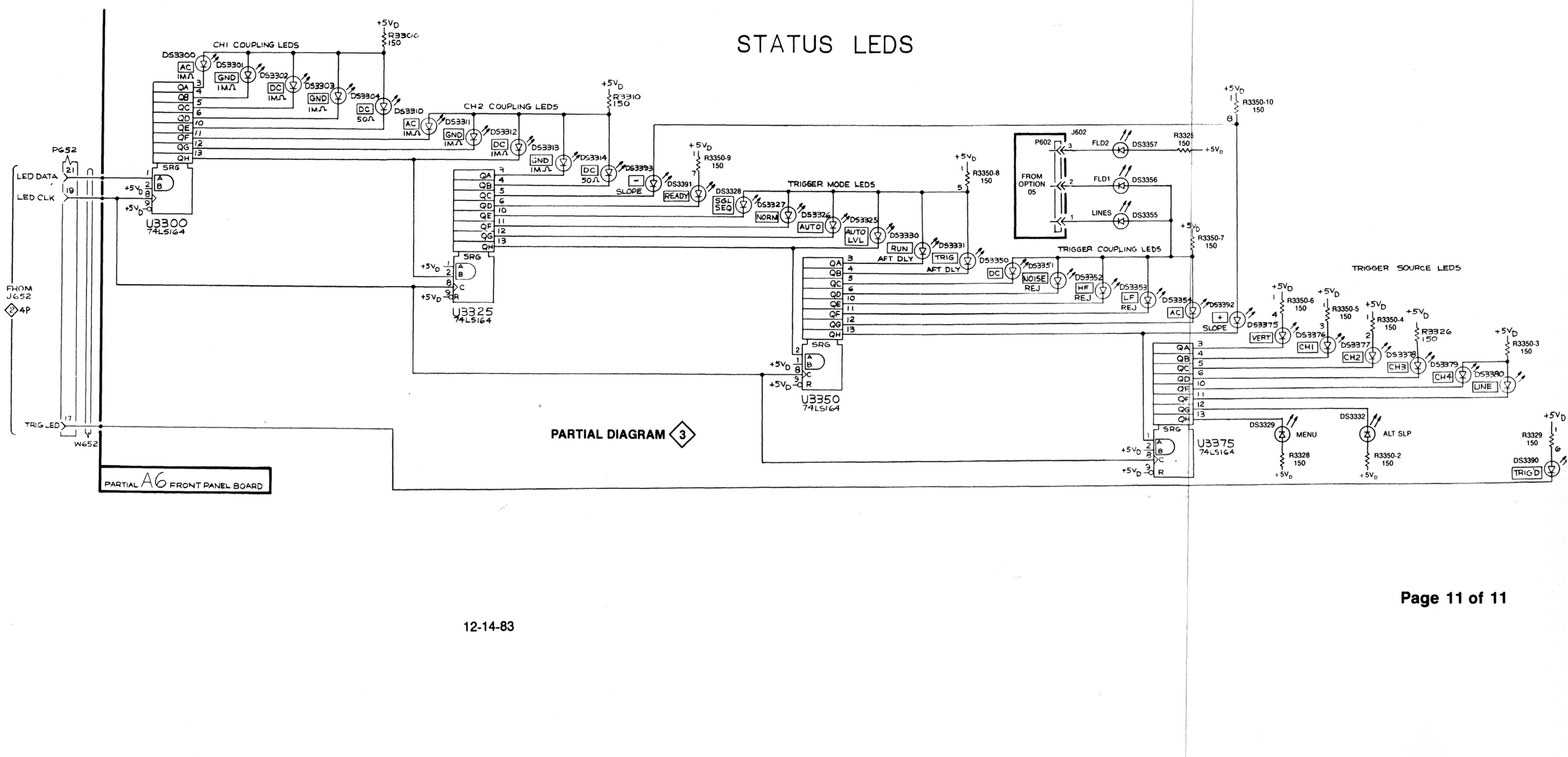
ASSEMBLY A6

CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION	CIRCUIT NUMBER	SCHEM LOCATION	BOARD LOCATION
CR3000	2J	2C	CR3250	5K	4D	DS3391	7G	1E	R3350-10	7M	2E
CR3001	2K	2C	CR3260	6J	4D	DS3392	8L	1E	S3000A	3J	2A
CR3002	2M	2C	CR3270	2B	4E	DS3393	7F	1E	S3000B	3K	2B
CR3003	2N	2C							S3000C	3M	2B
CR3010	2L	2A	DS3300	6B	4A	J601	5D	4A	S3000D	3N	2B
CR3011	3D	2C	DS3301	6C	4A	J602	8K	3F	S3010A	3L	2A
CR3012	3K	2B	DS3302	6C	4A	J671	7P	4F	S3010B	3D	2B
CR3020	3B	3A	DS3304	7D	4A				S3010C	3K	2B
CR3021	3B	3A	DS3303	7C	4A	P602	7K	3F	S3010D	3L	2B
CR3022	3B	3B	DS3310	7D	4B	P651	3S	2A	S3025	1B	4A
CR3023	3C	3B	DS3311	7E	4B	P652	1S	2F	S3030	4D	3B
CR3025	2C	4A	DS3312	7E	4B	P652	7A	2F	S3035	2C	4C
CR3030	5B	3B	DS3313	7E	4B				S3050A	2B	4D
CR3031	5B	3B	DS3314	7F	4B	R3021	3P	1A	S3050B	2A	4E
CR3032	5B	2B	DS3325	8H	2D	R3031	4P	1B	S3105	4J	1D
CR3033	5C	3B	DS3326	8H	2D	R3050	4P	4D	S3110A	4M	2C
CR3035	2C	4C	DS3327	8G	2D	R3075	5P	4E	S3110B	4L	2C
CR3050	2C	4E	DS3328	8G	2D	R3100	5P	1C	S3110C	4K	2D
CR3075	2B	4D	DS3329	10M	2D	R3125	5P	2C	S3175A	3H	3C
CR3105	4J	1D	DS3330	8J	3D	R3150	6P	2D	S3175B	5H	3C
CR3110	4M	1D	DS3331	8J	3D	R3190	3P	4C	S3200	3J	1D
CR3115	4L	2C	DS3332	10M	3D	R3200	6P	1D	S3210	4N	2E
CR3120	4K	2D	DS3350	8J	2E	R3210	6P	1E	S3220	5L	2D
CR3175	2F	3C	DS3351	8K	2E	R3300	6D	4A	S3250	5K	3D
CR3176	2F	3C	DS3352	8K	2E	R3310	7F	4B	S3260	5J	3E
CR3177	2F	3C	DS3353	8L	2E	R3325	7L	3E	S3270	1A	3E
CR3178	2G	3D	DS3354	8L	3E	R3326	9N	3E			
CR3179	2G	3C	DS3355	8L	3E	R3328	10M	2E	U3300	8B	4B
CR3180	5F	4D	DS3356	7L	3E	R3329	10P	1D	U3325	9E	3C
CR3181	6F	4C	DS3357	7L	3E	R3350-2	10M	2E	U3350	9H	3D
CR3182	6F	4C	DS3375	9M	2E	R3350-3	9P	2E	U3375	10L	3F
CR3183	6G	3C	DS3376	9M	2E	R3350-4	8N	2E			
CR3184	6G	4D	DS3377	9N	2E	R3350-5	8M	2E	W651	8S	2A
CR3185	5C	2C	DS3378	9N	2E	R3350-6	8M	2E	W652	10A	2F
CR3200	3J	1D	DS3379	9N	2E	R3350-7	8L	2E	W652	3S	2F
CR3210	4N	2E	DS3380	9P	3E	R3350-8	7J	2E			
CR3220	5L	2D	DS3390	10P	1E	R3350-9	7G	2E			



A6 FRONT PANAL BOARD
(SN B020000 AND ABOVE)

STATUS LEDS


A B C D E F G H J K L M N P
6 7 8 9 10
CH1 COUPLING LEDS
DS3300 AC 1MΩ
DS3301 GND 1MΩ
DS3302 DC 1MΩ
DS3303 GND 1MΩ
DS3304 DC 50Ω
DS3310 AC 1MΩ
DS3311 GND 1MΩ
DS3312 DC 1MΩ
DS3313 GND 1MΩ
DS3314 DC 50Ω
CH2 COUPLING LEDS
DS3393 SLOPE
DS3391 READY
TRIGGER MODE LEDS
DS3328 SGL SEQ
DS3327 NORM
DS3326 AUTO
DS3325 AUTO LVL
DS3330 RUN AFT DLY
DS3331 TRIG AFT DLY
TRIGGER COUPLING LEDS
DS3350 DC
DS3351 NOISE REJ
DS3352 HF REJ
DS3353 LF REJ
DS3354 AC
DS3392 SLOPE
TRIGGER SOURCE LEDS
DS3375 VERT
DS3376 CH1
DS3377 CH2
DS3378 CH3
DS3379 CH4
DS3380 LINE
DS3329 MENU
DS3332 ALT SLP
DS3390 TRIG'D
DS3357 FLD2
DS3356 FLD1
DS3355 LINES
R3300 150
R3310 150
R3350-9 150
R3350-8 150
R3350-10 150
R3325 150
R3350-7 150
R3350-6 150
R3350-5 150
R3350-4 150
R3326 150
R3350-3 150
R3329 150
R3328 150
R3350-2 150
U3300 74LS164
U3325 74LS164
U3350 74LS164
U3375 74LS164
SRG
P652
LED DATA
LED CLK
TRIG LED
FROM J652 4P
W652
FROM OPTION 05
P602 J602
PARTIAL DIAGRAM 3
PARTIAL A6 FRONT PANEL BOARD

Tektronix®
COMMITTED TO EXCELLENCE

MANUAL CHANGE INFORMATION

Date: 11-21-83 **Change Reference:** C5/1183

Product: 2445 SERVICE **Manual Part No.:** 070-3829-00

DESCRIPTION PG 38

TEXT CHANGES

Effective All Serial Numbers

Page 1-2 Table 1-1

Replace the Frequency Response and associated Characteristics with the following:

Frequency Response	Six-division reference signal from a terminated 50-Ω system, with VAR VOLTS/DIV control in calibrated detent.		
	VOLTS/DIV setting	**−3 dB bandwidth with standard-accessory probe or internal 50-Ω termination**	**−4.7 dB bandwidth with 50-Ω external termination on 1-MΩ input**
−15°C to +55°C	2 mV	DC to 80 MHz	DC to 80 MHz[a]
−15°C to +35°C	5 mV or greater	DC to 150 MHz	DC to 150 MHz[a]
+35°C to +55°C	5 mV or greater	DC to 100 MHz[a]	DC to 100 MHz[a]

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

See Below For Effective Serial numbers

CHANGE TO:

A9	670-7277-05	B013650	CKT BOARD ASSY: HIGH VOLTAGE BOARD
A9C1891	281-0773-00	B013650	CAP,FXD,CER DI: 0.01UF,10%,100V

CHASSIS PARTS

CHANGE TO:

R351	311-2174-00	ALL SN's	RES,VAR,NONWW: 5K OHM,20%,0.5W
R352	311-2174-00	ALL SN's	RES,VAR,NONWW: 5K OHM,20%,0.5W
R975	311-1482-00	ALL SN's	RES,VAR,NONWW: 5K OHM,20%,0.5W
R977	311-1482-00	ALL SN's	RES,VAR,NONWW: 5K OHM,20%,0.5W

DIAGRAM CHANGES

DIAGRAM ◇9◇ HIGH VOLTAGE SUPPLY

Change C1891 (location 3G) to a 0.01 μF capacitor. M52903
(SN B013650)

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MANUAL CHANGE INFORMATION

Date: 11/30/83 Change Reference: M52083, M52604

Product: 2445 Service Manual Part No.: 070-3829-00

DESCRIPTION PG. 38

EFF SN: B012000

REPLACEABLE ELECTRICAL PARTS LIST CHANGES

CHANGE TO:

A1	670-7285-07	CKT BOARD ASSY: MAIN (STANDARD)	M52083

REMOVE:

A1R223	315-0622-00	RES, FXD, CMPSN: 6.2 K OHM, 5%, 0.25 W	M52083

ADD:

A1C223	281-0770-00	CAP, FXD, CER DI: 1.0 uF, 20%, 100 V	M52083
A1C500	281-0812-00	CAP, FXD, CER DI: 1.0 uF, 10%, 100 V	M52604
A1C501	281-0812-00	CAP, FXD, CER DI: 1.0 uF, 10%, 100 V	M52604

DIAGRAM CHANGES

DIAGRAM 4 ATTENUATORS & PREAMPS

Replace R223 (location 3C) with C223, a 1.0 μF capacitor. M52083

DIAGRAM 11 POWER DISTRIBUTION A

Add C500 (.001 μF) from U500 pins 16, 33, 40, & 9 to ground at location 5E. M52604

Add C501 (.001 μF) from U500 pin 45 to ground at location 6E. M52604

GUERNSEY TYPE - GENERAL

All Mainframes supplied with an Option A - 2 Power Cord have a 5 Amp Fuse (Part Number 159-0093-00) fitted in the Plug.

4022/982

GUERNSEY TYPE 2445 - TENTATIVE S/N 100001
GUERNSEY TYPE 2465 - TENTATIVE S/N 100001

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A1C809	281-0759-00	Cap, Fxd, Cer, Di: 22pF 100V

4112/583

GUERNSEY TYPE 2445 - TENTATIVE SEN 100421
2465 - TENTATIVE S/N 100601

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A2R1331	321-0685-00	Cap, Fxd, Cer, Di: 30.0K 5%
A2R1332	321-0318-02	Cap, Fxd, Cer, Di: 20.0K 5%
A2R1357	321-0318-02	Cap, Fxd, Cer, Di: 20.0K 5%
A2R1358	321-0689-00	Cap, Fxd, Cer, Di: 24.9K 5%

4087/383

GUERNSEY TYPE 2445 - TENTATIVE S/N 100641
2465 - TENTATIVE S/N 100791

CHANGE TO:-

A1U450	156-0158-03	Integrated Circuit	2445/2465
A2U1281	156-0158-03	Integrated Circuit	2445 only
A9U1956	156-0158-03	Integrated Circuit	2465 only

4150/783

GUERNSEY TYPE 2445 - TENTATIVE S/N 100661
2465 - TENTATIVE S/N 100821

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A1CR101	152-0323-01	Semicond Device
A1CR201	152-0323-01	Semicond Device

4131/683

GUERNSEY TYPE 2445 - TENTATIVE S/N 100941
2465 - TENTATIVE S/N 100901

ELECTRICAL PARTS LIST CHANGE

ADD:-

A5R2025	315-0103-00	Resistor, Fxd, Cmpsn, 10K Ohm 5%

CHANGE TO:-

	670-7279-05	Circuit Board Assembly, Digital Control

Note: Add R2025 from the collector of Q2025 to common

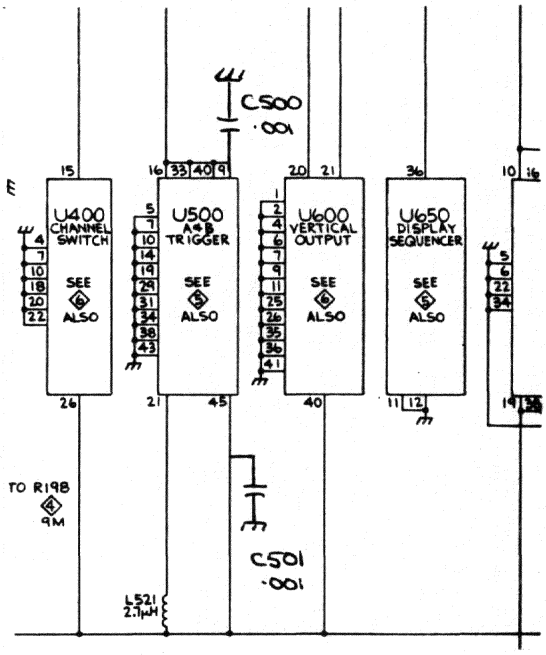
4191/1083

GUERNSEY TYPE 2445 - TENTATIVE S/N 101201
2465 - TENTATIVE S/N 101201

ELECTRICAL PARTS LIST CHANGE

ADD:-

A1C500	281-0812-00	Cap, Fxd, Cer, Di: .001uF 100V
A1C501	281-0812-00	Cap, Fxd, Cer, Di: .001uF 100V



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4218/1183

GUERNSEY TYPE 2445 - TENTATIVE S/N 101201
2465 - TENTATIVE S/N 101201

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A9C1891	281-0773-00	Cap, Fxd, Cer, Di: .01 uF

4219/1183

GUERNSEY TYPE 2445 - TENTATIVE S/N 102011
2465 - TENTATIVE S/N 101621

ELECTRICAL PARTS LIST CHANGE

ADD:-

A2C1222	281-0783-00	Cap, Fxd, Cer, Di: .1uF 20% 100V
A2R1010	301-0150-00	Res, Fxd, Cmpsn, 15 Ohm ½W 5%
A2R1019	301-0150-00	Res, Fxd, Cmpsn, 15 Ohm ½W 5%
A3R1073	301-0183-00	Res, Fxd, Cmpsn, 18K ½W 5%
A2R1287	315-0472-00	Res, Fxd, Cmpsn, 4.7K ¼W 5%

CHANGE TO:-

	670-7281-03	Regulator Assembly
	670-7282-03	Inverter Assembly
	672-1037-04	Low Voltage Power Supply
A2R1013	315-0753-00	Res, Fxd, Cmpsn, 75K ¼W 5%
A2R1014	315-0363-00	Res, Fxd, Cmpsn, 36K ¼W 5%
A2R1015	315-0363-00	Res, Fxd, Cmpsn, 36K ¼W 5%
A3R1029	315-0272-00	Res, Fxd, Cmpsn, 2.7K ¼W 5%
A3R1037	315-0272-00	Res, Fxd, Cmpsn, 2.7K ¼W 5%
A3R1069	301-0183-00	Res, Fxd, Cmpsn, 18K ½W 5%
A2R1208	315-0201-00	Res, Fxd, Cmpsn, 200 Ohm ¼W 5%

Note: Add R1073 with existing R1069 to form a teepee
Add R1010 in parallel with RT1010
Add R1019 in parallel with RT1016
Add R1287 teepeed in series with CR1281, attaching the cathode end of CR1281 to the resistor
Add C1222 attaching one lead to Pin 1 of U1281A and the other lead to the base of Q1221

4196/1183

GUERNSEY TYPE 2445 - TENTATIVE S/N 101611
2465 - TENTATIVE S/N 101391

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A5U2162	160-1994-XX	Eprom
A5U2378	160-1995-XX	Eprom

REMOVE:-

A5U2362	160-1627-XX	Eprom
A5U2178	160-1625-XX	Eprom

4214/1183

GUERNSEY TYPE 2445 - TENTATIVE S/N 102351

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A3T1020	120-1244-00	Transformer

REMOVE:-

A3R1017	315-0103-00	Resistor, Fxd, Cmpsn, 10K 5% ¼W
A3R1021	315-0103-00	Resistor, Fxd, Cmpsn, 10K 5% ¼W

4206/1183

GUERNSEY TYPE 2445 - TENTATIVE S/N 102060

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

A1R622	321-0226-00	Resistor, Fxd, Cmpsn, 2.21K 1%

4268/284

GUERNSEY TYPE 2445 - TENTATIVE S/N 102681
2465 - TENTATIVE S/N 101901

ELECTRICAL PARTS LIST CHANGE

ADD:

A9R1833	315-0103-00	Resistor, 10K 5%
A9R1901	315-0101-03	Resistor, 100 Ohm 5%
A9L1921	108-0262-00	Coil, 510nH

CHANGE TO:

	670-7277-06	High Voltage Assembly
A9R1834	315-0103-00	Resistor, 10K 5%
A9R1973	315-0124-00	Resistor, 120K 5%
A9R1992	315-0394-00	Resistor, 390K 5%

REMOVE:

A9C1909	281-0783-00	Cap, Fxd, Cer, Di:
A9R1820	315-0122-00	Resistor
A9R1933	315-0102-00	Resistor
A9R1921	315-0100-02	Resistor

Note: Add R1901 with circuit running from pin 6 of J901 to +87 Volts
R1834 will go to ground and added R1833 to +15V and their junction to Pin 12 of P191
Add L1921 in place of R1921

4205/983

GUERNSEY TYPE 2445 - TENTATIVE S/N 102681
2465 - TENTATIVE S/N 101901

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

V900	154-0850-01	Electron Tube

4222/1283

GUERNSEY TYPE 2445 - TENTATIVE S/N 102681
2465 - TENTATIVE S/N 101901

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

	670-7276-08	Main C/B Assembly 2465
	670-7285-08	Main C/B Assembly 1445
A1C203	283-0811-00	Cap, Fxd, Cer, Di: 0.01uF 100V

4224/1283

GUERNSEY TYPE 2445 - TENTATIVE S/N 102681
2465 - TENTATIVE S/N 101901

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:

A4R2921	321-0303-00	Resistor, Fxd, Cmpsn 14.0K 1%
A4R2930	315-0152-00	Resistor, Fxd, Cmpsn 1.5K 5%

4251/184

GUERNSEY TYPE 2445 - TENTATIVE S/N 102757
2465 - TENTATIVE S/N 102321

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A5U2162	160-1994-07	Microckt, Digital
A5U2378	160-1995-07	Microckt, Digital

4264/284

GUERNSEY TYPE 2445 - TENTATIVE S/N 103031
2465 - TENTATIVE S/N 102781

ELECTRICAL PARTS LIST CHANGE

CHANGE TO:-

A6S3185	260-2108-02	Switch, pushbutton

4288/984