

**Digital Equipment Corporation
Maynard, Massachusetts**



**PC09C
High Speed Paper Tape
Reader and Punch
Maintenance Manual**

PC09C
HIGH SPEED PAPER TAPE
READER AND PUNCH
MAINTENANCE MANUAL

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CHAPTER 1 GENERAL INFORMATION

1.1 DESCRIPTION AND PURPOSE

The DEC Type PC09C High-Speed Perforated-Tape Reader/Punch (Figure 1-1) is supplied as optional peripheral equipment with the PDP-9/L computer system. The device is made up of a DEC Type PC02 Punched-Paper-Tape Reader and a DEC Type PC03 Paper-Tape Punch.

The basic tape reader (PC02) consists of an electromechanical tape-feed system with associated current drivers, and a 9-channel photoelectric tape-read head, including photocell amplifiers. The PC02 reads 8-level, 1-in. wide perforated tape, under external control, at a rate of 300 characters per second; and transmits the data read from the tape to the PDP-9/L accumulator.

The basic tape punch (PC03) contains electromechanical tape-feed and punch systems. The PC03 consists of a Model 500 Royal-McBee Punch actuated by DEC control circuits. The punch operates at a rate of 50 characters per second and accepts data for punching from the PDP-9/L accumulator.

The functions of feeding, reading, and punching tape occur under direct control of circuits installed within the computer as part of the PC09C option. The PDP-9/L generates commands to implement these functions. The only exception to this is in the manual feeding of tape. On both the reader and punch, feed controls permit manual tape feeding under operator control. In the PDP-9/L system, the control logic circuits for the PC09C are located in the module bay at the rear of the computer rack.

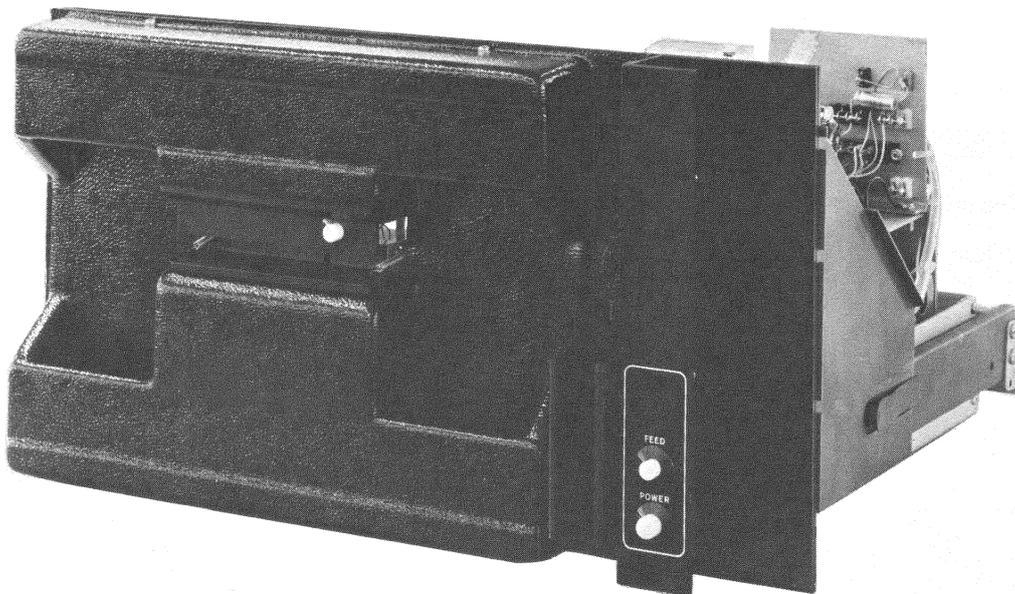


Figure 1-1 Type PC09C High-Speed Perforated Paper-Tape Reader/Punch

1.2 SPECIFICATIONS

1.2.1 Physical

The PC09C overall cabinet dimensions are 19-in. wide, 15-in. deep, and 10-1/2 in. high. The unit is mounted in the computer rack directly above the system console. Drawer slides are provided for ease of maintenance.

1.2.2 Environmental

No special environmental conditions need to be met for proper operation of the PC09C. Ambient temperature at the installation site can vary between 60° and 95°F (15° to 35°C) with no adverse effect on its operation. During shipping and storage, the ambient temperature may vary between 32° and 130°F (0° and 55°C). Although DEC treats exposed surfaces of all cabinets and hardware against corrosion, exposure of the unit to extreme humidity for long periods of time should be avoided.

1.3 INTERFACE

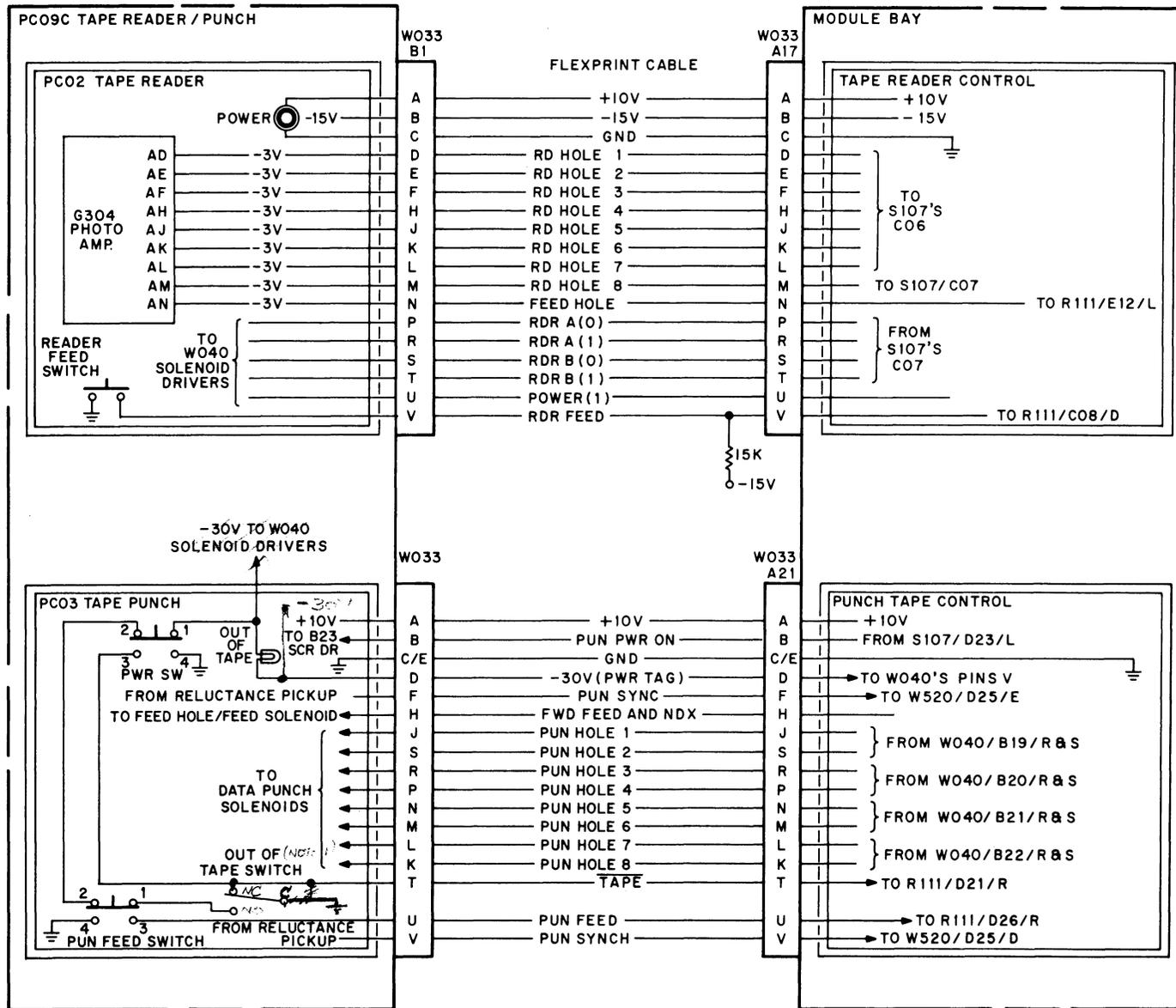
The PC09C Tape Reader/Punch interfaces with its control devices by two interconnecting cables as shown in Figure 1-2; one each for the reader and the punch. Each cable terminates at both ends in a W033 connector. The tape reader connector plugs into the W023 connector at position A1 on the reader FLIP CHIP connector block, while the tape punch connector plugs into the receptacle provided on the punch connector block. For more detailed information concerning interfacing to the PDP-9/L, refer to DEC-09-H7AA-D, "PDP-9/L Interface Manual."

1.4 EQUIPMENT SUPPLIED

Table 1-1 lists the equipment supplied as part of the PC09C High-Speed Perforated Paper Tape Reader/Punch.

Table 1-1
Equipment Supplied

Quantity per Unit	Name	Type Number
1	Perforated Tape Reader	PC02
1	Perforated Tape Punch	PC03
1	Signal Interface Cable consisting of,	
	2 Flexprint Cables and 4 Cable Connectors	W033
1	Power Cable	
1 set	FLIP CHIP Modules containing,	
1		G904
1		G913
2		R111
1		R302
1		R303
1		R401
1		S107
7		S202
1		S602
9		W040
1		W520
1		W990



1-4

Figure 1-2 PC09C/PDP-9/L Interfacing Diagram

CHAPTER 2 INSTALLATION

This chapter contains information concerning installation of the PC09C. It includes the siting requirements and procedures to be followed in unpacking and integrating the equipment into an existing PDP-9/L system. Turn-on and checkout procedures are given to confirm operation of equipment once it has been installed.

2.1 UNPACKING AND INSTALLATION

2.1.1 Unpacking and Special Handling

The PC09C is packed in accordance with best commercial practice. No special handling procedures are required beyond the normal care afforded any piece of scientific equipment. It is recommended that the carton, and all packing materials, be saved in case reshipment to the manufacturer should become necessary.

2.1.2 Inspection

Upon receipt of a PC09C, the equipment should be inspected for any visible damage in transit such as dents and abrasions. Any damage observed should be reported immediately to both the carrier and the manufacturer. Check the contents of the carton with the shipping document and with Table 1-1, Equipment Supplied, of this manual. Report any omissions immediately. Installation is not recommended until all materials are in hand.

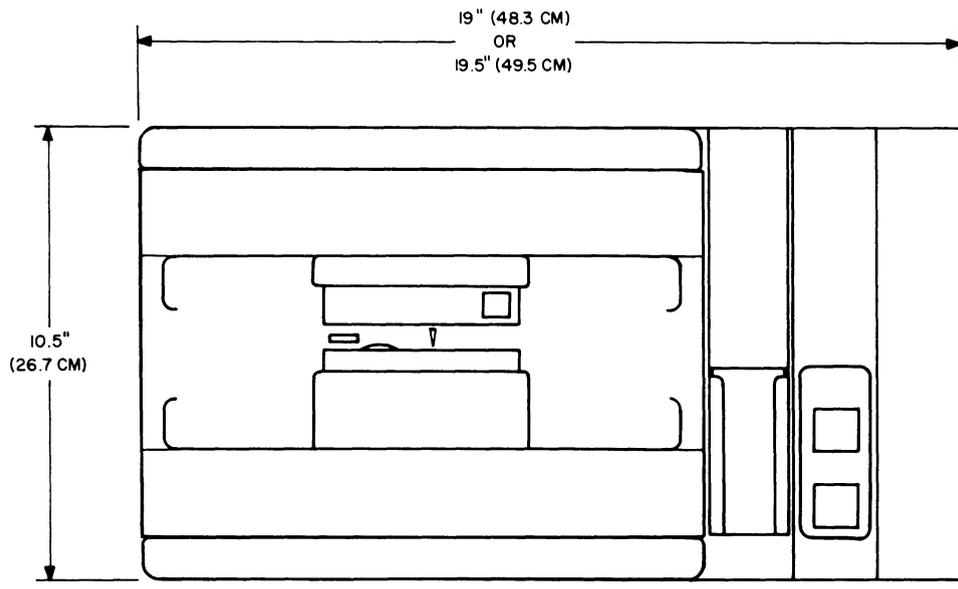
2.1.3 Power Requirements

The basic PDP-9/L has been designed to include power capability to accommodate the PC09C Tape Reader/Punch. Interconnection to power and signal sources and destinations are made in accordance with procedures given in Section 2.2. The 3-terminal 110 Vac power connectors, located at the rear of the chassis, provide both an input and an output point for primary power. The connectors, one male and one female, permit the inclusion of the PC09C in a power chain with other devices in the system. The following input voltages are required and are supplied from the PDP-9/L Type 712 Power Supply:

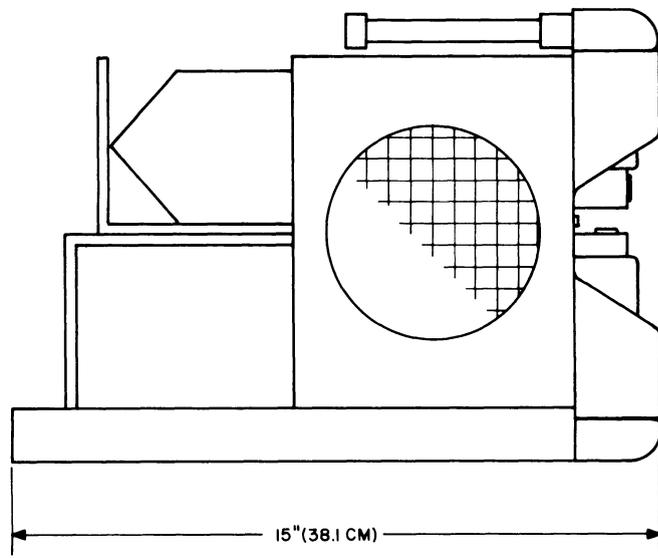
-15 Vdc (-14.5 to -16.5V)

+10 Vdc (9.5 to 11.5V)

-30 Vdc



FRONT VIEW



SIDE VIEW

Figure 2-1 PC09C External Dimensions

2.2 INSTALLATION AND CHECKOUT

2.2.1 Installation

When used with the PDP-9/L, the PC09C mounts in the space provided directly above the console. No special hardware is required as the attaching hardware used for the dummy panel may be used to install the unit. External dimensions, however, are shown in Figure 2-1. Otherwise, the unit is rack-mountable in either a 19 or 19-1/2 in. wide radio rack. Drawer slides are provided for ease of maintenance. The unit can be mounted in a cabinet which is 10-1/2 in. (26.7 cm.) high, 19 in. (48.3 cm.) wide, and 15 in. (38.1 cm.) deep. To install the PC09C, proceed as follows:

- a. Be sure that all power has been removed from the PDP-9/L system.
- b. Install with the hardware provided the tape reader control modules, listed in Table 2-1, in the locations specified for the rear hinged module bay of the PDP-9/L.
- c. Install with the hardware provided the tape punch control modules, listed in Table 2-2, in the locations specified for the rear hinged module bay of the PDP-9/L.
- d. Remove those PDP-9/L components specified in Table 2-3.
- e. On the front of the PDP-9/L cabinet, remove and retain the eight machine screws that secure the dummy panel directly above the console (see Figure 2-2).

NOTE

Securing nuts are captive.

- f. Set aside the dummy panel and in its place install the Tape Reader/Punch PC09C using the eight machine screws retained in step e above.

CAUTION

Be careful not to damage any exposed wiring during the installation.

Table 2-1
Tape Reader Control Modules to be Installed

Module Designation	Module Bay Location
R401	E03
G913	E04
S202	E11
S202	E13
W990	A16
W023 (Reader Cable)	A17

Table 2-2
Tape Punch Control Modules to be Installed

Module Designation	Module Bay Location
R111	D21, D26
R302	C25
R303	C27
S107	D23
S202	C20, C21, C22, C23, C24
S602	D24
W023 (Punch Cable)	A21
W040	B19, B20, B21, B22, B23
W520	D25

Table 2-3
PDP-9/L Parts to be Removed

Component	From	To
3.3 K Ω 1/4 W Res.	E05J	E05L
3.3 K Ω 1/4 W Res.	E05S	E05W
Module Designation	Module Bay Location	
S603	A01	
W990	A14, A15	

g. Remove the six FLIP CHIP modules from the packing case and install them in their receptacles in the rear of the Tape Reader (see Figure 2-3).

h. Unwrap the interfacing cable which is threaded through the rear slot of the PC09C chassis. Insert one W033 module connector into the receptacle provided on the punch.

i. Insert the W033 module connector on the other end of that cable into its receptacle on the punch control (A21) (see Figure 2-4).

j. Insert the remaining W033 connector in the receptacle provided on the reader (B1).

k. Insert the W033 connector on its opposite end in the receptacle provided on the reader control (A17) (see Figure 2-4).

l. Remove the power cable from the packing case and install it in the PC09C as shown in Figure 2-4.

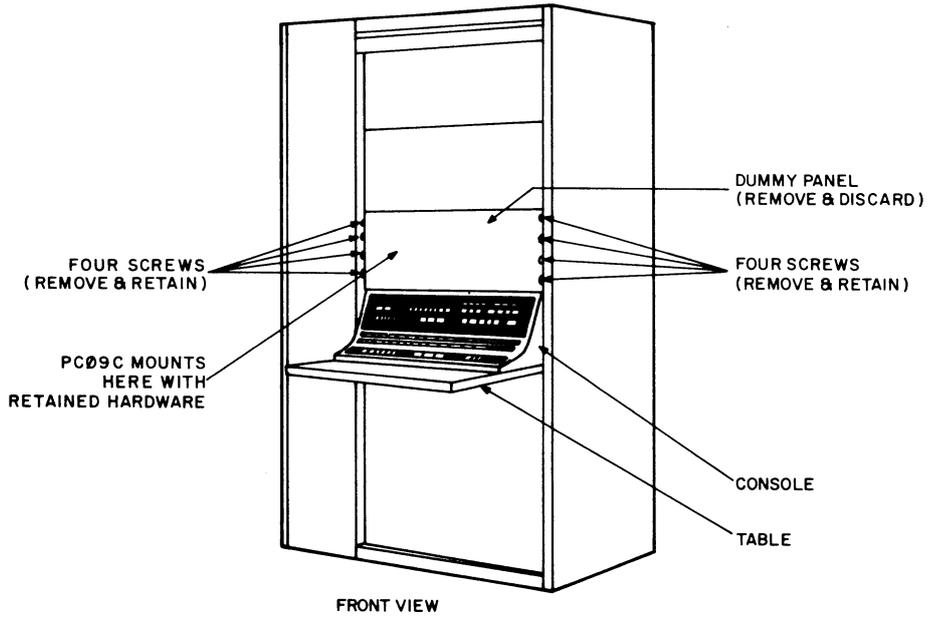


Figure 2-2 Locating PC09C Tape Reader/Punch

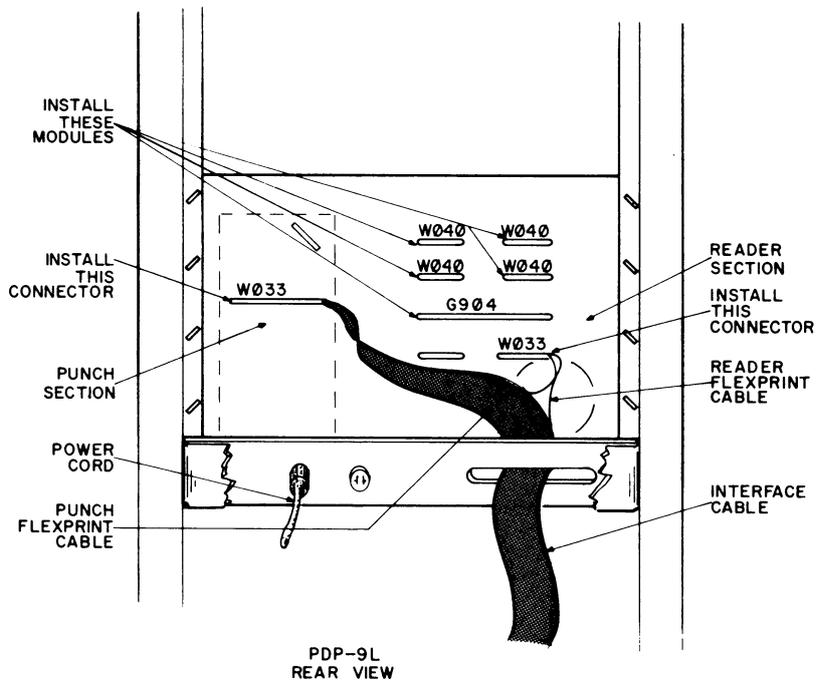


Figure 2-3 Installation of PC09C Modules and Connectors

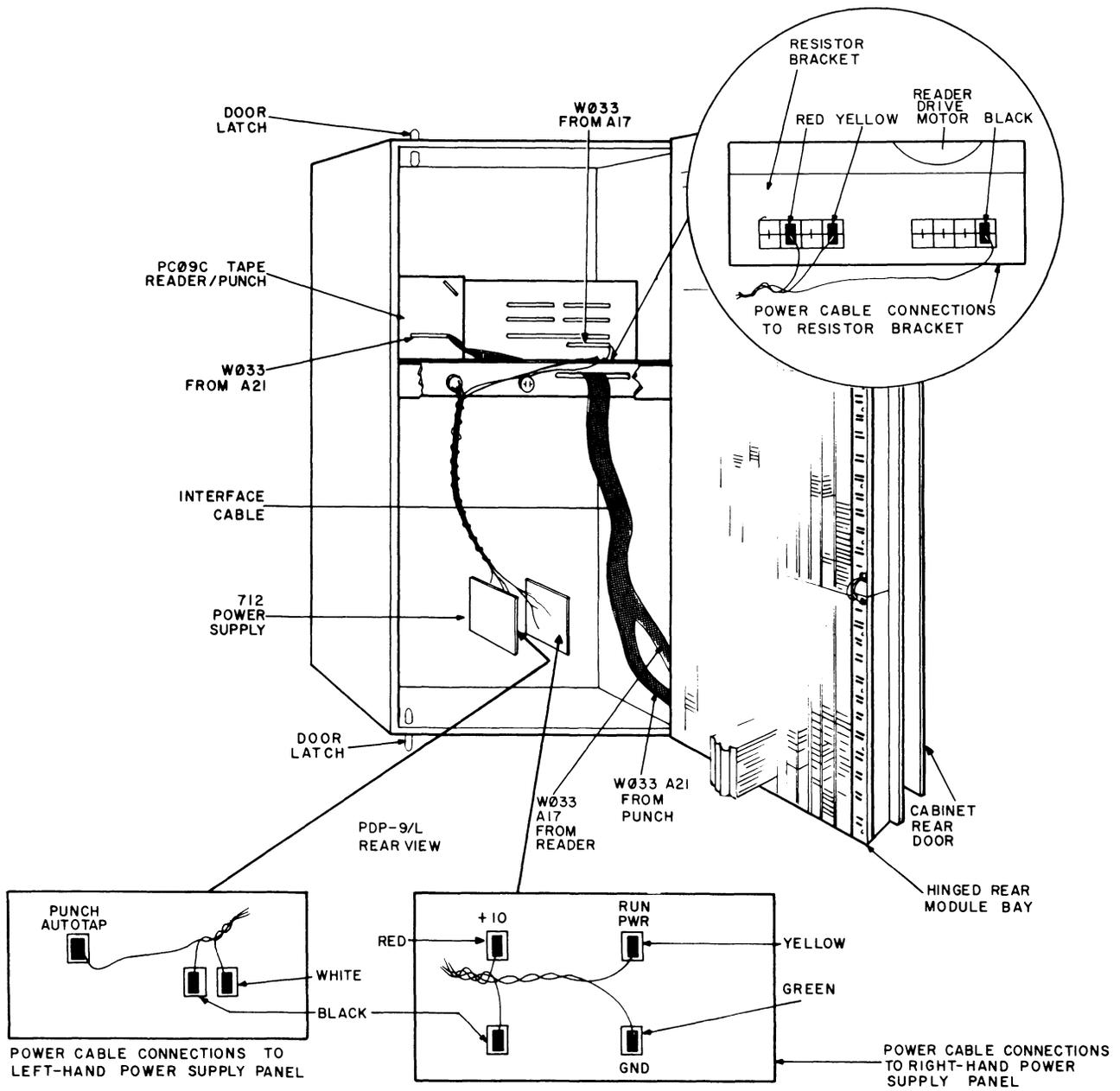


Figure 2-4 PC09C/Power Supply/Control Interconnection

2.2.2 Turn-On and Checkout

Once the PC09C has been installed, proceed as follows to check out the equipment:

- a. Apply power to the PDP-9/L computer system.
- b. Press the POWER button on the Reader/Punch front panel. The button should illuminate; if it does not, check to see if a fresh carton of perforator tape is installed in the well provided at the rear of the machine and that it is fed into the tape punch (see Section 3-5 for detailed loading instructions).
- c. Press the FEED button on the front panel of the unit. Tape should feed out of the tape slot. The tape should be unpunched except for feed holes. See that the holes are evenly spaced and that tape motion is even. The tape should not bind against the sides of the guides or slot.
- d. Hold the FEED button until a few feet of feed-hole-only tape has been punched. Tear it off and insert it in the reader head, feeding from right to left.
- e. Press the feed button on the reader and see that the tape feeds evenly without binding on the edges of its guides.
- f. Load the diagnostic tape, MAINDEC-9A-D2CB-PH, in the right-hand bin of the reader and run it through using the instructions contained in the document supplied with the tape. At the conclusion of the tape, the indications should be as called for in the document. If not, trouble is indicated; refer to Section 5-3 in the Maintenance Chapter of this manual.

NOTE

The Punch Test checks and verifies the operational status of the punch control logic, and the mechanical functions of the punch. A series of six tests are performed on the punch control, followed by nine tests on the punch itself. Provision is made to continuously loop in two of the six punch control tests, and any one of the punch data tests.

- g. Load the diagnostic tape, MAINDEC-9A-D2DB-PH, in the reader and run it through using the instructions contained in that document. Observe that the tape punches as called for by the diagnostic instructions and that at the conclusion the indications are as called for in the document. If not, trouble is indicated; refer to Section 5-3 in the Maintenance Chapter of this manual.

NOTE

The High-Speed Reader Test checks and verifies the operational status of the reader by testing the associated logic control and the reader mechanics. The program is in two parts with part 1 punching the tapes used in part 2 of the tests.

CHAPTER 3 OPERATION AND PROGRAMMING

This chapter contains a functional description of the PC09C at the block level. Included are operating features, identification of controls and indicators, a brief description of its operating sequence, and an introduction to its programming. All maintenance procedures to be performed by the operator are described in this chapter.

3.1 FUNCTIONAL OPERATION

The PC09C comprises two functional units; the PC02 Perforated-Tape Reader and the PC03 Paper-Tape Punch.

3.1.1 PC02 Perforated-Tape Reader

The PC02 consists of two basic elements, the tape reader and the tape transport. The read station (Figure 3-1) contains the nine photo-sensitive semiconductors (photo-voltaic cells) and their light source, eight which read perforations in the data tracks and a ninth which senses the presence of the sprocket feed hole.

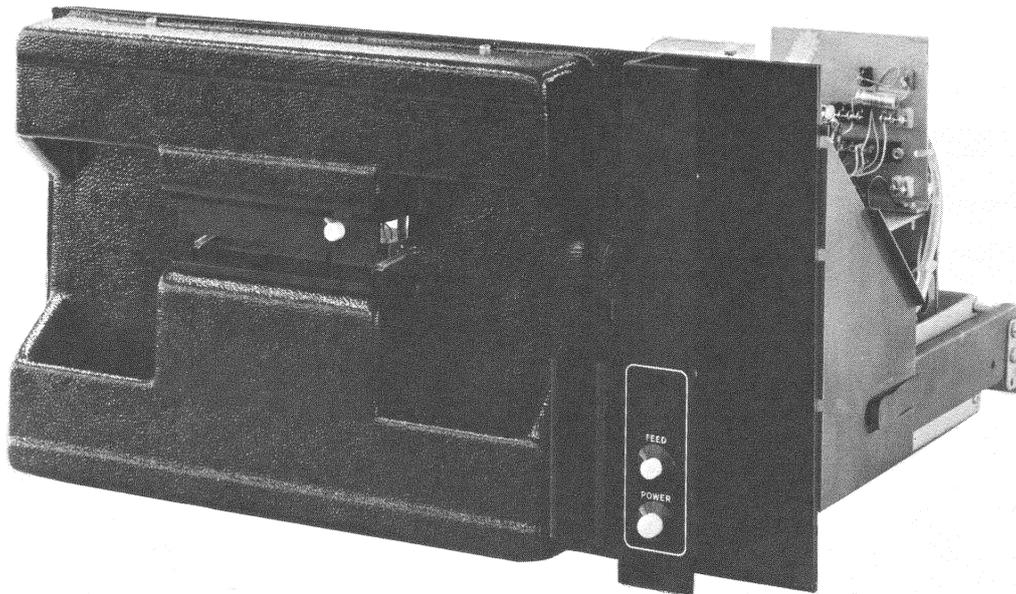


Figure 3-1 PC09C Perforated-Tape Reader/Punch, Front View

A feed-hole sprocket-drive system, actuated by a stepping motor (see Figure 3-2), transports tape through the read station. A snap-action tape retainer guides the tape over the read head and feed mechanism. A feed button permits manual control of tape motion by the operator. The reader will not read while the feed button is pressed.

Five FLIP CHIP circuit modules, mounted on a double connector block, contain the drivers and amplifiers used by the reader. The connector block, located above the stepping motor, likewise serves as an interface point for the signal cables attached to the unit. A fan, mounted on the left side of the chassis as viewed from the front, provides a flow of cooling air for the circuit modules and the motor.

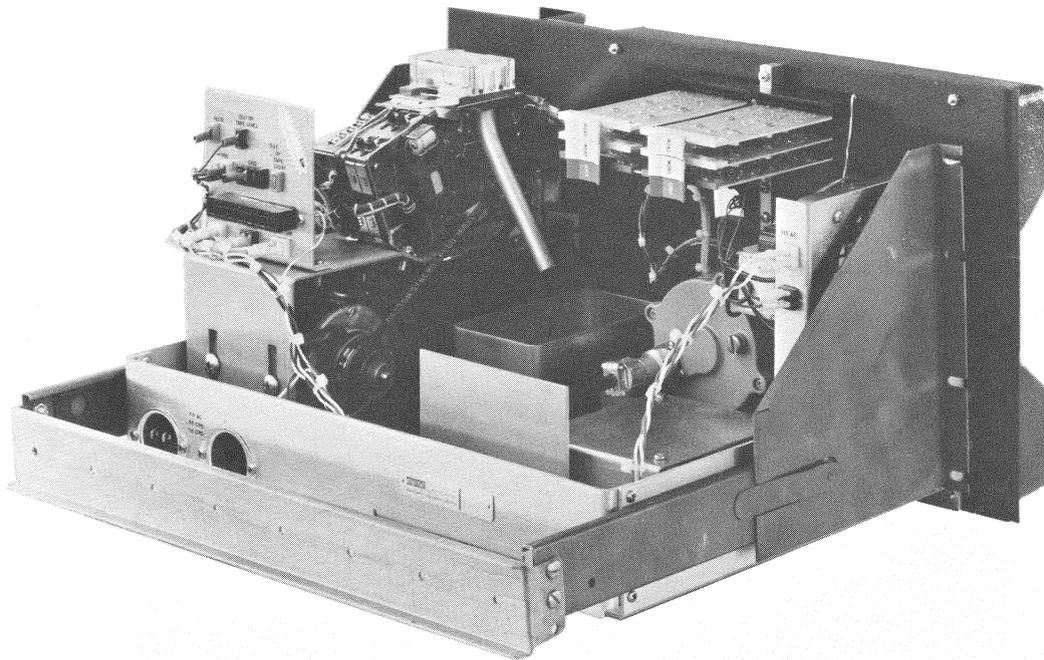


Figure 3-2 PC09C Perforated-Tape Reader/Punch, Rear View

The PC02 photoelectrically reads data which has been punched in paper tape, temporarily stores that data, and then retransmits it to the accumulator of the PDP-9/L. Logic circuits implement these functions by interpreting commands (IOP pulses) generated by the PDP-9/L. The basic PC09C system is shown in Figure 3-3.

A device code from the PDP-9/L provides the basic activating signal to the tape reader's logic control. Sensing of the device code by the logic circuits enables the receipt of the IOP pulses from which the IOT pulses are internally generated to control operation of the reader. The functions of the IOT pulses are as follows:

- IOT 0101 permits interrogation of the reader to determine its state of readiness.
- IOT 0102 clears the reader flag and then inclusively ORs the data stored in the buffer register of the reader control with the contents stored in the accumulator of the PDP-9/L.
- IOT 0112 clears both the reader flag and the accumulator and then transfers data stored in the buffer register of the reader control to the accumulator of the PDP-9/L. Data is transferred to the PDP-9/L on eight parallel interface lines.
- IOT 0104 clears the reader flag and selects the reader alphanumeric mode.
- IOT 0144 clears the reader flag and selects the reader binary mode.

The IOT pulses 0101, 0102, 0112, 0104 and 0144 result from computer program instructions RSF (skip on reader flag), RCF (transfer to AC), RRB (read reader buffer), RSA (select reader alpha), and RSB (select reader binary), respectively.

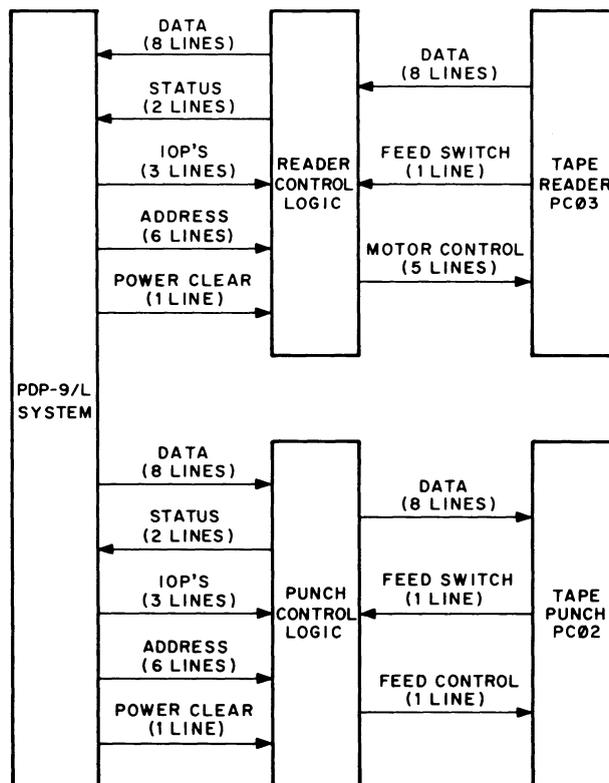


Figure 3-3 PC09C General Block Diagram

Circuits within the tape reader amplify the outputs of nine photodiodes (eight data and one feedhole) prior to their transmission to the reader control logic.

Circuits within the reader control logic actuate the tape feed motor in response to either RCF, RSA or RSB commands generated within the PDP-9/L. One of the five motor-control lines provides one of the two enabling signals required for actuation of driver circuits located within the tape reader. The remaining four lines are sequentially activated, in pairs, to produce the second signal required for operation of the motor drive circuits.

3.1.2 PC03 Paper-Tape Punch

The PC03 Paper-Tape Punch provides punching of data received from the accumulator of the PDP-9/L into paper tape. Logic circuits, which accept and interpret function commands (IOP pulses) generated in the PDP-9/L, implement this function. The PC03 is shown in Figure 3-1 as part of the PC09C.

As in the tape reader, a specific 6-bit device code, in the memory buffer of the PDP-9/L, provides the activating signal to its operation. Sensing of the device code by the punch logic circuits allows the IOP pulses to be received and the IOT pulses to be internally generated within the punch control circuitry. The IOT pulse functions are as follows:

IOT 0201	permits interrogation of the punch to determine its state of readiness.
IOT 0202	clears the punch flag, preparatory to the receipt of data from the PDP-9/L accumulator.
IOT 0204	clears the punch flag and selects the punch alphanumeric mode.
IOT 0214	clears both the punch flag and the accumulator, then selects the punch in alphanumeric mode and causes the punch to punch feed holes only.
IOT 0244	clears the punch flag and selects the punch binary mode.

The IOT pulses 0201, 0202, 0204, and 0244 result from computer program instructions PSF (skip on punch flag), PCF (clear punch flag), PSA (select punch alpha), and PSB (select punch binary), respectively.

Circuits located within the punch control logic provide actuation of the tape-punch feed solenoid in response to PSA or PSB commands generated within the PDP-9/L. The receipt of an IOP4 pulse generates an IOT 0204 pulse within the control circuits that actuate the current drivers connected to both the feed hole punch solenoid and the tape feed solenoid. In this way, the feed hole is punched and the tape is advanced one character position, regardless of the data stored in the punch buffer register.

3.1.3 Reader/Punch Status Functions

The tape-reader device flag is interfaced to the I/O skip facility, the program interrupt control, and to bit 1 of the IORS (input/output read status) word. The tape-reader-no-tape flag is interfaced to bit 8 of the IORS word. Execution of the IOT instruction IORS (octal code 700314) enters the state of device flags in specific bits of the AC. The state of a specific flag or group of flags can be quickly determined by programmed checks of the AC contents. Switching the REGISTER DISPLAY control on the PDP-9/L console to the STATUS position simulates the execution of the IORS instruction while the processor is in the "program stop" condition.

The contents of the IORS word (the states of the device flags) are displayed in the REGISTER indicators on the console at this time. The tape reader device flag is also interfaced with the API (priority level, address 50).

The paper tape-punch device flag is also interfaced to the I/O skip facility and to the program interrupt control. It is interfaced to bit 2 of the IORS word. The tape-punch-no-tape flag is interfaced to bit 9 of the IORS word.

Program instructions from the PDP-9/L for the PC02 Tape Reader are given in Table 3-1 and instructions for the PC03 Tape Punch are given in Table 3-2.

Table 3-1
Tape Reader IOT Instructions

Mnemonic Symbol	Octal Code	Operation Executed
RSF	700101	Skip the next instruction if reader flag is 1.
RCF	700102	Clear reader flag. Read the inclusive OR of the contents of reader buffer and AC into the AC.
RRB	700112	Clear reader flag. Read reader buffer. Clear AC and then transfer contents of reader buffer to AC.
RSA	700104	Select reader in alphanumeric mode. Clear the reader flag then read one 8-bit character into the reader buffer (right-justified). When complete, set reader flag to 1.
RSB	700144	Select reader in binary mode. Clear the reader flag and assemble three 6-bit characters into the reader buffer. When assembled, set reader flag to 1.

Table 3-2
Tape Punch IOT Instructions

Mnemonic Symbol	Octal Code	Operation Executed
PSF	700201	Skip the next instruction if the punch flag is 1.
PCF	700202	Clear the punch flag.
PSA	700204	Clear punch flag then punch a line of tape in alphanumeric mode (rightmost 8 bits of AC). When complete, set punch flag to 1.
Micro-coded	700214	Clear the AC and punch feed hole only.
PSB	700244	Clear punch flag then punch a line of tape in binary mode (rightmost 6 bits of AC). When complete, set punch flag to 1.

3.2 CONTROLS AND INDICATORS

The controls and indicators for the PC09C Tape Reader/Punch are shown in Figure 3-4 and defined in Table 3-3.

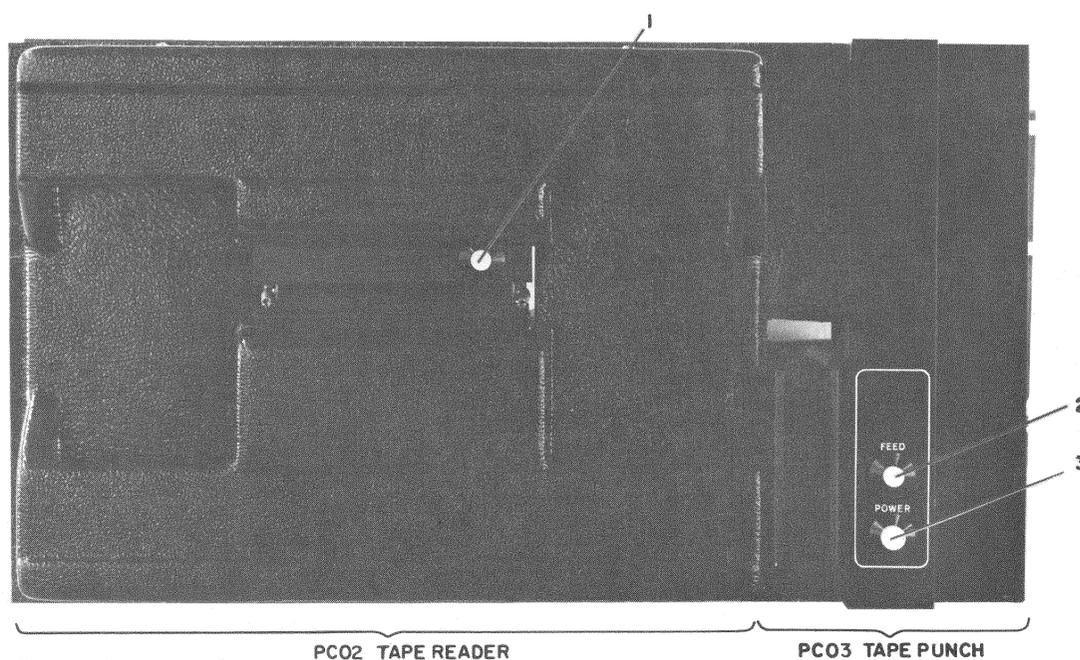


Figure 3-4 PC09C Controls and Indicators

Table 3-3
PC09C Tape Reader/Punch, Controls and Indicators

Index	Name	Function
1.	Feed button	Momentary pushbutton. Depressing, advances tape without reading; releasing, permits program control, manual control, or read-in operations.
2.	FEED button	Momentary pushbutton. Depressing, punches feed holes and advances tape; releasing, permits program control.
3.	POWER button and indicator	Two-condition latching pushbutton/indicator. Off position simulates 'PUN NO TAPE' condition. On position removes the condition. Indicator will light when tape is secured and button is pressed to the on position. Indicator will extinguish while FEED button is pressed.

3.3 SEQUENCE OF OPERATION

When the PC02 Tape Reader is selected by an IOT instruction, the reader control requests reader motion, transfers data from the reader to the reader buffer register, and signals the computer when the buffer is ready for data transfer to the computer. In order to maintain maximum reader speed (300 lines-per-second), a new select IOT must be issued in 1.76 ms.

When the reader is operated in alphanumeric mode (Figure 3-5 a) each select instruction causes one line of tape (eight bits) to be read and placed right-justified in the 18-bit buffer register. The rest of the buffer register is unused, and will contain 0s.

When the reader is operated in binary mode (Figure 3-5 b) each select instruction causes three lines of tape to be read. The six bits of each tape line are read and assembled in the buffer from left to right to form one 18-bit computer word. The seventh bit of a tape line is ignored. A line cannot be read unless the eighth bit is punched. A "read the reader buffer" instruction transfers the contents of the reader buffer into the computer's accumulator.

When effecting a transfer from paper tape to the AC; the instruction selects the mode and clears the buffer, the PDP-9/L waits for a reader flag which indicates that the buffer has been loaded, and then the buffer contents are transferred to the AC.

When the PC03 Tape Punch is selected by an IOT instruction, data in the PDP-9/L accumulator is transferred to the punch buffer and then, without further instruction, is punched in the tape. Operation of the punch is by programmed instruction. The motor runs only when the punch has been selected. An out-of-tape switch on the punch mechanism, through which the unpunched tape must pass, will close when approximately 1 in. of tape remains to inhibit punch operation.

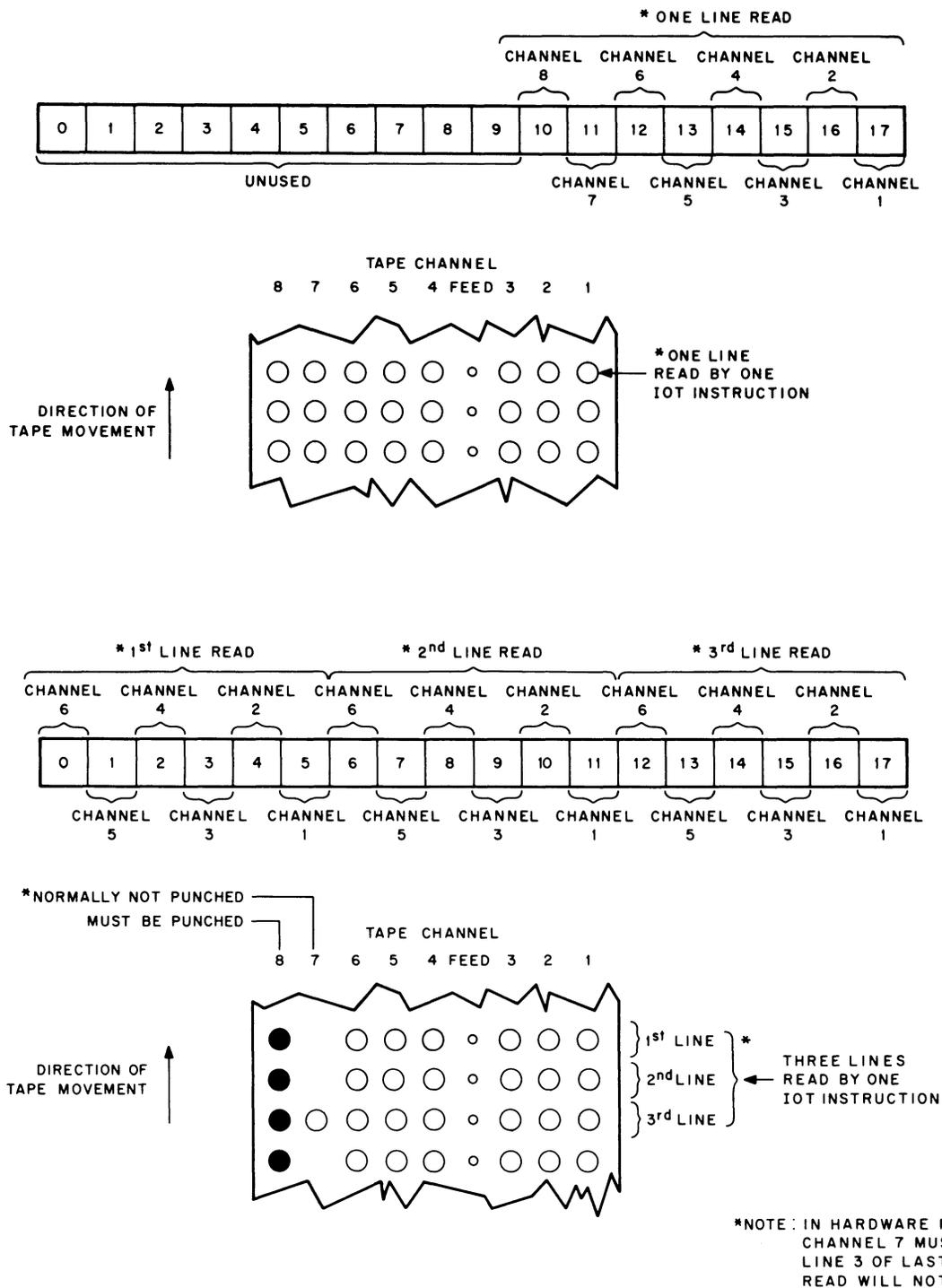


Figure 3-5 Perforated Tape Format

When the punch is operated in the alphanumeric mode, each select instruction causes one line of tape (eight bits) to be punched. Each hole in a tape channel corresponds to a binary 1 in the appropriate bit of the punch buffer. A feed hole is punched for each command, even if the buffer contains all 0s (see Figure 3-5 a).

When the punch is operated in the binary mode, each select instruction causes one line of tape (eight bits) to be punched. Holes are punched in channels 6 through 1 as a function of binary 1s in bits 12 through 17 of the accumulator, respectively. Channel 8 is always punched and channel 7 is not punched, thereby conforming to standard binary tape information format.

3.4 OPERATING INSTRUCTIONS

For routine operation of the PC09C refer to the explanations contained within Table 3-3, Controls and Indicators. For the occasional procedures of loading and replenishment of tape stock, refer to the step-by-step procedures given in this paragraph.

3.4.1 Loading Blank Tape

To load blank tape for punching, proceed as follows:

- a. Pull the PC09C straight out of the rack on its drawer slides, remove and discard the exhausted tape supply carton.
- b. Press the FEED button on the tape punch until the stub end of tape stops moving out of the machine.
- c. Pull the stub out of the exit slot.

CAUTION

Do not merely pull the tape out of the block. Doing so may jam the feed wheel. Pull gently and in-line with tape motion.

- d. Install a carton of tape in the well provided on the tape punch chassis (see Figure 3-6).

NOTE

If the chad box is full, it is a good practice to empty it at this time.

- e. Feed the new tape out of the carton, through the diagonal tape guide slot and directly into the punch block. Guide the tape into the block gently, as far as it will go.

- f. On the front panel, press and hold the FEED button. As punching occurs, gently push tape through the block until it feeds automatically.
- g. Release the FEED button and tear off the tape on the exit side of the tape tear plate.

NOTE

The tape should sever at the feed hole (see Figure 3-7 a).
If it does not, the tear plate position should be adjusted
(see Maintenance Chapter, Section 5.2.4).

- h. Press the FEED button again until a leader exits the machine. Splice the tail of the spent tape to the head of the fresh tape by either overlapping the edges and glueing (see Figure 3-7 b), or by butting the edges and securing with tape which has been designed for this purpose (see Figure 3-7 c)

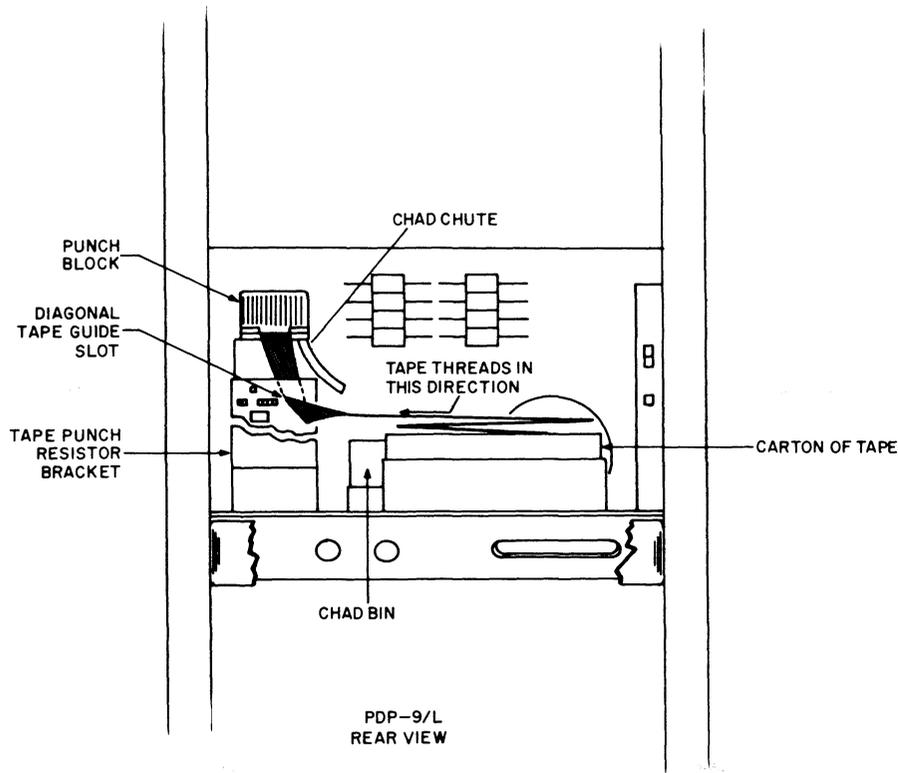


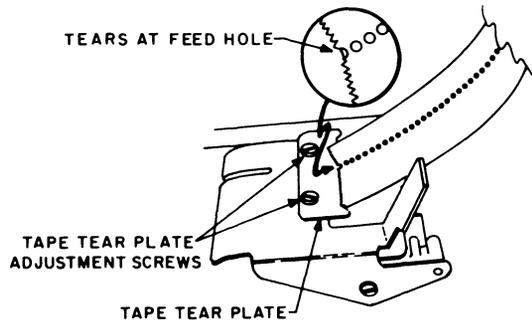
Figure 3-6 Loading New Tape in PC09C

3.4.2 Loading Prepunched Tape

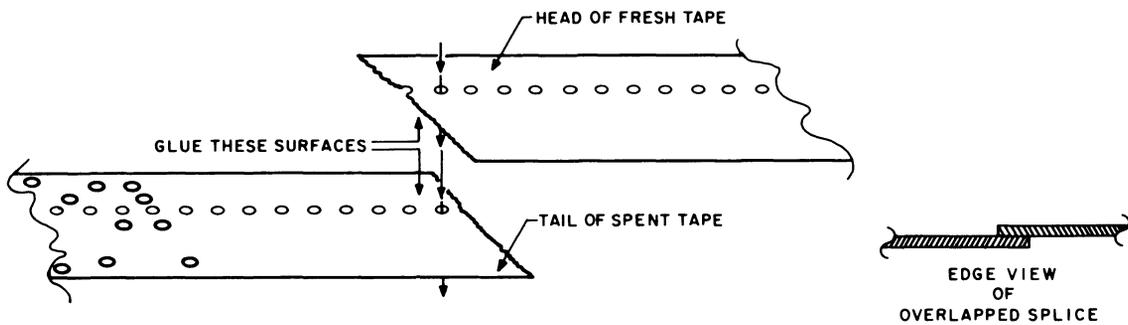
To load prepunched tape for readin, proceed as follows:

- a. Raise the tape retainer and load the tape into the right-hand bin. Position the tape on the platform with the feed holes engaged by teeth of the drive gear.
- b. Snap the retainer down.

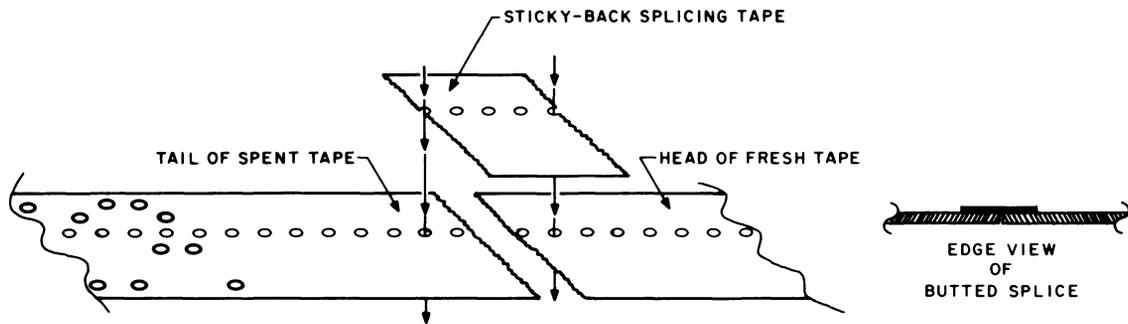
- c. Momentarily depress the tape feed pushbutton. This will correct any misalignment of the tape with respect to the drive teeth, and it will clear the reader out-of-tape flag.
- d. Set address switches 3 through 17 on the console to the starting address for the read-in.
- e. Depress the I/O RESET key and then the READ IN key to initiate reading of the tape.



a. TAPE PREPARED FOR SPLICING.



b. OVERLAPPED SPLICE.



c. BUTTED SPLICE

Figure 3-7 Tape Splicing

3.5 PROGRAMMING NOTES

In operating the PC09C under program control, the interaction of the various conditions which raise the device flag should be kept in mind so that no confusion will result as to what caused the flag to be raised. In the punch the POWER button, when in OFF position, is connected to the special PUN NO TAPE logic which can be sensed by the IORS facility; thus, the OFF position has the same effect as the TAPE switch in raising the PUN FLG. In the reader, a no tape condition will generate a PROG INT RQ and will raise the RDR FLG. An extended or unattended program should make use of the IORS facility to test the tape status before each RSA, RSB, PSA or PSB instruction.

CHAPTER 4

PRINCIPLES OF OPERATION

This chapter discusses the principles of operation of the PC09C. Included are a functional block diagram discussion and a detailed circuit analysis which define the operation of the PC09C specifically as part of the PDP-9/L system. Where necessary for clarity, the circuit analysis paragraphs trace the source or destination of certain signals to schematic and logic diagrams which are part of the basic PDP-9/L Maintenance Manual, but which are not included in this manual. In addition to the standard component references used in all previous manuals, an additional reference to grid coordinates has been included in these discussions. Interpretation of this referencing system is given in the circuit analysis paragraph.

4.1 FUNCTIONAL BLOCK DIAGRAM DISCUSSION

The PC09C Tape Reader/Punch is shown in drawing PC09-C-2 and functionally in the block diagram of Figure 4-1. The unit may be considered as two independent assemblies which share only grounds and some dc voltages.

The photoelectric tape reader consists of an electromagnetically stepped drive motor, a light source (OSRAM Lamp 6475), a photovoltaic read head, and a photoamplifier circuit (G904) for the photocell outputs. The read head, located below the tape, contains nine photovoltaic cells which are physically arranged to sense or read perforations in the light data tracks or channels of the tape in the tape feed-hole track. The light source is directly above the photocells.

Light passing through any hole in the tape will activate its individual photocell which, in turn, will feed an individual photoamplifier producing a -3V output (RD HOLE X) for transmission to the external processor. Circuits within the reader control regulate the transmission of data read from the tape.

The amplified output of the feed-hole diode may be used by the control circuits, if sampled between character locations, as a TAPE OUT indication. The reader feed switch, when pressed, feeds an enabling ground to the reader control resulting in 'tape-feed-without-read'.

The tape punch consists of an SCR-driven continuous-motion drive motor, a solenoid activated tape-punching mechanism which is fed by a solenoid driver register within the punch control, a reluctance pickup for synchronization of the punch-feed operations, and a 'punch feed/punch out-of-tape' circuit with its associated indicator and sensor. The 'feed' and 'out-of-tape' functions are interlocked with the punch POWER on/off switch.

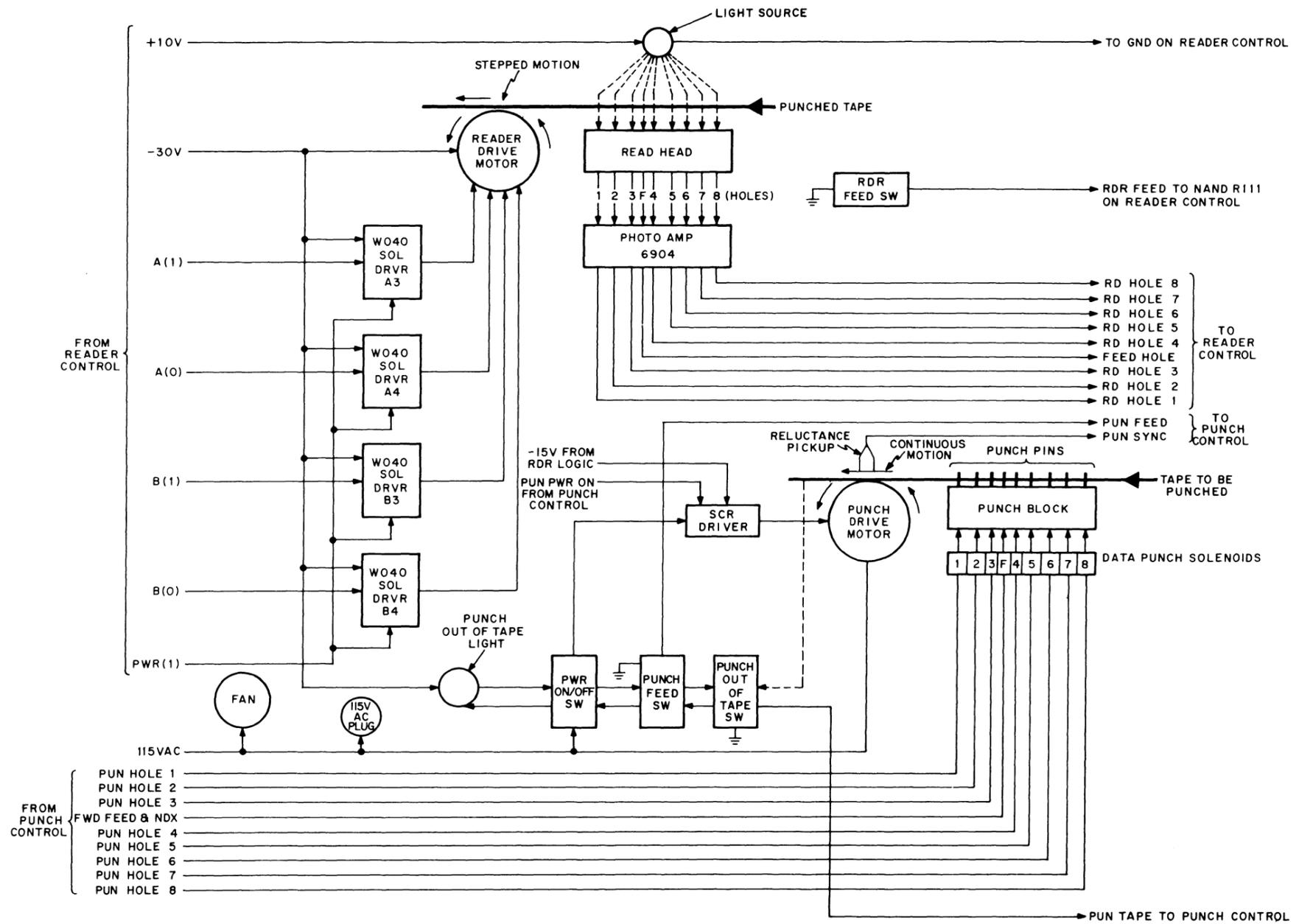


Figure 4-1 PC09C Functional Block Diagram

The 115 Vac power, which is applied by female connector to a panel-mounted receptacle at the rear of the PC09C, is shared by both a convenience outlet and the self-contained equipment fan.

4.2 THEORY OF OPERATION

4.2.1 General

As in previous sections of this manual, the PC09C Tape Reader/Punch theory of operation is divided into discussions of the two subassemblies. The PC02 Tape Reader discussion is followed by a discussion of the PC03 Tape Punch.

4.2.2 PC02 Tape Reader

A Type HS50 SLO-SYN Precision Stepping Motor is the primary element in the reader tape transport system. Electromagnetic stepping of the motor, under electronic control, frees the system of the maintenance problems inherent in mechanical stepping systems. The resultant reduction in moving parts increases the reliability of the unit at its higher speed of operation.

The motor contains four bifilar (counter-wound) windings. Driving current, applied to pairs of windings in the proper sequence, produces motor movement. The continuous application of drive current to a single pair of windings generates a holding force which does not develop rotational torque.

Solenoid drivers provide drive current to the four motor windings. External switching of the activating inputs to these drivers rotates the motor to feed the perforated tape past the read station.

Eight solenoid drivers, two for each winding, are provided. The stepped activation of both solenoids in each of two pairs (see Figure 4-2) causes rotation of the motor. When a holding force is required, the stepping action is stopped, and only one driver in each selected pair is activated. The single drivers produce sufficient force to hold the motor static, with a lower power drain and subsequent reduced heating effect in the motor and the drive circuits.

Switching the activation of the solenoid pairs at 1.667-ms intervals results in tape reading at the rate of 300 characters per second. The system may also be operated in a single-character stop-start mode at the rate of 25 characters per second.

Nine photosensitive diodes are arranged below the tape track perpendicular to the direction of tape movement. A light source, located directly above the diodes, provides the light necessary for sensing the holes in the tape. Eight of the diodes sense the coded holes; the ninth diode senses the presence of a feed hole. The photocell output, when shuttered from the light, sits at a -2.8 Vdc to -3.2 Vdc level, depending upon the setting of the threshold sensitivity potentiometer. When exposed

to the light, the output of the photocell increases (in a positive direction) above its preset shuttered value. Nine photoamplifiers continuously monitor the outputs of the diodes to provide a -3 Vdc output when a hole is sensed, and a 0 Vdc output when no hole is sensed.

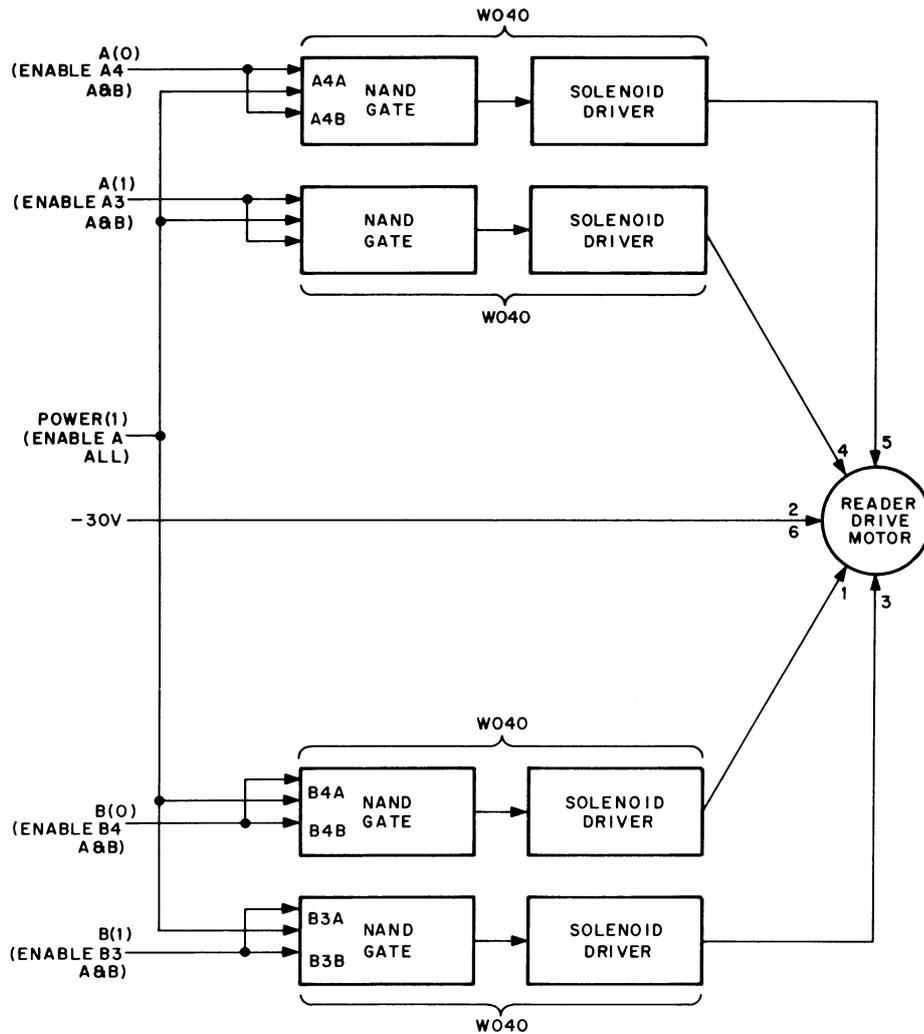


Figure 4-2 Reader Motor Drive Circuit, Simplified Block Diagram

By synchronizing its sampling of the photoamplifier's outputs with its inputs to the motor drive circuits, the external controller selects the output levels of the photoamplifiers which represent valid punched data.

The external controller provides pair-sequential inputs to motor-controlling solenoid drivers. The drivers generate the current needed to activate the windings of the synchronous tape-feed motor. Each switching of the paired inputs to the solenoid drivers causes the motor to rotate 1.8 degrees. Switching the driver inputs 200 times, therefore, results in one complete revolution of the motor (1.8 degrees x 200 = 360 degrees).

A sprocket wheel, containing 100 feed-hole engaging pins about its periphery, performs the actual tape feeding. This sprocket wheel mounts on, and rotates with, the shaft of the synchronous tape-feed motor. This results in tape movement equivalent to 100 character positions for each full revolution of the motor.

The following discussion describes the operation of the channel 1 photocell amplifying circuit. All other channels operate in an identical manner. The referenced amplifying circuit is on the left center of engineering drawing CS-C-G904-0-1 in Chapter 6 of this manual.

Photoamplifier G904 accepts the output of the photocell from channel 1, at terminal BN, through terminal N of the W023 Connector. When the photocell does not sense light (no hole) a bias level, determined by the setting of the threshold sensitivity potentiometer, is applied to terminal BN and the base of the left side of differential amplifier Q1. In this state, the left side of Q1 is cut off, permitting the right side of Q1 to conduct. The current flow through the right side of Q1 produces a voltage drop across R5 of approximately 10.7 Vdc. Current flows into the base of Q2, causing it to conduct. With Q2 conducting, the ground potential at its emitter is felt at the collector producing a 0 Vdc output at AD.

When the photocell senses light, a small positive voltage change occurs at terminal BN. This voltage drives the left side of Q1 to conduction, disturbing the balance of current flow and cutting off the right side of the transistor. With the right side of Q1 cut off, diode D1 clamps the right collector of Q1 and the base of Q2 to a point slightly more positive than ground. This cuts off the conduction of Q2. With Q2 cut off, diode D2 clamps both the collector and output terminal AD to a -3 Vdc level.

To summarize: the sensing of a hole in any channel of the tape produces an output of -3 Vdc from the photoamplifier terminal corresponding to that channel. The lack of a hole in any channel results in a photoamplifier output of 0 Vdc (ground).

The HS50 SLO-SYN Precision Stepping Motor drives the tape past the read station. This motor contains six input terminals connected as shown in Figure 4-3. Terminals 1, 3, 4, and 5 connect to Type W040 Solenoid Drivers, which supply drive current to the windings. Terminals 2 and 6 connect to the motor input-voltage supply (-30 Vdc). Correct operation of the system at the rate of 300 lines per second requires proper sequence and timing of the inputs to the solenoid drivers.

Drawing D-BS-PC09-C-2, located in Chapter 6 of this manual, shows the connection of the solenoid drivers to the motor. Note that each driver symbol contains an identifying letter/number code (A3, A4, B3, B4). This code refers to the physical location of the circuit module in the FLIP CHIP connector block.

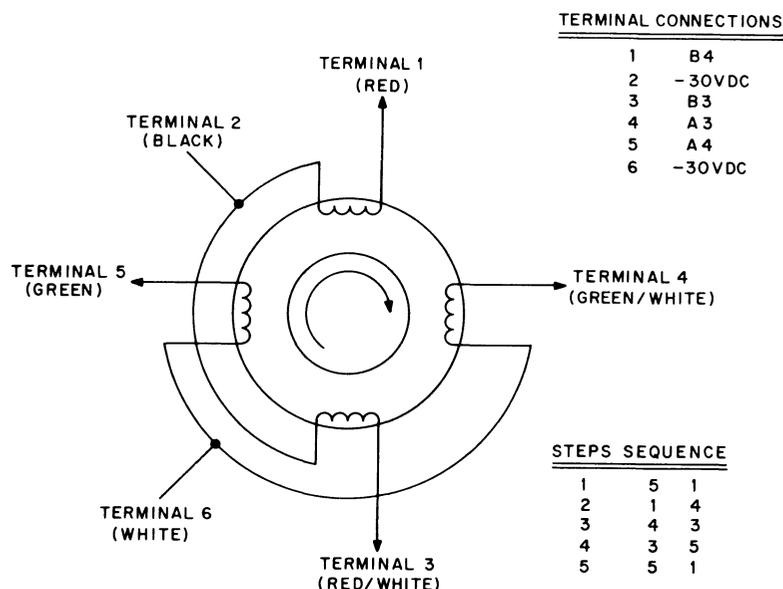


Figure 4-3 Tape Feed Motor, Simplified Schematic Diagram

The W040 Solenoid Driver module contains two discrete driver circuits with independent inputs and outputs. Each driver output circuit in this application feeds into a series-connected current-limiting resistor. The jumpered ends of the resistors from each module connect to one input winding of the motor. Each section of a driver module provides 600 mA to its winding for a total drive current of 1.2A per winding. The solenoid driver pairs produce the torque required for operation at a rate of 300 lines per second.

For the purpose of the discussion which follows, the A section consists of that section of the drive module served by inputs D and E. Conversely, the B section consists of that section of the module served by input K.

Each driver section contains a 2-input NAND gate. As shown in D-BS-PC09-C-2, terminal P of W023 at A1 provides one -3 Vdc level to each of the input gates (D, K) of driver A4. Terminal U of the W023 connector at A1 furnishes the second input to this and all other A sections of the driver at E. Terminal J of driver A4 is left unconnected, permitting terminal K to assume full control of the B section of the driver.

For instance, a -3 Vdc level, applied to terminals P and S of W023 at A1, supplies two of the four required inputs to modules A4 and B4. The application of a -3 Vdc level to pin E of all modules through pin U of the W023 connector at A1 provides the third required input to these drivers. (Terminals R and T of the W023 connector are at 0 Vdc, disabling drivers A3 and B3.)

Upon receipt of these three inputs, both sections of drivers A4 and B4 conduct, providing drive current to windings 5 (green) and 1 (red). The applied drive current rotates the motor 1.8 degrees and moves the tape a distance equal to one-half a character position (see Figure 4-3).

The application of a -3 Vdc level, 1.667 ms in duration, to pairs of input terminals in the sequence indicated below produces continuous tape feeding at the rate of 300 lines per second. A 3 Vdc level must be applied to terminal U of W023 for the entire period during which tape feeding is desired. A 0 Vdc (ground) level must be applied to the inactive terminals (see Figure 4-4).

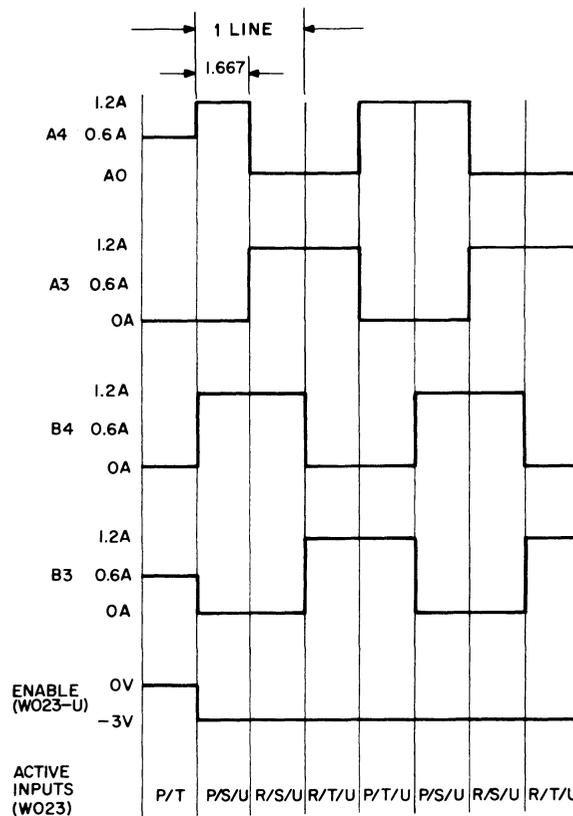


Figure 4-4 Sequence and Timing of Inputs to Solenoid Drivers

Assume that a step 1 (see below) P and T are active (-3 Vdc), and terminal U is inactive (0 Vdc). In this state, one section of driver A4 and one section of driver B3 are activated. The current produced is not sufficient to move the motor, but it is sufficient to hold the motor at rest.

<u>Step</u>	<u>Active W023 Terminals</u>
1	P,T
2	P,S,U
3	R,S,U
4	R,T,U
5	P,T,U

At step 2, P, S, and U are active, triggering both drivers in A4 and both drivers in B4. The motor rotates 1.8 degrees, moving the tape a distance equal to one-half line.

At step 3, R, S, and U are active, triggering A3 and B4. The motor rotates an additional 1.8 degrees providing a total tape movement to this point of one full line.

Similarly, steps 1 through 5 move the tape over a distance of two full characters. Continuous stepping of the inputs in this sequence at the rate of 1.667 ms per step produces a tape-feed rate of 300 lines per second.

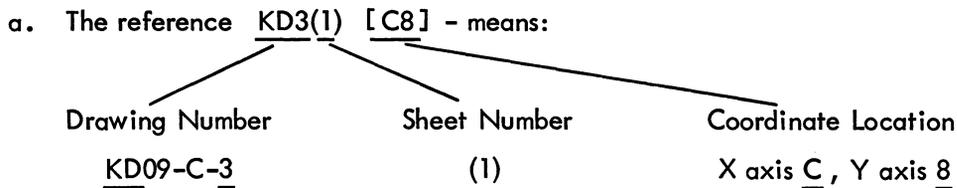
If the external controller cannot provide inputs at this rate, it is necessary to reduce the feed rate to approximately 25 lines per second. This requirement reflects the acceleration and deceleration characteristics of the motor. The inertial characteristics of the system require that operation not be started at the full 300 line per second rate. In the PDP-9/L, means have been provided to accelerate the system from a start to the full-speed rate in no more than 30 steps.

4.2.3 PC03 Tape Punch

Information concerning the theory of operation of the PC03 Tape Punch is covered in detail in the Royal McBee Maintenance Handbook provided with each piece of equipment.

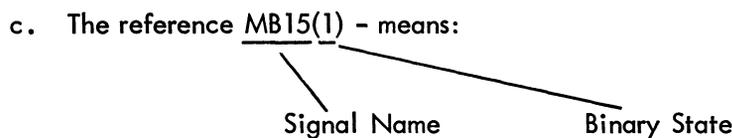
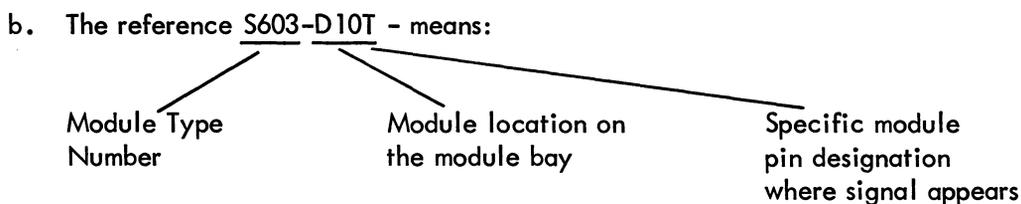
4.2.4 Tape Reader Control

The reader control is shown in drawing D-BS-KD09-C-9, sheets 1 and 2. The timing diagram for the reader control, while operating in either alphanumeric or binary mode, is given in drawing D-TD-KD09-C-17. The circuitry shown in drawing D-BS-PC09-C-2 is wired into the basic frame of the PDP-9/L. The following conventions have been adopted in referencing both drawings and circuit element locations to aid in reading the text.



NOTE

A drawing number and coordinate location is referenced each time the signal routes to another drawing. When discussion is confined within a single drawing, subsequent locations within that drawing are referenced alone. Therefore, when single coordinate locations appear in text, they refer to the last drawing number mentioned.



IOT instructions under program control start the reader, load an 18-bit buffer register with the information read from the tape, sense the status of the register, and transfer the information from the register to the AC via the input mixer I/O bus (B). The instructions select the reader for operation in either the binary or the alphanumeric mode, whichever is appropriate to the punched format.

Alternatively, the READ IN key on the operator's console can be used to enter data manually from the reader into core memory. A manual feed pushbutton above the reader's tape feed platform can be used to feed a tape through without reading. A ninth-channel photodiode senses the sprocket-driven feed holes in the tape. If the end of the tape is sensed, special RDR NO TAPE logic stops the reader and issues a program interrupt request.

An IOT RSA instruction selects reader operation in the alphanumeric mode. Each RSA causes one line of 8-bit information to be read into bits 10-17 of the reader buffer (RB). The binary mode is selected by an IOT RSB instruction. One 18-bit binary word occupies three lines of tape, each line

containing one 6-bit character. Each RSB instruction causes three successive lines of tape to be read into the appropriate bit positions of the RB (see Figure 4-5). In binary mode, channel 7 is never read (except during manual READ IN operations). Channel 8 must always be punched and read in order to gate each line into the respective RB positions; but it is ignored as an information bit. The reader flag goes up with each line in alphanumeric mode, and with every third line in binary mode.

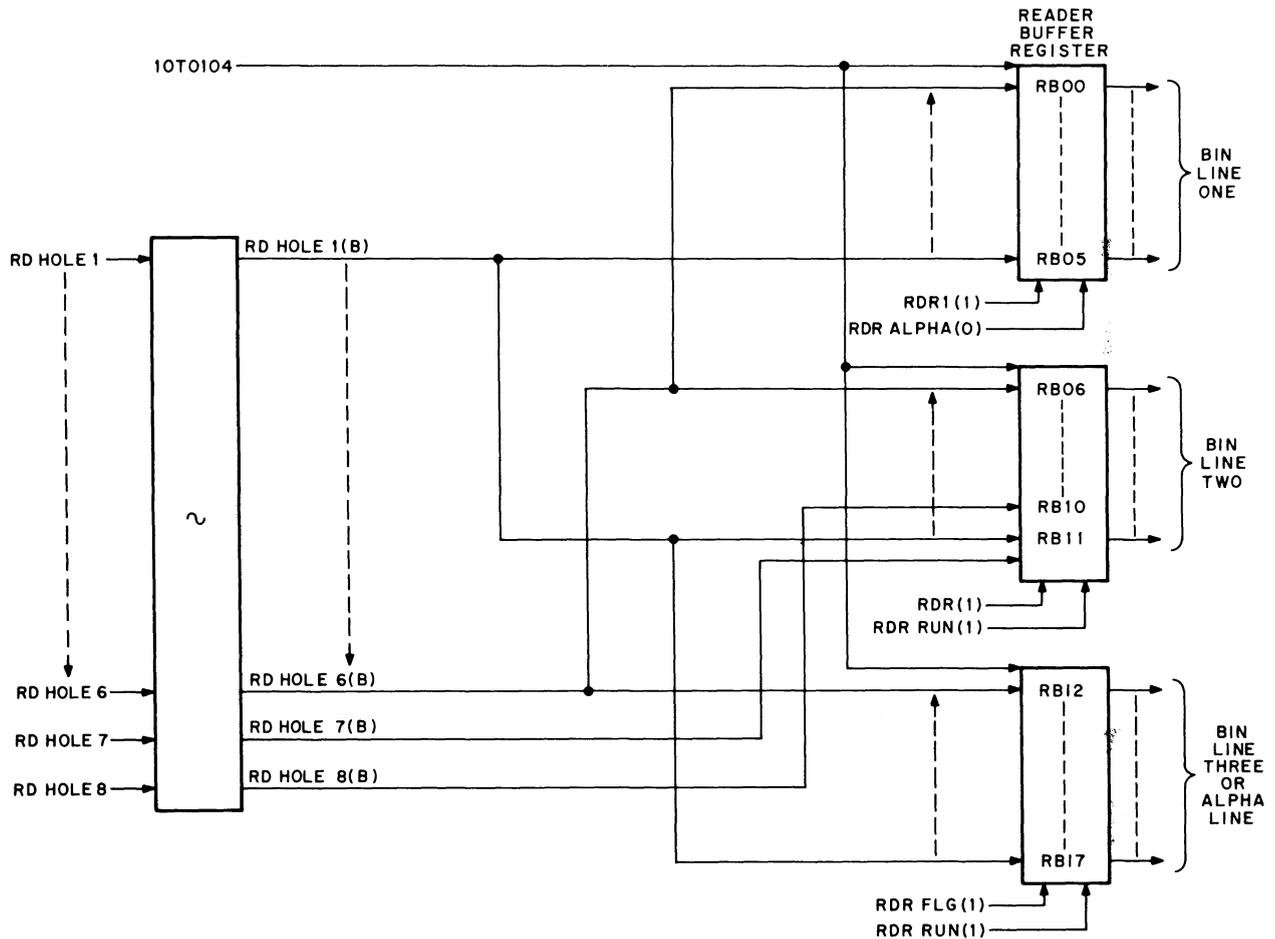


Figure 4-5 Reader Control, Functional Block Diagram

All IOT instructions associated with the reader are listed below. The logic functions that they perform follow.

IOT0101	RSF	Skip on reader flag
IOT0102	RCF	Clear reader flag and inclusively OR the RB and AC into the AC

IOT0112	RRB	Clear reader flag and AC, then transfer RB into AC
IOT0104	RSA	Clear reader flag and select reader in alphanumeric mode
IOT0144	RSB	Clear reader flag and select reader in binary mode

The RSB instruction 700144_g (select reader binary) is decoded in the CP's code detection circuits for the signal IOT(1). On drawing KD3(1) [C8], the IOT(1)B level samples the MB06-11 bits in the instruction to produce the appropriate DS0-5 levels, and IOT(1) [A7] further decodes DS0-2 to produce OXEN. OXEN is sent to the reader control, drawing KD9(1) [B7], to sample DS3-5, resulting in RDR SEL and RDR SEL B. RDR SEL then conditions the DCD gate at pulse amplifier S603-D10T. The gate now waits for the start of the third IOT execute period, at which time the CLK pulse counter IO0 steps to 0, strobing the MB15(1) gate on drawing KD3(3) [C6] to generate the IOP4P pulse.

IOP4P triggers the PA, on KD9(1) [C7], to generate the IOT0104 command. The generation of IOT0104 acts to reset the RDR FLG [D4], RDR 1 [D3], RDR 2 [D4], RDR ALPHA [D8] flip-flops; and sets the RDR RUN flip-flop [D7]. On KD9(2) [C8] it resets all the RB flip-flops. Note that RDR ALPHA is reset because SD0P is not generated on drawing KD3(1) [D1] due to a 1-condition of MB12.

RDR RUN(1) and RDR NO TAPE(0) are NANDed on KD9(1) [C3], and the grounded output is NORed to produce a negative RUN level. RUN is applied to NAND gate R111-E07R [B4]. Here the STOP DLY POS input is initially negative because the 45 ms STOP DLY is quiescent. RUN and the negative STOP DLY POS permit R111-E07UV to trigger the 1 μs GO DLY and to condition the RDR INDEX input DCD gate on drawing PC2 [C4]. When the GO DLY recovers, RDR GO sets the RDR CLK EN flip-flop [C6], applying RDR CLK ENABLE [B5] as a trigger to the reader CLK R401 and the clock control G913. At first the RDR CLK pulses occur at 5 ms intervals, but within 10 to 30 pulses the G913 accelerates the clock rate so that a RDR CLK pulse occurs every 1.67 ms. Each RDR CLK pulse strobes the conditioned DCD gate to generate RDR INDEX pulses.

The first RDR INDEX pulse sets the RDR PWR flip-flop [C4] and strobes the input gates of the RDR A and RDR B flip-flops [B7 and B6]. These flip-flops act as a Gray-code pulse counter whose outputs are used to drive the tape-reader synchro motor along with PWR(B) [D3] derived from the RDR PWR flip-flop. The RDR A and RDR B flip-flops step through a count of 00, 10, 11, 01, and back to 00 on successive RDR INDEX pulses. Their outputs go through S107 Inverters, on drawing KD9(2) [C3, C4], to four W040 Dual-Solenoid Driver modules at the reader motor (drawing PC2 [D5]). The solenoid driver modules actuate in pairs to drive two of four motor windings for motor rotation. The stepping RDR A and RDR B flip-flops sequentially select the pairs of solenoid drivers along with PWR (B) to drive two windings at a time for continuous motor rotation. This scheme requires that the RDR A and RDR B count be stepped twice to produce a tape movement equal to one line position. The RDR INDEX rate is thus twice the character rate (300 lines/s = 1 line/3.33 ms).

When a new tape has been loaded in the reader, or when the reader has completed a previous read operation, the tape will contain nothing but feed holes. This allows time for RDR CLK acceleration. The motor is driven by stepping RDR A and RDR B, but in the absence of punched holes in channel 8, the control logic prevents reading 0s into the RB, consequently preventing the RDR FLG from setting on three lines of blank tape. When the blank tape is exhausted and the first character is pulled into the reading position, RDR A and RDR B step to a count of either 00 or 11 (RDR A = RDR B). This indicates that the tape holes of the first character are in position above the photosensors. Since the reader is in the binary mode, the eighth channel is always punched and a RD HOLE 8 signal is seen at pin H of the S107 Inverter, on drawing KD9(2) [D4]. The RD HOLE 8 level becomes RD HOLE 8P + ALPHA which in turn conditions the DCD gate to the pulse amplifier S603-E08M, on drawing KD9(1) [C5]. At the same time, the sensed levels RD HOLE 1(B) through RD HOLE 6(B), on drawing KD9(2) [C5-7], condition the input gates to RB00-05 [C4-7].

On drawing PC2 [B7], the next RDR INDEX pulse steps RDR A and RDR B to 10 or 01, continuing motor rotation toward a between-character tape position. On drawing KD9(1) [C5], RDR A(1) and RDR B(0) or RDR A(0) and RDR B(1) produce the ground RDR COUNT level which will trigger pulse amplifier S603-E08M, since it has been conditioned by RD HOLE 8P + ALPHA, and as a result the RDR 1 flip-flop will be set. RDR 1(1) strobes the DCD gate conditioned by RDR ALPHA (0), on drawing KD9(2) [C8]. This gate triggers pulse amplifier S603-D10F which in turn strobes the DCD set gates on flip-flops RB00-05, placing 1s in any register positions conditioned by RD HOLE(B) levels. Since the RD HOLE(B) levels come from the tape-hole photosensors via S107 Inverters at W023-A17, a 1 in the RB denotes a punched hole and a 0 denotes a blank.

Returning to drawing PC2 [B7], the next RDR INDEX pulse will step RDR A and RDR B to 11 or 00 causing the drive motor to pull the next character into reading position. The second line of RD HOLE(B) levels are established at the DCD gates RB06-11 on drawing KD9(2) [C3-1 and B7].

Without any further reference to drawing numbers, the next RDR INDEX pulse produces the count of 01 or 10 resulting in another RDR COUNT. Since the RDR 1 flip-flop is already set, it has conditioned the DCD gate on the RDR 2 flip-flop permitting RDR COUNT to set the RDR 2 flip-flop. RDR 2(1) then triggers pulse amplifier S603-D10M which strobes the second character into RB06-11. The subsequent count of 00 or 11 causes reading of the third line of tape on the DCD gates for RB12-17.

On the next RDR INDEX, the count of 10 or 01 results in another RDR COUNT. Since the RDR 2 flip-flop has been set, the RDR FLG flip-flop DCD gate is now conditioned from NAND R111-E12 on drawing KD9(1) [C5], and RDR COUNT will set the flag. RDR FLG(1) triggers pulse amplifier S602-C09K on drawing KD9(2) [A7] strobing the third character into RB12-17. RDR FLG(1) also resets

the RDR RUN flip-flop on drawing KD9(1) [D7]; and generates both a PROG INT RQ from R111-E15 [D2], and RDR FLG(1)B to the CP via drawing KD4 [B8]. The PROG INT RQ goes to drawing KD3(2) [C4] to initiate a program interrupt.

Resetting the RDR RUN flip-flop on drawing KD9(1) [D7], results in \overline{RUN} from R111-C08 [C2], and disabling of the RDR 1 and RDR 2 latching sequence at PA S603-A01 [B6], R111-E12 [C5], and PA S603-E08 [C4]. It also disables the RDR INDEX to the RDR A and RDR B flip-flops on drawing PC2 [B7].

The program now enters a flag search and a service routine to transfer the contents of the RB in the AC, perform any desired operation on the contents, re-enable the PI facility, and issue another RSB to assemble the next word in the RB. If another RSB does not appear within 1.67 ms, the next RDR CLK pulse will reset the RDR CLK EN flip-flop on drawing PC2 [C6] since \overline{RUN} is now present at its DCD gate. RDR CLK EN (0) disables the RDR CLK [C4] and triggers the STOP DLY on drawing KD9(1) [B5]. The resultant STOP DLY POS from S107-E06(L) applied to R002-C03 on drawing PC2 [D7] holds RDR CLK EN in the reset state for approximately 60 ms, inhibiting RDR GO triggering. Upon recovery of the STOP DLY flip-flop a $\overline{STOP\ DLY}$ coincides with \overline{RUN} at the RUN PWR DCD gate on PC2 [C4] which resets the RUN PWR flip-flop, thereby disabling the reader motor and causing it to decelerate. The 60 ms delay (STOP DLY) prevents a late RSB from restarting the reader motor immediately.

The RSA instruction 700104_g (select reader alpha) is decoded similarly to the process just described for RSB, except that MB12 on KD3(1) [D2] is now 0, producing a ground level SD0 to set the RDR ALPHA flip-flop on drawing KD9(1) [D7]. RDR ALPHA (1) at S107-C07T on KD9(2) [D4] now provides the RD HOLE 8P + ALPHA conditioning level (since channel 8 may or may not be punched in the alphanumeric mode). When the RDR A and RDR B flip-flops on PC2 [C6, C7] step to $A \neq B$, RDR COUNT on drawing KD9(1) [C5] sets RDR 1 as usual, but it also sets the RDR FLG flip-flop since it is now conditioned at its DCD gate [D4] by RDR ALPHA (1) and RDR RUN(1) from R111-C08 pins R and S, respectively. The setting of RDR FLG immediately disables the RDR 1 and RDR 2 latching sequence, and turns on the DCD gate, drawing KD9(2) [A8], which has been conditioned by RDR RUN(1). This strobesc RD HOLE 1(B)-6(B) into RB17-12. In addition, RDR ALPHA (1) at R111-E07 strobesc RD HOLE 7(B) into RB11, and RD HOLE 8(B) into RB10. Since RDR FLG is set immediately, a PROG INT RQ from R111-E15 on KD9(1) [D2] is issued on every line read as opposed to every three lines for an RSB instruction.

During RSA or RSB operations, ground RDR COUNT levels occur on alternate steps of RDR A and RDR B when $A \neq B$. $\overline{RDR\ COUNT}$ on drawing KD9(1) [C6] is applied to the DCD gates of the RDR NO TAPE flip-flop to sample the FEED HOLE condition. Since the $A \neq B$ condition occurs only when the tape is in a between-characters position, the FEED HOLE level should be at ground. If it is negative at RDR COUNT time, the tape may have torn. This places a ground conditioning level at pin L

of the DCD set gate for the RDR NO TAPE flip-flop. When $\overline{\text{RDR COUNT}}$ occurs, it sets the RDR NO TAPE flip-flop, generating $\overline{\text{RUN}}$ at R111-C08HJ [D2]. $\overline{\text{RUN}}$ on drawing PC2 [C6] stops the reader by resetting RDR CLK EN on the next RDR CLK pulse, thus entering the STOP DLY period as for normal shut-down procedure. RDR NO TAPE(1) on KD9(1) [D5] also generates a PROG INT RQ [D2] as though the RDR FLG were raised. An extended or unattended program should make use of the read status (IORS) facility to test the RDR NO TAPE status before each RSB or RSA.

Paper tapes contain 2 ft. of leader, for loading ease, and may contain any amount of trailer. These leaders and trailers usually contain nothing but feed holes. Excess leader and trailer can be fed through to the take-up bin by depressing the feed button above the loading platform. When pressed, the feed button supplies a ground RDR FEED level to NOR gate R111-C08JH on drawing KD9(1) [D2], resulting in a negative RUN. RUN starts the reader as for programmed RSA and RSB operations, but the absence of RD HOLE 8P + ALPHA C5 inhibits input strobing of the RB. When released, the feed button removes the RDR FEED ground from the logic, turning on $\overline{\text{RUN}}$ to stop the reader via PC2 [C5].

The RCF instruction (700102) clears the RDR FLG, RDR 1, and RDR 2 flip-flops, inclusive-ORs the contents of the AC and the RB at I/O bus(B), then gates the result into the AC. The RRB instruction (700112) clears the AC and the flip-flops mentioned above, then gates the contents of the RB into the AC.

During the IOT fetch for the RCF instruction, the contents of the AC are transferred into the AR and MB14(0) is detected to set ARO and IO BUS ON. These levels place the AR contents on the I/O bus via the A bus and ADR at the beginning of IOT execute. During execute, the contents of the RB are gated into the input mixer and placed on I/O bus(B), where they are ORed with the contents on the I/O bus.

For the RRB instruction, MB14(1) is detected to set ACI. ACI(1) places 0s in the AC from the inactive O bus, thus clearing the AC. The fetch cycle logic for both cases is explained in the PDP-9/L Maintenance Manual under "Input/Output Transfer (IOT) Instructions."

In both cases, MB06-11 are detected in the I/O control logic to produce RDR SEL, and when IO1 sets, signaling the start of the second IOT execute period, it produces IOP2P on drawing KD9(1) [C3] in conjunction with MB16(1). IOP2P sets IOT0102 in conjunction with RDR SEL on drawing KD9(1) [C7].

When the IOT0102 flip-flop sets, IOT0102(1) triggers the DCD gate for PA S602-C09U to produce CLR RDR which is used to reset the RDR FLG, RDR 1 and RDR 2 flip-flops. IOT0102(1) also generates an INT RD RQ BUS level on drawing KD3(3) [C8]. This level is NORed at R111-F19UV [D5] for RD RQ(B), then NANDed for AC RD [D3] at CLK DLYD time. On drawing KC19(2) [C8], AC RD sets the ACI flip-flop. It also becomes AC RD(B) which, on drawing KC13 [D7], generates LIO.

At the input mixer, drawing KD7(1) [D5], IOT0102(1) generates RDR ON BUS. The RDR ON BUS level at [B8] gates RB00-17 at pins M into the input mixer gates (B141s). The gate outputs are NORed (R123s) onto I/O bus(B). In an RCF instruction, the contents of the AC (via the AR) will also be present at the output NOR gates from the I/O bus. If an RRB instruction is being executed, the AC will have been cleared and nothing will appear on the I/O bus. LIO gates the results on the I/O bus(B) onto the O bus, and ACI(1) then gates them from the O bus into the AC.

The RSF instruction 700101 (skip on reader flag) senses the status of the RDR FLG and, if it is set, the reader control logic issues a skip request to the CP causing the program to skip the next instruction. On drawing KD3(1) [C8], MB06-11 are detected as usual to produce RDR SEL on drawing KD9(1) [B7]. On KD3(3) [B7], IO0 sets, signaling the start of the first IOT execute period, producing IO0(1) which at [C3] joins MB17(1) to yield IOP1P.

On drawing KD9(1) [A8], IOP1(1) and RDR SEL(B) sample the state of the RDR FLG. If the RDR FLG is set, the INT SKP RQ BUS will go to ground which will trigger pulse amplifier W612-F18D on drawing KD3(3) [D6] producing the IO SKIP signal needed to set the SKIP flip-flop in the CP, drawing KC14 [D3].

The RSF instruction idles through its remaining execute periods until PCO(1) at [C5] of the BGN process word generates CI17 in conjunction with SKIP(1). CI17 initiates a carry in the ADR on drawing KC21(3) [C2], and PCO(1) on drawing DC20 [B7] gates the contents of the PC through the ADR to the MB for the next instruction fetch cycle. Thus, the address in the MB contains the PC address + 1.

4.2.5 Tape Punch Control

The punch control is shown on drawing D-BS-PC09-C-1, sheets 1 and 2. The timing diagram for the punch control for both alphanumeric and binary modes is given in drawing D-TD-KD09-C-10. The same referencing conventions adopted for discussion of the tape-reader control logic have been adopted for this discussion.

IOT instructions under program control start the punch, load a buffer register with 6-bit binary or 8-bit alphanumeric information from the AC (AR) via the I/O bus, and sense the status of the flag (see Figure 4-6). The instructions select the punch for operation in either the binary or the alphanumeric mode.

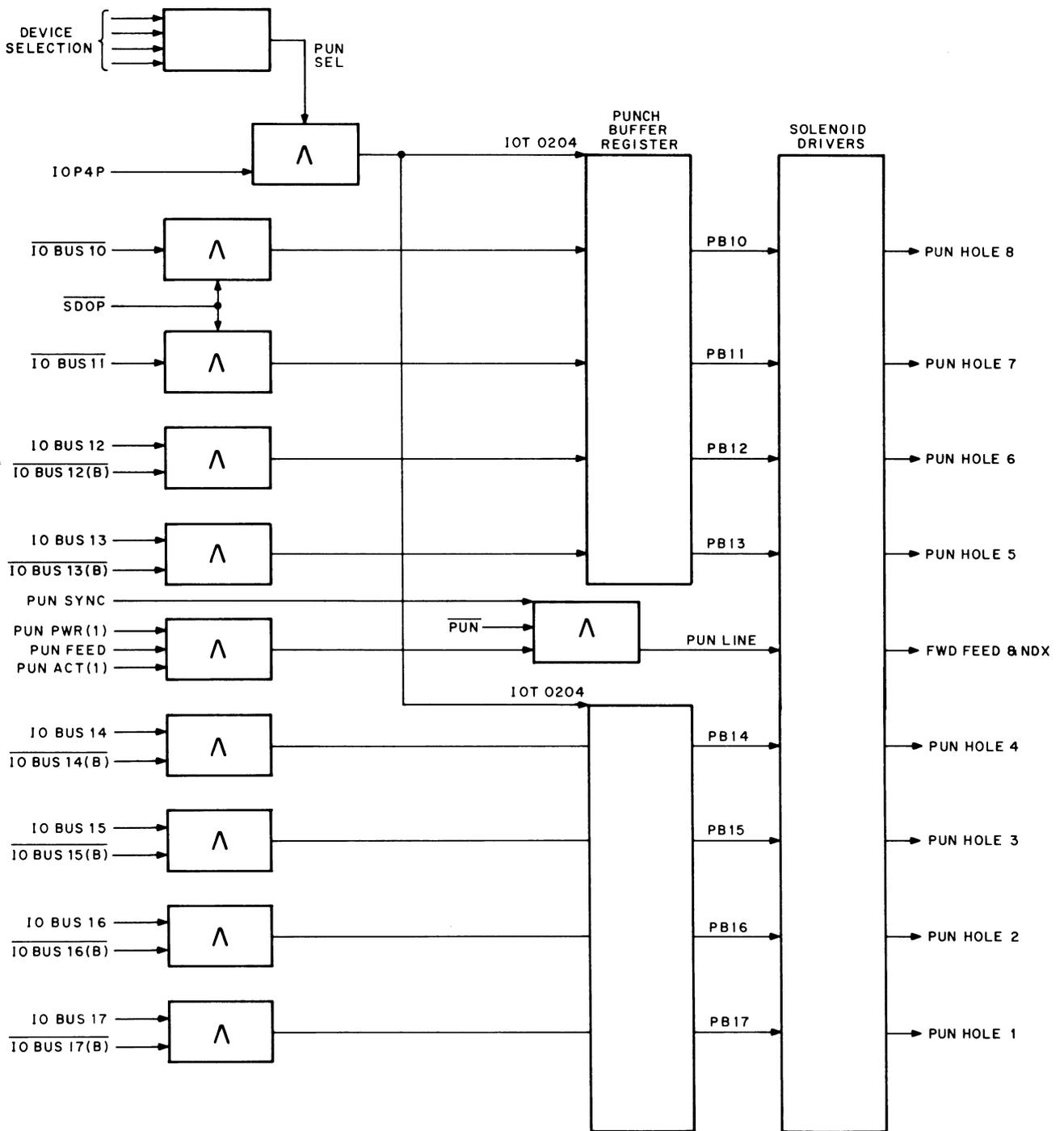


Figure 4-6 Punch Control, Functional Block Diagram

Alternatively, the manual FEED button on the punch panel may be used to drive the tape for punching nothing but feedholes. The POWER button on the punch panel should be pressed ON in either case for punch operation. The OFF position of the button is connected to special PUN NO TAPE logic. The PUN NO TAPE condition can be sensed by the IORS facility when the tape runs out or when the POWER button is OFF. PUN NO TAPE thus provides a warning when approximately 2 in. of tape remain.

An IOT PSA instruction selects the punch for alphanumeric operation. Each PSA causes one line of 8-bit information to be gated into the punch buffer (PB), and synchronizing circuits in the punch control logic use the buffer contents to drive the punch mechanism. An IOT PSB instruction selects the punch for binary operation, in which each PSB causes one line of 6-bit information to be gated into the PB. In binary mode, three successive lines of information comprise one 18-bit binary word. Channel 7 is never punched (except for READ IN use); channel 8 is always punched to indicate binary mode for the tape reader, but the bit is ignored as an information bit. The punch flag goes up with each line punched in either mode.

All IOT instructions associated with the punch are listed below. The logic functions that they perform follow.

<u>Instruction</u>	<u>Mnemonic</u>	<u>Logic Function</u>
IOT0201	PSF	Skip on punch flag
IOT0202	PCF	Clear punch flag
IOT0204	PSA	Clear flag and select punch in alphanumeric mode
IOT0214	(Micro coded)	Clear AC and flag, and select punch in alpha mode (punch feed holes only)
IOT0244	PSB	Clear flag and select punch in binary mode

The PSB instruction 700244 (select punch binary) is decoded in the CP's op-code detection circuits for IOT(1). On drawing KD3(1) [C8], the IOT(1)B level samples the MB06-11 bits in the instruction to produce the appropriate DS0-5 levels, and IOT(1) further decodes DS0-2 to produce OXEN. OXEN goes to the punch control, drawing PC1(1) [B7], to sample DS3-5, resulting in PUN SEL. PUN SEL conditions a DCD gate at pulse amplifier S602-D24K [C7]. The gate now waits for the start of the third IOT execute period, at which time the CLK pulse counter IO0 steps to 0, strobing the MB15(1) gate on drawing KD3(3) [C5] to generate IOP4P. The IOP4P pulse triggers the pulse amplifier on PC1(1) [C7] to generate the IOT0204 command.

IOT0204 resets the PUN FLG flip-flop [B5], sets the PUN ACT flip-flop [B4], and strobes the input DCD gates of the punch buffer flip-flops PB10-17 [C7-3]. Since PSB is an output transfer

instruction, the contents of the AC were placed in the AR, then gated onto the I/O bus and IO BUS(B) during the IOT fetch cycle. In binary mode, IO BUS 12 through IO BUS 17 on the PB12-17 DCD gates contain the first 6-bit character of the 18-bit word to be punched. These are strobed into PB12-17 by IOT0204. Also, in binary formatting, bit PB11 (hole 7) must always receive a 0 and bit PB10 (hole 8) must always receive a 1. In the PSB instruction, MB12 is 1, producing a ground SDOP on drawing KD3(1) [D2]. SDOP at ground, on drawing PC1(1) [C7], causes PB11 to reset and PB10 to set regardless of the I/O bus levels.

PUN ACT(1) [B4], set by IOT0204, starts the punching synchronization by triggering the 3s PUN PWR delay, R303-CD27D. On the leading edge of the 3s delay period, PUN PWR(1) issues the PUN PWR ON level to energize the punch drive motor, drawing PC2 [D3], and also triggers a 1s delay, R302-C25V. The 1s delay period allows the motor to accelerate to proper operating speed. Upon recovery, the inverted PUN SPD level goes negative.

PUN ACT(1) NORed at R111-D26NP on drawing PC1(1) [A7] enables R111-D26HJ with the recovered PUN SPD to condition the DCD gate at the 10-ms delay R302-C25M. The 10-ms delay is triggered by a PUN SYNC signal coming from a reluctance pickup coil at the punch motor shaft. When the pickup coil senses that the punch motor has rotated to a preadjusted punch position, the PUN SYNC signal is issued to trigger the delay. The delay output goes negative producing PUN for 10 ms, during which time the punching operations take place. The PUN signal at [A3] generates PUN LINE at S107-C19J. PUN LINE at [D7] then enables the solenoid driver gates W040 at the outputs of all PB flip-flops which are set to 1. The affected solenoid drivers supply the drive current to the respective bit punch mechanisms. PUN LINE at [C8] also enables the two parallel solenoid drivers which supply enough current to punch the feed hole (NDX) and to advance the tape to the next line (FWD FD).

When the 10-ms punching period lapses, PUN [B6] reverts to $\overline{\text{PUN}}$, setting the PUN FLG [B5] and resetting the PUN ACT flip-flop [B4]. The resulting PUN FLG(1) generates a PROG INT RQ for the I/O control logic from R111-C26H. Although PUN ACT has reset, the 3s PUN PWR delay remains to drive the punch motor at continuous operating speed. To punch the next line, another PSB follows in the service routine honoring the PROG INT RQ. Succeeding PSB instructions will retrigger the 3s PUN PWR delay before the previous delay runs out. When the last line is punched the last delay lapses to stop the motor.

The PSA instruction 700204 (select punch alpha) is decoded and processed in identical fashion to PSB resulting in the IOT0204 command, except that MB12 is 0, producing a negative level ($\overline{\text{SDOP}}$) which gates IO BUS 10 and IO BUS 11 levels into PB10 and PB11 for alphanumeric formatting.

When the PSA instruction is microcoded with a 1 in MB14 (700214), it will clear the AC and select the punch for alphanumeric mode. This instruction can be used to punch feed holes in tape

leaders and trailers, and to space the punching of information for timing purposes. MB14(1) is detected in the CP's op-code detection circuits to clear the AC during IOT fetch.

The PSF instruction 700201 (skip on punch flag) senses the status of the PUN FLG. If the flag is set, the punch control logic issues a skip request to the CP, and the program skips the next instruction.

MB06-11 are detected on drawing KD3(1) [D7] to produce PUN SEL on drawing PC1(1) [C4]. When IO0 sets, signaling the start of the first IOT execute period, it produces IOP1P on drawing KD3(3) [C2] in conjunction with MB17(1). IOP1P sets the IOP1 flip-flop yielding IOP1(1).

On drawing PC1(1) [D2], IOP1(1) and PUN SEL sample the state of the PUN FLG. If the PUN FLG is set, the INT SKP RQ BUS goes to ground, triggering pulse amplifier W612-F18D on drawing KD3(3) [D6]. The resultant IO SKIP signal sets the SKIP flip-flop in the CP, drawing KC14 [D3]. The PSF instruction idles through its remaining execute periods, until PCO(1) [C5] of the BGN process word generates CI17 in conjunction with SKIP(1). CI17 initiates a carry in the ADR on drawing KC21(3) [C2]; and PCO(1), on drawing KC20 [B7], gates the contents of the PC through the ADR to the MB for the next instruction fetch cycle. Thus, the address in the MB contains the PC address +1.

The PCF instruction 700202 (clear punch flag) clears the PUN FLG. On drawing KD3(1) [D7] MB06-11 are detected to produce PUN SEL as usual; and when clock pulse counter IO1 [B7] sets, signaling the start of the second IOT execute period, it produces IOP2P in conjunction with MB16(1) [C3]. On drawing PC1(1) [B6], IOP2P strobes the input DCD gate to pulse amplifier S602-D24U, preconditioned by PUN SEL. The resulting CLR PUN pulse resets the PUN FLG.

The POWER pushbutton S1 on the punch's front panel should be pressed to ON before any punch operation. Although unrelated to the application of power to the punch, the OFF position applies a ground $\overline{\text{TAPÉ}}$ level, drawing PC1(2) [C7], to the PUN NO TAPE gate R111-D21UV, drawing PC1(1) [B3]. The resulting PUN NO TAPE level appears as the IO BUS 09 status bit when using the read status (IORS) facility. Thus, the OFF position has the same effect as the $\overline{\text{TAPÉ}}$ switch S3. S3 is a microswitch which is mounted just ahead of the tape punches and whose contacts are separated by the threaded paper tape. If the tape tears, the contacts close.

The FEED pushbutton S2 on the punch's front panel can be depressed to punch feed holes in the tape. PUN FEED from the button triggers the 3s delay to produce PUN PWR ON as for a programmed IOT select instruction. The eventual PUN LINE level activates the FWD FD and NDX circuits to punch the feed holes and advance the tape. All other logic is disabled.

CHAPTER 5 MAINTENANCE

5.1 INTRODUCTION

Maintenance philosophy for the PC09C conforms to that of all electronic equipment presently in use, i.e., an optimum amount of preventive procedures, performed on a routine schedule, can eliminate many costly equipment breakdowns and can forecast impending failures long before they occur. When a specific item does fail, equipment design is such that quick replacement of modular elements can restore the main equipment to service in a minimum of time. The design objective of the PC09C High-Speed Perforated Paper-Tape Reader/Punch was to provide a dependable and relatively maintenance-free assembly. The tape reader motor is electromagnetically driven so that it does not experience the mechanical failures inherent in systems using ratchets, detents, and clutch-brake mechanisms. In this chapter procedures are divided between preventive and corrective categories. Any particular test setups have been included with pertinent procedures.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed at periodic intervals to ensure proper equipment operation and minimum unscheduled downtime. These tasks consist of visual inspection, operational checks, cleaning, lubrication, adjustment, and replacement of borderline, or partially defective parts.

Preventive maintenance scheduling depends upon the environmental and operating conditions existing at the installation site. Under normal environmental and work-load conditions; a schedule of preventive maintenance is recommended which consists of inspection, cleaning, and lubrication every 600 hours of operation (or every 4 months, which ever occurs first). Relatively extreme conditions of temperature, humidity, dust, or abnormally heavy work loads demand more frequent maintenance.

Maintenance activities for the PC09C require the standard test equipment and special materials listed in Table 5-1, plus standard hand tools, cleaners, test cables and probes.

Table 5-1
Test Equipment Required

Equipment	Manufacturer	Designation
Multimeter	Triplett or Simpson	Model 630-NA or 260
Oscilloscope	Tektronix	Type 547
Plug-in-Unit	Tektronix	Type CA
Clip-on Current Probe	Tektronix	Type P6016

Table 5-1 (Cont)
Test Equipment Required

Equipment	Manufacturer	Designation
X10 Probe	Tektronix	P6008
Recessed tip, 0.065 in. for wire-wrap terminals	Tektronix	206-052
Current Probe Amplifier	Tektronix	Type 131
Hand Unwrapping Tool	Gardner-Denver	500130
Hand-Operated Wire-Wrap Tool with a 26263 bit for 24 AWG Wire and 18840 Sleeve	Gardner-Denver	14H1C
Module Extender	DEC	Type W980
Diagnostic Self-Test Routine	DEC	High-Speed Reader/Punch

5.2.1 Preventive Maintenance Procedures

Preventive maintenance procedures for the PC03 Tape Punch are not included in this manual. For these procedures refer to the Royal McBee Maintenance Manual supplied with the equipment.

5.2.1.1 Mechanical Checks - Inspect the PC02 Tape Reader periodically as follows:

- a. Visually inspect the tape reader for completeness and general condition.
- b. Clean the interior and exterior of the tape reader using a vacuum cleaner or clean cloth moistened in nonflammable solvent.
- c. Lubricate the slide mechanisms with a light machine oil. Wipe off excess oil.
- d. Inspect all wiring and cables for cuts, breaks, fraying wear, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
- e. Inspect the following for mechanical security: feed switch, lamp assembly, diode assembly, all connectors and circuit modules, fan mounting bracket and fan, tape-feed motor, front cover, and resistor bracket.

5.2.1.2 Electrical Checks - Perform the power supply output checks described in Table 5-2. Use a multimeter to make the output voltage measurements with the normal load connected, and an oscilloscope to measure the peak-to-peak ripple content on all dc outputs of the supply. The +10 and -15 Vdc supplies are not adjustable; therefore, if any output voltage or ripple content is not within specifications, consider the power supply defective and initiate troubleshooting procedures.

Table 5-2
Power Supply Output Checks

Measurement Terminals at Power Supply Output	Nominal Output (Vdc)	Acceptable Output Range (V)	Maximum Output Current (A)	Maximum Peak-to-Peak Output Ripple (V)
Red (+) to Black (-)	+10	+9.5 to 11.5	5.0	0.5
Black (+) to Blue (-)	-15	+13.5 to 16.5	22.0	0.7
Black (+) to Yellow (-)	-30	-28.5 to 32.5	10.0	0.9
Black (+) to Brown (-)	-30	-28.5 to 32.5	5.0	0.9

NOTE

This power supply is the Type 712 located at the bottom of the PDP-9/L rack.

5.2.1.3 Electronic Checks - Periodically check the tape reader's W040 Solenoid Driver modules, drawing PC2 [A5 through D5]. Proceed as follows:

- a. Connect oscilloscope lead to pin R of the first module.
- b. Depress the reader feed button.
- c. While reader synchro motor is operating, the module output should change from 0 to -30V.
- d. Connect the scope lead to pin S of the module and check for the same output change.
- e. Repeat the checks for the three remaining modules.

5.3 CORRECTIVE MAINTENANCE

The simplicity of the system and the logic description provided in this manual should permit the use of standard troubleshooting techniques for isolating the trouble quickly and efficiently. For economical maintenance under most conditions, replace the inoperative module with one from spares and return the defective module to DEC for repair or replacement. DEC offers an optional spare modules kit containing one spare of each infrequent-use module and two each of the modules more likely to fail. Under normal operating conditions, the failure rate of DEC modules is well below the industry average; however, if the user so wishes, this spares kit can be optionally obtained.

Before commencing troubleshooting procedures, ensure that the processor portion of the PDP-9/L and the Type 712 Power Supplies are operating properly. Refer to the PDP-9/L Maintenance

Manual to determine status. Also examine the maintenance log to determine if the fault has occurred before and note what steps were taken to correct the condition. Visually inspect the physical and electrical security of all cables, connectors, modules, and wiring. Check the lamps for operation and their glass covers for cleanliness. Particularly check the security of ground connections between the reader/punch and the PDP-9/L. Faulty grounds can produce a variety of faults.

DEC provides special test programs (MAINDEC) including the one provided with the equipment, to exercise and check the operation of input/output equipment. These programs determine whether or not the peripheral is at fault and are designed to help in localizing the problem area.

After the localizing the fault within the functional logic element, program the computer to repeat an operation which uses all functions of that element. Trace signal flow through the suspected element with an oscilloscope by synchronizing the scope sweep with control signals or clock pulses from the CP or the control logic. Check for proper levels, durations, rise and fall times, and timing of all input and output signals.

Refer also to the PDP-9/L Maintenance Manual under Marginal Voltage Checks and perform those checks which pertain to the High-Speed Reader/Punch Control circuits. This aggravation technique can isolate borderline faults which otherwise could not be detected.

Since only two module types (W040 Solenoid Drivers and G904 Photodiode Amplifier) are used in the tape reader, the system troubleshooting for this assembly is relatively simple. Output checks of both card types should quickly determine the location of the fault. Remove these cards and reinstall them through a DEC Type W980 Module Extender.

CAUTION

Remove power to the computer before removing any modules.
Restore power only after the replacement has been reinstalled
either directly or through an extender.

The four W040 Solenoid Driver modules are tested as follows:

- a. Connect the oscilloscope to pins R and S of the module under test.
- b. Depress the manual feed button on the face of the reader.
- c. Observe on the oscilloscope, while the reader motor is turning, that the output of the W040 changes from 0 to -30V.

The G904 Photodiode Amplifier is tested as follows:

- a. Remove tape from the reader and place the tape hold-down bar in its down position.
- b. Set the REGISTER DISPLAY switch on the console to the STATUS position and depress the PROGRAM STOP and IO RESET keys. The STATUS bit 08 in the REGISTER indicator should be illuminated, indicating a reader no tape status.

5.3.1 G904 Adjustment Procedure (Reader Timing)

To adjust the PC09C reader timing, proceed as follows:

1. ✓ a. Make a tape loop of alternate 1s and 0s (i.e., all 8 channels of 1s and all 8 channels of 0s).

x b. Put the following program in core.

PDP-9
PROG.

LOC 100/RSA	= 700104	Select Reader Alpha
RSF	= 700101	Skip on Reader Flag
JMP-1	= 600101	
JMP-3	= 600100	

2 ✓ c. Place the tape loop made in step a in the reader.

d. Hang oscilloscope probe 1 on pin E12J in the I/O (R111E12J on drawing KD9(1) [C5]).

3 ✓ e. With probe 2 look at any one of the channel outputs at I/O pins A¹7D, E, F, H, J, K, L or M (RD HOLE 1 through RD HOLE 8), see drawing KD9(2) [D7 through D4]. of P.T.RDR LOGIC G904 OUTPUTS

4 ✓ f. Depress IO-RESET and START. SET 710440, 000100, REPEAT, XCT & SPEED SWITCHES TO SUITABLE SPEED.

x g. Synchronize the scope on the probe 1 signal and calibrate the scope so that one cycle of the signal on probe 2 = 10 cm.

h. The observed waveform should be a very nearly symmetrical square wave (see Figure 5-1). If necessary, adjust the G904 module for a 50% duty cycle (ON for 5 cm then OFF for 5 cm).

NOTE. THE ONE POT ADJUSTMENT IS FOR ALL 8 CHANS. ADJ FOR BEST OVERALL 8 CHANS. AFTER SETTING UP THE AMP OUTPUT WIDTHS TO APPROX 50:50 MS RATIO FOR ALTERNATE ONES & ZERO'S TAPE. CHECK STROBE TIMING

NOTE
PC09 - A02 DRAW M
The allowable deviation is ±5% between channels. 3A43-U



-VE TRANSITION TO BE IN CENTRE OF THE -VE (LIGHT) PORTION OF DATA.

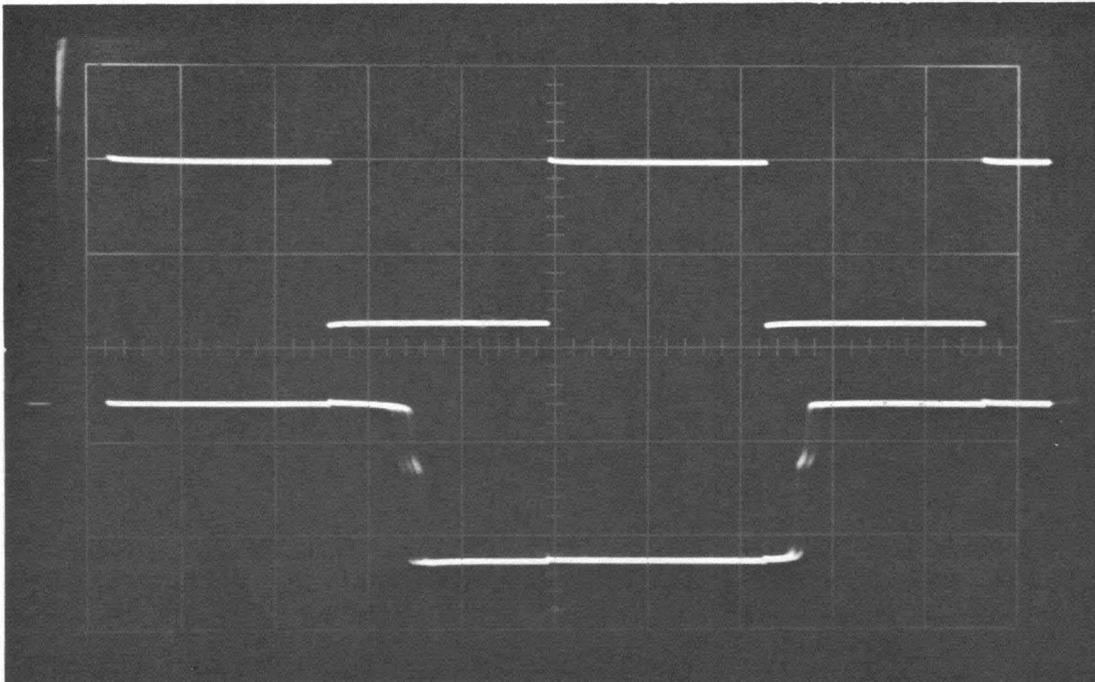


Figure 5-1 Reader Strobe Timing Adjustment

i. Strobing should occur during the UP clock (positive transition) of the strobe pulse which should be positioned so that it occurs in the center of the data. If the strobe is not positioned properly, loosen the four screws that hold the stepping motor. Rotate the motor to position the strobe and then tighten the four screws.

j. If it is impossible to position the strobe by rotating the motor, loosen the sprocket wheel and rotate it slightly. Tighten the sprocket wheel and set the final position of the strobe by loosening the four screws that hold the stepping motor and rotating the motor.

5.3.2 PC02 Tape Path Alignment Procedure

Proceed as follows:

a. Alignment of Two-Piece Tape Guide

- (1) Remove the external reader cover and the tape face plate against which the tape hold-down bar rests.
- (2) Set the tape hold-down bar in its upright position. The tape face plate should have a slot cut out in the lower right corner, which allows face plate adjustment without interference from the bottom screw on the diode assembly. (In some early models of the PC02 the slot was not made available, in which case the plate must be modified or replaced.)
- (3) Loosen the two Phillip screws that hold the left paper-tape guide and photocell block.
- (4) Punch approximately five fan folds of paper tape from the punch. Using the fan fold, tear the tape so that the result is two pieces of paper with double thickness and one long piece of paper tape.
- (5) Insert one piece of the double thickness tape over the left paper-tape guide and one piece over the photocell block. Ensure that these pieces of tape do not touch the sprocket wheel.
- (6) Place the long piece of paper tape over the sprocket wheel covering both of the previously inserted pieces of paper tape. The end result should be a triple thickness of tape over both the left paper-tape guide and photocell block and one piece over the sprocket wheel.
- (7) Place the tape hold-down bar in its down position so that it attempts to compress the tape between the photocell block and the left paper-tape guide. Then move the photocell block and left paper-tape guide up, so that they compress the tape between them and the hold-down bar. Check that the hold-down bar has not been raised from its original down position and ensure that the tape path is straight and parallel.
- (8) Tighten the two Phillip screws that secure the photocell block and the left paper-tape guide. Using a 6-in. steel ruler, recheck the parallelism and straightness of these parts.
- (9) Replace the tape face plate but do not secure it or move the tape hold-down bar up. Proceed to move the tape face plate up until it touches the tape hold-down bar equally along its whole top edge. Check that the tape face plate is parallel with the hold-down bar.
- (10) Tighten the screws for the tape face plate and move the double thickness of paper tape back and forth while the hold-down bar is in its down position. Observe that

there is a slight amount of drag on the paper tape. Ensure that the paper tape is not compressed so tightly that it cannot be moved.

b. Alignment of One-Piece Tape Guide

- (1) Remove external reader cover.
- (2) Raise tape hold-down bar and insert three pieces of fan-fold tape as described in steps (4), (5), and (6) of the two-piece alignment procedure.
- (3) Lower the tape hold-down bar so that the tape is compressed between the hold-down bar and the tape guide. Be very certain that the tape is firmly back against the reader face and that no tape is being pinched at the front edge of the tape guide.
- (4) Carefully raise the tape guide until there is a slight drag on the double-thickness tape. This drag should be equal at each end of the guide. At this time, the hold-down bar should be straight across and parallel to the tape guide.
- (5) Tighten the two 6-32 screws on each end of the tape guide and recheck for tape drag and straightness.

NOTE

PC02 Tape Readers may contain either one-piece or two-piece tape guides. Before performing this alignment, determine which type has been provided. Use the appropriate procedure below. This procedure is performed only when parts have been removed or replaced.

5.3.3 PC02 Sprocket Wheel Alignment

NOTE

This alignment is to be performed only if the motor or sprocket wheel have been removed.

Proceed as follows:

- a. Ensure that the machine is turned off and that power is removed from the PDP-9/L.
- b. Loosen the four Phillip screws that hold the stepping motor to the base plate.
- c. Place the motor in the center of its rotational play and secure the four screws three-fourths tight.
- d. Loosen the two Allen screws which secure the sprocket wheel to the motor shaft.
- e. Place the tape with all 1s through the tape path and over the sprocket wheel. Center the feed sprocket pin in the feed hole while holding light pressure against the sprocket wheel. This ensures that the back edge of the tape is against the reader plate.
- f. Rotate the sprocket wheel so that the punched holes are in alignment with the photo-diodes. Check that the tape is not skewed which would cause some parts of the holes to be covered.
- g. Tighten the Allen screws that secure the sprocket wheel to the motor shaft. Recheck the tape for proper alignment of sprocket and feed hole.

- h. Place a tape of alternate 1s and 0s in the reader.
- i. Attach an oscilloscope probe from trace A to the output of the clock accelerator circuit in the reader control logic, and from trace B to any one of the photocell amplifier data output pins (AD, AE, AF, AH, AJ, AK, AL, or AM). Synchronize the oscilloscope at pin E of any one of the solenoid driver modules.
- j. Load the MAINDEC reader test program as called out in that document, selecting the portion of the program which permits continuous cycling through the acceleration phase of the reader operation. Use a block length of six characters and a delay (stall) of approximately 150 ms.
- k. Start the program. Trace A will appear as a sawtooth waveform in which the first, and subsequently every other sawtooth peak, occurs simultaneously with strobe as shown in Figure 5-2. If necessary, loosen the four machine screws securing the motor to the reader plate and rotate the motor slightly to obtain the operating characteristics shown in Figure 5-2.

NOTE

If the rotational adjustment range of the motor is found to be insufficient to complete the procedure, the sprocket wheel must be adjusted to meet the operation requirements. Place the motor in the approximate center of its rotational play and secure the four motor-mounting machine screws. Complete the adjustment by loosening the two sprocket-wheel mounting screws and rotating the sprocket wheel slightly. Since the machine must be stopped for this adjustment, it will be necessary to determine the desired direction of movement of the sprocket wheel (or motor), make a tentative adjustment, and restart the program to check the results. If the sprocket-wheel adjustment becomes necessary, recheck the adjustment parameters of step e and f of this procedure.

It is important that the sawtooth peaks representing the strobe pulse be as nearly centered as possible on the first five to six data outputs. It may be necessary to compromise strobe centering on data outputs beyond this point, but the operating characteristics of the system are much less critical when the feed motor has reached full speed. It is far more important that the strobe be centered on the data output during the critical acceleration period of the motor.

- l. Rotate the motor to its final strobe position, if necessary. Tighten the Phillip screws that fasten the motor to the base plate.

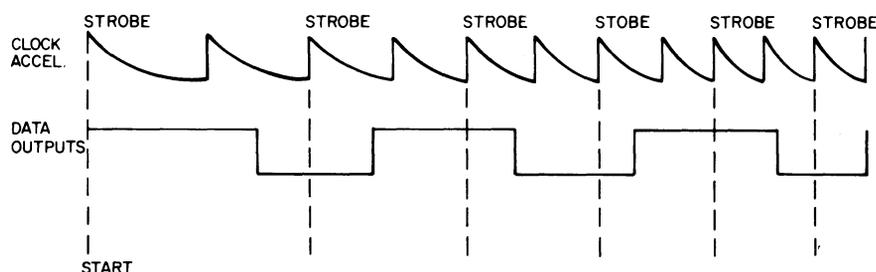


Figure 5-2 Waveforms for Sprocket-Wheel Alignment Procedure

5.3.4 Tape Punch Tape Tear Plate Adjustment Procedure

If punched tape, when torn off at its exit slot, does not sever at a feed hole, proceed as follows:

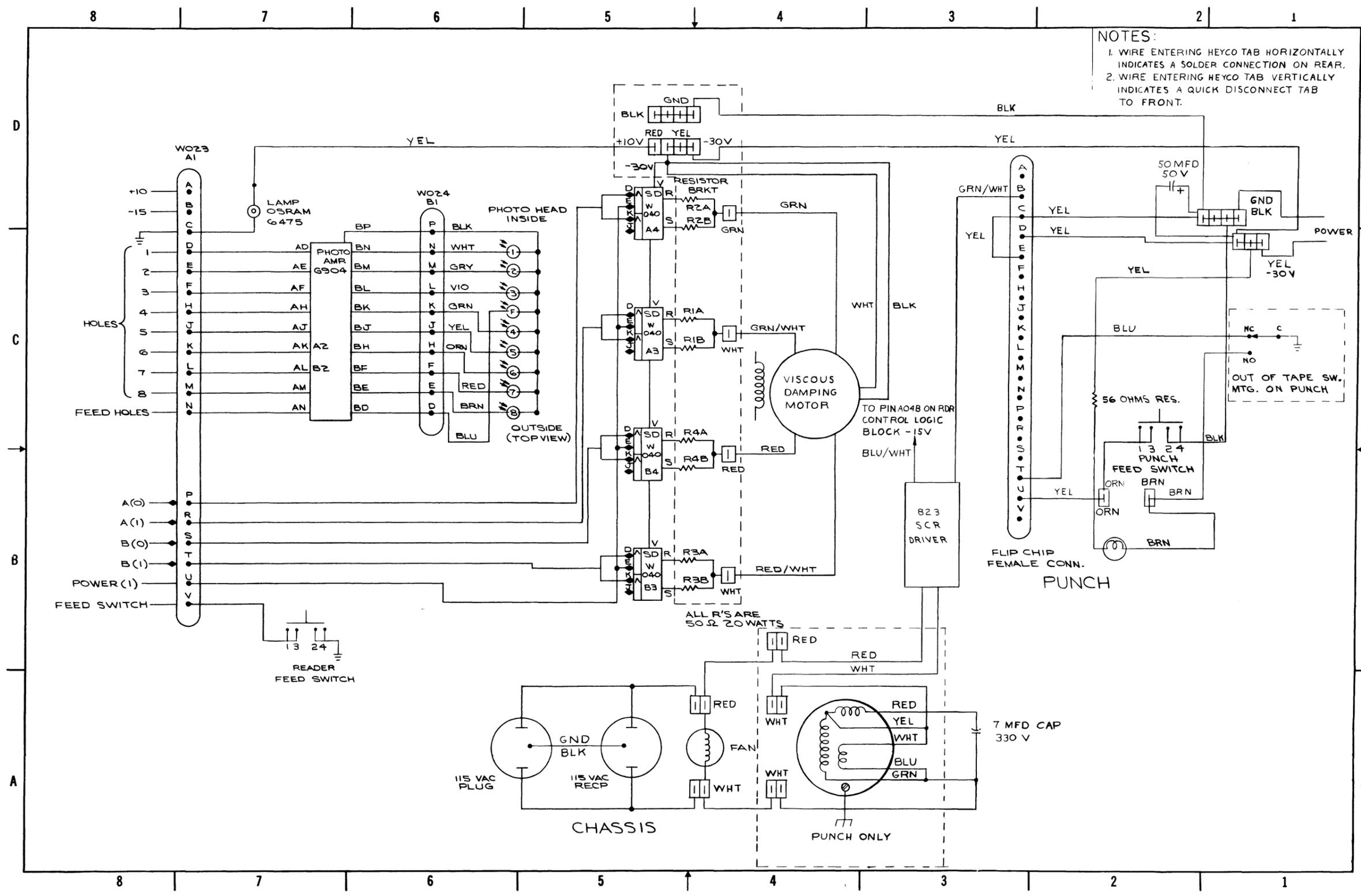
- a. Barely loosen the two screws which secure the tape tear plate to the punch block (see Figure 3-7a).
- b. Move the tear plate slowly in the direction of correction as indicated by the torn tape.
- c. When complete, retighten the two holding screws. For more information on this adjustment refer to the Royal-McBee Maintenance Manual covering the punch block mechanism of the PC03 Tape Punch.

CHAPTER 6
CIRCUIT DIAGRAMS

This chapter contains the circuit diagrams required for maintenance of the PC09C. Table 6-1 lists the drawings by number and title.

Table 6-1
PC09C Drawings

Drawing Number	Revision	Title
D-BS-PC09-0-2	C	PC09C Reader and Punch
D-BS-KD09-C-9		Reader Control
D-BS-PC09-C-1	-	High-Speed Punch Control
D-TD-KD09-C-17		Reader Control Timing Diagram
D-TD-KD09-C-10		Punch Control Timing Diagram
D-BS-PC09-C-2	-	High Speed Reader
C-CS-G913-0-1	-	Clock Control G913
B-CS-R401-0-1	M	Clock R401
B-CS-S202-0-1	D	Dual Flip-Flop S202



NOTES:
 1. WIRE ENTERING HEYCO TAB HORIZONTALLY INDICATES A SOLDER CONNECTION ON REAR.
 2. WIRE ENTERING HEYCO TAB VERTICALLY INDICATES A QUICK DISCONNECT TAB TO FRONT.

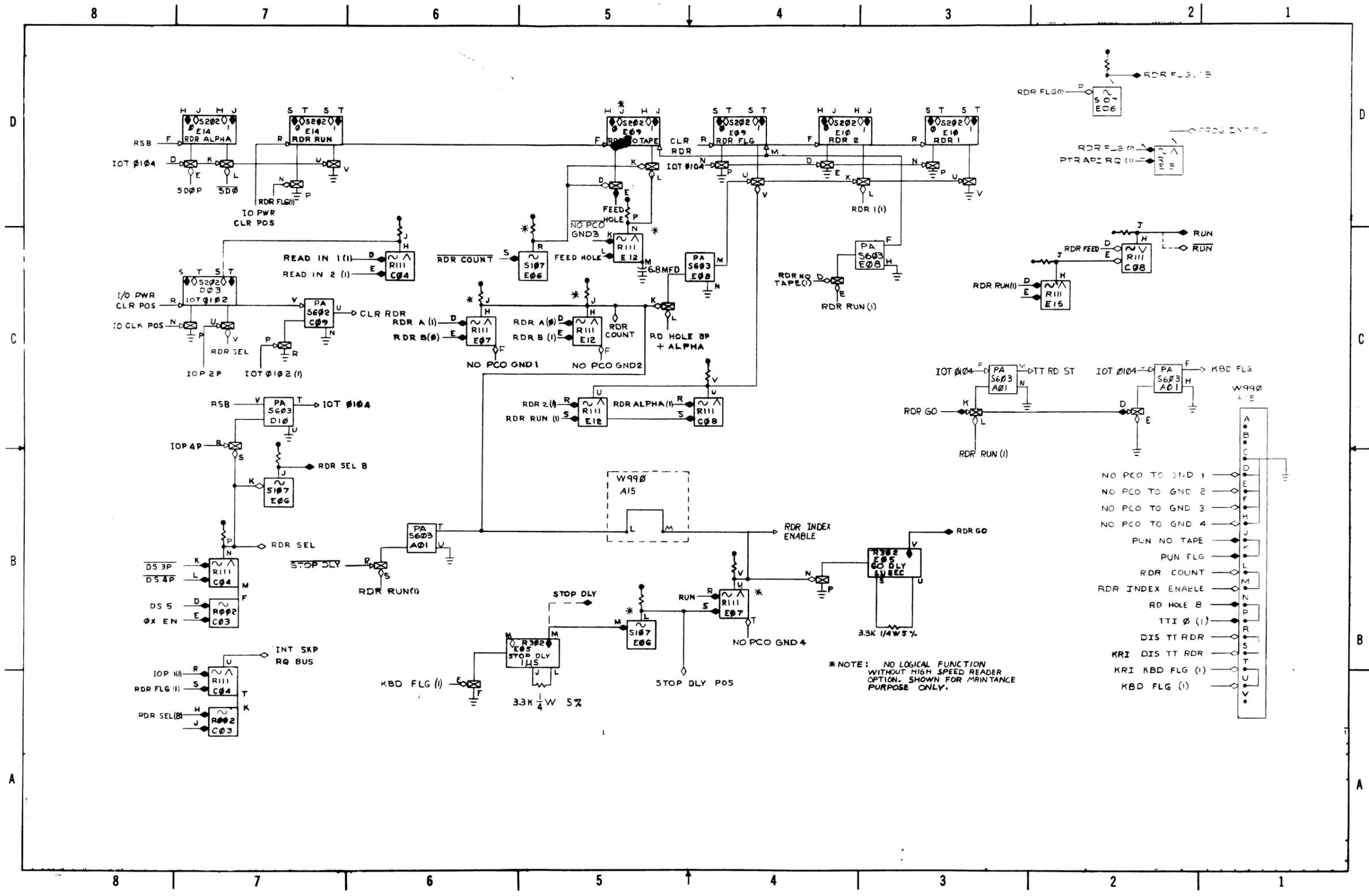
ALL R'S ARE 50 Ω 20 WATTS

OUT OF TAPE SW. MTG. ON PUNCH

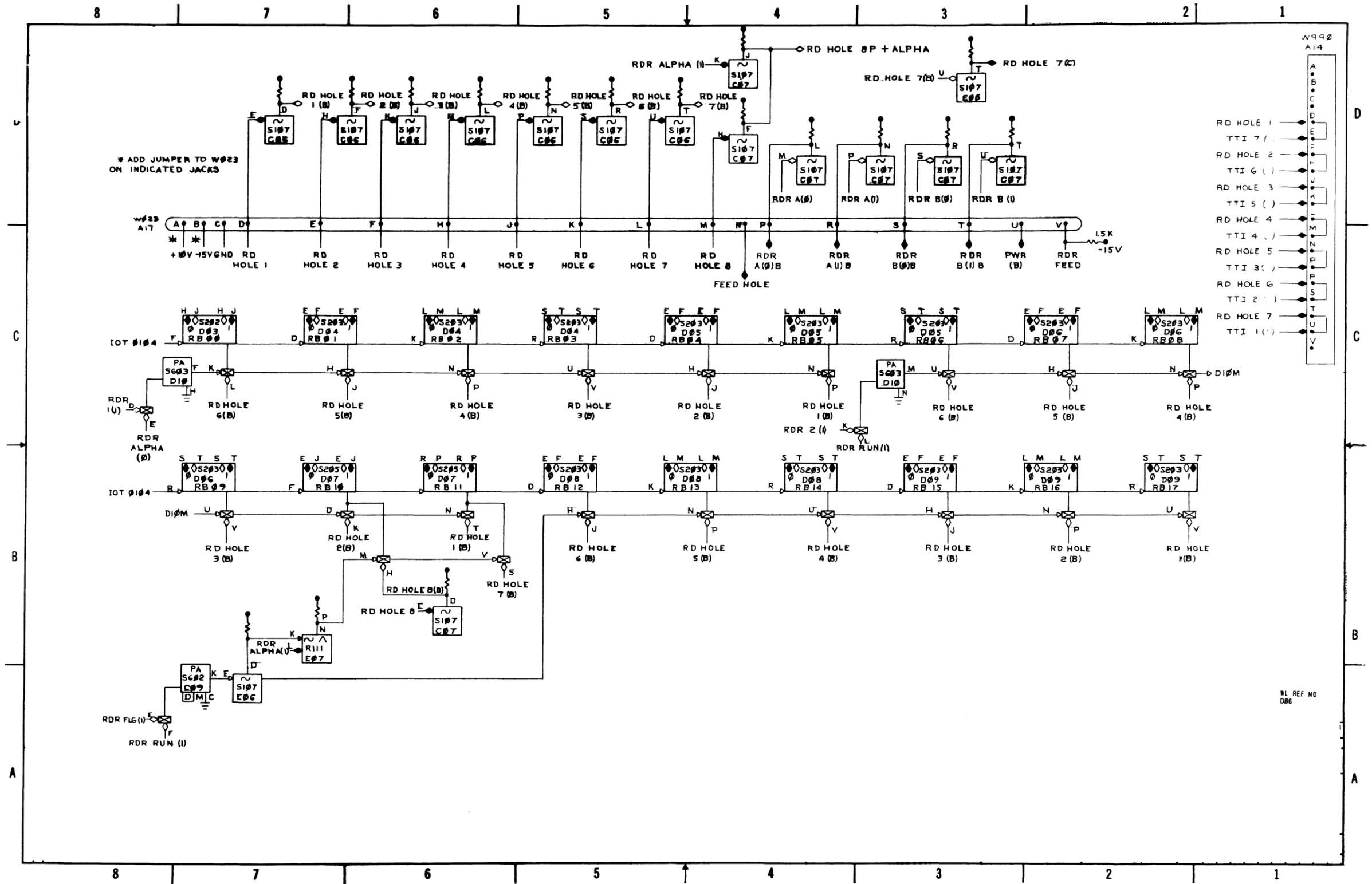
PUNCH

CHASSIS

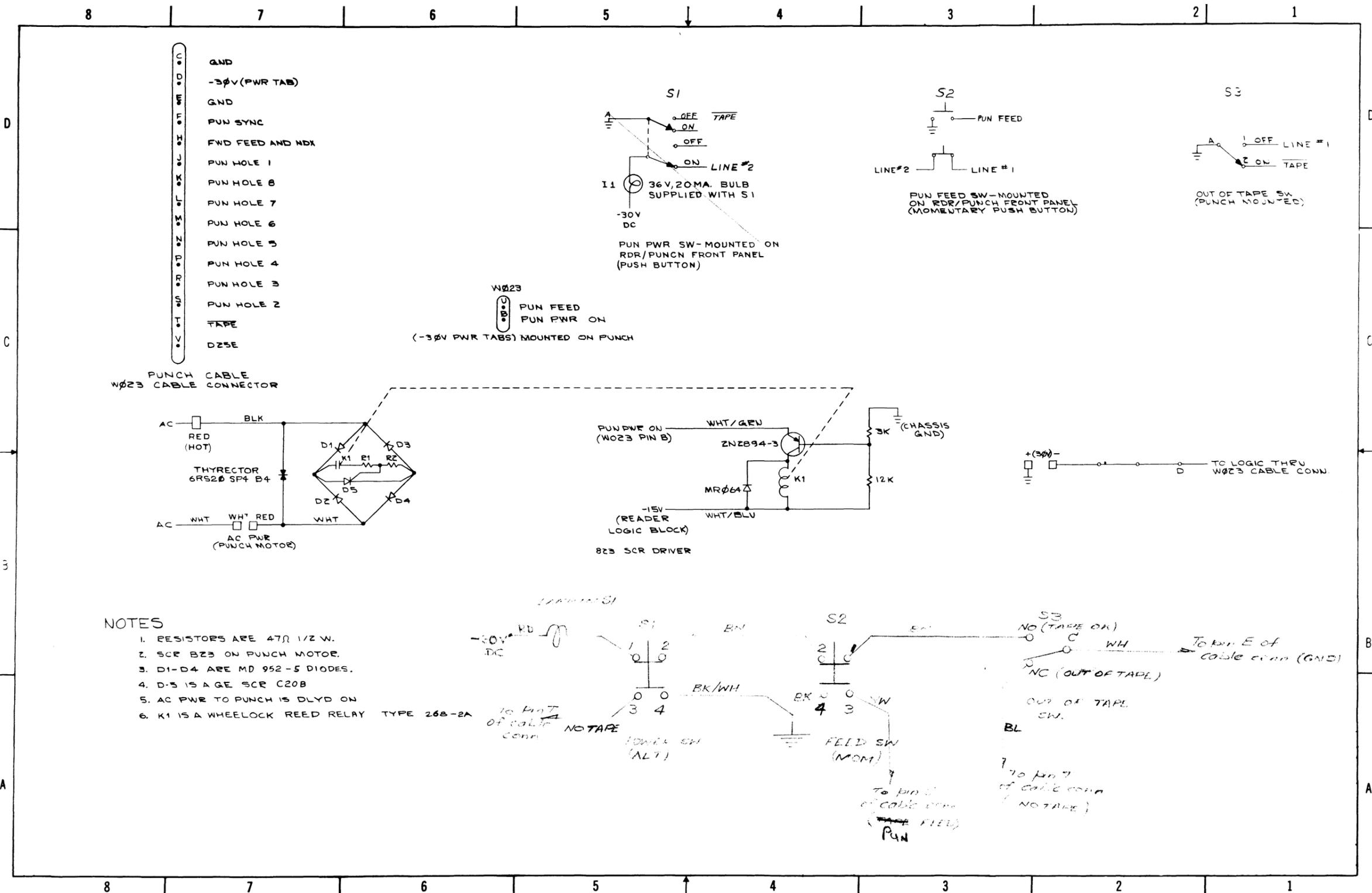
PUNCH ONLY



D-BS-KD09-C-9 (Sheet 1) Reader Control

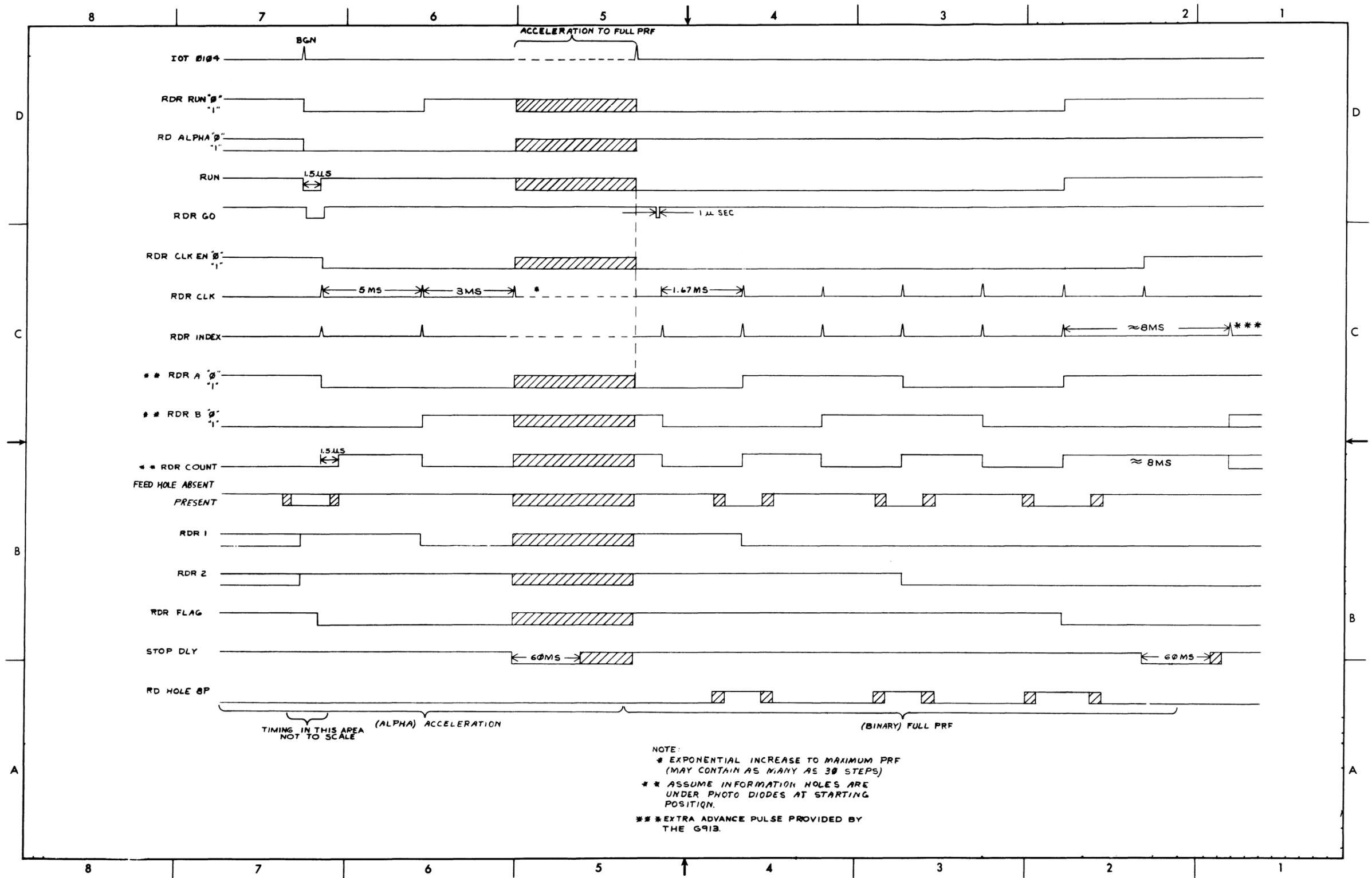


D-BS-KD09-C-9 (Sheet 2) Reader Control

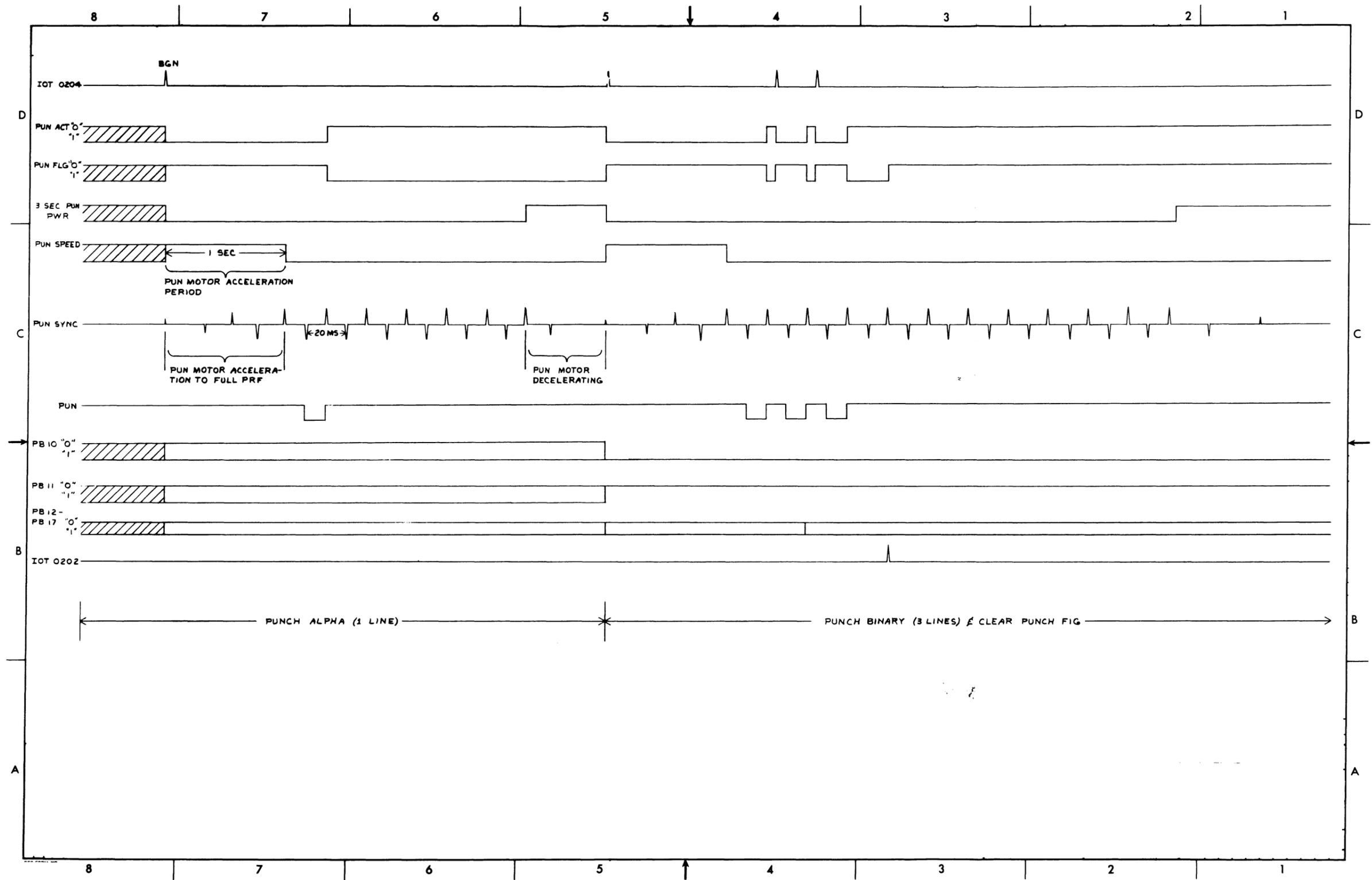


NOTES

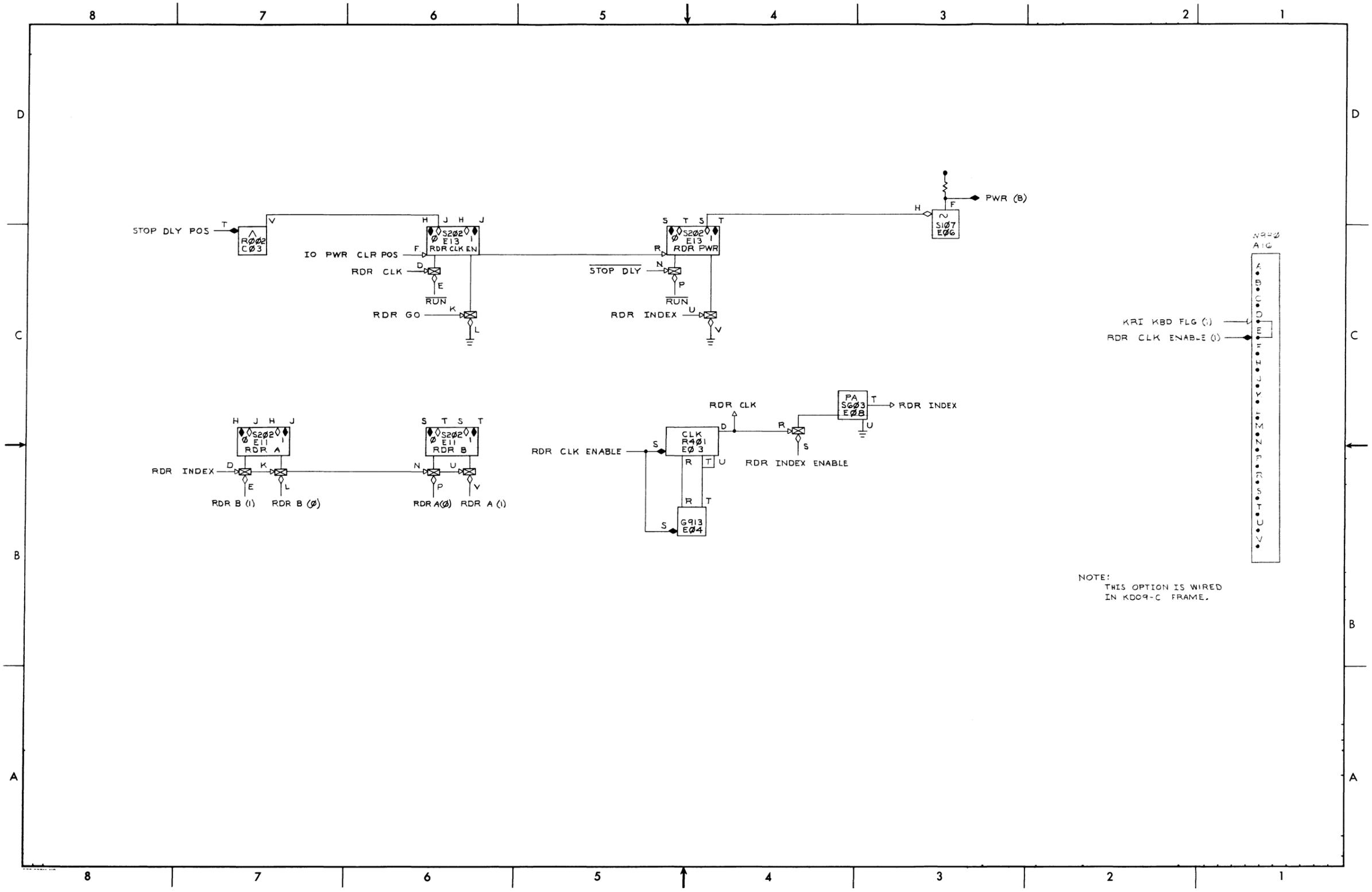
1. RESISTORS ARE 47Ω 1/2 W.
2. SCR BZ3 ON PUNCH MOTOR.
3. D1-D4 ARE MD 952-5 DIODES.
4. D-5 IS A GE SCR C20B
5. AC PWR TO PUNCH IS DLYD ON
6. K1 IS A WHELOCK REED RELAY TYPE 268-2A



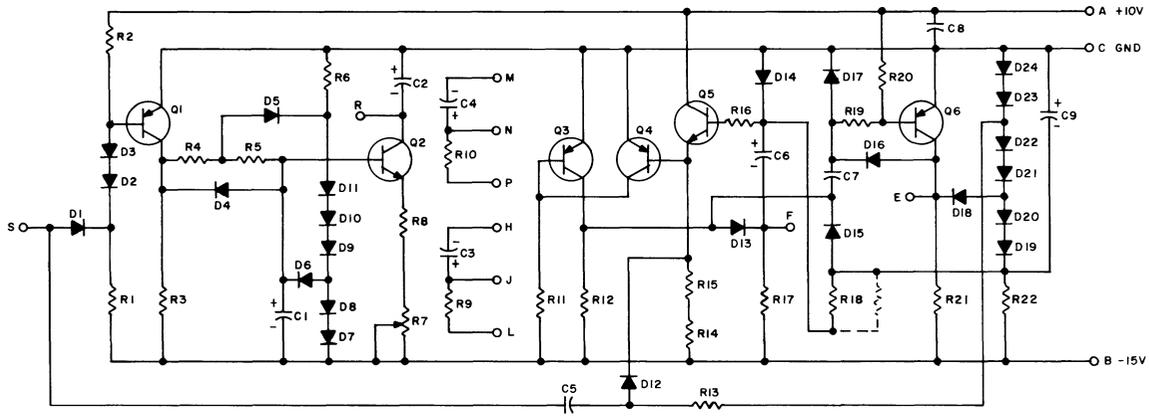
D-TD-KD09-C-17 Reader Control Timing Diagram



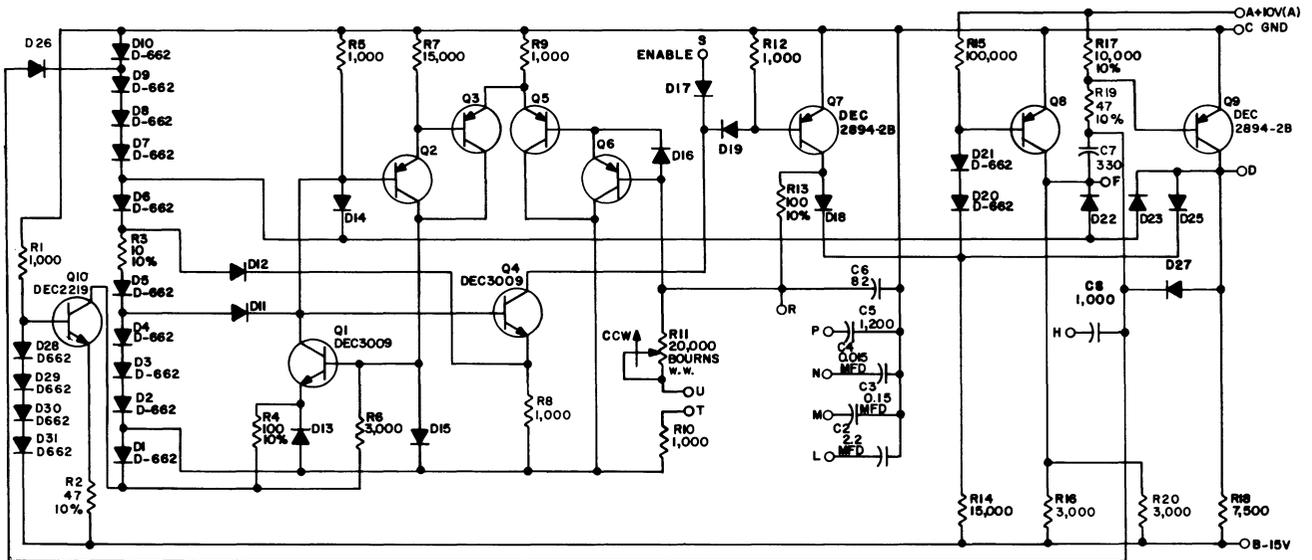
D-TD-KD09-C-10 Punch Control Timing Diagram



NOTE:
THIS OPTION IS WIRED
IN K009-C FRAME.

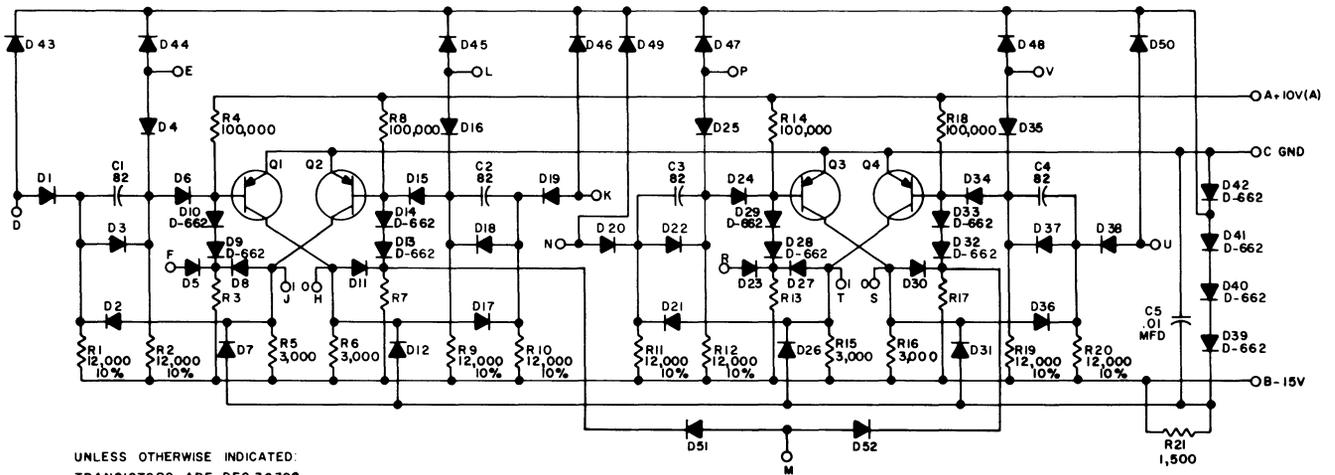


C-CS-G913-0-1 Clock Control G913



UNLESS OTHERWISE INDICATED:
 RESISTORS ARE 1/4W, 5%
 CAPACITORS ARE MMFD
 DIODES ARE D-664
 TRANSISTORS ARE DEC 3639-0
 R11 IS A #275P

B-CS-R401-0-1 Clock R401



UNLESS OTHERWISE INDICATED:
 TRANSISTORS ARE DEC 3639C
 RESISTORS ARE 1/4W, 5%
 CAPACITORS ARE MMFD
 DIODES ARE D-664

B-CS-S202-0-1 Dual Flip-Flop S202

**Digital Equipment Corporation
Maynard, Massachusetts**

